

SATURN V

Laboratory Maintenance
Instruction for LTE

Volume V

Programmable Test Controller

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VOLUME V OF V

Laboratory Maintenance Instructions

**SATURN V
LAUNCH VEHICLE DIGITAL COMPUTER
AND LAUNCH VEHICLE DATA ADAPTER
TEST EQUIPMENT**

International Business Machines Corporation

Contract NAS 8-11561

VOLUME V

Programmable Test Controller (IBM Part No. 6900900)

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LIST OF RELATED MANUALS

Equipment	Manufacturer	Manual Title
Platter Assembly Model 565	California Computer Products Incorporated	Instruction Manual for Digital Incremental Platter, Model 565
Power Supply Model M36-5-0V	Trygon Electronics, Inc.	Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M36-5-0V
Power Supply Model M15-10-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-10-0V
Power Supply Model M36-10A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M36-10A-0V
Power Supply Model M15-30A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-30A-0V
Automated Logic Diagrams	IBM Corporation	Saturn V LTE-Programmable Test Controller Automated, Logic Diagrams

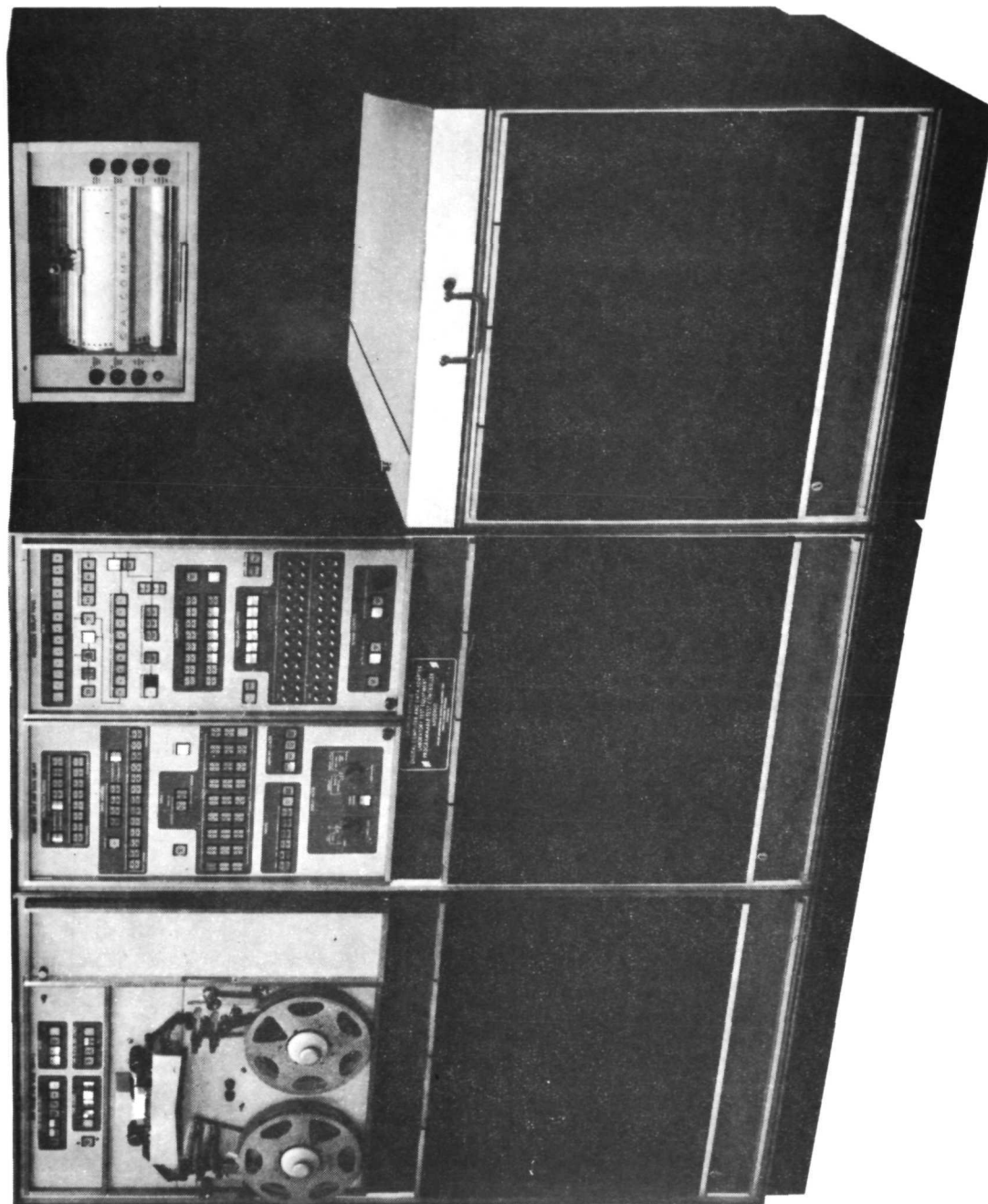


Figure 1-1. Programmable Test Controller

SECTION I

INTRODUCTION AND DESCRIPTION

1-1. SCOPE.

1-2. This section outlines the contents of this volume and specifies related publications and documents. This section also presents a general physical description of the Programmable Test Controller and its major component assemblies.

1-3. INTRODUCTION.

1-4. PURPOSE OF THIS VOLUME.

1-5. This volume of the manual provides operating and maintenance instructions for the Saturn V Programmable Test Controller (PTC), IBM part number 6900900, shown on figure 1-1. The PTC is manufactured by the International Business Machines Corporation, Federal Systems Division, Rockville, Maryland.

1-6. CONTENTS. This volume is composed of ten sections as follows:

Section I	Introduction and Description
Section II	Theory of Operation
Section III	Interface and Controls
Section IV	Test Equipment and Special Tools
Section V	Preparation for Use, Storage and Shipment
Section VI	Preventive Maintenance
Section VII	Calibration
Section IX	Repair
Section X	Diagrams

At the beginning of each section a paragraph labeled SCOPE describes the contents of the section and relates the contents of the section to applicable contents of other sections.

1-7. A glossary and index are located at the back of the volume. The glossary lists signal names and acronyms in alphabetical order. (Standard abbreviations in this volume conform with military standard MIL-STD-12B.) The topical index indicates the page or pages on which the discussion of a topic begins.

1-8. RELATED MANUALS. Maintenance information for PTC assemblies not built or modified by the Federal Systems Division is not included in this volume. This information is contained in the commercial manuals supplied with this volume. The List of Related Manuals in the front of this volume lists the titles and source of supply for these manuals.

1-9. Four copies of PTC Automated Logic Diagrams (ALD's) are also supplied by the IBM Corporation; the title of the books containing these diagrams is included in the List of Related Manuals.

1-10. LOGIC SYMBOLS. The logic symbols used in this volume and on the ALD's are defined in the table of logic symbols. A discussion of the physical layout and interpretation of the ALD's is included in Section X.

1-11. PART SYMBOLS. Symbols for standard electrical and electronic parts conform with military standard MIL-STD-15-1.

1-12. REFERENCE DESIGNATIONS. Reference designations for standard electrical and electronic parts conform with military standard MIL-STD-16B.

1-13. PURPOSE OF THE PTC.

1-14. The purpose of the PTC is to evaluate the Launch Vehicle Digital Computer and/or the Launch Vehicle Data Adapter by either the ADAPT or the ASTEC laboratory test equipments. (Refer to Volume I for the ADAPT and ASTEC descriptions.)

1-15. DESCRIPTION.

1-16. BASIC CONSTRUCTION.

1-17. The PTC is composed of three frames (01, 02, and 03, right to left on figure 1-1). Frames 02 and 03 are secured together by tie blocks and screws to form a unit approximately 58 inches long, 31 inches deep and 60 inches high that weighs approximately 1700 pounds. Frame 01 is not mechanically secured to frames 02 and 03. Frame 01 is approximately 30 inches wide, 31 inches deep and 60 inches high and weighs approximately 800 pounds. All three frames are further divided into modules. The upper module in each of these frames is designated module A; the lower module is designated module B.

1-18. Each module is composed primarily of hinged or slide mounted assemblies that can be pulled out from the frame to facilitate servicing the PTC. The side covers of each module can be removed to facilitate servicing assemblies that are fixed to the PTC frames.

1-19. Filtered openings at the base of the PTC permit the intake of cooling air. The cooling air is circulated through the PTC by fans and expelled through screened openings in the top of the PTC.

1-20. Casters at the bottom of each frame facilitate moving the PTC.

1-21. MAJOR ASSEMBLIES.

1-22. Each PTC assembly has a reference designation which identifies its location in the PTC. Each major assembly is referenced by a four-character designation that

identifies the frame (01, 02, or 03), module (A or B), and module assembly number (1 through 8) of the assembly. For example, the reference designation for assembly 1 in module A of frame 02 is 02A1.

1-23. The assignment of numbers for assemblies in a typical module B is shown on figure 1-2. A movable assembly in position 1, 2, 3, or 4 opens to the front of the module; a movable assembly in position 5, 6, 7, or 8 opens to the rear of the module.

1-24. The location of each major PTC assembly is shown on figure 1-3. The assembly name and reference designation for each assembly is shown in the legend for figure 1-3.

1-25. A brief description of each assembly shown on figure 1-3 is given in figure 1-4.

1-26. **GATE ASSEMBLIES.** The swinging gate assemblies contain the many printed circuit board assemblies that constitute the PTC logic circuitry. The gate assemblies and printed circuit board assemblies are discussed in detail in the following paragraphs.

1-27. Mechanical Features of the Gate Assemblies. The gate assemblies are hinged as shown on figure 1-5. Gate assemblies in B modules swing up to open.

1-28. Figure 1-6 illustrates a module B gate assembly in its fully extended position. The gate assembly is extended from the frame by pulling handle 2 toward handle 1 (to release the holding mechanism shown on figure 1-9) and pulling the gate assembly to the desired position in its arc; the gate assembly is stopped in its arc when handle 2 is released.

1-29. Access to the gate assembly handles is gained by rotating the cover plate away from the gate assembly. Cover plates for gate assemblies in B modules must be turned down, as shown on figure 1-6. The cover plate cannot be returned to its normal position until the gate assembly is returned into the frame. The latch engages the striker plate to hold the gate assembly in the frame.

1-30. As indicated on figure 1-6, a fan is mounted on the gate assembly to force cooling air over the logic circuits on the printed circuit board assemblies. The fans for module B gate assemblies are mounted on the bottom of the gate assemblies.

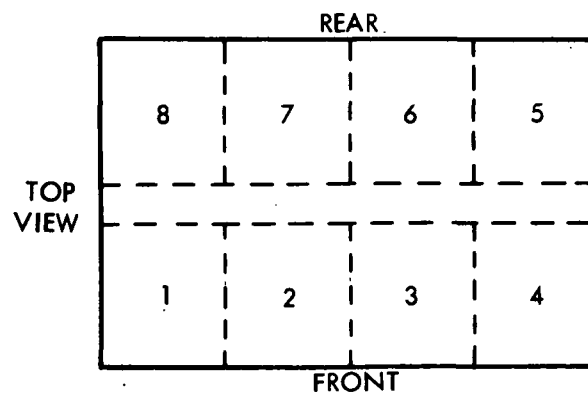
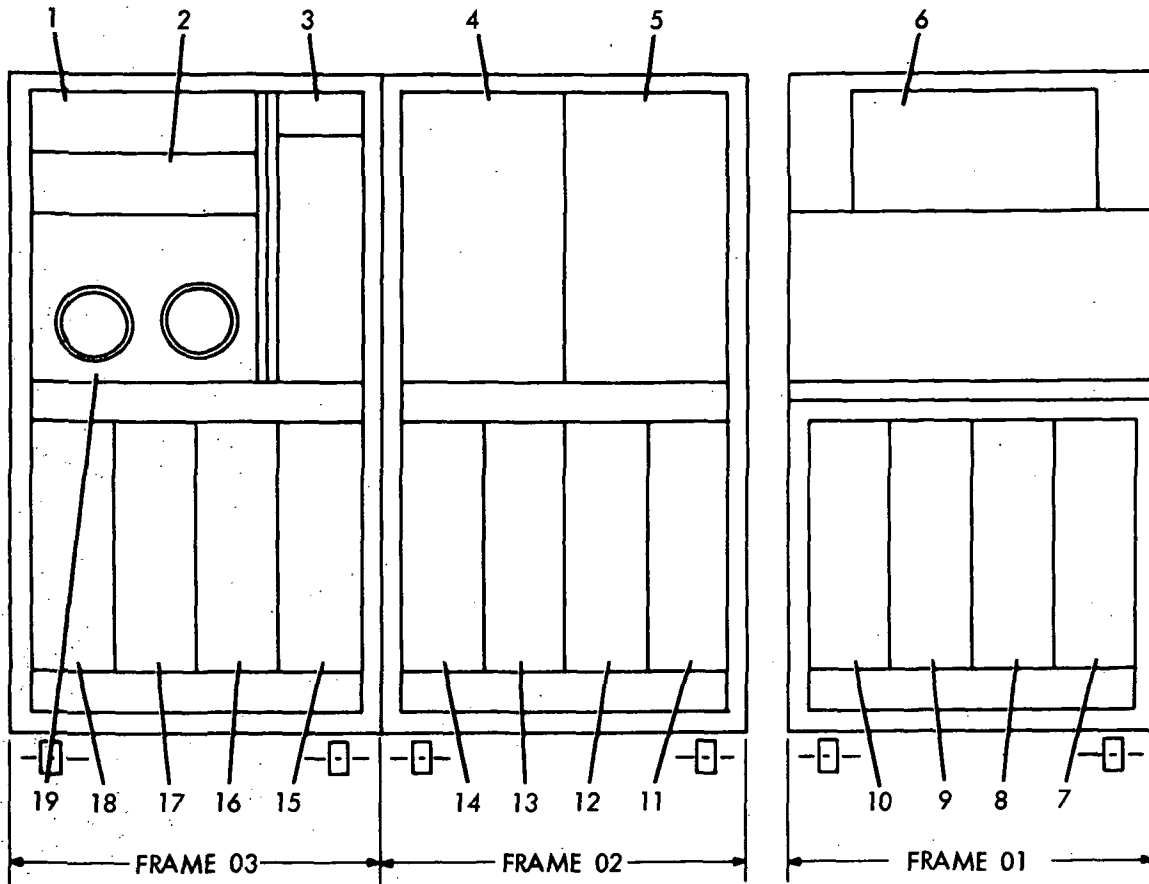


Figure 1-2. Numbering System for Module Assemblies

(Text continued on page 1-12.)

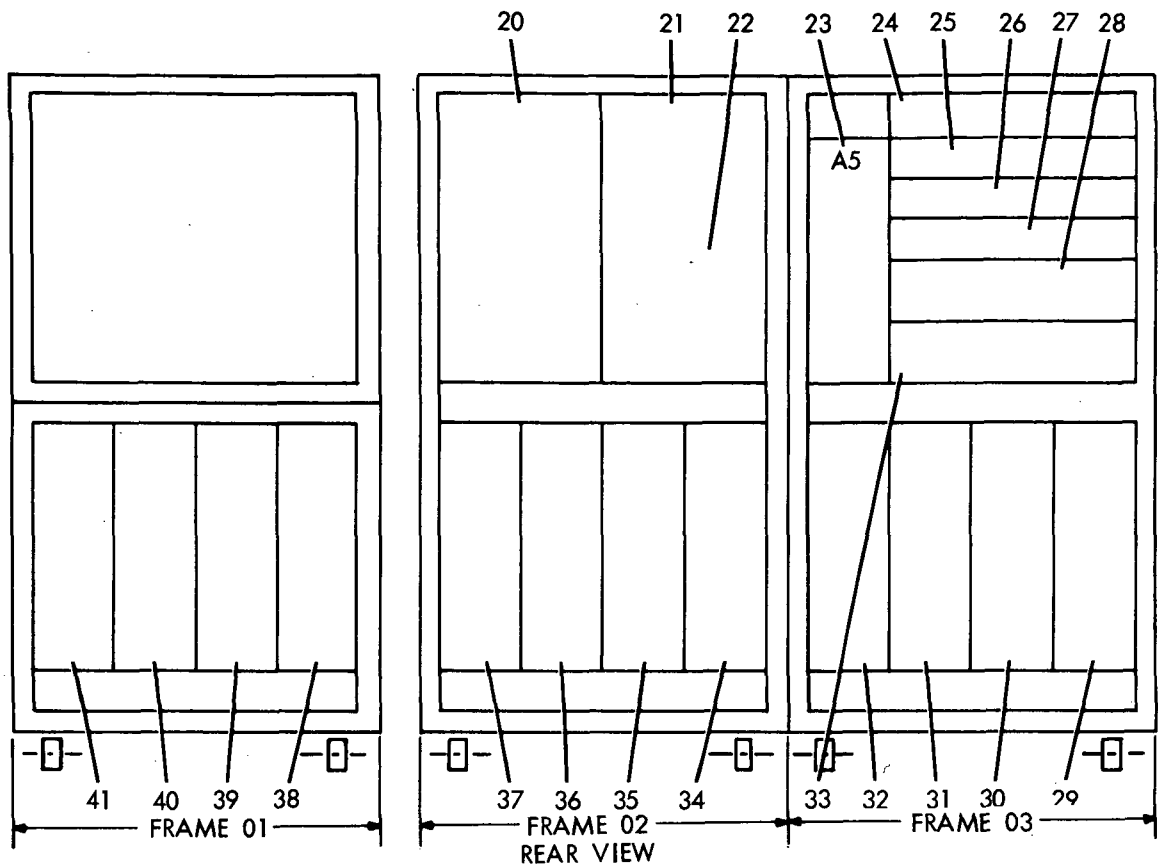


FRONT VIEW

Legend for Figure 1-3

<u>Index Number</u>	<u>Assembly Name and Reference Designation</u>
1.	Tape Reader Control Panel Assembly 03A1
2.	Tape Reader Assembly 03A2
3.	C. E. Panel Assembly 03A4
4.	Memory Load and Data Display Panel Assembly 02A1
5.	Processor Panel Assembly 02A2
6.	Plotter 01A1
7.	-48 VDC and -12 VDC Power Supply 01B4
8.	Gate Assembly 01B3
9.	Gate Assembly 01B2
10.	Gate Assembly 01B1
11.	Gate Assembly 02B4
12.	Gate Assembly 02B3
13.	Gate Assembly 02B2
14.	Gate Assembly 02B1
15.	Gate Assembly 03B4
16.	Gate Assembly 03B3
17.	Gate Assembly 03B2
18.	Gate Assembly 03B1
19.	Tape Spooler Assembly 03A3

Figure 1-3. PTC Assembly Locations (Sheet 1 of 2)



Legend for Figure 1-3 (cont)

<u>Index Number</u>	<u>Assembly Name and Reference Designation</u>
20.	Memory Array 02A4
21.	Memory Array 02A5
22.	Sense Cards Frame Assembly 02A6
23.	Relay Gate Assembly 03A5
24.	+30 VDC Power Supply 03A7
25.	+30 VDC Power Supply 03A6
26.	+12 VDC Power Supply 03A8
27.	+12 VDC Power Supply 03A9
28.	-28 VDC Power Supply 03A10
29.	Spare Gate 03B8
30.	Gate Assembly 03B7
31.	Gate Assembly 03B6
32.	Gate Assembly 03B5
33.	-12 VDC Power Supply 03A11
34.	Gate Assembly 02B8
35.	Gate Assembly 02B7
36.	Gate Assembly 02B6
37.	Gate Assembly 02B5
38.	-12 VDC and +30 VDC Power Supply 01B8
39.	-6 VDC and +12 VDC Power Supply 01B7
40.	Resonator Supply 01B6
41.	Interlock and Filter Box Assembly 01B5

Figure 1-3. PTC Assembly Locations (Sheet 2)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturer's Designation	Manufacturer	Description
01A1	6	Plotter Assembly	Model 565 (IBM Part Number 6900170)	California Computer Products Inc.	Provides a means of plotting digital data by plotting one variable against another. See maintenance instructions for this item. (Refer to list of related manuals.)
01B1	10	Gate Assembly	6900720	IBM Corp.	Hinged on top. Contains typewriter logic circuits.
01B2	9	Gate Assembly	6900730	IBM Corp.	Hinged on top. Contains plotter logic circuits.
01B3	8	Gate Assembly	6900800	IBM Corp.	Hinged on top. Contains printer logic circuits.
01B4	7	Power Supply	6900740	IBM Corp.	Hinged on top. Contains power supplies 473390 and 477250. Provides -48 VDC to the typewriter and -12 VDC to PTC logic circuits.
01B5	41	Interlock and Filter Box Assembly	6900540	IBM Corp.	Hinged on top.
01B6	40	Resonator Supply	6900810	IBM Corp.	Hinged on top. Contains power supplies 473400 and 477210. Provides -20 VDC to the printer and -6 VDC to PTC logic circuits.
01B7	39	Power Supply	6900790	IBM Corp.	Hinged on top. Contains power supplies 473390 and 473410. Provides -6 VDC and +12 VDC for PTC logic circuits.

Figure 1-4. PTC Assemblies (Sheet 1 of 5)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturer's Designation	Manufacturer	Description
01B8	38	Power Supply	6900780	IBM Corp.	Hinged on top. Contains power supplies 473380 and 473520. Provides -12 VDC and +30 VDC for PTC logic circuits.
02A1	4	Memory Load and Data Display Panel Assembly	6900830	IBM Corp.	Hinged on left side. Contains controls and indicators required during processor memory loading and verification. (Refer to figure 3-7 for the description of each control and indicator on this panel.)
02A2	5	Processor Panel Assembly	6900840	IBM Corp.	Hinged on right side. Contains controls and indicators required for controlling and verifying processor operation. (Refer to figure 3-7 for the description of each control and indicator on this panel.)
02A4	20	Memory Array	6900634	IBM Corp.	Inside rear cabinet door. Contains a 4096 word memory module.
02A5	21	Memory Array	6900633	IBM Corp.	Inside rear cabinet door. Contains a 4096 word memory module.
02A6	22	Sense Cards Frame Assembly	6900609	IBM Corp.	Inside rear cabinet door. Contains processor memory logic circuits.
02B1	14	Gate Assembly	6900850	IBM Corp.	Hinged on top. Contains processor memory logic circuits.
02B2	13	Gate Assembly	6900860	IBM Corp.	Hinged on top. Contains processor timing generator and accumulator logic circuits.

Figure 1-4. PTC Assemblies (Sheet 2)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturers Designation	Manufacturer	Description
02B3	12	Gate Assembly	6900870	IBM Corp.	Hinged on top. Contains processor transfer register, OP codes and address register logic circuits.
02B4	11	Gate Assembly	6900880	IBM Corp.	Hinged on top. Contains processor CIO decoding logic circuits.
02B5	37	Gate Assembly	6900280	IBM Corp.	Hinged on top. Contains processor logic circuits.
02B6	36	Unused			
02B7	35	Unused			
02B8	34	Unused			
03A1	1	Tape Reader Control Panel Assembly	6900470	IBM Corp.	Hinged on left side. Mounted on slide mounted rack with assemblies 03A2 and 03A3. Contains controls and indicators for the tape reader and tape spooler. (Refer to figure 3-7 for the description of each control and indicator on this panel.)
03A2	2	Tape Reader Assembly	Model RR-1002B	Rheem Electronic Corp.	Mounted on slide mounted rack with assemblies 03A1 and 03A3. See maintenance instructions for this item. (Refer to list of related manuals.)
03A3	19	Tape Spooler Assembly	Model RS-500A	Rheem Electronic Corp.	Mounted on slide mounted rack with assemblies 03A1 and 03A2. See maintenance instructions for this item. (Refer to list of related manuals.)

Figure 1-4. PTC Assemblies (Sheet 3)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturers Designation	Manufacturer	Description
03A4	3	C. E. Panel Assembly	6900650	IBM Corp.	Located behind panel door. Contains controls, indicators and test points required for trouble shooting the PTC. (Refer to figure 3-7 for the description of each control and indicator on this panel.)
03A5	23	Gate Assembly	6900660	IBM Corp.	Hinged on bottom. Contains voltage sequencing relays used during power-up and power-down operations.
03A6	25	Power Supply	Model M36-5-0V (IBM Part Number 6900542)	Trygon Electronic Inc.	Provides +30 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
03A7	24	Power Supply	Model M36-5-0V (IBM Part Number 6900542)	Trygon Electronic Inc.	Provides +30 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
03A8	26	Power Supply	Model M15-10-0V (IBM Part Number 6900524)	Trygon Electronic Inc.	Provides +12 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
03A9	27	Power Supply	Model M15-10-0V (IBM Part Number 6900524)	Trygon Electronic Inc.	Provides +12 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
03A10	28	Power Supply	Model M36-10A-0V (IBM Part Number 6900525)	Trygon Electronic Inc.	Provides -28 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)

Figure 1-4. PTC Assemblies (Sheet 4)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturers Designation	Manufacturer	Description
03A11	33	Power Supply	Model M15-30A-0V (IBM Part Number 6900541)	Trygon Electronic Inc.	Provides -12 VDC for PTC circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
03B1	18	Gate Assembly		IBM Corp.	Hinged on top. (Spare gate assembly)
03B2	17	Gate Assembly	6900680	IBM Corp.	Hinged on top. Contains address and OP code logic circuits.
03B3	16	Gate Assembly	6900690	IBM Corp.	Hinged on top. Contains sector, syllable, and module logic circuits.
03B4	15	Gate Assembly	6900890	IBM Corp.	Hinged on top. Contains lamp driver logic circuits.
03B5	32	Gate Assembly	6900670	IBM Corp.	Hinged on top. Contains tape reader register logic circuits.
03B6	31	Gate Assembly	6900770	IBM Corp.	Hinged on top. Contains tape reader and timing control logic circuits.
03B7	30	Gate Assembly	6900760	IBM Corp.	Hinged on top. Contains tape reader parity and serializer logic circuits.
03B8	29	Gate Assembly	6900750	IBM Corp.	Hinged on top. (Spare gate assembly)

Figure 1-4. PTC Assemblies (Sheet 5)

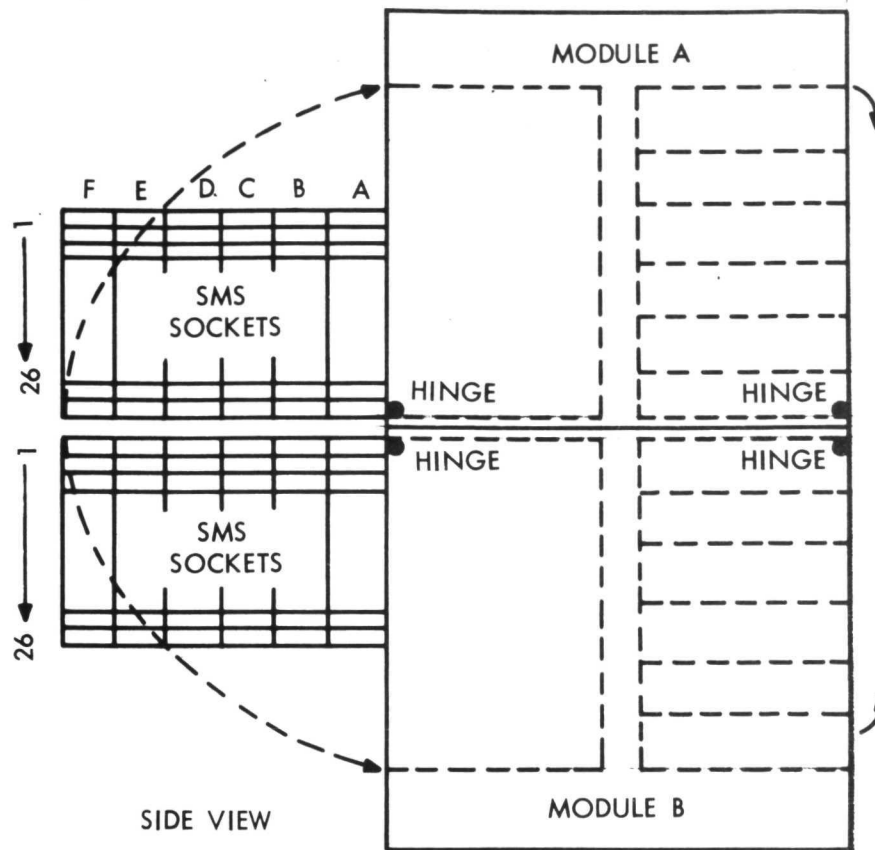


Figure 1-5. Gate Assembly Movement

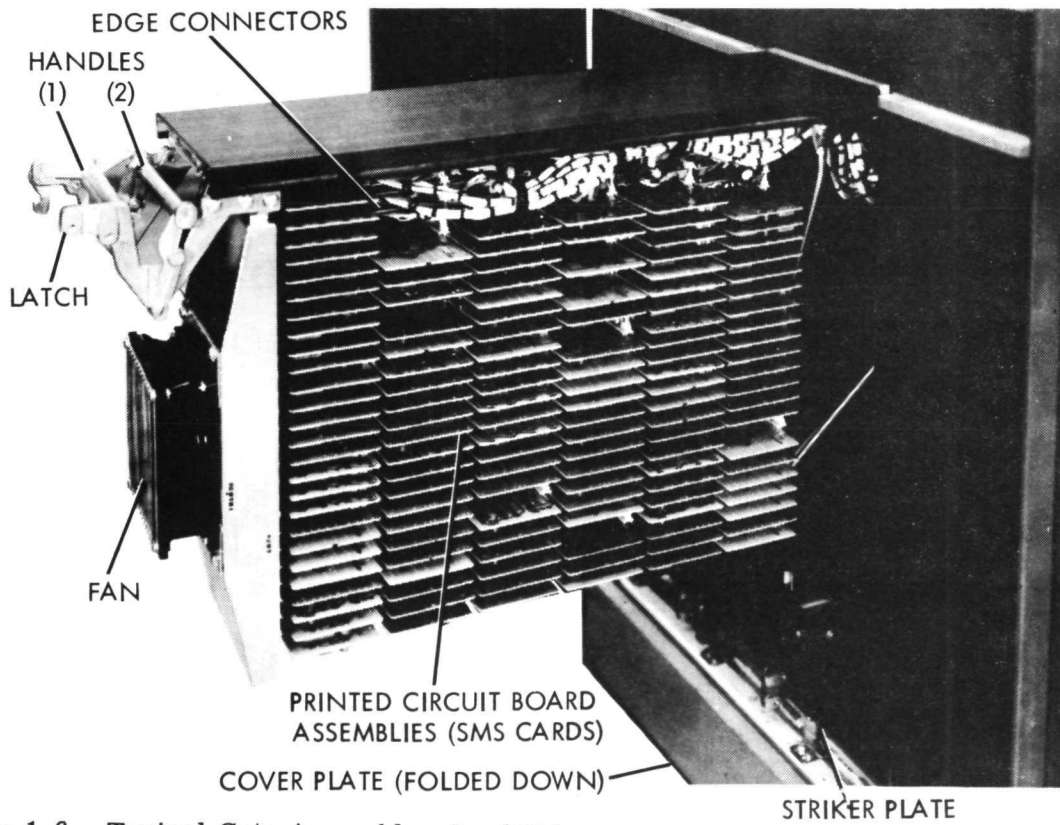


Figure 1-6. Typical Gate Assembly, Card Side

1-31. Each gate assembly contains 156 card sockets arranged in six columns and 26 rows. These sockets are the receptacles for the printed circuit board assemblies. Normally, the sockets in rows 1 and 2 of gate assemblies in the B modules are used for cable connectors. The cables that plug into these sockets are called edge connectors, since they make their connections at the edges of the gate assemblies.

1-32. Standard Modular System (SMS) Logic Cards. The logic circuits in the PTC are contained on printed circuit board assemblies called IBM Standard Modular System (SMS) cards. These pluggable printed circuit cards contain all the components and printed wiring necessary for a particular electronic function. A special program cap on some SMS printed circuit cards gives additional flexibility to this form of packaging, and reduces the number of cards required for field servicing. Each card is identified by a four-character card type code and a six- or seven-digit IBM part number. (See figure 1-7.)

1-33. The SMS single card, the kind used in the PTC, is made of an epoxy paper laminate material; it is approximately 1/16 inch thick, 4-1/2 inches long, and 2-1/2 inches wide. All of the electronic components and the program cap, if used, are mounted on the front side of the SMS card form. Connections to the components and program cap are made on the back side of the SMS card form by printed wiring patterns that terminate at contacts at the bottom of the card. These contacts, labeled A through R, couple the signals and voltages to the circuit components when the card is inserted into its receptacle. The printed circuit wiring (land pattern) depends on the type of circuit on the card.

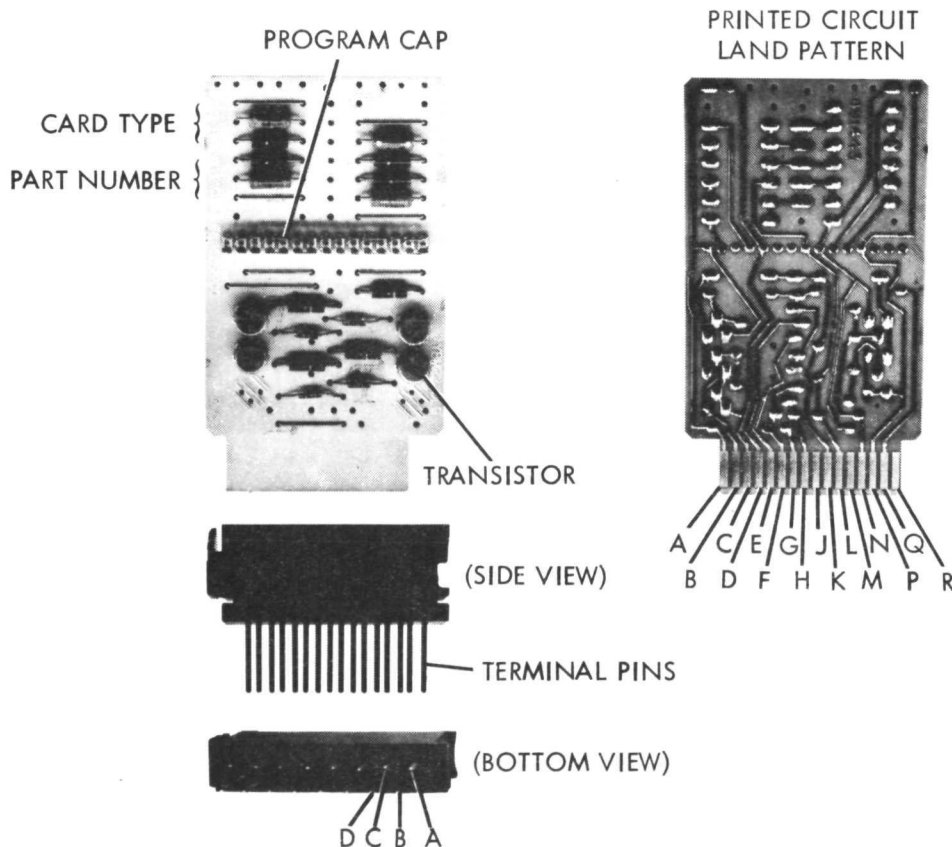


Figure 1-7. SMS Printed Circuit Card and Single-Position Receptacle

1-34. The program cap on the front of some SMS cards comprises two conductor rails which, in the pre-cut state, connect to tabs on the printed circuit land pattern. By cutting the program cap, various jumpering (cap) connections are made to the tabs to allow one SMS card to be used in several circuit configurations.

1-35. SMS Card Receptacles. The pluggable printed circuit cards are inserted into SMS card receptacles. The receptacles used in the PTC are the single-position type, shown on figure 1-7, and the eight-position type, which serves as a common receptacle for eight SMS cards, as shown on figure 1-8. Although the contacts are all in line on the card insertion side of the receptacle, they pass through the receptacle in a staggered arrangement. This arrangement allows additional room for wire-wrapping or soldering of wires to the terminal pins, as shown on figure 1-9.

1-36. Figure 1-9 shows how the pins of each SMS card (and receptacle) are identified, using an extension of the reference designation discussed previously.

1-37. Voltage Distribution Assemblies. Figure 1-9 also illustrates the standard position for a voltage distribution assembly in a module B gate assembly. A typical voltage distribution assembly is shown on figure 1-10.

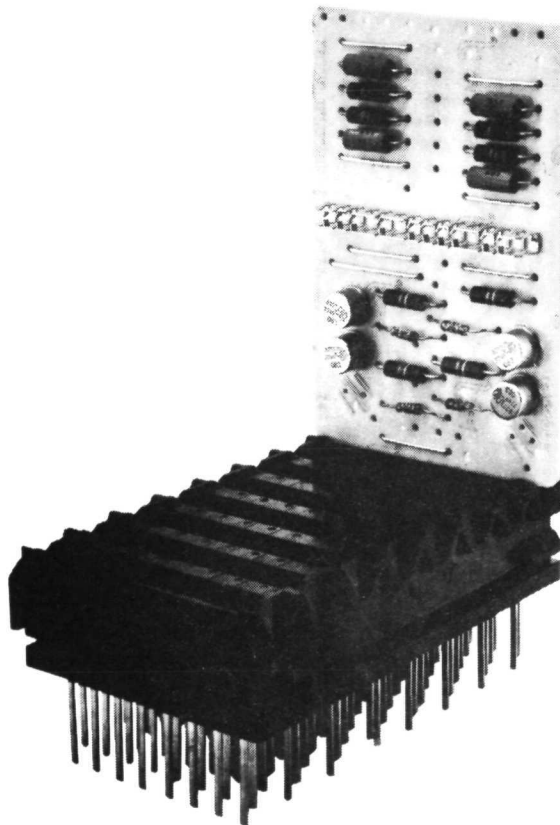


Figure 1-8. SMS Printed Circuit Card Inserted in Eight-Position Receptacle

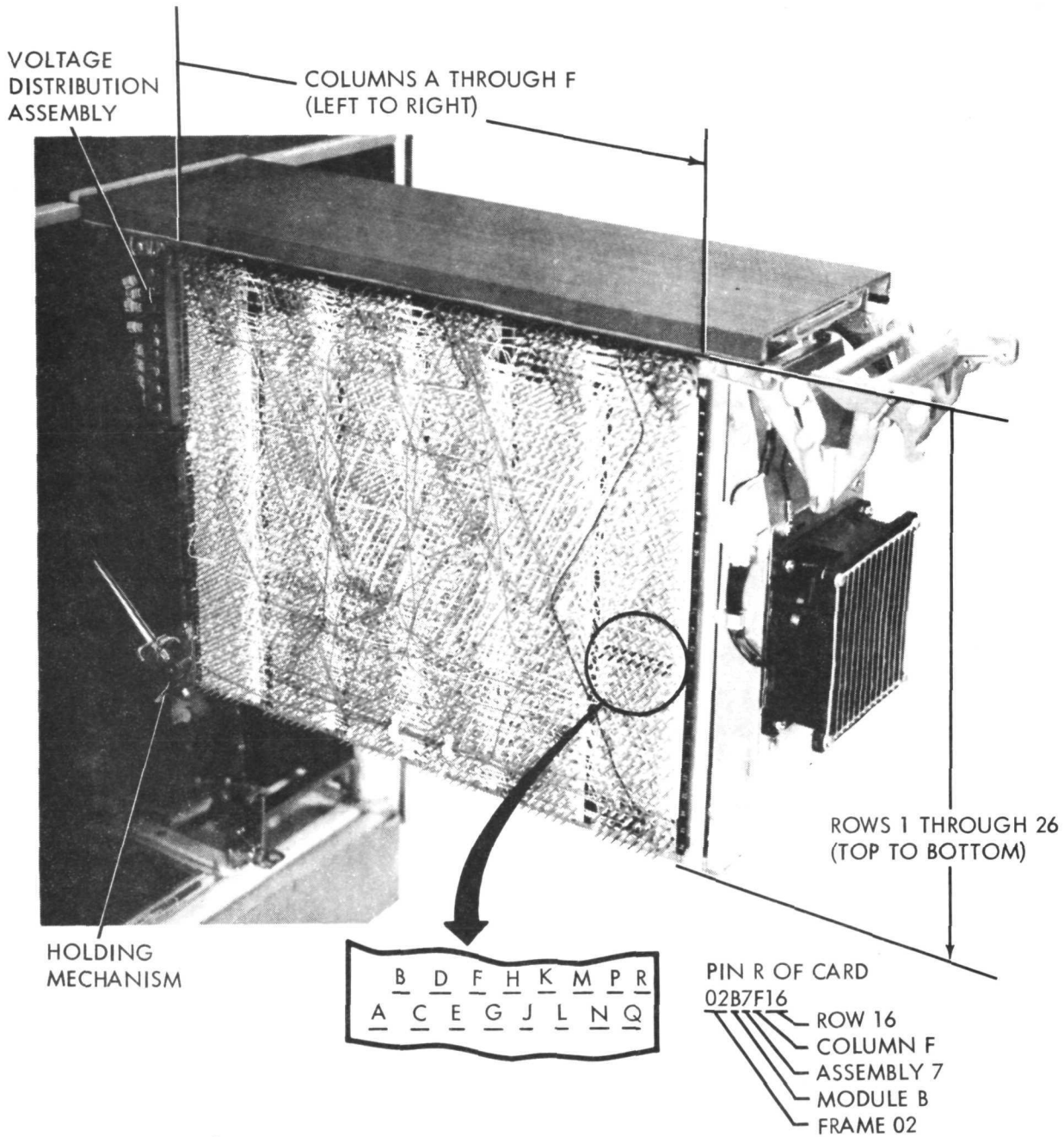


Figure 1-9. Typical Gate Assembly, Wiring Side

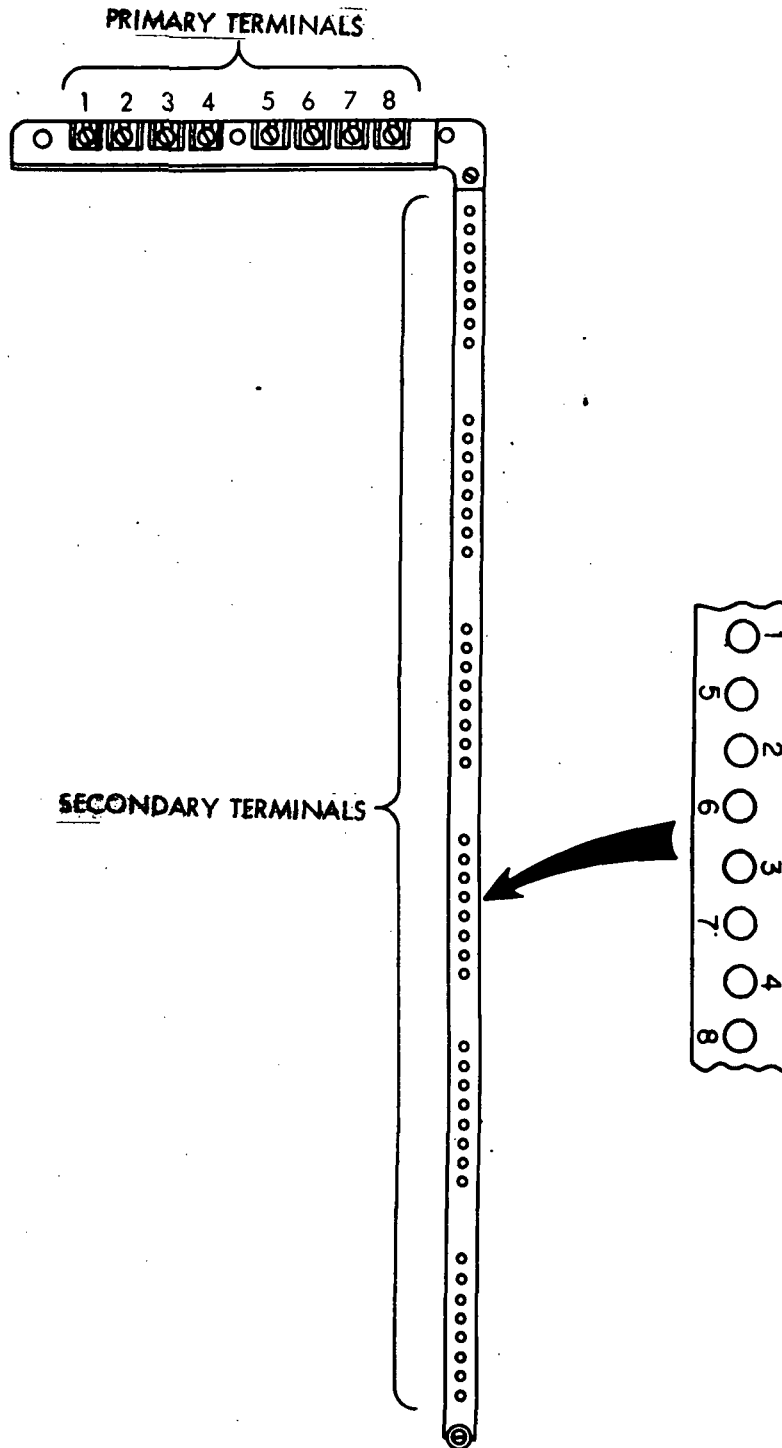


Figure 1-10. Typical Voltage Distribution Assembly

1-38. Each voltage distribution assembly contains a primary group of eight terminals and six secondary groups of eight terminals. Power is distributed within the assembly from the primary terminals to the secondary terminal of the same number; for example, power applied to the number 1 primary terminal is distributed to the eight number 1 secondary terminals of the voltage distribution assembly. Each secondary group of terminals transfers power to one row of SMS cards by jumpers from the secondary terminals to the SMS card receptacle pins. The jumpers from the secondary terminals are usually connected only to the pin of the nearest receptacle in which the voltage is used. From this first receptacle a voltage bus transmits the power to the pins of other receptacles in that row. Usually a voltage is restricted to pins of the same letter; for example, the K pin of most receptacles is connected to -6 VDC.

1-39. CONTROL PANELS. Each PTC control panel is divided into areas in which associated controls and indicators are mounted. The function of each group of controls and indicators is indicated by a prominent title in each area. Figure 3-8 (in Section III) lists and briefly describes all controls and indicators on these panels.

1-40. POWER SUPPLIES. Each of the six Trygon power supplies has been modified from the configurations shown in the maintenance manuals for these supplies. One modification is the replacement of the standard input plugs with plugs that fit the power supply receptacles in the PTC. The other modification is the removal of internal power supply jumpers to allow remote rather than local sensing of the power supply voltages.

1-41. Each power supply can provide an output that is current and/or voltage regulated. In the PTC, each current regulation circuit is disabled by placing the CURRENT potentiometer in the full clockwise position.

1-42. ELECTRICAL, MECHANICAL, AND ENVIRONMENTAL CHARACTERISTICS.

1-43. Figure 1-11 lists the salient electrical, mechanical, and environmental characteristics of the PTC.

<p>Input Power</p>	<p>Phase: 3 phase; 5 wire; wye connected; phase sequence is ABC</p> <p>Frequency: 60 (± 5) cycles/second.</p> <p>Voltage: 115 (± 11.5) VAC line-to-neutral (208 VAC line-to-line minimum)</p> <p>Current: 20 (minimum) to 30 (maximum) amperes/phase</p>
<p>Environment</p>	<p>Ambient Temperature: +60 +95 degrees Fahrenheit</p> <p>Relative Humidity: 10 to 80 percent</p>

Figure 1-11. Electrical, Mechanical and Environmental Characteristics (Sheet 1 of 2)

<p>Mechanical Packaging</p>	<p>Cabinet: Three frames. Two frames (02 and 03) mechanically and electrically bonded together</p> <p>Size: Height - 60 inches Length - 58 inches Depth - 31 inches Weight: 1700 pounds</p> <p>Frame 01 is not mechanically secured to frames 01 and 02 but is electrically connected.</p> <p>Size: Height - 60 inches Width - 30 inches Depth - 31 inches Weight: 800 pounds</p> <p>Logic Chassis Design: Hinged on one edge for ease of accessibility; a blower is mounted on each chassis for cooling of SMS circuit cards and components.</p> <p>Printed Circuit Cards: The basic logic subassembly is SMS cards.</p>
<p>Central Processing Unit</p>	<p>Storage: Core Memory - 8196 words of simplex storage</p> <p>Data Word Length: 28 bits - 26 data plus 2 parity bits</p> <p>Arithmetic: Add/Subtract - 82 microseconds/operation Data Accuracy - 25 bits plus sign</p> <p>Interrupts: 16 hardwire interrupts</p> <p>Instruction Word Length: 13 bits plus one parity bit; 2 instructions/computer word</p> <p>Timing: Clock Oscillator - 2.048 megacycles Computer Cycle - 81.9 microseconds Phases - Three phases/computer cycle; each phase 27.3 microseconds, labeled A, B, and C</p> <p>Bit Time: 14 bit times/phase time, numbered 1 through 14</p> <p>Clock Times: 4 clocks/bit time; clocks are labeled W, X, Y, Z; each occurs at 512 KC rate</p>

Figure 1-11. Electrical, Mechanical and Environmental Characteristics (Sheet 2)

SECTION II

THEORY OF OPERATION

2-1. SCOPE.

2-2. This section describes the operation of the PTC circuits. The PTC is composed of three functional units: (1) Central Processor, (2) Memory Loader/Data Display, and (3) Input/Output. A Self Check feature is also incorporated.

2-3. The descriptions contained in this section are as follows:

1. Power Distribution
 - a. AC Power Distribution
 - b. DC Power Distribution
2. Subsidiary Circuits
 - a. Exclusive OR Comparators
 - b. Binary Counters
 - c. Parity Detectors
 - d. Indicator Lamp Circuits
 - e. PTC Timing
3. Central Processor
4. Memory Loader/Data Display
5. Input/Output
6. Self Check

2-4. In describing the functions, simplified diagrams and timing charts are presented to familiarize the reader with the equipment. Detailed drawings are provided in Section X; reference to these drawings is made as necessary.

2-5. The signal names in the logic diagrams in Section X are preceded by voltage level symbols. The voltage levels represented by these symbols are as follows:

<u>Symbol</u>	<u>"1"</u>	<u>"0"</u>
+C	+1.3 VDC	-1.25 VDC
-C	-1.25 VDC	+1.3 VDC
+R	+12.0 VDC	0 VDC
-R	0 VDC	+12.0 VDC
+S	0 VDC	-12.0 VDC
-S	-12.0 VDC	0 VDC
+W	0 VDC	-48.0 VDC
-W	-48.0 VDC	0 VDC
+Y	0 VDC	-6.0 VDC
-Y	-6.0 VDC	0 VDC

2-6. POWER DISTRIBUTION.

2-7. AC POWER DISTRIBUTION. (See figures 10-7, 10-9, 10-10, 10-13, and 10-14.)

2-8. Primary power (115 VAC, 60 cycle, 3-phase) is applied to connector 01B5J1 (figure 10-7.) Each phase is applied through circuit breaker 01B5CB1 to movable contacts of relay 01B5K2. Phase B (through circuit breaker 01B5CB3) and phase C are also connected across the primary of transformer 01B5T1. The secondary winding of transformer 01B5T1 develops 24 volts. The 24 volts is used for power control when the jumper plug is installed on receptacle 9009J4 or when cable 6900915 is connected between receptacles 9009J4 and 01J11. The power control voltage is routed through the normally closed contacts of PTC MAIN PWR-EMERGENCY PULL switch 02A2S81 (figure 10-14), normally closed contacts of PTC MAIN PWR-PWR OFF switch 02A2S82, and normally closed contacts of relay 01B5K1 to PTC MAIN PWR-PWR OFF lamps 02A2DS70.

2-9. When PTC MAIN PWR-PWR ON switch 02A2S83 is actuated, relay 01B5K1 picks and holds through its own contacts. The power control voltage is now routed through normally closed contacts of switch 02A2S81; normally contacts of switch 02A2S82; interlock switches 03S4, 03S1, and 01S1; and normally closed contacts of relay 01B5K1 to PTC MAIN PWR-PWR ON lamp 02A2DS71.

2-10. Relay 01B5K2 picks when relay 01B5K1 picks. (See figure 10-7.) Primary power is then routed through the normally open contacts of relay 01B5K2 to fan motors, DC power supplies, tape reader and spooler, plotter, and typewriter and printer interface. The phases are distributed as follows (figure 10-9):

- Phase A: -48 VDC power supply (01B4PS1)
- 12 VDC power supply (01B4PS2)
- 12 VDC power supply (01B8PS1)
- +30 VDC power supply (01B8PS2)
- 6 VDC power supply (01B7PS1)
- +12 VDC power supply (01B7PS2)

- 6 VDC power supply (01B6PS1)

-20 VDC power supply (01B6PS2)

Regulator (01B6)

Phase B: All fan motors

+30 VDC power supply (03A6)

+30 VDC power supply (03A7)

+12 VDC power supply (03A8)

+12 VDC power supply (03A9)

-28 VDC power supply (03A10)

Printer interface

Phase C: Tape reader and spooler

Plotter

Typewriter interface

Printer interface

-12 VDC power supply (03A11)

2-11. When PTC MAIN PWR-PWR OFF switch 02A2S82 is actuated the control voltage is momentarily removed from the coil of relay 01B5K1. This action causes relays 01B5K1 and 01B5K2 to drop, removing primary power from the fan motors, DC power supplies, tape reader and spooler, plotter, and typewriter and printer interfaces.

2-12. DC POWER DISTRIBUTION . (See figures 10-11, 10-12, 10-17, 10-18, 10-19, 10-20, and 10-21.)

2-13. DC power distribution paths are controlled by relays and switches. The circuit paths vary when the relay and switch contacts are transferred. The subsequent description covers the initial conditions and the voltage sequencing during DC power on and DC power off operations.

NOTE

In the following discussion prefix all abbreviated reference designations with 03A5.

2-14. Initially all DC power distribution relays are deenergized and -28 VDC which is applied to PTC DC PWR-PWR OFF lamps 02A2DS72 is returned through the normally closed contacts of relay K12. When PTC DC PWR-PWR ON switch 02A2S85 is actuated relays K5A, K5B, K5C, and K5D pick. (See figure 10-20.) These relays are held picked

through the interlocks formed by the normally closed (NC.) contacts of relay K7 and the normally open (NO.) contacts of relay K5D. Relays K1, K2, K3, K8, and K10 are now picked by power supply voltages as follows (figures 10-18, 10-19, and 10-21):

<u>Relay</u>	<u>Power Supply</u>	<u>Interlock Switches</u>
K1	- 6 VDC (01B7)	K5B NO. contacts
K2	-12 VDC (03A11)	K5C NO. contacts
K3	+12 VDC (03A8)	K5A NO. and K6 NC. contacts
K8	+12 VDC (01B7)	K5A NO. contacts
K10	+12 VDC (03A9)	K5A NO. and K6 NC. contacts

2-15. When relays K1, K2, K3, K8, and K10 pick, energizing voltages are applied to time-delay relays K4, K9, and K11 as follows (figure 10-17):

<u>Relay</u>	<u>Power Supply</u>
K4	+30 VDC (03A6)
K9	+30 VDC (03A7)
K11	+30 VDC (01B8)

Relays K4, K9, and K11 pick after approximately 1.5 seconds applying 28 VDC across the coil of relay K12 and PTC DC PWR-PWR ON lamps 02A2DS73 completing the DC power on sequencing. (See figure 10-20).

2-16. The DC voltages are distributed as follows (figures 10-17, 10-18, 10-19 and 10-21):

- +12 VDC (03A8) -- Memory (through relay K5A NO. contacts).
- +12 VDC (03A9) -- Memory (through relay K5A NO. contacts).
- +12 VDC (01B7) -- Printer interface.
- Bus bar, memory, CE PANEL, MEMORY LOAD AND DATA DISPLAY panel, TAPE READER AND MODE CONTROL panel, and PROCESSOR DISPLAY PANEL (through relay K5A NO. contacts).
- 12 VDC (01B4) -- Printer interface
- 12 VDC (01B8) -- Indicator lamps (through relay K5B NO. contacts).
- 12 VDC (03A11) -- Memory and bus bar (through relay K5C NO. contacts).
- +30 VDC (03A6) -- Memory (through relays K1, K2, K3, K4, K8, and K10 NO. contacts).
- +30 VDC (03A7) -- Memory (through relays K1, K2, K3, K8, K9, and K10 NO. contacts).

- +30 VDC (01B8) -- Memory (through relays K1, K2, K3, K8, K10, and K11 NO. contacts).
- +28 VDC (03A10) -- MEMORY LOAD AND DATA DISPLAY panel, CE PANEL, PROCESSOR DISPLAY panel, TAPE READER AND MODE CONTROL panel, gate 03B6, and the coil of relay 01B4K1 (through relay K5D NO. contacts).
- 48 VDC (01B4) -- Typewriter interface (through relay 01B4K1 NO. contacts).
- 20 VDC (01B6) -- Printer interface.
- 6 VDC (01B6) -- Printer interface.
- 6 VDC (01B7) -- Bus bar, CE PANEL, memory, PROCESSOR DISPLAY PANEL, and MEMORY LOAD AND DATA DISPLAY panel.

2-17. When PTC DC PWR-PWR OFF switch 02A2S84 is actuated relay K6 picks and holds through the interlocks formed by relay K6 NO. and relay K7 NC. contacts. figure 10-20). When relay K6 picks; (1) energizing voltage is applied to time-delay relay K7; and (2) relays K3, K4, K9, K10, K11 and K12 are deenergized. Relay K7 picks after approximately 1.5 seconds. This action causes relays K1, K2, K5A, K5B, K5C, K5D, and K8 to deenergize. Also, when relay K7 picks, relay K6 is deenergized which in turn deenergizes relay K7. Relays K1 through K12 are now deenergized and the DC power off sequencing is complete.

2-18. SUBSIDIARY CIRCUITS.

2-19. Subsidiary circuits are those circuits that are related to more than one PTC function. These circuits are necessary to the operation of the PTC and are categorized as such only to prevent repetitious explanations.

2-20. EXCLUSIVE OR COMPARATORS.

2-21. The PTC contains many exclusive OR comparators that compare corresponding data from two sources. Figure 2-1 shows a typical exclusive OR comparator in which three parallel inputs (X1, X2, and X3) are compared with three other parallel inputs (Y1, Y2, and Y3).

2-22. If a compare exists, the input to each A0 will be unlike, and the output of each A0 will be a "1". This will result in a "1" on the COMPARE line and a "0" on the COMPARE NOT line. If a compare does not exist, at least one of the A0's will have two "1" inputs. This will result in a "0" on the COMPARE line and a "1" on the COMPARE NOT line.

2-23. Two additional A0's are required to compare each additional pair of inputs. A single stage comparator is used to compare serial data from two sources.

2-24. BINARY COUNTERS.

2-25. The PTC contains many binary counters which are alternately set or cleared everytime the signal they are monitoring changes from a "0" to a "1". Figure 2-2 shows a typical binary counter which is monitoring signal B and controlled by signal A.

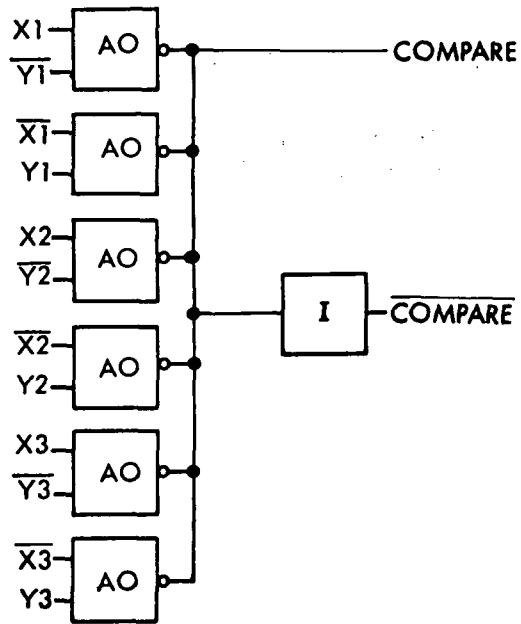


Figure 2-1. Typical Exclusive OR Comparator Circuit

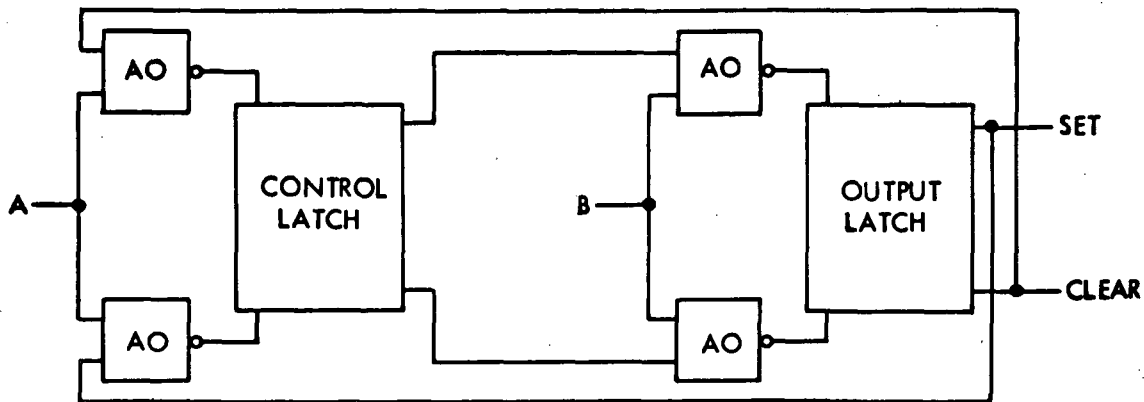


Figure 2-2. Typical Binary Counter

2-26. The control latch stores the configuration of the output latch providing A is a "1". The output latch is then alternately set or reset everytime B goes from a "0" to a "1". When A is a "0" the configuration of the output latch cannot be changed. The binary counter can be initially set or cleared by routing a signal through an inverter to the output latch set or reset input.

2-27. PARITY DETECTORS.

2-28. The PTC contains several parity detectors that are used for parity bit generation and parity error detection. These parity detectors detect whether an odd or even amount of "1's" is contained in the information feeding them. (See figure 2-3.)

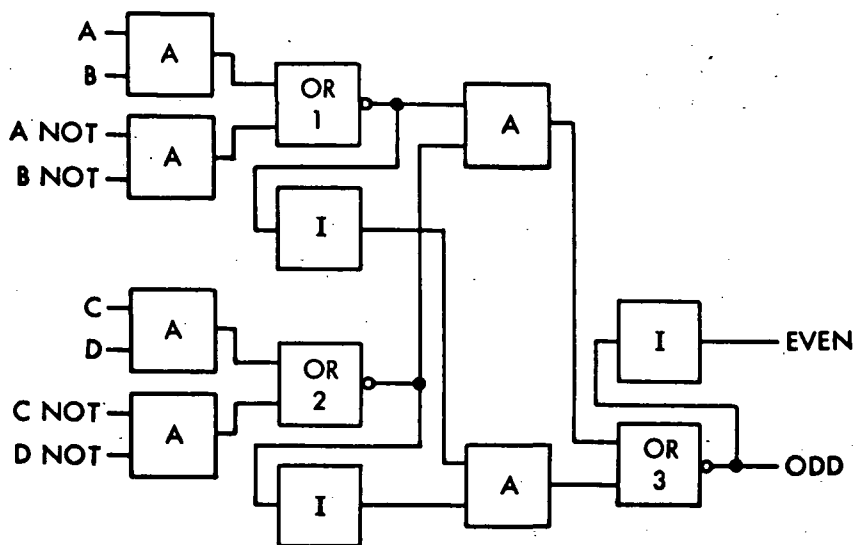


Figure 2-3. Typical Parity Detector

2-29. When none, 2, or four of the inputs A, B, C, and D are "1's" the outputs of OR circuits 1 and 2 are the same value. Therefore one of the inputs to OR circuit 3 is a "1" and the EVEN and ODD outputs are respectively a "1" and a "0". When an odd number of the inputs are "1's" the outputs of OR circuits 1 and 2 are unlike values. Thus the inputs to OR circuit 3 are "0's" and the EVEN and ODD outputs are a "0" and "1" respectively.

2-30. INDICATOR LAMP CIRCUITS.

2-31. The PTC contains many indicator lamps that are associated with either switches or latches. These lamps are all commonly connected to -12 VDC on one side. A lamp associated with a switch is lighted by providing a return path to ground for -12 VDC through the lamp and the normally open or normally closed contacts of the switch.

2-32. A lamp associated with a latch is connected in the collector circuit of an indicator driver. The lamp is lighted by a "1" input into the indicator driver which is fed by the set or reset output of a latch.

2-33. The lamps on the CE PANEL, PROCESSOR DISPLAY PANEL, MEMORY LOAD AND DATA DISPLAY, and TAPE READER AND MODE CONTROL panels are lighted when the associated LAMP TEST pushbuttons are depressed. When the LAMP TEST pushbuttons are depressed, the lamps are lighted as follows:

1. By applying ground to the lamps associated with switches.
2. By removing the +12 VDC control voltage which is normally applied to the indicator drivers and applying -28 VDC.

2-34. PTC TIMING.

2-35. The timing circuits generate timing signals for the operation of the PTC logic. The PTC timing is generated under control of external synchronization signals from the LVDCME or LVDAME. The timing circuits consist of the clock generator, the bit gate generator, the phase generator, and the sync control circuit. The timing relation between the various timing gates developed by the timing circuits is shown on figure 2-4.

2-36. In this section, timing is designated by a three-part notation that indicates the phase, bit-gate, and clock-time. For example phase B bit-gate 13 clock-time X is designated by the notation B-13-X time. In instances where the three levels of timing do not apply, only the timing levels specified appear in the notation. For example phase B bit-gate 13 and clock-time X are designated by B-13 time and X time respectively.

2-37. CLOCK GENERATOR (Figure 10-28, sheet 4). The clock generator is triggered by W clock pulses from the LVDCME or LVDAME. These pulses are delayed a total of four clock times by two delays. The delayed W clock (W DLY) triggers a single shot which produces the PTC W clock pulses (CPW). Similarly the W clock pulses are delayed five, six, and seven clock times to produce CPX, CPY, and CPZ respectively. The clock pulses occur at a repetition rate of 512 KC.

2-38. BIT GATE GENERATOR (Figure 10-28, sheets 5 and 6). The bit gate generator consists of a control circuit, a seven stage shift register, and a bit decoding circuit.

2-39. The control circuit is a binary counter which is complemented every Y time. The outputs of the binary counter (A and A NOT) control the rate at which the shift register is cycled.

2-40. The shift register produces seven outputs (G1 through G7) which change states as shown on figure 2-5. The bit decoder generates 14 signals that identify the 14 bit times. These signals are produced by ANDing the outputs of the shift register as follows:

BG1	=	G1 and G2 NOT
BG2	=	G2 and G3 NOT
BG3	=	G3 and G4 NOT
BG4	=	G4 and G5 NOT
BG5	=	G5 and G6 NOT
BG6	=	G6 and G7 NOT
BG7	=	G1 and G7
BG8	=	G1 NOT and G2
BG9	=	G2 NOT and G3
BG10	=	G3 NOT and G4
BG11	=	G4 NOT and G5
BG12	=	G5 NOT and G6
BG13	=	G6 NOT and G7
BG14	=	G1 NOT and G7 NOT

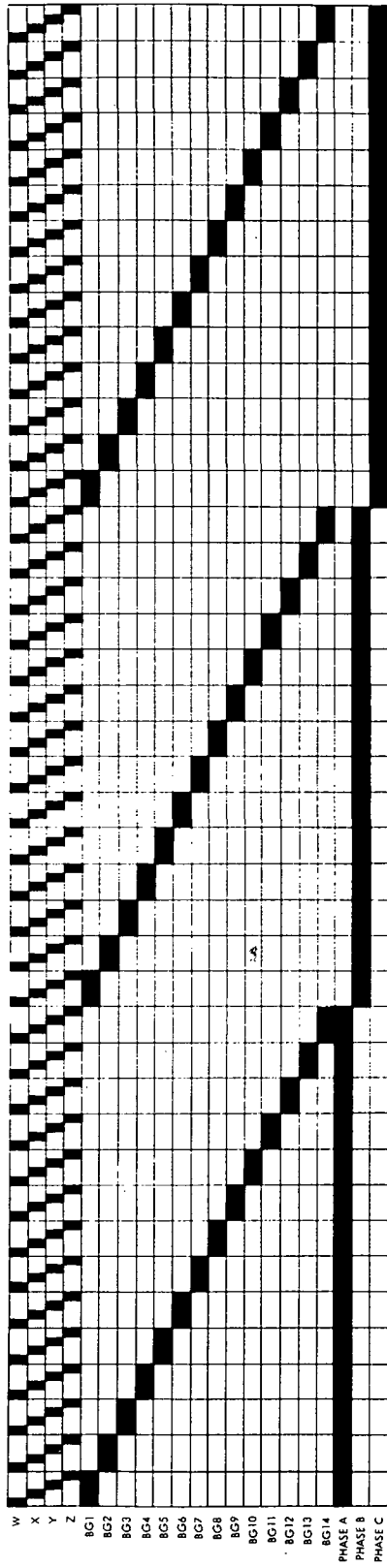


Figure 2-4. PTC Timing Gates

BIT TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	1	0	1	0	1	0	1	0	1	0	1	0	1	0
\bar{A}	0	1	0	1	0	1	0	1	0	1	0	1	0	
G1	0	0	0	0	0	0	1	0	0	0	0	0	0	
G2	0	1	0	0	0	0	0	0	1	0	0	0	0	
G3	0	0	1	0	0	0	0	0	0	1	0	0	0	
G4	0	0	0	1	0	0	0	0	0	0	1	0	0	
G5	0	0	0	0	1	0	0	0	0	0	0	1	0	
G6	0	0	0	0	0	1	0	0	0	0	0	0	1	
G7	0	0	0	0	0	0	1	0	0	0	0	0	0	

Figure 2-5. Bit Gate Generator Timing

2-41. PHASE GENERATOR (Figure 10-28, sheet 5). The phase generator is a three-step ring counter formed from three latches (PA, PB, and PC). The ring stabilizes itself with one latch set and two reset; the set condition is then stepped around the ring in alphabetical sequence each bit 1 time. At W time the next latch in the sequence is set; at the following Y time, the preceding latch is reset.

2-42. SYNC CONTROL CIRCUIT (Figure 10-28, sheets 4 and 7). The sync control circuit receives the phase B NOT signal from the LVDCME or LVDAME. This signal triggers a single shot which produces the sync control pulse (SYNC CTRL) every LVDCME or LVDAME B-1 time. This pulse is sent to the bit gate generator where it sets the control circuit and shift register to states that correspond to bit one time. The sync pulse is also sent to the phase generator where it sets the PB latch.

2-43. A sync error is generated if the PTC timing is not within one bit time of the LVDCME or LVDAME timing when the sync control pulse is generated. Sync errors are stored in a latch which produces an output, SYNC ERR. If a sync error is detected, the clock on/clock off trigger is reset which halts the generation of PTC clock pulses.

2-44. CENTRAL PROCESSOR

2-45. The following paragraphs describe the operation of the Central Processor. The general organization of the Central Processor is described first, followed by a description of the logic circuits.

2-46. CENTRAL PROCESSOR ORGANIZATION.

2-47. Functionally the Central Processor is a modified version of the Launch Vehicle Digital Computer. The following describes the organization of the Central Processor from the aspects of its functional organization, word organization and timing organization and the instructions it may be programmed to perform.

2-48. FUNCTIONAL ORGANIZATION. The Central Processor is a general purpose computer which, under control of a stored program, processes data using fixed point, two's complement arithmetic. Data is processed serially in an arithmetic section which performs addition, subtraction, and logical extractions.

2-49. The principal storage device is a random access ferite-core memory with separate controls for data and instruction addressing. The memory operating mode is program controlled. Temporary storage is provided by static and shift registers composed of latches.

2-50. The major parts of the Central Processor and how they are inter-connected are shown on figure 10-28, sheet 3. The Central Processor consists of the memory and memory control, data control, program control, arithmetic, and external control elements. The composition of these elements is as follows:

- Memory and Memory Control — Core Arrays A and B
Sense Amplifier A and B
Inhibit Drivers
Address Drivers
Memory Timing
Memory Buffer Register
Parity Check Logic
- Data Control — Transfer Register and Controls
- Program Control — Address Register
OP Code Register
Data Sector Register
Instruction Sector Register
Data Module Register
Instruction Module Register
HOP Saver Register
Instruction Word Syllable Control Logic
- Arithmetic — Accumulator Register and Controls
- External Control (Not shown on block diagram). — Central Processor Start Stop and Interrupt Control Logic.

2-51. Memory and Memory Control Element. The programmed instructions, and the constants and data required by the program are stored in the memory under control of the memory control circuits. The memory control circuits determine when a transfer will occur and select both the direction of transfer and the memory location to be exercised. Data being transferred into or out of the memory is routed through buffer storage.

2-52. The memory is composed of two arrays (module 0 and module 1) each of which contains 16 sectors (0 through 17₈). Each module contains different information and only one module can be selected at a time. Each sector contains 400₈ addresses ranging from 0 through 377₈. Sector 17₈ of module 0 is set aside for residual storage and its addresses range from 400₈ to 777₈.

2-53. Data words and constants are stored in the sector addresses in two segments called syllables. Thus, the memory is described as being divided into syllables. One syllable of data is transferred to or from the memory at a time; consequently, two memory cycles are necessary to transfer a complete data word. Instructions are only half the length of data words and thus are stored one per syllable.

2-54. A parity check is performed on information being read into memory and odd parity is assigned if required. A parity check is also performed on information being read out of memory and if odd parity does not exist a parity error is generated.

2-55. Data Control Element. Data words and constants enter the transfer register from the memory in two syllables. Each syllable enters the transfer register in parallel and is then serialized and distributed to the arithmetic element and the Memory-Loader/Data Display.

2-56. Data words which are bound for the memory enter the transfer register in serial form from the arithmetic element, the program control element, or the Memory Loader. The transfer register then divides them into syllables and forwards each syllable to the memory buffer register in parallel. At the memory buffer register, a "parity bit" is added to each syllable before it is stored in the memory. The parity counter monitors the number of "1's" entering the transfer register and assigns odd parity to the memory buffer register by controlling the parity bit.

2-57. Another item which enters the transfer register serially is the contents of the instruction counter. The instruction counter controls the normal sequencing of the program through the memory. Just before a new instruction is required, the contents of the instruction counter are shifted into the transfer register and transferred in parallel to the address register in the program control element. The address register then selects the memory sector address location of the new instruction.

2-58. When the new instruction is read, it is transferred from the memory buffer register into the transfer register. The instruction is then separated into an operation code and an operand address; the two parts are transferred in parallel to the program control element. The operation code is loaded into the operation code register and the operand address into the address register. The operand address of some instructions constitutes a special constant which, in addition to the parallel transfer, is shifted out of the transfer register in serial form.

2-59. Program Control Element. The program control element stores and decodes the programmed instructions and in addition, controls sequencing the program through the memory. The operation code register and the address register store their respective parts of the instructions. Outputs of the operation code register, and those of the operation decoders, control the arithmetic, data, and memory and memory control elements, and parts of the program control element to perform the commanded operations.

2-60. The address register selects the memory sector address location of the data to be used in the commanded operation. When the operation is complete, the address register is reloaded with the contents of the instruction counter to address the next instruction. The memory module and sector selection is controlled by (1) the data module register and the instruction module register and (2) by the data sector register and the instruction sector register.

2-61. The module and sector registers preselect an area of the memory within which the program must operate. As implied by the names of the registers, two selections

are made, one for data and one for instructions (the same area may be selected for both). The syllable selection for instructions is stored in the instruction word syllable control logic. Timing signals determine whether the stored selection will be used or whether the selection will be sequenced to read both syllables of a data word. The address register then selects individual locations within the preselected areas from which data and instructions will be read. Timing signals discriminate between instruction and data addressing. The contents of the module and sector registers are changed upon command of the program.

2-62. It was noted previously that the program control element controls sequencing the program through the memory. Actually, the program controls its own sequencing through the use of instructions which command the program control element to change the contents of the module and sector registers (discussed in the preceding paragraph), and the instruction counter.

NOTE

Although the instruction counter is logically part of the program control element, it is instrumented in the arithmetic element.

The instruction counter stores the address of the next instruction to be operated. Each time the Central Processor performs an instruction, the instruction address is incremented by one to develop the address of the following instruction. In this manner, the program steps sequentially through the area of memory selected by the instruction module register and the instruction sector register.

2-63. The sequential stepping continues until the program issues an instruction to alter the sequence or select a different area of the memory to read instructions from. Area selection is changed by shifting a "HOP constant" out of the transfer register which reloads the module and sector registers. The same HOP constant also reloads the instruction counter to select the starting location of the next instruction sequence. The instruction counter then begins stepping sequentially through the newly selected memory area beginning at the specified starting point.

2-64. The instruction counter can also be reloaded without affecting the module and sector registers. This feature permits repeating short program loops and enables the computer to make logical choices. When commanded, the computer can examine the contents of the accumulator register for certain conditions and alter the program sequence if the condition exists. If the condition is not met, sequential stepping continues.

2-65. The hop saver register is loaded with a HOP constant, every Central Processor cycle, which identifies the locations in memory currently selected. The contents of the hop saver register can then be stored in residual address 776g or 777g. Thus after transferring out of a routine the program may be directed back to that routine by referring to the HOP constant stored in address 776g or 777g.

2-66. Arithmetic Element. The arithmetic element performs addition, subtraction, shifts, and logical extractions. The accumulator register provides one of the operands for all arithmetic instructions and the memory provides the other. The two operands are combined in the accumulator control logic and the result is stored in the accumulator. The result can then be sensed to control logical decisions or it can be transferred

to the memory. After sensing or transfer the result remains unchanged in the accumulator register.

2-67. To illustrate a typical operation, assume that the Central Processor program has been initiated and is running smoothly. The area of the memory in which the program will operate has been selected and instructions are coming from syllable zero. For descriptive purposes, a typical operation begins with reading an instruction from the memory. The address of the instruction is shifted out of the instruction counter and applied to the transfer register and the accumulator control logic in the arithmetic element. The accumulator control logic increments the count by one and reinserts it into the accumulator register where it is circulated. The instruction address is shifted into the transfer register and then transferred in parallel to the address register.

2-68. Timing signals indicate to the memory control circuits that an instruction is due to be read. The memory control circuits then decode the contents of the instruction module and instruction sector registers rather than the data module and data sector registers. Syllable zero, which is the stored syllable selection for instructions, is also decoded. The memory control circuits then produce read timing pulses which enable the instruction to be transferred out of the addressed memory location.

2-69. The memory sense amplifiers transmit the instruction to the memory buffer register. The memory buffer register stores the instruction for parity checking and to enable the inhibit drivers during the restore memory cycle. The instruction is then transferred from the memory buffer register to the transfer register.

2-70. Reading information from a ferrite-core memory destroys the information in the memory. Consequently, a read operation must always be followed by a store (or restore) operation to preserve the contents of the memory. The restore operation is accomplished after the instruction has been transferred to the transfer register. The memory control circuits produce store timing pulses which transfer the instruction from the memory buffer register back into the memory through the inhibit drivers.

2-71. Upon entering the transfer register, the instruction is separated into an operation code and an operand address. The operation code defines what operation will be performed and the operand address gives the location in memory of the data to be used in the operation. The operation code is transferred in parallel to the operation code register and the operand address to the address register. The remainder of the operation is dependent upon the code transferred to the operation code register. The code can specify any of three general types of operations: 1) those which require data from memory; 2) those which place data into the memory; and 3) those which do not use the memory.

2-72. Assume first that the operation code requires data to be read from the memory. The instruction word syllable control circuit selects syllable zero, the first syllable of the data word. The memory control circuits decode the contents of the address, data sector, and data module registers. A read cycle is then initiated which transfers the first half of the data word to the memory buffer register. While in the memory buffer register, the half-data word is parity checked, then transferred to the transfer register and restored in the memory. The transfer register serializes the data by shifting it to the TRS output. The TRS output makes the data available to the Arithmetic, program and memory, and memory control elements and to the Memory Loader/Data Display. Outputs from the operation code register and the operation decoders determine which element will accept the data and how it will be used.

2-73. As the first half of the data word nears the end of the transfer register, the instruction word syllable control circuit selects syllable one and the memory control circuits initiate another read cycle. This read cycle transfers the second half of the data word into the memory buffer register where it is parity checked. Then, just in time to fall in behind the last bit of the first half data word, the second half of the data word is transferred into the transfer register. The transfer register continues shifting and the two halves of the data word appear as a continuous serial output on the TRS line.

2-74. When providing a data output, the transfer register is synchronized with the accumulator register. The output of the transfer register and the contents of the accumulator register are combined bit-for-bit in the accumulator control logic. The results of these operations are placed in the accumulator register for recirculation. As the last bit of the accumulator contents emerges from the accumulator register, timing signals end the arithmetic processes in the accumulator control logic and the contents of the instruction counter begin to emerge from the accumulator register. The accumulator control logic increments the instruction count by one and reinserts it in the accumulator register immediately behind the result of the arithmetic operation. Simultaneously, the instruction count is shifted into the transfer register to address the next instruction.

2-75. When the operation code specifies that data is to be transferred into the memory, the basic operations are reversed. Instead of transferring two syllables of data to the transfer register which serializes them into a continuous unit, a continuous unit of serial data is shifted into the transfer register which divides it into syllables. The syllables are then transferred to the memory in parallel. After the instruction is loaded into the operation code and address registers the data word to be stored begins to emerge from the accumulator register. Outputs from the operation code register and the operation decoders condition the transfer register to shift in step with the accumulator register and accept its output. As the data word enters the first position of the transfer register, a parity counter monitors the number of "1's" it contains.

2-76. Timing signals indicate to the memory control circuits that a data word is to be transferred to or from the memory. The operation code specifies that data is going to memory and the memory control circuits initiate a store cycle. The instruction word syllable control circuit selects syllable zero as the first syllable is to be transferred. The memory control circuits decode the contents of the address, data sector, and data module registers. Just before the last bits of the syllable enter the transfer register the memory control circuits produce read timing pulses which clear the addressed memory location.

2-77. Simultaneous with clearing the memory location, the last bit of the syllable enters the transfer register and the syllable is transferred to the memory buffer registers. The transfer register continues shifting and the second syllable of data starts to enter the transfer register. At the memory buffer registers, a "parity bit" is added to the syllable entering the memory. The parity bit is controlled by a parity count circuit so that the memory buffer register contains an odd number of "1's." The memory control circuits now produce store timing pulses and the first syllable of data enters the memory through the inhibit drivers. The second syllable of data enters the memory in the same manner as the first.

2-78. Operations which do not use the memory either shift the contents of the accumulator register or use the operand address as a constant for controlling the program. Shifting the contents of the accumulator register is accomplished by shortening or lengthening its circulation loop. Before the first bits of the accumulator contents are shifted, outputs from the operation code register and the operation decoders, along with

control bits from the address register, alter the recirculation path of the accumulator register to affect the shift. When the last bit has been shifted, timing signals restore the loop to normal to prevent shifting the contents of the instruction counter. The instruction counter is then incremented and shifted into the transfer register to address the next instruction.

2-79. Among the operations which do not use the memory are those which make logical decisions based on the contents of the accumulator register. As noted previously, logical decisions are made by altering the contents of the instruction counter if a specified condition exists in the accumulator register. If the condition exists, the operand address of the instruction replaces the existing contents of the instruction counter and the next instruction begins the new sequence. Logical decisions are implemented by continuously sampling the accumulator contents part way through the register for the conditions upon which decisions are based. Thus, when a logical decision is initiated, most of the accumulator contents have already been sampled and the Central Processor need not wait until the complete contents emerge from the register to make the decision. The contents of the instruction counter immediately follow the accumulator contents in the accumulator register. Consequently, when the last data bit has been sensed and the decision made, the contents of the instruction counter are still only part way through the accumulator register. If the condition is met, the accumulator register is broken just behind the last bit of the accumulator contents and the operand address is shifted into the accumulator register from the transfer register, replacing the existing instruction count.

NOTE

Since the memory is not being used, the transfer register is not needed to distribute data from it, and therefore is not cleared after the instruction is distributed to the program control element.

If the condition is not met, the accumulator register is not broken and the existing contents of the instruction counter are retained to address the next instruction.

2-80. External Control Element. Control over Central Processor start-stop and interrupt operations is provided by the external control element. The Central Processor cycles continuously under internal program control unless one of these operations is initiated.

2-81. The external control element stops the Central Processor operation as follows:

1. Until PTC DC power is completely sequenced on.
2. Momentarily when the RESET-HALT or RESET-MACHINE pushbutton is actuated.
3. Momentarily by every Data Display address compare when the MODE CONTROL switch is in the PROG CYCLE-REPEAT position.
4. When the Memory Loader/Data Display is in the ML mode unless a load or verify operation is in process.
5. When a Central Processor single step operation is initiated.

2-82. A Central Processor single step operation is commanded as follows:

1. By a Data Display address compare when the MODE CONTROL switch is in either the PROG CYCLE-ADR HOLD or SINGLE STEP position.
2. When the manual single step mode is selected under control of the MAN CST pushbutton.
3. By a CIO 114 command generated by the Central Processor.
4. By a memory parity error when the ERROR HOLD mode of operation is selected.
5. When a PTC single step command (ACNCST) is received from the LVDCME and the MODE CONTROL switch is not in either PROG CYCLE-ADR HOLD or SINGLE STEP positions.

2-83. After a single step operation is initiated Central Processor operation is normally not resumed until a restart signal is generated by actuating a PTC ADVANCE pushbutton or by a PTC advance command (ACGACISS) from the LVDCME. Central Processor operation is then resumed as follows:

1. Until another Data Display address compare occurs when the MODE CONTROL switch is in the PROG CYCLE-ADR HOLD position.
2. For one Central Processor cycle when: (1) the MODE CONTROL switch is in the PROG CYCLE-SINGLE STEP position; (2) in the ERROR HOLD mode if the parity error is not cleared; (3) when the MAN CST mode is selected; or (4) when the ACNCST signal is present.
3. Until another single step operation is initiated if the previous one was initiated by: (1) a CIO 114 command; or (2) a parity error in the ERROR HOLD mode and the parity error is now cleared.
4. Until another signal step operation is initiated: (1) upon exiting from the manual single step mode under control of the MAN CST pushbutton; or (2) when the ACNCST signal is dropped.

The single step command is removed for two Central Processor cycles when an interrupt command is received from the LVDAME. The single step command is also removed when the Memory Loader/Data Display is placed in the ML mode or when the RESET-HALT or MACHINE pushbutton is actuated.

2-84. A PTC single step (PTC CST) signal is sent to the LVDAME when a Central Processor single step operation is initiated by any method other than a ACNCST signal. The PTC CST signal is generated for approximately 62 microseconds when the single step operation was commanded by a CIO 114 command. The PTC CST signal is generated for the duration of the time the single step operation is maintained for any other condition.

2-85. The interrupt control circuit enables any one of 16 interrupts to break off normal sequencing of the program and direct it to process data of a higher priority. The interrupt control circuit allows the instruction in progress at the moment of the interruption to finish, then forces the selection of one of the residual addresses 400₈ through 417₈, if the INT B latch is reset. This latch is normally reset at the end of an interrupt processing routine. Residual addresses 400₈ through 417₈ contain "HOP" constants which direct the program to the start of an interrupt processing routine.

2-86. Interrupts 1 through 15 which force the selection of residual addresses 400g through 416g are generated by the LVDAME. When one of these interrupt signals is sent to the Central Processor it is stored by a latch in the external control element, but is not acted upon until its associated inhibit is removed. The removal of these inhibits is accomplished either under program control or manually with switches. When the INHIBIT CTRL pushbutton is not in the INHIBIT CTRL position the removal of the inhibits is under program control. If the INHIBIT CTRL position is selected an inhibit is removed when the corresponding pushbutton (I1/B1 through I15/B15) is actuated. Interrupt 16 which forces residual address 417g selection is generated under control of the I16 pushbutton.

2-87. WORD ORGANIZATION. The Central Processor uses a 28-bit word consisting of two 14-bit syllables. Each syllable includes 13 data bits and one parity bit (figure 2-6) and each syllable is stored separately in the memory. The parity bits are used only to check the accuracy of transfers to and from the memory which leaves a data word 26 bits in length.

2-88. The use of the data word is at the discretion of the programmer. Each of the 26 bits may be used as an indicator to show the presence or absence of some condition, or the word may be used as a binary number for arithmetic computations. Binary numbers are represented by a sign bit and 25 magnitude bits; negative numbers are shown in two's complement form.

2-89. In this section bit positions in the data word are designated SIGN and 1 through 25, proceeding toward the least significant digit (LSD). When used in this context, bits 1 through 25 are called "magnitude bits".

2-90. The Central Processor word is also used to store the instructions of the Central Processor program. Instructions are 13 bits in length with one instruction stored in each syllable of the Central Processor word. An instruction consists of a 4-bit operation code (OP1-OP4) and a 9-bit address (A9, A1-A8). Figure 2-7 shows how the instructions are placed in the Central Processor words.

2-91. TIMING ORGANIZATION. The basic unit of Central Processor timing is called the "Central Processor cycle." The duration of a Central Processor cycle is approximately 82 microseconds; this is the time required for the Central Processor to read, decode and operate its basic instructions. A Central Processor cycle is three phase times in duration.

2-92. The Central Processor cycle is separated into "instruction time" and "operation time". As the names imply, instruction time is the period in which an operation is read and decoded, and operation time is the period in which the operation commanded by the instruction is performed. Generally, the instruction time occurs during A time and the operation time occurs during B and C times.

BIT POSITION	SYLLABLE 1													SYLLABLE 0														
	1	2	3	4	5	6	7	8	9	10	11	12	13	PAR	1	2	3	4	5	6	7	8	9	10	11	12	13	PAR
BIT DESIGNATION	S	1	2	3	4	5	6	7	8	9	10	11	12		13	14	15	16	17	18	19	20	21	22	23	24	25	

Figure 2-6. Data Word Layout

BIT POSITION	SYLLABLE 0														SYLLABLE 1													
	1	2	3	4	5	6	7	8	9	10	11	12	13	PAR	1	2	3	4	5	6	7	8	9	10	11	12	13	PAR
DESIGNATION	A	A	A	A	A	A	A	A	A	O	O	O	O		A	A	A	A	A	A	A	A	A	O	O	O	O	
	8	7	6	5	4	3	2	1	9	P	P	P	P		8	7	6	5	4	3	2	1	9	P	P	P	P	
USE	OPERAND ADDRESS									OPERATION CODE					OPERAND ADDRESS									OPERATION CODE				

Figure 2-7. Instruction Word Layout

2-93. Notice the correlation between the organization of timing and word layout. The Central Processor cycle is defined by three phase times and involves three syllables of information: one syllable for an instruction and two syllables of data for an operand. The correlation also extends downward one step. A syllable consists of 14 bits (13 data, 1 parity) and each phase time is divided into 14 equal segments called "bits times." A bit time is the time each bit of data is stored in one position of a serial storage device before moving on to the next.

2-94. INSTRUCTION ORGANIZATION. The Central Processor uses a complement of 16 single address instructions which are composed of a 4-bit operation code and a 9-bit operand address. The 4-bit operation code can select one of 15 different instructions to be executed, this range is extended to 16 by grouping two instructions under one operation code, then using bit A8 of the address to discriminate between them. Bit A8 serves no other function for the instructions which are grouped. Figure 2-8 is a map of the operation codes showing the names of the instructions assigned to each code. Figure 2-9 shows how addition of each bit of the operation code narrows the field of selection by de-selecting half the remaining area of the map. A list of the 16 instructions available is given in figure 2-10 with the operation code and a brief description of each. Figure 2-11 lists the CIO codes used by the PTC.

2-95. The 9-bit operand address, figure 2-12 permits selection of memory addresses for use as operands or data storage locations. Address bits A1 through A8 select one of the addresses within a sector. Bit A9 determines whether the address will be in a sector previously selected by the program or in a special sector called "residual memory." Consequently, bit A9 is called the residual bit; residual memory is selected when A9 is a "1."

2-96. Instructions which do not require that data be read from the memory frequently use the operand address for special purposes. These special purposes are pointed out in the List of Instructions, figure 2-10, where they occur. For example the shift instructions (SHF) always manipulates the contents of the accumulator and thus requires no operand address; this frees the operand address for use as shift control.

2-97. MEMORY AND MEMORY CONTROL ELEMENT LOGIC CIRCUITS.

2-98. The Memory Element, figure 2-13 provides 4,096 locations of primary storage in each of two memory modules, memory module 0 and memory module 1. Each memory module operates independently on command from the memory control element. The memory modules are each divided into 20 octal sectors, sectors 0 through 17. Sector 17 of only memory module 0 is designated as the "Residual" sector. Each sector contains 400₈ locations or addresses and are designated 0₈ through 377₈ except residual locations. These are designated 400₈ through 777₈. Sector selection is identical for each module, and address selection is the same for every sector except the residual sector.

Address, sector, and module selections are controlled separately in the memory control element. As far as "addressing" in the usual sense is concerned, the memory control element provides only sector and individual location addressing signals. These signals are applied to both modules in the memory element and select the same address in each module. The memory control element then commands only the selected module to operate.

2-99. Toroidal ferrite cores are the storage medium in which coincident current addressing and destructive readout techniques are utilized. A restore cycle follows every read operation to preserve the contents of the memory. Each memory location stores a 28-bit word which is divided into two 14-bit syllables. The memory element transfers one syllable at a time which necessitates four operations (two read cycles and two restore cycles) to transfer a complete word. The Central Processor has random access to stored information within preselected sectors.

2-100. CORE MEMORY FUNDAMENTALS. Figure 2-14 illustrates the properties of a ferrite core. As shown in the figure, the core can be magnetized in either of two directions. By establishing that a core contains a "1" when magnetized in one direction and a "0" when magnetized in the opposite direction, the core can be used to store one "bit" of a binary number. The core is magnetized by passing a d-c current of $I/2$ through the X and Y drive lines in coincidence.

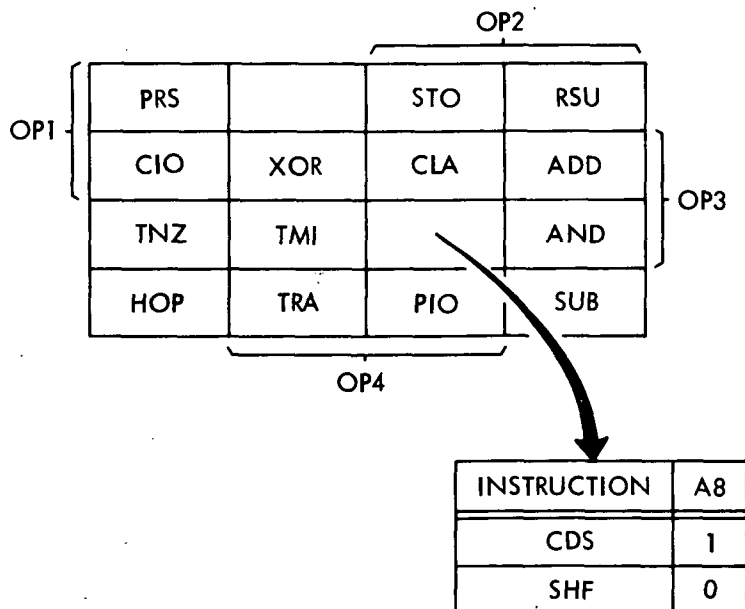


Figure 2-8. Operation Code Map

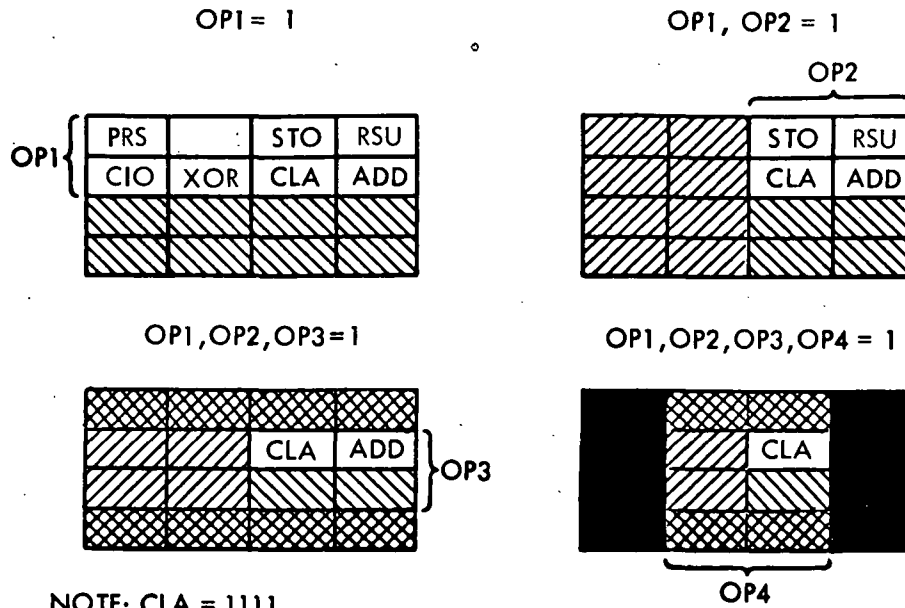


Figure 2-9. Selecting An Instruction

NOTE

I is the current necessary to drive the core into magnetic saturation. The directions of the currents in both the X and Y drive lines must be additive to operate the core.

The direction of magnetic flux about the core can be reversed by passing the same currents through the drive lines in the opposite direction. Reversing a core in this manner is called "switching" it. A sense winding, represented by S in figure 2-14, also passes through the core and lies within its magnetic field. When a core is switched, the resulting field collapses and then expands causing a pulse of voltage to be induced in the sense winding. Thus, if a core containing a "1" is switched to a "0", the resulting voltage pulse in the sense winding can be amplified and used to set a latch, indicating the core contained a "1". If the core already contained a "0", it would not switch and no voltage pulse would appear in the sense winding to set the latch.

2-101. The following method is used for reading information from a core memory. It is called "destructive readout" because after the core is read, it no longer contains the "1" which was sensed from it. The latch into which the "1" was read is a buffer between the core and the circuits which use the stored information. The "buffer latch" stores the "1" until it can be transferred into the Central Processor and until the core can be switched back to its original state. The process of driving a core to a "0" and sensing whether or not it produced an output is called "read cycle". Switching the core back to its original state is called a "store cycle".

Instruction	Operation Code				Description																																																																								
	4	3	2	1																																																																									
HOP	0	0	0	0	Transfers program to memory location specified by HOP constant. Operand address specified memory location of HOP constant used to load the registers shown in HOP constant format (below). Full HOP constant MUST be specified each time. First instruction following HOP comes from new location.																																																																								
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>S</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td> </tr> <tr> <td rowspan="2">I M</td> <td colspan="4">Data Sector</td> <td></td> <td>D M</td> <td></td> <td colspan="11">Instruction Address</td> <td>S Y L</td> <td colspan="4">Instruction Sector</td> </tr> <tr> <td></td><td>4</td><td>3</td><td>2</td><td>1</td> <td></td> <td></td> <td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td> <td></td> <td>4</td><td>3</td><td>2</td><td>1</td> <td></td><td></td> </tr> </table>						S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	I M	Data Sector					D M		Instruction Address											S Y L	Instruction Sector					4	3	2	1			A8	A7	A6	A5	A4	A3	A2	A1		4	3	2	1		
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25																																																				
I M	Data Sector					D M		Instruction Address											S Y L	Instruction Sector																																																									
		4	3	2	1			A8	A7	A6	A5	A4	A3	A2	A1		4	3	2	1																																																									
PRS	0	0	0	1	<p>Print store. Initiates a printer operation. The printer operation performed is specified by the operand address.</p> <table style="margin-left: 40px;"> <thead> <tr> <th style="text-align: left;"><u>Address</u></th> <th style="text-align: left;"><u>Operation</u></th> </tr> </thead> <tbody> <tr> <td>000₈ to 773₈</td> <td>Data in memory address specified is transferred to the printer.</td> </tr> <tr> <td>774₈</td> <td>A group markword mark is sent to the printer.</td> </tr> <tr> <td>775₈</td> <td>Data in the accumulator is transferred to the printer.</td> </tr> </tbody> </table>	<u>Address</u>	<u>Operation</u>	000 ₈ to 773 ₈	Data in memory address specified is transferred to the printer.	774 ₈	A group markword mark is sent to the printer.	775 ₈	Data in the accumulator is transferred to the printer.																																																																
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SUB	0	0	1	0	Subtracts contents of memory location specified in operand address from contents of accumulator. Places remainder in accumulator.																																																																								
TNZ	0	1	0	0	Conditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select <u>if accumulator contents are not zero</u> . Next instruction comes from new syllable and address. If accumulator is zero, perform next instruction in sequence.																																																																								
CIO	0	1	0	1	Controls the input, output operations of the Central Processor. The operand address bits specify the operation to be performed (see figure 2-11 for CIO codes used by PTC).																																																																								
AND	0	1	1	0	AND's contents of memory location specified in operand address with contents of accumulator. Result is placed in accumulator.																																																																								

Figure 2-10. List of Instructions (Sheet 1 of 3)

Instruction	Operation Code				Description
	4	3	2	1	
ADD	0	1	1	1	Adds contents of memory location specified in operand address to contents of accumulator. Sum is placed in accumulator.
TRA	1	0	0	0	Unconditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select. Next instruction comes from new syllable and address.
XOR	1	0	0	1	Exclusive - OR contents of memory location specified in operand address with contents of accumulator, bit-for-bit. When accumulator bit and bit from memory are different a "1" is placed in the corresponding bit of the accumulator; if accumulator bit and memory bit are alike, a "0" is placed in the accumulator.
PIO	1	0	1	0	Process input or output. Operand address specifies input or output and gives address of data source and destination. These codes are the same as the computer codes.
STO	1	0	1	1	Contents of accumulator is stored in memory location specified by operand address. Contents of accumulator is unchanged. A STO instruction with operand address 776 or 777 causes contents of HOP save register to be stored in memory location 776 or 777 as specified. These addresses are used for HOP save feature.
TMI	1	1	0	0	Conditional transfer. Transfer operand address (A1-A8) to instruction counter and A9 to syllable select if accumulator sign is minus. Next instruction comes from new syllable and address. If accumulator sign is plus, perform next instruction in sequence.
RSU	0	0	1	1	Reverse subtract. Contents of accumulator are subtracted from contents of memory location specified by operand address. Remainder is placed in accumulator.

Figure 2-10. List of Instructions (Sheet 2)

Instruction	Operation Code				Description																																																	
	4	3	2	1																																																		
SHF	1	1	1	0	<p>Contents of accumulator are shifted MSD or LSD a maximum of 6 bit positions as specified by operand address. On a MSD shift the vacated bit positions will become "0's", on a LSD shift the vacated bit positions will be assigned the value of the SIGN bit. A MSD shift occurs if A7 equals a "0" and a LSD shift occurs if A7 equals a "1". The number of bit positions shifted is determined by decoding address bits A1 through A6.</p> <table border="1"> <thead> <tr> <th>Shift</th> <th>A1</th> <th>A2</th> <th>A3</th> <th>A4</th> <th>A5</th> <th>A6</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>"1"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> </tr> <tr> <td>2</td> <td>"0"</td> <td>"1"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> </tr> <tr> <td>3</td> <td>"0"</td> <td>"0"</td> <td>"1"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> </tr> <tr> <td>4</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"1"</td> <td>"0"</td> <td>"0"</td> </tr> <tr> <td>5</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"1"</td> <td>"0"</td> </tr> <tr> <td>6</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"0"</td> <td>"1"</td> </tr> </tbody> </table>	Shift	A1	A2	A3	A4	A5	A6	1	"1"	"0"	"0"	"0"	"0"	"0"	2	"0"	"1"	"0"	"0"	"0"	"0"	3	"0"	"0"	"1"	"0"	"0"	"0"	4	"0"	"0"	"0"	"1"	"0"	"0"	5	"0"	"0"	"0"	"0"	"1"	"0"	6	"0"	"0"	"0"	"0"	"0"	"1"
						Shift	A1	A2	A3	A4	A5	A6																																										
1	"1"	"0"	"0"	"0"	"0"	"0"																																																
2	"0"	"1"	"0"	"0"	"0"	"0"																																																
3	"0"	"0"	"1"	"0"	"0"	"0"																																																
4	"0"	"0"	"0"	"1"	"0"	"0"																																																
5	"0"	"0"	"0"	"0"	"1"	"0"																																																
6	"0"	"0"	"0"	"0"	"0"	"1"																																																
CDS	1	1	1	0	<p>Change data sector. Operand address is used as a constant to load registers indicated below.</p> <table border="1"> <thead> <tr> <th>A</th> <th>A</th> <th>A</th> <th>A</th> <th>A</th> <th>A</th> <th>A</th> <th>A</th> <th>A</th> </tr> <tr> <th>9</th> <th>8</th> <th>7</th> <th>6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>D</td> <td colspan="4">Data Sector</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td>M</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> </tr> </tbody> </table>	A	A	A	A	A	A	A	A	A	9	8	7	6	5	4	3	2	1	0	1	0	0	D	Data Sector								M	4	3	2	1													
A	A	A	A	A	A	A	A	A																																														
9	8	7	6	5	4	3	2	1																																														
0	1	0	0	D	Data Sector																																																	
				M	4	3	2	1																																														
CLA	1	1	1	1	<p>Contents of memory location specified by the operand address are transferred to cleared accumulator.</p>																																																	

Figure 2-10. List of Instructions (Sheet 3)

CIO Operand Address	Operation
000	Enables the interrupt inhibit register latches to be set under control of accumulator data bits 11 through 25 (Data bit 11 sets interrupt inhibit latch 15, etc.)
004	Enables the interrupt inhibit register latches to be reset under control of accumulator data bits 11 through 25 (Data bit 25 resets interrupt inhibit latch 1, etc.)
010	Reset interrupt 1 latch
014	Reset interrupt 2 latch
020	Reset interrupt 3 latch
024	Reset interrupt 4 latch
030	Reset interrupt 5 latch
034	Reset interrupt 6 latch
040	Reset interrupt 7 latch
044	Reset interrupt 8 latch
050	Reset interrupt 9 latch
054	Reset interrupt 10 latch
060	Reset interrupt 11 latch
064	Reset interrupt 12 latch
070	Reset interrupt 13 latch
074	Reset interrupt 14 latch
100	Reset interrupt 15 latch
104	Reset interrupt 16 latch
110	Resets the main interrupt latch.
114	Generates a PTC single step command.
120	Generates a type alpha numeric command. Positions SIGN and 1 through 5, respectively, of the accumulator data word contain the "BA8421" code.

Figure 2-11. PTC Internal CIO Operations (Sheet 1 of 3)

CIO Operand Address	Operation														
124	Generates a type decimal command. Positions SIGN, 1, 2, and 3, respectively, of the accumulator data word contain the "8421" code.														
130	Generates a type octal command. Positions SIGN, 1, and 2, respectively, of the accumulator data word contain the "421" code.														
134	Generates a typewriter control command. Positions SIGN and 1 through 5 of the accumulator data word are decoded to perform one of six operations.														
	<table border="0"> <thead> <tr> <th><u>Data Bit</u></th> <th><u>Operation</u></th> </tr> </thead> <tbody> <tr> <td>SIGN</td> <td>Space</td> </tr> <tr> <td>1</td> <td>Black Ribbon</td> </tr> <tr> <td>2</td> <td>Red Ribbon</td> </tr> <tr> <td>3</td> <td>Index</td> </tr> <tr> <td>4</td> <td>Return</td> </tr> <tr> <td>5</td> <td>Tap</td> </tr> </tbody> </table>	<u>Data Bit</u>	<u>Operation</u>	SIGN	Space	1	Black Ribbon	2	Red Ribbon	3	Index	4	Return	5	Tap
<u>Data Bit</u>	<u>Operation</u>														
SIGN	Space														
1	Black Ribbon														
2	Red Ribbon														
3	Index														
4	Return														
5	Tap														
140	Generates an X plot command.														
144	Generates a Y plot command														
150	Generates a Z plot command.														
154	Stores the configuration of the interrupt latches in positions SIGN and 1 through 15 of the accumulator data word. (Data bit 1 stores interrupt latch 1 configuration, etc.)														
160	Generates a printer carriage control command. Positions SIGN and 1 through 5, respectively, of the accumulator data word contain the "BA8421" code.														
164	Generates a print octal command.														
170	Generates a print BCD command.														
204	Enables the program control display register to be loaded. Positions 21 through 25 of the accumulator data word are loaded into positions P40, P20, P10, P4, P2 and P1, respectively, of the program control display register.														
210	Enables one of six output discrettes to be generated. Discrettes 1 through 6, respectively, are controlled by positions 25, 24, 23, 22, 21, and 20 of the accumulator data word.														
214	Transfers the PROG REG A data word into the accumulator.														
220	Transfers the PROG REG B data word into the accumulator.														

Figure 2-11. PTC Internal CIO Operations (Sheet 2)

A8	A7	A6	A5	A4	A3	A2	A1	A9
LOCATION IN SECTOR								R

Figure 2-12. Operand Address Layout

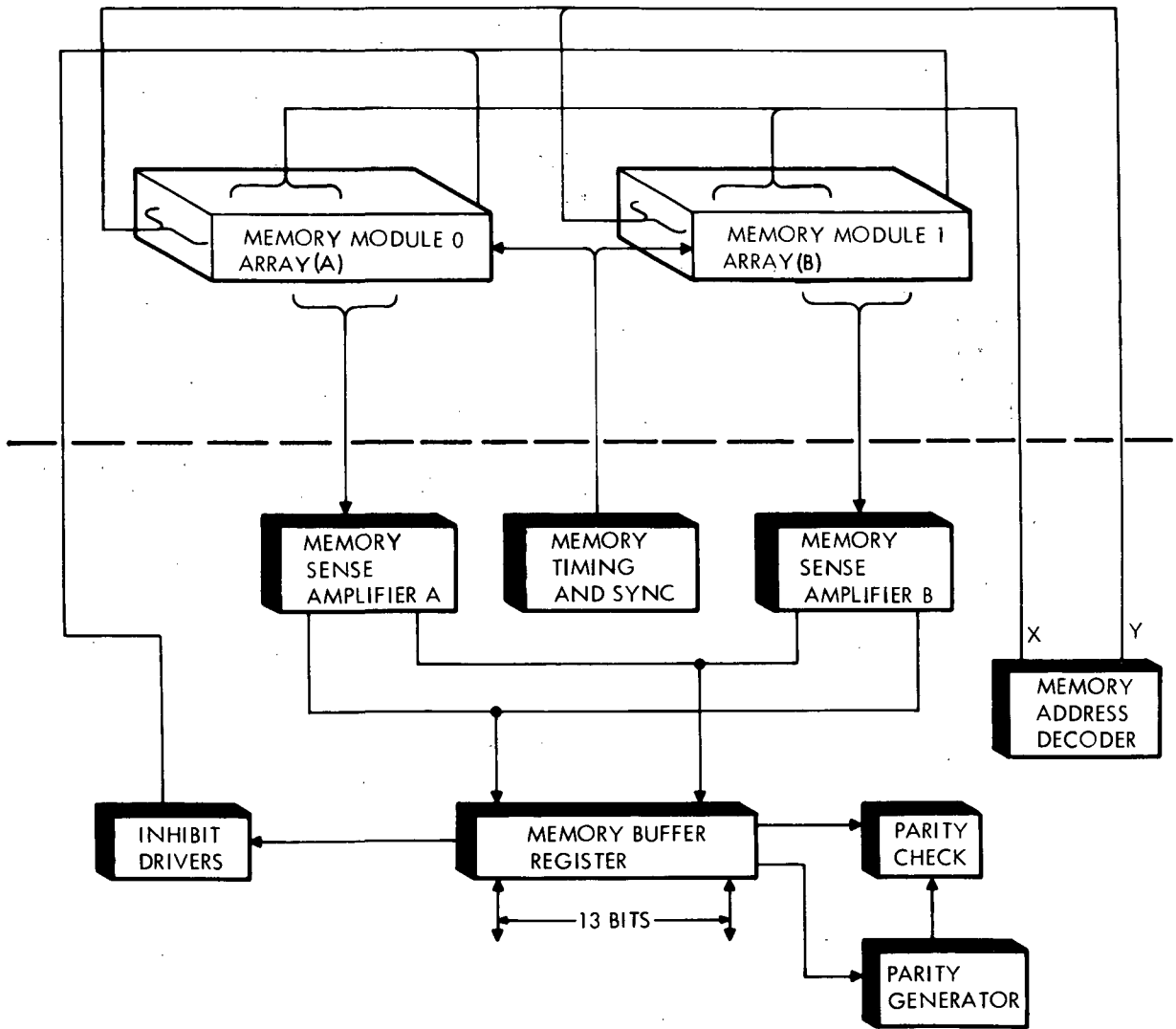


Figure 2-13. Memory Element Block Diagram

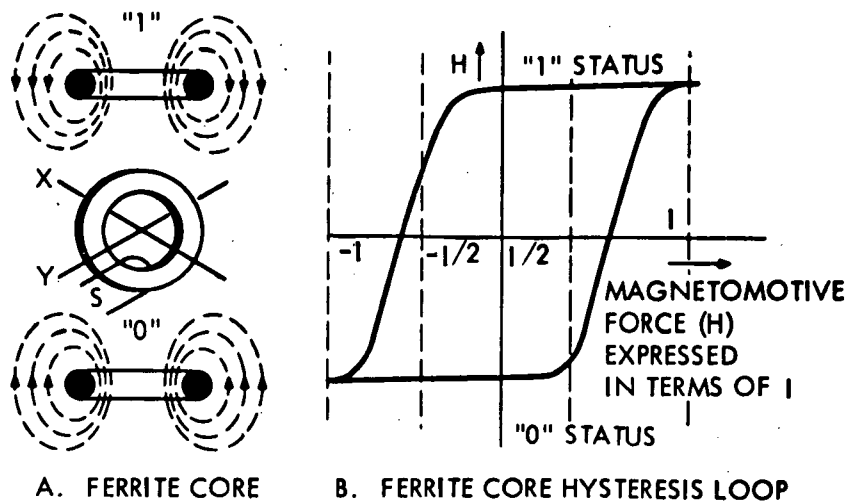


Figure 2-14. Ferrite Core Characteristics

2-102. The preceding paragraphs dealt with the operation of a single core. However, a single core can store only one bit of information while a core memory must store many bits and select each bit on command. This ability can be achieved by arranging cores in rows and columns as shown in figure 2-15. An X drive line passes through all the cores in two rows and a Y drive line through all the cores in two columns. The cores are held in place by the wires passing through them; the wires are fastened to a frame and the unit is called a plane. The cores are positioned on the drive lines in a pattern which puts the magnetic fields of adjacent cores 90 degrees apart; this eliminates interference between cores. The sense windings run parallel to the X drive lines and pass through all the cores in a segment of a plane. There are four segments to each plane, and the sense windings are interconnected as shown in figure 2-16. The sense winding is wound in a pattern which results in cancellation of "half-select" noise (discussed later).

2-103. The arrangement of cores into planes facilitates storing and addressing many bits of information, but still falls short of practicality, because only two bits can be addressed per plane. The Central Processor operates using "words" which comprise a number of bits, thus the memory must be expanded to store a complete word in each location. The expansion is accomplished by providing a separate plane for every two bits in each syllable of the word. (See figure 2-17.) The planes are stacked one above the other to form an "array" which accommodates a word of 13 bits and parity in each syllable. (See figure 2-18.)

2-104. Each plane has four separate sense windings: segments 1 and 2 for the even bits in both Syllables 0 and 1 and segments 2 and 1 for the odd bits in both syllables 0 and 1. (See figure 2-16.) Memory address register bit 5 controls sense amplifiers for two segments at a time while the buffer latches allow individual bits to be sensed. The problem, however, is encountered in attempting to restore the information back into memory. As presented up to this point, energizing drive lines switch all of the cores in the addressed location to the same state. There is (thus far) no provision for storing numbers which contain both "1's" and "0's". Therefore, another winding called an "inhibit" winding is wound through each quadrant of every plane to allow bits to be stored individually. The inhibit windings run parallel to the Y drive lines and carry the same current as the drive lines but operate only during the store cycles. During a store cycle, the drive lines attempt to switch every core in the addressed locations to "1's".

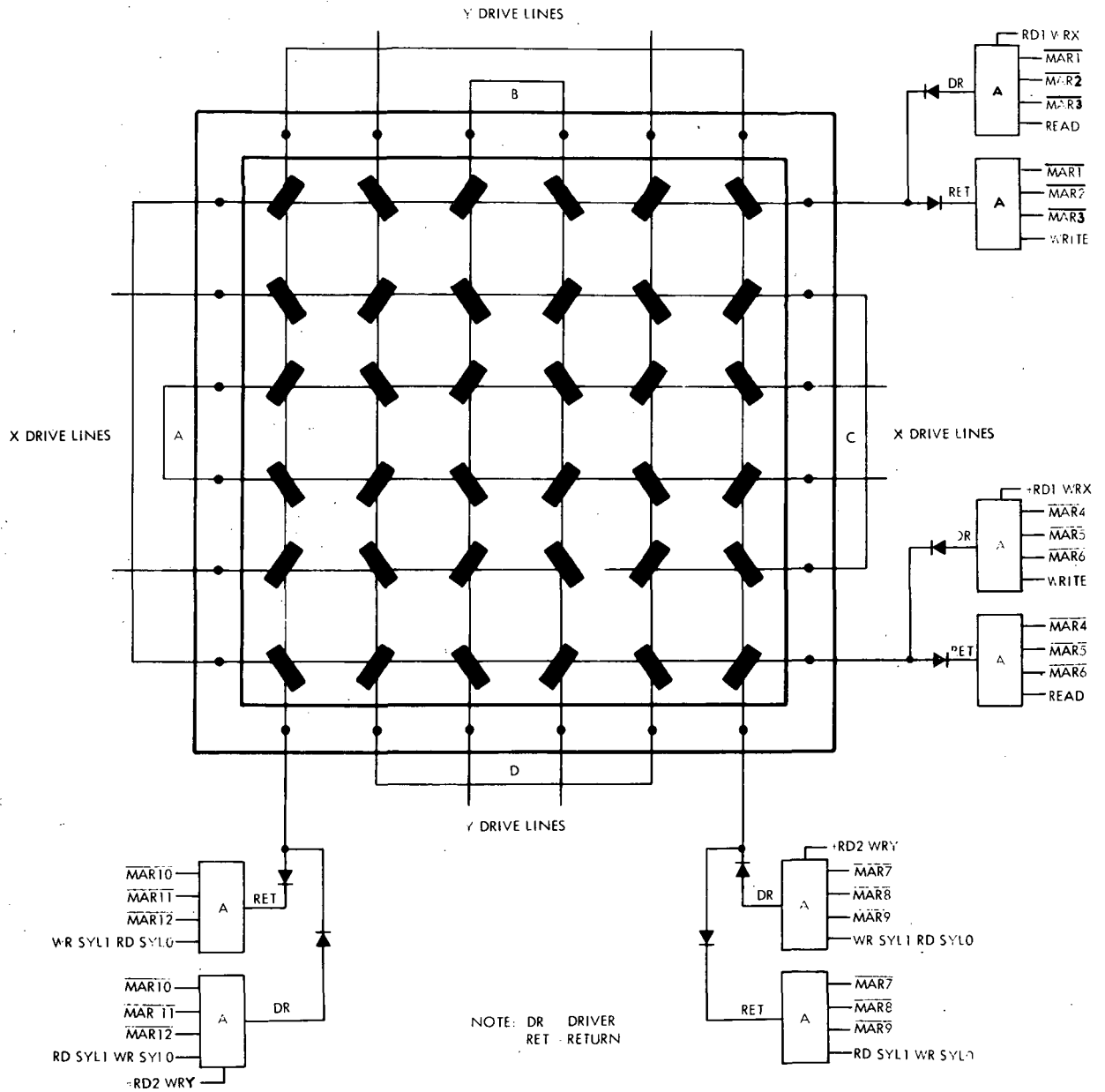


Figure 2-15. 6x6 Core Plane

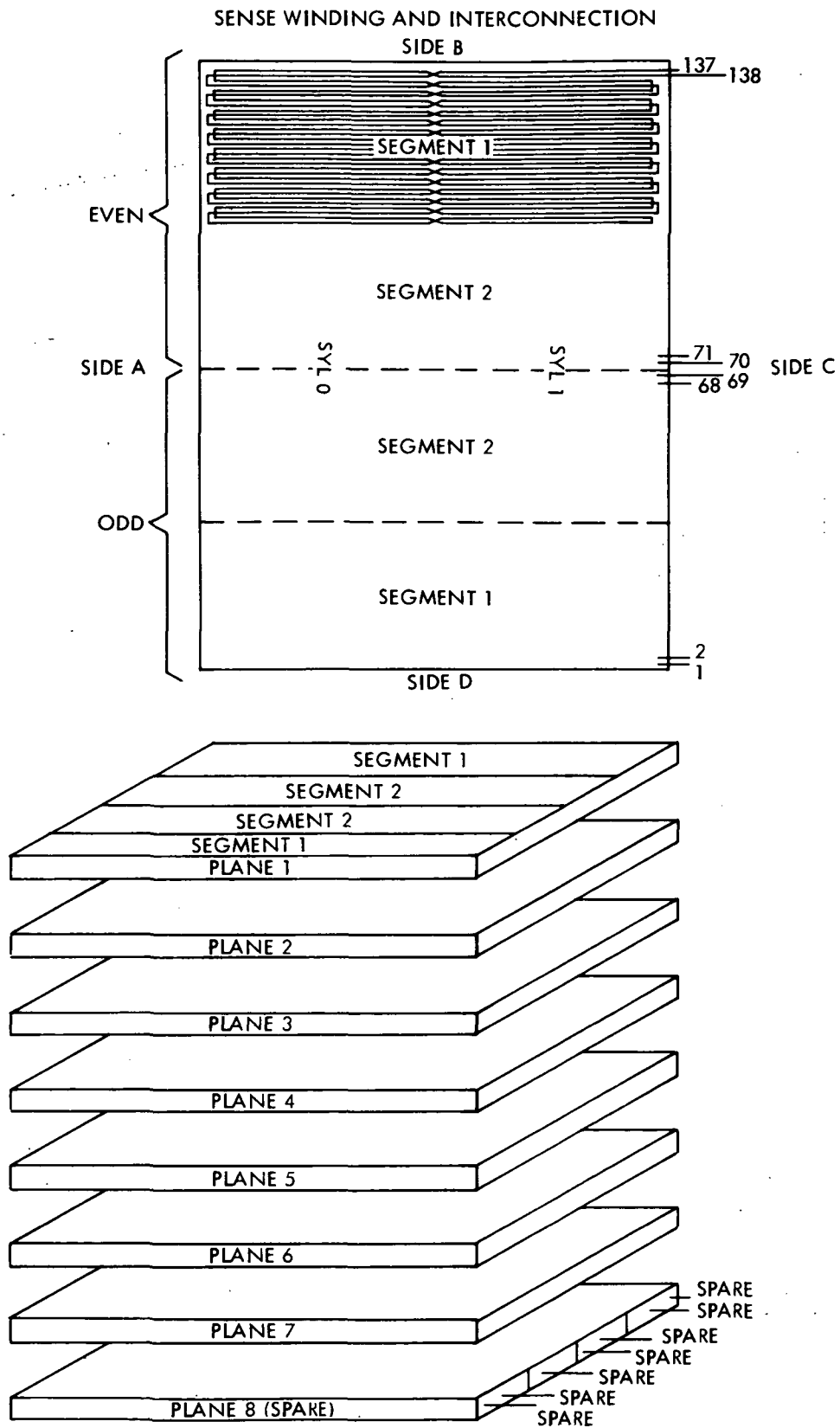


Figure 2-16. Memory Sense Winding and Interconnection Block Diagram

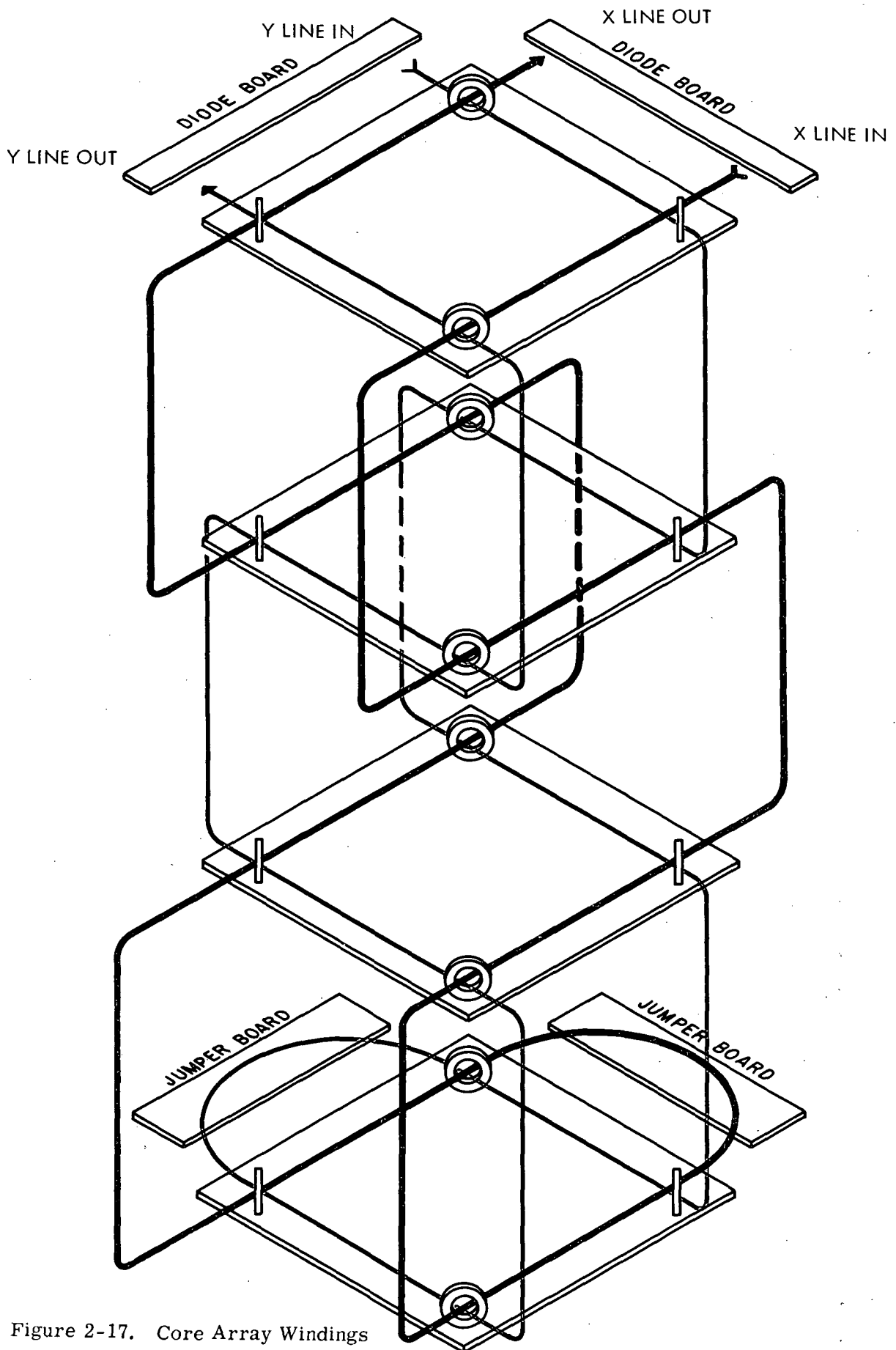


Figure 2-17. Core Array Windings

However, any buffer storage latches containing "0's" energize the inhibit windings in the quadrant of the bit position selected. (See figure 2-19.) Inhibit current opposes the current in the Y drive line and cancels its effect. Thus the addressed cores in the inhibit quadrants feel only the half selected current of the X drive line and do not switch. Since the cores in the addressed locations were all switched to "0's" when they were read, any inhibit cores will simply remain in the "0" state.

2-105. Associated with the array are a number of special circuits which are required to operate it. Included in these circuits are the sense amplifiers, some special timing circuits, and the circuits which provide power to the drive lines and inhibit windings. These circuits vary widely from system to system and therefore are not included in the description of Core Memory Fundamentals. Detailed operation of the circuits used in this system are described in subsequent paragraphs.

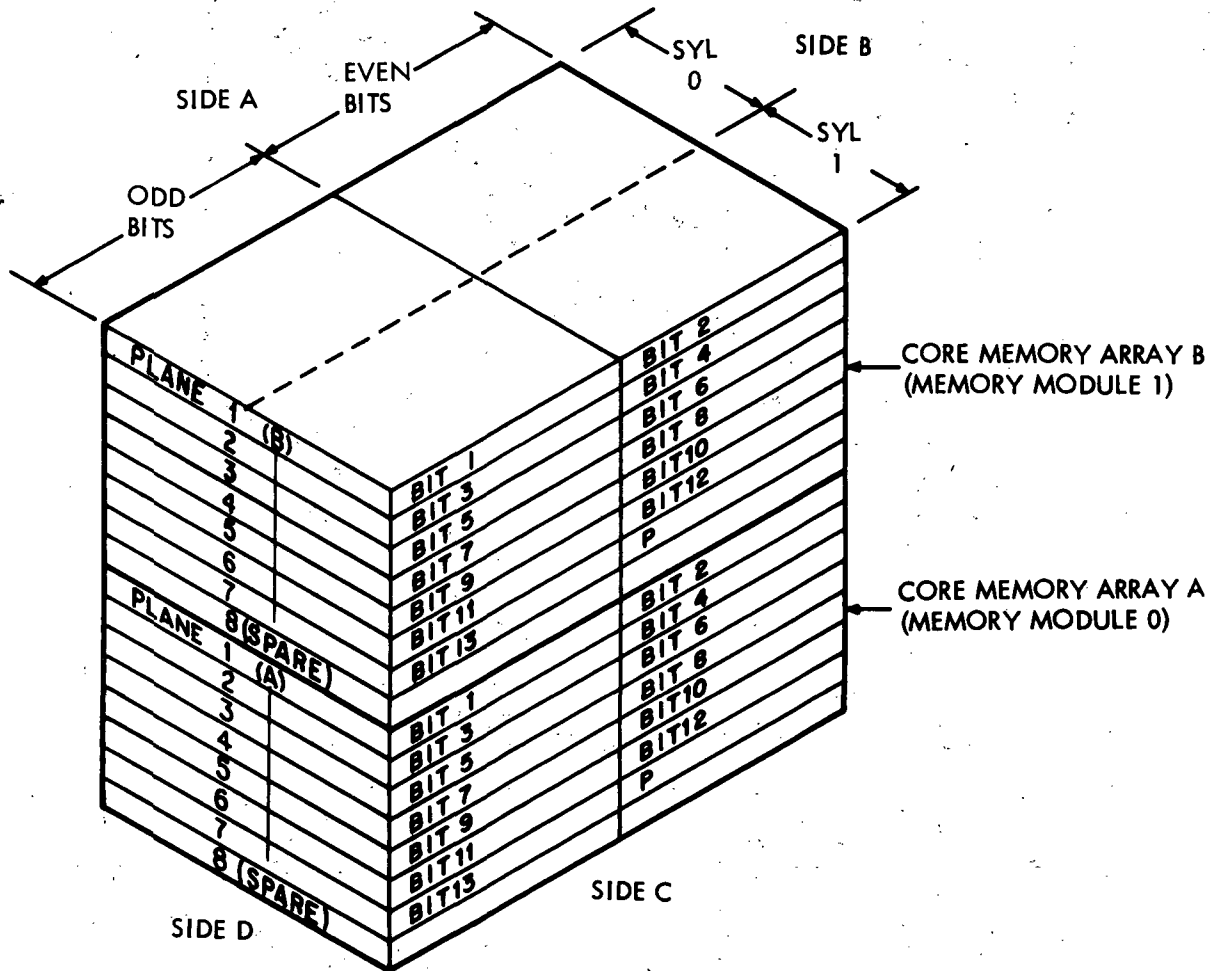


Figure 2-18. Physical Layout of PTC Memory Array

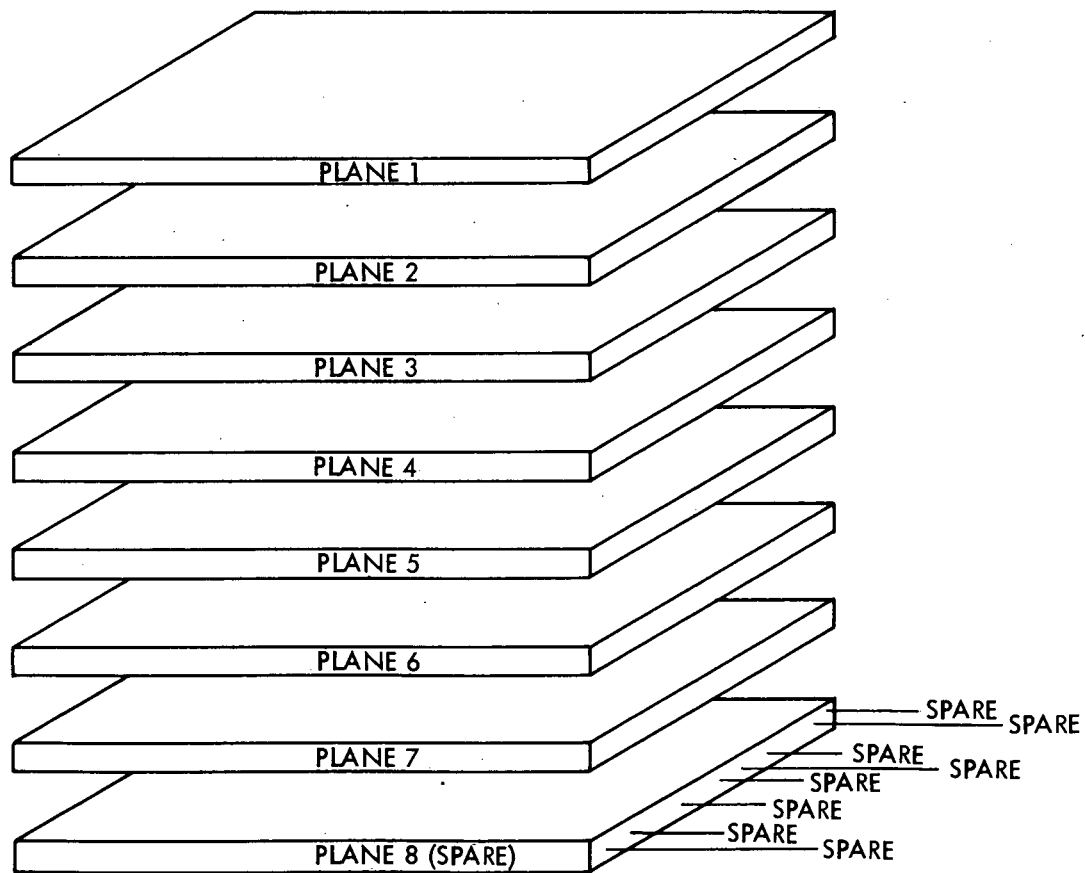
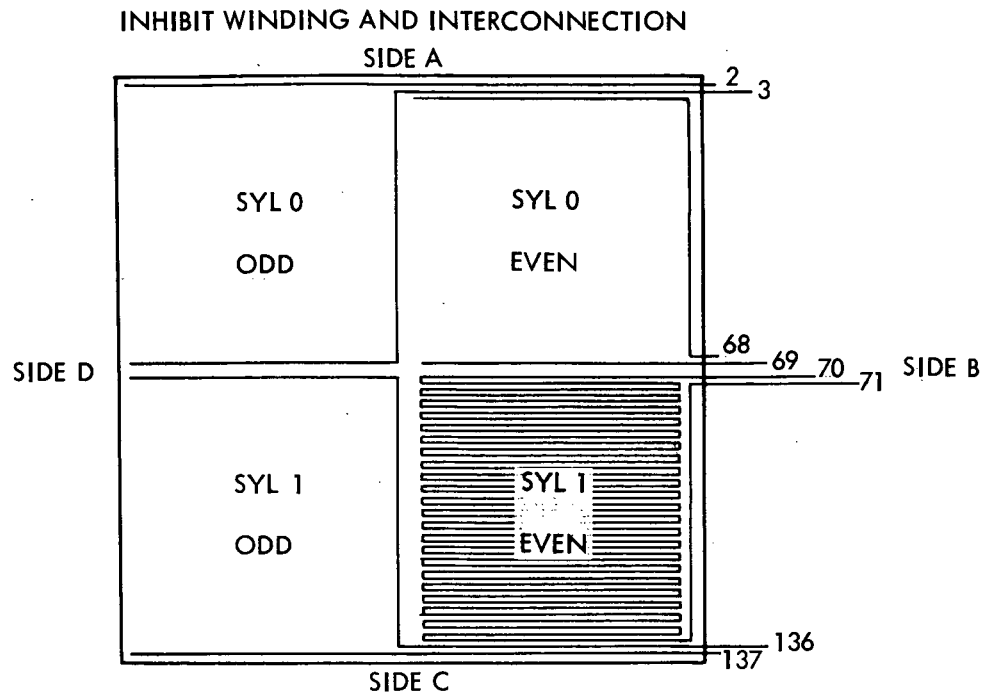


Figure 2-19. Memory Inhibit Winding and Interconnection Block Diagram

2-106. The location of cores can be defined by the X and Y drive lines which pass through them. The circuits which operate the plane are controlled so that two X and two Y drive lines carry current through four cores at any given time. The two selected cores at the intersection of the X and Y drive lines in each plane receive the coincident current necessary to switch them. An odd and an even bit can therefore be selected in either syllable, in all core planes. The two non-selected cores that have both X and Y lines passing through them have equal and opposite currents which cancel each other. This method of selecting memory locations is called "coincident-current addressing." When a memory location is selected by coincident current addressing, the selected cores along each drive line receive the full current to select them. However, there are a number of other cores along each of the selected lines which receive one-half the current of the selected cores; these cores are called "half-selects". Although half-select cores remain virtually at magnetic saturation, those containing "1's" will transmit small voltage spikes (called half select noise) into the sense winding. The sense winding is wired so that half-select noise from one core cancels that from another. Thus, half-selected noise cannot mask a "0" in the selected core.

2-107. MEMORY MODULES. The memory element is composed of two integral asynchronous memory modules, which operate under control of the memory control element. The modules are termed "integral" because each module is a complete memory in itself. Included in each module are a core array and all the circuits required to transfer information to and from it. Asynchronous refers to the fact that the timing signals within a module are not in synchronism with the other module in the Central Processor. When information is to be transferred to or from the memory element, the Central Processor delivers a "sync" impulse to the selected module, waits a reasonable time for the module to perform the transfer, and then continues assuming that the transfer is complete. During the memory cycle, the memory control element provides signals to the memory element which control addressing and determine the direction of transfer.

2-108. Figure 2-20 is a block diagram of a memory module showing all the circuits it comprises. The memory drive controls (upper left) receive the sync impulse from the Central Processor and convert it to a series of read or store timing pulses. The timing pulses turn the Memory Address Drivers and Inhibit Drivers on and off and strobe the Sense lines in the array. Addressing signals from the memory control element select one X and two Y drive lines by conditioning an X driver and return and a Y driver and return. When the timing pulses occur, the conditioned memory address drivers pass coincident current pulses through the selected drive lines to switch the cores in the addressed location. Diode matrices provide isolation between drive lines and return lines. A temperature controlled current regulator adjusts the memory address driver current to produce the optimum current output for the prevailing temperature in the array. A temperature sensing element near the array develops the inputs for the temperature controlled current regulator.

2-109. Static control signals from the memory control element determine whether information will be read or stored by conditioning the memory drive controls to produce the appropriate series of timing pulses. If information is to be read, a series of read pulses is generated causing the memory address drivers to switch all the addressed cores to "0's". Read timing includes a strobe pulse, for the sense amplifiers, which is delayed from the drive current to allow for the inductive reactance of the windings through the array. If the purpose of the read cycle is to clear the addressed location so that new information may be stored in it, the strobe pulse is inhibited and the sense amplifiers produce no outputs.

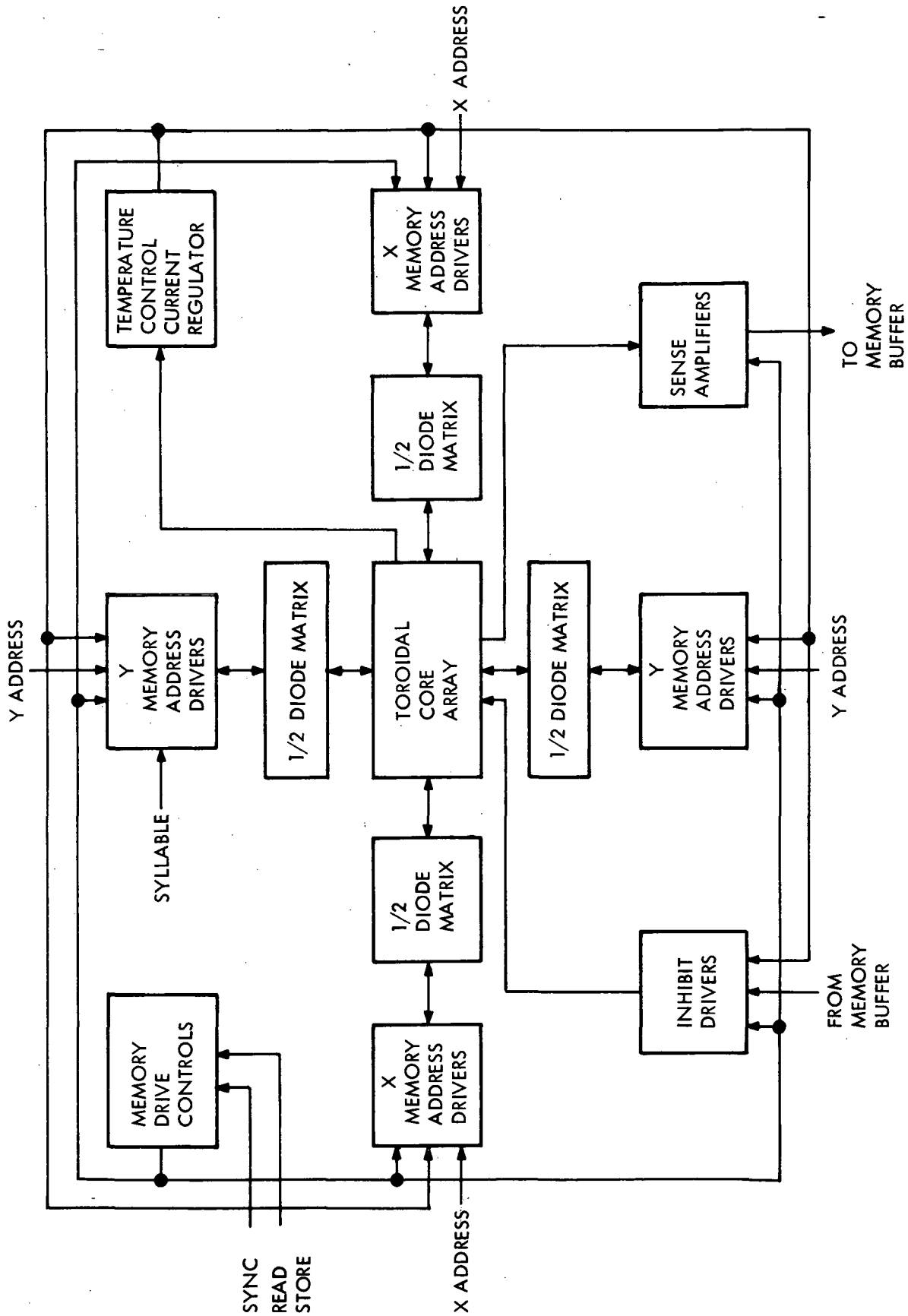


Figure 2-20. Memory Module Block Diagram

2-110. If a store cycle is required, the timing pulses produced by the memory clock drivers reverse the polarity of the memory address driver outputs. The memory address drivers then attempt to drive all the addressed cores to "1's"; however, the store pulses are also routed to the inhibit drivers. Any inhibit drivers conditioned by "0's" in the memory buffer register will produce an output opposing the Y drive current. Inhibited cores feel only the X half-select current and, therefore, remain in the "0" state.

2-111. Core Array. A memory module is built around a torodial core array with a capacity for storing 4,096 28-bit Central Processor words. The core array, figure 2-17, is a stack of 16 memory planes, 128 cores wide and 128 cores long. Each plane stores two bits of information, an odd bit and an even bit, for every location of the two syllables into which the Central Processor is divided. The array is electrically split into two 8 plane modules. The modules are stacked one on the other and are physically and electrically independent of each other. Each array is described as being divided into syllables, and the two halves of the array are called "Syllable 0" and "Syllable 1". Each syllable contains 4,096 14-bit locations which are defined by the X and Y drive lines passing through them.

The Y drive lines are connected between sides B and D of the planes and are numbered as shown on figure 2-21. The X drive lines are connected between sides A and C of the planes and are assigned specific numbers also. The Y drive lines as decoded determine syllable usage. Thus syllable selection is a part of the memory addressing scheme. Also wound through each plane are four sense windings and four inhibit windings. The sense windings run parallel to the X drive lines, and the inhibit windings run parallel to the Y drive lines.

2-112. Short pins protruding from all sides of the planes facilitate connections to the planes and interconnections between planes. The sense and inhibit windings are connected to pins, four pairs per plane, as shown on figures 2-16 and 2-19. Drive lines enter plane 1 from diode boards, and are then jumpered to plane 2. After passing through plane 2, they are jumpered to plane 3. In a similar fashion they weave their way down through plane 7. The lines exit plane 7, circle around via jumper boards, re-enter the plane on the same side, and weave their way up through the 7 planes. The drive lines exit plane 1 and are connected to the diode board.

2-113. To reduce congestion, adjacent drive lines enter from opposite directions. Thus drive currents in adjacent lines flow in opposite directions. (See figure 2-21.) The four pairs of inhibit windings then enter the planes at one side; each pair weaves it way back and forth through one quadrant of the plane. (See figure 2-19.) Consequently inhibit current reverses direction with each pass across a quadrant of the plane so as to always oppose Y drive current in that quadrant during store cycles. Drive current for both X and Y is provided by the memory address drivers; the direction of the drive current is controlled by the memory drive controls.

2-114. Memory Control. (See figure 10-28, sheet 25, and timing charts, figures 2-22, 2-23, 2-24 and 2-25.) Memory has the capability of performing four operations: reading syllable 0, reading syllable 1, writing syllable 0 and writing syllable 1. The read-write operations begin with the memory control circuits. A latch output level which starts all read-write operations is the SINK level. The SINK latch is set when initiating a read-memory during instruction time (A-13-Y time) or a read-memory during operation time (B-2-Y time or C-2-Y time), providing the read level (-Y RD) is present. The read level is present during memory operate (MOP) time when the operation decoded is not a store operation. The SINK latch is set when (1) initiating a write-into memory for storing into syllable 1 during A-2-Y time or (2) storing into syllable 0 during

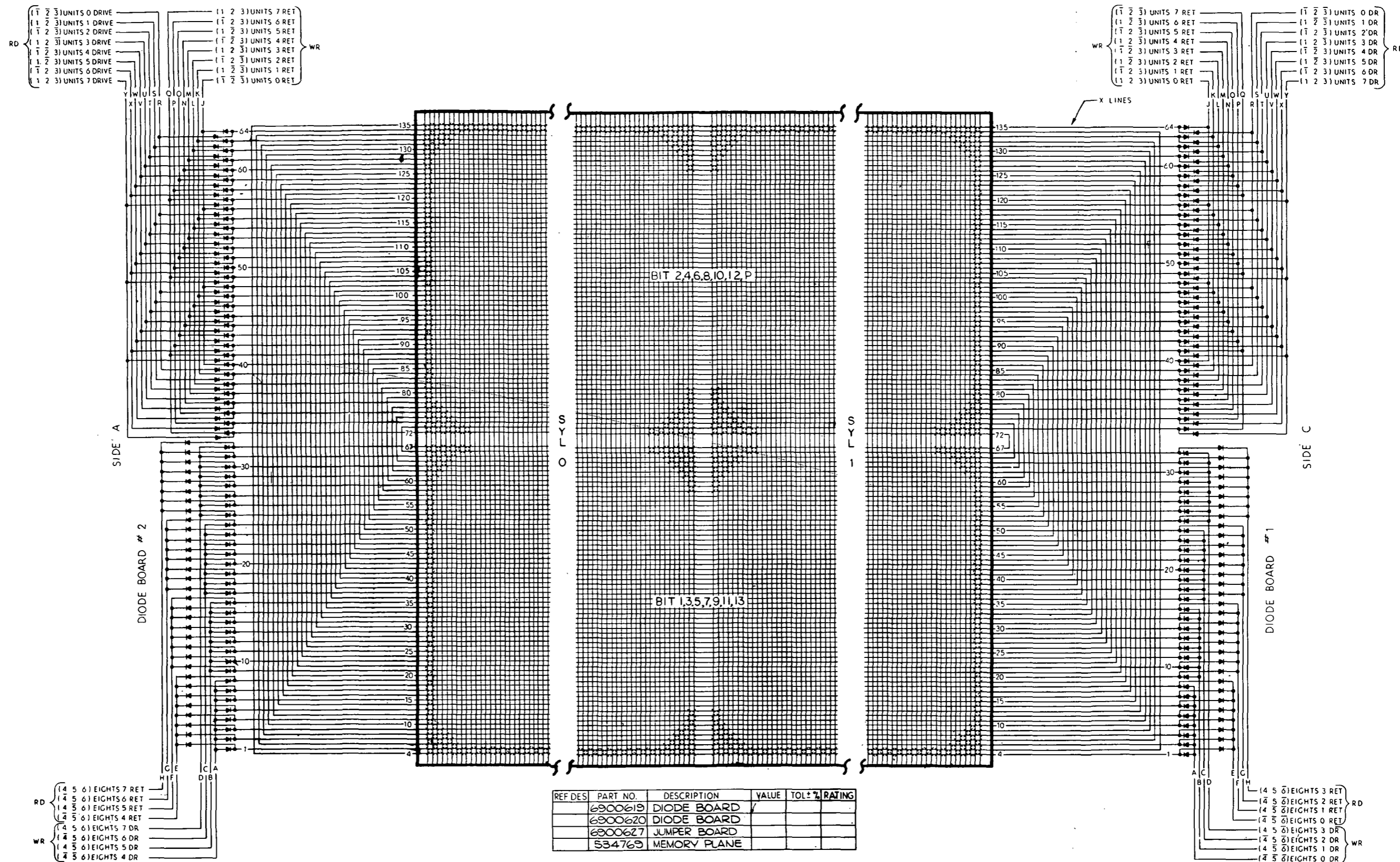
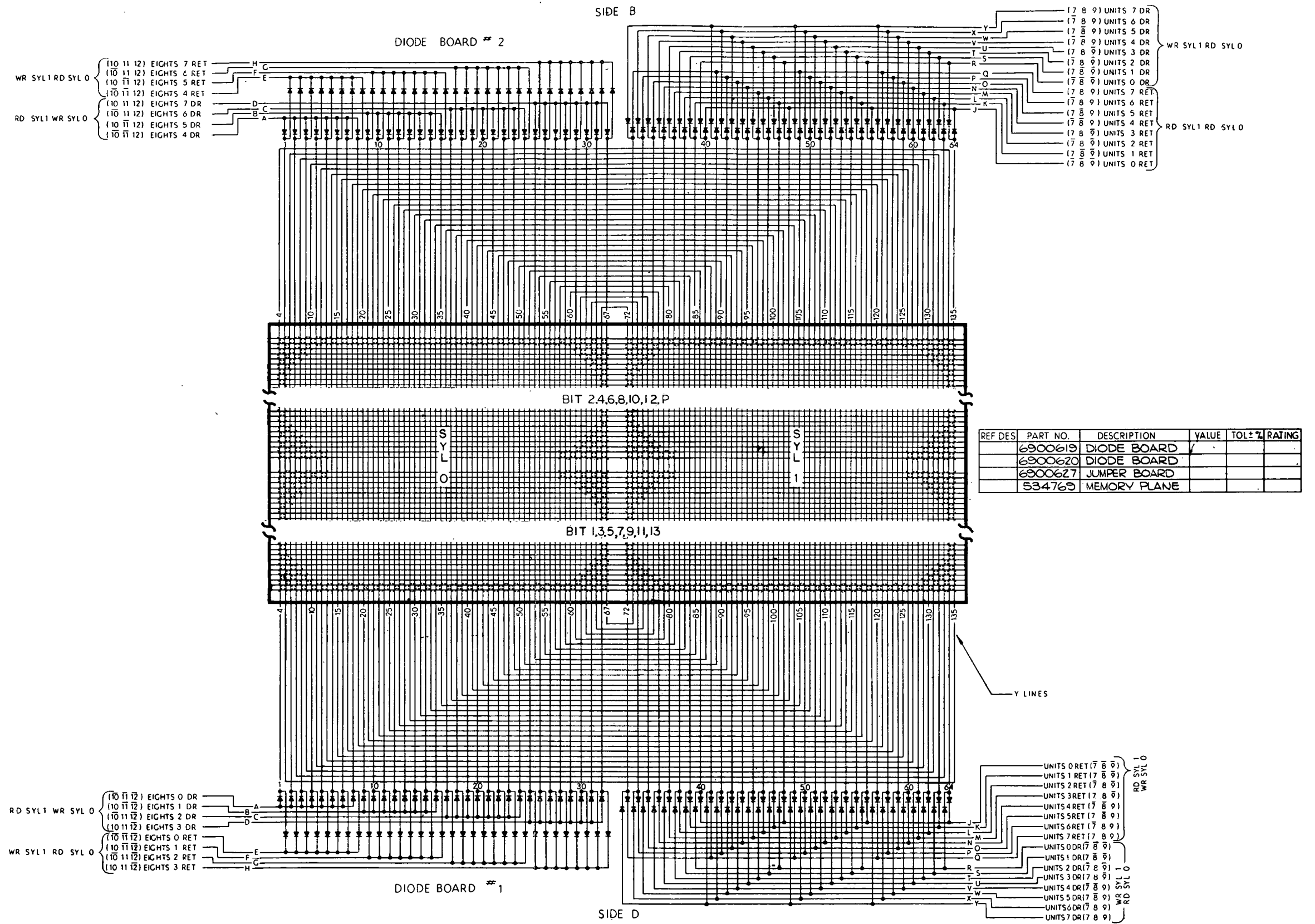


Figure 2-21. Memory Array Diode Jumper Schematic (Sheet 1 of 2)



REF DES	PART NO.	DESCRIPTION	VALUE	TOL%	RATING
	6900619	DIODE BOARD			
	6900620	DIODE BOARD			
	6900627	JUMPER BOARD			
	534769	MEMORY PLANE			

Figure 2-21. Memory Array Diode Jumper Schematic (Sheet 2)

C-2-Y time (3) or to force syllable 1 to zeroes during C-12-Y time. A read SINK is developed during memory operate at A-7-Z time for reading an instruction out of memory; during memory operate, a write SINK is developed at A-Z-10 time for restoring the instruction back into memory. A read or write SINK is initiated during memory operate and B-12-Z time either to read data from syllable 1 or to force syllable 0 into a store zeroes condition.

2-115. Memory operate (MOP) is a conditioning level which allows memory to operate. The absence of MOP causes memory timing to be inhibited. The MOP level is present at all times except when any one of seven gates (see figure 10-28, sheets 25 and 8) is conditioned. The gates are conditioned as follows:

1. When a change data sector (CDS) instruction, a transfer if minus (TMI) instruction, or a shift (SHF) instruction (OP1 NOT, OP3 and OP4) is decoded.
2. When in computer single step (CST) at 6 through 13 A time. (Instructions are prevented from being read.)
3. When in memory load (RUN NOT) at 6 through 13 A time. (Instructions are prevented from being read.)
4. When an interrupt (INT) is programmed at 6 through 13 time.
5. When a HOP is programmed during memory load.
6. When the operation code for an absolute transfer (TRA = OP1 NOT, OP2 NOT and OP3) is decoded.
7. When the operation code for a transfer if not zero (TRZ = OP1 NOT, OP2 NOT and OP4) is decoded.

2-116. During self-check, the FREE RUN SS level allows generation of MOP so that memory timing checks can be performed.

2-117. MEMORY MODULE SELECTION. Memory module selection circuits select data or instructions from a specified memory module. Data module and instruction module latches under control of the processor determine which module will be selected for data and instructions. Either memory module A or memory module B is started by means of a SYNC A or SYNC B starting pulse. (See figure 10-28, sheet 25.)

2-118. SYNC B is developed from either of two gates. One gate is conditioned by the output of the data module latch (DM1) during operation time (PAD, i. e., phase A delayed time). The gating level of SYNC B is a latch output which occurs from W to Z time with each SINK.

2-119. The other gate is conditioned during instruction time (PAD NOT) providing the residual sector is not selected (A9 NOT) when reference is made to memory B for an instruction word (IM1). The gating level in this case is the same as above, i. e., a latch output which occurs from W to Z time with each SINK.

2-120. SYNC A is developed similarly to SYNC B. The only difference is that the conditioning levels for selecting memory module A sync (sync A) are either DM0 or IM0 latch outputs. A case unique only to memory A is the development of a SYNC A when the residual sector is selected by address Bit A9 during operate time (PAD NOT). The gating level is the latch output which occurs from W to Z time with each SINK.

2-121. Memory Drive Controls. The Memory Drive Controls cause generation of timing pulses which gate information in and out of the array. During read cycles, read current pulses are gated out of the memory address drives and the sense amplifiers are strobed at the proper time. During the store cycle, pulses of store current are gated out of the memory address drivers and the selected inhibit drivers are turned on and off. Included in the memory drive controls are a binary counter which develops a read or write gate (RD-WRA) and an inhibit gate (INHIBIT GATE), five memory read or write delay circuits for proper sequencing of selection circuits, and a strobe gate. (See figure 10-28, sheets 24 and 27.) These circuits produce a series of read timing pulses and a store pulse sequence. A read memory (RDM) latch output (figure 10-28, sheets 25 and 24) in the Memory Control Element determines whether a read gate or write gate will be activated by each SYNC pulse.

2-122. Operation of a read cycle and a write cycle is identical, except for the strobe gate which applies only to read. Figures 2-22, 2-23, 2-24 and 2-25 show the timing of a read cycle, a write cycle and a strobe cycle. A memory cycle is initiated when the SYNC pulse starts the binary counter which produces a read or write gate (RD+WR). The read or write gate develops read or write delays. (See figure 10-28, sheet 24.) The read or write delays when gated by the read gate (RD GATE) control the timing and pulse width of the "read current" by timing the memory drivers on and off. The strobe gate, STROB, (figure 10-28, sheet 27) enables the memory sense amplifiers to sense the output of the cores at the proper time. The STROB output is normally a "1" level and is momentarily switched to "0" by the positive transition of the 2.25 read or write delay (RD+WR DLY 2.25) during sense amplifier enable time. When the outputs of the cores are not to be sensed, i. e., during a store operation, the inhibit strobe (STROBE INH) signal is enabled. When STROB INH is a "1" the strobe gate produces no output; consequently the memory sense amplifiers are not enabled and do not sense the core outputs. If a store cycle is required, the SYNC pulse starts the binary counter which produces the RD+WR gate. The RD+WR gate is developed just as in the read cycle. A write gate (WR GATE), however, controls the timing and pulse width of the write (store) current. Like the read, the memory address drivers are turned on and off. There is however a reversal of polarity of the memory address drivers, producing "store current" instead of "read current".

2-123. SYLLABLE SELECTION. (See figure 10-28, sheets 25 and 26.) The syllable select circuits determine which syllable of the memory will be addressed with each memory cycle. Syllable selection is determined by the SYL1 latch. The SYL1 latch is controlled by four gates in the sequence as follows:

1. At C-6-Z time the SYL1 latch is set which forces selection of SYL1.
2. At the following A-6-Y time the SYL1 latch is reset, if the syllable 1 control latch (SYLC1) is reset. SYLC1 if reset allows reading of instruction from syllable 0. If the SYLC1 latch is set at A-6-Y time, an instruction is read from syllable one.
3. At the following A-13-Y time, SYL1 latch resets or remains reset if already in the reset state. This allows syllable zero to be selected for a data read or store operation.
4. At the following B-6-Z time, if reading from memory (read level present) SYL1 latch is set and syllable one selected. If a store operation is underway syllable zero remains selected since SYL1 latch was previously reset.
5. At C-6-Z time, forced selection of syllable one is effected and the sequence of syllable selection is started again.

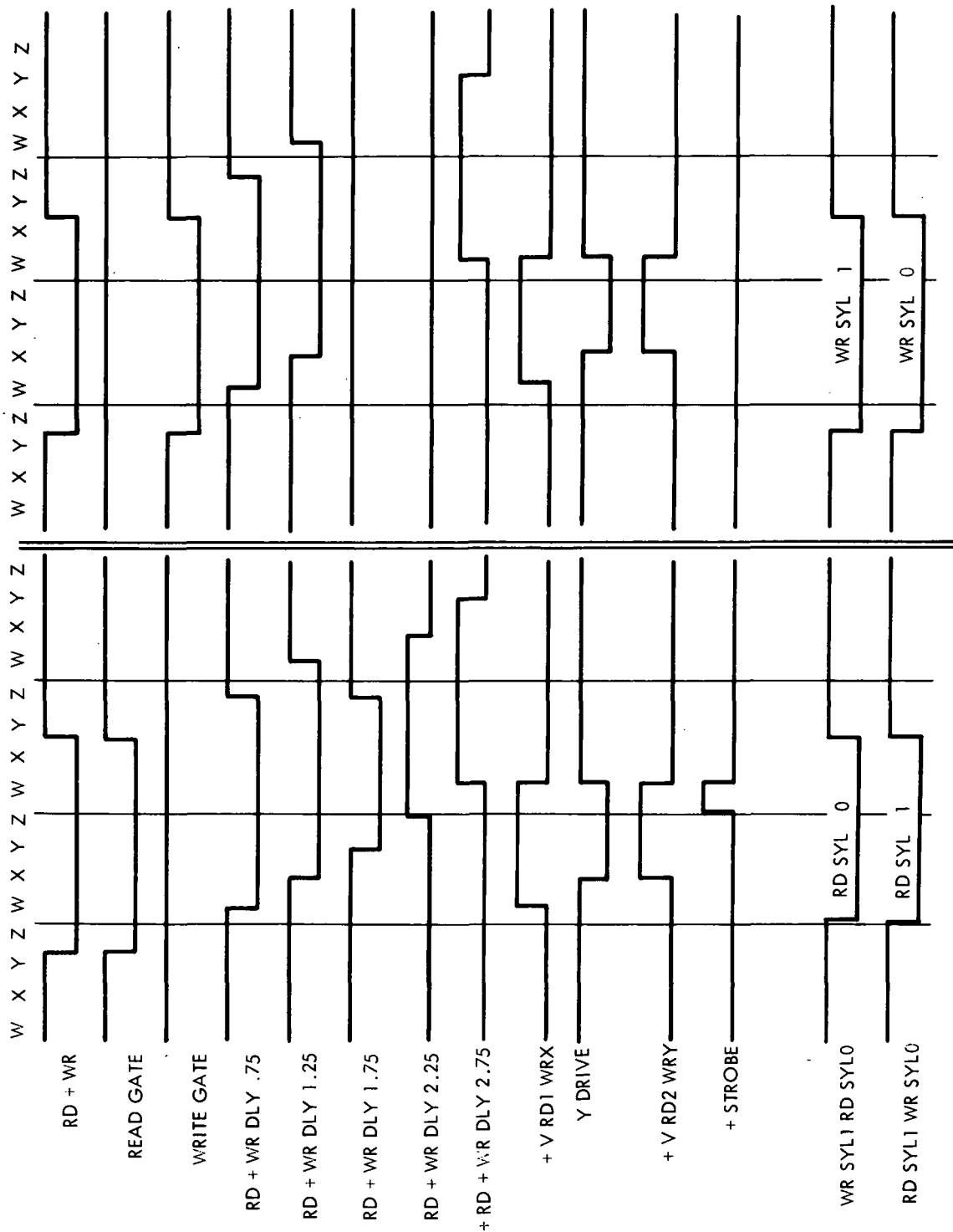


Figure 2-22. Memory Timing

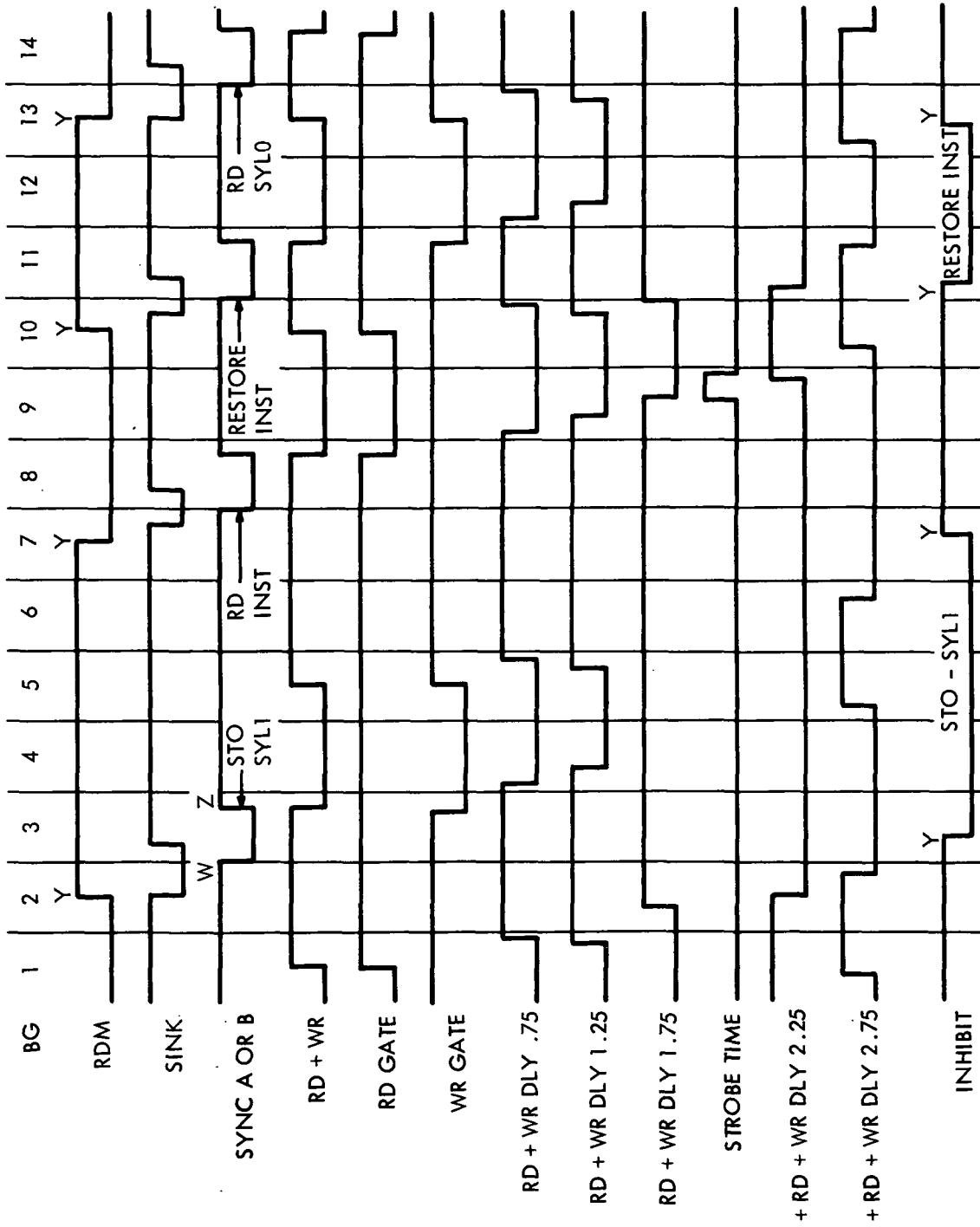


Figure 2-23. Central Processor Phase A Memory Timing

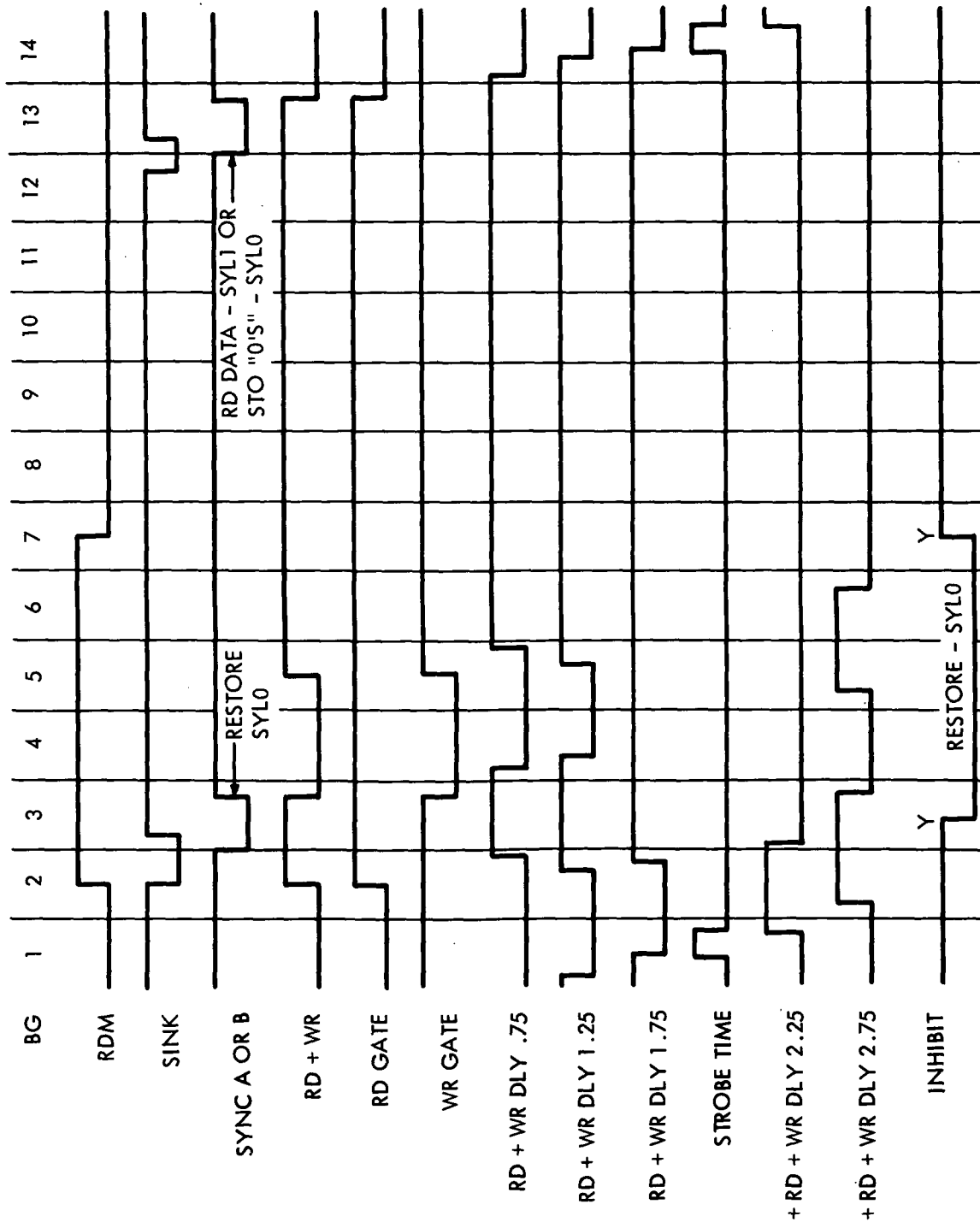


Figure 2-24. Central Processor Phase B Memory Timing

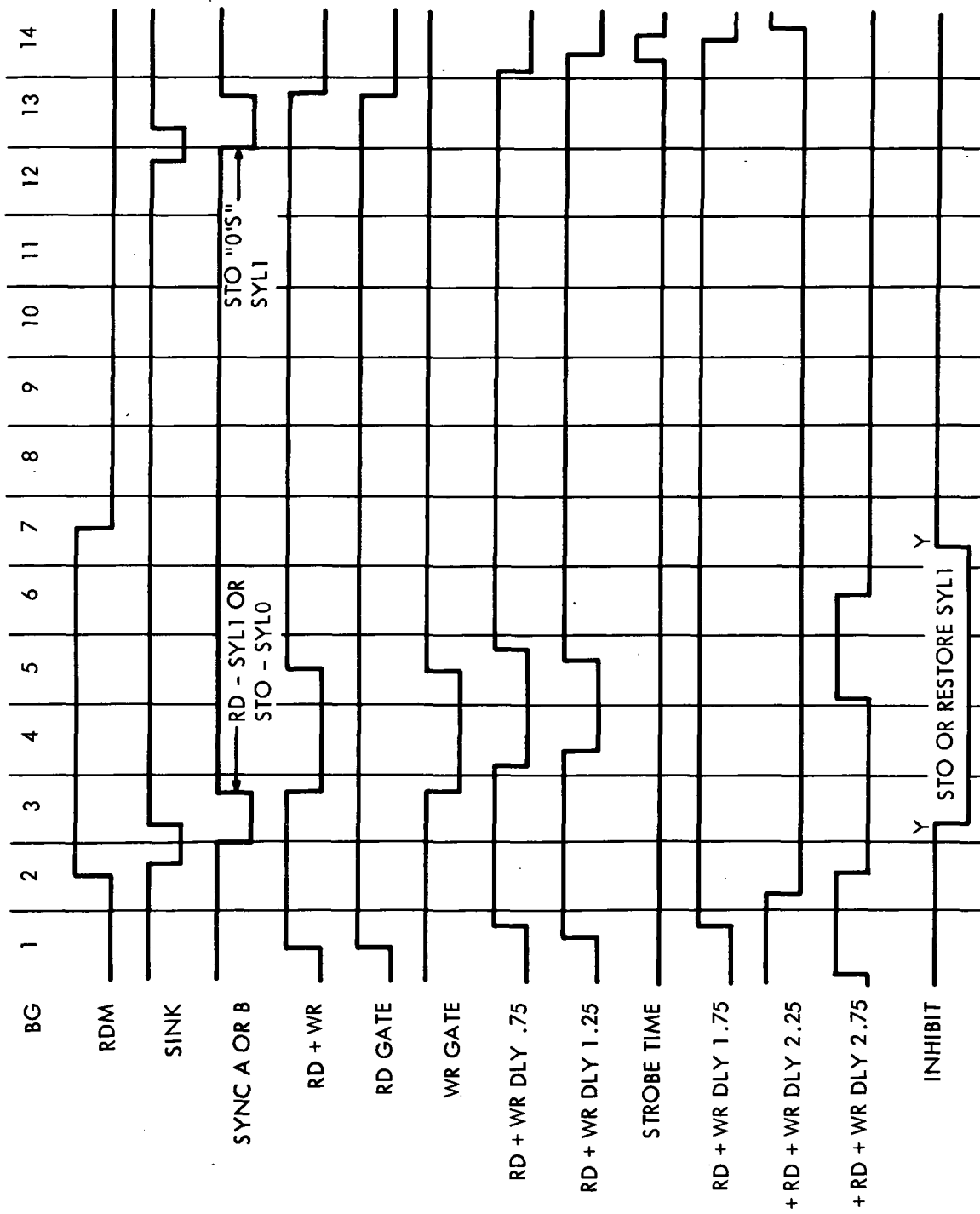


Figure 2-25. Central Processor Phase C Memory Timing

2-124. The syllable select latch outputs are ANDed with the read and write gates to form the memory drive controls. (See figure 10-28, sheet 26.) The memory drive control levels, write syllable 1 - read syllable 0 (WR SYL1 RD SYL0) and the read syllable 1 - write syllable 0 (RD SYL1 WR SYL0) for either memory A or B are developed as follows:

1. WR SYL1 RD SYL0 is developed when either the SYL1 latch is set coincident with the write gate (WR GATE) or when the SYL1 latch is reset coincident with the read gate (RD GATE).

2. RD SYL1 WR SYL0 is developed when either the SYL1 latch is set coincident with the RD GATE or when the SYL1 latch is reset coincident with the WR GATE.

2-125. MEMORY ADDRESSING (See figure 2-26.) - Random access to memory's contents facilitates variation in the programmed instruction sequence and processing similar data with a common program sub-routine. The system for specifying the location of information in the memory is the addressing scheme. A complete memory address specifies a memory module, a syllable within a module, a sector within the syllable and a location within the sector. The syllable selection applies to both modules, the sector address applies to both syllables of both modules, and the location address applies to all sectors of both syllables of both modules. But this is not yet a true picture of the memory addressing scheme because modules are not addressed in the usual sense. Instead a sector address and location address are combined in the memory address decoders to develop X-Y coordinate selection signals. These signals along with syllable selection signals, are applied to the memory address drivers of each module. The module is addressed by routing the sync impulse which initiates a memory cycle to only the selected module. Module SYNC selection has been previously described and the remainder of this discussion is limited to correlating the sector and location addresses to the X-Y coordinate of the array.

2-126. Two 4-bit registers in the processor store separate sector addresses for instructions and data words. The instruction sector register is used during instruction time and the data sector register during operation time. The content of these registers is changed at intervals in the program by special instructions located at appropriate points in the instruction sequence. The sector register latch outputs provide gated control levels which develop into A10, A11 and A12 memory address bits and augment a single 9-bit address register thereby selecting individual locations within the selected data or instruction sector. The address register is loaded twice per Central Processor cycle, once at the beginning of instruction time and again at the beginning of operation time.

2-127. The memory address decoders combine memory address register bits 10 through 12 (MAR10-12) developed from instruction sector, data sector and memory address registers in four 3-bit groups to form octal selection signals for the X-Y drivers. Figure 2-27 shows how the two addresses are combined and which set of X-Y drivers is selected by each 3-bit group. In the Lo X and Lo Y groups, octal values 0 through 7 select X and Y drivers 0 through 7 respectively; in the Hi X and Hi Y groups, the same values select X and Y drivers 00 through 70 respectively.

2-128. Notice that bit A9 of the memory address register overlaps the entire sector register in figure 2-27, part A. Bit A9 is a special purpose bit which provides the option of addressing data for one instruction from the residual sector instead of the pre-selected data sector. Because of its purpose, A9 is sometimes called the "residual bit". A "1" in bit A-9 appears to the memory address decoders as though the data sector register contained all "1's"; this overrides the registers actual content. The A9 option

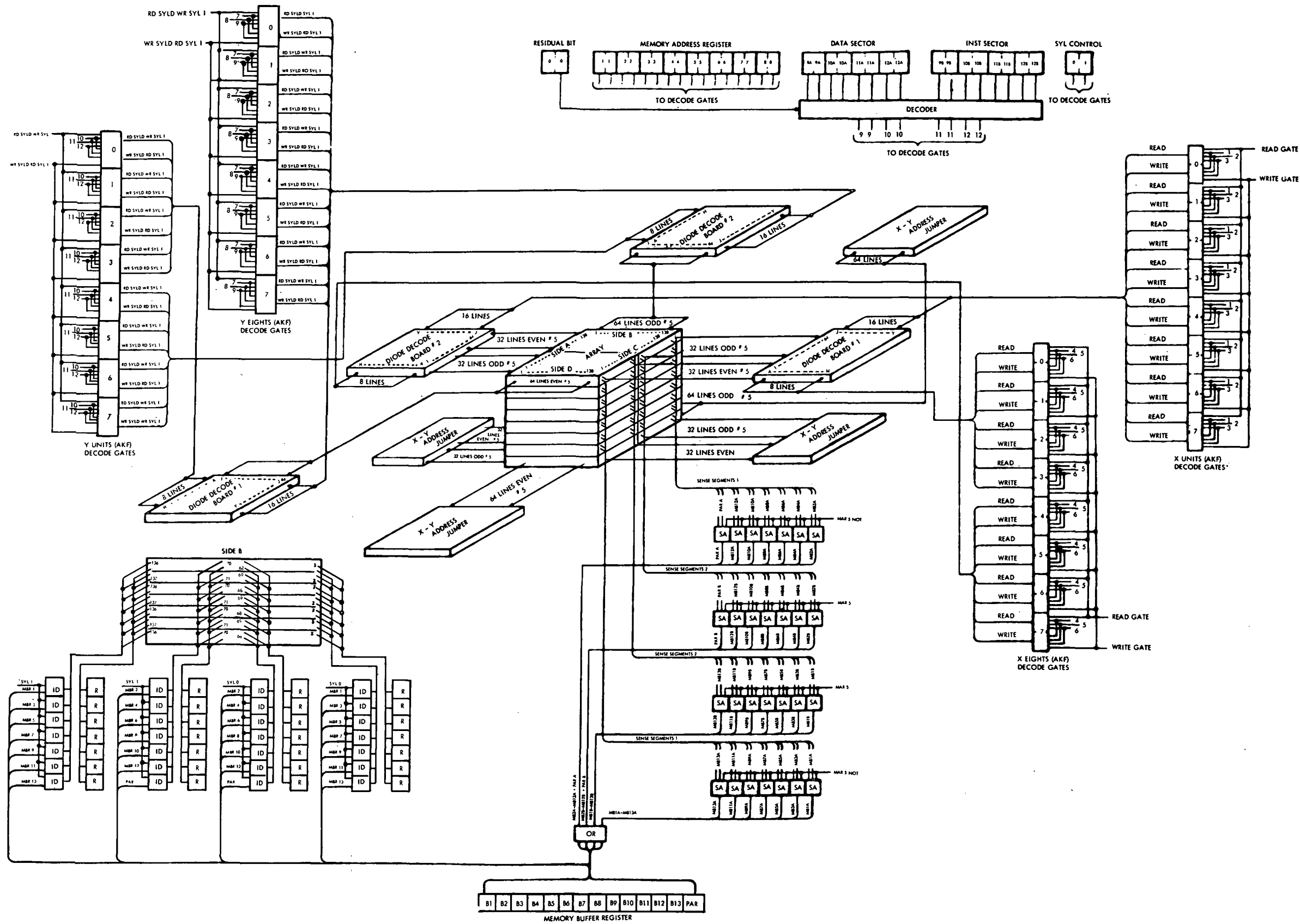
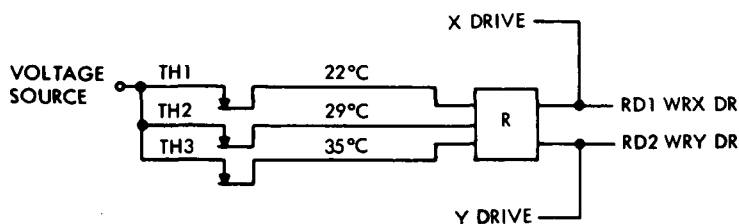


Figure 2-26. Central Processor Memory Block Diagram

REGISTER	SECTOR ADDRESS	LOCATION ADDRESSES								
MEMORY ADDRESS REG	A9	A8	A7	A6	A5	A4	A3	A2	A1	
SECTOR REG (IS/DS)	MAR12 3	MAR11 2	MAR10 1	4						
X-Y DRIVERS	HI Y	LO Y	HI X	LO X						

PART A - MEMORY ADDRESS DECODING



PART B - TEMPERATURE CONTROLLED CURRENT REGULATOR

Figure 2-27. Address Decoding and Drive Current Regulation

is not available for addressing instructions; however, instructions can be read from the residual sector by selecting it with the instruction sector register. Similarly, the residual sector can be selected by the data sector register but this defeats the purpose of the A9 bit.

2-129. Both syllables of the array are identically divided because syllable selection is independently controlled and constitutes a separate facet of memory addressing. The sectors in each syllable are assigned the octal addresses 0 through 17; sector 17 in memory module 0 is designated the residual sector. Every sector is made up of 400 octal addresses, and all but the residual sector are assigned the same set of addresses, 0 through 377. The locations in the residual sector are assigned addresses 400 through 777.

2-130. The addresses assigned to the residual sector seem to contradict figure 2-27. But, in the figure, address bit A9 is excluded from the location address in order to show its correlation to the sector register. Thus, addresses 400 through 777 exceed the capacity of the bits which specify the location address. However, each instruction contains a 9-bit operand address and it is convenient to consider all nine bits in describing data addresses. Thus the addresses in the residual sector become 400 through 777.

2-131. MEMORY ADDRESS DECODERS - (See figure 10-28, sheet 23.) The memory address decoders process memory addressing signals from the processors program control and data control sections, into conditioning levels for the memory address drivers. These conditioning levels originate in the 9-bit memory address register (MAR1 through 9) and the two 4-bit registers, instruction sector and data sector registers. The nine latches in the memory address register reflect gated transfer register bits

for selection of data addresses. MAR9 latch of the memory address register has other controls. These controls are inputs IS4 and DS4 which are the high-order bits of the instruction and data sector registers, respectively. Input IS4 is sensed at A-7-Z time concurrent with the instruction address transfer, and DS4 is sensed at A-13-Z time with the operand address transfer.

2-132. The three least significant bits of both sector addresses are developed into the hi-order octal selection bits of the Y-coordinate (MAR10, MAR11, MAR12 and inverses). Inputs are selected from the instruction sector register during instruction time and from the data sector register during operation time. During operation time (PAD NOT) when the residual sector is not selected (A9=0), DS1, DS2 and DS3 or their inverses are gated to form decode levels MAR10, MAR11 and MAR12 or their inverses, respectively. During instruction time (PAD), IS1, IS2 and IS3 or their inverses are gated to form decode levels MAR10, MAR11 and MAR12 or their inverses, respectively. When address bit A9 is a "1" during instruction time, MAR10, 11 and 12 bits are forced to "1" for residual sector selection regardless of contents of data sector latches.

2-133. Each MAR bit and its inverse is an input to a power inverter (figure 10-28, sheet 29) which has four outputs. Two outputs go to driver circuits and two to return circuits for X and Y drive line selection.

2-134. Memory Address Drivers. The Memory Address Drivers develop the X and Y drive currents and provide a means for selecting X and Y drive lines. Thirty two composite circuits represented as OR circuits on figure 10-28, sheet 29, are divided into two groups. There are 16 for X and 16 for Y, which implement a coincident current addressing scheme. Each group drives through a diode matrix (figure 2-21) to maintain isolation between drive lines. The memory address decoders develop the selection signals which condition an X drive and return circuit and a Y drive and return circuit at one time. The output of an X or Y driver is a "1" when all inputs are "0", and the output of an X or Y return is a "0" when all inputs are "0". When selected, the drivers produce coincident pulses of either read or store current through one X and one Y drive line. The five inputs to the memory address drivers are the memory address register bits (MAR and MAR NOT) and the memory drive control gates (read and write).

2-135. The logical layout of the PTC memory drive lines is illustrated on figure 2-28. When decoded, bits 1, 2 and 3 of the memory address register select 10_8 X drive lines in both the even and odd half of memory. The next three bits decoded (4, 5 and 6), select one X drive line in both the even and odd halves of memory. The 10_8 X lines selected are called the units drive lines while the single line selected as a result of the higher bits decoded is called the eights selection. The eights X drive line completes the path for current flow with one of the selected units X drive lines. It is readily seen that there are therefore 100 octal (0 through 77) X drive line selections possible in each half (odd and even) of memory. There are four gates originating in the memory timing controls which control X drive line selections for either reading or writing. They are the write syllable 1 - read syllable 0 gate (WR SYL1 RD SYL0), the read syllable 1 - write syllable 0 gate (RD SYL1 WR SYL0), the read 1 - write X gate (RD1 WRX DRIVE) and the read 2 - write Y gate (RD 2 WRY DRIVE). These gates are discussed in later paragraphs.

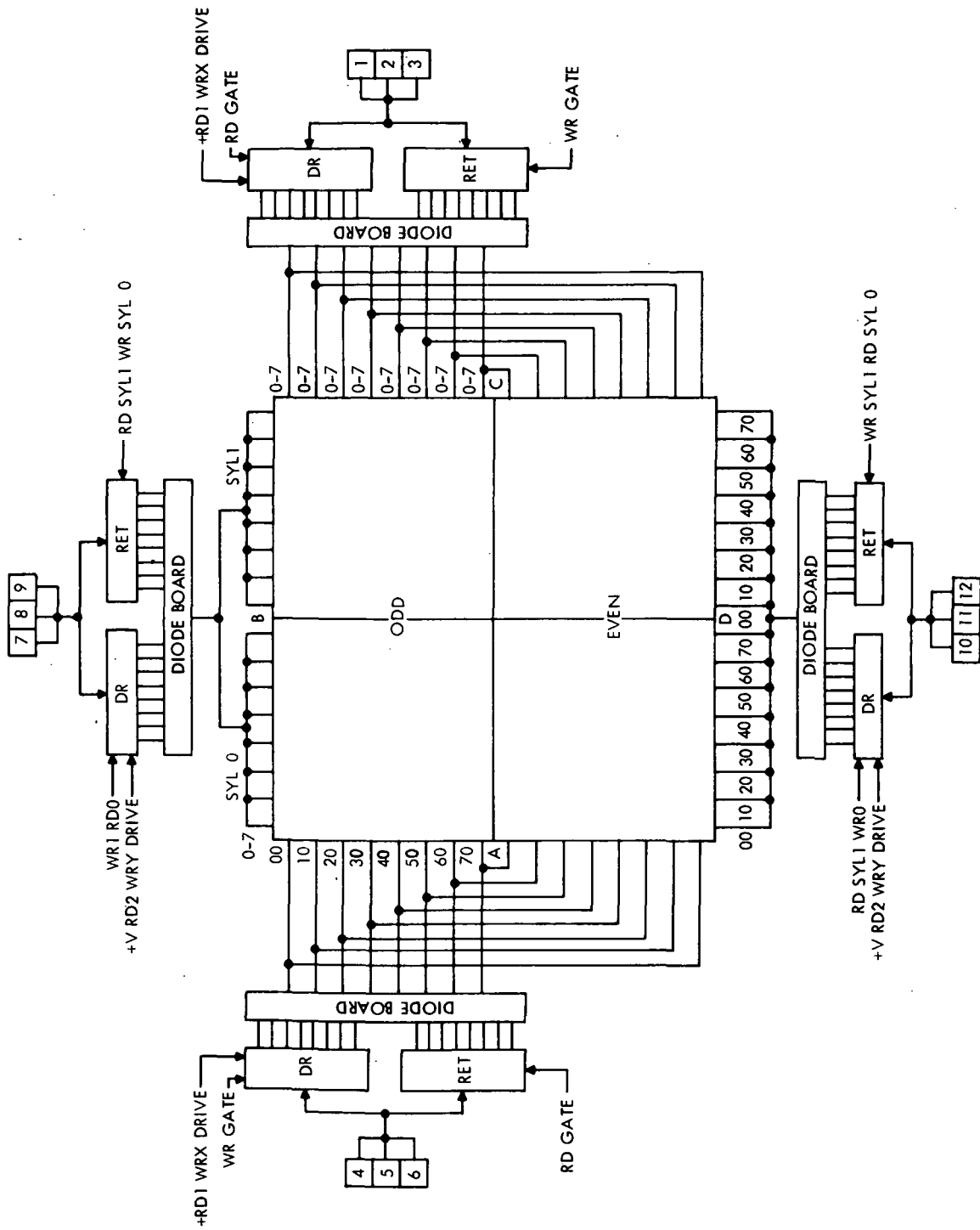


Figure 2-28. Logical Layout of Memory Drive Lines

2-136. The units and eights method for selecting Y drive lines is the same. Memory address register bits (7, 8 and 9) and (10, 11 and 12) are used for units and tens drive line selections respectively. There is however a major variation. Instead of odd - even bit selection, syllable selection (either 1 or 0) is made through the Y selection gates. The syllables are selected as a result of control gates which have their origin in the memory timing controls. They are the write syllable 1 - read syllable 0 gate (WR SYL1 RD SYL0), the read syllable 1 - write syllable 0 gate (RD SYL1 WR SYL0), and the read 2 - write Y gate (+URD2 WRY). (To be discussed later.)

2-137. In both the X and Y drive lines, read current flows in the opposite direction to write current. This allows selections of the same cores using the same drive lines but different drive sources. Figure 2-29 illustrates core selection for address location 00 during both read and write. The two selected cores in address 00 are in the corners of the plane where X and Y drives intersect. Note that the current flows from the return (RET) to the driver (DR) in every case and that half currents (in both X and Y) in the two corner cores are aiding while the coincident currents in the other two cores are opposing thereby cancelling each others effect. All other cores shown are half-selects.

2-138. Core locations for addresses that follow in the next higher order are not in close proximity to those in address 00. If it is desired to find the physical location of the cores in other address locations, find the X and Y drive lines (figure 2-21) from the decoded memory address bits. The locations where X and Y drives intersect and their currents are aiding reflects the address selected cores.

2-139. Temperature Controlled Current Regulator. (See figure 10-28, sheet 26.) The switching characteristics of ferrite cores are subject to change with variations in temperature. The temperature controlled current regulator continuously adjusts the X and Y driver output current to the optimum value for the temperature in the array. A shunt resistance (R) is controlled by thermal switches, which effectively changes the value of current supplied by the 40 watt current source. Decreases in memory ambient temperature require increases in drive current. As the temperature decreases, three resistors are successively shunted across a 40 watt current limiting resistor via thermal switches TH1, TH2 and TH3, thereby decreasing its resistance and permitting more current to flow. Thermal switches TH1 - TH3 open successively as the temperature increases thereby effectively increasing the resistance which decreases the drive current. (See figure 2-27, part B.)

2-140. The current developed passes through the selected X and Y drive lines at the times dictated by the read - write delays. The X drive current, called read 1 write X drive (RD 1 WRX DRIVE), starts earlier than the Y drive current (RD2 WRX DRIVE) to eliminate possible noise from simultaneous starting of X and Y drive currents.

2-141. Inhibit Drivers. The Inhibit Drivers facilitate storing each bit of an addressed memory location separately, by preventing cores which are to contain "0's" from being switches to "1's". Twenty-eight inhibit drivers (four per plane), such as the one shown in figure 2-30, are provided to drive the seven active planes of each memory array. During store or restore cycles, inhibit drivers conditioned by "0's" in the memory buffer registers develop current pulses equal in magnitude but opposing the Y half-select current. Memory timing causes inhibit drivers to turn on and off so that inhibit current overlaps the Y drive current. Thus, addressed cores in inhibited planes supply only the X half-select current and are not switched.

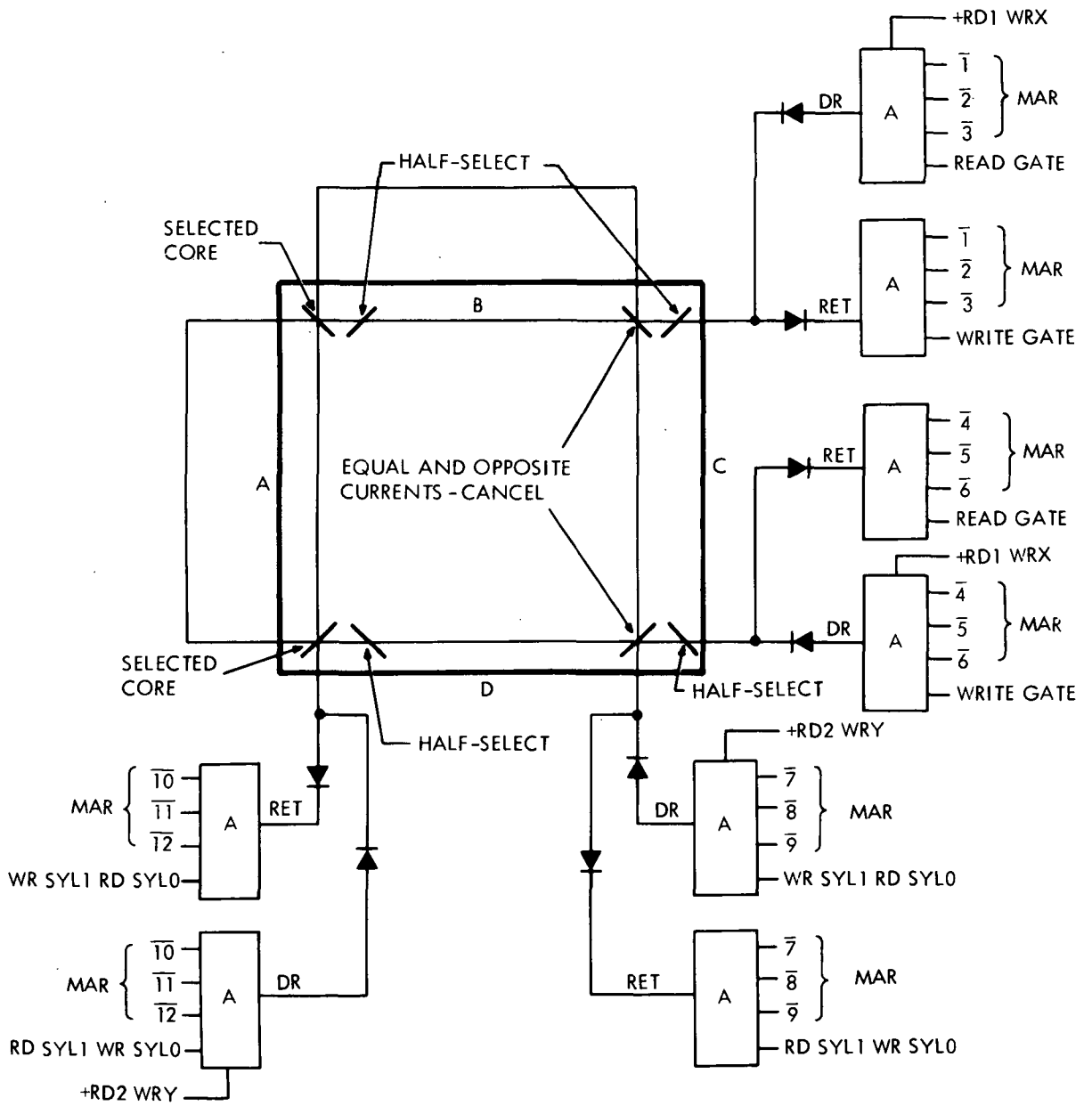


Figure 2-29. Core Selection for Location 00 During Read and Write

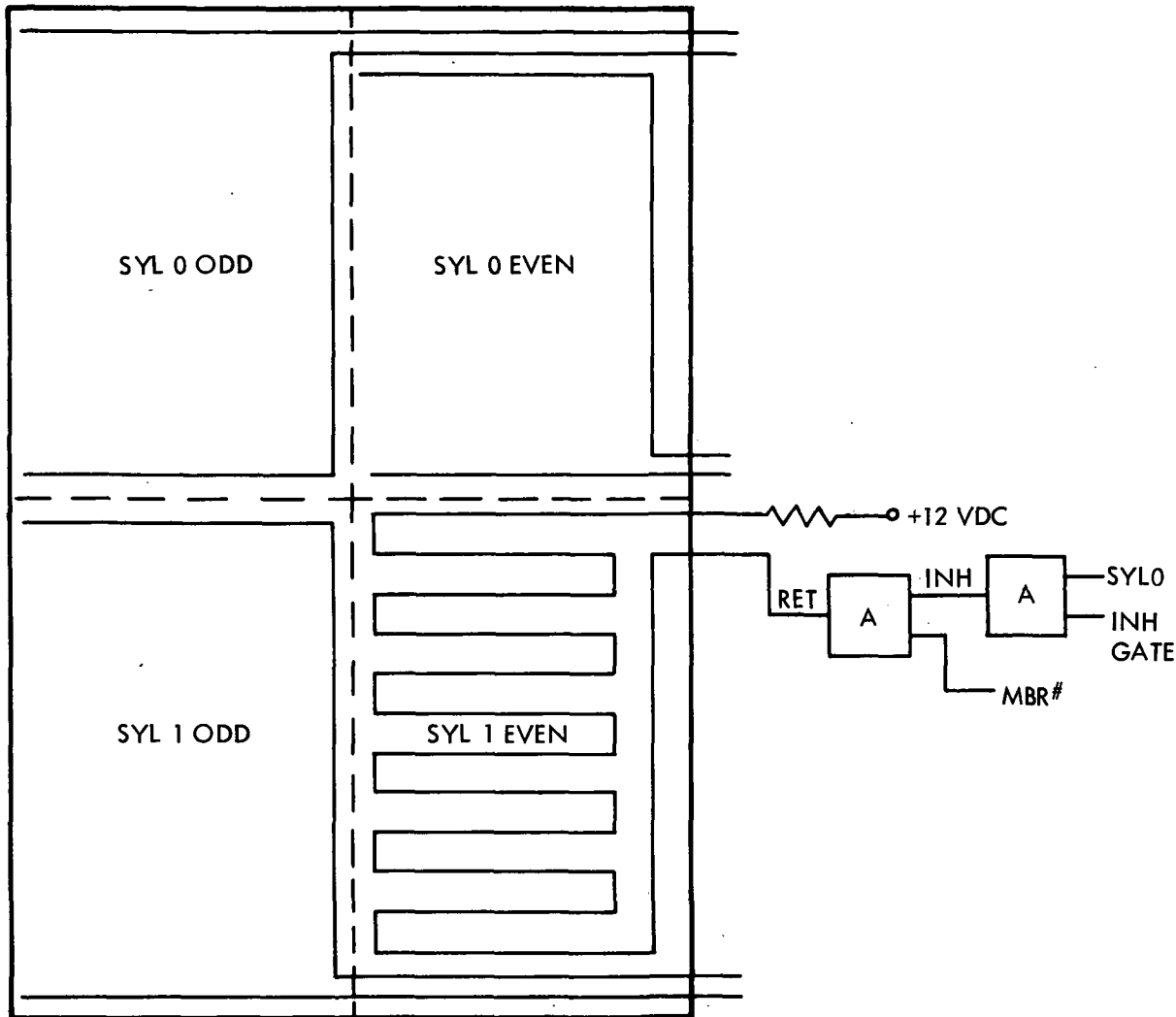


Figure 2-30. Inhibit Winding and Driver

Two signals condition an AND circuit which controls the turning on of each inhibit driver. They are the memory buffer register latches (bit = "0") and an inhibit (INH) level developed from memory timing controls. The INH level occurs for the syllable selected when the INHIBIT GATE is present. The INHIBIT GATE, a latch output level, is developed at each SYNC and Y time prior to the setting of the RD+ WR latch. (See figure 10-28, sheets 24 and 27 and figures 2-23, 2-24 and 2-25 for inhibit circuits and timing.) The INHIBIT GATE latch is reset every read memory time; therefore, an inhibit operation can take place only during a write time.

2-142. Memory Sense Amplifiers. (See block diagram, figure 2-26, for the overall sense amplifier scheme and figure 10-28, sheets 27 and 28 for particulars.) The memory sense amplifiers discriminate between "1's" and "0's" at the outputs of the memory plane segments sense windings. A separate memory sense amplifier (figure 2-31) is provided for each of the four segments of each plane of the array; thus, each bit of each syllable is sampled individually. Upon sensing a "1" in the sense winding, the memory sense amplifier delivers a timed output to the memory buffer latch corresponding to the bit which was sensed.

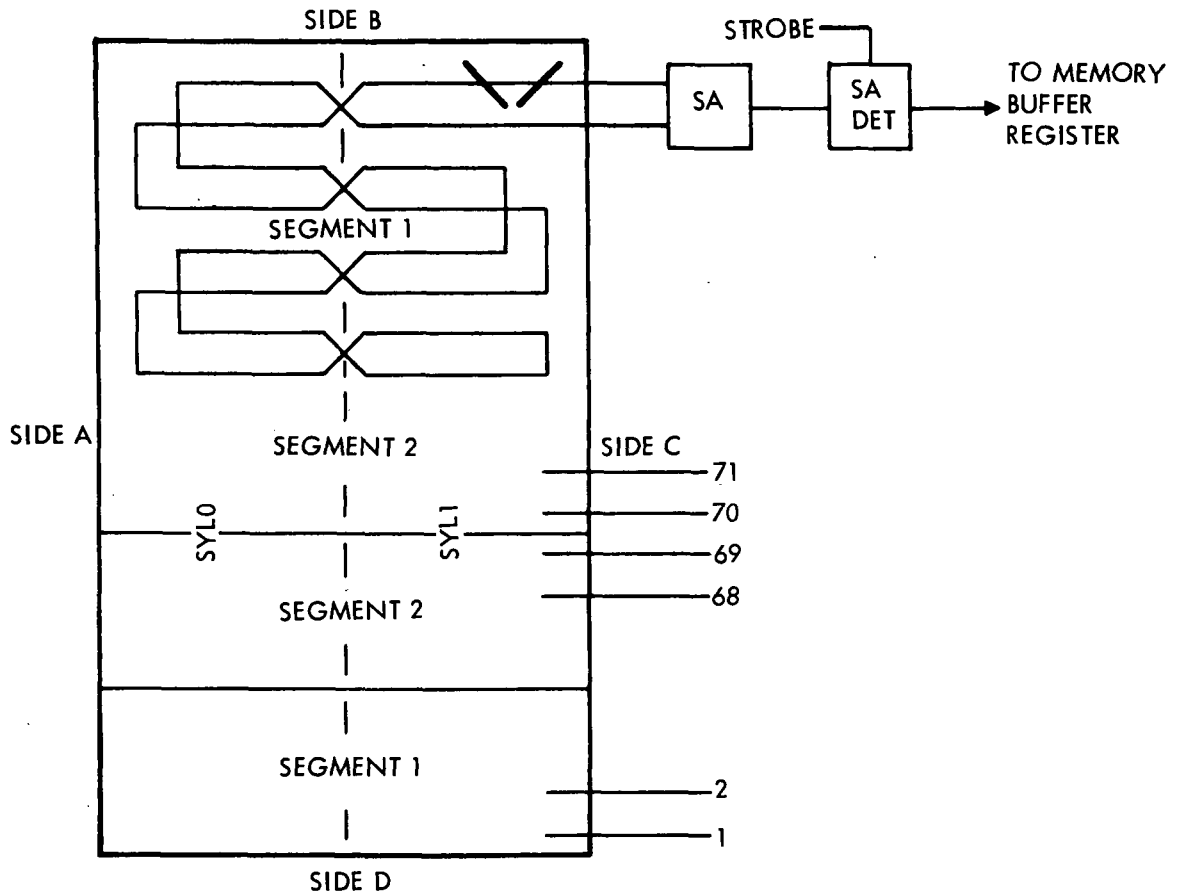


Figure 2-31. Memory Sense Amplifier and Winding

2-143. The input stage to the memory sense amplifier is a differential amplifier (SA); thus the circuit senses both positive and negative "1" outputs from the sense winding when enabled by bit A5 for proper segment selection (A5 = "0" enables segment 1, and A5 = "1" enables segment 2). The outputs of the differential amplifier are coupled to an output switching stage which is controlled by the input of a strobe gate (SA STROBE). The output switching stage (SA DET) is a strobed Schmitt trigger that produces a "1" output only when its associated sense amplifier senses a "1" and the strobe input is a "0". The SA STROBE is an inverted and amplifier STROBE. STROBE is a "1" during coincidence of decoded store operation and the 2.25 and 1.75 RD + WR DLY.

2-144. Memory Buffer Register. (See figure 10-28, sheet 21.) The memory buffer register is an intermediary register consisting of 14 latches which regulate information flow into and from the memory.

2-145. Computer memory readout is destructive: as data is read from the memory, the applicable memory bits are all driven to "0". The buffer registers hold the data read from memory long enough so that it can be read back in, thereby making the memory readout effectively non-destructive.

2-146. In addition to saving the memory from progressive obliteration, the memory buffer registers feed memory data to the transfer register and receive data to be stored in memory from the transfer register.

2-147. Each of the memory buffer latches is similar. A typical buffer latch with input controls and outputs is shown in figure 2-32.

2-148. Each memory buffer latch is controlled either manually or automatically (normal operation). The manual loading of the memory buffer register is a self-check device and its use is available only when the timing is stopped.

2-149. When manually selected, the memory buffer register switches (MBR SW#) on the CE PANEL condition set gates of the corresponding buffer latches. The condition of each buffer latch and associated manual selection switch is indicated by corresponding lamps on the CE PANEL. All previous information is cleared from the buffer by a buffer reset (MBRST) level. The MBRST, a positive level, is caused by the set output of a control latch together with a gating level which stops CE PANEL timing. The control latch is set when the LOAD switch (MEM LOAD SW) is pressed; the CE PANEL timing is stopped when the SINGLE PHASE switch is actuated. MBRST is inverted to form control buffer resets 1 and 2 (CBR1 and 2) which clear all of the memory buffer latches. When the LOAD switch is released, an AND gate is conditioned and the set memory buffer 1 and 2 (SET MBR 1 and 2) gating levels gate all of the selected switch information into the memory buffer register. At the same time, the reset buffer register level is removed. The first Y time after clock pulses start, the control latch is now reset causing the gating levels to be removed and the reset levels to be reapplied.

2-150. The buffer latches are set in two ways while operating automatically (normal operation). Transfer register bits (TR#) are gated into the buffer with a set buffer register level (SBR X, Y or Z). The set buffer register level is implemented only during a store operation during clock times X, Y or Z as shown on figure 10-28, sheet 21. A memory buffer register latch is also set whenever the output of the corresponding sense amplifier reflects a "1" level. The memory buffer register is reset every bit gate 6 time or A-14 time.

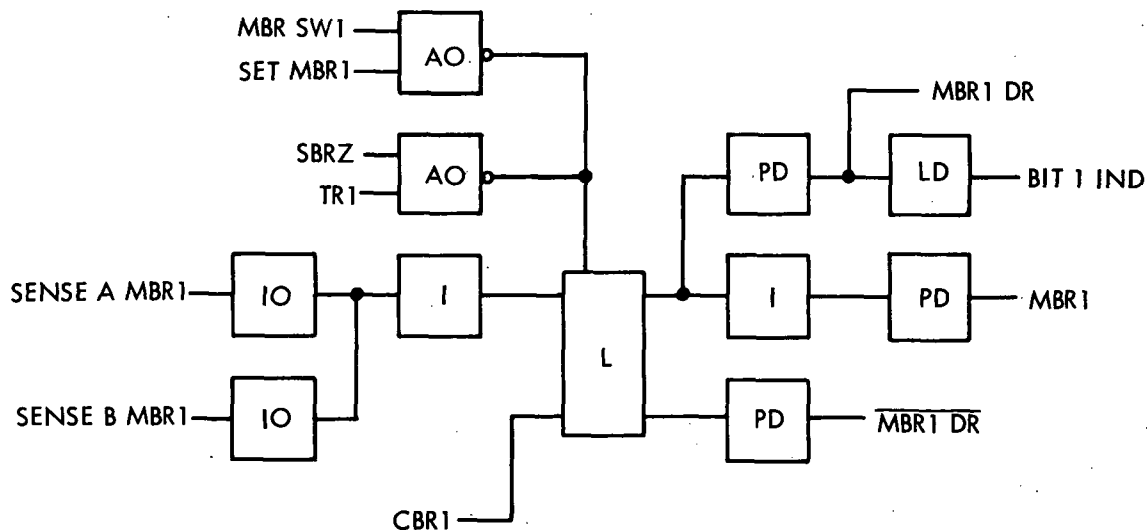


Figure 2-32. Typical Memory Buffer Latch

2-151. Each buffer latch has two outputs. The memory buffer drive (MBR #DR) goes to the transfer register and parity check circuits whereas the memory buffer output (MBR #) is applied to the inhibit drivers.

2-152. The condition of the memory buffer latches is displayed on the CE PANEL as previously described. Memory buffer register information can also be displayed on the PROCESSOR DISPLAY PANEL if desired. (See figure 10-28, sheet 23.) Buffer register or transfer register information is gated into the data lamps by memory buffer indicator inhibit not (MBR IND INH NOT) or transfer register indicator inhibit not (TR INDINH NOT) levels respectively. The generation of either of these two levels is developed by manually actuating alternate action switches: memory register switch (MEM REG SW) or transfer register switch (TR REG SW) on the PROCESSOR DISPLAY PANEL.

2-153. MEMORY PARITY CHECK. (See figure 10-28, sheet 22.) The memory buffer register, broken into four parts, is checked for odd parity by four parity detector circuits. The detector circuit outputs, called memory buffer register parity levels 1, 2, 3 and 4 (MBRL 1, 2, 3 and 4), are inputs to another parity detector circuit which finally determines total buffer register parity. (Typical parity detector circuits are described in detail in a previous paragraph and a diagram of a parity detector circuit is shown on figure 2-3.) When an even number of one's are detected the resultant is an error buffer register parity level (EAP) output. An EAP is checked for by a parity check latch. The checking time of the parity check latch is two clock pulses in duration at read memory time from A-10-Y, B-2-Y or C-2-Y times. If the error is coincident with the error check time, a PARITY ERROR latch is set and an error indicator lamp is lit on the CE PANEL.

2-154. DATA CONTROL ELEMENT LOGIC CIRCUITS.

2-155. TRANSFER REGISTER. (See figure 10-28, sheet 9.) The transfer register is a 13-bit shift register which receives from and sends inputs to the memory buffer register, arithmetic element, and the Memory Loader/Data Display. Figure 2-33 is a block diagram of the transfer register which consists of 19 latches connected in series. Serial inputs are applied to the TR1 latch and from there shifted bit-by-bit into the register. The serial inputs are DIN, HOPC1, and AI 1. DIN is the input from the Memory Loader. HOPC1 is the output of the automatic HOP save circuit and is gated into the transfer register for a STO 776_g or 777_g command (SSS). The 26 bit data word appearing on the AI 1 line is gated into the transfer register during a store operation unless the operand address is 776_g or 777_g (STACC). The instruction counter bits appearing on the AI 1 line are gated into the transfer register every central processor cycle from C-14 time to the following A-7 time.

2-156. Data is transferred in parallel into the transfer register from the memory buffer register (MBR1 DR through MBR13 DR). The data is transferred into the corresponding transfer register latches TR1 through TR13 at X time, except for latches TR2, TR4, TR7, and TR10 which have data shifted into them at Y time. These latches are loaded at Y time to avoid a double read-in.

2-157. The transfer register also receives parallel inputs from the external control element INTIME, and FORCE A1 through FORCE A4. These signals are generated during an interrupt operation and form a code which is loaded into latches TR5 through TR9. This action allows one of the residual addresses 400_g through 417_g to be loaded into the transfer register.

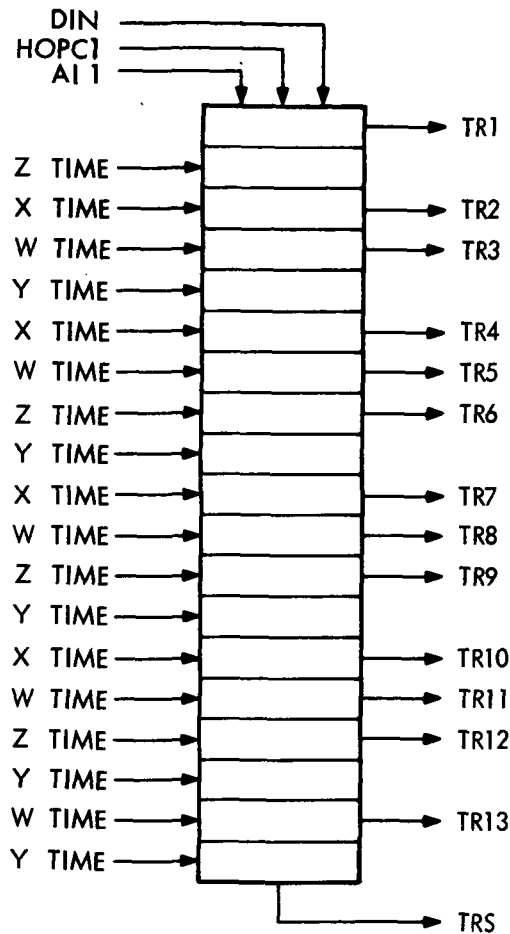


Figure 2-33. Transfer Register

2-158. **TRANSFER REGISTER CONTROL LOGIC.** (See Figure 10-28, sheet 8.) The transfer register control logic consists of the transfer register control latches SRTR, CLTR, and TBR, and the parity counter.

2-159. **Transfer Register Control Latches.** The control latches determine when data is shifted into, through, or out of the register (SRTR), when the register is cleared of data (CLTR), and when data is loaded into the register in parallel (TBR).

2-160. When the SRTR latch is set, data may be shifted into and through the register, or data in the register may be shifted out through the TRS latch. Stored data is shifted out of the TRS latch from B-3-Y time to the following A-7-Y time except when a TNZ, TMI, or TRA operation is being performed (TTT = "O"). When a TNZ, TMI, or TRA operation is being performed data is shifted out of the TRS latch starting at B-5-Y time. During a STO operation data is shifted into the transfer register from B-1-Y time to the following A-7-Y time. When the Central Processor operation is halted (RUN NOT = "1") and OP 2 = "1", the SRTR latch is reset at A-2-Y Time.

2-161. When the TBR latch is set, data is transferred from the memory buffer register into the transfer register. The instruction word is transferred at A-11 time. Syllable 0 and Syllable 1 of the data word are transferred at B-3 and C-2 times respectively.

2-162. When the CTRL latch is set the transfer register is cleared as follows:

1. At A-8-Y time prior to transfer of the instruction word from memory.
2. At A-14-Y time prior to the transfer of a data word from memory except when a TNZ, TMI, or TRA operation is being performed (TTT = "0").
3. When central processor operation is halted (RUN NOT = "1") and OP2 = "1" at A-2-Y time.

2-163. Parity Counter. The parity counter assigns parity bits by making all syllables have "odd" parity. Odd parity means that the total number of "1's" in a syllable is odd. The parity counter "counts" the number of "1's" in a syllable and adds a "1" as necessary, so that the total number of "1's" is an odd number. Thus, if the total number of "1's" is even, the parity counter adds a bit; if odd, no bit is added. The parity counter operates during a Store operation when data is loaded into the memory.

2-164. The parity bit counter consists of a binary counter whose outputs are PDD and PDD NOT, control latch CKP, and parity bit storage latch PAR. The binary counter is set every central processor cycle at A-1 time. During a store operation, bits are read into the transfer register during B and C times. As syllable zero bits 25 through 13 are shifted out of the TR1 latch into the TR2 latch, the bits are also read into the binary counter and the PAR latch. The PAR latch is unaffected by bits 25 through 14 because the input gates are closed (SBRZ = "0"). The first "1" out of TR1 clears the binary counter indicating that the total number of bits is odd and an odd parity bit is not needed. The next "1" sets the binary counter indicating that an odd parity bit is needed. Thus the first, third, fifth, etc. "1" resets the binary counter, while the second, fourth, sixth, etc. "1" set the binary counter.

2-165. When the last bit in syllable zero is read into the TR1 latch (bit 13 at 14 time) the entire syllable zero is stored in the transfer register. Syllable zero is now ready to be transferred to the buffer register. This transfer occurs at B-14-Z time when SBRZ = "1". The parity of the low order half of the data must be assigned prior to the transfer. At B-14-W time the binary counter contains the parity "state" of the first 12 bits of data. The TR1 latch contains bit 13 of the data word. These two pieces of information are applied to the set gates of the PAR latch. Two conditions may exist which necessitate a parity bit to be assigned to the syllable of data: if the number of "1's" in the first 12 bits is even (PDD = "1") and TR1 = "0", thus making the total even; or the number of "1's" in the first 12 bits is odd (PDD = 0) and TR1 = "1", also making the total even. When SBRZ = "1" both conditions will set the PAR latch and assign a "1" to the parity bit of the data placed in the memory. At the same time SBRZ will initialize to the zero, or even bit, condition. Note that parity is checked anytime data is shifted into, or out of, the transfer register (SRTR - "1" sets CKP = "1"). However, only a Store operation can set SBRZ = "1".

2-166. PROGRAM CONTROL ELEMENT LOGIC CIRCUITS.

2-167. ADDRESS REGISTER. (See figure 10-28, sheet 17.) The address register stores instruction or data word addresses while the selected word is read from memory. During an instruction word time, the address register stores the instruction address (from the instruction counter) to select the instruction word address; the operand address portion of the instruction word, stored during data word time, is used to select the data word address.

2-168. The address register consists of nine latches, A1 through A9. Latches A1 through A8 select one of the 4008 memory locations in a sector; latch A9 determines whether the addressed data will come from a pre-selected sector, or from the residual memory. The addresses of selected memory locations are loaded into the address register from the transfer register. The address register outputs condition the address decoders in the memory control element and provide control to the LVDCME and LVDAME for PIO and CIO operations. The transfer address (TA) latch provides timing and control for the register.

2-169. The instruction address (from the instruction counter) is stored in the address register from A-8-W through A-13-X time. During this period, the addressed instruction is read from memory and placed in the transfer register. The operand address portion of the instruction is then transferred to the address register at A-13-Z time for storage while the data word is read from memory. The address register stores the data word address from A-14-W through the following A-7-X time. The address register is reset at A-7-Y and A-13-Y times, prior to storing the instruction and data addresses.

2-170. The TA latch is set during two different periods. The TA latch is set from A-7-X to A-8-W time, during this period the address register is reset at A-7-Y time and is loaded with the instruction address at the following Z time. The TA latch is set again from A-13-X to A-14-W time; at this time the address register is reset at A-13-Y time and is loaded with the word address at the following Z time.

2-171. OP CODE REGISTER. (See figure 10-28, sheet 18.) The four-bit OP code register stores the code of the commanded instruction while the instruction is executed. The OP code register outputs control the operation of the circuits which execute the instructions.

2-172. The OP code register, loaded by the transfer register, stores the operation code from A-12-Y to A-5-Y time, nearly a full central processor cycle. Operation of the register differs slightly during a computer single step operation.

2-173. The single step (CST) signal generated in the external control element during C time of the selected central processor cycle, forces a TNZ operation code (OP3) into the OP code register. The TNZ code disables memory because it requires no operand. The central processor then idles in this condition until the CST signal is removed allowing the next operation code to be loaded into the OP code register.

2-174. DATA AND INSTRUCTION SECTOR REGISTERS. (See figure 10-28, sheets 18 and 19.) The data and instruction sector registers store sector codes to select one of 16 memory sectors during operation and instruction times, respectively. Sector codes are loaded into both registers during a HOP instruction, the data sector register is also loaded during a change data sector (CDS) instruction. The registers store the sector codes until the next HOP (or CDS) instruction commands them to change.

2-175. The data sector (DS) and instruction sector (IS) registers each contain four latches. The HOP constant appears as a 26-bit serial output of the transfer register serial output latch (TRS) during B and C times. The data sector code emerges from the TRS latch from C-9 time to C-12 time and is loaded into the corresponding DS register latches at Z time. The DS register can also be loaded with the code contained in operand address bits A1 through A4 of a CDS instruction. These bits are stored in latches TR5 through TR8 of the transfer register and are loaded into the DS register at A-7-Z time (CDS TAZ). The DS latches are reset at the Y time preceeding the Z time at which they are loaded.

2-176. The IS register is loaded in the same manner as the DS register with the following exceptions. The IS latches are set and reset only during a HOP instruction. The instruction sector code occupies a different position in the HOP constant than the data sector code and consequently requires different timing signals to accept it. The IS register is loaded at bit times B-5-Z through B-8-Z.

2-177. DATA AND INSTRUCTION MODULE REGISTERS. (See figure 10-28, sheet 19.) The data and instruction module registers control the selection of the memory modules during operation and instruction times respectively. Module codes are loaded into both registers during a HOP instruction; the data module register is also loaded during a CDS instruction. The registers store the module codes until the next HOP (or CDS) instruction commands them to change.

2-178. The data module (DM) and instruction module (IM) registers each contain one latch. For a HOP instruction the data module code emerges from the TRS latch during C-6 time and is loaded into the DM latch at Y time. During a CDS instruction the DM latch is loaded with the code contained in operand address bit A5. This bit is stored in the transfer register TR4 latch and is loaded into the DM latch at A-7-Z time (CDS TAZ). The DM latch is reset at the Y time preceding the Z time at which it is loaded.

2-179. The IM latch is loaded in the same manner as the DS latch with the following exceptions. The IM latch is set and reset only during a HOP instruction. The instruction module code emerges from the TRS latch during C-14 time and is loaded into the IM latch at Z time.

2-180. INSTRUCTION WORD SYLLABLE CONTROL LOGIC. (See figure 10-28, sheet 19.) The instruction word syllable control logic controls the selection of the memory syllable during instruction time. The instruction word syllable control logic consists of the SLYC1 latch and a control latch. The control latch is set when TRS = "1" at B-9-Z time (HOP constant syllable code = "1" or operand address A9 bit = "1"). The SLYC1 latch is then set at the next B-10-Z time, if a HOP TNZ, TMI, or TRA operation (UTR) is being performed. The control latch is reset every B-12-W time and the SLYC1 latch is reset at the Y time preceding the Z time at which it is loaded.

2-181. HOP SAVER REGISTER. (See figure 10-28, sheet 20.) The HOP saver register assembles a HOP constant; stores the HOP constant for approximately one Central Processor cycle and when commanded by the central processor program enables the transfer register to accept the HOP constant for storage in memory. The HOP constant will not be stored in memory unless a store instruction is given with an address of 7768 or 7778. The HOP constant register consists of a storage register and two serializers.

2-182. The storage register consists of 19 latches which are loaded with the HOP constant at A-14-Z time as follows:

1. Latches HIC1 through HIC8 are loaded from accumulator latches DLA 8, DLA 9, DLA 10, DLA 12, DLA 13, DLA 14, DLA 16, and DLA 17. These latches contain the instruction counter code.
2. Latches HDS1 through HDS4 are loaded with the data sector code contained in the data sector register.
3. Latches HIS1 through HIS4 are loaded with the instruction sector code contained in the instruction sector register.

4. Latches HDM1, HIM1, and HSYCL1 are loaded with the data module, instruction module, and instruction syllable codes respectively contained in the data module register, instruction module register, and instruction word syllable control logic.

The storage register latches are reset at the X time preceding the Y time at which they are loaded.

2-183. The outputs of the storage register latches are gated into the serializer which produces the HOPC1 signal by Z clock pulses during B and C times. The outputs of the sector and module registers and the instruction word syllable control logic are gated into the serializer which produces the HOPTL signal by Y clock pulses during B and C times. Figure 2-34 shows the order in which the information appears on the HOPC1 and HOPTL lines.

Bit Gate	HOPC1		HOPTL	
	Phase B	Phase C	Phase B	Phase C
BG1		HDM1		
BG2				
BG3	HIS1			
BG4	HIS2	HDM1	IS1	
BG5	HIS3		IS2	DM1
BG6	HIS4		IS3	
BG7	HSYLC1	HDS1	IS4	
BG8	HIC1	HDS2	SYLC1	DS1
BG9	HIC2	HDS3		DS2
BG10	HIC3	HDS4		DS3
BG11	HIC4			DS4
BG12	HIC5	HIM1		
BG13	HIC6			IM1
BG14	HIC7			

Figure 2-34. HOP Saver Serializer Outputs

2-184. INSTRUCTION COUNTER. The instruction address is incremented in the arithmetic element and stored in the unused portion of the accumulator register. The instruction address consists of nine bits but only eight bits are stored in the accumulator register. When the instruction address is transferred to the address register from the accumulator register to select an instruction, a "0" is forced into address register bit A9 position. The instruction address is increased by one each instruction time during normal operation. The instruction address is not increased after the commanded instruction is completed during computer single step (CST) operation. The instruction address is changed during a transfer operation; the instruction address currently stored in the accumulator-register is dropped and the transfer instruction operand address is loaded into the unused portion of the accumulator register. The instruction counter is actually part of the arithmetic element.

2-185. The instruction address is incremented by forcing a "1" into the C latch (figure 10-28, sheet 10) forcing the BOR latch to "0" during A time, and adding these two values, at the add-subtract circuit to the least significant digit of the instruction address when the bit arrives at A14. The subsequent address bits are also added with the C and BOR latch values but the C latch is reset when the first "1" of the instruction address reaches A14. (See arithmetic element for description of the add-subtract circuit.)

2-186. During normal operation, the C latch is reset when the first "0" of the instruction address is read from the accumulator register A14 latch. (A14 NOT equals "1" to reset the C latch.) The C latch operation differs during CST operation.

2-187. The instruction address is also prevented from increasing during a CST operation while CST equals "1". The C latch is repeatedly reset at A-2-X time when CST equals "1" to keep instruction address from increasing. To select the next programmed instruction during CST operation the externally controlled CST level becomes a "0" momentarily to allow the instruction address to increase by one.

2-188. The accumulator register stores the instruction address after the results of the arithmetic computations. The accumulator circulates the instruction address in the same manner that the arithmetic computations are circulated. The instruction address is loaded into the accumulator automatically by the add circuit and also, during transfer operations, by the transfer register serializer (TRS). The accumulator also supplies the transfer register with the instruction address to select programmed instructions.

2-189. During a transfer operation, the transfer instruction operand address is serialized through the transfer register and TRS latch to load ACC1 of the accumulator register. During this period, UTR equals "1" and UACCO equals "0" to enable TRS to load the new instruction address and inhibit the currently stored instruction address at ACCO. The ITR and UACCO levels originate at the same latch so can never equal "1" simultaneously. UACCO equals "1" during nontransfer operations to enable the current instruction address to be circulated through the accumulator. The AI1 latch of the accumulator register sequentially loads the TR1 latch of the transfer register with the instruction address during bit times C-14 through A-7. The instruction address, while stored in the transfer register, selects the next programmed instruction.

2-190. ARITHMETIC ELEMENT LOGIC CIRCUITS.

2-191. The Arithmetic Element performs the following general type of operations:

- a. Arithmetic (addition, subtraction and shifting).
- b. Logical extraction.
- c. Stores new operand and a new instruction counter (previously described).
- d. Modifies the stored instruction counter.

2-192. The Arithmetic Element consists of the following:

- a. Accumulator Control Circuits (Accum Control)
- b. Add/Subtract Circuit (A/S)
- c. Accumulator Register (Acc Reg)

The A/S Circuit and Acc Reg make up an accumulator which performs the arithmetic and logic operations and stores the results. The Acc Reg stores two pieces of data: the results of the arithmetic operation, called the stored operand, and the instruction counter.

2-193. The Accum Control Circuits provide timing and conditioning gates for the A/S and Acc Reg circuits. (The conditioning gates are instruction oriented.)

2-194. The A/S Circuit performs the following arithmetic and logical extraction operations:

Addition	(ADD)	}	Arithmetic
Subtraction	(SUB)		
Reverse-Subtraction	(RSU)		
Clear-and-Add	(CLA)		
And	(AND)	}	Logical Extraction
Exclusive Or	(XOR)		

In each of the preceding operations only the stored operand and the new operand are affected. During a CLA operation the stored operand is inhibited and the new operand enters the Acc Reg unaltered. Similarly, the input data from the input serializer and input data on the CIO data and PIO data lines enters through the A/S circuit and replaces the stored operand in the Acc Reg.

2-195. The Acc Reg is a circulating shift register which utilizes the A/S circuit to complete the loop. When no operations are called forth, the stored operand and instruction counter are continually circulated; the stored operand is unaltered and the instruction counter updated during each pass through the A/S circuit. A new instruction counter (required when performing one of the transfer operations) or a new instruction counter and HOP constant (which becomes the stored operand) may be entered directly into the Acc Reg when performing a HOP. Figure 2-35 shows the Acc Reg timing.

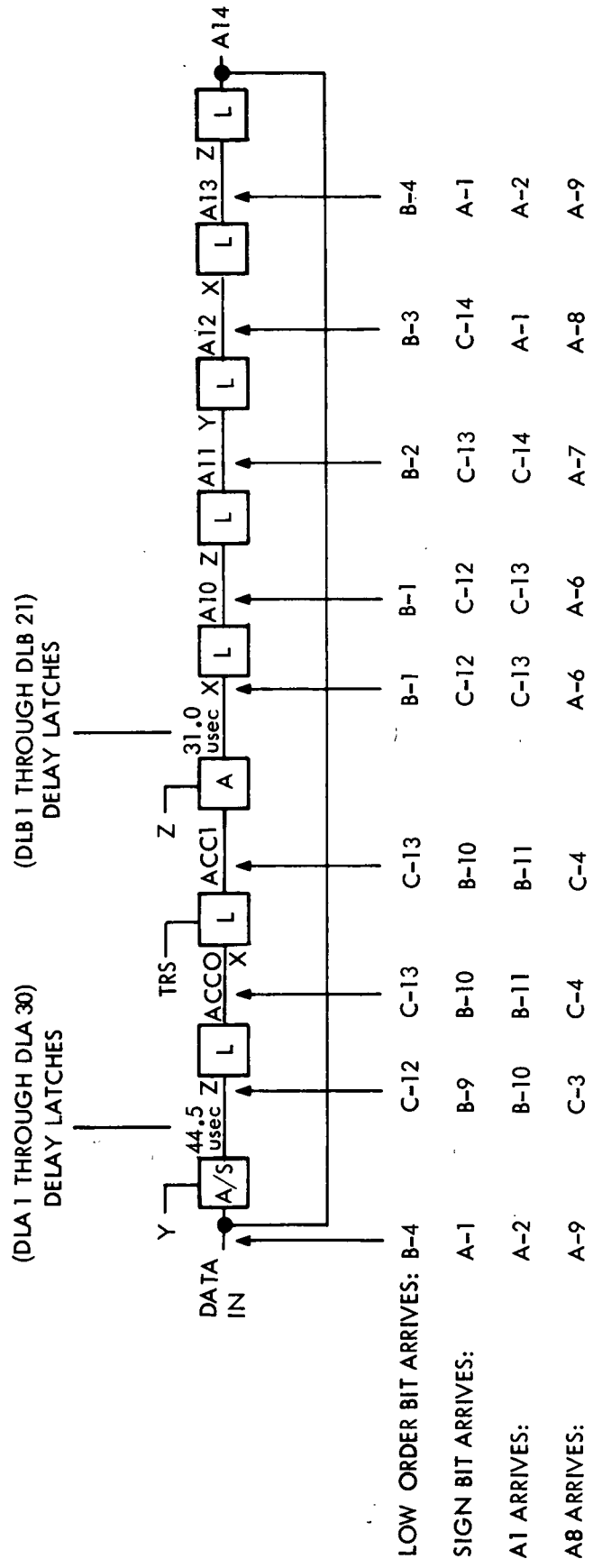


Figure 2-35. Accumulator Register Timing

2-196. ARITH CONTROL. The Arith Control circuits consist of the following three latches (figure 10-28, sheet 10):

- a. RAC
- b. ZER
- c. UTR-UACCO

2-197. RAC Latch. The RAC latch is set by the following instructions:

1. STO
2. TMI
3. TRA
4. PIO
5. SHF
6. CDS
7. CIO
8. TNZ
9. HOP
10. PRS 774₈ or 775₈

When the RAC latch is set, the contents of the Acc Reg are recirculated. The RAC latch is reset every A-14-Y time.

2-198. ZER Latch. The ZER latch stores the result of a check on the stored operand (ACCO). This check is necessary during TNZ and TMI operations. If the stored contents is not equal to zero or is negative (a "1" is present in ACCO), the latch is reset.

2-199. UTR-UACCO Latch. The latch may be set to UTR at B-10-Y time when the following instructions are set in the OP code register:

1. TNZ
2. TMI
3. HOP
4. TRA

Once the latch is set it cannot be reset until C-4-Y time. The period from B-10-Y time to C-4-Y time is the time when the instruction counter (A1 through A8) is available at the ACCO latch. During central processor single step, if the latch is set to UTR it is reset the following Z time.

2-200. A/S CIRCUIT. (See figure 10-28, sheets 11 and 12.) The A/S circuit consists of the BOR latch, C latch, and the A/S logic. This circuit performs the arithmetic operations and logical extractions previously mentioned.

2-201. BOR Latch. The BOR latch provides the one-bit storage needed to enter serial data from the transfer register (TRS), from the LVDCME or LVDAME (CIO DATA and PIO DATA), or from the input serializer (SCRS). The B latch also provides the entry point for the result during an RSU operation.

2-202. C Latch. The C latch provides a carry-borrow capability during arithmetic operations ADD, SUB, and RSU. The C latch remains set (or reset) as long as a carry-borrow (or no carry-borrow) is needed. The carry-borrow condition is always the result of the previous one bit summation.

2-203. A/S Logic. The A/S logic consists of the AND gates which are the inputs to the accumulator. These AND gates perform arithmetic computations.

2-204. ADDITION, SUBTRACTION, REVERSE SUBTRACTION, AND CLEAR AND ADD LOGIC DESCRIPTION. The A/S circuit (figure 2-36) serially adds or subtracts the contents of the accumulator (A14), the contents of the addressed memory location (B), and any carry (C) that develops from the previous bit summation. For each arithmetic operation the following equation is solved:

1. (ADD) $A/S = A14 + B + C$
2. (SUB) $A/S = A14 - (B + C)$
3. (RSU) $A/S = B - (A14 + C)$
4. (CLA) $A/S = B$

2-205. Figure 2-37 shows the truth table for all combinations of values of A14, B, and C required to solve equations 1. through 4. (Carry means the present value of carry that resulted from the last addition that will be used during this addition or subtraction; Next Carry means the value of the carry that will be used during the next addition or subtraction. The truth table shows that the values of A/S are the same for all addition and subtraction conditions of equations 1. through 4.

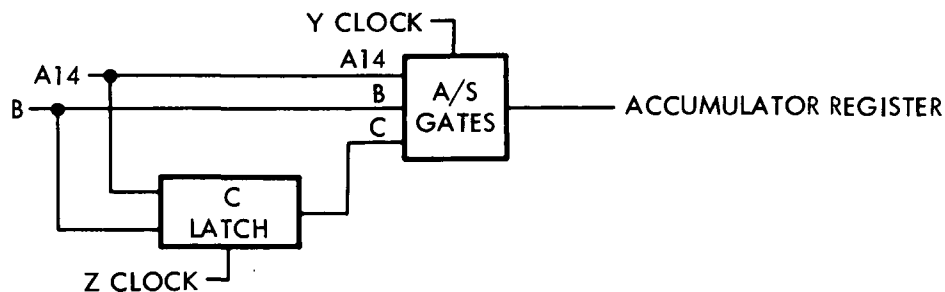


Figure 2-36. A/S Circuit, Simplified

			Sum or Remainder	ADD	SUB	RSU
AI4	B	Carry	A/S	Next Carry	Next Carry	Next Carry
0	0	0	0	0	0	0
1	0	0	1	0	0	1
0	1	0	1	0	1	0
1	1	0	0	1	0	0
0	0	1	1	0	1	1
1	0	1	0	1	0	1
0	1	1	0	1	1	0
1	1	1	1	1	1	1

Figure 2-37. A/S Circuit Truth Table

NOTE

Clear and Add (CLA) is a special addition when AI4 and C are both forced to zero.

2-206. AND gates A37 through A40 define when A/S is a "1". Since the truth table for A/S is the same for ADD, SUB, and RSU, these gates are applicable for all three arithmetic operations. The gate which makes A/S = 1 when B = 1 and AI4 and C = 0 also applies to CLA. Thus, gates A37 through A40 apply for all four arithmetic operations.

2-207. The carry latch is designed to change state according to the conditions established by the truth table (figure 2-37). The arrows indicate the values of B, AI4 and carry which cause the carry latch to change state for each arithmetic operation. For example: on the second line of the truth table, if the carry latch is reset (carry = 0) and a "1" (AI4) is subtracted (during RSU) from a "0" (B) a borrow shall be generated (Next carry = 1). OP code OP2VN and OP3V defines four operations. However, the only operation that is performed by the A/S circuit is RSU. Since AI4 = 1 and B = 0 are possible conditions when the contents of the accumulator is recirculating, RAC NOT is applied to prevent a carry from being generated during a recirculating condition. The carry latch will remain set until the carry condition no longer exists.

2-208. XOR LOGIC DESCRIPTION. During an XOR operation the contents of the Acc Reg (AI4) and the contents of the addressed memory location (B) are ORed exclusively bit-by-bit. The result is stored in the Acc Reg. The Add-Subtract Element is used to perform the operation. The following Boolean equation expresses the conditions required for an exclusive OR:

$$A/S = AI4 \cdot BN + AI4N \cdot B$$

The carry latch cannot be set during an XOR operation.

2-209. AND, LOGIC DESCRIPTION. During an AND operation the contents of the Accumulator (AI4) and the contents of the addressed memory location (B) are ANDed bit-by-bit. The result is stored in the Acc Reg. The A/S circuit is used to perform the operation. The following Boolean equation expresses the conditions required for an AND:

$$A/S = AI4 \cdot B$$

2-210. ACCUMULATOR REGISTER. The Acc Reg is a 3-phase, circulating shift register which stores the results of arithmetic and logical extraction operations and stores and updates the value of the instruction address. The Acc Reg, in conjunction with the A/S circuit and Accum Control, perform LSD and MSD shift operations.

2-211. SHIFT LOGIC DESCRIPTION. 12 shift operations can be commanded by the program:

LSD-1	MSD-1
LSD-2	MSD-2
LSD-3	MSD-3
LSD-4	MSD-4
LSD-5	MSD-5
LSD-6	MSD-6

2-212. LSD Shift. An LSD shift operation is performed during a STO operation if the value of the A7 bit of the operand address = "0". Bits A1 through A6 of the operand address denote the number of positions the data word is shifted. The value of the SIGN bit appears in all the MSD bit positions vacated by the shift.

2-213. The LSD shift operation is controlled by the RT SH and SIGN CTRL latch. The RT SH latch is set at B-4-X. The accumulator register circulation loop will then be shortened as specified by operand address bits A1 through A6. The SIGN CTRL latch is set at Y time of the bit time the RT SH latch is reset. This latch allows the value of the sign to be retained in the MSD positions.

2-214. MSD Shift. A MSD operation is performed during a STO operation if the value of the A7 bit of the operand address is "1". As in an LSD shift, bits A1 through A6 of the operand address denote the number of positions shifted. The value of the sign bit is lost and "0's" appear in the LSD bit positions vacated.

2-215. The LF SH latch controls the LSD shift operation. This latch is set at B-4-X time. This latch controls the clocks which shift the data word through the accumulator.

2-216. EXTERNAL CONTROL LOGIC CIRCUITS.

2-217. START-STOP CONTROL. The central processor program start-stop operation is controlled by two externally provided signals; (1) HALT 1 (figure 10-28, sheet 7); and (2) NCST (figure 10-28, sheet 69). The HALT 1 signal conditions the RUN latch to control the central processor program start-stop operation during normal operation. The CST (Central Processor Unit single step) signal conditions the CST gate to control the processor start-stop operation during computer single step operation.

2-218. RUN Latch. (See figure 10-28, sheet 25.) The RUN latch is set each A-6-Y time and remains set until the processor is externally commanded to halt; then HALT 1 equals "1" which resets the RUN latch at A-6-Z time. During the periods that the RUN latch is set the processor is permitted to operate as programmed. The processor program is initiated when the RUN latch becomes set by a simulated HOP to 000 instruction since the syllable latch, module, sector, OP code and address registers contain "0's". A HOP constant is stored in memory location 000 to start the processor program.

2-219. When the run latch is reset the processor program is halted in the following manner. The run latch disables memory during phase A, consequently instruction words cannot be read from memory. The transfer register and in turn the OP code and address registers will be loaded with "0's"; thus commanding a HOP to 000. When the HOP code is loaded into the OP code register the HOP latch becomes set. When both HOP and RUN equal "1" memory operation is also disabled during phases B and C. The reset run latch prevents the transfer of the instruction address into the transfer register; consequently the HOP to 000 command is continuously recycled.

2-220. The RUN signal enables the transfer register to be loaded from external sources via the DIN line. The DIN line is used during a memory load or verify operation. During memory load or verification, CLA and STO commands are loaded into the transfer during instruction time via the DIN line. During execution of these instructions memory operation is enabled during phases B and C but remains disabled during phase A. During data word time of STO commands, data is loaded into the transfer register via the DIN line for storage in memory. The RUN signal clears the transfer register at the completion of these command operations.

2-221. CST Gate. The output of the CST latch (figure 10-28, sheet 7) is called the CST gate. The CST gate inverts the externally provided CST signal to halt the processor program during single step operation. The CST signal forces a transfer nonzero (TNZ) operation code into the OP code register, prevents the instruction counter from stepping, and prevents the operand address from transferring from the transfer register into the instruction counter if the accumulator contains a nonzero number. Since the instruction counter is unable to increase and transfer is inhibited, the TNZ operation is continuously repeated halting the processor program. When the CST gate is disabled the next programmed instruction is performed.

2-222. The use of the CST feature when the PTC is used as a single unit or part of a system has been described earlier. The following is a list of the latches involved in the CST operation, presented with a brief description of each:

1. SET CST latch (figure 10-28, sheet 69) — is a primary latch which enables switch CST (SW CST) and SET CST gates to generate a data display compare (DD COMP) signal.
2. Address Compare latch (ADR COMP) — forces an address compare to take place during a CST operation.
3. DD COMP latch — enables CST operation under control of the ADR COMP level.
4. CST latch (figure 10-28, sheet 7) — generates the CST gate which is used throughout the processor to induce CST operation.
5. CC TWO latch (figure 10-28, sheet 69) — disables CST operation for two cycles (word times). The CC TWO latch is set by an interrupt.
6. First Compare (FIRST COMP) latch — is set when a like comparison of address switches and processor address is effected during data display and CST mode of operation. The latch remains set to force an address compare to take place during a subsequent CST operation.
7. ACP CST latch — stores the enabling level of the ACN CST line. The latch is disabled when (1) ACN CST is removed for more than one cycle if an ACG ACTSS is present, or (2) if ACN CST is removed when ACG ACISS is not present.
8. C STORED latch (figure 10-28, sheet 7) — remembers that a CST operation had been initiated. This latch is used during interrupt of a CST mode and during manual operation of the PTC.
9. ST ADV latch — stores a CST advance signal.
10. MAN CST latch (figure 10-28, sheet 69) — follows the MAN CST SW and removes the switch bounce effects.
11. SS HOLD INH latch — disables ACP CST latch if the data display mode switch is in address hold or single-step. If the mode switch is in either of the two positions, the latch is set by the first CST ADV and remains set for the duration of the switched position.
12. SS HOLD latch — is set by the first address compare when the data display switch is in address hold or single-step and remains set for the duration of the switched position. The output of this latch is one of the signals which generate a PTC CST signal for I/O usage.
13. C2-C11 latch — is used to cover the time when ACG ACISS is disabled and ACN CST is set.

2-223. PROCESSOR INTERRUPTS. (See figure 10-28, sheets 31, 32 and 33.) The PTC processes 16 interrupt signals, 15 from external equipment and one (INTRPT 16) from manually activating the interrupt 16 switch on the processor display panel. The 16 interrupts are stored in a 16-bit interrupt register until interrupt processing is complete. The processor reads the interrupt register with a programmed CIO 115 instruction.

2-224. The receipt of an interrupt causes the forced selection of a residual memory sector location (shown on figure 2-38), unless the recognition and subsequent processing of the interrupts (1 through 15) is inhibited. Automatic or manual inhibit is effected by setting any of the interrupt inhibit bits in the 15-bit inhibit register. Manual inhibit is accomplished by activating the inhibit control switch (INH CTRL SW) on the processor display panel. This places the inhibit register under manual control by setting all bit positions of the register. Individual inhibit bits are manually inhibited by pressing the desired inhibit bit switch, thus allowing the processing of only the specified interrupt. Automatic inhibit is accomplished first by turning off the inhibit switches on the display panel. The inhibit register can then be loaded by a CIO 000 and accumulator bits 25 through 11 (for inhibit bits 1 through 15) respectively. The inhibits are reset with a CIO 004 and accumulator bits 25 through 11 for interrupts 1 through 15 respectively. There is no provision for inhibiting interrupt 16.

2-225. MEMORY LOADER/DATA DISPLAY.

2-226. The Memory Loader/Data Display contains the circuits necessary to perform the memory load - memory verify and data display functions. (See figure 10-3, sheet 3.) The majority of these circuits are used in both the memory load - memory verify and data display functions. Consequently although this discussion treats the two functions separately only one circuit description is included.

LVDC/ DA-PTC Interrupt	Forced Residual Location Address (8)	Location Contents	Terminating CIO
1	400	Initiate Interrupt No. 1 Subroutine	010
2	401	Initiate Interrupt No. 2 Subroutine	014
3	402	Initiate Interrupt No. 3 Subroutine	020
4	403	Initiate Interrupt No. 4 Subroutine	024
5	404	Initiate Interrupt No. 5 Subroutine	030
6	405	Initiate Interrupt No. 6 Subroutine	034
7	406	Initiate Interrupt No. 7 Subroutine	040
8	407	Initiate Interrupt No. 8 Subroutine	044
9	408	Initiate Interrupt No. 9 Subroutine	050
10	409	Initiate Interrupt No. 10 Subroutine	054
11	410	Initiate Interrupt No. 11 Subroutine	060
12	411	Initiate Interrupt No. 12 Subroutine	064
13	412	Initiate Interrupt No. 13 Subroutine	070
14	413	Initiate Interrupt No. 14 Subroutine	074
15	414	Initiate Interrupt No. 15 Subroutine	100
16	417	Initiate Interrupt No. 16 Subroutine	104

Figure 2-38. Forced Addresses Caused by Interrupts

2-227. MEMORY LOAD - MEMORY VERIFY.

2-228. The memory load - memory verify function is selected (1) when PTC DC power is sequenced on or off and (2) under control of the ML/DD pushbutton. The central processor memory is loaded and/or verified when this function is selected. The contents of the tape reader register and the display registers are displayed by corresponding COMMAND and COMPUTER lamps respectively. These lamps are used in conjunction with the ERROR lamps for failure analysis. The memory load - memory verify function is divided into three operations as follows:

1. Tape reader control.
2. Tape reader register loading.
3. Data transfer.

2-229. TAPE READER CONTROL. The tape reader is controlled by the TAPE READER CONTROL and AUTO/MANUAL pushbuttons. The PWR ON/PWR OFF pushbutton turns the tape reader power on or off. Power is also removed from the tape reader if the tape reader timing circuit malfunctions. The direction of tape flow is controlled by the FORWARD/REVERSE pushbutton (FORWARD is a clockwise flow and REVERSE is a counterclockwise flow). The INHIBIT READER CONTROL pushbutton turns the tape spooler power on or off (this permits manual indexing of the tape). The tape reader can be operated in the AUTO or MANUAL mode.

2-230. The AUTO mode which is used for reading the tape is selected when the AUTO/MANUAL pushbutton is in the AUTO position. The tape is read in the FORWARD mode; the REVERSE mode is used for tape rewind. The tape reader is started by pressing the START pushbutton and continues to run until the stop pushbutton is pressed, an error is detected, or the last tape word is read (tape address of 00001). When the last tape word is read the tape automatically stops and rewinds to the beginning of the first tape word (tape address of 11111).

2-231. The MANUAL mode which is used for loading the tape on the tape spooler and for initially positioning the tape is selected when the AUTO/MANUAL pushbutton is in the MANUAL position. If the leader portion of the tape (sprocket holes only) is under the tape reader read head, the tape advances to the beginning of the first tape word when the MANUAL ADVANCE TAPE pushbutton is pressed. When the information portion of the tape is under the tape reader read head the tape advances one word every time the MANUAL ADVANCE TAPE pushbutton is pressed.

2-232. TAPE READER REGISTER LOADING. The tape reader register can be loaded with information generated automatically by the tape reader or manually with switches.

2-233. Automatic Tape Reader Register Loading. In the AUTO mode the tape reader register is loaded with information stored on the memory load and verify tape. This tape is comprised of eight channels and a sprocket hole (see figure 2-39). A tape word consists of nine tape characters each of which contains eight bit locations. The value of each bit will be a "1" if a hole is punched in the tape and a "0" if the tape is blank.

2-234. Channel 7 (Sequence Channel) always contains a "0" in tape characters 1 through 8 and a "1" in tape character 9. Channel 8 (Parity Channel) contains a "1" in any tape character that contains an even number of "1's" in channels 1 through 7. SYL1 PB will be a "1" if data bit locations SIGN and B1 through B12 contain an even number of "1's" and SYL0 PB will be a "1" if data bit locations B13 through B25 contain an even number of "1's".

				(Parity Channel)						Channel 8
				(Sequence Channel)					Always A one	Channel 7
DS1		OA9	OA3	B3	B9	B15	B21	SYL1 PB	Channel 6	
DS2	OP1	OA8	OA2	B4	B10	B16	B22	TAADR 5	Channel 5	
DS3	OP2	OA7	OA1	B5	B11	B17	B23	TAADR 4	Channel 4	
									Sprocket Holes	
DS4	OP3	OA6	SIGN	B6	B12	B18	B24	TAADR 3	Channel 3	
MM1	OP4	OA5	B1	B7	B13	B19	B25	TAADR 2	Channel 2	
		OA4	B2	B8	B14	B20	SYL0 PB	TAADR 1	Channel 1	
1	2	3	4	5	6	7	8	9	Tape Character	

NOTE

The tape address bits (TAADR 1 through TAADR 5) are used for automatic control of the tape reader and data transfer control circuits.

Figure 2-39. Memory Load and Verify Tape Format

2-235. The tape is read one tape character at a time at a rate of 500 characters per second until a complete tape word is read. The logic value of each bit located in channels 1 through 6 except SYL0 PB and SYL1 PB is stored in a corresponding position of the tape reader register. Parity and sequence checks are performed on each tape character and if an error is detected the tape stops. If any other error is detected the tape stops on tape character 9. When no errors are detected the next word is read. This process is continued until the complete tape is read.

2-236. Manual Tape Reader Register Loading. In the MANUAL mode the tape reader register is loaded with information generated by the DATA ADDRESS, DATA, and TAPE ADDRESS pushbuttons. Pressing a DATA ADDRESS or DATA pushbutton will complement the value stored in the corresponding position of the tape reader register.

These positions of the tape reader register are also cleared when the COMMAND DISPLAY RESET pushbutton is pressed. Pressing a TAPE ADDRESS pushbutton will complement the value stored in the corresponding position of the tape reader register providing the ADV CTR/SEL ADR pushbutton is in the SEL ADR position.

2-237. DATA TRANSFER. The data address and data information stored in the tape reader register is serialized at the central processor timing rate. This information is then sent to the central processor unless:

1. A serial parity error is detected in the AUTO or MANUAL REPEAT mode.
2. The VERIFY ONLY pushbutton is in the VERIFY ONLY position during a load operation.
3. The VERIFY ONLY pushbutton is in the VERIFY ONLY position and the tape address is 00010.
4. An error generated during the previous load or verify operation has not been reset.
5. The data information is not transferred during a verify operation or when a data address compare error occurs.

2-238. The central processor after receiving the data address information sends this information back to the memory loader. Correct data address transfer is then substantiated by comparing the data address information generated by the memory loader with the data address information received from the central processor. The current central processor sector, module, OP code, and operand address bit values contained in the data address information are stored in corresponding display register positions.

2-239. During a load operation (OP code 1011) the data information is sent to the central processor and loaded into the memory location specified by the sector, syllable, module, and operand address bit values. During a verify operation (OP code 1111) the data information contained in the memory location specified by the sector, module, and operand address bit values is sent to the memory loader. A correct memory load is verified by comparing the data information generated by the memory loader with the data information received from the central processor. The current data bit values contained in the data information are stored in corresponding data display shift register positions.

2-240. Data transfer occurs in either the AUTO or MANUAL mode. These two modes of transferring data are discussed in the following paragraphs.

2-241. Automatic Data Transfer. In the AUTO mode data is continuously sent to the central processor as long as the tape is running forward and an error is not detected. Since the data transfer is the same for each tape word, only the transfer of information for one tape word is discussed. Because the tape reader timing rate is much slower than the central processor timing rate, six central processor cycles (cycle 0 through cycle 5) are required to complete one load or verify operation. The transfer of information occurs while the tape is moving from character nine of the tape word being transferred to character one of the next tape word.

2-242. The tape reader register is loaded as tape characters one through nine are read (cycle 0). During B and C times of cycle 1 the serial parity check is performed. Data address information is sent to the central processor on the DIN line during cycles 2 and 3.

The sector and module bit values are transferred during B time of cycle 2 (DSMSO). The OP code and operand address bit values are transferred during C time of cycle 2 and A time of cycle 3 (INSSO).

2-243. Data address information is serially transferred from the central processor to the memory loader on the TRS and HOPTL lines and parallel transferred on the OP1 through OP4 and A1 through A9 lines. Sector and module bit values are gated into the sector-syllable-module buffer register. This data is then parallel transferred to the sector-syllable-module display register. OP code and operand address bit values are parallel transferred into the address buffer register and from there parallel transferred to the instruction display register.

2-244. Correct data address transfer to the central processor is substantiated during cycles 2 and 3 by performing two compares. Sector and module bit values appearing on the DSMSO line are compared with corresponding bit values appearing on (1) the TRS line during C time of cycle 2 and (2) the HOPTL line during C time of cycle 3. OP code and operand address bit values stored in the tape reader register are compared with corresponding bit values received from the central processor on the OP1 through OP4 and A1 through A9 lines. Several other compares are performed to substantiate the correct internal transfer of data between the buffer and display registers.

2-245. Data information is sent to the central processor on the DIN line during a load operation (DTSO). Data bit values 12 through 25 are transferred during B time of cycle 3 and data bit values SIGN and 1 through 11 are transferred during C time of cycle 3. During a verify operation data information is received from the central processor on the TRS and AI3 lines. TRS data is stored in the data display shift register if a TRS compare error occurs; AI3 data is stored in the data display shift register if an AI3 compare error occurs.

2-246. A correct memory load is verified by performing three compares during cycles 3, 4, and 5. The data bit values appearing on the DTSO line are delayed two bit times (2BDDTSO) and compared with the data bit values appearing on the TRS line during B and C times of cycle 3 and A time of cycle 4. The data bit values appearing on the DIN line are also compared with the data bit values appearing on the AI3 line during B and C times of cycle 4 and A time of cycle 5. The tape reader register data syllable 0 and syllable 1 parity bit values are compared with the parity bit values generated by the central processor memory circuits.

2-247. Manual Data Transfer. In the manual mode data transfer is controlled by the REPEAT/REPEAT and ADDRESS COMPUTER pushbuttons. When the REPEAT/REPEAT pushbutton is in the REPEAT position data transfer is accomplished every time the ADDRESS COMPUTER pushbutton is pressed. When a load operation is selected the data information is loaded into the central processor memory and then the memory load is automatically verified.

2-248. When the REPEAT/REPEAT pushbutton is in the REPEAT position data transfer is accomplished continuously. Load and verify operations are alternately performed as long as the REPEAT mode is maintained.

2-249. The timing for the transfer of data address and data information between the memory loader and the central processor is the same as in the AUTO mode. The compares performed are also the same as in the AUTO mode. The contents of the display registers are cleared when the COMPTR DISPLAY RESET pushbutton is pressed.

2-250. DATA DISPLAY.

2-251. The data display function is selected in the MANUAL mode under control of the ML/DD pushbutton. When this function is selected central processor data associated with a data address or instruction address can be monitored. The data display function is divided into two operations as follows:

1. Data selection.
2. Data storage.

2-252. DATA SELECTION. The data selection operation is initiated as follows:

1. When the central processor is placed in the single step mode of operation.
2. Each time the program is advanced one instruction during the single step mode of operation.
3. When an address compare occurs.

2-253. The single step and advance features are discussed under the central processor. An address compare occurs when an instruction or data address manually selected with switches corresponds with the central processor memory address selected.

2-254. Address Compare. Information generated by the INSTRUCTION ADDRESS or DATA ADDRESS pushbuttons is loaded into the tape reader register. The instruction address and data address positions of the tape reader register are displayed by corresponding COMMAND lamps. These positions are cleared when the COMMAND DISPLAY RESET pushbutton is actuated. Pressing an INSTRUCTION ADDRESS or DATA ADDRESS pushbutton complements the value stored in the corresponding position of the tape reader register.

2-255. The data address and instruction address bit values stored in the tape reader register are then compared with the current central processor data address or instruction address bit values. An address compare occurs on an instruction address when the ADDRESS COMPARE pushbutton is in the INS position. When this pushbutton is in the DATA position an address compare occurs on the data address.

2-256. An address compare occurs everytime the tape reader register and central processor address bit values correspond when the MODE CONTROL switch is in the DISPLAY-REPEAT position. When this switch is in the DISPLAY SINGLE position an address compare occurs the first time the tape reader register and central processor address bit values correspond after the COMPTR DISPLAY RESET pushbutton is actuated.

2-257. DATA STORAGE. Current central processor sector, syllable, and module bit values appearing on the TRS or HOPTL lines are gated into the sector-syllable-module buffer register (SSMBR). TRS information is gated into the SSMBR for a HOP instruction. HOPTL information is gated into the SSMBR for any other instruction. When the data selection operation is initiated the contents of the SSMBR are then parallel transferred into the sector-syllable-module display register.

2-258. Current central processor OP code and address bit values appearing on the OP1 through OP4 and A1 through A9 lines are parallel transferred into the address shift register. The address bit values (A1 through A8) are transferred at A-11 time; the OP code (OP1 through OP4) and operand address (OA1 through OA9) bit values are transferred at B-12 time. The address bit values and the OP code and operand address bit values are then parallel transferred into the instruction address display and instruction display registers respectively when the data selection operation is initiated.

2-259. The initiation of the data selection operation also serially gates TRS or AI3 information selected by the DISPLAY SELECT switch into the data display shift register. AI3-IA information appears in positions 1 through 8. All other information appears in positions SIGN and 1 through 25.

2-260. The contents of the display registers are displayed by the corresponding COMPUTER lamps. When the LVDCME forces the PTC into the single step mode of operation the display registers are cleared. This ensures that the data display is blank until the program is advanced. The display registers are also cleared when the COMPTR DISPLAY RESET pushbutton is actuated.

2-261. MEMORY LOADER/DATA DISPLAY CIRCUIT DESCRIPTIONS.

2-262. TAPE READER TIMING AND CONTROL CIRCUITS. The tape reader timing and control circuits provide the necessary signals to control the tape reader and to load information into the tape reader register. The breakdown of the tape reader timing and control circuits is shown on figure 2-40.

2-263. Tape Reader Start, Stop Control Logic. Automatic and manual control of the tape reader is accomplished by the tape reader start, stop control logic (see figure 10-28, sheets 49 and 50). The tape is transported in the reverse direction when the DRIVE LEFT signal is a "0" and in the forward direction when the DRIVE RIGHT signal is a "0". When both DRIVE LEFT and DRIVE RIGHT signals are "1's" the tape is stopped.

2-264. DRIVE LEFT and DRIVE RIGHT are two outputs of the run tratch. The three states of this tratch are as follows:

<u>State</u>	<u>RUN</u>	<u>DRIVE LEFT</u>	<u>DRIVE RIGHT</u>
1	"0"	"1"	"1"
2	"1"	"0"	"1"
3	"1"	"1"	"0"

The run tratch is forced to its first state by any one of the following: a STOP signal; a sequence error (SEQ ERR 2 RST INH) while the tape reader is in the FORWARD AUTO mode; or a tape reader clock pulse error (TRCP ERR). The run tratch is forced to its second and third states by R and F START signals respectively. When the PTC is in the SELF CHECK mode and the FREE RUN READER pushbutton is in the FREE RUN READER position the run tratch logic is bypassed. DRIVE RIGHT is now forced to a "0" if the FORWARD mode is selected.

2-265. The STOP signal is the set output of a latch (stop latch) which is set as follows:

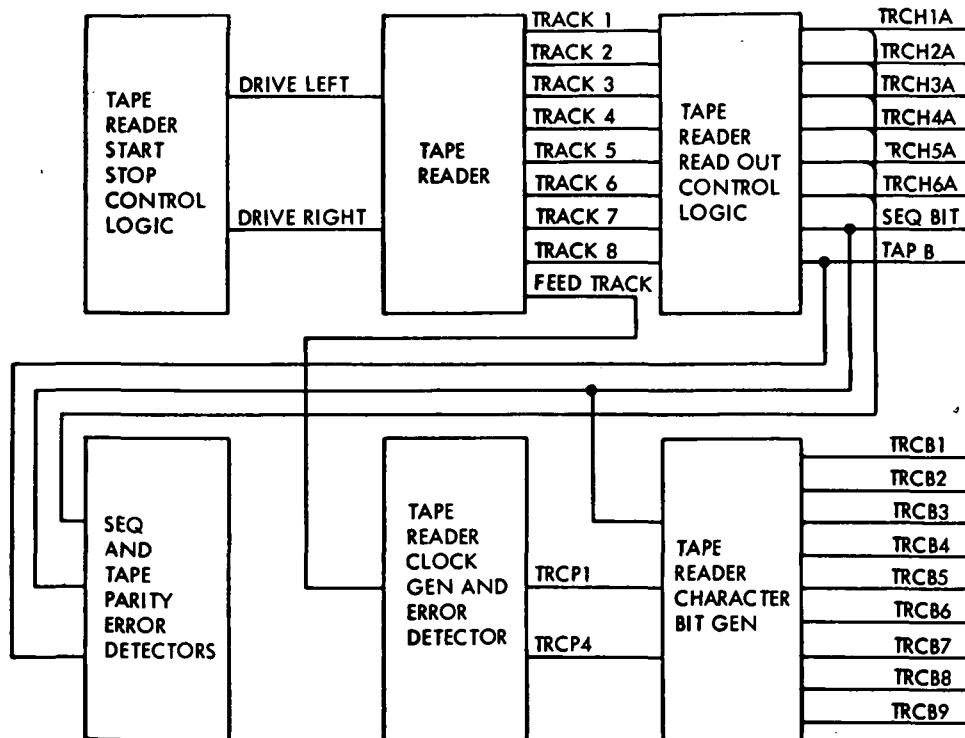
1. By pressing the STOP pushbutton.

2. By a tape address of 11111 when the tape reader is in the AUTO REVERSE mode.
3. By an EOP signal which is generated by a tape address of 00001 when the tape reader is in the AUTO FORWARD mode or by a FREE RUN SS signal.
4. By the first sequence bit sensed when the tape reader is in the MANUAL mode and the SKIP FIRST latch is reset.
5. By an error stop reader signal (ERR NOT INV) when the tape reader is in the AUTO FORWARD mode and a sequence bit is sensed (SAM ERRS).

The stop latch is reset by an error reset signal or at TRCP4 time. When the direction of tape flow is changed, the SKIP FIRST latch is set by the first and reset by the second sequence bit sensed. This insures that the tape will advance one word before the stop latch is set. The error stop reader signal is normally generated by a parity, tape, or compare error.

2-266. The R START signal is generated as follows:

1. By pressing the MANUAL ADVANCE TAPE pushbutton when the tape reader is in the MANUAL REVERSE mode.
2. By pressing the START pushbutton when the AUTO REVERSE, and ML modes are selected and KWAIN NOT A is a "1".
3. By an automatic reverse start signal (AUTO R START) generated by an EOP.



NOTE: DATA FLOW IS FOR THE AUTO MODE ONLY.

Figure 2-40. Tape Reader Timing and Control Circuits

The F START signal is generated as follows:

1. By pressing the MANUAL ADVANCE TAPE pushbutton when the tape reader is in the MANUAL FORWARD mode.
2. By pressing the START pushbutton when the AUTO FORWARD, and ML modes are selected KWAIN NOT A IS a "1", and the error latches are all reset.

When the tape reader is in the FREE RUN SS mode the R and F START levels are forced to "0's".

2-267. A KWAIN signal is generated (KWAIN NOT A IS A "0") as follows:

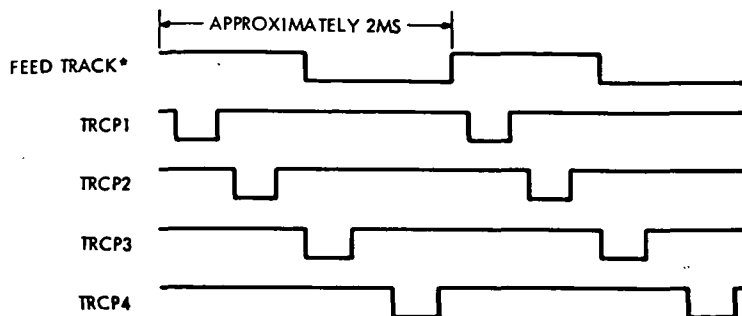
1. During the time prior to the sensing of the first sequence bit when PTC power is turned on.
2. During the time prior to the sensing of the first sequence bit after a sequence error 2 is generated.
3. If the control latches in the tape reader character bit generator stabilize in the wrong configuration when the tape reader stops.

2-268. Tape Reader Clock Generator. The tape reader clock generator generates four timing pulses (TRCP1, TRCP2, TRCP3, and TRCP4) which are used throughout the tape reader control circuitry. (See figure 10-28, sheet 46.) The tape reader clock generator is triggered as follows:

1. By the tape sprocket holes, when the tape reader is running. (See figure 2-41 for timing.)
2. By pressing any one of the INSTRUCTION ADDRESS, DATA ADDRESS, DATA, or TAPE ADDRESS pushbuttons when the tape reader is stopped and in the MANUAL mode.
3. By a 500 CPS multivibrator oscillator when the PTC is in the SELF CHECK and FREE RUN SS modes.

2-269. Tape Reader Clock Pulse Error Detector. Tape reader, clock pulse errors are stored in a latch which provides outputs TRCP ERR and TRCP ERR NOT (see figure 10-28, sheet 46.) A tape reader clock pulse error is generated as follows:

1. If a missing tape reader clock pulse is detected.
2. If an overlap occurs between adjacent tape reader clock pulses.
3. When an INSTRUCTION ADDRESS SECTOR IS1 through IS4 pushbutton is pressed and the tape reader is in the FREE RUN SS mode.
4. If the delay between tape reader clock pulse "1's" exceeds 30 MS when the tape reader is in the AUTO mode and running.
5. For the duration of the time an INSTRUCTION ADDRESS, DATA ADDRESS, DATA, or TAPE ADDRESS pushbutton is pressed when the tape reader is stopped in the MANUAL mode, and the PTC is not in the FREE RUN SS mode.



*FEED TRACK IS AN UP LEVEL FOR THE SPROCKET HOLE

Figure 2-41. Tape Reader Clock Pulse Timing

2-270. Tape Reader Character Bit Generator. The tape reader character bit generator generates nine bits (TRCB1 through TRCB9). (See figure 10-28, sheet 47.) These nine bits identify a specific tape character of a tape reader word. The tape reader character bits are generated automatically or manually with switches.

2-271. Automatic generation of the tape reader character bits occurs when the tape reader is in the AUTO FORWARD mode, or the PTC is in the FREE RUN SS mode. The configuration of 11 control latches determines the tape reader character bit timing. (See figure 2-42.) The outputs of these control latches are applied to AND circuits to product the tape reader character bits. Automatic generation of TRCB9 is also accomplished whenever a sequence bit is sensed and the tape reader is not in either the FREE RUN SS, or the AUTO FORWARD mode.

2-272. Tape reader character bits are generated manually by the DATA ADDRESS, DATA, or TAPE ADDRESS pushbuttons when the tape reader is stopped and in the MANUAL mode. The tape reader character bit affected will correspond to the tape character containing the information that the pushbutton is simulating. Each latch is set for the duration of the time that one of the group of pushbuttons feeding it is pressed. TRCB9 is forced to a "0" when the ADV CTR/SEL ADR pushbutton is in the ADV CTR position.

2-273. Tape Reader Read Out Control Logic. The tape reader read out control logic converts inputs from the tape reader, or from switches to eight output signals (TRCH1A through TRCH6A, SEQ BIT, and TAP B). (See figure 10-28, sheet 48.)

2-274. In the AUTO mode, tape reader information is sent to the tape reader read out control logic on eight lines (TRACK 1 through TRACK 8). These lines correspond to the eight tape channels. The inverses of TRACK 1 through TRACK 6 are sampled at TRCP1 time to determine the logic values of TRCH1A through TRCH6A, respectively. The inverses of TRACK 7 and TRACK 8 respectively determine the logic values of SEQ BIT and TAP B. The SEQ BIT and TAP B signals are forced to "0's" when the tape reader is not running.

2-275. In the MANUAL mode, pressing a DATA ADDRESS, DATA, or TAPE ADDRESS pushbutton will set one of six latches (LACH 1 through LACH 6) which correspond to tape channels 1 through 6. The set outputs of these latches are ANDed with the outputs of a control latch (MANCH latch) to determine the logic values of TRCH1A through TRCH6A. The MANCH latch is set when the tape reader register position that corresponds to the pushbutton pressed contains a "0".

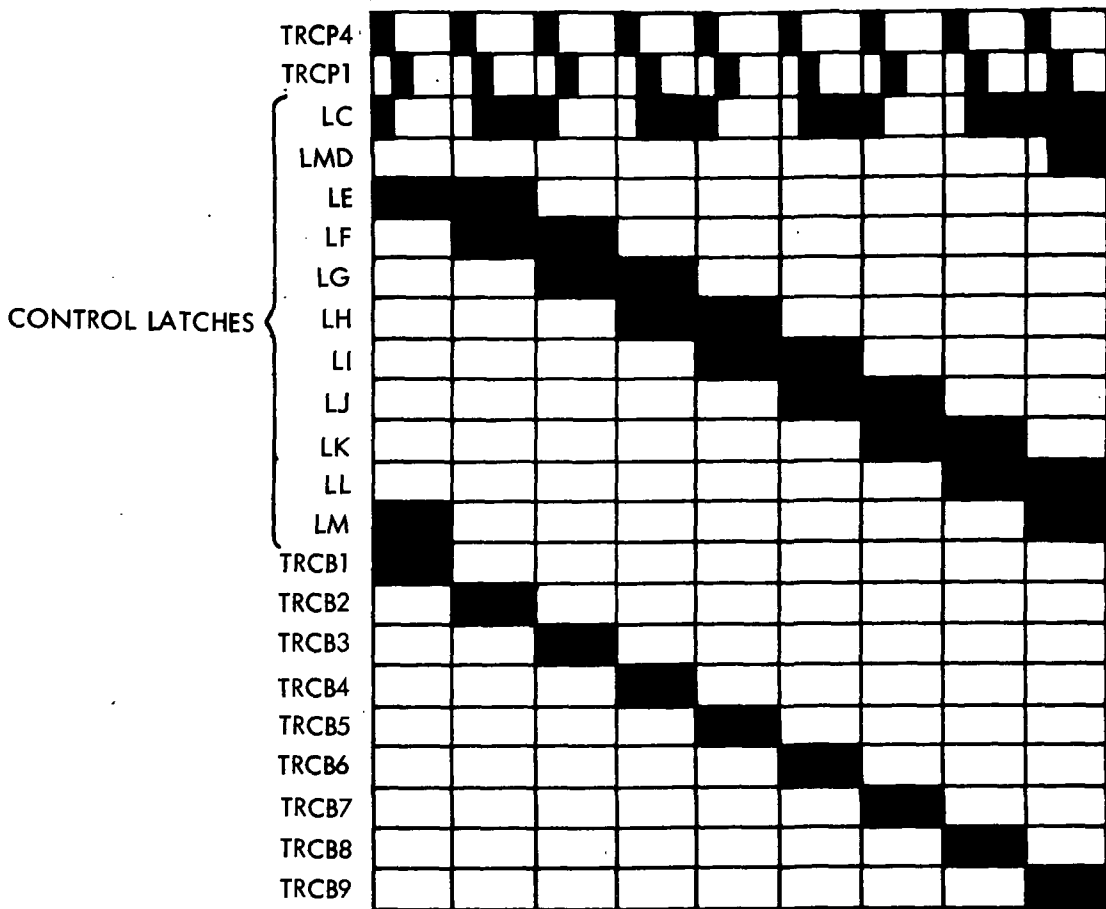


Figure 2-42. Tape Reader Character Bit Generator Timing

2-276. Sequence Error Detectors. Two sequence errors (SE1 and SE2) are generated if an error occurs when the tape reader is running forward. (See figure 10-28, sheet 49.) SE1 and SE2 are the set outputs of two latches which are set by SEQ BIT and TRCB9 NOT or SEQ BIT NOT and TRCB9 signals.

2-277. Tape Parity Error Detector. The tape parity error detector performs an odd parity check on each tape character when the tape reader is in the AUTO mode and running forward. (See figure 10-28, sheet 48.) A tape parity error is generated if an even number of "1" bits are detected. Tape parity errors are stored in a latch which produces an output TPE ERR NOT.

2-278. MODE SELECTION CIRCUITS. The mode selection circuits generate eight signals (AUTO, MAN A, DD A, DD NOT A, ML A, ML NOT A, FWD A, and RVS A) which control the mode of operation of the Memory Loader/Data Display and tape reader. (See figure 10-28, sheet 49 and 50.) The configuration of these signals can only be changed when the tape reader is stopped.

2-279. Auto and MAN A are the outputs of a latch, which is alternately set or reset when the AUTO/MANUAL pushbutton is actuated. DD A and ML A are the outputs of another latch which is alternately set or reset when the ML/DD pushbutton is pressed and the MANUAL mode is selected. When the AUTO mode is selected DD A is forced to a "0". The ML mode is forced when PTC DC power is sequenced on or off.

2-280. FWD A and RVS A are the outputs of binary counter which is complemented everytime the FORWARD/REVERSE pushbutton is actuated. The FORWARD mode is forced until the first sequence bit is sensed after PTC power is sequenced on. The REVERSE mode is forced when an AUTO R START signal is generated.

2-281. TAPE READER REGISTER. The tape reader register is a 63 position latch register that stores input information to the Memory Loader/Data Display. (See figure 10-28, sheets 51 through 58.) The contents of the tape reader register are displayed by corresponding COMMAND display and TAPE ADDRESS indicator lamps. The tape reader register is cleared except for the tape address positions by pressing the COMMAND DISPLAY RESET pushbutton.

2-282. Tape information or information generated by the DATA ADDRESS, DATA or TAPE ADDRESS pushbuttons is stored in 49 positions of the tape reader register. A specific bit of information is identified by sampling the tape reader channel containing this bit at the corresponding tape reader character bit time. The logic value of this bit is then stored in a latch. Additional control of the latch which stores the logic value of the OP3 bit is provided by two signals (STROP3 and RTOP3). This latch is set by a STROP3 signal and reset by a RTOP3 signal.

2-283. The remaining 14 positions of the tape reader register are used to store the instruction address information. The logic value of two control signals (LAST A and LARE A) determine whether a "1" or "0" is stored in these positions. The latch assigned to the INSTRUCTION ADDRESS pushbutton pressed will set if LAST A is a "1" and reset if LARE A is a "1". LAST A and LARE A are respectively identical to the set and reset outputs of a latch (LACH 7) when the tape reader is in the MANUAL mode. This latch is set when the tape reader register position that corresponds to the pushbutton pressed contains a "0".

2-284. TAPE READER REGISTER PARITY DETECTOR. The tape reader register parity detector generates a parity bit (SERIALIZER PARITY BIT) when the data address, instruction address, and data stored in the tape reader register contains an even number of "1's". (See figure 10-28, sheet 60.) Figure 2-43 shows the tape reader register parity detector which consists of four binary counters and a parity bit generator.

2-285. The configuration of the four binary counters (identified as "A", "B", "C", and "D" for this discussion) is determined by the number of "1's" contained in the information feeding them. In the AUTO mode the configuration of "B" is not changed. "A" which is set at the beginning of each tape word is complemented at tape reader character bit times 1, 2, 3, and 4 if the part of the data address located in these tape characters contain an odd number of "1's". "C" and "D" are respectively set by the presence or cleared by the absence of tape SYL 0 and SYL 1 parity bits.

2-286. In the MANUAL mode the binary counters are initially set when the COMMAND DISPLAY RESET pushbutton is pressed. Each counter is then complemented everytime one of the group of pushbuttons feeding it is pressed. "A" is also complemented everytime a CHANGE TROP3 signal is generated.

2-287. The outputs of the four binary counters are applied to a parity bit generator which produces outputs SER PB and SER PB NOT. SER PB and SER PB NOT are forced to a "1" and a "0" respectively when none, two or four of the binary counters are set. Any other condition will force SER PB and SER PB NOT respectively to a "0" and a "1".

2-288. TAPE READER SERIALIZER. The tape reader serializer receives parallel information from the tape reader register and transforms this information into serial

data on three lines. (See figure 10-28, sheet 59.) Data sector and module information appears on the DSMSO line, instruction information appears on the INSSO line, and data informations appears on the DTSO line.

2-289. The tape reader register data is gated through the serializer by bit gates. Figure 2-44 shows the order in which bits are transferred on the three serializer output lines.

2-290. The serializer also provides two additional output lines (2BDDTSSO and 2BDDTSSO NOT). These signals are the outputs of a three-state shift register which is fed by DTSO and DTSO NOT.

2-291. SERIAL PARITY ERROR DETECTOR. A serial parity error is generated if the number of "1's" contained in the information appearing on the serializer outputs differs from the number of "1's" contained in the information feeding the tape reader register. (See figure 10-28, sheet 61.) Figure 2-45 is a block diagram of the serial parity error detector.

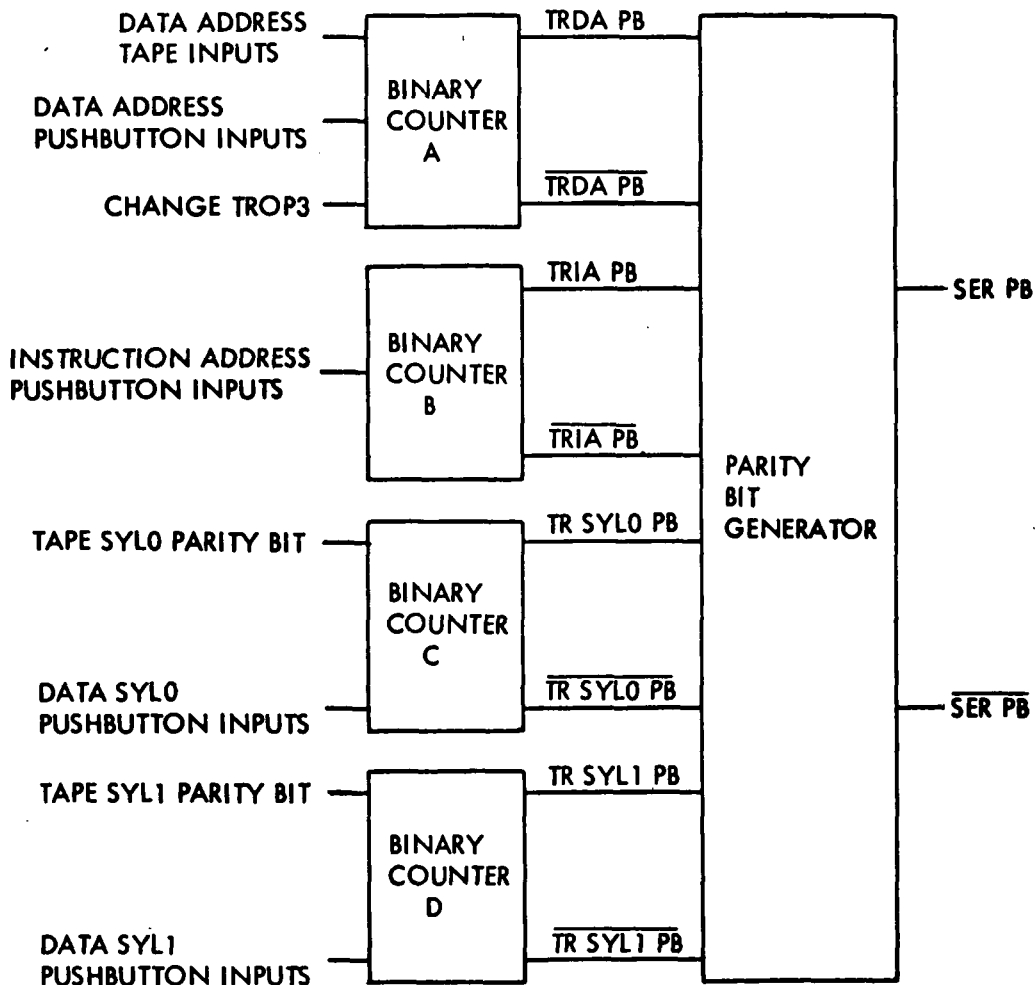


Figure 2-43. Tape Reader Register Parity Detector

	DSMSO			INSSO			DTSO		
	PHA	PHB	PHC	PHA	PHB	PHC	PHA	PHB	PHC
BG1				TROA3	TROA3	TROA3		TRB25	TRB11
BG2				TROA4	TROA4	TROA4		TRB24	TRB10
BG3				TROA5	TROA5	TROA5		TRB23	TRB9
BG4				TROA6	TROA6	TROA6		TRB22	TRB8
BG5				TROA7	TROA7	TROA7		TRB21	TRB7
BG6				TROA8	TROA8	TROA8		TRB20	TRB6
BG7	TRDM1	TRDM1	TRDM1					TRB19	TRB5
BG8				TROP1	TROP1	TROP1		TRB18	TRB4
BG9				TROP2	TROP2	TROP2		TRB17	TRB3
BG10	TRDS1	TRDS1	TRDS1	TROP3	TROP3	TROP3		TRB16	TRB2
BG11	TRDS2	TRDS2	TRDS2	TROP4	TROP4	TROP4		TRB15	TRB1
BG12	TRDS3	TRDS3	TRDS3	TROA9	TROA9	TROA9		TRB14	TRBSIGN
BG13	TRDS4	TRDS4	TRDS4	TROA1	TROA1	TROA1		TRB13	
BG14				TROA2	TROA2	TROA2		TRB12	

Figure 2-44. Tape Reader Serializer Outputs

2-292. Two binary counters (identified as "A" and "B" for this discussion) are used to count the number of "1's" appearing on the serializer outputs. These counters, which are cleared at 10 time of the preceding cycle 2 time are complemented every bit time whenever their inputs are "1's". Thus at A-6 time of cycle 2 both counters are set when an even number of "1's" appear on the serializer outputs except for two conditions:

1. A tape address of 00101 will cause "A" to be cleared.
2. A TRIA PB NOT will cause "B" to be cleared.

2-293. The outputs of the binary counters are compared and two signals (identified as Y and Y NOT for this discussion) which should correspond to SER PB and SER PB NOT are generated. These signals are applied to an exclusive OR comparator and if they do not correspond at A-6 time of cycle 2 a latch is set indicating a serial parity error.

2-294. DATA TRANSFER CONTROL. The data transfer control circuits control the flow of information between the memory loader and the central processor. The data transfer control circuits consists of the cycle generator, the DIN control circuit, and the manual mode control circuits. (See figure 10-28, sheet 61.)

2-295. Cycle Generator. The cycle generator provides additional timing gates for the memory load and memory verification operations. Figure 2-46 shows the cycle generator which consists of a three-stage shift register, a shift control circuit, and a decoding matrix.

2-296. The shift control circuit provides two shift control gates (ODD and EVEN) that occur during alternate A times. Another output from the shift control circuit (STCYC) permits the shift register to step. The shift register provides outputs C1, C1 NOT, C2, C2 NOT, C3, and C3 NOT. These outputs are applied to a matrix which produces the cycle gates as follows:

CYC1 = C1 and C2 NOT

CYC2 = C2 and C3 NOT

CYC3 = C1 and C3

CYC4 = C1 NOT and C2

CYC5 = C2 NOT and C3

CYC0 = C1 NOT and C3 NOT

2-297. In the AUTO mode the cycle generator is started (if the error latches are all reset and a transfer inhibit signal is not generated) by the first ODD gate after a sequence bit is read by the tape reader. The cycle generator stops automatically after the last cycle gate (CYC0) is generated. CYC0 is maintained until the next sequence bit is read from the tape.

2-298. In the MANUAL mode the cycle generator is started by the SRPT NOT signal. When the memory loader is in the REPEAT mode the cycle generator continues to operate as long as this mode is maintained. When the memory loader is in REPEAT, the cycle generator operates for a total of 12 cycles. The first six cycles are started by SPRT and the next cycles are started by STROP³, which is generated to enable automatic verification of manually loaded data.

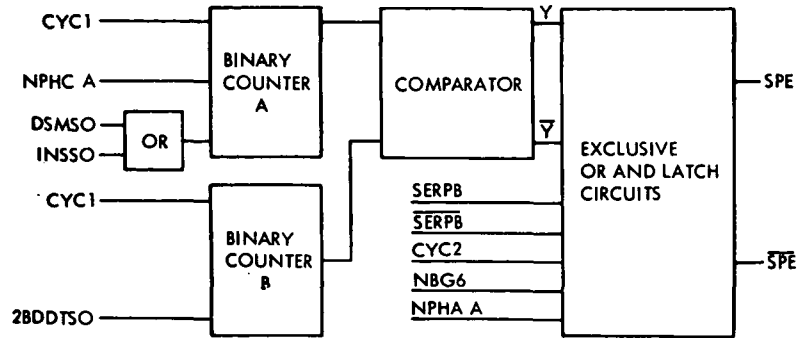
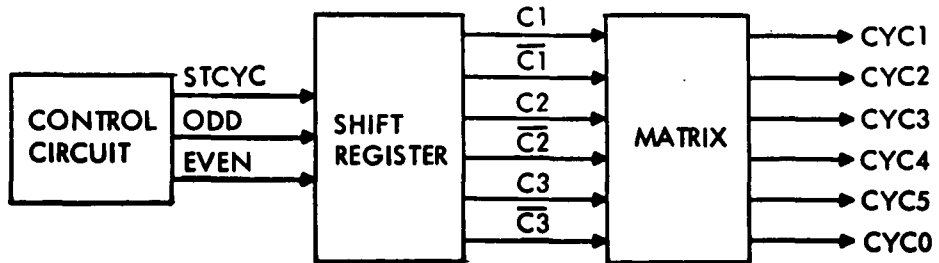


Figure 2-45. Serial Parity Error Detector



PHA										
ODD										
EVEN										
C1										
C2										
C3										
CYC1										
CYC2										
CYC3										
CYC4										
CYC5										
CYC0										

NOTE: RESTING STATE OF CYCLE GENERATOR IS CYC0 = "1"

Figure 2-46. Cycle Generator

2-299. DIN Control Circuit. The DIN control circuit organizes information appearing on the three serializer outputs and sends this information to the central processor on the DIN line. DSMSO information appears on the DIN line during B time of cycle 2. INSSO and DTSSO information appears on the DIN line when the TATC and TDTTC gates respectively are "1's". When the memory loader is in the REPEAT mode a serial parity error forces the DIN line to a "0".

2-300. The TATC gate is the output of a latch which is set from C-8 time of cycle 2 to A-8 time of cycle 3. The TDTTC gate is the output of a latch which is set from B-1 time cycle 3 to A-1 time cycle 4 except as follows:

1. When a verify command is generated (TROP3 NOT is a "0").
2. When a serial data compare error occurs (CETRS NOT is a "0") in the REPEAT mode.

2-301. Manual Mode Control Circuits. The manual mode control circuits generate seven signals (DTRPT, DTRPT NOT, SRPT NOT, CHANGE TROP3, STROP3, and RTOP3). These signals control the memory load and verification operations when the memory loader is in the MANUAL mode.

2-302. DTRPT and DTRPT NOT are the outputs of a binary counter which is complemented every time the REPEAT/REPEAT pushbutton is pressed. SRPT NOT is the reset output of a latch which is set in the REPEAT mode from C-10 time of cycle 0 to A-2 time of cycle 1 every time the ADDRESS COMPTR pushbutton is pressed if the error latches are all reset.

2-303. CHANGE TROP3, STROP3, and RTROP3 are the outputs of a tratch. The three configurations of this tratch are as follows:

<u>Configuration</u>	<u>CHANGE TROP3</u>	<u>STROP3</u>	<u>RTROP3</u>
1	"0"	"0"	"0"
2	"1"	"1"	"0"
3	"1"	"0"	"1"

The first configuration is forced every 12 time. The tratch is forced to its second configuration at A-11 time of cycle 5 when the tape reader register contains a store command. The third configuration is forced only in the REPEAT mode at A-10 time of cycle 5 when the tape reader register contains a clear and add command.

2-304. TRANSFER CONTROL CIRCUIT. (See figure 10-28, sheet 49.) The transfer control circuit controls the transfer of information to the central processor. A transfer inhibit signal is generated (TRANS INH NOT is forced to a "0") as follows:

1. For the duration of tape reader character bit 9 when the verify only latch is set and the tape reader register does not contain a clear and add command.
2. By a tape address of 00010 when the verify only latch is set.
3. When the skip first latch is set.
4. Whenever the tape reader is not in the FORWARD AUTO mode.

The verify only latch is alternately set or reset when the VERIFY ONLY pushbutton is actuated.

2-305. ERROR TEST AND ERROR RESET CIRCUITS.

2-306. The error test and error reset circuits (See figure 10-28, sheets 48 and 49.) generate four signals (ERR TEST and ERR RST and their inverses). The parity, tape, and compare error latches are all set when ERR TEST is a "1" and are all reset when ERR RST is a "1".

2-307. ERR TEST and ERR TEST NOT are the outputs of a latch which is set when the ERROR DEVICES TEST pushbutton is pressed and the tape reader is stopped. ERR RST and ERR RST NOT are forced to a "1" and a "0" respectively as follows:

1. When the ERROR RESET pushbutton on MEMORY LOAD AND DATA DISPLAY panel is pressed and the tape reader is stopped.
2. At tape reader clock pulse 2 time in the invert error mode by a tape address of 00100.

2-308. SECTOR-SYLLABLE-MODULE BUFFER REGISTER. (See figure 10-28, sheet 64.) The sector-syllable-module buffer register (SSMBR) is an 11 position latch register that receives information on the NTRS or NHOPC1 lines. The contents of the SSMBR appear on 11 parallel outputs as shown on figure 2-47.

2-309. The SSMBR is loaded with information appearing on the NTRS line during a central processor HOP instruction or NHOPC1 line during any other instruction. The SSMBR is loaded from B-6 time to the following A-1 time. In the ML mode the SSMBR cannot be loaded when a CESSMBR or CESSMSC exists, or after B-9 time of cycle 4.

2-310. Instruction sector and syllable information is subsequently gated into the SSMBR from B-6 time through B-10 time. Data module and data sector information is subsequently gated into the SSMBR at C-7, 10, 11, 12, and 13 times. Instruction module information is gated in the SSMBR at A-1 time.

2-311. The SSMBR is cleared as follows:

1. Every B-3 time unless a CESSMSC or CESSMBR exists.
2. By a CD RST signal.

2-312. SECTOR-SYLLABLE-MODULE DISPLAY REGISTER. (See figure 10-28, sheet 64.) The sector-syllable-module display register (SSMDR) is an 11 position latch register that is loaded with information from the SSMBR. The contents of the SSMDR are displayed by corresponding COMPUTER display indicator lamps.

2-313. The SSMDR latches are all initially reset at B-1 time when an ADR COMP signal is generated. The SSMDR latches are then set when the corresponding SSMBR latches are set, at B-2 time by an ADR COMP signal.

2-314. ADDRESS BUFFER REGISTER. (See figure 10-28, sheet 65.) The address buffer register (ADRBR) is a 13 position latch register that receives parallel information on the NOP1 through NOP4 and NA1 through NA9 lines. The contents of the ADRBR appear on 13 parallel outputs. The instruction address is loaded into the ADRBR at A-11 time; the OP code and operand address are loaded into the ADRBR at B-12 time. The ADRBR cannot be loaded when the central processor is in single step or when a CD RST signal is generated.

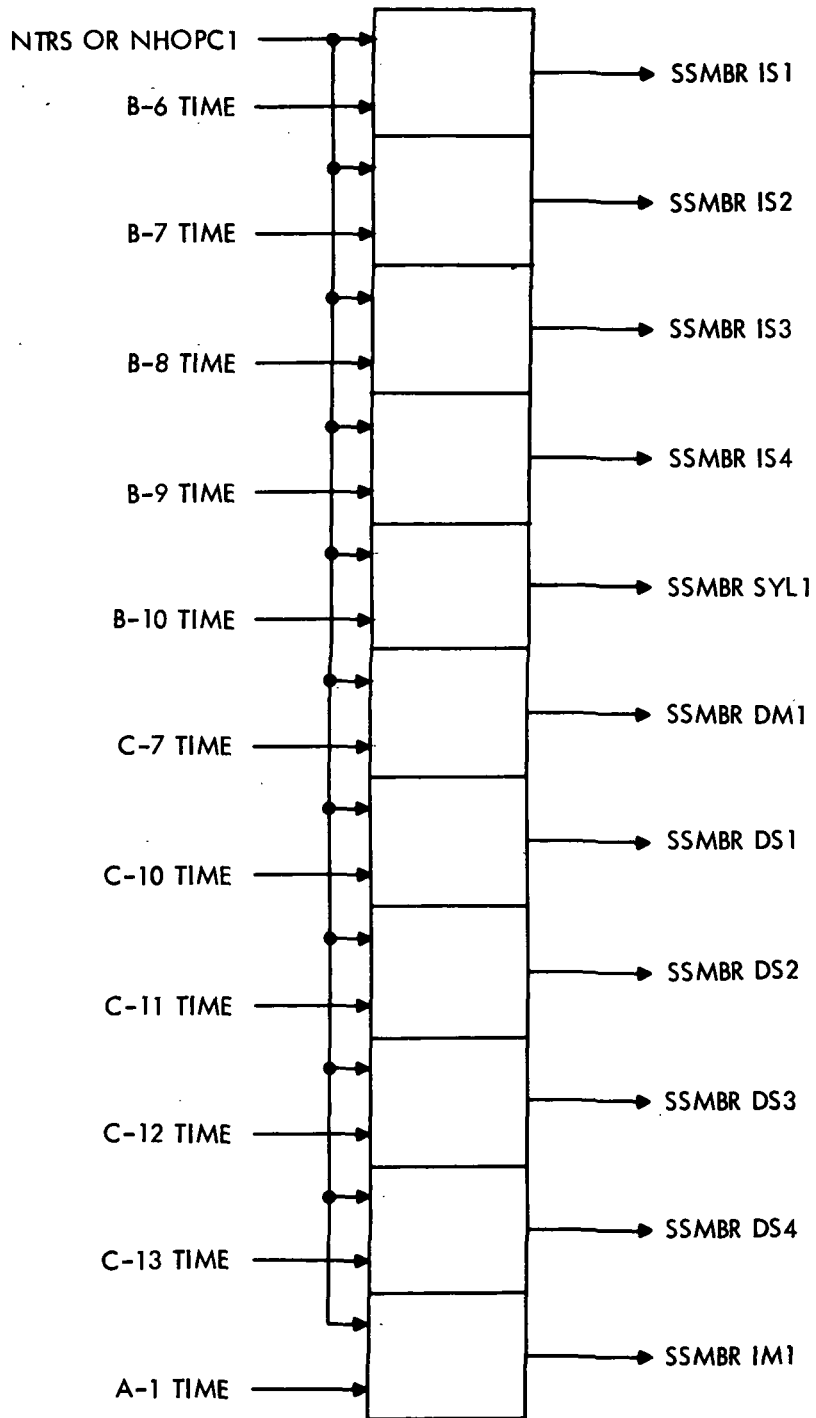


Figure 2-47. Sector-Syllable-Module Shift Register

2-315. INSTRUCTION ADDRESS DISPLAY REGISTER. (See figure 10-28, sheet 67.) The instruction address display register (IADR) is an eight position latch register that is loaded with the instruction address from the ADRBR. The contents of the IADR are displayed by the corresponding COMPUTER lamps.

2-316. The IADR latches which are all initially reset at B-1 time by an ADR COMP signal, are then set at B-2 time when the corresponding ADRBR latches are set. The IADR cannot be loaded during cycle 4 time in the ML mode and is cleared by a CD RST signal.

2-317. INSTRUCTION DISPLAY REGISTER. (See figure 10-28, sheet 67.) The instruction display register (INSDR) is a 13 position latch register that is loaded with the OP code and operand address from the ADRBR. The contents of the INSDR are displayed by the corresponding COMPUTER lamps.

2-318. The INSDR latches which are all initially reset at B-13 time by an ADR COMP signal are then set at B-14 time when the corresponding ADRBR latches are set. The INSDR like the IADR cannot be loaded during cycle 4 time in the ML mode and is cleared by a CD RST signal.

2-319. DATA DISPLAY SHIFT REGISTER. (See figure 10-28, sheet 68.) The data display shift register (DTDR) receives serial information on the NTRS and NAI3 lines. Information stored in the DTDR appears on 26 parallel outputs which are displayed by the corresponding COMPUTER lamps.

2-320. Data is loaded into the DTDR when shift clock pulses (DTDR CP1, 2, 3, and 4) are generated. The DTDR is then cleared by a CD RST signal. Figure 2-48 is a block diagram of the DTDR which consists of 35 latches connected in series.

2-321. In the ML mode NTRS or NAI3 data is gated into the DTDR by CTRS and CAI3 signals respectively. Whenever an error occurs new data cannot be entered into the DTDR until the error is reset.

2-322. In the DD mode NTRS or NAI3 information selected by the MODE CONTROL switch is gated into the DTDR when an ADR COMPARE signal is generated. AI3-IA information is shifted into positions SIGN and 1 through 7 from A-3 time to A-10 time. AI3-DATA and TRS data information is shifted in positions SIGN and 1 through 25 from B-5 time to the following A-2 time.

2-323. PARITY BIT INDICATORS. (See figure 10-28, sheet 69.) The parity bit indicator circuits generate three signals (INS BR PB, SYLO BR, and SYL1 BR) that indicate the value of the central processor instruction word and data word parity bits. The INS BR PB signal indicates the value of the instruction word parity bit. The SYLO BR and SYL1 BR signals indicate the value of the data word parity bits when the MODE control switch is in the TRS position.

2-324. INS BR PB, SYLO BR, and SYL1 BR are the outputs of three latches which are set by corresponding central processor parity bits as follows:

1. In the ML mode at A-5 time of cycle 4.
2. In the DD mode at the A-5 time following the generation of the ADR COMP signal.

The INS BR PB, SYLO BR, and SYL1 BR latches are reset as follows:

1. In the ML mode at A-4 time of cycle 4.
2. In the DD mode at the A-4 time following the generation of the ADR COMP signal.
3. By a CD reset signal.

2-325. The presence of instruction word and data word parity bits are detected and stored in three latches. These latches control the setting of the INS BR PB, SYLO BR, and SYL1 BR latches and are set by an MBR 14 signal as follows:

<u>Control Latch</u>	<u>Set Duration</u>
INS BR PB	A-12 time to the following A-11 time.
SYLO BR	C-4 time to the following A-3 time during a central processor store cycle. B-4 time to the following A-3 time during a central processor read cycle.
SYL1 BR	A-4 time to the following A-3 time during a central processor store cycle. C-4 time to the following A-3 time during a central processor read cycle.

2-326. INPUT/OUTPUT PROCESSOR.

2-327. The Input/Output Processor contains the circuits necessary to control the transfer of information into or out of the Central Processor. The Input/Output Processor contains control logic for the following:

1. Printer
2. Typewriter
3. Digital Data Plotter
4. Input Serializer
5. Discrete Output and Display Register
6. Program Control Mode Display Register

2-328. PRINTER LOGIC.

2-329. The printer control logic (figure 2-49) consists of: (1) a 26-bit parallel register; (2) a BCD and octal decoder; (3) a 12-state counter; (4) an asynchronous timer; (5) program control logic; and (6) an odd parity generator.

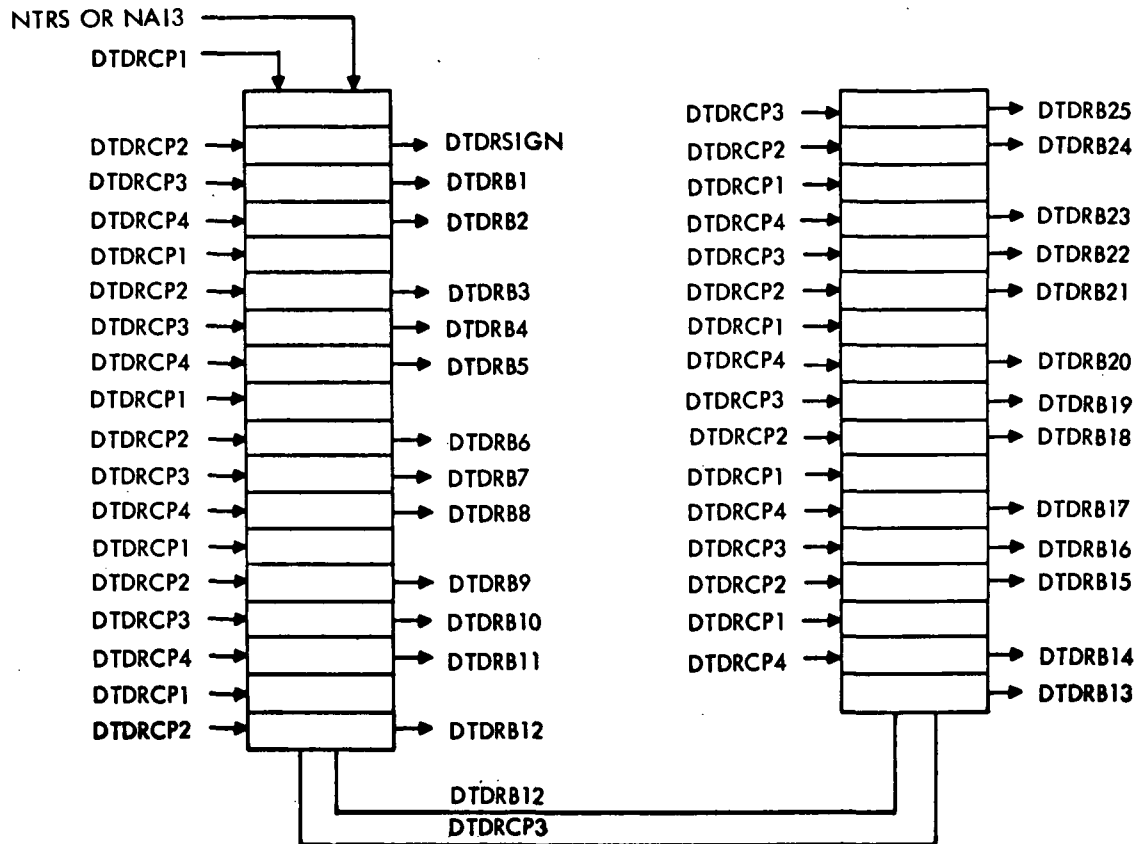


Figure 2-48. Data Display Shift Register

2-330. TWENTY-SIX BIT PARALLEL REGISTER. (See figure 10-28, sheet 42.) The 26-bit register provides storage for one complete processor data word. Data bits SIGN and 1 through 5 are gated into the register with a print-store or carriage gate (PRS + CARR GATE) at A-1-Z time. The gate is developed when either the print-store 774 NOT (PRS 774 NOT) latch or carriage control (CARR CTRL) latch is set. The PRS 774 NOT latch is set when any print-store instruction except 774 is programmed. This indicates that data line transfers to the printer are allowable. The CARR CTRL latch is set when a CIO 160 is programmed. This commands a control carriage skip operation in the printer. The number of skips is dictated by a decode of the first six data bits. Data bits SIGN and 1 through 25 are gated into the 26-bit register at A-1-Z time by means of a print-store gate (PRS GATE). The PRS GATE is developed when PRS 774 NOT latch is set. The 26-bit register is reset with a machine reset (MACH RST) or a printer reset (PRINT RST). The MACH RST level clears the 26-bit register when PTC power is cycled on or when the machine reset pushbutton on the PTC is pressed. The PRINT RST level causes the clearing of the 26-bit register and it occurs: (1) when the buffer register within the printer is loaded with 4, BCD characters; (2) when the buffer register within the printer is loaded with 12 octal characters; (3) when the buffer register within the printer is loaded with a carriage control instruction; or (4) when the processor is released for the following operation as dictated by the PROCESSOR RELEASE level fed back to the processor from the printer. The clearing of the 26-bit register initializes the register for the next instruction word.

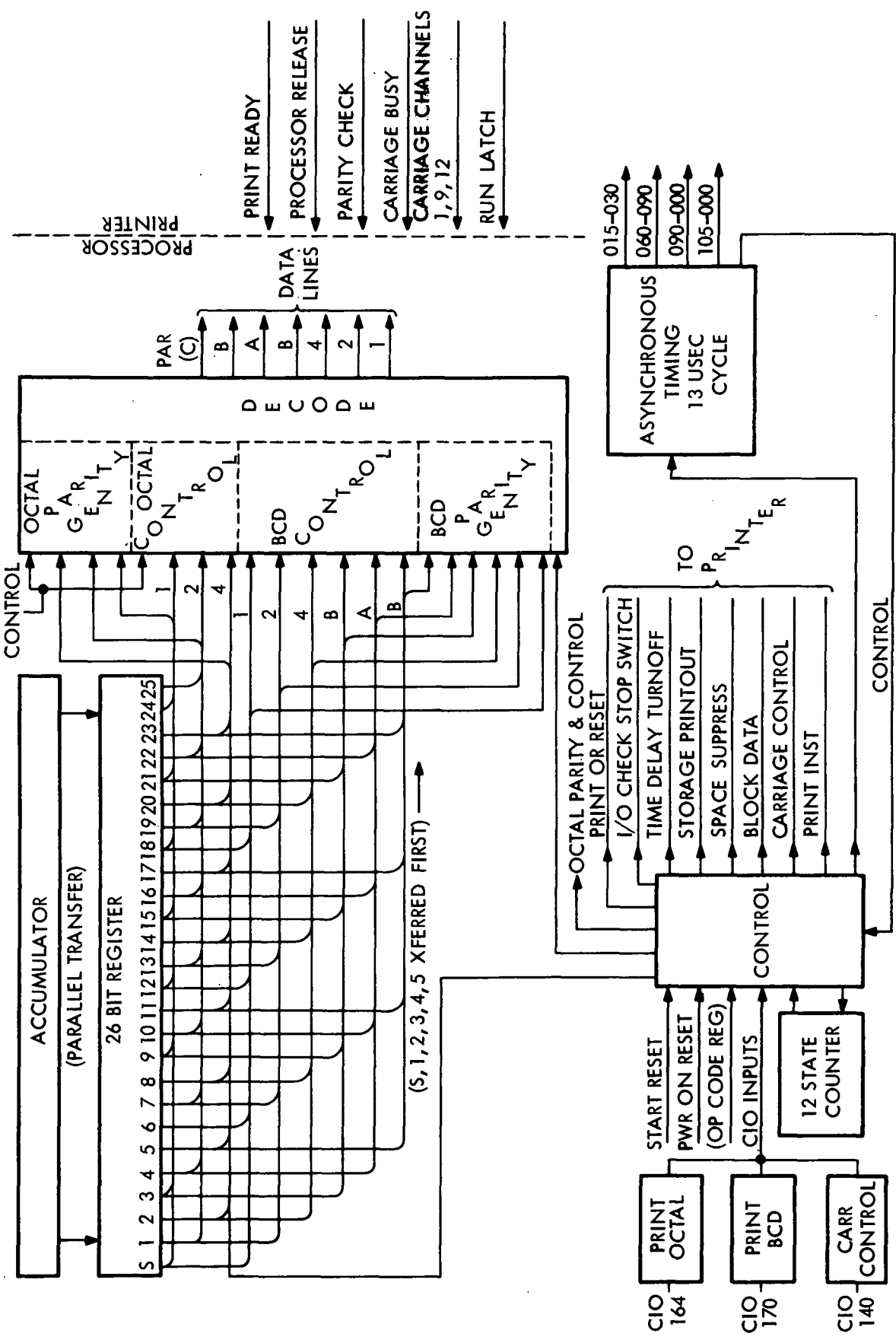


Figure 2-49. Printer Controls Block Diagram

2-331. DECODER. The data word is decoded and furnished to the printer parallel-by-bit (either 3 or 6 bits per character) and serial-by-character on seven data lines (figure 10-28, sheets 43 and 44) designated DATA 1, DATA 2, DATA 4, DATA 8, DATA A, and DATA B. (See figure 2-50 for printer character coding.) Another line furnished is DATA C which is an assigned parity bit (odd) for each character group transmitted. Data is transferred in 26-bit word groups in either octal (OCTAL) or binary coded decimal (BCD) modes. In the OCTAL mode, the 26-bit data word is serialized into eight 3-bit characters and one 2-bit character. Each character is transferred with its parity bit to the printer. After each 9 character data word is transferred an automatic three character spacing is instituted by holding all data lines to zero during counts 10, 11 and 12 of the 12-state counter, while providing a parity bit. The 12 character transfers are itemized by the 12-state counter and are completed within two instruction times. In the BCD mode, the 26-bit data word is divided into four 6-bit characters. Each character is transferred to the printer under regulation of the 12-state counter. The four character transfers require less than one instruction time.

2-332. TWELVE-STATE COUNTER. The 12-state counter (figure 10-28, sheet 45) which controls sorting bits into BCD and octal characters is controlled by 4 triggers which are aligned into a four position counter. The counter starts to cycle when the processors asynchronous timer reaches 015-030 time and adds a count each succeeding time the asynchronous timer goes to 015-030 time. The counts of the 4 triggers are decoded into twelve decimal counts (DEC 1 through DEC 12) thereby forming the 12-state counter. The triggers are reset, rendering a zero count by means of a machine reset or a control reset (CNT RST). The machine reset is explained in a previous paragraph and the CNT RST is developed the same as the PRINT RST in the 26-bit register. This also is explained in a previous paragraph.

2-333. ASYNCHRONOUS TIMER. The asynchronous timer is a delay type network which produces four sequential gates (015-030, 060-090, 090-000, and 105-000) occurring within 13 USEC, but not less than 11.1 USEC. Each cycle of the timing generator institutes a character transfer from the processor to the printer while also controlling functions within the printer.

2-334. The timing generator is started when either the printer is set to print in character position 1 (PRINT CHAR POS 1) due to PARITY CHECK level (indicating parity error in printers previous line of print) received from the printer or during a print instruction. In both cases the printer buffer must be initialized to receive data and no inhibit must be present to prevent starting the timing generator. The timing generator is inhibited: (1) during BCD mode when the 12-state counter is at decimal 4 (DEC 4) time and the timing generator is presently at 090-000 time; (2) during octal mode when the 12-state counter is at decimal 12 (DEC 12) time and the timing generator is presently at 090-000 time; or (3) when an end of line of print is reached as indicated by the group mark-word mark latch being reset (GMWM LTCH) and the timing generator is presently at 090-000 time. The inhibits indicate that the last octal or BCD character of a word is being transferred and a new cycle is not ready to start or that the processor is not released to start a new cycle.

2-335. PROGRAM CONTROL. In order for the printer to perform its functions, it must be programmed to do so. The programming instructions for printer controls are as follows:

1. CIO 170 — This programmed instruction resets the BCD latch (BCD LTCH) and allows a BCD mode of operation. The BCD mode is inhibited when data is forced to the carriage control latches of the printer, or by the printer being ready to print or by a carriage instruction.

2. CIO 164 — This programmed instruction sets the octal latch (OCTAL LTCH) and allows octal mode of operation. Octal mode is inhibited by the same inhibit conditions as in the BCD mode above. Sequential print-store operations cannot be programmed in the octal mode since it requires two instruction cycles to process all the octal characters in one word.

3. CIO 160 — The printer carriage is controlled by a CIO 160 and the decoded data bits shown in figure 2-51. Carriage control depends on a paper tape within the printer. If a hole is sensed in channel 12 of the carriage control tape an automatic skip to channel 1 will occur. This provides automatic page control for a standard format output on the printer paper without the use of a programmed CIO.

4. PRS 774 — The print-store 774 instruction sets the PRS 774 NOT latch, which causes blocking of the data lines to the printer and filling the remaining buffer positions with space characters. One line of print is thereby initiated.

5. PRS 775 — The print-store 775 instruction causes transfer of data from the accumulator into the printer buffer. A print cycle occurs if the buffer is filled.

6. PRS 000-773 — The print-store 000-773 instruction causes the transfer of data from the memory address specified to the accumulator and then to the printer buffer.

2-336. A non-programmed control is the printer ready level (PRNTR READY). PRNTR READY (figure 10-28, sheet 44) allows printer operation if bit 25 of the processors A switches is not sensed when the level is present. If the A switch is sensed ("0") a printer busy level is developed which prevents printer operation. The PRNTR READY level is present when the printer feeds back to the processor controls concurrent levels indicating readiness of the printer to perform another function.

2-337. PARITY CHECKING. The data line outputs (figure 10-28, sheet 44) are checked for correct parity (odd) by parity detector circuits. A typical parity detector is explained earlier in subsidiary circuit descriptions. If even parity is detected during character transfer, a "1" is added to the existing even parity thereby generating correct parity (odd). The generated bit is placed on the DATA C line and transferred to the printer along with all the data bits which make up the character.

2-338. Another parity check is made when data is transferred from the printer buffer to the printing mechanism within the printer. If an error is detected the printer is not stopped but a PARITY CHECK level is routed back to the Central Processor as a control to identify the error. The possible errors and means of identification are as follows: (See figure 10-28, sheet 44 for parity error controls.)

1. BCD error during buffer load or print is identified by a character "b" printed in the first position of the next line of print providing the next line of print is BCD. The BCD printout is indented one print position from the normal place that a line of print is started.

2. BCD error during buffer load or print is identified by a character, "b" printed in the first position after the first word of octal print (tenth position), providing the next line of print is octal.

3. Octal error during buffer load is identified by a character "-" printed in the second space after the word in which the error occurred (eleventh position).

To	CIO Code	Data Line					
		1	2	4	8	A	B
<u>Immediate Skip</u>							
Channel 1	160	X					
Channel 2	160		X				
Channel 3	160	X	X				
Channel 4	160			X			
Channel 5	160	X		X			
Channel 6	160		X	X			
Channel 7	160	X	X	X			
Channel 8	160				X		
Channel 9	160	X			X		
Channel 10	160		X		X		
Channel 11	160	X	X		X		
Channel 12	160			X	X		
<u>Immediate Space</u>							
1 Space	160	X					X
2 Spaces	160		X				X
3 Spaces	160	X	X				X
<u>Skip After Print</u>							
Channel 1	160	X				X	X
Channel 2	160		X			X	X
Channel 3	160	X	X			X	X
Channel 4	160			X		X	X
Channel 5	160	X		X		X	X
Channel 6	160		X	X		X	X
Channel 7	160	X	X	X		X	X
Channel 8	160				X	X	X
Channel 9	160	X			X	X	X
Channel 10	160		X		X	X	X
Channel 11	160	X	X		X	X	X
Channel 12	160			X	X	X	X
<u>Space After Print</u>							
1 Space	160	X				X	
2 Spaces	160		X			X	
3 Spaces	160	X	X			X	
Note: "X" represents a "1".							

Figure 2-51. Printer Carriage Control Codes

4. Octal error during print, providing the next line of print is BCD, is identified by a character "b" printed in the first position of the next line of print. The octal printout is indented one print position from the start of a line of print.

5. Octal error during print, provided the next line of print is octal, is identified by a character "b" in the first position after the first word of octal print (tenth position).

2-339. TYPEWRITER LOGIC. (See block diagram figure 2-52 and figure 10-28, sheets 37 and 38.)

2-340. The typewriter control logic is activated by four CIO commands (CIO 120, 124, 130 and 134). The first three CIO's, in the order shown, control three print modes: (1) print (type) alpha numeric; (2) print (type) decimal; and (3) print (type) octal, respectively. CIO 134 performs the following control functions when the indicated accumulator bits are present:

<u>Accumulator Bit</u>	<u>Function</u>
SIGN	Space
1	Select black ribbon
2	Select red ribbon
3	Set index
4	Provide carriage return
5	Set tab

2-341. During the time that the 6 hi-order bits of the accumulator are being transferred to the 6 typewriter binary coded decimal (BCD) latches, a decoder latch is set (from B-1 through A-2 time) to provide mode selection and function control gates. These gates are; print alpha-numeric (PRINT ALPH NUM), print decimal (PRINT DEC), print octal (PRINT OCT) and PRINT CONTROLS. The PRINT ALPH NUM or PRINT CONTROLS gate allows gating of 6-bits of accumulator information into the BCD latches to set up either one alpha-numeric character of type or one control function. Print decimal (PRINT DEC) allows gating of 4-bits of accumulator information into four BCD latches to set up one decimal coded character of type. Print octal (PRINT OCT) allows gating of 3-bits of accumulator information into three BCD latches to set up one octal coded character of type. (See figure 2-53 for decoded accumulator bits at the BCD latches.)

2-342. There are five control latches which provide gating levels for five specific typewriter control functions. The functions are as follows: (See timing charts figures 2-54 and 2-55 for control and print timing charts.)

1. Alpha-numeric spacing (ALP SPA) --- is a latch controlled level developed during PRINT ALPH NUM mode, providing PRINT DEC mode is not selected.

2. PRINT DATA --- is a latch output gating level which occurs during any print mode.

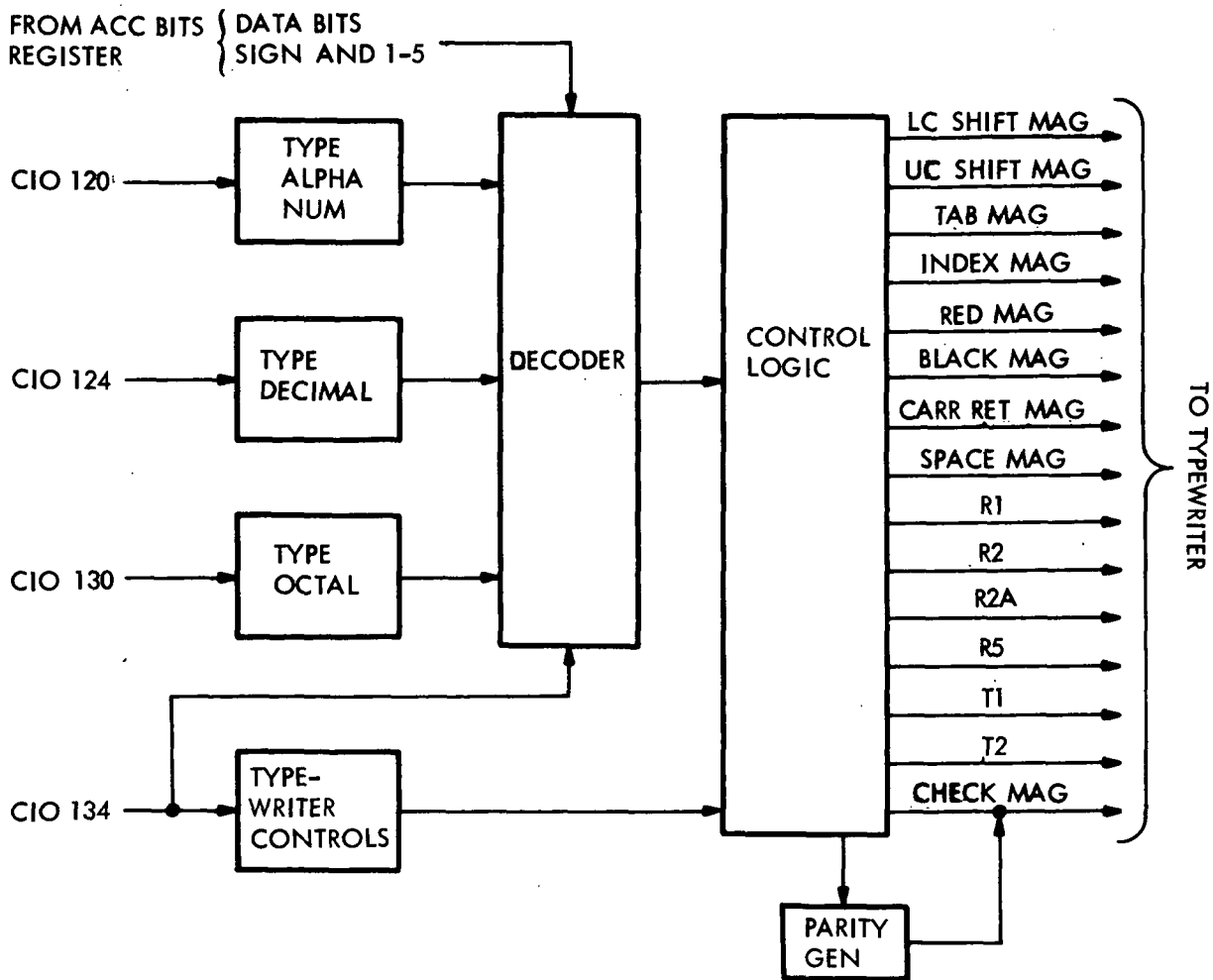


Figure 2-52. Typewriter Controls Block Diagram

3. Spacing and tilt selection level (GATE L) --- is developed during any print mode at A-3-Z time. This allows time for data to be gated out of the accumulator into data latches at A-1-Z time.

4. Typewriter controls gate (PRINT CONTROLS) --- is developed only during CIO 134.

5. Octal decode gate to print drivers --- is developed under control of the PRINT OCT mode and is used only to force zero in the octal mode when a condition of "no data present" prevails.

Character Selected	Accumulator Bits					
	5	4	3	2	1	SIGN
	BCD Code					
	1	2	4	8	A	B
A	X				X	X
B		X			X	X
C	X	X			X	X
D			X		X	X
E	X		X		X	X
F		X	X		X	X
G	X	X	X		X	X
H				X	X	X
I	X			X	X	X
J	X					X
K		X				X
L	X	X				X
M			X			X
N	X		X			X
O		X	X			X
P	X	X	X			X
Q				X		X
R	X			X		X
S		X			X	
T	X	X			X	
U			X		X	
V	X		X		X	

Figure 2-53. Typewriter Character Coding (Sheet 1 of 4)

Character Selected	Accumulator Bits					
	5	4	3	2	1	SIGN
	BCD Code					
	1	2	4	8	A	B
W		X	X		X	
X	X	X	X		X	
Y				X	X	
Z	X			X	X	
1	X					
2		X				
3	X	X				
4			X			
5	X		X			
6		X	X			
7	X	X	X			
8				X		
9	X			X		
0		X		X		
?		X		X	X	X
⌘			X	X	X	X
[X		X	X	X	X
!		X		X		X
*			X	X		X
]	X		X	X		X
≠		X		X	X	
%			X	X	X	

Figure 2-53. Typewriter Character Coding (Sheet 2)

Character Selected	Accumulator Bits					
	5	4	3	2	1	SIGN
	BCD Code					
	1	2	4	8	A	B
@	X		X	X	X	
:	X		X	X		
>		X	X	X		
;		X	X	X		
√	X	X	X	X		
\		X	X	X	X	
<		X	X	X	X	X
Δ	X	X	X	X		X
⌘	X	X	X	X	X	
⌘	X	X	X	X	X	X
-						X
#	X	X		X		
¢					X	
&					X	X
\$	X	X		X		X
,	X	X		X	X	
.	X	X		X	X	X
/	X				X	
Space						

Note: "X" indicates a "1" in the bit position.

Figure 2-53. Typewriter Character Coding (Sheet 3)

Character Selected	Accumulator Bits		
	2	1	SIGN
	OCTAL Code		
	1	2	4
1	X		
2		X	
3	X	X	
4			X
5	X		X
6		X	X
7	X	X	X
0			

Note: "X" indicates a "1" in the bit position

Figure 2-53. Typewriter Character Coding (Sheet 4)

2-343. The five control latches and the six BCD latches are all reset at the same times, after a print cycle is completed NORMAL RESET and during a regular machine reset (STRT RESET).

2-344. TYPE CYCLE TIMING. The type cycle timing is determined by the case location (upper or lower case) of the previously typed character and is controlled by the case control latch. The lower case which contains capital letters is used normally since capital letters are the only letters available. Shifting to upper case allows use of special symbols. The case control latch is reset to lower case (LC LATCH) as follows:

1. When a lower case character is programmed and the typewriter is in upper case if printing is not inhibited by the presence of the BLOCK TILT AND ROTATE gate and a ready condition (TILT SELECT gate) is present. The BLOCK TILT AND ROTATE gate indicates that a CIO 134 is programmed and that the typewriter is busy, i. e., mechanically shifting case (SCC TRANSFER latch is set). The TILT SELECT gate is present when; (1) the typewriter is not busy (SCC TRANSFER latch reset); (2) the typewriter is waiting for a shift operation; and (3) the function control latches, GATE L and PRINT DATA, are set.

2. Approximately 64 MSEC after a machine reset (MACH RESET) is initiated if the typewriter is not busy (SCC TRANSFER latch is reset).

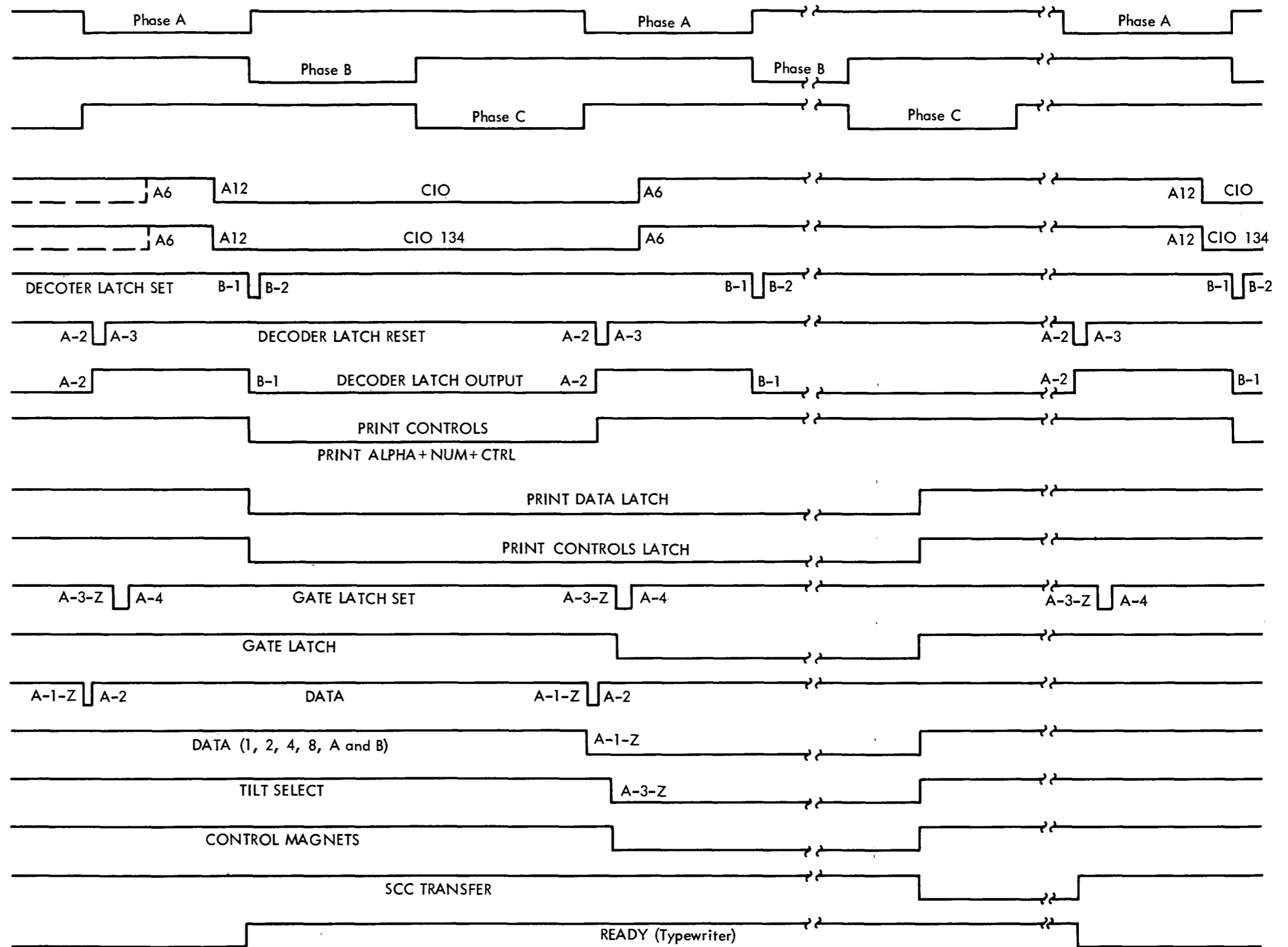


Figure 2-54. Typewriter Control, Timing Chart

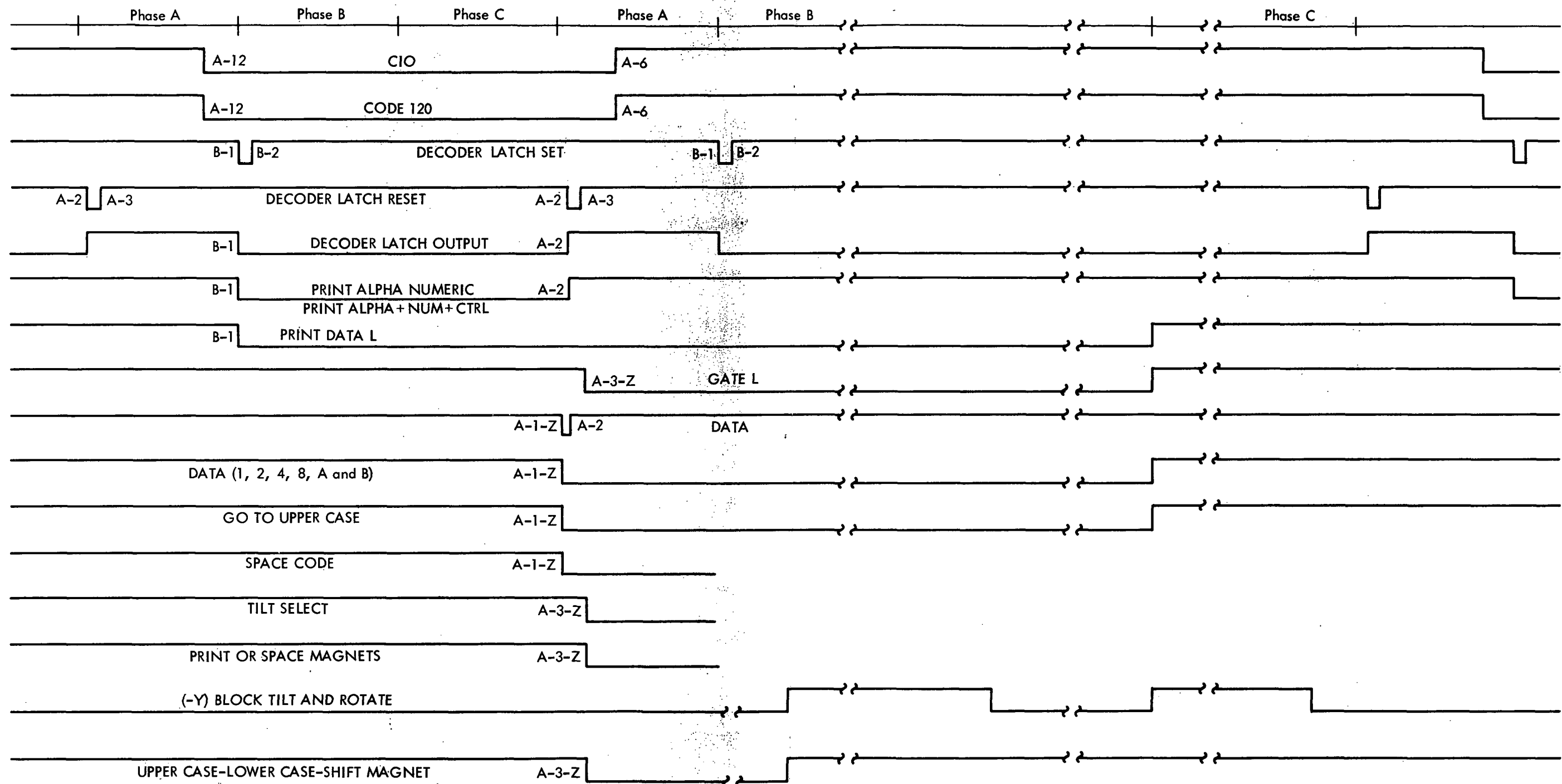


Figure 2-55. Typewriter Print, Timing Chart (Sheet 1 of 2)

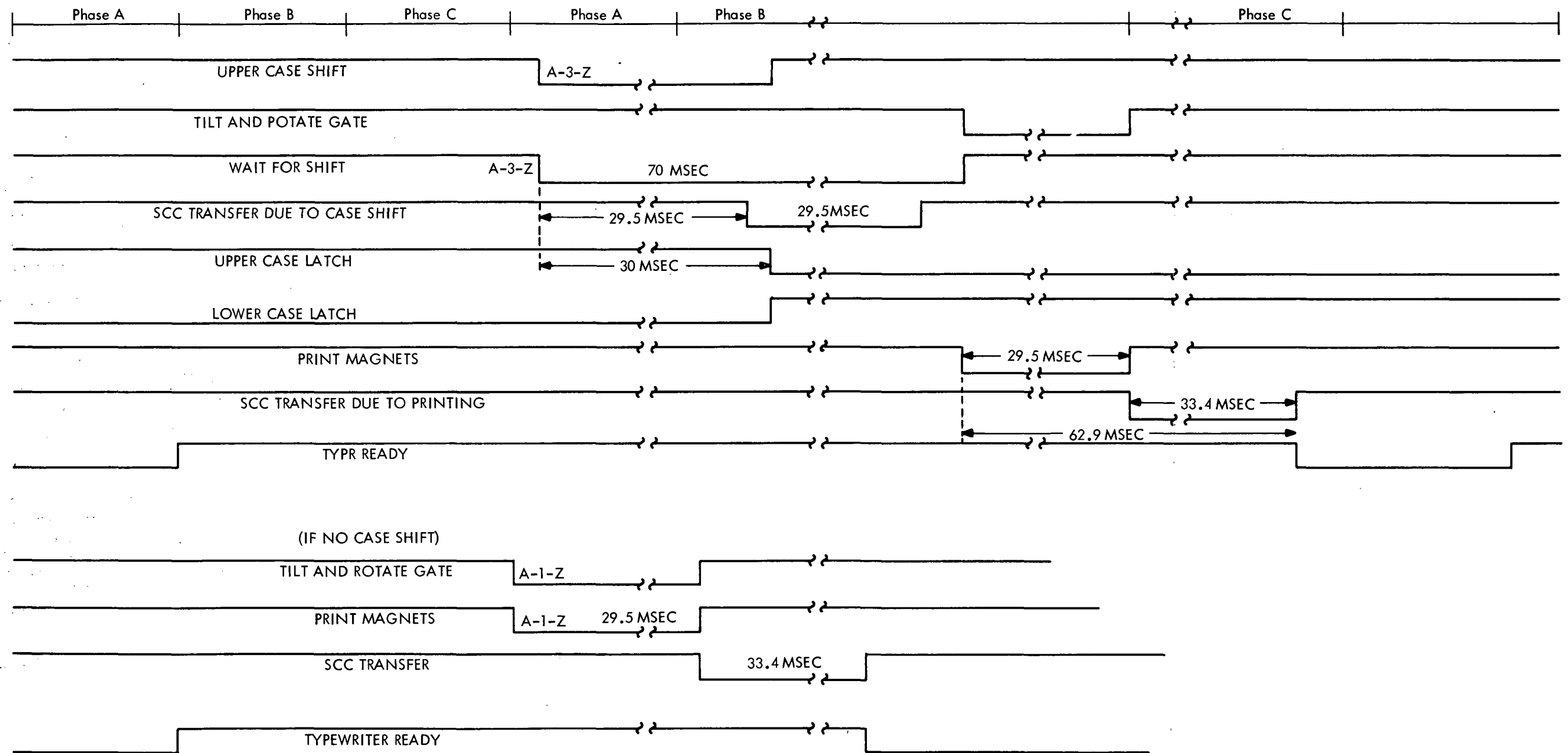


Figure 2-55. Typewriter Print, Timing Chart (Sheet 2)

2-345. The case control latch is set to upper case (UC LATCH) when; (1) an upper case character is programmed, and the typewriter is presently in lower case; (2) when printing is not inhibited by BLOCK TILT AND ROTATE gate; and (3) when the TILT SELECT gate is present.

2-346. The case control latch remains in its present state until programmed to change. Each time the status of the case control latch changes, the corresponding case control magnet in the typewriter is actuated and the type head positioned accordingly.

2-347. CONTROL FUNCTIONS. There are six typewriter control functions. (See figure 10-28, sheet 38.) Each control function is developed from two control gates (TILT SELECT and PRINT CONTROLS) and a BCD latch decode characteristic of that function. The concurrence of these three levels causes a typewriter magnet to pick and the programmed function to take place. One function, the carriage return function, is peculiar in that its magnet (CAR RET MAG) can also be picked in another way. It is picked when the READY level and the RIGHT MARGIN level occur at the same time. The READY level is present when; (1) the typewriter is not waiting for a shift (WAIT FOR SHIFT level is a "1"); (2) when the typewriter feedback circuits indicate completion of that last print cycle (SCC TRANSFER = "1"); and (3) the tab and carrier return interlock is cleared to allow a carriage return. The RIGHT MARGIN level is a feedback from the typewriter which indicates that the printing has reached the right extreme. The WAIT FOR SHIFT level is a "0" (delayed 70 MS) which allows going from upper case to lower case and conversely. The delayed WAIT FOR SHIFT level inhibits normal reset during case change.

2-348. The typewriter sends several cam operated and interlock feedback levels to the control logic. These levels are designated on figure 10-28, sheet 38 as a letter or a letter prefixed by a lozenger (⌘), and indicates functions status. The feedback levels set or reset three control latches whose outputs collectively relay to the control logic the present typewriter status, i. e., that the typewriter is either ready for another operation or is busy. The three control latches and their feedback controls are as follows:

1. The selectric common contacts transfer latch (SCC TRANSFER) is set when ground potential is routed through the normally open contacts of the print feedback cams resulting in feedback Z or ⌘ N indicating a print cycle is still underway. When the carriage return index is reached, the normally open carriage return index cam contacts produce feedback ⌘ B, causing the latch to set by routing ground to its set control. This indicates that the typewriter is busy. The SCC TRANSFER latch is reset when feedbacks ⌘ A and W are at ground potential. The normally closed cam operated contacts (which indicate that a print cycle is not in progress; that a case shift is not underway; and that space, backspace, tab, and carriage return operations are not in progress) allow routing ground back to the reset control of the SCC TRANSFER latch.

2. The tab and carriage return interlock latch (TAB AND CRTN INTLK) is set when feedback ⌘ C is at ground potential. The ground level is routed through the normally open tab interlock contacts and indicates that the typewriter is busy. The TAB AND CRTN INTLK latch is reset when feedback ⌘ Y is present. The feedback is ground level routed through the normally closed contacts and indicates that no tab or carriage return operation is under way.

3. The right margin latch (RIGHT MARGIN) is set when feedback ⌘ E is at ground potential. Ground is routed through the normally closed END OF LINE interlock contacts indicating that the end of the line is not yet reached and that the typewriter is

ready for another operation. When the end of the line is reached the interlock contacts cause ground to be routed through the normally open contacts. Feedback \bar{A} F resets the right margin latch which effectively prevents another operation until the print head returns to the left margin.

2-349. PRINT CONTROLS. The type head must be positioned for proper selection of the desired letter or symbol to be printed. This is done by selection of the correct combination of rotate print drivers R1, R2, R2A and RS and tilt print drivers T1 and T2. (See figure 2-56 for the selection and tilt rotate schedule of each letter or symbol on the typewriter keyboard.) The combination of print drivers selected is a result of the outputs of the BCD latches gated by the TILT AND ROTATE gate. (See figure 10-28, sheet 38.) The TILT AND ROTATE gate allows tilting and rotating of the type head and is made up of all the pre-required conditions for the tilt-rotate operation to take place. These conditions are as follows:

1. The typewriter must be in upper or lower case operation.
2. The presence of any print mode at A-3-Z time (PRINT DATA L and GATE L latches set).
3. The tilt-rotate operation is not blocked due to a function caused by CIO 134 or to the typewriter being busy (SCC TRANSFER latch set).
4. The typewriter is not waiting for a shift operation, i. e., no case change is in progress.

2-350. PARITY CHECKING. The outputs of the tilt and rotate drivers are checked for correct parity (odd) by the parity detector circuits. The parity detector used here (figure 10-28, sheet 38) is the same as the typical parity detector explained earlier in subsidiary circuit descriptions. If even parity is detected during the time the print driver gating level (TILT AND ROTATE GATE) is present, the check magnet is picked in the typewriter and a check bit is developed. A "1" is therefore added to the existing even parity thereby generating correct parity (odd).

BCD Keyboard										
Upper Case	Lower Case	T 2	Check Bit	T 1	R2 A	R 1	R 2	R 5	TLT	ROT
Upper case is blank except as indicated.	A		X		X	X	X	X	3	-5
	B		X		X		X		3	+1
	C				X		X	X	3	-4
	D			X		X			3	+2
	E					X	X		3	-3
	F					X			3	+3

Figure 2-56. Selection and Tilt-Rotate Schedule (Sheet 1 of 3)

BCD Keyboard											
Upper Case	Lower Case	T 2	Check Bit	T 1	R ₂ A	R 1	R 2	R 5	TLT	ROT	
?	G		X		X			X	3	-2	
	H		X			X		X	3	-1	
	I					X			3	+4	
	J			X	X	X	X	X	2	-5	
	K			X	X		X		2	+1	
	L		X	X	X		X	X	2	-4	
	M			X	X	X			2	+2	
	N			X	X	X	X	X	2	-3	
	O			X	X	X			2	+3	
	P			X	X			X	2	-2	
	*	Q			X		X		X	2	-1
		R		X	X		X			2	+4
	%	S	X			X		X		1	+1
		T	X	X		X		X	X	1	-4
		U	X			X	X			1	+2
		V	X	X		X	X		X	1	-3
		W	X	X		X				1	+3
		X	X			X			X	1	-2
		Y	X				X		X	1	-1
		Z	X	X			X			1	+4
		1	X	X	X	X	X	X	X	0	-5
		2	X	X	X	X		X		0	+1
	3	X		X	X		X	X	0	-4	
	4	X	X	X	X	X	X	X	0	+2	

Figure 2-56. Selection and Tilt-Rotate Schedule (Sheet 2)

BCD Keyboard										
Upper Case	Lower Case	T 2	Check Bit	T 1	R2 A	R 1	R 2	R 5	TLT	ROT
	5	X		X	X	X		X	0	-3
	6	X		X	X				0	+3
	7	X	X	X	X			X	0	-2
	8	X	X	X		X		X	0	-1
:	9	X		X		X			0	+4
	∅	X		X				X	0	0
;	-		X	X	X	X	X		2	0
		X	X	X					0	+5
		X	X		X	X	X		1	0
					X	X	X		3	0
	\$			X					2	+5
	,	X							1	+5
	.		X						3	+5
		X			X	X	X	X	1	-5

Note: "X" indicates that typewriter solenoid is energized.

Figure 2-56. Selection and Tilt-Rotate Schedule (Sheet 3)

2-351. DIGITAL DATA PLOTTER.

2-352. The digital data plotter is controlled by three commands, CIO 140, 144 and 150. (See block diagram, figure 2-57.) The CIO 140 and 144 commands control direction of plotting and the CIO 150 command raises or lowers the plotting pen.

2-353. A CIO 140 command drives the plotting paper in the forward or reverse direction for plotting along the X axis of the pen. A CIO 144 command drives the pen to the left or right for plotting along the Y axis of the pen. Plotting is performed in 0.01 inch steps at a rate of 300 steps per second. The plotter can be stepped a maximum of 1024 times (approximately 10 inches) along the X or Y axis of the pen by each X or Y command.

2-354. The direction of plotting is determined by the value of the SIGN bit contained in the central processor accumulator data word at the time an X or Y command is issued.

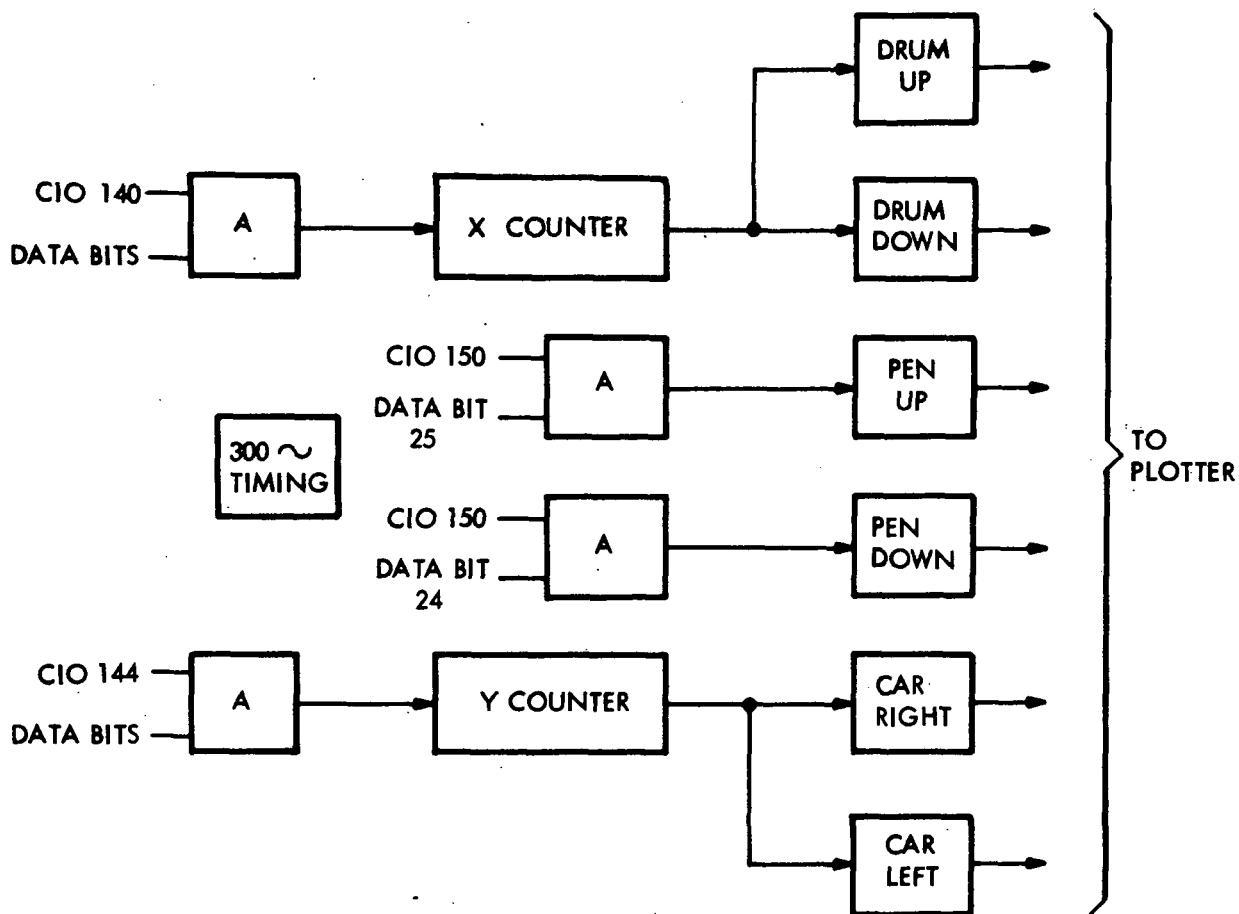


Figure 2-57. Plotter Block Diagram

(See figure 10-28, sheet 39.) A "0" value enables the plotting paper to be driven in the forward direction (DRUM DOWN PLOT) or enables the pen to be driven to the left (CARR LEFT PLOT). A "1" value enables the plotting paper to be driven in the reverse direction (DRUM UP PLOT) or enables the pen to be driven to the right (CARR RIGHT PLOT).

2-355. A plotting operation which consists of an X and/or a Y command allows the plotter to be stepped along the X and Y axes simultaneously. The number of plotting steps performed along each axis is determined by the binary count contained in data bit locations 16 through 25 of the central processor accumulator at the time a plotting operation is commanded. The number of plotting steps to be performed along the X and Y axes is loaded into two ten trigger counters (one counter for X and one counter for Y). (See figure 10-28, sheets 40 and 41.) The counters are stepped down by the 300 cycle per second counter under control of CIO 144. When both the X and Y counters reach the zero count, the plotting operation stops.

2-356. A CIO 150 command raises the pen (PEN UP) if the central processor accumulator data bit 25 value is a "1". The pen is lowered (PEN DOWN) when the central processor accumulator data bit 24 value is a "1". The position of the pen can be changed a maximum of ten times per second.

2-357. INPUT SERIALIZER.

2-358. The input serializer takes parallel information from the intercept latches, program register "B" switches, or program register "A" switches for the purpose of either exercising program control or for manually inserting data into the processor. (See block diagram, figure 2-58.) The interrupt latches are read into the serializer under control of a CIO 154; the program register "A" switches are read into the serializer under control of a CIO 214; and the program register "B" switches are read into the serializer under control of a CIO 220. The bits loaded into the serializer are serialized into the accumulator at the specific phase and bit gate times shown on figure 10-28, sheet 36.

2-359. The PTC program register "A" switches have dual usage of bits 17 through 25. Discrete inputs six through one are routed through the "0" side of "A" switch bits 17 through 22. The typewriter busy, plotter busy and printer busy signals are routed through the "0" side of "A" switch bits 23, 24 and 25, respectively.

2-360. DISCRETE OUTPUT AND DISPLAY REGISTER. (See block diagram, figure 2-59.)

2-361. The discrete output and display register is a six latch register (figure 10-28, sheet 7) whose latches are set by the six low order bits of the accumulator when a CIO 120 is programmed. Each latch output goes to a line driver and a lamp driver. Each line driver output effects the read-out of one of the six channels of LVDCME delay lines (in ASTEC configuration) when programmed to do so, whereas the indicators indicate latch status. The register can also be used similarly to the program control mode display register (as a programmers tool) to indicate that a program sequence (e. g., a pass count) has occurred.

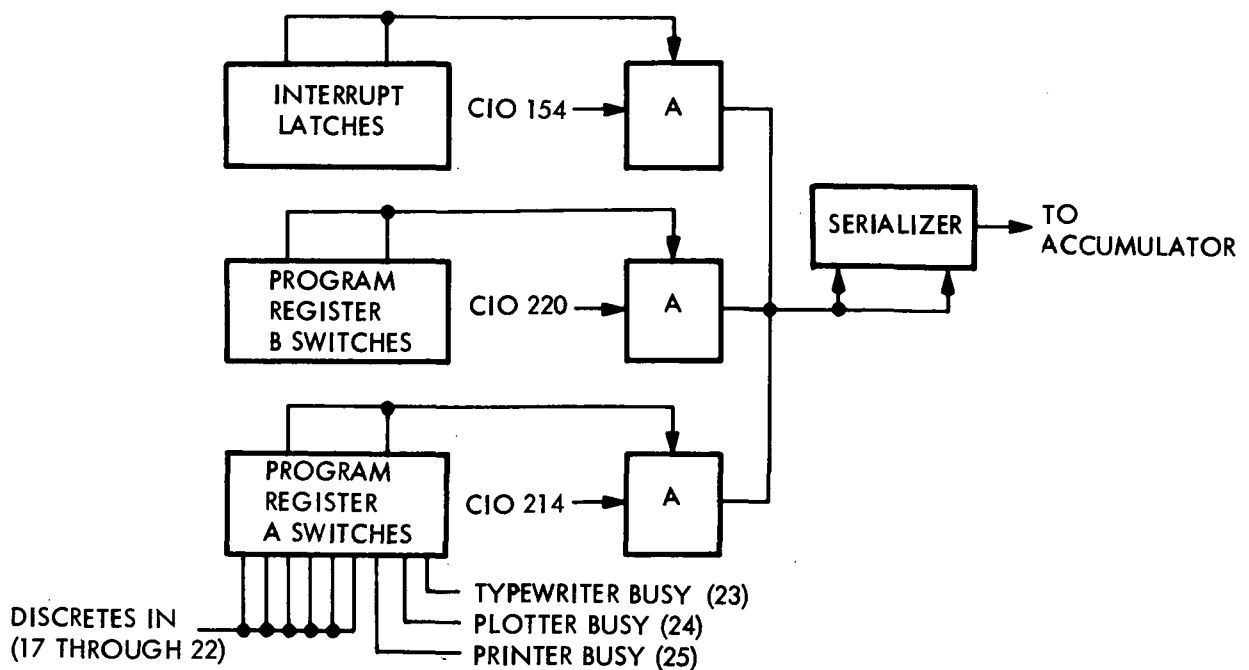


Figure 2-58. Input Serializer, Block Diagram

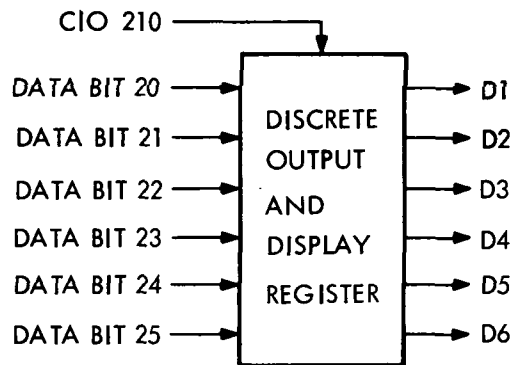


Figure 2-59. Discrete Output and Display Register, Block Diagram

2-362. PROGRAM CONTROL MODE DISPLAY REGISTER. (See block diagram, figure 2-60.)

2-363. The program control mode register is a six latch register (figure 10-28, sheet 7) used as a program tag for the programmers use only. The latches in the register are set by the six low order bits of the accumulator when a CIO 204 is programmed at A-1 time. As each latch is programmed to "set", a corresponding lamp is lit indicating a desired program sequence (e. g. , a pass count) has occurred.

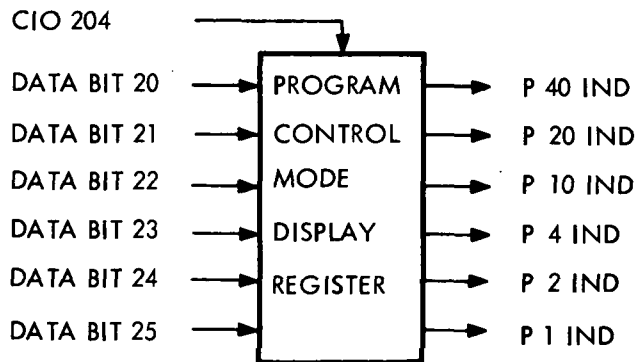


Figure 2-60. Program Control Mode, Block Diagram

SECTION III

INTERFACE AND CONTROLS

3-1. SCOPE.

3-2. This section describes the locations of all PTC interface connectors and references the drawings that identify the signal at each pin of these connectors. This section also describes the function of each control or indicator on the PTC control panels; drawings of the control panels are included in this section.

3-3. INTERFACE.

3-4. INTERFACE WITH LVDAME.

3-5. All of the PTC-LVDAME interface signals appear at pins of connectors 9009J1 through 9009J6 located on the left side feature strip of the 03 frame, shown on figure 3-1. The signals on the pins of these connectors are identified on figure 10-4, sheets 10, 13 through 18, 32, and 41.

3-6. INTERFACE WITH 1443 PRINTER.

3-7. All of the PTC-1443 Printer interface signals appear at the pins of connectors 01J3, 01J4, and 01J5 located on the left side of the 01 frame, shown on figure 3-2. The signals on the pins of these connectors are identified on figure 10-4, sheet 27.

NOTE

Connectors 01J6 through 01J12 shown on figure 3-2 are used for PTC self-check cables. The signals on the pins of these connectors are given on figure 10-4, sheets 20 through 24.

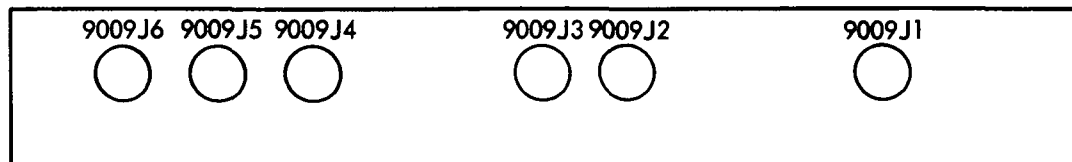


Figure 3-1. PTC-LVDAME Interface Panel

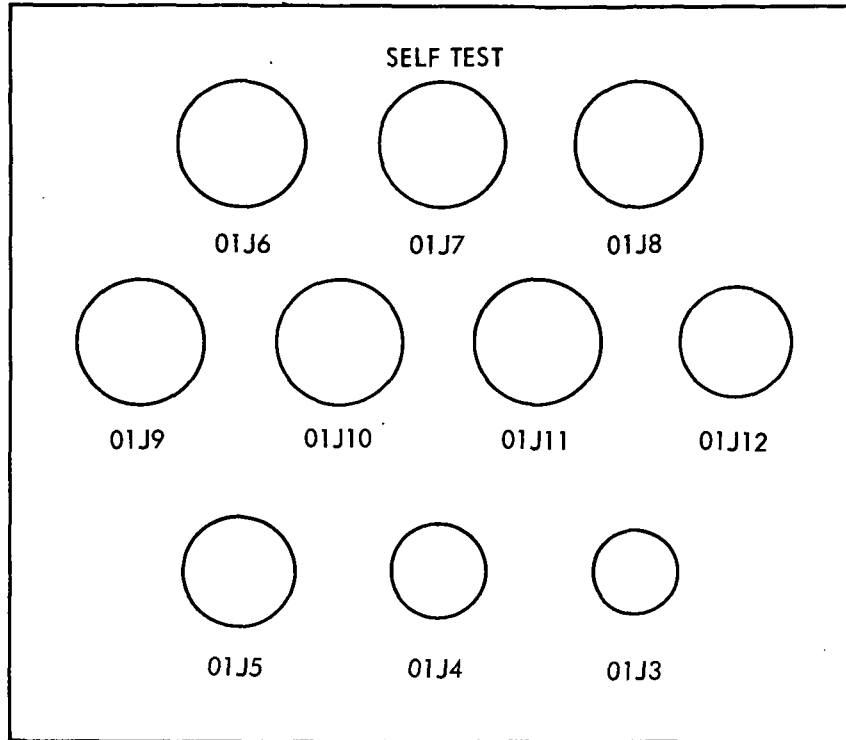


Figure 3-2. PTC-1443 Printer Interface Panel

3-8. INTERFACE WITH TYPEWRITER.

3-9. All of the PTC-Typewriter interface signals appear at the pins of plug 01P13, which connects to the 01J13 connector located on the rear of the typewriter. The signals on the pins of this plug are identified on figure 10-4, sheet 18.

3-10. CONTROLS AND INDICATORS.

3-11. The PTC operating controls and indicators are shown on figures 3-3 through 3-6; these controls and indicators are described in figure 3-7. The location of each control panel on the PTC is shown on figure 1-3.

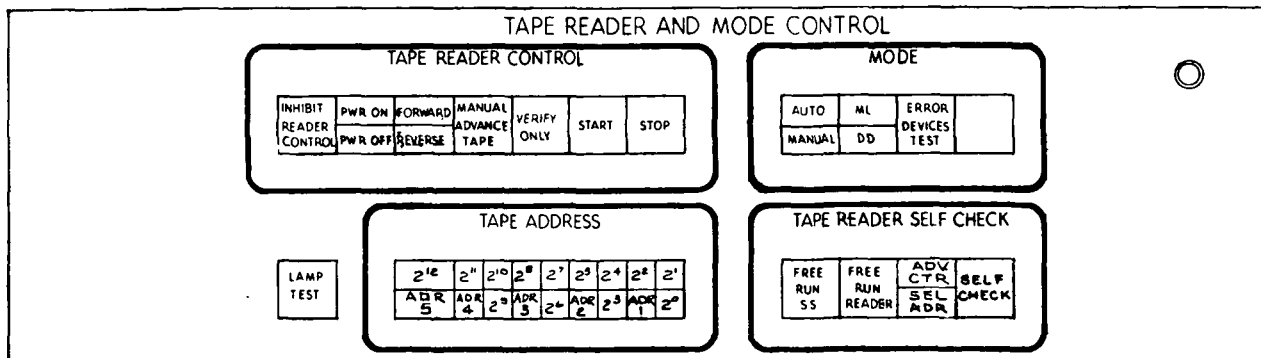


Figure 3-3. Tape Reader and Mode Control Panel

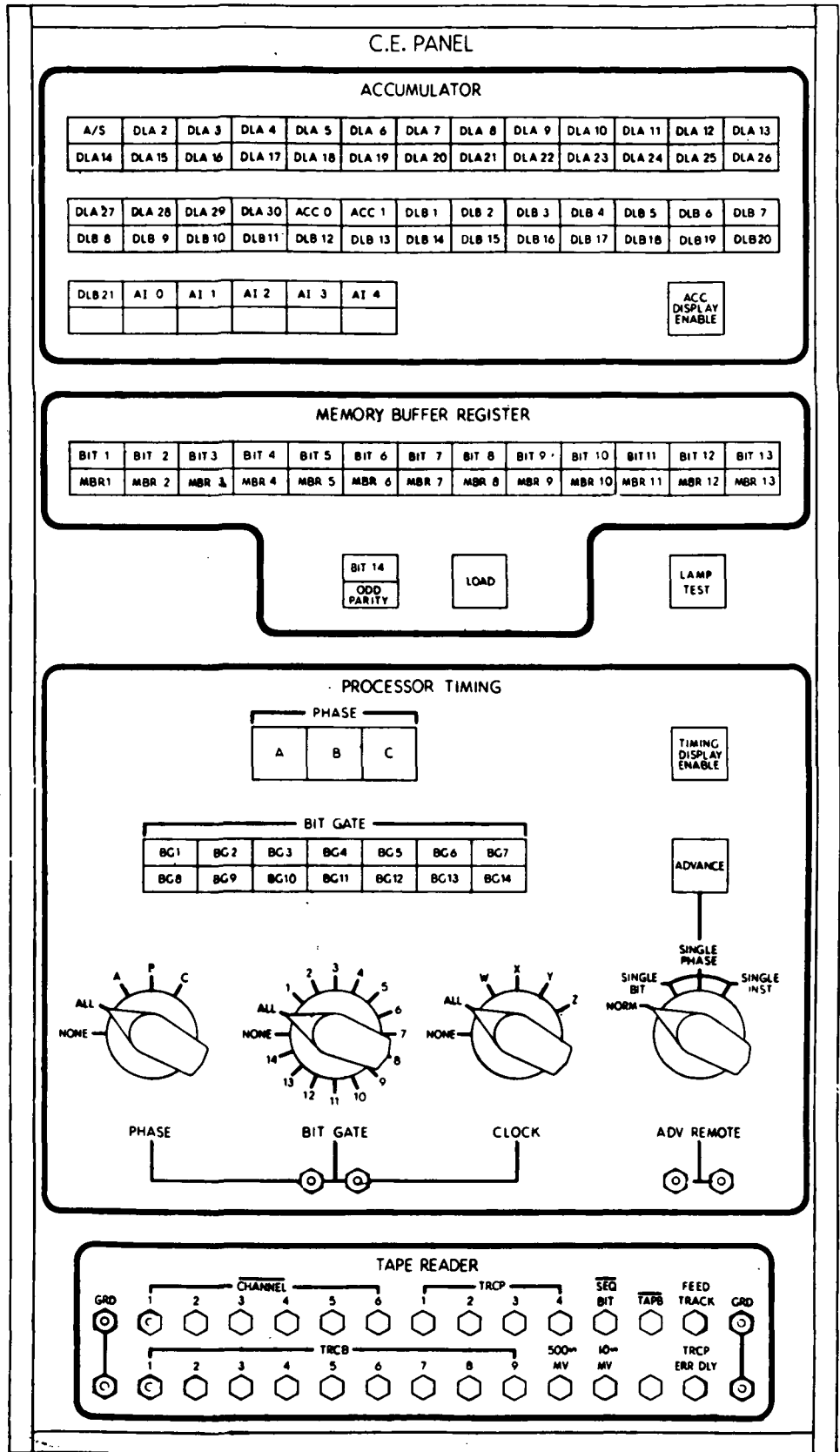


Figure 3-4. C. E. Panel

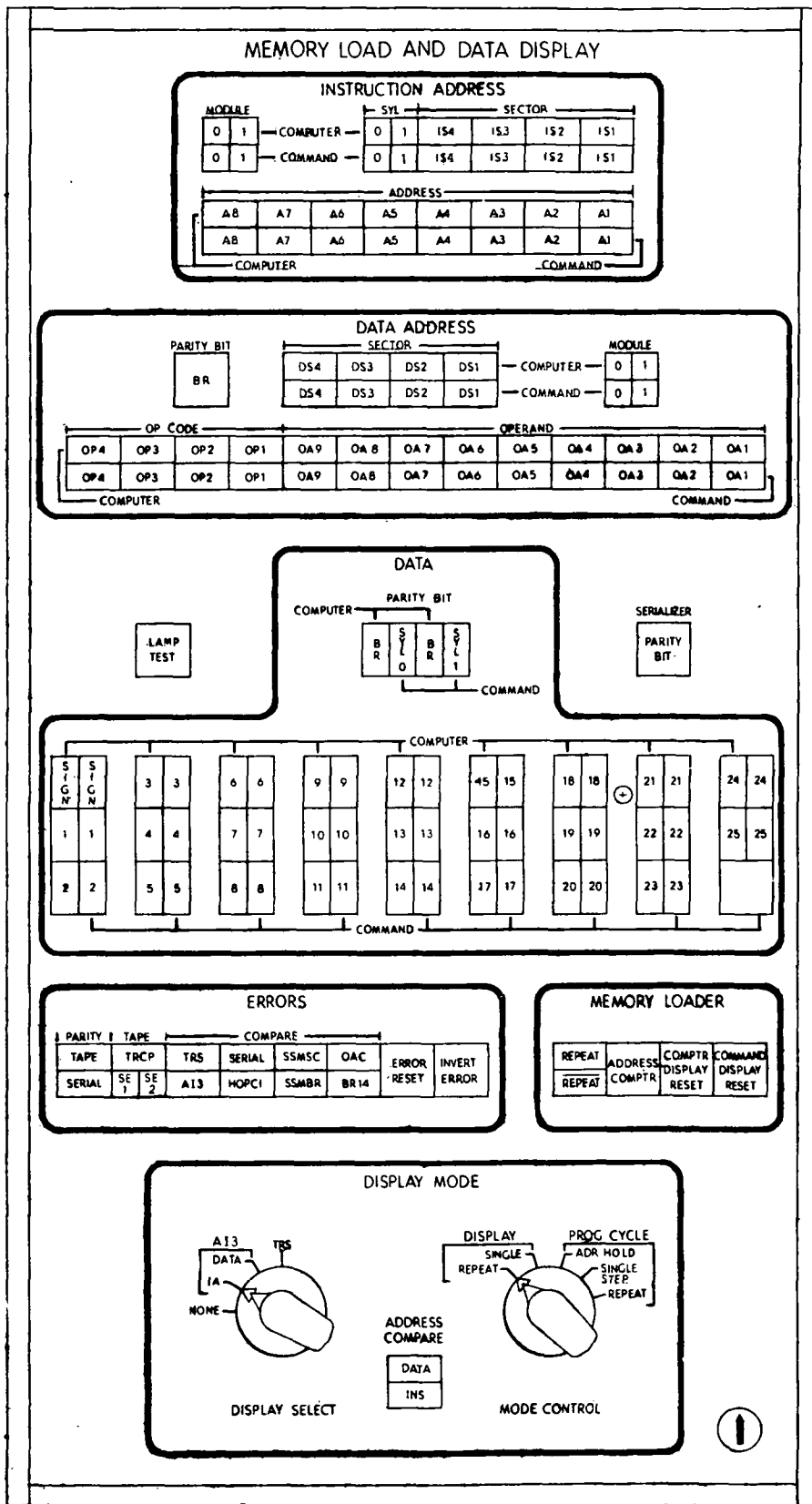


Figure 3-5. Memory Load and Data Display Panel

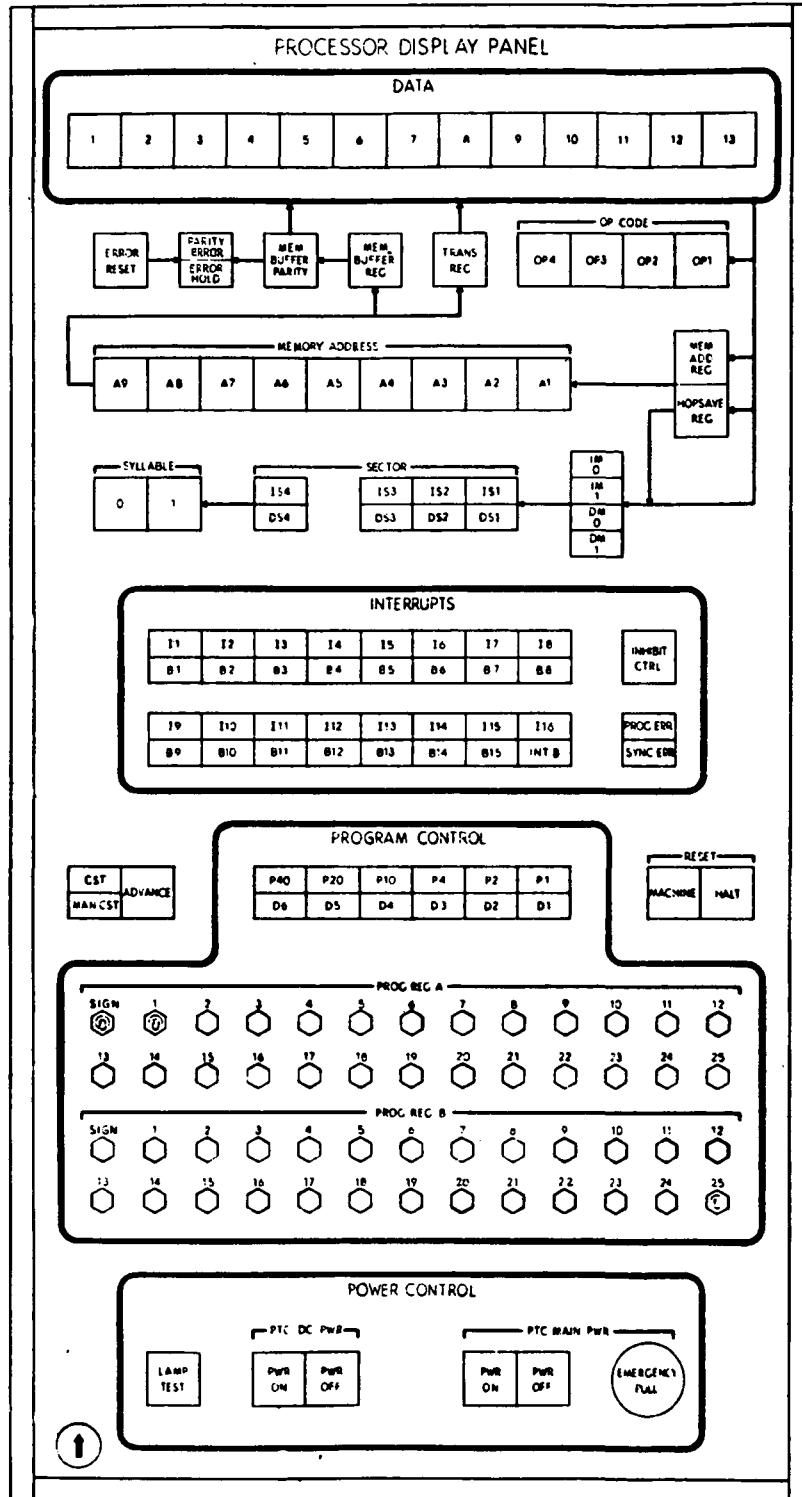


Figure 3-6. Processor Display Panel

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
<p>TAPE READER AND MODE CONTROL (figure 3-3)</p> <p>NOTE</p> <p>All reference designations for parts on this panel must be prefixed by 03A1, the reference designation for this panel.</p>	<p>TAPE READER CONTROL</p>	<p>INHIBIT READER CONTROL</p>	<p>S20, DS20</p>	<p>Alternate action pushbutton/lamp which turns off the tape spooler without turning off the tape reader.</p>
		<p>PWR ON/PWR OFF</p>	<p>S19, DS19</p>	<p>Alternate action pushbutton/lamp which controls application of main power to tape reader and spooler.</p>
		<p>FORWARD/REVERSE</p>	<p>S18, DS18</p>	<p>Alternate action pushbutton/lamp which controls tape direction.</p>
		<p>MANUAL ADVANCE TAPE</p>	<p>S17, DS17</p>	<p>Momentary action pushbutton/lamp which causes the tape to be manually advanced one tape word, in either the forward or reverse direction, as determined by the FORWARD/REVERSE switch. When lit, the lamp indicates that the tape must be advanced.</p>
		<p>VERIFY ONLY</p>	<p>S16, DS16</p>	<p>Alternate action pushbutton/lamp which inhibits the transfer of tape data to the central processor unit (DIN line) during a load operation or when a tape address of 00010 is programmed.</p>
		<p>START</p>	<p>S15, DS15</p>	<p>Momentary action pushbutton/lamp which starts the tape reader when the AUTO mode is selected.</p>
		<p>STOP</p>	<p>S14, DS14</p>	<p>Momentary action pushbutton/lamp which stops the tape reader.</p>
	<p>MODE</p>	<p>AUTO/MANUAL</p>	<p>S3, DS3</p>	<p>Alternate action pushbutton/lamp which allows the operator to load the memory from the tape reader (AUTO) or from the MEMORY LOAD AND DATA DISPLAY panel (MANUAL).</p>

Figure 3-7. Controls and Indicators (Sheet 1 of 17)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
TAPE READER AND MODE CONTROL (figure 3-3)	MODE	ML/DD	S2, DS2	Alternate action pushbutton/lamp. The ML position is used for memory loading or verifying. The DD position is used for displaying data from the Central Processor.
		ERROR DEVICES TEST	S1, DS1	Momentary action pushbutton/lamp which sets the latches that control the ERROR lamps on the MEMORY LOAD AND DATA DISPLAY panel. This checks the output latch, the lamp driver, and the lamp.
		Blank		Not used.
	TAPE ADDRESS	ADR 1 through 5 2 ⁰ through 2 ¹²	S4, DS4 through S8, DS8 S4, DS4 through S8, DS8	Alternate action pushbutton/lamps that indicate the address bits (of the tape format) of the tape word being read. These bits do not indicate actual tape addresses, but instead they initiate PTC functions. These pushbuttons can be used to manually insert address bits into the tape reader register when the SEL ADR portion of the SEL ADR/ADV CTR switch is lit. Special action pushbutton/lamps that indicate the contents of the binary counter which counts the tape sequence bits in the AUTO mode when the tape reader is running forward. In the MANUAL mode the counter is controlled by the pushbuttons when the ADV CTR portion of the SEL ADR/ADV CTR switch is lit. (Refer to paragraph 3-22.)
	TAPE READER SELF CHECK	FREE RUN SS	S13, DS13	Alternate action pushbutton/lamp that causes all single shots, counters, and delays to cycle continuously during self-check.

Figure 3-7. Controls and Indicators (Sheet 2)

Panel	Area	Control/Indicator	Ref Des.	Description and Function
TAPE READER AND MODE CONTROL (figure 3-3)	TAPE READER SELF CHECK	FREE RUN READER	S12, DS12	Alternate action pushbutton/lamp that starts or stops the tape reader and tape spooler during self-check. (This switch by-passes the RUN tratch.)
		SEL ADR/ADV CTR	S11, DS11	Alternate action pushbutton/lamp that allows word counter (2 ⁰ through 2 ¹²) to be manually advanced when ADV CTR is lit. SEL ADR allows manual selection of the tape address (ADR 1 through ADR 5).
C. E. PANEL (figure 3-4)		SELF CHECK	S21, DS21	Alternate action pushbutton/lamp that enables the PTC self-check circuits.
	None	LAMP TEST	S10	Momentary action pushbutton used to check all indicator lamps on this panel.
	ACCUMULATOR	A/S and DLA 2 through DLA 26 (26 lamps); DLA 27 through 30, ACC 0, ACC 1, and DLB 1 through 20 (26 lamps); DLB 21 and AI 0 through 4 (6 lamps)	DS1 through DS26 and DS28 through DS33	Indicator lamps that show the state of all latches in the Central Processor accumulator.
NOTE All reference designations for parts on this panel must be prefixed by 03A4, the reference designation for this panel.		ACC DISPLAY ENABLE	S1, DS27	Alternate action pushbutton/lamp that disables the ACCUMULATOR display if the Central Processor is not being checked.
	MEMORY BUFFER REGISTER	BIT 1 through BIT 13 (top row lamps) and MBR 1 through MBR 13 (bottom row lamps)	S2, DS34 through S14, DS46	Alternate action pushbutton/lamps. The top row of lamps display data that has been loaded into the memory buffer register. The bottom row of lamps display data to be loaded into the memory buffer register.

Figure 3-7. Controls and Indicators (Sheet 3)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
C. E. PANEL (figure 3-4)	MEMORY BUFFER REGISTER	BIT 14/ODD PARITY	S17, DS49	Alternate action pushbutton/lamp that provides odd parity situation if MBR switches are in an even condition (ODD PARITY lamp lit). The BIT 14 lamp displays parity bit that has been loaded into the memory buffer register.
	ACCUMULATOR	LOAD	S16	Momentary action pushbutton that transfers data from MEMORY BUFFER REGISTER switches (MBR 1 MBR 13) into the memory buffer register. The memory buffer register can be loaded only during single phase operation.
	PROCESSOR TIMING	PHASE - A, B, and C BIT GATE - BG1 through BG14 TIMING DISPLAY ENABLE PHASE, BIT GATE, and CLOCK NORM, SINGLE BIT, SINGLE PHASE, and SINGLE INST	DS51, DS52, DS53 DS55 through DS61 S18, DS50 S21, S22, S23, and TP3, TP4 S20	Indicator lamps that display the phase at which the processor timing stops. Indicator lamps that display the bit gate at which the processor timing stops. Alternate action pushbutton/lamp that disables timing displays if processor timing is not being checked. Rotary switches and test jacks (two) that provide the phase, bit gate, and clock pulse to be used externally for oscilloscope synchronization during trouble shooting. Rotary switch which selects the mode of timing performance, as follows: NORM: Normal timing operation. SINGLE BIT: Timing stops at clock pulse Z. It can be advanced to the next clock pulse Z by the ADVANCE switch on either this or the PROCESSOR DISPLAY panel, or remotely via the ADV REMOTE jacks on this panel.

Figure 3-7. Controls and Indicators (Sheet 4)

Panel	Area	Control Indicator	Ref. Des.	Description and Function
C. E. PANEL (figure 3-4)	PROCESSOR TIMING	NORM, SINGLE BIT, SINGLE PHASE, and SINGLE INST (cont)	S20	<p>SINGLE PHASE: Timing stops at A-10-Z, B-2-Z, or C-1-Z time. The timing can be advanced through these successive steps by the ADVANCE switch on either this or the PROCESSOR DISPLAY panel, or remotely via the ADV REMOTE jacks on this panel.</p> <p>SINGLE INST: Timing stops at A-10-Z time. The timing can be advanced to the next A-10-Z time (one cycle) by the ADVANCE switch on either this or the PROCESSOR DISPLAY panel, or remotely via the ADV REMOTE jacks on this panel.</p>
		ADVANCE	S19	<p>Momentary action pushbutton used to advance the timing as described for the NORM, SINGLE BIT, SINGLE PHASE, and SINGLE INST switches. This pushbutton/lamp is also used to control the Central Processor during a CST condition.</p>
		ADV REMOTE	TP1, TP2	<p>Jacks to which an external (remote) switch can be applied. The switch provides the same function as ADVANCE.</p>
	TAPE READER	GRD, CHANNEL, TRCP, SEQ BIT, TAPB, FEED TRACK, GRD, TRCB, 500~MV, 10~MV, and TRCP ERR DLY	TP5 through TP34	<p>Test points that monitor various signals in the tape reader control logic.</p>
	None	LAMP TEST	S15	<p>Momentary action pushbutton used to check all indicator lamps on this panel.</p>

Figure 3-7. Controls and Indicators (Sheet 5)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
<p>MEMORY LOAD AND DATA DISPLAY (figure 3-5)</p> <p>NOTE</p> <p>All reference designations for parts on this panel must be prefixed by 02A1, the reference designation for this panel.</p>	INSTRUCTION ADDRESS	MODULE - 0/1	S6, DS6	<p>Alternate action pushbutton/lamp that controls the one-bit memory module selection code when reference to memory is made for an instruction. The lower (COMMAND) lamps indicate the module to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor memory module compared on.</p>
		SYL - 0/1	S5, DS5	<p>Alternate action pushbutton/lamp that selects either syllable 0 or syllable 1 for instruction word. The lower (COMMAND) lamps indicate commanded syllable to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor memory syllable compared on.</p>
		SECTOR - IS 1 through IS 4	S1, DS1 through S4, DS4	<p>Alternate action pushbutton/lamps that control the four-bit instruction sector address code. The lower (COMMAND) lamps indicate commanded sector address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor memory sector address bits compared on.</p>
		ADDRESS - A1 through A8	S7, DS7 through S14, DS14	<p>Alternate action pushbutton/lamps that control the eight-bit instruction address code. The lower (COMMAND) lamps indicate commanded memory instruction address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor memory instruction address bits compared on.</p>

Figure 3-7. Controls and Indicators (Sheet 6)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DATA ADDRESS	PARITY BIT - BR SECTOR - DS1 through DS4	DS20 S16, DS16 through S19, DS19	Indicator lamp that indicates the presence of instruction word parity in the Central Processor memory buffer register. Alternate action pushbutton/lamps that control the four-bit data sector address code. The lower (COMMAND) lamps indicate the commanded data sector address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor memory data sector address bits compared on.
	INSTRUCTION ADDRESS	MODULE - 0/1	S15, DS15	Alternate action pushbutton/lamp that controls the one-bit memory module selection code when reference is made to memory for data. The lower (COMMAND) lamps indicate the data memory module to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor data memory module compared on.
	DATA ADDRESS	OP CODE - OP 1 through OP 4 OPERAND - OA 1 through OA 9	S29, DS30 through S32, DS33 S20, DS21 through S28, DS29	Alternate action pushbutton/lamps that control Central Processor operation code bits (ML mode only). The lower (COMMAND) lamps indicate the commanded operation code bits to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor operation code bits compared on. Alternate action pushbutton/lamps that control Central Processor operand address code bits. The lower (COMMAND) lamps indicate the commanded operand address code bits to be used for compare; the upper (COMPUTER) lamps indicate the actual Central Processor operand address code bits compared on.

Figure 3-7. Controls and Indicators (Sheet 7)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function									
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	None	LAMP TEST	S33	Momentary action pushbutton used to check all indicator lamps on this panel.									
		SERIALIZER - PARITY BIT	DS34	Indicator lamp that indicates odd parity in the tape reader register.									
	DATA	PARITY BIT - BR	DS35, DS36	Indicator lamps that indicate the presence of Central Processor buffer register data parity bits.									
		PARITY BIT - SYL 0 and SYL 1	DS35, DS36	Indicator lamps that indicate the presence of data word (COMMAND) parity bits in syllables 0 and 1.									
		SIGN through 25	S34, DS38 through S59, DS63	Alternate action pushbutton/lamps that control the bits of a data word to be loaded into the Central Processor. The lamps on the right half of the pushbuttons indicate the commanded bits; the lamps on the left display the actual Central Processor data bits.									
		Blank		Not used.									
	ERRORS	Refer to Description and Function column.		Lamps that indicate errors as follows:									
			DS75	<table border="0"> <tr> <td><u>Section</u></td> <td><u>Lamp</u></td> <td><u>Type of Error</u></td> </tr> <tr> <td>PARITY</td> <td>{ TAPE SERIAL</td> <td>Tape parity Serial parity</td> </tr> <tr> <td>TAPE</td> <td>{ TRCP SE 1 SE 2</td> <td>Tape reader clock pulse Tape sequence Tape sequence</td> </tr> </table>	<u>Section</u>	<u>Lamp</u>	<u>Type of Error</u>	PARITY	{ TAPE SERIAL	Tape parity Serial parity	TAPE	{ TRCP SE 1 SE 2	Tape reader clock pulse Tape sequence Tape sequence
<u>Section</u>	<u>Lamp</u>	<u>Type of Error</u>											
PARITY	{ TAPE SERIAL	Tape parity Serial parity											
TAPE	{ TRCP SE 1 SE 2	Tape reader clock pulse Tape sequence Tape sequence											
			DS74										

Figure 3-7. Controls and Indicators (Sheet 8)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function																											
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	ERRORS	Refer to Description and Function column. (cont)	DS73	<table border="0"> <tr> <td><u>Section</u></td> <td><u>Lamp</u></td> <td><u>Type of Error</u></td> </tr> <tr> <td></td> <td>TRS</td> <td>Transfer register serial output compare</td> </tr> <tr> <td></td> <td>SERIAL</td> <td>Serial compare</td> </tr> <tr> <td></td> <td>SSMSC</td> <td>Sector/syllable/module serial compare</td> </tr> <tr> <td></td> <td>OAC</td> <td>Operand Address compare</td> </tr> <tr> <td></td> <td>AI3</td> <td>Accumulator data compare</td> </tr> <tr> <td></td> <td>HOPC1</td> <td>HOP constant compare</td> </tr> <tr> <td></td> <td>SSMBR</td> <td>Sector/syllable/module buffer register compare</td> </tr> <tr> <td></td> <td>BR14</td> <td>Parity bit compare</td> </tr> </table>	<u>Section</u>	<u>Lamp</u>	<u>Type of Error</u>		TRS	Transfer register serial output compare		SERIAL	Serial compare		SSMSC	Sector/syllable/module serial compare		OAC	Operand Address compare		AI3	Accumulator data compare		HOPC1	HOP constant compare		SSMBR	Sector/syllable/module buffer register compare		BR14	Parity bit compare
	<u>Section</u>		<u>Lamp</u>	<u>Type of Error</u>																											
	TRS	Transfer register serial output compare																													
	SERIAL	Serial compare																													
	SSMSC	Sector/syllable/module serial compare																													
	OAC	Operand Address compare																													
	AI3	Accumulator data compare																													
	HOPC1	HOP constant compare																													
	SSMBR	Sector/syllable/module buffer register compare																													
	BR14	Parity bit compare																													
			DS72 DS71 DS70 DS73 DS72 DS71 DS70	<p>COM-PARE</p> <p>Momentary action pushbutton that resets all indicators in the ERRORS area on this panel.</p> <p>Indicator lamp that indicates the condition of the invert error latch.</p>																											
	DISPLAY MODE	DISPLAY SELECT	S67	<p>Rotary switch that selects data for display as follows:</p> <table border="0"> <tr> <td><u>Position</u></td> <td><u>Type of Data</u></td> </tr> <tr> <td>NONE</td> <td>None</td> </tr> <tr> <td>AI3-IA</td> <td>Instruction address</td> </tr> <tr> <td>AI3-DATA</td> <td>Accumulator data</td> </tr> <tr> <td>TRS</td> <td>Transfer register serial</td> </tr> </table>	<u>Position</u>	<u>Type of Data</u>	NONE	None	AI3-IA	Instruction address	AI3-DATA	Accumulator data	TRS	Transfer register serial																	
<u>Position</u>	<u>Type of Data</u>																														
NONE	None																														
AI3-IA	Instruction address																														
AI3-DATA	Accumulator data																														
TRS	Transfer register serial																														

Figure 3-7. Controls and Indicators (Sheet 9)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DISPLAY MODE	ADDRESS COMPARE - DATA/INS	S65, DS76	Alternate action pushbutton/lamp that selects either the operand (DATA ADDRESS) data or the INSTRUCTION ADDRESS data to be compared to the actual memory address data.
	MEMORY LOADER	REPEAT/ <u>REPEAT</u>	S63, DS67	Alternate action pushbutton/lamp that causes the selected memory location to be loaded and verified repeatedly (REPEAT) or just once (REPEAT). (See ADDRESS COMPTR control.)
		ADDRESS COMPTR	S62	Momentary action pushbutton that causes the memory location to be loaded and verified just once when the <u>REPEAT</u> portion of the REPEAT/ <u>REPEAT</u> switch is lit.
		COMPTR DISPLAY RESET	S61	Momentary action pushbutton that resets all Central Processor display latches, causing the lamps connected to the set outputs of these latches to be extinguished. The lamps connected to the reset sides of these latches will be lit. The 0 (COMPUTER) portions of MODULE - 0/1 and SYL - 0/1 in the INSTRUCTION ADDRESS area and MODULE 0/1 in the DATA ADDRESS area will be lit.
		COMMAND DISPLAY RESET	S60	Momentary action pushbutton that switches off all COMMAND switches. The indicator lamps connected to these switches will indicate the off condition. The 0 (COMMAND) portions of MODULE - 0/1 and SYL - 0/1 in the INSTRUCTION ADDRESS area and MODULE 0/1 in the DATA ADDRESS area will be lit.

Figure 3-7. Controls and Indicators (Sheet 10)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DISPLAY MODE	MODE CONTROL	S66	<p>Rotary switch that selects display mode of operation as follows:</p> <p><u>Position</u></p> <p>DISPLAY - REPEAT</p> <p><u>Type of Operation</u></p> <p>The Central Processor runs normally under program control. Each time the Central Processor address (either data address or instruction address, as determined by the ADDRESS COMPARE - DATA INS switch) coincides with that selected by the panel switches (DATA ADDRESS or INSTRUCTION ADDRESS switches), a new display of data is generated in the DATA lamps.</p> <p>DISPLAY - SINGLE</p> <p>The DATA lamps display data (selected by the DISPLAY SELECT switch) generated during the first operation cycle in which the Central Processor address (either data address or instruction address, as determined by the ADDRESS COMPARE - DATA/INS switch) coincides with that selected by the panel switches (DATA ADDRESS or INSTRUCTION ADDRESS). The Central Processor will continue to "free run", but no further displays will be generated until</p>

Figure 3-7. Controls and Indicators (Sheet 11)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DISPLAY MODE	MODE CONTROL (cont)		<p data-bbox="349 945 381 1050"><u>Position</u></p> <p data-bbox="349 1050 381 1260">the COMPTR DISPLAY RESET switch is pressed.</p> <p data-bbox="349 1260 381 1470"><u>Type of Operation</u></p> <p data-bbox="349 1470 381 1837">Upon address compare, the Central Processor is forced into a CST condition. When the ADVANCE switch on the C. E. PANEL or PROCESSOR DISPLAY PANEL is pressed, the Central Processor shall "free run" until another address compare occurs.</p>
				<p data-bbox="511 357 544 420">PROG</p> <p data-bbox="511 420 544 630">CYCLE -</p> <p data-bbox="511 630 544 735">ADR HOLD</p> <p data-bbox="511 735 544 840">Upon address compare, a CST condition is forced upon the Central Processor. The current Central Processor address and data are displayed on the panel indicators. When the ADVANCE switch (on the C. E. PANEL or PROCESSOR DISPLAY PANEL) is pressed, the Central Processor performs the next instruction in the program, and then another CST condition is forced.</p>
				<p data-bbox="673 357 706 420">PROG</p> <p data-bbox="673 420 706 630">CYCLE -</p> <p data-bbox="673 630 706 735">SINGLE</p> <p data-bbox="673 735 706 840">STEP</p> <p data-bbox="673 840 706 1050">Upon address compare, the Central Processor operation is halted, forcing instruction module 0 sector 0, syllable 0, and address 000g to be</p>

Figure 3-7. Controls and Indicators (Sheet 12)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DISPLAY MODE	MODE CONTROL (cont)		<p><u>Position</u></p> <p><u>Type of Operation</u></p> <p>selected. The Central Processor then resumes operating until another address compare occurs.</p>
PROCESSOR DISPLAY PANEL (figure 3-6)	DATA	1 through 13	DS1 through DS13	Indicator lamps that display the contents of the transfer register or the memory buffer register.
NOTE	None	OP CODE - OP 1 through OP 4	DS14 through DS17	Indicator lamps that display the contents of the op code register.
All reference designations for parts on this panel must be prefixed by 02A2, the reference designation for this panel.		MEM ADD REG	S5, DS23	Alternate action pushbutton/lamp which causes the contents of the memory address register to be displayed.
		HOPSAVE REG	S6, DS24	Alternate action pushbutton/lamp which causes the contents of the HOPSAVE register to be displayed by the DATA lamps. NOTE: If the MEM ADD REG and the HOPSAVE REG lamps are both lit or both not lit, nothing will be displayed.
		IM 0/IM 1	DS34	Indicator lamps (2) which indicate whether instruction module 0 or 1 is selected.
		DM 0/DM 1	DS35	Indicator lamps (2) which indicate whether data module 0 or 1 is selected.
		SECTOR - IS 1/DS 1 through IS 4/DS 4	DS36 through DS39	Indicator lamps which display the contents of the instruction sector register and the data sector register.

Figure 3-7. Controls and Indicators (Sheet 13)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
PROCESSOR DISPLAY PANEL (figure 3-6)	None	SYLLABLE - 0, 1 MEMORY ADDRESS - A1 through A9 TRANS REG MEM BUFFER REG	DS40, DS41 DS25 through DS33 S1, DS18 S2, DS19	Indicator lamps that indicate the module syllable from which an instruction is read. Indicator lamps that display the contents of the memory address register. Alternate action pushbutton/lamp that allows the contents of the transfer register to be displayed by the DATA lamps. Alternate action pushbutton/lamp that allows the contents of the memory buffer register to be displayed by the DATA lamps. NOTE: If the TRANS REG and the MEM BUFFER REG lamps are both lit or both not lit, nothing will be displayed.
		MEM BUFFER PARITY	DS20	Indicator lamp which displays the memory buffer parity bit.
		PARITY ERROR/ERROR HOLD	S3, DS21	Alternate action pushbutton/lamp. PARITY ERROR displays the parity error latch condition. ERROR HOLD will cause the machine to CST and display the address of the instruction on which follows the instruction having the error.
		ERROR RESET	S4	Momentary action pushbutton that resets the error latch. When in ERROR HOLD condition, this switch will not take the Central Processor out of CST; ADVANCE switches on this panel or C. E. PANEL will take machine out of CST.

Figure 3-7. Controls and Indicators (Sheet 14)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
PROCESSOR DISPLAY PANEL (figure 3-6)	INTERRUPTS	I1/B1 through I15/B15	S8, DS43 through S15, DS50 and S18, DS53 through S24, DS59	Momentary action pushbutton/lamps. I1 through I15 are lamps that indicate the Interrupt that is stored in the Interrupt register. B1 through B15 are the lamps that indicate the interrupt inhibits. The pushbuttons are used to manually remove the inhibiting of the interrupts.
		I16/INT B	S17, DS52	Momentary action pushbutton/lamp that initiates the processing of Interrupt number 16. No provision is made to inhibit this interrupt. The INT B lamp is lit when the INT B latch is set. The INT B latch is set during the processing of an interrupt, this latch must be reset by C10 I10 before the processing of another interrupt is begun.
		INHIBIT CTRL	S7, DS42	Alternate action pushbutton/lamp that sets all inhibit latches and prevents Interrupt from being processed. If the INHIBIT CTRL is ON, the individual Interrupt pushbuttons can be used to reset the Inhibit latches allowing associated Interrupts to be recognized. If the INHIBIT CTRL is OFF, the Inhibit latches are under program control only.
		PROGRAM ERROR/SYNC ERROR	S16, DS51	Momentary action pushbutton/lamp. The PROGRAM ERROR portion becomes lit when the program detects an error; when the switch face is pressed, the program error indication circuit is reset and the lamp is extinguished. The SYNC ERROR portion becomes lit when the timing circuits are out of synchronization; this error indication circuit is reset (and the lamp extinguished) when the RESET - MACHINE switch is pressed.

Figure 3-7. Controls and Indicators (Sheet 15)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
PROCESSOR DISPLAY PANEL (figure 3-6)	None	CST/MAN CST	S28, DS69	Alternate action pushbutton/lamp. The pushbutton places the PTC in the CST (Computer Single Step) mode of operation. The MAN CST lamp is controlled by the pushbutton switch; the CST lamp indicates that the PTC is in the CST mode. When the ADVANCE switch is pressed, the Central Processor performs the next instruction in its program.
		ADVANCE		Momentary action pushbutton used to advance the timing as described for the timing mode switch (NORM, SINGLE BIT, SINGLE PHASE, SINGLE INST) on the C. E. PANEL panel. This pushbutton/lamp is also used to control the Central Processor operation during a CST condition.
		RESET - MACHINE	S25	Momentary action pushbutton that resets the Central Processor control latches and causes operation to be resumed with instruction module 0, sector 0, syllable 0, and address 000g selected.
		RESET - HALT		Pushbutton that disables the RUN latch, forcing Central Processor operation to be resumed with instruction module 0, sector 0, syllable 0, and address 000g selected.
	PROGRAM CONTROL	P1, P2, P4, P10, P20 and P40	DS62 through DS67	Indicator lamps which display the six low order bits of the data word from the accumulator upon command C10 204.
		D1 through D6	DS62 through DS67	Indicator lamps which display the six discrete outputs from the PTC upon command C10 210.

Figure 3-7. Controls and Indicators (Sheet 16)

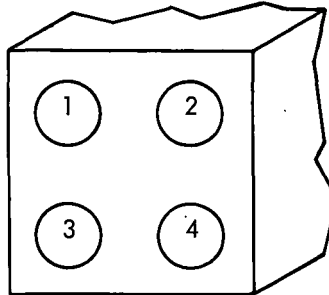
Panel	Area	Control/Indicator	Ref. Des.	Description and Function
PROCESSOR DISPLAY PANEL (figure 3-6)	PROGRAM CONTROL	PROG REG A-SIGN and 1 through 25 and PROG REG B-SIGN and 1 through 25	S29 through S80	Toggle switches which provide a means of entering two data words (26 bits) into the Central Processor accumulator. Bits positions 17 through 22 (PROG REG A) can accept six externally generated discrete inputs. Bit position 23 (PROG REG A) is used to indicate that the typewriter is BUSY; bit position 24 (PROG REG A) is used to indicate that the plotter is BUSY, and bit position 25 (PROG REG A) is used to indicate that the printer is BUSY. If the discrete switches are OFF (down position), the discrete signal is entered ("0" or "1"). If the discrete switches are ON (up position), the discrete are overridden, and the positions always contain a "1".
	POWER CONTROL	LAMP TEST PTC DC PWR - PWR ON PTC DC PWR - PWR OFF PTC MAIN PWR - POWER ON PTC MAIN PWR - POWER OFF PTC MAIN PWR - EMERGENCY PULL	S86 S85, DS72 S84, DS71 S83, DS80 S82, DS70 S81	Momentary action pushbutton which is used to check all indicator lamps on this panel. Momentary action pushbutton/lamp that starts the PTC DC power-on sequence and indicates when lit that sequencing is complete. Momentary action pushbutton/lamp that starts the PTC DC power-off sequence and indicates when lit that sequencing is complete. Momentary action pushbutton/lamp that starts the PTC AC power-on sequence and indicates when lit that sequencing is complete. Momentary action pushbutton/lamp that starts the PTC AC power-off sequence and indicates when lit that sequencing is complete. Switch that removes (when pulled) all PTC power.

Figure 3-7. Controls and Indicators (Sheet 17)

3-12. In addition to the controls and indicators described in figure 3-7, the Filter-Interlock Gate Assembly (01B5) at the rear of the PTC contains an elapsed time meter (9999.9 hour) and the circuit breakers for the PTC input power.

3-13. The controls and indicators on the commercial equipment in the PTC (plotter 01A1 and power supplies 03A6 through 03A11) are described in the commercial manuals for these units. (Refer to the list of related manuals in the front of this volume.)

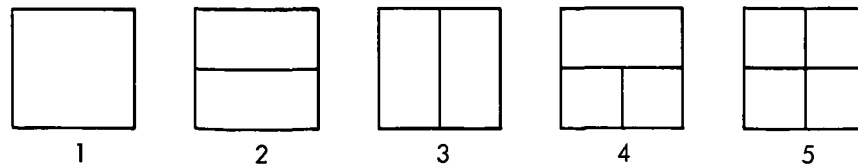
3-14. Many of the PTC controls and indicators are pushbutton switches housed with four lamp bulbs that light under certain conditions. The four bulbs (1, 2, 3 and 4) are arranged as shown here:



3-15. These bulbs can be wired in many configurations; the following five configurations are used on the PTC.

1. Bulbs 1 and 3 constitute one indication.
2. Bulb 1 or bulb 2 constitutes one indication; bulb 3 or bulb 4 constitutes a second indication.
3. Bulb 1 or bulb 4 constitutes one indication; bulb 2 or bulb 3 constitutes a second indication.
4. Bulb 1 or bulb 2 constitutes one indication; bulb 3 constitutes a second indication; and bulb 4 constitutes a third indication.
5. Each lamp constitutes a different indication.

3-16. These wiring configurations, listed in paragraph 3-15, correspond to the following patterns on the switch faces:



NOTE

Some indicator lamps are housed with pushbutton switches to which they are not electrically connected. The indications given by these lamps are explained in figure 3-7.

3-17. PUSHBUTTON SWITCH NOMENCLATURE. The nomenclature discussed in the following paragraphs is used in figure 3-7.

3-18. Momentary Action Pushbutton. A momentary action pushbutton is a momentary action pushbutton switch. The function controlled by the switch is a "1" only while the switch face (button) is being pressed.

3-19. Momentary Action Pushbutton/lamp. A momentary action pushbutton/lamp is a momentary action pushbutton switch housed with lamp bulbs. The function controlled by the switch is in the "1" state only while the bulbs within the switch assembly are lit. Normally the bulbs become lit when the switch face (button) is pressed (or soon afterward) and remain lit until another switch is pressed, forcing the bulbs of the first switch to be extinguished. For example, the PWR ON and PWR OFF switches shown here operate in this manner:



When power is off, PWR OFF is lit, and PWR ON is not lit. When PWR ON is pressed, PWR OFF becomes not lit and PWR ON becomes lit when the power-on sequencing is complete. When PWR OFF is pressed, PWR ON becomes not lit and PWR OFF becomes lit when power-off sequencing is complete.

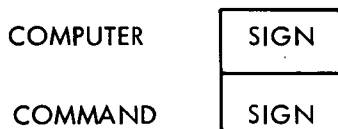
3-20. As noted in paragraph 3-16, some of the bulbs housed in certain switch assemblies are not electrically connected to the switches in the assemblies. In some cases certain bulbs are independent of the state of the switch with which they are housed while the others in that housing are directly controlled by the switch. In other cases the bulbs become lit when errors occur, and the switch in that assembly is used to reset the error indication circuit that controls the bulbs; a momentary action switch is normally used for this purpose. These special switch configurations are described in figure 3-7.

3-21. Alternate Action Pushbutton/lamp. An alternate action pushbutton/lamp is a DPDT pushbutton switch housed with lamp bulbs; the state of the switch is complemented by pressing the switch face. The lamp bulbs may be wired in one of the following ways:

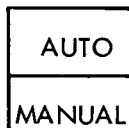
1. Bulbs within the switch assembly are lit only when the function the switch controls is a "1". For example, the SELF CHECK alternate action pushbutton/lamp shown here is lit only while a self-check operation is in progress.



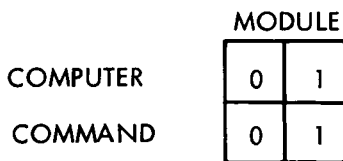
2. The type of indication discussed in item 1 can be restricted to one half of a switch face. For example, in the SIGN switch shown here, the lamps in the lower (COMMAND) portion function as described in item 1; the lamps in the upper (COMPUTER) portion indicate the SIGN output from the Central Processor ("1" if lit, "0" if not lit). The lamps in the upper portion are not electrically connected to the switch. (This type of operation was noted in paragraph 3-16.)



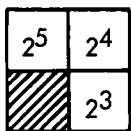
3. A bulb (or bulbs) is always lit to indicate the state of the function controlled by the switch. For example the AUTO portion of the AUTO/MANUAL alternate action pushbutton/lamp shown here is lit only when the automatic mode of operation is selected; when the AUTO portion is lit, the MANUAL portion is not lit, and vice versa.



4. The type of indication discussed in item 3 can be restricted to one half of a switch face. For example, in the MODULE-0/1 switch shown here, the lamp bulbs in the lower (COMMAND) portion function as described in item 3; the lamp bulbs in the upper (COMPUTER) portion indicate the module output from the Central Processor. The lamps in the upper portion are not electrically connected to the switch.



3-22. Special Action Pushbutton/lamp. A special action pushbutton/lamp is a momentary action pushbutton switch housed with lamp bulbs that light in a binary counting sequence. The face of each switch is partitioned into four sections as shown here.



No. 2



No. 1

(The shaded portions of these switch faces are not used in the binary counting sequence.)

3-23. When none of the lamps are lit, pressing switch No. 1 causes the 2^0 portion to light, thus indicating the binary number 000 001. When switch No. 1 is pressed again, the 2^0 portion becomes not lit and the 2^1 portion becomes lit, thus indicating 000 010. When switch No. 1 has been pressed seven times, the 2^0 , 2^1 , and 2^2 portions will be lit. Pressing switch No. 1 again forces the 2^3 portion of switch No. 2 to become lit and the 2^0 , 2^1 , and 2^2 portions of switch No. 1 to become not lit, thus indicating 001000.

3-24. Because each switch face represents three binary positions, the total indication on each switch face can be read as one position in an octal number. (Refer to the TAPE ADDRESS area of the TAPE READER AND MODE CONTROL panel in figure 3-7.)

SECTION IV

TEST EQUIPMENT AND SPECIAL TOOLS

4-1. SCOPE.

4-2. This section contains the list of standard test equipment and the list and illustrations of the special tools recommended for maintenance of the PTC. The application of the standard test equipment is described in the calibration procedures in Section VII. The applications of the special tools are briefly described in this section; the applications of many of these tools are further described in the repair procedures in Section IX.

4-3. TEST EQUIPMENT.

4-4. STANDARD TEST EQUIPMENT.

4-5. Figure 4-1 is the list of standard test equipment recommended for maintenance of the PTC. This equipment is not supplied with the PTC. Equipment having the same range and accuracy as those listed in figure 4-1 may be substituted for the items listed.

4-6. SPECIAL TEST EQUIPMENT.

4-7. No special test equipment is required for maintenance of the PTC.

4-8. SPECIAL TOOLS.

4-9. The special tools recommended for maintenance of the PTC are listed in figure 4-2 and illustrated on figure 4-3. These tools are not supplied with the PTC. Equivalent tools may be substituted for the items listed.

Name	Model or Type	Vendor
Oscilloscope	585A	Tektronix, Inc.
Plug-in Unit	M	Tektronix, Inc.
Plug-in Adapter	81	Tektronix, Inc.
Differential Voltmeter AC/DC	803-B	John Fluke Mfg. Co., Inc.
Digital Voltmeter	456	Kintel Division, Cohu Electronics, Inc.
AC Converter	452	Kintel Division, Cohu Electronics, Inc.
Digital Readout	473A	Kintel Division, Cohu Electronics, Inc.
Milliammeter (0-15 ma)	901	Weston Instrument Division, Daystrom Inc.
Volt-Ohm-Ammeter	630-A	Triplett Electrical Instrument Co.
Volt-Ohmmeter	269	Simpson Electric Co.
Capacitance Bridge	650-A	General Radio Co.

Figure 4-1. Recommended Standard Test Standard



Name	Vendor Part No.	Application	Illustration Figure 4-3
SMS Card Puller	IBM 6072429	Facilitates insertion or removal of SMS cards.	Part A
SMS Card Contact Lubricant	IBM 6072430	Insures low contact resistance and reduces wear of the gold-plated SMS card contact surfaces.	Part B
SMS Card Extender	IBM 6072431	Allows access to the components and wiring of an SMS card while the card is connected into the system.	Part C
SMS Card Socket Terminal Extractor	IBM 6072432	Used to remove SMS card socket terminals (contacts).	Part D
Soldering Handle	Hexacon P25	Handle for soldering tip.	Part E
Soldering Tip	Hexacon HT248D	Used to remove or install SMS card socket terminals that are soldered to a printed circuit overlay or a voltage chain.	Part F
Hand Wire-Wrap Tool	IBM 6072438	A manual, squeeze-type wire-wrap tool used to wire-wrap SMS card socket terminals.	Part G
Wrapping Bit-22	Keller A-18632	Used with hand wire-wrap tool to wrap AWG22 wire.	Part H
Wrapping Bit-20	Keller A-18633	Used with hand wire-wrap tool to wrap AWG20 wire.	
Wrapping Bit-24	Keller A-26232	Used with hand wire-wrap tool to wrap AWG24 wire.	
Wrapping Bit-26	Keller A-27611	Used with hand wire-wrap tool to wrap AWG26 wire.	
Sleeve - 26	Keller A-17611-2	Used with hand wire-wrap tool to wrap AWG24-26 wire.	
Sleeve - 22, 24	Keller A-18840	Used with hand wire-wrap tool to wrap AWG22 wire.	
Sleeve - 20	Keller A-18285	Used with hand wire-wrap tool to wrap AWG20 wire.	

Figure 4-2. List of Recommended Special Tools (Sheet 1 of 3)


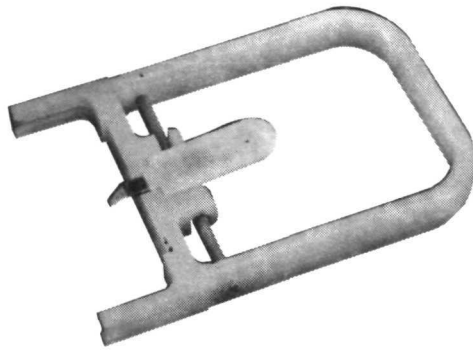
Name	Vendor Part No.	Application	Illustration Figure 4-3
Unwrap Tool	IBM 6072437	Used to unwrap both right and left-hand wraps.	Part J
Crimping Tool Kit	Bendix 11-7295	Used to crimp size 12, 16 and 20 type connector contacts.	Part K
Insertion Tool	Bendix 11-6781-16	Used to insert size 16 contacts in Bendix type connectors.	Part L
Insertion Tool	Bendix 11-8107-20	Used to insert size 20 contacts in Bendix type connectors.	Part M
Contact Removing Tool Kit	Bendix 11-6900	Used to remove size 16 and 20 contacts in Bendix type connectors.	Part N
Spanner Wrench	Bendix 11-3544	Used on Bendix type connector spanner nuts.	Part O
Connector Pliers	Bendix 6147-1	Used to hold knurled or serrated surfaces on Bendix type connectors.	Part P
Crimping Tool	AMP 59501	Used to crimp AWG22-24 solid or stranded wire.	Part Q
Crimping Tool	Berg HT-3-20	Used to crimp AWG20 solid or stranded wire to a slip-on terminal.	Part R
Crimping Tool	Berg HT-3-22	Used to crimp AWG22 solid or stranded wire to a slip-on terminal.	
Crimping Tool	Berg HT-3-24	Used to crimp AWG24 solid or stranded wire to a slip-on terminal.	
Attenuator Probe	Tektronix P-6017	General purpose probe with nine-foot cable terminating at a UHF connector.	
Current Probe	Tektronix P-6016	Special purpose probe used when monitoring current characteristics.	Part T

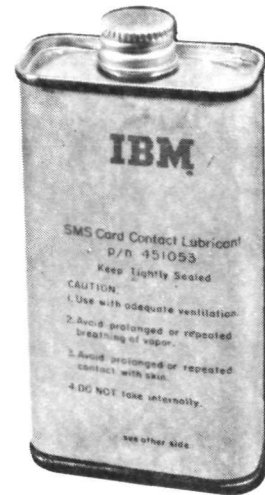
Figure 4-2. List of Recommended Special Tools (Sheet 2)

Name	Vendor Part No.	Application	Illustration Figure 4-3
Passive Termination	Tektronix 011-028	Used with the current probe when monitoring current characteristics.	Part U
Switch Assembly Wrench	IBM 6900017	Facilitates removal of switches from switch housings.	Part V
Switch Assembly Extractor	IBM 6900020	Facilitates removal of screens and light modules from switch housings.	Part W
Tool Case	IBM 6445032	Used for carrying tools.	Part X
Intercase	IBM 6445698	Used for carrying tools.	Part Y

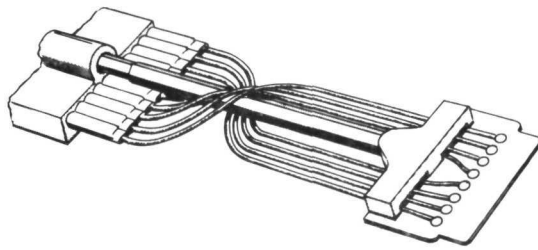
Figure 4-2. List of Recommended Special Tools (Sheet 3)



Part A. SMS Card Puller



Part B. SMS Card Contact Lubricant



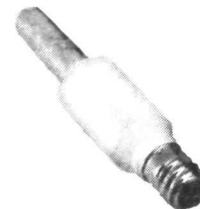
Part C. SMS Card Extender



Part D. SMS Card Socket Terminal Extractor



Part E. Soldering Handle



Part F. Soldering Tip

Figure 4-3. Recommended Special Tools (Sheet 1 of 4)



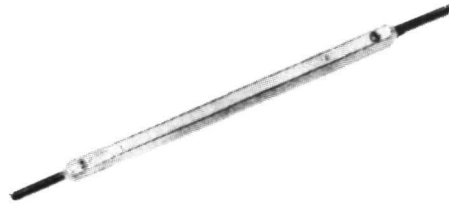
Part G. Hand Wire-Wrap Tool



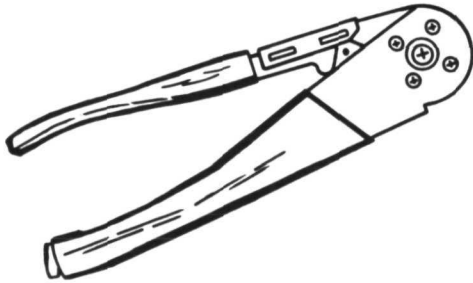
Part H. Wrapping Bit (Typical)



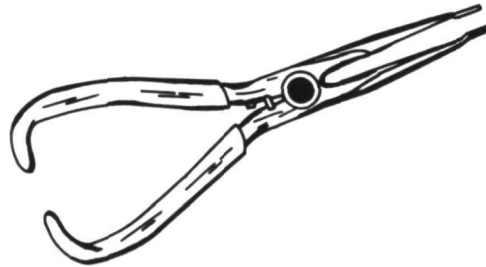
Part I. Sleeve (Typical)



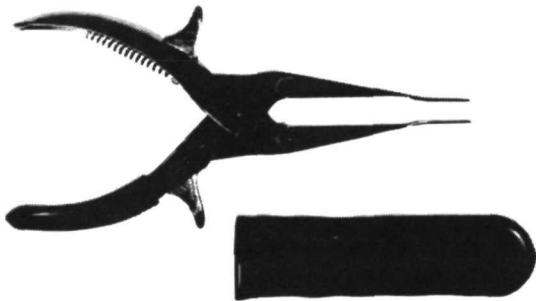
Part J. Unwrap Tool



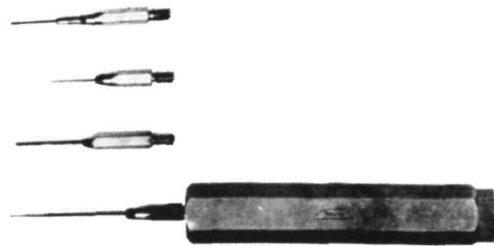
Part K. Crimping Tool Kit



Part L. Insertion Tool

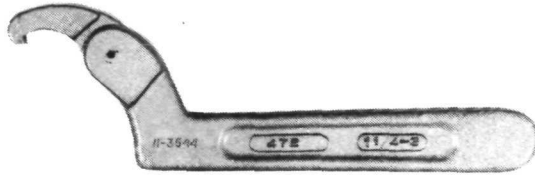


Part M. Insertion Tool

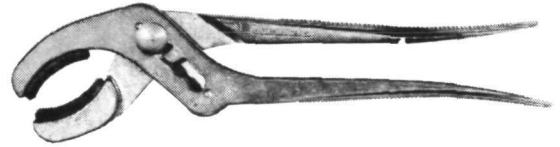


Part N. Contact Removing Tool Kit

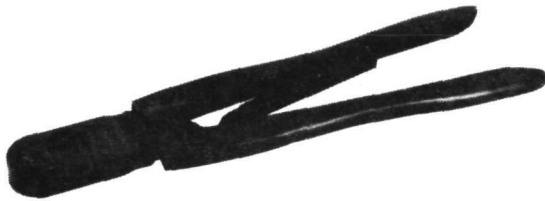
Figure 4-3. Recommended Special Tools (Sheet 2)



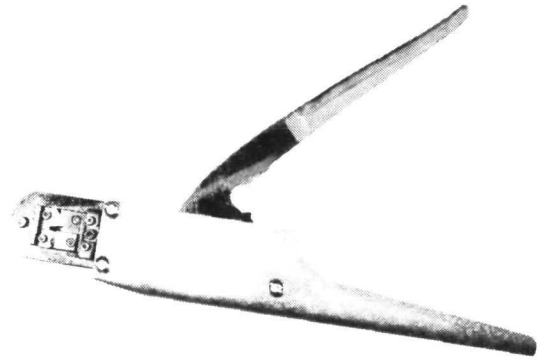
Part O. Spanner Wrench



Part P. Connector Pliers



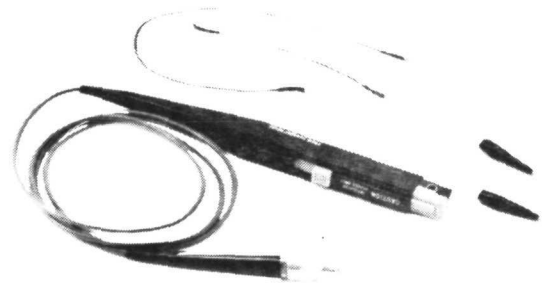
Part Q. Crimping Tool



Part R. Crimping Tool (Typical)



Part S. Attenuator Probe

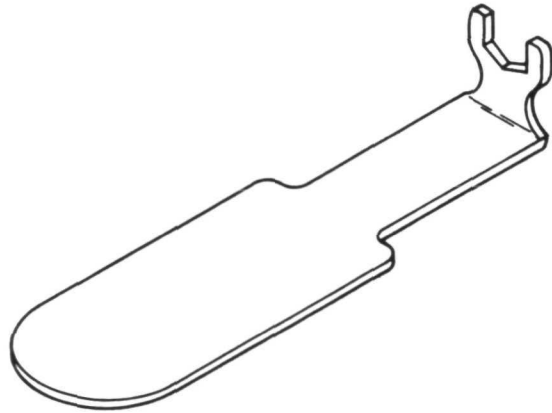


Part T. Current Probe

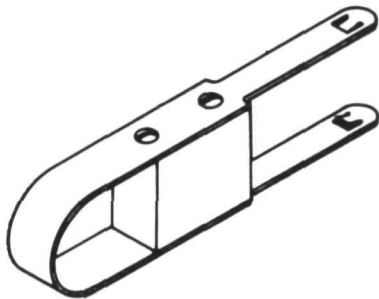
Figure 4-3. Recommended Special Tools (Sheet 3)



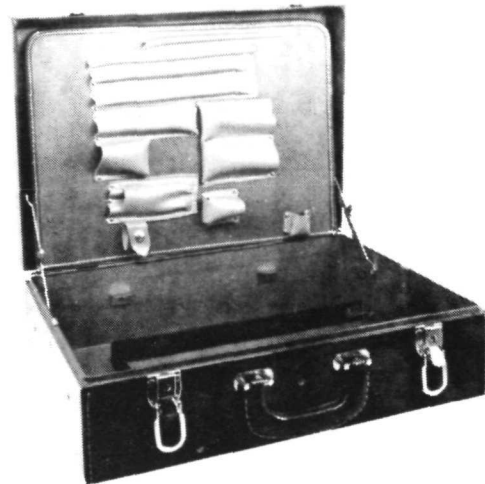
Part U. Passive Termination



Part V. Switch Assembly Wrench



Part W. Switch Assembly Extractor



Part X. Tool Case



Part Y. Intercase

Figure 4-3. Recommended Special Tools (Sheet 4)

SECTION V

PREPARATION FOR USE, STORAGE, AND SHIPMENT

5-1. SCOPE.

5-2. This section describes the procedures for preparing the PTC for use, storage, and shipment.

5-3. PREPARATION FOR USE.

5-4. UNPACKING.

5-5. The PTC is not packed for shipment. No unpacking is necessary.

5-6. ASSEMBLY.

5-7. The PTC is assembled before shipment. No assembling is necessary.

5-8. INSPECTION.

5-9. The PTC should be inspected for evidence of damage caused by improper handling during shipment.

5-10. INSTALLATION.

5-11. Refer to Volume I for installation instructions.

5-12. TESTS.

5-13. Before using the PTC, perform all calibration checks as described in Section VII.

5-14. PREPARATION FOR STORAGE.

5-15. Prepare the PTC for storage as follows:

- a. Close all hinged panels and card gates.
- b. Install connector dust caps on all connectors.
- c. Cover PTC with dust cover.

5-16. PREPARATION FOR SHIPMENT.

5-17. Prepare the PTC for shipment as described in paragraph 5-15.

SECTION VI

PREVENTIVE MAINTENANCE

6-1. SCOPE.

6-2. This section describes the recommended inspection and preventive maintenance schedules for the PTC.

6-3. INSPECTION.

6-4. There is no recommended inspection schedule for the PTC. However, if exterior damage, or deterioration or discoloration of panel markings is noted during daily use of the PTC, repair the fault as described in Section IX.

CAUTION

Never allow an object to obstruct the air intake vents at the bottom of the PTC or the air exhaust vents on the top of the PTC. The air intake vents and air exhaust vents must be open to allow cooling of PTC circuit components.

6-5. PREVENTIVE MAINTENANCE.

6-6. Because the PTC uses SMS cards, preventive maintenance is held at a minimum. Figures 6-1 through 6-5 prescribe the preventive maintenance schedule for the PTC. These figures list the items to be maintained, the location of each item, the frequency at which each item should be inspected, and the method of inspection and maintenance. Refer to the List of Related Manuals in the front of this Volume for the commercial manuals referenced in figures 6-2 through 6-5.

ASSEMBLY PTC (690090) General REFERENCE MANUAL						
Item	Location	Frequency	Observe	Clean	Lubricate	Note
Furnace Type Filters	Bottom of Frames 01, 02, and 03.	Monthly	Check for cleanliness.			Replace if necessary.
Fans	Top and bottom, and front and rear of Frames 01, 02, and 03.	Monthly	Check for any obvious faults such as noisy operation, wear, cleanliness, etc.			Clean or replace if necessary.

Figure 6-1. PTC General Preventive Maintenance

ASSEMBLY Plotter Assembly 6900170 (Calif. Computer Products, Inc. Model 565) REFERENCE MANUAL Instruction Manual for Digital Incremental Plotter, Model 565						
Item	Location	Frequency	Observe	Clean	Lubricate	Note
Operational Checkout	Refer to paragraph 4-13, page 17 of the reference manual.	Weekly				If the plotter is used in- frequently, this opera- tional checkout should be performed. If the instrument is in fre- quent use, this check- out may be omitted since it should nor- mally be performed at the start of each re- cording run.
Carriage Rods and Drum Surface		As required		Clean as required with a soft, dry cloth. If necessary, the cloth may be moistened with Freon 12 cleaning sol- vent (E. I. Dupont Nemours and Company, Inc.) to remove foreign matter.		
Metal Plunger and Pen Assembly	See figure 5-3, page 23 of the reference manual.			Clean inside of the pen assembly plunger by pushing one corner of a soft, dry cloth through the center. If the plunger is clogged, it should be dipped in Freon 12 cleaning sol- vent and then wiped dry.		CAUTION Use care to avoid dam- age to the teflon insula- tion on the carriage drive cable. This cable supplies -24 volt power to the pen solenoid.
Ballpoint Pen		See Note column.		See Note column.		The ballpoint pen accumulates ink at the tip. The pen should be removed and cleaned about every hour of operation. Pen life is approximately 5 to 7 hours. Pen replace- ment should be con- sidered before critical drawings are made to reduce the possibility of smear.

Figure 6-2. Plotter Assembly (01A1) Preventive Maintenance

ASSEMBLY Tape Reader 6901110 (Rheem Electronics Model RR1002-B-333)
 REFERENCE MANUAL Rheem TRM-306E

Item	Location	Frequency	Observe	Clean	Lubricate	Note												
Photocell Block	Front panel (See figure 4-7, page 19, No. 10 of reference manual).	Semi-weekly	Check for cleanliness of the glass slide covering the aperture plate.	Use stiff bristle brush for general cleaning. Use a cotton swab and water, if necessary to remove foreign matter.														
Focusing Lens	Front panel (See figure 4-3, page 13, of reference manual).	Semi-weekly	Check for cleanliness.	Use same materials as above for any necessary cleaning.														
Jam and Drive Rollers	Front panel (See figure 4-1, page 12, of reference manual).	Semi-weekly	Check for wear or indentations on roller surfaces.	If necessary, clean by abrading surfaces with a soft eraser (Eraser Stik, A. W. Faber or equivalent).														
Brake Shoes	Front panel (See figure 4-7, page 19, No. 4, of reference manual).	Semi-monthly	Check for accumulation of foreign matter that might tend to reduce braking force.	Clean with stiff bristle brush.														
Power Supply Voltages	See figures 4-5 and 4-6, pages 17 and 18, of reference manual for location of components and terminals listed under the "observe" column.	Monthly	With the same voltmeter, check and record all voltages listed below. Use the same voltmeter for each monthly test. A change in voltage may be indicative of a gradual component failure. A period of about 30 minutes should be allowed for warm up before the readings are taken. All voltage readings should be $\pm 5\%$.															
			<table border="1"> <thead> <tr> <th>Voltage</th> <th>From</th> <th>To</th> </tr> </thead> <tbody> <tr> <td>-56V</td> <td>C1, -terminal</td> <td>TP1</td> </tr> <tr> <td>-10V</td> <td>F3, terminal 2</td> <td>TP1</td> </tr> <tr> <td>+4V</td> <td>C1, +terminal</td> <td>TP1</td> </tr> </tbody> </table>		Voltage	From	To	-56V	C1, -terminal	TP1	-10V	F3, terminal 2	TP1	+4V	C1, +terminal	TP1		
Voltage	From	To																
-56V	C1, -terminal	TP1																
-10V	F3, terminal 2	TP1																
+4V	C1, +terminal	TP1																

Figure 6-3. Tape Reader Assembly (03A2) Preventive Maintenance (Sheet 1 of 2)

ASSEMBLY Tape Reader 6901110 (Rheem Electronics Model RR1002-B-333) REFERENCE MANUAL Rheem TRM-306E						
Item	Location	Frequency	Observe	Clean	Lubricate	Note
Belt	See figure 4-6, page 18, No. 2, of reference manual.	Monthly	Check for wear or fraying of the belt which might cause slippage or an eventual break.			Replace if necessary.
Lamp	See figure 4-3, page 13, of reference manual.	* 18 Months				Replace lamp and go through necessary adjustments and calibration as outlined in Sections 4.2.2, page 11, and 4.2.3, page 14, of reference manual.
Symmetry of Track Output	See figure 4-5, page 17, of reference manual for location of test points listed under the "Note" column.	When lamp above is replaced or a tape material changes.				Check the output of test points 1 and 2 for 45% "on time" (refer to Section 4.2.3 for Symmetry Adjustment in reference manual).

*This frequency is good only if the estimated reader on-time per week is ≈ 10 hours. If the reader on-time per week (t) is estimated to be > 10 hours, use the following formula to establish a different frequency:

$$\text{frequency (in weeks)} = \frac{4,060}{t + 42}$$

Figure 6-3. Tape Reader Assembly (03A2) Preventive Maintenance (Sheet 2)

ASSEMBLY Tape Spooler 6901120 (Rheem Electronics Model RSS00A)
 REFERENCE MANUAL Rheem TSM-306A

Item	Location	Frequency	Observe	Clean	Lubricate	Note
Fawick Brake		Monthly	See "Note" column first. Then inspect the brake lining and replace when excessively worn.	See "Note" column first. Then clean the brake lining with a stiff bristle brush.		Remove the collar from the rear of each motor shaft, and slide the brake disk off.
Relay K1 Voltage	See figure 4-2, page 15, of reference manual	Monthly				Check the voltage across the coil of relay K1 in its operated state (refer to Section 4.2.3 on Relay Voltage Calibration in the reference manual).
Tension of the Tape Sensing Arm	See figure 4-5, page 18, No. 19, of reference manual.	Quarterly				Check the force on the Tape Sensing Arm at the end of the arm (refer to Section 4.2.1, page 12, on Adjustment of Tape Sensing Arm Tension in reference manual).
Gear in Drive Motor, M1	See figure 4-2, page 15, of reference manual.	Semi-Yearly			Apply one or two drops of 80 weight ciling oil (Kerrus Pacific Corp., 330 North Batavia Street, Orange, California, or equivalent) to each gear.	
Spring in Reel Retainer Housing		Semi-Yearly			Place a small amount of light grade oil (Mobil Vacuoline Oil E, Socony Mobil Oil Co., or equivalent) between the chambered section of the knob and the two locking pins: A small amount of light grade oil is also required on the inside surface of the knob.	

Figure 6-4. Tape Spooler Assembly (03A3) Preventive Maintenance

ASSEMBLY Trygon Power Supply (See below for applicable assembly numbers and models)
 REFERENCE MANUAL Trygon Instruction and Maintenance Manual

Item	Location	Frequency	Observe	Clean	Lubricate	Note
Fan Motor		Monthly			Oil Motor shaft at tubes on each end of motor with a light oil (Mobil Vacuoline Oil E, Socony Mobil Co., or equivalent).	
<p>The above P. M. applies to the following assemblies:</p> <ol style="list-style-type: none"> 03A6 and 03A7 PTC, 6078151 (Trygon Model M36-5-0V) 03A8 and 03A9 PTC, 6078408 (Trygon Model M15-10-0V) 						

Figure 6-5. Power Supplies (Trygon) Preventive Maintenance

SECTION VII

CALIBRATION

7-1. SCOPE.

7-2. This section contains the calibration and adjustment procedure for the PTC. This procedure is contained in figures 7-1 through 7-11. The calibration and adjustment procedure consists of (1) power checks and necessary adjustments, and (2) logic checks and necessary adjustments. The logic checks consists of manual and automatic (programmed) checks.

7-3. CALIBRATION INTERVAL.

7-4. The calibration procedure shall be performed monthly. The procedure may be performed at any time for trouble isolation.

7-5. The procedure is presented in such a manner that the entire procedure may be performed in the sequence given, or any one check may be performed by itself.

7-6. SPECIAL TEST EQUIPMENT REQUIRED FOR CALIBRATION.

7-7. The special test equipment specified in the procedure is listed in figure 4-1. The special test equipment shall be calibrated prior to use in accordance with the appropriate commercial manual. In addition to the special test equipment, test program tapes IBM part numbers 6001232, 6001236, and 6001247 are required.

7-8. GENERAL CALIBRATION PROCEDURES.

7-9. Prior to starting the procedure, the cables listed in figure 7-1 shall be connected as shown, and plug 01P13 shall be connected to jack 01J13. The NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch on the CE PANEL shall be set to the NORM position unless otherwise stated in the procedures.

7-10. If a failure occurs, as evidenced by indications other than the normal indications listed, refer to the applicable adjustments or to Trouble Isolation in Section VIII.

7-11. ABBREVIATIONS USED IN CALIBRATION PROCEDURES.

7-12. The following abbreviations are used in the PANEL column of the figures containing the procedure.

<u>Abbreviation</u>	<u>Definition</u>
PD	PROCESSOR DISPLAY PANEL
TRMC	TAPE READER AND MODE CONTROL PANEL
MLDD	MEMORY LOAD AND DATA DISPLAY PANEL
CE	C E PANEL
NA	Not applicable

7-13. POWER CHECKS AND ADJUSTMENTS.

7-14. The power checks and adjustments substantiate that the power distribution circuits are functioning properly and that the DC voltages are within required tolerances. The power checks and adjustments are listed sequentially in figure 7-2.

7-15. LOGIC ADJUSTMENTS AND CHECKS.

7-16. If the calibration is being started here, or if only one group of the logic checks is being performed and power is not on, perform the following steps:

1. Verify that all interlock switches are closed, the EMERGENCY PULL switch is reset (pushed-in), and that all circuit breakers located in end panel 01B are on.
2. Verify that all AC ON and ON switches on the Trygon power supplies and all circuit breakers for the SMS power supplies are at the ON position.
3. Press and release PTC MAIN PWR-PWR ON pushbutton/lamp (PROCESSOR DISPLAY PANEL), and allow 15 minutes minimum for power supply warm-up. Note that PTC MAIN PWR-PWR ON lamp lights; PTC MAIN PWR-PWR OFF lamp goes out; and PTC DC PWR-PWR ON lamp lights.
4. Press and release PTC DC PWR-PWR ON pushbutton/lamp. Note that PTC DC PWR-PWR ON lamp lights after a noticeable delay and PTC DC PWR-PWR OFF lamp goes out.

7-17. TIMING ADJUSTMENTS.

7-18. The timing adjustments listed in figure 7-3 substantiate that the single shots and variable delays contained in the PTC are adjusted properly. Timing durations shall be measured at the 50 percent amplitude level for all waveshapes. Timing durations of 2 MS or less shall be measured with the oscilloscope in the "A" DEL'D by "B" mode using the DELAY TIME MULTIPLIER dial.

7-19. The 1270 NSEC delay cards, which are variable from 320 to 1270 NSEC increments, are referenced for several adjustments. Desired delays are obtained by jumpering together various combinations of the pins on these cards. (See figure 7-4.)

7-20. TAPE READER CONTROLS AND PTC AND PRINTER TIMING CHECKS.

7-21. The tape reader controls, and PTC and printer timing Checks substantiate that the tape reader timing and control circuits, Phase/Bit Gate/Glock selection circuits, and printer timing circuits are functioning properly. These checks are listed sequentially in figure 7-5. The tape reader exercise tape referenced in step 3.82 is a strip of paper tape five feet long. Holes are punched in each channel of the tape for every other tape character. Holes are punched in channels 1, 3, 5, and 7 for the first tape character and channels 2, 4, 6, and 8 for the next tape character, etc. The ends of the tape are then spliced together to form a continuous loop. This tape is supplied with the PTC.

7-22. MEMORY LOADER AUTOMATIC CHECKS.

7-23. The memory loader automatic checks substantiate that the memory loader circuits and controls are functioning properly when in the AUTO mode. A special program used for subsequent checks is loaded into the central processor memory during these checks. The memory loader automatic checks are listed sequentially in figure 7-6.

7-24. MEMORY LOADER MANUAL CHECKS.

7-25. The memory loader manual checks substantiate that the controls and indicators of the memory loader circuits are functioning properly when in the MANUAL mode. These checks are listed sequentially in figure 7-7. The memory loader manual checks can not be performed unless the special program has been loaded into the central processor memory (steps 4. 1 through 4. 84 in figure 7-6).

7-26. DATA DISPLAY CHECKS.

7-27. The data display checks substantiate that the data display circuits, controls, and indicators are functioning properly. These checks are listed sequentially in figure 7-8. The data display checks can not be performed unless the special program has been loaded into the central processor memory (steps 4. 1 through 4. 84 in figure 7-6).

7-28. CENTRAL PROCESSOR MANUAL CHECKS.

7-29. The central processor manual checks substantiate that the controls and indicators on the CE PANEL and PROCESSOR DISPLAY PANEL are operational and that the halt and single step features are functioning properly. These checks are listed sequentially in figure 7-9. The central processor manual checks can not be performed unless the special program has been loaded into the central processor memory (steps 4. 1 through 4. 84 in figure 7-6).

7-30. CENTRAL PROCESSOR MEMORY AUTOMATIC CHECKS.

7-31. The memory automatic checks substantiate that all locations of the central processor memory can be exercised without error. These checks are listed sequentially in figure 7-10.

7-32. SELF-TEST PROGRAM CHECKS.

7-33. The self-test program checks substantiate that the central processor plotter, printer, typewriter, and interrupt logic are functioning properly. These checks are listed sequentially in figure 7-11.

7-34. If a malfunction occurs while running one of the test program routines, the PROGRAM ERROR lamp will light. Information pertaining to ten errors may be retained at any given time. The first nine errors detected are stored in nine blocks of five words each. The tenth block will contain data for the last error detected before the test was stopped. In addition the total error count and error count for the first pass are stored. The five data words and their symbolic names are as follows:

- (1) VAR3 — The current value of the program pass counter.
- (2) VAR1 — A HOP constant referencing an individual test or block of tests.
- (3) ACCUM — The contents of the accumulator at the time the error was detected.
- (4) VAR4 or V4 — A HOP constant referencing an individual test. Used when VAR1 refers to a block of tests.
- (5) VAR5 or V5 — A data word defining an individual test. Used when a subroutine is performing several tests with a block of test data and test patterns.

A comparison is then made with the test program flow diagram and listings (figures 7-12, 7-13, 7-14, and 7-15).

7-35. Figure 7-12 is the test program flow diagram which illustrates the test program functions. The flow diagrams are made up of four types of symbols: the circle, the diamond, the rectangle and the oval. The circle denotes a connective or tie point in the flow diagram; the diamond denotes a decision block; the rectangle denotes an operation being performed; and the oval denotes a reset operation. Symbolic codes are used throughout the flow diagrams to correlate the actual test program location with the flow diagram location.

7-36. The test program listing is divided into three parts as follows:

a. Test Program. (See figure 7-13.) The listing contains fifteen columns of test program data and information. (See figure 7-16 for column data definitions.)

b. Test Program Symbolic Table. (See figure 7-14.) The symbolic table contains a symbolic code which is located in the second column. The table also contains ten other columns which may contain a number (X, XX, X, XXX) which depicts an instruction module, instruction sector, syllable and a memory location respectively, representative of the symbol.

c. Memory Location Contents. (See figure 7-15.) This figure contains memory words (12 digits) which are counted octally from left to right. The first number in each row indexes the octal memory location of the memory words in that row. The last three digits of each memory word in the listing are not part of the word. The last digit designates the syllable usage of that word. Numbers 1, 2 and 3 designate syllables 0, 1 and both 0 and 1 respectively. The other two of the last three digits are not used.

7-37. After the detection of an error and the error information is stored, the program will perform the next test unless PROG REG A-14 toggle switch is set to ON. When this switch is set to ON, a HOP on VAR1 is performed and the program is re-entered at the beginning of the failed test. When PROG REG A-16 toggle switch is set to ON, the PTC will go into single step when an error is detected. Actuating the ADVANCE pushbutton once will cause VAR3 (associated with first error) to be displayed by the DATA area COMPUTER lamps on the MEMORY LOAD AND DATA DISPLAY panel if the DISPLAY SELECT switch is set to the AI3-DATA position. Actuating the ADVANCE pushbutton again will cause VAR1 to be displayed, etc.

7-38. Because of the dual use of VAR1 as a test identifier and a return HOP constant, several types of error information are required. The types and their method of implementation are described as follows (VAR3 and ACCUM are the same for all types):

Type 1 - Independent Test

- A. (Test 1) TNZ to Error Routine
- B. (Test 2)

VAR1 - Location of failed test (A)
VAR2 - Location of next test (B)
VAR4 - Not applicable
VAR5 - Not applicable

Type 1a - Same as Type 1 except that the test data is stored in VAR5.

Type 3 - Common Test Routine using address modification to obtain successive test data and test patterns.

- A. Perform test with changing test data
- B. Test results with changing test pattern
- C. Increment addresses in A and B for next test
- D. Reset registers, etc. for next test
GO TO A if not finished

VAR1 - Location D
 VAR2 - Location C
 VAR4 - Not applicable
 VAR5 - Data used in A for failed test

Type 3a - Similar to Type 3 except that more than one test is performed in each loop. The location of the particular test being executed is stored in VAR4.

Type 4 - Used in PTC Interrupts Test Only

- A. Test previous HOP on interrupt store location of A in VAR4. Force next interrupt and HOP to B.
- B. CLA unique data word
TRA C
- C. STO 777
Save Data Word
STO 777 in VAR5
- D. Test Data Word

VAR1 - Location of beginning of Interrupts test (L12P1)
 VAR2 - Next location following D
 VAR4 - Location (A) of block of instructions preceding HOP
 VAR5 - Location B + 2 (Shows where TRA to C originated)

7-39. The types of error information are used as follows:

<u>Symbolic Location of Test</u>	<u>Error Type</u>
L5P2 - L5P2FF	None
L5P3 - L7P55	1
L9P2 - L9P72	1
L10P1 - L10P45	2
L11P1 - L11P17	1
L11P18 - L11P32	1
L12P1 - L17P1	4
L20P2 - L26P1	3a
L27P1 - L28P2	2
L29P2 - L29P4	1
L30P1 - L31P5	3
L32P1 - L33P1	3

Symbolic Location of Test

Error Type

L32P1 – L33P1	1a
L33P2 –	3
L33P3	1a
L34P1 – L34P3	3
L35P1	1a
L35P2 – L38P3	3
L38P4 – L39P1	1
L39P2 – L39P3	2
L39P4 – L42P2	1
L45P2 – L45P3	2
L47P1	1
Routines 7 and 8	None
JAC1 – JAK1	2
JAA2 – JWE3	1
JAG2 – JAH3	2
JAC4 – JFF5	1
JHB1 – JHE3	2
JJB1 – JKB3	None
JLB1 – JVJ5	2
JXC1 – JXB2	None
JYB1 – JYH1	None
MAC1 – MAH1	None
JXF2 – JZG4	1
Routine 11	1
Routine 12	None

Cable Part Number	From	To
6900912	9009J1	01J8
6900913	9009J2	01J9
6900914	9009J3	01J10
6900915	9009J4	01J11
6900916	9009J5	01J6
6900917	9009J6	01J7
6900168	01J5	01J12

Figure 7-1. Preliminary Cable Connection

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
EXP	NA	Steps 1.1 through 1.40 substantiate that PTC main power can be sequenced on and off, and that the interlocks, EMERGENCY OFF switch, and blower fans are operational.										
1.1	01B5	Connect primary power cable between AC power source and power receptacle 01B5J1.										
1.2	01B5	Remove end panel 01B and verify all circuit breakers are set.										
1.3	01B5	Record elapsed time indicator reading.								Reading	-----	
1.4	01B	Install end panel 01B.										
1.5	PD	Reset (push in) PTC MAIN PWR EMERGENCY PULL switch.										
1.6	PD	Observe PTC MAIN PWR-PWR OFF lamp.								Lit	-----	
1.7	PD	Press and release PTC MAIN PWR PWR ON pushbutton lamp.										
1.8	PD	Observe PTC MAIN PWR-PWR ON lamp.								Lit	-----	
1.9	01B	Remove end panel 01B.										
1.10	PD	Observe PTC MAIN PWR-PWR ON lamp.								Not lit	-----	
1.11	PD	Observe PTC MAIN PWR-PWR OFF lamp.								Lit	-----	

Figure 7-2. Power Checks (Sheet 1 of 15)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
1.12	01B	Install end panel 01B.		
1.13	PD	Press and release PTC MAIN PWR-PWR ON pushbutton.		
1.14	PD	Observe PTC MAIN PWR-PWR ON lamp.	Lit	
1.15	03A	Remove end panel 03A.		
1.16	PD	Observe PTC MAIN PWR-PWR ON lamp.	Not lit	
1.17	PD	Observe PTC MAIN PWR-PWR OFF lamp.	Lit	
1.18	03A	Install end panel 03A.		
1.19	PD	Press and release PTC MAIN PWR-PWR ON pushbutton lamp.		
1.20	PD	Observe PTC MAIN PWR-PWR ON lamp.	Not lit	
1.21	03A5	Extend relay gate 03A5.		
1.22	PD	Observe PTG MAIN PWR-PWR ON lamp.	Not lit	
1.23	PD	Observe PTC MAIN PWR-PWR OFF lamp.	Lit	
1.24	03A5	Close relay gate 03A5.		
1.25	PD	Set (pull out) PTC MAIN PWR-EMERGENCY PULL switch.		
1.26	PD	Observe PTC MAIN PWR-PWR OFF lamp.	Not lit	
1.27	PD	Reset (push in) MAIN Power EMERGENCY OFF switch.		

Figure 7-2. Power Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation									Normal Indication	Data	
1.28	PD	Observe PTC MAIN PWR-PWR OFF lamp.									Lit		
1.29	03A6 thru 03A11	Verify that all AC ON or ON switches on Trygon power supplies are ON.											
1.30	PD	Press and release PTC MAIN PWR-PWR ON pushbutton/lamp.											
1.31	PD	Observe PTC MAIN PWR-PWR ON lamp.									Lit		
1.32	PD	Observe PTC MAIN PWR-PWR OFF lamp.									Not lit		
1.33	PD	Observe PTC DC PWR-PWR OFF lamp.									Lit		
1.34	NA	Observe all blower fans.									Operating		
1.35	03A6 thru 03A11	Observe POWER ON lamps on Trygon power supplies.									Lit		
1.36	PD	Press and release PTC MAIN PWR PWR OFF pushbutton/lamp.											
1.37	PD	Observe PTC MAIN PWR-PWR ON lamp.									Not lit		
1.38	PD	Observe PTC MAIN PWR-PWR OFF lamp.									Lit		
1.39	NA	Observe all blower fans.									Not operating		
1.40	03A6 thru 03A11	Observe POWER ON lamps on Trygon power supplies.									Not lit		
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Figure 7-2. Power Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES--				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
EXP	NA	Steps 1.41 through 1.109 substantiate that PTC DC power can be sequenced on and off and that PTC DC power is automatically sequenced off by a loss of one of the DC voltages supplying the memory unit.		
1.41	PD	Press and release PTC MAIN PWR-PWR ON pushbutton/lamp.		
1.42	PD	Observe PTC MAIN PWR-PWR ON lamp.	Lit	_____
1.43	PD	Observe PTC MAIN PWR-PWR OFF lamp.	Not lit	_____
1.44	PD	Observe PTC DC PWR-PWR OFF lamp.	Lit	_____
1.45	03A6 thru 03A11	Verify that CURRENT ADJUST and CURRENT VERNIER pots on Trygon power supplies are positioned fully clockwise.		
1.46	PD	Press and release PTC DC PWR-PWR ON pushbutton/lamp.		
1.47	PD	Observe PTC DC PWR-PWR OFF lamp.	Not lit	_____
1.48	PD	Observe PTC DC PWR-PWR ON lamp.	Lit (after noticeable delay)	
1.49	PD	Press and release PTC DC PWR-PWR OFF pushbutton/lamp.		

Figure 7-2. Power Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:									UNIT NO.											
Step	Panel	Operation					Normal Indication		Data											
1.50	PD	Observe PTC DC PWR-PWR OFF lamp.					Lit													
1.51	PD	Observe PTC DC PWR-PWR ON lamp.					Not lit													
1.52	02A3	Disconnect plugs 02P9, 02P10, 02P12, 02P13 and 02P14 from the memory unit.																		
1.53	PD	Press and release PTC DC PWR-PWR ON pushbutton/lamp.																		
1.54	PD	Observe PTC DC PWR-PWR OFF lamp.					Not lit													
1.55	PD	Observe PTC DC PWR-PWR ON lamp.					Lit													
1.56	01B8	Set circuit breaker for +30 VDC fixed power supply to OFF.																		
1.57	PD	Observe PTC DC PWR-PWR OFF lamp.					Lit													
1.58	PD	Observe PTC DC PWR-PWR ON lamp.					Not lit													
1.59	01B8	Set circuit breaker for +30 VDC fixed power supply to ON.																		
1.60	PD	Observer PTC DC PWR-PWR OFF lamp.					Not lit													
1.61	PD	Observer PTC DC PWR-PWR ON lamp.					Lit													
1.62	03A6	Set power on switch on +30 VDC variable power supply to OFF.																		
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Figure 7-2. Power Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
1.76	PD	Observe PTC DC PWR-PWR ON lamp.				Not lit			
1.77	03A8	Set power on switch on +12 VDC variable power supply to ON.							
1.78	PD	Observe PTC DC PWR-PWR OFF lamp.				Not lit			
1.79	PD	Observe PTC DC PWR-PWR ON lamp.				Lit			
1.80	03A9	Set power on switch on +12 VDC variable power supply to OFF.							
1.81	PD	Observe PTC DC PWR-PWR OFF lamp.				Lit			
1.82	PD	Observe PTC DC PWR-PWR ON lamp.				Not lit			
1.83	03A9	Set power on switch on +12 VDC variable power supply to ON.							
1.84	PD	Observe PTC DC PWR-PWR OFF lamp.				Not lit			
1.85	PD	Observe PTC DC PWR-PWR ON lamp.				Lit			
1.86	03A11	Set power on switch on -12 VDC variable power supply to OFF.							
1.87	PD	Observe PTC DC PWR-PWP OFF lamp.				Lit			
1.88	PD	Observe PTC DC PWR-PWR ON lamp.				Not lit			

Figure 7-2. Power Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—															
UNIT NAME:												UNIT NO.			
Step	Panel	Operation										Normal Indication	Data		
1.63	PD	Observe PTC DC PWR-PWR OFF lamp.										Lit			
1.64	PD	Observe PTC DC PWR-PWR ON lamp.										Not lit			
1.65	03A6	Set power on switch on +30 VDC variable power supply to ON.													
1.66	PD	Observe PTC DC PWR-PWR OFF lamp.										Not lit			
1.67	PD	Observe PTC DC PWR-PWR ON lamp.										Lit			
1.68	03A7	Set power on switch on +30 VDC variable power supply to OFF.													
1.69	PD	Observe PTC DC PWR-PWR OFF lamp.										Lit			
1.70	PD	Observe PTC DC PWR-PWR ON lamp.										Not lit			
1.71	03A7	Set power on switch on +30 VDC variable power supply to ON.													
1.72	PD	Observe PTC DC PWR-PWR OFF lamp.										Not lit			
1.73	PD	Observe PTC DC PWR-PWR ON lamp.										Lit			
1.74	03A8	Set power on switch on +12 VDC variable power supply to OFF.													
1.75	PD	Observe PTC DC PWR-PWR OFF lamp.										Lit			
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Figure 7-2. Power Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
1.89	03A11	Set power on switch on -12 VDC variable power supply to ON.								
1.90	PD	Observe PTC DC PWR-PWR OFF lamp.					Not lit	_____		
1.91	PD	Observe PTC DC PWP-PWR ON lamp.					Lit	_____		
1.92	01B7	Set circuit breaker for +12 VDC fixed power supply to OFF.								
1.93	PD	Observe the PTC DC PWR-PWR OFF lamp.					Lit	_____		
1.94	PD	Observe the PTC DC PWR-PWR ON lamp.					Not lit	_____		
1.95	01B7	Set circuit breaker for +12 VDC fixed power supply to ON.								
1.96	PD	Observe the PTC DC PWR-PWR OFF lamp.					Not lit	_____		
1.97	PD	Observe the PTC DC PWR-PWR ON lamp.					Lit	_____		
1.98	01B7	Set circuit breaker for -6 VDC fixed power supply to OFF.								
1.99	PD	Observe the PTC DC PWR-PWR OFF lamp:					Not lit	_____		
1.100	PD	Observe the PTC DC PWR-PWP ON lamp.					Lit	_____		
1.101	NA	Observe that any display lamps lit are lit at half brilliancy.								

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Figure 7-2. Power Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-																						
UNIT NAME:							UNIT NO.															
Step	Panel	Operation				Normal Indication	Data															
1.102	PD	Press and release PTC DC PWR-PW OFF pushbutton lamp.																				
1.103	PD	Observe the PTC DC PWR-PWR OFF lamp.				Lit																
1.104	PD	Observe the PTC DC PWR-PWR ON lamp.				Not lit																
1.105	PD	Press and release PTC DC PWR-PWR ON pushbutton/lamp.																				
1.106	PD	Observe the PTC DC PWR-PWR OFF lamp.				Lit																
1.107	PD	Observe PTC DC PWR-PWR ON lamp.				Not lit																
1.108	PD	Press and release PTC DC PWR-PWR OFF pushbutton/lamp.																				
1.108.1	01B7	Set circuit breaker for -6 VDC fixed power supply to on.																				
1.109	02A3	Connect plugs 02P9, 02P10, 02P12, 02P13, and 02P14 to jacks J1 through J5 respectively on the memory unit.																				
EXP	NA	Steps 1.110 through 1.136 substantiate that DC power is applied to and removed from the memory unit in the correct sequence. Allow 30 seconds to elapse after cycling power on before cycling power off one vice-verse.																				
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES		NUMBER
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Figure 7-2. Power Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
1.110	02A3	Connect preamplifier channels A and B to memory unit test jacks 1 (+30 VDC) and 6 (-12 VDC) respectively.							
1.111	PD	While observing oscilloscope press and release PTC DC PWR-PWR ON pushbutton/lamp.							
1.112	02A3	Observe that +30 VDC is applied after -12 VDC.				1.5 seconds minimum			
1.113	PD	Observe PTC DC PWR-PWR ON lamp.				Lit			
1.114	PD	Observe PTC DC PWR-PWR OFF lamp.				Not lit			
1.115	PD	While observing oscilloscope press and release PTC DC PWR-PWR OFF pushbutton/lamp.							
1.116	02A3	Observe that +30 VDC is removed before -12 VDC.				1.5 seconds minimum			
1.117	PD	Observe PTC DC PWR-PWR OFF lamp.				Lit			
1.118	PD	Observe PTC DC PWR-PWR ON lamp.				Not lit			
1.119	02A3	Disconnect preamplifier from memory unit test jack 1 and connect to test jack 3 (+30 VDC).							
1.120	PD	While observing oscilloscope press and release PTC DC PWR-PWR ON pushbutton/lamp.							

Figure 7-2. Power Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES -																					
UNIT NAME:											UNIT NO.										
Step	Panel	Operation									Normal Indication	Data									
1.121	02A3	Observe that +30 VDC is applied after -12 VDC.									1.5 seconds minimum	_____									
1.122	PD	Observe PTC DC PWR-PWR ON lamp.									Lit	_____									
1.123	PD	Observe PTC DC PWR-PWR OFF lamp.									Not lit	_____									
1.124	PD	While observing oscilloscope press and release PTC DC PWR-PWR OFF pushbutton/lamp.										_____									
1.125	02A3	Observe that +30 VDC is removed before -12 VDC.									1.5 seconds minimum	_____									
1.126	PD	Observe PTC DC PWR-PWR ON lamp.									Not lit	_____									
1.127	PD	Observe PTC DC PWR-PWR OFF lamp.									Lit	_____									
1.128	02A3	Disconnect preamplifier from memory unit test jack 3 and connect to test jack 2 (+30 VDC).										_____									
1.129	PD	While observing oscilloscope press and release PTC DC PWR-PWR ON pushbutton/lamp.										_____									
1.130	02A3	Observe that +30 VDC is applied after -12 VDC.									1.5 seconds minimum	_____									
1.131	PD	Observe PTC DC PWR-PWR ON lamp.									Lit	_____									
1.132	PD	Observe PTC DC PWR-PWR OFF lamp.									Not lit	_____									
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-2. Power Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:								UNIT NO.												
Step	Panel	Operation					Normal Indication	Data												
1.133	PD	While observing oscilloscope press and release PTC DC PWR-PWR OFF pushbutton/lamp.																		
1.134	02A3	Observe that +30 VDC is removed before -12 VDC.					1.5 seconds minimum													
1.135	PD	Observe PTC DC PWR-PWR ON lamp.					Not lit													
1.136	PD	Observe PTC DC PWR-PWR OFF lamp.					Lit													
EXP	NA	Steps 1.137 through 1.150 substantiate that all panel lamps are operational.																		
1.137	03A4	Verify that CE panel is extended.																		
1.138	PD	Press and release PTC DC PWR-PWR ON pushbutton lamp.																		
1.139	PD	Observe PTC DC PWR-PWR ON lamp.					Lit													
1.140	PD	Observe PTC DC PWR-PWR OFF lamp.					Not lit													
1.141	CE	Observe ACC DISPLAY ENABLE and TIMING DISPLAY ENABLE lamps (press and release if not lit).					Lit													
1.142	CE	Press and hold LAMP TEST pushbutton/lamp.																		
1.143	CE	Observe all lamps on CE panel.					Lit													
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-2. Power Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:								UNIT NO.												
Step	Panel	Operation					Normal Indication	Data												
1.144	TRMC	Observe PWR OFF lamp (press and release if not lit).					Lit													
1.145	TRMC	Press and hold LAMP TEST push-button/lamp.																		
1.146	TRMC	Observe all lamps on TRMC panel.					Lit													
1.147	MLDD	Press and hold LAMP TEST push-button/lamp.																		
1.148	MLDD	Observe all lamps on MLDP panel.					Lit													
1.149	PD	Press and hold LAMP TEST push-button/lamp.																		
1.150	PD	Observe all lamps on PD panel except PTC MAIN PWR-PWR OFF, PTC DC PWR-PWR OFF, and MAN CST.					Lit													
EXP	NA	Steps 1.151 through 1.168 substantiate the PTC DC voltages are within required tolerances.																		
NOTE																				
Verify that 15 minutes have elapsed since power was turned on before taking the following voltage measurements.																				
1.151	03A10	Connect digital voltmeter between and G test jacks on -28 VDC Trygon power supply. Adjust VOLTAGE VERNIER and VOLTAGE ADJUST controls to obtain voltage indicated in Normal Indication column.					-32 ±0.5 VDC													
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-2. Power Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
1.152	03A3	Connect digital voltmeter between the following test jacks on the memory unit. Adjust VOLTAGE VERNIER and VOLTAGE ADJUST controls of associated Trygon power supplies until the measured voltages are within $\pm 2\%$ of the corresponding voltages indicated on the Memory Characteristics Strobe Setting Tag.										
1.153	03A6	Test jacks 1 and 9 (Ret.). (+30 VDC Trygon power supply.)										
1.154	03A7	Test jacks 2 and 9 (Ret.). (+30 VDC Trygon power supply.)										
1.155	03A8	Test jacks 7 and 9 (Ret.). (+12 VDC Trygon power supply.)										
1.156	03A9	Test jacks 8 and 9 (Ret.). (+12 VDC Trygon power supply.)										
1.157	03A11	Connect digital voltmeter between terminals 1 and 2 (Ret.) of hockey stick located in gate 01B3. Adjust VOLTAGE VERNIER and VOLTAGE ADJUST controls of -12 VDC Trygon power supply to obtain voltage indicated in Normal Indication column.							-11.9 \pm 0.5 VDC			
1.158	NA	Connect digital voltmeter between the following points. Adjust screw-driver adjust located between CB1 and CB2 of associated SMS power supplies to obtain voltages in Normal Indication column.										
A B C D E F G H I J K L M N O P Q R PAGE										PAGES		NUMBER
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Figure 7-2. Power Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES—																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation							Normal Indication	Data											
1.159	01B6	Terminals 3 and 2 (Ret.) of hockey stick in gate 03B6. (-6 VDC SMS power supply.)							-6.08 ± .01 VDC												
1.160	01B6	Terminals 5 and 2 (Ret.) of hockey stick in gate 01B3. (+12 VDC SMS power supply).							+12.05 ± .05 -.01 VDC												
1.161	01B8	Test jacks 3 and 9 (Ret.) on the memory unit. (+30 VDC SMS power supply.)							+30.0 ± .6 VDC												
1.162	NA	Using a digital voltmeter measure and record the voltages appearing between the following points.																			
1.163	02A3	Test jacks 4 and 9 (Ret.) on the memory unit.							+11.76 to +12.24 VDC												
1.164	02A3	Test jacks 5 and 9 (Ret.) on the memory unit.							-5.68 to -6.12 VDC												
1.165	02A3	Test jacks 6 and 9 (Ret.) on memory unit.							-11.76 to -12.24 VDC												
1.166	03B8	Terminals 1 and 2 (Ret.) of hockey stick in gate 03B8.							-11.76 to -12.24 VDC												
1.167	03B8	Terminals 3 and 2 (Ret.) of hockey stick in gate 03B8.							-5.88 to -6.12 VDC												
1.168	03B8	Terminals 5 and 2 (Ret.) of hockey stick in gate 03B8.							+11.76 to +12.24 VDC												
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
																			OF		A-

Figure 7-2. Power Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:			UNIT NO.																		
Step	Panel	Operation	Normal Indication	Data																	
EXP	NA	Steps 2.1 through 2.11 substantiate that the single shots which develop 500 CPS MV and 10 CPS MV signals are adjusted properly.																			
2.1	01A	On the Plotter turn Power to OFF.																			
2.2	TRMC	Observe SELF CHECK lamp (press and release if not lit).	Lit	_____																	
2.3	TRMC	Observe ML lamp (press and release if not lit).	Lit	_____																	
2.4	TRMC	Observe FREE RUN SS lamp (press and release if not lit).	Lit	_____																	
2.5	CE	Connect preamplifier channel A to 500 MV test jack																			
2.6	NA	Trigger oscilloscope internally.																			
2.7	03B6	Observe duration of negative going portion of waveshape (adjust potentiometer on card 03B6).	$1 \pm .02 \text{ MS}$	_____																	
2.8	03B6	Observe duration of positive going portion of waveshape (adjust potentiometer on card B14).	$1 \pm .02 \text{ MS}$	_____																	
2.9	CE	Connect preamplifier channel A to 10 MV test jack.																			
2.10	03B6	Observe duration of positive going portion of waveshape (adjust potentiometer on card B17).	$50 \pm 3 \text{ MS}$	_____																	
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER	
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Fig 7-3, Sheet 1

Figure 7-3. Timing Adjustments (Sheet 1 of 16)

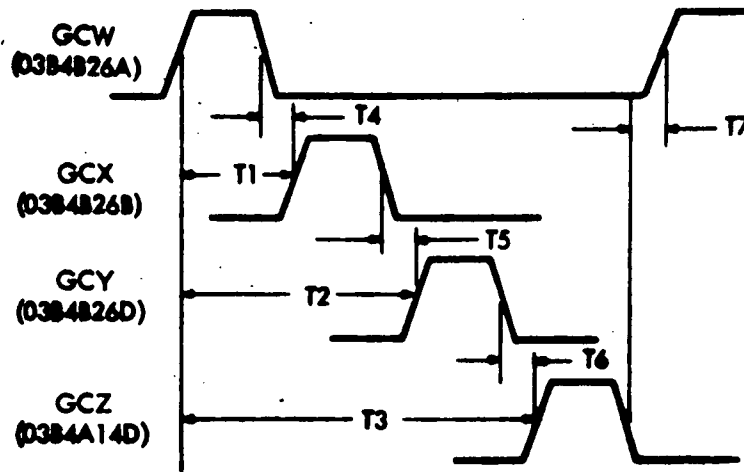
INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation						Normal Indication	Data												
2.11	03B6	Observe duration of negative going portion of waveshape (adjust potentiometer on card A18).						50 ± 3 MS	_____												
EXP	NA	Steps 2.12 through 2.39 substantiate that the single shots and delays which develop clock sync timing and phase sync timing pulses are adjusted properly.																			
2.12	03B4	Connect preamplifier channel A to B26A.																			
2.13	03B4	Trigger oscilloscope externally on D15R.																			
2.14	NA	On the oscilloscope set the time Base to .2 usec/cm. and then using the variable time base knob place the leading edges of 2 consecutive W clocks (Positive going) 8 cm's apart at their 50% points (see Illustration A).																			
2.15	03B4	Connect preamplifier channel B to B26P.																			
2.16	NA	Observe the duration of T1 (see Illustration A) (1270 Nsec delay card A17).						2 ± .1 cm	_____												
2.17	03B4	Disconnect preamplifier channel B from B26P and connect to B26D.																			
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.



WHERE: $T4 = T5 = T6 = T7$

Illustration A. PTC Clock Sync Timing

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation					Normal Indication	Data													
2.18	NA	Observe the duration of T2 (see Illustration A) (1270 Nsec delay card A19).					4 ± .1 cm	_____													
2.19	03B4	Disconnect preamplifier channel B from B26D and connect to A14D.																			
2.20	NA	Observe the duration of T3 (see Illustration A) (1270 Nsec Delay card A18).					6 ± .1 cm	_____													
2.21	NA	On oscilloscope set the variable time base knob fully clockwise.					-														
2.22	NA	Observe the duration of T7 (see Illustration A) (adjust potentiometer on card A26).					70 ± 10 nsec	_____													
2.23	03B4	Disconnect preamplifier channel B from A14D and connect to B26P.																			
2.24	NA	Observe the duration of T4 (see Illustration A) (adjust potentiometer on card A24).					70 ± 10 nsec	_____													
2.25	03B4	Disconnect preamplifier channel A from B26A and connect to B26D.																			
2.26	NA	Observe the duration of T5 (see Illustration A) (adjust potentiometer on card A25).					70 ± 10 nsec	_____													
2.27	03B4	Disconnect preamplifier channel B from B26P and connect to A14D.																			
2.28	NA	Observe the duration of T6 (see Illustration A) (adjust potentiometer on card A20).					70 ± 10 nsec	_____													
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—																					
UNIT NAME:								UNIT NO.													
Step	Panel	Operation					Normal Indication	Data													
2. 29		Disconnect preamplifier channel B.																			
2. 30	03B4	Connect preamplifier channel A to D16B (trigger scope internally).																			
2. 31	NA	Observe the duration of the negative going portion of the waveform.					.6 + .07, -.03 usec	_____													
2. 32	03B4	Connect preamplifier channel A to D17B.																			
2. 33	NA	Observe the duration of the negative going portion of the waveform.					.6 + .07 -.03 usec	_____													
2. 34	03B4	Connect preamplifier channel A to E16B.																			
2. 35	NA	Observe the duration of the negative going portion of the waveform.					.6 + .07 -.03 usec	_____													
2. 36	03B4	Connect preamplifier channel A to F17B.																			
2. 37	NA	Observe the duration of the negative portion of the waveform.					.6 + .07 -.03 usec	_____													
2. 38	03B4	Connect preamplifier channel A to A21P.																			
2. 39	03B4	Observe duration of negative going portion of waveshape (adjust potentiometer on card A21).					400 ± 50 nsec	_____													
EXP	NA	Steps 2. 40 through 2. 43 substantiate that the single shots which develop MACH RST signal are adjusted properly.																			
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	of	PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
2.40	03B4	Connect preamplifier channel A to A22P																			
2.41	03B4	Observe duration of negative going portion of waveshape (adjust potentiometer on card A22).								40 ± 3 MS	_____										
2.42	03B4	Connect preamplifier channel A to A23P																			
2.43	03B4	Observe duration of negative going portion of waveshape (adjust potentiometer on card A23).								40 ± 3 MS	_____										
EXP	NA	Steps 2.44 through 2.61 substantiate that the single shots and delays which develop typewriter control signals are adjusted properly.																			
2.44	01B1	Connect preamplifier channel A to D12F and channel B to D12E.																			
2.45	CE	Trigger oscilloscope externally with 10 CPS MV signal (10MV test jack).																			
2.46	01B1	Observe that rise of pulse on channel B is delayed from rise of pulse on channel A (adjust potentiometer on card D12).								20 ± 2 MS	_____										
2.47	01B1	Connect preamplifier channel A to D13F and channel B to D13E.																			
2.48	01B1	Observe that rise of pulse on channel B is delayed from rise of pulse on channel A (adjust potentiometer on card D13).								20 ± 2 MS	_____										
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
																			OF	A-	

Figure 7-3. Timing Adjustments (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation							Normal Indication	Data										
2.49	01B1	Connect preamplifier channel A to B07B.																		
2.50	NA	Trigger oscilloscope internally.																		
2.51	01B1	Observe duration of negative going portion of waveshape (adjust potentiometer on card B07).							75 ± 5 MS	_____										
2.52	01B1	Connect preamplifier channel A to C10B.																		
2.53	01B1	Observe duration of negative going portion of waveshape (adjust potentiometer on card C10).							50 ± 5 MS	_____										
2.54	01B1	Connect preamplifier channel A to D22F and channel B to D22E.																		
2.55	CE	Trigger oscilloscope externally with 10 CPS MV signal (10MV test jack).																		
2.56	01B1	Connect a jumper from B23R to B23																		
2.57	01B1	Observe that rise of pulse on channel B is delayed from rise of pulse on channel A (adjust potentiometer on card D22).							50 ± 5 MS	_____										
2.58	01B1	Connect preamplifier channel A to D23B.																		
2.59	NA	Trigger oscilloscope internally.																		
2.60	01B1	Observe duration of negative going portion of waveshape (adjust potentiometer on card D23).							20 ± 2 usec	_____										
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:							UNIT NO.														
Step	Panel	Operation				Normal Indication	Data														
2.61	01B1	Remove jumper from B23R to B23J																			
EXP	NA	Steps 2.62 through 2.72 substantiate that the single shots and delay which develop plotter control signals are adjusted properly.																			
2.62	01B2	Connect preamplifier channel A to A23B.																			
2.63	01B2	Connect a jumper between B13P to B13J																			
2.64	01B2	Observe duration of negative going portion of waveshape (adjust potentiometer on card A23).				100 ± 5 MS	_____														
2.65	01B2	Remove jumper between B19P and B13J.																			
2.66	01B2	Connect preamplifier channel A to B18F and channel B to B18E																			
2.67	CE	Trigger oscilloscope externally with 10 CPS MV signal (10 MV test jack).																			
2.68	01B2	Observe that rise of pulse on channel B is delayed from rise of pulse on channel A (adjust potentiometer on card B18).				3.6 ± .1MS	_____														
2.69	01B2	Connect preamplifier channel A to B14B.																			
2.70	NA	Trigger oscilloscope internally.																			
2.71	01B2	Observe duration of negative going portion of waveshape (adjust potentiometer on card B14).				2.8 ± .1MS	_____														
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER	
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Figure 7-3. Timing Adjustments (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
2.72	01B2	Observe duration of positive going portion of waveshape (adjust potentiometer on card B15).	.6 ± .05MS	_____
EXP	NA	Steps 2.73 through 2.91 substantiate the single shots and delay which develop tape reader timing and control signals are adjusted properly.		
2.73	03B6	Connect preamplifier channel A to A13B.		
2.74	03B6	Observe duration of negative going portion of waveshape (adjust potentiometer on card A13).	100 ± 2 usec	_____
2.75	CE	Connect preamplifier channel A to TRCP1 test jack and channel B to TRCP2 test jack.		
2.76	CE	Trigger oscilloscope externally with 500 MV signal (500 MV test jack).		
2.77	03B6	Observe duration of T1 (see Illustration B (adjust potentiometer on card A14).	250 ± 10 usec	_____
2.78	03B6	Observe duration of T2 (see Illustration B (adjust potentiometer on card A15).	350 ± 10 usec	_____
2.79	03B6	Observe duration of T3 (see Illustration B (adjust potentiometer on card B15).	250 ± 10 usec	_____
2.80	CE	Connect preamplifier channel A to TRCP3 test jack and channel B to TRCP4 test jack.		

Figure 7-3. Timing Adjustments (Sheet 9)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

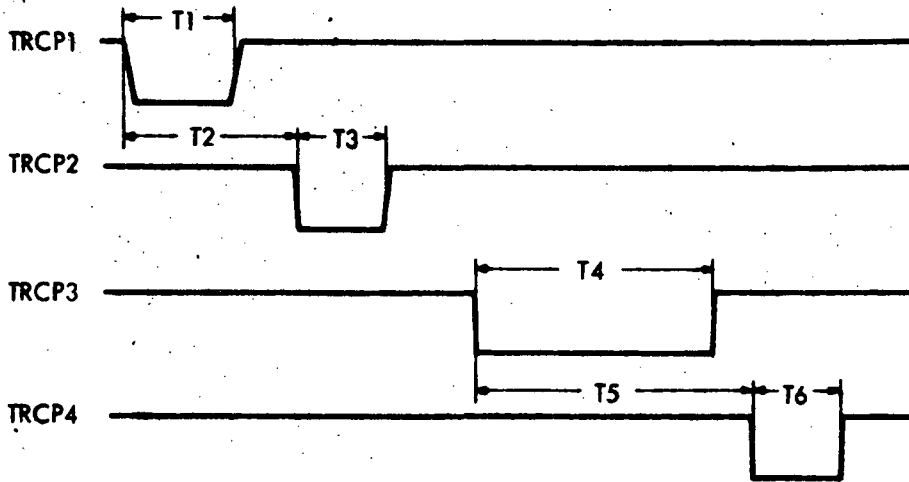


Illustration B. Tape Reader Clock Timing

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER	
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Figure 7-3. Timing Adjustments (Sheet 10)

INTERNATIONAL BUSINESS MACHINES--												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
2.81	03B6	Observe duration of T4 (see Illustration B (adjust potentiometer on card A16).							500 ± 10 usec	_____		
2.82	03B6	Observe duration of T5 (see Illustration B (adjust potentiometer on card A17).							600 ± 20 usec	_____		
2.83	03B6	Observe duration of T6 (see Illustration B (adjust potentiometer on card B16).							200 ± 10 usec	_____		
2.84	03B6	Connect preamplifier channel A to B18F and channel B to B18E.										
2.85	CE	Trigger oscilloscope externally with 10 CPS MV signal (10MV test jack).										
2.86	03B6	Observe that rise of pulse on channel B is delayed from rise of pulse on channel A (adjust potentiometer on card B18).							30 ± 2 MS	_____		
2.87	03B6	Connect preamplifier channel A to A19-B.										
2.88	NA	Trigger oscilloscope internally.										
2.89	03B6	Observe duration of negative going portion of waveshape (adjust potentiometer on card A19).							6 ± .3 MS	_____		
2.90	03B6	Connect preamplifier channel A to A20B.										
2.91	03B6	Observe duration of negative going portion of waveshape (adjust potentiometer on card A20).							.5 ± .1 MS	_____		

Figure 7-3. Timing Adjustments (Sheet 11)

INTERNATIONAL BUSINESS MACHINES--										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
EXP	NA	Steps 2.92 through 2.99 substantiate that the single shot which develops printer RST process signal is adjusted properly.								
2.92	01B3	Connect preamplifier channel A to D05B.								
2.93	01B3	Observe duration of negative going portion of waveshape (adjust potentiometer on card D05).					1.42 ± .01 usec	_____		
2.94	01B3	Connect preamplifier channel A to F17B.								
2.95	01B3	Observe duration of negative going portion of waveshape (adjust potentiometer on card F17).					.5 ± .1 usec	_____		
2.96	01B3	Connect scope channel A to F08B.								
2.97	NA	Observe duration of the negative going portion of the waveshape (adjust potentiometer on card F08).					5 ± .5 usec	_____		
2.98	01B3	Connect scope channel A to F07B.								
2.99	NA	Observe duration of the negative going portion of waveshape (adjust potentiometer on card F07).								
EXP	NA	Steps 2.100 through 2.102 substantiate that the single shot which develops interrupt INH CTRL signals is adjusted properly.								

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 12)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:									UNIT NO.											
Step	Panel	Operation					Normal Indication	Data												
2.100	PD	Observe INHIBIT control pushbutton/lamp (press and release if not lit).					Lit	_____												
2.101	02B5	Connect preamplifier channel A to A14B.						_____												
2.102	02B5	Observe duration of negative going portion of waveshape (adjust potentiometer on card A14).					30 ± 2 MS	_____												
EXP	NA	Steps 2.103 through 2.131 substantiate that the single shots and delays which develop memory timing are adjusted properly.						_____												
2.103	02B1	Connect preamplifier channel A to E06Q (RD + WR A).						_____												
2.104	02A4	Connect preamplifier channel B to E19B (RD + WR DLY 0.75 A).						_____												
2.105	CE	Trigger oscilloscope externally on phase A bit gate 8 signal (PHASE/BIT GATE/CLOCK jack).						_____												
2.106	02B1	Observe duration of T1 (see Illustration C) (1270 NSEC delay card E25).					780 + 30 NSEC	_____												
2.107	02B1	Connect preamplifier channel A to F14E (RD + WR B).						_____												
2.108	02A4	Connect preamplifier channel B to E19D (RD + WR DLY 0.75 B).						_____												
2.109	02B1	Observe duration of T1 (see Illustration C) (1270 NSEC delay card E22).					780 + 30 NSEC	_____												
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 13)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

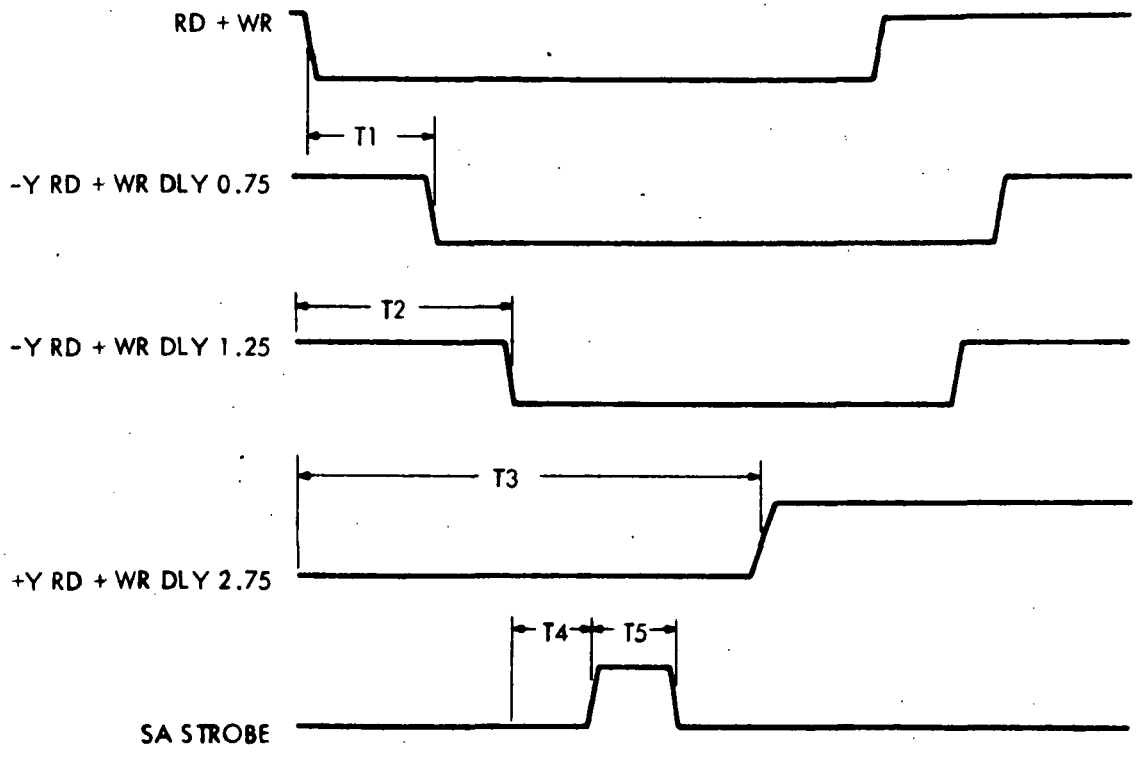


Illustration C. Memory Timing

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Figure 7-3. Timing Adjustments (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
2.110	02B1	Connect preamplifier channel A to E06Q (RD + WR A).								
2.111	02A4	Connect preamplifier channel B to E18R (RD + WR DLY 1.25 A).								
2.112	02B1	Observe duration of T2 (see Illustration C) (1270 NSEC delay card E23).					1200 ± 30 NSEC			
2.113	02B1	Connect preamplifier channel A to F14E (RD + WR B).								
2.114	02A4	Connect preamplifier channel B to E18B (RD + WR DLY 1.25 B).								
2.115	02B1	Observe duration of T2 (see Illustration C) (1270 NSEC delay card F23).					1200 ± 30 NSEC			
2.116	02B1	Connect preamplifier channel A to E06Q (RD + WR A).								
2.117	02A4	Connect preamplifier channel B to E19A (RD + WR DLY 2.75 A).								
2.118	02B1	Observe duration of T3 (see Illustration C) (1270 NSEC delay card E24).					3000 ± 20 NSEC			
2.119	02B1	Connect preamplifier channel A to F14E (RD + WR B).								
2.120	02A4	Connect preamplifier channel B to E19E (RD + WR DLY 2.75 B).								
2.121	02B1	Observe duration of T3 (see Illustration C) (1270 NSEC delay card F22).					3000 ± 20 NSEC			

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Figure 7-3. Timing Adjustments (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:							UNIT NO.													
Step	Panel	Operation				Normal Indication	Data													
2.122	02A4	Connect preamplifier channel A to E18R (RD + WR DLY 1.25 A).																		
2.123	02A6	Connect preamplifier channel B to C19R (SA STROBE A).																		
2.124	02B1	Observe that duration of T4 (see Illustration C) is within ± 30 NSEC of A timing indicated on Memory Strobe Setting tag (1270 NSEC delay card C25).																		
2.125	02B1	Observe duration of T5 (see Illustration C) (1270 NSEC delay card D21).				600 ± 50 NSEC	_____													
2.126	02A4	Connect preamplifier channel A to E18B (RD + WR DLY 1.25 B).																		
2.127	02A6	Connect preamplifier channel B to C10 R (SA STROBE B).																		
2.128	02B1	Observe that duration of T4 (see Illustration D) is within ± 30 NSEC of B timing indicated on Memory Strobe setting tag. (1270 NSEC delay card F24).																		
2.129	02B1	Observe duration of T5 (see Illustration C) (1270 NSEC delay card D25).				600 ± 50 NSEC	_____													
2.130	TRMC	Press and release Free Run Single Shot pushbutton/lamp.																		
2.131	TRMC	Observe Free Run Single Shot lamp				Not lit	_____													
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-3. Timing Adjustments (Sheet 16)

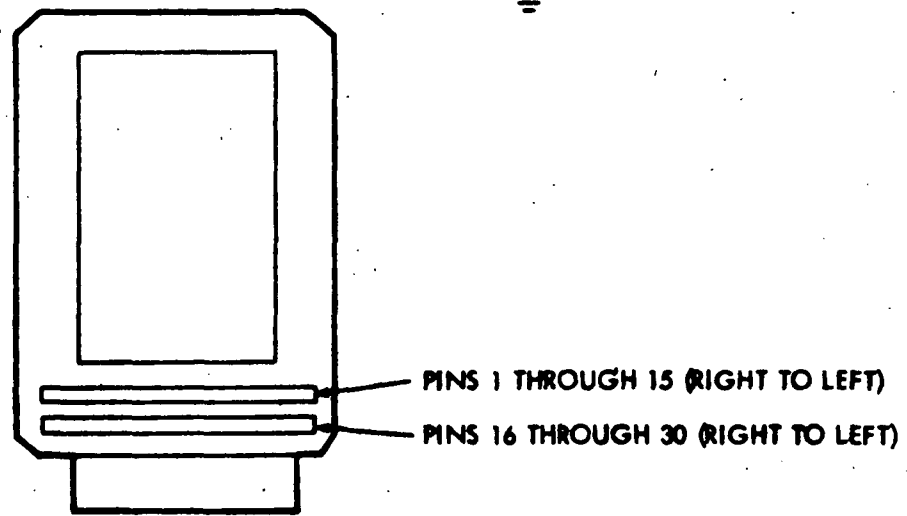
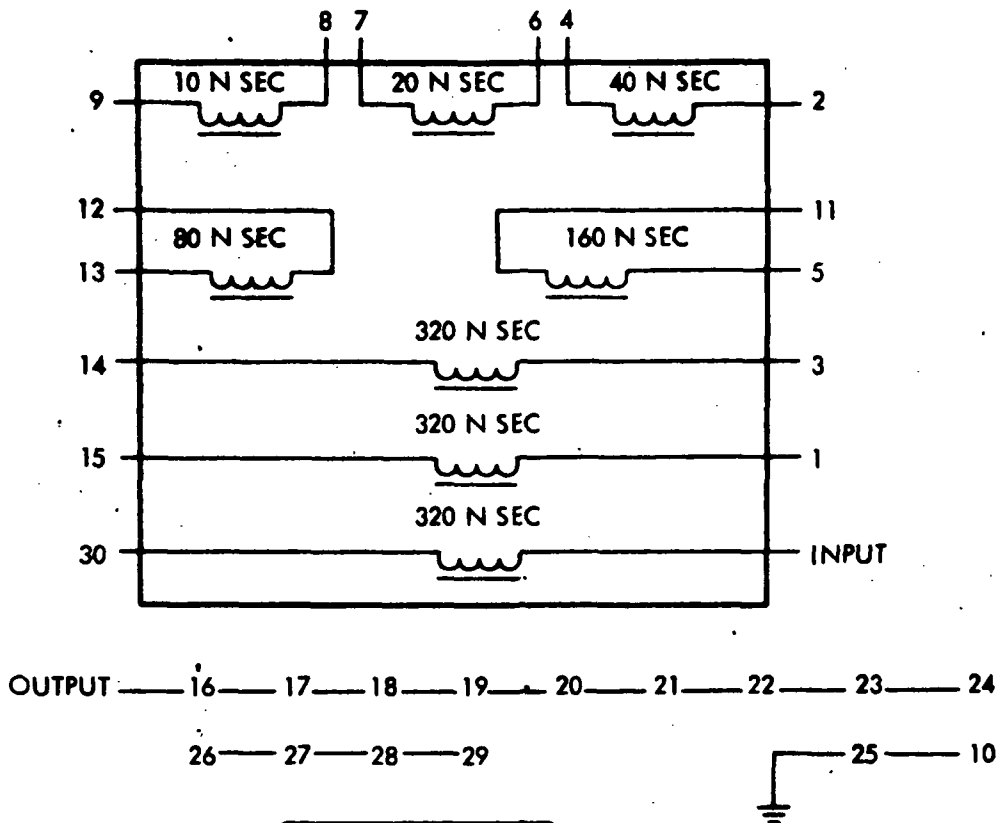


Figure 7-4. 1270 NSEC Delay Card

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:											UNIT NO.										
Step	Panel	Operation									Normal Indication	Data									
EXP	NA	Steps 3. 1 through 3. 32 substantiate that the tape reader control circuits are functioning properly.																			
3. 1	TRMC	Observe REVERSE lamp (press and release if lit).									Not lit	_____									
3. 2	TRMC	Observe FORWARD lamp.									Lit	_____									
3. 3	TRMC	Observe AUTO lamp (press and release if lit).									Not lit	_____									
3. 4	TRMC	Observe MANUAL lamp.									Lit	_____									
3. 5	TRMC	Observe DD lamp (press and release if not lit).									Lit	_____									
3. 6	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.																			
3. 7	TRMC	Observe AUTO lamp									Lit	_____									
3. 8	TRMC	Observe MANUAL lamp.									Not lit	_____									
3. 9	TRMC	Observe ML lamp.									Lit	_____									
3. 10	TRMC	Observe DD lamp.									Not lit	_____									
3. 11	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.																			
3. 12	TRMC	Observe AUTO lamp.									Not lit	_____									
3. 13	TRMC	Observe MANUAL lamp.									Lit	_____									
3. 14	TRMC	Observe START lamp.									Not lit	_____									
3. 15	TRMC	Observe STOP lamp.									Lit	_____									
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 1 of 14)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:												UNIT NO.								
Step	Panel	Operation										Normal Indication	Data							
3.16	TRMC	Observe FREE RUN SS lamp (press and release if lit).										Not lit	_____							
3.17	TRMC	Observe FREE RUN READER lamp (press and release if lit).										Not lit	_____							
3.18	TRMC	Observe SELF CHECK lamp (press and release if not lit).										Lit	_____							
3.19	MLDD	Press and release ERROR RESET pushbutton/lamp.																		
3.20	TRMC	Observe PWR ON lamp (press and release if not lit).										Lit	_____							
3.21	TRMC	Observe PWR OFF lamp.										Not lit	_____							
3.22	TRMC	Observe INHIBIT READER CONTROL lamp (press and release if lit).										Not lit	_____							
3.23	TRMC	Observe MANUAL ADVANCE TAPE lamp.										Lit	_____							
3.24	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.																		
3.25	TRMC	Observe STOP lamp.										Not lit	_____							
3.26	TRMC	Observe MANUAL ADVANCE TAPE lamp.										Not lit	_____							
3.27	TRMC	Press and release FREE RUN SS pushbutton/lamp.																		
3.28	TRMC	Observe FREE RUN SS lamp.										Lit	_____							
3.29	TRMC	Observe PWR ON lamp.										Not lit	_____							
3.30	TRMC	Observe PWR OFF lamp.										Lit	_____							
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
3.31	TRMC	Observe MANUAL ADVANCE TAPE lamp.				Lit	_____		
3.32	TRMC	Observe STOP lamp.				Lit	_____		
EXP	NA	Steps 3.33 through 3.47 substantiate that the tape reader clock pulse error circuit is functioning properly.							
3.33	MLDD	Observe TAPE-TRCP lamp (press and release ERROR RESET pushbutton if lit).				Not lit	_____		
3.34	MLDD	Press and release IS1 pushbutton/lamp.							
3.35	MLDD	Observe TAPE-TRCP lamp.				Lit	_____		
3.36	MLDD	Press and release ERROR RESET pushbutton/lamp.							
3.37	MLDD	Observe TAPE-TRCP lamp				Not lit	_____		
3.38	MLDD	Press and release IS2 pushbutton/lamp.							
3.39	MLDD	Observe TAPE-TRCP lamp				Lit	_____		
3.40	MLDD	Press and release ERROR RESET pushbutton/lamp.							
3.41	MLDD	Observe TAPE-TRCP lamp.				Not lit	_____		
3.42	MLDD	Press and release IS3 pushbutton/lamp.							
3.43	MLDD	Observe TAPE-TRCP lamp.				Lit	_____		

Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation							Normal Indication	Data										
3.44	MLDD	Press and release ERROR RESET pushbutton/lamp.																		
3.45	MLDD	Observe TAPE-TRCP lamp							Not lit	_____										
3.46	MLDD	Press and release IS4 pushbutton/lamp.																		
3.47	MLDD	Observe TAPE-TRCP lamp.							Lit	_____										
EXP	NA	Steps 3.48 through 3.64 substantiate that the tape reader character bits can be monitored at corresponding test jacks on CE panel.																		
3.48	CE	Connect preamplifier channels A and B to TRCB 1 and 2 test jacks respectively.																		
3.49	CE	Trigger oscilloscope externally on TCCB 1 signal (TRCB 1 test jack).																		
3.50	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A							1.8 to 2.2 MS	_____										
3.51	CE	Disconnect preamplifier from TRCB 2 test jack and connect to TRCB 3.																		
3.52	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							3.6 to 4.4 MS	_____										
3.53	CE	Disconnect preamplifier from TRCB 3 test jack and connect to TRCB 4 test jack.																		
3.54	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							5.4 to 6.6 MS	_____										
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES -												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
3.55	CE	Disconnect preamplifier from TRCB 4 test jack and connect to TRCB 5 test jack.										
3.56	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							7.2 to 8.8 MS			
3.57	CE	Disconnect preamplifier from TRCB 5 test jack and connect to TRCB 6 test jack										
3.58	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							9.0 to 11.0 MS			
3.59	CE	Disconnect preamplifier from TRCB 6 test jack and connect to TRCB 7 test jack.										
3.60	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							10.8 to 13.2 MS			
3.61	CE	Disconnect preamplifier from TRCB 7 test jack and connect to TRCB 8 test jack.										
3.62	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							12.6 to 15.4 MS			
3.63	CE	Disconnect preamplifier from TRCB 8 test jack and connect to TRCB 9 test jack.										
3.64	CE	Observe that fall of pulse on channel B is delayed from fall of pulse on channel A.							14.4 to 17.6 MS			

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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
EXP	NA	Steps 3.65 through 3.111 substantiate that tape information read by the tape reader can be monitored at CHANNEL-1 through 6, SEQ BIT TAPB, and FEED TRACK test jacks on CE panel.		
3.65	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.		
3.66	TRMC	Observe AUTO lamp.	Lit	_____
3.67	TRMC	Observe MANUAL lamp.	Not lit	_____
3.68	TRMC	Press and release FREE RUN SS pushbutton/lamp		
3.69	TRMC	Observe FREE RUN SS lamp	Not lit	_____
3.70	TRMC	Observe MANUAL ADVANCE TAPE lamp.	Not lit	_____
3.71	MLDD	Press and release ERROR RESET pushbutton/lamp.		
3.72	TRMC	Observe PWR ON lamp.	Lit	_____
3.73	TRMC	Observe PWR OFF lamp.	Not lit	_____
3.74	TRMC	Observe START lamp.	Lit	_____
3.75	MLDD	Observe TAPE TRCP lamp.	Not lit	_____
3.76	TRMC	Press and release AUTO/MANUAL pushbutton/lamp		
3.77	TRMC	Observe START lamp.	Not lit	_____
3.78	TRMC	Observe AUTO lamp.	Not lit	_____

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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
3.79	TRMC	Observe MANUAL lamp.	Lit	_____
3.80	NA	Remove plastic guard from tape spooler		
3.81	NA	Lower tape guide on read step photocell assembly to its bottom stop (A on Illustration A).		
3.82	NA	Thread tape reader exercise tape as shown on Illustration A.		
3.83	NA	Check for proper alignment of the tape within the guides of the read station.		
3.84	NA	Raise the tape guide.		
3.85	NA	Replace plastic guard.		
3.86	TRMC	Press and release FREE RUN READER pushbutton/lamp.		
3.87	TRMC	Observe FREE RUN READER lamp.	Lit	_____
3.88	NA	Observe that tape is continuously driven in the clockwise direction.		
3.89	CE	Connect preamplifier channel A to FEED TRACK test jack		
3.90	NA	Trigger oscilloscope internally		
3.91	CE	Observe duration of square wave	1.8 to 2.2 MS	_____
3.92	CE	Connect preamplifier channel A to TAPB test jack.		

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

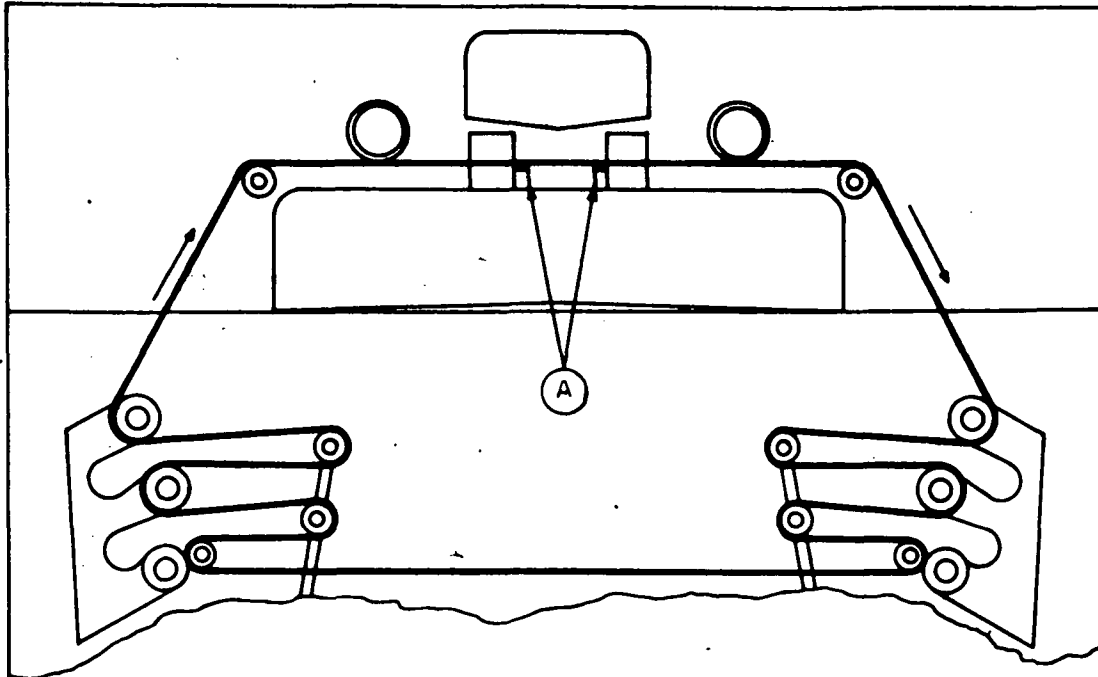


ILLUSTRATION A

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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:							UNIT NO.			
Step	Panel	Operation					Normal Indication	Data		
3.93	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.94	CE	Connect preamplifier channel A to SEQ BIT test jack.						_____		
3.95	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.96	CE	Connect preamplifier channel A to CHANNEL 1 test jack.						_____		
3.97	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.98	CE	Connect preamplifier channel A to CHANNEL 2 test jack.						_____		
3.99	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.100	CE	Connect preamplifier channel A to CHANNEL 3 test jack.						_____		
3.101	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.102	CE	Connect preamplifier channel A to CHANNEL 4 test jack.						_____		
3.103	CE	Observe duration of positive going portion of waveshape.					0.8 to 1.2 MS	_____		
3.104	CE	Connect preamplifier channel A to CHANNEL 5 test jack.						_____		
3.105	CE	Observe duration of positive going portion of waveshape					0.8 to 1.2 MS	_____		

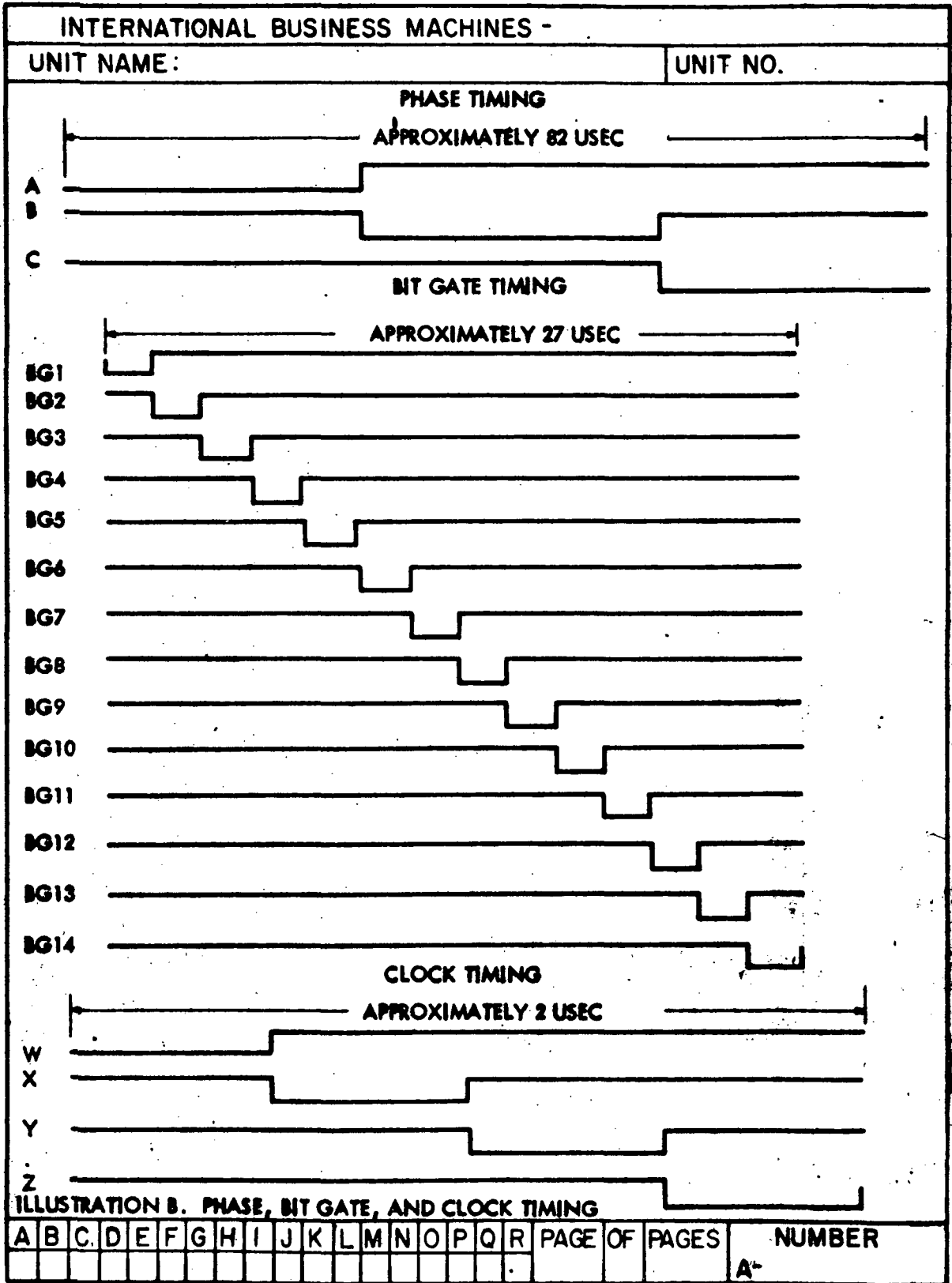
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
3.106	CE	Connect preamplifier channel A to CHANNEL 6 test jack.										
3.107	CE	Observe duration of positive going portion of waveshape.								0.8 to 1.2 MS	_____	
3.108	CE	Press and release FREE RUN READER pushbutton/lamp.										
3.109	CE	Observe FREE RUN READER pushbutton/lamp.								Not lit	_____	
3.110	NA	Observe that tape is stopped.										
3.111	NA	Remove tape from tape spooler and reader.										
EXP	NA	Steps 3.112 through 3.119 substantiate that timing pulses selected by the PHASE/BIT GATE/CLOCK switch appear at the PHASE/BIT GATE/CLOCK jack on CE panel.										
3.112	CE	Connect preamplifier channel A to PHASE/BIT GATE/CLOCK jack.										
3.113	NA	Trigger oscilloscope externally on phase A signal (02B2026L).										
3.114	CE	Set BIT GATE and CLOCK switches to the ALL position.										
3.115	CE	Observe that waveshapes for the A, B, and C positions of PHASE switch are as shown in Illustration B.									_____	
3.116	CE	Set PHASE switch to the ALL position.										

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 10)



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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES--																																																				
UNIT NAME:								UNIT NO.																																												
Step	Panel	Operation					Normal Indication	Data																																												
3.117	CE	Observe that waveshapes for the 1 through 14 positions of BIT GATE switch are as shown in Illustration B.						_____																																												
3.118	CE	Set BIT GATE switch to the ALL position.						_____																																												
3.119	CE	Observe that waveshapes for the W, X, Y, and Z positions of CLOCK switch are as shown in Illustration B.						_____																																												
EXP	NA	Steps 3.120 through 3.136 substantiate that the printer timing pulses are within tolerance.						_____																																												
3.120	TRMC	Press and release FREE RUN SS pushbutton/lamp.						_____																																												
3.121	TRMC	Observe FREE RUN SS lamp.					Lit	_____																																												
3.122	01B3	Connect a jumper between pins C13D and C13J.						_____																																												
3.123	01B3	Connect preamplifier channels A and B to C14L and F21E respectively						_____																																												
3.124	01B3	Trigger oscilloscope externally on signal at 01B3D06A.						_____																																												
3.125	01B3	Observe duration of T1 (see Illustration C).					8.70 to 10.20 USEC	_____																																												
3.126	01B3	Observe duration of T2 (see Illustration C).					2.90 to 3.30 USEC	_____																																												
3.127	01B3	Disconnect preamplifier from F21E and connect to F21L.						_____																																												
3.128	01B3	Observe duration of T3 (see Illustration C).					1.45 to 1.70 USEC	_____																																												
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

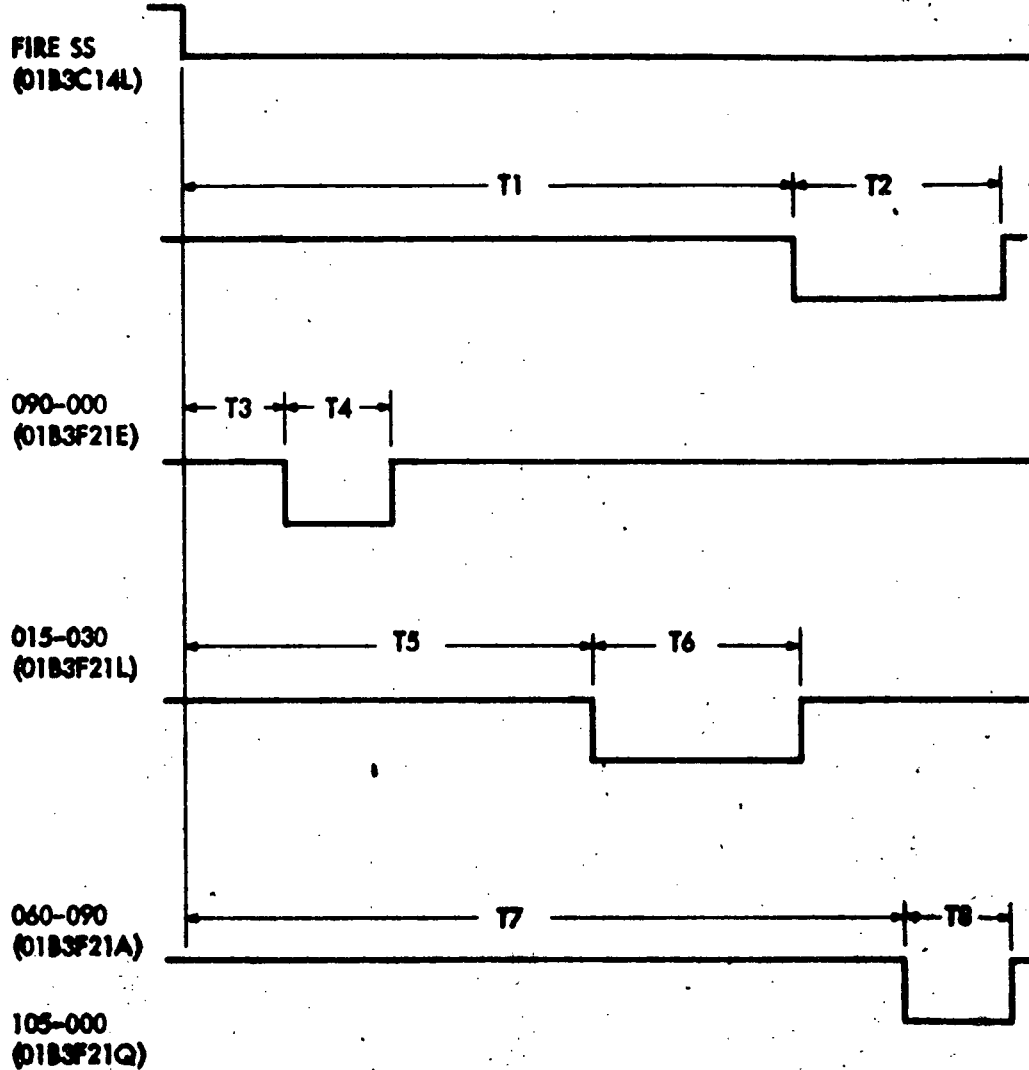


ILLUSTRATION C. PRINTER TIMING

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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
3.129	01B3	Observe duration of T4 (see Illustration C).					1.40 to 1.45 USEC	_____		
3.130	01B3	Disconnect preamplifier from F21L and connect to F21A.						_____		
3.131	01B3	Observe duration of T5 (see Illustration C).					5.80 to 6.80 USEC	_____		
3.132	01B3	Observe duration of T6 (see Illustration C).					2.90 to 3.30 USEC	_____		
3.133	01B3	Disconnect preamplifier from F21A and connect to F21Q.						_____		
3.134	01B3	Observe duration of T7 (see Illustration C)					10.15 to 11.90 USEC	_____		
3.135	01B3	Observe duration of T8 (see Illustration C).					1.40 to 1.45 USEC	_____		
3.136	01B3	Remove jumper from pins C13D and C13J.						_____		

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-5. Tape Reader Controls and PTC and Printer Timing Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES -																				
UNIT NAME:											UNIT NO.									
Step	Panel	Operation								Normal Indication	Data									
EXP	NA	Steps 4.1 through 4.21 substantiate that the TAPE READER CONTROL, MODE, TAPE ADDRESS, and TAPE READER SELF CHECK pushbutton/lamp are functioning properly and are in the correct configuration.																		
4.1	TRMC	Observe FREE RUN SS lamp (press and release if lit).								Not lit	_____									
4.2	TRMC	Observe FREE RUN READER lamp (press and release if lit).								Not lit	_____									
4.3	TRMC	Observe PWR OFF lamp (press and release if lit)								Not lit	_____									
4.4	TRMC	Observe PWR ON lamp								Lit	_____									
4.5	TRMC	Observe INHIBIT READER CONTROL lamp (press and release if not lit).								Lit	_____									
4.6	TRMC	Observe REVERSE lamp (press and release if lit).								Not lit	_____									
4.7	TRMC	Observe FORWARD lamp.								Lit	_____									
4.8	TRMC	Observe VERIFY ONLY lamp (press and release if lit).								Not lit	_____									
4.9	TRMC	Observe STOP lamp.								Lit	_____									
4.10	TRMC	Observe AUTO lamp (press and release if lit).								Not lit	_____									
4.11	TRMC	Observe MANUAL lamp.								Lit	_____									
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-6. Memory Loader Automatic Checks (Sheet 1 of 14)

INTERNATIONAL BUSINESS MACHINES-											
UNIT NAME:									UNIT NO.		
Step	Panel	Operation					Normal Indication	Data			
4.12	TRMC	Observe DD lamp (press and release if lit).					Not lit	_____			
4.13	TRMC	Observe ML lamp.					Lit	_____			
4.14	TRMC	Observe ADV CTR lamp (press and release if lit).					Not lit	_____			
4.15	TRMC	Observe SEL ADR lamp.					Lit	_____			
4.16	TRMC	Observe SELF CHECK lamp (press and release if not lit).					Lit	_____			
4.17	TRMC	Observe ADR 1 through ADR 5 lamps (press and release if lit).					Not lit	_____			
4.18	TRMC	Press and release ADV CTR/SEL ADR pushbutton/lamp.						_____			
4.19	TRMC	Observe ADV CTR lamp.					Not lit	_____			
4.20	TRMC	Observe SEL ADR lamp.					Not lit	_____			
4.21	TRMC	Observe tape word counter lamps (2 ⁰ through 2 ¹²) (if any lamps are lit press and release as many times as necessary starting with lowest order lamp lit).					Not lit	_____			
EXP	NA	Steps 4.22 through 4.33 substantiate that the tape reader and display self test tape is correctly loaded on the tape spooler and reader.						_____			
4.22	NA	Remove plastic guard from tape spooler.						_____			

Figure 7-6. Memory Loader Automatic Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:							UNIT NO.			
Step	Panel	Operation					Normal Indication	Data		
4.23	NA	Lower tape guide on read step photocell assembly to its bottom stop (B on Illustration A).								
4.24	NA	Place the reel containing self test tape part number 6001247 on left nub with edge of tape closest to sprocket holes next to panel.								
4.25	NA	Thread tape as shown on Illustration A.								
4.26	NA	Position the tape so that leader portion (sprocket holes only) following the punched title is under the photocell.								
4.27	NA	Check for proper alignment of the tape within the guides of the read station.								
4.28	NA	Raise the tape guide.								
4.29	NA	Adjust tape tension by rotating both reels manually until the tension arms (A on Illustration A) are located at the approximate center of their swing.								
4.30	NA	Replace plastic guard.								
4.31	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.								
4.32	NA	Observe that tape advances until the beginning of the punched area is reached.								

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		
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Figure 7-6. Memory Loader Automatic Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

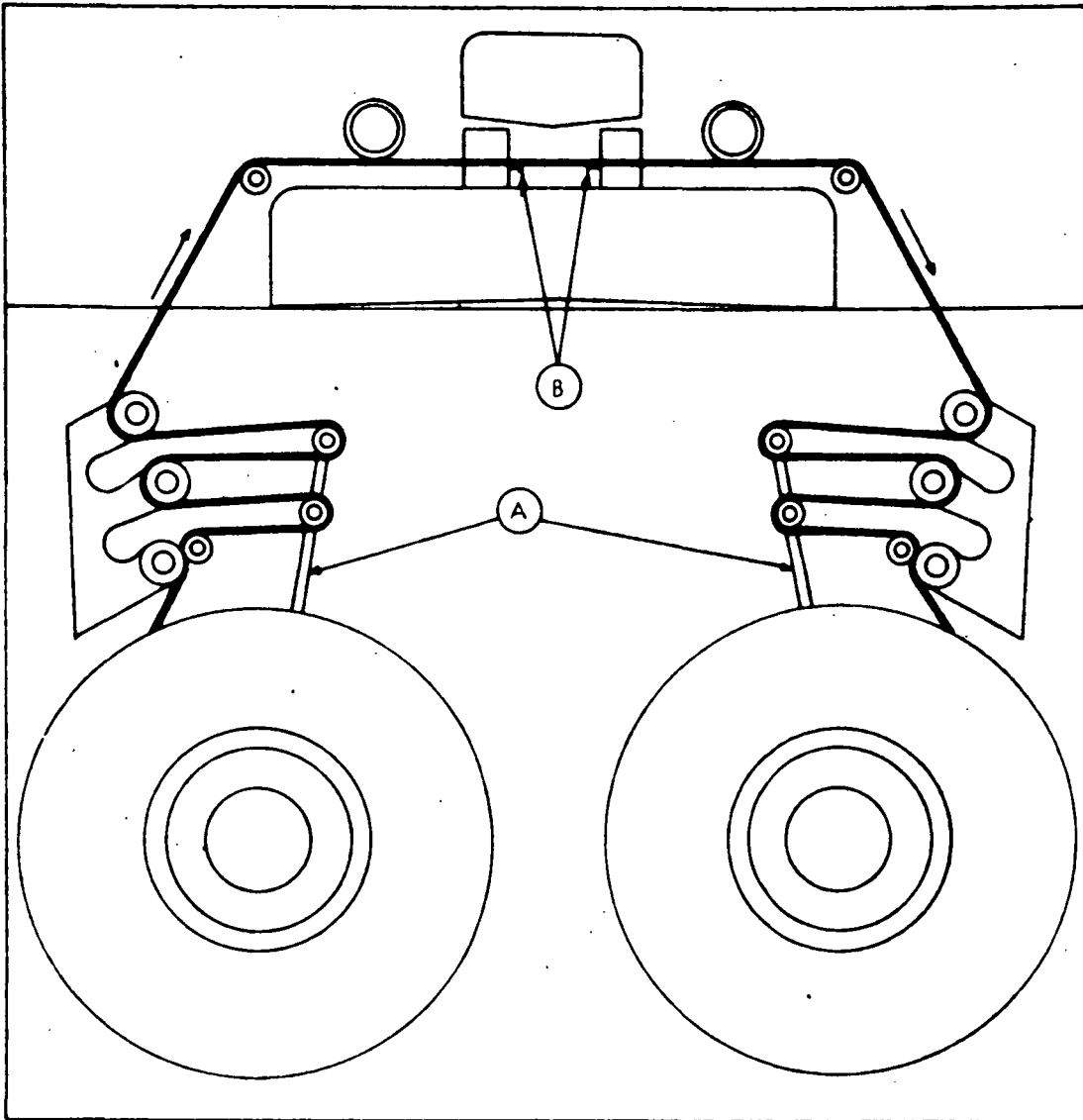


ILLUSTRATION A

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
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Figure 7-6. Memory Loader Automatic Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
4.33	TRMC	Observe that tape word counter lamps indicate a count of one (20 only is lit).										
EXP	NA	Steps 4.34 through 4.46 substantiate that the error test, error reset, and invert error features are functioning properly.										
4.34	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.										
4.35	TRMC	Observe AUTO lamp.							Lit			
4.36	TRMC	Observe START lamp.							Lit			
4.37	TRMC	Observe MANUAL lamp.							Not lit			
4.38	TRMC	Press and release ERROR DEVICES TEST pushbutton/lamp.										
4.39	MLDD	Observe PARITY, TAPE, and COMPARE ERRORS lamps.							Lit			
4.40	MLDD	Press and release ERROR RESET pushbutton/lamp.										
4.41	MLDD	Observe PARITY, TAPE, and COMPARE ERRORS lamps.							Not lit			
4.42	TRMC	Press and release START pushbutton/lamp.										
4.43	NA	Observe that tape advances and stops.										

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Figure 7-6. Memory Loader Automatic Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:										UNIT NO.			
Step	Panel	Operation								Normal Indication	Data		
4.44	TRMC	Observe that tape word counter lamps indicate a count of four (2 ² only is lit).									_____		
4.45	MLDD	Observe INVERT ERROR lamp.								Lit	_____		
4.46	MLDD	Observe PARITY, TAPE, and COMPARE lamps.								Not lit	_____		
EXP	NA	Steps 4.47 through 4.50 substantiate that parity error and tape error circuits are functioning properly.											
4.47	TRMC	Press and release START pushbutton/lamp.											
4.48	NA	Observe that tape advances and stops.									_____		
4.49	MLDD	Observe TAPE-SE2 lamp.								Lit	_____		
4.50	TRMC	Observe that tape word counter lamps indicate a count of 32g (2 ⁴ , 2 ³ , 2 ¹ only are lit).									_____		
EXP	NA	Steps 4.51 through 4.84 substantiate that information can be correctly loaded into the central processor memory in the AUTO mode.											
4.51	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.											
4.52	TRMC	Observe MANUAL lamp.								Lit	_____		

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Figure 7-6. Memory Loader Automatic Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
4.53	TRMC	Observe AUTO lamp.					Not lit	_____		
4.54	TRMC	Observe START lamp.					Not lit	_____		
4.55	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.								
4.56	NA	Observe that tape advances and stops.						_____		
4.57	TRMC	Observe that tape word counter lamps indicate a count of 33g (2 ⁴ , 2 ³ , 2 ¹ , and 2 ⁰ only are lit).						_____		
4.58	MLDD	Press and release ERROR RESET pushbutton/lamp.								
4.59	MLDD	Observe TAPE-SE2 ERRORS lamp.					Not lit	_____		
4.60	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.								
4.61	TRMC	Observe AUTO lamp.					Lit	_____		
4.62	TRMC	Observe START lamp.					Lit	_____		
4.63	TRMC	Observe MANUAL lamp.					Not lit	_____		
4.64	TRMC	Press and release START pushbutton/lamp.								
4.65	NA	Observe that tape advances and stops.								

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Figure 7-6. Memory Loader Automatic Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
4.66	TRMC	Observe that tape word counter lamps indicate a count of 235g (2 ⁷ , 2 ⁴ , 2 ³ , 2 ² , and 2 ⁰ only are lit).		
4.67	MLDD	Observe TAPE-SE2 lamp.	Lit	_____
4.68	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.		
4.69	TRMC	Observe MANUAL lamp.	Lit	_____
4.70	TRMC	Observe AUTO lamp.	Not lit	_____
4.71	TRMC	Observe START lamp.	Not lit	_____
4.72	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.		
4.73	NA	Observe that tape advances and stops.		_____
4.74	TRMC	Observe that tape word counter lamps indicate a count of 236g (2 ⁷ , 2 ⁴ , 2 ³ , 2 ² , and 2 ¹ only are lit).		_____

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Figure 7-6. Memory Loader Automatic Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
4.75	MLDD	Press and release ERROR RESET pushbutton/lamp.							
4.76	MLDD	Observe TAPE-SE2 ERRORS lamp.				Not lit	_____		
4.77	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.							
4.78	TRMC	Observe AUTO lamp.				Lit	_____		
4.79	TRMC	Observe START lamp.				Lit	_____		
4.80	TRMC	Observe MANUAL lamp.				Not lit	_____		
4.81	TRMC	Press and release START pushbutton/lamp.							
4.82	NA	Observe that tape advances and stops.					_____		
4.83	TRMC	Observe that tape word counter lamps indicate a count of 437 ₈ (2 ⁸ , 2 ⁴ , 2 ³ , 2 ² , 2 ¹ , and 2 ⁰ only are lit).					_____		
4.84	MLDD	Observe TAPE-SE2 lamp.				Lit	_____		
EXP	NA	Steps 4.85 through 4.137 substantiate that the compare error circuits are functioning properly.							
4.85	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.							
4.86	TRMC	Observe MANUAL lamp.				Lit	_____		
4.87	TRMC	Observe AUTO lamp.				Not lit	_____		
4.88	TRMC	Observe START lamp.				Not lit	_____		

Figure 7-6. Memory Loader Automatic Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES--														
UNIT NAME:											UNIT NO:			
Step	Panel	Operation									Normal Indication	Data		
4.89	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.												
4.90	NA	Observe that tape advances and stops										_____		
4.91		Observe that tape word counter lamps indicate a count of 440g (2 ⁸ and 2 ⁵ only are lit).												
4.92	MLDD	Press and release ERROR RESET pushbutton/lamp.												
4.93	MLDD	Observe TAPE-SE2 ERRORS lamp									Not lit	_____		
4.94	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.												
4.95	TRMC	Observe AUTO lamp.									Lit	_____		
4.96	TRMC	Observe START lamp.									Lit	_____		
4.97	TRMC	Observe MANUAL lamp.									Not lit	_____		
4.98	TRMC	Press and release START pushbutton/lamp.												
4.99	NA	Observe that tape advances and stops										_____		
4.100	TRMC	Observe that tape word counter lamps indicate a count of 441g (2 ⁸ , 2 ⁵ , and 2 ⁰ only are lit).												
4.101	MLDD	Observe COMPARE-TRS and SERIAL lamps.									Lit	_____		
4.102	MLDD	Press and release ERROR RESET pushbutton												
4.103	MLDD	Observe COMPARE-TRS and SERIAL lamps.									Not lit	_____		
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Figure 7-6. Memory Loader Automatic Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES—																																																				
UNIT NAME:									UNIT NO.																																											
Step	Panel	Operation					Normal Indication	Data																																												
4 104	TRMC	Press and release START push-button/lamp.																																																		
4.105	NA	Observe that tape advances and stops.																																																		
4.106	TRMC	Observe tape word counter lamps indicate a count of 6128 (2^8 , 2^7 , 2^3 , and 2^1 only are lit)																																																		
4.107	MLDD	Observe COMPARE-AI3, SERIAL, and BR14 lamps.					Lit																																													
4.108	MLDD	Press and release ERROR RESET pushbutton.																																																		
4.109	MLDD	Observe COMPARE-AI3, SERIAL, and BR14 lamps.					Not lit																																													
4.110	TRMC	Press and release START push-button/lamp.																																																		
4.111	NA	Observe that tape advances and stops.																																																		
4.112	TRMC	Observe that tape word counter lamps indicate a count of 613 (2^8 , 2^7 , 2^3 , 2^1 , and 2^0 only are lit).																																																		
4.113	MLDD	Observe COMPARE-AI3, SERIAL, and BR14 lamps.					Lit																																													
4.114	MLDD	Press and release ERROR RESET pushbutton/lamp.																																																		
4.115	MLDD	Observe COMPARE-AI3, SERIAL, and BR14 lamps.					Not lit																																													
4.116	TRMC	Press and release START push-button/lamp.																																																		
4.117	NA	Observe that tape advances and stops.																																																		
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>I</td><td>J</td><td>K</td><td>L</td><td>M</td><td>N</td><td>O</td><td>P</td><td>Q</td><td>R</td><td>PAGE</td><td>PAGES</td><td>NUMBER</td> </tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>of</td><td>A-</td> </tr> </table>											A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER																				of	A-
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Figure 7-6. Memory Loader Automatic Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES—												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
4.118	TRMC	Observe that tape word counter lamps indicate a count of 616g (2 ⁸ , 2 ⁷ , 2 ³ , 2 ² , and 2 ¹ only are lit).									_____	
4.119	MLDD	Observe COMPARE-HOPC1, SSMSC, and SSMBR lamps.								Lit	_____	
4.120	MLDD	Press and release ERROR RESET pushbutton.										
4.121	MLDD	Observe COMPARE-HOPC1, SSMSC, and SSMBR lamps.								Not lit	_____	
4.122	TRMC	Press and release START pushbutton/lamp.										
4.123	NA	Observe that tape advances and stops.									_____	
4.124	TRMC	Observe that tape word counter lamps indicate a count of 643g (2 ⁸ , 2 ⁷ , 2 ⁵ , 2 ¹ , and 2 ⁰ only are lit).									_____	
4.125	MLDD	Observe COMPARE-TRS, SSMSC, and SSMBR lamps.								Lit	_____	
4.126	MLDD	Press and release ERROR RESET pushbutton.										
4.127	MLDD	Observe COMPARE-TRS, SSMSC, and SSMBR lamps.								Not lit	_____	
4.128	TRMC	Press and release START pushbutton/lamp.										
4.129	NA	Observe that tape advances and stops.									_____	
4.130	TRMC	Observe that tape word counter lamps indicate a count of 743g (2 ⁸ , 2 ⁷ , 2 ⁶ , 2 ⁵ , 2 ¹ , and 2 ⁰ only are lit).									_____	
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Figure 7-6. Memory Loader Automatic Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
4.131	MLDD	Observe COMPARE-OAC and SSMBR lamps.							Lit	_____		
4.132	MLDD	Press and release ERROR RESET pushbutton.								_____		
4.133	MLDD	Observe COMPARE-OAC and SSMBR lamps.							Not lit	_____		
4.134	TRMC	Press and release START pushbutton/lamp.								_____		
4.135	NA	Observe that tape advances and stops								_____		
4.136	TRMC	Observe that tape word counter lamps indicate a count of 744g (2 ⁸ , 2 ⁷ , 2 ⁶ , 2 ⁵ , and 2 ² lamps).								_____		
4.137	TRMC	Observe TAPE-SE2 ERRORS lamp.							Lit	_____		
EXP	NA	Steps 4.138 through 4.158 substantiate that the verify only and automatic re-wind features are functioning properly.								_____		
4.138	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.								_____		
4.139	TRMC	Observe MANUAL lamp.							Lit	_____		
4.140	TRMC	Observe AUTO lamp.							Not lit	_____		
4.141	TRMC	Observe START lamp.							Not lit	_____		
4.142	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.								_____		
4.143	NA	Observe that tape advances and stops.								_____		

Figure 7-6. Memory Loader Automatic Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:							UNIT NO.													
Step	Panel	Operation					Normal Indication	Data												
4.144	TRMC	Observe that tape word counter lamps indicate a count of 745g (2 ⁸ , 2 ⁷ , 2 ⁶ , 2 ⁵ , 2 ² , and 2 ⁰ only are lit).																		
4.145	MLDD	Press and release ERROR RESET pushbutton/lamp.																		
4.146	MLDD	Observe TAPE-SE2 ERRORS lamp.					Not lit													
4.147	TRMC	Press and release AUTO MANUAL pushbutton lamp.																		
4.148	TRMC	Observe AUTO lamp.					Lit													
4.149	TRMC	Observe START lamp.					Lit													
4.150	TRMC	Observe MANUAL lamp.					Not lit													
4.151	TRMC	Press and release VERIFY ONLY pushbutton/lamp.																		
4.152	TRMC	Observe VERIFY ONLY lamp.					Lit													
4.153	TRMC	Press and release START pushbutton/lamp.																		
4.154	NA	Observe that tape advances to the end of the punched area. Tape then rewinds back to the beginning of the punched area.																		
4.155	TRMC	Observe that tape word counter lamps indicate a count of 754g (2 ⁸ , 2 ⁷ , 2 ⁶ , 2 ⁵ , 2 ³ , and 2 ² only are lit)																		
4.156	TRMC	Observe REVERSE lamp.					Lit													
4.157	TRMC	Observe FORWARD lamp.					Not lit													
4.158	MLDD	Observe PARITY, TAPE, and COMPARE lamps.					Not lit													
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Figure 7-6. Memory Loader Automatic Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation							Normal Indication	Data											
EXP.	NA	Steps 5.1 through 5.20 substantiate that pushbutton/ lamps and switches which affect the memory loader are in the correct configuration.																			
5.1	TRMC	Observe AUTO lamp (press and release if lit).							Not lit	_____											
5.2	TRMC	Observe MANUAL lamp.							Lit	_____											
5.3	TRMC	Observe DD lamp (press and release if lit).							Not lit	_____											
5.4	TRMC	Observe ML lamp.							Lit	_____											
5.5	TRMC	Observe FREE RUN SS lamp (press and release if lit).							Not lit	_____											
5.6	TRMC	Observe ADV CTR lamp (press and release if lit).							Not lit	_____											
5.7	TRMC	Observe SEL ADR lamp.							Lit	_____											
5.8	TRMC	Observe SELF CHECK lamp (press							Lit	_____											
5.9	TRMC	Observe ADR 1 through ADR 5 lamps (press and release if lit).							Not lit	_____											
5.10	MLDD	Observe PARITY, TAPE, and COMPARE lamps (press and release ERROR RESET pushbutton if lit).							Not lit	_____											
5.11	MLDD	Observe REPEAT lamp.							Not lit	_____											
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Figure 7-7. Memory Loader Manual Checks (Sheet 1 of 20)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.12	MLDD	Observe <u>REPEAT</u> lamp.	Lit	_____
5.13	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		_____
5.14	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps (INSTRUCTION ADDRESS area)	Lit	_____
5.15	MLDD	Observe COMMAND and COMPUTER SYL-0 lamps (INSTRUCTION ADDRESS area).	Lit	_____
5.16	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps (DATA ADDRESS area).	Lit	_____
5.17	MLDD	Observe COMMAND PARITY BIT-SYL 0 and SYL 1 lamps (DATA area).	Lit	_____
5.18	MLDD	Observe all other COMMAND and COMPUTER lamps.	Not lit	_____
5.19	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.20	MLDD	Verify that DISPLAY SELECT switch is set to TRS.		_____
EXP.	NA	Steps 5.21 through 5.170 substantiate that different combinations of data bits can be manually loaded into the tape reader register, compared on correctly, and displayed. NOTE Each time an INSTRUCTION ADDRESS, DATA ADDRESS,		

Figure 7-7. Memory Loader Manual Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-					
UNIT NAME:			UNIT NO.		
Step	Panel	Operation	Normal Indication	Data	
NOTE (cont.)					
DATA, or TAPE ADDRESS pushbutton is pressed, the TAPE TRCP lamp (MLDD panel) lights and goes out when the pushbutton is released.					
5.21	MLDD	Press and release OP4, OP3, OP2, OP1, OA3, SIGN and 1 through 12 pushbutton/lamps.			
5.22	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA3, SIGN; and 1 through 12 lamps.	Lit	_____	
5.23	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____	
5.24	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____	
5.25	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____	
5.26	MLDD	Press and release ADDRESS COMPTR pushbuttons.			
5.27	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, SIGN, and 1 through 12 lamps.	Lit	_____	
5.28	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Lit	_____	
5.29	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____	
5.30	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____	
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Figure 7-7. Memory Loader Manual Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.31	MLDD	Press and release SIGN and 1 through 12 pushbutton/lamps.		
5.32	MLDD	Observe COMMAND-SIGN and 1 through 12 lamps.	Not lit	_____
5.33	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.34	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.35	MLDD	Press and release COMPTR DISPLAY RESET pushbuttons.		
5.36	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, SIGN, and 1 through 12 lamps.	Not lit	_____
5.37	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.38	MLDD	Press and release OA1 and 13 through 25 pushbutton/lamps.		
5.39	MLDD	Observe COMMAND-OA1 and 13 through 25 lamps.	Lit	_____
5.40	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Not lit	_____
5.41	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.42	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.43	MLDD	Press and release ADDRESS COMPTR pushbuttons.		

Figure 7-7. Memory Loader Manual Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
5.44	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, OA1, and 13 through 25 lamps.	Lit	_____
5.45	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.46	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Lit	_____
5.47	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.48	MLDD	Press and release OA1 and 13 through 25 pushbutton/lamps.		
5.49	MLDD	Observe COMMAND-OA1 and 13 through 25 lamps.	Not lit	_____
5.50	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.51	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.52	MLDD	Press and release COMPTR DISPLAY RESET pushbuttons.		
5.53	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, OA1, and 13 through 25 lamps.	Not lit	_____
5.54	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.55	MLDD	Press and release OA2, SIGN, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, and 24 pushbutton/lamps.		

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Figure 7-7. Memory Loader Manual Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.56	MLDD	Observe COMMAND-OA2, SIGN, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, and 24 lamps.	Lit	_____
5.57	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.58	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____
5.59	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.60	MLDD	Press and release ADDRESS COMPTR pushbuttons.		
5.61	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, OA2, SIGN, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, and 24 lamps.	Lit	_____
5.62	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Lit	_____
5.63	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.64	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.65	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
5.66	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA3, OA2, SIGN, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, and 24 lamps.	Not lit	_____
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Figure 7-7. Memory Loader Manual Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.67	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.68	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.69	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.70	MLDD	Press and release OP4, OP3, OP2, OP1, OA3, OA2, OA1, 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, and 25 pushbutton/lamps.		
5.71	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA3, OA2, OA1, 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, and 25 lamps.	Lit	_____
5.72	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Not lit	_____
5.73	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.74	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.75	MLDD	Press and release ADDRESS COM-PTR pushbuttons.		
5.76	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA3, OA2, OA1, 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, and 25 lamps.	Lit	_____
5.77		(This step deleted.)		

Figure 7-7. Memory Loader Manual Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.78	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Lit	_____
5.79	MLDD	Observe PARITY. TAPE, and COMPARE lamps.	Not lit	_____
5.80	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
5.81	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA3, OA2, OA1, 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, and 25 lamps	Not lit	_____
5.82	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.83	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.84	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, SIGN, 1 through 5, and 19 through 25 pushbutton/lamps.		
5.85	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, SIGN, 1 through 5, and 19 through 25 lamps.	Lit	_____
5.86	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Not lit	_____
5.87	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.88	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.89	MLDD	Press and release ADDRESS COMPTR pushbuttons.		

Figure 7-7. Memory Loader Manual Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
5.90	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, SIGN, 1 through 5, and 19 through 25 lamps.	Lit	_____
5.91	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.92	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area)	Lit	_____
5.93	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.94	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY pushbuttons.		
5.95	MLDD	Observe COMMAND and COMPUTER OP4, OP3, OP2, OP1, OA4, SIGN, 1 through 5, and 19 through 25 lamps.	Not lit	_____
5.96	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.97	MLDD	Observe COMPUTER PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____
5.98	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, OA1, and 6 through 18 pushbutton/lamps.		
5.99	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, OA1, and 6 through 18 lamps.	Lit	_____
5.100	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____

Figure 7-7. Memory Loader Manual Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:										UNIT NO.
Step	Panel	Operation	Normal Indication	Data						
5.101	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____						
5.102	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____						
5.103	MLDD	Press and release ADDRESS COMPTR pushbuttons.								
5.104	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA1, and 6 through 18 lamps.	Lit	_____						
5.105	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Lit	_____						
5.106	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area)	Not lit	_____						
5.107	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____						
5.108	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.								
5.109	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA4, OA1, and 6 through 18 lamps.	Not lit	_____						
5.110	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____						
5.111	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp.	Lit	_____						
5.112	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____						
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Figure 7-7. Memory Loader Manual Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.113	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, OA2, SIGN, 1, 2, 6, 7, 8, 13, 14, 15, 19, 20, 21, and 22 pushbutton/lamps.		
5.114	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, OA2, SIGN, 1, 2, 6, 7, 8, 13, 14, 15, 19, 20, 21, and 22 lamps.	Lit	_____
5.115	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Not lit	_____
5.116	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.117	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.118	MLDD	Press and release ADDRESS COMPTR pushbuttons.		
5.119	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA2, SIGN, 1, 2, 6, 7, 8, 13, 14, 15, 19, 20, 21, and 22 lamps.	Lit	_____
5.120	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.121	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Lit	_____
5.122	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.123	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		

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Figure 7-7. Memory Loader Manual Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME:

UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.124	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA4, OA2, SIGN, 1, 2, 6, 7, 8, 13, 14, 15, 19, 20, 21, and 22 lamps.	Not lit	_____
5.125	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.126	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.127	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.128	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, OA2, OA1, 3, 4, 5, 9, 10, 11, 12, 16, 17, 18, 23, 24, and 25 pushbutton/lamps.		
5.129	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, OA2, OA1, 3, 4, 5, 9, 10, 11, 12, 16, 17, 18, 23, 24, and 25 lamps.	Lit	_____
5.130	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.131	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____
5.132	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.133	MLDD	Press and release ADDRESS COMPTR pushbuttons.		
5.134	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA2, OA1, 3, 4, 5, 9, 10, 11, 12, 16, 17, 18, 23, 24, and 25 lamps.	Lit	_____

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Figure 7-7. Memory Loader Manual Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.135	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Lit	_____
5.136	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.137	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.138	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
5.139	MLDD	Observe COMMAND and COMPUTER OP4, OP3, OP2, OP1, OA4, OA2, OA1, 3, 4, 5, 9, 10, 11, 12, 16, 17, 18, 23, 24, and 25 lamps.	Not lit	_____
5.140	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.141	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.142	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, OA3, SIGN, 1, 3, 6, 7, 9, 10, 13, 14, 16, 19, 20, and 23 pushbutton/lamps.		
5.143	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, OA3, SIGN, 1, 3, 6, 7, 9, 10, 13, 14, 16, 19, 20, and 23 lamps.	Lit	_____
5.144	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.145	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Not lit	_____

Figure 7-7. Memory Loader Manual Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES--

UNIT NAME :

UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.146	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.147	MLDD	Press and release ADDRESS COMPTR pushbuttons.		
5.148	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA3, SIGN, 1, 3, 6, 7, 9, 10, 13, 14, 16, 19, 20, and 23 lamps.	Lit	_____
5.149	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Lit	_____
5.150	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.151	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.152	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
5.153	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA4, OA3, SIGN, 1, 3, 6, 7, 9, 10, 13, 14, 16, 19, 20, and 23 lamps.	Not lit	_____
5.154	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.155	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.156	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____

Figure 7-7. Memory Loader Manual Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.157	MLDD	Press and release OP4, OP3, OP2, OP1, OA4, OA3, OA1, 2, 4, 5, 8, 11, 12, 15, 17, 18, 21, 22, 24, and 25 pushbutton/lamps.		
5.158	MLDD	Observe COMMAND-OP4, OP3, OP2, OP1, OA4, OA3, OA1, 2, 4, 5, 8, 11, 12, 15, 17, 18, 21, 22, 24, and 25 lamps.	Lit	_____
5.159	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Not lit	_____
5.160	MLDD	Observe COMMAND PARITY BIT-SYL 1 lamp (DATA area).	Lit	_____
5.161	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.162	MLDD	Press and release ADDRESS COMPTR pushbuttons.		
5.163	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA3, OA1, 2, 4, 5, 8, 11, 12, 15, 17, 18, 21, 22, 24, and 25 lamps.	Lit	_____
5.164		(This step deleted.)		
5.165	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Lit	_____
5.166	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.167	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		

Figure 7-7. Memory Loader Manual Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.168	MLDD	Observe COMMAND and COMPUTER-OP4, OP3, OP2, OP1, OA4, OA3, OA1, 2, 4, 5, 8, 11, 12, 15, 17, 18, 21, 22, 24, and 25 lamps.	Not lit	_____
5.169	MLDD	Observe COMMAND PARITY BIT-SYL 0 lamp (DATA area).	Lit	_____
5.170	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
EXP.	NA	Steps 5.171 through 5.193 demonstrate that an address in the central processor memory can be correctly loaded and verified and that the repeat feature of the memory loader is functioning properly.		
5.171	MLDD	Press and release DS4, DS3, DS2, DS1, OP4, OP2, OP1, SIGN, and 1 through 25 pushbutton/lamps.		
5.172	MLDD	Observe COMMAND-DS4, DS3, DS2, DS1, OP4, OP2, OP1, SIGN, and 1 through 25 lamps.	Lit	_____
5.173	MLDD	Observe COMMAND PARITY BIT-SYL 0 and SYL 1 lamps (DATA area).	Not lit	_____
5.174	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	_____
5.175	MLDD	Press and release REPEAT/REPEAT pushbutton/lamp.		
5.176	MLDD	Observe REPEAT lamp.	Lit	_____
5.177	MLDD	Observe REPEAT lamp.	Not lit	_____

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Figure 7-7. Memory Loader Manual Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
5.178	MLDD	Observe COMPUTER-DS4, DS3, DS2, DS1, OP4, OP2, OP1, SIGN, and 1 through 25 lamps.	Lit	_____
5.179	MLDD	Observe that COMPUTER-OP3 lamp is lit dimly.		
5.180	MLDD	Observe COMMAND OP3 lamp.	Lit(dimly)	_____
5.181	MLDD	Observe COMPUTER PARITY BIT-BR SYL 0 lamp (DATA area).	Not lit	_____
5.182	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
5.183	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	_____
5.184	MLDD	Observe PARITY, TAPE, and COMPARE lamps.	Not lit	_____
5.185	MLDD	Press and release REPEAT/REPEAT pushbutton, lamp.		
5.186	MLDD	Observe REPEAT lamp.	Not lit	_____
5.187	MLDD	Observe REPEAT lamp.	Lit	_____
5.188	MLDD	Observe COMMAND-OP3 lamp (press and release if not lit).	Lit	_____
5.189	MLDD	Press and release ADDRESS COMPTR pushbutton.		
5.190	MLDD	Observe COMPUTER-DS4, DS3, DS2, DS1, OP4, OP3, OP2, OP1, SIGN, and 1 through 25 lamps.	Lit	_____
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Figure 7-7. Memory Loader Manual Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME:		UNIT NO.		
Step	Panel	Operation	Normal Indication	Data
5.191	MLDD	Press and release COMPUTER DISPLAY RESET pushbuttons.		
5.192	MLDD	Observe COMPUTER DS4, DS3, DS2, DS1, OP4, OP3, OP2, OP1, and 1 through 25 lamps.	Not lit	_____
5.193	MLDD	Observe COMPUTER PARITY BIT-BR SYL 1 lamp (DATA area).	Not lit	_____
EXP.	NA	Steps 5.194 through 5.223 demonstrate that different tape addresses can be manually loaded into the tape reader register and acted upon correctly.		
5.194	TRMC	Press and release $2^{11}/2^{10}/ADR\ 4/2^9$ pushbutton/lamp.		
5.195	TRMC	Observe ADR 4 lamp.	Lit	_____
5.196	MLDD	Observe INVERT ERROR pushbutton/lamp.	Lit	_____
5.197	TRMC	Press and release SELF CHECK pushbutton/lamp.		
5.198	TRMC	Observe SELF CHECK lamp.	Not lit	_____
5.199	MLDD	Observe INVERT ERROR lamp.	Not lit	_____
5.200	TRMC	Press and release SELF CHECK pushbutton/lamp.		
5.201	TRMC	Observe SELF CHECK lamp.	Lit	_____
5.202	TPMC	Press and release $2^{11}/2^{10}/ADR\ 4/2^9$ pushbutton/lamp twice.		
5.203	MLDD	Observe INVERT ERROR lamp.	Lit	_____

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Figure 7-7. Memory Loader Manual Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
5.204	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR 4/2 ⁹ pushbutton/lamp.		
5.205	TRMC	Observe ADR 4 lamp.	Not lit	_____
5.206	MLDD	Observe INVERT ERROR lamp.	Lit	_____
5.207	TRMC	Press and release 2 ⁸ /2 ⁷ /ADR 3/2 ⁶ pushbutton/lamp.		
5.208	TRMC	Observe ADR 3 lamp.	Lit	_____
5.209	MLDD	Observe INVERT ERROR lamp.	Lit	_____
5.210	TRMC	Press and release 2 ⁵ /2 ⁴ /ADR 2/2 ³ pushbutton/lamp.		
5.211	TRMC	Observe ADR 2 lamp.	Lit	_____
5.212	MLDD	Observe INVERT ERROR lamp.	Lit	_____
5.213	TRMC	Press and release 2 ² /2 ¹ /ADR 1/2 ⁰ pushbutton/lamp.		
5.214	TRMC	Observe ADR 1 lamp.	Lit	_____
5.215	MLDD	Observe INVERT ERROR lamp.	Not lit	_____
5.216	TRMC	Press and release 2 ¹² /ADR 5 pushbutton/lamp.		
5.217	TRMC	Observe ADR 5 lamp.	Lit	_____
5.218	TRMC	Press and release 2 ⁸ /2 ⁷ /ADR 3/2 ⁶ pushbutton/lamp.		
5.219	TRMC	Observe ADR 3 lamp.	Not lit	_____
5.220	TRMC	Press and release 2 ² /2 ¹ /ADR 1/2 ⁰ pushbutton/lamp.		
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Figure 7-7. Memory Loader Manual Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
EXP	NA	Steps 6.1 through 6.11 substantiate that pushbutton/lamps and switches which affect the data display are in the correct configuration.		
6.1	TRMC	Observe AUTO lamp (press and release if lit).	Not lit	
6.2	TRMC	Observe MANUAL lamp.	Lit	
6.3	PD	Verify that PROG REG A-SIGN and 1 through 25 toggle switches are off (down).		
6.4	TRMC	Observe FREE RUN SS lamp (press and release if lit).	Not lit	
6.5	TRMC	Observe SELF CHECK lamp (press and release if not lit).	Lit	
6.6	MLDD	Verify that DISPLAY SELECT switch is set to TRS.		
6.7	MLDD	Verify that MODE CONTROL switch is set to DISPLAY-REPEAT.		
6.8	PD	Press and release RESET-MACHINE pushbutton/lamp.		
6.9	PD	Observe MAN CST lamp (press and release if lit).	Not lit	
6.10	TRMC	Observe ML lamp (press and release if lit).	Not lit	
6.11	TRMC	Observe DD lamp.	Lit	

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Figure 7-8. Data Display Checks (Sheet 1 of 15)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.20	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Not lit	
6.21	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.22	MLDD	Press and release MODULE-0/1, SYL- 0/1, IS4, IS3, IS2, IS1, and A8 pushbutton/lamps.		
6.23	MLDD	Observe COMMAND and COMPUTER MODULE-1, SYL-1, IS4, IS3, IS2, IS1, and A8 lamps.	Not lit	
6.24	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Lit	
6.25	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.26	MLDD	Press and release A1 through A7 pushbutton/lamps.		
6.27	MLDD	Observe COMMAND and COMPUTER- A1 through A7 lamps.	Lit	
6.28	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.29	MLDD	Press and release A1 through A7 pushbutton/lamps.		
6.30	MLDD	Observe COMMAND and COMPUTER- A1 through A7 lamps.	Not lit	
6.31	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	

Figure 7-8. Data Display Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME:		UNIT NO.		
Step	Panel	Operation	Normal Indication	Data
6.32	MLDD	Press and release MODULE-0/1, IS4, IS2, A8, A6, A4, and A2 pushbutton/lamps.		
6.33	MLDD	Observe COMMAND and COMPUTER MODULE-1, IS4, IS2, A8, A6, A4, and A2 lamps.	Lit	
6.34	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Not lit	
6.35	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.36	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.37	MLDD	Observe COMMAND and COMPUTER MODULE-1, IS4, IS2, A8, A6, A4, and A2 lamps.	Not lit	
6.38	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Lit	
6.39	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.40	MLDD	Press and release SYL-0/1, IS3, IS1, A7, A5, A3, and A1 pushbutton/lamps.		
6.41	MLDD	Observe COMMAND and COMPUTER SYL-1, IS3, IS1, A7, A5, A3, and A1 lamps.	Lit	
6.42	MLDD	Observe COMMAND and COMPUTER SYL-0 lamps.	Not lit	
6.43	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	

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Figure 7-8. Data Display Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
6.44	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.75	MLDD	Observe COMMAND and COMPUTER SYL-1, IS3, IS1, A7, A5, A3 and A1 lamps.	Not lit	
6.76	MLDD	Observe COMMAND and COMPUTER SYL-0 lamps.	Lit	
6.47	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.48	MLDD	Press and release MODULE-0/1, SYL-0/1, IS4, IS3, A3, A2, and A1 pushbutton/lamps.		
6.49	MLDD	Observe COMMAND and COMPUTER MODULE-1, SYL-1, IS4, IS3, A3, A2, and A1 lamps.	Lit	
6.50	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Not lit	
6.51	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.52	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.53	MLDD	Observe COMMAND and COMPUTER MODULE-1, SYL-1, IS4, IS3, A3, A2, and A1 lamps.	Not lit	
6.54	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Lit	
6.55	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	

Figure 7-8. Data Display Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.56	MLDD	Press and release IS2, IS1, and A4 through A8 pushbutton/lamps.		
6.57	MLDD	Observe COMMAND and COMPUTER IS2, IS1, and A4 through A8 lamps.	Lit	
6.58	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.59	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.60	MLDD	Observe COMMAND and COMPUTER IS2, IS1, and A4 through A8 lamps.	Not lit	
6.61	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.62	MLDD	Press and release MODULE-0/1, SYL-0/1, IS2, IS1, A7, A6, and A3 pushbutton/lamps.		
6.63	MLDD	Observe COMMAND and COMPUTER MODULE-1, SYL-1, IS2, IS1, A7, A6, and A3 lamps.	Lit	
6.64	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Not lit	
6.65	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.66	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.67	MLDD	Observe COMMAND and COMPUTER MODULE-1, SYL-1, IS2, IS1, A7, A6, and A3 lamps.	Not lit	

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Figure 7-8. Data Display Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6. 68	MLDD	Observe COMMAND and COMPUTER MODULE-0 and SYL-0 lamps.	Lit	
6. 69	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6. 70	MLDD	Press and release IS4, IS3, A8, A5, A4, A2, and A1 pushbutton/lamps.		
6. 71	MLDD	Observe COMMAND and COMPUTER-IS4, IS3, A8, A5, A4, A2 and A1 lamps.	Lit	
6. 72	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
EXP	NA	Steps 6. 73 through 6. 131 demonstrate that different combinations of data addresses can be manually loaded into the tape reader register, compared on correctly, and displayed. Ignore COMMAND and COMPUTER lamps not located in DATA ADDRESS area.		
6. 73	MLDD	Press and release ADDRESS COMPARE-DATA/INS pushbutton/lamp.		
6. 74	MLDD	Observe ADDRESS COMPARE-DATA lamp.	Lit	
6. 75	MLDD	Observe ADDRESS COMPARE-INS lamp.	Not lit	
6. 76	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6. 77	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Lit	
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Figure 7-8. Data Display Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6. 89	MLDD	Observer COMMAND and COMPUTER-OA1 through OA7 pushbutton/lamps.	Lit	
6. 89. 1	MLDD	Observe PARITY BIT-BR lamp.	Not lit	
6. 90	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6. 91	MLDD	Press and release OA1 through OA7 pushbutton/lamps.		
6. 92	MLDD	Observe COMMAND and COMPUTER-OA1 through OA7 lamps.	Not lit	
6. 93	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6. 94	MLDD	Press and release DS4, DS2, MODULE-0/1, OA8, OA6, OA4, and OA2 pushbutton/lamps.		
6. 95	MLDD	Observe COMMAND and COMPUTER-DS4, DS2, MODULE-1, OA8, OA6, OA4, and OA2 lamps.	Lit	
6. 96	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Not lit	
6. 96. 1	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6. 97	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6. 98	MLDD	Observe COMMAND and COMPUTER-DS4, DS2, MODULE-1, OA8, OA6, OA4, and OA2 lamps.	Not lit	
6. 99	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Lit	
6. 100	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	

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Figure 7-8. Data Display Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.101	MLDD	Press and release DS3, DS1, OA9, OA7, OA5, OA3. and OA1 pushbutton/lamps.		
6.102	MLDD	Observe COMMAND and COMPUTER-DS3, DS1, OA9, OA7, OA5, OA3, and OA1 lamps.	Lit	
6.103	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.104	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.105	MLDD	Observe COMMAND and COMPUTER-DS3, DS1, OA9, OA7, OA5, OA3, and OA1 lamps.	Not lit	
6.106	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.107	MLDD	Press and release DS1 through DS4 and OA1 through OA3 pushbutton/lamps.		
6.108	MLDD	Observe COMMAND and COMPUTER-DS1 through DS4 and OA1 through OA3 pushbutton/lamps.	Lit	
6.109	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.110	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.111	MLDD	Observe COMMAND and COMPUTER-DS1 through DS4 and OA1 through OA3 lamps.	Not lit	

Figure 7-8. Data Display Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES--				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.112	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.113	MLDD	Press and release MODULE-0/1 and OA4 through OA9 pushbutton/lamps.		
6.114	MLDD	Observe COMMAND and COMPUTER MODULE-1 and OA4 through OA9 lamps.	Lit	
6.115	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamp.	Not lit	
6.116	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.117	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.118	MLDD	Observe COMMAND and COMPUTER MODULE-1 and OA4 through OA9 lamps.	Not lit	
6.119	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Lit	
6.120	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.121	MLDD	Press and release DS4, DS3, MODULE-0/1, OA9, OA7, OA6, and OA3 pushbutton/lamps.		
6.122	MLDD	Observe COMMAND and COMPUTER DS4, DS3, MODULE-1, OA9, OA7, OA6, and OA3 lamps.	Lit	

Figure 7-8. Data Display Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.123	MLDD	Observe COMMAND and COMPUTER MODULE-0 lamps.	Not lit	
6.123	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.125	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.		
6.126	MLDD	Observe COMMAND and COMPUTER-DS4, DS3, MODULE-1, OA9, OA7, OA6, and OA3 lamps.	Not lit	
6.127	MLDD	Observe COMMAND and COMPUTER-MODULE-0 lamps.	Lit	
6.128	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.129	MLDD	Press and release DS2, DS1, OA8, OA5, OA4, OA2, and OA1 pushbutton/lamps.		
6.130	MLDD	Observe COMMAND and COMPUTER DS2, DS1, OA8, OA5, OA4, OA2, and OA1 lamps.	Lit	
6.131	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
EXP	NA	Steps 6.122 through 6.142 demonstrate that the DISPLAY-SINGLE and DISPLAY-REPEAT features of the data display are functioning properly.		
6.132	MLDD	Set MODE CONTROL switch to DISPLAY-SINGLE.		

Figure 7-8. Data Display Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.133	MLDD	Press and release COMMAND DISPLAY RESET pushbutton/lamp.		
6.134	MLDD	Observe COMMAND-DS2, DS1, OA8, OA5, OA4, OA2, and OA1 lamps.	Not lit	
6.135	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Lit	
6.136	MLDD	Press and release OA4, OA3, OA2, and COMPTR DISPLAY RESET pushbutton/lamps in succession.		
6.137	MLDD	Observe COMMAND-OA4, OA3, and OA2 lamps.	Lit	
6.138	MLDD	Observe SERIALIZER-PARITY BIT lamp.	Not lit	
6.139	MLDD	Set PROG REG A-1 toggle switch to on (up).		
6.140	MLDD	Observe COMPUTER-OP4, OP3, OP2, OP1, OA4, OA3, OA2, and 25 lamps.	Lit	
6.141	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.		
6.142	MLDD	Observe that DATA area COMPUTER lamps indicate an advancing binary count.		
EXP	NA	Steps 6.143 through 6.163 demonstrate that the central processor can be placed in PROG CYCLE-ADR HOLD, SINGLE STEP, and REPEAT modes of operation by a data display address compare.		

Figure 7-8. Data Display Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.143	MLDD	Set DISPLAY SELECT switch to A13-DATA.		
6.144	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.		
6.145	MLDD	Observe that binary count indicated on DATA area COMPUTER lamps stops advancing.		
6.146	PD	Press and release ADVANCE pushbutton several times.		
6.147	MLDD	Observe that binary count indicated on DATA area COMPUTER lamps advances every second time the ADVANCE pushbutton/lamp is actuated.		
6.148	MLDD	Press and release ADDRESS COMPARE-DATA/INS pushbutton/lamp.		
6.149	MLDD	Observe ADDRESS COMPARE-DATA lamp.	Not lit	
6.150	MLDD	Observe ADDRESS COMPARE-INS lamp.	Lit	
6.151	MLDD	Press and release A5, A4, A3, and A1 pushbutton/lamps.		
6.152	MLDD	Set MODE CONTROL switch to PROG CYCLE-REPEAT.		
6.153	PD	Press and release RESET-MACHINE pushbutton.		

Figure 7-8. Data Display Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
6.154	MLDD	Observe that DATA area COMPUTER lamps indicate an advancing binary count.		
6.155	MLDD	Press and release A1 pushbutton/lamp.		
6.156	MLDD	Observe that binary count indicated on DATA area COMPUTER lamps stops advancing.		
6.157	MLDD	Press and release COMMAND DISPLAY RESET pushbutton.		
6.158	MLDD	Set DISPLAY SELECT switch to AI3-IA and MODE CONTROL switch to PROG CYCLE-SINGLE STEP.		
6.159	MLDD	Observe COMPUTER-8 lamp.	Lit	
6.160	MLDD	Observe COMPUTER-A1 through A8 and 1 through 7 lamps.	Not lit	
6.161	MLDD	Press and release ADVANCE pushbutton.		
6.162	MLDD	Observe COMPUTER-A1 and 7 lamps.	Lit	
6.163	MLDD	Observe COMPUTER-A2 through A8, 1 through 6, and 8 lamp.	Not lit	

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Figure 7-8. Data Display Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation								Normal Indication	Data									
EXP	NA	Steps 7.1 through 7.12 substantiate that pushbutton/lamps and switches which affect central processor operation are in the correct configuration.																		
7.1	TRMC	Observe AUTO lamp (press and release if lit).								Not lit										
7.2	TRMC	Observe MANUAL lamp.								Lit										
7.3	PD	Verify that PROG REG A- SIGN and 125 toggle switches are off (down).																		
7.4	TRMC	Observe FREE RUN SS lamp (press and release if lit).								Not lit										
7.5	TRMC	Observe SELF CHECK lamp (press and release if not lit).								Lit										
7.6	TRMC	Observe ML lamp (press and release if lit).								Not lit										
7.7	TRMC	Observe DD lamp.								Lit										
7.8	PD	Observe MAN CST lamp (press and release if lit).																		
7.9	MLDD	Observe ADDRESS COMPARE-DATA lamp (press and release if lit).								Not lit										
7.10	MLDD	Observe ADDRESS COMPARE-INS lamp.								Lit										
7.11	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.																		
7.12	MLDD	Press and release COMMAND DISPLAY RESET pushbuttons.																		
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Figure 7-9. Central Processor Manual Checks (Sheet 1 of 56)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
EXP	NA	Steps 7.13 through 7.87 demonstrate that the single instruction advance feature is functioning properly and that the MEMORY ADDRESS SYLLABLE, SECTOR, IM, and DM lamps on PD panel display correct information.											
7.13	MLDD	Press and release A5 and A4 push-button/lamps.											
7.14	MLDD	Observe COMMAND-A5 and A4 lamps.								Lit			
7.15	PD	Press and release RESET-MACHINE pushbuttons.											
7.16	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A5 and A4 lamps.								Lit			
7.17	PD	Observe HOPSAVE REG lamp (press and release if lit).								Not lit			
7.18	PD	Observe MEM ADD REG lamp (press and release if not lit).								Lit			
7.19	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.											
7.20	CE	Press and release ADVANCE push-buttons.											
7.21	PD	Observe A5, A4, A1, SYLLABLE-0, IM0, and DM0 lamps.								Lit			
7.22	PD	Observe A2, A3, A6 through A9, SYLLABLE-1, IS1 through IS4, DS1 through DS4, IM1, and DM1 lamps.								Not lit			
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Figure 7-9. Central Processor Manual Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—															
UNIT NAME:												UNIT NO.			
Step	Panel	Operation										Normal Indication	Data		
7.23	PD	Press and release ADVANCE push-buttons.													
7.24	PD	Observe A1 through A7, SYLLABLE-0, DS2, DS1, IM0, and DM0 lamps.										Lit			
7.25	PD	Observe A9, A8, SYLLABLE-1, IS1 through IS4, DS4, DS3, IM1, and DM1 lamps.										Not lit			
7.26	PD	Press and release MEM ADD REG pushbutton/lamp.													
7.27.	PD	Observe A1 through A7, SYLLABLE-0, DS2, DS1, IM0, DM0, and MEM ADD REG lamps.										Not lit			
7.28	PD	Press and release HOPSAVE REG pushbutton/lamp.													
7.29	PD	Observe A5, A4, A2, SYLLABLE-0, IM0, DM0, and HOPSAVE REG lamps.										Lit			
7.30	PD	Observe A6 through A9, A3, A1, SYLLABLE-1, IS1 through IS4, DS1 through DS4, IM1, and DM1 lamps.										Not lit			
7.31	PD	Press and release ADVANCE push-buttons.													
7.32	PD	Observe A8, SYLLABLE-0, DS2, DS1, IM0, and DM0 lamps.										Lit			
7.33	PD	Observe A1 through A7, A9, IS1 through IS4, DS4, DS3, IM1, and DM1 lamps.										Not lit			

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Figure 7-9. Central Processor Manual Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation						Normal Indication	Data			
7.34	PD	Press and release MEM ADD REG pushbutton/lamp.										
7.35	PD	Observe A8, SYLLABLE-0, DS2, DS1, IM0, and DM0.						Not lit				
7.36	PD	Press and release HOP SAVE REG pushbutton/lamp.										
7.37	PD	Observe A4 through A8, SYLLABLE-0, IS2, IS1, DS3, DS1, IM0, DM0, and MEM ADD REG lamps.						Lit				
7.38	PD	Observe A1 through A3, SYLLABLE-1, IS4, IS3, DS4, DS2, IM1, and DM1 lamps.						Not lit				
7.39	PD	Press and release ADVANCE push-buttons.										
7.40	PD	Observe A7, A5, A3, A1, SYLLABLE-1, IS3, IS1, DS1 through DS4, IM0, and DM0 lamps.						Lit				
7.41	PD	Observe A9, A8, A6, A4, A2, SYLLABLE-0, IS4, IS2, IM1, and DM1 lamps.						Not lit				
7.42	PD	Press and release MEM ADD REG pushbutton/lamp.										
7.43	PD	Press and release HOPSAVE REG pushbutton/lamp.										
7.44	PD	Observe A1, A4 through A8, SYLLABLE-0, IS2, IS1, DS3, DS1, IM0, DM0, and HOPSAVE REG lamps.						Lit				

Figure 7-9. Central Processor Manual Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation										Normal Indication	Data
7.45	PD	Observe A9, A3, A2, A1, SYLLABLE-1, IS4, IS3, DS4, DS2, IM1, and DM1 lamps.										Not lit	
7.46	PD	Press and release ADVANCE push-buttons.											
7.47	PD	Observe A7, A5, A3, A2, SYLLABLE-1, IS3, IS1, DS1 through DS4, IM0, and DM0 lamps.										Lit	
7.48	PD	Observe A9, A8, A6, A4, A1, SYLLABLE-0, IS4, IS2, IM1, and DM1 lamps.										Not lit	
7.49	PD	Press and release HOPSAVE REG pushbutton/lamps.											
7.50	PD	Press and release MEM ADD REG pushbutton/lamp.											
7.51	PD	Observe A8, A5, A4, A2, A1, SYLLABLE-0, IS4, IS3, IM0, DM1, and MEM ADD REG lamps.										Lit	
7.52	PD	Observe A9, A7, A6, A3, SYLLABLE-1, IS2, IS1, DS1 through DS4, IM1, and DM0 lamps.										Not lit	
7.53	PD	Press and release ADVANCE push-buttons.											
7.54	PD	Observe A7, A6, A3, SYLLABLE-1, IS2, IS1, DS4, DS2, IM1, and DM1 lamps.										Lit	
7.55	PD	Observe A9, A8, A5, A4, A2, A1, SYLLABLE-0, IS4, IS3, DS3, DS1, IM0, and DM0 lamps.										Not lit	
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Figure 7-9. Central Processor Manual Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation						Normal Indication	Data												
7.56	PD	Press and release MEM ADD REG pushbutton/lamp.																			
7.57	PD	Press and release HOPSAVE REG pushbutton/lamp.																			
7.58	PD	Observe A8, A5, A4, A3, SYLLABLE-0, IS4, IS3, IM0, DM1, and HOPSAVE REG lamps.						Lit													
7.59	PD	Observe A9, A7, A6, A2, A1, SYLLABLE-1, IS2, IS1, DS1 through DS4, IM1, and DM0 lamps.						Not lit													
7.60	PD	Press and release ADVANCE push-buttons.																			
7.61	PD	Observe A7, A6, A3, A1, SYLLABLE-1, IS2, IS1, DS4, DS2, IM1, and DM1 lamps.						Lit													
7.62	PD	Observe A9, A8, A5, A4, A2, A1, SYLLABLE-1, IS2, IS1, DS4, DS2, IM0, and DM0 lamps.						Not lit													
7.63	PD	Press and release HOPSAVE REG pushbutton/lamp.																			
7.64	PD	Press and release MEM ADD REG pushbutton/lamp.																			
7.65	PD	Observe A7, A6, A3, A1, SYLLABLE-1, IS2, IS1, DS4, DS2, IM1, DM1, and MEM ADD REG lamps.						Lit													
7.66	PD	Observe A9, A8, A5, A4, A2, SYLLABLE-0, IS2, IS1, DS4, DS2, IM0, and DM0 lamps.						Not lit													
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Figure 7-9. Central Processor Manual Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-																
UNIT NAME:													UNIT NO.			
Step	Panel	Operation										Normal Indication	Data			
7.67	PD	Press and release ADVANCE push-buttons.														
7.68	PD	Observe A8, A6, A4, A2, SYLLABLE-0, IS4, IS2, DS4, DS3, IM1, and DM0 lamps.										Lit				
7.69	PD	Observe A9, A7, A5, A3, A1, SYLLABLE-1, IS3, IS1, DS2, DS1, IM0, and IM1 lamps.										Not lit				
7.70	PD	Press and release MEM ADD REG pushbutton/lamp.														
7.71	PD	Press and release HOPSAVE REG pushbutton/lamp.														
7.72	PD	Observe A7, A6, A3, A2, SYLLABLE-1, IS2, IS1, DS4, DS2, IM1, DM1, and HOPSAVE REG lamps.										Lit				
7.73	PD	Observe A9, A8, A5, A4, A1, SYLLABLE-0, IS4, IS3, DS3, DS1, IM0, and DM0 lamps.										Not lit				
7.74	PD	Press and release ADVANCE push-buttons.														
7.75	PD	Observe A8, A6, A4, A2, A1, SYLLABLE-0, IS4, IS2, DS4, DS3, IM1, and DM1 lamps.										Lit				
7.76	PD	Observe A9, A7, A5, A3, SYLLABLE-1, IS3, IS1, DS2, DS1, IM0, and DM0 lamps.										Not lit				
7.77	PD	Press and release HOPSAVE REG pushbutton/lamp.														

Figure 7-9. Central Processor Manual Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:							UNIT NO.													
Step	Panel	Operation				Normal Indication	Data													
7.78	PD	Press and release MEM ADD REG pushbutton/lamp.																		
7.79	PD	Observe A3, A2, A1, SYLLABLE-1, IS3, IS4, DS1 through DS4, DM1 and MEM ADD REG lamps.				Lit														
7.80	PD	Observe A4 through A9, SYLLABLE-0, IS1, IS2, IM1, and DM0 lamps.				Not lit														
7.81	PD	Press and release ADVANCE pushbutton/lamp.																		
7.82	PD	Observe A8, SYLLABLE-1, IS1 through IS4, IM1, and DM0 lamps.				Lit														
7.83	PD	Observe A9, A1 through A7, SYLLABLE-0, DS1 through DS4, IM0, and DM1 lamps.				Not lit														
7.84	PD	Press and release MEM ADD REG pushbutton/lamp.																		
7.85	PD	Press and release HOPSAVE REG pushbutton/lamp.																		
7.86	PD	Observe A4, SYLLABLE-1, IS4, IS3, DS1 through DS4, IM1, DM1, and HOPSAVE REG lamps.				Lit														
7.87	PD	Observe A5 through A9, A3, A2, A1, SYLLABLE-0, IS2, IS1, IM0, and DM0 lamps.				Not lit														
EXP	NA	Steps 7.88 through 7.158 demonstrate that the single phase advance feature is functioning properly and that the ACCUMULATOR and MEMORY BUFFER, REGISTER lamps on CE panel display correct information.																		
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Figure 7-9. Central Processor Manual Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-															
UNIT NAME:												UNIT NO.			
Step	Panel	Operation										Normal Indication	Data		
7.88	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE PHASE.													
7.89	CE	Observe ACC DISPLAY ENABLE lamp (press and release if not lit).										Lit			
7.90	CE	Observe MEM BUFFER REG lamp (press and release if not lit).										Lit			
7.91	PD	Observe TRANS REC lamp (press and release if lit).										Not lit			
7.92	CE	Press and release ADVANCE push-button/lamp.													
7.93	CE	Observe BIT 14 lamp.										Lit			
7.94	CE	Observe BIT 1 through BIT 13 lamps.										Not lit			
7.95	PD	Observe DATA-1 through 13 lamps.										Not lit			
7.96	CE	Press and release ADVANCE push-button/lamp.													
7.97	CE	Observe BIT 1 through BIT 13 lamps.										Lit			
7.98	CE	Observe BIT 14 lamp.										Not lit			
7.99	CE	Press and release ADVANCE push-button/lamp twice.													
7.100	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 1 of Table 1.													

Figure 7-9. Central Processor Manual Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-																							
UNIT NAME:											UNIT NO.												
Step	Panel	Operation	Normal Indication	Data																			
7.101	PD	Observe that the status of the DATA lamps is as shown for test 1 of Table 1.																					
7.102	CE	Press and release ADVANCE push-button.																					
7.103	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 2 of Table 1.																					
7.104	PD	Observe that the status of the DATA lamps is as shown for test 2 of Table 1.																					
7.105	CE	Press and release ADVANCE push-button twice.																					
7.106	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 3 of Table 1.																					
7.107	PD	Observe that the status of the DATA lamps is as shown for test 3 of Table 1.																					
7.108	CE	Press and release ADVANCE push-button.																					
7.109	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 4 of Table 1.																					
7.110	PD	Observe that the status of the DATA lamps is as shown for test 4 of Table 1.																					
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Figure 7-9. Central Processor Manual Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
7.111	CE	Press and release ADVANCE push-button twice.										
7.112	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 5 of Table 1.										
7.113	PD	Observe that the status of the DATA lamps is as shown for test 5 of Table 1.										
7.114	CE	Press and release ADVANCE push-button.										
7.115	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 6 of Table 1.										
7.116	PD	Observe that the status of the DATA lamps is as shown for test 6 of Table 1.										
7.117	CE	Press and release ADVANCE push-button twice.										
7.118	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 7 of Table 1.										
7.119	PD	Observe that the status of the DATA lamps is as shown for test 7 of Table 1.										
7.120	CE	Press and release ADVANCE push-button.										
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Figure 7-9. Central Processor Manual Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:									UNIT NO.	
Step	Panel	Operation						Normal Indication	Data	
7.121	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 8 of Table 1.								
7.122	PD	Observe that the status of the DATA lamps is as shown for test 8 of Table 1.								
7.123	CE	Press and release ADVANCE push-button twice.								
7.124	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 9 of Table 1.								
7.125	PD	Observe that the status of the DATA lamps is as shown for test 9 of Table 1.								
7.126	CE	Press and release ADVANCE push-button.								
7.127	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 10 of Table 1.								
7.128	PD	Observe that the status of the DATA lamps is as shown for test 10 of Table 1.								
7.129	CE	Press and release ADVANCE push-button twice.								

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Figure 7-9. Central Processor Manual Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
7.130	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 11 of Table 1.										
7.131	PD	Observe that the status of the DATA lamps is as shown for test 11 of Table 1.										
7.132	CE	Press and release ADVANCE push-button.										
7.133	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 12 of Table 1.										
7.134	PD	Observe that the status of the DATA lamps is as shown for test 12 of Table 1.										
7.135	CE	Press and release ADVANCE push-button twice.										
7.136	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 13 of Table 1.										
7.137	PD	Observe that the status of the DATA lamps is as shown for test 13 of Table 1.										
7.138	CE	Press and release ADVANCE push-button.										
7.139	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 14 of Table 1.										
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Figure 7-9. Central Processor Manual Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
7.140	PD	Observe that the status of the DATA lamps is as shown for test 14 of Table 1.										
7.141	CE	Press and release ADVANCE push-button twice.										
7.142	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 15 of Table 1.										
7.143	PD	Observe that the status of the DATA lamps is as shown for test 15 of Table 1.										
7.144	CE	Press and release ADVANCE push-button.										
7.145	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 16 of Table 1.										
7.146	PD	Observe that the status of the DATA lamps is as shown for test 16 of Table 1.										
7.147	CE	Press and release ADVANCE push-button twice.										
7.148	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 17 of Table 1.										
7.149	PD	Observe that the status of the DATA lamps is as shown for test 17 of Table 1.										
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Figure 7-9. Central Processor Manual Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
7.150	CE	Press and release ADVANCE push-button.																			
7.151	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 18 of Table 1.																			
7.152	PD	Observe that the status of the DATA lamps is as shown for test 18 of Table 1.																			
7.153	CE	Press and release ADVANCE push-button twice.																			
7.154	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 19 of Table 1.																			
7.155	PD	Observe that the status of the DATA lamps is as shown for test 19 of Table 1.																			
7.156	CE	Press and release ADVANCE push-button.																			
7.157	CE	Observe that the status of the ACCUMULATOR and MEMORY BUFFER REGISTER lamps is as shown for test 20 of Table 1.																			
7.158	PD	Observe that the status of the DATA lamps is as shown for test 20 of Table 1.																			
EXP	NA	Steps 7.159 through 7.207 substantiate that the PHASE and BIT GATE lamps on CE panel display correct information and that the single bit advance feature is functioning properly.																			
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Figure 7-9. Central Processor Manual Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
7.159	CE	Observe TIMING DISPLAY ENABLE lamp (press and release if not lit).								Lit			
7.160	CE	Press and release ADVANCE push-button.											
7.161	CE	Observe PHASE-A and BG10 lamps.								Lit			
7.162	CE	Observe PHASE-B and C, BG1 through BG9, and BG11 through BG14 lamps.								Not lit			
7.163	CE	Press and release ADVANCE push-button/lamp.											
7.164	CE	Observe PHASE-B and BG2 lamps.								Lit			
7.165	CE	Observe PHASE-A and B, BG1, and BG2 through BG14 lamps.								Not lit			
7.166	CE	Press and release ADVANCE push-button/lamp.											
7.167	CE	Observe PHASE-C and BG1 lamps.								Lit			
7.168	CE	Observe PHASE-A and B and BG2 through BG14 lamps.								Not lit			
7.169	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE BIT.											
7.170	CE	Press and release ADVANCE push-button/lamp.											
7.171	CE	Observe BG2 lamp.								Lit			
7.172	CE	Observe BG1 and BG3 through BG14 lamps.								Not lit			

Figure 7-9. Central Processor Manual Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
7.173	CE	Press and release ADVANCE push-button/lamp.											
7.174	CE	Observe BG3 lamp.								Lit			
7.175	CE	Observe BG1, BG2, and BG4 through BG14 lamps.								Not lit			
7.176	CE	Press and release ADVANCE push-button/lamp.											
7.177	CE	Observe BG4 lamp.								Lit			
7.178	CE	Observe BG1, BG2, BG3, and BG5 through BG14 lamps.								Not lit			
7.179	CE	Press and release ADVANCE push-button/lamp.											
7.180	CE	Observe BG5 lamp.								Lit			
7.181	CE	Observe BG1 through BG4 and BG6 through BG14 lamps.								Not lit			
7.182	CE	Press and release ADVANCE push-button/lamp.											
7.183	CE	Observe BG6 lamp.								Lit			
7.184	CE	Observe BG1 through BG5 and BG7 through BG14 lamps.								Not lit			
7.185	CE	Press and release ADVANCE push-button/lamp.											
7.186	CE	Observe BG7 lamp.								Lit			
7.187	CE	Press and release ADVANCE push-button/lamp.											

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Figure 7-9. Central Processor Manual Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
7.188	CE	Observe BG8 lamp.								Lit			
7.189	CE	Observe BG1 through BG7 and BG9 through BG14 lamps.								Not lit			
7.190	CE	Press and release ADVANCE push-button/lamp.											
7.191	CE	Observe BG9 lamp.								Lit			
7.192	CE	Observe BG1 through BG8 and BG10 through BG14 lamps.								Not lit			
7.193	CE	Press and release ADVANCE push-button/lamp.											
7.194	CE	Observe BG10 lamp.								Lit			
7.195	CE	Observe BG1 through BG9 and BG11 through BG14 lamps.								Not lit			
7.196	CE	Press and release ADVANCE push-button/lamp.											
7.197	CE	Observe BG11 lamp.								Lit			
7.198	CE	Observe BG1 through BG10, BG12, BG13, and BG14 lamps.								Not lit			
7.199	CE	Press and release ADVANCE push-button/lamp.											
7.200	CE	Observe BG12 lamp.								Lit			
7.201	CE	Observe BG1 through BG11, BG13, and BG14 lamps.								Not lit			
7.202	CE	Press and release ADVANCE push-button/lamp.											

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Figure 7-9. Central Processor Manual Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES—										
UNIT NAME:									UNIT NO.	
Step	Panel	Operation						Normal Indication	Data	
7.203	CE	Observe BG13 lamp.						Lit		
7.204	CE	Observe BG1 through BG12 and BG14 lamps.						Not lit		
7.205	CE	Press and release ADVANCE push-button/lamp.								
7.206	CE	Observe PHASE-C and BG14 lamps.						Lit		
7.207	CE	Observe PHASE-A and B and BG1 through BG13 lamps.						Not lit		
EXP	NA	Steps 7.208 through 7.246 demonstrate that the OP CODE lamps on PD panel display correct information.								
7.208	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.								
7.209	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.								
7.210	MLDD	Press and release MODULE-0/1, IS4, IS2, A8, A6, A4, and A2 pushbutton/lamps (INSTRUCTION ADDRESS area).								
7.211	PD	Press and release ADVANCE push-button/lamp.								
7.212	MLDD	Observe COMMAND and COMPUTER-MODULE-1, SYL-0, IS4, IS2, A8, A6, A4, and A2 lamps. (INSTRUCTION ADDRESS area.)						Lit		

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Figure 7-9. Central Processor Manual Checks (Sheet 20)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation							Normal Indication	Data											
7. 213	MLDD	Observe COMMAND and COMPUTER-MODULE-0, SYL-1, IS2, IS1, A7, A5, A3, and A1 lamps. (INSTRUCTION ADDRESS area.)							Not lit												
7. 214	MLDD	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.																			
7. 215	PD	Press and release ADVANCE push-button.																			
7. 216	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE PHASE.																			
7. 217	CE	Press and release ADVANCE push-button three times.																			
7. 218	PD	Observe OP1 through OP4 lamps.							Lit												
7. 219	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.																			
7. 220	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbuttons.																			
7. 221	MLDD	Press and release MODULE-0/1, SYL-0/1, IS4, IS3, IS2, IS1, A8 A4, and A3 pushbutton/lamps. (INSTRUCTION ADDRESS area.)																			
7. 222	CE	Press and release ADVANCE push-button.																			
7. 223	MLDD	Observe COMMAND and COMPUTER-MODULE-1, SYL-1, IS4, IS3, IS2, IS1, A8, A4, and A3 lamps. (INSTRUCTION ADDRESS area.)							Lit												
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Figure 7-9. Central Processor Manual Checks (Sheet 21)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation							Normal Indication	Data										
7.224	MLDD	Observe COMMAND and COMPUTER-MODULE-0, SYL-0, A7, A6, A5, A2, and A1 lamps. (INSTRUCTION ADDRESS area.)							Not lit											
7.225	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.																		
7.226	PD	Press and release ADVANCE push-buttons.																		
7.227	PD	Observe OP1 and OP3 lamps.							Lit											
7.228	PD	Observe OP2 and OP4 lamps.							Not lit											
7.229	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.																		
7.230	PD	Set PROG REG A- SIGN toggle switch to on (up).																		
7.231	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbutton.																		
7.232	MLDD	Press and release A6, A3, A2, and A1 pushbutton/lamps.																		
7.233	PD	Press and release ADVANCE push-buttons.																		
7.234	MLDD	Observe COMMAND and COMPUTER-MODULE-0, SYL-0, A6, A3, A2, and A1 lamps. (INSTRUCTION ADDRESS area.)							Lit											
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Figure 7-9. Central Processor Manual Checks (Sheet 22)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
7. 235	MLDD	Observe COMMAND and COMPUTER-MODULE-1, SYL-1, A6, A3, A2, and A1 lamps.				Not lit			
7. 236	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.							
7. 237	CE	Press and release ADVANCE push-button.							
7. 238	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE PHASE.							
7. 239	PD	Observe OP1 through OP3 lamps.				Lit			
7. 240	PD	Observe OP4 lamp.				Not lit			
7. 241	PD	Press and release ADVANCE push-button three times.							
7. 242	PD	Observe OP1, OP2, and OP4 lamps.				Lit			
7. 243	PD	Observe OP3 lamp.				Not lit			
7. 244	PD	Press and release ADVANCE push-button/lamp three times.							
7. 245	PD	Observe OP2 and OP3 lamps.				Lit			
7. 246	PD	Observe OP1 and OP4 lamps.				Not lit			
EXP	NA	Steps 7. 247 through 7. 323 substantiate that the manual machine reset and halt reset features are functioning properly.							

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Figure 7-9. Central Processor Manual Checks (Sheet 23)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:									UNIT NO.											
Step	Panel	Operation					Normal Indication	Data												
7.247	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.																		
7.247.1	TRMC	Press and release ML/DD push-button/lamp.																		
7.248	TRMC	Observe ML lamp.					Lit													
7.249	TRMC	Observe DD lamp.					Not lit													
7.250	MLDD	Set MODE control switch to DISPLAY-REPEAT.																		
7.251	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET pushbutton/lamp.																		
7.252	MLDD	Press and release OP4, OP2, OP1, OA4, OA3, OA2, and OA1 push-button/lamps.																		
7.253	PD	Press and release RESET-MACHINE pushbutton/lamp.																		
7.254	MLDD	Press and release REPEAT/ $\overline{\text{REPEAT}}$ pushbutton/lamp.																		
7.255	MLDD	Observe REPEAT lamp.					Lit													
7.256	MLDD	Observe $\overline{\text{REPEAT}}$ lamp.					Not lit													
7.257	MLDD	Observe COMMAND and COMPUTER-MODULE-0 OP4, OP3, OP2, OP1, OA4, OA3, OA2, and OA1 lamps (DATA ADDRESS area).					Lit													
7.258	MLDD	Observe COMMAND and COMPUTER-DS1 through DS4, MODULE-1, and OA5 through OA9 lamps. (DATA ADDRESS area.)					Not lit													
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Figure 7-9. Central Processor Manual Checks (Sheet 24)

INTERNATIONAL BUSINESS MACHINES--										
UNIT NAME:								UNIT NO.		
Step	Panel	Operation					Normal Indication	Data		
7.259	PD	Set PROG REG A- SIGN toggle switch to off.								
7.260	MLDD	Press and release REPEAT/ $\overline{\text{REPEAT}}$ pushbutton/lamp.								
7.261	MLDD	Observe REPEAT lamp.					Lit			
7.262	MLDD	Observe $\overline{\text{REPEAT}}$ lamp.					Not lit			
7.263	TRMC	Press and release ML/DD pushbutton/lamp.								
7.264	TRMC	Observe ML lamp.					Not lit			
7.265	TRMC	Observe DD lamp.					Lit			
7.266	MLDD	Verify that DISPLAY SELECT switch is set to AI3-DATA.								
7.267	MLDD	Press and release ADDRESS COMPARE-DATA/INS pushbutton/lamp.								
7.268	MLDD	Observe ADDRESS COMPARE-DATA lamp.					Lit			
7.269	MLDD	Observe ADDRESS COMPARE-INS lamp.					Not lit			
7.270	MLDD	Press and release OA4, OA3, and OA2 pushbutton/lamps.								
7.271	PD	Set PROG REG A- SIGN toggle switch to on.								
7.272	MLDD	Observe COMMAND and COMPUTER-MODULE-0, OA4, OA3, and OA2 lamps (DATA ADDRESS area).					Lit			

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Figure 7-9. Central Processor Manual Checks (Sheet 25)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
7.273	MLDD	Observe COMMAND and COMPUTER-DS4, DS3, DS2, DS1, MODULE-1, OA6 through OA9, and OA1 lamps. (DATA ADDRESS area.)								Not lit			
7.274	MLDD	Observe COMPUTER-25 lamp.								Lit			
7.275	MLDD	Observe COMPUTER-SIGN and 2 through 24 lamps.								Not lit			
7.276	PD	Observe that P40 lamp is flashing.											
7.277	PD	Press and release RESET-MACHINE pushbutton/lamp.											
7.278	MLDD	Observe COMPUTER-24 lamp.								Lit			
7.279	MLDD	Observe COMPUTER-SIGN, 1 through 23, and 25 lamps.								Not lit			
7.280	PD	Observe P40 lamp.								Flashing			
7.281	PD	Press and release RESET-MACHINE pushbutton/lamp.											
7.282	MLDD	Observe COMPUTER-24 and 25 lamps.								Lit			
7.283	MLDD	Observe COMPUTER-SIGN and 1 through 23 lamps.								Not lit			
7.284	PD	Observe P40 lamp.								Flashing			
7.285	PD	Press and hold RESET-HALT pushbutton/lamp.											
7.286	PD	Observe P40 lamp.								Not flashing			

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Figure 7-9. Central Processor Manual Checks (Sheet 26)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
7.287	MLDD	Observe COMPUTER-24 and 25 lamps.					Lit		
7.288	MLDD	Observe COMPUTER- SIGN and 1 through 23 lamps.					Not lit		
7.289	PD	Release RESET-HALT pushbutton/lamp.							
7.290	MLDD	Observe COMPUTER- 23 lamp.					Lit		
7.291	MLDD	Observe COMPUTER-SIGN, 1 through 22, 24, and 25 lamps.					Not lit		
7.292	PD	Observe P40 lamp.					Flashing		
7.293	MLDD	Press and release ADDRESS COMPARE-DATA/INS pushbutton/lamp.							
7.294	MLDD	Observe ADDRESS COMPARE-DATA lamp.					Not lit		
7.295	MLDD	Observe ADDRESS COMPARE-INS lamp.					Lit		
7.296	MLDD	Press and release A6, A3, A2, and A1 pushbutton/lamps.							
7.297	MLDD	Observe COMMAND and COMPUTER-MODULE-0, SYL-0, A6, A3, A2, and A1 lamps (INSTRUCTION ADDRESS area).							
7.298	MLDD	Observe COMMAND and COMPUTER-MODULE-1, SYL-1, A8, A7, A5, A4, and A1 lamps (INSTRUCTION ADDRESS area).							
7.299	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.							

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Figure 7-9. Central Processor Manual Checks (Sheet 27)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
7.300	PD	Observe P40 lamp.					Not flashing		
7.301	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.							
7.302	PD	Press and release MEM ADD REG pushbutton/lamp.							
7.303	PD	Observe MEM ADD REG lamp.					Lit		
7.304	PD	Press and release HOPSAVE REG pushbutton/lamp.							
7.305	PD	Observe HOPSAVE REG lamp.					Not lit		
7.306	PD	Press and release ADVANCE pushbutton twice.							
7.307	PD	Observe A6, A4, and A1 lamps.					Lit		
7.308	PD	Observe A9, A8, A7, A5, A3, and A2 lamps.					Not lit		
7.309	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.							
7.310	MLDD	Press and release ADDRESS COMPARE-DATA/INS pushbutton/lamp.							
7.311	MLDD	Observe ADDRESS COMPARE-DATA lamp.					Lit		
7.312	MLDD	Observe ADDRESS COMPARE-INS lamp.					Not lit		
7.313	MLDD	Press and release OA4, OA3, and OA2 pushbutton/lamps.							

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Figure 7-9. Central Processor Manual Checks (Sheet 28)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
7.314	PD	Press and release RESET-HALT pushbutton/lamp.																			
7.315	PD	Observe A6, A4, and A1 lamps.								Lit											
7.316	PD	Observe A9, A8, A7, A5, A3, and A2 lamps.								Not lit											
7.317	PD	Press and release RESET-MACHINE pushbutton/lamp.																			
7.318	PD	Observe A6, A4, and A1 lamps.								Not lit											
7.319	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.																			
7.320	CE	Press and release ADVANCE pushbutton/lamp.																			
7.321	MLDD	Observe COMPUTER- 23, and 25 lamps.								Lit											
7.322	MLDD	Observe COMPUTER-SIGN and 1 through 22, and 24 lamps.								Not lit											
7.323	PD	Observe P40 lamp.								Flashing											
EXP	NA	Steps 7.324 through 7.455 substantiate that data can be correctly entered in the central processor with the PROG REG A and B toggle switches and that P1 through P40 lamps display correct information.																			
7.324	PD	Set PROG REG A-2, 7, and 12 toggle switches to on (up).																			
7.325	PD	Verify that all other PROG REG-A and B toggle switches are off (down).																			
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Figure 7-9. Central Processor Manual Checks (Sheet 29)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
7.326	PD	Press and release RESET-MACHINE pushbutton/lamp.							
7.327	MLDD	Press and release COMMAND DISPLAY RESET pushbutton/lamp.							
7.328	MLDD	Press and release ADDRESS COMPARE-DATA/INS lamp.							
7.329	MLDD	Observe ADDRESS COMPARE-DATA lamp.					Not lit		
7.330	MLDD	Observe ADDRESS COMPARE-INS lamp.					Lit		
7.331	MLDD	Press and release A6, A5, A4, and A3 pushbutton/lamps.							
7.332	MLDD	Observe COMMAND and COMPUTER-A6, A5, A4, and A3 lamps.					Lit		
7.333	MLDD	Observe COMMAND and COMPUTER-A8, A7, A2, and A1 lamps.					Not lit		
7.334	PD	Set PROG REG B-25, toggle switch to on (up).							
7.335	MLDD	Observe COMPUTER-25 lamp.					Lit		
7.336	PD	Observe P1 lamp.					Lit		
7.337	PD	Observe P2, P4, P10, P20 and P40 lamps.					Not lit		
7.338	PD	Set PROG REG B-25 toggle switch to off and PROG REG B-24 toggle switch to on.							
7.339	MLDD	Observe COMPUTER-24 lamp.					Lit		

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Figure 7-9. Central Processor Manual Checks (Sheet 30)

INTERNATIONAL BUSINESS MACHINES-										
UNIT NAME:									UNIT NO.	
Step	Panel	Operation						Normal Indication	Data	
7.340	PD	Observe P2 lamp.						Lit		
7.341	PD	Observe P1, P4, P10, P20, and P40 lamps.						Not lit		
7.342	PD	Set PROG REG B-24 toggle switch to off and PROG REG B-23 toggle switch to on.								
7.343	MLDD	Observe COMPUTER-23 lamp.						Lit		
7.344	PD	Observe P4 lamp.						Lit		
7.345	PD	Observe P1, P2, P10, P20, and P40 lamps.						Not lit		
7.346	PD	Set PROG REG B-23 toggle switch to off and PROG REG B-22 toggle switch to on.								
7.347	MLDD	Observe COMPUTER-22 lamp.						Lit		
7.348	PD	Observe P10 lamp.						Lit		
7.349	PD	Observe P1, P2, P4, P20, and P40 lamps.						Not lit		
7.350	PD	Set PROG REG B-22 toggle switch to off and PROG REG B-21 toggle switch to on.								
7.351	MLDD	Observe COMPUTER-21 lamp.						Lit		
7.352	PD	Observe P20 lamp.						Lit		
7.353	PD	Observe P1, P2, P4, P10, and P40 lamps.						Not lit		
7.354	PD	Set PROG REG B-21 toggle switch to off and PROG REG B-20 toggle switch to on.								

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Figure 7-9. Central Processor Manual Checks (Sheet 31)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation									Normal Indication	Data	
7.355	MLDD	Observe COMPUTER-20 lamp.									Lit		
7.356	PD	Observe P40 lamp.									Lit		
7.357	PD	Observe P1, P2, P4, P10, and P20 lamps.									Not lit		
7.358	PD	Set PROG REG B-20 toggle switch to off and PRO REG B-19 toggle switch to on.											
7.359	MLDD	Observe COMPUTER-19 lamp.									Lit		
7.360	PD	Observe P1 through P40 lamps.									Not lit		
7.361	PD	Set PROG REG B-19 toggle switch to off and PROG REG B-18 toggle switch to on.											
7.362	MLDD	Observe COMPUTER-18 lamp.									Lit		
7.363	PD	Set PROG REG B-18 toggle switch to off and PROG REG B-17 toggle switch to on.											
7.364	MLDD	Observe COMPUTER-17 lamp.									Lit		
7.365	PD	Set PROG REG B-17 toggle switch to off and PROG REG B-16 toggle switch to on.											
7.366	MLDD	Observe COMPUTER-16 lamp.									Lit		
7.367	PD	Set PROG REG B-16 toggle switch to off and PROG REG B-15 toggle switch to on.											
7.368	MLDD	Observe COMPUTER-15 lamp.									Lit		
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Figure 7-9. Central Processor Manual Checks (Sheet 32)

INTERNATIONAL BUSINESS MACHINES-											
UNIT NAME:										UNIT NO.	
Step	Panel	Operation								Normal Indication	Data
7.369	PD	Set PROG REG B-15 toggle switch to off and PROG REG B-14 toggle switch to on.									
7.370	MLDD	Observe COMPUTER-14 lamp.								Lit	
7.371	PD	Set PROG REG B-14 toggle switch to off and PROG REG B-13 toggle switch to on.									
7.372	MLDD	Observe COMPUTER-13 lamp.								Lit	
7.373	PD	Set PROG REG B-13 toggle switch to off and PROG REG B-12 toggle switch to on.									
7.374	MLDD	Observe COMPUTER-12 lamp.								Lit	
7.375	PD	Set PROG REG B-12 toggle switch to off and PROG REG B-11 toggle switch to on.									
7.376	MLDD	Observe COMPUTER-11 lamp.								Lit	
7.377	PD	Set PROG REG B-11 toggle switch to off and PROG REG B-10 toggle switch to on.									
7.378	MLDD	Observe COMPUTER-10 lamp.								Lit	
7.379	PD	Set PROG REG B-10 toggle switch to off and PROG REG B-9 toggle switch to on.									
7.380	MLDD	Observe COMPUTER-9 lamp.								Lit	
7.381	PD	Set PROG REG B-9 toggle switch to off and PROG REG B-8 toggle switch to on.									

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Figure 7-9. Central Processor Manual Checks (Sheet 33)

INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
7.382	MLDD	Observe COMPUTER-8 lamp.								Lit			
7.383	PD	Set PROG REG B-8 toggle switch to off and PROG REG B-7 toggle switch to on.											
7.384	MLDD	Observe COMPUTER-7 lamp.								Lit			
7.385	PD	Set PROG REG B-7 toggle switch to off and PROG REG B-6 toggle switch to on.											
7.386	MLDD	Observe COMPUTER-6 lamp.								Lit			
7.387	PD	Set PROG REG B-6 toggle switch to off and PROG REG-5 toggle switch to on.											
7.388	MLDD	Observe COMPUTER-5 lamp.								Lit			
7.389	PD	Set PROG REG B-5 toggle switch to off and PROG REG B-4 toggle switch to on.											
7.390	MLDD	Observe COMPUTER-4 lamp.								Lit			
7.391	PD	Set PROG REG B-4 toggle switch to off and PROG REG B-3 toggle switch to on.											
7.392	MLDD	Observe COMPUTER-3 lamp.								Lit			
7.393	PD	Set PROG REG B-3 toggle switch to off and PROG REG B-2 toggle switch to on.											
7.394	MLDD	Observe COMPUTER-2 lamp.								Lit			
7.395	PD	Set PROG REG B-2 toggle switch to off and PROG REG B-1 toggle switch to on.											
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INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:										UNIT NO.			
Step	Panel	Operation								Normal Indication	Data		
7.396	MLDD	Observe COMPUTER-1 lamp.								Lit			
7.397	PD	Set PROG REG B-1 toggle switch to off and PROG REG B-SIGN toggle switch to on.											
7.398	MLDD	Observe COMPUTER-SIGN lamp.								Lit			
7.399	PD	Set PROG REG B-SIGN toggle switch to off.											
7.400	MLDD	Observe COMPUTER-SIGN lamp.								Not lit			
7.401	MLDD	Press and release COMMAND DISPLAY RESET pushbutton/lamp.											
7.402	PD	Set PROG REG A-2, 7, and 12 toggle switches to off.											
7.403	PD	Set PROG REG A-25 toggle switch to on.											
7.404	MLDD	Observe COMPUTER-25 lamp.								Lit			
7.405	PD	Set PROG REG A-25 toggle switch to off and PROG REG A-24 toggle switch to on.											
7.406	MLDD	Observe COMPUTER-24 lamp.								Lit			
7.407	PD	Set PROG REG A-24 toggle switch to off and PROG REG A-23 toggle switch to on.											
7.408	MLDD	Observe COMPUTER-23 lamp.								Lit			
7.409	PD	Set PROG REG A-23 toggle switch to off and PROG REG A-22 toggle switch to on.											
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INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation									Normal Indication	Data	
7.410	MLDD	Observe COMPUTER-22 lamp.									Lit		
7.411	PD	Set PROG REG A-22 toggle switch to off and PROG REG A-21 toggle switch to on.											
7.412	MLDD	Observe COMPUTER-21 lamp.									Lit		
7.413	PD	Set PROG REG A-21 toggle switch to off and PROG REG A-20 toggle switch to on.											
7.414	MLDD	Observe COMPUTER-20 lamp.									Lit		
7.415	PD	Set PROG REG A-20 toggle switch to off and PROG REG A-19 toggle switch to on.											
7.416	MLDD	Observe COMPUTER-19 lamp.									Lit		
7.417	PD	Set PROG REG A-19 toggle switch to off and PROG REG A-18 toggle switch to on.											
7.418	MLDD	Observe COMPUTER-18 lamp.									Lit		
7.419	PD	Set PROG REG A-18 toggle switch to off and PROG REG A-17 toggle switch to on.											
7.420	MLDD	Observe COMPUTER-17 lamp.									Lit		
7.421	PD	Set PROG REG A-17 toggle switch to off and PROG REG A-16 toggle switch to on.											
7.422	MLDD	Observe COMPUTER-16 lamp.									Lit		
7.423	PD	Set PROG REG A-16 toggle switch to off and PROG REG A-15 toggle switch to on.											
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Figure 7-9. Central Processor Manual Checks (Sheet 36)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
7.424	MLDD	Observe COMPUTER-15 lamp.								Lit		
7.425	PD	Set PROG REG A-15 toggle switch to off and PROG REG A-14 toggle switch to on.										
7.426	MLDD	Observe COMPUTER-14 lamp.								Lit		
7.427	PD	Set PROG REG A-14 toggle switch to off and PROG REG A-13 toggle switch to on.										
7.428	MLDD	Observe COMPUTER-13 lamp.								Lit		
7.429	PD	Set PROG REG A-13 toggle switch to off and PROG REG A-12 toggle switch to on.										
7.430	MLDD	Observe COMPUTER-12 lamp.								Lit		
7.431	PD	Set PROG REG A-12 toggle switch to off and PROG REG A-11 toggle switch to on.										
7.432	MLDD	Observe COMPUTER-11 lamp.								Lit		
7.433	PD	Set PROG REG A-11 toggle switch to off and PROG REG A-10 toggle switch to on.										
7.434	MLDD	Observe COMPUTER-10 lamp.								Lit		
7.435	PD	Set PROG REG A-10 toggle switch to off and PROG REG A-9 toggle switch to on.										
7.436	MLDD	Observe COMPUTER-9 lamp.								Lit		

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INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
7.437	PD	Set PROG REG A-9 toggle switch to off and PROG REG A-8 toggle switch to on.																			
7.438	PD	Observe COMPUTER-AA lamp.								Lit											
7.439	PD	Set PROG REG A-8 toggle switch to off and PROG REG A-7 toggle switch to on.																			
7.440	MLDD	Observe COMPUTER-7 lamp.								Lit											
7.441	PD	Set PROG REG A-7 toggle switch to off and PROG REG A-6 toggle switch to on.																			
7.442	MLDD	Observe COMPUTER-6 lamp.								Lit											
7.443	PD	Set PROG REG A-6 toggle switch to off and PROG REG A-5 toggle switch to on.																			
7.444	MLDD	Observe COMPUTER-5 lamp.								Lit											
7.445	PD	Set PROG REG A-5 toggle switch to off and PROG REG A-4 toggle switch to on.																			
7.446	MLDD	Observe COMPUTER-4 lamp.								Lit											
7.447	PD	Set PROG REG A-4 toggle switch to off and then set PROG REG A-3 toggle switch to on.																			
7.448	MLDD	Observe COMPUTER-3 lamp.								Lit											
7.449	PD	Set PROG REG A-3 toggle switch to off and PROG REG A-2 toggle switch to on.																			
7.450	MLDD	Observe COMPUTER-2 lamp.								Lit											
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Figure 7-9. Central Processor Manual Checks (Sheet 38)

INTERNATIONAL BUSINESS MACHINES--						
UNIT NAME:					UNIT NO.	
Step	Panel	Operation	Normal Indication	Data		
7.451	PD	Set PROG REG A-2 toggle switch to off and PROG REG A-1 toggle switch to on.				
7.452	MLDD	Observe COMPUTER-1 lamp.	Lit	_____		
7.453	PD	Set PROG REG A-1 toggle switch to off and PROG REG A-SIGN toggle switch to on.				
7.454	MLDD	Observe COMPUTER-SIGN lamp.	Lit	_____		
7.455	PD	Observe P40 lamp.	Flashing	_____		
EXP	NA	Steps 7.456 through 7.480 substantiate that data can be manually loaded into the central processor memory with the MEMORY BUFFER REGISTER pushbuttons.				
7.456	MLDD	Press and release A6 and A4, pushbutton/lamps.				
7.457	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.				
7.458	MLDD	Observe COMMAND and COMPUTER-A6, A4, and A1 lamps.	Lit	_____		
7.459	MLDD	Observe COMMAND and COMPUTER-A8, A7, A5, A3, and A2 lamps.	Not lit	_____		
7.460	PD	Observe PARITY ERROR lamp (if lit press and release ERROR RESET pushbutton/lamp).	Not lit	_____		
7.461	PD	Observe ERROR HOLD lamp (press and release if lit).	Not lit	_____		
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UNIT NAME:								UNIT NO.																																													
Step	Panel	Operation					Normal Indication	Data																																													
7.462	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.																																																			
7.463	CE	Press and release ADVANCE push-button.																																																			
7.464	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE PHASE.																																																			
7.465	CE	Press and release ADVANCE pushbutton.																																																			
7.466	CE	Observe MBR 1 through MBR 13 and ODD PARITY lamps (press and release if lit).					Not lit																																														
7.467	CE	Press and release BIT 4/MBR 4 and BIT 14/ODD PARITY push-button/lamps.																																																			
7.468	CE	Observe MBR 2 and ODD PARITY lamps.					Lit																																														
7.469	CE	Press and release LOAD pushbutton.																																																			
7.470	CE	Observe BIT 4 and BIT 14 lamps.					Lit																																														
7.471	CE	Press and release ADVANCE push-button twice.																																																			
7.472	CE	Press and release BIT 2/MBR 2, BIT 10/MBR 10, BIT 11/MBR 11, BIT 12/MBR 12 and BIT 14/MBR 14 pushbutton lamps.																																																			
7.473	CE	Observe MBR 2, MBR 4, MBR 10, MBR 11, and MBR 12 lamps.					Lit																																														
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INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation						Normal Indication	Data			
7.474	CE	Press and release LOAD pushbutton/lamp.										
7.475	CE	Observe BIT 2, BIT 4, BIT 10, BIT 11, BIT 12, and BIT 14 lamps.						Lit	_____			
7.476	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.										
7.477	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.										
7.478	CE	Press and release ADVANCE pushbutton.										
7.479	PD	Observe P20 lamp.						Flashing	_____			
7.480	PD	Observe P40 lamp.						Not flashing	_____			
EXP	NA	Steps 7.481 through 7.539 demonstrate that the error hold feature and remote advance feature are functioning properly.										
7.481	PD	Press and release PARITY ERROR/ERROR HOLD pushbutton/lamp.										
7.482	PD	Observe ERROR HOLD lamp.						Lit	_____			
7.483	PD	Observe P20 lamp.						Not flashing	_____			
7.484	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, A4, A2, and A1 lamps.						Lit	_____			
7.485	MLDD	Observe COMPUTER-MODULE-1, SYL-1, IS1 through IS4, A8, A7, A5 and A3 lamps.						Not lit	_____			
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INTERNATIONAL BUSINESS MACHINES—												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation						Normal Indication	Data			
7.486	CE	Connect the remote advance switch to ADV REMOTE jacks.										
7.487	CE	Actuate the remote advance switch.										
7.488	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, A4, and A3 lamps.						Lit	_____			
7.489	MLDD	Observe COMPUTER-MODULE-1, SYL-1, DS1 through DS4, A8, A7, A2, and A1 lamps.						Not lit	_____			
7.490	MLDD	Press and release A6, A4, and A1 pushbutton/lamps.										
7.491	MLDD	Observe COMMAND-A6, A4, and A1 lamps.						Lit	_____			
7.492	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.										
7.493	PD	Press and release ERROR RESET pushbutton/lamp.										
7.494	PD	Observe PARITY ERROR lamp.						Not lit	_____			
7.495	CE	Actuate the remote advance switch.										
7.496	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, A4 and A1 lamps.						Lit	_____			
7.497	MLDD	Observe COMPUTER-MODULE-1, SYL-1, A8, A7, A5, A3, and A2 lamps.						Not lit	_____			
7.498	PD	Observe PARITY ERROR lamp.						Not lit	_____			
7.499	MLDD	Press and release A2 and A1 pushbutton/lamps.										

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INTERNATIONAL BUSINESS MACHINES--				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
7.500	CE	Actuate the remote advance switch.		
7.501	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, A4, and A2 lamps.	Lit	_____
7.502	MLDD	Observe COMPUTER-MODULE-1, SYL-1, A8, A7, A5, A3, and A1 lamps.	Not lit	_____
7.503	PD	Observe PARITY ERROR lamp.	Lit	_____
7.504	MLDD	Press and release A2 pushbutton/lamp.		
7.505	PD	Press and release ERROR RESET pushbutton/lamp.		
7.506	PD	Observe PARITY ERROR lamp.	Not lit	_____
7.507	CE	Actuate the remote advance switch.		
7.508	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, and A4 lamps.	Lit	_____
7.509	MLDD	Observe COMPUTER-MODULE-1, SYL-1, A8, A7, A5, A3, A2, and A1 lamps.	Not lit	_____
7.510	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE INST.		
7.511	CE	Actuate the remote advance switch.		
7.512	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to SINGLE PHASE.		
7.513	CE	Actuate the remote advance switch.		

Figure 7-9. Central Processor Manual Checks (Sheet 43)

INTERNATIONAL BUSINESS MACHINES—										
UNIT NAME:									UNIT NO.	
Step	Panel	Operation					Normal Indication	Data		
7.514	PD	Observe PARITY ERROR lamp.					Lit	_____		
7.515	CE	Observe BIT 4 and BIT 14 lamps.					Lit	_____		
7.516	CE	Observe BIT 1, BIT 2, BIT 3, and BIT 5 through BIT 13 lamps.					Not lit	_____		
7.517	CE	Press and release BIT 2/MBR 2, BIT 10/MBR 10, BIT 11/MBR 11, and BIT 12/MBR 12 lamps.								
7.518	CE	Observe MBR 4 lamp.					Lit	_____		
7.519	CE	Observe MBR 1, MBR 2, MBR 3, MBR 5 through MBR 13, and ODD PARITY lamps.					Not lit	_____		
7.520	CE	Press and release LOAD pushbutton/lamp.								
7.521	CE	Observe BIT 4 lamp.					Lit	_____		
7.522	CE	Observe BIT 1, BIT 2, BIT 3, and BIT 4 through BIT 14 lamps.					Not lit	_____		
7.523	CE	Actuate the remote advance switch twice.								
7.524	CE	Observe BIT 2, BIT 4, BIT 10, BIT 11 and BIT 12 lamps.					Lit	_____		
7.525	CE	Observe BIT 1, BIT 3, BIT 5 through BIT 9, BIT 13 and BIT 14 lamps.					Not lit	_____		
7.526	CE	Press and release BIT 2/MBR 2, BIT 10/MBR 10, BIT 11/MBR 11, BIT 12/MBR 12, and BIT 14/MBR 14 pushbutton/lamps.								

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Figure 7-9. Central Processor Manual Checks (Sheet 44)

INTERNATIONAL BUSINESS MACHINES--												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
7.527	CE	Observe MBR 2, MBR 4, MBR 10, MBR 11, MBR 12, and ODD PARITY lamps.							Lit	_____		
7.528	CE	Observe MBR 1, MBR 3, MBR 5 through MBR 9, and MBR 13 lamps.							Not lit	_____		
7.529	CE	Press and release LOAD pushbutton/lamp.								_____		
7.530	CE	Observe BIT 2, BIT 4, BIT 10, BIT 11, BIT 12, and BIT 14 lamps.							Lit	_____		
7.531	CE	Observe BIT 1, BIT 3, BIT 5 through BIT 9, and BIT 13 lamps.							Not lit	_____		
7.532	CE	Set NORM/SINGLE BIT/SINGLE PHASE/SINGLE INST switch to NORM.								_____		
7.533	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.								_____		
7.534	PD	Press and release ERROR RESET pushbutton/lamp.								_____		
7.535	PD	Observe PARITY ERROR lamp.							Not lit	_____		
7.536	CE	Actuate the remote advance switch.								_____		
7.537	MLDD	Observe COMPUTER-MODULE-0, SYL-0, A6, A4, A2, and A1 lamps.							Lit	_____		
7.538	MLDD	Observe COMPUTER-MODULE-1, SYL-1, A8, A7, A5, and A3 lamps.							Not lit	_____		
7.539	PD	Observe PARITY ERROR lamp.							Lit	_____		

Figure 7-9. Central Processor Manual Checks (Sheet 45)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
EXP	NA	Steps 7.539 through 7.549 substantiate that the PTC can be manually placed into a single step condition.							
7.540	PD	Press and release PARITY ERROR/ERROR HOLD pushbutton/lamp.							
7.541	PD	Observe ERROR HOLD lamp.				Not lit	_____		
7.542	PD	Press and release RESET-MACHINE pushbutton/lamp.							
7.543	PD	Observe P20 lamp.				Flashing	_____		
7.544	PD	Press and release CST/MAN CST pushbutton/lamp.							
7.545	PD	Observe CST and MAN CST lamps.				Lit	_____		
7.546	PD	Observe P20 lamp.				Not flashing	_____		
7.547	PD	Press and release CST/MAN CST pushbutton/lamp.							
7.548	PD	Observe CST and MAN CST lamps.				Not lit	_____		
7.549	PD	Observe P20 lamp.				Flashing	_____		
	NA	Steps 7.550 through 7.564 substantiate that the PTC can be placed into a CST condition under external control (ACNCST).							
7.550	MLDD	Press and release ADDRESS COMPARE-DATA/INS lamp.							
7.551	MLDD	Observe ADDRESS COMPARE-DATA lamp.				Lit	_____		

Figure 7-9. Central Processor Manual Checks (Sheet 46)

INTERNATIONAL BUSINESS MACHINES-																																																					
UNIT NAME:									UNIT NO.																																												
Step	Panel	Operation					Normal Indication	Data																																													
7.552	MLDD	Press and release COMMAND DISPLAY RESET pushbutton/lamp.																																																			
7.553	MLDD	Press and release OA4, OA3, and OA2 pushbutton/lamps.																																																			
7.554	PD	Set PROG REG A-SIGN toggle switch to off.																																																			
7.555	PD	Set PROG REG A-1 toggle switch to on.																																																			
7.556	MLDD	Observe COMMAND and COMPUTER-MODULE 0, OA4, OA3, and OA2 lamps.					Lit	_____																																													
7.557	MLDD	Observe COMMAND and COMPUTER-DS1 through DS4, MODULE 1, OA5 through OA9, and OA1 lamps.					Not lit	_____																																													
7.558	MLDD	Observe that binary count indicated on DATA area COMPUTER lamps is incrementing.						_____																																													
7.559	TRMC	Observe SEL ADR lamp (press and release if lit).					Not lit	_____																																													
7.560	TRMC	Observe ADR 3 and ADR 4 lamps (press and release if not lit).					Lit	_____																																													
7.561	TRMC	Observe ADR 1, ADR 2, and ADR 5 lamps.					Not lit	_____																																													
7.562	PD	Observe CST lamp.					Lit	_____																																													
7.563	MLDD	Observe MODULE-0 and SYL-0 (INSTRUCTION ADDRESS area) and MODULE-0 (DATA ADDRESS area) COMPUTER lamps.					Lit	_____																																													
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Figure 7-9. Central Processor Manual Checks (Sheet 47)

INTERNATIONAL BUSINESS MACHINES—																																																						
UNIT NAME:									UNIT NO.																																													
Step	Panel	Operation						Normal Indication	Data																																													
7.564	MLDD	Observe all other COMPUTER lamps.						Not lit																																														
EXP	NA	Steps 7.565 through 7.568 substantiate that the PTC recognizes and stores an interrupt while in a single step condition.																																																				
7.565	PD	Press and release I16 pushbutton lamp.																																																				
7.566	PD	Observe I16 and INT B lamps						Lit																																														
7.567	MLDD	Observe COMPUTER-A7 and A1 lamps.						Lit																																														
7.568	MLDD	Observe COMPUTER-A8 and A2 through A6 lamps.						Not lit																																														
	NA	Steps 7.569 through 7.578 substantiate that the PTC can be advanced under external control (ACGACISS) while in a CST condition																																																				
7.569	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ pushbutton/lamp.																																																				
7.570	TRMC	Observe ADR4 lamp.						Not lit																																														
7.571	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp																																																				
7.572	TRMC	Observe ADR5 lamp.						Lit																																														
7.573	MLDD	Observe COMPUTER-A7 and A2 lamps.						Lit																																														
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Figure 7-9. Central Processor Manual Checks (Sheet 48)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:									UNIT NO.											
Step	Panel	Operation					Normal Indication	Data												
7.574	MLDD	Observe COMPUTER-A8, A6, A5, A4, A3, and A1 lamps.					Not lit	_____												
7.575	PD	Observe I16 lamp.					Not lit	_____												
7.576	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp twice.						_____												
7.577	MLDD	Observe COMPUTER-A7, A2, and A1 lamps.					Lit	_____												
7.578	MLDD	Observe COMPUTER-A8, A6, A5, A4, and A3 lamps.					Not lit	_____												
EXP	NA	Steps 7.579 through 7.586 substantiate that the PTC can not be advanced under external control while the PROG CYCLE-ADR HOLD or SINGLE STEP modes are selected.						_____												
7.579	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.						_____												
7.580	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp twice.						_____												
7.581	MLDD	Observe COMPUTER-A7, A2, and A1 lamps.					Lit	_____												
7.582	MLDD	Observe COMPUTER-A8, A6, A5, A4, and A3 lamps.					Not lit	_____												
7.583	MLDD	Set MODE CONTROL switch to PROG CYCLE - SINGLE STEP.						_____												
7.584	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp twice.						_____												
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Figure 7-9. Central Processor Manual Checks (Sheet 49)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
7.585	MLDD	Observe COMPUTER-A7, A2, and A1 lamps.					Lit	_____	
7.586	MLDD	Observe COMPUTER-A8, A6, A5 and A3 lamps.					Not lit	_____	
EXP	NA	Steps 7.587 through 7.593 substantiate the PTC can be placed into a single step condition by a CIO 114g command.							
7.587	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.							
7.588	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ , 2 ⁵ /2 ⁴ /ADR2/2 ³ and 2 ² /2 ⁴ ADR1/2 ⁰ pushbutton/lamp.							
7.589	TRMC	Observe ADR5, ADR4, ADR2, and ADR1 lamps.					Lit	_____	
7.590	TRMC	Press and release 2 ⁸ /2 ⁹ /ADR3/2 ⁶ pushbutton lamp.							
7.591	TRMC	Observe ADR3 lamp.					Not lit	_____	
7.592	MLDD	Observe COMPUTER-A7 and A4 lamps.					Lit	_____	
7.593	MLDD	Observe COMPUTER-A8, A6, A5, A3, A2, and A1 lamps.					Not lit	_____	
		Steps 7.594 through 7.656 substantiate that the circuit which generates the PTC CST signal is functioning properly.							

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Figure 7-9. Central Processor Manual Checks (Sheet 50)

INTERNATIONAL BUSINESS MACHINES—												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
7.594	PD	Observe I15 lamp.								Lit	_____	
7.595	TRMC	Press and release 2 ⁵ /2 ⁴ /ADR ² /2 ³ and 2 ² /2 ¹ /ADR1/2 ⁰ pushbutton lamps.										
7.596	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp.										
7.597	TRMC	Observe ADR5, ADR2, and ADR1 lamps.								Not lit	_____	
7.598	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ pushbutton/lamp.										
7.599	TRMC	Observe ADR4 lamp.								Not lit	_____	
7.600	TRMC	Press and release 2 ¹² /ADR5 pushbutton/lamp.										
7.601	TRMC	Observe ADR5 lamp.								Lit	_____	
7.602	MLDD	Observe COMPUTER-A7, A4, and A1 lamps.								Lit	_____	
7.603	MLDD	Observe COMPUTER-A8, A6, A5, A3, and A1 lamps.								Not lit.	_____	
7.604	PD	Observe I15 lamp.								Not lit	_____	
7.605	PD	Press and release CST/MAN CST pushbutton/lamp										
7.606	PD	Observe CST and MAN CST lamps.								Lit	_____	
7.607	TRMC	Press 2 ¹² /ADR5 pushbutton/lamp twice.										

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Figure 7-9. Central Processor Manual Checks (Sheet 51)

INTERNATIONAL BUSINESS MACHINES—									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
7.608	MLDD	Observe COMPUTER-A7, A4, and A2 lamps.					Lit	_____	
7.609	MLDD	Observe COMPUTER-A8, A6, A5, A3, and A1 lamps.					Not lit	_____	
7.610	PD	Observe I15 lamp.					Lit	_____	
7.611	PD	Press and release CST/MAN CST lamp.						_____	
7.612	MLDD	Observe COMPUTER-A7, A4, A2, and A1 lamps.					Lit	_____	
7.613	MLDD	Observe COMPUTER-A8, A6, A5, A3, and A1 lamps.					Not lit	_____	
7.614	PD	Observe I15 lamp.					Not lit	_____	
7.615	MLDD	Set MODE CONTROL switch to PROG CYCLE-SINGLE STEP						_____	
7.616	MLDD	Press and release ADDRESS COMPARE - DATA/INS pushbutton/lamp.						_____	
7.617	MLDD	Observe ADDRESS COMPARE-INS lamp.					Lit	_____	
7.618	MLDD	Press and release A7, A4 and A3 pushbutton/lamps.						_____	
7.619	PD	Press and release ADVANCE pushbutton.						_____	
7.620	MLDD	Observe COMMAND and COMPUTER A7, A4, and A3 lamps.					Lit	_____	

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Figure 7-9. Central Processor Manual Checks (Sheet 52)

INTERNATIONAL BUSINESS MACHINES-				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
7. 621	MLDD	Observe COMMAND and COMPUTER A8, A6, A5, A2, and A1 lamps.	Not lit	
7. 622	PD	Observe I15 lamp.	Lit	
7. 623	PD	Observe INT B lamp.	Lit	
7. 624	MLDD	Set MODE CONTROL switch to DISPLAY-REPEAT.		
7. 625	PD	Press and release 2 ¹² /ADR5 pushbutton/lamp twice.		
7. 626	MLDD	Observe COMPUTER-A7, A4, A3, and A1 lamps.	Lit	
7. 627	MLDD	Observe COMPUTER-A8, A6, A5, and A2 lamps.	Not lit	
7. 628	MLDD	Observe I15 lamp.	Lit	
7. 629	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ 2 ⁵ /2 ⁴ /ADR2/2 ³ and 2 ² /1 ²¹ /ADR1/2 ⁰ pushbutton/lamps.		
7. 630	TRMC	Observe ADR4, ADR2, and ADR1 lamps.	Lit	
7. 631	TRMC	Press and release 2 ⁸ /2 ⁷ /ADR3/2 ⁶ pushbutton lamp.		
7. 632	TRMC	Observe ADR3 lamp.	Not lit	
7. 633	PD	Observe CST lamp.	Not lit	
7. 634	PD	Observe PARITY ERROR lamp (if lit press and release ERROR RESET)	Not lit	

Figure 7-9. Central Processor Manual Checks (Sheet 53)

INTERNATIONAL BUSINESS MACHINES-											
UNIT NAME:									UNIT NO.		
Step	Panel	Operation					Normal Indication	Data			
7. 635	PD	Press and release PARITY ERROR/ ERROR HOLD pushbutton lamp.									
7. 636	PD	Observe ERROR HOLD lamp.					Lit				
7. 637	PD	Set PROG REG A-SIGN toggle switch to on.					Lit				
7. 638	MLDD	Observe COMPUTER A6, A4, and A2 lamps.					Lit				
7. 639	MLDD	Observe COMPUTER A8, A7, A5, A3, and A1 lamps.					Lit				
7. 640	PD	Observe PARITY ERROR, CST, and I15 lamps.					Not lit				
7. 641	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ pushbutton/lamp.									
7. 642	TRMC	Observe ADR4 lamp.					Not lit				
7. 643	TRMC	Press and release 2 ¹² /ADR5, 2 ⁵ /2 ⁴ / ADR2/2 ³ , and 2 ² /2 ¹ /ADR1/2 ⁰ lamp.									
7. 644	TRMC	Observe ADR5, ADR2, and ADR1 lamps.					Not lit				
7. 645	PD	Press and release ERROR HOLD pushbutton/lamp.									
7. 646	PD	Observe ERROR HOLD lamp.					Not lit				
7. 647	PD	Press and release ADVANCE pushbutton.									
7. 648	PD	Observe P20 lamp.					Flashing				

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Figure 7-9. Central Processor Manual Checks (Sheet 54)

INTERNATIONAL BUSINESS MACHINES-																																																				
UNIT NAME:									UNIT NO.																																											
Step	Panel	Operation					Normal Indication	Data																																												
7. 649	PD	Set PROG REG A-SIGN toggle switch to off.																																																		
7. 650	PD	Set PROG REG A-5, 7, and 9 and PROG REG B-3 toggle switches to on.																																																		
7. 651	PD	Press and release RESET-MACHINE pushbutton.																																																		
7. 652	PD	Set PROG REG A-3 toggle switch to on and then back to off.																																																		
7. 653	PD	Set PROG REG A-5, 7, and 9 and PROG REG B-3 toggle switches to off.																																																		
7. 654	PD	Set PROG REG A-6 toggle switch to on.																																																		
7. 655	PD	Set PROG REG A-3 toggle switch to on and then back to off.																																																		
7. 656	PD	Observe I15 lamp.					Not lit																																													
EXP	NA	Steps 7. 657 through 7 substantiate that the syne error circuit is functioning properly.																																																		
7. 657	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ , 2 ⁵ /2 ⁴ /ADR2/2 ³ , and 2 ² /2 ¹ /ADR1/2 ⁰ pushbutton/lamps.																																																		
7. 658	TRMC	Observe ADR4, ADR2, and ADR1 lamps.					Lit																																													
7. 659	PD	Observe SYNC ERROR lamp					Lit																																													
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Figure 7-9. Central Processor Manual Checks (Sheet 55)

INTERNATIONAL BUSINESS MACHINES-																																																								
UNIT NAME:										UNIT NO.																																														
Step	Panel	Operation								Normal Indication	Data																																													
7.660	TRMC	Press and release 2 ¹¹ /2 ¹⁰ /ADR4/2 ⁹ , 2 ⁵ /2 ⁴ /ADR2/2 ³ , and 2 ² /2 ¹ /ADR1/2 ⁰ pushbutton/lamps.																																																						
7.661	TRMC	Observe ADR4, ADR2, and ADR1 lamps.								Not lit																																														
7.662	PD	Press and release RESET-MACHINE pushbutton/lamp.																																																						
7.663	PD	Observe SYNC ERROR lamp.								Not lit																																														
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Figure 7-9. Central Processor Manual Checks (Sheet 56)

INTERNATIONAL BUSINESS MACHINES--									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
EXP	NA	Steps 8.1 through 8.33 substantiate that the test program for memory module 1 is loaded correctly into the central processor memory.							
8.1	TRMC	Observe FREE RUN SS lamp (press and release if lit).				Not lit			
8.2	TRMC	Observe FREE RUN READER lamp (press and release if lit).				Not lit			
8.3	TRMC	Observe PWR ON lamp (press and release if not lit).				Lit			
8.4	TRMC	Observe INHIBIT READER lamp (press and release if lit).				Not lit			
8.5	TRMC	Observe FORWARD lamp (press and release if not lit).				Lit			
8.6	TRMC	Observe REVERSE lamp.				Not lit			
8.7	TRMC	Observe VERIFY ONLY lamp (press and release if lit).				Not lit			
8.8	TRMC	Observe AUTO lamp (press and release if lit).				Not lit			
8.9	TRMC	Observe MANUAL lamp.				Lit			
8.10	TRMC	Observe ML lamp (press and release if not lit).				Lit			
8.11	TRMC	Observe DD lamp.				Not lit			
8.12	TRMC	Observe SEL ADR lamp (press and release if not lit).				Lit			

Figure 7-10. Central Processor Memory Automatic Checks (Sheet 1 of 8)

INTERNATIONAL BUSINESS MACHINES-												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
8.13	TRMC	Observe ADR 1 through ADR 5 lamps (press and release if lit).								Not lit		
8.14	TRMC	Observe SELF CHECK lamp (press and release if not lit).								Lit		
8.15	NA	Remove plastic guard from tape spooler.										
8.16	NA	Lower tape guide on read step photo-cell assembly to its bottom stop (B on illustration A).										
8.17	NA	Place the reel containing self test tape part number 6001232 on left hub with edge of tape closest to sprocket holes next to panel.										
8.18	NA	Thread tape as shown on illustration A.										
8.19	NA	Position the tape so that leader portion (sprocket holes only) following the punched title is under the photo-cell.										
8.20	NA	Check for proper alignment of the tape within the guides of the read station.										
8.21	NA	Raise the tape guide one stop. Note that the guide has three discernible stops.										
8.22	NA	Adjust tape tension by rotating both reels manually until the tension arms (A on illustration A) are located at the approximate center of their swing.										
A B C D E F G H I J K L M N O P Q R PAGE										PAGES		NUMBER
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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

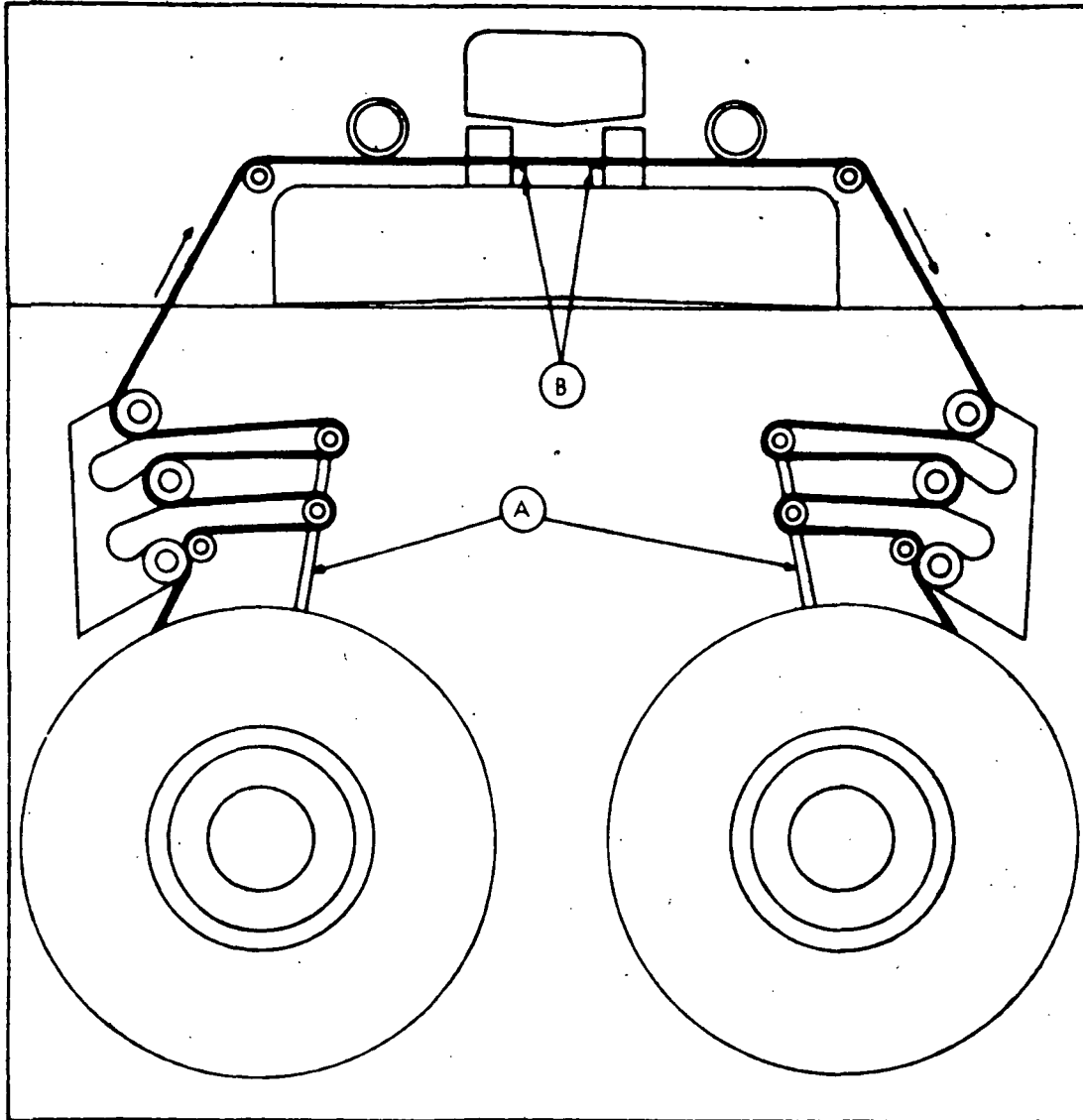


ILLUSTRATION A

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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES--										
UNIT NAME:							UNIT NO.			
Step	Panel	Operation					Normal Indication	Data		
8.23	NA	Replace plastic guard.								
8.24	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.								
8.25	NA	Observe that tape advances until the beginning of the punched area is reached.								
8.26	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.								
8.27	TRMC	Observe AUTO lamp					Lit			
8.28	TRMC	Observe MANUAL lamp.					Not lit			
8.29	MLDD	Press and release ERROR RESET pushbutton/lamp.								
8.30	MLDD	Observe PARITY, TAPE, and COMPARE lamps.					Not lit			
8.31	MLDD	Press and release START pushbutton/lamp.								
8.32	NA	Observe that tape advances until the end of the punched area is reached.								
8.33	MLDD	Observe PARITY, TAPE, and COMPARE lamps.					Not lit			
EXP	NA	Steps 8.34 through 8.49 substantiate that information can be wrote into all locations in memory module 1 and then read out correctly.								
8.34	MLDD	Verify that MODE CONTROL switch is set to DISPLAY-REPEAT.								
A B C D E F G H I J K L M N O P Q R PAGE							PAGES		NUMBER	
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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
8.35	PD	Observe PARITY ERROR lamp (press and release error reset if lit).								Not lit			
8.36	PD	Observe ERROR HOLD lamp (press and release if lit).								Not lit			
8.37	PD	Observe MAN CST lamp (press and release if lit).								Not lit			
8.38	PD	Observe INHIBIT CTRL lamp (press and release if lit).								Not lit			
8.39	PD	Observe PROGRAM ERROR lamp (press and release if lit).								Not lit			
8.40	PD	Verify that all PROG REG A and PROG REG B toggle switches are off (down).											
8.41	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.											
8.42	TRMC	Press and release ML/DD pushbutton/lamp.											
8.43	TRMC	Observe ML/lamp.								Not lit			
8.44	MLDD	Observe DD lamp.								Lit			
8.45	PD	Set PROG REG A-5 toggle switch to on (up).											
8.46	PD	Set PROG REG A-16 toggle switch to on (up).											
8.47	PD	Observe that binary count indicated on P1, P2, and P4 lamps is incremented approximately once per minute.											

Figure 7-10. Central Processor Memory Automatic Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:								UNIT NO.	
Step	Panel	Operation					Normal Indication	Data	
8.48	PD	When P1, P2 and P4 lamps indicate a count of five (P1 and P4 only, are lit) set PROG REG A-5 and 16 toggle switches to off.							
8.49	PD	Observe PROGRAM ERROR lamp.					Not lit		
EXP	NA	Steps 8.50 through 8.61 substantiate that the test program for memory module 0 is loaded correctly into the central processor memory.							
8.50	TRMC	Press and release ML/DD push-button lamp.							
8.51	TRMC	Observe ML lamp.					Lit		
8.52	TRMC	Observe DD lamp.					Not lit		
8.53	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/lamp.							
8.54	NA	Observe that tape advances until the beginning of the second punched area of the tape is reached.							
8.55	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.							
8.56	TRMC	Observe AUTO lamp.					Lit		
8.57	TRMC	Observe MANUAL lamp					Not lit		
8.58	MLDD	Observe PARITY, TAPE, and COMPARE lamps (if any are lit, press and release ERROR RESET push-button).					Not lit		
A B C D E F G H I J K L M N O P Q R PAGE						PAGES	NUMBER		
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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-															
UNIT NAME:												UNIT NO.			
Step	Panel	Operation										Normal Indication	Data		
8.59	TRMC	Press and release START push-button/lamp.													
8.60	NA	Observe that tape advances until the end of the punched area is reached. Tape then rewinds back to the beginning of the first punched area of the tape.													
8.61	MLDD	Observe PARITY, TAPE, and COMPARE lamps.										Not lit			
EXP	NA	Steps 8.61 through 8.70 substantiate that information can be wrote into all locations in memory module 0 and then read out correctly.													
8.62	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.													
8.63	TRMC	Press and read ML/DD pushbutton lamp.													
8.64	TRMC	Observe ML lamp.										Not lit			
8.65	TRMC	Observe DD lamp.										Lit			
8.66	PD	Set PROG REG A-5 toggle switch to on.													
8.67	PD	Set PROG REG A-16 toggle switch to on.													
8.68	PD	Observe that the binary count indicated on P1, P2, and P4 lamps is incremented approximately once per minute.													

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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—																																																							
UNIT NAME:										UNIT NO.																																													
Step	Panel	Operation								Normal Indication	Data																																												
8.69	PD	When P1, P2, and P4 lamps indicate a count of five (P1 and P4 only are lit) set PROG REG A-5 and 16 toggle switches to off.																																																					
8.70	PD	Observe PROGRAM ERROR lamp.								Not lit																																													
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>I</td><td>J</td><td>K</td><td>L</td><td>M</td><td>N</td><td>O</td><td>P</td><td>Q</td><td>R</td><td>PAGE</td><td></td><td>PAGES</td><td>NUMBER</td> </tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>OF</td><td></td><td>A-</td> </tr> </table>												A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER																				OF		A-
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Figure 7-10. Central Processor Memory Automatic Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:								UNIT NO.												
Step	Panel	Operation					Normal Indication	Data												
EXP	NA	Steps 9.1 through 9.28 substantiate that the self test program is loaded correctly into the central processor memory.																		
9.1	TRMC	Observe FORWARD lamp (press and release if not lit).					Lit													
9.2	TRMC	Observe REVERSE lamp.					Not lit													
9.3	TRMC	Observe VERIFY ONLY lamp (press and release if lit).					Not lit													
9.4	TRMC	Observe AUTO lamp (press and release if lit).					Not lit													
9.5	TRMC	Observe MANUAL lamp.					Lit													
9.6	TRMC	Observe ML lamp (press and release if not lit).					Lit													
9.7	TRMC	Observe DD lamp.					Not lit													
9.8	TRMC	Observe SEL ADR lamp (press and release if not lit).					Lit													
9.9	TRMC	Observe ADR 1 through ADR 5 lamps (press and release if lit).					Not lit													
9.9.1		Verify the plotter is turned on.																		
9.10	NA	Remove plastic guard from tape spooler.																		
9.11	NA	Lower tape guide on read step photo-cell assembly to its bottom stop (B on illustration A).																		
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Figure 7-11. Self-Test Program Checks (Sheet 1 of 22)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME:

UNIT NO.

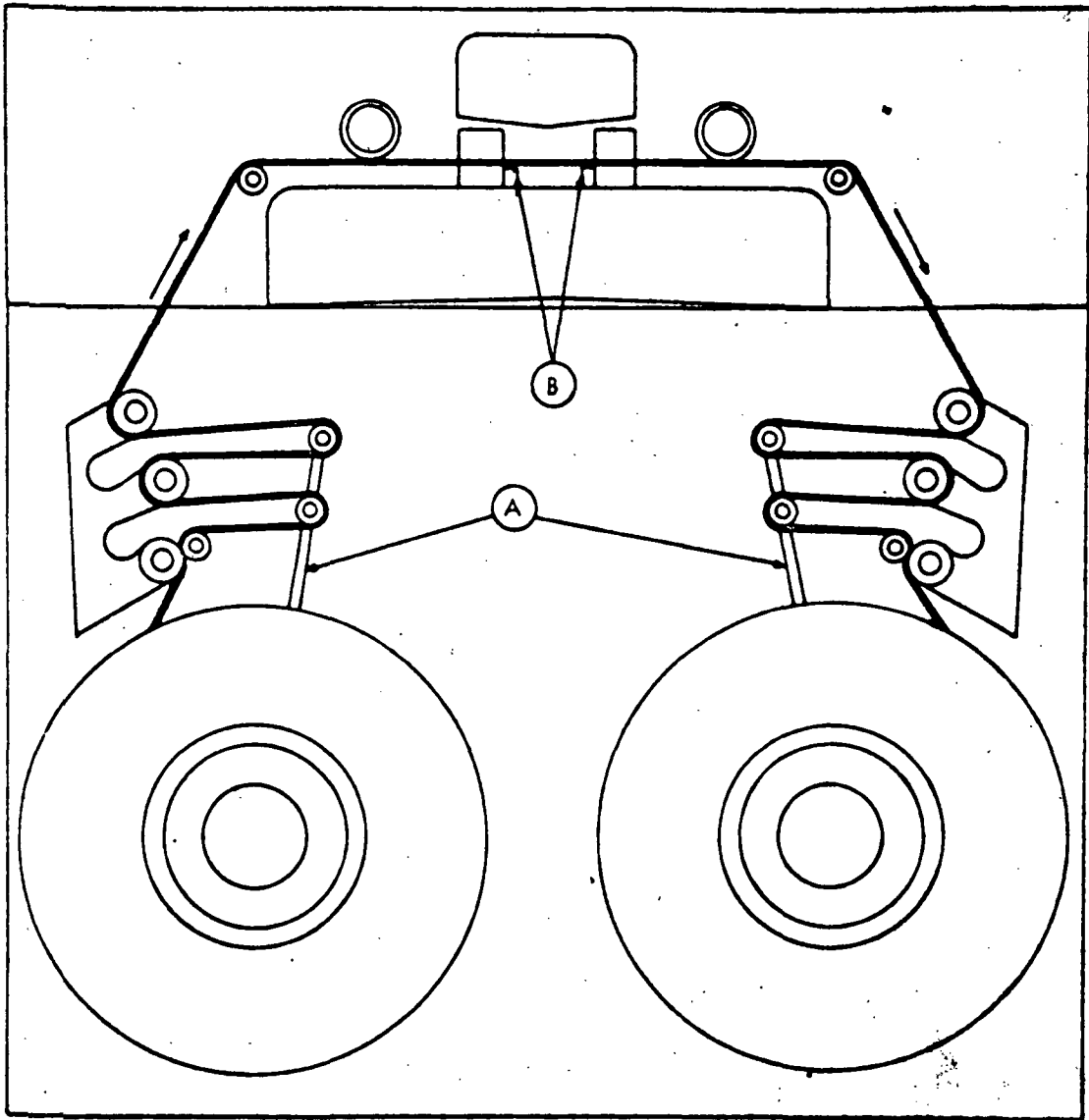


ILLUSTRATION A

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Figure 7-11. Self-Test Program Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation							Normal Indication	Data										
9.12	NA	Place the reel containing self test tape part number 6001236 on left nub with edge of tape closest to sprocket holes next to panel.																		
9.13	NA	Thread tape as shown on Illustration A.																		
9.14	NA	Position the tape so that leader portion (sprocket holes only) following the punched title is under the photocell.																		
9.15	NA	Check for proper alignment of the tape within the guides of the read station.																		
9.16	NA	Raise the tape guide one stop.																		
9.17	NA	Adjust tape tension by rotating both reels manually until the tension arms (A on Illustration A) are located at the approximate center of their swing.																		
9.18	NA	Replace plastic guard.																		
9.19	TRMC	Press and release MANUAL ADVANCE TAPE pushbutton/ lamp.																		
9.20	NA	Observe that tape advances until the beginning of the punched area is reached.																		
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-11. Self-Test Program Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation							Normal Indication	Data											
9.21	TRMC	Press and release AUTO/ MANUAL pushbutton/ lamp.																			
9.22	TRMC	Observe AUTO lamp.							Lit												
9.23	TRMC	Observe MANUAL lamp.							Not lit												
9.24	MLDD	Press and release ERROR RESET pushbutton/ lamp.																			
9.25	MLDD	Observe PARITY, TAPE, and COMPARE lamps.							Not lit												
9.26	MLDD	Press and release START pushbutton/ lamp.																			
9.27	NA	Observe that tape advances until the end of the punched area is reached. Tape then rewinds back to the beginning of the punched area.																			
9.28	MLDD	Observe PARITY, TAPE, and COMPARE lamps.							Not lit												
EXP	NA	Steps 9.29 through 9.44 substantiate the test program control loop is cycling and that error storage is cleared.																			
9.29	MLDD	Verify that MODE CONTROL switch is set to DISPLAY-REPEAT.																			
9.30	PD	Observe PARITY ERROR lamp (press and release error reset if lit).							Not lit												
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Figure 7-11. Self-Test Program Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:								UNIT NO.													
Step	Panel	Operation					Normal Indication	Data													
9.31	PD	Observe ERROR HOLD lamp (press and release if lit).					Not lit														
9.32	PD	Observe MAN CST lamp (press and release if lit).					Not lit														
9.33	PD	Observe INHIBIT CTRL lamp (press and release if lit).					Not lit														
9.34	PD	Observe PROGRAM ERROR lamp (press and release if lit).					Not lit														
9.35	PD	Verify that all PROG REG A and PROG REG B toggle switches are off (down).																			
9.35.1	TRMC	Press and release AUTO/MANUAL pushbutton/lamp.																			
9.36	TRMC	Press and release ML/DD pushbutton/lamp.																			
9.37	TRMC	Observe ML/lamp.					Not lit														
9.38	MLDD	Observe DD lamp.					Lit														
9.39	PD	Set PROG REG A-SIGN toggle switch to on (up).																			
9.40	PD	Press and release RESET-MACHINE pushbutton/lamp.																			
9.41	PD	Set PROG REG A-SIGN toggle switch to off.																			
9.42	PD	Observe D1 through D6 lamps.					Not lit														
9.43	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																			
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Figure 7-11. Self-Test Program Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
9.44	PD	Observe PROGRAM ERROR lamp.								Not lit											
EXP	NA	Steps 9.45 through 9.47 substantiate that routine 1 of the test program can be run without errors. This routine checks HOP and transfer operations.																			
9.45	PD	Set PROG REG A-1 toggle switch to on.																			
9.46	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																			
9.47	PD	Observe PROGRAM ERROR lamp.								Not lit											
EXP	NA	Steps 9.48 through 9.51 substantiate that routine 2 of the test program can be run without errors. This routine checks the central processor internal operations.																			
9.48	PD	Set PROG REG A-1 toggle switch to off.																			
9.49	PD	Set PROG REG A-2 toggle switch to on.																			
9.50	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																			
9.51	PD	Observe PROGRAM ERROR lamp.								Not lit											
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
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Figure 7-11. Self-Test Program Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—																				
UNIT NAME:									UNIT NO.											
Step	Panel	Operation						Normal Indication	Data											
EXP	NA	Steps 9.52 through 9.55 substantiate that routine 3 of the test program can be run without errors. This routine tests CIO and PIO addressing, discrete outputs, discrete inputs, accumulator interface lines, and interrupt logic.																		
9.52	PD	Set PROG REG B-1 and PROG REG A-3 toggle switches to on.																		
9.53	PD	Set PROG REG A-2 toggle switch to off.																		
9.54	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																		
9.55	PD	Observe PROGRAM ERROR lamp.						Not lit												
EXP	NA	Steps 9.56 through 9.59 substantiate that routine 4 of the test program can be run without errors. This routine checks the typewriter control logic.																		
9.56	PD	Set PROG REG A-3 and PROG REG B-1 toggle switches to off.																		
9.57	PD	Set PROG REG A-4 toggle switch to on.																		
9.58	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																		
9.59	PD	Observe PROGRAM ERROR lamp.						Not lit												
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-11. Self-Test Program Checks (Sheet 7)

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INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:										UNIT NO.										
Step	Panel	Operation						Normal Indication	Data											
EXP	NA	Steps 9.60 through 9.63 substantiate that routine 5 of the test program can be run without errors. This routine checks the printer control logic.																		
9.60	PD	Set PROG REG A-4 toggle switch to off.																		
9.61	PD	Set PROG REG A-5 toggle switch to on.																		
9.62	PD	Observe that binary count indicated on P1 through P40 lamps is incrementing.																		
9.63	PD	Observe PORGRAM ERROR lamp.						Not lit												
EXP	NA	Steps 9.64 through 9.68 substantiate that routine 6 of the test program can be run without errors. This routine checks the plotter control logic.																		
9.64	PD	Set PROG REG A-5 toggle switch to off.																		
9.65	PD	Set PROG REG A-6 toggle switch to on and then back to off.																		
9.66		(This step deleted.)																		
9.67	PD	Observe PROGRAM ERROR lamp.						Not lit												
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER
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Figure 7-11. Self-Test Program Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation								Normal Indication	Data	
9.68	NA	Observe that pattern plotted is as shown on Illustration B.										
9.69		(This step deleted.)										
EXP	NA	Steps 9.70 through 9.96 substantiate that D1 through D6 lamps display correct information.										
9.70	MLDD	Observe ADDRESS COMPARE-INS lamp (press and release if not lit).								Lit		
9.71	MLDD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select the instruction-module, syllable, sector, and address listed directly after cal point 1 of routine 3 in the test program listing.										
9.72	MLDD	Set MODE CONTROL switch to PROG CYCLE-ADR HOLD.										
9.73	PD	Set PROG REG B-1 toggle switch to on.										
9.74	PD	Set PROG REG A-3 toggle switch to on.										
9.75	PD	Observe D1 lamp.								Lit		
9.76	PD	Observe D2 through D6 lamps.								Not lit		
9.77	MLDD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module syllable, sector, and address listed directly after Cal. Point 2 of routine 3 in the test program listing.										

Figure 7-11. Self-Test Program Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES -																				
UNIT NAME:														UNIT NO.						
Illustration B																				
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Figure 7-11. Self-Test Program Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES—																																																											
UNIT NAME:												UNIT NO.																																															
Step	Panel	Operation										Normal Indication	Data																																														
9.78	PD	Press and release ADVANCE pushbutton.																																																									
9.79	PD	Observe D2 lamp.										Lit																																															
9.80	PD	Observe D1, D3, D4, D5 and D6 lamps.										Not lit																																															
9.81	MLDD	Press and release INSTRUCTION ADDRESS pushbutton as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 3 of routine 3 in the test program listing.																																																									
9.82	PD	Press and release ADVANCE pushbutton.																																																									
9.83	PD	Observe D3 lamp.										Lit																																															
9.84	PD	Observe D1, D2, D4, D5 and D6 lamps.										Not lit																																															
9.85	MLDD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 4 of routine 3 in the test program listing.																																																									
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Figure 7-11. Self-Test Program Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation							Normal Indication	Data											
9.86	PD	Press and release ADVANCE pushbutton.																			
9.87	PD	Observe D4 lamp.							Lit												
9.88	PD	Observe D1, D2, D3, D5, and D6 lamps.							Not lit												
9.89	MLDD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 5 of routine 3 in the test program listing.																			
9.90	PD	Press and release ADVANCE pushbutton.																			
9.91	PD	Observe D5 lamp.							Lit												
9.92	PD	Observe D1, D2, D3, D4 and D6 lamps.							Not lit												
9.93	MLDD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 6 of routine 3, in the test program listing.																			
9.94	PD	Press and release ADVANCE pushbutton.																			
9.95	PD	Observe D6 lamp.							Lit												
9.96	PD	Observe D1, D2, D3, D4 and D5 lamps.							Not lit												
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Figure 7-11. Self-Test Program Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-									
UNIT NAME:							UNIT NO.		
Step	Panel	Operation				Normal Indication	Data		
EXP	NA	Steps 9.97 through 9.199 substantiate the manual interrupt controls are functioning properly. Ignore PROGRAM ERROR lamp.							
9.97		Press and release INHIBIT CONTROL pushbutton/ lamp.							
9.98		Observe INHIBIT CONTROL and B1 through B15 lamps.				Lit			
9.99		Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 7 of routine 3 in the test program listing.							
9.100		Press and release ADVANCE pushbutton.							
9.101		Observe I1 through I15 lamps.				Lit			
9.102		Observe HOPSAVE REG lamp (press and release if not lit).				Lit			
9.103	PD	Observe MEM ADD REG lamp (press and release if lit).				Not lit			
9.104	PD	Observe that the instruction and data-module syllable, sector, and address listed directly after Cal Point 8 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, IM, and DM lamps.							

Figure 7-11. Self-Test Program Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-														
UNIT NAME:										UNIT NO.				
Step	Panel	Operation							Normal Indication	Data				
9.105	PD	Press and release I1/B1 pushbutton/lamp.												
9.106	PD	Observe B1 lamp.							Not lit					
9.107	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 9 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.												
9.108	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.												
9.109	PD	Observe B1 through B15 lamps.							Lit					
9.110	PD	Press and release ADVANCE pushbutton.												
9.111	PD	Press and release I2/B2 pushbutton/lamp.												
9.112	PD	Observe B2 lamp.							Not lit					
9.113	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 10 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.												
9.114	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.												
9.115	PD	Observe B1 through B15 lamps.							Lit					
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Figure 7-11. Self-Test Program Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-																																																						
UNIT NAME:									UNIT NO.																																													
Step	Panel	Operation					Normal Indication	Data																																														
9.116	PD	Press and release ADVANCE pushbutton.																																																				
9.117	PD	Press and release I3/B3 pushbutton/lamp.																																																				
9.118	PD	Observe B3 lamp.					Not lit																																															
9.119	MLDD	Observe that instruction-module, syllable, sector, and address listed directly after Cal Point 11 of routine 3 in the test program listing are displayed by the INSTRUCTION ADDRESS COMPUTER lamps.																																																				
9.120	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																																																				
9.121	PD	Observe B1 through B15 lamps.					Lit																																															
9.122	PD	Press and release ADVANCE pushbutton.																																																				
9.123	PD	Press and release I4/B4 pushbutton/lamp.																																																				
9.124	PD	Observe B4 lamp.					Not lit																																															
9.125	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 12 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																																																				
9.126	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																																																				
<table border="1"> <tr> <td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>I</td><td>J</td><td>K</td><td>L</td><td>M</td><td>N</td><td>O</td><td>P</td><td>Q</td><td>R</td><td>PAGE</td><td></td><td>PAGES</td><td>NUMBER</td> </tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>of</td><td></td><td>A-</td> </tr> </table>											A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE		PAGES	NUMBER																				of		A-
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Figure 7-11. Self-Test Program Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-											
UNIT NAME:									UNIT NO.		
Step	Panel	Operation					Normal Indication	Data			
9.127	PD	Observe B1 through B15 lamps.					Lit				
9.128	PD	Press and release ADVANCE push-button.									
9.129	PD	Press and release I5/B5 pushbutton/lamp.									
9.130	PD	Observe B5 lamp.					Not lit				
9.131	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 13 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.									
9.132	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.									
9.133	PD	Observe B1 through B15 lamps.					Lit				
9.134	PD	Press and release ADVANCE push-button.									
9.135	PD	Press and release I6/B6 pushbutton/lamp.									
9.136	PD	Observe B6 lamp.					Not lit				
9.137	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 14 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM and IM lamps.									
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Figure 7-11. Self-Test Program Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES--												
UNIT NAME:										UNIT NO.		
Step	Panel	Operation							Normal Indication	Data		
9.138	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.										
9.139	PD	Observe B1 through B15 lamps.							Lit			
9.140	PD	Press and release ADVANCE pushbutton.										
9.141	PD	Press and release I7/B7 pushbutton/lamp.										
9.142	PD	Observe B7 lamp.							Not lit			
9.143	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 15 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.										
9.144	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.										
9.145	PD	Observe B1 through B15 lamps.							Lit			
9.146	PD	Press and release ADVANCE pushbutton.										
9.147	PD	Press and release I8/B8 pushbutton/lamp.										
9.148	PD	Observe B8 lamp.							Not lit			
9.149	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 16 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.										
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Figure 7-11. Self-Test Program Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES-																				
UNIT NAME:							UNIT NO.													
Step	Panel	Operation					Normal Indication	Data												
9.150	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																		
9.151	PD	Observe B1 through B15 lamps.					Lit													
9.152	PD	Press and release ADVANCE pushbutton.																		
9.153	PD	Press and release I9/B9 pushbutton/lamp.																		
9.154	PD	Observe B9 lamp.					Not lit													
9.155	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 17 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																		
9.156	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																		
9.157	PD	Observe B1 through B15 lamps.					Lit													
9.158	PD	Press and release ADVANCE pushbutton.																		
9.159	PD	Press and release I10/B10 pushbutton/lamp.																		
9.160	PD	Observe B10 lamp.					Not lit													
9.161	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 18 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																		
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Figure 7-11. Self-Test Program Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES-																																																				
UNIT NAME:									UNIT NO.																																											
Step	Panel	Operation					Normal Indication	Data																																												
9.162	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																																																		
9.163	PD	Observe B1 through B15 lamps.					Lit																																													
9.164	PD	Press and release ADVANCE pushbutton.																																																		
9.165	PD	Press and release I11/B11 pushbutton/lamp.																																																		
9.166	PD	Observe B11 lamp.					Not lit																																													
9.167	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 19 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																																																		
9.168	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																																																		
9.169	PD	Observe B1 through B15 lamps.					Lit																																													
9.170	PD	Press and release ADVANCE pushbutton.																																																		
9.171	PD	Press and release I12/B12 pushbutton/lamp.																																																		
9.172	PD	Observe B12 lamp.					Not lit																																													
9.173	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 20 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																																																		
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>I</td><td>J</td><td>K</td><td>L</td><td>M</td><td>N</td><td>O</td><td>P</td><td>Q</td><td>R</td><td>PAGE</td><td>PAGES</td><td>NUMBER</td> </tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>of</td><td>A-</td> </tr> </table>											A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER																				of	A-
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Figure 7-11. Self-Test Program Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES-																					
UNIT NAME:										UNIT NO.											
Step	Panel	Operation								Normal Indication	Data										
9.174	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																			
9.175	PD	Observe B1 through B15 lamps.								Lit											
9.176	PD	Press and release ADVANCE pushbutton.																			
9.177	PD	Press and release I13/B13 pushbutton/lamp.																			
9.178	PD	Observe B13 lamp.								Not lit											
9.179	PD	Observe that instruction and data-module, syllable, sector, and address listed for Cal Point 21 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																			
9.180	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.																			
9.181	PD	Observe B1 through B15 lamps.								Lit											
9.182	PD	Press and release ADVANCE pushbutton.																			
9.183	PD	Press and release I14/B14 pushbutton/lamp.																			
9.184	PD	Observe B14 lamp.								Not lit											
9.185	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 22 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.																			
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
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Figure 7-11. Self-Test Program Checks (Sheet 20)

INTERNATIONAL BUSINESS MACHINES-													
UNIT NAME:											UNIT NO.		
Step	Panel	Operation								Normal Indication	Data		
9.186	PD	Press and release INHIBIT CTRL pushbutton/lamp twice.											
9.187	PD	Observe B1 through B15 lamps.								Lit			
9.188	PD	Press and release ADVANCE pushbutton.											
9.189	PD	Press and release I15/B15 pushbutton/lamp.											
9.190	PD	Observe B15 lamp.								Not lit			
9.191	PD	Observe that instruction and data-module, syllable, sector, and address listed directly after Cal Point 23 of routine 3 in the test program listing are displayed by the MEMORY ADDRESS, SYLLABLE, SECTOR, DM, and IM lamps.											
9.192	PD	Press and release INSTRUCTION ADDRESS pushbuttons as necessary to select instruction-module, syllable, sector, and address listed directly after Cal Point 24 of routine 3 in the test program listing.											
9.193	PD	Press and release INHIBIT CTRL pushbutton/lamp.											
9.194	PD	Observe INHIBIT CTRL lamp.								Not lit			
9.195	PD	Press and release ADVANCE pushbutton.											
9.196		(This step deleted.)											

Figure 7-11. Self-Test Program Checks (Sheet 21)

INTERNATIONAL BUSINESS MACHINES-																																																						
UNIT NAME:										UNIT NO.																																												
Step	Panel	Operation								Normal Indication	Data																																											
9.197		(This step deleted.)																																																				
9.198	PD	Press and release I16 pushbutton/lamp.																																																				
9.199	MLDD	Observe that instruction-module, syllable, sector, and address listed for Cal Point 24 of routine 3 in the test program listing are displayed by the INSTRUCTION ADDRESS COMPUTER lamps.																																																				
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td><td>G</td><td>H</td><td>I</td><td>J</td><td>K</td><td>L</td><td>M</td><td>N</td><td>O</td><td>P</td><td>Q</td><td>R</td><td>PAGE</td><td>PAGES</td><td>NUMBER</td> </tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>OF</td><td></td><td>A-</td> </tr> </table>													A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	PAGES	NUMBER																			OF		A-
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Figure 7-11. Self-Test Program Checks (Sheet 22)

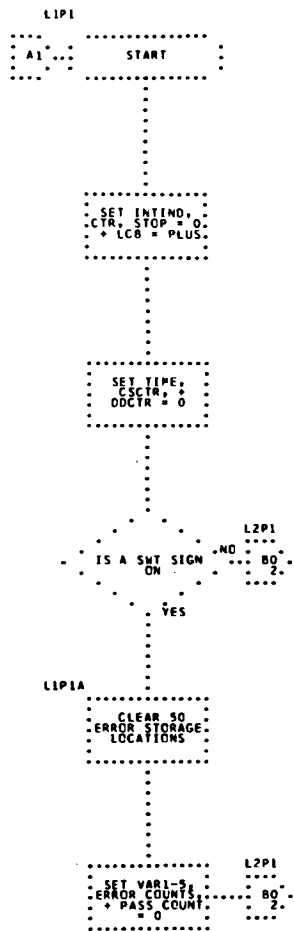


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 1 of 62)

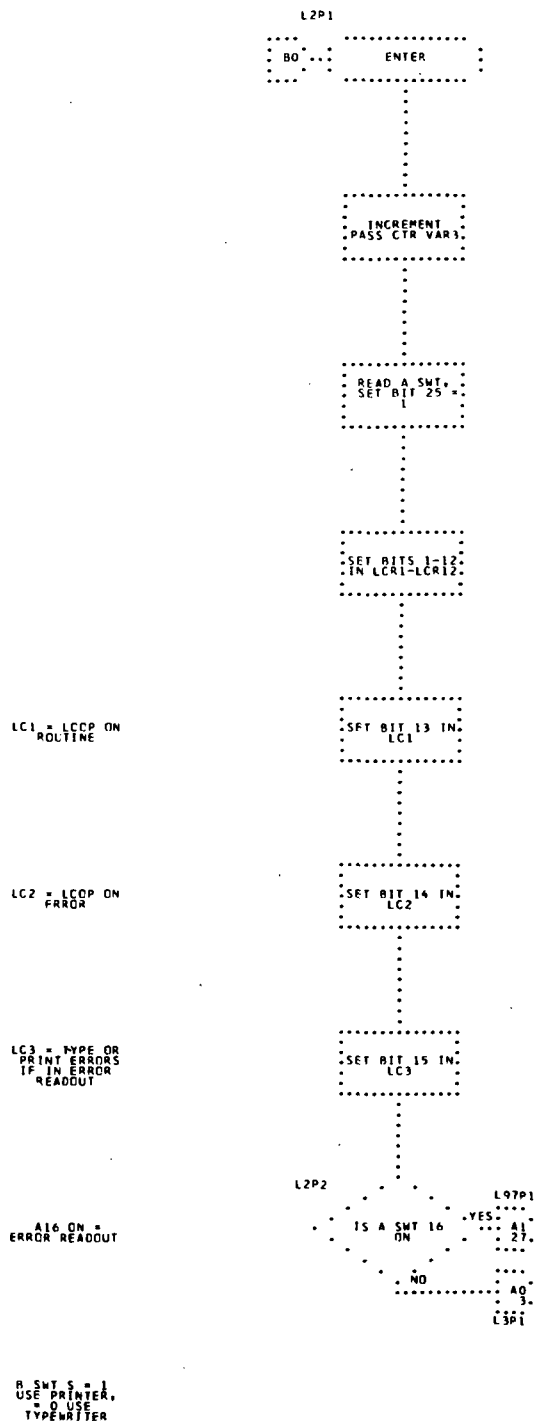


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 2)

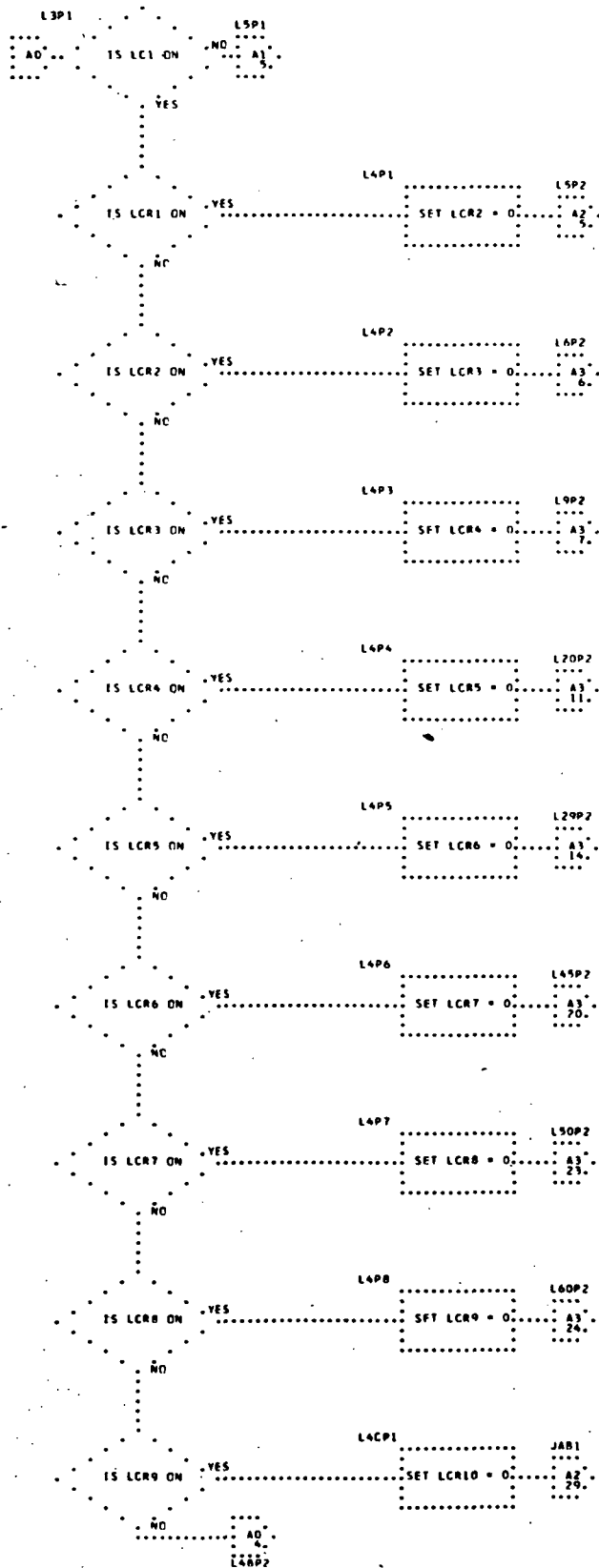


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 3)

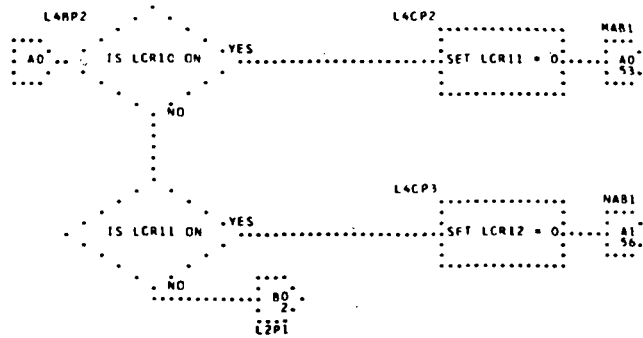


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 4)

ROUTINE 1 *
 CHECK MDP *
 TRANSFERS

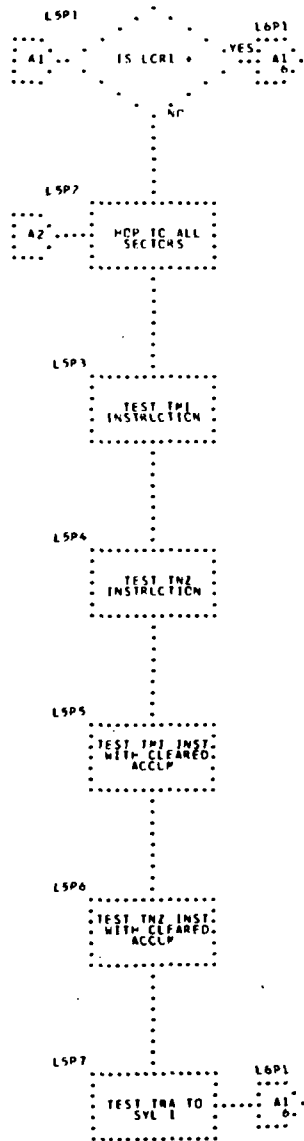


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 5)

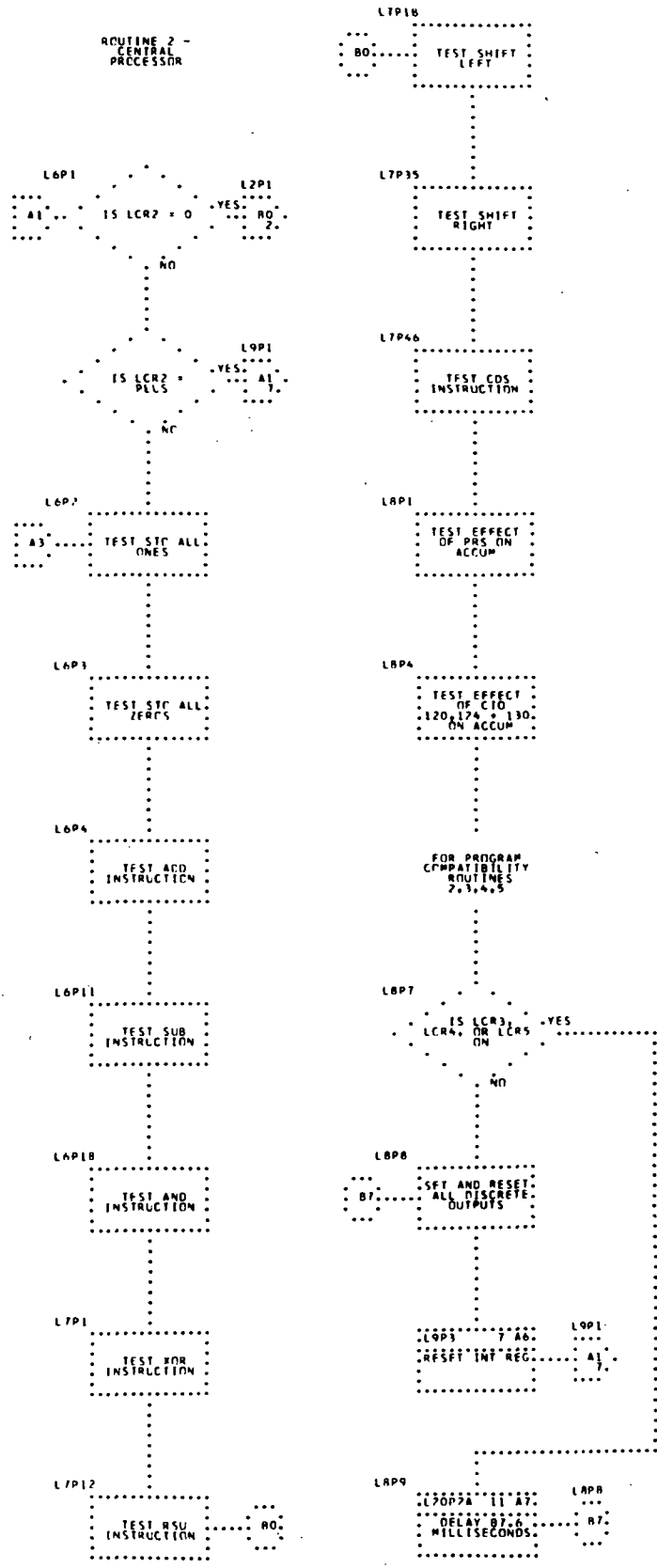


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 6)

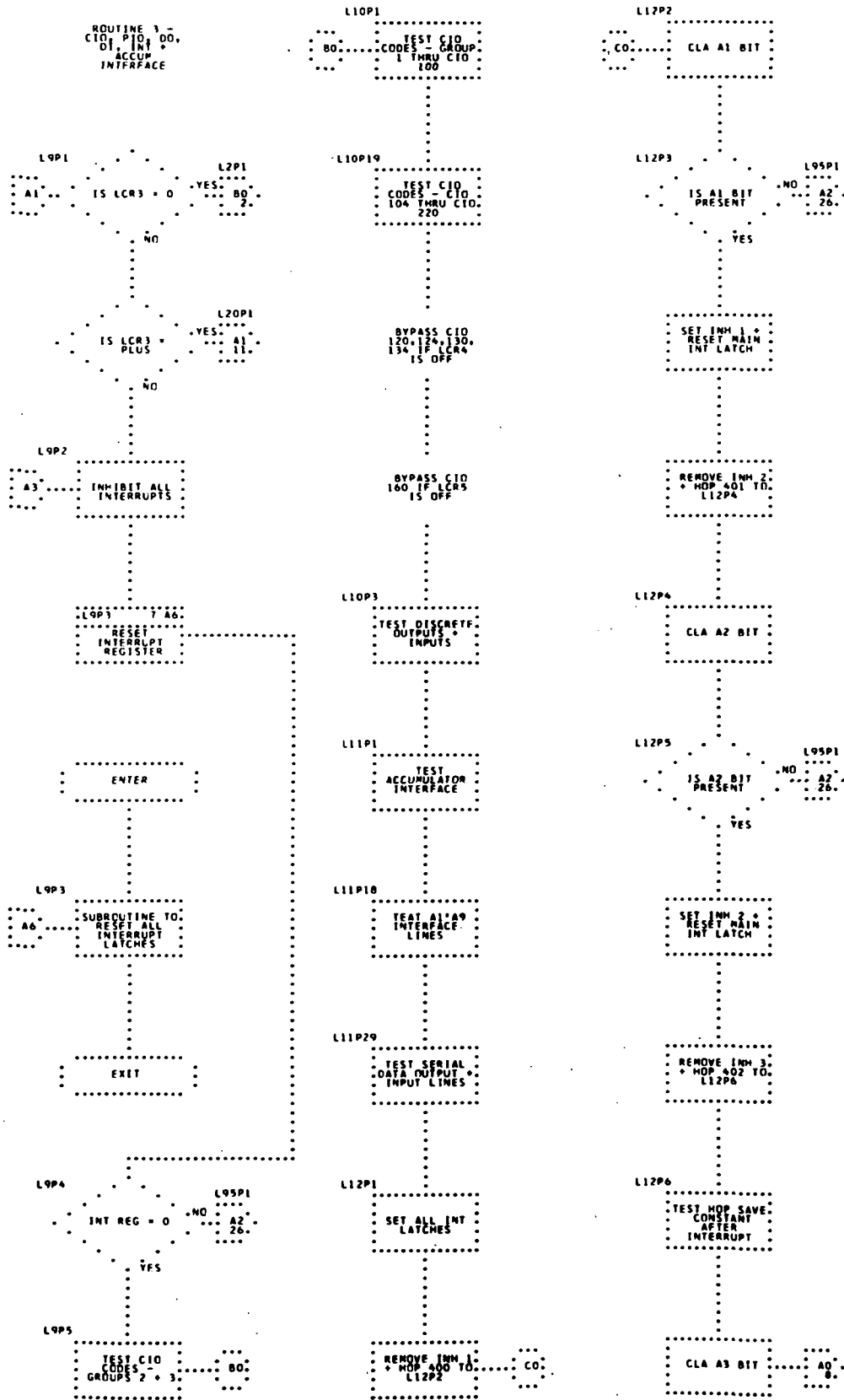


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 7)

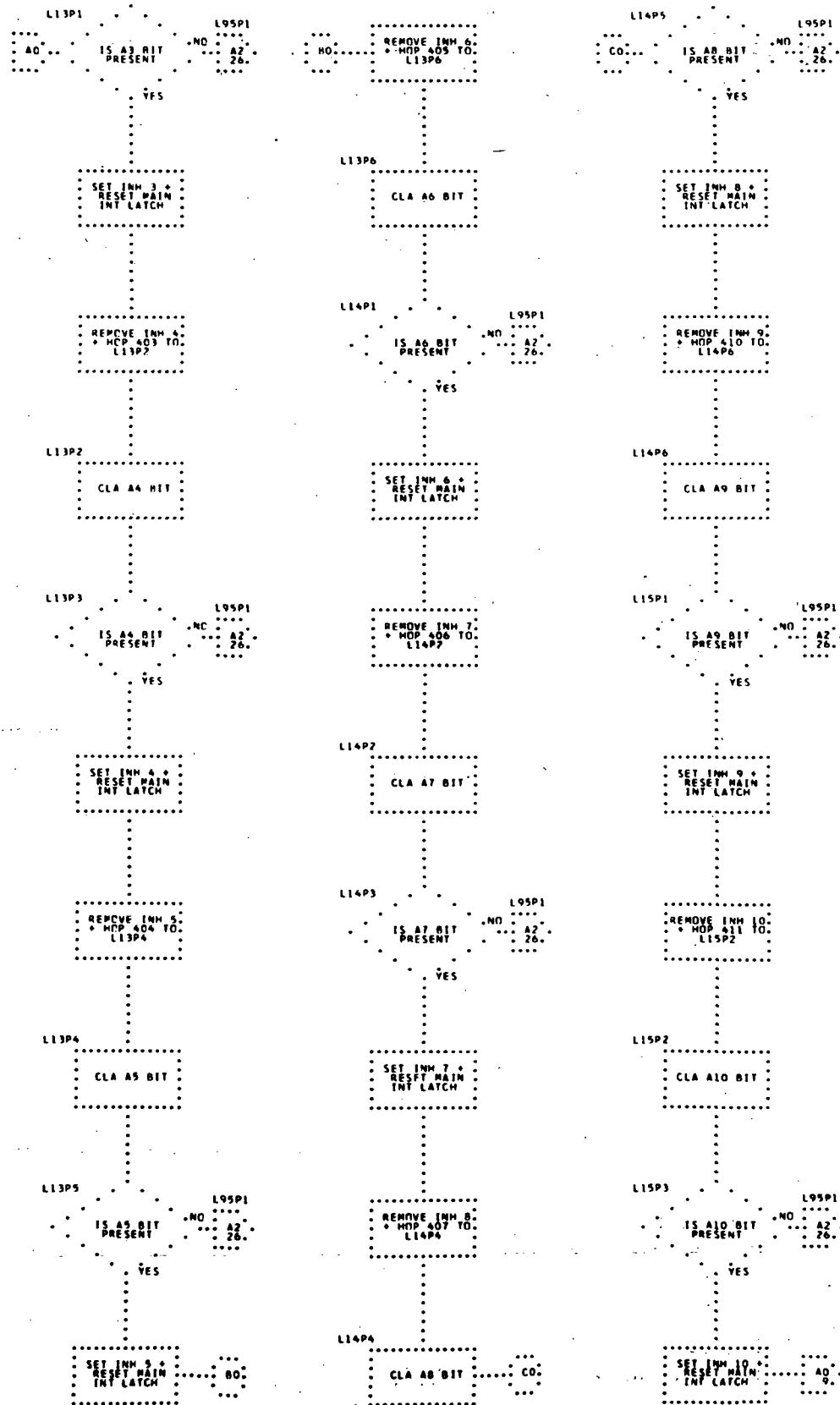


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 8)

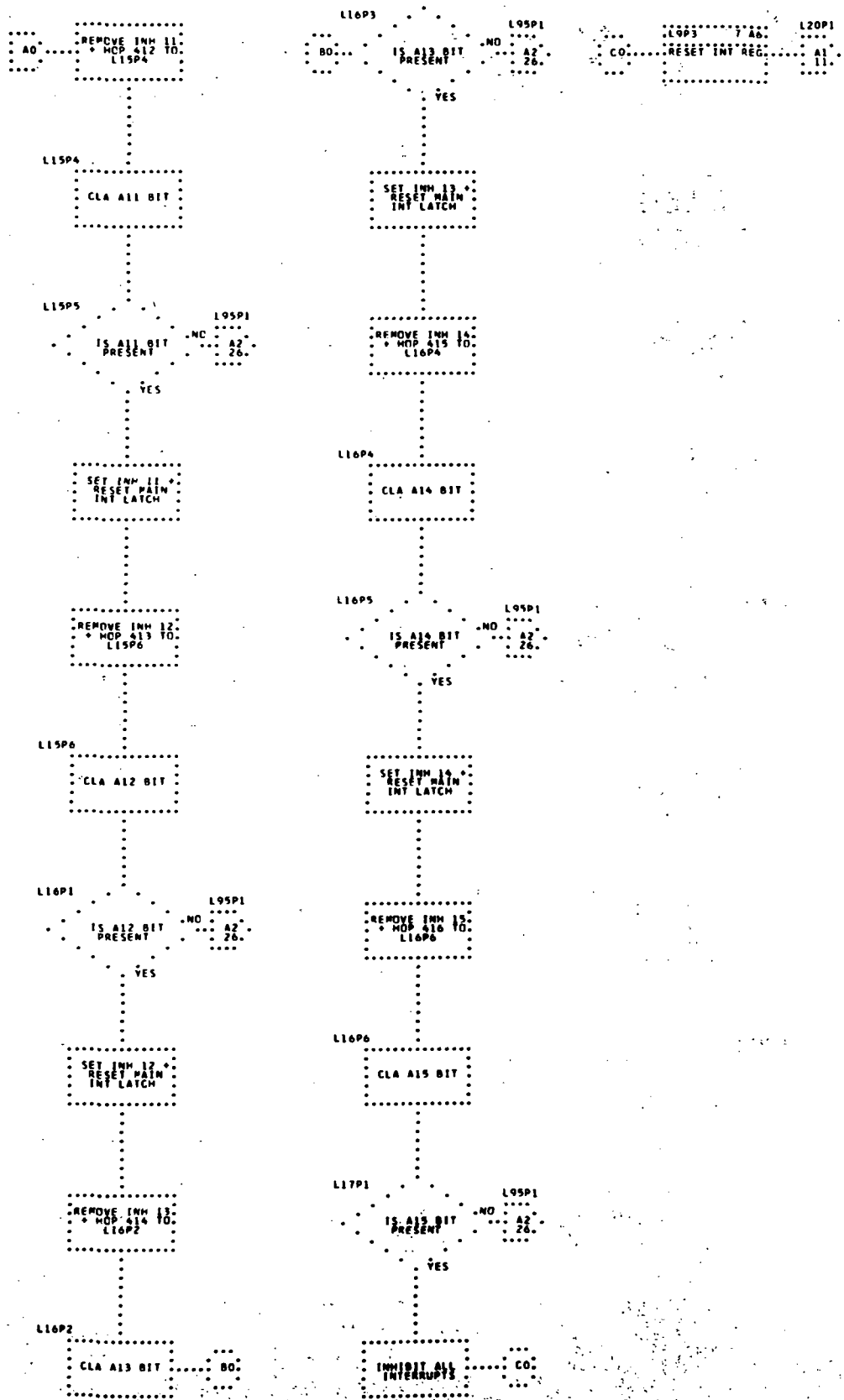


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 9)

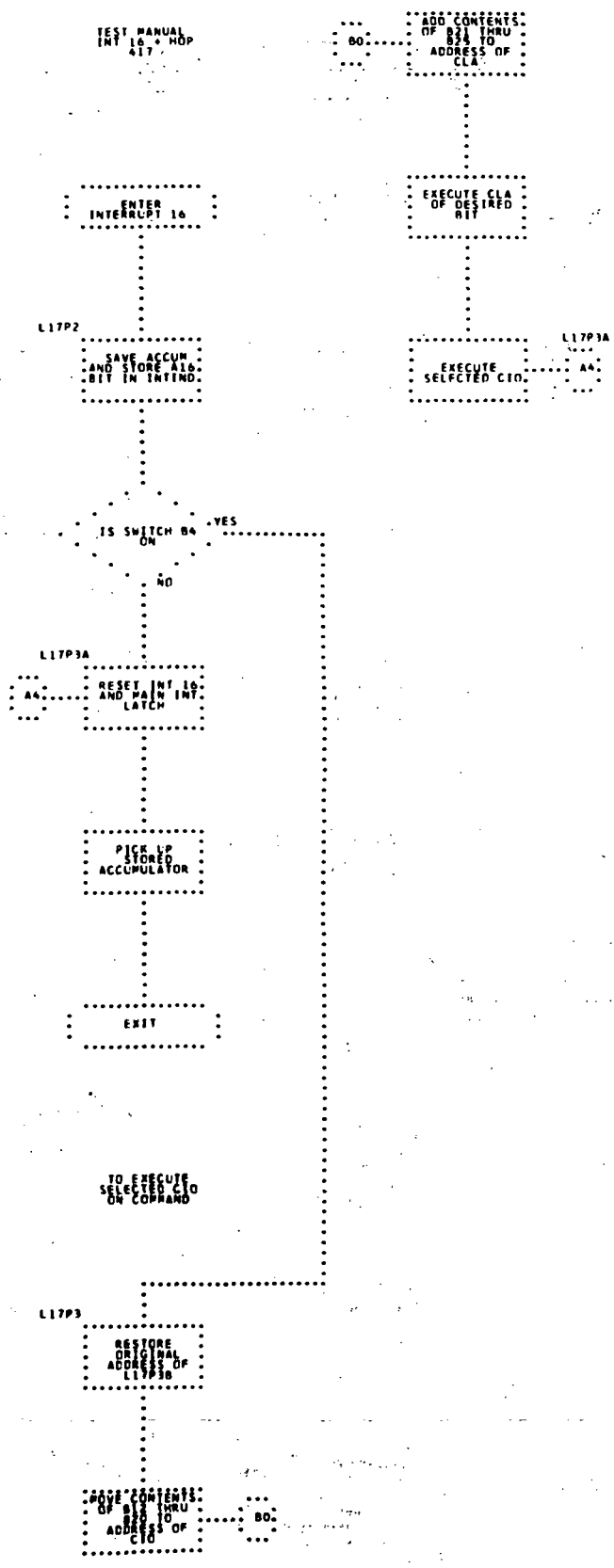


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 10)

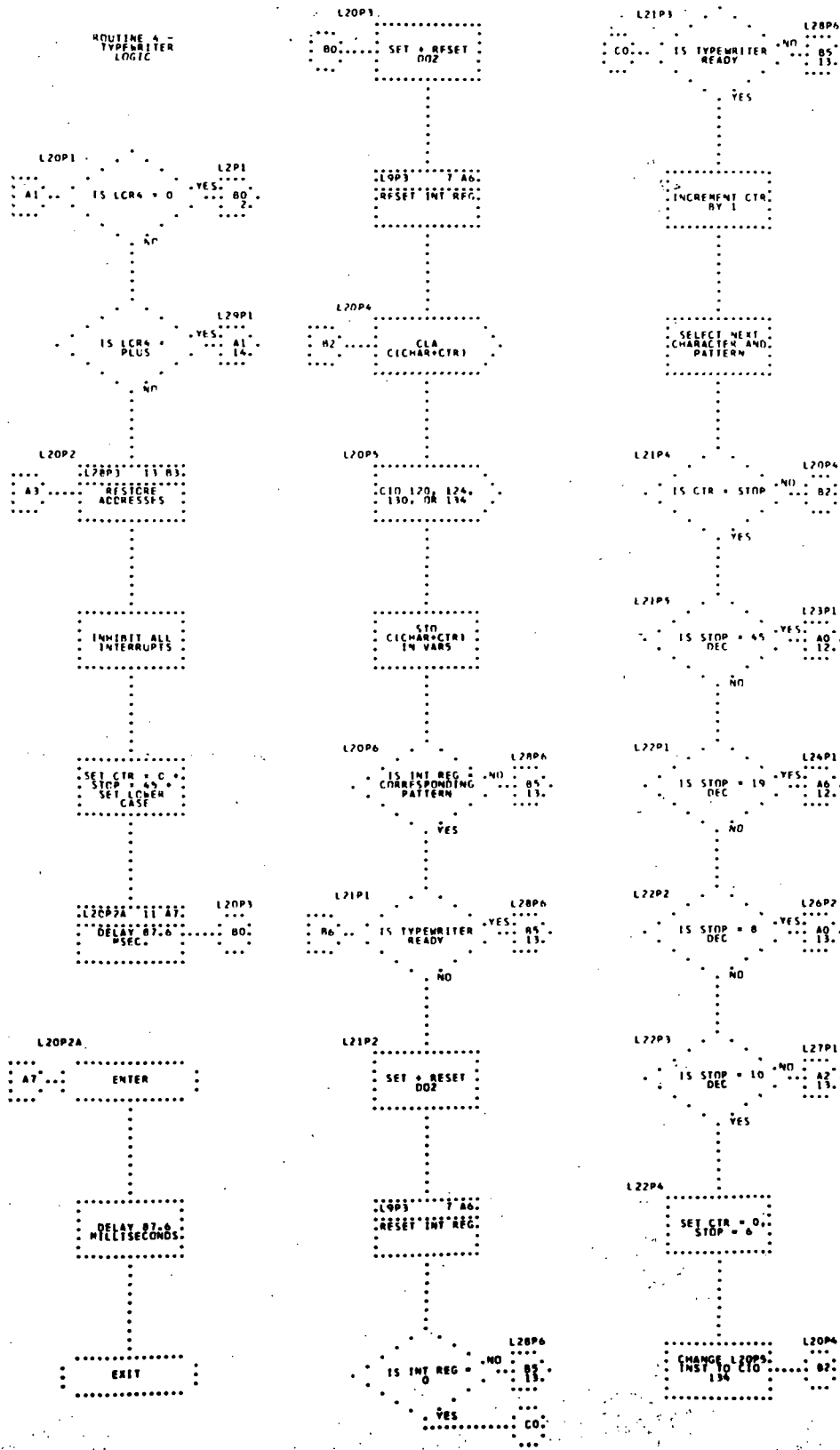


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 11)

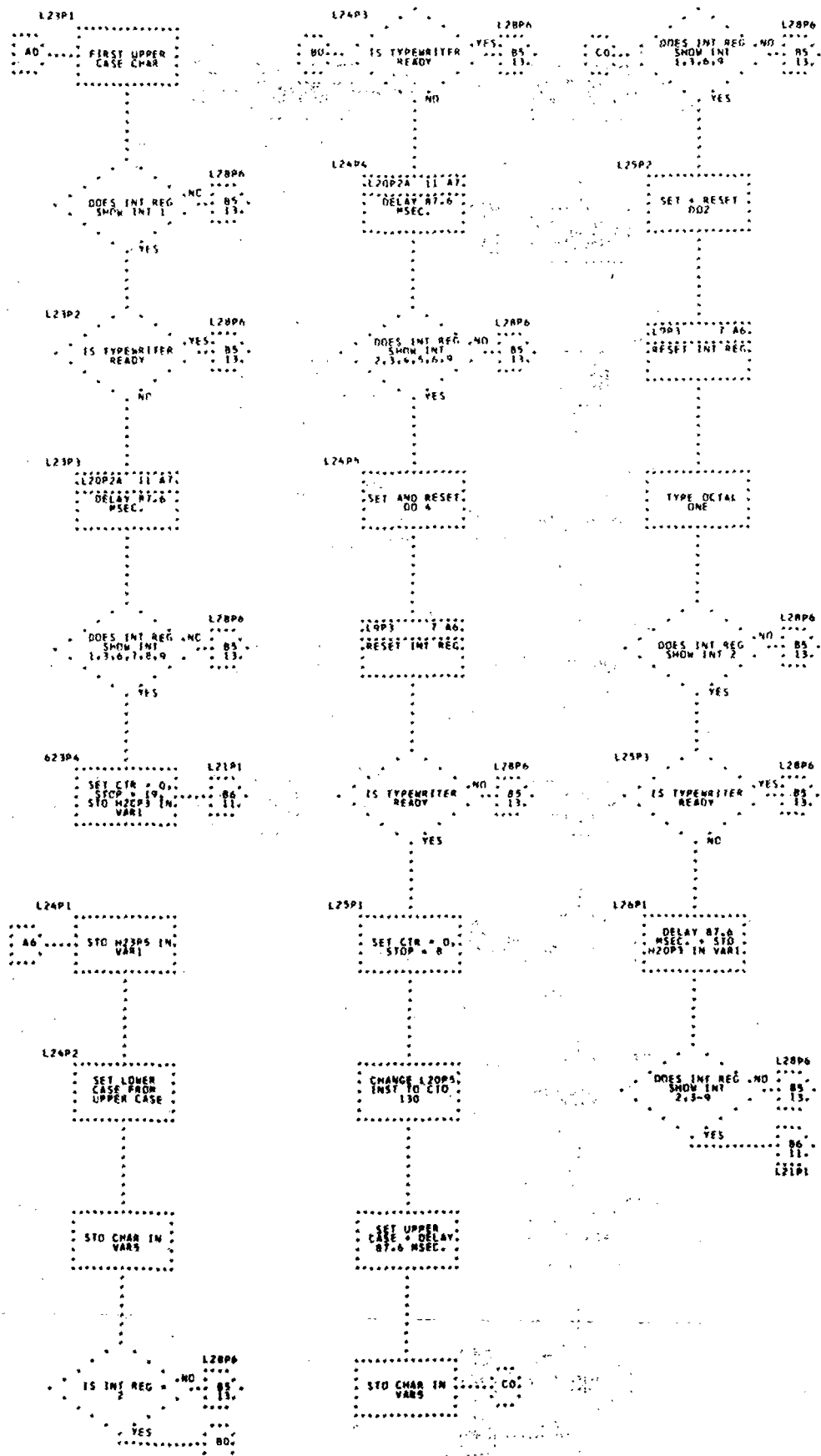


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 12)

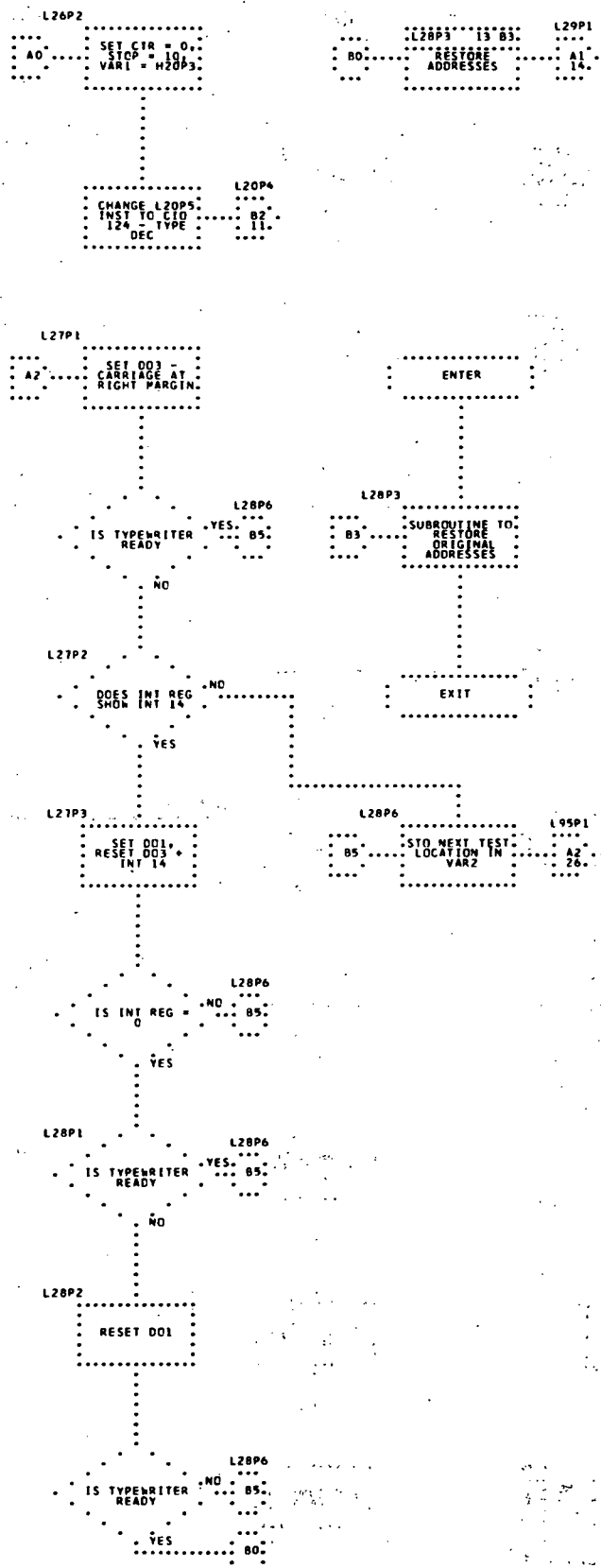


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 13)

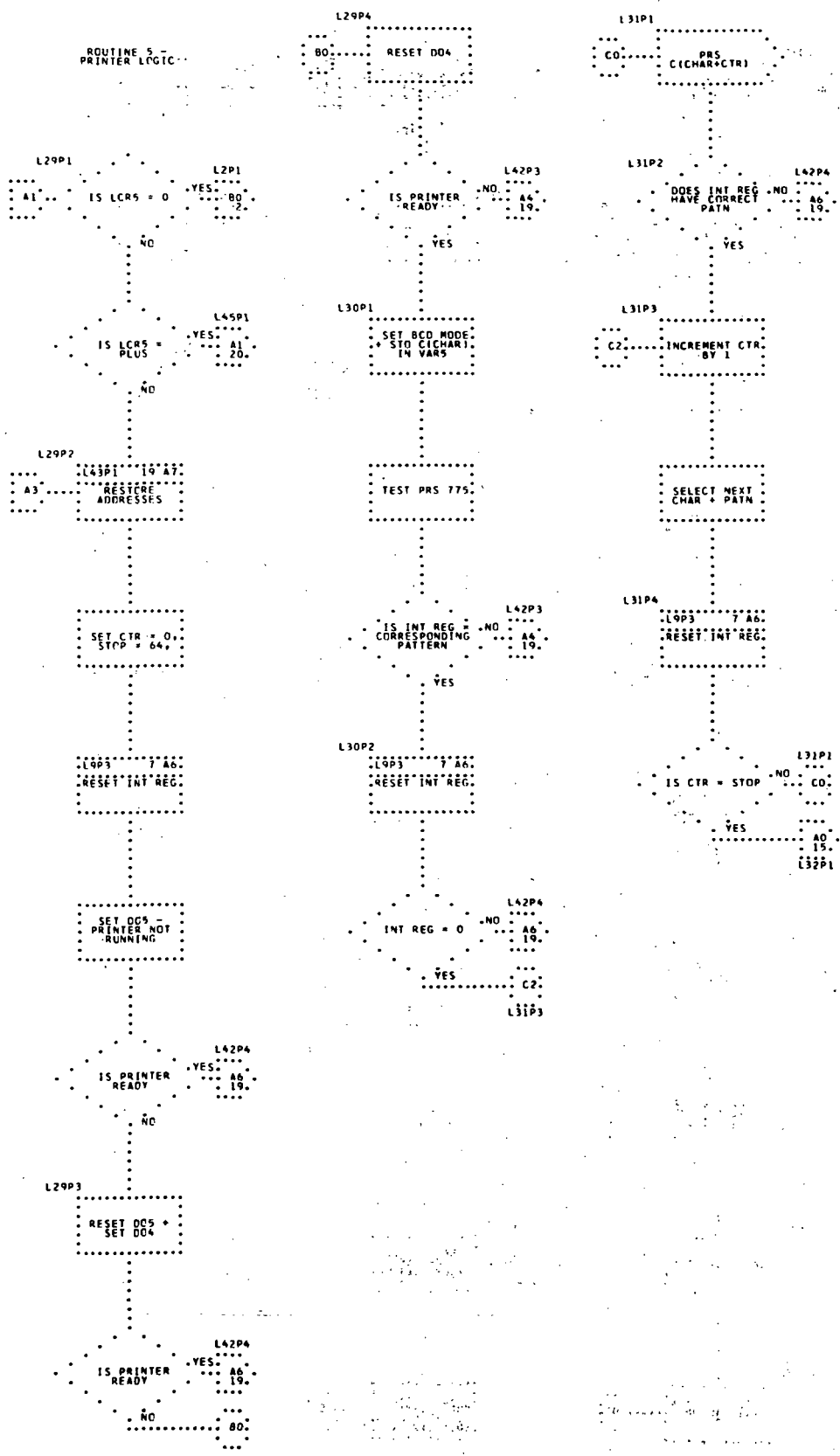


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 14)

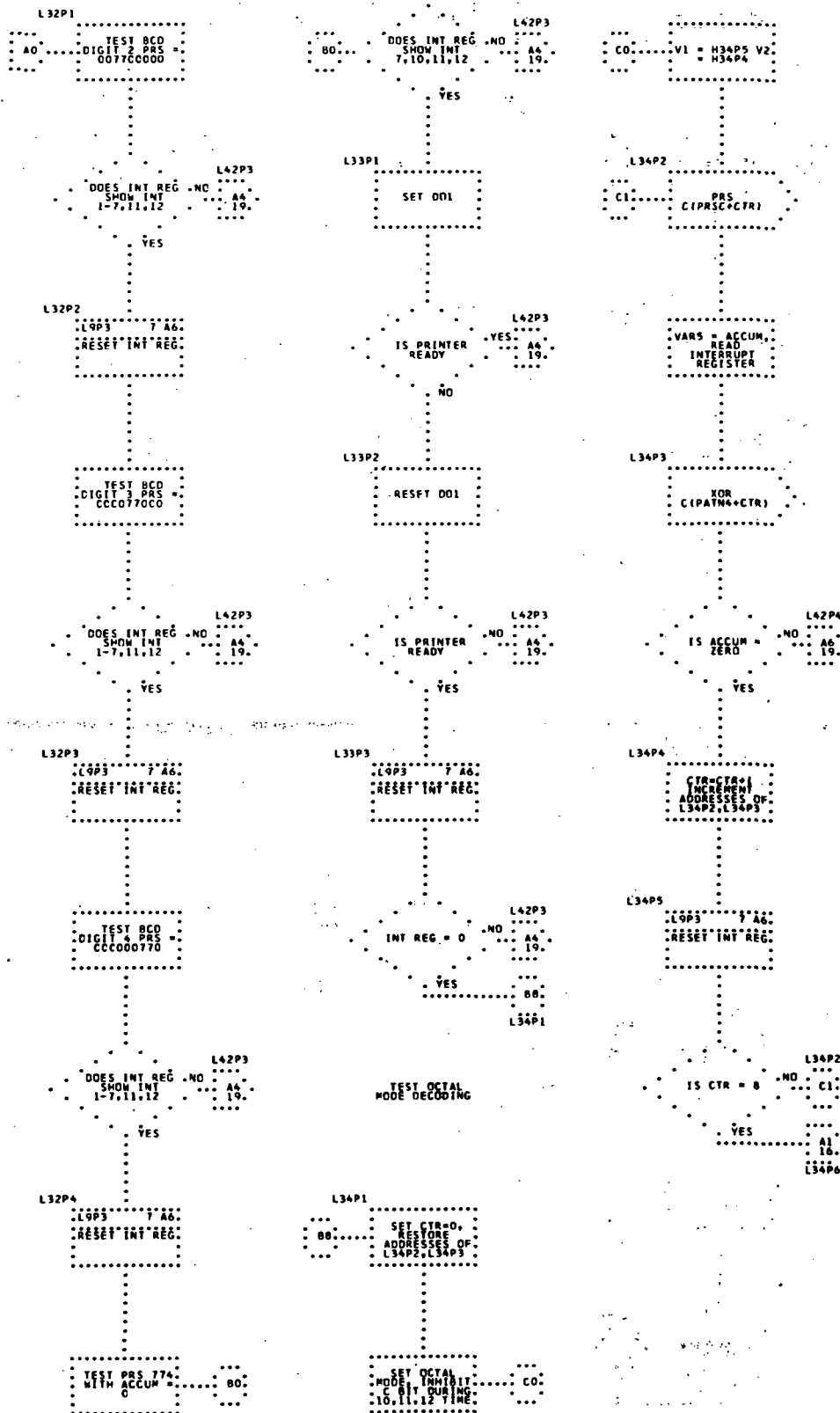


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 15)

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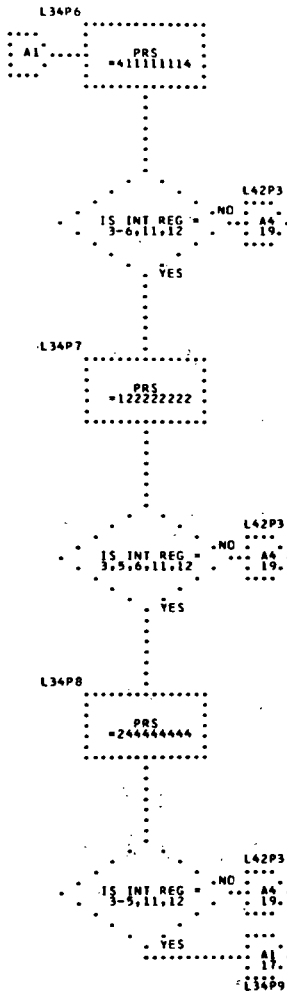


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 16)

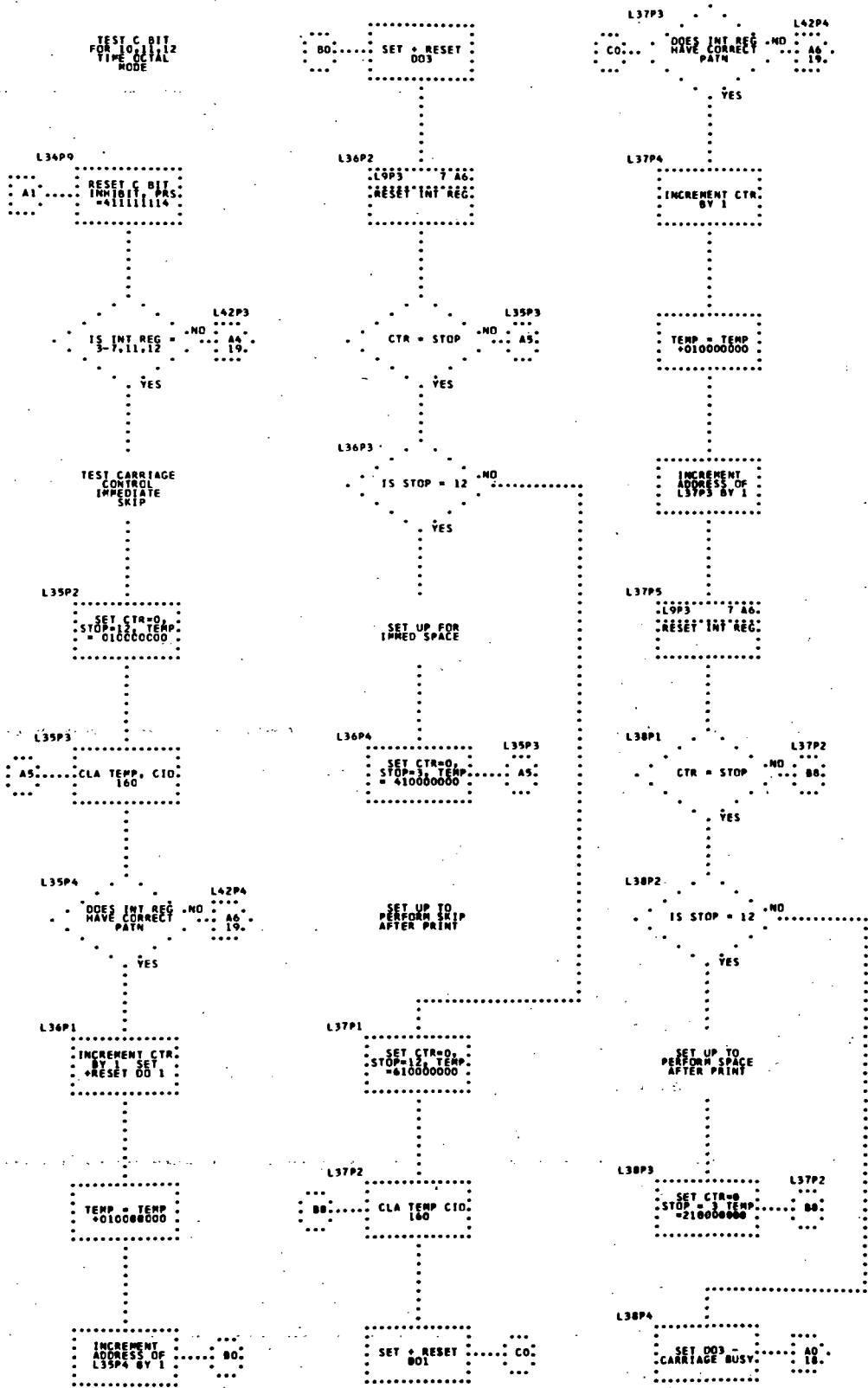


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 17)

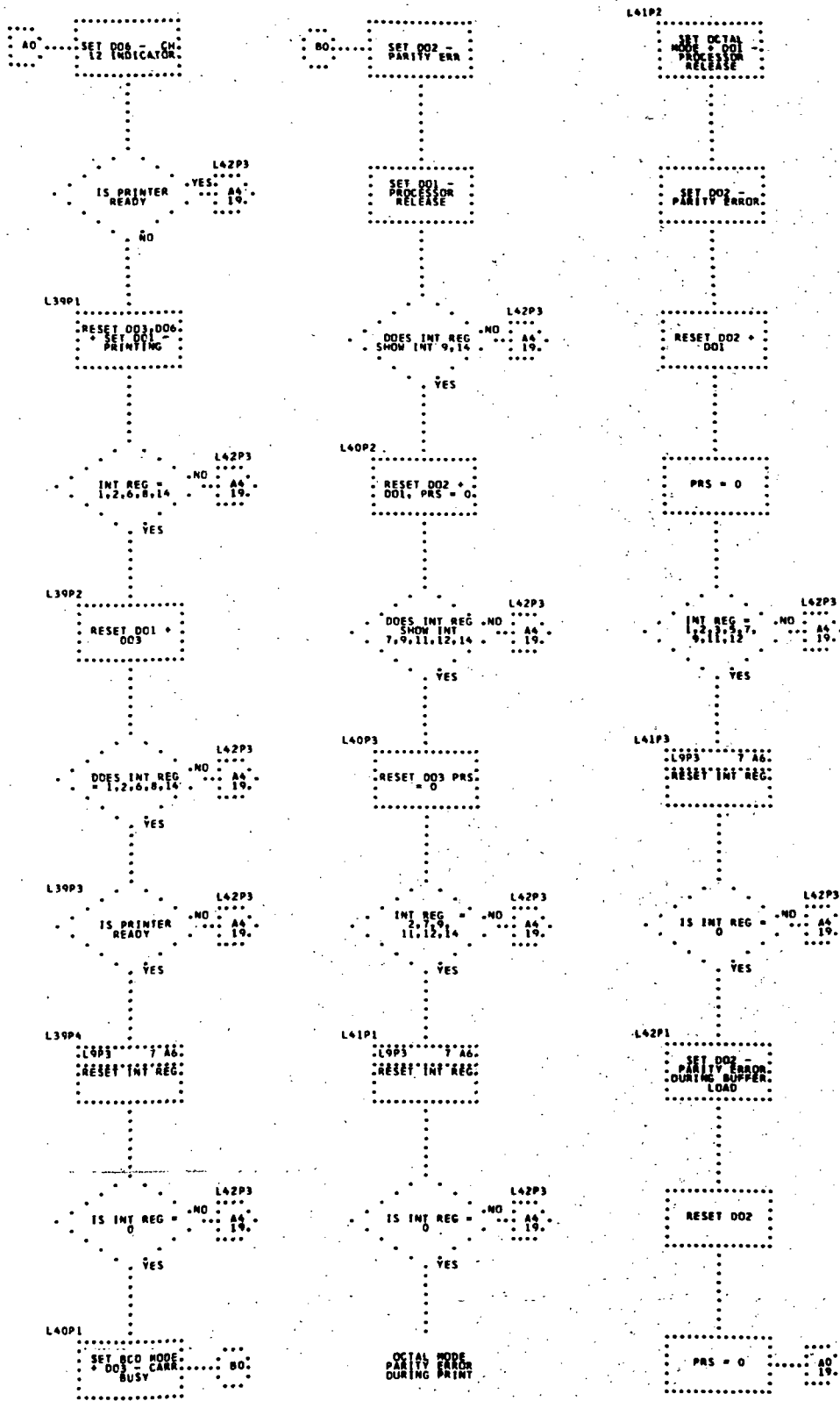


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 18)

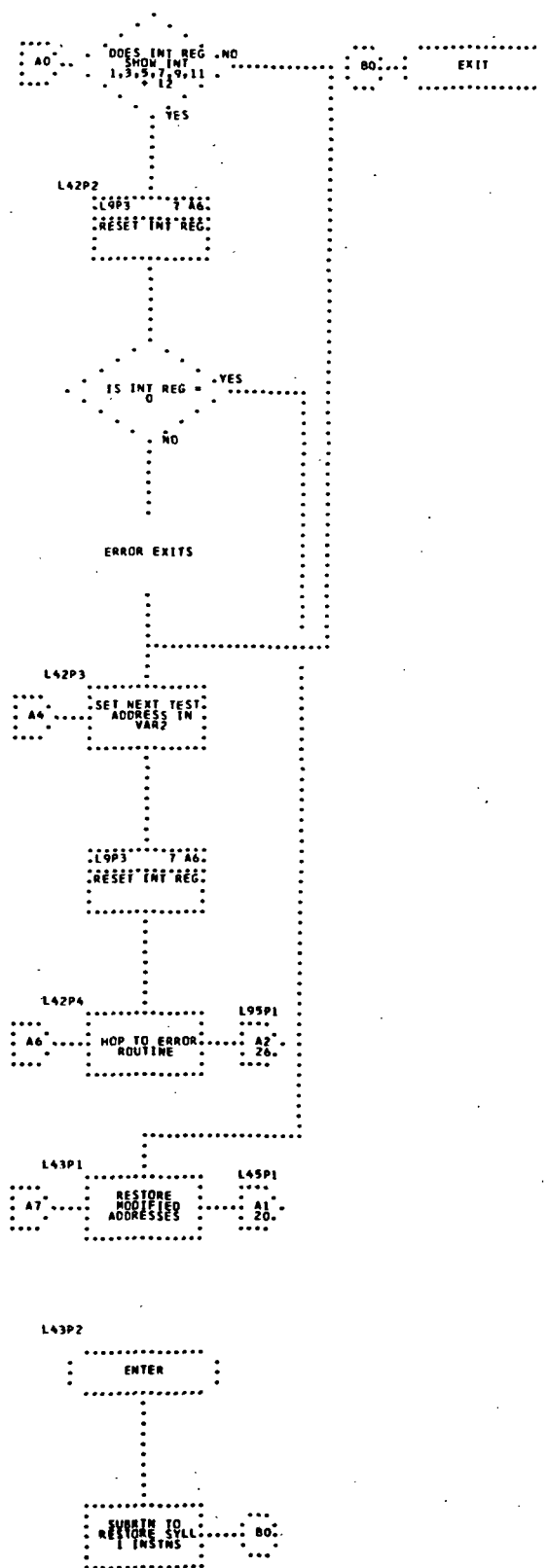


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 19)

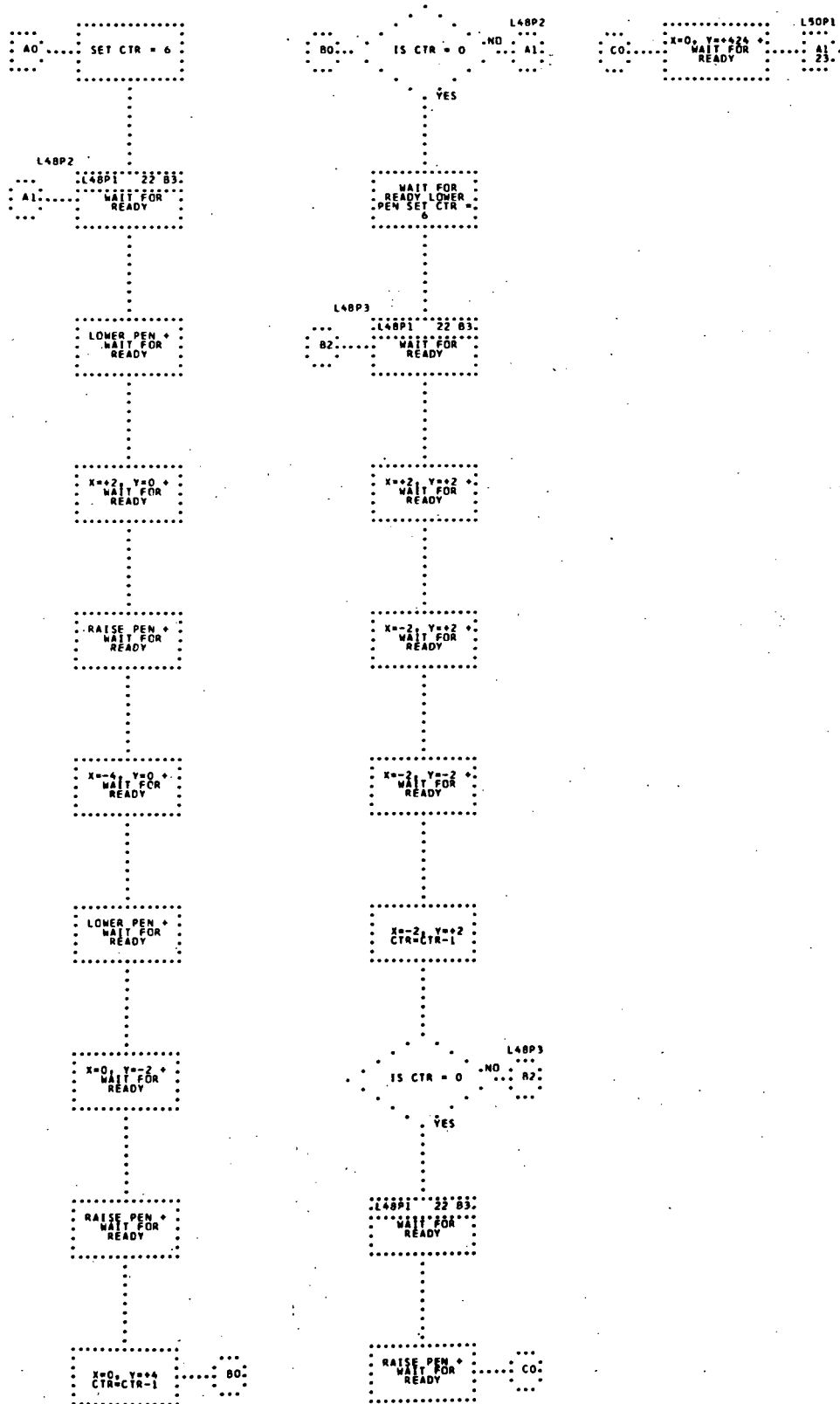


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 21)

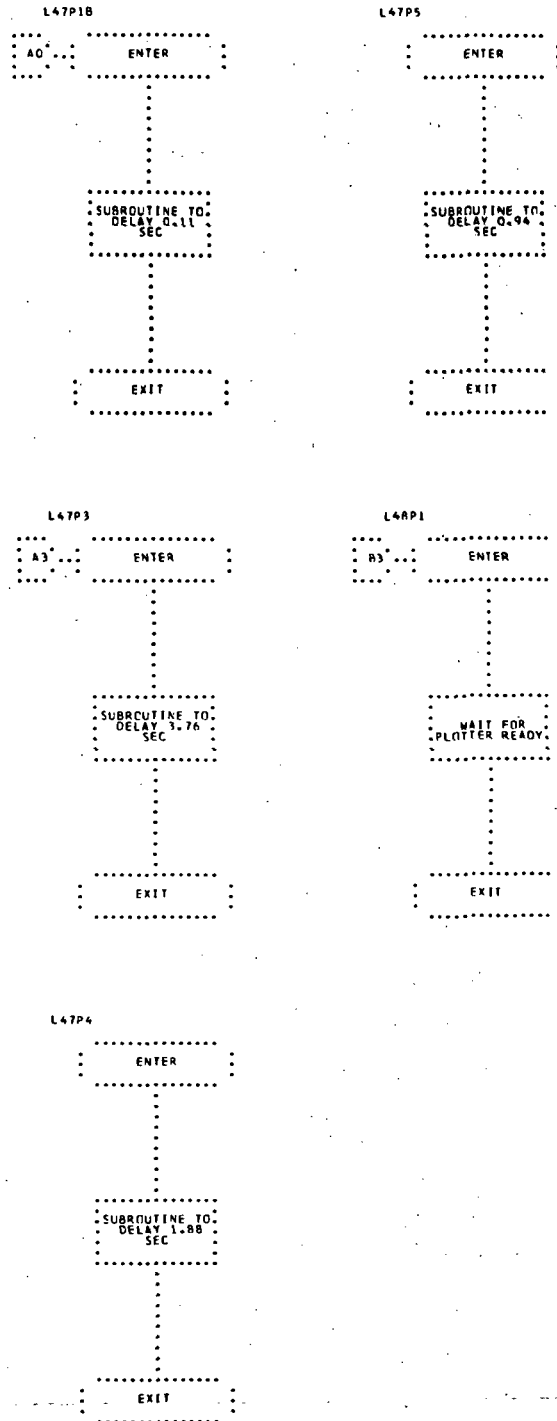


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 22)

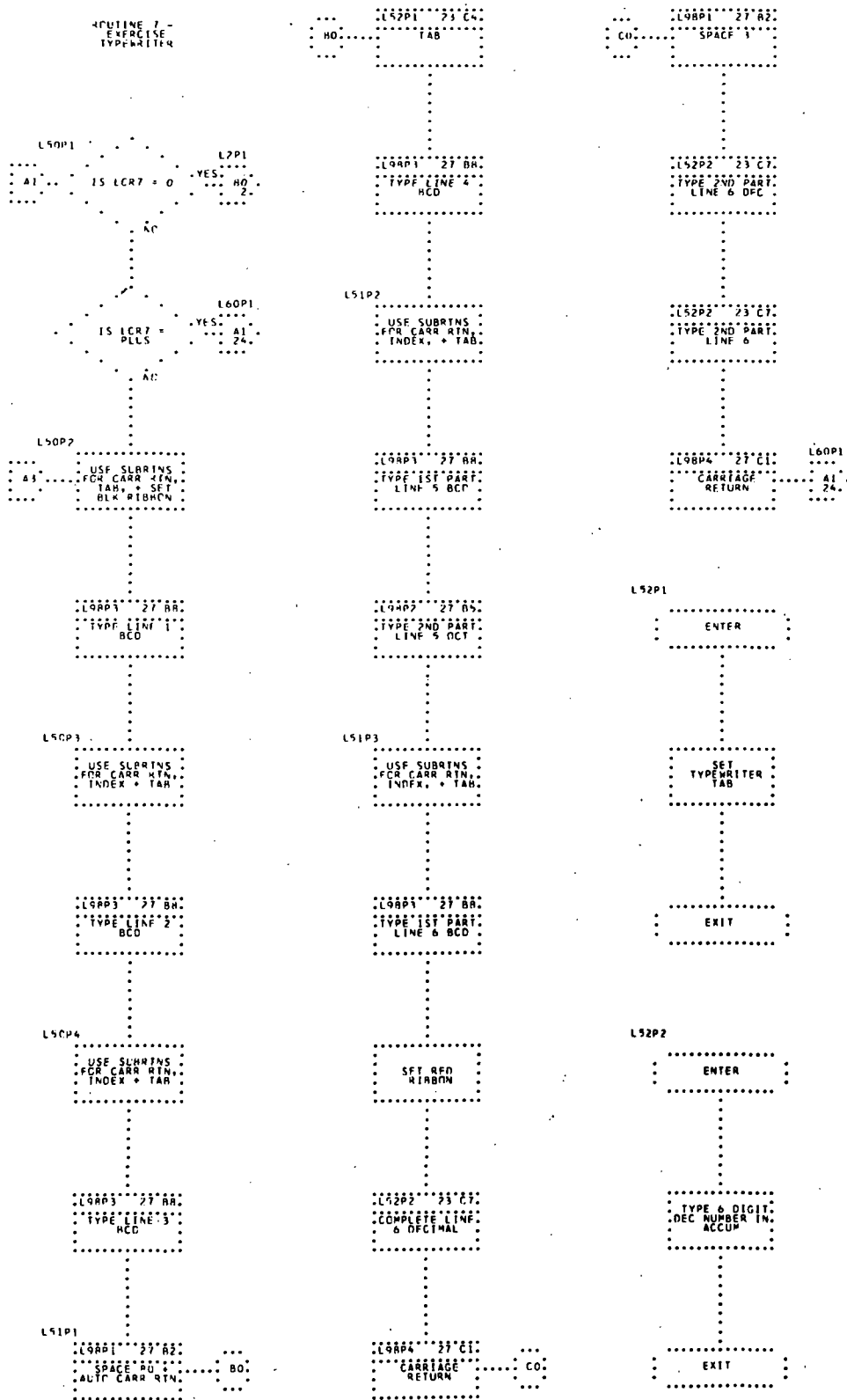


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 23)

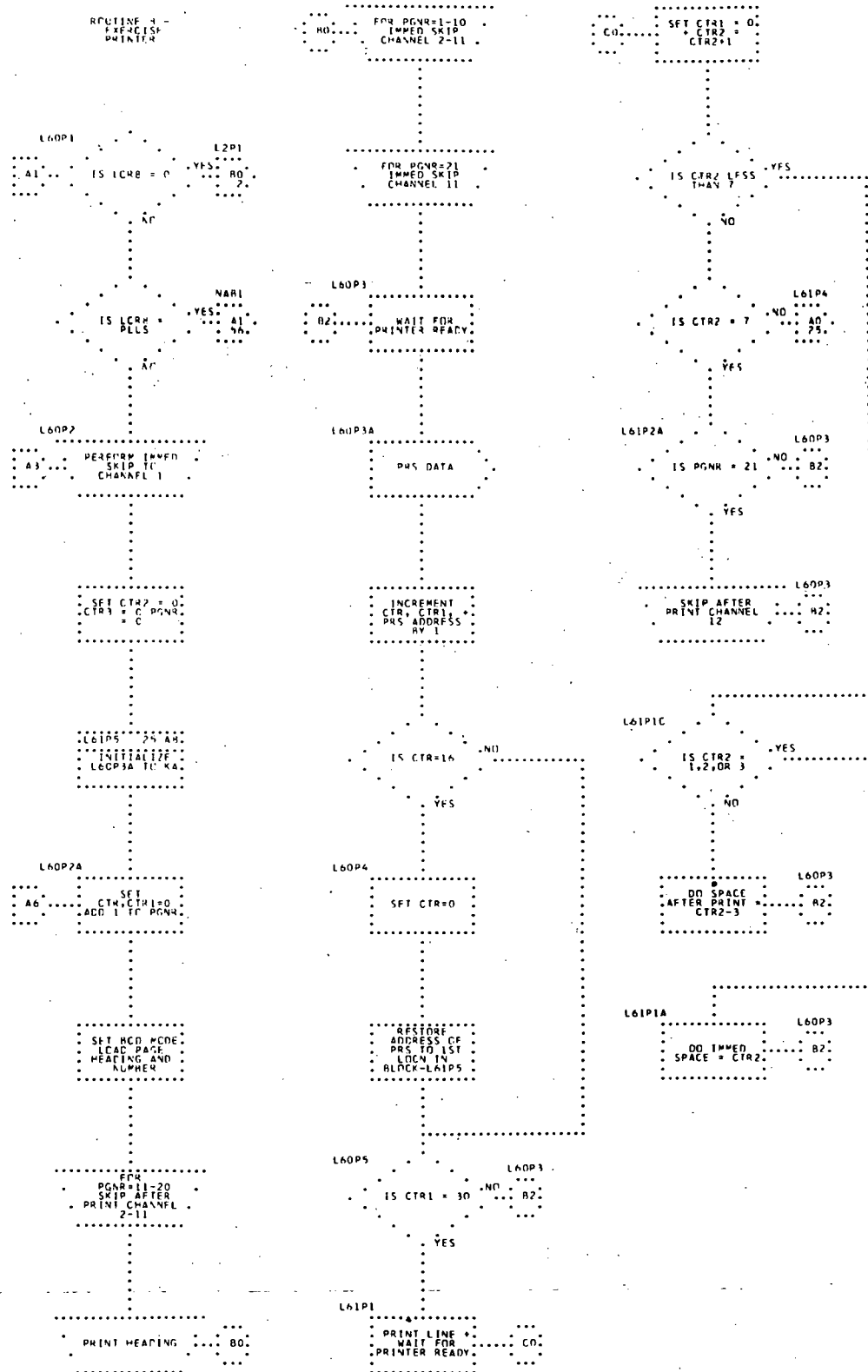


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 24)

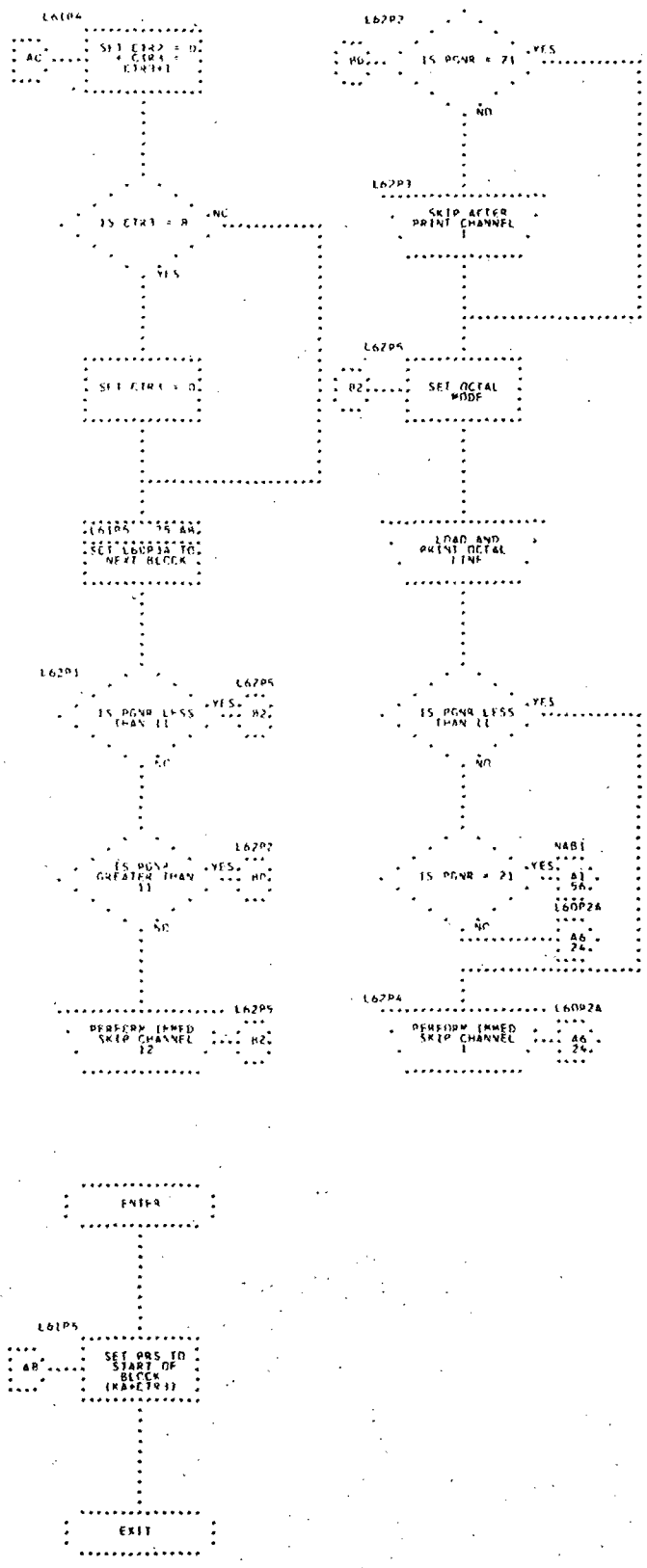


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 25)

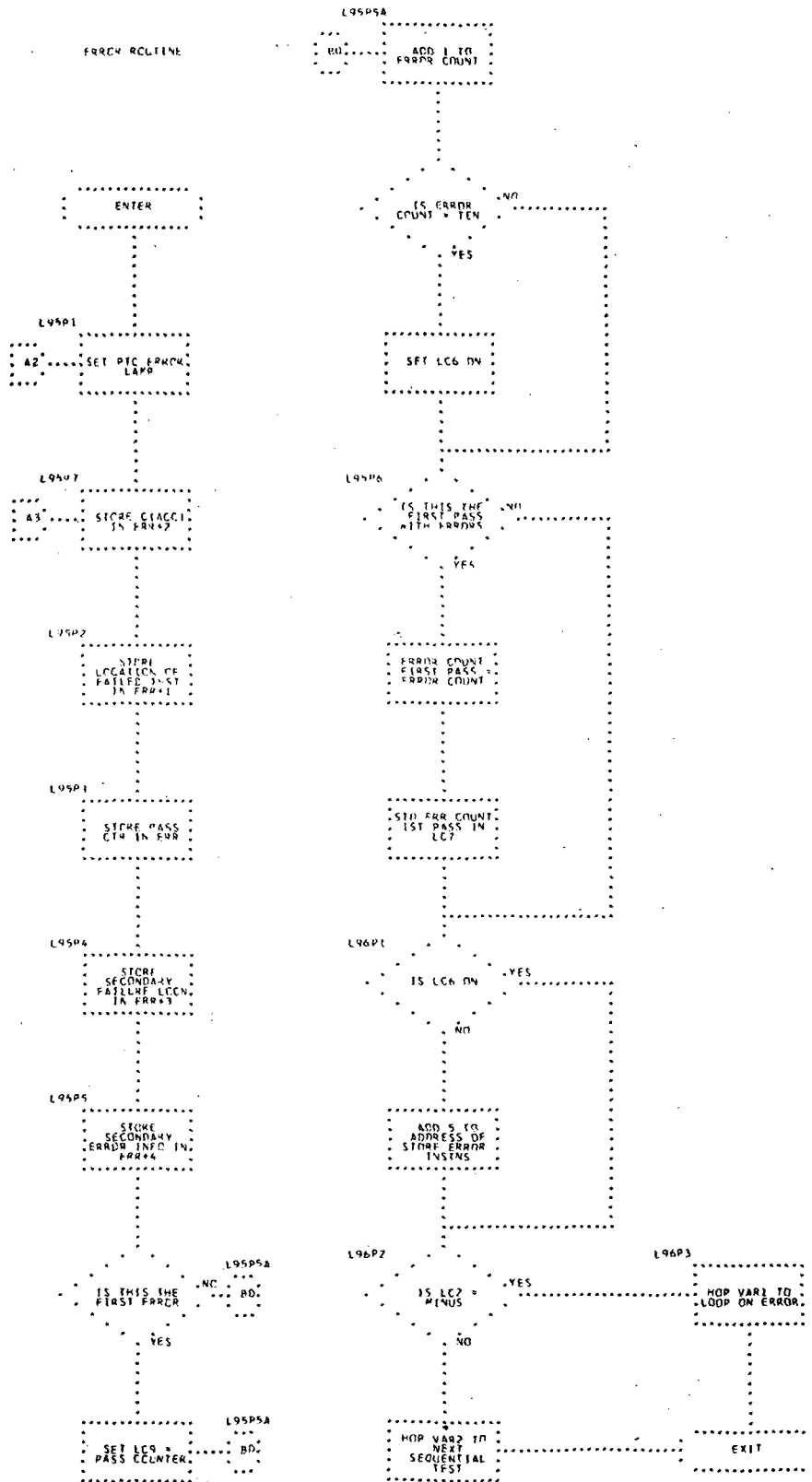


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 26)

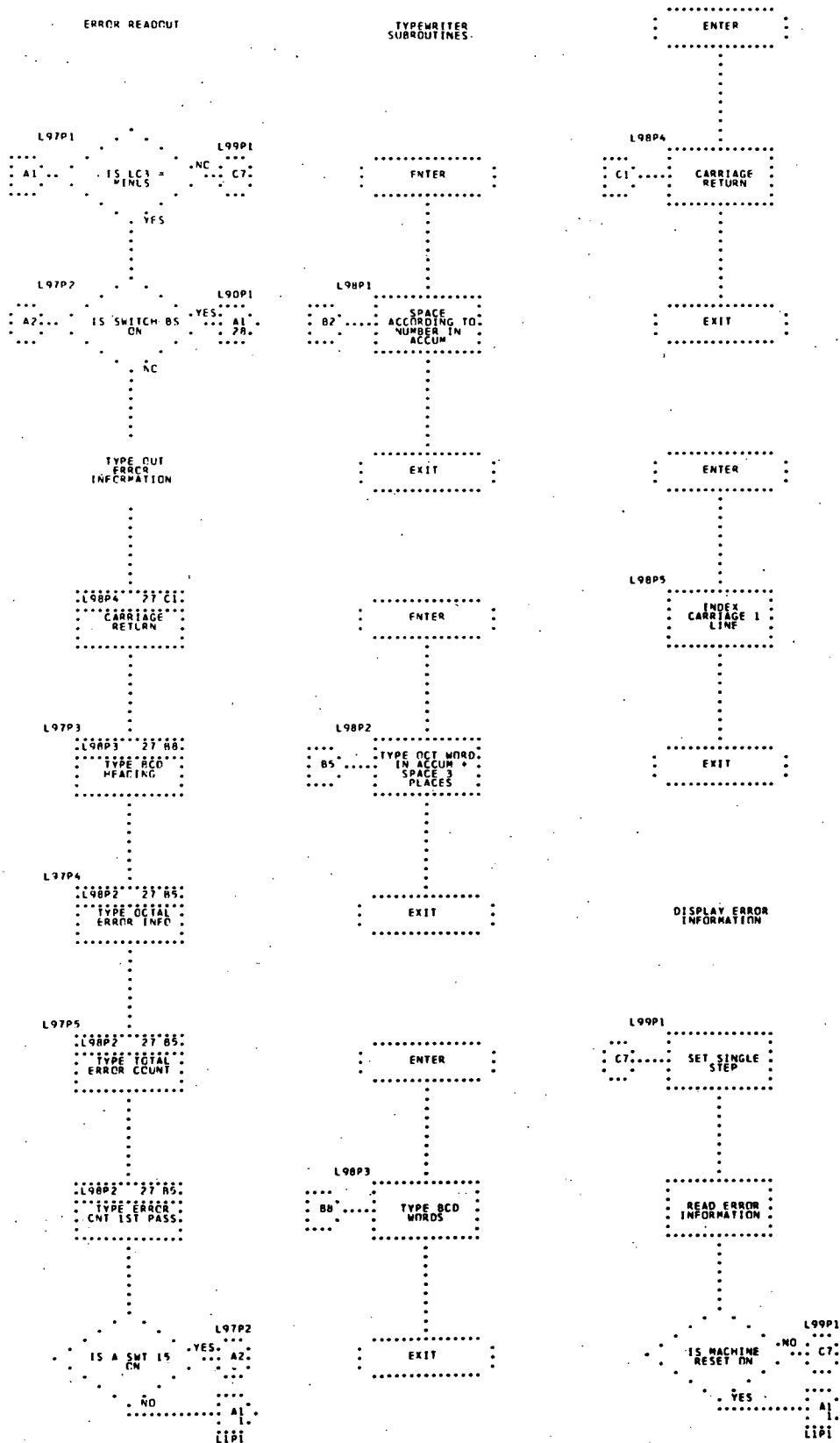


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 27)

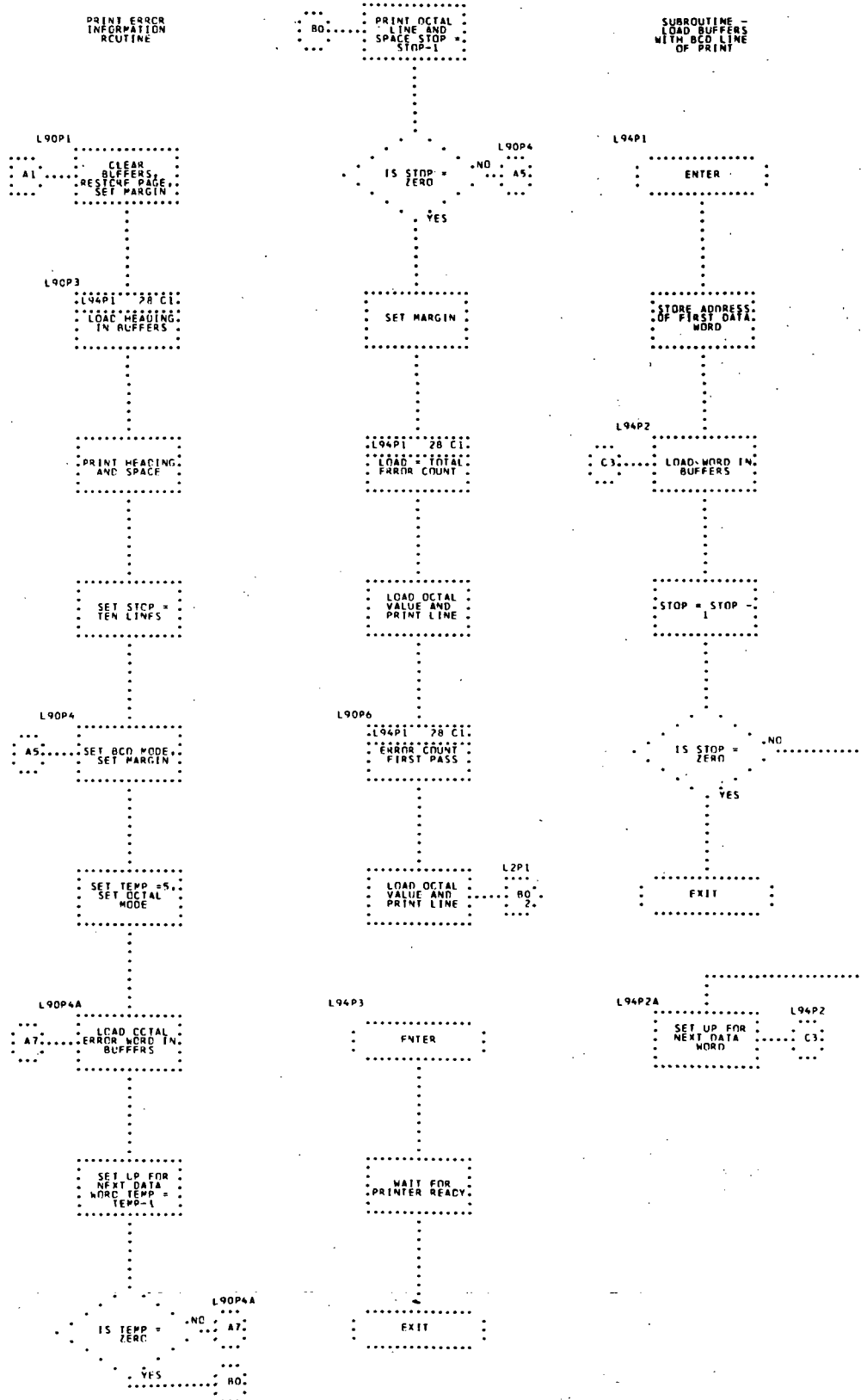


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 28)

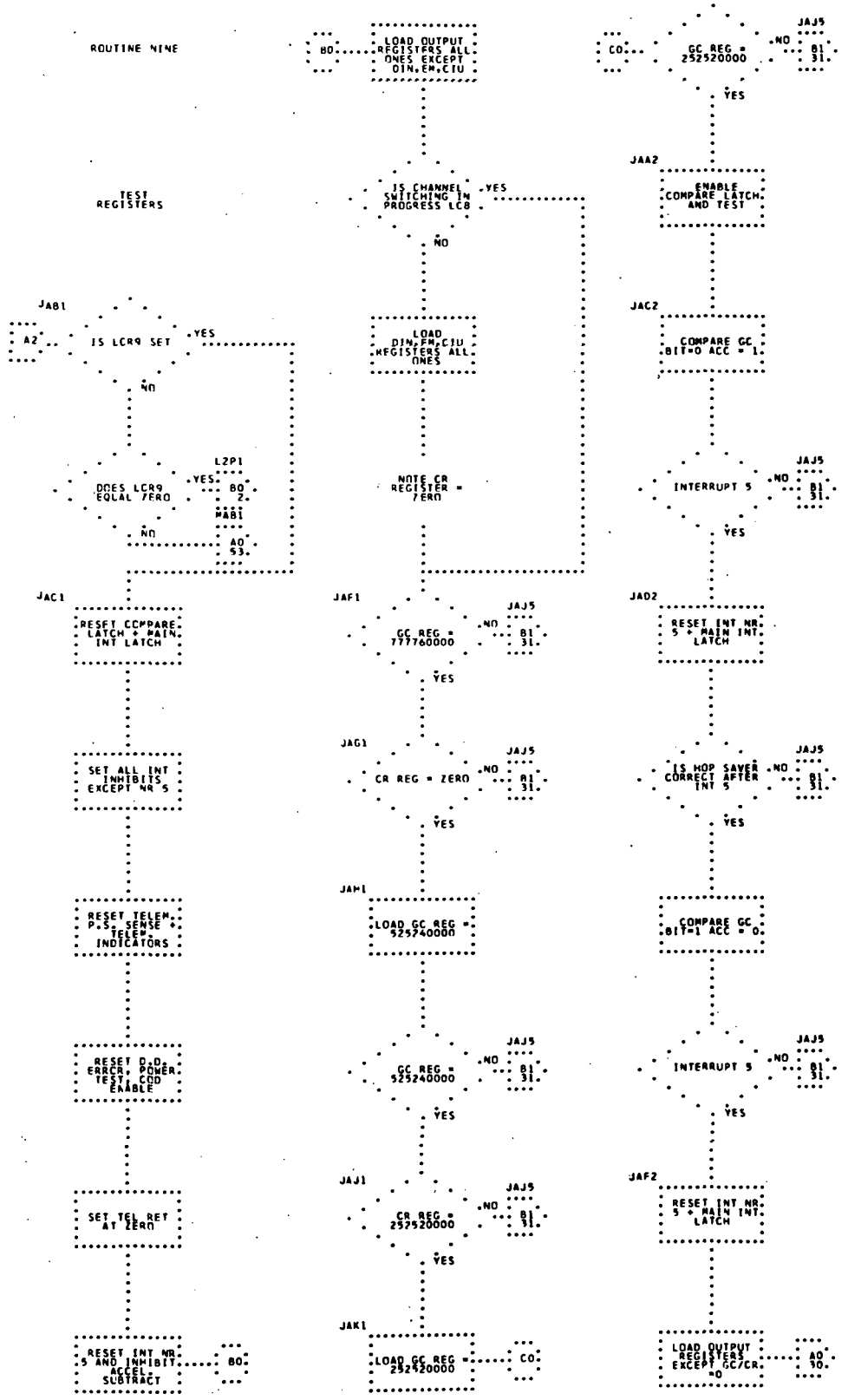


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 29)

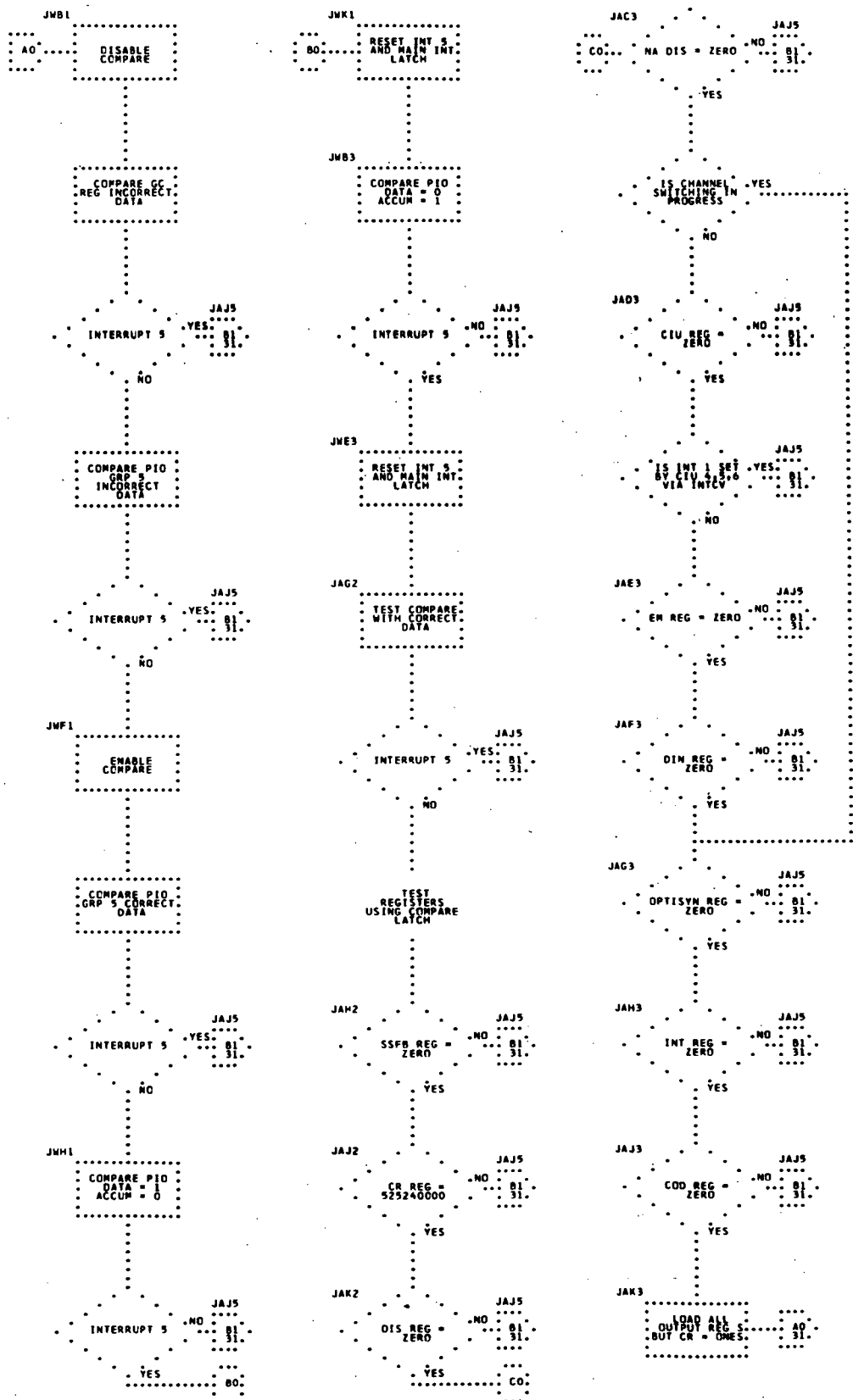


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 30)

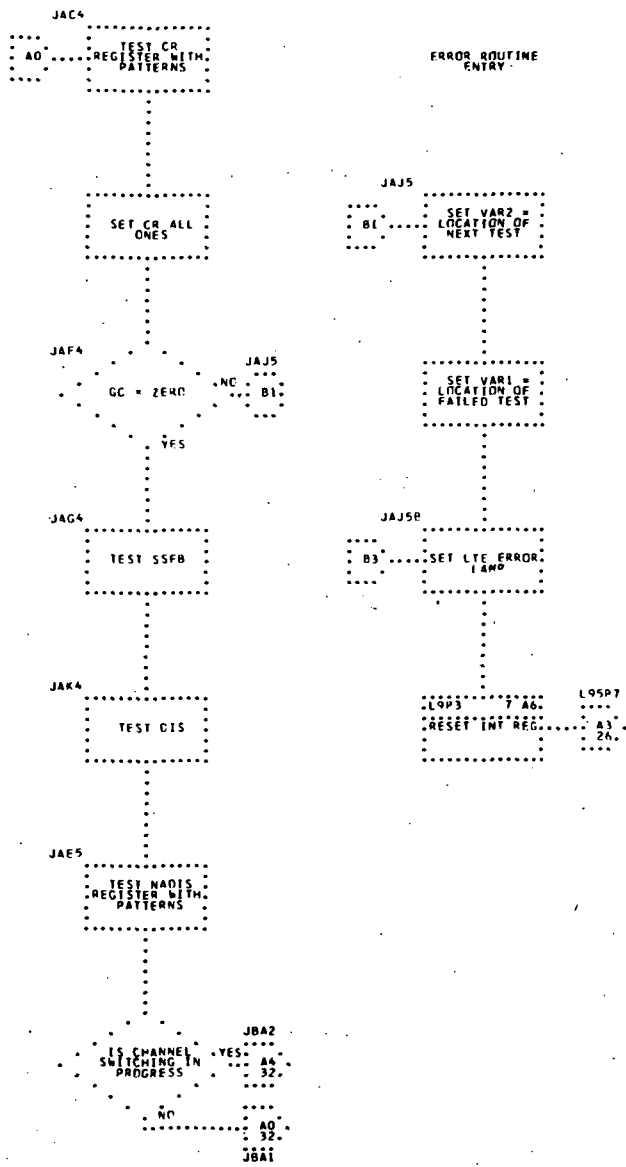


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 31)

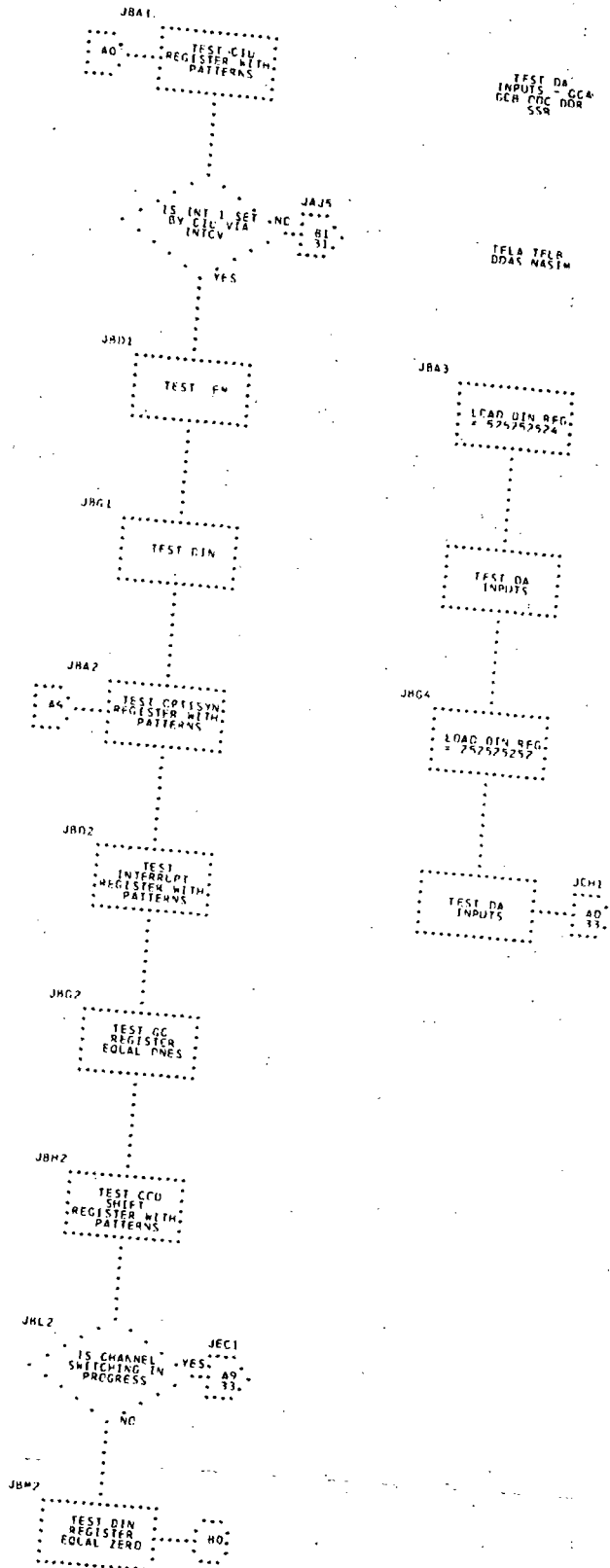


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 32)

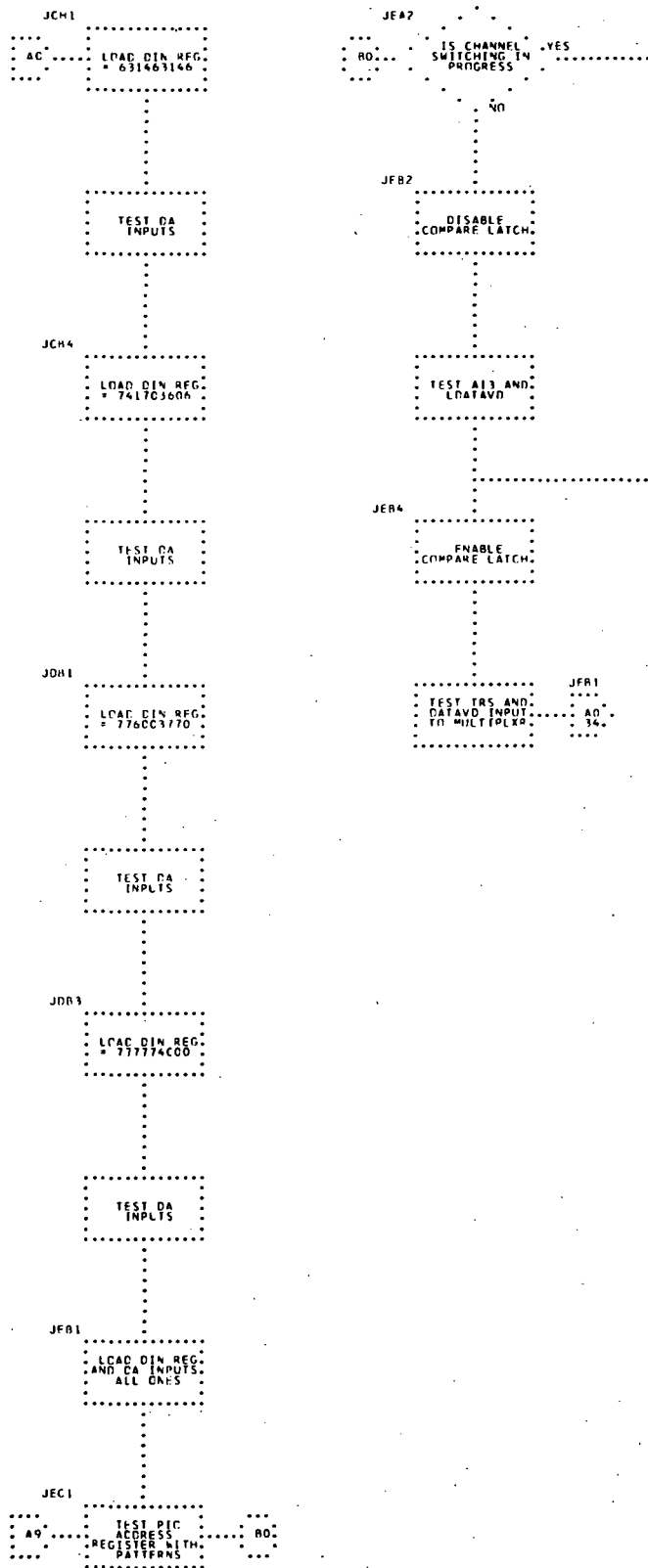


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 33)

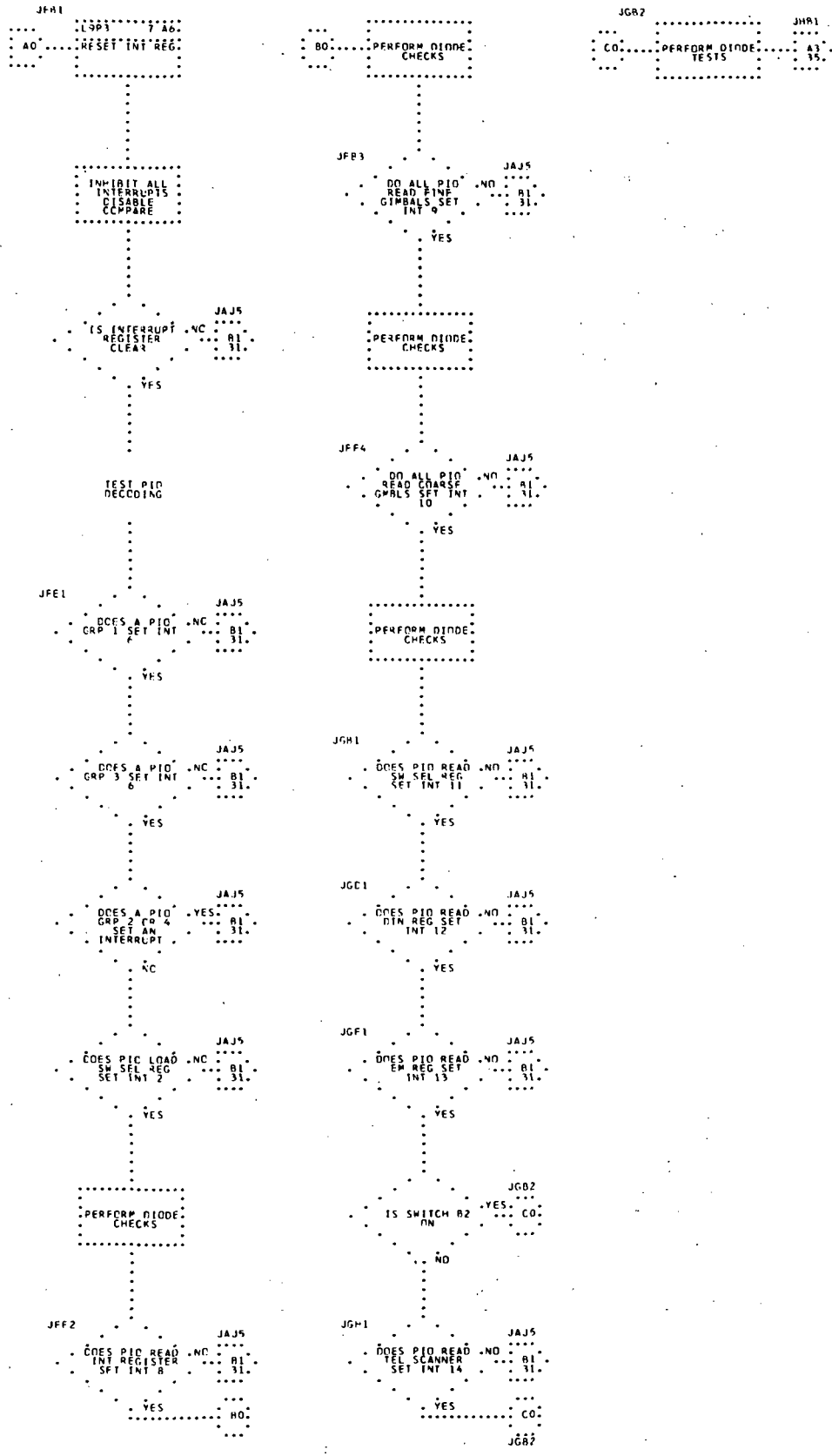


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 34)

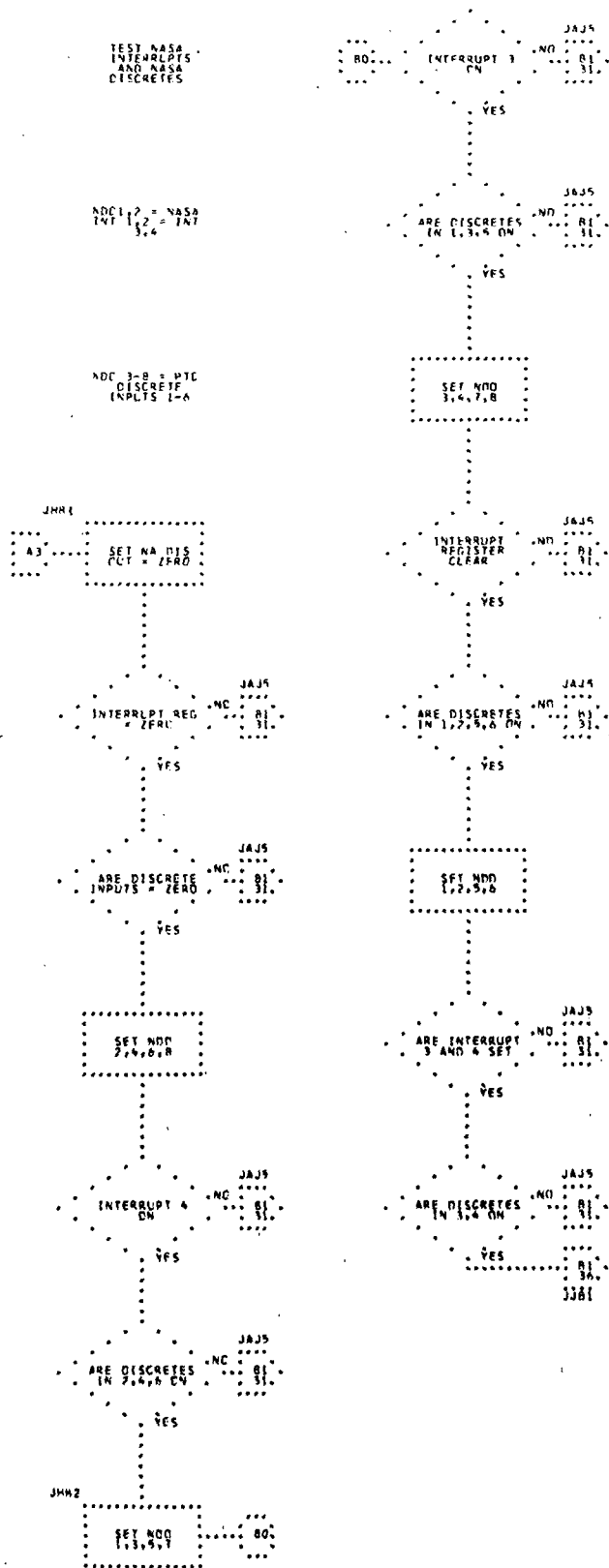


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 35)

TEST
TSYNC/DC SYNC
CIRCUITRY

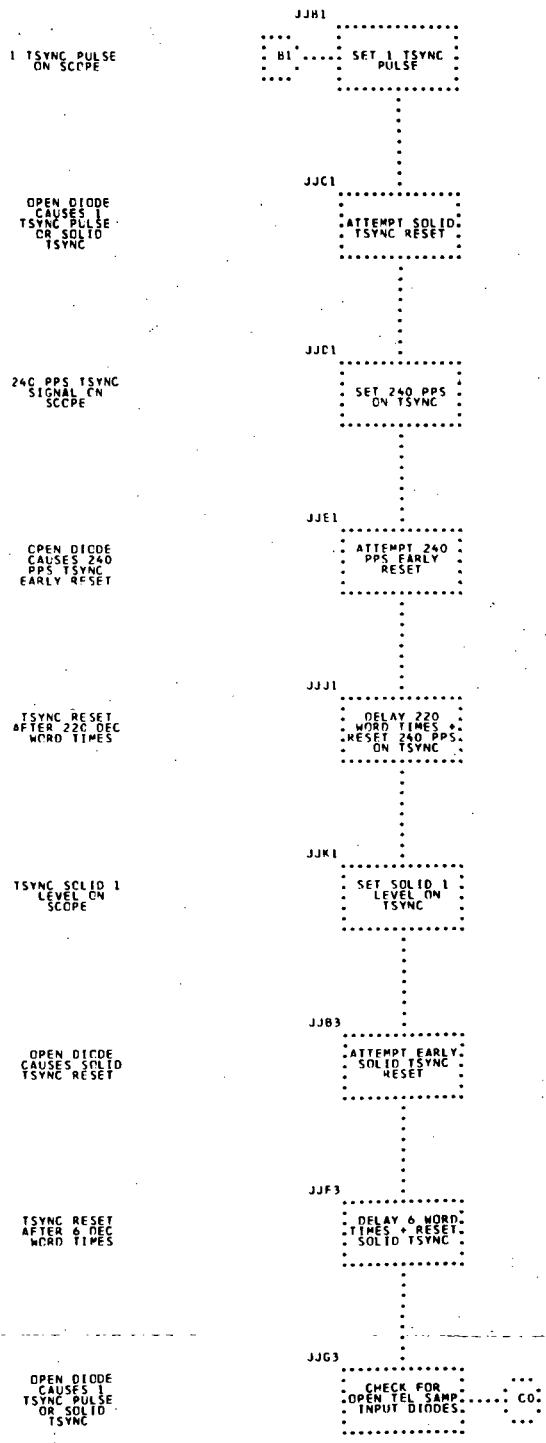
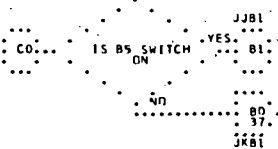


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 36)

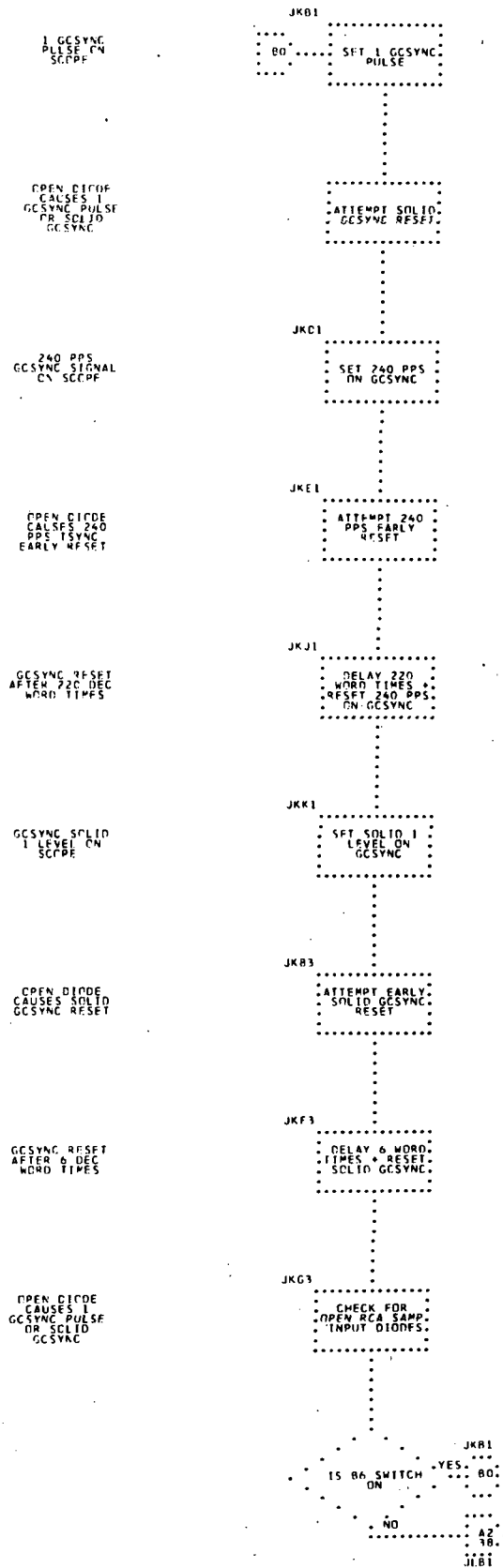


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 37)

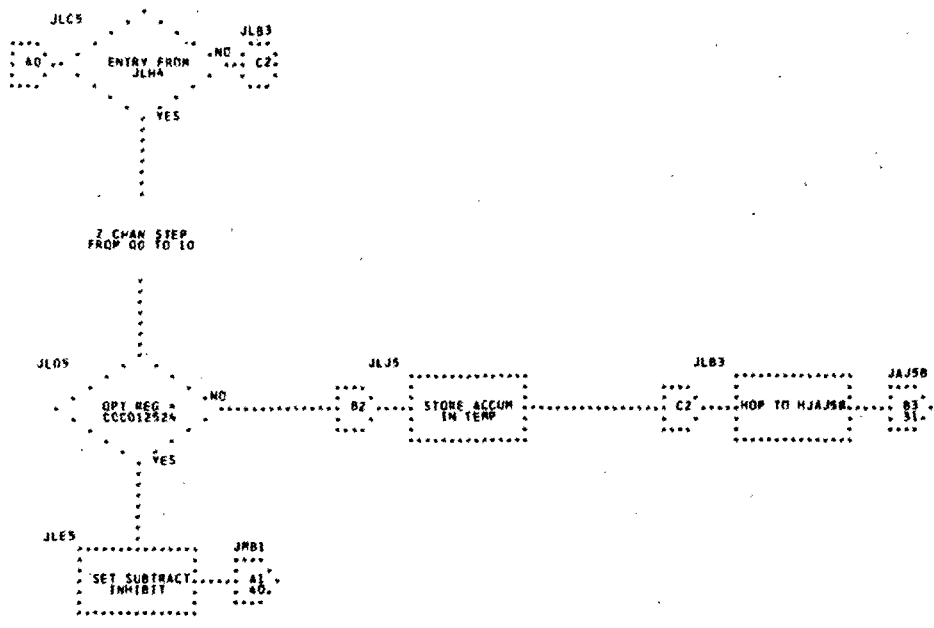


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 39)

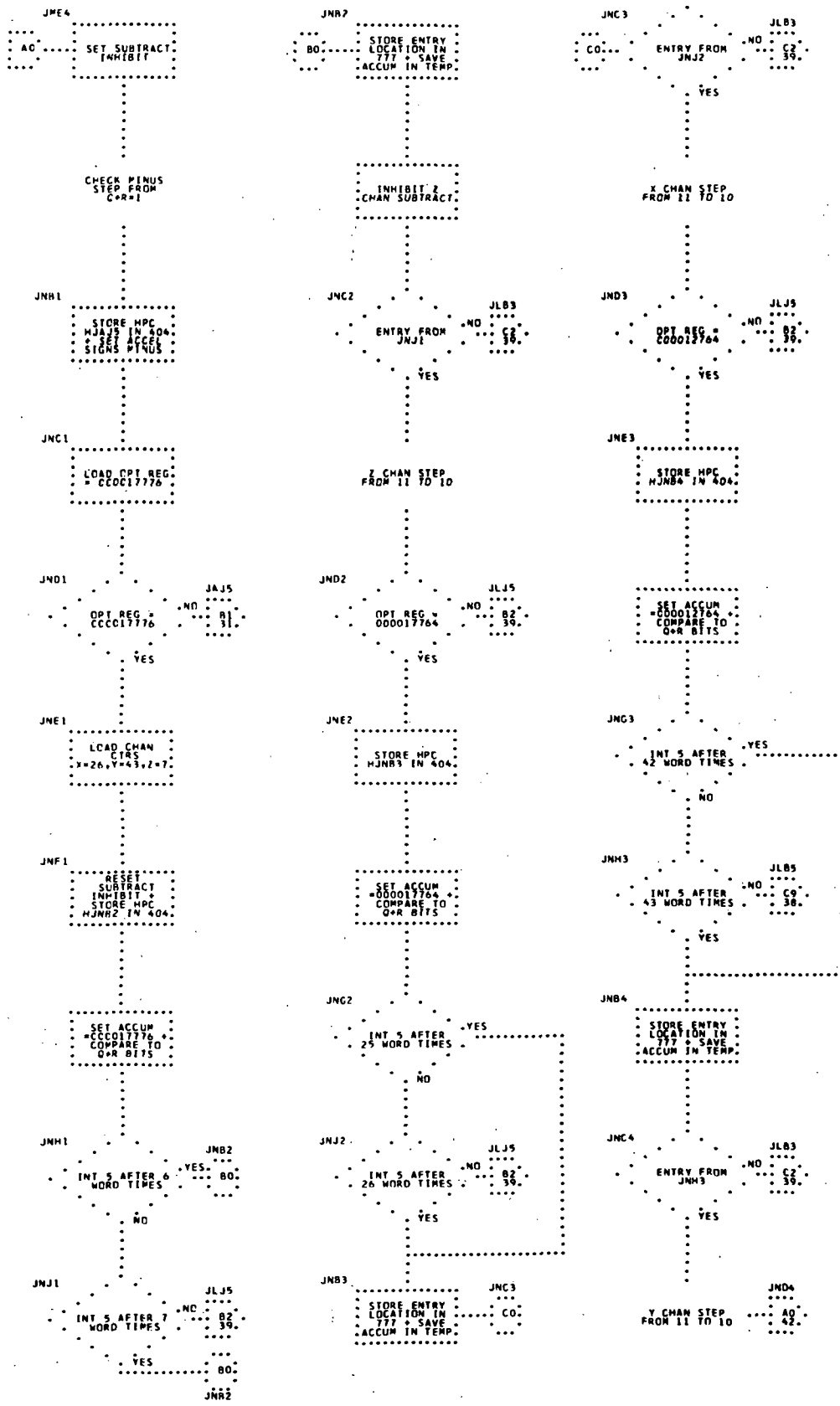


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 41)

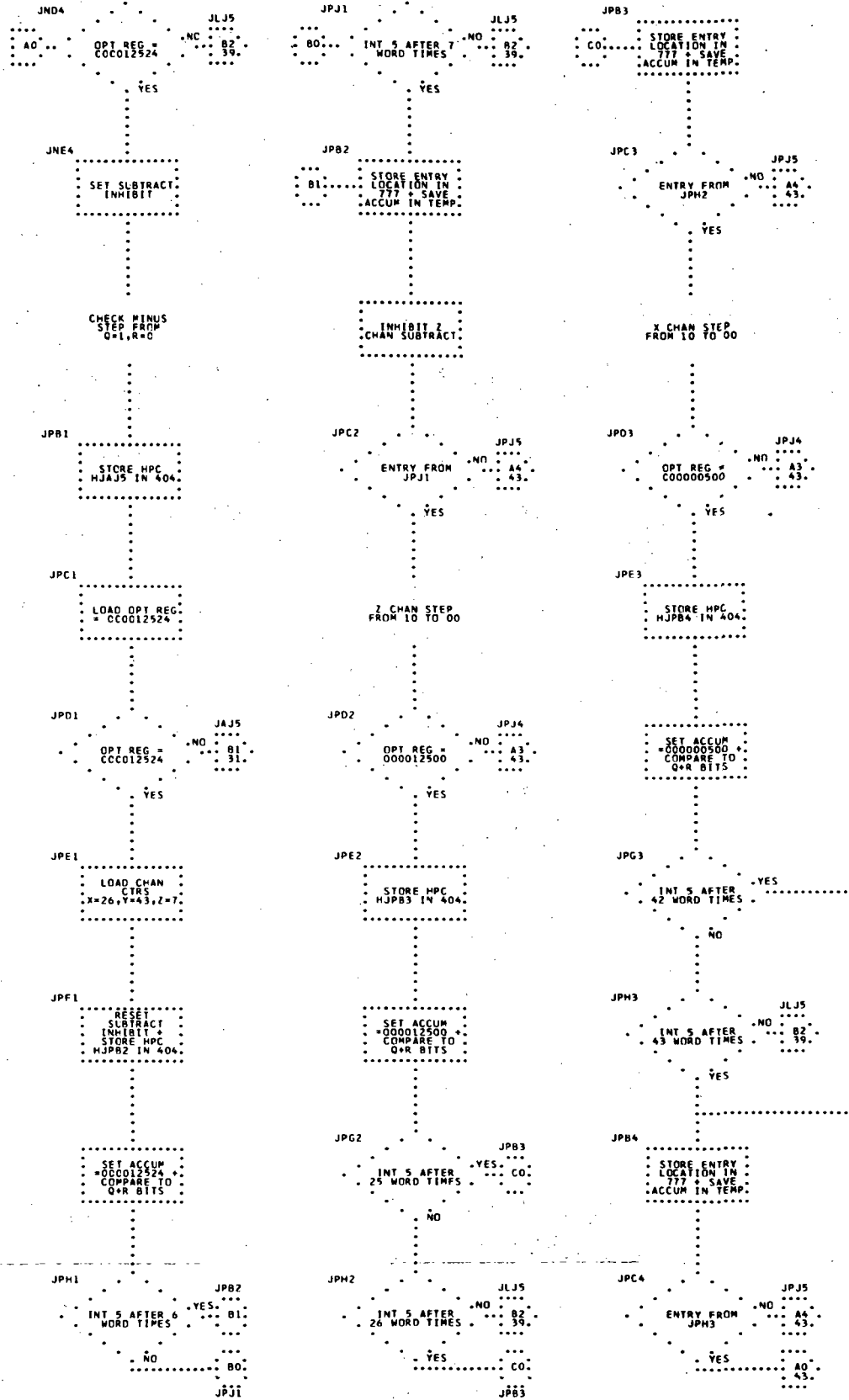


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 42)

Y CHAN STEP
PROP IC TO 00

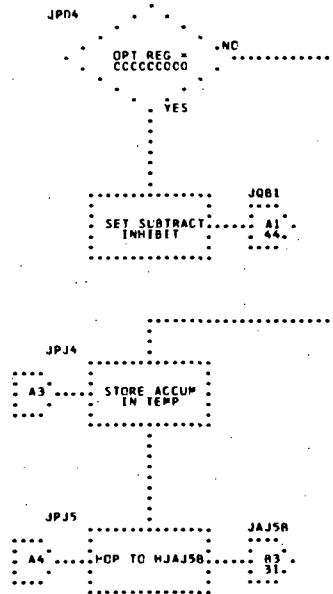


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 43)

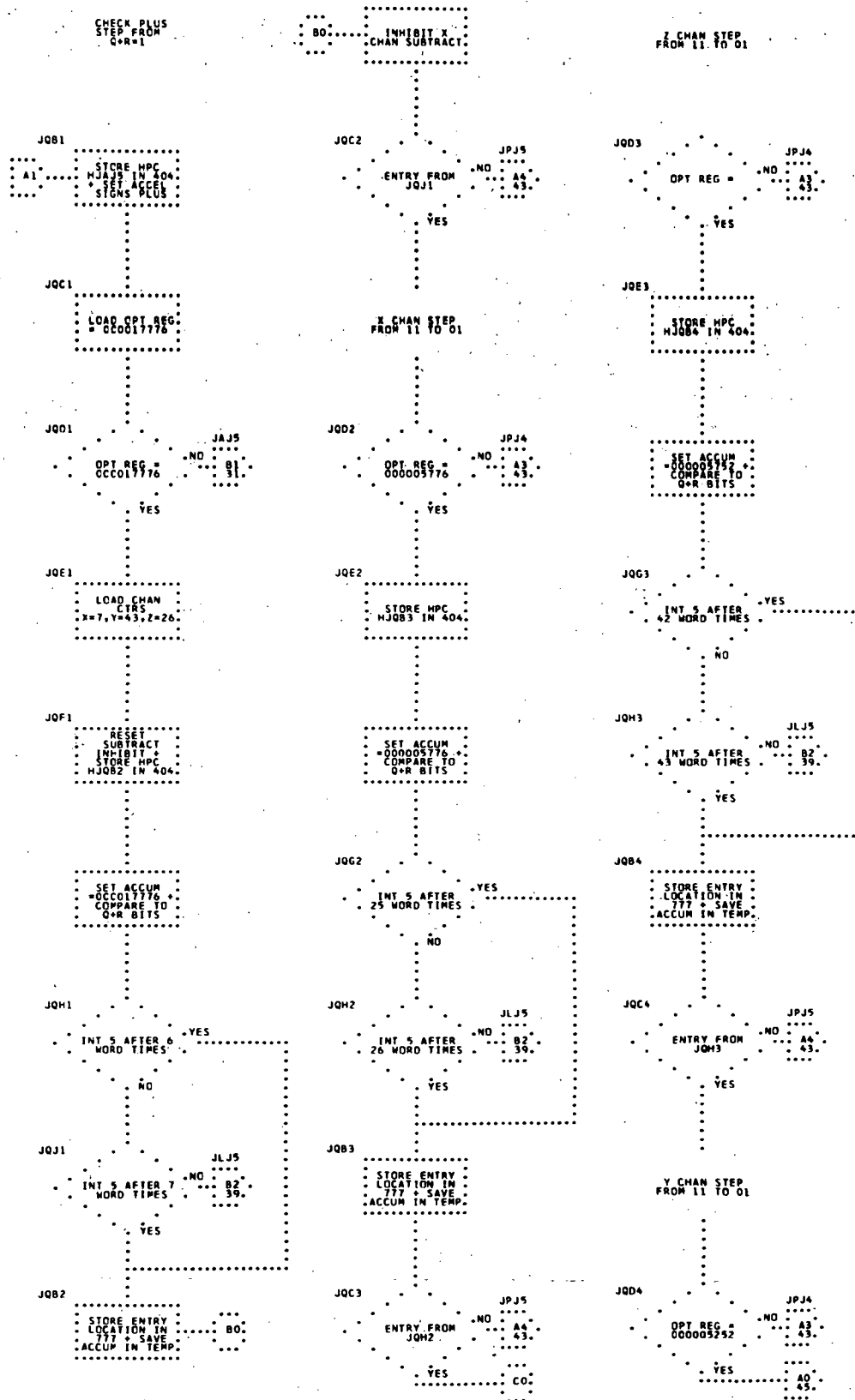


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 44)

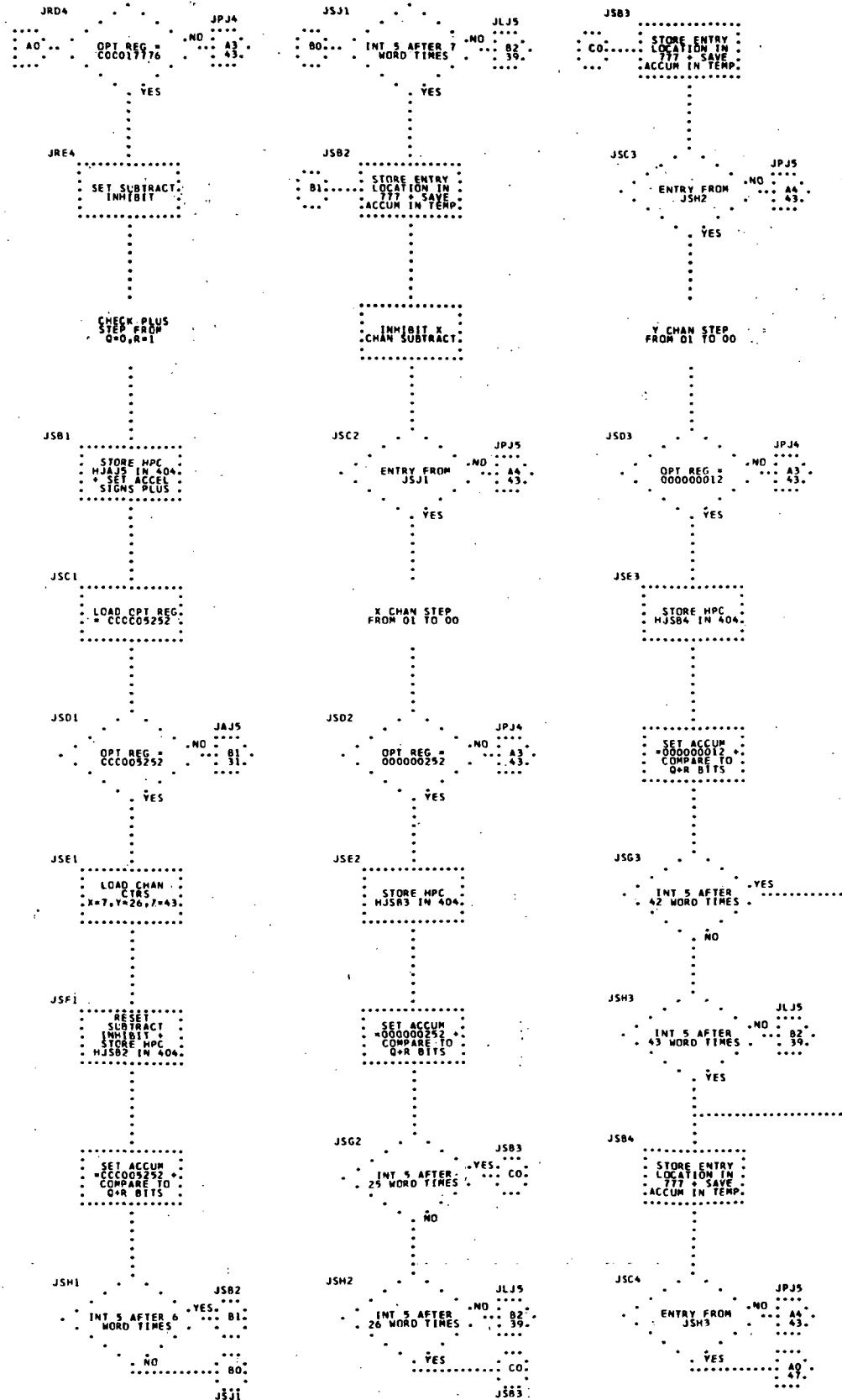


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 46)

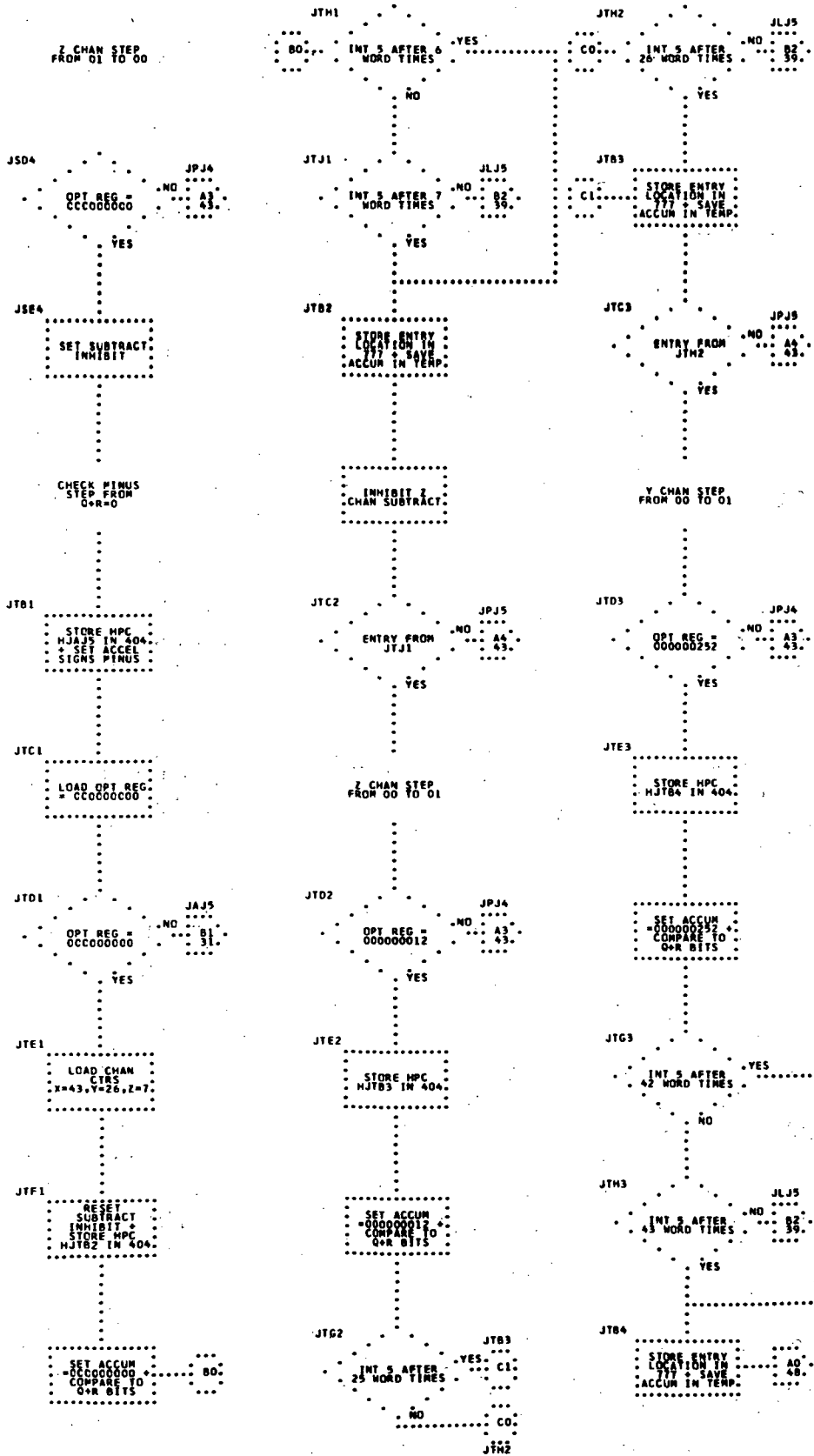


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 47)

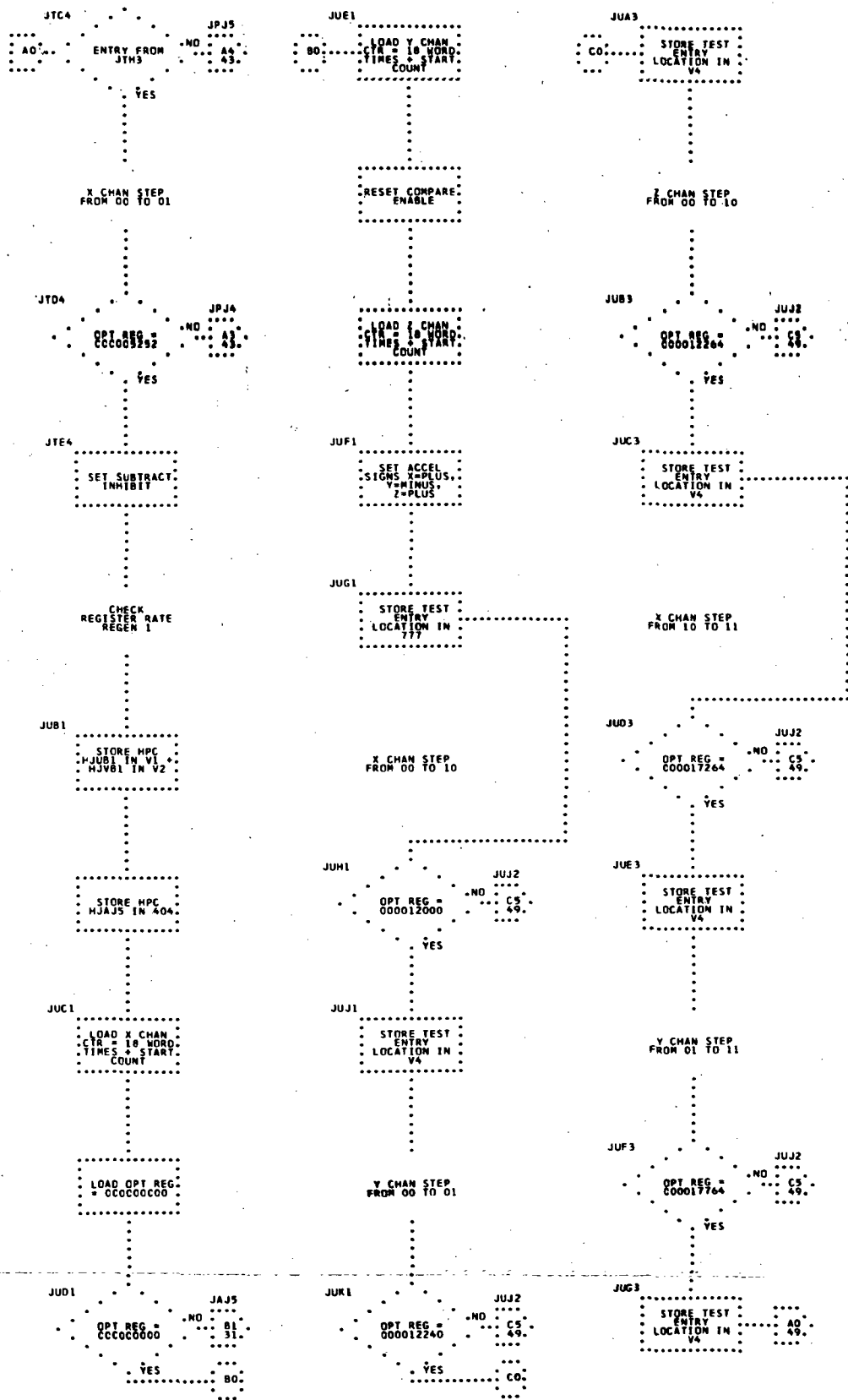


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 48)

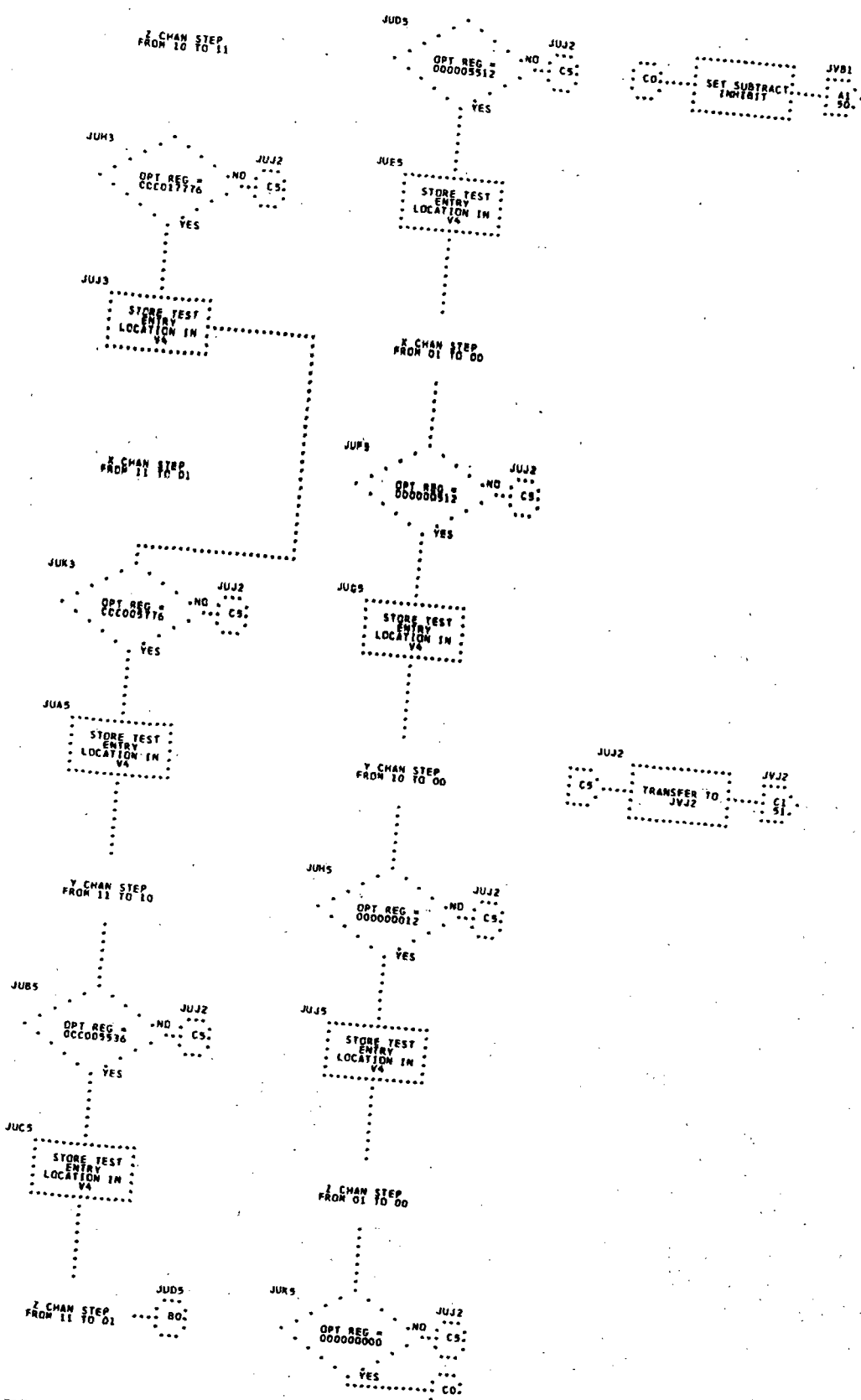


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 49)

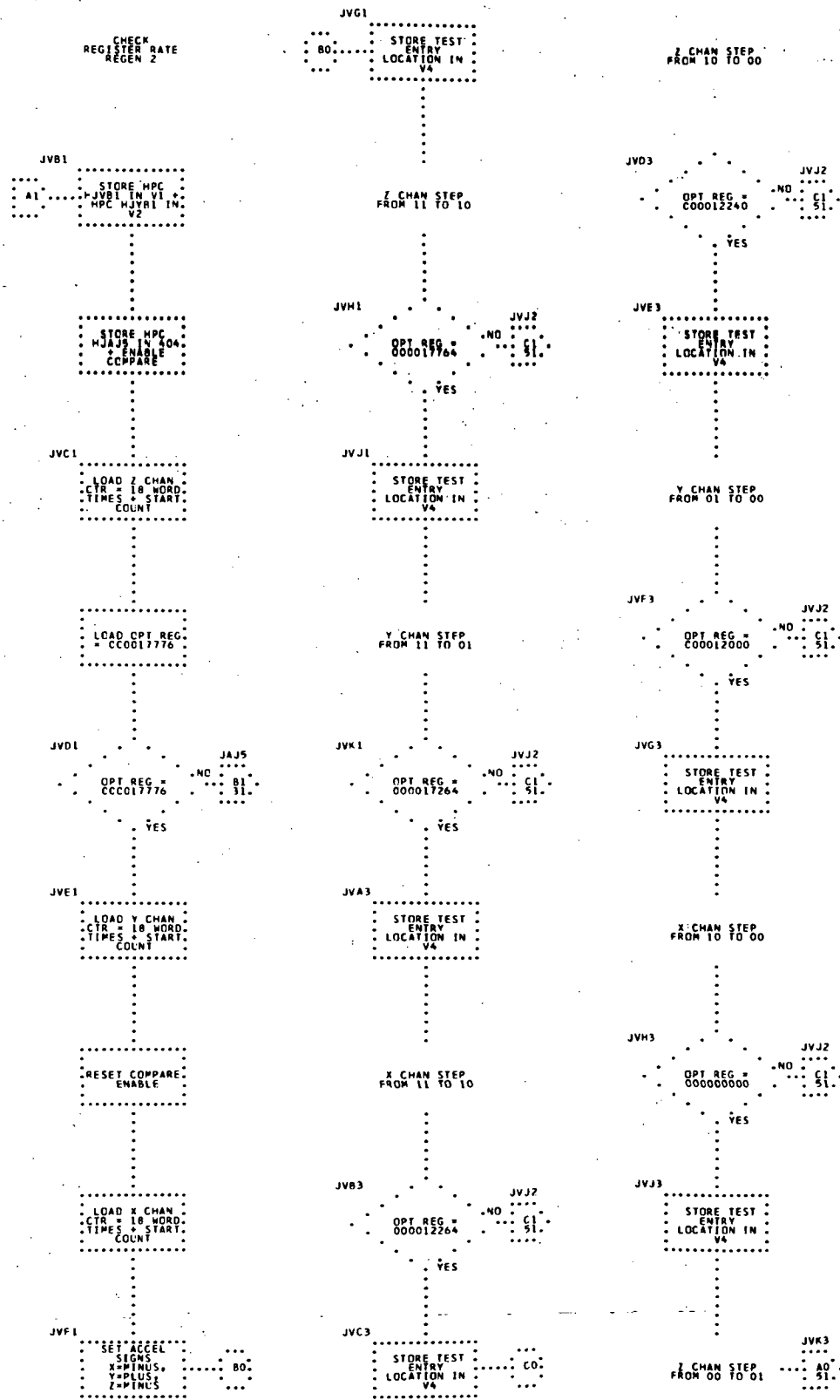


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 50)

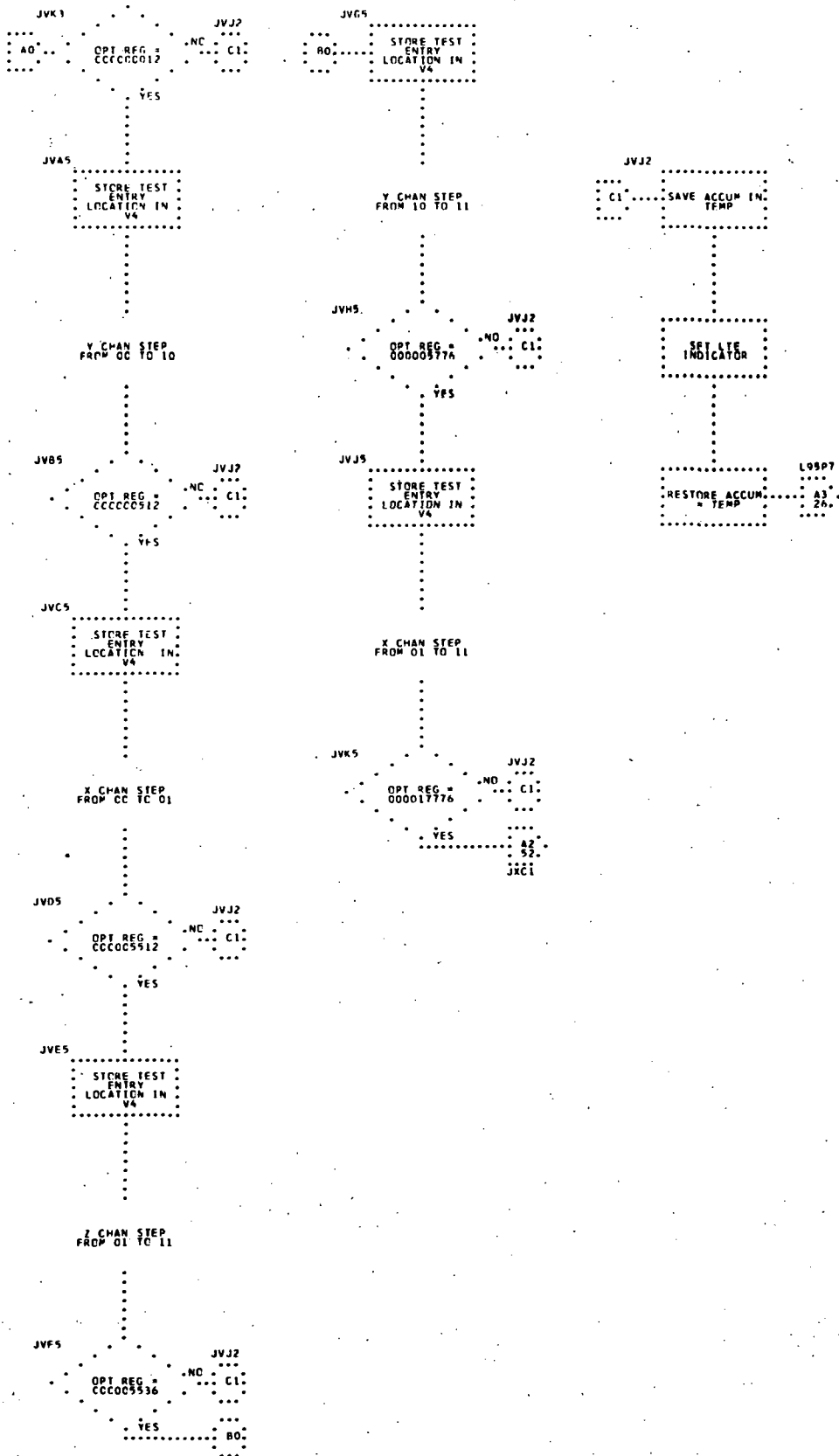


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 51)

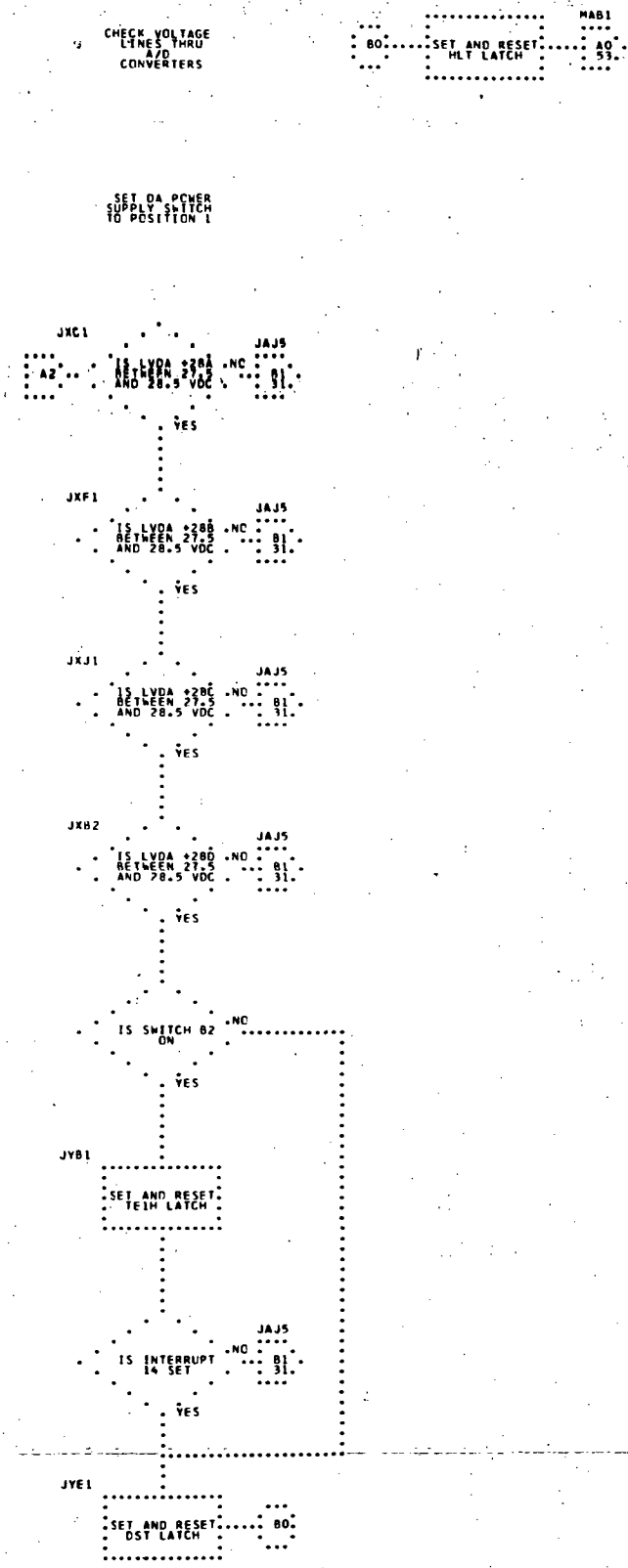


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 52)

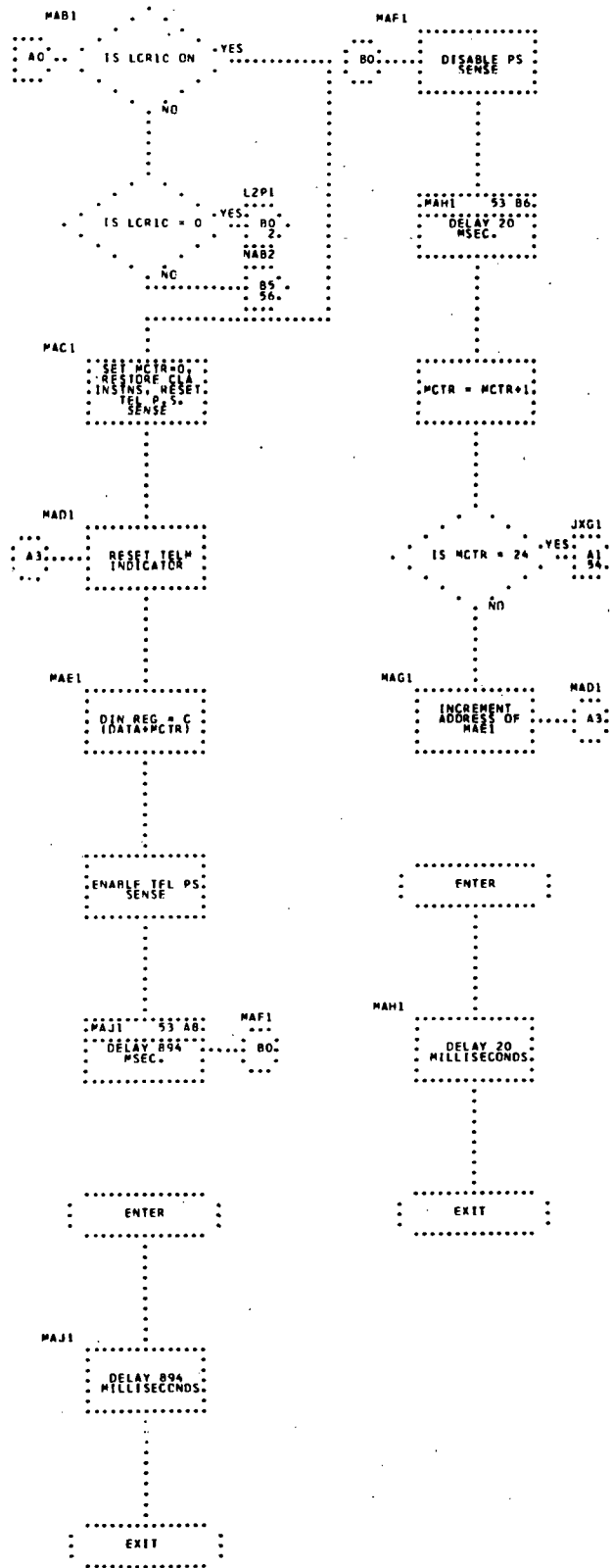


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 53)

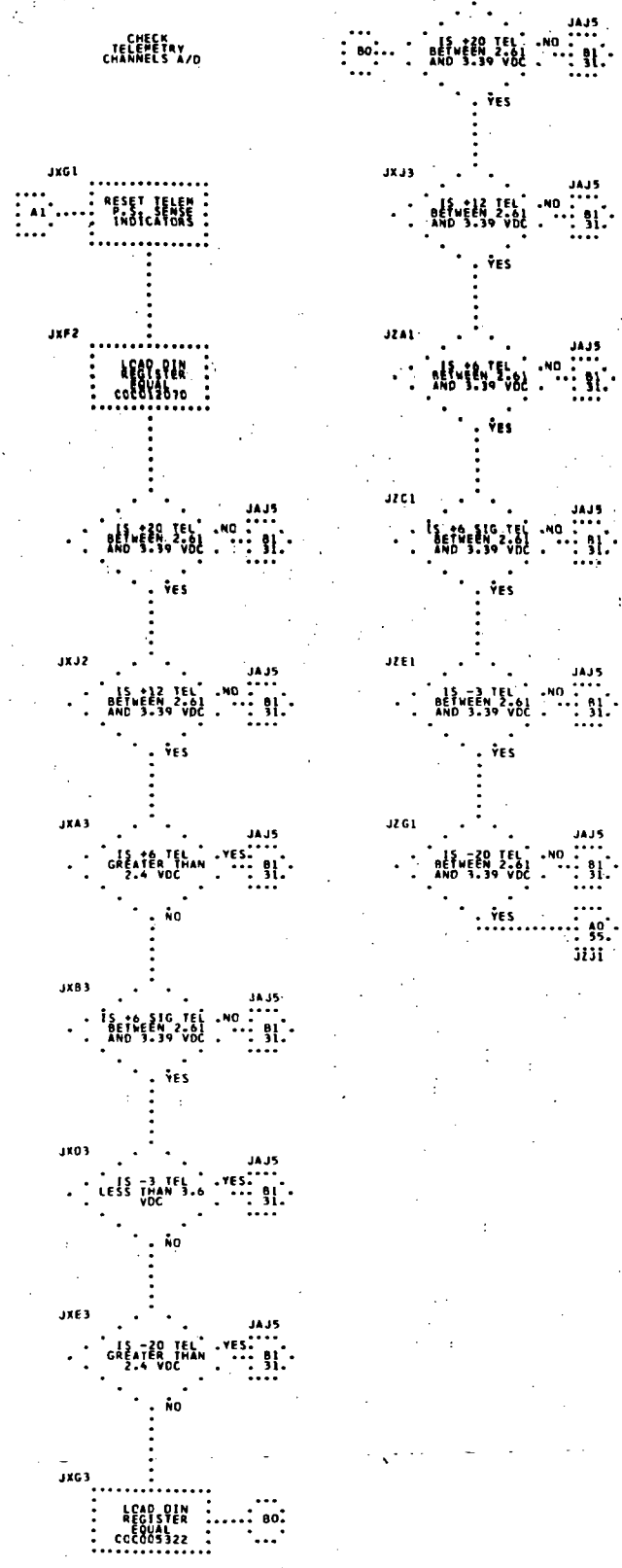


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 54)

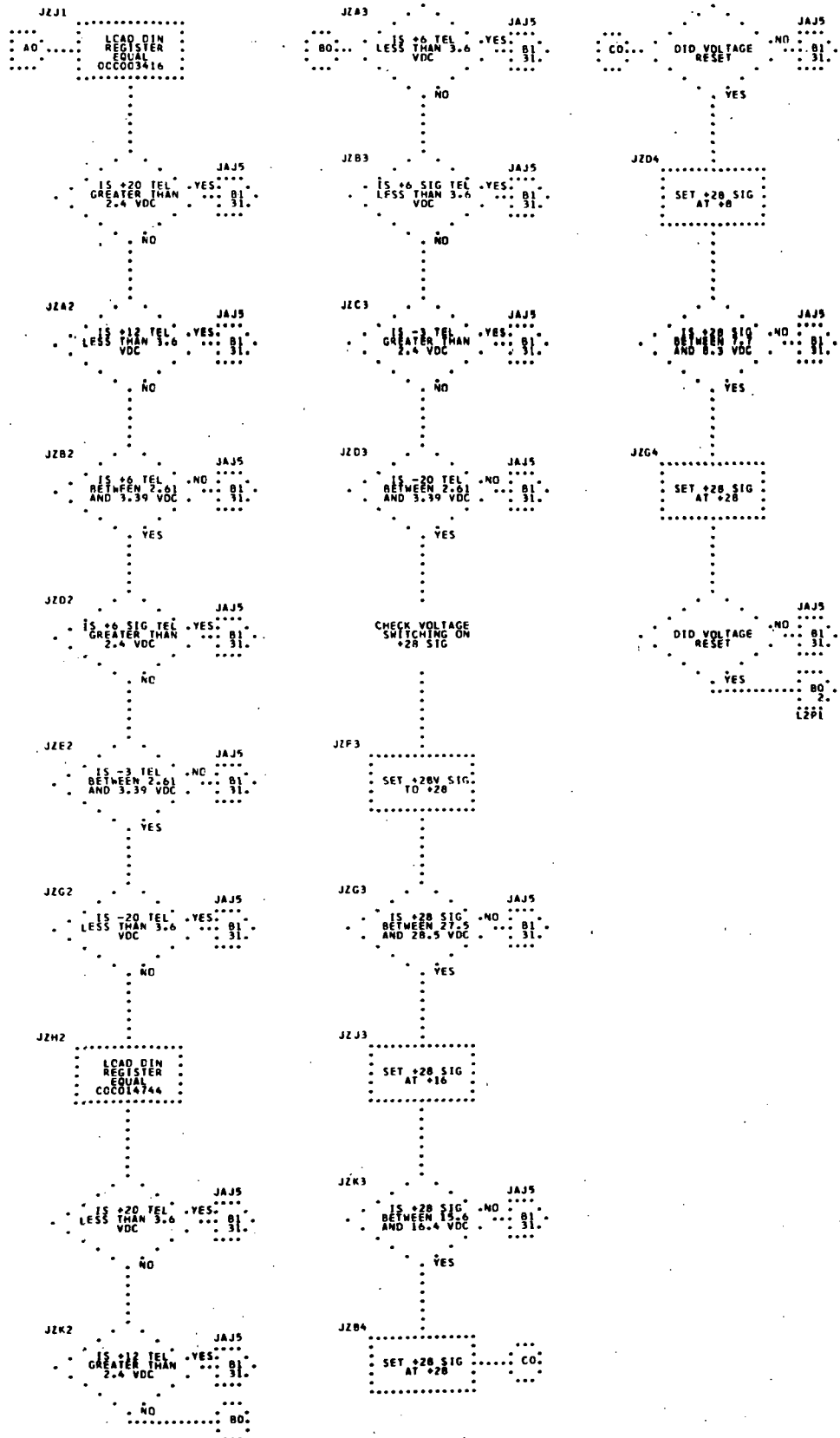


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 55)

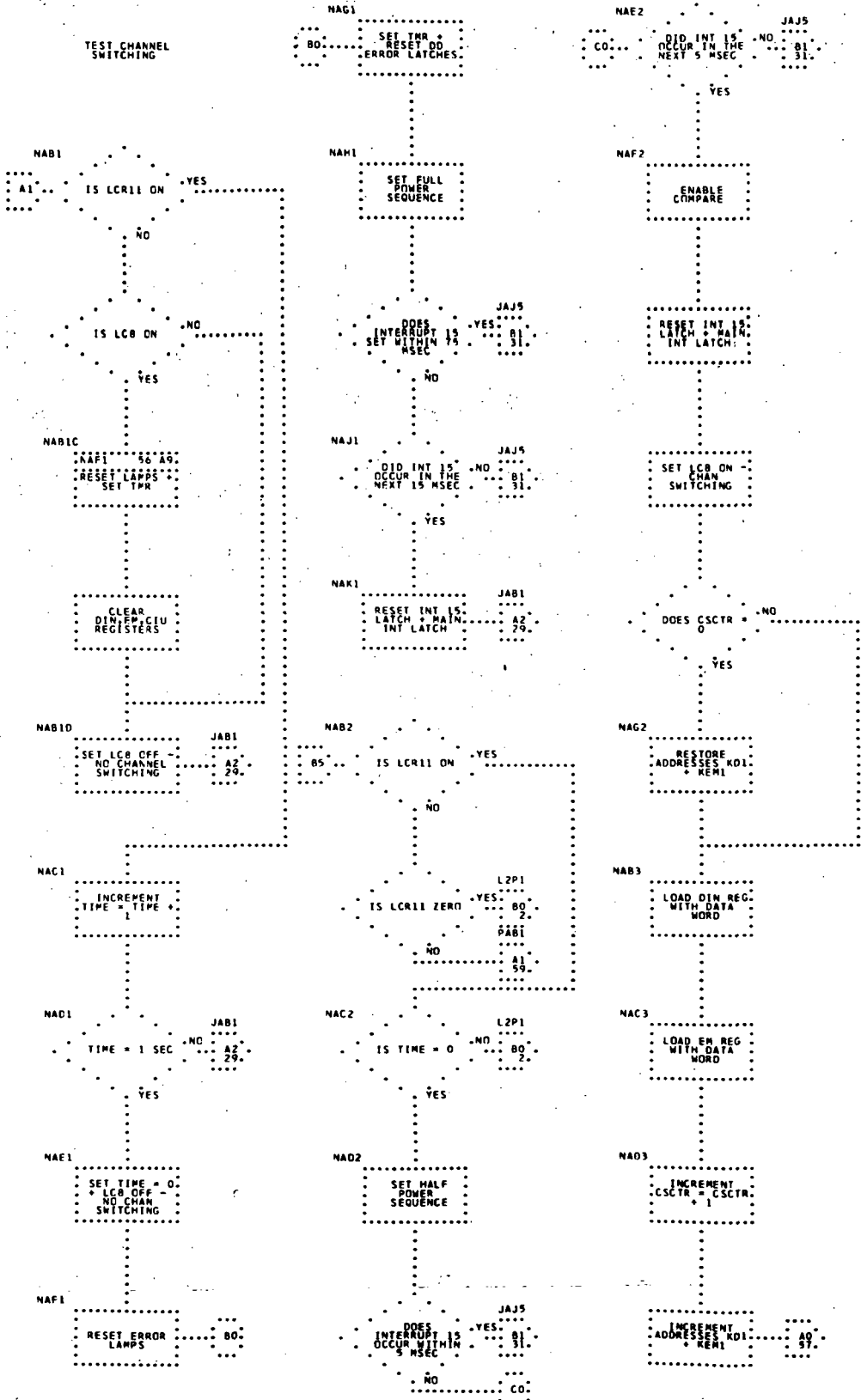


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 56)

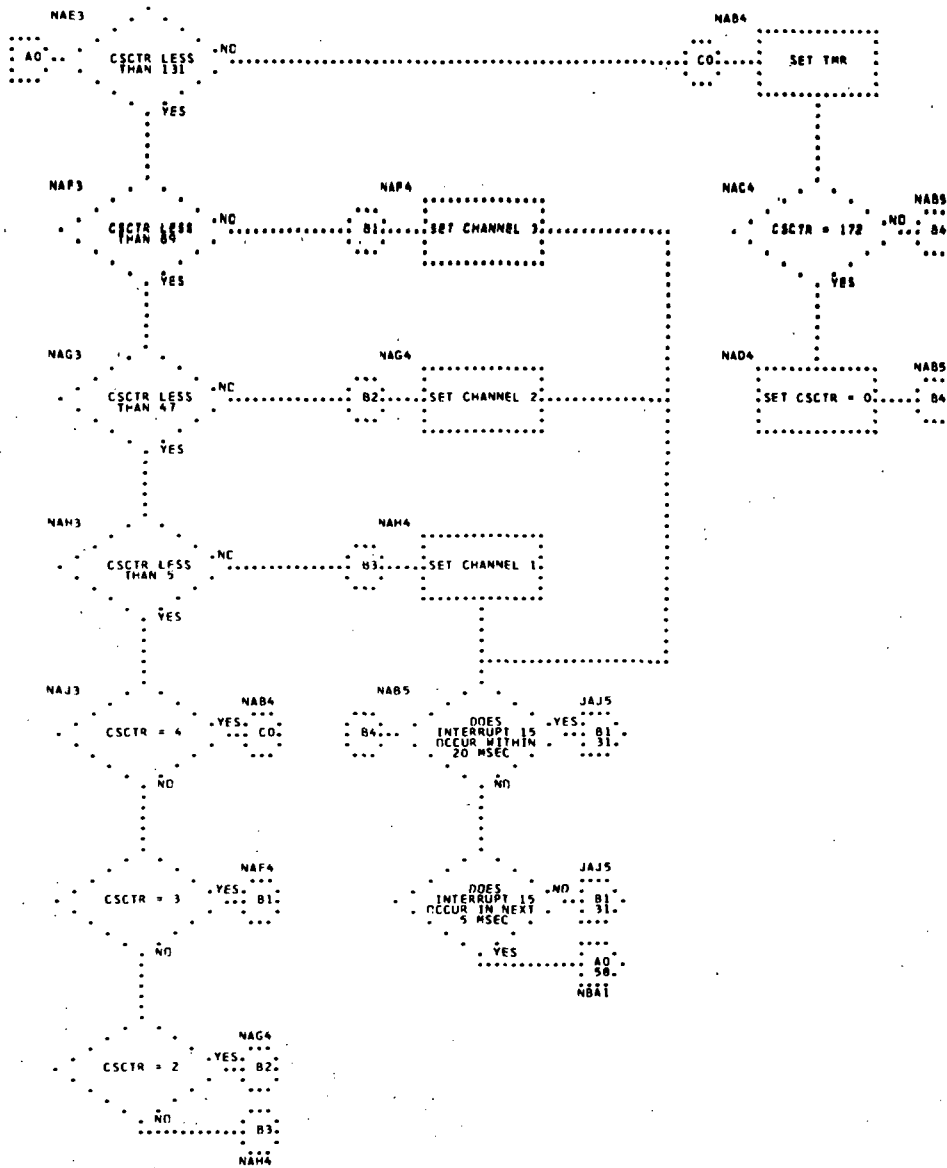


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 57)

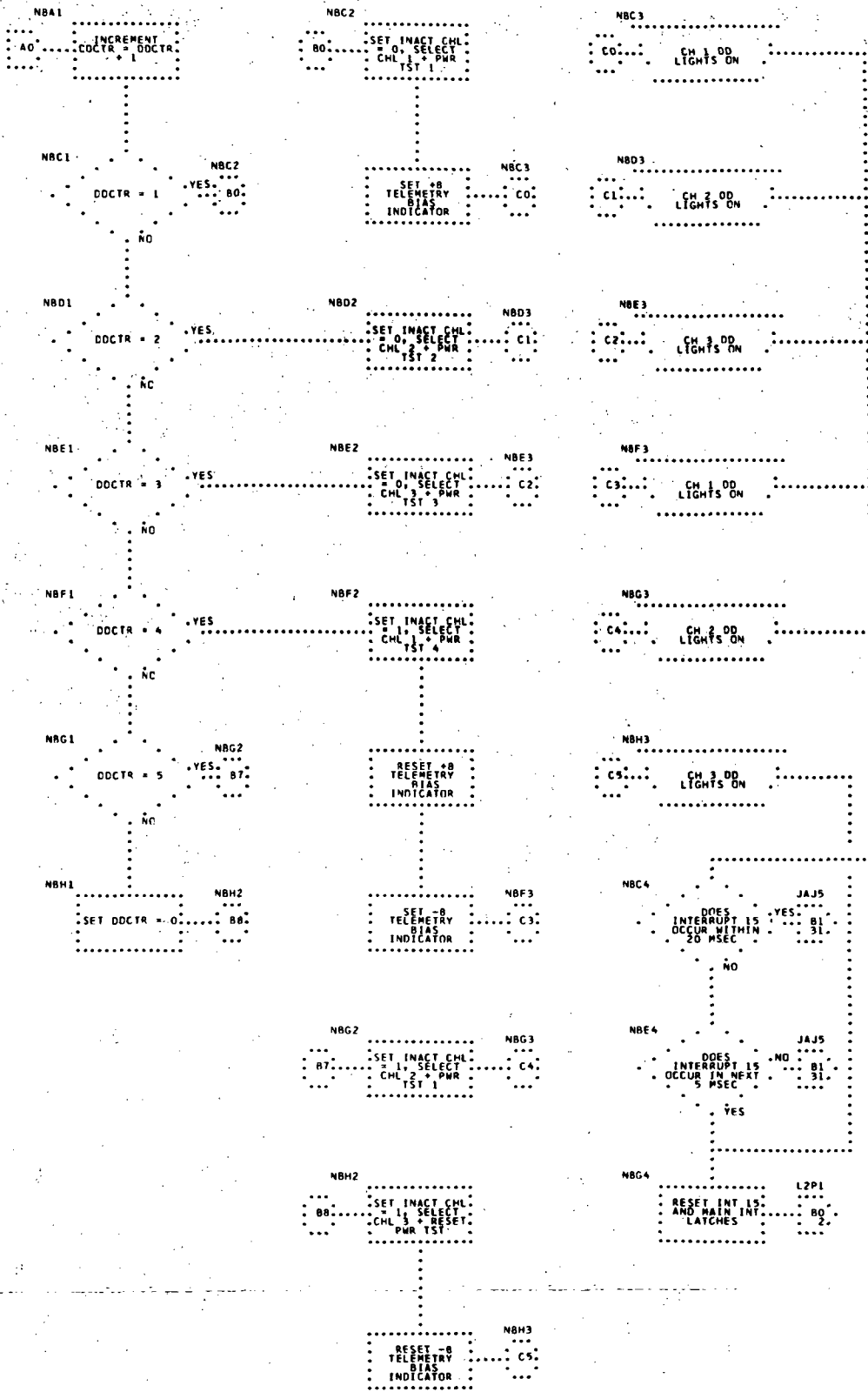


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 58)

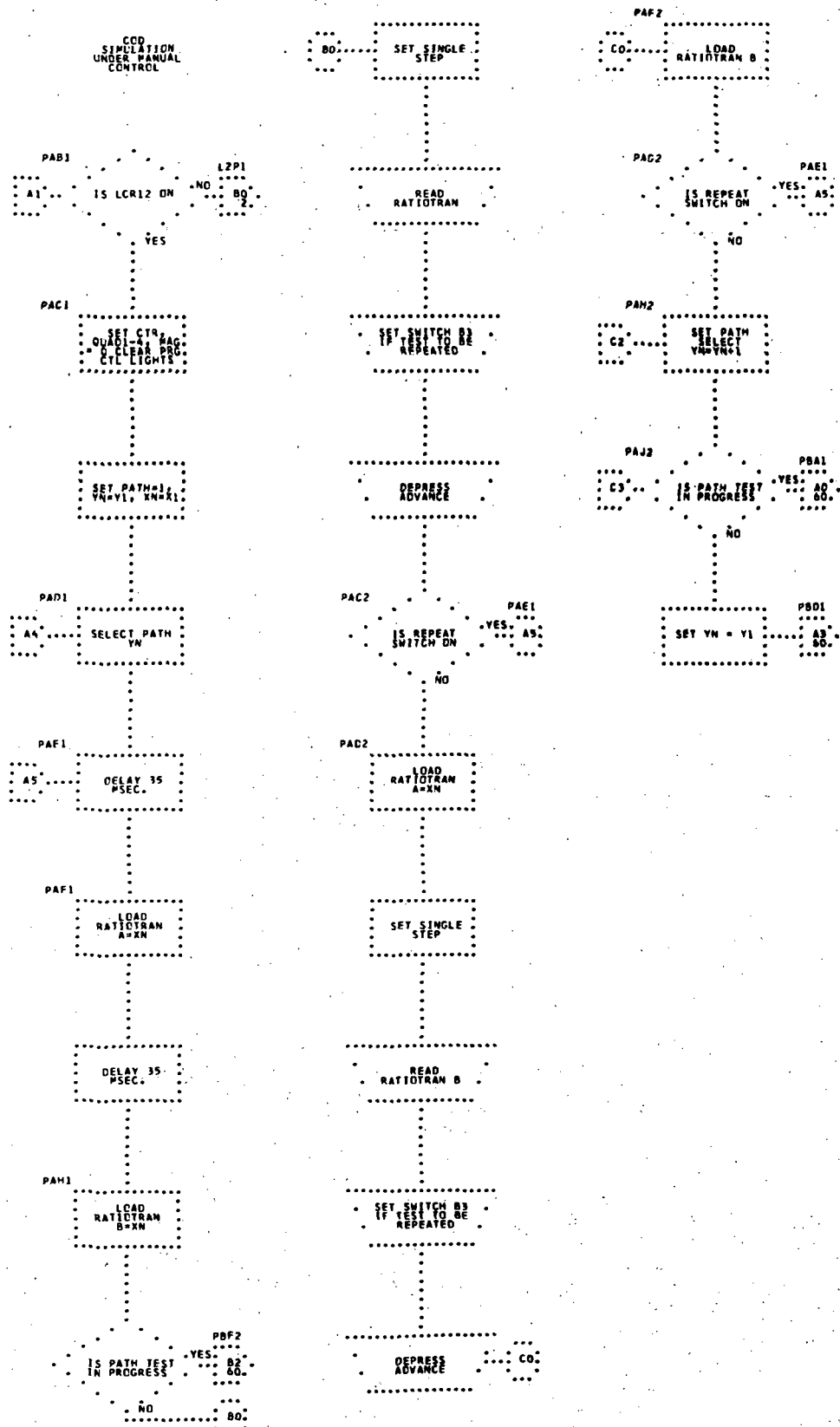


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 59)

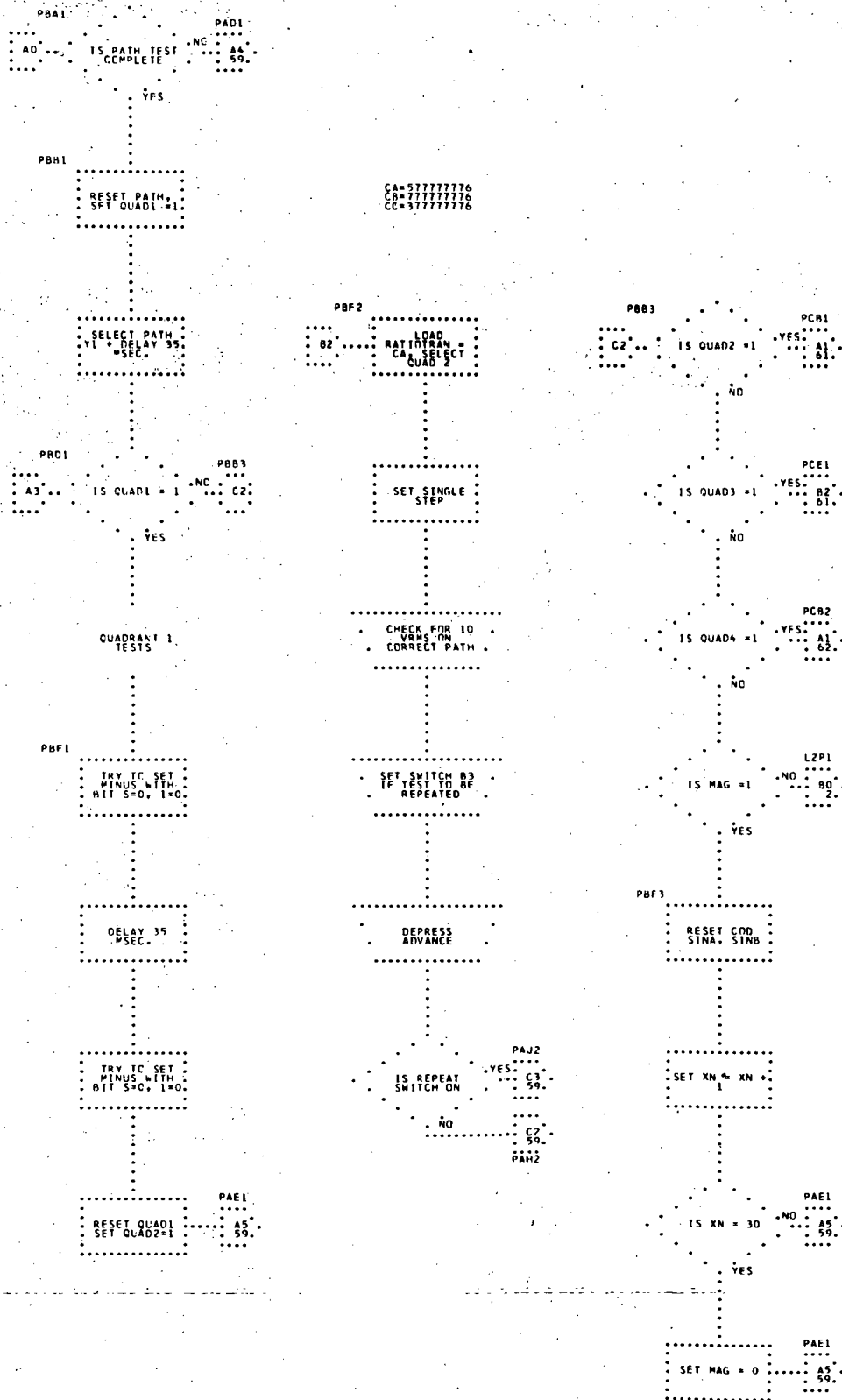


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 60)

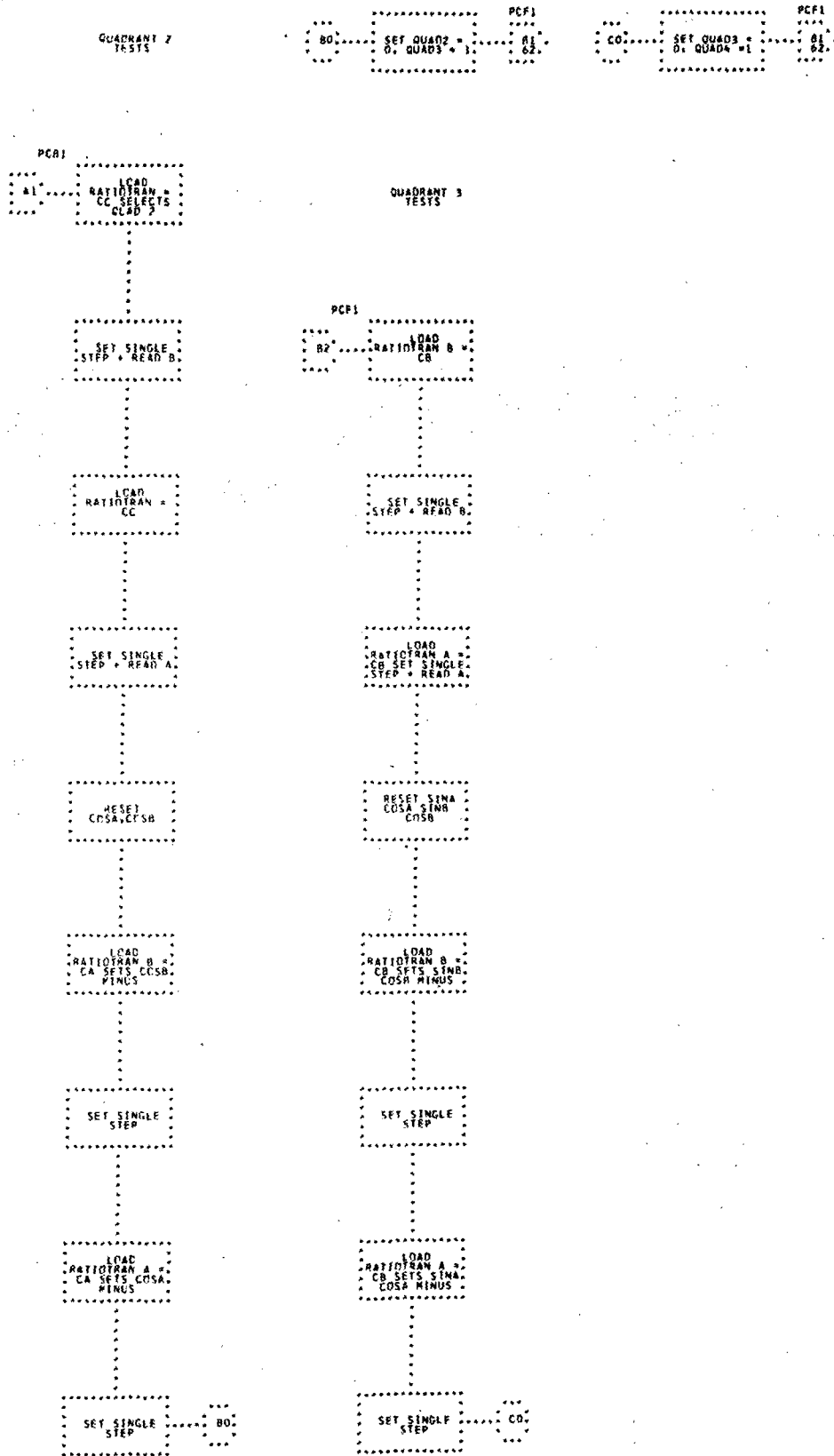


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 61)

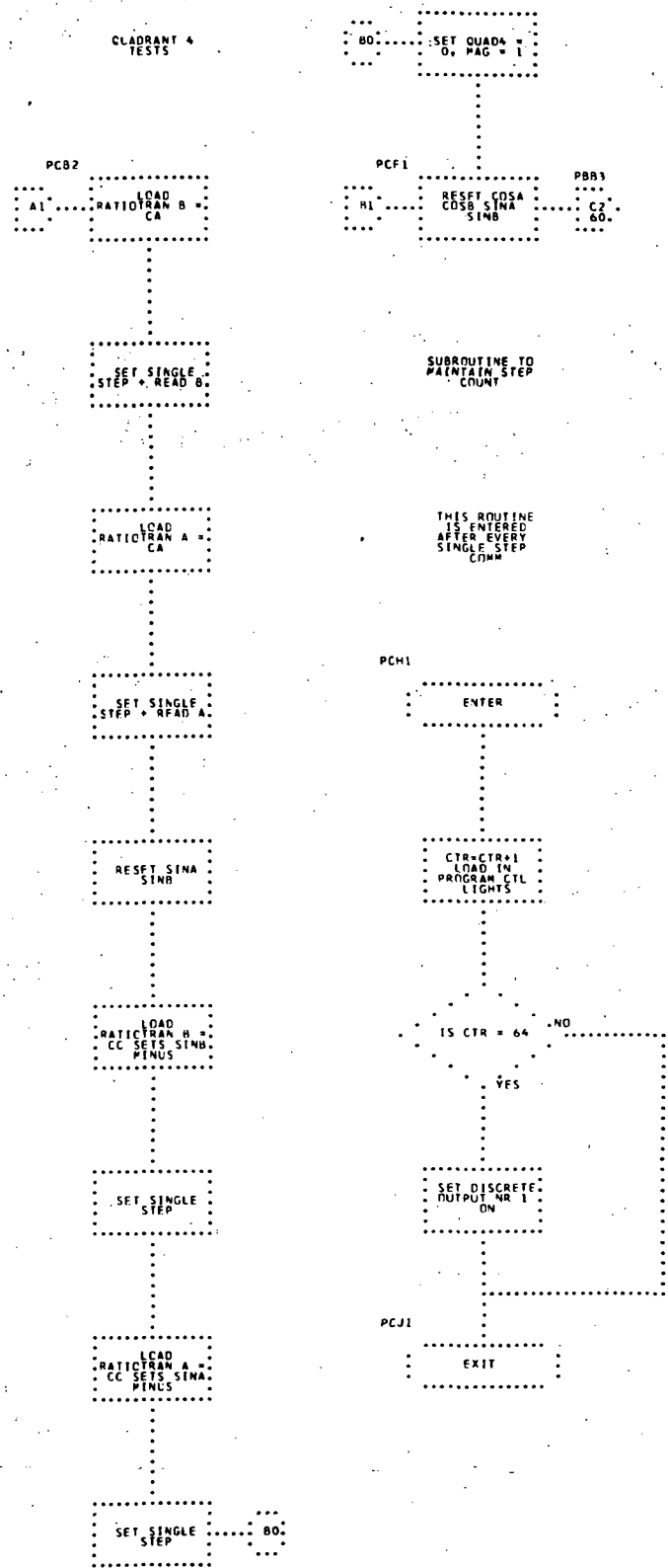


Figure 7-12. PTC ADAPT Self-Test Program Flow Diagram (Sheet 62)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	UFC	VARIABLE	COMMENT	SEC	NO
0	0	0	0					0				TAPE	6001236		20	
0	17							0				DOC	0,17,0		30	
0	17							0				BSS	15		40	
0	17							20			H17P2	HPC	L17P2		50	
0	17							21			ZENG	OCI	000000000		60	
0	17							22			RH	OCI	000000010		70	
0	17							23	130144130		H2P1	HPC	L2P1		80	
0	17							24			H9P3	HPC	L7P3		90	
0	17							25	140066210		H43P2	HPC	L43P2		100	
0	17							26	100136700		H8P1A	HPC	L8P1		110	
0	17							27	130020210		H95P1	HPC	L95P1		120	
0	17							28	160000560		H95P7	HPC	L95P7		130	
0	17							30	160001160		HJAJ5	HPC	JAJ5		140	
0	17							31	501047200		HJAJ5B	HPC	JAJ5B		150	
0	17							32	501052200		K1	OCI	000000002		160	
0	17							33	2		K77	OCI	777777776		170	
0	17							34	777777776		K1303	OCI	130300000		180	
0	17							35	130300000		K1324	OCI	000001520		190	
0	17							36	1520		K51	OCI	002000000		200	
0	17							37	2000000		K52	OCI	000000100		210	
0	17							40	100		KX1	OCI	000000100		220	
0	17							41	7777776		KX2	OCI	000777776		230	
0	17							42	270000000		KX3	OCI	270000000		240	
0	17							43	260000000		KX4	OCI	260000000		250	
0	17							44	250000000		KX5	OCI	250000000		260	
0	17							45	240000000		KX6	OCI	240000000		270	
0	17							46	777000000		KX7	OCI	777000000		280	
0	17							47	37740		KX8	OCI	777740036		290	
0	17							50	777740036		LC2	OCI	000000000		300	
0	17							51	0		LC3	OCI	000000000		310	
0	17							52	0		LC5	OCI	000000000		320	
0	17							53	0		LC7	OCI	000000000		330	
0	17							54	0		LC8	OCI	000000000		340	
0	17							55	0		LCR2	OCI	000000000		350	
0	17							56	0		LCR3	OCI	000000000		360	
0	17							57	0		LCR4	OCI	000000000		370	
0	17							60	0		LCR5	OCI	000000000		380	
0	17							61	0		LCR6	OCI	000000000		390	
0	17							62	0		LCR7	OCI	000000000		400	
0	17							63	0		LCR8	OCI	000000000		410	
0	17							64	0		LCR9	OCI	000000000		420	
0	17							65	0		LCR10	OCI	000000000		430	
0	17							66	0		LCR11	OCI	000000000		440	
0	17							67	0		LCR12	OCI	000000000		450	
0	17							70	0		VAR1	OCI	000000000		460	
0	17							71	0		VAR2	OCI	000000000		470	
0	17							72	0		VAR3	OCI	000000000		480	
0	17							73	0		VAR4	OCI	000000000		490	
0	17							74	0		VAR5	OCI	000000000		500	
0	17							75	0		INTINC	OCI	000000000		510	
0	17							76	0		TEMP	OCI	000000000		520	
0	17							77	0		TEMP1	OCI	000000000		530	
0	17							100	0		STOP	OCI	000000000		540	
0	17							101	0		CTR	OCI	000000000		550	
0	17							102	0		CTR3	OCI	000000000		560	
0	17							103	0		HSTRN	OCI	000000000		570	
0	17							104	610000000		CHAR	OCI	610000000		580	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 1 of 171)

IM	IS	S	LOC	OP	UM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	17							105	620000000			OC1	620000000	B	590	
0	17							106	630000000			OC1	630000000	C	600	
0	17							107	640000000			OC1	640000000	D	610	
0	17							110	650000000			OC1	650000000	E	620	
0	17							111	660000000			OC1	660000000	F	630	
0	17							112	670000000			OC1	670000000	G	640	
0	17							113	700000000		C7	OC1	700000000	H	650	
0	17							114	710000000			OC1	710000000	I	660	
0	17							115	410000000		C9	OC1	410000000	J	670	
0	17							116	420000000			OC1	420000000	K	680	
0	17							117	430000000			OC1	430000000	L	690	
0	17							120	440000000			OC1	440000000	M	700	
0	17							121	450000000			OC1	450000000	N	710	
0	17							122	460000000			OC1	460000000	O	720	
0	17							123	470000000			OC1	470000000	P	730	
0	17							124	500000000			OC1	500000000	Q	740	
0	17							125	510000000			OC1	510000000	R	750	
0	17							126	220000000			OC1	220000000	S	760	
0	17							127	230000000			OC1	230000000	T	770	
0	17							130	240000000			OC1	240000000	U	780	
0	17							131	250000000			OC1	250000000	V	790	
0	17							132	260000000			OC1	260000000	W	800	
0	17							133	270000000			OC1	270000000	X	810	
0	17							134	300000000			OC1	300000000	Y	820	
0	17							135	310101010			OC1	310101010	Z	830	
0	17							136	100000000		C26	OC1	010000000	1	840	
0	17							137	200000000		C27	OC1	020000000	2	850	
0	17							140	300000000		C28	OC1	030000000	3	860	
0	17							141	400000000		C29	OC1	040000000	4	870	
0	17							142	500000000			OC1	050000000	5	880	
0	17							143	600000000		C31	OC1	060000000	6	890	
0	17							144	700000000			OC1	070000000	7	900	
0	17							145	100000000			OC1	100000000	8	910	
0	17							146	110000000			OC1	110000000	9	920	
0	17							147	120000000			OC1	120000000	0	930	
0	17							150	130000000		C36	OC1	130000000	SPECIAL	940	
0	17							151	200000000		C37	OC1	200000000	CHARS	950	
0	17							152	210000000		C38	OC1	210000000		960	
0	17							153	330000000			OC1	330000000		970	
0	17							154	400000000		C40	OC1	400000000		980	
0	17							155	530000000			OC1	530000000		990	
0	17							156	600000000		C42	OC1	600000000		1000	
0	17							157	730000000			OC1	730000000		1010	
0	17							160	0			OC1	000000000		1020	
0	17							161	140000000		C45	OC1	140000000	SPACE	1030	
0	17							162	150000000			OC1	150000000	UPPER	1040	
0	17							163	160000000			OC1	160000000	CASE	1050	
0	17							164	170000000			OC1	170000000		1060	
0	17							165	320000000			OC1	320000000		1070	
0	17							166	340000000			OC1	340000000		1080	
0	17							167	350000000			OC1	350000000		1090	
0	17							170	360000000			OC1	360000000		1100	
0	17							171	370000000			OC1	370000000		1110	
0	17							172	520000000			OC1	520000000		1120	
0	17							173	540000000			OC1	540000000		1130	
0	17							174	550000000			OC1	550000000		1140	
0	17							175	560000000			OC1	560000000		1150	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 2)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OC	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	17							176	570000000			GCT	570000000		1160	
0	17							177	720000000			GCT	720000000		1170	
0	17							200	740000000	C60		GCT	740000000		1180	
0	17							201	750000000			GCT	750000000		1190	
0	17							202	760000000			GCT	760000000		1200	
0	17							203	770000000			GCT	770000000		1210	
0	17							204	110000000			GCT	110000000		1220	
0	17							205	210000000	C64		GCT	210000000		1230	
0	17							206	310000000			GCT	310000000		1240	
0	17							207	410000000			GCT	410000000		1250	
0	17							210	510000000			GCT	510000000		1260	
0	17							211	610000000			GCT	610000000		1270	
0	17							212	710000000			GCT	710000000		1280	
0	17							213	100000000			GCT	100000000		1290	
0	17							214	500000000			GCT	500000000		1300	
0	17							215	110000000			GCT	110000000		1310	
0	17							216	150000000			GCT	150000000		1320	
0	17							217	210000000			GCT	210000000		1330	
0	17							220	250000000			GCT	250000000		1340	
0	17							221	310000000			GCT	310000000		1350	
0	17							222	350000000			GCT	350000000		1360	
0	17							223	410000000			GCT	410000000		1370	
0	17							224	450000000			GCT	450000000		1380	
0	17							225	510000000			GCT	510000000		1390	
0	17							226	400000000			GCT	400000000		1400	
0	17							227	100000000			GCT	100000000		1410	
0	17							230	200000000			GCT	200000000		1420	
0	17							231	400000000			GCT	400000000		1430	
0	17							232	100000000			GCT	100000000		1440	
0	17							233	200000000			GCT	200000000		1450	
0	17							234	RORC			BCI			1460	
0	17							235	ZNVO			BCI			1470	
0	17							236	7*OV			BCI			1480	
0	17							237	GVKT			BCI				
0	17							240	ZBVO			BCI				
0	17							241	CHPV			BCI				
0	17							242	FRZC			BCI				
0	17							243	VR00			BCI				
0	17							244	CHPV			BCI				
0	17							245	O/LL			BCI				
0	17							246	O/LP			BCI				
0	17							247	Y/ND			BCI				
0	17							250	MVRZ			BCI				
0	17							251	T0ZN			BCI				
0	17							252	OSL/			BCI				
0	17							253	TK00			BCI				
0	17							254	/STU			BCI				
0	17							255	VHXY			BCI				
0	17							256	ZJKL			BCI				
0	17							257	MNUP			BCI				
0	17							260	QRBC			BCI				
0	17							261	DEFG			BCI				
0	17							262	HI*1			BCI				
0	17							263	2345			BCI				
LINE1 BCI TYPE ALL ALPHANUMERIC IN BLACKS 1470																
LINE3 RCI ABCDEFGHIJKLMNOPQRSTUVWXYZ,1234567890S 1480																

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 3)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	17							264	6789							
0	17							265	0000							
0	17							266	141516170	LINE4	OCT		141516170	SPECIAL CHARACTERS		1490
0	17							267	323435360		OCT		323435360			1500
0	17							270	372052210		OCT		372052210			1510
0	17							271	565772740		OCT		565772740			1520
0	17							272	757677130		OCT		757677130			1530
0	17							273	543355400		OCT		543355400			1540
0	17							274	536073000		OCT		536073000			1550
0	0	0	0					300		LINE5	DOG		0.17:300			1560
0	17							300	CHPV		BCI		TYPE OCTAL CHARACTERS\$			1570
0	17							301	001C							
0	17							302	/LOT							
0	17							303	Y/R/							
0	17							304	TCVR							
0	17							305	8000							
0	17							306	12345670	LINE5A	OCT		012345670			1580
0	17							307	CHPV		BCI		TYPE DECIMAL INTEGERS IN RED\$			1590
0	17							310	OUVT							
0	17							311	ZM/L							
0	17							312	OZNC							
0	17							313	VXVR							
0	17							314	80ZN							
0	17							315	ORVU							
0	17							316	0000							
0	17							317	44321260	LINE6A	OCT		044321260			1600
0	17							320	361150000	LINE68	OCT		361150000			1610
0	17							321	150055500	H30P2A	HPC		L30P2A			1620

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 4)

IM	IS	LUC	OP	DM	DS	Y	ADR	OCT.	VAL	LHS	RPC	VARIABLE	COMMENT	SEC	NO
0	0	0	0	0	0	0	0	130074000	H5P3	HPC	ORG	L5P3		1640	
0	0	0	0	0	0	0	1	130077400	H5P4	HPC		L5P4		1650	
0	0	0	0	0	0	0	2	130103000	H5P5	HPC		L5P5		1660	
0	0	0	0	0	0	0	3	130107000	H5P6	HPC		L5P6		1670	
0	0	0	0	0	0	0	4	130175600	H5P7	HPC		L5P7		1680	
0	0	0	0	0	0	0	5	130114000	H6P1	HPL		L6P1		1690	
0	0	0	0	0	0	0	6	130116400	H6P2	HPL		L6P2		1700	
0	0	0	0	0	0	0	7	130125400	H6P3	HPC		L6P3		1710	
0	0	0	0	0	0	0	10	130132000	H6P4	HPC		L6P4		1720	
0	0	0	0	0	0	0	11	130137000	H6P5	HPC		L6P5		1730	
0	0	0	0	0	0	0	12	130143000	H6P6	HPC		L6P6		1740	
0	0	0	0	0	0	0	13	130146400	H6P7	HPC		L6P7		1750	
0	0	0	0	0	0	0	14	130152400	H6P8	HPC		L6P8		1760	
0	0	0	0	0	0	0	15	130156400	H6P9	HPC		L6P9		1770	
0	0	0	0	0	0	0	16	130162000	H6P10	HPC		L6P10		1780	
0	0	0	0	0	0	0	17	130164000	H6P11	HPC		L6P11		1790	
0	0	0	0	0	0	0	20	130171400	H6P12	HPC		L6P12		1800	
0	0	0	0	0	0	0	21	13000200	H6P13	HPC		L6P13		1810	
0	0	0	0	0	0	0	22	130003600	H6P14	HPC		L6P14		1820	
0	0	0	0	0	0	0	23	130007200	H6P15	HPC		L6P15		1830	
0	0	0	0	0	0	0	24	130013200	H6P16	HPC		L6P16		1840	
0	0	0	0	0	0	0	25	130016570	H6P17	HPC		L6P17		1850	
0	0	0	0	0	0	0	26	130022600	H6P18	HPL		L6P18		1860	
0	0	0	0	0	0	0	27	130026200	H6P19	HPC		L6P19		1870	
0	0	0	0	0	0	0	30	130031600	H6P20	HPC		L6P20		1880	
0	0	0	0	0	0	0	31	130035600	H6P21	HPC		L6P21		1890	
0	0	0	0	0	0	0	32	130041200	H6P22	HPC		L6P22		1900	
0	0	0	0	0	0	0	33	130044600	H6P23	HPC		L6P23		1910	
0	0	0	0	0	0	0	34	130050200	H7P1	HPC		L7P1		1920	
0	0	0	0	0	0	0	35	130051600	H7P2	HPC		L7P2		1930	
0	0	0	0	0	0	0	36	130057200	H7P3	HPC		L7P3		1940	
0	0	0	0	0	0	0	37	130062600	H7P4	HPC		L7P4		1950	
0	0	0	0	0	0	0	40	130066200	H7P5	HPC		L7P5		1960	
0	0	0	0	0	0	0	41	130071600	H7P6	HPC		L7P6		1970	
0	0	0	0	0	0	0	42	130076200	H7P7	HPC		L7P7		1980	
0	0	0	0	0	0	0	43	130101600	H7P8	HPL		L7P8		1990	
0	0	0	0	0	0	0	44	130105200	H7P9	HPC		L7P9		2000	
0	0	0	0	0	0	0	45	130111200	H7P10	HPC		L7P10		2010	
0	0	0	0	0	0	0	46	130115200	H7P11	HPC		L7P11		2020	
0	0	0	0	0	0	0	47	130121200	H7P12	HPC		L7P12		2030	
0	0	0	0	0	0	0	50	130125200	H7P13	HPC		L7P13		2040	
0	0	0	0	0	0	0	51	130131200	H7P14	HPC		L7P14		2050	
0	0	0	0	0	0	0	52	130135200	H7P15	HPC		L7P15		2060	
0	0	0	0	0	0	0	53	130140600	H7P16	HPC		L7P16		2070	
0	0	0	0	0	0	0	54	130144200	H7P17	HPC		L7P17		2080	
0	0	0	0	0	0	0	55	130150200	H7P18	HPC		L7P18		2090	
0	0	0	0	0	0	0	56	130154200	H7P19	HPC		L7P19		2100	
0	0	0	0	0	0	0	57	130157600	H7P20	HPL		L7P20		2110	
0	0	0	0	0	0	0	60	130163200	H7P21	HPC		L7P21		2120	
0	0	0	0	0	0	0	61	130167200	H7P22	HPC		L7P22		2130	
0	0	0	0	0	0	0	62	130001410	H7P23	HPC		L7P23		2140	
0	0	0	0	0	0	0	63	130005410	H7P24	HPC		L7P24		2150	
0	0	0	0	0	0	0	64	130011410	H7P25	HPC		L7P25		2160	
0	0	0	0	0	0	0	65	130015410	H7P26	HPC		L7P26		2170	
0	0	0	0	0	0	0	66	130021410	H7P27	HPC		L7P27		2180	
0	0	0	0	0	0	0	67	130025010	H7P28	HPC		L7P28		2190	
														2200	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 5)

TM	IS	S	LUC	UP	DM	DS	9	AUR	NCT	VAL	L/S	OPC	VARIABLE	COMMENT	SEC	NO
0	13							70	130030410	H7P29	HPC	L7P29			2210	
0	13							71	130046410	H7P30	HPC	L7P30			2220	
0	13							72	130042410	H7P31	HPC	L7P31			2230	
0	13							73	130046410	H7P32	HPC	L7P32			2240	
0	13							74	130052410	H7P33	HPC	L7P33			2250	
0	13							75	130056410	H7P34	HPC	L7P34			2260	
0	13							76	130062410	H7P35	HPC	L7P35			2270	
0	13							77	130066410	H7P36	HPC	L7P36			2280	
0	13							100	130072010	H7P37	HPC	L7P37			2290	
0	13							101	130075410	H7P38	HPC	L7P38			2300	
0	13							102	130101410	H7P39	HPC	L7P39			2310	
0	13							103	130105410	H7P40	HPC	L7P40			2320	
0	13							104	130111410	H7P41	HPC	L7P41			2330	
0	13							105	130116410	H7P42	HPC	L7P42			2340	
0	13							106	130122410	H7P43	HPC	L7P43			2350	
0	13							107	130126410	H7P44	HPC	L7P44			2360	
0	13							110	130132010	H7P45	HPC	L7P45			2370	
0	13							111	130135410	H7P46	HPC	L7P46			2380	
0	13							112	130143410	H7P47	HPC	L7P47			2390	
0	13							113	130147410	H7P48	HPC	L7P48			2400	
0	13							114	130153410	H7P49	HPC	L7P49			2410	
0	13							115	130157410	H7P50	HPC	L7P50			2420	
0	13							116	130163410	H7P51	HPC	L7P51			2430	
0	13							117	130167410	H7P52	HPC	L7P52			2440	
0	13							120	130001210	H7P53	HPC	L7P53			2450	
0	13							121	130007430	H7P54	HPC	L7P54			2460	
0	13							122	130013430	H7P54B	HPC	L7P54B			2470	
0	13							123	130020210	H8P1	HPC	L8P1			2480	
0	13							124	130024210	H8P2	HPC	L8P2			2490	
0	13							125	130030210	H8P3	HPC	L8P3			2500	
0	13							126	130034210	H8P4	HPC	L8P4			2510	
0	13							127	130040210	H8P5	HPC	L8P5			2520	
0	13							130	130044210	H8P6	HPC	L8P6			2530	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 6)

IM	IS	S	LOC	IP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	0	0	0	17	0	13	1	020				PROGRAM	ENTRANCE.		2550	
0	0	0	1	13	0	13	1	075			L1P1	CLA	ZERO		2560	
0	0	0	2	13	0	13	1	100				STU	INTIND		2570	
0	0	0	3	13	0	13	1	101				STC	STOP		2580	
0	0	0	4	13	0	13	1	054				STU	CTK		2590	
0	0	0	5	16	1	13	233					STU	LCR		2600	
0	0	0	6	13	1	13	000					STC	1,13		2610	
0	0	0	7	13	1	13	001					STU	TIME		2620	
0	0	0	10	13	1	13	002					STO	CSCTR		2630	
0	0	0	11	16	0	13	213					STU	DDCTR		2640	
0	0	0	12	5	0	13	214					CCS	0,13		2650	
0	0	0	13	14	0	13	015					CTU	214		2660	
0	0	0	14	10	0	13	016					TML	L1P1A		2670	
0	0	0	15	00	0	13	132		160010160			TRA	L2P1		2680	
0	0	0	16	17	0	13	172				L2P1	TRA*	L1P1A1		2690	
0	0	0	17	7	0	13	133		000000002			CLA	VAP3		2700	
0	0	0	20	13	0	13	172					ACL	=0000000002		2710	
0	0	0	21	5	0	13	204					STU	VAK3		2720	
0	0	0	22	17	0	13	1020					CTC	Z04		2730	
0	0	0	23	13	0	13	1073					CLA	ZEP0		2740	
0	0	0	24	13	0	13	1074					STU	VAK4		2750	
0	0	0	25	5	0	13	214					STU	VAK5		2760	
0	0	0	26	7	0	13	1032					CTC	Z14	ASHT	2770	
0	0	0	27	16	0	13	001					ACL	K1		2780	
0	0	0	30	13	0	13	134					SHL	I		2790	
0	0	0	31	16	0	13	001					STO	LCN1	A1	2800	
0	0	0	32	13	0	13	1055					SHL	I		2810	
0	0	0	33	16	0	13	001					STC	LCX2	A2	2820	
0	0	0	34	13	0	13	1056					SHL	I		2830	
0	0	0	35	16	0	13	001					STU	LCN3	A3	2840	
0	0	0	36	13	0	13	1057					SHL	I		2850	
0	0	0	37	16	0	13	001					STC	LCX4	A4	2860	
0	0	0	40	13	0	13	1060					SHL	I		2870	
0	0	0	41	16	0	13	001					STU	LCX5	A5	2880	
0	0	0	42	13	0	13	1061					SHL	I		2890	
0	0	0	43	16	0	13	001					STC	LCX6	A6	2900	
0	0	0	44	13	0	13	1062					SHL	I		2910	
0	0	0	45	16	0	13	001					STU	LCR7	A7	2920	
0	0	0	46	13	0	13	1063					SHL	I		2930	
0	0	0	47	16	0	13	001					STU	LCX8	A8	2940	
0	0	0	50	13	0	13	1064					SHL	I		2950	
0	0	0	51	16	0	13	001					STC	LCX9	A9	2960	
0	0	0	52	13	0	13	1065					SHL	I		2970	
0	0	0	53	16	0	13	001					STC	LCR10	A10	2980	
0	0	0	54	13	0	13	1066					SHL	I		2990	
												STU	LCR11	ALL	3000	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 7)

IM	IS	S	LOC	UP	DM	DS	9	ADR	DCF	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NC
0	0	0	55	16	0	13	001					SHL	I		3010	
0	0	0	56	13	0	13	067					STU	LCR12	A12	3020	
0	0	0	57	16	0	13	001					SHL	I		3030	
0	0	0	60	13	0	13	135					STC	LC1	A13	3040	
0	0	0	61	16	0	13	001					SHL	I		3050	
0	0	0	62	13	0	13	050					STU	LC2	A14	3060	
0	0	0	63	16	0	13	001					SHL	I		3070	
0	0	0	64	13	0	13	051					STC	LC3	A15	3080	
0	0	0	65	16	0	13	001					SHL	I		3090	
0	0	0	66	14	0	13	070					TMI	L2P2	A16	3100	
0	0	0	67	10	0	13	071					TRA	L3P1		3110	
0	0	0	70	00	0	13	136	160003760			L2P2	TRA*	L97P1		3120	
0	0	0	71	17	0	13	135				L3P1	CLA	LC1		3140	
0	0	0	72	14	0	13	074					TMI	**2		3150	
0	0	0	73	10	0	13	164					TRA	L5P1		3160	
0	0	0	74	17	0	13	134					CLA	LCR1		3170	
0	0	0	75	14	0	13	123					TMI	L4P1		3180	
0	0	0	76	17	0	13	055					CLA	LCR2		3190	
0	0	0	77	14	0	13	126					TMI	L4P2		3200	
0	0	0	100	17	0	13	056					CLA	LCR3		3210	
0	0	0	101	14	0	13	131					TMI	L4P3		3220	
0	0	0	102	17	0	13	057					CLA	LCR4		3230	
0	0	0	103	14	0	13	134					TMI	L4P4		3240	
0	0	0	104	17	0	13	060					CLA	LCR5		3250	
0	0	0	106	17	0	13	137					TMI	L4P5		3260	
0	0	0	107	14	0	13	142					CLA	LCR6		3270	
0	0	0	110	17	0	13	062					TMI	L4P6		3280	
0	0	0	111	14	0	13	145					CLA	LCR7		3290	
0	0	0	112	17	0	13	063					TMI	L4P7		3300	
0	0	0	113	14	0	13	150					CLA	LCR8		3310	
0	0	0	114	17	0	13	064					TMI	L4P8		3320	
0	0	0	115	14	0	13	153					CLA	LCR9		3330	
0	0	0	116	17	0	13	065					TMI	L4CP1		3340	
0	0	0	117	14	0	13	156					CLA	LCR10		3350	
0	0	0	120	17	0	13	066					TMI	L4CP2		3360	
0	0	0	121	14	0	13	161					CLA	LCR11		3370	
0	0	0	122	10	0	13	016					TRA	L2P1		3390	
0	0	0	123	17	0	13	020				L4P1	CLA	ZERO		3400	
0	0	0	124	13	0	13	055					STU	LCR2		3410	
0	0	0	125	10	0	13	167					TRA	L5P2		3420	
0	0	0	126	17	0	13	020					CLA	ZERK		3430	
0	0	0	127	13	0	13	056					STU	LCR3		3440	
0	0	0	130	10	0	13	235				L4P3	TRA	L6P2		3450	
0	0	0	131	17	0	13	020					CLA	ZERO		3460	
0	0	0	132	13	0	13	137	140062210				STU	LCR4		3470	
0	0	0	133	00	0	13	137					TRA*	L9P2		3480	
0	0	0	134	17	0	13	020				L4P4	CLA	ZERU		3490	
0	0	0	135	13	0	13	060					STU	LCR5		3500	
0	0	0	136	00	0	13	142	150037660			L4P5	TRA*	L20P2		3510	
0	0	0	137	17	0	13	020					CLA	ZERU		3520	

TO ROUTINE 1
TO ROUTINE 2

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 8)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	0	0	140	13	0	13	1	061				STO	LCR6		3530	
0	0	0	141	00	0	13	1	143	120020500		L4P6	TRA*	L29P2		3540	
0	0	0	142	17	0	13	1	020				CLA	ZERO		3550	
0	0	0	143	13	0	13	1	062				STO	LCR7		3560	
0	0	0	144	00	0	13	1	144	150002710		L4P7	TRA*	L45P2		3570	
0	0	0	145	17	0	13	1	020				CLA	ZERO		3580	
0	0	0	146	13	0	13	1	063				STO	LCR8		3590	
0	0	0	147	00	0	13	1	145	110005110		L4P8	TRA*	L50P2		3600	
0	0	0	150	17	0	13	1	020				CLA	ZERO		3610	
0	0	0	151	13	0	13	1	064				STO	LCR9		3620	
0	0	0	152	00	0	13	1	146	050001240		L4CP1	TRA*	L60P2		3630	
0	0	0	153	17	0	13	1	020				CLA	ZERO		3640	
0	0	0	154	13	0	13	1	065	501004000		L4CP2	TRA*	LCR10		3650	
0	0	0	155	00	0	13	1	147				STO	JAB1		3660	
0	0	0	156	17	0	13	1	020				CLA	ZERO		3670	
0	0	0	157	13	0	13	1	066				STO	LCR11		3680	
0	0	0	160	00	0	13	1	150	511010050		L4CP3	TRA*	MAB1		3690	
0	0	0	161	17	0	13	1	020				CLA	ZERO		3700	
0	0	0	162	13	0	13	1	067				STO	LCR12		3710	
0	0	0	163	00	0	13	1	151	531020270		LSP1	TRA*	MAB1		3720	
0	0	0	164	17	0	13	1	134				CLA	LCR1		3730	
0	0	0	165	14	0	13	1	167				TMI	LSP2		3740	
0	0	0	166	10	0	13	230					TRA	L6P1		3750	
															3760	
															3770	
															3780	
															3790	
															3800	
															3810	
															3820	
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															3950	
															3960	
															3970	
															3980	
															3990	
															4000	
															4010	
															4020	
															4030	
															4040	
															4050	
															4060	
															4070	
															4080	
															4090	
															4090	

BEGINNING OF ROUTINE ONE
CHECK COMPUTER FOR ABILITY TO HOP TO ALL SECTORS.

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 9)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	10	1	77	0	0	16	367	160127710			LSP2H	HOP	MP9		4100	
				0	0	16	367				MP9	MPC	LSP2I		4110	
0	11	1	257	0	0	16	370				•	SECTOR 11.		4120		
0	11	1	257	0	0	16	370	160000120			LSP2I	HOP	.11.1.257.16,	4130		
				0	0	16	370				MP10	HPC	LSP2J	4140		
0	12	0	0	0	0	16	371				•	SECTOR 12.		4150		
0	12	0	0	0	0	16	371				LSP2J	HOP	.12.1.16,	4160		
				0	0	16	371	160177330			MP11	HPC	LSP2K	4170		
0	13	1	376	0	0	16	372				•	SECTOR 13.		4180		
0	13	1	376	0	0	16	372	160014140			LSP2K	HOP	.13.1.376.16,	4190		
				0	0	16	372				MP12	HPC	LSP2L	4200		
0	14	0	30	0	0	16	373				•	SECTOR 14.		4210		
0	14	0	30	0	0	16	373	160177150			LSP2L	HOP	.14.1.30.16,	4220		
				0	0	16	373				MP13	HPC	LSP2M	4230		
0	15	0	376	0	0	16	374				•	SECTOR 15.		4240		
0	15	0	376	0	0	16	374	160000160			LSP2M	HOP	.15.1.376.16,	4250		
				0	0	16	374				MP14	HPC	LSP2N	4260		
0	16	0	0	0	0	16	376				•	SECTOR 16.		4270		
0	16	0	0	0	0	16	376	160151370			LSP2N	HOP	.16.1.0.16.376	4280		
				0	0	16	376				MP15	HPC	LSP2P	4290		
0	17	1	277	0	0	16	377				•	SECTOR 17.		4300		
0	17	1	277	10	0	16	322				LSP2P	HOP	.17.1.277.16,	4310		
0	17	1	322	0	0	16	377	401000000			•	TRA...		4320		
				0	0	16	377				LSP2P	HOP	MP16	4330		
1	0	0	0	1	0	1	0				MP16	HPC	LSP2Q	4340		
1	0	0	0	1	0	001	1				•	MEMORY MODULE 1		4400		
				0	1	0	1	411000610			•	SECTOR 0 MMI		4410		
1	1	1	1	1	1	1	2				LSP2Q	HOP	1.1.1.1.1.1.2	4420		
1	1	1	1	0	1	1	002				MP17	HPC	LSP2R	4430		
1	1	1	1	1	1	1	2	421001020			•	SECTOR 1 MMI		4440		
1	2	0	2	0	1	2	003				LSP2R	HOP	MP18	4450		
1	2	0	2	0	1	2	3	431001430			MP18	HPC	LSP2S	4460		
1	3	0	3	0	1	3	004				•	SECTOR 2 MMI		4470		
1	3	0	3	0	1	3	4	441002040			LSP2S	HOP	1.2.1.1.2.3	4480		
				0	1	3	4				MP19	HPC	LSP2T	4490		
1	4	0	4	0	1	4	005				•	SECTOR 3 MMI		4500		
1	4	0	4	0	1	4	5	451002650			LSP2T	HOP	1.3.1.1.3.4	4510		
				0	1	4	5				MP20	HPC	LSP2U	4520		
1	5	1	5	1	5	6	6				•	SECTOR 4 MMI		4530		
1	5	1	5	0	1	5	006				LSP2U	HOP	1.4.1.1.4.5	4540		
				0	1	5	6	461030060			MP21	HPC	LSP2V	4550		
1	5	1	5	1	5	6	6				•	SECTOR 5 MMI		4560		
1	5	1	5	0	1	5	006				LSP2V	HOP	1.5.1.1.5.6	4570		
				0	1	5	6				MP22	HPC	LSP2W	4580		
				0	1	5	6				•	SECTOR 6 MMI		4590		
				0	1	5	6							4600		
				0	1	5	6							4610		
				0	1	5	6							4620		
				0	1	5	6							4630		
				0	1	5	6							4640		
				0	1	5	6							4650		

GENERATED TRANSFER

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 10)

IM	IS	S	LOC	OP	OM	OS	9	ADR	OCT	VAL	LWS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	0	60	0	1	6	7				LSP2M	ORG	1,6,,60,1,6,7		4660	
1	6	0	60	0	1	6	007				HP23	HOP	HP23		4670	
1	7	0	37	0	1	7	17		471017470		•	SECTOR 7			4680	
1	7	0	37	0	1	7	017				LSP2X	HOP	1,7,,37,1,7,17		4690	
1	7	0	37	0	1	7	17		501040100		•	SECTOR 10 MMI		4700		
1	10	0	100	0	1	10	27				LSP2Y	HOP	1,10,,100,1,10,27		4710	
1	10	0	100	0	1	10	027				HP25	HPC	HP25		4720	
1	11	0	200	0	1	11	37		511100110		•	SECTOR 11 MMI		4730		
1	11	0	200	0	1	11	037				LSP2Z	HOP	1,11,,200,1,11,37		4740	
1	11	0	200	0	1	11	37		521177120		•	SECTOR 12 MMI		4750		
1	12	0	376	0	1	12	377				LSP2AA	HOP	1,12,,376,1,12,377		4760	
1	12	0	376	0	1	12	377				HP27	HPC	HP27		4770	
1	13	0	376	0	1	13	377		531177130		•	SECTOR 13 MMI		4780		
1	13	0	376	0	1	13	377				LSP2BB	HOP	1,13,,376,1,13,377		4790	
1	13	0	376	0	1	13	377		541077540		•	SECTOR 14 MMI		4800		
1	14	0	177	0	1	14	377				LSP2CC	HOP	1,14,,177,1,14,377		4810	
1	14	0	177	0	1	14	377				HP29	HPC	HP29		4820	
1	15	0	7	0	1	15	177		551003550		•	SECTOR 15 MMI		4830		
1	15	0	7	0	1	15	177				LSP2DD	HOP	1,15,,7,1,15,177		4840	
1	15	0	7	0	1	15	177		561000360		•	SECTOR 16 MMI		4850		
1	16	1	0	0	1	16	100				LSP2EE	HOP	1,16,1,,1,16,100		4860	
1	16	1	0	0	1	16	100				HP31	HPC	HP31		4870	
1	17	1	375	0	1	17	77		571176770		•	SECTOR 17 MMI		4880		
1	17	1	375	0	1	17	077				LSP2FF	HOP	1,17,1,,375,1,17,77		4890	
1	17	1	375	0	1	17	77		130074000		•	SECTOR 18 MMI		4900		
											MP32	HPC	MP32		4910	
											LSP3	HPC	LSP3		4920	
											LSP3	HPC	LSP3		4930	
											LSP3	HPC	LSP3		4940	
											LSP3	HPC	LSP3		4950	
											LSP3	HPC	LSP3		4960	
											LSP3	HPC	LSP3		4970	
											LSP3	HPC	LSP3		4980	
											LSP3	HPC	LSP3		4990	
											LSP3	HPC	LSP3		5000	
											LSP3	HPC	LSP3		5010	
											LSP3	HPC	LSP3		5020	
											LSP3	HPC	LSP3		5030	
											LSP3	HPC	LSP3		5040	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 11)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	0	0	373		0	13		132					BEGIN CHECK OF TRANSFER CLASS INSTRUCTIONS.	5060		
0	0	0	373	10	0	13		226					ORG ..373..13,	5070		
0	0	0	373		0	13		226					TRA L5P7A	5080		
0	0	1	373		0	13		133					TEST TRA TO SYLL 1	5090		
0	0	1	373	17	0	13		152	500000000				ORG ..1.373..13,	5100		
0	0	1	374	10	0	13		226					CLA -050000000	5110		
0	0	1	374		0	13		226					TRA L5P7A	5120		
0	0	0	170		0	13		134					TEST TMI INSTRUCTION.	5130		
0	0	0	170		0	13		134					ORG ..170..13,	5140		
0	0	0	170	17	0	13		000					CLA H5P3	5150		
0	0	0	171	13	0	13		070					STO VARI	5160		
0	0	0	172	17	0	13		001					CLA H5P4	5170		
0	0	0	173	13	0	13		071					STO VAR2	5180		
0	0	0	174	17	0	13		153	400000000				CLA -040000000	5190		
0	0	0	175	14	0	13		177					TMI L5P4	5200		
0	0	0	176	0	0	13		026					HOP H95P1	5210		
0	0	0	177	17	0	13		001					TEST TNZ INSTRUCTION.	5220		
0	0	0	200	13	0	13		070					CLA H5P4	5230		
0	0	0	201	17	0	13		002					STO VARI	5240		
0	0	0	202	13	0	13		071					CLA H5P5	5250		
0	0	0	203	17	0	13		133	000000002				STO VAR2	5260		
0	0	0	204	4	0	13		206					CLA -000000002	5270		
0	0	0	205	0	0	13		026					TNZ L5P5	5280		
0	0	0	206	17	0	13		002					HOP H95P1	5290		
0	0	0	207	13	0	13		070					TEST TMI WITH CLEARED ACCUMULATOR.	5300		
0	0	0	210	17	0	13		003					CLA H5P5	5310		
0	0	0	211	13	0	13		071					STO VARI	5320		
0	0	0	212	17	0	13		154	000000000				CLA H5P6	5330		
0	0	0	213	14	0	13		227					STO VAR2	5340		
0	0	0	214	10	0	13		216					CLA -000000000	5350		
0	0	0	215	0	0	13		026					TMI L15P1L	5360		
0	0	0	216	17	0	13		003					TRA L5P4	5370		
0	0	0	217	13	0	13		070					HOP H95P1	5380		
0	0	0	220	17	0	13		004					TEST TNZ WITH CLEARED ACCUMULATOR.	5390		
0	0	0	221	13	0	13		071					CLA H5P6	5400		
0	0	0	222	17	0	13		154	000000000				STO VARI	5410		
0	0	0	223	4	0	13		227					CLA H5P7	5420		
0	0	0	224	10	0	13		1373					STO VAR2	5430		
0	0	0	225	0	0	13		026					CLA -000000000	5440		
0	0	0	226	14	0	13		230					TNZ L15P1L	5450		
0	0	0	227	00	0	13		155	160000560				TRA L5P7	5460		
0	0	0	227	00	0	13		155					HOP H95P1	5470		
0	0	0	227	00	0	13		155					TMI L6P1	5480		
0	0	0	227	00	0	13		155					L15P1L TRA*	5490		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 12)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	0	0	230	17	0	13	1	055							5510	
0	0	0	231	14	0	13	235								5520	
0	0	0	232	4	0	13	234								5530	
0	0	0	233	10	0	13	016								5550	
0	0	0	234	00	0	13	156								5560	
0	0	0	235	17	0	13	006		140057610		L6P1A	TRA*			5570	
0	0	0	236	13	0	13	1 070				L6P2	CLA			5580	
0	0	0	237	17	0	13	007					STO	VAR1		5590	
0	0	0	240	13	0	13	1 071					STO	VAR2		5600	
0	0	0	241	17	0	13	157		777777776			CLA	=0777777776		5610	
0	0	0	242	4	0	13	244					TNZ	**2		5620	
0	0	0	243	00	0	13	155		160000560		TRA*	L95P1			5630	
0	0	0	244	13	0	13	1 077				STO	TEMP1			5640	
0	0	0	245	17	0	13	154		000000000		CLA	-0000000000			5650	
0	0	0	246	17	0	13	1 077				CLA	TEMP1			5660	
0	0	0	247	4	0	13	251				TNZ	L6P2A			5670	
0	0	0	250	00	0	13	155		160000560		TRA*	L95P1			5680	
0	0	0	251	7	0	13	133		000000002		ADC	=0000000002			5690	
0	0	0	252	4	0	13	173				TNZ	L1SP1K			5700	
0	0	0	253	17	0	13	007					CHK	STO WITH ALL ZEROS.		5710	
0	0	0	254	13	0	13	1 070				CLA	H6P3			5720	
0	0	0	255	17	0	13	010				STC	VAR1			5730	
0	0	0	256	13	0	13	1 071				CLA	H6P4			5740	
0	0	0	257	17	0	13	154				STO	VAR2			5750	
0	0	0	260	13	0	13	1 077		000000000		CLA	=0000000000			5760	
0	0	0	261	17	0	13	1 077				STO	TEMP1			5770	
0	0	0	262	17	0	13	157		777777776		CLA	=0777777776			5780	
0	0	0	263	4	0	13	173				CLA	TEMP1			5790	
0	0	0	263	4	0	13	173				TNZ	L1SP1K			5800	
															5810	

Figure 7-13. PTCADAPT Self-Test Program (Sheet 13)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	0	0	264	17	0	13	0	010			L6P4	CLA	H6P4		5830	
0	0	0	265	13	0	13	1	070				STC	VARI	CAN ACCUMULATOR BE FILLED BY ADD.	5840	
0	0	0	266	17	0	13	0	011				CLA	H6P5		5850	
0	0	0	267	13	0	13	1	071				STC	VAR2		5860	
0	0	0	270	17	0	13	1	154	000000000			CLA	=000000000		5870	
0	0	0	271	7	-0	13	1	157	777777776			ACC	=077777776		5880	
0	0	0	272	4	0	13	1	274				TNZ	**2		5890	
0	0	0	273	10	0	13	1	173				TRA	L15PIK		5900	
0	0	0	274	2	0	13	1	157				SUB	=077777776		5910	
0	0	0	275	4	0	13	1	173	777777776			TNZ	L15PIK		5920	
0	0	0	276	17	0	13	0	011				CLA	H6P5	CAN ACCUMULATOR BE CHANGED BY ADDING ZERO	5930	
0	0	0	277	13	0	13	1	070			L6P5	STC	VARI		5940	
0	0	0	300	17	0	13	0	012				CLA	H6P6		5950	
0	0	0	301	13	0	13	1	071				STC	VAR2		5960	
0	0	0	302	17	0	13	1	157	777777776			CLA	=077777776		5970	
0	0	0	303	7	0	13	1	154	000000000			ACC	=000000000		5980	
0	0	0	304	2	0	13	1	157	777777776			SUR	=077777776		6000	
0	0	0	305	4	0	13	1	173				TNZ	L15PIK		6010	
0	0	0	306	17	0	13	0	012				CLA	H6P6	CAN ACCUMULATOR BE CLEARED BY ADD.	6020	
0	0	0	307	13	0	13	1	070			L6P6	STC	VARI		6030	
0	0	0	310	17	0	13	0	013				CLA	H6P7		6040	
0	0	0	311	13	0	13	1	071				STC	VAR2		6050	
0	0	0	312	17	0	13	1	157	777777776			CLA	=077777776		6060	
0	0	0	313	7	0	13	1	133	000000002			ACC	=000000002		6070	
0	0	0	314	4	0	13	1	173				TNZ	L15PIK		6080	
0	0	0	315	17	0	13	0	013			L6P7	CLA	H6P7	SAME AS L5P5 EXCEPT CONSTANTS REVERSED.	6100	
0	0	0	316	13	0	13	1	070				STC	VARI		6110	
0	0	0	317	17	0	13	0	014				CLA	H6P8		6120	
0	0	0	320	13	0	13	1	071				STC	VAR2		6130	
0	0	0	321	17	0	13	1	133	000000002			CLA	=000000002		6140	
0	0	0	322	7	0	13	1	157	777777776			ACC	=077777776		6150	
0	0	0	323	4	0	13	1	173				TNZ	L15PIK		6160	
0	0	0	324	10	0	13	1	325				TRA	L6P8		6170	
0	0	0	325	17	0	13	0	014			L6P8	CLA	H6P8	CHECK FOR CHANGE OF SIGN BIT.	6180	
0	0	0	326	13	0	13	1	070				STC	VARI		6190	
0	0	0	327	17	0	13	0	015				CLA	H6P9		6200	
0	0	0	330	13	0	13	1	071				STC	VAR2		6210	
0	0	0	331	17	0	13	1	160	200000000			CLA	=020000000		6220	
0	0	0	332	7	0	13	1	160	200000000			ACC	=020000000		6230	
0	0	0	333	14	0	13	1	335				TMI	L6P9		6240	
0	0	0	334	10	0	13	1	173				TRA	L15PIK		6250	
0	0	0	335	17	0	13	0	015			L6P9	CLA	H6P9	SAME AS L5P7.	6260	
0	0	0	336	13	0	13	1	070				STC	VARI		6270	
0	0	0	337	17	0	13	0	016				CLA	H6P10		6280	
0	0	0	340	13	0	13	1	071				STC	VAR2		6290	
0	0	0	341	17	0	13	1	153	400000000			CLA	=040000000		6300	
0	0	0	342	7	0	13	1	153	400000000			ACC	=040000000		6310	
0	0	0	343	14	0	13	1	173				TMI	L15PIK		6320	
0	0	0	344	17	0	13	0	016			L6P10	CLA	H6P10	ALL BIT COMBINATIONS ON ADD	6330	
0	0	0	345	13	0	13	1	070				STC	VARI		6340	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 14)

IM	IS	LOC	OP	DM	OS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	0	346	17	0	13		017				CLA	H6P11		6400	
0	0	347	13	0	13	1	071				STG	VARZ		6410	
0	0	350	17	0	13		161	252642550			CLA	=0252642550		6420	
0	0	351	7	0	13		162	107301660			ADD	=0107301660		6430	
0	0	352	2	0	13		163	362144430			SUB	=0362144430		6440	
0	0	353	4	0	13	1	173				TNZ	L15PIK		6450	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 15)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	DPC	VARIABLE	COMMENT	SEQ	NC
0	0	0	354	17	0	13	0	17			L6P11	CLA	H6P11	CHECK SIMPLE SUBTRACTION.	6470	
0	0	0	355	13	0	13	1	070			VAR1	STC	VAR1		6480	
0	0	0	356	17	0	13	1	020			VAR2	CLA	H6P12		6490	
0	0	0	357	13	0	13	1	071			VAR2	STO	VAR2		6500	
0	0	0	360	17	0	13	1	153	400000000			CLA	=0400000000		6510	
0	0	0	361	2	0	13	1	153	400000000			SUB	=0400000000		6520	
0	0	0	362	4	0	13	1	173			TNZ	L15PIK			6530	
0	0	0	363	17	0	13	0	020			L6P12	CLA	H6P12	CHECK SUBTRACTION OF LOW ORDER BIT.	6540	
0	0	0	364	13	0	13	1	070			VAR1	STC	VAR1		6550	
0	0	0	365	17	0	13	0	021			VAR2	CLA	H6P13		6560	
0	0	0	366	13	0	13	1	071			VAR2	STC	VAR2		6570	
0	0	0	367	17	0	13	1	133	000000002			CLA	=0000000002		6580	
0	0	0	370	2	0	13	1	133	000000002			SUB	=0000000002		6590	
0	0	0	371	4	0	13	1	173			TNZ	L15PIK			6600	
0	0	0	372	10	0	13	1	374			TRA**	TRA	L6P13	GENERATED TRANSFER	6610	
0	0	0	374	10	0	13	1	000			ORG	ORG	**1...13.		6620	
0	0	1	0	17	0	13	0	135			L6P13	CLA	H6P13		6630	
0	0	1	1	13	0	13	1	070			VAR1	STO	VAR1		6640	
0	0	1	2	17	0	13	0	022			VAR2	CLA	H6P14		6650	
0	0	1	3	13	0	13	1	071	525252524			CLA	=0525252524		6660	
0	0	1	4	17	0	13	1	164	525252524			STO	VAR2		6670	
0	0	1	5	2	0	13	1	164			SUB	=0525252524		6680		
0	0	1	6	4	0	13	1	173			TNZ	L15PIK		6690		
0	0	1	7	17	0	13	0	022			L6P14	CLA	H6P14	SUBTRACT ALL EVEN BITS.	6700	
0	0	1	10	13	0	13	1	070			VAR1	STC	VAR1		6710	
0	0	1	11	17	0	13	0	023			VAR2	CLA	H6P15		6720	
0	0	1	12	13	0	13	1	071			VAR2	STO	VAR2		6730	
0	0	1	13	17	0	13	1	165	252525252			CLA	=0252525252		6740	
0	0	1	14	2	0	13	1	165	252525252			SUB	=0252525252		6750	
0	0	1	15	4	0	13	1	173			TNZ	L15PIK		6760		
0	0	1	16	17	0	13	0	023			L6P15	CLA	H6P15	FILL ACCUMULATOR WITH SUBTRACT.	6770	
0	0	1	17	13	0	13	1	070			VAR1	STO	VAR1		6780	
0	0	1	20	17	0	13	1	024			VAR2	CLA	H6P16		6790	
0	0	1	21	13	0	13	1	071			VAR2	STO	VAR2		6800	
0	0	1	22	17	0	13	1	154	000000000			CLA	=0000000000		6810	
0	0	1	23	2	0	13	1	133	000000002			SUB	=0000000002		6820	
0	0	1	24	2	0	13	1	157	777777776			TNZ	L15PIK		6830	
0	0	1	25	4	0	13	1	173			L6P16	CLA	H6P16	CHECK SUBTRACT ZERO.	6840	
0	0	1	26	17	0	13	0	024			VAR1	STO	VAR1		6850	
0	0	1	27	13	0	13	1	070			VAR2	CLA	H6P17		6860	
0	0	1	30	17	0	13	0	025			VAR2	STO	VAR2		6870	
0	0	1	31	13	0	13	1	071			VAR2	CLA	=0000000000		6880	
0	0	1	32	17	0	13	1	154	000000000			SUB	=0000000000		6890	
0	0	1	33	2	0	13	1	154	000000000			TNZ	L15PIK		6900	
0	0	1	34	4	0	13	1	173			L6P17	CLA	H6P17	SUB - ALL COMBINATIONS	6910	
0	0	1	35	17	0	13	0	025			VAR1	STO	VAR1		6920	
0	0	1	36	13	0	13	1	070			VAR2	CLA	H6P18		6930	
0	0	1	37	17	0	13	0	026			VAR2	STC	VAR2		6940	
0	0	1	40	13	0	13	1	071			TNZ	L15PIK		6950		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 16)

1M	IS	S	LOC	OP	DM	OS	9	ADR	QCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NC
0	0	1	41	17	0	13	166		046453224		L6P18	CLA	=0046453224		7030	
0	0	1	42	2	0	13	167		114722350			SUB	=0114722350		7040	
0	0	1	43	2	0	13	170		731530654			SUB	=0731530654		7050	
0	0	1	44	4	0	13	173					TNZ	L15PIK		7060	
0	0	1	45	17	0	13	026					CLA	CHECK AND FOR CLEARING ACCUMULATOR.		7070	
0	0	1	46	13	0	13	070					STO	H6P19		7080	
0	0	1	47	17	0	13	027					CLA	H6P19		7090	
0	0	1	50	13	0	13	071					STO	VAR2		7100	
0	0	1	51	17	0	13	164		525252524			CLA	=0525252524		7110	
0	0	1	52	6	0	13	165		252525252			AND	=0252525252		7120	
0	0	1	53	4	0	13	173					TNZ	L15PIK		7130	
0	0	1	54	17	0	13	027					CLA	CHECK FOR EVEN BITS.		7140	
0	0	1	55	13	0	13	070					STO	H6P19		7150	
0	0	1	56	17	0	13	030					CLA	VAR1		7160	
0	0	1	57	13	0	13	071					STO	H6P20		7170	
0	0	1	60	17	0	13	165		252525252			CLA	=0252525252		7180	
0	0	1	61	6	0	13	164		525252524			AND	=0525252524		7190	
0	0	1	62	4	0	13	173					TNZ	L15PIK		7200	
0	0	1	63	17	0	13	030					CLA	CHECK FOR ABILITY TO RETAIN ACCUMULATOR		7210	
0	0	1	64	13	0	13	070					STO	H6P20		7220	
0	0	1	65	17	0	13	031					CLA	VAR1		7230	
0	0	1	66	13	0	13	071					STO	H6P21		7240	
0	0	1	67	17	0	13	157		777777776			CLA	=0777777776		7250	
0	0	1	70	6	0	13	157		777777776			AND	=0777777776		7260	
0	0	1	71	2	0	13	157		777777776			SUB	=0777777776		7270	
0	0	1	72	4	0	13	173					TNZ	L15PIK		7280	
0	0	1	73	17	0	13	031					CLA	CHECK AND ZERO TO CHANGE ACCUMULATOR.		7290	
0	0	1	74	13	0	13	070					STO	H6P21		7300	
0	0	1	75	17	0	13	032					CLA	VAR1		7310	
0	0	1	76	13	0	13	071					STO	H6P22		7320	
0	0	1	77	17	0	13	154		000000000			CLA	=0000000000		7330	
0	0	1	100	6	0	13	154		000000000			AND	=0000000000		7340	
0	0	1	101	4	0	13	173					TNZ	L15PIK		7350	
0	0	1	102	17	0	13	032					CLA	CHECK AND ZERO TO CLEAR ACCUMULATOR.		7360	
0	0	1	103	13	0	13	070					STO	H6P22		7370	
0	0	1	104	17	0	13	033					CLA	VAR1		7380	
0	0	1	105	13	0	13	071					STO	H6P23		7390	
0	0	1	106	17	0	13	157		777777776			CLA	=0777777776		7400	
0	0	1	107	6	0	13	154		000000000			AND	=0000000000		7410	
0	0	1	110	4	0	13	173					TNZ	L15PIK		7420	
0	0	1	111	17	0	13	033					CLA	CHECK AND OF ALL BITS.		7430	
0	0	1	112	13	0	13	070					STO	H6P23		7440	
0	0	1	113	17	0	13	034					CLA	VAR1		7450	
0	0	1	114	13	0	13	071					STO	H7P1		7460	
0	0	1	115	17	0	13	154		000000000			CLA	=0000000000		7470	
0	0	1	116	6	0	13	157		777777776			AND	=0777777776		7480	
0	0	1	117	4	0	13	173					TNZ	L15PIK		7490	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 17)

FM	IS	S	LOC	UP	DM	DS	9	ADR	CCT	VAL	LHS	UPC	VARIABLE	COMMENT	SEC	NO
0	0	1	120	17	0	13	034				L7P1	CLA	H7P1	CHECK XOR OF ALL BITS.	7573	
0	0	1	121	13	0	13	1 070				STU	VAK1			7580	
0	0	1	122	17	0	13	035				CLA	H7P2			7590	
0	0	1	123	13	0	13	1 071				STG	VAK2			7600	
0	0	1	124	17	0	13	157	77777776			CLA	=07777776			7610	
0	0	1	125	15	0	13	157	77777776			XOR	=07777776			7620	
0	0	1	126	4	0	13	1 173				TNZ	L15PIK			7630	
0	0	1	127	17	0	13	035				CLA	H7P2	CHECK XOR WITH ALL ZEROS.	7640		
0	0	1	130	13	0	13	1 070				STC	VAK1			7650	
0	0	1	131	17	0	13	036				CLA	H7P3			7670	
0	0	1	132	13	0	13	1 071				STU	VAK2			7680	
0	0	1	133	17	0	13	154	00000000			CLA	=00000000			7690	
0	0	1	134	15	0	13	154	00000000			XOR	=00000000			7700	
0	0	1	135	4	0	13	1 173				TNZ	L15PIK			7710	
0	0	1	136	17	0	13	036				CLA	H7P3	CHECK SIGN BITS.	7720		
0	0	1	137	13	0	13	1 070				STU	VAK1			7730	
0	0	1	140	17	0	13	037				CLA	H7P4			7740	
0	0	1	141	13	0	13	1 071				STC	VAK2			7750	
0	0	1	142	17	0	13	153	40000000			CLA	=04000000			7760	
0	0	1	143	15	0	13	153	40000000			XOR	=04000000			7770	
0	0	1	144	4	0	13	1 173				TNZ	L15PIK			7780	
0	0	1	145	17	0	13	037				CLA	H7P4	CHECK ALL RUT SIGN BITS.	7790		
0	0	1	146	13	0	13	1 070				STU	VAK1			7800	
0	0	1	147	17	0	13	040				CLA	H7P5			7810	
0	0	1	150	13	0	13	1 071				STC	VAK2			7820	
0	0	1	151	17	0	13	171	37777776			CLA	=03777776			7830	
0	0	1	152	15	0	13	171	37777776			XOR	=03777776			7840	
0	0	1	153	4	0	13	1 173				TNZ	L15PIK			7850	
0	0	1	154	17	0	13	040				CLA	H7P5	CHECK LOW ORDER BITS.	7860		
0	0	1	155	13	0	13	1 070				STU	VAK1			7870	
0	0	1	156	17	0	13	041				CLA	H7P6			7880	
0	0	1	157	13	0	13	1 071				STG	VAK2			7900	
0	0	1	160	17	0	13	133	00000002			CLA	=00000002			7910	
0	0	1	161	15	0	13	133	00000002			XOR	=00000002			7920	
0	0	1	162	4	0	13	1 173				TNZ	L15PIK			7930	
0	0	1	163	17	0	13	041				CLA	H7P6	CHECK LOW ORDER BIT WITH ZEROS.	7940		
0	0	1	164	13	0	13	1 070				STC	VARI			7950	
0	0	1	165	17	0	13	042				CLA	H7P7			7980	
0	0	1	166	13	0	13	1 071				STC	VAK2			7990	
0	0	1	167	17	0	13	172	77777774			CLA	=07777774			8000	
0	0	1	170	15	0	13	172	77777774			XOR	=07777774			8010	
0	0	1	171	4	0	13	1 173				TNZ	L15PIK			8020	
0	0	1	172	10	0	13	1 174				TRA	L7P7			8030	
0	0	1	173	00	0	13	155	160000560			L15PIK	TRAP	L95PI	CHECK ALL UDC BITS.	8040	
0	0	1	174	17	0	13	042				STU	VAK1			8050	
0	0	1	175	13	0	13	1 070				CLA	H7P7			8060	
0	0	1	176	17	0	13	043				CLA	H7P8			8070	
0	0	1	177	13	0	13	1 071				STU	VAK2			8080	
0	0	1	200	17	0	13	164	525252524			CLA	=05252524			8100	
0	0	1	201	15	0	13	164	525252524			XOR	=05252524			8110	
															8120	
															8130	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 18)

IM	IS	S	LOC	OP	DM	DS	9	ADR	QCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	AC
0	0	1	202	4	0	13	1	173			L7P8	TNZ	L15PIK		8140	
0	0	1	203	17	0	13	043					CHECK	ALL EVEN BITS.		8150	
0	0	1	204	13	0	13	1	070				CLA	H7P8		8160	
0	0	1	205	17	0	13	044					STC	VARI		8170	
0	0	1	206	13	0	13	1	071				CLA	H7P9		8180	
0	0	1	207	17	0	13	165					STC	VAR2		8190	
0	0	1	210	15	0	13	165		252525252			CLA	=0252525252		8200	
0	0	1	211	4	0	13	1	173		252525252		XOR	=0252525252		8210	
0	0	1	212	17	0	13	044					TNZ	L15PIK		8220	
0	0	1	213	13	0	13	1	070				FILL	ACCUMULATOR WITH XOR.		8230	
0	0	1	214	17	0	13	045				L7P9	STC	H7P9		8240	
0	0	1	215	13	0	13	1	071				CLA	VARI		8250	
0	0	1	216	17	0	13	157					CLA	H7P10		8260	
0	0	1	217	15	0	13	154		777777776			STC	VAR2		8270	
0	0	1	218	2	0	13	154		000000000			CLA	=0777777776		8280	
0	0	1	219	2	0	13	157		777777776			XOR	=0000000000		8290	
0	0	1	220	4	0	13	1	173		777777776		SUB	=0777777776		8300	
0	0	1	221	4	0	13	1	173				TNZ	L15PIK		8310	
0	0	1	222	17	0	13	045					SAME	AS L7P9		8320	
0	0	1	223	13	0	13	1	070			L7P10	CLA	H7P10		8330	
0	0	1	224	17	0	13	046					STC	VARI		8340	
0	0	1	225	13	0	13	1	071				CLA	H7P11		8350	
0	0	1	226	17	0	13	154		000000000			STC	VAR2		8360	
0	0	1	227	15	0	13	157		777777776			CLA	=0000000000		8370	
0	0	1	228	2	0	13	157		777777776			XOR	=0777777776		8380	
0	0	1	230	2	0	13	157		777777776			SUB	=0777777776		8390	
0	0	1	231	4	0	13	1	173				TNZ	L15PIK		8400	
0	0	1	232	17	0	13	046					SAME	AS L7P9 WITH ODD BITS		8410	
0	0	1	233	13	0	13	1	070			L7P11	CLA	H7P11		8420	
0	0	1	234	17	0	13	047					STC	VARI		8430	
0	0	1	235	13	0	13	1	071				CLA	H7P12		8440	
0	0	1	236	17	0	13	164					STC	VAR2		8450	
0	0	1	237	15	0	13	165		525252524			CLA	=0525252524		8460	
0	0	1	240	2	0	13	157		252525252			XOR	=0252525252		8470	
0	0	1	241	4	0	13	1	173		777777776		SUB	=0777777776		8480	
0	0	1	242	17	0	13	047					TNZ	L15PIK		8490	
0	0	1	243	13	0	13	1	070				SAME	AS L7P9 WITH EVEN BITS		8500	
0	0	1	244	17	0	13	050				L7P12	CLA	H7P12		8510	
0	0	1	245	13	0	13	1	071				STC	VARI		8520	
0	0	1	246	17	0	13	165					CLA	H7P13		8530	
0	0	1	247	15	0	13	164		252525252			STC	VAR2		8540	
0	0	1	250	2	0	13	157		525252524			CLA	=0252525252		8550	
0	0	1	251	4	0	13	1	173		777777776		SUB	=0777777776		8560	
0	0	1	252	17	0	13	050					TNZ	L15PIK		8570	
0	0	1	253	13	0	13	1	070				CHECK	RSU		8580	
0	0	1	254	17	0	13	051				L7P13	CLA	H7P13		8590	
0	0	1	255	13	0	13	1	071				STC	VARI		8600	
0	0	1	256	17	0	13	157					CLA	H7P14		8610	
0	0	1	257	3	0	13	172		777777776			STC	VAR2		8620	
0	0	1	260	2	0	13	157		777777774			CLA	=0777777776		8630	
0	0	1	261	4	0	13	1	173		777777776		SUB	=0777777774		8640	
0	0	1	262	17	0	13	051					TNZ	L15PIK		8650	
0	0	1	263	13	0	13	1	070				CHECK	RSU		8660	
											L7P14	CLA	H7P14		8670	
											STC	VARI			8680	
															8700	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 19)

IM	IS	S	LUC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEL	NO
0	0	1	264	17	0	13	052					CLA	H7P15			8710
0	0	1	265	13	0	13	1 071					STC	VAR2			8720
0	0	1	266	17	0	13	133		000000002			CLA	=0000000002			8730
0	0	1	267	3	0	13	154		000000000			RSU	=0000000000			8740
0	0	1	270	2	0	13	157		777777776			SUB	=0777777776			8750
0	0	1	271	4	0	13	1 173					TNZ	LI5PIK			8760
0	0	1	272	17	0	13	052					CHECK	RSU			8770
0	0	1	273	13	0	13	1 070				L7P15	CLA	H7P15			8780
0	0	1	274	17	0	13	053					STO	VAR1			8790
0	0	1	275	13	0	13	1 071					CLA	H7P16			8800
0	0	1	276	17	0	13	157		777777776			STC	VAR2			8810
0	0	1	277	3	0	13	157		777777776			CLA	=0777777776			8820
0	0	1	300	4	0	13	1 173					RSU	=0777777776			8830
0	0	1	301	17	0	13	053					TNZ	LI5PIK			8840
0	0	1	302	13	0	13	1 070					CHECK	RSU			8850
0	0	1	303	17	0	13	054				L7P16	CLA	H7P16			8860
0	0	1	304	13	0	13	1 071					STO	VAR1			8870
0	0	1	305	17	0	13	154		000000000			CLA	H7P17			8880
0	0	1	306	3	0	13	154		000000000			STO	VAR2			8890
0	0	1	307	4	0	13	1 173					CLA	=0000000000			8900
0	0	1	310	17	0	13	054					RSU	=0000000000			8910
0	0	1	311	13	0	13	1 070					TNZ	LI5PIK			8920
0	0	1	312	17	0	13	055					CHECK	RSU			8930
0	0	1	313	13	0	13	1 071				L7P17	CLA	H7P17			8940
0	0	1	314	17	0	13	157		777777776			STO	VAR1			8950
0	0	1	315	3	0	13	154		000000000			CLA	H7P18			8960
0	0	1	316	2	0	13	133		000000002			STC	VAR2			8970
0	0	1	317	4	0	13	1 173					CLA	H7P19			8980
0	0	1	320	17	0	13	055					RSU	=0777777776			8990
0	0	1	321	13	0	13	1 070					STO	=0000000000			9000
0	0	1	322	17	0	13	056					SUB	=0000000002			9010
0	0	1	323	13	0	13	1 071					TNZ	LI5PIK			9020
0	0	1	324	17	0	13	173		331033100			CHECK	RSU			9030
0	0	1	325	3	0	13	174		265026500			CLA	H7P18			9040
0	0	1	326	2	0	13	175		733773400			STO	VAR1			9050
0	0	1	327	4	0	13	1 173					CLA	H7P19			9060
0	0	1	330	17	0	13	056					RSU	=0331033100			9070
0	0	1	331	13	0	13	1 070					STC	=0265026500			9080
0	0	1	332	17	0	13	057					SUB	=0733773400			9090
0	0	1	333	13	0	13	1 071					TNZ	LI5PIK			9100
0	0	1	334	17	0	13	153		400000000			CHECK	RSU			9110
0	0	1	335	16	0	13	001					CLA	H7P18			9120
0	0	1	336	4	0	13	1 173					STO	VAR1			9130
0	0	1	337	17	0	13	057					CLA	H7P19			9140
0	0	1	340	13	0	13	1 070					STC	VAR2			9150
0	0	1	341	17	0	13	060					CLA	H7P20			9160
0	0	1	342	13	0	13	1 071					STC	VAR2			9170
0	0	1	343	17	0	13	160		200000000			CLA	=0400000000			9180
0	0	1	335	16	0	13	001					SPL	1			9190
0	0	1	336	4	0	13	1 173					TNZ	LI5PIK			9200
0	0	1	337	17	0	13	057					CLA	H7P20			9210
0	0	1	340	13	0	13	1 070					STO	VAR1			9220
0	0	1	341	17	0	13	060					CLA	H7P21			9230
0	0	1	342	13	0	13	1 071					STO	VAR2			9240
0	0	1	343	17	0	13	160		200000000			CLA	=0200000000			9250
0	0	1	343	17	0	13	160					STC				9260

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 20)

IR	IS	S	LOC	DP	DM	DS	9	ADR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	0	1	344	16	0	13	002					SHL	2		9270	
0	0	1	345	4	0	13	173					TNZ	L15PIK		9280	
0	0	1	346	17	0	13	060				*	CLA	CHECK SHIFT LEFT ONE OF ALL ODD BITS.	9290		
0	0	1	347	13	0	13	070				L7P21	CLA	H7P21	9300		
0	0	1	350	14	0	13	061					STC	VARI	9310		
0	0	1	351	13	0	13	071					CLA	H7P22	9320		
0	0	1	352	17	0	13	164		525252524			STC	VAR2	9330		
0	0	1	353	16	0	13	001					CLA	=0525252524	9340		
0	0	1	354	2	0	13	176					SHL	1	9350		
0	0	1	355	4	0	13	173		252525250			SUB	=0252525250	9360		
0	0	1	356	14	0	13	061				*	TNZ	L15PIK	9370		
0	0	1	357	13	0	13	070				L7P22	CLA	CHECK SHIFT LEFT TWO OF ALL ODD BITS.	9380		
0	0	1	360	17	0	13	062					STC	VARI	9390		
0	0	1	361	13	0	13	071					CLA	H7P23	9400		
0	0	1	362	17	0	13	164		525252524			STU	VAR2	9410		
0	0	1	363	16	0	13	002					CLA	=0525252524	9420		
0	0	1	364	2	0	13	177					SHL	2	9430		
0	0	1	365	4	0	13	173		525252520			SUB	=0252525250	9440		
0	0	1	366	00	0	13	200		130001410			TNZ	L15PIK	9450		
0	1	0	3	17	0	13	136					TRA*	L7P23	9460		
0	1	0	3	17	0	13	062				*	ORG	V1,3,13,	9470		
0	1	0	4	13	0	13	070				L7P23	CLA	CHECK SHIFT LEFT ONE OF ALL EVEN BITS.	9480		
0	1	0	5	17	0	13	063					STC	VARI	9490		
0	1	0	6	13	0	13	071					CLA	H7P24	9500		
0	1	0	7	17	0	13	165		252525252			STU	VAR2	9510		
0	1	0	10	16	0	13	001					CLA	=0252525252	9520		
0	1	0	11	2	0	13	164					SHL	1	9530		
0	1	0	12	4	0	13	234		525252524			SUB	=0525252524	9540		
0	1	0	13	17	0	13	063					TNZ	L15PIJ	9560		
0	1	0	14	13	0	13	070				*	CLA	CHECK SHIFT LEFT TWO OF ALL EVEN BITS.	9570		
0	1	0	15	17	0	13	064				L7P24	CLA	H7P24	9580		
0	1	0	16	13	0	13	071					STC	VARI	9590		
0	1	0	17	17	0	13	165		252525252			CLA	H7P25	9600		
0	1	0	20	16	0	13	002					STC	VAR2	9610		
0	1	0	21	2	0	13	176					SHL	2	9620		
0	1	0	22	4	0	13	234		252525250			SUB	=0252525250	9630		
0	1	0	23	17	0	13	064					TNZ	L15PIJ	9640		
0	1	0	24	13	0	13	070				*	CLA	CHECK SHIFT LEFT ONE OF ALL BITS.	9650		
0	1	0	25	17	0	13	065				L7P25	CLA	H7P25	9660		
0	1	0	26	13	0	13	071					STC	VARI	9670		
0	1	0	27	17	0	13	157		777777776			CLA	H7P26	9680		
0	1	0	30	16	0	13	001					STO	VAR2	9690		
0	1	0	31	2	0	13	172					SHL	1	9700		
0	1	0	32	4	0	13	234		777777774			SUB	=0777777774	9710		
0	1	0	33	17	0	13	065				*	TNZ	L15PIJ	9720		
0	1	0	33	17	0	13	065				L7P26	CLA	CHECK SHIFT LEFT TWO OF ALL BITS.	9730		
0	1	0	33	17	0	13	065					SHL	2	9740		
0	1	0	33	17	0	13	065					SUB	=0777777774	9750		
0	1	0	33	17	0	13	065					TNZ	L15PIJ	9760		
0	1	0	33	17	0	13	065				*	CLA	CHECK SHIFT LEFT TWO OF ALL BITS.	9770		
0	1	0	33	17	0	13	065				L7P26	CLA	H7P26	9780		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 21)

IM	IS	S	LOC	OP	DM	DS	9	ADR	CCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	AC
0	1	0	34	13	0	13	1	070				STC	VARI		9780	
0	1	0	35	17	0	13	066					CLA	H7P27		9790	
0	1	0	36	13	0	13	071					STG	VAK2		9800	
0	1	0	37	17	0	13	157		77777776			CLA	=077777776		9810	
0	1	0	40	16	0	13	002					SHL	2		9820	
0	1	0	41	2	0	13	201					SUP	=07777777C		9830	
0	1	0	42	4	0	13	234		77777770			TNZ	L15PIJ		9840	
0	1	0	43	17	0	13	066					CLA	H7P27		9850	
0	1	0	44	13	0	13	070					STG	VARI		9860	
0	1	0	45	17	0	13	067					CLA	H7P2H		9870	
0	1	0	46	13	0	13	071					STC	VAK2		9880	
0	1	0	47	17	0	13	154		000000000			CLA	=0C0000000		9900	
0	1	0	50	16	0	13	001					SHL	1		9910	
0	1	0	51	4	0	13	234					TNZ	L15PIJ		9920	
0	1	0	52	17	0	13	067					CLA	H7P28		9930	
0	1	0	53	13	0	13	070					STG	VARI		9940	
0	1	0	54	17	0	13	070					CLA	H7P29		9950	
0	1	0	55	13	0	13	071					STC	VAK2		9960	
0	1	0	56	17	0	13	154		000000000			CLA	=0C000C000C		9970	
0	1	0	57	16	0	13	002					SHL	2		9980	
0	1	0	60	4	0	13	234					TNZ	L15PIJ		9990	
															10000	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 22)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LMS	UPC	VARIABLE	COMMENT	SEC	ADD
0	1	0	61	17	0	13	070				L7P29	CLA	H7P29	SHIFT BIT LEFT THROUGH ALL POSITIONS.	100274	
0	1	0	62	13	0	13	1 070					STC	VARI		10030	
0	1	0	63	17	0	13	071					CLA	H7P30		10040	
0	1	0	64	13	0	13	1 071					STU	VAR2		10050	
0	1	0	65	17	0	13	133		000000002			CLA	=000000002		10060	
												SHL	25		10070	
															10080	
0	1	0	66	16	0	13	040					SUB	=040000000		10090	
0	1	0	67	16	0	13	040		400000000			TNZ	L15P1J		10100	
0	1	0	70	16	0	13	040					CLA	H7P30		10110	
0	1	0	71	16	0	13	040					STU	VARI		10120	
0	1	0	72	16	0	13	001					CLA	H7P31		10130	
0	1	0	73	2	0	13	153					STC	VAR2		10140	
0	1	0	74	4	0	13	234		042104212			CLA	=0042104212		10150	
												SHL	3		10160	
0	1	0	102	16	0	13	004		421042120			XOR	=0421042120		10180	
0	1	0	103	15	0	13	203					TNZ	L15P1H		10190	
0	1	0	104	4	0	13	234					CLA	H7P31		10200	
0	1	0	105	17	0	13	072					STC	VARI		10210	
0	1	0	106	13	0	13	1 070					CLA	H7P32		10220	
0	1	0	107	17	0	13	073					STU	VAR2		10230	
0	1	0	110	13	0	13	1 071		020410206			CLA	=0020410206		10240	
0	1	0	111	17	0	13	204					SHL	4		10250	
0	1	0	112	16	0	13	010		410204140			XOR	=0410204140		10280	
0	1	0	113	15	0	13	205					TNZ	L15P1H		10290	
0	1	0	114	4	0	13	234					CLA	H7P32		10300	
0	1	0	115	17	0	13	073					STU	VARI		10310	
0	1	0	116	13	0	13	1 070					CLA	H7P33		10320	
0	1	0	117	17	0	13	074					STU	VAR2		10330	
0	1	0	120	13	0	13	1 071		010101012			CLA	=0010101012		10340	
0	1	0	121	17	0	13	206					SHL	5		10350	
0	1	0	122	16	0	13	020		404040500			XOR	=0404040500		10360	
0	1	0	123	15	0	13	207					TNZ	L15P1H		10370	
0	1	0	124	4	0	13	234					CLA	H7P33		10380	
0	1	0	125	17	0	13	074					STU	VARI		10390	
0	1	0	126	13	0	13	1 070					CLA	H7P34		10400	
0	1	0	127	17	0	13	075					STU	VAR2		10410	
0	1	0	130	13	0	13	1 071		004020102			CLA	=004020102		10420	
0	1	0	131	17	0	13	210					SHL	6		10430	
0	1	0	132	16	0	13	040		402010200			XOR	=0402010200		10450	
0	1	0	133	15	0	13	211					TNZ	L15P1H		10460	
0	1	0	134	4	0	13	234					CLA	H7P34		10470	
0	1	0	135	17	0	13	075					STU	VARI		10480	
0	1	0	136	13	0	13	1 070					CLA	H7P34		10490	
												STU	VARI		10490	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 23)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SFL	LOC
0	1	0	137	17	C	13	076					CLA	H7P35		10500	
0	1	0	140	13	0	13	071					STU	VAR2		10510	
0	1	0	141	17	0	13	165		252525252			CLA	=0252525252		10520	
0	1	0	142	16	0	13	040					SHL	6		10530	
0	1	0	143	2	0	13	212		252525200			SUB	=0252525200		10540	
0	1	0	144	4	0	13	234					TNZ	LI5PIH		10550	
0	1	0	145	17	0	13	076					CLA	H7P35		10560	
0	1	0	146	13	0	13	070					STU	VAR1		10570	
0	1	0	147	17	0	13	077					CLA	H7P36		10580	
0	1	0	150	13	0	13	071					STC	VAR2		10590	
0	1	0	151	17	0	13	164		525252524			CLA	=0525252524		10600	
0	1	0	152	16	0	13	040					SHL	6		10610	
0	1	0	153	2	0	13	213		525252400			SUB	=0525252400		10620	
0	1	0	154	4	0	13	234					TNZ	LI5PIH		10630	
0	1	0	155	17	0	13	077					CLA	H7P36		10640	
0	1	0	156	13	0	13	070					STU	VAR1		10650	
0	1	0	157	17	0	13	100					CLA	H7P37		10660	
0	1	0	160	13	0	13	071					STC	VAR2		10670	
0	1	0	161	17	0	13	133		000000002			CLA	=000000002		10680	
0	1	0	162	16	0	13	101					SHR	1		10690	
0	1	0	163	4	0	13	234					TNZ	LI5PIJ		10700	
0	1	0	164	17	0	13	100					CLA	H7P37		10710	
0	1	0	165	13	0	13	100					STU	VAR1		10720	
0	1	0	166	17	0	13	101					CLA	H7P38		10730	
0	1	0	167	13	0	13	101					STC	VAR2		10740	
0	1	0	170	17	0	13	214		000000004			CLA	=000000004		10750	
0	1	0	171	16	0	13	102					SHR	2		10760	
0	1	0	172	4	0	13	234					TNZ	LI5PIJ		10770	
0	1	0	173	17	0	13	101					CLA	H7P38		10780	
0	1	0	174	13	0	13	101					STU	VAR1		10790	
0	1	0	175	17	0	13	102					CLA	H7P39		10800	
0	1	0	176	13	0	13	101					STC	VAR2		10810	
0	1	0	177	17	0	13	164		525252524			CLA	=0525252524		10820	
0	1	0	200	16	0	13	101					SHR	1		10830	
0	1	0	201	2	0	13	215		652525252			SUB	=0652525252		10840	
0	1	0	202	4	0	13	234					TNZ	LI5PIJ		10850	
0	1	0	203	17	0	13	102					CLA	H7P39		10860	
0	1	0	204	13	0	13	1070					STC	VAR1		10870	
0	1	0	205	17	0	13	103					CLA	H7P40		10880	
0	1	0	206	13	0	13	1071					STC	VAR2		10890	
0	1	0	207	17	0	13	164		525252524			CLA	=0525252524		10900	
0	1	0	210	16	0	13	102					SHR	2		10910	
0	1	0	211	2	0	13	216		725252524			SUB	=0725252524		10920	
0	1	0	212	4	0	13	234					TNZ	LI5PIJ		10930	
0	1	0	213	17	0	13	103					CLA	H7P40		10940	
0	1	0	213	17	0	13	103					SHR	2		10950	
0	1	0	213	17	0	13	103					SHR	2		10960	
0	1	0	210	16	0	13	102					SUB	=0725252524		10970	
0	1	0	211	2	0	13	216		725252524			TNZ	LI5PIJ		10980	
0	1	0	212	4	0	13	234					CLA	H7P40		10990	
0	1	0	213	17	0	13	103					SHR	2		11000	
0	1	0	213	17	0	13	103					SHR	2		11000	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 24)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NC
0	1	0	214	13	0	13	1	070				STC	VARI		11010	
0	1	0	215	17	0	13	104					CLA	H7P41		11020	
0	1	0	216	13	0	13	1071					STO	VAR2		11030	
0	1	0	217	17	0	13	165	252525252				CLA	=0252525252		11040	
												SHR	1		11050	
0	1	0	220	16	0	13	101					SUB	=0125252524		11060	
0	1	0	221	2	0	13	217	125252524				TNZ	L15P1J		11070	
0	1	0	222	4	0	13	234					TNZ	L15P1J		11080	
															11090	
0	1	0	223	17	0	13	104					CLA	H7P41		11100	
0	1	0	224	13	0	13	1070					STO	VARI		11110	
0	1	0	225	17	0	13	105					CLA	H7P42		11120	
0	1	0	226	13	0	13	1071					STO	VAR2		11130	
0	1	0	227	17	0	13	165	252525252				CLA	=0252525252		11140	
												SHR	2		11150	
0	1	0	230	16	0	13	102					SUB	=0052525252		11160	
0	1	0	231	2	0	13	220	052525252				TNZ	L15P1J		11170	
0	1	0	232	4	0	13	234					TRA	L7P42		11180	
0	1	0	233	10	0	13	235					TRA	L7P42		11190	
0	1	0	234	00	0	13	155	160000560				L15P1J	TRAP		11200	
												L15P1H	SYN		11210	
															11220	
0	1	0	235	17	0	13	105					CLA	H7P42		11230	
0	1	0	236	13	0	13	1070					STO	VARI		11240	
0	1	0	237	17	0	13	106					CLA	H7P43		11250	
0	1	0	240	13	0	13	1071					STO	VAR2		11260	
0	1	0	241	17	0	13	157	777777776				CLA	=0777777776		11270	
												SHR	1		11280	
0	1	0	242	16	0	13	101					SUB	=0777777776		11290	
0	1	0	243	2	0	13	157	777777776				TNZ	L15P1J		11300	
0	1	0	244	4	0	13	234					TNZ	L15P1J		11310	
															11320	
0	1	0	245	17	0	13	106					CLA	H7P43		11330	
0	1	0	246	13	0	13	1070					STO	VARI		11340	
0	1	0	247	17	0	13	107					CLA	H7P44		11350	
0	1	0	250	13	0	13	1071					STO	VAR2		11360	
0	1	0	251	17	0	13	157	777777776				CLA	=0777777776		11370	
												SHR	2		11380	
0	1	0	252	16	0	13	102					SUB	=0777777776		11390	
0	1	0	253	2	0	13	157	777777776				TNZ	L15P1J		11400	
0	1	0	254	4	0	13	234					TNZ	L15P1J		11410	
															11420	
0	1	0	255	17	0	13	107					CLA	H7P44		11430	
0	1	0	256	13	0	13	1070					STO	VARI		11440	
0	1	0	257	17	0	13	110					CLA	H7P45		11450	
0	1	0	260	13	0	13	1071					STO	VAR2		11460	
0	1	0	261	17	0	13	154	000000000				CLA	=0000000000		11470	
												SHR	1		11480	
0	1	0	262	16	0	13	101					SUB	=0777777776		11490	
0	1	0	263	4	0	13	234					TNZ	L15P1J		11500	
															11510	
0	1	0	264	17	0	13	110					TNZ	L15P1J		11520	
0	1	0	265	13	0	13	1070					CLA	H7P45		11530	
0	1	0	266	17	0	13	111					STU	VARI		11540	
0	1	0	267	13	0	13	1071					CLA	H7P46		11550	
0	1	0	270	17	0	13	154	000000000				STO	VAR2		11560	
												CLA	=0000000000		11570	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 25)

IM	IS	S	LOC	OP	UM	DS	9	ADR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
C	1	0	271	16	0	13		102				SHR	2		11530	
C	1	0	272	4	0	13		234				TNZ	L15P1J		11540	
0	1	0	273	17	0	13		111			*	SHIFT BIT RIGHT THROUGH ALL POSITIONS.		11550		
C	1	0	274	13	0	13		1070			L7P46	CLA	H7P46		11560	
C	1	0	275	17	0	13		112				STC	VARI		11570	
0	1	0	276	13	0	13		1071				CLA	H7P47		11580	
0	1	0	277	17	0	13		153		400000000		STC	VAR2		11590	
C	1	0	300	16	0	13		140				CLA	=0400000000		11600	
C	1	0	301	16	0	13		140				SHR	25		11610	
0	1	0	302	16	0	13		140								
C	1	0	303	16	0	13		140								
0	1	0	304	16	0	13		101								
0	1	0	305	2	0	13		157								
0	1	0	306	4	0	13		234		777777776		SUB	=0777777776		11620	
0	1	0	307	17	0	13		112			*	TNZ	L15P1J		11630	
0	1	0	310	13	0	13		1070			L7P47	CLA	H7P47		11640	
0	1	0	311	17	0	13		113				STC	VARI		11650	
C	1	0	312	13	0	13		1071				CLA	H7P48		11660	
C	1	0	313	17	0	13		221		210421042		STC	VAR2		11670	
0	1	0	314	16	0	13		104				CLA	=0210421042		11680	
0	1	0	315	15	0	13		222		021042104		SPR	3		11690	
0	1	0	316	4	0	13		234							11700	
0	1	0	317	17	0	13		113			*	XOR	=0021042104		11710	
0	1	0	320	13	0	13		1070			L7P48	TNZ	L15P1H		11720	
0	1	0	321	17	0	13		114				CHECK	SHR4		11730	
0	1	0	322	13	0	13		1071				CLA	H7P48		11740	
0	1	0	323	17	0	13		223		214102040		STC	VARI		11750	
0	1	0	324	16	0	13		110				CLA	H7P49		11760	
0	1	0	325	15	0	13		224		010604102		STC	VAR2		11770	
0	1	0	326	4	0	13		234				CLA	=0214102040		11780	
0	1	0	327	17	0	13		114			*	SHR	4		11790	
0	1	0	330	13	0	13		1070			L7P49	XOR	=0010604102		11800	
0	1	0	331	17	0	13		115				TNZ	L15P1H		11810	
0	1	0	332	13	0	13		1071				CHECK	SHR5		11820	
0	1	0	333	17	0	13		225		202020200		CLA	H7P49		11830	
0	1	0	334	16	0	13		120			*	STC	VARI		11840	
0	1	0	335	15	0	13		226		004040404		CLA	H7P50		11850	
C	1	0	336	4	0	13		234				STC	VAR2		11860	
0	1	0	337	17	0	13		115				CLA	=0202020200		11870	
0	1	0	340	13	0	13		1070			*	SHR	5		11880	
0	1	0	341	17	0	13		116			L7P50	XOR	=004040404		11890	
0	1	0	342	13	0	13		1071				TNZ	L15P1H		11900	
0	1	0	343	17	0	13		227		201004220		CHECK	SHR6		11910	
0	1	0	344	16	0	13		140				CLA	H7P50		11920	
0	1	0	345	15	0	13		230		002010042		STC	VARI		11930	
C	1	0	346	4	0	13		234				CLA	H7P51		11940	
0	1	0	347	13	0	13		1071				STC	VAR2		11950	
0	1	0	348	17	0	13		227		201004220		CLA	=0201004220		11960	
0	1	0	349	16	0	13		140				SHR	6		11970	
0	1	0	350	15	0	13		230		002010042		XOR	=0002010042		11980	
C	1	0	351	4	0	13		234				TNZ	L15P1H		11990	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 26)

IM	IS	S	LOC	OP	DS	9	ADR	OCT	VAL	LHS	CPC	VARIABLE	COMMENT	SEC	NC
0	1	0	347	17	0	13	116					CHECK SHR6 EVEN BITS		12000	
0	1	0	350	13	0	13	1070			L7P51	CLA	H7P51		12010	
0	1	0	351	17	0	13	117				STO	VAR1		12020	
0	1	0	352	13	0	13	171				CLA	H7P52		12030	
0	1	0	353	17	0	13	165	252525252			STC	VAR2		12040	
0	1	0	354	16	0	13	140				CLA	=0252525252		12050	
0	1	0	355	2	0	13	231				SHR	6		12060	
0	1	0	356	4	0	13	234	002525252			SUB	=002525252		12070	
0	1	0	357	17	0	13	117				TNZ	L15PIH		12080	
0	1	0	360	13	0	13	1070				CLA	H7P52		12100	
0	1	0	361	17	0	13	120				STC	VAR1		12110	
0	1	0	362	13	0	13	1071				CLA	H7P53		12120	
0	1	0	363	17	0	13	164	525252524			STO	VAR2		12130	
0	1	0	364	16	0	13	140				CLA	=0525252524		12140	
0	1	0	365	2	0	13	232	775252524			SHR	6		12150	
0	1	0	366	4	0	13	234				SUB	=0775252524		12160	
0	1	0	367	10	0	13	102				TNZ	L15PIH		12170	
0	1	1	2	17	0	13	137				TRA	L7P53		12180	
0	1	1	3	13	0	13	1070				CHECK CDS			12190	
0	1	1	4	17	0	13	121				ORG	*1,1,2,*13,		12200	
0	1	1	5	13	0	13	1071				CLA	H7P53		12210	
0	1	1	6	17	0	13	154	000000000			STC	VAR1		12220	
0	1	1	7	16	1	7	227				CLA	H7P54		12230	
0	1	1	10	17	1	7	375				STC	VAR2		12240	
0	1	1	11	16	0	10	210				CLA	=0C00000000		12250	
0	1	1	12	14	0	10	1015				CCS	1,07		12260	
0	1	1	13	16	0	10	001				CLA	KMA		12270	
0	1	1	14	14	0	10	016				CCS	0,10		12280	
0	1	1	15	00	0	10	374	130116010			TMI	L15PIT		12290	
0	1	1	16	17	0	10	375				SHL	1		12300	
0	1	1	17	14	0	10	1021				TMI	**2		12310	
0	1	1	20	10	0	10	1015				TRA	L15PIT		12320	
0	1	1	21	16	0	10	002				CLA	KMB		12330	
0	1	1	22	14	0	10	1024				TMI	**2		12340	
0	1	1	23	10	0	10	1015				TRA	L15PIT		12350	
0	1	1	24	16	0	10	001				SHL	2		12360	
0	1	1	25	4	0	10	015				TMI	**2		12370	
0	1	1	26	16	0	0	200				TRA	L15PIT		12380	
0	1	1	27	17	0	0	375				SHL	1		12390	
0	1	1	30	16	0	13	213				TNZ	L15PIT		12400	
0	1	1	31	16	0	13	002				CDS	0,0		12410	
0	1	1	32	14	0	13	234				CLA	KMR		12420	
0	1	1	33	4	0	13	1035				CCS	0,13		12430	
0	1	1	34	10	0	13	234				SHL	2		12440	
0	1	1	35	16	0	13	002				TMI	L15PIT		12450	
0	1	1	36	4	0	13	234				TNZ	**2		12460	
											TRA	L15PIT		12470	
											SHL	2		12480	
											TNZ	L15PIT		12490	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 27)

IM	IS	S	LOC	OP	UM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	1	1	37	00	0	13		233	130007430		*	CHK	HOP	SAVE	CONSTANT	12500
0	3	0	17	13	0	13		140				TRA*	L7P54			12510
0	3	0	17	13	0	13		140				ORG	3,17,13,			12520
0	3	0	20	17	0	13		121			L7P54	STC	776			12530
0	3	0	21	13	0	13		121			CLA	F7P54				12540
0	3	0	22	17	0	13		122			STC	VAR1				12550
0	3	0	22	17	0	13		122			CLA	H7P54B				12560
0	3	0	23	13	0	13		140	571165370		H7P55B	HPC	L7P55			12570
0	3	0	23	13	0	13		140			L7P54A	STC	VAR2			12580
0	3	0	24	17	0	13		1376			CLA	776				12600
0	3	0	25	15	0	13		1025			XOR	HRP1A				12610
0	3	0	26	4	0	13		030			TNZ	L95P1A				12630
0	3	0	27	0	0	13		140			L7P54B	HOP	H7P55B			12640
0	3	0	30	0	0	13		1026			L95P1A	HPC	H95P1			12650
1	17	1	352	13	1	17		100			L7P55	STC	777			12660
1	17	1	352	13	1	17		101			CLA	H7P55				12670
1	17	1	353	17	1	17		101			STC	VAR1				12680
1	17	1	354	13	1	17		1070			CLA	HRP1A				12690
1	17	1	355	17	1	17		1025			STC	VAR2				12700
1	17	1	356	13	1	17		1071			L7P55A	STC	VAR2			12720
1	17	1	357	17	1	17		1377			CLA	777				12740
1	17	1	360	15	1	17		100			XOR	H95P1A				12750
1	17	1	361	4	1	17		100	130014030		H95P1A	HPC	L95P1A			12760
1	17	1	362	0	1	17		1363			TNZ	L15P1M				12770
1	17	1	362	0	1	17		1025			HOP	HRP1A				12780
1	17	1	362	0	1	17		101	571165370		H7P55	HPC	L7P55			12790
1	17	1	363	00	1	17		000	160000560		L15P1M	TRA*	L95P1			12810
0	1	1	40	17	0	13		141			ORG	1,1,40,13,				12820
0	1	1	40	17	0	13		123			CLA	HRP1				12830
0	1	1	41	13	0	13		1070			STC	VAR1				12840
0	1	1	42	17	0	13		124			CLA	HRP2				12850
0	1	1	43	13	0	13		1071			STC	VAR2				12860
0	1	1	44	17	0	13		234	123456702		CLA	=0123456702				12870
0	1	1	45	1	0	13		1375			PRS	775				12880
0	1	1	46	15	0	13		234	123456702		XOR	=0123456702				12890
0	1	1	47	4	0	13		136			TNZ	L15P1M				12900
0	1	1	50	17	0	13		124			CLA	HRP2				12910
0	1	1	51	13	0	13		1070			STC	VAR1				12920
0	1	1	52	17	0	13		125			CLA	HRP3				12930
0	1	1	53	13	0	13		1071			STC	VAR2				12940
0	1	1	54	17	0	13		235	765432106		CLA	=0765432106				12950
0	1	1	55	1	0	13		1374			PRS	774				12960
0	1	1	56	15	0	13		235	765432106		XOR	=0765432106				12970
0	1	1	57	4	0	13		136			TNZ	L15P1M				12980
0	1	1	60	17	0	13		125			CLA	HRP3				12990
0	1	1	61	13	0	13		1070			STC	VAR1				13000
0	1	1	62	17	0	13		126			CLA	HRP4				13010
0	1	1	63	13	0	13		1071			STC	VAR2				13020
0	1	1	64	17	0	13		157	777777776		CLA	=077777776				13030
0	1	1	64	17	0	13		157			CLA					13040
0	1	1	64	17	0	13		157			CLA					13050
0	1	1	64	17	0	13		157			CLA					13060

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 28)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	1	1	65	1	C	13		125				PRS	H8P3		13070	
0	1	1	66	15	0	13		125				XDR	H8P3		13080	
0	1	1	67	4	0	13		136				TNZ	L15PIN		13090	
														CHECK AFFECT OF CIU L20 ON ACCUMULATOR		
0	1	1	70	17	0	13		126			L8P4	CLA	H8P4		13100	
0	1	1	71	13	0	13		127				STU	VARI		13120	
0	1	1	72	17	0	13		127				CLA	H8P5		13130	
0	1	1	73	13	0	13		127				STO	VARI		13140	
0	1	1	74	17	0	13		157	777777776			CLA	=0777777776		13150	
0	1	1	75	5	0	13		120				CIU	L20		13160	
0	1	1	76	15	0	13		157	777777776			XDR	=0777777776		13170	
0	1	1	77	4	0	13		136				TNZ	L15PIN		13180	
													SAML AS ABOVE FOR CIU 124			
0	1	1	100	17	0	13		127			L8P5	CLA	H8P5		13190	
0	1	1	101	13	0	13		127				STU	VARI		13200	
0	1	1	102	17	0	13		130				CLA	H8P6		13210	
0	1	1	103	13	0	13		130				STO	VARI		13220	
0	1	1	104	17	0	13		157	777777776			CLA	=0777777776		13230	
0	1	1	105	5	0	13		124				CIU	L24		13240	
C	1	1	106	15	0	13		157	777777776			XDR	=0777777776		13250	
0	1	1	107	4	0	13		136				TNZ	L15PIN		13260	
													SAME AS ABOVE FOR CIU 130			
0	1	1	110	17	0	13		130			L8P6	CLA	H8P6		13270	
0	1	1	111	13	0	13		127				STU	VARI		13280	
0	1	1	112	17	0	13		141				CLA	H9P1		13290	
0	1	1	113	13	0	13		141	140057610		H9P1	HPC	L9P1		13300	
0	1	1	114	17	0	13		157	777777776			STO	VARI		13310	
0	1	1	115	5	0	13		130				CLA	=0777777776		13320	
0	1	1	116	15	0	13		157	777777776			CIU	L30		13330	
0	1	1	117	4	0	13		136				XDR	=0777777776		13340	
0	1	1	120	17	0	13		136			L8P7	TNZ	L15PIN		13350	
0	1	1	121	14	0	13		134				CLA	LCR4		13360	
0	1	1	122	17	0	13		156				TMI	L8P9		13370	
0	1	1	123	14	0	13		134				CLA	LCR3		13380	
0	1	1	124	17	0	13		134				TMI	L8P9		13390	
0	1	1	125	14	0	13		134				CLA	LCR5		13400	
0	1	1	126	17	0	13		134				TMI	L8P9		13410	
0	1	1	127	5	0	13		210			L8P8	CLA	K77		13420	
0	1	1	130	17	0	13		120				CIU	ZERO		13430	
0	1	1	131	5	0	13		210				CIU	ZERO		13440	
0	1	1	132	0	0	13		123				HOP	H9P3		13450	
0	1	1	133	0	0	13		141				HOP	H9P1		13460	
0	1	1	134	00	0	13		236	120000270		L8P9	TRA*	L20P2A		13470	
0	1	1	135	10	0	13		126				TRA	L8P8		13480	
0	1	1	136	00	0	13		155	160000560		L15PIN	TRA*	L95P1		13490	
0	1	1	136	0	0	375						OGG	1,375		13500	
0	1	1	136	0	0	375			440000000		KMR	OCT	440000000		13510	
0	1	1	136	0	1	375						OGG	1,375		13520	
0	1	1	136	0	2	375			420000000		KMP	OCT	420000000		13530	
0	1	1	136	0	2	375						OGG	2,375		13540	
0	1	1	136	0	3	375			410000000		KMC	OCT	410000000		13550	
0	1	1	136	0	3	375						OGG	3,375		13560	
0	1	1	136	0	4	375			404000000		KMD	OCT	404000000		13570	
0	1	1	136	0	4	375						OGG	4,375		13580	
0	1	1	136	0	4	375			402000000		KME	OCT	402000000		13590	
0	1	1	136	0	5	375						OGG	5,375		13600	
														FOR PROGRAM COMPATIBILITY		
														SET AND RESET ALL DO S		
														DELAY		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 29)

IM	IS	S	LOC	CP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
C	1	1	136					5	375	401000000	KMF	OCT	401000000		13640	
								6	375			D0G	*6.375		13650	
O	1	1	136					7	375	400400000	KMG	OCT	400400000		13660	
								7	375			D0G	*7.375		13670	
O	1	1	136					10	375	400001000	KMQ	OCT	400001000		13680	
								10	375			D0G	*10.375		13690	
O	1	1	136					11	375	500000000	KMB	OCT	500000000		13700	
								11	375			D0G	*11.375		13710	
O	1	1	136					12	375	400200000	KMH	OCT	400200000		13720	
								12	375			D0G	*12.375		13730	
O	1	1	136					13	375	400100000	KMJ	OCT	400100000		13740	
								13	375			D0G	*13.375		13750	
O	1	1	136					14	375	400040000	KMK	OCT	400040000		13760	
								14	375			D0G	*14.375		13770	
O	1	1	136					15	375	400020000	KML	OCT	400020000		13780	
								15	375			D0G	*15.375		13790	
C	1	1	136					16	375	400010000	KPM	OCT	400010000		13800	
								16	375			D0G	*16.375		13810	
O	1	1	136					17	375	400004000	KPN	OCT	400004000		13820	
								17	375			D0G	*17.375		13830	
C	1	1	136					17	375	400002000	KMO	OCT	400002000		13840	
								17	375			D0G	*17.375		13850	
								17	375	200000000	KMA	OCT	200000000		13860	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 30)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEC	NC
0	1	1	136	0	14	0	0	0	140062210	H9P2	00G	*14*0			13880	
				0	14	0	1	1	140001020	H9P4	HPC	L9P2			13890	
				0	14	1	1	1	140002020	H9P5	HPC	L9P4			13900	
				0	14	3	3	3	140005020	H9P6	HPC	L9P5			13910	
				0	14	4	4	4	140007420	H9P7	HPC	L9P6			13920	
				0	14	5	5	5	140012420	H9P8	HPC	L9P7			13930	
				0	14	6	6	6	140015420	H9P9	HPC	L9P8			13940	
				0	14	7	7	7	140021020	H9P10	HPC	L9P9			13950	
				0	14	10	10	10	140024420	H9P11	HPC	L9P10			13960	
				0	14	11	11	11	140030020	H9P12	HPC	L9P11			13970	
				0	14	12	12	12	140033020	H9P13	HPC	L9P12			13980	
				C	14	13	13	13	140036020	H9P14	HPC	L9P13			13990	
				0	14	14	14	14	140041420	H9P15	HPC	L9P14			14000	
				0	14	15	15	15	140045020	H9P16	HPC	L9P15			14010	
				0	14	16	16	16	140050420	H9P17	HPC	L9P16			14020	
				0	14	17	17	17	140054020	H9P18	HPC	L9P17			14030	
				0	14	20	20	20	140057420	H9P19	HPC	L9P18			14040	
				0	14	21	21	21	140063020	H9P20	HPC	L9P19			14050	
				0	14	22	22	22	140066420	H9P21	HPC	L9P20			14060	
				0	14	23	23	23	140072020	H9P22	HPC	L9P21			14070	
				0	14	24	24	24	140075420	H9P23	HPC	L9P22			14080	
				0	14	25	25	25	140101020	H9P24	HPC	L9P23			14090	
				0	14	26	26	26	140104420	H9P25	HPC	L9P24			14100	
				0	14	31	31	31	140110020	H9P26	00G	L9P25			14110	
				C	14	31	31	31	140110020	H9P26	HPC	*14*31			14120	
				0	14	32	32	32	140113420	H9P27	HPC	L9P26			14130	
				0	14	33	33	33	140117020	H9P28	HPC	L9P27			14140	
				0	14	34	34	34	140122420	H9P29	HPC	L9P28			14150	
				C	14	35	35	35	140126020	H9P30	HPC	L9P29			14160	
				0	14	36	36	36	140131420	H9P31	HPC	L9P30			14170	
				0	14	37	37	37	140135020	H9P32	HPC	L9P31			14180	
				0	14	40	40	40	140140420	H9P33	HPC	L9P32			14190	
				0	14	41	41	41	140144020	H9P34	HPC	L9P33			14200	
				0	14	42	42	42	140147420	H9P35	HPC	L9P34			14210	
				0	14	43	43	43	140153020	H9P36	HPC	L9P35			14220	
				C	14	44	44	44	140156420	H9P37	HPC	L9P36			14230	
				0	14	45	45	45	140162020	H9P38	HPC	L9P37			14240	
				0	14	46	46	46	140165420	H9P39	HPC	L9P38			14250	
				0	14	47	47	47	140001220	H9P40	HPC	L9P39			14260	
				0	14	50	50	50	140004620	H9P41	HPC	L9P40			14270	
				0	14	51	51	51	140010220	H9P42	HPC	L9P41			14280	
				0	14	52	52	52	140013620	H9P43	HPC	L9P42			14290	
				0	14	53	53	53	140017220	H9P44	HPC	L9P43			14300	
				0	14	54	54	54	140022620	H9P45	HPC	L9P44			14310	
				0	14	55	55	55	140026220	H9P46	HPC	L9P45			14320	
				0	14	56	56	56	140031620	H9P47	HPC	L9P46			14330	
				0	14	57	57	57	140035220	H9P48	HPC	L9P47			14340	
				0	14	60	60	60	140040620	H9P49	HPC	L9P48			14350	
				0	14	61	61	61	140044220	H9P50	HPC	L9P49			14360	
				0	14	62	62	62	140047620	H9P51	HPC	L9P50			14370	
				0	14	63	63	63	140053220	H9P52	HPC	L9P51			14380	
				C	14	64	64	64	140056620	H9P53	HPC	L9P52			14390	
				0	14	65	65	65	140062220	H9P54	HPC	L9P53			14400	
				0	14	66	66	66	140065620	H9P55	HPC	L9P54			14410	
				0	14	67	67	67	140071220	H9P56	HPC	L9P55			14420	
				0	14	70	70	70	140074620	H9P57	HPC	L9P56			14430	
															14440	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 31)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	2	0	4	17	0	14		002			L9P5	CLA	H9P5		15020	
0	2	0	5	13	0	14		073				STC	VAR4		15030	
0	2	0	6	17	0	14		111	777777776			CLA	=0777777776		15040	
0	2	0	7	5	0	14		000				CIC	000		15050	
0	2	0	10	5	0	14		154				CIC	154		15060	
0	2	0	11	4	0	14		356				TNZ	L15PIP	READ INT REG R	15070	
0	2	0	12	17	0	14		003			L9P6	CLA	H9P6		15080	
0	2	0	13	13	0	14		073				STC	VAR4		15090	
0	2	0	14	5	0	14		003				CIC	003		15100	
0	2	0	15	5	0	14		154				CIC	154		15110	
0	2	0	16	4	0	14		356				TNZ	L15PIP		15120	
0	2	0	17	17	0	14		004			L9P7	CLA	H9P7		15130	
0	2	0	20	13	0	14		073				STC	VAR4		15140	
0	2	0	21	17	0	14		020				CLA	ZERO		15150	
0	2	0	22	5	0	14		004				CIC	004		15160	
0	2	0	23	5	0	14		154				CIC	154		15170	
0	2	0	24	4	0	14		356				TNZ	L15PIP		15180	
0	2	0	25	17	0	14		005			L9P8	CLA	H9P8		15190	
0	2	0	26	13	0	14		073				STC	VAR4		15200	
0	2	0	27	5	0	14		001				CIC	001	SET I3	15210	
0	2	0	30	5	0	14		154	100000000			CIC	154		15220	
0	2	0	31	15	0	14		167				X04	=0100000000		15230	
0	2	0	32	4	0	14		020				TNZ	L15PIP		15240	
0	2	0	33	5	0	14		020			L9P9	CIC	020	RST I3	15250	
0	2	0	34	17	0	14		006				CLA	H9P9		15260	
0	2	0	35	13	0	14		073				STC	VAR4		15270	
0	2	0	36	5	0	14		002				CIC	002	SET I1	15280	
0	2	0	37	5	0	14		154				CIC	154		15290	
0	2	0	40	15	0	14		221	400000000			X0R	=0400000000		15300	
0	2	0	41	4	0	14		356			L9P10	TNZ	L15PIP	RST I1	15310	
0	2	0	42	5	0	14		010				CIC	010		15320	
0	2	0	43	17	0	14		007				CLA	H9P10		15330	
0	2	0	44	13	0	14		073				STC	VAR4		15340	
0	2	0	45	5	0	14		005				CIC	005	SET I4	15350	
0	2	0	46	5	0	14		154				CIC	154		15360	
0	2	0	47	15	0	14		222	040000000			X04	=0040000000		15370	
0	2	0	50	4	0	14		356			L9P11	TNZ	L15PIP	RST I4	15380	
0	2	0	51	5	0	14		024				CIC	024		15390	
0	2	0	52	17	0	14		010				CLA	H9P11		15400	
0	2	0	53	13	0	14		073				STC	VAR4		15410	
0	2	0	54	5	0	14		006				CIC	006	SET I2	15420	
0	2	0	55	5	0	14		154				CIC	154		15430	
0	2	0	56	15	0	14		223	200000000			X0R	=0200000000		15440	
0	2	0	57	4	0	14		356			L9P12	TNZ	L15PIP	RST I2	15450	
0	2	0	60	5	0	14		014				CIC	014		15460	
0	2	0	61	17	0	14		011				CLA	H9P12		15470	
0	2	0	62	13	0	14		073				STC	VAR4		15480	
0	2	0	63	5	0	14		007				CIC	007	SET I5	15490	
0	2	0	64	5	0	14		154				CIC	154		15500	
0	2	0	65	4	0	14		356				TNZ	L15PIP		15510	
0	2	0	66	17	0	14		012			L9P13	CLA	H9P13		15520	
0	2	0	67	13	0	14		073				STC	VAR4		15530	
0	2	0	70	5	0	14		011				CIC	011		15540	
0	2	0	71	5	0	14		154				CIC	154		15550	
0	2	0	72	15	0	14		224	020000000			X0R	=0020000000		15560	
0	2	0	73	4	0	14		356			L9P14	TNZ	L15PIP	RST I5	15570	
0	2	0	74	5	0	14		030				CIC	030		15580	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 33)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	2	0	75	17	0	14	013					CLA	H9P14		15590	
0	2	0	76	13	0	14	1 073					STO	VAR4		15600	
0	2	0	77	5	0	14	012					CIO	012	SET I3	15610	
0	2	0	100	5	0	14	154					CIO	154		15620	
0	2	0	101	15	0	14	167		100000000			XOR	=0100000000		15630	
0	2	0	102	4	0	14	1 356				L9P15	TNZ	L15PIP		15640	
0	2	0	103	5	0	14	020					CIO	020	RST I3	15650	
0	2	0	104	17	0	14	014					CLA	H9P15		15660	
0	2	0	105	13	0	14	1 073					STO	VAR4	SET I6	15670	
0	2	0	106	5	0	14	015					CIO	015		15680	
0	2	0	107	5	0	14	154					CIO	154		15690	
0	2	0	110	15	0	14	225		010000000			XOR	=0010000000		15700	
0	2	0	111	4	0	14	1 356					TNZ	L15PIP		15710	
0	2	0	112	5	0	14	034				L9P16	CIO	034	RST I6	15720	
0	2	0	113	17	0	14	1 073					CLA	H9P16		15730	
0	2	0	114	13	0	14	1 073					STO	VAR4		15740	
0	2	0	115	5	0	14	016					CIO	016	SET I4	15750	
0	2	0	116	5	0	14	154					CIC	154		15760	
0	2	0	117	15	0	14	222		040000000			XOR	=0040000000		15770	
0	2	0	120	4	0	14	1 356					TNZ	L15PIP		15780	
0	2	0	121	5	0	14	024				L9P17	CIO	024	RST I4	15790	
0	2	0	122	17	0	14	016					CLA	H9P17		15800	
0	2	0	123	13	0	14	1 073					STO	VAR4		15810	
0	2	0	124	5	0	14	021					CIO	021	SET I7	15820	
0	2	0	125	5	0	14	154					CIO	154		15830	
0	2	0	126	15	0	14	226		004000000			XOR	=0040000000		15840	
0	2	0	127	4	0	14	1 356					TNZ	L15PIP		15850	
0	2	0	130	5	0	14	040				L9P18	CIO	040	RST I7	15860	
0	2	0	131	17	0	14	017					CLA	H9P18		15870	
0	2	0	132	13	0	14	1 073					STO	VAR4		15880	
0	2	0	133	5	0	14	022					CIC	022	SET I5	15890	
0	2	0	134	5	0	14	154					CIO	154		15900	
0	2	0	135	15	0	14	224		020000000			XOR	=0020000000		15910	
0	2	0	136	4	0	14	1 356					TNZ	L15PIP		15920	
0	2	0	137	5	0	14	030				L9P19	CIO	030	RST I5	15930	
0	2	0	140	17	0	14	020					CLA	H9P19		15940	
0	2	0	141	13	0	14	1 073					STO	VAR4		15950	
0	2	0	142	5	0	14	025					CIO	025	SET I8	15960	
0	2	0	143	5	0	14	154					CIO	154		15970	
0	2	0	144	15	0	14	227		002000000			XOR	=0020000000		15980	
0	2	0	145	4	0	14	1 356					TNZ	L15PIP		15990	
0	2	0	146	5	0	14	044				L9P20	CIO	044	RST I8	16000	
0	2	0	147	17	0	14	021					CLA	H9P20		16010	
0	2	0	150	13	0	14	1 073					STO	VAR4		16020	
0	2	0	151	5	0	14	026					CIO	026	SET I6	16030	
0	2	0	152	5	0	14	154					CIO	154		16040	
0	2	0	153	15	0	14	225		010000000			XOR	=0010000000		16050	
0	2	0	154	4	0	14	1 356					TNZ	L15PIP		16060	
0	2	0	155	5	0	14	034				L9P21	CIO	034	RST I6	16070	
0	2	0	156	17	0	14	022					CLA	H9P21		16080	
0	2	0	157	13	0	14	1 073					STO	VAR4		16090	
0	2	0	160	5	0	14	031					CIO	031	SET I9	16100	
0	2	0	161	5	0	14	154					CIO	154		16110	
0	2	0	162	15	0	14	230		001000000			XOR	=0001000000		16120	
0	2	0	163	4	0	14	1 356					TNZ	L15PIP		16130	
0	2	0	164	5	0	14	050				L9P22	CIO	050	RST I9	16140	
0	2	0	165	17	0	14	023					CLA	H9P22		16150	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 34)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	2	0	166	13	0	14	1	073				STO	VAR4		16160	
0	2	0	167	5	0	14	032					CIO	032	SET I7	16170	
0	2	0	170	5	0	14	154					CIO	154		16180	
0	2	0	171	15	0	14	226		004000000			XOR	-0004000000		16190	
0	2	0	172	4	0	14	1	356				TNZ	L15PIP		16200	
0	2	0	173	5	0	14	040				L9P23	CIO	040	RST I7	16210	
0	2	0	174	17	0	14	024					CLA	H9P23		16220	
0	2	0	175	13	0	14	1	073				STO	VAR4		16230	
0	2	0	176	5	0	14	035					CIO	035	SET I10	16240	
0	2	0	177	5	0	14	154					CIO	154		16250	
0	2	0	200	15	0	14	231		000400000			XOR	-0000400000		16260	
0	2	0	201	4	0	14	1	356				TNZ	L15PIP		16270	
0	2	0	202	5	0	14	054				L9P24	CIO	054	RST I10	16280	
0	2	0	203	17	0	14	025					CLA	H9P24		16290	
0	2	0	204	13	0	14	1	073				STO	VAR4		16300	
0	2	0	205	5	0	14	036					CIO	036	SET I8	16310	
0	2	0	206	5	0	14	154					CIO	154		16320	
0	2	0	207	15	0	14	227		002000000			XOR	-0002000000		16330	
0	2	0	210	4	0	14	1	356				TNZ	L15PIP		16340	
0	2	0	211	5	0	14	044				L9P25	CIO	044	RST I8	16350	
0	2	0	212	17	0	14	026					CLA	H9P25		16360	
0	2	0	213	13	0	14	1	073				STO	VAR4		16370	
0	2	0	214	5	0	14	041					CIO	041	SET I11	16380	
0	2	0	215	5	0	14	154					CIO	154		16390	
0	2	0	216	15	0	14	232		000200000			XOR	-0002000000		16400	
0	2	0	217	4	0	14	1	356				TNZ	L15PIP		16410	
0	2	0	220	5	0	14	060				L9P26	CIO	060	RST I11	16420	
0	2	0	221	17	0	14	031					CLA	H9P26		16430	
0	2	0	222	13	0	14	1	073				STO	VAR4		16440	
0	2	0	223	5	0	14	042					CIO	042	SET I9	16450	
0	2	0	224	5	0	14	154					CIO	154		16460	
0	2	0	225	15	0	14	230		001000000			XOR	-0001000000		16470	
0	2	0	226	4	0	14	1	356				TNZ	L15PIP		16480	
0	2	0	227	5	0	14	050				L9P27	CIO	050	RST I9	16490	
0	2	0	230	17	0	14	032					CLA	H9P27		16500	
0	2	0	231	13	0	14	1	073				STO	VAR4		16510	
0	2	0	232	5	0	14	045					CIO	045	SET I12	16520	
0	2	0	233	5	0	14	154					CIO	154		16530	
0	2	0	234	15	0	14	233		000100000			XOR	-0001000000		16540	
0	2	0	235	4	0	14	1	356				TNZ	L15PIP		16550	
0	2	0	236	5	0	14	064				L9P28	CIO	064	RST I12	16560	
0	2	0	237	17	0	14	033					CLA	H9P28		16570	
0	2	0	240	13	0	14	1	073				STO	VAR4		16580	
0	2	0	241	5	0	14	046					CIO	046	SET I10	16590	
0	2	0	242	5	0	14	154					CIO	154		16600	
0	2	0	243	15	0	14	231		000400000			XOR	-0000400000		16610	
0	2	0	244	4	0	14	1	356				TNZ	L15PIP		16620	
0	2	0	245	5	0	14	054				L9P29	CIO	054	RST I10	16630	
0	2	0	246	17	0	14	034					CLA	H9P29		16640	
0	2	0	247	13	0	14	1	073				STO	VAR4		16650	
0	2	0	250	5	0	14	051					CIO	051	SET I13	16660	
0	2	0	251	5	0	14	154					CIO	154		16670	
0	2	0	252	15	0	14	234		000040000			XOR	-0000400000		16680	
0	2	0	253	4	0	14	1	356				TNZ	L15PIP		16690	
0	2	0	254	5	0	14	070				L9P30	CIO	070	RST I3	16700	
0	2	0	255	17	0	14	035					CLA	H9P30		16710	
0	2	0	256	13	0	14	1	073				STO	VAR4		16720	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 35)

IM	IS	S	LDC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEC	NC
0	2	0	257	5	0	14	052					CIO	052	SET 11	16730	
0	2	0	260	5	0	14	154					CIO	154		16740	
0	2	0	261	15	0	14	232		000200000			XOR	=00C0200000		16750	
0	2	0	262	4	0	14	1356				L9P31	TNZ	L15PIP	RST 11	16760	
0	2	0	263	5	0	14	060					CIO	060		16770	
0	2	0	264	17	0	14	036					CLA	H9P31		16780	
0	2	0	265	13	0	14	1073					STO	VAR4		16790	
0	2	0	266	5	0	14	055					CIO	055	SET 14	16800	
0	2	0	267	5	0	14	154					CIO	154		16810	
0	2	0	270	15	0	14	235		000020000			XOR	=000002C000		16820	
0	2	0	271	4	0	14	1356					TNZ	L15PIP	RST 14	16830	
0	2	0	272	5	0	14	074				L9P32	CIO	074		16840	
0	2	0	273	17	0	14	037					CLA	H9P32		16850	
0	2	0	274	13	0	14	1073					STO	VAR4		16860	
0	2	0	275	5	0	14	056					CIO	056	SET 12	16870	
0	2	0	276	5	0	14	154					CIO	154		16880	
0	2	0	277	15	0	14	233		000100000			XOR	=0000100000		16890	
0	2	0	300	4	0	14	1356					TNZ	L15PIP	RST 12	16900	
0	2	0	301	5	0	14	064				L9P33	CIO	064		16910	
0	2	0	302	17	0	14	040					CLA	H9P33		16920	
0	2	0	303	13	0	14	1073					STC	VAR4		16930	
0	2	0	304	5	0	14	061					CIO	061	SET 15	16940	
0	2	0	305	5	0	14	154					CIO	154		16950	
0	2	0	307	4	0	14	1356		000010000			XOR	=0000010000		16960	
0	2	0	310	5	0	14	100				L9P34	CIO	100	RST 15	16970	
0	2	0	311	17	0	14	041					CLA	H9P34		16980	
0	2	0	312	13	0	14	1073					STO	VAR4		16990	
0	2	0	313	5	0	14	062					CIO	062	SET 13	17000	
0	2	0	314	5	0	14	154					CIO	154		17010	
0	2	0	315	15	0	14	234		000040000			XOR	=000004C000		17020	
0	2	0	316	4	0	14	1356					TNZ	L15PIP	RST 13	17030	
0	2	0	317	5	0	14	070				L9P35	CIO	070		17040	
0	2	0	320	17	0	14	042					CLA	H9P35		17050	
0	2	0	321	13	0	14	1073					STO	VAR4		17060	
0	2	0	322	5	0	14	065					CIO	065	SET 9	17070	
0	2	0	323	5	0	14	154					CIO	154		17080	
0	2	0	324	15	0	14	230		001000000			XOR	=0001000000		17090	
0	2	0	325	4	0	14	1356					TNZ	L15PIP	RST 9	17100	
0	2	0	326	5	0	14	050				L9P36	CIO	050		17110	
0	2	0	327	17	0	14	043					CLA	H9P36		17120	
0	2	0	330	13	0	14	1073					STO	VAR4		17130	
0	2	0	331	5	0	14	066					CIO	066	SET 14	17140	
0	2	0	332	5	0	14	154					CIO	154		17150	
0	2	0	333	15	0	14	235		000020000			XOR	=0000020000		17160	
0	2	0	334	4	0	14	1356					TNZ	L15PIP	RST 14	17170	
0	2	0	335	5	0	14	074				L9P37	CIO	074		17180	
0	2	0	336	17	0	14	044					CLA	H9P37		17190	
0	2	0	337	13	0	14	1073					STO	VAR4		17200	
0	2	0	340	5	0	14	071					CIO	071	SET 10	17210	
0	2	0	341	5	0	14	154					CIO	154		17220	
0	2	0	342	15	0	14	231		000400000			XOR	=0000400000		17230	
0	2	0	343	4	0	14	1356					TNZ	L15PIP	RST 1C	17240	
0	2	0	344	5	0	14	054				L9P38	CIO	054		17250	
0	2	0	345	17	0	14	045					CLA	H9P38		17260	
0	2	0	346	13	0	14	1073					STO	VAR4		17270	
0	2	0	347	5	0	14	072					CIO	072	SET 15	17280	
0	2	0	347	5	0	14	072					CIO	072		17290	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 36)

IM	IS	S	LDC	OP	DM	DS	9	ADR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	2	0	350	5	0	14	154					CIO	154		17300	
0	2	0	351	15	0	14	236		000010000			XOR	-0000010000		17310	
0	2	0	352	4	0	14	356				L9P39	TNZ	L15PIP	RST 15	17320	
0	2	0	353	5	0	14	100					CIO	100		17330	
0	2	0	354	17	0	14	046					CLA	H9P39		17340	
0	2	0	355	13	0	14	073					STO	VAR4		17350	
0	2	0	356	5	0	14	075					CIO	075	SET 1	17360	
0	2	0	357	5	0	14	154					CIO	154		17370	
0	2	0	360	15	0	14	221		400000000			XOR	-0400000000		17380	
0	2	0	361	4	0	14	356					TNZ	L15PIP		17390	
0	2	0	362	10	0	14	002					TRA	L9P40		17400	
0	2	1	2	0	14	111						ORG	*2,1,2,,14,		17410	
0	2	1	2	5	0	14	010				L9P40	CIO	010	RST 1	17420	
0	2	1	3	17	0	14	047					CLA	H9P40		17430	
0	2	1	4	13	0	14	073					STO	VAR4		17440	
0	2	1	5	5	0	14	076					CIO	076	SET 11	17450	
0	2	1	6	5	0	14	154					CIO	154		17460	
0	2	1	7	15	0	14	232		000200000			XOR	-0002000000		17470	
0	2	1	10	4	0	14	356					TNZ	L15PIP		17480	
0	2	1	11	5	0	14	060				L9P41	CIO	060	RST 11	17490	
0	2	1	12	17	0	14	050					CLA	H9P41		17500	
0	2	1	13	13	0	14	073					STO	VAR4		17510	
0	2	1	14	5	0	14	101					CIO	101	SET 2	17520	
0	2	1	15	5	0	14	154					CIO	154		17530	
0	2	1	16	15	0	14	223		200000000			XOR	-0200000000		17540	
0	2	1	17	4	0	14	356					TNZ	L15PIP		17550	
0	2	1	20	5	0	14	014				L9P42	CIO	014	RST 2	17560	
0	2	1	21	17	0	14	051					CLA	H9P42		17570	
0	2	1	22	13	0	14	073					STO	VAR4		17580	
0	2	1	23	5	0	14	102					CIO	102	SET 13	17590	
0	2	1	24	5	0	14	154					CIO	154		17600	
0	2	1	25	15	0	14	234		000040000			XOR	-0000040000		17610	
0	2	1	26	4	0	14	356					TNZ	L15PIP		17620	
0	2	1	27	5	0	14	070				L9P43	CIO	070	RST 2	17630	
0	2	1	30	17	0	14	052					CLA	H9P43		17640	
0	2	1	31	13	0	14	073					STO	VAR4		17650	
0	2	1	32	5	0	14	105					CIO	105	SET 3	17660	
0	2	1	33	5	0	14	154					CIO	154		17670	
0	2	1	34	15	0	14	167		100000000			XOR	-0100000000		17680	
0	2	1	35	4	0	14	356					TNZ	L15PIP		17690	
0	2	1	36	5	0	14	020				L9P44	CIO	020	RST 3	17700	
0	2	1	37	17	0	14	053					CLA	H9P44		17710	
0	2	1	40	13	0	14	073					STO	VAR4		17720	
0	2	1	41	5	0	14	104					CIO	104	SET 1	17730	
0	2	1	42	5	0	14	154					CIO	154		17740	
0	2	1	43	15	0	14	221		400000000			XOR	-0400000000		17750	
0	2	1	44	4	0	14	356					TNZ	L15PIP		17760	
0	2	1	45	5	0	14	010				L9P45	CIO	010	RST 1	17770	
0	2	1	46	17	0	14	054					CLA	H9P45		17780	
0	2	1	47	13	0	14	073					STO	VAR4		17790	
0	2	1	50	5	0	14	111					CIO	111	SET 4	17800	
0	2	1	51	5	0	14	154					CIO	154		17810	
0	2	1	52	15	0	14	222		040000000			XOR	-0040000000		17820	
0	2	1	53	4	0	14	356					TNZ	L15PIP		17830	
0	2	1	54	5	0	14	024				L9P46	CIO	024	RST 4	17840	
0	2	1	55	17	0	14	055					CLA	H9P46		17850	
0	2	1	56	13	0	14	073					STO	VAR4		17860	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 37)

1M	1S	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	2	1	57	5	0	14	112					CIC	112	SET 2	17870	
C	2	1	60	5	0	14	154					CIC	154		17880	
0	2	1	61	15	0	14	223	200000000				XOR	=0200000000		17890	
0	2	1	62	4	0	14	1356					TNZ	L15PIP	RST 2	17900	
C	2	1	63	5	0	14	014				L9P47	CLA	H9P47		17910	
0	2	1	64	17	0	14	056					STC	VAR4	SET 5	17930	
0	2	1	65	13	0	14	1073					CIC	115		17940	
0	2	1	66	5	0	14	115					CIC	154		17950	
0	2	1	67	5	0	14	154					XOR	=0020C00000		17960	
0	2	1	70	15	0	14	224	020000000				TNZ	L15PIP	RST 5	17970	
0	2	1	71	4	0	14	1356				L9P48	CIC	030		17980	
0	2	1	72	5	0	14	030					CLA	H9P48		17990	
0	2	1	73	17	0	14	057					STO	VAR4	SET 3	18000	
0	2	1	74	13	0	14	1073					CIC	116		18010	
0	2	1	75	5	0	14	116					CIC	154		18020	
0	2	1	76	5	0	14	154					XOR	=010000C000		18030	
0	2	1	77	15	0	14	167	100000000				TNZ	L15PIP	RST 3	18040	
0	2	1	100	4	0	14	1356					CIC	020		18050	
0	2	1	101	5	0	14	020				L9P49	CLA	H9P49	SET 6	18060	
0	2	1	102	17	0	14	060					STO	VAR4		18070	
0	2	1	103	13	0	14	1073					CIC	121		18080	
0	2	1	104	5	0	14	121					CIC	154		18090	
0	2	1	105	5	0	14	154					XOR	=0010000000		18100	
0	2	1	106	15	0	14	225	010000000				TNZ	L15PIP	RST 6	18110	
0	2	1	107	4	0	14	1356					CIC	034		18120	
0	2	1	110	5	0	14	034				L9P50	CLA	H9P50	SET 4	18130	
0	2	1	111	17	0	14	061					STO	VAR4		18140	
0	2	1	112	13	0	14	1073					CIC	122		18150	
0	2	1	113	5	0	14	122					CIC	154		18160	
0	2	1	114	5	0	14	154					XOR	=0040000000		18170	
0	2	1	115	15	0	14	222	040000000				TNZ	L15PIP	RST 4	18180	
0	2	1	116	4	0	14	1356					CIC	024		18190	
0	2	1	117	5	0	14	024				L9P51	CLA	H9P51	SET 7	18200	
0	2	1	120	17	0	14	062					STC	VAR4		18210	
0	2	1	121	13	0	14	1073					CIC	125		18220	
0	2	1	122	5	0	14	125					CIC	154		18230	
0	2	1	123	5	0	14	154					XOR	=0004000000		18240	
0	2	1	124	15	0	14	226	004000000				TNZ	L15PIP	RST 7	18250	
0	2	1	125	4	0	14	1356					CIC	040		18260	
0	2	1	126	5	0	14	040				L9P52	CLA	H9P52	SET 5	18270	
0	2	1	127	17	0	14	063					STO	VAR4		18280	
0	2	1	130	13	0	14	1073					CIC	126		18290	
0	2	1	131	5	0	14	126					CIC	154		18300	
0	2	1	132	5	0	14	154					XOR	=0020C00000		18310	
0	2	1	133	15	0	14	224	020000000				TNZ	L15PIP	RST 5	18320	
C	2	1	134	4	0	14	1356					CIC	030		18330	
0	2	1	135	5	0	14	030				L9P53	CLA	H9P53	SET 8	18340	
0	2	1	136	17	0	14	064					STO	VAR4		18350	
0	2	1	137	13	0	14	1073					CIC	131		18360	
0	2	1	140	5	0	14	131					CIC	154		18370	
0	2	1	141	5	0	14	154					XOR	=0002000000		18380	
0	2	1	142	15	0	14	227	002000000				TNZ	L15PIP	RST 8	18390	
0	2	1	143	4	0	14	1356				L9P54	CIC	044		18400	
0	2	1	144	5	0	14	044					CLA	H9P54		18410	
0	2	1	145	17	0	14	065					STC	VAR4		18420	
0	2	1	146	13	0	14	1073					CIC	132	SET 6	18430	
0	2	1	147	5	0	14	132									

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 38)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	2	1	150	5	0	14	154					CIO	154		18440	
0	2	1	151	15	0	14	225		010000000			XOR	-0010000000		18450	
0	2	1	152	4	0	14	1	356			L9P55	TNZ	L15P1P	RST 6	18460	
0	2	1	153	5	0	14	034					CIO	034		18470	
0	2	1	154	17	0	14	066					CLA	H9P55		18480	
0	2	1	155	13	0	14	1	073				STO	VAR4	SET 9	18490	
0	2	1	156	5	0	14	135					CIO	135		18500	
0	2	1	157	5	0	14	154					CIO	154		18510	
0	2	1	160	15	0	14	230		001000000			XOR	-0001000000		18520	
0	2	1	161	4	0	14	1	356			L9P56	TNZ	L15P1P	RST 9	18530	
0	2	1	162	5	0	14	050					CIO	050		18540	
0	2	1	163	17	0	14	067					CLA	H9P56		18550	
0	2	1	164	13	0	14	1	073				STO	VAR4	SET 7	18560	
0	2	1	165	5	0	14	136					CIO	136		18570	
0	2	1	166	5	0	14	154					CIO	154		18580	
0	2	1	167	15	0	14	226		004000000			XOR	-0004000000		18590	
0	2	1	170	4	0	14	1	356			L9P57	TNZ	L15P1P	RST 7	18600	
0	2	1	171	5	0	14	040					CIO	040		18610	
0	2	1	172	17	0	14	070					CLA	H9P57		18620	
0	2	1	173	13	0	14	1	073				STO	VAR4	SET 10	18630	
0	2	1	174	5	0	14	141					CIO	141		18640	
0	2	1	175	5	0	14	154					CIO	154		18650	
0	2	1	176	15	0	14	231		000400000			XOR	-0000400000		18660	
0	2	1	177	4	0	14	1	356			L9P58	TNZ	L15P1P	RST10	18670	
0	2	1	200	5	0	14	054					CIO	054		18680	
0	2	1	201	17	0	14	071					CLA	H9P58		18690	
0	2	1	202	13	0	14	1	073				STO	VAR4	SET 8	18700	
0	2	1	203	5	0	14	142					CIO	142		18710	
0	2	1	204	5	0	14	154					CIO	154		18720	
0	2	1	205	15	0	14	227		002000000			XOR	-0002000000		18730	
0	2	1	206	4	0	14	1	356			L9P59	TNZ	L15P1P	RST 8	18740	
0	2	1	207	5	0	14	044					CIO	044		18750	
0	2	1	210	17	0	14	072					CLA	H9P59		18760	
0	2	1	211	13	0	14	1	073				STO	VAR4	SET 11	18770	
0	2	1	212	5	0	14	145					CIO	145		18780	
0	2	1	213	5	0	14	154					CIO	154		18790	
0	2	1	214	15	0	14	232		000200000			XOR	-0000200000		18800	
0	2	1	215	4	0	14	1	356			L9P60	TNZ	L15P1P	RST 11	18810	
0	2	1	216	5	0	14	060					CIO	060		18820	
0	2	1	217	17	0	14	073					CLA	H9P60		18830	
0	2	1	220	13	0	14	1	073				STO	VAR4	SET 9	18840	
0	2	1	221	5	0	14	146					CIO	146		18850	
0	2	1	222	5	0	14	154					CIO	154		18860	
0	2	1	223	15	0	14	230		001000000			XOR	-0001000000		18870	
0	2	1	224	4	0	14	1	356			L9P61	TNZ	L15P1P	RST 9	18880	
0	2	1	225	5	0	14	050					CIO	050		18890	
0	2	1	226	17	0	14	074					CLA	H9P61		18900	
0	2	1	227	13	0	14	1	073				STO	VAR4	SET 12	18910	
0	2	1	230	5	0	14	151					CIO	151		18920	
0	2	1	231	5	0	14	154					CIO	154		18930	
0	2	1	232	15	0	14	233		000100000			XOR	-0000100000		18940	
0	2	1	233	4	0	14	1	356			L9P62	TNZ	L15P1P	RST 12	18950	
0	2	1	234	5	0	14	064					CIO	064		18960	
0	2	1	235	17	0	14	075					CLA	H9P62		18970	
0	2	1	236	13	0	14	1	073				STO	VAR4	SET 10	18980	
0	2	1	237	5	0	14	152					CIO	152		18990	
0	2	1	240	5	0	14	154					CIO	154		19000	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 39)

IM	IS	S	LOC	OP	DP	RS	Y	ADR	OCT	VAL	LHS	UPC	VARIABLE	COMMENT	SPC
0	2	1	241	15	0	14	231		000400000			XCR	=0000400000		19016
0	2	1	242	4	C	14	1	356			L9P63	TNZ	L15PIP	RST 16	19026
C	2	1	243	5	C	14	054					CIC	054		19036
C	2	1	244	17	0	14	076					CLA	F9P63		19046
0	2	1	245	13	0	14	1	073				STL	VAR4		19056
0	2	1	246	5	C	14	156					CIC	156	SET 11	19066
0	2	1	247	5	0	14	154					CIC	154		19076
0	2	1	250	15	C	14	232		000200000			XDR	=0002000000		19086
C	2	1	251	4	C	14	1	356			L9P64	TNZ	L15PIP	RST 11	19096
0	2	1	252	5	0	14	060					CIC	060		19106
0	2	1	253	17	C	14	077					CLA	F9P64		19116
0	2	1	254	13	C	14	1	073				STL	VAR4		19126
0	2	1	255	5	C	14	162					CIC	162		19136
0	2	1	256	5	C	14	154					CIC	154		19146
0	2	1	257	15	C	14	233		000100000			XDR	=0001000000		19156
0	2	1	260	4	C	14	1	356			L9P65	TNZ	L15PIP	RST 12	19166
0	2	1	261	5	0	14	064					CIC	054		19176
0	2	1	262	17	C	14	100					CLA	F9P65		19186
C	2	1	263	13	C	14	1	073				STL	VAR4		19196
0	2	1	264	5	0	14	166					CIC	166	SET 13	19206
0	2	1	265	5	0	14	154					CIC	154		19216
0	2	1	266	15	C	14	234		000040000			XDR	=0000400000		19226
0	2	1	267	4	C	14	1	356			L9P66	TNZ	L15PIP	RST 13	19236
0	2	1	270	5	C	14	070					CIC	070		19246
0	2	1	271	17	C	14	101					CLA	F9P66		19256
0	2	1	272	13	C	14	1	073				STL	VAR4		19266
0	2	1	273	5	C	14	172					CIC	172	SET 14	19276
0	2	1	274	5	0	14	154					CIC	154		19286
0	2	1	275	15	C	14	235		000020000			XCR	=0000200000		19296
0	2	1	276	4	C	14	1	356			L9P67	TNZ	L15PIP	RST 14	19306
0	2	1	277	5	0	14	074					CIC	074		19316
0	2	1	300	17	C	14	102					CLA	F9P67		19326
0	2	1	301	13	C	14	1	073				STL	VAR4		19336
0	2	1	302	5	0	14	176					CIC	176	SET 15	19346
0	2	1	303	5	C	14	154					CIC	154		19356
0	2	1	304	15	C	14	236		000010000			XDR	=0000100000		19366
0	2	1	305	4	C	14	1	356			L9P68	TNZ	L15PIP	RST 15	19376
0	2	1	306	5	0	14	100					CIC	100		19386
0	2	1	307	17	0	14	103					CLA	F9P68		19396
0	2	1	310	13	C	14	1	073				STL	VAR4		19406
0	2	1	311	5	0	14	202					CIC	202	SET 17	19416
0	2	1	312	5	0	14	154					CIC	154		19426
0	2	1	313	15	C	14	233		000100000			XDR	=0001000000		19436
0	2	1	314	4	C	14	1	356			L9P69	TNZ	L15PIP	RST 14	19446
0	2	1	315	5	C	14	064					CIC	064		19456
0	2	1	316	17	0	14	104					CLA	F9P69		19466
0	2	1	317	13	0	14	1	073				STL	VAR4		19476
0	2	1	320	5	0	14	206					CIC	206	SET 14	19486
0	2	1	321	5	0	14	154					CIC	154		19496
0	2	1	322	15	C	14	235		000020000			XDR	=0000200000		19506
0	2	1	323	4	0	14	1	356			L9P70	TNZ	L15PIP	RST 14	19516
0	2	1	324	5	0	14	074					CIC	074		19526
0	2	1	325	17	C	14	105					CLA	F9P70		19536
0	2	1	326	13	C	14	1	073				STL	VAR4		19546
0	2	1	327	5	0	14	212					CIC	212	SET 1	19556
0	2	1	330	5	C	14	154					CIC	154		19566
0	2	1	331	15	0	14	221		400000000			XDR	=4000000000		19576

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 40)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	2	1	332	4	0	14	1	356				TNZ	L15PIP		19580	
0	2	1	333	5	0	14	010				L9P71	C10	O10	RST 1	19590	
0	2	1	334	17	0	14	106					CLA	M9P71		19600	
0	2	1	335	13	0	14	073					STO	VAR4		19610	
0	2	1	336	5	0	14	216					C10	216	SET 2	19620	
0	2	1	337	5	0	14	154					C10	154		19630	
0	2	1	340	15	0	14	223		200000000			XOR	=0200000000		19640	
0	2	1	341	4	0	14	1356					TNZ	L15PIP		19650	
0	2	1	342	5	0	14	014				L9P72	C10	O14	RST 2	19660	
0	2	1	343	17	0	14	107					CLA	M9P72		19670	
0	2	1	344	13	0	14	073					STO	VAR4		19680	
0	2	1	345	5	0	14	155					C10	155		19690	
0	2	1	346	5	0	14	161					C10	161		19700	
0	2	1	347	5	0	14	165					C10	165		19710	
0	2	1	350	5	0	14	171					C10	171		19720	
0	2	1	351	5	0	14	175					C10	175		19730	
0	2	1	352	4	0	14	1356					TNZ	L15PIP		19740	
0	2	1	353	5	0	14	154					C10	154		19750	
0	2	1	354	4	0	14	1356					TNZ	L15PIP		19760	
0	2	1	355	00	0	14	237		140014430			TRA	L10P1		19770	
0	2	1	356	13	0	14	1377				L15PIP	STO	777		19780	
0	2	1	357	13	0	14	1076				LPPA	STO	TEMP		19790	
0	2	1	360	17	0	14	1377					CLA	777		19800	
0	2	1	361	13	0	14	1071					STO	VAR2		19810	
0	2	1	362	17	0	14	1073					CLA	VAR4		19820	
0	2	1	363	13	0	14	1070					STO	VAR1		19830	
0	2	1	364	17	0	14	1020					CLA	ZERO		19840	
0	2	1	365	13	0	14	1073					STO	VAR4		19850	
0	2	1	366	0	0	14	1023					HOP	M9P3		19860	
0	2	1	367	17	0	14	1076					CLA	TEMP		19870	
0	2	1	370	0	0	14	1026					HOP	M95P1		19880	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 41)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	3	0	31	0	14	112						ORG	BEGIN TEST OF CIO CODES GROUP 1		19900	
0	3	0	31	16	0	14					L10P1	CCS	*3,31,14,		19910	
0	3	0	32	17	0	14						CLA	0,14		19920	
0	3	0	33	13	0	14						STO	H10P1		19930	
0	3	0	34	5	0	14						CIO	VAR4		19940	
0	3	0	35	5	0	14						CIC	002		19950	
0	3	0	36	5	0	14						CIC	006		19960	
0	3	0	37	5	0	14						CIC	012		19970	
0	3	0	38	5	0	14						CIC	016		19980	
0	3	0	39	5	0	14						CIC	022		19990	
0	3	0	40	5	0	14						CIC	026		20000	
0	3	0	41	5	0	14						CIC	032		20010	
0	3	0	42	5	0	14						CIC	036		20020	
0	3	0	43	5	0	14						CIC	042		20030	
0	3	0	44	5	0	14						CIC	046		20040	
0	3	0	45	5	0	14						CIC	052		20050	
0	3	0	46	5	0	14						CIC	056		20060	
0	3	0	47	5	0	14						CIC	062		20070	
0	3	0	50	5	0	14						CIC	066		20080	
0	3	0	51	5	0	14						CIC	072		20090	
0	3	0	53	5	0	14						CIC	000		20100	
0	3	0	54	5	0	14						CIC	154		20110	
0	3	0	55	15	0	14			777770000			XOR	=077770000		20120	
0	3	0	56	4	0	14						TNZ	L15P1Q		20130	
0	3	0	57	5	0	14						CIC	010		20140	
0	3	0	60	5	0	14						CIO	154		20150	
0	3	0	61	15	0	14			377770000			XOR	=037770000		20160	
0	3	0	62	4	0	14						TNZ	L15P1Q		20170	
0	3	0	63	17	0	14					L10P2	CLA	H10P2		20180	
0	3	0	64	13	0	14						STU	VAR4		20190	
0	3	0	65	17	0	14						CLA	ZERO		20200	
0	3	0	66	5	0	14						CIC	014		20210	
0	3	0	67	4	0	14						TNZ	L15P1Q		20220	
0	3	0	70	17	0	14					L10P3	CLA	H10P3		20230	
0	3	0	71	13	0	14						STC	VAR4		20240	
0	3	0	72	5	0	14						CIC	154		20250	
0	3	0	73	15	0	14			177770000			XOR	=017770000		20260	
0	3	0	74	4	0	14						TNZ	L15P1Q		20270	
0	3	0	75	17	0	14					L10P4	CLA	H10P4		20280	
0	3	0	76	13	0	14						STO	VAR4		20290	
0	3	0	77	5	0	14						CIO	002		20300	
0	3	0	100	17	0	14			470000000			CLA	=047000000		20310	
0	3	0	101	5	0	14						CIC	020		20320	
0	3	0	102	15	0	14			470000000			XOR	=047000000		20330	
0	3	0	103	4	0	14						TNZ	L15P1Q		20340	
0	3	0	104	5	0	14						CIC	154		20350	
0	3	0	105	15	0	14			477770000			XOR	=047770000		20360	
0	3	0	106	4	0	14						TNZ	L15P1Q		20370	
0	3	0	110	13	0	14					L10P5	CLA	H10P5		20380	
0	3	0	111	17	0	14						STC	VAR4		20390	
0	3	0	112	5	0	14			110000000			CLA	=011000000		20400	
0	3	0	113	5	0	14						CIO	024		20410	
0	3	0	114	15	0	14			437770000			XOR	=043770000		20420	
0	3	0	115	4	0	14						TNZ	L15P1Q		20430	
0	3	0	116	17	0	14					L10P6	CLA	H10P6		20440	
0	3	0	117	13	0	14						STC	VAR4		20450	
0	3	0	117	13	0	14						STC	VAR4		20460	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 42)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	3	0	120	17	0	14	225		010000000		CLA	-0010000000			20470	
0	3	0	121	5	0	14	030				CIO	030		RST 5, 130 SET 3 THRU 9	20480	
0	3	0	122	5	0	14	154				XOR	L54		230 SP	20490	
0	3	0	123	15	0	14	247		417770000		XOR	-0417770000			20500	
0	3	0	124	4	0	14	1305				TNZ	L15P1Q			20510	
0	3	0	125	17	0	14	121			L10P7	CLA	H10P7			20520	
0	3	0	126	13	0	14	1073				CLA	VAR4			20530	
0	3	0	127	17	0	14	020				CLA	ZERO			20540	
0	3	0	130	5	0	14	034				CIO	034		RST 6, 234 SP	20550	
0	3	0	131	5	0	14	154				CIO	154			20560	
0	3	0	132	15	0	14	250		407770000		XOR	-0407770000			20570	
0	3	0	133	4	0	14	1305				TNZ	L15P1Q			20580	
0	3	0	134	17	0	14	122			L10P8	CLA	H10P8			20590	
0	3	0	135	13	0	14	1073				STO	VAR4			20600	
0	3	0	136	17	0	14	020				CLA	ZERO			20610	
0	3	0	137	5	0	14	040				CIO	040		RST 7	20620	
0	3	0	140	5	0	14	154				CIO	154		140 PLT X, 240 SP	20630	
0	3	0	141	15	0	14	251				XOR	-0403770000			20640	
0	3	0	142	4	0	14	1305		403770000		TNZ	L15P1Q			20650	
0	3	0	143	17	0	14	123			L10P9	CLA	H10P9			20660	
0	3	0	144	13	0	14	1073				STO	VAR4			20670	
0	3	0	145	17	0	14	020				CLA	ZERO			20680	
0	3	0	146	5	0	14	044				CIO	044			20690	
0	3	0	147	5	0	14	154				CIO	154		RST 8	20700	
0	3	0	150	15	0	14	252		401770000		XOR	-0401770000		144 PLT Y, 244 SP	20710	
0	3	0	151	4	0	14	1305				TNZ	L15P1Q			20720	
0	3	0	152	17	0	14	124			L10P10	CLA	H10P10			20730	
0	3	0	153	13	0	14	1073				STO	VAR4			20740	
0	3	0	154	17	0	14	020				CLA	ZERO			20750	
0	3	0	155	5	0	14	050				CIO	050		RST 9	20760	
0	3	0	156	5	0	14	154				CIO	154		150 PLT Z, 250 SP	20770	
0	3	0	157	15	0	14	253		400770000		XOR	-0400770000			20780	
0	3	0	160	4	0	14	1305				TNZ	L15P1Q			20790	
0	3	0	161	17	0	14	125			L10P11	CLA	H10P11			20800	
0	3	0	162	13	0	14	1073				STO	VAR4			20810	
0	3	0	163	17	0	14	020				CLA	ZERO			20820	
0	3	0	164	5	0	14	054				CIO	054			20830	
0	3	0	165	4	0	14	1305				TNZ	L15P1Q			20840	
0	3	0	166	17	0	14	126			L10P12	CLA	H10P12			20850	
0	3	0	170	13	0	14	1073				STO	VAR4			20860	
0	3	0	171	15	0	14	254		400370000		XOR	-0400370000			20870	
0	3	0	172	4	0	14	1305				TNZ	L15P1Q			20880	
0	3	0	173	17	0	14	127			L10P13	CLA	H10P13			20890	
0	3	0	174	13	0	14	1073				STO	VAR4			20900	
0	3	0	175	17	0	14	167		100000000		CLA	-0100000000			20920	
0	3	0	176	5	0	14	060				CIO	060			20930	
0	3	0	177	5	0	14	154				CIO	154		RST 11	20940	
0	3	0	200	15	0	14	255		400170000		XOR	-0400170000		160 SET 3,8,12	20950	
0	3	0	201	4	0	14	1305				TNZ	L15P1Q		260 SP	20960	
0	3	0	202	17	0	14	130			L10P14	CLA	H10P14			20970	
0	3	0	203	13	0	14	1073				STO	VAR4			20980	
0	3	0	204	5	0	14	084				CIO	084			20990	
0	3	0	205	5	0	14	154				CIO	154		RST 12	21000	
0	3	0	206	15	0	14	256		400070000		XOR	-0400070000		164 PRT OCTAL	21010	
0	3	0	207	4	0	14	1305				TNZ	L15P1Q		264 SP	21020	
0	3	0	210	17	0	14	131			L10P15	CLA	H10P15			21030	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 43)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEC	NO
0	3	0	211	13	0	14	1	073				STO	VAR4		21040	
0	3	0	212	5	0	14	1	070				CIO	070	RST 13	21050	
0	3	0	213	5	0	14	1	154				CIO	154	170 PRT BCD	21060	
0	3	0	214	15	0	14	1	257	400030000			XOR	=0400030000	270 SP	21070	
0	3	0	215	4	0	14	1	305			L10P16	TNZ	L15P1Q		21080	
0	3	0	216	17	0	14	1	132				CLA	H10P16		21090	
0	3	0	217	13	0	14	1	073				STO	VAR4		21100	
0	3	0	220	5	0	14	1	074				CIO	074	174,274 SP	21110	
0	3	0	221	5	0	14	1	154				CIO	154		21120	
0	3	0	222	15	0	14	1	260	400010000			XOR	=0400010000		21130	
0	3	0	223	4	0	14	1	305			L10P17	TNZ	L15P1Q		21140	
0	3	0	224	17	0	14	1	133				CLA	H10P17		21150	
0	3	0	225	13	0	14	1	073				VAR4	VAR4		21160	
0	3	0	226	5	0	14	1	100				CIO	100	RST 15	21170	
0	3	0	227	5	0	14	1	154				CIO	154	200,300 SP	21180	
0	3	0	230	15	0	14	1	221	400000000			XOR	=0400000000		21190	
0	3	0	231	4	0	14	1	305				TNZ	L15P1Q		21200	
0	3	0	232	17	0	14	1	134				TEST	DISCRETE OUTPUTS + INPUTS ALL ZERO		21210	
0	3	0	233	13	0	14	1	073			L10P18	CLA	H10P18		21220	
0	3	0	234	17	0	14	1	020				STC	VAR4		21230	
0	3	0	235	5	0	14	1	210				CLA	ZERO		21240	
0	3	0	236	4	0	14	1	305				CIO	210	RESET 00 S	21250	
0	3	0	237	17	0	14	1	261	000000006			TNZ	L15P1Q	214,220 READ A,B SWTS	21260	
0	3	0	240	5	0	14	1	214				CLA	=0000000006		21270	
0	3	0	241	6	0	14	1	262	000001760			CIO	214	READ A SWTS	21280	
0	3	0	242	4	0	14	1	305				ANC	=0000001760	17-22 00 S + DI S ALL DOWN	21290	
0	3	0	243	17	0	14	1	135				TNZ	L15P1Q	210 SET 00 1,2	21300	
0	3	0	244	13	0	14	1	073				CLA	H10P19		21310	
0	3	0	245	17	0	14	1	263	660000176			STO	VAR4		21320	
0	3	0	246	5	0	14	1	110				CLA	=0660000176		21330	
0	3	0	247	5	0	14	1	154				CIC	110	C10 RST1, 210 SET D.O.	21340	
0	3	0	250	15	0	14	1	221	400000000			CIO	154	114 STOP PRG, 120 SET 5	21350	
0	3	0	251	4	0	14	1	305				XOR	=0400000000	130 SET 5,7,8	21360	
0	3	0	252	13	0	14	1	073			L10P20	TNZ	L15P1Q		21370	
0	3	0	253	17	0	14	1	136				CLA	H10P20		21380	
0	3	0	254	5	0	14	1	004				STC	VAR4		21390	
0	3	0	255	17	0	14	1	264	300000040			CIC	006	SET 2	21400	
0	3	0	256	5	0	14	1	214				CLA	=03000000040		21410	
0	3	0	257	6	0	14	1	262	000001760			CIC	214	CHECK FOR D.O. SET	21420	
0	3	0	260	4	0	14	1	305				ANC	=0000001760		21430	
0	3	0	261	5	0	14	1	154				TNZ	L15P1Q		21440	
0	3	0	262	15	0	14	1	265	600000000			CIO	154	224 ACC SET 3	21450	
0	3	0	263	4	0	14	1	305				XOR	=0600000000	204 TURN ON P20 LIGHT	21460	
0	3	0	264	17	0	14	1	137				TNZ	L15P1Q	C14 RST 2	21470	
0	3	0	265	13	0	14	1	073				CLA	H10P21		21480	
0	3	0	266	5	0	14	1	072				STO	VAR4		21490	
0	3	0	267	17	0	14	1	266	120000000			CIO	072	SET 15	21500	
0	3	0	270	5	0	14	1	104				CLA	=0120000000		21510	
0	3	0	271	5	0	14	1	154				CIO	104	124 SET 6,7,8	21520	
0	3	0	272	15	0	14	1	267	600010000			CIO	154	100 RST 15,004 FORCED MOP.	21530	
0	3	0	273	4	0	14	1	305				XOR	=0600010000	304 SP	21540	
0	3	0	274	17	0	14	1	057				TNZ	L15P1Q		21550	
0	3	0	275	14	0	14	1	302				CLA	LCR4	IS ROUTINE 4 SELECTED	21560	
0	3	0	276	5	0	14	1	010				TMI	L10P22		21570	
0	3	0	277	5	0	14	1	014				CIO	010		21580	
0	3	0	277	5	0	14	1	014				CIC	014		21590	
0	3	0	277	5	0	14	1	014				CIC	014		21600	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 44)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	3	0	300	5	0	14	100					CIG	100		21610	
0	3	0	301	10	0	14	1045					TRA	L10P27		21620	
0	3	0	302	17	0	14	140				L10P22	CLA	H10P22		21630	
0	3	0	303	13	0	14	1073					STU	VAR4		21640	
0	3	0	304	5	0	14	012					CLA	012	SET3	21650	
0	3	0	305	17	0	14	270		460000000			CLA	=04600000000		21660	
0	3	0	306	5	0	14	120					C10	120	SET 5,7,9	21670	
0	3	0	307	17	0	14	1055					CLA	LCR2		21680	
0	3	0	310	14	0	14	312					TMT	**2		21700	
0	3	0	311	10	0	14	313					TRA	L20P2A		21710	
0	3	0	312	00	0	14	271		120000270			TRA*			21720	
0	3	0	313	17	0	14	272		000000004			CLA	=00000000004		21730	
0	3	0	314	5	0	14	210					C10	210		21740	
0	3	0	315	17	0	14	1020					CLA	ZERO		21750	
0	3	0	316	5	0	14	210					C10	210		21760	
0	3	0	317	5	0	14	154					ANC	=017770000	124 SET 3,7,8,130 SET 3 THRU 9	21770	
0	3	0	320	6	0	14	242		177770000			XOR	=0125010C0C	020 RST 3,100 RST 15,320 SP	21780	
0	3	0	321	15	0	14	273		125010000			C10	120,124,130 MAY SET 1 OR 2 IF CASE SHIFT OCCURS	21790		
0	3	0	322	4	0	14	1305					TNZ	L15P1Q		21800	
0	3	0	323	17	0	14	141				L10P23	CLA	H10P23		21810	
0	3	0	324	13	0	14	1073					STU	VAR4		21820	
0	3	0	325	5	0	14	010					C10	010	RESET 1,3,5,7,9,15	21830	
0	3	0	326	5	0	14	020					C10	020		21840	
0	3	0	327	5	0	14	030					C10	030		21850	
0	3	0	330	5	0	14	040					C10	040		21860	
0	3	0	331	5	0	14	050					C10	050		21870	
0	3	0	332	5	0	14	100					C10	100		21880	
0	3	0	333	5	0	14	016					C10	016		21890	
0	3	0	334	17	0	14	274		510000000			CLA	=05100000000		21900	
0	3	0	335	5	0	14	124					C10	124	SET 6,7,8	21910	
0	3	0	336	15	0	14	274		510000000			XOR	=05100000000	154 READ INT REG	21920	
0	3	0	337	4	0	14	1305					TNZ	L15P1Q		21930	
0	3	0	340	17	0	14	142				L10P24	CLA	H10P24	024 RST 4,120 SET 3,7,9	21940	
0	3	0	341	13	0	14	1073					STU	VAR4	224 SET 1,3,6,134 SET 8,10,12	21950	
0	3	0	342	17	0	14	272		000000004			CLA	=00000000004		21960	
0	3	0	343	5	0	14	210					C10	210		21970	
0	3	0	344	17	0	14	1020					CLA	ZERU		21980	
0	3	0	345	5	0	14	210					C10	210		21990	
0	3	0	346	5	0	14	154					CLA	154	144 PLT,164 PRT OCTAL	22000	
0	3	0	347	6	0	14	242		177770000			ANC	=017770000	174,324 SP	22010	
0	3	0	350	15	0	14	275		056000000			XOR	=005600000		22020	
0	3	0	351	4	0	14	1305					TNZ	L15P1Q		22030	
0	3	0	352	10	0	14	1002					TRA	L10P25		22040	
0	3	1	2	17	0	14	113					ORG	,3,1,2,,14,		22050	
0	3	1	3	13	0	14	143				L10P25	CLA	H10P25		22060	
0	3	1	4	5	0	14	020					STC	VAR4		22070	
0	3	1	5	5	0	14	024					C10	020	RST 3,4,7,8	22080	
0	3	1	6	5	0	14	040					C10	040		22090	
0	3	1	7	5	0	14	044					C10	044		22100	
0	3	1	10	5	0	14	022					C10	022		22110	
0	3	1	11	17	0	14	276		300000000			CLA	=03000000000		22120	
0	3	1	12	5	0	14	130					CLA	130		22130	
0	3	1	13	17	0	14	272		000000004			CLA	=00000000004		22140	
0	3	1	14	5	0	14	210					C10	210	SET 5	22150	
0	3	1	15	17	0	14	1020					CLA	ZERO	SET 4,5,6,7,8	22160	
0	3	1	15	17	0	14	1020					CLA	ZERO		22170	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 45)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	3	1	16	5	0	14		210				C10	210		22180	
0	3	1	17	5	0	14		154				C10	154		22190	
0	3	1	20	6	0	14		242	177770000			ANC	-0177770000	030 RST 5,134 SET 7,12	22200	
0	3	1	21	15	0	14		277	076000000			XDR	=0076000000	120 SET 3,6,R,160 SET 3,8,12	22210	
0	3	1	22	4	0	14		305			L10P26	TNZ	L15PIQ	110 HOP, 170 PRT 8CD	22220	
0	3	1	23	17	0	14		144				CLA	H10P26	230 SP	22230	
0	3	1	24	13	0	14		073				STO	VAR4		22240	
0	3	1	25	5	0	14		010				C10	010	RST 1 THRU 5,7,8	22250	
0	3	1	26	5	0	14		014				C10	014		22260	
0	3	1	27	5	0	14		024				C10	020		22270	
0	3	1	30	5	0	14		024				C10	024		22280	
0	3	1	31	5	0	14		030				C10	030		22290	
0	3	1	32	5	0	14		040				C10	040		22300	
0	3	1	33	5	0	14		044				C10	044		22310	
0	3	1	34	17	0	14		300	060000000			CLA	=0060000000		22320	
0	3	1	35	5	0	14		134	000000004			C10	134	SET 11,14	22330	
0	3	1	36	17	0	14		272				CLA	=0000000004		22340	
0	3	1	37	5	0	14		210				C10	210		22350	
0	3	1	40	17	0	14		020				CLA	ZERO		22360	
0	3	1	41	5	0	14		210				C10	210		22370	
0	3	1	42	5	0	14		154				C10	154	034 RST 6,124 SET 5,7,8	22380	
0	3	1	43	15	0	14		301	010220000			XDR	=0102200000	130 SET 5,7,R,164 PRT OCTAL	22390	
0	3	1	44	4	0	14		102			L10P27	TNZ	L15PIQ	234 SP	22400	
0	3	1	45	17	0	14		145				CLA	H10P27		22410	
0	3	1	46	13	0	14		073				STG	VAR4		22420	
0	3	1	47	5	0	14		034				C10	034		22430	
0	3	1	50	5	0	14		060				C10	060		22440	
0	3	1	51	5	0	14		074				C10	074		22450	
0	3	1	52	5	0	14		032				C10	032	SET 7	22460	
0	3	1	53	5	0	14		036				C10	036	SET 8	22470	
0	3	1	54	5	0	14		042				C10	042	SET 9	22480	
0	3	1	55	17	0	14		020				CLA	ZERO		22490	
0	3	1	56	5	0	14		140				C10	140	040 RST 7	22500	
0	3	1	57	5	0	14		144				C10	144	044 RST 8	22510	
0	3	1	60	5	0	14		154				C10	154		22520	
0	3	1	61	15	0	14		302	007000000			XDR	=0007000000		22530	
0	3	1	62	4	0	14		102			L10P28	TNZ	L15PIQ		22540	
0	3	1	63	17	0	14		146				CLA	H10P28		22550	
0	3	1	64	13	0	14		073				STC	VAR4		22560	
0	3	1	65	17	0	14		020				CLA	ZERO		22570	
0	3	1	66	5	0	14		150				C10	150		22580	
0	3	1	67	4	0	14		102				TNZ	L15PIQ	154 READ INT REG	22590	
0	3	1	70	5	0	14		154				C10	154		22600	
0	3	1	71	15	0	14		302	007000000			XDR	=0007000000	050 RST 9	22610	
0	3	1	72	4	0	14		102			L10P29	TNZ	L15PIQ		22620	
0	3	1	73	17	0	14		147				CLA	H10P29		22630	
0	3	1	74	13	0	14		073				STO	VAR4		22640	
0	3	1	75	5	0	14		052				C10	052	SET 11	22650	
0	3	1	76	17	0	14		060				CLA	LCR5	IS ROUTINE 5 SELECTED	22660	
0	3	1	77	14	0	14		103				TNI	**4		22670	
0	3	1	100	17	0	14		303	132100000			CLA	=01321	SET 3,5,6,8,12	22680	
0	3	1	101	5	0	14		224				C10	224		22690	
0	3	1	102	10	0	14		114				TRA	L10P30		22700	
0	3	1	103	17	0	14		304	130000000			CLA	=0130000000		22710	
0	3	1	104	5	0	14		160				C10	160		22720	
0	3	1	105	17	0	14		305	000000176			CLA	=0000000176	SET 3,5,6,8,12	22730	
0	3	1	106	5	0	14		210				C10	210	RESET DATA LINES	22740	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 46)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SPC	NC
0	3	1	107	17	0	14	1	020			CLA	ZERU			22750	
0	3	1	110	5	0	14	210				CIC	210			22760	
0	3	1	111	5	0	14	154				CIC	154			22770	
0	3	1	112	15	0	14	306	137300000			XDR	=013730C000	060 RST 11,164 PRT OCTAL		22780	
0	3	1	113	4	0	14	305				TNZ	L15PIQ	260 SP		22790	
0	3	1	114	17	0	14	150			L10P30	CLA	H10P30			22800	
0	3	1	115	13	0	14	173			STC	VAR4	VAR4			22810	
0	3	1	116	17	0	14	222	040000000			CLA	=0040C0C000	160 SET 4		22820	
0	3	1	117	5	0	14	164				CIC	164	064 RST 12		22830	
0	3	1	120	5	0	14	154				CIC	154			22840	
0	3	1	121	15	0	14	306	137300000			XDR	=0137300000			22850	
0	3	1	122	4	0	14	305			TNZ	L15PIQ	L15PIQ			22860	
0	3	1	123	17	0	14	151			L10P31	CLA	H10P31			22870	
0	3	1	124	13	0	14	173			STU	VAR4	VAR4			22880	
0	3	1	125	5	0	14	062			CIO	062	062	SET 13		22890	
0	3	1	126	5	0	14	170			CIO	170	170	070 RST 13		22900	
0	3	1	127	5	0	14	154			CIO	154	154			22910	
0	3	1	130	15	0	14	307	137340000			XDR	=013734C00C			22920	
0	3	1	131	4	0	14	305			TNZ	L15PIQ	L15PIQ			22930	
0	3	1	132	17	0	14	157			L10P33	CLA	H10P33			22940	
0	3	1	133	13	0	14	173			STO	VAR4	VAR4			22950	
0	3	1	134	5	0	14	066			CIO	066	066	SET 14		22960	
0	3	1	135	5	0	14	072			CIO	072	072	SET 15		22970	
0	3	1	136	17	0	14	174			CLA	ZERU	ZERU	C74 RST 14		22980	
0	3	1	140	17	0	14	261	000000006			CLA	=0000000006	204 RST P LIGHTS TO 3		23000	
0	3	1	141	5	0	14	200			CIO	200	200	210 SET D.O. 1 + 2		23010	
0	3	1	142	5	0	14	154			CIO	154	154	100 RST 15		23020	
0	3	1	143	15	0	14	310	137370000			XDR	=0137370000			23030	
0	3	1	144	4	0	14	1305			TNZ	L15PIQ	L15PIQ			23040	
0	3	1	145	17	0	14	153			L10P34	CLA	H10P34			23050	
0	3	1	146	13	0	14	173			STC	VAR4	VAR4			23060	
0	3	1	147	17	0	14	173			CLA	ZERU	ZERU			23070	
0	3	1	150	5	0	14	214			CIC	214	214	CHECK FOR DU 5+6		23080	
0	3	1	151	6	0	14	262	000001760			ANC	=000001760			23090	
0	3	1	152	4	0	14	1305			TNZ	L15PIQ	L15PIQ			23100	
0	3	1	153	17/	0	14	154			L10P35	CLA	H10P35			23110	
0	3	1	154	13	0	14	173			STO	VAR4	VAR4			23120	
0	3	1	155	17	0	14	173			CLA	ZERU	ZERU			23130	
0	3	1	156	5	0	14	204			CIO	204	204	214 READ A SMTS		23140	
0	3	1	157	4	0	14	1305			TNZ	L15PIQ	L15PIQ			23150	
0	3	1	160	17	0	14	155			L10P36	CLA	H10P36			23160	
0	3	1	161	13	0	14	173			STO	VAR4	VAR4			23170	
0	3	1	162	17	0	14	221	400000000			CLA	=0400000000			23180	
0	3	1	163	5	0	14	220			CIO	220	220	224 SET 1		23190	
0	3	1	164	15	0	14	223	200000000			XDR	=0200000000			23200	
0	3	1	165	4	0	14	1305			TNZ	L15PIQ	L15PIQ			23210	
0	3	1	166	17	0	14	156			L10P37	CLA	H10P37			23220	
0	3	1	167	13	0	14	173			STC	VAR4	VAR4			23230	
0	3	1	170	5	0	14	154			CIC	154	154			23240	
0	3	1	171	15	0	14	310	137370000			XDR	=0137370000			23250	
0	3	1	172	4	0	14	1305			TNZ	L15PIQ	L15PIQ			23260	
0	3	1	173	17	0	14	157			L10P38	CLA	H10P38			23270	
0	3	1	174	13	0	14	173			STO	VAR4	VAR4			23280	
0	3	1	175	5	0	14	020			CIO	020	020	RESET INT REG		23290	
0	3	1	176	5	0	14	030			CIO	030	030			23300	
0	3	1	177	5	0	14	034			CIC	034	034			23310	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 47)

TM	IS	S	LOC	UP	DM	DS	Y	APR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	AC
0	3	1	200	5	C	14	040					CLC	C40		23329	
0	3	1	201	5	0	14	044					CLC	044		23330	
0	3	1	202	5	C	14	050					CLC	050		23340	
0	3	1	203	5	C	14	060					CLC	060		23345	
0	3	1	204	5	C	14	064					CLC	064		23346	
0	3	1	205	5	C	14	070					CLC	070		23376	
0	3	1	206	5	0	14	074					CLC	074		23380	
0	3	1	207	5	C	14	100					CLC	100		23390	
0	3	1	210	17	0	14	305		000000176			CLC	=000000176	CIO 210 SFTS D.O.S	23405	
0	3	1	211	12	0	14	210					CLC	210		23410	
0	3	1	212	5	0	14	214					CLC	214		23420	
0	3	1	213	6	0	14	262		0000001760			ANL	=000001760		23430	
0	3	1	214	4	0	14	1 305					FNZ	CLP4		23440	
0	3	1	215	17	0	14	160					CLC	L10P43		23450	
0	3	1	216	13	0	14	1 073					STC	VAR4		23460	
0	3	1	217	17	0	14	311		000000002			CLC	VAR4	SET DO 1	23470	
0	3	1	220	5	0	14	210					CLC	210	CAL POINT NR 1	23500	
0	3	1	221	5	0	14	214					CLC	214		23510	
0	3	1	222	6	0	14	262		000001760			ANL	=000001760		23520	
0	3	1	223	15	0	14	312		000000070			XOR	=000000070		23530	
0	3	1	224	4	0	14	1 305					FNZ	L15P14		23540	
0	3	1	225	17	0	14	161					CLC	L10P40		23550	
0	3	1	226	13	0	14	1 073					STC	VAR4		23560	
0	3	1	227	17	0	14	272		000000004			CLC	VAR4	RST DO1, SET DO 2	23570	
0	3	1	230	5	0	14	210					CLC	210	CAL POINT NR 2	23590	
0	3	1	231	5	0	14	214					CLC	214		23600	
0	3	1	232	6	0	14	262		000001760			ANL	=000001760		23610	
0	3	1	233	15	0	14	313		000000040			XOR	=000000040		23620	
0	3	1	234	4	0	14	1 305					FNZ	L15P14		23630	
0	3	1	235	17	0	14	162					CLC	L10P41		23640	
0	3	1	236	13	0	14	1 073					STC	VAR4		23650	
0	3	1	237	17	0	14	314		000000010			CLC	VAR4	RST DO2, SET DO3	23660	
0	3	1	240	5	0	14	210					CLC	210	CAL POINT NR 3	23670	
0	3	1	241	5	0	14	214					CLC	214		23680	
0	3	1	242	6	0	14	262		000001760			ANL	=000001760		23690	
0	3	1	243	15	0	14	315		000000100			XOR	=000000100		23700	
0	3	1	244	4	0	14	1 305					FNZ	L15P14		23710	
0	3	1	245	17	0	14	163					CLC	L10P42		23720	
0	3	1	246	13	0	14	1 073					STC	VAR4		23730	
0	3	1	247	17	0	14	312		000000070			CLC	VAR4	RST DO 3, SET DO 4	23740	
0	3	1	250	5	0	14	210					CLC	210	CAL POINT NR 4	23750	
0	3	1	251	5	0	14	214					CLC	214		23760	
0	3	1	252	6	0	14	262		000001760			ANL	=000001760		23770	
0	3	1	253	15	0	14	316		000000200			XOR	=000000200		23780	
0	3	1	254	4	0	14	1 305					FNZ	L15P14		23790	
0	3	1	255	17	0	14	164					CLC	L10P43		23800	
0	3	1	256	13	0	14	1 073					STC	VAR4		23810	
0	3	1	257	17	0	14	313		000000040			CLC	VAR4	RST DO 4, SET DO 5	23820	
0	3	1	260	5	0	14	210					CLC	210	CAL POINT NR 5	23840	
0	3	1	261	5	0	14	214					CLC	214		23850	
0	3	1	262	6	0	14	262		000001760			ANL	=000001760		23860	
0	3	1	262	6	0	14	262					CLC	214		23870	
0	3	1	262	6	0	14	262					ANL	=000001760		23880	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 48)

IM	IS	S	LOC	OP	DM	DS	9	ADR	ICT	VAL	LMS	GPC	VARIABLE	COMMENT	SEQ	NO
0	3	1	263	15	0	14	317		000000400		XCR			TEST DD 5, DI 5 UP	23900	
0	3	1	264	4	0	14	1 305				LNZ				23900	
0	3	1	265	17	0	14	1 165				LIOP44				23910	
0	3	1	266	13	0	14	1 073				STC				23920	
0	3	1	267	17	0	14	1 315		000000100		CLA			RST DD 5, SET DC 6	23930	
0	3	1	270	5	0	14	210				CIC			CAL POINT NR 6	23940	
0	3	1	271	5	0	14	214				CIC				23950	
0	3	1	272	6	0	14	262		000001760		AND				23960	
0	3	1	273	15	0	14	320		000001000		XCR			TEST DD 6, DI 6 UP	23970	
0	3	1	274	4	0	14	1 305				LNZ				23980	
0	3	1	275	17	0	14	1 166				LIOP45				23990	
0	3	1	276	13	0	14	1 073				STC				24000	
0	3	1	277	17	0	14	1 020				CLA				24010	
0	3	1	300	5	0	14	210				CLA				24020	
0	3	1	301	5	0	14	214				CIC				24030	
0	3	1	302	6	0	14	262		000001760		AND			RST DD 6	24040	
0	3	1	303	4	0	14	1 305				LNZ			TEST RST DD 6	24050	
0	3	1	304	10	0	14	1 315				TRA				24060	
0	3	1	305	13	0	14	1 076				LIOP45				24070	
0	3	1	306	17	0	14	1 170				STC				24080	
0	3	1	307	13	0	14	1 071				CLA				24090	
0	3	1	310	17	0	14	1 113				STC				24100	
0	3	1	311	13	0	14	1 070				CLA				24110	
0	3	1	312	0	0	14	1 023				HOP				24120	
0	3	1	313	17	0	14	1 076				CLA				24130	
0	3	1	314	00	0	14	321		160000560		TRA*				24140	
									140014430		H1OP1				24150	
									140031430		H1OP2				24160	
									140036430		H1OP3				24170	
									140043430		H1OP4				24180	
									140047030		H1OP5				24190	
									140052430		H1OP6				24200	
									140061630		H1OP7				24210	
									140065030		H1OP8				24220	
									140070430		H1OP9				24230	
									140073030		H1OP10				24240	
									140075430		H1OP11				24250	
									140101030		H1OP12				24260	
									140104030		H1OP13				24270	
									140107030		H1OP14				24280	
									140112030		H1OP15				24290	
									140115030		H1OP16				24300	
									140121430		H1OP17				24310	
									140125030		H1OP18				24320	
									140132030		H1OP19				24330	
									140141030		H1OP20				24340	
									140151430		H1OP21				24350	
									140160030		H1OP22				24360	
									140001230		H1OP23				24370	
									140011630		H1OP24				24380	
									140022630		H1OP25				24390	
									140031630		H1OP26				24400	
									140035630		H1OP27				24410	
									140046230		H1OP28				24420	
											H1OP29				24430	
											H1OP30				24440	
															24450	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 49)

IM	IS	S	LDC	UP	DM	DS	Y	ADR	DCT	VAL	LHS	RPC	VARIABLE	COMMENT	SPC	NC
0	14							151	140051630		H10P31	HPC	L10P11		24460	
0	14							152	140052330		H10P33	HPC	L10P13		24470	
0	14							153	140067630		H10P34	HPC	L10P14		24480	
0	14							154	140065630		H10P35	HPC	L10P15		24490	
0	14							155	140070230		H10P36	HPC	L10P16		24500	
0	14							156	140073230		H10P37	HPC	L10P17		24510	
0	14							157	140075630		H10P38	HPC	L10P18		24520	
0	14							160	140106630		H10P39	HPC	L10P19		24530	
0	14							161	140112630		H10P40	HPC	L10P40		24540	
0	14							162	140116630		H10P41	HPC	L10P41		24550	
0	14							163	140127630		H10P42	HPC	L10P42		24560	
0	14							164	140126630		H10P43	HPC	L10P43		24570	
0	14							165	140132630		H10P44	HPC	L10P44		24580	
0	14							166	140136630		H10P45	HPC	L10P45		24590	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 50)

IM	IS	S	LDC	UP	DM	DS	9	ADR	DCI	VAL	LMS	RPC	VA	TABLE	COMMENT	SEC	NO.
0	3	1	315	17	0	14	170				L11P1	CLA	011P1			24610	
0	3	1	316	13	0	14	1 073					STC	VAK4			24620	
0	3	1	317	0	0	14	1 023					HOP	VAK4			24630	
0	3	1	320	17	0	14	1 020					CLA	VAK4			24640	
0	3	1	321	5	0	14	224					CIC	VAK4			24650	
0	3	1	322	4	0	14	1 361					FNZ	L15PIR			24660	
0	3	1	323	17	0	14	171					CLA	L11P2			24670	
0	3	1	324	13	0	14	1 073					STC	VAK4			24680	
0	3	1	325	5	0	14	154					CIC	VAK4			24690	
0	3	1	326	4	0	14	1 361					FNZ	L15PIR			24700	
0	3	1	327	17	0	14	172					CLA	L11P3			24710	
0	3	1	330	13	0	14	1 073					STC	VAK4			24720	
0	3	1	331	17	0	14	322		400000002			CLA	=04000000002			24730	
0	3	1	332	5	0	14	224					CIC	VAK4			24740	
0	3	1	333	5	0	14	154					CIC	VAK4			24750	
0	3	1	334	13	0	14	323		400200000			FNZ	=04002000000			24760	
0	3	1	335	4	0	14	1 361					CIC	L15PIR			24770	
0	3	1	336	17	0	14	173					CLA	L11P4			24780	
0	3	1	337	13	0	14	1 073					STC	VAK4			24790	
0	3	1	340	5	0	14	010					CIC	VAK4			24800	
0	3	1	341	5	0	14	060					CIC	VAK4			24810	
0	3	1	342	17	0	14	324		200000004			CLA	=02000000004			24820	
0	3	1	343	5	0	14	224					CIC	VAK4			24830	
0	3	1	344	5	0	14	154					CIC	VAK4			24840	
0	3	1	345	13	0	14	325		200400000			FNZ	=02040000000			24850	
0	3	1	346	4	0	14	1 361					CIC	L15PIR			24860	
0	3	1	347	17	0	14	174					CLA	L11P5			24870	
0	3	1	350	13	0	14	1 073					STC	VAK4			24880	
0	3	1	351	5	0	14	014					CIC	VAK4			24890	
0	3	1	352	5	0	14	054					CIC	VAK4			24900	
0	3	1	353	17	0	14	326		100000010			CLA	=01000000010			24910	
0	3	1	354	5	0	14	224					CIC	VAK4			24920	
0	3	1	355	5	0	14	154					CIC	VAK4			24930	
0	3	1	356	13	0	14	327		101000000			FNZ	=01010000000			24940	
0	3	1	357	4	0	14	1 361					CIC	L15PIR			24950	
0	3	1	360	00	0	14	330		140001040			FNZ	L11P6			24960	
0	3	1	361	13	0	14	1 377					STC	VAK4			24970	
0	3	1	362	13	0	14	1 076					STC	VAK4			24980	
0	3	1	363	17	0	14	1 073					STC	VAK4			24990	
0	3	1	364	13	0	14	1 070					STC	VAK4			25000	
0	3	1	365	17	0	14	1 377					STC	VAK4			25010	
0	3	1	366	13	0	14	1 071					STC	VAK4			25020	
0	3	1	367	0	0	14	1 023					HOP	VAK4			25030	
0	3	1	370	17	0	14	1 076					CLA	VAK4			25040	
0	3	1	371	0	0	14	1 026					HOP	VAK4			25050	
0	3	1	371	0	0	14	1 026					HOP	VAK4			25060	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 51)

IM	LS	LUC	UP	OM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO.
0	4	0	2				0 14 167			L11P6	URG	*4**2**14,		25080	
0	4	0	2				17 0 14 175			L11P6	CLA	L11P6		25090	
0	4	0	3				13 0 14 1 073				STP	VAR4		25100	
0	4	0	4				5 0 14 020				CIU	070	RST3	25110	
0	4	0	5				2 0 14 050				CIU	050	RST9	25120	
0	4	0	6				17 0 14 331		040000020		CLA	=0040000020	A1,A22	25130	
0	4	0	7				5 0 14 224				CIU	224		25140	
0	4	0	10				5 0 14 154				CIU	154		25150	
0	4	0	11				13 0 14 332		042000000		XDM	=0042000000		25160	
0	4	0	12				4 0 14 137				TNZ	LPR		25170	
0	4	0	13				17 0 14 176			L11P7	CLA	L11P7		25180	
0	4	0	14				13 0 14 1 073				STL	VAR4		25190	
0	4	0	15				5 0 14 024				CIU	024	RST 4	25200	
0	4	0	16				5 0 14 044				CIU	044	RST 8	25210	
0	4	0	17				17 0 14 333		070000040		CLA	=0020000040	A4, A71	25220	
0	4	0	20				5 0 14 224				CIU	224		25230	
0	4	0	21				5 0 14 154				CIU	154		25240	
0	4	0	22				15 0 14 334		024000000		TNZ	=0024000000		25250	
0	4	0	23				4 0 14 137				LPR	LPR		25260	
0	4	0	24				17 0 14 177			L11P8	CLA	L11P8		25270	
0	4	0	25				13 0 14 1 073				STL	VAR4		25280	
0	4	0	26				5 0 14 030				CIU	030	RST 5	25290	
0	4	0	27				2 0 14 040				CIU	040	RST 7	25300	
0	4	0	30				17 0 14 335		010100000		CLA	=0010100000	A7, A11	25310	
0	4	0	31				5 0 14 224				CIU	224		25320	
0	4	0	32				5 0 14 154				CIU	154		25330	
0	4	0	33				15 0 14 335		010100000		XDR	=0010100000		25340	
0	4	0	34				4 0 14 137				TNZ	LPR		25350	
0	4	0	35				17 0 14 200			L11P9	CLA	L11P9		25360	
0	4	0	36				13 0 14 1 073				STL	VAR4		25370	
0	4	0	37				5 0 14 034				CIU	034	RST 6	25380	
0	4	0	40				5 0 14 064				CIU	064	RST 12	25390	
0	4	0	41				17 0 14 336		004040000		CLA	=0004040000	A6, A17	25400	
0	4	0	42				5 0 14 224				CIU	224		25410	
0	4	0	43				5 0 14 154				CIU	154		25420	
0	4	0	44				15 0 14 336		004040000		XDR	=0004040000		25430	
0	4	0	45				4 0 14 137				TNZ	LPR		25440	
0	4	0	46				10 0 14 053				TRA	L11P10		25450	
0	4	0	53				17 0 14 170				ORG	*4**53**14,		25460	
0	4	0	54				13 0 14 1 073			L11P10	CLA	L11P10		25470	
0	4	0	55				5 0 14 040				STP	VAR4		25480	
0	4	0	56				5 0 14 070				CIU	070	RST 7	25490	
0	4	0	57				17 0 14 337		002020100		CLA	=0002020100	RST 13	25500	
0	4	0	60				5 0 14 224				CIU	224	A7, A13, A20	25520	
0	4	0	61				5 0 14 154				CIU	154		25530	
0	4	0	62				15 0 14 340		012020000		XDR	=0012020000		25540	
0	4	0	63				4 0 14 137				TNZ	LPR		25550	
0	4	0	64				17 0 14 202			L11P11	CLA	L11P11		25560	
0	4	0	65				13 0 14 1 073				STP	VAR4		25570	
0	4	0	66				5 0 14 044				CIU	044	RST 8	25580	
0	4	0	67				5 0 14 074				CIU	074	RST 14	25590	
0	4	0	70				5 0 14 034				CIU	034	RST 6	25600	
0	4	0	71				17 0 14 341		001010200		CLA	=0001010200	A8, A14, A19	25610	
0	4	0	72				5 0 14 224				CIU	224		25620	
0	4	0	73				5 0 14 154				CIU	154		25630	
0	4	0	74				15 0 14 342		021010000		XDR	=0021010000		25640	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 52)

IM	IS	S	LIC	UP	DM	DS	ADR	PCT	VAL	LMS	OPC	VARIABLE	COMMENT	REL
0	4	0	75	4	0	14	137			L11P12	FNZ	LPR		25659
0	4	0	76	17	0	14	203			L11P12	CLA	H11P12		25660
0	4	0	77	13	0	14	073			VAR4	STC	VAR4		25676
0	4	0	100	5	0	14	030			C1U	C1U	030	RST 5	25680
0	4	0	101	5	0	14	050			C1U	C1U	050	RST 9	25690
0	4	0	102	5	0	14	100			C1U	C1U	100	RST 15	25700
0	4	0	103	17	0	14	343	000404400		CLA	CLA	=000404400	A9, A15, A18	25710
0	4	0	104	5	0	14	224			C1C	C1C	224		25720
0	4	0	105	5	0	14	154			C1C	C1C	154		25730
0	4	0	106	15	0	14	344	440400000		XOR	XOR	=044040000		25740
0	4	0	107	4	0	14	137			FNZ	FNZ	LPR		25750
0	4	0	110	17	0	14	204			L11P13	CLA	H11P13		25760
0	4	0	111	13	0	14	073			STC	STC	VAR4		25770
0	4	0	112	5	0	14	010			C1U	C1U	010	RST 1	25780
0	4	0	113	5	0	14	024			C1U	C1U	024	RST 4	25790
0	4	0	114	5	0	14	054			C1C	C1C	C54	RST 10	25800
0	4	0	115	17	0	14	345	000701000		CLA	CLA	=0300001000	A10, A17	25810
0	4	0	116	5	0	14	274			C1C	C1C	224		25820
0	4	0	117	5	0	14	154			C1U	C1U	154		25830
0	4	0	120	17	0	14	346	100200000		XOR	XOR	=0100200000		25840
0	4	0	121	4	0	14	137			FNZ	FNZ	LPR		25850
0	4	0	122	17	0	14	205			L11P14	CLA	H11P14		25860
0	4	0	123	13	0	14	073			STC	STC	VAR4		25870
0	4	0	124	5	0	14	020			L11P14	C1U	G20		25880
0	4	0	125	5	0	14	060			C1C	C1C	063	RST 3	25890
0	4	0	126	17	0	14	347	000002000		CLA	CLA	=0000002000	RST 11	25900
0	4	0	127	5	0	14	224			C1U	C1U	224	A16	25910
0	4	0	130	5	0	14	154			C1U	C1U	154		25920
0	4	0	131	15	0	14	223	200000000		XOR	XOR	=0200000000		25930
0	4	0	132	4	0	14	137			FNZ	FNZ	LPR		25940
0	4	0	133	17	0	14	206			L11P15	CLA	H11P15		25950
0	4	0	134	13	0	14	073			STC	STC	VAR4		25960
0	4	0	135	5	0	14	014			C1C	C1C	014	RST 2	25970
0	4	0	136	10	0	14	141			TRA	TRA	L11P18		25980
0	4	0	137	13	0	14	137			STC	STC	777		25990
0	4	0	140	00	0	14	350	140171230		LPR	TRA*	LPR4		26000
0	4	0	141	17	0	14	207			CL	CL	CL	CHECK PIO + A1 THRU A9 INTERFACE LINES	26020
0	4	0	142	13	0	14	073			L11P18	CLA	H11P18		26030
0	4	0	143	12	0	14	000			STU	STU	VAR4		26040
0	4	0	144	5	0	14	154			PIU	PIU	000		26050
0	4	0	145	4	0	14	305			C1U	C1U	154		26060
0	4	0	146	17	0	14	210			FNZ	FNZ	L11P26		26070
0	4	0	147	13	0	14	073			L11P19	CLA	H11P19		26080
0	4	0	150	12	0	14	001			STC	STC	VAR4		26090
0	4	0	151	5	0	14	154			PIU	PIU	001	SET INT 1	26100
0	4	0	152	15	0	14	221	400000000		C1C	C1C	154		26110
0	4	0	153	4	0	14	305			XOR	XOR	=0400000000		26120
0	4	0	154	17	0	14	211			FNZ	FNZ	L11P28		26130
0	4	0	155	13	0	14	073			L11P20	CLA	H11P20		26140
0	4	0	156	5	0	14	010			STU	STU	VAR4		26150
0	4	0	157	12	0	14	002			C1U	C1U	010	RST 1	26160
0	4	0	160	5	0	14	154			PIU	PIU	002	SET 2	26170
0	4	0	161	15	0	14	223	200000000		C1U	C1U	154		26180
0	4	0	162	4	0	14	305			XOR	XOR	=0200000000		26190
0	4	0	163	17	0	14	212			L11P21	CLA	H11P21		26200
0	4	0	163	17	0	14	212			CL	CL	CL		26210

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 53)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SLC	NO
0	4	0	164	13	0	14	1	073				STC	VAR4		26221	
0	4	0	165	3	0	14	014					CIC	U14	RST 2	26230	
0	4	0	166	12	0	14	004					PIC	004	S.T 3	26234	
0	4	0	167	5	0	14	154					CIC	154		26251	
0	4	0	176	5	0	14	167		100000000			XOR	=010000000		26266	
0	4	0	171	4	0	14	305					TNZ	L11P28		26277	
0	4	0	172	17	0	14	213				L11P22	STU	L11P22		26278	
0	4	0	173	13	0	14	1	073				VAR4	VAR4	RST 3	26279	
0	4	0	174	5	0	14	020					CIC	020	SET 4	26306	
0	4	0	175	17	0	14	010					PIU	010		26310	
0	4	0	176	3	0	14	154					CIC	154		26326	
0	4	0	177	15	0	14	222		040000000			XOR	=004000000		26330	
0	4	0	200	4	0	14	305					TNZ	L11P24		26346	
0	4	0	201	17	0	14	214				L11P23	CLA	L11P23		26350	
0	4	0	202	13	0	14	1	073				STU	VAR4		26360	
0	4	0	203	5	0	14	074					CIC	074	RST 4	26376	
0	4	0	204	17	0	14	020					PIU	020	SET 5	26380	
0	4	0	205	5	0	14	154					CIC	154		26390	
0	4	0	206	15	0	14	224		020000000			XOR	=0C2000000		26400	
0	4	0	207	4	0	14	305					TNZ	L11P28		26410	
0	4	0	210	17	0	14	215				L11P24	CLA	L11P24		26420	
0	4	0	211	13	0	14	1	073				STC	VAR4		26430	
0	4	0	212	5	0	14	030					CIC	030		26440	
0	4	0	213	12	0	14	040					PIU	040	RST 5	26450	
0	4	0	214	5	0	14	154					CIC	154	SET 6	26460	
0	4	0	215	15	0	14	225		010000000			XOR	=001000000		26470	
0	4	0	216	4	0	14	305					TNZ	L11P28		26480	
0	4	0	217	17	0	14	216				L11P25	CLA	L11P25		26490	
0	4	0	220	13	0	14	1	073				STC	VAR4		26500	
0	4	0	221	5	0	14	034					CIC	034	RST 6	26510	
0	4	0	222	12	0	14	100					PIU	100	SET 7	26520	
0	4	0	223	15	0	14	154					CIC	154		26530	
0	4	0	224	15	0	14	226		004000000			XOR	=000400000		26540	
0	4	0	225	4	0	14	305					TNZ	L11P28		26550	
0	4	0	226	17	0	14	217				L11P26	CLA	L11P26		26560	
0	4	0	227	13	0	14	1	073				STC	VAR4		26570	
0	4	0	230	5	0	14	040					CIC	040	RST 4	26580	
0	4	0	231	12	0	14	200					PIU	200	SET 8	26590	
0	4	0	232	5	0	14	154					CIC	154		26600	
0	4	0	233	15	0	14	227		002000000			XOR	=00C200000		26610	
0	4	0	234	4	0	14	305					TNZ	L11P28		26620	
0	4	0	235	17	0	14	220				L11P27	CLA	L11P27		26630	
0	4	0	236	13	0	14	1	073				STC	VAR4		26640	
0	4	0	237	5	0	14	044					CIC	044	RST 8	26650	
0	4	0	240	12	0	14	1	000				PIU	400	SET 9	26660	
0	4	0	241	5	0	14	154					CIC	154		26670	
0	4	0	242	15	0	14	230		001000000			XOR	=000100000		26680	
0	4	0	243	4	0	14	305					TNZ	L11P28		26690	
0	4	0	244	5	0	14	050					CIC	050	RST 9	26700	
0	4	0	245	13	0	14	1	376			* CHECK SERIAL DATA LINES AT3 + CIU DATA	STU	776	26710		
0	4	0	246	17	0	14	1	020			L11P29	CLA	ZER0	26720		
0	4	0	247	13	0	14	1	073				STU	VAR4	26730		
0	4	0	250	17	0	14	351		252525252			CLA	=0252525252	26740		
0	4	0	251	5	0	14	234					CIC	234	26750		
0	4	0	252	5	0	14	001					CIC	001	26760		
0	4	0	253	15	0	14	352		525252524			CIC	001	26770		
												XOR	=0525252524	26780		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 54)

IM	IS	S	L	LOC	UP	DM	DS	9	ADR	LOC	VAL	LMS	CPC	VARIABLE	COMMENT	SEC	LOC
0	4	0	254		4	0	14	307						L11P33		26770	
0	4	0	255		13	0	14	376						776		26408	
0	4	0	256		17	0	14	352		525252524		L11P30	STC	CL	-0525252524	26410	
0	4	0	257		9	0	14	234						CIC	734	26426	
0	4	0	260		5	0	14	001						CIC	001	26430	
0	4	0	261		15	0	14	353		252525250				XDR	ED252525250	26440	
0	4	0	262		4	0	14	307						747		26450	
0	4	0	263		13	0	14	376						CHECK	PERS & PED DATA LINES	26460	
0	4	0	264		17	0	14	351		252525252		L11P31	STC	776		26470	
0	4	0	265		13	0	14	003						403		26480	
0	4	0	266		17	0	14	020						747		26490	
0	4	0	267		5	0	14	240						230		26500	
0	4	0	270		12	0	14	003						603		26520	
0	4	0	271		19	0	14	352		525252524				XDR	ED2525252524	26530	
0	4	0	272		4	0	14	307						L11P33		26540	
0	4	0	273		13	0	14	376				L11P32	STC	776		26550	
0	4	0	274		17	0	14	352		525252524				403		26560	
0	4	0	275		13	0	14	003						747		26570	
0	4	0	276		17	0	14	020						230		26580	
0	4	0	277		9	0	14	230						CIC	734	26590	
0	4	0	306		12	0	14	003						PIC	403	27000	
0	4	0	307		19	0	14	353		252525250				603		27010	
0	4	0	308		4	0	14	307						L11P33		27020	
0	4	0	309		13	0	14	023						403		27030	
0	4	0	304		9	0	14	354		150009460				TRA*		27040	
0	4	0	305		13	0	14	377				L11P29	STC	777		27050	
0	4	0	306		17	0	14	355		140167676				LPA*		27060	
0	4	0	307		13	0	14	377				L11P33	STC	777		27070	
0	4	0	310		13	0	14	076						TEMP		27080	
0	4	0	311		17	0	14	377						747		27090	
0	4	0	312		13	0	14	071						VA42		27100	
0	4	0	313		17	0	14	376						776		27110	
0	4	0	314		13	0	14	070						VAP1		27120	
0	4	0	315		9	0	14	023						POP3		27130	
0	4	0	316		17	0	14	076						TEMP		27140	
0	4	0	317		9	0	14	026						POP1		27150	
0	4	0	170		0	14	170			140144630		H11P1	HPC	L11P1		27170	
0	4	0	171		0	14	171			140151630		H11P2	HPC	L11P2		27180	
0	4	0	172		0	14	172			140153630		H11P3	HPC	L11P3		27190	
0	4	0	173		0	14	173			140157230		H11P4	HPC	L11P4		27200	
0	4	0	174		0	14	174			140161630		H11P5	HPC	L11P5		27210	
0	4	0	175		0	14	175			140001040		H11P6	HPC	L11P6		27220	
0	4	0	176		0	14	176			140005440		H11P7	HPC	L11P7		27230	
0	4	0	177		0	14	177			140012040		H11P8	HPC	L11P8		27240	
0	4	0	200		0	14	200			140016440		H11P9	HPC	L11P9		27250	
0	4	0	201		0	14	201			140025440		H11P10	HPC	L11P10		27260	
0	4	0	202		0	14	202			140032040		H11P11	HPC	L11P11		27270	
0	4	0	203		0	14	203			140037040		H11P12	HPC	L11P12		27280	
0	4	0	204		0	14	204			140044040		H11P13	HPC	L11P13		27290	
0	4	0	205		0	14	205			140051040		H11P14	HPC	L11P14		27300	
0	4	0	206		0	14	206			140055440		H11P15	HPC	L11P15		27310	
0	4	0	207		0	14	207			140060440		H11P16	HPC	L11P16		27320	
0	4	0	210		0	14	210			140063040		H11P17	HPC	L11P17		27330	
0	4	0	211		0	14	211			140066040		H11P20	HPC	L11P20		27340	
0	4	0	212		0	14	212			140071440		H11P21	HPC	L11P21		27350	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 55)

1M	IS	S	LOC	UP	UM	DS	Q	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
				0	14			213	140075040		H11P22	HPC	L11P22		27360	
				0	14			214	140100440		H11P23	HPC	L11P23		27370	
				0	14			215	140100440		H11P24	HPC	L11P24		27380	
				0	14			216	140107440		H11P25	HPC	L11P25		27400	
				0	14			217	140113040		H11P26	HPC	L11P26		27410	
				0	14			220	140116440		H11P27	HPC	L11P27			

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 56)

IN	IS	LOC	OP	RM	MS	9	ADR	QCT	VAL	LMS	OPC	VARIABLE	COMMENT	SIC
0	0	1	U	15	0		0	150023060	H12P3		ORG	TEST PIC INTERRUPTS		27430
0	0	1	C	15	0		0	150032000	H12P3		HPC	66110155C		27440
0	0	1	C	15	1		1	150041060	H12P5		HPC	L12P5		27450
0	0	2	C	15	2		2	150050060	H13P1		HPC	L13P1		27460
0	0	3	C	15	3		3	150050060	H13P3		HPC	L13P3		27470
0	0	4	C	15	4		4	150050060	H13P5		HPC	L13P5		27480
0	0	5	C	15	5		5	150066060	H14P1		HPC	L14P1		27490
0	0	6	C	15	6		6	150075060	H14P3		HPC	L14P3		27500
0	0	7	C	15	7		7	150104060	H14P5		HPC	L14P5		27510
0	0	10	C	15	10		10	150113060	H15P1		HPC	L15P1		27520
0	0	11	C	15	11		11	150122060	H15P3		HPC	L15P3		27530
0	0	12	C	15	12		12	150131060	H15P5		HPC	L15P5		27540
0	0	13	C	15	13		13	150140060	H16P1		HPC	L16P1		27550
0	0	14	C	15	14		14	150147060	H16P3		HPC	L16P3		27560
0	0	15	C	15	15		15	150156060	H16P5		HPC	L16P5		27570
0	0	16	C	15	16		16	150165060	H17P1		HPC	L17P1		27580
0	0	17	C	15	17		17	150000460	H12P1		HPC	L12P1		27590
0	0	20	C	15	20		20	150173060	H12P2		HPC	L12P2		27600
0	0	21	C	15	21		21	150174060	H12P4		HPC	L12P4		27610
0	0	22	C	15	22		22	150000260	H12P6		HPC	L12P6		27620
0	0	23	C	15	23		23	150004260	H13P2		HPC	L13P2		27630
0	0	24	C	15	24		24	150005260	H13P4		HPC	L13P4		27640
0	0	25	C	15	25		25	150006260	H13P6		HPC	L13P6		27650
0	0	26	C	15	26		26	150007260	H14P2		HPC	L14P2		27660
0	0	27	C	15	27		27	150010260	H14P4		HPC	L14P4		27670
0	0	30	C	15	30		30	150011260	H14P6		HPC	L14P6		27680
0	0	31	C	15	31		31	150012260	H15P2		HPC	L15P2		27690
0	0	32	C	15	32		32	150013260	H15P4		HPC	L15P4		27700
0	0	33	C	15	33		33	150014260	H15P6		HPC	L15P6		27710
0	0	34	C	15	34		34	150015260	H16P2		HPC	L16P2		27720
0	0	35	C	15	35		35	150016260	H16P4		HPC	L16P4		27730
0	0	36	C	15	36		36	150017260	H16P6		HPC	L16P6		27740
0	0	1	C	15	017		017		L12P1		CLA	H12P1		27750
0	0	2	C	15	1		017				CLA	VAK4		27770
0	0	3	C	15	020		020				CLA	H12P2		27780
0	0	4	C	15	1		000				STU	40C		27790
0	0	5	C	15	071		071				CLA	H12P4		27800
0	0	6	C	15	1		001				STU	401		27810
0	0	7	C	15	022		022				CLA	H12P6		27820
0	0	10	C	15	1		002				STU	402		27830
0	0	11	C	15	023		023				CLA	H13P2		27840
0	0	12	C	15	1		003				STU	403		27850
0	0	13	C	15	024		024				CLA	H13P4		27860
0	0	14	C	15	1		004				STU	404		27870
0	0	15	C	15	025		025				CLA	H13P6		27880
0	0	16	C	15	1		005				STU	405		27890
0	0	17	C	15	026		026				CLA	H14P2		27900
0	0	20	C	15	1		006				STU	406		27910
0	0	21	C	15	027		027				CLA	H14P4		27920
0	0	22	C	15	1		007				STU	407		27930
0	0	23	C	15	030		030				CLA	H14P6		27940
0	0	24	C	15	1		010				STU	410		27950
0	0	25	C	15	031		031				CLA	H15P2		27960
0	0	26	C	15	1		011				STU	411		27970
0	0	27	C	15	032		032				CLA	H15P4		27980

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 57)

IM	IS	S	LIC	UP	DM	DS	9	ADR	OCT	VAL	LHS	RPC	VARIABLE	COMMENT	SFC	NC
0	6	0	30	13	0	15	1	012				STC	412		28000	
0	6	0	31	17	0	15	0	033				CLA	H15P6		28010	
0	6	0	32	13	0	15	1	013				STO	413		28020	
0	6	0	33	17	0	15	0	034				CLA	H16P2		28030	
0	6	0	34	13	0	15	1	014				STC	414		28040	
0	6	0	35	17	0	15	0	035				CLA	F16P4		28050	
0	6	0	36	13	0	15	1	015				STU	415		28060	
0	6	0	37	17	0	15	0	036				CLA	H16P6		28070	
0	6	0	40	13	0	15	1	016				STC	416		28080	
0	6	0	41	17	0	15	0	037	777777776			CLA	=077777776	SET ALL INT LATCHES	28100	
0	6	0	42	5	0	15	224					CIC	224	CAL POINT NR 7	28110	
0	6	0	43	5	0	15	110					CIC	110	RST MAIN PTC INT LATCH	28120	
0	6	0	44	17	0	15	040		000000002			CLA	=000000002	CAL POINT NR 8	28130	
0	6	0	45	5	0	15	004					CIC	004	REMOVE INH ON INT 1	28140	
0	6	0	46	13	0	15	1	377				STC	777	SHOULD FORCE HOP 400 TO L12P2	28150	
0	6	0	47	13	0	15	1	076				STU	TEMP	SAVE PREVIOUS LOCN+1	28160	
0	6	0	50	17	0	15	1	377				CLA	777		28180	
0	6	0	51	13	0	15	1	074				STU	VAK5		28190	
0	6	0	52	17	0	15	1	076				CLA	TEMP		28200	
0	6	0	53	15	0	15	1	054	200000000			XOR	=020000000		28210	
0	6	0	54	4	0	15	1	040				FNZ	L15P15		28220	
0	6	0	55	17	0	15	1	073				CLA	H12P3		28230	
0	6	0	56	13	0	15	1	037				STC	VAK4		28240	
0	6	0	57	17	0	15	0	037	777777776			CLA	=077777776		28250	
0	6	0	60	5	0	15	000					CIC	000	SET INT INHIBIT	28260	
0	6	0	61	5	0	15	110					CIC	110	RST MAIN INT LATCH	28270	
0	6	0	62	17	0	15	277		000000004			CLA	=000000004	REMOVE INH ON INT 2	28280	
0	6	0	63	5	0	15	004					CIC	004	REMOVE INH ON INT 2	28290	
0	6	0	64	13	0	15	1	377				STU	777	SHOULD FORCE HOP 401 TO L12P4	28300	
0	6	0	65	13	0	15	1	076				STU	TEMP		28310	
0	6	0	66	17	0	15	1	377				CLA	777		28320	
0	6	0	67	13	0	15	1	074				STC	VAK5		28330	
0	6	0	70	17	0	15	1	076				CLA	TEMP		28340	
0	6	0	71	15	0	15	300		100000000			XOR	=010000000		28350	
0	6	0	72	4	0	15	1	040				FNZ	L15P15		28360	
0	6	0	73	17	0	15	0	001				CLA	F12P5		28370	
0	6	0	74	13	0	15	1	073				STC	VAK4		28380	
0	6	0	75	17	0	15	0	037	777777776			CLA	=077777776		28390	
0	6	0	76	5	0	15	000					CIC	000	SET INT INHIBIT	28400	
0	6	0	77	5	0	15	110					CIC	110	RST MAIN INT LATCH	28410	
0	6	0	100	17	0	15	301		000000010			CLA	=000000010	REMOVE INH ON INT 3	28420	
0	6	0	101	5	0	15	004					CIC	004	REMOVE INH ON INT 3	28430	
0	6	0	102	13	0	15	1	377				STC	777	SHOULD FORCE HOP 402 TO L12P6	28440	
0	6	0	103	13	0	15	1	076				STU	TEMP		28450	
0	6	0	104	17	0	15	1	377				CLA	777		28460	
0	6	0	105	13	0	15	1	074				STC	VAK5		28470	
0	6	0	106	17	0	15	1	076				CLA	TEMP		28480	
0	6	0	110	4	0	15	302		040000000			XOR	=004000000		28490	
0	6	0	111	17	0	15	1	040				FNZ	L15P15		28500	
0	6	0	112	17	0	15	0	002				CLA	H13P1		28510	
0	6	0	113	13	0	15	1	073	777777776			STU	VAK4		28520	
0	6	0	113	17	0	15	0	037				CLA	=077777776		28530	
															28540	
															28550	
															28560	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 58)

IM	IS	S	LOC	UP	UM	DS	9	ADR	OCT	VAL	LMS	DPC	VARIABLE	COMMENT	SEC	NO
0	6	0	114	5	0	15	000					CIC	000	SET INT INHIBIT	28570	
0	6	0	115	5	0	15	110					CIC	110	RST MAIN INT LATCH	28580	
0	6	0	116	17	0	15	503		000000020			CLA	=000000020	REMOVE INH ON INT 4	28590	
0	6	0	117	5	0	15	004					CIC	004		28600	
0	6	0	120	13	0	15	1 377				*	STC	SHOULD FORCE HOP 403 TO L13P2		28610	
0	6	0	121	13	0	15	1 076				L13P3	STU	TEMP		28620	
0	6	0	122	17	0	15	1 377					CLA	TEMP		28630	
0	6	0	123	13	0	15	1 076					STC	VAR5		28640	
0	6	0	124	17	0	15	1 076					CLA	VAR5		28650	
0	6	0	125	15	0	15	304		020000000			XDR	=0020000000		28660	
0	6	0	126	4	0	15	1 040					TNZ	L15P15		28670	
0	6	0	127	17	0	15	003					CLA	H13P3		28680	
0	6	0	131	17	0	15	1 073		777777776			STC	VAR4		28700	
0	6	0	132	5	0	15	000					CLA	=077777776		28710	
0	6	0	133	5	0	15	110					CIC	000	SET INT INHIBIT	28720	
0	6	0	134	17	0	15	305		000000040			CLA	110	RST MAIN INT LATCH	28730	
0	6	0	135	5	0	15	004					CIC	=000000040	REMOVE INH ON INT 5	28740	
0	6	0	136	13	0	15	1 377				*	STC	SHOULD FORCE HOP 404 TO L13P4		28750	
0	6	0	137	13	0	15	1 076				L13P5	STU	TEMP		28760	
0	6	0	140	17	0	15	1 377					CLA	TEMP		28780	
0	6	0	141	13	0	15	1 074					STC	VAR5		28790	
0	6	0	142	17	0	15	1 076					CLA	VAR5		28800	
0	6	0	143	15	0	15	306		010000000			CLA	TEMP		28810	
0	6	0	144	4	0	15	1 040					XDR	=0010000000		28820	
0	6	0	145	17	0	15	004					TNZ	L15P15		28830	
0	6	0	146	13	0	15	1 073					CLA	H13P5		28840	
0	6	0	147	17	0	15	037		777777776			STC	VAR4		28850	
0	6	0	150	5	0	15	000					CLA	=077777776		28860	
0	6	0	151	5	0	15	110					CIC	000	SET INT INHIBIT	28870	
0	6	0	152	17	0	15	307		000000100			CLA	110	RST MAIN INT LATCH	28880	
0	6	0	153	5	0	15	004					CLA	=000000100	REMOVE INH ON INT 6	28890	
0	6	0	154	13	0	15	1 377				*	STC	SHOULD FORCE HOP 405 TO L13P6		28900	
0	6	0	155	13	0	15	1 076				L14P1	STU	TEMP		28910	
0	6	0	156	17	0	15	1 377					CLA	TEMP		28920	
0	6	0	157	13	0	15	1 074					CLA	TEMP		28930	
0	6	0	160	17	0	15	1 076					STC	VAR5		28940	
0	6	0	161	15	0	15	310		004000000			CLA	VAR5		28950	
0	6	0	162	4	0	15	1 040					CLA	TEMP		28960	
0	6	0	163	17	0	15	005					XDR	=0004000000		28970	
0	6	0	164	13	0	15	1 073					TNZ	L15P15		28980	
0	6	0	165	17	0	15	037		777777776			CLA	H14P1		28990	
0	6	0	166	5	0	15	000					STU	VAR4		29000	
0	6	0	167	5	0	15	110					CLA	=077777776		29010	
0	6	0	170	17	0	15	311		000000200			CIC	000	SET INT INHIBIT	29020	
0	6	0	171	5	0	15	004					CLA	110	RST MAIN INT LATCH	29030	
0	6	0	172	13	0	15	1 377				*	STC	SHOULD FORCE HOP 406 TO L14P2		29040	
0	6	0	173	13	0	15	1 076				L14P3	STU	TEMP		29050	
0	6	0	174	17	0	15	1 377					CLA	TEMP		29060	
0	6	0	175	13	0	15	1 074					CLA	TEMP		29070	
0	6	0	176	17	0	15	1 076					STU	VAR5		29080	
0	6	0	177	15	0	15	312		002000000			STU	VAR5		29090	
0	6	0	200	4	0	15	1 040					XDR	=0002000000		29100	
												TNZ	L15P15		29110	
															29120	
															29130	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 59)

IM	IS	S	LUC	UP	DM	DS	9	ADR	CCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	LC
0	6	0	201	17	0	15	1	006				CLA	H14P3		29140	
0	6	0	202	13	0	15	1	073				STU	VAR4		29150	
0	6	0	203	17	0	15	1	037	77777776			CLA	=07777776		29160	
0	6	0	204	5	0	15	000					CIC	000	SET INT INHIBIT	29170	
0	6	0	205	5	0	15	110					CIC	110	RST MAIN INT LATCH	29180	
0	6	0	206	17	0	15	313		000000400			CLA	=000000400	REMOVE INH ON INT H	29190	
0	6	0	207	5	0	15	004					CIC	004		29200	
0	6	0	210	13	0	15	1	377				STU	777	SHOULD FORCE HUP 412 TO L14P4	29210	
0	6	0	211	13	0	15	1	076				STU	TEMP		29220	
0	6	0	212	17	0	15	1	377				CLA	777		29230	
0	6	0	213	13	0	15	1	074				STU	VAR5		29240	
0	6	0	214	17	0	15	1	076				CLA	TEMP		29250	
0	6	0	215	15	0	15	314		001000000			XCR	=000100000		29260	
0	6	0	216	4	0	15	1	040				TNZ	L15P15		29270	
0	6	0	217	17	0	15	007					CLA	H14P5		29280	
0	6	0	220	13	0	15	1	073				STU	VAR4		29290	
0	6	0	221	17	0	15	037					CLA	=07777776		29300	
0	6	0	222	5	0	15	000		77777776			CIC	000		29310	
0	6	0	223	5	0	15	110					CIC	110	SET INT INHIBIT	29320	
0	6	0	224	17	0	15	315		000001000			CLA	=000001000	RST MAIN INT LATCH	29330	
0	6	0	225	5	0	15	004					CIC	004	REMOVE INH ON INT 9	29340	
0	6	0	226	13	0	15	1	377				STU	777		29350	
0	6	0	227	13	0	15	1	076				STU	TEMP	SHOULD FORCE HUP 410 TO L14P6	29360	
0	6	0	230	17	0	15	1	377				CLA	777		29370	
0	6	0	231	13	0	15	1	074				STU	VAR5		29380	
0	6	0	232	17	0	15	1	076				CLA	TEMP		29390	
0	6	0	233	15	0	15	316		000400000			CLA	=000400000		29400	
0	6	0	234	4	0	15	1	040				TNZ	L15P15		29410	
0	6	0	235	17	0	15	010					CLA	H15P1		29420	
0	6	0	236	13	0	15	1	073				STU	VAR4		29430	
0	6	0	237	17	0	15	037		77777776			CLA	=07777776		29440	
0	6	0	240	5	0	15	000					CIC	000	SET INT INHIBIT	29450	
0	6	0	241	5	0	15	110					CIC	110	RST MAIN INT LATCH	29460	
0	6	0	242	17	0	15	317		000002000			CLA	=000002000	REMOVE INH ON INT10	29470	
0	6	0	243	5	0	15	004					CIC	004		29480	
0	6	0	244	13	0	15	1	377				STU	777	SHOULD FORCE HUP 411 TO L15P2	29490	
0	6	0	245	13	0	15	1	076				STU	TEMP		29500	
0	6	0	246	17	0	15	1	377				CLA	777		29510	
0	6	0	247	13	0	15	1	074				STU	VAR5		29520	
0	6	0	250	17	0	15	1	076				CLA	TEMP		29530	
0	6	0	251	15	0	15	320		000200000			XCR	=000020000		29540	
0	6	0	252	4	0	15	1	040				TNZ	L15P15		29550	
0	6	0	253	17	0	15	011					CLA	H15P3		29560	
0	6	0	254	13	0	15	1	073				STU	VAR4		29570	
0	6	0	255	17	0	15	037		77777776			CLA	=07777776		29580	
0	6	0	256	5	0	15	000					CIC	000	SET INT INHIBIT	29590	
0	6	0	257	5	0	15	110					CIC	110	RST MAIN INT LATCH	29600	
0	6	0	260	17	0	15	321		000004000			CLA	=000004000	REMOVE INH ON INT 11	29610	
0	6	0	261	5	0	15	004					CIC	004		29620	
0	6	0	262	13	0	15	1	377				STU	777	SHOULD FORCE HUP 412 TO L15P4	29630	
0	6	0	263	13	0	15	1	076				STU	TEMP		29640	
0	6	0	264	17	0	15	1	377				CLA	777		29650	
0	6	0	265	13	0	15	1	074				STU	VAR5		29660	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 60)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC
0	6	0	266	17	0	15	1	076				CLA	TEMP		29710
0	6	0	267	15	0	15	322		000100000		XOR	=0000100000		29720	
0	6	0	270	4	0	15	1	040			TNZ	L15P15		29730	
0	6	0	271	17	0	15	012				CLA	H15P5		29740	
0	6	0	272	13	0	15	1	073			STG	VAR4		29750	
0	6	0	273	17	0	15	037		777777776		CLA	=0777777776		29760	
0	6	0	274	5	0	15	000				CIO	000	SET INT INHIBIT	29770	
0	6	0	275	5	0	15	110				CIO	110	RST MAIN INT LATCH	29780	
0	6	0	276	17	0	15	323		000010000		CLA	=0000010C00	REMOVE INH ON INT 12	29790	
0	6	0	277	5	0	15	004				CIO	004		29800	
0	6	0	300	13	0	15	1	377			* L16P1	STG	SHOULD FORCE HOP 413 TO L15P6	29810	
0	6	0	301	13	0	15	1	076			STG	TEMP		29820	
0	6	0	302	17	0	15	1	377			CLA	777		29830	
0	6	0	303	13	0	15	1	074			STG	VAR5		29840	
0	6	0	304	17	0	15	1	076			CLA	TEMP		29850	
0	6	0	305	15	0	15	324		000040000		XOR	=0000040000		29860	
0	6	0	306	4	0	15	1	040			TNZ	L15P15		29870	
0	6	0	307	17	0	15	013				CLA	H16P1		29880	
0	6	0	310	13	0	15	1	073			STG	VAR4		29890	
0	6	0	311	17	0	15	037		777777776		CLA	=0777777776		29900	
0	6	0	312	5	0	15	000				CIO	000	SET INT INHIBIT	29910	
0	6	0	313	5	0	15	110				CIO	110	RST MAIN INT LATCH	29930	
0	6	0	314	17	0	15	325		000020000		CLA	=0000020000	REMOVE INH ON INT 13	29940	
0	6	0	315	5	0	15	004				CIO	004		29950	
0	6	0	316	13	0	15	1	377			* L16P3	STG	SHOULD FORCE HOP 414 TO L16P2	29960	
0	6	0	317	13	0	15	1	076			STG	TEMP		29970	
0	6	0	320	17	0	15	1	377			CLA	777		29980	
0	6	0	321	13	0	15	1	074			STG	VAR5		29990	
0	6	0	322	17	0	15	1	076			CLA	TEMP		30000	
0	6	0	323	15	0	15	325		000020000		XOR	=0000020000		30010	
0	6	0	324	4	0	15	1	040			TNZ	L15P15		30020	
0	6	0	325	17	0	15	014				CLA	H16P3		30030	
0	6	0	326	13	0	15	1	073			STG	VAR4		30040	
0	6	0	327	17	0	15	037		777777776		CLA	=0777777776		30050	
0	6	0	330	5	0	15	000				CIO	000	SET INT INHIBIT	30070	
0	6	0	331	5	0	15	110				CIO	110	RST MAIN INT LATCH	30080	
0	6	0	332	17	0	15	324		000040000		CLA	=0000040000	REMOVE INH ON INT 14	30090	
0	6	0	333	5	0	15	004				CIO	004		30100	
0	6	0	334	13	0	15	1	377			* L16P5	STG	SHOULD FORCE HOP 415 TO L16P4	30110	
0	6	0	335	13	0	15	1	076			STG	TEMP		30120	
0	6	0	336	17	0	15	1	377			CLA	777		30130	
0	6	0	337	13	0	15	1	074			STG	VAR5		30140	
0	6	0	340	17	0	15	1	076			CLA	TEMP		30150	
0	6	0	341	15	0	15	323		000010000		XOR	=0000010000		30160	
0	6	0	342	4	0	15	1	040			TNZ	L15P15		30170	
0	6	0	343	17	0	15	015				CLA	H16P5		30180	
0	6	0	344	13	0	15	1	073			STG	VAR4		30190	
0	6	0	345	17	0	15	037		777777776		CLA	=0777777776		30200	
0	6	0	346	5	0	15	000				CIO	000	SET INT INHIBIT	30220	
0	6	0	347	5	0	15	110				CIO	110	RST MAIN INT LATCH	30230	
0	6	0	350	17	0	15	322		000100000		CLA	=0000100000	REMOVE INH ON INT 15	30240	
0	6	0	351	5	0	15	004				CIO	004		30250	
0	6	0	352	13	0	15	1	377			* L17P1	STG	SHOULD FORCE HOP 416 TO L16P6	30260	
															30270

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 61)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ. NO
0	6	0	353	13	0	15	1	076				STU	TEMP		30280
0	6	0	354	17	0	15	1	377				CLA	777		30290
0	6	0	355	13	0	15	1	074				STO	VARS		30300
0	6	0	356	17	0	15	1	076				CLA	TEMP		30310
0	6	0	357	15	0	15	1	321	000004000			XOR	=000004000		30320
0	6	0	360	4	0	15	1	040				TNZ	L15P1S		30330
0	6	0	361	17	0	15	0	37	777777776			CLA	=077777776		30340
0	6	0	362	5	0	15	0	00				C10	000		30350
0	6	0	363	5	0	15	1	10				TRA*	L10		30360
0	6	0	364	00	0	15	1	326	140066210			TRA	L9P3		30370
0	6	0	365	10	0	15	1	060				TRA	L20P1		30380
0	6	0	366	17	0	15	0	054	200000000		L12P2	CLA	=020000000		30390
0	6	0	367	10	0	15	0	46				TRA	L12P3		30400
0	6	0	370	17	0	15	3	00	100000000		L12P4	CLA	=010000000		30410
0	6	0	371	10	0	15	0	64				TRA	L12P5		30420
0	6	1	0	0	15	0	15	37				ORC	.6,1,0,15,		30430
0	6	1	0	13	0	15	1	377			L12P6	STO	777		30440
0	6	1	1	17	0	15	0	22				CLA	H12P6		30460
0	6	1	2	13	0	15	1	073				STO	VAR4		30470
0	6	1	3	17	0	15	1	377				CLA	777		30480
0	6	1	4	15	0	15	0	02				XOR	H13P1		30490
0	6	1	5	4	0	15	1	040				TNZ	L15P1S		30500
0	6	1	6	17	0	15	3	02	040000000			CLA	=040000000		30510
0	6	1	7	10	0	15	1	02				TRA	L13P1		30520
0	6	1	10	17	0	15	3	04	020000000		L13P2	CLA	=020000000		30530
0	6	1	11	10	0	15	1	20				TRA	L13P3		30540
0	6	1	12	17	0	15	3	06	010000000		L13P4	CLA	=010000000		30550
0	6	1	13	10	0	15	1	36				TRA	L13P5		30560
0	6	1	14	17	0	15	3	10	004000000		L13P6	CLA	=004000000		30570
0	6	1	15	10	0	15	1	54				TRA	L14P1		30580
0	6	1	16	17	0	15	3	12	002000000		L14P2	CLA	=002000000		30590
0	6	1	17	10	0	15	1	72				TRA	L14P3		30600
0	6	1	20	17	0	15	3	14	001000000		L14P4	CLA	=001000000		30610
0	6	1	21	10	0	15	2	10				TRA	L14P5		30620
0	6	1	22	17	0	15	3	16	000400000		L14P6	CLA	=000400000		30630
0	6	1	23	10	0	15	2	26				TRA	L15P1		30640
0	6	1	24	17	0	15	3	20	000200000		L15P2	CLA	=000200000		30650
0	6	1	25	10	0	15	2	44				TRA	L15P3		30660
0	6	1	26	17	0	15	3	22	000100000		L15P4	CLA	=000100000		30670
0	6	1	27	10	0	15	2	62				TRA	L15P5		30680
0	6	1	30	17	0	15	3	24	000040000		L15P6	CLA	=000040000		30690
0	6	1	31	10	0	15	3	00				TRA	L16P1		30700
0	6	1	32	17	0	15	3	25	000020000		L16P2	CLA	=000020000		30710
0	6	1	33	10	0	15	3	16				TRA	L16P3		30720

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 62)

IM	IS	S	LUC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NC
0	6	1	34	17	0	15	323		000010000		L16P4	CLA	=0000010000		30850	
0	6	1	35	10	0	15	334					TRA	L16P5	CAL POINT NR 22	30860	
0	6	1	36	17	0	15	321		000004000		L16P6	CLA	=0000004000		30870	
0	6	1	37	10	0	15	352					TRA	L17P1	CAL POINT NR 23	30880	
0	6	1	40	13	0	15	1 377				L15P1S	STU	777		30900	
0	6	1	41	13	0	15	1 076					STU	TEMP		30910	
0	6	1	42	17	0	15	1 377					CLA	777		30920	
0	6	1	43	13	0	15	1 071					STU	VAR2		30930	
0	6	1	44	17	0	15	0 17					CLA	H1ZP1		30940	
0	6	1	45	13	0	15	1 070					STU	VAR1		30950	
0	6	1	46	17	0	15	1 076					CLA	TEMP		30960	
0	6	1	47	0	0	15	1 026				HOP	H95P1		30970		
0	13	0	310	0	13	0	250								30980	
0	13	0	310	13	0	13	1 377								31000	
0	13	0	311	13	0	13	237				L17P2	STU	777		31010	
0	13	0	312	17	0	13	240		000002000			CLA	=0000002000		31020	
0	13	0	313	13	0	13	1 075								31030	
0	13	0	314	5	0	13	220					STC	INTIND	CAL POINT NR 24	31040	
0	13	0	315	13	0	13	241					CIO	220		31050	
0	13	0	316	6	0	13	242					STO	TEMP2	READ B SWITCHES	31060	
0	13	0	317	6	0	13	324		020000000			AND	=0020C00000	84	31070	
0	13	0	320	5	0	13	104					TNZ	L17P3		31080	
0	13	0	321	5	0	13	110				L17P3A	CIO	104		31090	
0	13	0	322	17	0	13	237					CLA	SAVE		31100	
0	13	0	323	0	0	13	1 377					HOP	777		31110	
0	13	0	324	17	0	13	353								31120	
0	13	0	325	6	0	13	046					CLA	K17P3B		31130	
0	13	0	326	13	0	13	243					STU	TEMP3		31140	
0	13	0	327	17	0	13	350					AND	L17P3B		31150	
0	13	0	330	6	0	13	047					CLA	KX8		31160	
0	13	0	331	15	0	13	243					XOR	TEMP3		31170	
0	13	0	332	13	0	13	350					STO	L17P3B		31180	
0	13	0	333	17	0	13	241					SHR	L		31190	
0	13	0	334	16	0	13	101								31200	
0	13	0	335	6	0	13	046					AND	KX7		31210	
0	13	0	336	13	0	13	243					TEMP3	TEMP3		31220	
0	13	0	337	17	0	13	351					CLA	L17P3C		31230	
0	13	0	340	6	0	13	047					AND	KX8		31240	
0	13	0	341	15	0	13	243					XOR	TEMP3		31250	
0	13	0	342	13	0	13	351					STU	L17P3C		31260	
0	13	0	343	17	0	13	241					CLA	TEMP2		31270	
0	13	0	344	6	0	13	244		000000076			AND	=0C00000076		31280	
0	13	0	345	16	0	13	020					SHL	5		31290	
0	13	0	346	7	0	13	350					ACU	L17P3B		31300	
0	13	0	347	13	0	13	350					STU	L17P3B		31310	
0	13	0	350	17	0	13	250				L17P3B	CLA	BIT		31320	
0	13	0	351	5	0	13	000				L17P3C	CIO	000		31330	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 63)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	13	0	352	10	0	13		320				TRA	L17P3A		31400	
0	13	0	353	17	0	13		250			K17P3B	CLA	RIT		31410	
									0		BIT	OCF	0		31420	
0	13	251			0	13		251	400000000			OCF	4		31430	
0	13	252			0	13		252	200000000			OCF	2		31440	
0	13	253			0	13		253	100000000			OCF	1		31450	
0	13	254			0	13		254	400000000			OCF	04		31460	
0	13	255			0	13		255	200000000			OCF	02		31470	
0	13	256			0	13		256	100000000			OCF	01		31480	
0	13	257			0	13		257	400000000			OCF	004		31490	
0	13	260			0	13		260	200000000			OCF	002		31500	
0	13	261			0	13		261	100000000			OCF	001		31510	
0	13	262			0	13		262	400000000			OCF	0004		31520	
0	13	263			0	13		263	200000000			OCF	0002		31530	
0	13	264			0	13		264	100000000			OCF	0001		31540	
0	13	265			0	13		265	400000000			OCF	00004		31550	
0	13	266			0	13		266	200000000			OCF	00002		31560	
0	13	267			0	13		267	100000000			OCF	00001		31570	
0	13	270			0	13		270	400000000			OCF	000004		31580	
0	13	271			0	13		271	200000000			OCF	000002		31590	
0	13	272			0	13		272	100000000			OCF	000001		31600	
0	13	273			0	13		273	400000000			OCF	0000004		31610	
0	13	274			0	13		274	200000000			OCF	0000002		31620	
0	13	275			0	13		275	100000000			OCF	0000001		31630	
0	13	276			0	13		276	400000000			OCF	00000004		31640	
0	13	277			0	13		277	200000000			OCF	00000002		31650	
0	13	300			0	13		300	100000000			OCF	00000001		31660	
0	13	301			0	13		301	400000000			OCF	000000004		31670	
0	13	302			0	13		302	200000000			OCF	000000002		31680	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 64)

IM	IS	S	LUC	UP	DP	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	6	1	60													31700
0	6	1	60	17	0	15	1	057			L20P1	DRG	BEGINNING OF ROUTINE FOUR		31710	
0	6	1	61	14	0	15	1	065			L20P2	DRG	CHECK TYPERWRITER LOGIC AND INTERFACE		31720	
0	6	1	62	4	0	15	1	064			L20P2	DRG	*6,1,60,15,		31730	
0	6	1	63	00	0	15	3	327			L29P1A	TNZ	L29P1A		31740	
0	6	1	64	00	0	15	3	330	130007000		L29P1A	TRA*	L29P1A		31750	
0	6	1	65	16	0	12	2	212	120016100		L29P1	TRA*	L29P1		31760	
0	6	1	66	17	0	12	1	131			L20P2	CLS	0,12		31770	
0	6	1	67	13	0	12	1	073			L20P2	CLS	VAR4		31780	
0	6	1	70	17	0	12	1	132			STC	STC	VAR4		31790	
0	6	1	71	13	0	12	1	070			CLA	CLA	H20P3		31800	
0	6	1	72	00	0	12	1	162			STC	STC	VAR1		31810	
0	6	1	73	17	0	12	1	033	070003100		L28P3	TRA*	L28P3		31820	
0	6	1	74	5	0	12	0	000			CLA	CLA	K77		31830	
0	6	1	75	17	0	12	1	020			CLA	CLA	OC0	RESTORE INSTRUCTIONS	31840	
0	6	1	76	5	0	12	1	130			CLA	CLA	ZEK0	INHIBIT ALL INT	31850	
0	6	1	77	13	0	12	1	101			CIC	CIC	L30	SET LOWER CASE	31860	
0	6	1	100	17	0	12	1	163			CIC	CIC	CTK	EQUAL 45 DECIMAL	31870	
0	6	1	101	13	0	12	1	100	000000132		CLA	CLA	=000000132		31880	
0	6	1	102	00	0	12	1	164	120000270		STC	STC	STUP		31890	
0	6	1	103	00	0	12	1	165	120002670		TRA*	TRA*	L20P2A		31900	
0	7	1	0	0	0	12	0	0			L20P3	TRK*	L20P3		31920	
0	7	1	0	13	0	12	1	376			L20P2A	STC	776	DELAY 87.6 MSEC.	31930	
0	7	1	1	17	0	12	1	166	000002040		STC	STC	=000002040		31940	
0	7	1	2	2	0	12	1	167	000000002		L20P2B	SUB	=000000002		31950	
0	7	1	3	4	0	12	1	002			L20P3	TNZ	L20P2B		31960	
0	7	1	4	0	0	12	1	376			HOP	HOP	776		31970	
0	7	1	5	17	0	12	1	170			CLA	CLA	=0000000004		31980	
0	7	1	6	5	0	12	2	210	000000004		CIC	CIC	Z10	SET DD 2	31990	
0	7	1	7	17	0	12	1	020			CLA	CLA	ZEK0	RESET D.U.2	32000	
0	7	1	10	5	0	12	2	210			CIC	CIC	Z10		32010	
0	7	1	11	00	0	12	1	171	140066210		TRA*	TRA*	L9P3	RESET INT REG	32020	
0	7	1	12	17	0	12	1	104			CLA	CLA	CHAR		32030	
0	7	1	13	5	0	12	1	120			L20P5	C10	L20	TYPE CHAR	32040	
0	7	1	14	13	0	12	1	074			STU	STU	VAR5	FOR ERROR INFO	32050	
0	7	1	15	17	0	12	1	133			CLA	CLA	H20P4		32060	
0	7	1	16	13	0	12	1	073			STU	STU	VAR4		32070	
0	7	1	17	5	0	12	1	154			C10	C10	154		32080	
0	7	1	20	15	0	12	0	011			L20P6	XOK	PATN		32090	
0	7	1	21	4	0	12	1	354			L20P6	TNZ	L28P6		32100	
0	7	1	22	17	0	12	1	134			L21P1	CLA	H21P1		32110	
0	7	1	23	13	0	12	1	073			STU	STU	VAR4		32120	
0	7	1	24	5	0	12	2	214			C10	C10	214		32130	
0	7	1	25	6	0	12	1	021			AND	AND	BB	CHECK READY LINE	32140	
0	7	1	26	4	0	12	1	030			TNZ	TNZ	L21P2		32150	
0	7	1	27	10	0	12	1	354			FRA	FRA	L28P6		32160	
0	7	1	30	17	0	12	1	135			CLA	CLA	H21P2		32170	
0	7	1	31	13	0	12	1	073			STU	STU	VAR4		32180	
0	7	1	32	17	0	12	1	170	000000004		CLA	CLA	=0000000004	SET + RESET DD 2	32190	
0	7	1	33	5	0	12	2	210			CIC	CIC	Z10		32200	
0	7	1	34	17	0	12	1	020			CLA	CLA	ZEK0		32210	
0	7	1	35	5	0	12	1	210			CIC	CIC	Z10		32220	
0	7	1	36	0	0	12	1	023			HOP	HOP	H9P3		32230	
0	7	1	37	5	0	12	1	154			C10	C10	154		32240	
0	7	1	40	4	0	12	1	354			TNZ	TNZ	L28P6		32250	
0	7	1	40	4	0	12	1	354			TNZ	TNZ	L28P6		32260	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 65)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	7	1	41	17	0	12	136				L21P3	CLA	H21P3		32270	
0	7	1	42	13	0	12	1073				STU	STU	VAR4		32280	
0	7	1	43	5	0	12	214				CIC	CIC	214		32290	
0	7	1	44	6	0	12	1021				AND	AND	RB	CHECK READY LINE	32300	
0	7	1	45	4	0	12	1354				TNZ	TNZ	L28P6		32310	
0	7	1	46	16	0	7	207				CDS	CDS	0+07		32320	
0	7	1	47	17	0	7	012				CLA	CLA	L20P4		32330	
0	7	1	50	13	0	7	036				ADC	ADC	K51	INCREMENT ADDRESS	32340	
0	7	1	51	13	0	7	012				STU	STU	L20P4		32350	
0	7	1	52	17	0	7	020				CLA	CLA	L20P6	XUR PATN + CTR	32360	
0	7	1	53	7	0	7	036				ADD	ADD	K51		32370	
0	7	1	54	13	0	7	020				CDS	CDS	0+12		32380	
0	7	1	55	16	0	12	212				CLA	CLA	CTR		32390	
0	7	1	56	17	0	12	101				ADD	ADD	K1		32400	
0	7	1	57	7	0	12	1032				STU	STU	CTR		32410	
0	7	1	60	13	0	12	101				STU	STU	CTR		32420	
0	7	1	61	2	0	12	100				SUB	SUB	STOP		32430	
0	7	1	62	4	0	12	1012				TNZ	TNZ	L20P4		32440	
0	7	1	63	17	0	12	100				CLA	CLA	STOP		32450	
0	7	1	64	2	0	12	163		000000132		SUB	SUB	=0000000132	IS STOP = 45	32460	
0	7	1	65	4	0	12	1067				TNZ	TNZ	L22P1	IF YES	32470	
0	7	1	66	10	0	12	116				TRA	TRA	L23P1		32480	
0	7	1	67	17	0	12	100				CLA	CLA	STUP		32490	
0	7	1	70	2	0	12	172		000000046		SUB	SUB	=0000000046	IS STOP = 19	32500	
0	7	1	71	4	0	12	1073				TNZ	TNZ	L22P2	IF YES	32510	
0	7	1	72	10	0	12	1152				TRA	TRA	L24P1		32520	
0	7	1	73	17	0	12	100				CLA	CLA	STOP	IS STOP = 8	32530	
0	7	1	74	2	0	12	173		000000020		SUB	SUB	=0000000020	IF YES	32540	
0	7	1	75	4	0	12	1077				TNZ	TNZ	L22P3	IF YES	32550	
0	7	1	76	10	0	12	1270				TRA	TRA	L26P2		32560	
0	7	1	77	17	0	12	100				CLA	CLA	STOP	IS STOP = 10	32570	
0	7	1	100	2	0	12	174		000000024		SUB	SUB	=0000000024	IF YES	32580	
0	7	1	101	4	0	12	1304				TNZ	TNZ	L27P1	RESET CTR	32590	
0	7	1	102	13	0	12	101				CLA	CLA	CTR	6	32600	
0	7	1	103	17	0	12	175		000000014		CLA	CLA	=0C00C00014		32610	
0	7	1	104	13	0	12	100				STU	STU	STOP		32620	
0	7	1	105	16	0	7	207				CDS	CDS	0+07		32630	
0	7	1	106	17	0	7	013				CLA	CLA	L20P5		32640	
0	7	1	107	6	0	7	040				AND	AND	KX1	REMOVE ADDRESS	32650	
0	7	1	110	15	0	7	041				XOR	XOR	KX2	= CIO 134	32660	
0	7	1	111	13	0	7	013				STU	STU	L20P5		32670	
0	7	1	112	16	0	12	212				CDS	CDS	0+12		32680	
0	7	1	113	17	0	12	137				CLA	CLA	H22P4		32690	
0	7	1	114	13	0	12	1073				STU	STU	VAR4	CARRIAGE CONTROL	32700	
0	7	1	115	10	0	12	1012				TRA	TRA	L20P4		32710	
0	7	1	116	17	0	12	140				CLA	CLA	H23P1		32720	
0	7	1	117	13	0	12	1073				STU	STU	VAR4		32730	
0	7	1	120	13	0	12	143				CLA	CLA	H23P5		32740	
0	7	1	121	13	0	12	1070				STU	STU	VAR1		32750	
0	7	1	122	17	0	12	161				CLA	CLA	C45	FIRST UPPER CASE CHAR	32760	
0	7	1	123	5	0	12	120				CIC	CIC	VAR5	INT REG	32770	
0	7	1	124	13	0	12	1074				STU	STU	VAR5		32780	
0	7	1	125	5	0	12	154				XOR	XOR	154		32790	
0	7	1	126	15	0	12	1176		400000000		XOR	XOR	=0400000000		32800	
0	7	1	127	4	0	12	1354				TNZ	TNZ	L28P6		32810	
0	7	1	130	17	0	12	141				CLA	CLA	H23P2		32820	
0	7	1	131	13	0	12	1073				STU	STU	VAR4		32830	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 66)

IM	IS	S	LDC	OP	UM	US	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	7	1	132	5	0	12		214				CIC	214	READY LINE	32840	
0	7	1	133	6	0	12		1 021				ANC	BB		32850	
0	7	1	134	4	0	12		1 136				TNZ	L23P3		32860	
0	7	1	135	10	0	12		1 354			L23P3	TRA	L28P6		32870	
0	7	1	136	17	0	12		1 42			CLA	H23P3		32880		
0	7	1	137	13	0	12		1 073			STU	VAR4		32890		
0	7	1	140	10	0	12		1 000			TRA	L20P2A	DELAY 87.6 MSEC.	32900		
0	7	1	141	5	0	12		1 254			CIC	L54		32910		
0	7	1	142	15	0	12		056			XOR	P45	1.5*6.9	32920		
0	7	1	143	4	0	12		1 354			TNZ	L28P6		32930		
0	7	1	144	13	0	12		1 101			CTR	VAR4	RESET CTR	32940		
0	7	1	145	17	0	12		1 172	000000046		CLA	=0000000046	19	32950		
0	7	1	146	13	0	12		1 100			STU	STU		32960		
0	7	1	147	17	0	12		1 132			CLA	H20P3		32970		
0	7	1	150	13	0	12		1 070			STU	VAR1		32980		
0	7	1	151	10	0	12		1 022			TRA	L21P1		32990		
0	7	1	152	17	0	12		1 44			CLA	H24P1		33000		
0	7	1	153	13	0	12		1 073			STD	VAR4		33010		
0	7	1	154	17	0	12		1 43			CLA	H23P5		33020		
0	7	1	155	13	0	12		1 070			STD	VAR1		33030		
0	7	1	156	17	0	12		1 104			CLA	CHAR		33040		
0	7	1	157	5	0	12		1 20			CIC	L20	SET LOWER CASE FROM UPPER CASE	33050		
0	7	1	160	13	0	12		1 074			STU	VAR5		33060		
0	7	1	161	15	0	12		1 154			CIU	L54		33070		
0	7	1	162	15	0	12		1 177	200000000		XOR	=0200000000		33080		
0	7	1	163	4	0	12		1 354			TNZ	L28P6		33090		
0	7	1	164	17	0	12		1 45			CLA	H24P3		33100		
0	7	1	165	13	0	12		1 073			STU	VAR4		33110		
0	7	1	166	5	0	12		1 214			CIC	L214	READY LINE	33120		
0	7	1	167	6	0	12		1 021			ANC	BR		33130		
0	7	1	170	4	0	12		1 172			TNZ	L24P4		33140		
0	7	1	171	10	0	12		1 354			TRA	L28P6		33150		
0	7	1	172	17	0	12		1 46			CLA	H24P4		33160		
0	7	1	173	13	0	12		1 073			STU	VAR4		33170		
0	7	1	174	10	0	12		1 000			TRA	L20P2A	DELAY 87.6 MSEC.	33180		
0	7	1	175	5	0	12		1 154	371000000		CIU	L54		33190		
0	7	1	177	4	0	12		1 354			TNZ	L28P6		33200		
0	7	1	200	17	0	12		1 147			STU	VAR4		33210		
0	7	1	201	13	0	12		1 073			CLA	H24P5	SET AND RESET DD4	33220		
0	7	1	202	17	0	12		1 173	000000020		CLA	=0000000020		33230		
0	7	1	203	5	0	12		1 210			CIU	ZERO		33240		
0	7	1	204	17	0	12		1 020			CLA	ZERO		33250		
0	7	1	205	5	0	12		1 210			CIC	Z10		33260		
0	7	1	206	00	0	12		1 171	140066210		TRA*	L9P3	RESET INT REG	33270		
0	7	1	207	5	0	12		1 214			CIU	Z14	READY LINE	33280		
0	7	1	210	6	0	12		1 021			AND	HH		33290		
0	7	1	211	4	0	12		1 354			TNZ	L28P6		33300		
0	7	1	212	13	0	12		1 101			TEST	OCTAL MODE		33310		
0	7	1	213	17	0	12		1 150			STU	CTR	RESET CTR	33320		
0	7	1	214	13	0	12		1 073			CLA	H25P1		33330		
0	7	1	215	17	0	12		1 173			STU	VAR4		33340		
0	7	1	216	13	0	12		1 100	000000020		CLA	=0000000020	8	33350		
0	7	1	217	16	0	7		207			STU	STOP		33360		
0	7	1	218	16	0	7		207			CDS	0,07		33370		
0	7	1	220	17	0	7		013			CLA	L20P5	REMOVE ADDRESS	33380		
0	7	1	221	6	0	7		1 040			AND	KX1		33390		
0	7	1	221	6	0	7		1 040			AND	KX1		33400		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 67)

IM	IS	S	L	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	7	1	222	15	0	7	1	042					XOR	KX3	= CIO 130	33410	
0	7	1	223	13	0	7	1	013					STU	L20P5		33420	
0	7	1	224	16	0	12	212						CDS	0,12	SET UPPER CASE	33430	
0	7	1	225	17	0	12	120						CLA	C60		33440	
0	7	1	226	5	0	12	120						CIC	120		33450	
0	7	1	227	13	0	12	1074						STO	VAR5		33460	
0	7	1	230	10	0	12	1000						TRA	L20P2A	DELAY 87.6 MSEC.	33470	
0	7	1	231	5	0	12	154						CIO	154		33480	
0	7	1	232	15	0	12	201		511000000				XOR	=0511000000	1,316,9	33490	
0	7	1	233	4	0	12	1354						TNZ	L28P6		33500	
0	7	1	234	17	0	12	151						REGIN	OCTAL		33510	
0	7	1	235	13	0	12	1073						CLA	H25P2		33520	
0	7	1	236	17	0	12	170						VAR4			33530	
0	7	1	237	5	0	12	210		000000004				CLA	=0000000004	SET AND RESET DO 2	33540	
0	7	1	240	17	0	12	1020						CIO	210		33550	
0	7	1	241	5	0	12	210						CLA	ZERO		33560	
0	7	1	242	00	0	12	171		140066210				TRA*	L9P3	RESET INT REG	33580	
0	7	1	243	17	0	12	1204						CLA	C64	OCTAL 1	33590	
0	7	1	244	5	0	12	130						CIO	130		33600	
0	7	1	245	13	0	12	1074						STO	VAR5		33610	
0	7	1	246	5	0	12	154						CIO	154		33620	
0	7	1	247	15	0	12	177						XOR	=0200000000		33630	
0	7	1	250	4	0	12	1354		200000000				TNZ	L28P6		33640	
0	7	1	251	17	0	12	152						CLA	H25P3		33650	
0	7	1	252	13	0	12	1073						STO	VAR4		33660	
0	7	1	253	5	0	12	214						CIO	214		33670	
0	7	1	254	6	0	12	1021						ANC	BB	READY LINE	33680	
0	7	1	255	4	0	12	1257						TNZ	L26P1		33690	
0	7	1	256	10	0	12	1354						TRA	L28P6		33700	
0	7	1	257	17	0	12	153						CLA	H26P1		33710	
0	7	1	260	13	0	12	1073						STC	VAR4		33720	
0	7	1	261	10	0	12	1000						TRA	L20P2A	DELAY 87.6 MSEC.	33730	
0	7	1	262	17	0	12	132						CLA	H20P3		33740	
0	7	1	263	13	0	12	1070						STU	VAR1		33750	
0	7	1	264	5	0	12	154						CIC	154		33760	
0	7	1	265	15	0	12	202		377000000				XOR	=0377000000	2 THRU 9	33770	
0	7	1	266	4	0	12	1354						TNZ	L28P6		33780	
0	7	1	267	10	0	12	1022						TRA	L21P1		33790	
0	7	1	270	13	0	12	1101						TYPE	DECIMAL		33800	
0	7	1	271	17	0	12	132						STU	CTR	RESET CTR	33810	
0	7	1	272	13	0	12	1070						CLA	H20P3		33820	
0	7	1	273	17	0	12	174						STU	VAR1		33830	
0	7	1	274	13	0	12	174		000000024				CLA	=0000000024	10	33840	
0	7	1	275	16	0	12	1100						STC	STOP		33850	
0	7	1	275	16	0	7	207						CDS	0,07		33860	
0	7	1	276	17	0	7	013						CLA	L20P5		33870	
0	7	1	277	6	0	7	1040						ANC	KX1		33880	
0	7	1	300	15	0	7	1043						XOR	KX4	REMOVE ADDRESS	33890	
0	7	1	301	13	0	7	013						STU	L20P5	= CIO 124	33900	
0	7	1	302	16	0	12	212						CDS	0,12		33910	
0	7	1	303	10	0	12	1012						TRA	L20P4		33920	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 68)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OCT	VAL	LHS	DPC	VARIABLE	COMMENT	SEC	NO
0	7	1	304	17	0	12	154				L27P1	CLA	TYPEWRITER CONTROL		33940	
0	7	1	305	13	0	12	1 073					STU	H27P1		33950	
0	7	1	306	13	0	12	1 070					STU	VAR4		33960	
0	7	1	307	17	0	12	203		000000010			CLA	VAR1		33970	
0	7	1	310	5	0	12	210					CLA	=0C00000010	CARRIAGE AT RIGHT-	33980	
0	7	1	311	5	0	12	214					CIC	210	HAND PARGE	33990	
0	7	1	312	5	0	12	214					CIC	214		34000	
0	7	1	312	6	0	12	1 021					ANC	HB		34010	
0	7	1	313	4	0	12	1 315					TNZ	L27P2		34020	
0	7	1	314	10	0	12	1 354					TRA	L28P6		34030	
C	7	1	315	17	0	12	1 55					CLA	H27P2		34040	
0	7	1	316	13	0	12	1 073					STC	VAR4		34050	
0	7	1	317	5	0	12	1 54					CIC	154		34060	
0	7	1	320	15	0	12	204		000020000			XOR	=0000020000		34070	
0	7	1	321	4	0	12	1 354					TNZ	L28P6		34080	
0	7	1	322	17	0	12	1 56					CLA	H27P3		34090	
0	7	1	323	13	0	12	1 073					STC	VAR4		34100	
0	7	1	324	17	0	12	1 032					CLA	K1	SET 00 1 AND RESET 00 3	34110	
0	7	1	325	5	0	12	210					CIC	210		34120	
0	7	1	326	5	0	12	074					CIC	074		34130	
0	7	1	327	5	0	12	1 54					CIC	154		34140	
0	7	1	330	4	0	12	1 354					TNZ	L28P6		34150	
0	7	1	331	17	0	12	1 57					CLA	H28P1		34160	
0	7	1	332	13	0	12	1 073					STC	VAR4		34170	
0	7	1	333	5	0	12	214					CIC	214		34180	
0	7	1	334	6	0	12	1 021					ANC	88		34190	
0	7	1	335	4	0	12	1 337					TNZ	L28P2		34200	
0	7	1	336	10	0	12	1 354					TRA	L28P6		34210	
0	7	1	337	17	0	12	1 60					CLA	H28P2		34220	
0	7	1	340	13	0	12	1 073					STU	VAR4		34230	
0	7	1	341	17	0	12	1 020					CLA	ZERO	RST 0-0. 1	34240	
0	7	1	342	5	0	12	210					CIC	210		34250	
0	7	1	343	5	0	12	214					CIC	214		34260	
0	7	1	344	6	0	12	1 021					ANC	88		34270	
0	7	1	345	4	0	12	1 354					TNZ	L28P6		34280	
C	7	1	346	13	0	12	1 073					STU	VAR4		34290	
0	7	1	347	13	0	12	1 074					STC	VAR5		34300	
0	7	1	350	00	0	12	1 62		070003100			TRA*	L28P3		34310	
0	7	1	351	00	0	12	205		120016100			TRA*	L29P1	FINISHED	34320	
0	7	1	352	15	0	12	1 104					CLA	CHAK		34330	
0	7	1	353	15	0	12	001					XOR	PATN		34340	
0	7	1	354	13	0	12	1 376					STC	776		34350	
0	7	1	355	00	0	12	206		070000500			TRA*	L28P6B		34360	
0	10	0	0	0	0	7	376					ORG	*10...0...7.		34370	
0	10	0	0	13	0	7	1 376					STO	776		34380	
0	10	0	1	13	0	7	1 076					STO	TEMP		34390	
0	10	0	2	17	0	7	1 376					CLA	776		34400	
0	10	0	3	13	0	7	1 071					STU	VAR2		34410	
0	10	0	4	17	0	7	1 076					CLA	TEMP		34420	
0	10	0	5	0	0	7	1 026					HOP	H95P1		34430	
0	10	0	6	13	0	7	1 376					STC	776	RESTORE ORIGINAL INSTRUCTIONS	34440	
0	10	0	7	17	0	7	1 012					CLA	L20P4		34450	
0	10	0	10	6	0	7	1 040					ANC	KX1	REMOVE ADDRESS	34460	
0	10	0	11	13	0	7	1 076					STC	TEMP		34470	
0	10	0	12	17	0	7	352					CLA	L28P4		34480	
0	10	0	13	6	0	7	1 045					ANC	KX6		34500	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 69)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	10	0	14	15	0	7	1	076				XOR	TEMP		34510	
0	10	0	15	13	0	7	012				STO	L20P4			34520	
0	10	0	16	17	0	7	013				CLA	L20P5			34530	
0	10	0	17	6	0	7	1 040				ANC	KX1	REMOVE ADDRESS		34540	
0	10	0	20	15	0	7	1 044				XOR	KX5	= CIC 120		34550	
0	10	0	21	13	0	7	013				STC	L20P5			34560	
0	10	0	22	17	0	7	020				CLA	L20P6			34570	
0	10	0	23	6	0	7	1 040				ANC	KX1	REMOVE ADDRESS		34580	
0	10	0	24	13	0	7	1 076				STC	TEMP			34590	
0	10	0	25	17	0	7	353				CLA	L28P5			34600	
0	10	0	26	6	0	7	1 045				ANC	KX6			34610	
0	10	0	27	15	0	7	1 076				XOR	TEMP			34620	
0	10	0	30	13	0	7	020				STC	L20P6			34630	
0	10	0	31	0	0	7	1 376				HOP	776			34640	
0	10	0	31	0	0	12	1				DOG	0,12			34650	
0	10	0	32	00	0	12	162		070003100		TRA*	ERROR RETURN			34660	
0	10	0	33	00	0	12	207		150032660		TRA*	L28P3			34670	
											L23P5	L20P2			34680	
											PATN				34700	
									171000000		OCT	L71000000	INTERRUPTS SET-A		34710	
									610000000		OCT	061000000	R		34720	
									700000000		OCT	070000000	C		34730	
									121000000		OCT	121000000	D		34740	
									130000000		OCT	130000000	E		34750	
									200000000		OCT	020000000	F		34760	
									310000000		OCT	031000000	G		34770	
									111000000		OCT	111000000	H		34780	
									100000000		OCT	100000000	I		34790	
									174000000		OCT	174000000	J		34800	
									640000000		OCT	064000000	K		34810	
									750000000		OCT	075000000	L		34820	
									124000000		OCT	124000000	M		34830	
									135000000		OCT	135000000	N		34840	
									250000000		OCT	025000000	O		34850	
									340000000		OCT	034000000	P		34860	
									114000000		OCT	114000000	Q		34870	
									105000000		OCT	105000000	R		34880	
									620000000		OCT	062000000	S		34890	
									730000000		OCT	073000000	T		34900	
									122000000		OCT	122000000	U		34910	
									133000000		OCT	133000000	V		34920	
									230000000		OCT	023000000	W		34930	
									320000000		OCT	032000000	X		34940	
									112000000		OCT	112000000	Y		34950	
									103000000		OCT	103000000	Z		34960	
									177000000		OCT	177000000	1 BCD		34970	
									067000000		OCT	067000000	2		34980	
									076000000		OCT	076000000	3		34990	
									127000000		OCT	127000000	4		35000	
									136000000		OCT	136000000	5		35010	
									260000000		OCT	026000000	6		35020	
									370000000		OCT	037000000	7		35030	
									117000000		OCT	117000000	8		35040	
									106000000		OCT	106000000	9		35050	
									160000000		OCT	016000000	0	SPECIAL CHARS	35060	
									700000000		OCT	007000000			35070	
									163000000		OCT	163000000				

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 70)

TM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMPENT	SEC	NC
0	12							47	17200000			UCT	17200000		35080	
0	12							50	2000000			UCT	00200000		35090	
0	12							51	165000000			UCT	165000000		35100	
0	12							52	4000000			UCT	00400000		35110	
0	12							53	160000000			UCT	160000000		35120	
0	12							54	1000000			UCT	00100000		35130	
0	12							55	10000			UCT	00001000	SPACE	35140	
0	12							56	517000000	P45		UCT	517000000	UPPER CASE	35150	
0	12							57	106000000			UCT	106000000		35160	
0	12							60	16000000			UCT	01600000		35170	
0	12							61	7000000			UCT	00700000		35180	
0	12							62	12000000			UCT	03200000		35190	
0	12							63	112000000			UCT	112000000		35200	
0	12							64	103000000			UCT	103000000		35210	
0	12							65	163000000			UCT	163000000		35220	
0	12							66	2000000			UCT	00200000		35230	
0	12							67	34000000			UCT	03400000		35240	
0	12							70	114000000			UCT	114000000		35250	
0	12							71	105000000			UCT	105000000		35260	
0	12							72	165000000			UCT	165000000		35270	
0	12							73	4000000			UCT	00400000		35280	
0	12							74	31000000			UCT	03100000		35290	
0	12							75	111000000			UCT	111000000		35300	
0	12							76	100000000			UCT	100000000		35310	
0	12							77	160000000			UCT	160000000		35320	
0	12							100	1000000			UCT	00100000	1	35330	
0	12							101	177000000			UCT	177000000	2	35340	
0	12							102	67000000			UCT	06700000	3	35350	
0	12							103	76000000			UCT	07600000	4	35360	
0	12							104	127000000			UCT	127000000	5	35370	
0	12							105	136000000			UCT	136000000	6	35380	
0	12							106	26000000			UCT	02600000	7	35390	
0	12							107	37000000			UCT	03700000	8	35400	
0	12							110	16000000			UCT	01600000	9	35410	
0	12							111	177000000			UCT	177000000	DECIMAL 1	35420	
0	12							112	67000000			UCT	06700000	2	35430	
0	12							113	76000000			UCT	07600000	3	35440	
0	12							114	127000000			UCT	127000000	4	35450	
0	12							115	136000000			UCT	136000000	5	35460	
0	12							116	26000000			UCT	02600000	6	35470	
0	12							117	37000000			UCT	03700000	7	35480	
0	12							120	117000000			UCT	117000000	8	35490	
0	12							121	106000000			UCT	106000000	9	35500	
0	12							122	16000000			UCT	01600000	C	35510	
0	12							123	10000			UCT	00001000	SPACE - CNTRL OPNS	35520	
0	12							124	400000			UCT	00040000	TAB	35530	
0	12							125	20000			UCT	00020000	CARR RTN	35540	
0	12							126	200000			UCT	00020000	INDEX	35550	
0	12							127	100000			UCT	00010000	RED	35560	
0	12							130	40000			UCT	00004000	BLACK	35570	
0	12							131	150032660	H20P2	HPC	UCT	H20P2		35580	
0	12							132	120002670	H20P3	HPC	UCT	H20P3		35590	
0	12							133	120005270	H20P4	HPC	UCT	H20P4		35600	
0	12							134	120011270	H21P1	HPC	UCT	H21P1		35610	
0	12							135	120014270	H21P2	HPC	UCT	H21P2		35620	
0	12							136	120020670	H21P3	HPC	UCT	H21P3		35630	
0	12							137	120041270	H22P4	HPC	UCT	H22P4		35640	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 71)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	GPC	VARIABLE	COMMENT	SEQ	NO
0	12							140	120047270	H23P1	HPC	L23P1			35650	
0	12							141	120054270	H23P2	HPC	L23P2			35660	
0	12							142	120057270	H23P3	HPC	L23P3			35670	
0	12							143	120015100	H23P5	HPC	L23P5			35680	
0	12							144	120065270	H24P1	HPC	L24P1			35690	
0	12							145	120072270	H24P3	HPC	L24P3			35700	
0	12							146	120075270	H24P4	HPC	L24P4			35710	
0	12							147	120100270	H24P5	HPC	L24P5			35720	
0	12							150	120105270	H25P1	HPC	L25P1			35730	
0	12							151	120116270	H25P2	HPC	L25P2			35740	
0	12							152	120124670	H25P3	HPC	L25P3			35750	
0	12							153	120127670	H26P1	HPC	L26P1			35760	
0	12							154	120142270	H27P1	HPC	L27P1			35770	
0	12							155	120146670	H27P2	HPC	L27P2			35780	
0	12							156	120151270	H27P3	HPC	L27P3			35790	
0	12							157	120154670	H28P1	HPC	L28P1			35800	
0	12							160	120157670	H28P2	HPC	L28P2			35810	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 72)

IM	IS	S	LOC	UP	DM	DS	9	ADR	ECT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	10	0	14	17	0	12	1	060				CLA	BEGINNING OF ROUTINE FIVE		35830	
0	10	0	35	14	0	12	041				L29P1	CHK	CHECK PRINTER LOGIC AND INTERFACE		35840	
0	10	0	36	4	0	17	040					LCR5			35850	
0	10	0	37	00	0	17	210					TNZ	L45PIA		35860	
0	10	0	40	00	0	12	211	130007000			L45PIA	TRA*			35870	
0	10	0	41	17	0	12	161	150000310			L29P2	CLA	L45PI		35880	
0	10	0	42	13	0	12	1070					H29P2	H29P2		35890	
												V1	V1		35900	
												HPC	L29P2		35910	
												SYN	VAK1		35920	
												SYN	VAK2		35930	
												SYN	VAK3		35940	
												SYN	VAK4		35950	
												SYN	VAK5		35960	
												CLS	U+15		35970	
												CLA	H29P4		35980	
												STC	V2		35990	
												TRA	L43PI		36000	
												CLA	ZERU		36010	
												CLS	170		36020	
												PRS	775		36030	
												CIC	164		36040	
												PRS	775		36050	
												STL	CTR		36060	
												CLA	=0000000200	64 DECIMAL	36070	
												HOP	HOP3		36080	
												CLA	=0000000040	RST INT NEG	36100	
												CIC	210	SET DO 5	36120	
												CIC	214	PRINTER NCT RUNNING	36130	
												ANL	K1		36140	
												TNZ	L29P3		36150	
												TRA	L42P4		36160	
												CLA	H29P3		36170	
												STG	V1		36180	
												CLA	ZERU		36190	
												CIC	210	RST DO 5	36200	
												CLA	=0000000020	SET DO 4	36210	
												CIC	214		36220	
												ANL	K1		36230	
												TNZ	L29P4		36240	
												TRA	L42P4		36250	
												CLA	H29P4		36260	
												STG	V1		36270	
												CLA	F30P1		36280	
												STC	V2		36290	
												CLA	ZERU		36300	
												CIC	210		36310	
												CIC	214		36320	
												ANL	K1		36330	
												TNZ	L42P3		36340	
												CLA	H30P1		36350	
												STC	V1		36360	
												CLA	H30P2		36370	
												STC	V2		36380	
															36390	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 73)

IM	IS	S	LUC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	10	0	115	5	0	15	170					CIC	I70	BCD MODE	36400	
0	10	0	116	17	0	15	1104					CLA	CHAR		36410	
0	10	0	117	13	0	15	1074					STU	V5		36420	
0	10	0	120	1	0	15	1375					PRS	775		36430	
0	10	0	121	5	0	15	154					TEST	PRS 775	READ INT REG	36440	
0	10	0	122	15	0	15	116					CIU	154		36450	
0	10	0	123	4	0	15	1232					XOR	PATN1		36460	
0	10	0	124	17	0	15	060					TNZ	L42P3		36470	
0	10	0	125	13	0	15	1070				L30P2	CLA	H30P2		36480	
0	10	0	126	17	0	15	1321				STU	V1	H30P2A		36490	
0	10	0	127	13	0	15	1071				STU	V2			36510	
0	10	0	130	0	0	15	1023				HOP	H9P3		RST INT REG	36520	
0	10	0	131	5	0	15	154				CIU	154			36530	
0	10	0	132	4	0	15	1240				TNZ	L42P4			36540	
0	10	0	133	17	0	15	062				ENTER	8CU LOOP			36550	
0	10	0	134	13	0	15	1070				L30P2A	CLA	H31P4		36560	
0	10	0	135	17	0	15	061				STU	V1			36570	
0	10	0	136	13	0	15	1071				CLA	H31P3			36580	
0	10	0	137	10	0	15	145				STU	V2			36590	
0	10	0	140	1	0	15	1104				TRA	L31P3			36600	
0	10	0	141	13	0	15	1074				TEST	PRS MEMORY AND DECODE LOGIC			36610	
0	10	0	142	5	0	15	154				L31P1	PRS	CHAR		36620	
0	10	0	143	15	0	15	116				STU	V5			36630	
0	10	0	144	4	0	15	1240				CIC	154		READ INT REG	36640	
0	10	0	145	17	0	15	1101				XOR	PATN1			36650	
0	10	0	146	7	0	15	1032				TNZ	L42P4			36660	
0	10	0	147	13	0	15	1101				CLA	C1K			36670	
0	10	0	150	16	0	10	210				ADC	K1			36680	
0	10	0	151	17	0	10	140				STU	CTR			36690	
0	10	0	152	7	0	10	1037				CDS	O+10			36700	
0	10	0	153	13	0	10	140				CLA	L31P1			36710	
0	10	0	154	17	0	10	143				ACC	K52			36720	
0	10	0	155	7	0	10	1037				STU	L31P1			36730	
0	10	0	156	13	0	10	143				CLA	L31P2			36740	
0	10	0	157	16	0	15	215				ADC	K52			36750	
0	10	0	160	0	0	15	1023				STU	L31P2			36760	
0	10	0	161	17	0	15	1101				CDS	O+15			36770	
0	10	0	162	2	0	15	1100				HOP	H9P3		RST INT REG	36780	
0	10	0	163	4	0	15	140				CLA	CTR			36790	
0	10	0	164	1	0	15	331				SUB	STOP			36800	
0	10	0	165	13	0	15	1074				TNZ	L31P1		NOT EQUAL - CONTINUE	36810	
0	10	0	166	17	0	15	041			007700000	L32P1	PRS	=0007700000		36820	
0	10	0	167	13	0	15	1070				STU	V5			36830	
0	10	0	170	5	0	15	154				CLA	H32P1			36840	
0	10	0	171	15	0	15	332			150072100	H32P1	HPC	L32P1		36850	
0	10	0	172	4	0	15	1232				STU	V1			36860	
0	10	0	173	17	0	15	063			774300000	CIU	154			36880	
0	10	0	174	13	0	15	1070				XOR	=0774300000			36890	
0	10	0	175	0	0	15	1023				TNZ	L42P3		1-7,11,12	36900	
0	10	0	176	1	0	15	333				CLA	H32P2			36910	
0	10	0	177	13	0	15	1074				STU	V1			36920	
0	10	0	200	5	0	15	154			000077000	HOP	H9P3		RST INT REG	36930	
0	10	0	200	5	0	15	154				PRS	=0000077000			36940	
0	10	0	200	5	0	15	154				STU	V5			36950	
0	10	0	200	5	0	15	154				CIU	154			36960	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 74)

JM JS S LDC	DP	DM	DS	9	ADR	DCT VAL	LMS	DPL	VARIABLE	COMMENT	SEC NC
0 10 0 201	15	0	15	332				XOR	=0774300000		36970
0 10 0 202	4	0	15	1 232	774300000			TNZ	L42P3		36980
0 10 0 203	17	0	15	064		L32P3		CLA	H32P3		36990
0 10 0 204	13	0	15	1 070				STU	V1		37000
0 10 0 205	0	0	15	1 023				HCP	H9P3	RST INT REG	37010
0 10 0 206	1	0	15	334	000000770			PRS	=0000000770		37020
0 10 0 207	13	0	15	1 074				STU	V5		37030
0 10 0 210	5	0	15	154				CIU	L54		37040
0 10 0 211	15	0	15	332	774300000			XOR	=0774300000		37050
0 10 0 212	4	0	15	1 232				TNZ	L42P3		37060
0 10 0 213	17	0	15	065				TEST PRS	774		37070
0 10 0 214	13	0	15	1 070		L32P4		CLA	H32P4		37080
0 10 0 215	0	0	15	1 023				STU	V1		37090
0 10 0 216	17	0	15	1 020				HOP	H9P3	RST INT REG	37100
0 10 0 217	1	0	15	1 374				CLA	ZERO		37110
0 10 0 220	13	0	15	1 074				PKS	774		37120
0 10 0 221	5	0	15	154				STU	V5		37130
0 10 0 222	4	0	15	1 232	004700000			CIU	L54		37140
0 10 0 223	15	0	15	335				XOR	=0004700000	7,10,11,12	37150
0 10 0 224	17	0	15	066				TNZ	L42P3		37160
0 10 0 225	13	0	15	1 070		L33P1		CLA	H33P1		37170
0 10 0 226	17	0	15	1 032				STU	V1		37180
0 10 0 227	5	0	15	210				CLA	K1		37190
0 10 0 230	5	0	15	214				CIU	214		37200
0 10 0 231	6	0	15	1 032				AND	K1	SET DO 1	37210
0 10 0 232	4	0	15	1 234				TNZ	L33P2		37220
0 10 0 233	10	0	15	1 232				TRA	L42P3		37230
0 10 0 234	17	0	15	067		L33P2		CLA	H33P2		37240
0 10 0 235	13	0	15	1 070				STU	V1		37250
0 10 0 236	17	0	15	1 020				CLA	ZERU		37260
0 10 0 237	5	0	15	210				CIU	210	RESET DO 1	37270
0 10 0 240	5	0	15	214				CIU	214		37280
0 10 0 241	6	0	15	1 032				AND	K1		37290
0 10 0 242	4	0	15	1 232				TNZ	L42P3		37300
0 10 0 243	17	0	15	070		L33P3		CLA	H33P3		37310
0 10 0 244	13	0	15	1 070				STU	V1		37320
0 10 0 245	0	0	15	1 023				HOP	H9P3	RST INT REG	37330
0 10 0 246	5	0	15	154				CIU	L54		37340
0 10 0 247	4	0	15	1 232				TNZ	L42P3		37350
0 10 0 250	17	0	15	1 020				TEST OCTAL MODE DECODING			37360
0 10 0 251	13	0	15	1 101		L34P1		CLA	ZERO		37370
0 10 0 252	16	0	10	210				STU	CTR		37380
0 10 0 253	17	0	10	372				CDS	0,10		37390
0 10 0 254	6	0	10	1 046				CLA	K34P2		37400
0 10 0 255	13	0	10	1 076				AND	KX7	RETAIN ADDRESS	37410
0 10 0 256	17	0	10	1 076				STC	TEMP		37420
0 10 0 257	6	0	10	1 047				CLA	L34P2		37430
0 10 0 260	15	0	10	1 076				AND	KX8	REMOVE ADDRESS	37440
0 10 0 261	13	0	10	301				XOR	TEMP		37450
0 10 0 262	17	0	10	373				STU	L34P2		37460
0 10 0 263	6	0	10	1 046				AND	K34P3		37470
0 10 0 264	13	0	10	1 076				STU	KX7		37480
0 10 0 265	17	0	10	304				CLA	L34P3		37490
0 10 0 266	6	0	10	1 047				AND	KX8		37510
0 10 0 267	15	0	10	1 076				XOR	TEMP		37520
0 10 0 267	15	0	10	1 076				XOR	TEMP		37530

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 75)

IM IS S. LOC	OP	UM	DS	9	ADR	OCT VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NC
0 10 0 270	13	0	10	304				STO	L34P3		37540
0 10 0 271	16	0	15	215				CDS	0*15		37550
0 10 0 272	5	0	15	164				CIO	164	SET OCTAL MODE	37560
0 10 0 273	17	0	15	072				CLA	H34P5		37570
0 10 0 274	13	0	15	1 070				STO	VI		37580
0 10 0 275	17	0	15	071				CLA	H34P4		37590
0 10 0 276	13	0	15	1 071				STO	V2		37600
0 10 0 277	17	0	15	336		400000000		CLA	=04	INHIBIT CHECK BIT AT 10.11.12 TIME	37610
0 10 0 300	5	0	15	250				CIO	250		37620
0 10 0 301	1	0	15	042			L34P2	PRS	PRSC		37630
0 10 0 302	13	0	15	1 074				STO	V5		37640
0 10 0 303	5	0	15	154				CIO	154		37650
0 10 0 304	15	0	15	216			L34P3	XDR	PATN4		37660
0 10 0 305	4	0	15	1 240				TNZ	L42P4		37670
0 10 0 306	17	0	15	1 101			L34P4	CLA	CTR		37680
0 10 0 307	7	0	15	1 036				ADD	KS1		37690
0 10 0 310	13	0	15	1 101				STO	CTR		37700
0 10 0 311	16	0	10	210				CDS	0*10		37710
0 10 0 312	17	0	10	301				CLA	L34P2		37720
0 10 0 313	7	0	10	1 037				ADD	KS2		37730
0 10 0 314	13	0	10	301				STO	L34P2		37740
0 10 0 315	17	0	10	304				CLA	L34P3		37750
0 10 0 316	7	0	10	1 037				ADC	KS2		37760
0 10 0 317	13	0	10	304				STO	L34P3		37770
0 10 0 320	16	0	15	215			L34P5	HDP	0*15		37780
0 10 0 321	0	0	15	1 023				CLA	H9P3		37790
0 10 0 322	17	0	15	1 101				CTR	CTR		37800
0 10 0 323	2	0	15	1 137				SUB	C27	=8	37810
0 10 0 324	4	0	15	301				TNZ	L34P2		37820
				42		0	PRSC	OCT	0		37830
				43		111111112		OCT	111111112		37840
				44		222222222		OCT	222222222		37850
				45		333333332		OCT	333333332		37860
				46		444444444		OCT	444444444		37870
				47		555555554		OCT	555555554		37880
				50		666666666		OCT	666666666		37890
				51		777777774		OCT	777777774		37900
								TEST DIGITS 2 THRU 9 DECODE			37920
0 10 0 325	17	0	15	073			L34P6	CLA	H34P6		37930
0 10 0 326	13	0	15	1 070				STO	VI		37940
0 10 0 327	1	0	15	337		411111114		PRS	=0411111114		37950
0 10 0 330	7	0	15	1 020				ADD	ZERO		37960
0 10 0 331	5	0	15	154				CIO	154		37970
0 10 0 332	15	0	15	340		170300000		XDR	=0170300000	3-6.11.12	37980
0 10 0 333	4	0	15	1 232				TNZ	L42P3		37990
0 10 0 334	17	0	15	074			L34P7	CLA	H34P7		38000
0 10 0 335	13	0	15	1 070				STO	VI		38010
0 10 0 336	0	0	15	1 023				HDP	H9P3		38020
0 10 0 337	1	0	15	341				PRS	=0122222222		38030
0 10 0 340	7	0	15	1 020		122222222		ADD	ZERO		38040
0 10 0 341	5	0	15	154				CIO	154		38050
0 10 0 342	15	0	15	1 034				XDR	K1303	3.5.6.11.12	38060
0 10 0 343	4	0	15	1 232				TNZ	L42P3		38070
0 10 0 344	17	0	15	075				CLA	H34P8		38080
0 10 0 345	13	0	15	1 070			L34P8	STO	VI		38090
0 10 0 346	0	0	15	1 023				HDP	H9P3		38100

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 76)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	10	0	347	1	0	15	342		244444444			PRS	=02444444444		38110	
0	10	0	350	7	0	15	1 020					ADC	ZEMO		38120	
0	10	0	351	5	0	15	154					CIC	154		38130	
0	10	0	352	15	0	15	343		160300000			XOK	=01603000000	3-5,11,12	38140	
0	10	0	353	4	0	15	1 232					TNZ	L42P3		38150	
0	10	0	354	17	0	15	076					TEST	CHECK BIT FOR 10,11,12 TIME OCTAL MODE		38160	
0	10	0	355	13	0	15	1 070				L34P9	CLA	H34P9		38170	
0	10	0	356	0	0	15	1 023					STO	V1		38180	
0	10	0	357	17	0	15	054					HOP	H9P3		38190	
0	10	0	360	5	0	15	250		200000000			CLA	=02		38200	
0	10	0	361	1	0	15	344		4111111140			CIC	250		38210	
0	10	0	362	7	0	15	1 020					PRS	=0411111114	RESET CHECK BIT INHIBIT	38220	
0	10	0	363	5	0	15	154					ADC	ZEMO		38230	
0	10	0	364	15	0	15	345		174300000			CIU	154		38240	
0	10	0	365	4	0	15	1 232					XOR	=01743000000	3-7,11,12	38250	
0	10	0	366	0	0	15	1 023					TNZ	L42P3		38260	
0	10	0	367	00	0	15	346		150130110			HOP	H9P3		38270	
0	10	0	370	1	0	15	1 04					TRA*	L35P2		38280	
0	10	0	371	15	0	15	116				K31P1	PRS	CHAR		38290	
0	10	0	372	1	0	15	042				K31P2	XOR	PATN1		38300	
0	10	0	373	15	0	15	216				K34P2	PRS	PRSC		38310	
0	10	0	373	15	0	15	216				K34P3	XOR	PATN4		38320	
0	11	0	260	0	15	52						CARRIAGE CONTROL TESTS			38340	
0	11	0	260	17	0	15	052					IMMEDIATE SKIP			38350	
0	11	0	261	13	0	15	1 070		150147510			ORG	,11,,260,,15,		38360	
0	11	0	262	17	0	15	053				L35P2	CLA	H36P2		38370	
0	11	0	263	13	0	15	1 071				H36P2	HPC	L36P2		38380	
0	11	0	264	17	0	15	1 020					STU	V1		38390	
0	11	0	265	13	0	15	1 101					CLA	H36P1		38400	
0	11	0	266	17	0	15	347					HPC	L36P1		38410	
0	11	0	267	13	0	15	1 100		000000030			STC	V2		38420	
0	11	0	270	17	0	15	1 136					CLA	ZEMO		38430	
0	11	0	271	13	0	15	1 076					STU	CTR		38440	
0	11	0	272	17	0	15	1 076					CLA	=0000000030	=12	38450	
0	11	0	273	13	0	15	1 074					STC	STOP		38460	
0	11	0	274	5	0	15	160					CIU	160		38470	
0	11	0	275	5	0	15	154					CIO	154		38480	
0	11	0	276	15	0	15	226					XOR	PATN2		38490	
0	11	0	277	4	0	15	343					TNZ	L42P4A		38500	
0	11	0	300	17	0	15	1 101					CLA	CTR		38510	
0	11	0	301	7	0	15	1 032					ADU	K1		38520	
0	11	0	302	13	0	15	1 101					STU	CTR		38530	
0	11	0	303	17	0	15	1 032					CLA	K1		38540	
0	11	0	304	5	0	15	210					CIU	210		38550	
0	11	0	305	17	0	15	1 020					CLA	ZEMO		38560	
0	11	0	306	5	0	15	210					CIO	210		38570	
0	11	0	307	17	0	15	1 076					CLA	TEMP		38580	
0	11	0	310	7	0	15	1 136					ACC	C26		38600	
0	11	0	311	13	0	15	1 076					STO	TEMP		38620	
0	11	0	312	16	0	11	211					CDS	O,11		38630	
0	11	0	313	17	0	11	276					CLA	L35P4		38640	
0	11	0	314	7	0	11	1 037					ADD	K52		38650	
															38660	
															38670	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 77)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	11	0	315	13	0	15	1	276				STO	L35P4		38680	
0	11	0	316	16	0	15	1	215				CDS	0*15		38690	
0	11	0	317	0	0	15	1	023			L36P2	HOP	H9P3	RST INT REG	38700	
0	11	0	320	17	0	15	1	101				CLA	CTR		38710	
0	11	0	321	2	0	15	1	100				SUB	STOP	CONTINUE IN LOOP	38720	
0	11	0	322	4	0	15	1	272			L36P3	TNZ	L35P3		38730	
0	11	0	323	17	0	15	1	100				CLA	STOP		38740	
0	11	0	324	2	0	15	1	347	000000030			SUB	=0000000030	IS STOP = 12	38750	
0	11	0	325	4	0	15	1	334				TNZ	L37P1		38760	
0	11	0	326	13	0	15	1	101				STU	CTR	RST CTR	38780	
0	11	0	327	17	0	15	1	350			L36P4	CLA	=0000000006	=3	38790	
0	11	0	330	13	0	15	1	100	000000006			STO	STOP		38800	
0	11	0	331	17	0	15	1	115				CLA	C9	=410000000	38810	
0	11	0	332	13	0	15	1	076				STO	TEMP		38820	
0	11	0	333	10	0	15	1	272				TRA	L35P3		38830	
0	11	0	334	17	0	15	1	100				CLA	H37P5	SKIP AFTER PRINT	38840	
0	11	0	335	13	0	15	1	070			L37P1	STO	V1		38850	
0	11	0	336	17	0	15	1	077				CLA	H37P4		38860	
0	11	0	337	13	0	15	1	071				STO	V2		38870	
0	11	0	340	17	0	15	1	020				CLA	ZERO		38880	
0	11	0	341	13	0	15	1	101				STU	CTR		38890	
0	11	0	342	00	0	15	1	351	150000300			TRA*	L37P1A		38900	
0	11	0	343	0	0	15	1	026			L42P4A	HOP	H95P1		38910	
0	11	0	344	15	0	15	1	226			K35P4	XOR	PATN2		38920	
0	10	1	0	0	0	15	1	54				ORG	*10*1*1*15*		38950	
0	10	1	1	13	0	15	1	100	000000030		L37P1A	CLA	=00000000030	=12	38960	
0	10	1	2	17	0	15	1	104				CLA	CHAK		38970	
0	10	1	3	13	0	15	1	076				STO	TEMP	=610000000	38980	
0	10	1	4	17	0	15	1	076			L37P2	CLA	TEMP		38990	
0	10	1	5	13	0	15	1	074				STO	V5		39000	
0	10	1	6	5	0	15	1	160				C10	160		39010	
0	10	1	7	17	0	15	1	032				CLA	K1		39020	
0	10	1	10	5	0	15	1	210				C10	210	SET DD 1	39030	
0	10	1	11	17	0	15	1	020				CLA	ZERO		39040	
0	10	1	12	5	0	15	1	210				C10	210	RST DD 1	39050	
0	10	1	13	5	0	15	1	154				C10	154		39060	
0	10	1	14	15	0	15	1	245			L37P3	XOR	PATN3		39070	
0	10	1	15	4	0	15	1	240				FNZ	L42P4		39080	
0	10	1	16	17	0	15	1	101			L37P4	CLA	CTR		39090	
0	10	1	17	7	0	15	1	032				ADD	K1		39100	
0	10	1	20	13	0	15	1	101				STO	TEMP		39110	
0	10	1	21	17	0	15	1	076				CLA	TEMP		39120	
0	10	1	22	7	0	15	1	136				ADD	C26		39130	
0	10	1	23	13	0	15	1	076				STO	TEMP	=010000000	39140	
0	10	1	24	16	0	10	1	210				CDS	0*10		39150	
0	10	1	25	17	0	10	1	014				CLA	L37P3		39160	
0	10	1	26	7	0	10	1	036				ADC	K51		39170	
0	10	1	27	13	0	10	1	014				STO	L37P3		39180	
0	10	1	30	16	0	15	1	215				CDS	0*15		39190	
0	10	1	31	0	0	15	1	023			L37P5	HOP	H9P3		39200	
0	10	1	32	17	0	15	1	101			L38P1	CLA	CTR	RST INT REG	39210	
0	10	1	33	2	0	15	1	100				SUB	STOP		39220	
0	10	1	34	4	0	15	1	004				TNZ	L37P2		39230	
0	10	1	34	4	0	15	1	004				TNZ	L37P2		39240	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 78)

EM	IS	LOC	UP	UM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	10	1	35	17	0	15	1	100			CLA	STDP		39250	
0	10	1	36	7	0	15	347	000000030		L38P2	SUB	=0000000030	=L2	39260	
0	10	1	37	4	0	15	1	046			TNZ	L38P4		39270	
0	10	1	40	13	0	15	1	101		L38P3	STC	CTR	=ZERO	39280	
0	10	1	41	17	0	15	350	000000006			CLA	=0000000006	=3	39290	
0	10	1	42	13	0	15	1	100			STC	STUP		39300	
0	10	1	43	17	0	15	1	152			CLA	CJR	=710C00000	39310	
0	10	1	44	13	0	15	1	076			STO	TEMP		39320	
0	10	1	45	10	0	15	1	004			TRA	L37P2		39330	
* AUTOMATIC CARRIAGE SKIP AND PRINTER READY LINE CHECK															
0	10	1	46	17	0	15	1	071		L38P4	CLA	H38P4		39350	
0	10	1	47	13	0	15	1	070			STC	VI		39360	
0	10	1	50	17	0	15	1	020			CLA	ZERO		39370	
0	10	1	51	13	0	15	1	074			STC	VAR5		39380	
0	10	1	52	17	0	15	352	000000110			CLA	=0000000110	DU 3 CARR BUSY DU 6 CHANNEL 12 INDICATOR	39390	
0	10	1	53	5	0	15	210				CIU	210		39420	
0	10	1	54	5	0	15	214				CIU	214		39430	
0	10	1	55	6	0	15	1	032			ANC	K1		39440	
0	10	1	56	4	0	15	1	060			TNZ	L39P1	READY LINE	39450	
0	10	1	57	10	0	15	1	232			TRA	L42P3		39460	
0	10	1	60	17	0	15	1	02		L39P1	CLA	H39P1		39470	
0	10	1	61	13	0	15	1	070			STO	VI		39480	
0	10	1	62	17	0	15	1	020			CLA	ZERO	RESET DU 3,6	39490	
0	10	1	63	5	0	15	210				CIU	210		39500	
0	10	1	64	17	0	15	1	032			CLA	K1	SET DU 1 (PRINTING)	39510	
0	10	1	65	5	0	15	210				CIU	210		39520	
0	10	1	66	5	0	15	154				CIU	154		39530	
0	10	1	67	15	0	15	353	612020000			XOR	=0612020000	1,2,6,8,14	39540	
0	10	1	70	4	0	15	1	232		L39P2	TNZ	L42P3		39550	
0	10	1	71	17	0	15	1	03			CLA	H39P2		39560	
0	10	1	72	13	0	15	1	070			STU	VI		39570	
0	10	1	73	13	0	15	1	073			STO	V4		39580	
0	10	1	74	17	0	15	1	020			CLA	ZERO		39590	
0	10	1	75	5	0	15	210				CIC	210	RESET 001,003 GENERATED TRANSFER	39600	
0	10	1	76	10	0	15	1	100			TRA**			39610	
0	10	1	100	5	0	15	154				CIC	154		39620	
0	10	1	101	15	0	15	353	612020000		L39P2A	XOR	=0612020000	1,2,6,8,14	39630	
0	10	1	102	4	0	15	1	232			TNZ	L42P3		39640	
0	10	1	103	17	0	15	1	04		L39P3	CLA	H39P3		39650	
0	10	1	104	13	0	15	1	073		L39P3A	STO	V4		39660	
0	10	1	105	5	0	15	214				CIU	214		39670	
0	10	1	106	6	0	15	1	032			ANC	K1		39680	
0	10	1	107	4	0	15	1	232			TNZ	L42P3		39690	
0	10	1	110	17	0	15	1	05		L39P4	CLA	H39P4		39700	
0	10	1	111	13	0	15	1	070			STU	VI		39710	
0	10	1	112	17	0	15	1	020			CLA	ZERO		39720	
0	10	1	113	13	0	15	1	073			STO	VAR4		39730	
0	10	1	114	0	0	15	1	023			HOP	H9P3	RST INT REG	39740	
0	10	1	115	5	0	15	154				CIU	154		39750	
0	10	1	116	4	0	15	1	232			TNZ	L42P3		39760	
* BCU MODE PARITY ERROR															
0	10	1	117	17	0	15	106			L40P1	CLA	H40P1		39770	
0	10	1	120	13	0	15	1	070			STU	VI		39780	
0	10	1	121	5	0	15	170				CIU	170	SET BCD MODE	39800	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 79)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	10	1	122	17	0	15		301	000000010			CLA	=0000000010	SET DO 3 (CARR BUSY)	39810	
0	10	1	123	5	0	15		210			C1C	210			39820	
0	10	1	124	17	0	15		354	000000014			CLA	=0000000014		39830	
0	10	1	125	5	0	15		210			C1U	210		SET DO 2 (PARITY ERROR)	39840	
0	10	1	126	17	0	15		355	000000016			CLA	=0C00000016		39850	
0	10	1	127	5	0	15		210			C1U	210		SET DO 1 (PROCESSOR RELEASE)	39860	
0	10	1	130	5	0	15		264			C1C	264			39870	
0	10	1	131	5	0	15		154			C1U	154			39880	
0	10	1	132	15	0	15		356	001020000			XOR	=0001020000	9,14	39890	
0	10	1	133	4	0	15		1232			TNZ	L42P3			39900	
0	10	1	134	17	0	15		107		L40P2		CLA	H40P2		39910	
0	10	1	135	13	0	15		1070			STO	V1			39920	
0	10	1	136	17	0	15		301	000000010			CLA	=0000000010	RST DO1, DO2	39930	
0	10	1	137	5	0	15		210			C1O	210			39940	
0	10	1	140	1	0	15		020			PRS	ZERO			39950	
0	10	1	141	5	0	15		154			C1U	154			39960	
0	10	1	142	15	0	15		357	005320000			XOR	=0005320000	7,9,11,12,14	39970	
0	10	1	143	4	0	15		1232			TNZ	L42P3			39980	
0	10	1	144	17	0	15		110		L40P3		CLA	H40P3		39990	
0	10	1	145	13	0	15		1070			STO	V1			40000	
0	10	1	146	17	0	15		020			CLA	ZERO			40010	
0	10	1	147	5	0	15		210			C1U	210		RST DO 3	40020	
0	10	1	150	1	0	15		1375			PKS	775			40030	
0	10	1	151	5	0	15		154			C1U	154			40040	
0	10	1	152	15	0	15		360	205320000			XOR	=0205320000		40050	
0	10	1	153	4	0	15		1232			TNZ	L42P3		2,7,9,11,12,14	40060	
0	10	1	154	17	0	15		111		L41P1		CLA	H41P1		40070	
0	10	1	155	13	0	15		1070			STO	V1			40080	
0	10	1	156	13	0	15		023			HOP	H9P3		RST INT REG	40090	
0	10	1	157	5	0	15		154			C1O	154			40100	
0	10	1	160	4	0	15		1232			TNZ	L42P3			40110	
0	10	1	161	17	0	15		112			OPC	CLA		OCTAL MODE - PARITY ERROR DURING PRINT	40130	
0	10	1	162	13	0	15		1070		L41P2		CLA	H41P2		40140	
0	10	1	163	5	0	15		164			STO	V1			40150	
0	10	1	164	17	0	15		032			C1O	164		SET OCTAL MODE	40160	
0	10	1	165	5	0	15		210			CLA	K1		SET DO 1 (PROC. RELEASE)	40170	
0	10	1	166	17	0	15		350	000000006			C1U	210		40180	
0	10	1	167	5	0	15		210			CLA	=0000000006		SET DO 2 (PTY ERROR)	40190	
0	10	1	170	5	0	15		264			C1O	210			40200	
0	10	1	171	17	0	15		032			C1O	264			40210	
0	10	1	172	5	0	15		210			CLA	K1		RST DO 2	40220	
0	10	1	173	17	0	15		020			CLA	210			40230	
0	10	1	174	5	0	15		210			CLA	ZERO			40240	
0	10	1	175	1	0	15		1375			PKS	775		RST DO 1	40250	
0	10	1	176	7	0	15		020			ADC	ZERO			40260	
0	10	1	177	5	0	15		154			C1O	154			40270	
0	10	1	200	15	0	15		361	725300000			XOR	=0725300000	1,2,3,5,7,9,11,12	40280	
0	10	1	201	4	0	15		1232			TNZ	L42P3			40290	
0	10	1	202	17	0	15		113		L41P3		CLA	H41P3		40300	
0	10	1	203	13	0	15		070			STO	V1			40310	
0	10	1	204	0	0	15		023			HOP	H9P3			40320	
0	10	1	205	5	0	15		154			C1O	154			40330	
0	10	1	206	4	0	15		1232			TNZ	L42P3			40340	
															40350	
															40370	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 80)

IM	IS	S	LOC	OP	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
C	10	1	207	17	0	15	114			L42P1	CLA	H42P1		40380	
C	10	1	210	13	0	15	1 070			STO	STO	VI		40390	
C	10	1	211	17	0	15	277	000000004		CLA	CLA	=0000000004	SET DC 2	40400	
0	10	1	212	5	0	15	210			CIC	CIC	210		40410	
0	10	1	213	5	C	15	264			CIC	CIC	264		40420	
0	10	1	214	17	0	15	1 020			CLA	CLA	ZERU	RST	40430	
0	10	1	215	5	0	15	210			CIC	CIC	210		40440	
0	10	1	216	1	0	15	1 375			PRS	PRS	775		40450	
0	10	1	217	7	0	15	1 020			ACC	ACC	ZERU		40460	
0	10	1	220	5	0	15	154			CIC	CIC	154		40470	
0	10	1	221	15	0	15	362	525300000		XOR	XOR	=0525300000	1,3,5,7,9,11,12	40480	
0	10	1	222	4	0	15	1 232			L42P3	TNZ	L42P3		40490	
0	10	1	223	17	C	15	115			H42P2	CLA	H42P2		40500	
0	10	1	224	13	0	15	1 070			STO	STO	VI		40510	
0	10	1	226	5	0	15	154			HOP	HOP	H9P3		40520	
0	10	1	227	4	0	15	1 232			CIU	CIU	154		40530	
C	10	1	230	10	0	15	1 242			TNZ	TNZ	L42P3		40540	
C	10	1	231	00	0	15	363	150000310		TRA	TRA*	L43P1	TU ROUTINE 6	40550	
0	10	1	232	13	0	15	1 376			TO ERROR ROUTINE	TRA*	L43P1		40560	
C	10	1	233	13	0	15	1 077			STU	STU	776		40570	
0	10	1	234	17	C	15	1 376			STO	STO	TEMP1		40580	
0	10	1	235	13	0	15	1 071			CLA	CLA	776		40590	
0	10	1	236	0	C	15	1 023			STO	STO	VAR2		40600	
0	10	1	240	00	0	15	364	160000560		HOP	HOP	H9P3		40620	
0	10	1	241	15	C	15	245			CLA	CLA	TEMP1		40630	
0	15	55								L42P4	TRA*	L95P1		40640	
0	15	56								K37P3	XOR	PATN3		40650	
C	15	56								H29P3	HPC	L29P3		40670	
0	15	57								H29P4	HPC	L29P4		40680	
0	15	60								H30P1	HPC	L30P1		40690	
0	15	61								H30P2	HPC	L30P2		40700	
0	15	62								H31P3	HPC	L31P3		40710	
0	15	63								H31P4	HPC	L31P4		40720	
0	15	64								H32P2	HPC	L32P2		40730	
0	15	65								H32P3	HPC	L32P3		40740	
0	15	66								H32P4	HPC	L32P4		40750	
0	15	67								H33P1	HPC	L33P1		40760	
C	15	70								H33P2	HPC	L33P2		40770	
0	15	71								H33P3	HPC	L33P3		40780	
0	15	72								H34P4	HPC	L34P4		40790	
0	15	73								H34P5	HPC	L34P5		40800	
0	15	74								H34P6	HPC	L34P6		40810	
0	15	75								H34P7	HPC	L34P7		40820	
C	15	76								H34P8	HPC	L34P8		40830	
0	15	77								H34P9	HPC	L34P9		40840	
0	15	100								H37P4	HPC	L37P4		40850	
0	15	101								H37P5	HPC	L37P5		40860	
0	15	102								H38P4	HPC	L38P4		40870	
0	15	103								H39P1	HPC	L39P1		40880	
0	15	104								H39P2	HPC	L39P2		40890	
0	15	105								H39P3	HPC	L39P3		40900	
0	15	106								H39P4	HPC	L39P4		40910	
0	15	107								H40P1	HPC	L40P1		40920	
0	15	110								H40P2	HPC	L40P2		40930	
0	15	110								H40P3	HPC	L40P3		40940	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 81)

IM	IS	S	LDC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	15				111				150066300		H41P1	HPC	L41P1		40950	
0	15				112				150070700		H41P2	HPC	L41P2		40960	
0	15				113				150101300		H41P3	HPC	L41P3		40970	
0	15				114				150103700		H42P1	HPC	L42P1		40980	
0	15				115				150111700		H42P2	HPC	L42P2		40990	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 82)

IM	IS	S	LCC	OP	DM	DS	9	ADR	CCT	VAL	LMS	CPC	VARIABLE	COMMENT	SEQ	NO
0	15	116							614300000		PATNI	UCI	614300000	A	PRTR	41010
C	15	117							624300000			UCI	624300000	B		41020
0	15	120							634300000			UCI	634300000	C		41030
0	15	121							644300000			UCI	644300000	D		41040
0	15	122							654300000			UCI	654300000	E		41050
0	15	123							664300000			UCI	664300000	F		41060
0	15	124							674300000			UCI	674300000	G		41070
0	15	125							704300000			UCI	704300000	H		41080
0	15	126							714300000			UCI	714300000	I		41090
0	15	127							414300000			UCI	414300000	J		41100
0	15	130							424300000			UCI	424300000	K		41110
C	15	131							434300000			UCI	434300000	L		41120
0	15	132							444300000			UCI	444300000	M		41130
0	15	133							454300000			UCI	454300000	N		41140
0	15	134							464300000			UCI	464300000	O		41150
0	15	135							474300000			UCI	474300000	P		41160
0	15	136							504300000			UCI	504300000	Q		41170
0	15	137							514300000			UCI	514300000	R		41180
0	15	140							274300000			UCI	274300000	S		41190
C	15	141							234300000			UCI	234300000	T		41200
0	15	142							244300000			UCI	244300000	U		41210
0	15	143							254300000			UCI	254300000	V		41220
0	15	144							264300000			UCI	264300000	W		41230
0	15	145							274300000			UCI	274300000	X		41240
0	15	146							304300000			UCI	304300000	Y		41250
0	15	147							310300000			UCI	310300000	Z		41260
0	15	150							143000000			UCI	143000000	I	BCD	41270
0	15	151							243000000			UCI	243000000	2		41280
0	15	152							343000000			UCI	343000000	3		41290
0	15	153							443000000			UCI	443000000	4		41300
0	15	154							543000000			UCI	543000000	5		41310
0	15	155							643000000			UCI	643000000	6		41320
C	15	156							743000000			UCI	743000000	7		41330
0	15	157							104300000			UCI	104300000	8		41340
0	15	160							114300000			UCI	114300000	9		41350
0	15	161							124300000			UCI	124300000	0		41360
0	15	162							134300000			UCI	134300000	SPCL	CHARS	41370
C	15	163							204300000			UCI	204300000			41380
0	15	164							214300000			UCI	214300000			41390
0	15	165							334300000			UCI	334300000			41400
0	15	166							404300000			UCI	404300000			41410
0	15	167							534300000			UCI	534300000			41420
0	15	170							604300000			UCI	604300000			41430
0	15	171							734300000			UCI	734300000			41440
0	15	172							4300000			UCI	4300000			41450
0	15	173							144300000			UCI	144300000			41460
0	15	174							154300000			UCI	154300000			41470
0	15	175							164300000			UCI	164300000			41480
0	15	176							174300000			UCI	174300000			41490
0	15	177							324300000			UCI	324300000			41500
0	15	200							344300000			UCI	344300000			41510
0	15	201							354300000			UCI	354300000			41520
0	15	202							364300000			UCI	364300000			41530
0	15	203							374300000			UCI	374300000			41540
0	15	204							524300000			UCI	524300000			41550
0	15	205							544300000			UCI	544300000			41560
0	15	206							554300000			UCI	554300000			41570

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 83)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	15							207	564300000			OCT	564300000		41580	
0	15							210	574300000			OCT	574300000		41590	
0	15							211	724300000			OCT	724300000		41600	
0	15							212	744300000			OCT	744300000		41610	
0	15							213	754300000			OCT	754300000		41620	
0	15							214	764300000			OCT	764300000		41630	
0	15							215	774300000			OCT	774300000		41640	
0	15							216	124300000	PATN4		OCT	124300000	END BCD	41650	
0	15							217	130300000			OCT	130300000	0 OCTAL	41660	
0	15							220	120300000			OCT	120300000	1	41670	
0	15							221	134300000			OCT	134300000	2	41680	
0	15							222	160300000			OCT	160300000	3	41690	
0	15							223	174300000			OCT	174300000	4	41700	
0	15							224	164300000			OCT	164300000	5	41710	
0	15							225	170300000			OCT	170300000	6	41720	
0	15							226	121000000	PATN2		OCT	012100000	7	41730	
0	15							227	221000000			OCT	022100000	8	41740	
0	15							230	361000000			OCT	036100000	9	41750	
0	15							231	421000000			OCT	042100000	10	41760	
0	15							232	561000000			OCT	056100000	11	41770	
0	15							233	661000000			OCT	066100000	12	41780	
0	15							234	721000000			OCT	072100000	1	41790	
0	15							235	102100000			OCT	102100000	2	41800	
0	15							236	116100000			OCT	116100000	3	41810	
0	15							237	126100000			OCT	126100000	4	41820	
0	15							240	132100000			OCT	132100000	5	41830	
0	15							241	146100000			OCT	146100000	6	41840	
0	15							242	416100000			OCT	416100000	7	41850	
0	15							243	426100000			OCT	426100000	8	41860	
0	15							244	432100000			OCT	432100000	9	41870	
0	15							245	612100000	* PATN3		SKIP	612100000	1	41880	
0	15							246	622100000			OCT	622100000	2	41890	
0	15							247	636100000			OCT	636100000	3	41900	
0	15							250	642100000			OCT	642100000	4	41910	
0	15							251	656100000			OCT	656100000	5	41920	
0	15							252	666100000			OCT	666100000	6	41930	
0	15							253	672100000			OCT	672100000	7	41940	
0	15							254	702100000			OCT	702100000	8	41950	
0	15							255	716100000			OCT	716100000	9	41960	
0	15							256	726100000			OCT	726100000	10	41970	
0	15							257	732100000			OCT	732100000	11	41980	
0	15							260	746100000			OCT	746100000	12	41990	
0	15							261	216100000	* SPACE	AFTER PRINT	OCT	216100000	1	42010	
0	15							262	226100000			OCT	226100000	2	42020	
0	15							263	232100000			OCT	232100000	3	42030	
															42040	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 84)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OC	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NC
0	10	1	242	13	0	15	1	376			* L43P1	STC	RESTORE		42060	
0	10	1	243	17	0	15	1	376				STC	ORIGINAL		42070	
0	10	1	244	13	0	15	1	103				STC	INSTRUCTIONS		42080	
0	10	1	245	16	0	10	210					STC	776		42090	
0	10	1	246	17	0	10	370					STC	HRTN		42100	
0	10	1	247	13	0	10	1	076				STC	O*10		42110	
0	10	1	250	17	0	10	1	40				STC	K31P1		42120	
0	10	1	251	00	0	10	376		160000160			STC	TEMP		42130	
0	10	1	252	13	0	10	140					STC	L31P1		42140	
0	10	1	253	17	0	10	371					STC	L1P1C		42150	
0	10	1	254	13	0	10	1	076				STC	L31P1		42160	
0	10	1	255	17	0	10	1	43				STC	K31P2		42170	
0	10	1	256	00	0	10	376		160000360			STC	TEMP		42180	
0	10	1	257	13	0	10	143					STC	L31P2		42190	
0	10	1	260	16	0	11	211					STC	L1P1C		42200	
0	10	1	261	17	0	11	344					STC	L31P2		42210	
0	10	1	262	13	0	11	1	076				STC	L1P1C		42220	
0	10	1	263	17	0	11	276					STC	O*11		42230	
0	10	1	264	00	0	11	345					STC	K35P4		42240	
0	10	1	265	13	0	11	276		160000360			STC	TEMP		42250	
0	10	1	266	16	0	10	210					STC	L35P4		42260	
0	10	1	267	17	0	10	241					STC	L1P1C		42270	
0	10	1	270	13	0	10	1	076				STC	O*10		42280	
0	10	1	271	17	0	10	014					STC	K37P3		42290	
0	10	1	272	10	0	10	1	275				STC	TEMP		42300	
0	10	1	273	13	0	10	014					STC	L37P3		42310	
0	10	1	274	0	0	10	1	103				STC	L43P2		42320	
0	10	1	275	13	0	10	1	376				STC	HCP		42330	
0	10	1	276	6	0	10	1	040				STC	HRTN		42340	
0	10	1	277	13	0	10	1	077				STC	SYLLABLE		42350	
0	10	1	300	17	0	10	1	076				STC	I		42360	
0	10	1	301	6	0	10	1	045				STC	INSTRUCTION		42370	
0	10	1	302	15	0	10	1	077				STC	REMOVE		42380	
0	10	1	303	0	0	10	1	376				STC	ADDRESS		42390	
												STC	KEEP		42400	
												STC	ADDRESS		42410	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 85)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	11	1	0	0	15	264							BEGINNING OF ROUTINE SIX		42430	
0	11	1	0	17	0	15	1	061					EXCHANGE CALCOMP DIGITAL		42440	
0	11	1	1	14	0	15	1	005			L45P1	CLA	11,1,1,1,15,		42450	
0	11	1	2	4	0	15	1	004					INCREMENTAL PLOTTER		42460	
0	11	1	3	00	0	15	327								42470	
0	11	1	4	00	0	15	365		130007000						42480	
0	11	1	5	17	0	15	264								42500	
0	11	1	6	13	0	15	1	070							42510	
0	11	1	7	17	0	15	265								42520	
0	11	1	10	13	0	15	1	071		110000110	H50P1	HPC			42530	
0	11	1	11	17	0	15	1	032							42540	
0	11	1	12	5	0	15	150								42550	
0	11	1	13	10	0	15	1	126							42560	
0	11	1	14	5	0	15	214								42570	
0	11	1	15	6	0	15	270								42580	
0	11	1	16	4	0	15	1	043							42590	
0	11	1	17	13	0	15	1	073							42600	
0	11	1	20	17	0	15	266								42610	
0	11	1	21	5	0	15	267		400003774				RAISE PEN		42620	
0	11	1	22	10	0	15	1	264		400001774	KMAXM	CTI	DELAY 0.11 SEC		42630	
0	11	1	23	5	0	15	214								42640	
0	11	1	24	6	0	15	270								42650	
0	11	1	25	4	0	15	1	043							42660	
0	11	1	26	17	0	15	270								42670	
0	11	1	27	5	0	15	150								42680	
0	11	1	30	10	0	15	1	126							42690	
0	11	1	31	5	0	15	214								42700	
0	11	1	32	6	0	15	270								42710	
0	11	1	33	4	0	15	1	043							42720	
0	11	1	34	17	0	15	271								42730	
0	11	1	35	5	0	15	140		3774						42740	
0	11	1	36	17	0	15	1	020	1774						42750	
0	11	1	37	5	0	15	144								42760	
0	11	1	40	5	0	15	214								42770	
0	11	1	41	6	0	15	270								42780	
0	11	1	42	4	0	15	1	051							42790	
0	11	1	43	13	0	15	1	376							42800	
0	11	1	44	13	0	15	1	076							42810	
0	11	1	45	17	0	15	1	376							42820	
0	11	1	46	13	0	15	1	073							42830	
0	11	1	47	17	0	15	1	076							42840	
0	11	1	50	0	0	15	1	026							42850	
0	11	1	51	10	0	15	1	264							42860	
0	11	1	52	17	0	15	272								42870	
0	11	1	53	5	0	15	144								42880	
0	11	1	54	10	0	15	1	271							42890	
0	11	1	55	17	0	15	273								42900	
0	11	1	55	17	0	15	273		776		L45P5	CLA			42910	
											KHP	CTI			42920	
															42930	
															42940	
															42950	
															42960	
															42970	
															42980	
															42990	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 86)

IM	IS	S	LDC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	11	1	56	5	0	15	140					CIC	L4C	DRUM DOWN	43000	
0	11	1	57	17	0	15	274					CLA	KHM		43010	
									400000776		KHM	OC1	400000776		43020	
0	11	1	60	5	0	15	144					CIC	L44	CARR RIGHT	43030	
0	11	1	61	10	0	15	1276					TRA	L47P5		43040	
0	11	1	62	17	0	15	274					CLA	KHM	DRUM UP	43050	
0	11	1	63	5	0	15	140					CIC	L40		43060	
0	11	1	64	17	0	15	274					CLA	KHM	CARR RIGHT	43070	
0	11	1	65	5	0	15	144					CIC	L44		43080	
0	11	1	66	10	0	15	1276					TRA	L47P5		43090	
0	11	1	67	17	0	15	267					CLA	KMAXM	DRUP UP	43100	
0	11	1	70	5	0	15	140					CIC	L40		43110	
0	11	1	71	17	0	15	272					CLA	KMAXP	CARR LEFT	43120	
0	11	1	72	5	0	15	144					CIC	L44		43130	
0	11	1	73	10	0	15	1271					TRA	L47P4		43140	
0	11	1	74	17	0	15	267					CLA	KMAXM	CARR RIGHT	43150	
0	11	1	75	5	0	15	144					CIC	L44		43160	
0	11	1	76	10	0	15	1271					TRA	L47P4		43170	
0	11	1	77	17	0	15	272					CLA	KMAXP	DRUM DOWN	43180	
0	11	1	100	5	0	15	140					CIC	L40	CARR LEFT	43190	
0	11	1	101	5	0	15	144					CIC	L44		43200	
0	11	1	102	10	0	15	1271					TRA	L47P4	DRUM UP	43210	
0	11	1	103	17	0	15	267					CLA	KMAXM		43220	
0	11	1	104	5	0	15	140					CIC	L40		43230	
0	11	1	105	17	0	15	1270					CLA	ZERO		43240	
0	11	1	106	5	0	15	144					CIC	L44		43250	
0	11	1	107	10	0	15	1271					TRA	L47P4		43260	
0	11	1	110	17	0	15	1032					CLA	K1	RAISE PEN	43270	
0	11	1	111	5	0	15	150					CIC	L50	CARR RIGHT	43280	
0	11	1	112	17	0	15	274					CLA	KHM		43290	
0	11	1	113	5	0	15	144					CIC	L44		43300	
0	11	1	114	10	0	15	1276					TRA	L47P5		43310	
0	11	1	115	17	0	15	273					CLA	KHP	DRUM DOWN	43320	
0	11	1	116	5	0	15	140					CIC	L40		43330	
0	11	1	117	17	0	15	1020					CLA	ZERU		43340	
0	11	1	120	5	0	15	144					CIC	L44		43350	
0	11	1	121	10	0	15	1276					TRA	L47P5		43360	
0	11	1	122	17	0	15	270					CLA	K2		43370	
0	11	1	123	5	0	15	150					CIC	L50	LOWER PEN	43380	
0	11	1	124	10	0	15	126					TRA	L47P1B	DELAY 0.11 SEC	43390	
0	11	1	125	10	0	15	133					TRA	L47P1C		43400	
0	11	1	126	13	0	15	1377					STC	777		43410	
0	11	1	127	17	0	15	366		000002466			CLA	=0000002466	DELAY 110 MSEC.	43420	
0	11	1	130	2	0	15	1032					SUB	K1		43430	
0	11	1	131	4	0	15	1130					TNZ	L47P1A		43440	
0	11	1	132	0	0	15	1377					HOP	777		43450	
0	11	1	133	17	0	15	275		150051310			HPC	H47P1		43460	
0	11	1	134	13	0	15	1070					STC	VANL		43470	
0	11	1	135	17	0	15	276					CLA	H47P2		43480	
									150061310		H47P2	HPC	H47P2		43490	
0	11	1	136	13	0	15	1071					STC	L47P2	CARR RIGHT	43500	
0	11	1	137	5	0	15	214					CIC	VAR2		43510	
0	11	1	140	6	0	15	270					ANL	K2		43520	
0	11	1	141	4	0	15	1043					TNZ	L45P3A		43530	
0	11	1	142	17	0	15	274					CLA	KHM		43540	
0	11	1	143	5	0	15	144					CIC	L44	CARR RIGHT	43550	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 87)

IM	IS	S	LOC	UP	DM	OS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
0	11	1	144	10	0	15	1	276				TRA	L47P5		43570	
0	11	1	145	17	0	15	1	032				CLA	K1		43580	
0	11	1	146	5	0	15	150					CIC	150	RAISE PEN	43590	
0	11	1	147	17	0	15	367		000002260			CLA	=0000002260	600 DEC.	43600	
0	11	1	150	5	0	15	140					CIC	140	DRUM DOWN	43610	
0	11	1	151	17	0	15	370		000002400			CLA	=0000002400	640 DEC.	43620	
0	11	1	152	5	0	15	144					CIC	144	CARR. LEFT	43630	
0	11	1	153	17	0	15	354		000000014			CLA	=0000000014		43640	
0	11	1	154	13	0	15	101					STU	CTR	WAIT	43650	
0	11	1	155	10	0	15	1303				L48P2	TRA	L48P1	LOWER PEN	43660	
0	11	1	156	17	0	15	270					CLA	K2		43670	
0	11	1	157	5	0	15	150					CIO	150		43680	
0	11	1	160	10	0	15	1303					TRA	L48P1	WAIT	43690	
0	11	1	161	17	0	15	270					CLA	K2	DRUM DOWN 2	43700	
0	11	1	162	5	0	15	140					CIC	140		43710	
0	11	1	163	17	0	15	020					CLA	ZEMO		43720	
0	11	1	164	5	0	15	144					CIC	144		43730	
0	11	1	165	10	0	15	1303					TRA	L48P1		43740	
0	11	1	166	17	0	15	032					CLA	K1		43750	
0	11	1	167	5	0	15	150					CIC	150	RAISE PEN	43760	
0	11	1	170	10	0	15	1303		400000010			TRA	L48P1	DRUM UP 4	43770	
0	11	1	171	17	0	15	371					CLA	=0400000010		43780	
0	11	1	172	5	0	15	140					CIO	140		43790	
0	11	1	173	17	0	15	020					CLA	ZEMO		43800	
0	11	1	174	5	0	15	144					CIC	144		43810	
0	11	1	175	10	0	15	1303					TRA	L48P1	LOWER PEN	43820	
0	11	1	176	17	0	15	270					CLA	K2		43830	
0	11	1	177	5	0	15	150					CIO	150		43840	
0	11	1	200	10	0	15	1303					TRA	L48P1	CARR. RIGHT 2	43850	
0	11	1	201	17	0	15	372		400000004			CLA	=0400000004		43860	
0	11	1	202	5	0	15	144					CIO	144		43870	
0	11	1	203	10	0	15	1303					TRA	L48P1		43880	
0	11	1	204	17	0	15	032					CLA	K1	RAISE PEN	43890	
0	11	1	205	5	0	15	150					CIC	150		43900	
0	11	1	206	10	0	15	1303					TRA	L48P1		43910	
0	11	1	207	17	0	15	021					CLA	BB	CARR LEFT 4	43920	
0	11	1	210	5	0	15	144					CIC	144		43930	
0	11	1	211	17	0	15	101					CLA	CTR		43940	
0	11	1	212	2	0	15	032					SUB	K1		43950	
0	11	1	213	13	0	15	101					STU	CTR		43960	
0	11	1	214	4	0	15	155					TNZ	L48P2		43970	
0	11	1	215	10	0	15	1303					TRA	L48P1	WAIT	43980	
0	11	1	216	17	0	15	270					CLA	K2	LOWER PEN	43990	
0	11	1	217	5	0	15	150					CIC	150		44000	
0	11	1	220	17	0	15	354		000000014			CLA	=0000000014		44010	
0	11	1	221	13	0	15	101					STU	CTR		44020	
0	11	1	222	10	0	15	1303				L48P3	TRA	L48P1	WAIT	44030	
0	11	1	223	17	0	15	270					CLA	K2	DRUM DOWN 2	44040	
0	11	1	224	5	0	15	140					CIC	140		44050	
0	11	1	225	5	0	15	144					CIC	144	CARR LEFT 2	44060	
0	11	1	226	10	0	15	1303					TRA	L48P1	WAIT	44070	
0	11	1	227	17	0	15	372		400000004			CLA	=0400000004	DRUM UP 2	44080	
0	11	1	230	5	0	15	140					CIC	140		44090	
0	11	1	231	17	0	15	270					CLA	K2	CARR LEFT 2	44100	
0	11	1	232	5	0	15	144					CIC	144		44110	
0	11	1	233	10	0	15	1303					TRA	L48P1	CARR LEFT 2	44120	
0	11	1	234	17	0	15	372		400000004			CLA	=0400000004	WAIT	44130	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 88)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
0	11	1	235	5	0	15		140				CIC	L40			44140
0	11	1	236	5	0	15		144				CIC	L44	DRUM UP 2		44150
0	11	1	237	10	0	15		1303				TRA	L48P1	CARR RIGHT 2		44160
0	11	1	240	17	0	15		372	400000004			CLA	=04GG0C004	WAIT		44170
0	11	1	241	5	0	15		140				CIC	L40	DRUM UP 2		44180
0	11	1	242	17	0	15		270				CLA	K2	CARR LEFT 2		44190
0	11	1	243	5	0	15		144				CIC	L44			44200
0	11	1	244	17	0	15		101				CLA	CTR			44210
0	11	1	245	2	0	15		032				SUB	K1			44220
0	11	1	246	13	0	15		101				STU	CTR			44230
0	11	1	247	4	0	15		222				FNZ	L48PJ			44240
0	11	1	250	10	0	15		303				TRA	L48P1			44250
0	11	1	251	17	0	15		032				CLA	K1	WAIT		44260
0	11	1	252	5	0	15		150				CIC	L50	RAISE PEN		44270
0	11	1	253	10	0	15		1303				TRA	L48P1	WAIT		44280
0	11	1	254	17	0	15		035				CLA	K324	424 DECIMAL		44290
0	11	1	255	5	0	15		144				CIC	L44	GENERATED TRANSFER		44300
0	11	1	256	10	0	15		260				TRA**				44310
0	11	1	260	10	0	15		303				TRA	L48P1	WAIT		44320
0	11	1	261	00	0	15		365	110000110			TRA*	L50P1			44330
0	11	1	264									ORG	=11,1,264,,15.			44340
0	11	1	264	13	0	15		376			L47P3	CLA	=000131002	DELAY 3.76 SEC.		44350
0	11	1	265	17	0	15		373	000131002			CLA	K1			44360
0	11	1	266	2	0	15		032			L47P3A	SUB				44370
0	11	1	267	4	0	15		1266				TRZ	L47P3A			44380
0	11	1	270	0	0	15		1376			HOP	776				44390
0	11	1	271	13	0	15		376			L47P4	STC				44400
0	11	1	272	17	0	15		374			L47P4A	CLA	=000054402	DELAY 1.88 SEC.		44410
0	11	1	273	2	0	15		032	000054402			SUB	K1			44420
0	11	1	274	4	0	15		1273			L47P4A	TRZ	L47P4A			44430
0	11	1	275	0	0	15		1376			HOP	776				44440
0	11	1	276	13	0	15		376			L47P5	STO				44450
0	11	1	277	17	0	15		377			L47P5A	CLA	=000026202	DELAY .94 SEC.		44460
0	11	1	300	2	0	15		032	000026202			SUB	K1			44470
0	11	1	301	4	0	15		1300			L47P5A	TRZ	L47P5A			44480
0	11	1	302	0	0	15		1376			HOP	776				44490
0	11	1	303	13	0	15		1376			L48P1	STO		WAIT FOR READY		44500
0	11	1	304	5	0	15		214				CIC	214			44510
0	11	1	305	6	0	15		270			ANL	K2				44520
0	11	1	306	4	0	15		1304			**	TRZ	**			44530
0	11	1	307	0	0	15		1376			HOP	776				44540

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 89)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	11	0	0	0	11	0	11	260					BEGINNING OF ROUTINE SEVEN		44550	
0	11	0	0	17	0	11	1	062					EXERCISE TYPEWRITER		44560	
0	11	0	1	14	C	11	012				L50P1	ORG	,11,*,*11,260		44570	
0	11	0	2	4	0	11	136					CLA	L50P2		44580	
0	11	0	3	00	0	11	346		130007000			TMI	L60P1		44590	
												TNZ	L2P1		44600	
												TRA*	L2P1		44610	
0	11	0	4	17	0	11	1	234				SET RIGHT MARGIN BETWEEN 120 AND 124		44620		
0	11	0	5	17	0	11	1	244				SET LEFT MARGIN AT C		44630		
0	11	0	6	17	C	11	1	254				SET TAB AT 10		44640		
0	11	0	7	17	0	11	1	266			KL1	CLA	LINE1		44650	
0	11	0	10	17	0	11	1	300			KL2	CLA	LINE2		44660	
0	11	0	11	17	0	11	1	307			KL3	CLA	LINE3		44670	
0	11	0	12	00	0	11	1	347			KL4	CLA	LINE4		44680	
0	11	0	13	10	0	11	1	107			KL5	CLA	LINE5		44690	
0	11	0	14	5	0	11	1	214			KL6	CLA	LINE6		44700	
0	11	0	15	6	0	11	1	021			L50P2	TRA*	L98P4	CARR RTN	44710	
0	11	0	16	4	0	11	1	014		160064760		TRA	L52P1	TAB	44720	
0	11	0	17	17	0	11	1	350				CIC	214		44730	
0	11	0	20	5	0	11	1	134		200000000		ANC	88		44740	
0	11	0	21	17	0	11	1	351				TNZ	*-2		44750	
0	11	0	22	13	0	11	1	100		000000020		CLA	=D200000000	SET BLACK RIBBON	44760	
0	11	0	23	17	0	11	1	004				CIC	134		44770	
0	11	0	24	00	0	11	1	352				CLA	=0000000020		44780	
0	11	0	25	00	0	11	1	347				STC	STOP		44790	
0	11	0	26	00	0	11	1	353				STC	STOP		44800	
0	11	0	27	10	0	11	1	107				CLA	KL1		44810	
0	11	0	30	17	0	11	1	351		160065160	L50P3	TRA*	L98P3	TYPE LINE 1	44820	
0	11	0	31	13	0	11	1	100		160064760		TRA*	L98P4	CARR RTN	44830	
0	11	0	32	17	0	11	0	005		160070360		TRA*	L52P1	INDEX	44840	
0	11	0	33	00	C	11	1	352				TRA*	L52P1	TAB	44850	
0	11	0	34	00	0	11	1	347				CLA	=0000000020		44860	
0	11	0	35	00	0	11	1	353				STU	STOP		44870	
0	11	0	36	10	0	11	1	107		000000024		CLA	KL2		44880	
0	11	0	37	17	0	11	1	107				CLA	KL3		44890	
0	11	0	40	13	0	11	1	100		160065160	L50P4	TRA*	L98P3	TYPE LINE 2	44900	
0	11	0	41	17	0	11	1	006		160064760		TRA*	L98P4	CARR RTN	44910	
0	11	0	42	00	C	11	1	352		160070360		TRA*	L98P5	INDEX	44920	
0	11	0	43	17	0	11	1	355		000000024		TRA*	L52P1	TAB	44930	
0	11	0	44	00	0	11	1	356				CLA	=0000000024		44940	
0	11	0	45	10	0	11	1	107				STU	STOP		44950	
0	11	0	46	17	0	11	1	357		160065160	L51P1	TRA*	L98P3	TYPE LINE 3	44960	
0	11	0	47	13	0	11	1	100		000000240		CLA	=0000000240	80 SPACES	44970	
0	11	0	50	17	C	11	0	007		160044760		TRA*	L98P1	SPACE	44980	
0	11	0	51	00	0	11	1	352				TRA*	L98P4	SHOULD HIT RIGHT MARGIN AND EXECUTE AUTOMATIC CARRIAGE RETURN	44990	
0	11	0	52	00	0	11	1	347				TRA*	L98P5	AND COMPLETE SPACING	45000	
0	11	0	53	00	C	11	1	353				TRA*	L52P1		45010	
0	11	0	54	10	0	11	1	107				CLA	KL4		45020	
0	11	0	55	17	0	11	1	360		000000014	L51P2	TRA*	L98P3	TYPE LINE 4	45030	
0	11	0	56	13	C	11	1	010				TRA*	L98P4	CARR RTN	45040	
0	11	0	57	17	0	11	1	010				TRA*	L98P5	INDEX	45050	
0	11	0	60	00	C	11	1	352		160065160		CLA	=0000000014	TAB	45060	
												STU	STOP		45070	
												CLA	KL5		45080	
												TRA*	L98P3	TYPE 1ST PART LINE 5	45090	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 90)

IM	IS	S	LOC	UP	DM	DS	9	ADR	CCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NC
0	11	0	61	17	0	11	1	306				CLA	LINESA		45120	
0	11	0	62	00	0	11	1	361	160052760			TRA*	L98P2		45130	
0	11	0	63	00	C	11	347		160064760		L51P3	TRA*	L98P4	CARR RTN	45140	
0	11	0	64	00	0	11	353		160070360			TRA*	L98P5	INDEX	45150	
0	11	0	65	10	0	11	107					CLA	L52P1	TAR	45160	
0	11	0	66	17	0	11	357		000000016			CLA	=0C00000016		45170	
0	11	0	67	13	0	11	100					STO	STOP		45180	
0	11	0	70	17	0	11	011					CLA	KL6		45190	
0	11	0	71	00	0	11	352		160065160			TRA*	L98P3	TYPE 1ST PART LINE 6	45200	
0	11	0	72	5	0	11	214					CIC	214		45210	
C	11	0	73	6	0	11	021					ANC	PH		45220	
C	11	0	74	4	0	11	072					TNZ	*-2		45230	
0	11	0	75	17	0	11	362		100000000			CLA	=01CCCC0000	SET RED RIBBON	45240	
0	11	0	76	5	0	11	134					CIC	I34		45250	
0	11	0	77	17	0	11	363		000000006			CLA	=0000000006	SPACE 3	45260	
0	11	0	100	0C	C	11	356		160044760			TRA*	L98P1	TYPE 2ND PART LINE 6	45280	
0	11	0	101	17	0	11	116					CLA	LINESA		45290	
0	11	0	102	10	0	11	116					TRA	L52P2		45300	
0	11	0	103	17	C	11	320					CLA	LINE6B		45310	
0	11	0	104	10	0	11	116					TRA	L52P2		45320	
0	11	0	105	00	C	11	347		160064760			TRA*	L98P4	CARR RTN	45330	
0	11	0	106	10	0	11	136					TRA	L60P1		45350	
0	11	0	107	13	C	11	1376					TRA CONTROL			45360	
0	11	0	110	5	0	11	214				L52P1	STG	776		45370	
0	11	0	111	6	0	11	021					ANC	PH		45380	
0	11	0	112	4	0	11	110					TNZ	*-2		45390	
0	11	0	113	17	0	11	364		010000000			CLA	=0010000000		45400	
0	11	0	114	5	0	11	134					CIC	I34		45410	
0	11	0	115	0	0	11	1376					HCP	776		45420	
0	11	0	116	13	0	11	1376					TYPE DECIMAL NUMBER			45440	
0	11	0	117	13	0	11	076				L52P2	STG	776		45450	
0	11	0	120	17	0	11	360		000000014			CLA	TEMP		45460	
0	11	0	121	13	0	11	100					STO	=0000000014		45470	
0	11	0	122	5	0	11	214				L52P2A	CIC	214		45480	
0	11	0	123	6	0	11	021					ANC	PH		45490	
0	11	0	124	4	0	11	122					TNZ	*-2		45500	
0	11	0	125	17	0	11	076					CLA	TEMP		45510	
0	11	0	126	5	0	11	124					CIC	I24		45520	
0	11	0	127	16	0	11	010					SHL	4		45530	
0	11	0	130	13	C	11	1076					STO	TEMP		45540	
0	11	0	131	17	0	11	100					CLA	STOP		45550	
0	11	0	132	2	0	11	032					SUB	KL1		45560	
0	11	0	133	13	0	11	100					STO	STOP		45570	
0	11	0	134	4	C	11	122					TNZ	L52P2A		45580	
0	11	0	135	0	0	11	1376					HOP	776		45590	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 91)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	4	1	136	17	0	11	1	063			*		BEGINNING OF ROUTINE EIGHT	45620		
0	4	1	137	14	0	11	1	142			*		EXERCISE PRINTER	45630		
0	4	1	140	4	0	11	1	143			L60P1	CLA	LCRB	45640		
0	4	1	141	00	0	11	1	346				TNZ	L60P2B	45650		
0	4	1	142	00	0	11	1	365	130007000			TRA*	NAB1B	45660		
0	4	1	143	00	0	11	1	366	050001240			TRA*	L2P1	45670		
0	4	1	2	0	5	11	11		531020270			ORG	L60P2	45680		
0	4	1	2	17	0	5	1	136			L60P2	CLA	*4,1,2,*,5,11	45700		
0	4	1	3	5	0	5	1	160				C10	C26	45710		
0	4	1	4	17	0	5	1	020				CLA	160	45720		
0	4	1	5	13	0	5	1	000				CLA	ZERO	45730		
0	4	1	6	13	0	5	1	102				STC	CTR2	45740		
0	4	1	7	13	0	5	1	001				STC	CTR3	45750		
0	4	1	10	10	0	5	1	233				STC	PGNR	45760		
0	4	1	11	17	0	5	1	020			L60P2A	CLA	L61P5	45770		
0	4	1	12	13	0	5	1	101				STC	ZERO	45780		
0	4	1	13	13	0	5	1	002				STC	CTR	45790		
0	4	1	14	17	0	5	1	001				STC	CTR1	45800		
0	4	1	15	17	0	5	1	004				CLA	PGNR	45810		
0	4	1	16	13	0	5	1	001	000001000			ADD	=0000001	45820		
0	4	1	17	5	0	5	1	214				STC	PGNR	45830		
0	4	1	20	6	0	5	1	032				C10	214	45840		
0	4	1	21	4	0	5	1	017				ANC	K1	45850		
0	4	1	22	5	0	5	1	170			*	TNZ	**2	45860		
0	4	1	23	17	0	5	1	005				C10	170	45870		
0	4	1	24	13	0	5	1	100	000000024			CLA	SET BCD MODE	45880		
0	4	1	25	1	0	5	1	020			L60P2J	STC	TEN	45890		
0	4	1	26	17	0	5	1	100				STC	STC	45900		
0	4	1	27	2	0	5	1	032				CLA	ZERO	45910		
0	4	1	30	4	0	5	1	024				CLA	STOP	45920		
0	4	1	31	1	0	5	1	234				SUB	KL	45930		
0	4	1	32	1	0	5	1	235				TNZ	L60P2J	45940		
0	4	1	33	1	0	5	1	236				PRC	KK	45950		
0	4	1	34	1	0	5	1	237				PRC	KK+1	45960		
0	4	1	35	1	0	5	1	240				PRC	KK+2	45970		
0	4	1	36	1	0	5	1	241				PRC	KK+3	45980		
0	4	1	37	1	0	5	1	242				PRC	KK+4	45990		
0	4	1	40	1	0	5	1	243				PRC	KK+5	46000		
0	4	1	41	1	0	5	1	244				PRC	KK+6	46010		
0	4	1	42	17	0	5	1	006				PRC	KK+7	46020		
0	4	1	43	13	0	5	1	100	000000020			CLA	=0000C00020	46030		
0	4	1	44	1	0	5	1	020			L60P2C	STC	STOP	46040		
0	4	1	45	17	0	5	1	100				PRC	ZERO	46050		
0	4	1	46	2	0	5	1	032				CLA	STOP	46060		
0	4	1	47	4	0	5	1	043				SUB	KL	46070		
0	4	1	50	1	0	5	1	245				TNZ	L60P2C	46080		
0	4	1	51	1	0	5	1	246				PRC	KL	46090		
0	4	1	52	17	0	5	1	001				PRC	KL+1	46100		
0	4	1	53	2	0	5	1	007	000012000			CLA	PGNR	46110		
0	4	1	54	14	0	5	1	101				SUB	=0C00012	46120		
0	4	1	55	17	0	5	1	001				TMI	L60P2E	46130		
0	4	1	56	2	0	5	1	011	00002*000			CLA	PGNR	46140		
0	4	1	57	14	0	5	1	103				SUB	=0000024	46150		
0	4	1	58	4	0	5	1	062				TMI	L60P2F	46160		
0	4	1	60	4	0	5	1	062				TNZ	**2	46170		
0	4	1	61	4	0	5	1	062				TNZ	**2	46180		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 92)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NC
0	4	1	61	17	0	5	007	000012000				CLA	=0000012		46190	
0	4	1	62	15	0	5	250	000200000			L60P2C	XDR	=00002	1ST DIGIT = 2	46200	
0	4	1	63	1	0	5	375					PRS	775		46210	
0	4	1	64	17	0	5	001					CLA	PGNR		46220	
0	4	1	65	2	0	5	251	000013000				SUB	=0000013	= 11	46230	
0	4	1	66	14	0	5	111					TH1	L60P2C		46240	
0	4	1	67	13	0	5	076					TH1	TEMP		46250	
0	4	1	70	2	0	5	007	000012000				SUB	=0000012	TEN	46260	
0	4	1	71	14	0	5	123					TH1	L60P2H		46270	
0	4	1	72	1	0	5	374					PRS	774		46280	
0	4	1	73	5	0	5	214					C10	214		46290	
0	4	1	74	6	0	5	032					ANC	K1		46300	
0	4	1	75	4	0	5	073					TNZ	*-2		46310	
0	4	1	76	17	0	5	252	130000000				CLA	=013	IMMED SKIP CH 11	46320	
0	4	1	77	5	0	5	160					C10	160		46330	
0	4	1	100	10	0	5	133					TRA	L60P3		46340	
0	4	1	101	17	0	5	001				L60P2E	CLA	PGNR		46350	
0	4	1	102	10	0	5	063					TRA	L60P2U		46360	
0	4	1	103	17	0	5	001				L60P2F	CLA	PGNR		46370	
0	4	1	104	2	0	5	007	000012000				SUB	=0000012	TEN	46380	
0	4	1	105	4	0	5	107					TNZ	*+2		46390	
0	4	1	106	17	0	5	007	000012000				CLA	=0000012		46400	
0	4	1	107	15	0	5	253	000100000				XDR	=00001		46410	
0	4	1	110	10	0	5	1063					TRA	L60P2D		46420	
0	4	1	111	1	0	5	374				L60P2G	PRS	774		46430	
0	4	1	112	5	0	5	214					C10	214		46440	
0	4	1	113	6	0	5	032					ANC	K1		46450	
0	4	1	114	4	0	5	112					TNZ	*-2		46460	
0	4	1	115	17	0	5	001					CLA	PGNR		46470	
0	4	1	116	7	0	5	004	000001000				ACC	=0000001		46480	
0	4	1	117	16	0	5	040					SHL	12		46490	
0	4	1	120	16	0	5	040					C10	160	IMMED SKIP CH 2- 11	46500	
0	4	1	121	5	0	5	160					TRA	L60P3		46510	
0	4	1	122	10	0	5	133				L60P2H	CLA	FEMP		46520	
0	4	1	123	17	0	5	076	000002000				ADD	=0000002		46530	
0	4	1	124	7	0	5	254					SHL	12		46540	
0	4	1	125	16	0	5	040					XDR	=06	SKIP AFTER PRINT CH 2-11	46550	
0	4	1	126	16	0	5	040					C10	160		46560	
0	4	1	127	15	0	5	255	600000000				PRS	774		46570	
0	4	1	130	5	0	5	160					TRA	L60P3		46580	
0	4	1	131	1	0	5	374					C10	214		46590	
0	4	1	132	10	0	5	133				L60P3	ANE	K1	CHECK PRINTER READY	46600	
0	4	1	133	5	0	5	214					TNZ	L60P3		46610	
0	4	1	134	6	0	5	032				L60P3A	PRS	KA		46620	
0	4	1	135	4	0	5	133					CLA	CTR1		46630	
0	4	1	136	1	0	5	012					ADD	KS1		46640	
0	4	1	140	7	0	5	036					STO	CTR1		46650	
0	4	1	141	13	0	5	002					CES	0.4		46660	
0	4	1	142	16	0	5	204					CLA	L60P3A		46670	
0	4	1	143	17	0	5	136					ADD	KS1		46680	
0	4	1	144	7	0	5	036					STC	L60P3A		46690	
0	4	1	145	13	0	5	136					CES	0.5		46700	
0	4	1	146	16	0	5	205					CLA	CTR		46710	
0	4	1	147	17	0	5	101									

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 93)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	4	1	150	7	C	5	1	036				ADC	KSI		46720	
0	4	1	151	13	0	5	1	101				STO	CTR		46730	
0	4	1	152	2	0	5	1	141				SUB	C29	= 16	46740	
0	4	1	153	4	C	5	1	156			L60P5	TNZ	L60P5		46750	
0	4	1	154	13	0	5	1	101			L60P4	STC	CTR		46760	
0	4	1	155	10	0	5	1	233				TRA	L61P5		46770	
0	4	1	156	17	C	5	0	02			L60P5	CLA	CTR1		46780	
0	4	1	157	2	0	5	256		0740000000			SUB	=0074000000	= 30	46790	
0	4	1	160	4	0	5	1	133			L61P1	TNZ	L60P3		46800	
0	4	1	161	13	0	5	0	02				STO	CTR1		46810	
0	4	1	162	1	0	5	1	374				PRS	774	PRINT LINE	46820	
0	4	1	163	5	C	5	214				C10	214	214		46830	
0	4	1	164	6	0	5	1	032			ANC	K1	K1		46840	
0	4	1	165	4	0	5	1	163			TNZ	*-2	*-2		46850	
0	4	1	166	17	0	5	0	00			CLA	CTR2	CTR2		46860	
0	4	1	167	17	0	5	1	036			ADC	KSI	KSI		46870	
0	4	1	170	13	0	5	0	00			STO	CTR2	CTR2		46880	
0	4	1	171	2	0	5	257		0160000000			SUR	=0016000000	= 7	46890	
0	4	1	172	14	0	5	1	175			TMI	L61P1C	L61P1C		46900	
0	4	1	173	4	0	5	1	221			TNZ	L61P4	L61P4		46910	
0	4	1	174	10	0	5	1	213			TRA	L61P2A	L61P2A		46920	
0	4	1	175	17	0	5	0	00			L61P1C	CLA	CTR2		46930	
0	4	1	176	6	0	5	1	136			C26	C26	C26	= 0100000000	46940	
0	4	1	177	4	0	5	1	205			TNZ	L61P1A	L61P1A		46950	
0	4	1	200	17	C	5	0	00			CLA	CTR2	CTR2		46960	
0	4	1	201	16	0	5	0	02			SHL	2	2		46970	
0	4	1	202	15	0	5	1	154			XOR	C40	C40		46980	
0	4	1	203	5	0	5	1	160			C10	160	160	SPACE	46990	
0	4	1	204	10	0	5	1	133			TRA	L60P3	L60P3		47000	
0	4	1	205	17	0	5	0	00			L61P1A	CLA	CTR2		47010	
0	4	1	206	2	0	5	260		0060000000			SUR	=0006000000		47020	
0	4	1	207	16	0	5	0	02			SHL	2	2		47030	
0	4	1	210	15	0	5	1	151			XOR	C37	C37	= 2000000000	47040	
0	4	1	211	5	0	5	1	160			C10	160	160		47050	
0	4	1	212	10	0	5	1	133			TRA	L60P3	L60P3		47060	
0	4	1	213	17	0	5	0	01			L61P2A	CLA	PCNK		47070	
0	4	1	214	2	0	5	261		0000250000			SUR	=0000025	= 21	47080	
0	4	1	215	4	0	5	1	133			TNZ	L60P3	L60P3		47090	
0	4	1	216	17	C	5	262		7400000000			CLA	=074	SKIP AFTER PRINT CH 12	47100	
0	4	1	217	5	0	5	1	160			C10	160	160		47110	
0	4	1	220	10	0	5	1	133			TRA	L60P3	L60P3		47120	
0	4	1	221	17	0	5	1	020			L61P4	CLA	ZERU		47130	
0	4	1	222	13	0	5	0	00			STO	CTR2	CTR2		47140	
0	4	1	223	17	0	5	1	102			CLA	CTR3	CTR3		47150	
0	4	1	224	7	0	5	1	036			ADC	KSI	KSI		47160	
0	4	1	225	13	0	5	1	102			STU	CTR3	CTR3		47170	
0	4	1	226	2	C	5	263		0200000000			SUB	=002		47180	
0	4	1	227	4	0	5	1	231			TNZ	*+2	*+2		47190	
0	4	1	230	13	C	5	1	102			STO	CTR3	CTR3		47200	
0	4	1	231	10	0	5	1	233			TRA	L61P5	L61P5		47210	
0	4	1	232	10	0	5	1	266			TRA	L62P1	L62P1		47220	
0	4	1	233	13	C	5	1	376			L61P5	STO	776		47230	
0	4	1	234	16	0	4	204				CCS	0+4	0+4		47240	
0	4	1	235	17	C	4	255				CLA	K61P3A	K61P3A	RETAIN ADDRESS	47250	
0	4	1	236	6	0	4	1	045			ANC	KX6	KX6		47260	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 94)

IM	IS	S	LOC	OP	DM	DS	Y	ADR	OCT	VAL	LMS	GPC	VARIABLE	COMMENT	SEQ	NC
0	4	1	237	7	C	4	1	102				ACC	CTR3	= CLA C(LA + CTR3)	47270	
0	4	1	240	13	0	4	1	076				STU	TEMP		47280	
0	4	1	241	17	0	4	1	245				CLA	L61P3A		47290	
0	4	1	242	6	C	4	1	040				AND	KX1	REMOVE ADDRESS	47300	
0	4	1	243	15	C	4	1	076				XCR	TEMP		47310	
0	4	1	244	13	0	4	1	245				STC	L61P3A		47320	
0	4	1	245	17	0	4	1	256				CLA	LA	RETAIN ADDRESS	47330	
0	4	1	246	6	0	4	1	045				AND	KX6		47340	
0	4	1	247	13	0	4	1	076				STC	TEMP		47350	
0	4	1	250	17	0	4	1	136				CLA	L60P3A	PKS INSTRUCTION	47360	
0	4	1	251	6	C	4	1	040				AND	KX1	REMOVE ADDRESS	47370	
0	4	1	252	15	C	4	1	076				XDR	TEMP	COMLINE ADDRESS AND OP CODE	47380	
0	4	1	253	13	0	4	1	136				STC	L60P3A		47390	
0	4	1	254	0	0	4	1	376				HOP	776		47400	
0	4	1	255	17	C	4	1	256				CLA	LA		47410	
0	4	1	255	12	0	5	12					COG	0.5.		47420	
0	4	1	256	1	0	5	012					KA	KA		47430	
0	4	1	257	1	0	5	033					PRB	KB		47440	
0	4	1	260	1	0	5	054					PRB	KC		47450	
0	4	1	261	1	C	5	075					PRB	KD		47460	
0	4	1	262	1	0	5	116					PRB	KE		47470	
0	4	1	263	1	0	5	137					PRB	KF		47480	
0	4	1	264	1	0	5	160					PRB	KG		47490	
0	4	1	265	1	0	5	201					PRB	KH		47500	
0	4	1	266	17	0	5	001		000013000			CLA	PGNR		47510	
0	4	1	267	2	0	5	251					SUB	=0000013	= 11	47520	
0	4	1	270	14	0	5	1306					TMI	L62P5		47530	
0	4	1	271	4	C	5	1300					TNZ	L62P2		47540	
0	4	1	272	17	0	5	264		140000000			CLA	=014	IMMED SKIP CH 12	47550	
0	4	1	273	5	0	5	160					CIC	L60		47560	
0	4	1	274	5	0	5	214					CIC	214		47570	
0	4	1	275	6	0	5	1032					AND	K1		47580	
0	4	1	276	4	0	5	1274					TNZ	*-2		47590	
0	4	1	277	10	0	5	1306					TRA	L62P5		47600	
0	4	1	300	17	0	5	001					CLA	PGNR		47610	
0	4	1	301	2	C	5	261		000025000			SUB	=000C025	=21	47620	
0	4	1	302	4	C	5	1304					TNZ	L62P3		47630	
0	4	1	303	10	C	5	1306					TRA	L62P5		47640	
0	4	1	304	17	0	5	265		610000000			CLA	=G61	SKIP AFTER PRINT CH 1	47650	
0	4	1	305	5	0	5	160					CIC	L60		47660	
0	4	1	306	5	0	5	164					CIC	PRINT OCTAL LINE		47680	
0	4	1	307	1	C	5	222					PRB	L64	SET OCTAL MODE	47690	
0	4	1	310	7	0	5	020					ACC	KJ	LOAD BUFFERS	47700	
0	4	1	311	1	0	5	223					PRB	ZERU		47710	
0	4	1	312	7	C	5	1020					ACC	KJ+1		47720	
0	4	1	313	1	0	5	224					PRB	ZERU		47730	
0	4	1	314	7	C	5	1020					ACC	KJ+2		47740	
0	4	1	315	1	0	5	225					PRB	ZERC		47750	
0	4	1	316	7	0	5	1020					ACC	KJ+3		47760	
0	4	1	317	1	C	5	226					PRB	ZERU		47770	
0	4	1	320	7	0	5	1020					ACC	KJ+4		47780	
0	4	1	321	1	0	5	227					PRB	ZERC		47790	
0	4	1	322	7	C	5	1020					ACC	KJ+5		47800	
0	4	1	323	1	0	5	230					PRB	ZERC		47810	
0	4	1	324	7	C	5	1020					ACC	KJ+6		47820	
0	4	1	324	7	C	5	1020					ACC	ZERU		47830	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 95)

IM	IS	S	LOC	UP	UM	DS	9	ADR	OCT	VAL	LHS	GPC	VARIABLE	COMMENT	SEC	NO
0	4	1	325	1	0	5	231					PRS	KJ+7		47840	
0	4	1	326	7	0	5	1	020				ACC	ZERG		47850	
0	4	1	327	1	0	5	232					PRS	KJ+8		47860	
0	4	1	330	7	0	5	1	020				ACC	ZERG		47870	
0	4	1	331	1	0	5	233					PRS	KJ+9		47880	
0	4	1	332	7	0	5	1	020				ACC	ZERG		47890	
0	4	1	333	1	0	5	1	374				PRS	774		47900	
0	4	1	334	5	0	5	214					CIU	214	CHECK READY LINE	47910	
0	4	1	335	6	0	5	1	032				ANC	K1		47920	
0	4	1	336	4	0	5	1	334				TNZ	8--2		47930	
0	4	1	337	17	0	5	201					CLA	PGNK		47940	
0	4	1	340	2	0	5	251		000013000			SUR	=0000013	= 11	47950	
0	4	1	341	14	0	5	1	345				TMI	L62P4	LESS THAN 11	47960	
0	4	1	342	2	0	5	007		000012000			SUB	=0000012	=10	47970	
0	4	1	343	4	0	5	1	011				TNZ	L60P2A	FINISHED	47980	
0	4	1	344	00	0	5	266		531020270			TRA*	NABL	IMMED SKIP CH 1	47990	
0	4	1	345	17	0	5	267		010000000		L62P4	CLA	=001	48000		
0	4	1	346	5	0	5	160					CIC	160	48010		
0	4	1	347	10	0	5	1	011				TRA	L60P2A	48020		
0	5	12		0	5	12			141516170		KA	OCT	141516170	48040		
0	5	13		0	5	13			323536370			OCT	323536370	48050		
0	5	14		0	5	14			525556570			OCT	525556570	48060		
0	5	15		0	5	15			727576770			OCT	727576770	48070		
0	5	16		0	5	16			132040530			OCT	132040530	48080		
0	5	17		0	5	17			336021340			OCT	336021340	48090		
0	5	20		0	5	20			745473000			OCT	745473000	48100		
0	5	21		0	5	21			/STU			BCI	ABCDEFGHIJKLMN	48110		
0	5	22		0	5	22			VMXY							
0	5	23		0	5	23			ZJKL							
0	5	24		0	5	24			MNOP							
0	5	25		0	5	25			QRBC							
0	5	26		0	5	26			DEFG							
0	5	27		0	5	27			HI01							
0	5	30		0	5	30			2345							
0	5	31		0	5	31			6789							
0	5	32		0	5	32			0000							
0	5	33		0	5	33			111415160							
0	5	34		0	5	34			173233360							
0	5	35		0	5	35			375255560							
0	5	36		0	5	36			577275760							
0	5	37		0	5	37			771320400							
0	5	40		0	5	40			533360210							
0	5	41		0	5	41			347454730							
0	5	42		0	5	42			0/ST							
0	5	43		0	5	43			UVMX							
0	5	44		0	5	44			YZJK							
0	5	45		0	5	45			LMNO							
0	5	46		0	5	46			PQRB							
0	5	47		0	5	47			CDEF							
0	5	50		0	5	50			GHI0							
0	5	51		0	5	51			1234							
0	5	52		0	5	52			5678							
0	5	53		0	5	53			0000							
0	5	54		0	5	54			101114150							
0	5	55		0	5	55			101114150		KC	OCT	101114150	48200		
0	5	56		0	5	56			111415160							
0	5	57		0	5	57			173233360							
0	5	58		0	5	58			375255560							
0	5	59		0	5	59			577275760							
0	5	60		0	5	60			771320400							
0	5	61		0	5	61			533360210							
0	5	62		0	5	62			347454730							
0	5	63		0	5	63			ABCDEFGHIJKLMN							
0	5	64		0	5	64			OPQRSTUWXYZ0123456789							

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 96)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SFC	INC
0	5	55							161732350			CCI	161732350		48210	
0	5	56							363752550			CCI	363752550		48220	
0	5	57							565772750			CCI	565772750		48230	
0	5	60							767713200			CCI	767713200		48240	
0	5	61							405333600			CCI	405333600		48250	
0	5	62							213474540			CCI	213474540		48260	
0	5	63							/O/S			BCI	. ABCDEFGHIJKLMNOPQRSTUVWXYZC12345678		48270	
0	5	64							TUVW							
0	5	65							XYZJ							
0	5	66							KLMN							
0	5	67							OPCR							
0	5	70							BCDE							
0	5	71							FGHI							
0	5	72							0123							
0	5	73							4567							
0	5	74							0000							
0	5	75							71011140	KD		CCI	071011140		48280	
0	5	76							151617320			CCI	151617320		48290	
0	5	77							353637520			CCI	353637520		48300	
0	5	100							555657720			CCI	555657720		48310	
0	5	101							757677130			CCI	757677130		48320	
0	5	102							204053330			CCI	204053330		48330	
0	5	103							602134740			CCI	602134740		48340	
0	5	104							*+0/			BCI	*. ABCDEFGHIJKLMNOPQRSTUVWXYZC1234568		48350	
0	5	105							STUV							
0	5	106							WXYZ							
0	5	107							JKLM							
0	5	110							NOPC							
0	5	111							RBCD							
0	5	112							EFGH							
0	5	113							I012							
0	5	114							3456							
0	5	115							0000							
0	5	116							60710110	KE		CCI	060710110		48360	
0	5	117							141516170			CCI	141516170		48370	
0	5	120							323536370			CCI	323536370		48380	
0	5	121							525556570			CCI	525556570		48390	
0	5	122							727576770			CCI	727576770		48400	
0	5	123							132040530			CCI	132040530		48410	
0	5	124							336021340			CCI	336021340		48420	
0	5	125							(*+0			BCI	1*. ABCDEFGHIJKLMNOPQRSTUVWXYZC123458		48430	
0	5	126							/STU							
0	5	127							VMXY							
0	5	130							ZJKL							
0	5	131							MNOP							
0	5	132							QRBC							
0	5	133							DEFG							
0	5	134							HI01							
0	5	135							2345							
0	5	136							0000							
0	5	137							506071100	KF		CCI	0506071100		48440	
0	5	140							111415160			CCI	111415160		48450	
0	5	141							173235360			CCI	173235360		48460	
0	5	142							375255560			CCI	375255560		48470	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 97)

IM	IS	S	LOC	OP	OM	DS	9	ADR	OCT VAL	LHS	CPC	VARIABLE	COMMENT	SEC NO
0	5	143						577275760			OCT	577275760		48480
0	5	144						771320400			OCT	771320400		48490
0	5	145						533360210			OCT	533360210		48500
0	5	146						11*			BCI	11*.. ABCDEFGHIJKLMNOPQRSTUVWXYZ012345		48510
0	5	147						0/ST						
0	5	150						UVWX						
0	5	151						YZJK						
0	5	152						LMNC						
0	5	153						PQRS						
0	5	154						CDEF						
0	5	155						GHI0						
0	5	156						1234						
0	5	157						0000						
0	5	160						40506070	KG		OCT	040506070		48520
0	5	161						101114150			OCT	101114150		48530
0	5	162						161732350			OCT	161732350		48540
0	5	163						363752550			OCT	363752550		48550
0	5	164						565772750			OCT	565772750		48560
0	5	165						767713200			OCT	767713200		48570
0	5	166						405333600			OCT	405333600		48580
0	5	167						11*			BCI	11*.. ABCDEFGHIJKLMNOPQRSTUVWXYZ012345		48590
0	5	170						0/75						
0	5	171						TUVW						
0	5	172						XYZJ						
0	5	173						KLPN						
0	5	174						OPQR						
0	5	175						BCDE						
0	5	176						FGHI						
0	5	177						0123						
0	5	200						0000						
0	5	201						30405060	KH		OCT	030405060		48600
0	5	202						71011140			OCT	071011140		48610
0	5	203						151617320			OCT	151617320		48620
0	5	204						353637520			OCT	353637520		48630
0	5	205						555657720			OCT	555657720		48640
0	5	206						757677130			OCT	757677130		48650
0	5	207						204053330			OCT	204053330		48660
0	5	210						11*			RCI	11*.. ABCDEFGHIJKLMNOPQRSTUVWXYZ012345		48670
0	5	211						0/						
0	5	212						STUV						
0	5	213						WXYZ						
0	5	214						JKLM						
0	5	215						NOPQ						
0	5	216						RBCD						
0	5	217						EFGH						
0	5	220						1012						
0	5	221						0000						
0	5	222						12345670	KJ		OCT	012345670		48680
0	5	223						123456700			OCT	123456700		48690
0	5	224						234567012			OCT	234567012		48700
0	5	225						345670122			OCT	345670122		48710
0	5	226						456701234			OCT	456701234		48720
0	5	227						567012344			OCT	567012344		48730
0	5	230						670123456			OCT	670123456		48740

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 98)

IM	IS	LOC	OP	DM	US	ADR	CCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	5					231	701234566			OCI	701234566		48750	
0	5					232	12345670			OCI	012345670		48760	
0	5					233	123456700			OCI	123456700		48770	
0	5					234	RDEC		KK	BCI	ROUTINE 8	EXERCISE 1443 PRINTER\$	48780	
0	5					235	ZNYO							
0	5					236	8000							
0	5					237	VGVR							
0	5					240	TZBV							
0	5					241	0144							
0	5					242	30PR							
0	5					243	ZNCV							
0	5					244	R000							
0	5					245	P/YV		KL	BCI	PAGE NR \$		48790	
0	5					246	ONKO							
0	5					247	0000							

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 99)

IM	IS	S	LOC	OP	DM	DS	9	ADR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ
0	16	0	1					212					ERRM ROUTINE		48810
				0	16			212					.16, .1, .16, 212		48820
				0	16			212					50		48830
0	16	0	1	5	0	16		240			ERR		240		48840
0	16	0	2	13	0	16		214			L95P1		ERR+2		48850
0	16	0	3	17	0	16	1	070			L95P7		CLA VARI	SET PTC ERROR LAMP	48860
C	16	0	4	13	0	16	1	213			L95P2		ERR+1		48870
C	16	0	5	17	0	16	1	072			L95P3		VAR3		48880
0	16	0	6	13	0	16	1	212			L95P4		ERR		48890
0	16	0	7	17	0	16	1	073			L95P5		VAR4		48900
0	16	0	10	13	0	16	1	215			L95P6		ERR+3		48910
C	16	0	11	17	0	16	1	C74			L95P4		VAR5		48920
C	16	0	12	13	0	16	1	216			L95P5		ERR+4		48930
C	16	0	13	17	0	16	1	052			L95P5		CLA LC5		48940
0	16	0	14	4	0	16	1	020			TNZ		**4		48950
0	16	0	15	17	0	16	1	072			CLA		VAR3		48960
0	16	0	16	13	0	16	1	052			CLA		LC9		48970
0	16	0	17	17	0	16	1	052			CLA		LC5		48980
0	16	0	20	7	0	16	1	032			ADC		K1		48990
0	16	0	21	13	0	16	1	052			STC		LC5		49000
0	16	0	22	2	0	16	211		000000024		STC		=0000000C024		49010
C	16	0	23	4	0	16	026				TNZ		L95P6		49020
0	16	0	24	17	0	16	1	C33			CLA		K77		49030
0	16	0	25	13	0	16	1	274			STC		LC6		49040
0	16	0	26	17	0	16	1	C72			CLA		VAR3		49050
0	16	0	27	15	0	16	1	210			L95P6		LC9		49060
0	16	0	30	4	0	16	033				CLA		L96P1		49070
0	16	0	31	17	0	16	1	C52			CLA		LC5		49080
0	16	0	32	13	0	16	1	053			STC		LC7		49090
0	16	0	33	17	0	16	1	274			L96P1		LC6	ERROR COUNT FIRST PASS	49100
0	16	0	34	14	0	16	054				CLA		L96P2		49110
0	16	0	35	17	0	16	002				TMI		L96P2		49120
C	16	0	36	7	0	16	275		0000000500		CLA		L95P7		49130
C	16	0	37	13	0	16	002				ADC		=00000000500		49140
C	16	0	40	17	0	16	004				STC		L95P7		49150
0	16	0	41	7	0	16	004		0000000500		CLA		L95P2		49160
C	16	0	42	13	0	16	004				ADC		=00000000500		49170
0	16	0	44	7	0	16	275				CLA		L95P3		49180
0	16	0	45	13	0	16	006		0000000500		ADC		=00000000500		49190
0	16	0	46	17	0	16	010				STC		L95P3		49200
0	16	0	47	7	0	16	275		0000000500		CLA		L95P4		49210
C	16	0	50	13	0	16	010				ADC		=00000000500		49220
0	16	0	51	17	0	16	012				STC		L95P4		49230
0	16	0	52	7	0	16	275		0000000500		CLA		L95P5		49240
0	16	0	53	13	0	16	G12				ADC		=00000000500		49250
0	16	0	54	17	0	16	1	050			STC		L95P5		49260
0	16	0	55	14	0	16	057				CLA		LC2		49270
C	16	0	56	0	0	16	1	C71			L96P2		CLA		49280
0	16	0	57	0	0	16	1	070			CLA		L96P3		49290
0	16	0	60	17	0	16	144				HOP		VAR2		49300
0	16	0	61	13	0	16	1	076			L96P3		VAR1		49310
C	16	0	62	17	0	16	070				L1P1A1		CLA		49320
0	16	0	63	13	0	16	1	0C0			STC		K95P3		49330
0	16	0	64	13	0	16	070				CLA		TEMP		49340
0	16	0	65	17	0	16	332		000000144		TRA		L1P1B		49350
C	16	0	66	13	0	16	1	100			STC		L1P1C		49360
											CLA		=0000000144		49370
											STC		STOP		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 100)

IM	IS	S	LOC	OP	DP	DS	9	AOR	OCT VAL	LMS	OPC	VARIABLE	COMMENT	SEC AC
C	16	0	67	17	C	16	1	020			CLA	ZERU		49380
C	16	0	70	13	0	16	212				STC	ERR		49390
C	16	C	71	17	0	16	070			L1P1B	CLA	L1P1B		49400
C	16	0	72	7	0	16	333		000000100		ACC	=0000000100		49410
C	16	C	73	13	0	16	070				STC	L1P1H		49420
C	16	0	74	17	C	16	100				CLA	STOP		49430
C	16	0	75	2	0	16	032				SUP	K1		49440
C	16	0	76	13	0	16	100				STC	STOP		49450
C	16	C	77	4	0	16	067				INZ	L1P1H-1		49460
C	16	0	100	13	0	16	072				STC	VAR3		49470
C	16	0	101	13	C	16	052				STC	LC5		49480
C	16	0	102	13	0	16	274				STC	LC6		49490
C	16	0	103	13	0	16	053				STC	LC7		49500
C	16	0	104	5	0	16	210				CIC	210		49510
C	16	0	105	17	0	16	142				CLA	K95P1		49520
C	16	C	106	13	C	16	076				STC	TEMP		49530
C	16	C	107	17	0	16	002				CLA	L95P7		49540
C	16	0	110	10	0	16	1000				TRA	L1P1C		49550
C	16	0	111	13	0	16	002				STC	L95P7		49560
C	16	0	112	17	0	16	143				CLA	K95P2		49570
C	16	C	113	13	C	16	076				STC	TEMP		49580
C	16	0	114	17	C	16	004				CLA	L95P2		49590
C	16	0	115	10	0	16	1000				TRA	L1P1C		49600
C	16	0	116	13	0	16	004				STC	L95P2		49610
C	16	0	117	17	C	16	144				CLA	K95P3		49620
C	16	0	120	13	0	16	076				STC	TEMP		49630
C	16	0	121	17	0	16	006				CLA	L95P3		49640
C	16	0	122	10	0	16	1000				TRA	L1P1C		49650
C	16	0	123	13	0	16	006				STC	L95P3		49660
C	16	0	124	17	C	16	145				CLA	K95P4		49670
C	16	0	125	13	0	16	076				STC	TEMP		49680
C	16	0	126	17	0	16	010				CLA	L95P4		49690
C	16	0	130	13	0	16	010				STC	L95P4		49700
C	16	0	131	17	0	16	146				CLA	K95P5		49720
C	16	0	132	13	0	16	076				STC	TEMP		49730
C	16	0	133	17	0	16	012				CLA	L95P5		49740
C	16	0	134	10	0	16	1000				TRA	L1P1C		49750
C	16	0	135	13	0	16	012				STC	L95P5		49760
C	16	C	136	0	0	16	022				HOP	H2P1		49770
C	16	1	0	0	0	16	274				ORG	.16*1...16,		49780
C	16	1	0	13	0	16	376				STC	776		49790
C	16	1	1	6	C	16	334		777740036	L1P1C	ANC	=0777740036		49800
C	16	1	2	13	0	16	077				STC	TEMP1		49810
C	16	1	3	17	0	16	076				CLA	TEMP		49820
C	16	1	4	6	0	16	335		000037740		ANC	=0000037740		49830
C	16	1	5	15	0	16	077				XOR	TEMP1		49840
C	16	1	6	0	0	16	376				HOP	776		49850
C	16	0	142	13	0	16	275				ORG	.16*0.142...16,		49860
C	16	0	142	13	0	16	214				STC	ERR*2		49870
C	16	0	143	13	C	16	213				STC	ERR*1		49880
C	16	0	144	13	C	16	212				STC	ERR		49890
C	16	0	145	13	C	16	215				STC	ERR*3		49900
C	16	0	146	13	C	16	216				STC	ERR*4		49910
C	16	0	147	17	0	16	276				CLA	KHDG		49920
C	16	0	150	17	0	16	314				CLA	KHDG1		49930
C	16	0	151	17	C	16	323				CLA	KHDG2		49940

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 101)

IM	IS	S	LOC	UP	DM	DS	9	ADR	CCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	16	0	152	13	C	16	1	376			L98P3	STC	TYPE BCD WORDS		49950	
0	16	0	153	6	0	16	1	336	000037776		L98P3	ANL	=0000037776	SAVE SYLL 0	49960	
0	16	0	154	17	C	16	1	076				STC	TEMP		49970	
0	16	0	155	13	C	16	1	163				CLA	L98P3A		49980	
0	16	0	156	6	0	16	1	337	777740000			ANL	=07774CCCC	SAVE SYLL 1	50000	
0	16	0	157	15	0	16	1	076				XGR	TEMP	COMBINE SYLLABLES	50010	
0	16	0	160	13	0	16	1	163				STC	L98P3A		50020	
0	16	0	161	17	C	16	1	340	000000010		L98P3C	CLA	=000000010		50030	
0	16	0	162	13	0	16	1	077				STU	TEMP1		50040	
0	16	0	163	17	0	16	1	341			L98P3A	CLA	WORD		50050	
0	16	0	164	13	0	16	1	076				STC	TEMP		50060	
0	16	0	165	5	0	16	1	214			L98P3B	CIC	214		50070	
0	16	0	166	6	0	16	1	021				ANL	BB		50080	
0	16	0	167	4	0	16	1	165				TNZ	L98P3B		50090	
0	16	0	170	17	0	16	1	076				CLA	TEMP		50100	
0	16	0	171	5	0	16	1	120				CIC	120		50110	
0	16	0	172	16	0	16	1	040				SPL	6		50120	
0	16	0	173	13	0	16	1	076				STC	TEMP		50130	
0	16	0	174	17	0	16	1	077				CLA	TEMP1		50140	
0	16	0	175	2	0	16	1	032				SUB	K1		50150	
0	16	0	176	13	0	16	1	077				STC	TEMP1		50160	
0	16	0	177	4	0	16	1	165				TNZ	L98P3B		50170	
0	16	0	200	17	C	16	1	163				CLA	L98P3A		50180	
0	16	0	201	7	0	16	1	037				ADL	K52		50190	
0	16	0	202	13	0	16	1	163				STC	L98P3A		50200	
0	16	0	203	17	0	16	1	100				CLA	STOP		50210	
0	16	0	204	2	C	16	1	032				SUB	K1		50220	
0	16	0	205	13	0	16	1	100				STC	STOP		50230	
0	16	0	206	4	0	16	1	161				TNZ	L98P3C		50240	
0	16	0	207	0	0	16	1	376				HOP	776		50250	
0	16	1	7	7	0	16	1	276				ORG	*16.1.7.16.		50260	
0	16	1	7	17	0	16	1	051				ERROR	HEADOUT		50270	
0	16	1	10	14	C	16	1	013			L97P1	CLA	LC3		50280	
0	16	1	11	00	0	16	1	342				TMI	L97P2		50290	
0	16	1	12	00	0	16	1	343	160142300			TRA*	L99P1		50300	
0	16	1	13	5	0	16	1	220	160050260			TRA*	L90P1		50310	
0	16	1	14	14	0	16	1	012				TYPE	ERROR INFORMATION	TU PRINTER ROUTINE	50320	
0	16	1	15	10	0	16	1	151				CIC	220	B SWITCHES	50330	
0	16	1	16	17	0	16	1	110				TMI	L90P1A	USE PRINTER	50340	
0	16	1	17	13	C	16	1	076				TRA	L98P4	CARRIAGE RETURN	50350	
0	16	1	17	13	C	16	1	076				CLA	K97P4A		50360	
0	16	1	20	17	0	16	1	041				STC	TEMP		50370	
0	16	1	21	17	0	16	1	024				CLA	L97P4A		50380	
0	16	1	22	13	0	16	1	041				HOP	H43P2		50390	
0	16	1	23	17	0	16	1	211				STU	L97P4A		50400	
0	16	1	24	10	0	16	1	111	000000024			TYPE	HEADING	INDENT 10 SPACES	50410	
0	16	1	25	17	0	16	1	344				CLA	=000000024		50420	
0	16	1	26	13	0	16	1	100	000000034			TRA	L98P1	14 4-CHAR WORDS	50430	
0	16	1	27	17	0	16	1	147				CLA	=000000034		50440	
0	16	1	30	10	C	16	1	152				STU	STOP	ADDRESS OF HEADING	50450	
0	16	1	31	10	C	16	1	151				TRA	K97P3		50460	
0	16	1	32	10	0	16	1	160				TRA	L98P3	CARR RTN	50470	
0	16	1	32	10	0	16	1	160				TRA	L98P4	INDEX 1	50480	
0	16	1	32	10	0	16	1	160				TRA	L98P5		50490	
0	16	1	32	10	0	16	1	160				TYPE	OCTAL ERROR INFORMATION		50500	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 102)

IM	IS	S	LOC	OP	DM	DS	9	ADR	DCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC NO				
0	16	1	33	17	C	16	211		000000024			CLA	=000000024	10 LINES	50510				
0	16	1	34	13	0	16	1	101			L97P4	STC	CTR		50520				
0	16	1	35	17	0	16	211		000000024			CLA	=0000000024	INDENT 10	50530				
0	16	1	36	10	0	16	1	111				TRA	L98P1		50540				
0	16	1	37	17	0	16	345		000000012			CLA	=000000012	5 WORDS PER LINE	50550				
0	16	1	40	13	0	16	1	077				STC	TEMPI		50560				
0	16	1	41	17	0	16	212				L97P4A	CLA	ERR		50570				
0	16	1	42	10	0	16	1	125				TRA	L98P2		50580				
0	16	1	43	17	0	16	041					CLA	L97P4A		50590				
0	16	1	44	17	0	16	1	C36				AEC	KSI		50600				
0	16	1	45	13	0	16	041				STC	L97P4A		INCREMENT ADDRESS	50610				
0	16	1	46	17	0	16	1	C77				CLA	TEMPI		50620				
0	16	1	47	2	0	16	1	032				SUB	KI		50630				
0	16	1	50	13	0	16	1	C77				STC	TEMPI		50640				
0	16	1	51	4	0	16	1	041				TNZ	L97P4A		50650				
0	16	1	52	10	0	16	1	151				TRA	L98P4		50660				
0	16	1	53	10	0	16	1	160				TRA	L98P5		50670				
0	16	1	54	17	0	16	1	101				CLA	CTR		50680				
0	16	1	55	2	0	16	1	032				SUB	KI		50690				
0	16	1	56	13	0	16	1	101				STC	L97P4		50700				
0	16	1	57	4	0	16	1	035				TNZ	L97P4		50710				
0	16	1	60	17	0	16	211		000000024			CLA	=000000024	INDENT 10	50720				
0	16	1	61	10	0	16	1	111			L97P5	TRA	L98P1		50730				
0	16	1	62	17	0	16	346		000000014			CLA	=0000000014	6 4-CHAR WORDS	50740				
0	16	1	63	13	0	16	1	100				STC	STOP		50750				
0	16	1	64	17	0	16	1	50				CLA	K97P5		50760				
0	16	1	65	10	0	16	1	52				TRA	L98P3		50770				
0	16	1	66	17	0	16	1	052				CLA	LC5		50780				
0	16	1	67	10	0	16	1	125				TRA	L98P2		50790				
0	16	1	70	10	0	16	1	151				TRA	L98P4		50800				
0	16	1	71	10	0	16	1	160				TRA	L98P5		50810				
0	16	1	72	17	0	16	211		000000024			CLA	=0000000024	INDENT 10	50820				
0	16	1	73	10	0	16	1	111				TRA	L98P1		50830				
0	16	1	74	17	0	16	346		000000014			CLA	=0000000014	6 4-CHAR WORDS	50840				
0	16	1	75	13	0	16	1	100				STC	STOP		50850				
0	16	1	76	17	0	16	1	151				CLA	K97P5A		50860				
0	16	1	77	10	0	16	1	52				TRA	L98P3		50870				
0	16	1	100	17	0	16	1	053				CLA	LC7		50880				
0	16	1	101	10	0	16	1	125				TRA	L98P2		50890				
0	16	1	102	10	0	16	1	151				TRA	L98P4		50900				
0	16	1	103	10	0	16	1	160				TRA	L98P5		50910				
0	16	1	104	5	0	16	214		000004000			CIC	214		50920				
0	16	1	105	6	0	16	347					ANE	=0000004000		50930				
0	16	1	106	4	0	16	1	013				TNZ	L97P2		50940				
0	16	1	107	00	0	16	350		130000000			TRA*	L1P1		50950				
0	16	1	110	17	0	16	212				K97P4A	CLA	ERR		50960				
											KH0G	BCI	PASS NR	LOCATION	VAR54	50970			
													ERR	ACCUM	VAR4	50980			
																		VAR55	50980

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 103)

IM	IS	LOC	OP	OR	OS	9	ADR	OP	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	16	307					00E7								
0	16	310					R400								
0	16	311					0000								
0	16	312					00E7								
0	16	313					R500								
0	16	314					C0C7								
0	16	315					LOVR								
0	16	316					R0R0								
0	16	317					T0DN								
0	16	320					C000								
0	16	321					0000								
0	16	322					0000								
0	16	323					VRRG								
0	16	324					ROTO								
0	16	325					DMCO								
0	16	326					WZRB								
0	16	327					COPT								
0	16	330					BB00								
0	16	331					0000								
0	16	1111	13	0	16	1	376								
0	16	1112	13	0	16	1	351								
0	16	1113	5	0	16	214									
0	16	1114	6	0	16	1	021								
0	16	1115	4	0	16	1	113								
0	16	1116	17	0	16	352									
0	16	1117	5	0	16	134			400000000						
0	16	1120	17	0	16	351									
0	16	1121	2	0	16	1	032								
0	16	1122	13	0	16	351									
0	16	1123	4	0	16	1	113								
0	16	1124	0	0	16	1	376								
0	16	1125	13	0	16	1	376								
0	16	1126	13	0	16	341									
0	16	1127	17	0	16	1	376								
0	16	1130	13	0	16	1	103								
0	16	1131	17	0	16	353									
0	16	1132	13	0	16	354			000000022						
0	16	1133	5	0	16	214									
0	16	1134	6	0	16	1	021								
0	16	1135	4	0	16	1	133								
0	16	1136	17	0	16	341									
0	16	1137	5	0	16	130									
0	16	1140	16	0	16	004									
0	16	1141	13	0	16	341									
0	16	1142	17	0	16	354									
0	16	1143	2	0	16	1	032								
0	16	1144	13	0	16	354									
0	16	1145	4	0	16	1	133								
0	16	1146	17	0	16	355			000000006						

KMDG1	BC1		TOTAL ERROR COUNT	\$					50990
KMDG2	BC1		ERROR COUNT FIRST PASS	\$					51000

L98P1	STC	776	SPACE PER NUMBER IN ACCUMULATOR						51010
L98P1	STC	N							51020
L98P1A	C10	214							51030
	ANC	BB							51040
	TNZ	**2							51050
	CLA	=040000000							51060
	C1C	134							51070
	CLA	N							51080
	SUB	K1							51090
	STC	N							51100
	TNZ	L98P1A							51110
	HOP	776							51120
									51130
L98P2	STC	776	TYPE OCTAL WORD IN ACCUMULATOR						51140
	STC	WORD							51150
	CLA	776							51160
	STC	HRTRN							51170
	CLA	=000000022							51180
	STC	NINE							51190
L98P2A	C1C	214							51200
	ANC	68							51210
	TNZ	**2							51220
	CLA	WORD							51230
	C1C	130							51240
	SHL	3							51250
	STC	WORD							51260
									51270
	CLA	NINE							51310
	SUB	K1							51320
	STC	NINE							51330
	TNZ	L98P2A							51340
	CLA	=000000006							51350

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 104)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	GPC	VARIABLE	COMMENT	SEQ	NO
0	16	1	147	10	0	16	1	111				TRA	L98P1		51360	
0	16	1	150	0	0	16	1	103			*	HOP	HRTKN		51370	
0	16	1	151	13	0	16	1	376			L98P4	STC	CARRIAGE RETURN 776		51380	
0	16	1	152	5	0	16	1	214				CIO	214		51420	
0	16	1	153	6	0	16	1	021				ANC	BB		51430	
0	16	1	154	4	0	16	1	152				TNZ	*-2		51440	
0	16	1	155	17	0	16	1	356	020000000			CLA	=0020000000		51450	
0	16	1	156	5	0	16	1	134				CIO	134		51460	
0	16	1	157	0	0	16	1	376			*	HOP	776		51470	
0	16	1	160	13	0	16	1	376			L98P5	STC	INDEX CARRIAGE ONE LINE 776		51480	
0	16	1	161	5	0	16	1	214				CIO	214		51520	
0	16	1	162	6	0	16	1	021				ANC	BB		51530	
0	16	1	163	4	0	16	1	161				TNZ	*-2		51540	
0	16	1	164	17	0	16	1	357	040000000			CLA	=0040000000		51550	
0	16	1	165	5	0	16	1	134				CIO	134		51560	
0	16	1	166	0	0	16	1	376				HOP	776		51570	
0	16	1	167	1	0	16	1	276			K90P3	PRS	KHDCG		51580	
0	16	1	170	1	0	16	1	314			K90P5	PRS	KHDGI		51590	
0	16	1	171	1	0	16	1	323			K90P6	PRS	KHDG2		51600	
0	10	1	304	5	0	16	1	332				ORG	*10+1+304+16+		51610	
0	10	1	304	5	0	16	1	114			L99P1	CIC	114		51620	
0	10	1	305	17	0	16	1	212				CLA	ERR		51630	
0	10	1	306	17	0	16	1	213				CLA	ERR+1		51640	
0	10	1	307	17	0	16	1	214				CLA	ERR+2		51650	
0	10	1	310	17	0	16	1	215				CLA	ERR+3		51660	
0	10	1	311	17	0	16	1	216				CLA	ERR+4		51670	
0	10	1	312	17	0	16	1	217				CLA	ERR+5		51680	
0	10	1	313	17	0	16	1	220				CLA	ERR+6		51690	
0	10	1	314	17	0	16	1	221				CLA	ERR+7		51700	
0	10	1	315	17	0	16	1	222				CLA	ERR+8		51710	
0	10	1	316	17	0	16	1	223				CLA	ERR+9		51720	
0	10	1	317	17	0	16	1	224				CLA	ERR+10		51730	
0	10	1	320	17	0	16	1	225				CLA	ERR+11		51740	
0	10	1	321	17	0	16	1	226				CLA	ERR+12		51750	
0	10	1	322	17	0	16	1	227				CLA	ERR+13		51760	
0	10	1	323	17	0	16	1	230				CLA	ERR+14		51770	
0	10	1	324	17	0	16	1	231				CLA	ERR+15		51780	
0	10	1	325	17	0	16	1	232				CLA	ERR+16		51790	
0	10	1	326	17	0	16	1	233				CLA	ERR+17		51800	
0	10	1	330	17	0	16	1	235				CLA	ERR+18		51810	
0	10	1	331	17	0	16	1	236				CLA	ERR+19		51820	
0	10	1	332	17	0	16	1	237				CLA	ERR+20		51830	
0	10	1	333	17	0	16	1	240				CLA	ERR+21		51840	
0	10	1	334	17	0	16	1	241				CLA	ERR+22		51850	
0	10	1	335	17	0	16	1	242				CLA	ERR+23		51860	
0	10	1	336	17	0	16	1	243				CLA	ERR+24		51870	
0	10	1	337	17	0	16	1	244				CLA	ERR+25		51880	
0	10	1	340	17	0	16	1	245				CLA	ERR+26		51890	
0	10	1	341	17	0	16	1	246				CLA	ERR+27		51900	
0	10	1	342	17	0	16	1	247				CLA	ERR+28		51910	
0	10	1	342	17	0	16	1	247				CLA	ERR+29		51920	

SET SINGLE STEP

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 105)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	MC
0	10	1	343	17	0	16		250				CLA	ERR+3C		51930	
0	10	1	344	17	0	16		251				CLA	ERR+31		51940	
0	10	1	345	17	0	16		252				CLA	ERR+32		51950	
0	10	1	346	17	0	16		253				CLA	ERR+33		51960	
0	10	1	347	17	0	16		254				CLA	ERR+34		51970	
0	10	1	350	17	0	16		255				CLA	ERR+35		51980	
0	10	1	351	17	0	16		256				CLA	ERR+36		51990	
0	10	1	352	17	0	16		257				CLA	ERR+37		52000	
0	10	1	353	17	0	16		260				CLA	ERR+38		52010	
0	10	1	354	17	0	16		261				CLA	ERR+39		52020	
0	10	1	355	17	0	16		262				CLA	ERR+40		52030	
0	10	1	356	17	0	16		263				CLA	ERR+41		52040	
0	10	1	357	17	0	16		264				CLA	ERR+42		52050	
0	10	1	360	17	0	16		265				CLA	ERR+43		52060	
0	10	1	361	17	0	16		266				CLA	ERR+44		52070	
0	10	1	362	17	0	16		267				CLA	ERR+45		52080	
0	10	1	363	17	0	16		270				CLA	ERR+46		52090	
0	10	1	364	17	0	16		271				CLA	ERR+47		52100	
0	10	1	365	17	0	16		272				CLA	ERR+48		52110	
0	10	1	366	17	0	16		273				CLA	ERR+49		52120	
0	10	1	367	10	0	16		304				TRA	L99P1		52130	
0	6	1	120		C	16		333				ORG	TO RESUME NORMAL OPERATION HIT MACHINE RESET		52140	
0	6	1	120	10	0	16		272				TRA	PRINT ERROR INFORMATION		52150	
0	6	1	121	1	0	16		374			L90P1	PR	ERR+61,120,+16,		52160	
0	6	1	122	10	0	16		272			TRA	L94P3	CLEAR BUFFERS		52170	
0	6	1	123	17	0	16		136			CLA	L94P3	CHECK READY		52180	
0	6	1	124	5	0	16		160			CIO	C26	CHECK READY		52190	
0	6	1	125	5	0	16		170			CIO	160	SKIP TO CHANNEL 1		52200	
0	6	1	126	10	0	16		170			CIO	170			52210	
0	6	1	127	1	0	16		1020			TRA	L94P3			52220	
0	6	1	127	1	0	16		1020			PR	ZERO			52230	
0	6	1	130	1	0	16		1020			PR	ZERO			52240	
0	6	1	131	1	0	16		1020			PR	ZERO			52250	
0	6	1	132	17	0	16		344		000000034	L90P3	PRINT HEADING			52260	
0	6	1	133	13	0	16		100			CLA	=0000000034			52270	
0	6	1	134	17	0	16		167			STO	STOP			52280	
0	6	1	135	10	0	16		1245			CLA	K90P3			52290	
0	6	1	136	1	0	16		374			TRA	L94P1	LOAD BUFFERS		52300	
0	6	1	137	10	0	16		272			PR	774			52310	
0	6	1	140	17	0	16		360		410000000	TRA	L94P3	CHECK READY		52320	
0	6	1	141	5	0	16		160			CLA	=0+10000000	SPACE 1		52330	
0	6	1	142	16	0	6		206			CIC	160			52340	
0	6	1	143	17	0	6		244			CDS	0+6			52350	
0	6	1	144	6	0	6		1045			CLA	K90P4A			52360	
0	6	1	145	13	0	6		1076			ANC	KX6			52370	
0	6	1	146	17	0	6		164			STO	TEMP			52380	
0	6	1	147	6	0	6		1040			CLA	L90P4A			52390	
0	6	1	150	15	0	6		1076			ANC	KX1			52400	
0	6	1	151	13	0	6		164			XOR	TEMP	RESTORE ORIGINAL ADDRESS		52410	
0	6	1	152	16	0	16		216			STO	L90P4A			52420	
0	6	1	153	17	0	16		211		000000024	CDS	0+16	TEN		52430	
0	6	1	154	13	0	16		100			CLA	=0000000024			52440	
0	6	1	155	5	0	16		170			STC	STOP			52450	
0	6	1	156	17	0	16		345		000000012	CIO	170	SET BCD MODE		52460	
0	6	1	157	13	0	16		1076			CLA	=0000000012	FIVE		52470	
0	6	1	157	13	0	16		1076			STO	TEMP			52480	
0	6	1	157	13	0	16		1076			STO	TEMP			52490	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 106)

IM	IS	S	LDC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
0	6	1	160	1	0	16	1	020				PRS	ZERO		52500	
0	6	1	161	1	0	16	1	020				PRS	ZERO		52510	
C	6	1	162	1	0	16	1	020				PRS	ZERO		52520	
0	6	1	163	5	0	16	1	164			L90P4A	PRS	ERR	SET OCTAL MODE	52530	
0	6	1	164	1	0	16	2	212				PRS	ERR		52540	
C	6	1	165	16	C	6	206					CDS	U,6		52550	
0	6	1	166	17	0	6	164					CLA	L90P4A		52560	
0	6	1	167	7	0	6	1	036				ADD	KSI		52570	
0	6	1	170	13	0	6	164					STC	L90P4A		52580	
0	6	1	171	16	0	16	216					CDS	O,16		52590	
0	6	1	172	17	0	16	1	076				CLA	TEMP		52600	
0	6	1	173	2	0	16	1	032				SUB	KI		52610	
0	6	1	174	13	0	16	1	076				STC	TEMP		52620	
0	6	1	175	4	0	16	1	164				TNZ	L90P4A		52630	
0	6	1	176	1	0	16	1	374				PRS	774	PRINT OCTAL LINE	52640	
C	6	1	177	10	C	16	1	272				TRA	L94P3		52650	
0	6	1	200	17	0	16	360		410000000			CLA	=0410000000		52660	
0	6	1	201	5	0	16	160					CIO	L60		52670	
0	6	1	202	10	0	16	1	272				TRA	L94P3		52680	
0	6	1	203	17	0	16	1	100				CLA	L94P3		52690	
0	6	1	204	2	0	16	1	032				SUB	KI		52700	
0	6	1	205	13	0	16	1	100				STC	STOP		52710	
0	6	1	206	4	0	16	1	155				TNZ	L90P4		52720	
0	6	1	207	5	0	16	1	170				CIO	L70		52730	
0	6	1	210	1	0	16	1	020				PRS	ZERO	SET BCD MODE	52740	
0	6	1	211	1	0	16	1	020				PRS	ZERO		52750	
0	6	1	212	1	0	16	1	020				PRS	ZERO		52760	
0	6	1	213	17	0	16	346		000000014			CLA	=0000000014	SIX	52770	
0	6	1	214	13	0	16	1	100				STC	STOP		52780	
0	6	1	215	17	0	16	1	170				CLA	K90P5		52790	
0	6	1	216	10	0	16	1	245				TRA	L94P1		52800	
0	6	1	217	5	0	16	1	164				CIO	L64	SET OCTAL MODE	52810	
0	6	1	220	1	0	16	1	052				PRS	LC5		52820	
0	6	1	221	7	0	16	1	020				PRC	ZERO	PRINT TOTAL ERROR COUNT	52830	
0	6	1	222	1	0	16	1	374				PRS	774		52840	
0	6	1	223	10	0	16	1	272				TRA	L94P3		52850	
0	6	1	224	17	0	16	360		410000000			CLA	=0410000000		52860	
0	6	1	225	5	0	16	160					CIO	L60		52870	
C	6	1	226	5	0	16	170					CIO	L70		52880	
0	6	1	227	10	0	16	1	272				TRA	L94P3		52890	
0	6	1	230	1	0	16	1	020			L90P6	PRS	ZERO	SET BCD MODE	52900	
C	6	1	231	1	C	16	1	020				PRS	ZERO	CHECK READY	52910	
0	6	1	232	1	0	16	1	020				PRS	ZERO		52920	
0	6	1	233	17	0	16	346		000000014			CLA	=0000000014	SIX	52930	
0	6	1	234	13	0	16	1	100				STC	STOP		52940	
0	6	1	235	17	0	16	171					CLA	K90P6		52950	
0	6	1	236	10	0	16	1	245				TRA	L94P1		52960	
0	6	1	237	5	0	16	1	164				CIO	L64	SET OCTAL MODE	52970	
0	6	1	240	1	0	16	1	053				PRS	LC7		52980	
0	6	1	241	7	0	16	1	020				ADD	ZERO		52990	
0	6	1	242	1	0	16	1	374				PRS	774	PRINT ERROR COUNT FIRST PASS	53000	
0	6	1	243	0	0	16	1	022				HDP	H2P1	FINISHED	53010	
0	6	1	244	1	0	16	212				K90P4A	PRS	ERR		53020	
0	6	1	245	13	0	16	1	376				PRC	ZERO		53040	
0	6	1	246	6	0	16	1	045			L94P1	STC	776	LOAD BUFFERS WITH BCD LINE OF PRINT	53050	
												ANC	KX6		53060	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 107)

IM	IS	S	LOC	OP	DM	DS	9	ADR	CCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
0	6	1	247	13	0	16	1	076				STO	TEMP		53070	
0	6	1	250	16	0	6	206					CDS	0.6		53080	
0	6	1	251	17	0	6	256					CLA	L94P2		53090	
0	6	1	252	6	0	6	1040					AND	KX1		53100	
0	6	1	253	15	0	6	1076					XOR	TEMP		53110	
0	6	1	254	13	0	6	256					STO	L94P2		53120	
0	6	1	255	16	0	16	216					CDS	0.16		53130	
0	6	1	256	1	0	16	341				L94P2	PRS	WORD		53140	
0	6	1	257	17	0	16	1100					CLA	STOP		53150	
0	6	1	260	2	0	16	1032					SUB	K1		53160	
0	6	1	261	13	0	16	1100					STC	STOP		53170	
0	6	1	262	4	0	16	1284					TNZ	++2		53180	
0	6	1	263	0	0	16	1376					HOP	776		53190	
0	6	1	264	16	0	6	206					CDS	0.6		53200	
0	6	1	265	17	0	6	256					CLA	L94P2		53210	
0	6	1	266	7	0	6	1036					ACC	K1		53220	
0	6	1	267	13	0	6	256					STO	L94P2		53230	
0	6	1	270	16	0	16	216					CDS	0.16		53240	
0	6	1	271	10	0	16	1256					TRA	L94P2		53250	
0	6	1	272	13	0	16	1376					STO	776		53260	
0	6	1	273	5	0	16	214					CIO	214		53270	
0	6	1	274	6	0	16	1032					AND	K1		53280	
0	6	1	275	4	0	16	1273					TNZ	++2		53290	
0	6	1	276	0	0	16	1376					HOP	776		53300	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 108)

IM IS S LOC	OP DM DS 9	ADR	OCT VAL	LHS	OPC	VARIABLE	COMMENT	SEC NO
1 0 0 10	1 10	30		JAB1	ORG	1...10.1.10.		53320
1 0 0 11	1 10	064			CLA			53330
1 0 0 12	1 10	015			TMI	JAC1		53340
1 0 0 13	0 10	000	130007000		TNZ	MAB1B		53350
1 0 0 14	0 10	001	511010050	MAB1B	TRA*	L2P1		53360
					TRA*	MAB1		53370
								53390
								53400
1 0 0 15	1 10	020		JAC1	CLA	ZERO		53420
1 0 0 16	1 10	376			STC	776		53430
1 0 0 17	1 10	066			CIC	066	RESET COMPARE LATCH	53440
1 0 0 20	1 10	002	777777776		CLA	=077777776		53450
1 0 0 21	1 10	000			CIC	000	SET INT INHIBITS	53460
1 0 0 22	1 10	003	000152204		CLA	=0000152204	RESET	53470
1 0 0 23	1 10	223			CIC	623		53480
1 0 0 24	1 10	004	000020000		CLA	=000002		53490
1 0 0 25	1 10	213			CIC	613		53500
1 0 0 26	1 10	005	000000040		CLA	=000000040		53510
1 0 0 27	1 10	030			CIC	030	RST INT 5 LATCH	53520
1 0 0 30	1 10	004			CIC	004	RST INT 5 INHIBIT	53530
1 0 0 31	1 10	110			CIC	110	RST MAIN INT LATCH	53540
1 0 0 32	1 10	033			CLA	K77	INHIBIT ACCEL. SUBTRACTS	53550
1 0 0 33	1 10	126			CIC	126		53560
								53570
1 0 0 34	1 10	006			CIC	006	SSFB	53580
1 0 0 35	1 10	012			CIC	012	RCA GC DATA	53590
1 0 0 36	1 10	026			CIC	026	DIS REG	53600
1 0 0 37	1 10	032			CIC	032	MASA DISCRETES	53610
1 0 0 40	1 10	136			CIC	136	LOAD ACCEL. DELAY LINES	53620
1 0 0 41	1 10	142			CIC	142	LOAD ACCEL. DELAY LINES	53630
1 0 0 42	1 10	146			CIC	146	LOAD ACCEL. DELAY LINES	53640
1 0 0 43	1 10	046			CIC	046	INT REG	53650
1 0 0 44	1 10	052			CIC	052	OPTI SYN NEG	53660
1 0 0 45	1 10	056			CIC	056	COD SHIFT REG	53670
1 0 0 46	1 10	377			CIC	377	ADDRESS REG	53680
1 0 0 47	1 10	054			PIA	777		53690
1 0 0 50	1 10	055			TMI	LC8		53700
1 0 0 51	1 10	002			CLA	JAF1		53710
1 0 0 52	1 10	022	777777776		CLA	=077777776		53720
1 0 0 53	1 10	036			CIC	022	LOAD DIN REG	53730
1 0 0 54	1 10	042			CIC	036		53740
								53750
1 0 0 55	1 10	1 377			CIC	042	TEST GC DATA REGISTER FOR ONES	53760
1 0 0 56	1 10	1 377		JAF1	STO	777	LOCN OF FAILED TEST	53770
1 0 0 57	1 10	1 073			CLA	777		53780
1 0 0 60	1 10	020			STO	V4		53790
1 0 0 61	1 10	061			CLA	ZERO	RD GC DATA	53800
1 0 0 62	1 10	006	777760000		CIC	061		53810
1 0 0 63	1 10	1 116			XOR	=077776000		53820
					TNZ	JAJ5		53830
								53840
1 0 0 64	1 10	1 377			STO	777		53850
1 0 0 65	1 10	1 377		JAG1	STO	777		53860
1 0 0 66	1 10	1 073			CLA	V4		53870
1 0 0 67	1 10	065			STO	V4		53880
1 0 0 68	1 10	065			CIC	065	RD CR DATA	
1 0 0 70	1 10	1 116			TNZ	JAJ5		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 109)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ
1	0	0	71	13	1	10	1	377			JAJ1	STO	777		53890
1	0	0	72	17	1	10	1	377			CLC	777			53900
1	0	0	73	13	1	10	1	073			STO	V4			53910
1	0	0	74	17	1	10	007	525240000			CLA	=0525240000	LOAD GC DATA		53920
1	0	0	75	5	1	10	012				CIO	012			53930
1	0	0	76	17	1	10	1	020			CLA	ZERO			53940
1	0	0	77	5	1	10	061				CIO	061			53950
1	0	0	100	15	1	10	007	525240000			XOR	=0525240000			53960
1	0	0	101	4	1	10	116				TNZ	JAJ5			53970
1	0	0	102	13	1	10	1	377			STO	777	CHECK CR DATA FOR COMPLEMENT PATTERN		53980
1	0	0	103	17	1	10	1	377			CLA	777			54000
1	0	0	104	13	1	10	1	073			STO	V4			54010
1	0	0	105	5	1	10	065				CIO	065			54020
1	0	0	106	15	1	10	010	252520000			XOR	=0252520000			54030
1	0	0	107	4	1	10	116				TNZ	JAJ5			54040
1	0	0	110	13	1	10	1	377			STO	777			54050
1	0	0	111	17	1	10	1	377			CLA	777			54060
1	0	0	112	13	1	10	1	073			STO	V4			54070
1	0	0	113	17	1	10	010	252520000			CLA	=0252520000			54080
1	0	0	114	5	1	10	012				CIO	012			54090
1	0	0	115	17	1	10	1	020			CLA	ZERO			54100
1	0	0	116	5	1	10	061				CIO	061			54110
1	0	0	117	15	1	10	010	252520000			XOR	=0252520000			54120
1	0	0	120	4	1	10	116				TNZ	JAJ5			54130
1	0	0	121	13	1	10	1	376			STO	776	TEST COMPARE LATCH		54140
1	0	0	122	17	1	10	1	020			CLA	ZERO			54150
1	0	0	123	13	1	10	1	073			STO	V4			54160
1	0	0	124	17	1	10	011	400000000			CLA	=0400000000	ENABLE COMPARE		54170
1	0	0	125	5	1	10	066				CIO	066			54180
1	0	0	126	17	1	10	030				CLA	HJAD2			54190
1	0	0	127	13	1	10	1	004			HJAD2	JAD2			54200
1	0	0	130	13	1	10	1	376			STO	404	INT 5 WILL HOP TO NEXT TEST		54210
1	0	0	131	17	1	10	012				STO	776	TEST COMPARE WITH ACC BIT =1, GC BIT =0		54220
1	0	0	132	5	1	10	061				CLA	=0652520000			54230
1	0	0	133	10	1	10	116				CIO	061			54240
1	0	0	134	13	1	10	1	376			HPC	JAD2			54250
1	0	0	135	5	1	10	030				STO	776	TEST COMPARE WITH ACC BIT =1, GC BIT =0		54260
1	0	0	136	5	1	10	110				CLA	=0652520000			54270
1	0	0	137	17	1	10	1	376			CIO	061			54280
1	0	0	140	15	1	10	031				TRA	JAJ5			54290
1	0	0	141	4	1	10	116				STO	776	CHECK HOP SAVE AFTER INT 5		54300
1	0	0	142	13	1	10	1	376			CIO	030	RST INT 5		54310
1	0	0	143	17	1	10	032				CIO	110	RST MAIN INT LATCH		54320
1	0	0	144	13	1	10	1	004			CLA	776			54330
1	0	0	145	17	1	10	013				CLA	HJAC2A			54340
1	0	0	146	5	1	10	061				HPC	JAC2A			54350
1	0	0	147	10	1	10	116				TNZ	JAJ5			54360
1	0	0	150	17	1	10	1	030			STO	776			54370
1	0	0	151	4	1	10	116				STU	776			54380
1	0	0	152	13	1	10	1	376			CLA	HJAF2			54390
1	0	0	153	17	1	10	032				STO	404			54400
1	0	0	154	13	1	10	1	004			HPC	JAF2			54410
1	0	0	155	17	1	10	013				CLA	=0212520000			54420
1	0	0	156	5	1	10	061				CIO	061			54430
1	0	0	157	10	1	10	116				TRA	JAJ5			54440
1	0	0	158	17	1	10	1	030			CLA	HJAJ5			54450

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 110)

IM	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	0	0	151	13	1	10	1 004				STU	404		54460	
1	0	0	152	5	1	10	030				C1U	030	4RESET INT 5	54470	
1	0	0	153	5	1	10	110				C1U	110	RESET MAIN INT LATCH	54480	
1	0	0	154	17	1	10	1 020				CLA	ZERO		54490	
1	0	0	155	5	1	10	006				C1C	006		54500	
1	0	0	156	5	1	10	026				C1C	026		54510	
1	0	0	157	5	1	10	032				C1U	032		54520	
1	0	0	160	5	1	10	046				C1C	046		54530	
1	0	0	161	5	1	10	052				C1U	052		54540	
1	0	0	162	5	1	10	056				C1U	056		54550	
1	0	0	163	17	1	10	1 054				CLA	LC8		54560	
1	0	0	164	14	1	10	171				THI	JWE1		54570	
1	0	0	165	17	1	10	1 020				CLA	ZERO		54580	
1	0	0	166	5	1	10	022				C1C	022		54590	
1	0	0	167	5	1	10	036				C1C	036	DDAS REG	54600	
1	0	0	170	5	1	10	042				C1C	042	EM REG	54610	
1	0	0	171	13	1	10	1 376				STU	776	CHECK COMPARE LATCH WITH ENABLE COMPARE RESET	54620	
1	0	0	172	17	1	10	014	253500000		JWPI	CLA	=025350000		54630	
1	0	0	173	5	1	10	066				C1U	066	DISABLE COMPARE	54640	
1	0	0	174	5	1	10	061				C1U	061	READ GC	54650	
1	0	0	175	13	1	10	1 376				STU	776	NO INT 5 SHOULD OCCUR	54660	
1	0	0	176	17	1	10	015	002000002		JWD1	CLA	=000200002		54670	
1	0	0	177	13	1	10	1 373				STU	773	PIC GRP 5 WITH ERS NOT EQUAL TO ACCUM	54680	
1	0	0	200	17	1	10	016	000000100			CLA	=0000000100		54690	
1	0	0	201	12	1	10	1 373				PIO	773		54700	
1	0	0	202	13	1	10	1 376				STU	776	NO INT 5 SHOULD OCCUR	54710	
1	0	0	203	17	1	10	033				STU	776	CHECK COMPARE WITH PIO GRP 5	54720	
1	0	0	204	5	1	10	066				CLA	K77	CORRECT DATA	54730	
1	0	0	205	17	1	10	015	002000002			C1U	066		54740	
1	0	0	206	12	1	10	1 373				PIO	773		54750	
1	0	0	207	13	1	10	1 376				STU	776	NO INT 5 SHOULD OCCUR	54760	
1	0	0	210	17	1	10	033				CLA	HJMK1	CHECK COMPARE WITH PIO GRP 5	54770	
1	0	0	211	13	1	10	1 004	501106400		HJMK1	HPC	HJMK1		54780	
1	0	0	212	17	1	10	1 020				STC	404		54790	
1	0	0	213	12	1	10	1 373				CLA	ZE-R0		54800	
1	0	0	214	10	1	10	1 116				PIO	773	NO INT 5 SHOULD OCCUR	54810	
1	0	0	215	5	1	10	030				TRA	JAJ5	INCORRECT DATA WITH PIO GRP 5	54820	
1	0	0	216	5	1	10	110				C1U	030		54830	
1	0	0	217	13	1	10	1 376				C1U	110		54840	
1	0	0	220	17	1	10	034	501113400			CLA	ZE-R0		54850	
1	0	0	221	13	1	10	1 004				PIO	773	INT 5 SHOULD OCCUR HERE	54860	
1	0	0	222	17	1	10	017	002000000		JMK1	TRA	JAJ5		54870	
1	0	0	223	13	1	10	1 373				C1U	030	RESET INT 5	54880	
1	0	0	224	17	1	10	015	002000002		JW83	C1U	110		54890	
1	0	0	225	12	1	10	1 373				CLA	HJME3		54900	
											HPC	JME3		54910	
											STU	404		54920	
											CLA	=0002000000		54930	
											STU	773		54940	
											CLA	=0002000002		54950	
											PIO	773		54960	
											INT 5 SHOULD OCCUR HERE			54970	
											INT 5 SHOULD OCCUR HERE			54980	
											INT 5 SHOULD OCCUR HERE			54990	
											INT 5 SHOULD OCCUR HERE			55000	
											INT 5 SHOULD OCCUR HERE			55010	
											INT 5 SHOULD OCCUR HERE			55020	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 111)

IM	IS	S	LOC	OP	DM	OS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	0	0	226	10	1	10	1	116			JME3	TRA	JAJ5		55030	
1	0	0	227	17	1	10	1	030				CLA	HJAJ5		55040	
1	0	0	230	13	1	10	1	004				STO	404		55050	
1	0	0	231	5	1	10	1	030				CIU	030		55060	
1	0	0	232	5	1	10	1	110				CIU	110		55070	
1	0	0	233	13	1	10	1	376			*	TEST COMPARE WITH CORRECT ACCUMULATOR		55080		
1	0	0	234	17	1	10	1	010	252520000		JAG2	STO	776		55090	
1	0	0	235	5	1	10	1	061				CIU	061		55100	
1	0	0	236	13	1	10	1	377			*	TEST SSPB REG FOR ZERO		55110		
1	0	0	237	17	1	10	1	377			JAM2	STO	777		55120	
1	0	0	240	13	1	10	1	073				CLA	777		55130	
1	0	0	241	17	1	10	1	073				STO	V4		55140	
1	0	0	242	5	1	10	1	020				CLA	ZERO		55150	
1	0	0	242	5	1	10	1	055				CIU	055		55160	
1	0	0	243	13	1	10	1	377			*	TEST CR REG FOR COMPLIMENT OF GC		55170		
1	0	0	244	17	1	10	1	377			JA12	STU	777		55180	
1	0	0	245	13	1	10	1	073				CLA	777		55190	
1	0	0	246	17	1	10	1	007				STO	V4		55200	
1	0	0	247	5	1	10	1	065	525240000			CLA	=0525240000		55210	
1	0	0	250	13	1	10	1	377			*	TEST DISCRETE INPUT SPARES (DIS) FOR ZERO		55220		
1	0	0	251	17	1	10	1	377			JAK2	STC	777		55230	
1	0	0	252	13	1	10	1	073				CLA	777		55240	
1	0	0	253	17	1	10	1	020				STU	V4		55250	
1	0	0	254	5	1	10	1	075				CLA	ZERO		55260	
1	0	0	255	13	1	10	1	377			*	TEST NASA DISCRETES (NA DIS) FOR ZERO		55270		
1	0	0	256	17	1	10	1	377			JAC3	CIU	075		55280	
1	0	0	257	13	1	10	1	073				STC	V4		55290	
1	0	0	260	17	1	10	1	020				CLA	ZERO		55300	
1	0	0	261	5	1	10	1	011				CIU	101		55310	
1	0	0	262	17	1	10	1	054				CLA	LCR		55320	
1	0	0	263	14	1	10	1	313				IMI	JAC3		55330	
1	0	0	264	13	1	10	1	377			*	TEST CIU REG FOR ZERO		55340		
1	0	0	265	17	1	10	1	377			JAD3	STO	777		55350	
1	0	0	266	13	1	10	1	073				CLA	777		55400	
1	0	0	267	17	1	10	1	020				STC	V4		55410	
1	0	0	270	5	1	10	1	105				CLA	ZERO		55420	
1	0	0	271	7	1	10	1	020			*	TEST INT 1 NOT SET BY CIU 4,5,6 VIA INTCV		55430		
1	0	0	272	0	1	10	1	023				ADD	ZERO		55440	
1	0	0	273	13	1	10	1	377				HOP	H9P3		55450	
1	0	0	274	17	1	10	1	377				STU	777		55460	
1	0	0	275	13	1	10	1	073				CLA	777		55470	
1	0	0	276	5	1	10	1	154				STC	V4		55480	
1	0	0	277	4	1	10	1	116				CIU	154		55490	
1	0	0	300	7	1	10	1	020				TNZ	JAJ5		55500	
1	0	0	301	13	1	10	1	377			*	TEST EM REG FOR ZERO		55510		
1	0	0	302	17	1	10	1	377			JAE3	ADD	ZERO		55520	
1	0	0	303	13	1	10	1	073				STU	777		55530	
1	0	0	304	17	1	10	1	020				CLA	V4		55540	
1	0	0	305	5	1	10	1	111				CIU	ZERO		55550	
											*	TEST DISCRETE INPUTS (DIN REG) FOR ZERO		55560		
												CIU	111		55570	
															55580	
															55590	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 112)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	0	0	306	13	1	10	1	377			JAF3	STO	777		55600	
1	0	0	307	17	1	10	1	377				CLA	777		55610	
1	0	0	310	17	1	10	1	073				STU	V4		55620	
1	0	0	311	17	1	10	1	020				CLA	ZERO		55630	
1	0	0	312	5	1	10	071					CIO	071		55640	
1	0	0	313	13	1	10	1	377			*	TEST OPTISYN REG FOR ZERO			55650	
1	0	0	314	17	1	10	1	377			JAG3	STU	777		55660	
1	0	0	315	13	1	10	1	073				CLA	777		55670	
1	0	0	316	17	1	10	1	020				STO	V4		55680	
1	0	0	317	5	1	10	121				*	TEST INT SIGNAL REG FOR ZERO			55690	
1	0	0	320	13	1	10	1	377			JAH3	STO	777		55700	
1	0	0	321	17	1	10	1	377				CLA	777		55720	
1	0	0	322	13	1	10	1	073				STU	V4		55730	
1	0	0	323	17	1	10	1	020				CLA	ZERO		55740	
1	0	0	324	5	1	10	115				*	TEST COD SHIFT REGISTER FOR ZERO			55750	
1	0	0	325	13	1	10	1	377			JAJ3	STU	777		55760	
1	0	0	326	17	1	10	1	377				CLA	777		55770	
1	0	0	327	13	1	10	1	073				STU	V4		55780	
1	0	0	330	17	1	10	1	020				CLA	ZERO		55800	
1	0	0	331	5	1	10	131					CIO	131	TE3A	55810	
1	0	0	332	5	1	10	141					CIO	141	TE3B	55820	
1	0	0	333	10	1	10	1	010			*	LOAD ALL OUTPUT REGISTERS EXCEPT CR ALL ONES			55830	
1	0	1	10	1	10	1	35				JAK3	ORG	1,1,10,1,10,		55840	
1	0	1	11	13	1	10	1	073				CLA	ZERO		55850	
1	0	1	12	17	1	10	002		777777776			STU	V4		55860	
1	0	1	13	5	1	10	012					CLA	=077777776		55880	
1	0	1	14	5	1	10	026					CIL	012		55900	
1	0	1	15	5	1	10	032					CIO	026		55910	
1	0	1	16	5	1	10	046					CIO	032		55920	
1	0	1	17	5	1	10	052					CIO	046		55930	
1	0	1	20	5	1	10	056					CIO	052		55940	
1	0	1	21	5	1	10	006					CIO	056		55950	
1	0	1	22	17	1	10	054					CIO	006		55960	
1	0	1	23	14	1	10	030					CLA	LCH		55970	
1	0	1	24	17	1	10	002		777777776			TMI	JAC4		55980	
1	0	1	25	5	1	10	022					CLA	=077777776		55990	
1	0	1	26	5	1	10	036					CIO	022		56000	
1	0	1	27	5	1	10	042				*	TEST CR REG			56010	
1	0	1	30	13	1	10	1	376			JAC4	STU	776		56030	
1	0	1	31	17	1	10	020		002520000			CLA	=002520000		56040	
1	0	1	32	5	1	10	016					CIO	016		56050	
1	0	1	33	5	1	10	065					CIO	065		56060	
1	0	1	34	13	1	10	1	376			JAD4	STU	776		56070	
1	0	1	35	17	1	10	021		001240000			CLA	=001240000		56080	
1	0	1	36	5	1	10	016					CIO	016		56090	
1	0	1	37	5	1	10	065					CIL	065		56100	
1	0	1	40	13	1	10	1	376			JAE4	STU	776		56110	
1	0	1	41	17	1	10	006		777760000			CLA	=077760000		56120	
1	0	1	42	5	1	10	016					CIL	016		56130	
1	0	1	43	5	1	10	065				*	TEST GC FOR COMPLEMENT OF CR			56140	
															56150	
															56160	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 113)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	0	1	44	13	1	10	1	376			JAF4	STC	776		56170	
1	0	1	45	17	1	10	1	020			CLA	ZERO			56180	
1	0	1	46	5	1	10	061				CIU	061			56190	
													TEST SSFB REGISTER		56200	
1	0	1	47	13	1	10	1	376			JAG4	STU	776		56210	
1	0	1	50	17	1	10	020		002520000		CLA	=0002520000		56220		
1	0	1	51	5	1	10	006				CIU	006		56230		
1	0	1	52	5	1	10	055				CIU	055		56240		
1	0	1	53	13	1	10	1	376			JAH4	STC	776		56250	
1	0	1	54	17	1	10	022		001250000		CLA	=0001250000		56260		
1	0	1	55	5	1	10	006				CIU	006		56270		
1	0	1	56	5	1	10	055				CIU	055		56280		
1	0	1	57	13	1	10	1	376			JAJ4	STC	776		56290	
1	0	1	60	17	1	10	023		003770000		CLA	=0003770000		56300		
1	0	1	61	5	1	10	006				CIU	006		56310		
1	0	1	62	5	1	10	055				CIU	055		56320		
													TEST DIS REGISTER		56330	
1	0	1	63	13	1	10	1	376			JAK4	STC	776		56340	
1	0	1	64	17	1	10	024		524000000		CLA	=0524000000		56350		
1	0	1	65	5	1	10	026				CIU	026		56360		
1	0	1	66	5	1	10	075				CIU	075		56370		
1	0	1	67	13	1	10	1	376			JAC5	STC	776		56380	
1	0	1	70	17	1	10	025		252000000		CLA	=0252000000		56390		
1	0	1	71	5	1	10	026				CIU	026		56400		
1	0	1	72	5	1	10	075				CIU	075		56410		
1	0	1	73	13	1	10	1	376			JAD5	STC	776		56420	
1	0	1	74	17	1	10	026		776000000		CLA	=0776000000		56430		
1	0	1	75	5	1	10	026				CIU	026		56440		
1	0	1	76	5	1	10	075				CIU	075		56450		
													TEST NA DIS REGISTER		56480	
1	0	1	77	13	1	10	1	376			JAE5	STC	776		56490	
1	0	1	100	17	1	10	035		000000524		CLA	=0000000524		56500		
1	0	1	101	5	1	10	032				CIU	032		56510		
1	0	1	102	5	1	10	101				CIU	101		56520		
1	0	1	103	13	1	10	1	376			JAF5	STC	776		56530	
1	0	1	104	17	1	10	036		000000252		CLA	=0000000252		56540		
1	0	1	105	5	1	10	032				CIU	032		56550		
1	0	1	106	5	1	10	101				CIU	101		56560		
1	0	1	107	13	1	10	1	376			JAG5	STC	776		56570	
1	0	1	110	17	1	10	037		000000776		CLA	=0000000776		56580		
1	0	1	111	5	1	10	032				CIU	032		56590		
1	0	1	112	5	1	10	101				CIU	101		56600		
1	0	1	113	17	1	10	1	054			CLA	LCH		56610		
1	0	1	114	14	1	10	1	220			TMI	JRA2		56620		
1	0	1	115	10	1	10	1	131			TRA	JBA1		56630		
1	0	1	116	13	1	10	1	377			JAJ5A	STU	TEMP		56640	
1	0	1	120	17	1	10	1	076			CLA	777		56650		
1	0	1	121	13	1	10	1	071			STU	VAR2		56660		
1	0	1	122	17	1	10	1	376			CLA	776		56670		
1	0	1	123	13	1	10	1	070			STU	VAR1		56680		
1	0	1	124	17	1	10	040		000000400		CLA	=00000000400		56690		
1	0	1	125	5	1	10	1	203			CIU	603		56700		
1	0	1	126	0	1	10	1	023			HOP	H9P3		56710		
1	0	1	127	17	1	10	1	076			CLA	TEMP		56720		
													SET LTE ERROR LAMP		56730	
													RESET ALL INT LATCHES		56730	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 114)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	0	1	130	0	1	10	1	027				HOP	H95P7		56740	
1	0	1	131	13	1	10	1	376			JRA1	TEST	CIU REGISTER	TO ERROR ROUTINE	56750	
1	0	1	132	17	1	10	041		525000000			CLA	=0250000000		56760	
1	0	1	133	5	1	10	036					CIU	036		56770	
1	0	1	134	5	1	10	105					CIU	105		56780	
1	0	1	135	13	1	10	1	376			JBH1	STU	776		56800	
1	0	1	136	17	1	10	042		252400000			CLA	=0252400000		56810	
1	0	1	137	5	1	10	036					CIU	036		56820	
1	0	1	140	5	1	10	105					CIU	105		56830	
1	0	1	141	13	1	10	1	376			JBC1	STU	776		56840	
1	0	1	142	17	1	10	043		777400000			CLA	=0777400000		56850	
1	0	1	143	5	1	10	036					CIU	036		56860	
1	0	1	144	5	1	10	105					CIU	105		56870	
1	0	1	145	7	1	10	1	020				TEST	INT 1 SET BY CIU VIA INTCV		56880	
1	0	1	146	13	1	10	1	376			ADU	ZEMO		56890		
1	0	1	147	5	1	10	154				STU	776		56900		
1	0	1	150	6	1	10	011		400000000			AND	L54		56910	
1	0	1	151	4	1	10	1	153				AND	=0400000000		56920	
1	0	1	152	10	1	10	1	116			TNZ	**2		56930		
1	0	1	153	5	1	10	010				TRA	JAJ5		56940		
1	0	1	154	5	1	10	110				CIU	010	RESET INT 1	56950		
1	0	1	155	13	1	10	1	376			CIU	110		56960		
1	0	1	156	17	1	10	044		525250000			TEST	EM REGISTER		56970	
1	0	1	157	5	1	10	042				STU	776		56980		
1	0	1	160	5	1	10	111				CLA	=0525250000		56990		
1	0	1	161	13	1	10	1	376			CIU	111		57000		
1	0	1	162	17	1	10	045		252524000			STU	776		57010	
1	0	1	163	5	1	10	042				CLA	=0252524000		57020		
1	0	1	164	5	1	10	111				CIU	042		57030		
1	0	1	165	13	1	10	1	376			CIU	111		57040		
1	0	1	166	17	1	10	046		777774000			STU	776		57050	
1	0	1	167	5	1	10	042				CLA	=0777774000		57060		
1	0	1	170	5	1	10	111				CIU	042		57070		
1	0	1	171	10	1	10	1	210			CIU	111		57080		
1	0	1	210	17	1	10	047				TRA	JBG1		57090		
1	0	1	211	13	1	10	1	376			TEST	DIM REGISTER		57100		
1	0	1	212	5	1	10	022		252525252		ORG	L*1,210,1,10,		57110		
1	0	1	213	5	1	10	071				CLA	=0252525252		57120		
1	0	1	214	13	1	10	1	376			STU	776		57130		
1	0	1	215	17	1	10	050		525252524			CLA	=0525252524		57140	
1	0	1	216	5	1	10	022				CIU	022		57150		
1	0	1	217	5	1	10	071				CIU	022		57160		
1	0	1	220	13	1	10	1	376			TEST	OPTISYN REGISTER		57170		
1	0	1	221	17	1	10	051		000012524		STU	776		57180		
1	0	1	222	5	1	10	052				CLA	=0000012524		57190		
1	0	1	223	5	1	10	121				CIU	042		57200		
1	0	1	224	13	1	10	1	376			CIU	121		57210		
1	0	1	225	17	1	10	052		000005252		STU	776		57220		
1	0	1	226	5	1	10	052				CLA	=000005252		57230		
1	0	1	227	5	1	10	121				CIU	052		57240		
1	0	1	227	5	1	10	121				CIU	121		57250		
															57260	
															57270	
															57280	
															57290	
															57300	

CAL POINT NR 25

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 115)

IM	IS	S	LOC	OP	DM	DS	9	ADR	UCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ NO
1	0	1	230	13	1	10	1	376			JRC2	STU	776		57310
1	0	1	231	17	1	10	053		000017776		CLA	=000017776		57320	
1	0	1	232	5	1	10	052				C1U	052		57330	
1	0	1	233	5	1	10	121				C1U	121		57340	
1	0	1	234	13	1	10	1 376				*	TEST INI SIGNAL REGISTER		57350	
1	0	1	235	17	1	10	054		125200000		J8D2	STU	776	57360	
1	0	1	236	5	1	10	046				CLA	=012520000		57370	
1	0	1	237	5	1	10	115				C1U	046		57380	
1	0	1	240	13	1	10	1 376				C1U	115		57390	
1	0	1	241	17	1	10	055		052500000		J8E2	STU	776	57400	
1	0	1	242	5	1	10	046				CLA	=005250000		57410	
1	0	1	243	5	1	10	115				C1U	046		57420	
1	0	1	244	13	1	10	1 376				C1C	115		57430	
1	0	1	245	17	1	10	056		177700000		J8F2	STU	776	57440	
1	0	1	246	5	1	10	046				CLA	=017770000		57450	
1	0	1	247	5	1	10	115				C1U	046		57460	
1	0	1	250	13	1	10	1 376				*	LOAD AND TEST GC REG ALL ONES		57470	
1	0	1	251	17	1	10	006		777760000		J8G2	STU	776	57480	
1	0	1	252	5	1	10	012				CLA	=017776000		57490	
1	0	1	253	5	1	10	061				C1U	012		57500	
1	0	1	254	13	1	10	1 376				*	FEST COD REGISTER		57510	
1	0	1	255	17	1	10	057		252505252		J8H2	STU	776	57520	
1	0	1	256	5	1	10	056				CLA	=0252505252		57530	
1	0	1	257	5	1	10	131				C1U	056		57540	
1	0	1	260	5	1	10	141				C1U	131		57550	
1	0	1	261	13	1	10	1 376				C1U	141		57560	
1	0	1	262	5	1	10	062				STC	776		57570	
1	0	1	263	17	1	10	060		125202524		J8J2	STU	776	57580	
1	0	1	264	5	1	10	056				CLA	=0125202524		57590	
1	0	1	265	5	1	10	131				C1U	056		57600	
1	0	1	266	5	1	10	141				C1U	131		57610	
1	0	1	267	13	1	10	1 376				C1U	141		57620	
1	0	1	270	17	1	10	061		377707776		J8K2	STU	776	57630	
1	0	1	271	5	1	10	056				CLA	=0377707776		57640	
1	0	1	272	5	1	10	131				C1U	056		57650	
1	0	1	273	5	1	10	141				C1U	131		57660	
1	0	1	274	17	1	10	062				CLA	=000000004		57670	
1	0	1	275	5	1	10	1 223				C1C	623		57680	
1	0	1	276	17	1	10	054				CLA	LCH		57690	
1	0	1	277	14	1	10	1 301				JMI	JECIA		57700	
1	0	1	300	00	1	10	063		501034060		TRA*	JBM2		57710	
1	0	1	301	00	1	10	064		501045410		TRA*	JEC1		57720	
1	6	0	70	1	10	1	37				ORG	1.6*76.1.10.		57730	
1	6	0	70	17	1	10	1 020				*	TEST DIN REC FOR ZERO		57750	
1	6	0	71	13	1	10	1 376				CLA	ZERU		57760	
1	6	0	72	5	1	10	022				STU	776		57770	
1	6	0	73	5	1	10	071				C1C	022		57780	
1	6	0	74	13	1	10	1 376				C1U	071		57810	
1	6	0	75	17	1	10	050				*	CHECK DA INPUTS AND MULTIPLEXER		57820	
1	6	0	76	5	1	10	022		525252524		J8A3	STU	776	57830	
1	6	0	77	5	1	10	071				CLA	=0525252524		57840	
1	6	0	100	13	1	10	1 376				C1U	022		57850	
1	6	0	100	13	1	10	1 376				J8B3	STU	776	57860	
														57870	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 116)

IM	IS	S	LDC	UP	OM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	0	101	17	1	10	047	252525252				CLA	=0252525252		57880	
1	6	0	102	5	1	10	005				J8C3	CIU	005	GC A DATA IN	57890	
1	6	0	103	13	1	10	1 376	525250000				STU	776		57900	
1	6	0	104	17	1	10	044					CLA	=0525250000	GC B DATA IN	57910	
1	6	0	105	5	1	10	011				J8D3	CIU	011		57920	
1	6	0	106	13	1	10	1 376					STU	776		57930	
1	6	0	107	17	1	10	1 020					CLA	ZEK0		57940	
1	6	0	110	5	1	10	015				J8E3	CIU	015	ORBITAL CHECKOUT	57950	
1	6	0	111	13	1	10	1 376	525250000				STU	776		57960	
1	6	0	112	17	1	10	044				J8F3	CLA	=0525250000	DOR IN	57970	
1	6	0	113	5	1	10	021					CIU	021		57980	
1	6	0	114	13	1	10	1 376	252520000				STU	776		57990	
1	6	0	115	17	1	10	010				J8G3	CLA	=0252520000	SSR IN	58000	
1	6	0	116	5	1	10	031					CIU	031		58010	
1	6	0	117	13	1	10	1 376	525252524				STU	776		58020	
1	6	0	120	17	1	10	050				J8H3	CLA	=0525252524	TEL DATA A	58030	
1	6	0	121	5	1	10	035					CIU	035		58040	
1	6	0	122	13	1	10	1 376	252520000			J8B4	STU	776	TEL DATA B	58050	
1	6	0	123	17	1	10	010					CLA	=025252C000		58060	
1	6	0	124	5	1	10	041	525250000			J8C4	CIU	041		58070	
1	6	0	125	13	1	10	1 376					STU	776		58080	
1	6	0	126	17	1	10	044					CLA	=052525C000	DDAS (CIU) DATA IN	58090	
1	6	0	127	5	1	10	045	252525252				CIU	045		58100	
1	6	0	130	13	1	10	1 376				J8G4	STU	776		58110	
1	6	0	131	17	1	10	047					CLA	=0252525252	NA SIM LAB IN	58120	
1	6	0	132	5	1	10	051					CIU	051		58130	
1	6	0	133	13	1	10	1 376				J8G4	LOAD	DIN REG		58140	
1	6	0	134	17	1	10	047	252525252				STU	776		58150	
1	6	0	135	5	1	10	022					CLA	=0252525252		58160	
1	6	0	136	5	1	10	071				J8B5	CIU	022	READ	58170	
1	6	0	137	13	1	10	1 376	525252524				CIU	071		58180	
1	6	0	140	17	1	10	050				J8C5	STU	776		58190	
1	6	0	141	5	1	10	005					CLA	=0525252524	GC A	58200	
1	6	0	142	13	1	10	1 376	252520000			J8D5	CIU	005		58210	
1	6	0	143	17	1	10	010					STU	776		58220	
1	6	0	144	5	1	10	011				J8D5	CIU	011	GC B	58230	
1	6	0	145	13	1	10	1 376	000000002				STU	776		58240	
1	6	0	146	17	1	10	065				J8E5	CLA	=0000000002	OCV	58250	
1	6	0	147	5	1	10	015	252500000				CIU	015		58260	
1	6	0	150	13	1	10	1 376				J8F5	STU	776		58270	
1	6	0	151	17	1	10	066					CLA	=025250C000	DOR	58280	
1	6	0	152	5	1	10	021	525250000			J8F5	CIU	021		58290	
1	6	0	153	13	1	10	1 376					STU	776		58300	
1	6	0	154	17	1	10	044	525250000			J8G5	CLA	=0525250000	SSR	58310	
1	6	0	155	5	1	10	031					CIU	031		58320	
1	6	0	156	13	1	10	1 376	252525252			J8H5	STU	776	TEL A	58330	
1	6	0	157	17	1	10	047					CLA	=0252525252		58340	
1	6	0	160	5	1	10	035				J8B1	CIU	035	TEL B	58350	
1	6	0	161	13	1	10	1 376	125250000				STU	776		58360	
1	6	0	162	17	1	10	067				J8C1	CLA	=0125250000		58370	
1	6	0	163	5	1	10	041	252520000				CIU	041		58380	
1	6	0	164	13	1	10	1 376					STU	776		58390	
1	6	0	165	17	1	10	010				J8C1	CLA	=0252520000		58400	
1	6	0	166	5	1	10	045	525252524				CIU	045	DDAS IN	58410	
1	6	0	167	13	1	10	1 376				J8C1	STU	776		58420	
1	6	0	170	17	1	10	050					CLA	=0525252524		58430	
1	6	0	170	17	1	10	050					CLA	=0525252524		58440	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 117)

IM	IS	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NO
1	6	0	171	5	1	10	051				CIO	051	NA SIM	58450
1	6	0	172	13	1	10	1 376				LOAD	DIN REG		58460
1	6	0	173	17	1	10	070	631463146		JCH1	STU	776		58470
1	6	0	174	5	1	10	022				CLA	=0631463146		58480
1	6	0	175	5	1	10	071				CIO	022	DIN	58490
1	6	0	176	13	1	10	1 376			JCB2	STU	776		58500
1	6	0	177	17	1	10	071	714631462			CLA	=0714631462		58510
1	6	0	200	5	1	10	005				CIO	005	GC A	58520
1	6	0	201	13	1	10	1 376			JCC2	STU	776		58530
1	6	0	202	17	1	10	072	746310000			CLA	=0746310000		58540
1	6	0	203	5	1	10	011			JCD2	CIO	011	GC B	58550
1	6	0	204	13	1	10	1 376				STU	776		58560
1	6	0	205	17	1	10	020				CLA	ZERO	OCV	58570
1	6	0	206	5	1	10	015			JCEZ	CIO	015		58580
1	6	0	207	13	1	10	1 376	171440000			STU	776		58590
1	6	0	210	17	1	10	073			JCF2	CLA	=0171440000	DOR	58600
1	6	0	211	5	1	10	021				CIO	021		58610
1	6	0	212	13	1	10	1 376			JCG2	STU	776		58620
1	6	0	214	5	1	10	031	474630000			CLA	=0474630000	SSR	58630
1	6	0	215	13	1	10	1 376			JCH2	CIO	031		58640
1	6	0	216	17	1	10	075	636314630			STU	776		58650
1	6	0	217	5	1	10	035			JCG2	CLA	=0636314630	TEL A	58660
1	6	0	218	5	1	10	077				CIO	035		58670
1	6	0	220	13	1	10	1 376	317140000		JCH2	STU	776		58680
1	6	0	221	17	1	10	076			JCJ2	CLA	=0317140000	TEL B	58690
1	6	0	222	5	1	10	041				CIO	041		58700
1	6	0	223	13	1	10	1 376	147460000		JCJ2	STU	776		58710
1	6	0	224	17	1	10	077				CLA	=0147460000		58720
1	6	0	225	5	1	10	045			JCK2	CIO	045	DDAS	58730
1	6	0	226	13	1	10	1 376	363146314			STU	776		58740
1	6	0	227	17	1	10	143			JCK2	CLA	=0363146314		58750
1	6	0	230	5	1	10	051				CIO	051	NA SIM	58760
1	6	0	231	13	1	10	1 376			JCB4	LOAD	DIN REGISTER		58770
1	6	0	232	17	1	10	144	741703606			STU	776		58780
1	6	0	233	5	1	10	022				CLA	=0741703606		58790
1	6	0	234	5	1	10	071			JCE4	CIO	022		58800
1	6	0	235	13	1	10	1 376				STU	071		58810
1	6	0	236	17	1	10	145	760741702		JCE4	CLA	=0760741702		58820
1	6	0	237	5	1	10	005				CIO	005	GC A	58830
1	6	0	240	13	1	10	1 376	770360000		JCF4	STU	776		58840
1	6	0	241	17	1	10	146				CLA	=0770360000		58850
1	6	0	242	5	1	10	011			JCG4	CIO	011	GC B	58860
1	6	0	243	13	1	10	1 376				STU	776		58870
1	6	0	244	17	1	10	020			JCH4	CLA	ZERO	OCV	58880
1	6	0	245	5	1	10	015				CIO	015		58890
1	6	0	246	13	1	10	1 376	176050000		JCH4	STU	776		58900
1	6	0	250	5	1	10	021				CLA	=0176050000		58910
1	6	0	251	13	1	10	1 376			JCJ4	CIO	021	DOR	58920
1	6	0	252	17	1	10	150	077030000			STU	776		58930
1	6	0	253	5	1	10	031			JCB5	CLA	=0077030000	SSR	58940
1	6	0	254	13	1	10	1 376				CIO	031		58950
1	6	0	255	17	1	10	151	037417036			CLA	=0037417036		58960
1	6	0	256	5	1	10	035				CIO	035	TEL A	58970
1	6	0	257	13	1	10	1 376			JCC5	STU	776		58980
1	6	0	257	13	1	10	1 376				STU	776		58990
1	6	0	257	13	1	10	1 376				STU	776		59010

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 118)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	6	0	260	17	1	10	152		017600000			CLA	=001760000		59020	
1	6	0	261	5	1	10	041					CIO	041	TEL B	59030	
1	6	0	262	13	1	10	376				JCD5	STU	776		59040	
1	6	0	263	17	1	10	153		607700000			CLA	=060770000	ODAS	59050	
1	6	0	264	5	1	10	045					CIO	045		59060	
1	6	0	265	13	1	10	376				JCE5	STU	776		59070	
1	6	0	266	17	1	10	154		374170360			CLA	=0374170360	NA SIP	59080	
1	6	0	267	5	1	10	051					CIO	051		59090	
1	6	0	270	00	1	10	155		501005010			TRAB	JEB1		59100	
1	1	0	12				40					ORG	1,1,0,12,1,1,10,		59110	
1	1	0	12	17	1	10	156		776003770		JOB1	CLA	=0776003770		59120	
1	1	0	13	13	1	10	376					STU	776		59130	
1	1	0	14	5	1	10	022					CIO	022		59140	
1	1	0	15	5	1	10	071					CIO	071		59150	
1	1	0	16	13	1	10	376				JDE1	STU	776		59160	
1	1	0	17	17	1	10	157		377001774			CLA	=0377001774		59170	
1	1	0	20	5	1	10	005					CIO	005		59180	
1	1	0	21	13	1	10	376		177400000		JDF1	STU	776	GC A	59190	
1	1	0	22	17	1	10	160					CLA	=0177400000		59200	
1	1	0	23	5	1	10	011					CIO	011	GC B	59210	
1	1	0	24	13	1	10	376				JOG1	STU	776		59220	
1	1	0	25	17	1	10	065		000000002			CLA	=0000000002		59230	
1	1	0	26	5	1	10	015					CIO	015	OCV	59240	
1	1	0	27	13	1	10	376		637700000		JDH1	STU	776		59250	
1	1	0	30	17	1	10	161					CLA	=0637700000		59260	
1	1	0	31	5	1	10	021				JDJ1	STU	776	DDR	59270	
1	1	0	32	13	1	10	376		717740000			CLA	=0717740000		59280	
1	1	0	33	17	1	10	162					CIO	031	SSR	59290	
1	1	0	34	5	1	10	031					CLA	=0717740000		59300	
1	1	0	35	13	1	10	376		747760036		JDB2	STU	776		59310	
1	1	0	36	17	1	10	163					CLA	=0747760036	TEL A	59320	
1	1	0	37	5	1	10	035					CIO	035		59330	
1	1	0	40	13	1	10	376		363770000		JDC2	STU	776		59340	
1	1	0	41	17	1	10	164					CLA	=0363770000		59350	
1	1	0	42	5	1	10	041					CIO	041	TEL B	59360	
1	1	0	43	13	1	10	376				JDC2	STU	776		59370	
1	1	0	44	17	1	10	165		771770000			CLA	=0771770000		59380	
1	1	0	45	5	1	10	045					CIO	045	ODAS	59390	
1	1	0	46	13	1	10	376		477600376		JDE2	STU	776		59400	
1	1	0	47	17	1	10	166					CLA	=0477600376	NA SIP	59410	
1	1	0	50	5	1	10	051					CIO	051		59420	
1	1	0	51	13	1	10	376				JDB3	STU	776		59430	
1	1	0	52	17	1	10	046		777774000			CLA	=0777740000		59440	
1	1	0	53	5	1	10	022					CIO	022		59450	
1	1	0	54	5	1	10	071					CIO	071		59460	
1	1	0	55	13	1	10	376				JDE3	STU	776		59470	
1	1	0	56	17	1	10	167		377776000			CLA	=0377776000		59480	
1	1	0	57	5	1	10	005					CIO	005		59490	
1	1	0	60	13	1	10	376				JDF3	STU	776	GC A	59500	
1	1	0	61	17	1	10	170		177770000			CLA	=0177700000		59510	
1	1	0	62	5	1	10	011					CIO	011	GC B	59520	
1	1	0	63	13	1	10	376				JDG3	STU	776		59530	
1	1	0	64	17	1	10	1020					CLA	ZERO		59540	
1	1	0	65	5	1	10	015					CIO	015	OCV	59550	
1	1	0	66	13	1	10	376				JDH3	STU	776		59560	
1	1	0	66	13	1	10	376					STU	776		59570	
1	1	0	66	13	1	10	376					STU	776		59580	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 119)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	1	0	67	17	1	10	1	171	037750000			CLA	=0037750000		59590	
1	1	0	70	5	1	10	0	021			CIU	021		DIR	59600	
1	1	0	71	13	1	10	1	376			STO	776			59610	
1	1	0	72	17	1	10	1	172	017770000		JDJ3	CLA	=0017770000		59620	
1	1	0	73	5	1	10	0	031			CIU	031		SSR	59630	
1	1	0	74	13	1	10	1	376			STO	776			59640	
1	1	0	75	17	1	10	1	173	007777740		JDR4	CLA	=0007777740		59650	
1	1	0	76	5	1	10	0	035			CIU	035		TEL A	59660	
1	1	0	77	13	1	10	1	376			STO	776			59670	
1	1	0	100	17	1	10	1	023	003770000		JDC4	CLA	=0003770000		59680	
1	1	0	101	5	1	10	0	041			CIU	041		TEL B	59690	
1	1	0	102	13	1	10	1	376			STO	776			59700	
1	1	0	103	17	1	10	1	174	001770000		CLA	=0001770000			59710	
1	1	0	104	5	1	10	0	045			CIU	045		DDAS	59720	
1	1	0	105	13	1	10	1	376			STO	776			59730	
1	1	0	106	17	1	10	1	175	077777400		JDE4	CLA	=007777400		59740	
1	1	0	107	5	1	10	0	051			CIU	051		NA SIM	59750	
1	1	0	110	17	1	10	0	002	777777776		* JEB1	CLA	=077777776	TEST P10 ADDRESS REGISTER AND MPLXR GATES	59760	
1	1	0	111	5	1	10	0	022			CIU	022		LOAD P10 REG	59770	
1	1	0	112	5	1	10	0	071			CIU	071		READ P10 REG	59780	
1	1	0	113	13	1	10	1	376			* JEC1	STU	776	TEST P10 ADDRESS REGISTER	59800	
1	1	0	114	12	1	10	0	000			PIU	000			59810	
1	1	0	115	17	1	10	1	020			CLA	ZER0		READ ADDRESS REG	59820	
1	1	0	116	5	1	10	1	125			CIU	L25			59830	
1	1	0	117	13	1	10	1	376			JEE1	STU	776		59840	
1	1	0	120	12	1	10	1	376			PIU	776			59850	
1	1	0	121	17	1	10	1	176	000001774		CLA	=0000001774			59860	
1	1	0	122	5	1	10	1	125			CIU	L25			59870	
1	1	0	123	13	1	10	1	376			STU	776			59880	
1	1	0	124	12	1	10	1	125			PIU	525			59890	
1	1	0	125	17	1	10	1	177	000001252		CLA	=0000001252			59900	
1	1	0	126	5	1	10	1	125			CIU	L25			59910	
1	1	0	127	13	1	10	1	376			JEJ1	STU	776		59920	
1	1	0	130	12	1	10	2	252			PIU	252			59930	
1	1	0	131	17	1	10	0	035	000000524		CLA	=000000524			59940	
1	1	0	132	5	1	10	1	125			CIU	L25			59950	
1	1	0	133	17	1	10	1	054			* JEA2	CLA		TEST A13 AND LDATAV INTERFACE	59960	
1	1	0	134	14	1	10	2	055			LCB	JEB4		DISABLE COMPARE LATCH	59970	
1	1	0	135	17	1	10	1	020			JEB2	CLA	ZER0		59980	
1	1	0	136	5	1	10	0	066			CIU	066			59990	
1	1	0	137	13	1	10	1	376			JEC2	STU	776		60000	
1	1	0	140	17	1	10	0	050	525252524		CLA	=0525252524			60010	
1	1	0	141	12	1	10	1	137			PIU	137			60020	
1	1	0	142	5	1	10	1	111			X0K	111			60030	
1	1	0	143	15	1	10	2	000	525200000		TNZ	JEJ5			60040	
1	1	0	144	4	1	10	2	666			STU	776		LOAD EM REG	60050	
1	1	0	145	13	1	10	1	376			JEE2	CLA	=0252525252	READ EM REG	60060	
1	1	0	146	17	1	10	0	047	252525252		PIU	137			60070	
1	1	0	147	12	1	10	1	137			CIU	137			60080	
1	1	0	150	5	1	10	1	111			XOR	111			60090	
1	1	0	151	15	1	10	0	066	252500000		XOR	=0252500000			60100	
1	1	0	152	4	1	10	2	666			TNZ	JEJ5			60110	
1	1	0	153	13	1	10	1	376			JEG2	STU	776		60120	
1	1	0	154	17	1	10	1	176			PIU	137			60130	
1	1	0	155	13	1	10	1	376			XOR	=0252500000			60140	
1	1	0	156	4	1	10	2	666			TNZ	JEJ5			60150	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 120)

IM	IS	S	LOC	UP	OM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
1	1	0	154	17	1	10		201	036077776			CLA	=0036077776		60160	
1	1	0	155	12	1	10		137			PIU	137			60170	
1	1	0	156	5	1	10		111			CIU	111			60180	
1	1	0	157	15	1	10		202	036000000			XOK	=0036000000		60190	
1	1	0	160	4	1	10		266			TNZ	JEJ5			60200	
1	1	0	161	13	1	10		1	741777776		JEB3	STO	776		60210	
1	1	0	162	17	1	10		203			CLA	=0741777776			60220	
1	1	0	163	12	1	10		137			PIU	137			60230	
1	1	0	164	5	1	10		111			CIU	111			60240	
1	1	0	165	15	1	10		204	741700000		XOK	=0741700000			60250	
1	1	0	166	4	1	10		266			TNZ	JEJ5			60260	
1	1	0	167	13	1	10		1	770077776		JED3	STU	776		60270	
1	1	0	170	17	1	10		205			CLA	=0770077776			60280	
1	1	0	171	12	1	10		137			PIU	137			60290	
1	1	0	172	5	1	10		111			CIU	111			60300	
1	1	0	173	15	1	10		206	770000000		XOK	=0770000000			60310	
1	1	0	174	4	1	10		266			TNZ	JEJ5			60320	
1	1	0	175	13	1	10		1	007777776		JEF3	STO	776		60330	
1	1	0	176	17	1	10		207			CLA	=0007777776			60340	
1	1	0	177	12	1	10		137			PIU	137			60350	
1	1	0	200	5	1	10		111			CIU	111			60360	
1	1	0	201	15	1	10		210	007700000		XOK	=0007700000			60370	
1	1	0	202	4	1	10		266			TNZ	JEJ5			60380	
1	1	0	203	17	1	10		002	777777776		JEH3	CLA	=0777777776		60390	
1	1	0	204	5	1	10		042			CIU	042		LOAD EM REG	60400	
1	1	0	205	5	1	10		066			* TEST	TRS AND DATAV	INPUT TO MPLXR		60410	
1	1	0	206	13	1	10		1	525252524		JEB4	CIU	066	ENABLE COMPARE	60420	
1	1	0	207	17	1	10		050			JEC4	STU	776		60430	
1	1	0	210	13	1	10		003			CLA	=0525252524			60440	
1	1	0	211	12	1	10		003			STC	403			60450	
1	1	0	212	13	1	10		1			PIU	403			60460	
1	1	0	213	17	1	10		047	252525252		JED4	STU	776		60470	
1	1	0	214	13	1	10		003			CLA	=0252525252			60480	
1	1	0	215	12	1	10		003			STO	403			60490	
1	1	0	216	13	1	10		1			PIU	403			60500	
1	1	0	217	17	1	10		070	631463146		JEE4	STU	776		60510	
1	1	0	220	13	1	10		003			CLA	=0631463146			60520	
1	1	0	221	12	1	10		003			STO	403			60530	
1	1	0	222	13	1	10		1			PIU	403			60540	
1	1	0	223	17	1	10		211	146314630		JEF4	STO	776		60550	
1	1	0	224	13	1	10		003			CLA	=0146314630			60560	
1	1	0	225	12	1	10		003			STO	403			60570	
1	1	0	226	13	1	10		1			PIU	403			60580	
1	1	0	227	17	1	10		144	741703606		JEG4	STO	776		60590	
1	1	0	230	13	1	10		003			CLA	=0741703606			60600	
1	1	0	231	12	1	10		003			STO	403			60610	
1	1	0	232	13	1	10		1			PIU	403			60620	
1	1	0	233	17	1	10		212	036074170		JEH4	STU	776		60630	
1	1	0	234	13	1	10		003			CLA	=0036074170			60640	
1	1	0	235	12	1	10		003			STU	403			60650	
1	1	0	236	13	1	10		1			PIU	403			60660	
1	1	0	237	17	1	10		156	776003770		JEB5	STO	776		60670	
1	1	0	240	13	1	10		003			CLA	=0776003770			60680	
1	1	0	241	12	1	10		003			STU	403			60690	
1	1	0	242	13	1	10		1			PIU	403			60700	
1	1	0	243	17	1	10		213	001774006		JEC5	STU	776		60710	
1	1	0	243	17	1	10		213			CLA	=0001774006			60720	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 121)

IM	IS	S	LOC	UP	UM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEC	NC
1	1	0	244	13	1	10	1	003				STU	403		60730	
1	1	0	245	12	1	10	1	003				PIU	403		60740	
1	1	0	246	13	1	10	1	376			JED>	STU	776		60750	
1	1	0	247	17	1	10	0	46	777774000			CLA	=0777774000		60760	
1	1	0	250	13	1	10	1	003				STU	403		60770	
1	1	0	251	12	1	10	1	003				PIU	403		60780	
1	1	0	252	13	1	10	1	376			JEE>	STU	776		60790	
1	1	0	253	17	1	10	1	214	000003776			CLA	=000003776		60800	
1	1	0	254	13	1	10	1	003				STU	403		60810	
1	1	0	255	12	1	10	1	003				PIU	403		60820	
1	1	0	256	17	1	10	1	020				CLA	ZERO		60830	
1	1	0	257	13	1	10	1	003				STU	403		60840	
1	1	0	260	5	1	10	0	32				CIU	032	CLEAR NA DIS	60850	
1	1	0	261	17	1	10	1	054				CLA	LC8		60860	
1	1	0	262	14	1	10	1	012				THI	JFB1		60870	
1	1	0	263	17	1	10	1	020				CLA	ZERO		60880	
1	1	0	264	5	1	10	0	36				CIU	036		60890	
1	1	0	265	10	1	10	1	012				TRA	JF=1	CLEAR DDAS (CIU)	60900	
1	1	0	266	13	1	10	1	377				STU	777		60910	
1	1	0	267	00	1	10	1	215	501047600		JEJ5	STU	777		60920	
1	1	1	12	1	10	41						TRA*	JAJ5A		60930	
1	1	1	12	0	1	10	1	023			*	TEST	PIO DECODING AND INTERRUPTS		60940	
1	1	1	13	17	1	10	1	020			JF81	ORG	1,1,1,1,2,1,10,	RESET ALL INT LATCHES	60950	
1	1	1	14	5	1	10	0	66				HOP	H9P3		60960	
1	1	1	15	17	1	10	0	02	777777776		*	CLA	ZERO	DISABLE COMPARE	60970	
1	1	1	16	5	1	10	0	00				CIU	066		60980	
1	1	1	17	17	1	10	1	054				CLA	=0777777776		60990	
1	1	1	20	14	1	10	1	022				LC8			61000	
1	1	1	21	10	1	10	1	023				THI	JJUBA		61010	
1	1	1	22	00	1	10	1	216				TRA	*+2		61020	
1	1	1	23	13	1	10	1	376	501066420		JJB1A	TRA*			61030	
1	1	1	24	5	1	10	1	54				STU	JJB1		61040	
1	1	1	25	4	1	10	2	66				CIU	776		61050	
1	1	1	26	13	1	10	1	376			*	CIU	154		61060	
1	1	1	27	12	1	10	1	010			JFE1	TNZ	JEJ5		61070	
1	1	1	30	7	1	10	1	020				STU	776	CHECK PIO GROUP 1 OR 3 SET INT 6	61080	
1	1	1	31	5	1	10	1	154				PIU	010	GROUP 1	61090	
1	1	1	32	15	1	10	2	17				ACC	ZERO		61100	
1	1	1	33	4	1	10	2	66	010000000			CIU	154	READ INTERRUPT REG.	61110	
1	1	1	34	13	1	10	1	376				XOR	=0010000000		61120	
1	1	1	35	5	1	10	0	34			JFG1	TNZ	JEJ5		61130	
1	1	1	36	12	1	10	0	01				STU	776		61140	
1	1	1	37	7	1	10	1	020				CIU	034	RST INT 6	61150	
1	1	1	40	5	1	10	1	54				PIU	001	GROUP 3	61160	
1	1	1	41	15	1	10	2	17	010000000			ADD	ZERO		61170	
1	1	1	42	4	1	10	2	66				XOR	=0010000000		61180	
1	1	1	43	13	1	10	1	376			JFJ1	TNZ	JEJ5		61190	
1	1	1	44	5	1	10	0	34				STU	776	RST INT 6	61200	
1	1	1	45	12	1	10	0	06				CIU	034	GRP 2	61210	
1	1	1	46	12	1	10	2	77				PIU	000		61220	
1	1	1	47	5	1	10	0	00				CIU	277		61230	
1	1	1	50	7	1	10	1	020				ACC	000		61240	
1	1	1	51	5	1	10	1	54				ZERU	ZERU		61250	
1	1	1	52	4	1	10	2	66				CIU	154		61260	
1	1	1	52	4	1	10	2	66				TNZ	JEJ5		61270	
1	1	1	52	4	1	10	2	66				TNZ	JEJ5		61280	
1	1	1	52	4	1	10	2	66				TNZ	JEJ5		61290	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 122)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	1	1	53	13	1	10	1	376			JF82	CHECK	PIU LOAD SW SEL REG SETS INT 2		61300	
1	1	1	54	12	1	10	036					STU	776		61310	
1	1	1	55	7	1	10	020					PIU	036		61320	
1	1	1	56	5	1	10	154					ACC	ZERO		61330	
1	1	1	57	15	1	10	220	200000000				CIU	154		61340	
1	1	1	60	4	1	10	266					TNZ	JEJ5		61350	
															61360	
1	1	1	61	13	1	10	1	376			JF02	PERFORM	DIODF TESTS		61370	
1	1	1	62	5	1	10	014					STG	776		61380	
1	1	1	63	12	1	10	037					CIU	014		61390	
1	1	1	64	12	1	10	034					PIU	037	RST INT 2	61400	
1	1	1	65	12	1	10	032					PIU	034		61410	
1	1	1	66	12	1	10	026					PIU	032		61420	
1	1	1	67	12	1	10	016					PIU	026		61430	
1	1	1	70	12	1	10	076					PIU	016		61440	
1	1	1	71	12	1	10	136					PIU	076		61450	
1	1	1	72	17	1	10	1	054				PIU	136		61460	
1	1	1	73	14	1	10	1	076				CLA	LC8		61470	
1	1	1	74	17	1	10	1	020				TNI	**3		61480	
1	1	1	75	5	1	10	036					CLA	ZERO		61490	
1	1	1	76	5	1	10	034					CIU	036		61500	
1	1	1	77	5	1	10	154					CIU	034	RESET INT 6	61510	
1	1	1	100	4	1	10	266					CIU	154		61520	
															61530	
1	1	1	101	13	1	10	1	376			JFF2	CHECK	PIU READ INTERRUPT REGISTER SET INT 8		61540	
1	1	1	102	12	1	10	137					STU	776		61550	
1	1	1	103	7	1	10	020					PIU	137		61560	
1	1	1	104	5	1	10	154					ACC	ZERO		61570	
1	1	1	105	15	1	10	017	002000000				CIU	154		61580	
1	1	1	106	4	1	10	266					XOR	=0002000000		61590	
															61600	
1	1	1	107	13	1	10	1	376			JFH2	PERFORM	NEGATIVE TESTS		61610	
1	1	1	110	5	1	10	044					STU	776		61620	
1	1	1	111	12	1	10	135					CIU	044	RST INT 8	61630	
1	1	1	112	12	1	10	133					PIU	135		61640	
1	1	1	113	12	1	10	127					PIU	133		61650	
1	1	1	114	12	1	10	117					PIU	127		61660	
1	1	1	115	12	1	10	177					PIU	117		61670	
1	1	1	116	5	1	10	137					PIU	177		61680	
1	1	1	117	5	1	10	034					CIU	137		61690	
1	1	1	120	5	1	10	154					CIU	034	RESET INT 6	61700	
1	1	1	121	4	1	10	266					CIU	154		61710	
															61720	
1	1	1	122	13	1	10	1	376			JF83	CHECK	PIU READ FINE GIMBAL SETS INT 9		61730	
1	1	1	123	12	1	10	223					STU	776		61740	
1	1	1	124	7	1	10	020					PIU	223		61750	
1	1	1	125	5	1	10	154					ADL	ZERO		61760	
1	1	1	126	15	1	10	221	001000000				CIU	154		61770	
1	1	1	127	4	1	10	266					XOR	=0001000000		61780	
1	1	1	130	13	1	10	1	376			JF03	PERFORM	DIODF TESTS		61790	
1	1	1	131	5	1	10	050					STU	776		61800	
1	1	1	132	12	1	10	227					CIU	050	RST INT 9	61810	
1	1	1	133	7	1	10	020					PIU	227		61820	
1	1	1	134	5	1	10	154					ADL	ZERO		61830	
1	1	1	135	15	1	10	221	001000000				CIU	154		61840	
1	1	1	136	4	1	10	266					XOR	=0001000000		61850	
															61860	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 123)

IM	IS	S	LDC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NO
1	1	1	137	13	1	10	1	376			JFF3	STC	776		61870
1	1	1	140	5	1	10	050					CIO	050	RST INT 9	61880
1	1	1	141	12	1	10	353					P10	353		61890
1	1	1	142	7	1	10	020					ADC	ZERO		61900
1	1	1	143	5	1	10	154					CIO	154		61910
1	1	1	144	15	1	10	221	001000000				XOR	=0001C00000		61920
1	1	1	145	4	1	10	266					TNZ	JEJ5		61930
1	1	1	146	13	1	10	376				JFH3	STC	776		61940
1	1	1	147	5	1	10	050					CIO	050	RST INT 9	61950
1	1	1	150	12	1	10	363					P10	363		61960
1	1	1	151	7	1	10	020					ADC	ZERO		61970
1	1	1	152	5	1	10	154					CIO	154		61980
1	1	1	153	15	1	10	221	001000000				XOR	=0001C00000		61990
1	1	1	154	4	1	10	266					TNZ	JEJ5		62000
1	1	1	155	13	1	10	376				JFB4	STC	776		62010
1	1	1	156	5	1	10	050					CIO	050	RST INT 9	62020
1	1	1	157	12	1	10	222					P10	222		62030
1	1	1	160	12	1	10	221					P10	221		62040
1	1	1	161	5	1	10	223					CIO	223		62050
1	1	1	162	12	1	10	303					P10	303		62060
1	1	1	163	12	1	10	313					P10	313		62070
1	1	1	164	12	1	10	317					P10	317		62080
1	1	1	165	12	1	10	253					P10	253		62090
1	1	1	166	12	1	10	263					P10	263		62100
1	1	1	167	12	1	10	373					P10	373		62110
1	1	1	170	12	1	10	357					P10	357		62120
1	1	1	171	12	1	10	323					P10	323		62130
1	1	1	172	12	1	10	367					P10	367		62140
1	1	1	173	12	1	10	203					P10	203		62150
1	1	1	174	12	1	10	213					P10	213		62160
1	1	1	175	5	1	10	034					CIO	034	RESET INT 6	62180
1	1	1	176	5	1	10	154					CIO	154		62190
1	1	1	177	4	1	10	266					TNZ	JEJ5		62200
1	1	1	200	13	1	10	376				JFF4	STC	776		62210
1	1	1	201	12	1	10	243					P10	243		62220
1	1	1	202	7	1	10	020					ADC	ZERO		62230
1	1	1	203	5	1	10	154					CIO	154		62240
1	1	1	204	15	1	10	222	000400000				XOR	=0000400000		62250
1	1	1	205	4	1	10	266					TNZ	JEJ5		62260
1	1	1	206	13	1	10	376				JFH4	STC	776		62270
1	1	1	207	5	1	10	054					CIO	054	RST INT 10	62280
1	1	1	210	12	1	10	343					P10	343		62290
1	1	1	211	7	1	10	020					ADC	ZERO		62300
1	1	1	212	5	1	10	154					CIO	154		62310
1	1	1	213	15	1	10	222	000400000				XOR	=0000400000		62320
1	1	1	214	4	1	10	266					TNZ	JEJ5		62330
1	1	1	215	13	1	10	376				JFB5	STC	776		62340
1	1	1	216	5	1	10	054					CIO	054	RST INT 10	62350
1	1	1	217	12	1	10	233					P10	233		62360
1	1	1	220	7	1	10	020					ADC	ZERO		62370
1	1	1	221	5	1	10	154					CIO	154		62380
1	1	1	222	15	1	10	222	000400000				XOR	=0000400000		62390
1	1	1	223	4	1	10	266					TNZ	JEJ5		62400
1	1	1	224	13	1	10	376				JFD5	STC	776		62420
1	1	1	225	5	1	10	054					CIO	054	RST INT 10	62430

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 124)

IM IS S LOC	UP DM DS 9	ADR	OCT VAL	LHS	OPC	VARIABLE	COMMENT	SEG NO
1 1 1 226	12	1 10	333		PIO	333		62440
1 1 1 227	7	1 10	020		ADD	ZERO		62450
1 1 1 230	5	1 10	154		CIO	154		62460
1 1 1 231	15	1 10	222		XOR	-0000400000		62470
1 1 1 232	4	1 10	266		TNZ	JEJ5		62480
1 1 1 233	13	1 10	1 376	JFF5	PERFORM	DIODE TESTS		62490
1 1 1 234	5	1 10	054		STO	776	RST INT 10	62500
1 1 1 235	12	1 10	247		CIO	054		62510
1 1 1 236	12	1 10	347		PIO	247		62520
1 1 1 237	12	1 10	237		PIO	347		62530
1 1 1 240	12	1 10	273		PIO	237		62540
1 1 1 241	12	1 10	340		PIO	273		62550
1 1 1 242	12	1 10	337		PIO	340		62560
1 1 1 243	12	1 10	043		PIO	337		62570
1 1 1 244	5	1 10	034		PIO	043		62580
1 1 1 245	5	1 10	154		CIO	034	RESET INT 6	62590
1 1 1 246	4	1 10	266		CIO	154		62600
1 1 1 246	4	1 10	266		TNZ	JEJ5		62610
1 1 1 247	13	1 10	1 376	JG81	CHECK	PIO READ SW SEL REG SETS INT 11		62650
1 1 1 250	12	1 10	077		STU	776		62660
1 1 1 251	7	1 10	020		PIO	077		62670
1 1 1 252	5	1 10	154		ADD	ZERO		62680
1 1 1 253	15	1 10	223		CIO	154		62690
1 1 1 254	4	1 10	266		XOR	-0000200000		62700
1 1 1 255	13	1 10	1 376	JG01	CHECK	PIO READ DIN REG SETS INT 12		62710
1 1 1 256	5	1 10	060		STU	776		62720
1 1 1 257	12	1 10	057		CIO	060	RST INT 11	62730
1 1 1 260	7	1 10	020		PIO	057		62740
1 1 1 261	5	1 10	154		ACC	ZERO		62750
1 1 1 262	15	1 10	224		CIO	154		62760
1 1 1 263	4	1 10	266		XOR	-0000100000		62770
1 1 1 264	13	1 10	1 376	JG61	CHECK	PIO READ EM REG SETS INT 13		62780
1 1 1 265	5	1 10	064		STU	776		62790
1 1 1 266	12	1 10	023		CIO	064	RST INT 12	62800
1 1 1 267	7	1 10	020		PIO	023		62810
1 1 1 270	5	1 10	154		ACC	ZERO		62820
1 1 1 271	15	1 10	225		CIO	154		62830
1 1 1 272	4	1 10	266		XOR	-0000040000		62840
1 1 1 273	13	1 10	1 376	JG61	CHECK	PIO READ TEL SCANNER SETS INT 14		62850
1 1 1 274	5	1 10	070		STU	776		62860
1 1 1 275	5	1 10	220		CIO	070	RST INT 13	62870
1 1 1 276	6	1 10	226		CIO	220	READ B SWITCHES	62880
1 1 1 277	4	1 10	1 305		ANC	-0100000000	BZ	62890
1 1 1 300	12	1 10	067		TNZ	JG82		62900
1 1 1 301	7	1 10	020		PIO	067		62910
1 1 1 302	5	1 10	154		ADD	ZERO		62920
1 1 1 303	15	1 10	004		CIO	154		62930
1 1 1 304	4	1 10	266		XOR	-0000020000		62940
1 1 1 305	13	1 10	1 376	JG82	CHECK	DIODE TESTS		62950
1 1 1 305	13	1 10	1 376		STU	776		62960

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 125)

IM	IS	S	LDC	OP	DM	DS	9	ADR	OCT	VAL	LHS	UPC	VARIABLE	COMMENT	SEQ	NO
1	1	1	306	5	1	10	074					C10	074	RST INT 14	63010	
1	1	1	307	12	1	10	073					P10	073		63030	
1	1	1	310	12	1	10	075					P10	075	SETS INT 6	63040	
1	1	1	311	12	1	10	157					P10	157		63050	
1	1	1	312	12	1	10	257					P10	257		63060	
1	1	1	313	12	1	10	047					P10	047		63070	
1	1	1	314	12	1	10	017					P10	017		63080	
1	1	1	315	12	1	10	053					P10	053		63090	
1	1	1	316	12	1	10	056					P10	056		63100	
1	1	1	317	12	1	10	123					P10	123		63110	
1	1	1	320	12	1	10	003					P10	003		63120	
1	1	1	321	12	1	10	063					P10	063		63130	
1	1	1	322	12	1	10	033					P10	033		63140	
1	1	1	323	12	1	10	021					P10	021		63150	
1	1	1	324	12	1	10	022					P10	022	SETS INT 6	63160	
1	1	1	325	12	1	10	027					P10	027		63170	
1	1	1	326	12	1	10	167					P10	167		63180	
1	1	1	327	12	1	10	267					P10	267		63190	
1	1	1	330	12	1	10	047					P10	047		63200	
1	1	1	331	12	1	10	027					P10	027		63210	
1	1	1	332	12	1	10	066					P10	066		63220	
1	1	1	333	12	1	10	065					P10	065	SET INT 6	63230	
1	1	1	334	12	1	10	063					P10	063		63240	
1	1	1	335	5	1	10	034					C10	034		63250	
1	1	1	336	5	1	10	023					C10	023		63260	
1	1	1	337	7	1	10	020					ADC	ZERO		63270	
1	1	1	340	5	1	10	154					C10	154		63280	
1	1	1	341	4	1	10	266					TNZ	JEJ5		63290	
1	1	1	342	00	1	10	227	501006020				TRA*	JH1		63300	
1	2	0	14	1	10	42						ORG	1,2,0,14,1,10,		63310	
1	2	0	14	17	1	10	020					CLA	ZERO	CHECK NASA INT 1 AND 2, NDI 1-6	63320	
1	2	0	15	13	1	10	1376				JH81	STO	776		63330	
1	2	0	16	5	1	10	032					C10	032		63340	
1	2	0	17	13	1	10	1377				JH1	STO	777	LOAD NA DIS REG	63350	
1	2	0	20	17	1	10	1377					CLA	777		63360	
1	2	0	21	13	1	10	1073					STC	VAR4		63370	
1	2	0	22	7	1	10	1073					ADC	ZERO		63380	
1	2	0	23	5	1	10	154					C10	154		63390	
1	2	0	24	4	1	10	153					TNZ	JHJ5		63400	
1	2	0	25	13	1	10	1377					STO	777		63410	
1	2	0	26	17	1	10	1377					CLA	777		63420	
1	2	0	27	13	1	10	1073					STO	V4		63430	
1	2	0	30	5	1	10	214					C10	214		63440	
1	2	0	31	6	1	10	230	000001760				AND	=0000001760		63450	
1	2	0	32	4	1	10	153					TNZ	JHJ5		63460	
1	2	0	33	13	1	10	1376					STO	776		63470	
1	2	0	34	17	1	10	035	000000524				CLA	=000000524		63480	
1	2	0	35	5	1	10	032					C10	032		63490	
1	2	0	36	13	1	10	1377					STO	777		63500	
1	2	0	37	17	1	10	1377					CLA	777		63510	
1	2	0	40	13	1	10	1073					STO	V4		63520	
1	2	0	41	7	1	10	1020					ADC	ZERO		63530	
1	2	0	42	5	1	10	154					C10	154		63540	
1	2	0	43	15	1	10	231	040000000				XOR	=0040000000	INT 4	63550	
1	2	0	44	4	1	10	153					TNZ	JHJ5		63570	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 126)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	2	0	45	13	1	10	1	377			JHG1	STO	777		63580	
1	2	0	46	17	1	10	1	377				CLA	777		63590	
1	2	0	47	13	1	10	1	073				STO	V4		63600	
1	2	0	50	5	1	10	214					CIO	214		63610	
1	2	0	51	6	1	10	230		000001760			ANC	=000001760		63620	
1	2	0	52	15	1	10	232		000001240			XOR	=000001240	DI 2,4,6	63630	
1	2	0	53	4	1	10	153					TNZ	JHJ5		63640	
1	2	0	54	13	1	10	1376				JH82	STU	776		63650	
1	2	0	55	17	1	10	020					CLA	ZERO		63660	
1	2	0	56	5	1	10	032					CIO	032		63670	
1	2	0	57	5	1	10	024					CIO	024		63680	
1	2	0	60	17	1	10	036		000000252			CIO	=000000252	RST 4	63690	
1	2	0	61	5	1	10	032					CLA	032		63700	
1	2	0	62	13	1	10	1377				JHC2	STO	777		63710	
1	2	0	63	17	1	10	1377					CLA	777		63720	
1	2	0	64	13	1	10	073					STU	V4		63730	
1	2	0	65	7	1	10	020					ADD	ZERO		63740	
1	2	0	66	5	1	10	154					CIO	154		63750	
1	2	0	67	15	1	10	226		100000000			CIO	=010000000	INT 3	63760	
1	2	0	70	4	1	10	153					TNZ	JHJ5		63770	
1	2	0	71	13	1	10	1377				JHD2	STO	777		63780	
1	2	0	72	17	1	10	1377					CLA	777		63790	
1	2	0	73	13	1	10	073					STU	V4		63800	
1	2	0	74	5	1	10	214					CIO	214		63810	
1	2	0	75	6	1	10	230		000001760			ANC	=000001760		63820	
1	2	0	76	15	1	10	233		000000520			XOR	=000000520	DI 1,3,5	63830	
1	2	0	77	4	1	10	153					TNZ	JHJ5		63840	
1	2	0	100	13	1	10	1376				JHE2	STO	776		63850	
1	2	0	101	17	1	10	020					CLA	ZERO		63860	
1	2	0	102	5	1	10	032					CIO	032		63870	
1	2	0	103	5	1	10	020					CIO	020		63880	
1	2	0	104	17	1	10	234		000000630			CLA	=000000630	RESET INT 3	63890	
1	2	0	105	5	1	10	032					CIO	032		63900	
1	2	0	106	13	1	10	1377				JHF2	STO	777		63910	
1	2	0	107	17	1	10	1377					CLA	777		63920	
1	2	0	110	13	1	10	073					STU	V4		63930	
1	2	0	111	7	1	10	020					ADD	ZERO		63940	
1	2	0	112	5	1	10	154					CIO	154		63950	
1	2	0	113	4	1	10	153					TNZ	JHJ5		63960	
1	2	0	114	13	1	10	1377		000001760			ANC	=000001760		63970	
1	2	0	115	17	1	10	1377		000001460			XOR	=000001460	DI 1,2,5,6	64010	
1	2	0	116	13	1	10	073					TNZ	JHJ5		64020	
1	2	0	117	5	1	10	214					STU	V4		64030	
1	2	0	120	6	1	10	230		000001760			ANC	=000001760		64040	
1	2	0	121	15	1	10	235		000001460			XOR	=000001460		64050	
1	2	0	122	4	1	10	153				JH83	STO	776		64060	
1	2	0	123	13	1	10	1376					CLA	=000000146		64070	
1	2	0	124	17	1	10	236		000000146			CLA	=000000146		64080	
1	2	0	125	5	1	10	032					CIO	032		64090	
1	2	0	126	13	1	10	1377				JHC3	STU	777		64100	
1	2	0	127	17	1	10	1377					CLA	777		64110	
1	2	0	130	13	1	10	073					STU	V4		64120	
1	2	0	131	7	1	10	020					ADD	ZERO		64130	
1	2	0	132	5	1	10	154					CIO	154		64140	
1	2	0	133	15	1	10	237		140000000			XOR	=014000000	INT 3,4	64150	
1	2	0	134	4	1	10	153					TNZ	JHJ5		64160	
1	2	0	135	13	1	10	1377				JHD3	STU	777		64170	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 127)

IM	IS	S	LOC	OP	DM	DS	9	ADR	DCI	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NO
1	2	0	136	17	1	10	1	377				CLA	777		64150
1	2	0	137	13	1	10	1	073				STO	V4		64160
1	2	0	140	5	1	10	1	214				CIO	ZL4		64170
1	2	0	141	6	1	10	230		000001760			AND	=0C00001760		64180
1	2	0	142	15	1	10	240		000000300			XOR	=000000300	DI 3+4	64190
1	2	0	143	4	1	10	153					TNZ	JHJ5		64200
1	2	0	144	17	1	10	1	020			JHE3	CLA	ZERO		64210
1	2	0	145	5	1	10	032					CIO	032		64220
1	2	0	146	13	1	10	1	073				STO	V4		64230
1	2	0	147	5	1	10	020					CIO	020		64240
1	2	0	150	5	1	10	024					CIO	024		64250
1	2	0	151	5	1	10	110					CIO	110		64260
1	2	0	152	10	1	10	155					TRA	JJ81		64270
1	2	0	153	13	1	10	1	377			JHJ5	STO	777		64280
1	2	0	154	00	1	10	215		501047600			TRA*	JAJ5A		64290
											*			CHECK OF TSYNC/GCSYNC CIRCUITRY	64300
											*			CORRECT OPERATION MONITORED BY OSCILLOSCOPE ONLY	64310
1	2	0	155	17	1	10	241		677777776		JJ81	CLA	=0677777776		64330
1	2	0	156	5	1	10	072					CIO	072	SET 1 TSYNC PULSE	64340
1	2	0	157	17	1	10	242		000000014			CLA	=0000000014		64350
1	2	0	160	2	1	10	1	032				SUB	K1		64360
1	2	0	161	4	1	10	160					TNZ	*-1		64370
1	2	0	162	17	1	10	243		277777776			CLA	=0277777776	ATTEMPT SOLID TSYNC RESET - DIODE CHK	64380
1	2	0	163	5	1	10	072					CIO	072		64390
1	2	0	164	17	1	10	242		000000014			CLA	=0C00000014		64400
1	2	0	165	2	1	10	1	032				SUB	K1		64410
1	2	0	166	4	1	10	165					TNZ	*-1		64420
1	2	0	167	17	1	10	241		677777776			CLA	=0677777776		64430
1	2	0	170	5	1	10	072					CIO	072	SELECT TSYNC MODE	64440
1	2	0	171	5	1	10	102					CIO	102	SET 240 PPS ON TSYNC	64450
1	2	0	172	17	1	10	242		000000014			CLA	=0000000014		64460
1	2	0	173	2	1	10	1	032				SUB	*-1		64470
1	2	0	174	4	1	10	173					TNZ	*-1		64480
1	2	0	175	17	1	10	243		277777776			CLA	=0277777776		64490
1	2	0	176	5	1	10	072					CIO	072	ATTEMPT EARLY RESET -DIODE CHK	64500
1	2	0	177	17	1	10	244		000000334			CLA	=0000000334		64510
1	2	0	200	2	1	10	1	032				SUB	K1		64520
1	2	0	201	4	1	10	200					TNZ	*-1	COUNT 220 DEC WORD TIMES	64530
1	2	0	202	17	1	10	241		677777776			CLA	=0677777776	RESET 240 PPS ON TSYNC	64540
1	2	0	203	5	1	10	072					CIO	072		64550
1	2	0	204	17	1	10	242		000000014			CLA	=0000000014		64560
1	2	0	205	2	1	10	1	032				SUB	K1		64570
1	2	0	206	4	1	10	205					TNZ	*-1		64580
1	2	0	207	17	1	10	002		777777776			CLA	=0777777776	SET SOLID TSYNC	64590
1	2	0	210	5	1	10	072					CIO	072		64600
1	2	0	211	17	1	10	062		000000004		JJ83	CLA	=0000000004	ATTEMPT SOLID TSYNC RESET - DIODE CHK	64610
1	2	0	212	5	1	10	076					CIO	076		64620
1	2	0	213	2	1	10	1	032				SUB	*-1	COUNT 6 DEC WORD TIMES	64630
1	2	0	214	4	1	10	213					TNZ	*-1		64640
1	2	0	215	17	1	10	243		277777776			CLA	=0277777776	RESET SOLID TSYNC	64650
1	2	0	216	5	1	10	072					CIO	072		64660
1	2	0	217	7	1	10	1	020				ADC	ZERO		64670
1	2	0	220	17	1	10	245		537777776			CLA	=0537777776	DIODE CHK	64680
1	2	0	221	5	1	10	076					CIO	076		64690
1	2	0	222	7	1	10	1	020				ADC	ZERO		64700
1	2	0	223	7	1	10	1	020				ADC	ZERO		64710

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 128)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	2	0	224	5	1	10		220					TO LOOP ON TSYNC PLACE 85 SWITCH UP		64720	
1	2	0	225	6	1	10		217	010000000			CIO	220		64730	
1	2	0	226	4	1	10		155				AND	=001		64740	
1	2	0	227	17	1	10		246	737777776	JK81		TNZ	JJ81		64750	
1	2	0	230	5	1	10		076				CLA	=0737777776		64760	
1	2	0	231	17	1	10		242	000000014			CLA	076	SET I GCSYNC PULSE	64770	
1	2	0	232	2	1	10		032				SUB	K1		64780	
1	2	0	233	4	1	10		232				TNZ	*-1		64790	
1	2	0	234	17	1	10		245	537777776			CLA	=0537777776		64800	
1	2	0	235	5	1	10		076				CIO	076		64810	
1	2	0	236	17	1	10		242	000000014			CLA	=0000000014	ATTEMPT SOLID GCSYNC RESET -DIODE CHK	64820	
1	2	0	237	2	1	10		032				SUB	K1		64830	
1	2	0	240	4	1	10		237				TNZ	*-1		64840	
1	2	0	241	17	1	10		246	737777776			CLA	=0737777776		64850	
1	2	0	242	5	1	10		076				CIO	076		64860	
1	2	0	243	5	1	10		102				CIO	102		64870	
1	2	0	244	17	1	10		242	000000014			CLA	=0000000014	SELECT GCSYNC MODE	64880	
1	2	0	245	2	1	10		032				SUB	K1	SET 240 PPS ON GCSYNC	64890	
1	2	0	246	4	1	10		245				TNZ	*-1		64900	
1	2	0	247	17	1	10		245	537777776			CLA	=0537777776		64910	
1	2	0	250	5	1	10		076				CIO	076		64920	
1	2	0	251	17	1	10		244	000000334			CLA	=0000000334	ATTEMPT EARLY RESET - DIODE CHK	64930	
1	2	0	252	2	1	10		032				SUB	K1		64940	
1	2	0	253	4	1	10		252				TNZ	*-1	COUNT 220 DECIMAL WORD TIMES	64950	
1	2	0	254	17	1	10		246	737777776			CLA	=0737777776		64960	
1	2	0	255	5	1	10		076				CIO	076	RESET 240 PPS ON GCSYNC	64970	
1	2	0	256	17	1	10		242	000000014			CLA	=0000000014		64980	
1	2	0	257	2	1	10		032				SUB	K1		64990	
1	2	0	260	4	1	10		257				TNZ	*-1		65010	
1	2	0	261	17	1	10		002	777777776			CLA	=0777777776		65020	
1	2	0	262	5	1	10		076				CIO	076	SET SOLID GCSYNC	65030	
1	2	0	263	17	1	10		062	000000004	JK83		CLA	=0000000004		65040	
1	2	0	264	5	1	10		072				CIO	072	ATTEMPT SOLID GCSYNC RESET -DIODE CHK	65050	
1	2	0	265	2	1	10		032				SUB	K1		65060	
1	2	0	266	4	1	10		265				TNZ	*-1	COUNT 6 DEC WORD TIMES	65070	
1	2	0	267	17	1	10		245	537777776			CLA	=0537777776		65080	
1	2	0	270	5	1	10		076				CIO	076	RESET SOLID GCSYNC	65090	
1	2	0	271	7	1	10		020				ADC	ZERO		65100	
1	2	0	272	17	1	10		243	277777776			CLA	=0277777776		65110	
1	2	0	273	5	1	10		072				CIO	072	DIODE CHK	65120	
													TO LOOP ON GCSYNC PLACE 86 SWITCH UP		65130	
1	2	0	274	5	1	10		220				CIO	220		65140	
1	2	0	275	6	1	10		247	004000000			AND	=0004		65150	
1	2	0	276	4	1	10		227				TNZ	JK81		65160	
1	2	0	277	00	1	10		250	511006220			TRA*	JL81		65170	
1	2	1	14		1	11		40					ORG 1,2,1,14,1,11, CHECK ACCELEROMETER SIMULATOR	65190		
													CHECK PLUS STEP FROM Q+R=0	65200		
1	2	1	14	17	1	11		040				CLA	HJ81		65210	
1	2	1	15	13	1	11		376				STU	776		65220	
1	2	1	16	13	1	11		40	51105620	HJ81		HPC	JM81		65230	
1	2	1	17	17	1	11		071				STU	V2		65240	
1	2	1	17	17	1	11		000	777777776			CLA	=0777777776	ENABLE COMPARE	65250	
1	2	1	20	5	1	11		066				CIO	066	SET ACCEL SIGNS PLUS	65260	
1	2	1	21	5	1	11		132				CIO	132		65280	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 129)

IM	IS	S	LDC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NO
1	2	1	22	5	1	11	1	126				C10	126	SET SUBTRACT INHIBIT	65290
1	2	1	23	17	1	11	1	030				CLA	HJAJ5		65300
1	2	1	24	13	1	11	1	004				STU	404		65310
1	2	1	25	17	1	11	1	020				CLA	ZERO		65320
1	2	1	26	5	1	11	1	052				C10	052	LOAD OPT REG Q+R=0	65330
1	2	1	27	5	1	11	1	121				C10	121	CHECK OPT REG LOAD	65340
1	2	1	30	17	1	11	1	001	0015000016			CLA	=0001500016		65350
1	2	1	31	5	1	11	1	136				C10	136	LOAD X CHAN CTR	65360
1	2	1	32	5	1	11	1	142				C10	142	LOAD Y CHAN CTR	65370
1	2	1	33	17	1	11	1	002	002540000			CLA	=0002540000		65380
1	2	1	34	5	1	11	1	146				C10	146	LOAD Z CHAN CTR	65390
1	2	1	35	5	1	11	1	126				C10	126	RESET SUBTRACT INHIBIT	65400
1	2	1	36	17	1	11	1	003	0000000040			CLA	=0000000040	RST INT 5 INHIBIT	65410
1	2	1	40	7	1	11	1	020				C10	004		65420
1	2	1	41	17	1	11	1	041				ADD	ZERO		65430
1	2	1	42	13	1	11	1	004	511023620		HJL82	CLA	HJL82		65440
1	2	1	43	17	1	11	1	020				HPC	JL82		65450
1	2	1	44	5	1	11	1	121				STU	404		65460
1	2	1	45	5	1	11	1	121				CLA	ZERO		65470
1	2	1	46	10	1	11	1	131			JLK1	C10	121	COMPARE	65480
1	2	1	47	13	1	11	1	377			JL82	C10	121	NO COMPARE - INT 5	65490
1	2	1	50	13	1	11	1	076				TRA	JLJ5		65500
1	2	1	51	17	1	11	1	021				STU	777		65510
1	2	1	52	5	1	11	1	126				TEMP	TEMP		65520
1	2	1	53	5	1	11	1	030				BB	BB		65530
1	2	1	54	5	1	11	1	110				CLA	126	INH X CHAN SUBTRACT	65540
1	2	1	55	17	1	11	1	377				C10	030	RESET INT 5	65550
1	2	1	56	13	1	11	1	073				C10	110	RESET MAIN INT LATCH	65560
1	2	1	57	15	1	11	1	042				CLA	777		65570
1	2	1	60	4	1	11	1	132	511023220		HJLK1	XOR	V4	CORRECT ENTRY LOCATION	65580
1	2	1	61	17	1	11	1	076				HPC	HJLK1		65590
1	2	1	62	15	1	11	1	004				JL83	JLK1		65600
1	2	1	63	4	1	11	1	131	000012000			CLA	TEMP		65610
1	2	1	64	17	1	11	1	043				CLA	TEMP	X CHAN STEP FROM 00 TO 10	65620
1	2	1	65	13	1	11	1	004				XOR	JLJ5		65630
1	2	1	66	17	1	11	1	004				TNZ	JLJ5		65640
1	2	1	67	5	1	11	1	121				CLA	JL84		65650
1	2	1	70	5	1	11	1	131				HPC	JL84		65660
1	2	1	71	10	1	11	1	131				STU	404		65670
1	2	1	72	13	1	11	1	377				STU	404		65680
1	2	1	73	13	1	11	1	076				CLA	=000001200		65690
1	2	1	74	5	1	11	1	030				C10	121	COMPARE	65700
1	2	1	75	5	1	11	1	110				C10	121	NO COMPARE - INT 5	65710
1	2	1	76	17	1	11	1	377			JLJ2	TRA	JLJ5	RESET INT 5	65720
1	2	1	77	13	1	11	1	073			JL84	STU	777	RESET MAIN INT LATCH	65730
1	2	1	100	15	1	11	1	044				CLA	777		65740
1	2	1	101	4	1	11	1	132	511034620		HJLJ2	XOR	V4	CORRECT ENTRY LOCATION	65750
1	2	1	102	17	1	11	1	076				HPC	HJLJ2		65760
1	2	1	103	15	1	11	1	005				TNZ	JL83		65770
1	2	1	104	4	1	11	1	131	000012500			CLA	TEMP		65780
1	2	1	105	17	1	11	1	045				XOR	=0000012500	Y CHAN STEP FROM 00 TO 10	65800
1	2	1	105	4	1	11	1	131				TNZ	JLJ5		65810
1	2	1	105	17	1	11	1	045				CLA	HJL85		65820
1	2	1	105	15	1	11	1	045	511045620		HJL85	HPC	JL85		65830
1	2	1	105	4	1	11	1	045				CLA	JL85		65840
1	2	1	105	15	1	11	1	045				HPC	JL85		65850

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 130)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	2	1	106	13	1	11	1	004				STO	404		65860	
1	2	1	107	17	1	11	1	005	000012500			CLA	=0000012500	COMPARE	65870	
1	2	1	110	5	1	11	1	121				CIO	121	NO COMPARE - INT 5	65880	
1	2	1	111	5	1	11	1	121			JLJ4	CIO	121		65890	
1	2	1	112	10	1	11	1	131			JLJ5	TRA	JLJ5		65900	
1	2	1	113	13	1	11	1	377			JL85	STU	777		65910	
1	2	1	114	13	1	11	1	076				STU	TEMP	RESET INT 5	65920	
1	2	1	115	5	1	11	1	030				CIO	030	RESET MAIN INT LATCH	65930	
1	2	1	116	5	1	11	1	110				CIO	110		65940	
1	2	1	117	17	1	11	1	377				STU	777		65950	
1	2	1	120	13	1	11	1	073				CLA	V4	CORRECT ENTRY LOCATION	65960	
1	2	1	121	15	1	11	1	046	511045220		HJLJ4	XOR	HJLJ4		65970	
1	2	1	122	4	1	11	1	132				HPC	JLJ4		65980	
1	2	1	123	17	1	11	1	076				TNZ	JL83		65990	
1	2	1	124	15	1	11	1	006	000012524			CLA	TEMP	Z CHAN STEP FROM 00 TO 10	66000	
1	2	1	125	4	1	11	1	131				XOR	=000012524		66010	
1	2	1	126	17	1	11	1	033				TNZ	JLJ5		66020	
1	2	1	127	5	1	11	1	126				CLA	K77	SET SUBTRACT INHIBIT	66030	
1	2	1	130	10	1	11	1	133			JLJ5	TRA	JM81		66040	
1	2	1	131	13	1	11	1	076			JL83	STO	JM81		66050	
1	2	1	132	0	1	11	1	031			*	HOP	HJAJ58		66060	
1	2	1	133	13	1	11	1	376			JM81	STU	776	CHECK PLUS STEP FROM Q=L,R=0	66070	
1	2	1	134	17	1	11	1	047	5111121620		HJN81	CLA	HJN81		66080	
1	2	1	135	13	1	11	1	071				HPC	JM81		66090	
1	2	1	136	17	1	11	1	030				V2	V2		66100	
1	2	1	137	13	1	11	1	004				CLA	HJAJ5		66110	
1	2	1	140	17	1	11	1	006	000012524			STU	404		66120	
1	2	1	141	5	1	11	1	052				CLA	052	LOAD OPT REG Q=L,R=0	66130	
1	2	1	142	5	1	11	1	121				CIO	052	CHECK OPT REG LOAD	66140	
1	2	1	143	17	1	11	1	007	000340064			CLA	=0000340064		66150	
1	2	1	144	5	1	11	1	136				CIO	136	LOAD X CHAN CTR	66160	
1	2	1	145	5	1	11	1	142				CIO	142	LOAD Y CHAN CTR	66170	
1	2	1	146	17	1	11	1	002	002540000			CLA	=0002540000		66180	
1	2	1	147	5	1	11	1	146				CIO	146	LOAD Z CHAN CTR	66190	
1	2	1	150	5	1	11	1	020				ADD	ZERO	RESET SUBTRACT INHIBIT	66200	
1	2	1	151	7	1	11	1	020				ADD	ZERO		66210	
1	2	1	152	7	1	11	1	020				ADD	ZERO		66220	
1	2	1	153	7	1	11	1	020				ADD	ZERO		66230	
1	2	1	154	17	1	11	1	050	511071220		HJM82	CLA	HJM82		66240	
1	2	1	155	13	1	11	1	004				HPC	404		66250	
1	2	1	156	17	1	11	1	006	000012524			CLA	=0000012524	COMPARE	66260	
1	2	1	157	5	1	11	1	121				CIO	121	NO COMPARE - INT 5	66270	
1	2	1	160	5	1	11	1	121				CIO	121		66280	
1	2	1	161	10	1	11	1	131			JM81	TRA	JLJ5		66290	
1	2	1	162	13	1	11	1	377			JM82	STO	777		66300	
1	2	1	163	13	1	11	1	076				STO	TEMP		66310	
1	2	1	164	17	1	11	1	010	000000004			CLA	=0000000004		66320	
1	2	1	165	5	1	11	1	126				CIO	126	INH Y CHAN SUBTRACT	66330	
1	2	1	166	5	1	11	1	030				CIO	030	RESET INT 5	66340	
1	2	1	167	5	1	11	1	110				CIO	110	RESET MAIN INT LATCH	66350	
1	2	1	170	17	1	11	1	377				CLA	777		66360	
1	2	1	171	13	1	11	1	073				STU	V4		66370	
1	2	1	172	15	1	11	1	051			HJM81	XOR		CORRECT ENTRY LOCATION	66380	
															66390	
															66400	
															66410	
															66420	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 131)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	2	1	173	4	1	11	1	51	511070620		HJMK1	HPC	JMK1		66430	
1	2	1	174	17	1	11	1	132					JL83		66440	
1	2	1	175	15	1	11	1	076	000012764			CLA	TEMP	Y CHAN STEP FROM 10 TO 11	66450	
1	2	1	176	4	1	11	1	011				XOR	=0000012764		66460	
1	2	1	177	17	1	11	1	131				TNZ	JLJ5		66470	
1	2	1	177	17	1	11	1	052	511102620		HJMB3	CLA	HJMB3		66480	
1	2	1	200	13	1	11	1	004				HPC	JMB3		66490	
1	2	1	201	17	1	11	1	011	000012764			CLA	404		66500	
1	2	1	202	5	1	11	1	121				CIO	=0000012764		66510	
1	2	1	203	5	1	11	1	121				CIO	121		66520	
1	2	1	204	10	1	11	1	131			JMJ2	TRA	JLJ5		66530	
1	2	1	205	13	1	11	1	377			JMB3	STU	777		66540	
1	2	1	206	13	1	11	1	076				STU	TEMP		66550	
1	2	1	207	5	1	11	1	030				CIO	030	RESET INT 5	66570	
1	2	1	210	5	1	11	1	110				CIO	110	RESET MAIN INT LATCH	66580	
1	2	1	211	17	1	11	1	377				CLA	777		66590	
1	2	1	212	13	1	11	1	073				STU	V4		66600	
1	2	1	213	15	1	11	1	053	511102220		HJMJ2	XOR	HJMJ2	CORRECT ENTRY LOCATION	66610	
1	2	1	214	4	1	11	1	132				HPC	JMJ2		66620	
1	2	1	215	17	1	11	1	076				TNZ	JL83		66630	
1	2	1	216	15	1	11	1	012	000017764			CLA	TEMP	X CHAN STEP FROM 10 TO 11	66640	
1	2	1	217	4	1	11	1	131				XOR	=0000017764		66650	
1	2	1	220	17	1	11	1	054	511113220		HJMB4	CLA	JLJ5		66660	
1	2	1	221	13	1	11	1	004				HPC	HJMB4		66670	
1	2	1	222	17	1	11	1	012	000017764			STU	404		66680	
1	2	1	223	5	1	11	1	121				CLA	=0000017764		66690	
1	2	1	224	5	1	11	1	121				CIO	121		66700	
1	2	1	225	10	1	11	1	131			JMJ3	TRA	JLJ5		66710	
1	2	1	226	13	1	11	1	377			JMB4	STU	777		66720	
1	2	1	227	13	1	11	1	076				STU	TEMP		66730	
1	2	1	230	5	1	11	1	030				CIO	030	RESET INT 5	66750	
1	2	1	231	5	1	11	1	110				CIO	110	RESET MAIN INT LATCH	66760	
1	2	1	232	17	1	11	1	377				CLA	777		66770	
1	2	1	233	13	1	11	1	073				STU	V4		66780	
1	2	1	234	15	1	11	1	055	511112620		HJMJ3	XOR	HJMJ3	CORRECT ENTRY LOCATION	66790	
1	2	1	235	4	1	11	1	132				HPC	JMJ3		66800	
1	2	1	236	17	1	11	1	076				TNZ	JL83		66820	
1	2	1	237	15	1	11	1	013	000017776			CLA	TEMP	Z CHAN STEP FROM 10 TO 11	66830	
1	2	1	240	4	1	11	1	131				XOR	=0000017776		66840	
1	2	1	241	17	1	11	1	033				TNZ	JLJ5		66850	
1	2	1	242	5	1	11	1	126				CLA	K77		66860	
1	2	1	243	13	1	11	1	376				CIO	126	SET SUBTRACT INHIBIT	66870	
1	2	1	244	17	1	11	1	056			JNB1	STU	776	SET SUBTRACT INHIBIT	66880	
1	2	1	245	13	1	11	1	071				HPC	HJP81		66890	
1	2	1	246	17	1	11	1	030	511010030		HJP81	CLA	JP81		66900	
1	2	1	247	13	1	11	1	004				STU	V2		66910	
1	2	1	250	17	1	11	1	020				CLA	HJAJ5		66930	
1	2	1	251	5	1	11	1	132				CLA	404		66940	
1	2	1	252	17	1	11	1	013				CLA	ZEN0		66950	
1	2	1	253	5	1	11	1	052	000017776			CLA	132	SET ACCEL SIGNS MINUS	66960	
1	2	1	254	5	1	11	1	121				CIO	052	LOAD OPT REG Q#R=1	66970	
1	2	1	254	5	1	11	1	121				CIO	121	CHECK OPT REG LOAD	66990	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 132)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	2	1	255	17	1	11	014		000340000			CLA	=000340000		67000	
1	2	1	256	5	1	11	146					C10	146	LOAD Z CHAN CTR	67010	
1	2	1	257	17	1	11	015		002540064			CLA	=002540064		67020	
1	2	1	260	5	1	11	142					C10	142	LOAD Y CHAN CTR	67030	
1	2	1	261	5	1	11	136					C10	136	LOAD X CHAN CTR	67040	
1	2	1	262	17	1	11	020					CLA	ZERO		67050	
1	2	1	263	5	1	11	126					C10	126	RESET SUBTRACT INHIBIT	67060	
1	2	1	264	7	1	11	020					ADD	ZERO		67070	
1	2	1	265	7	1	11	020					ADD	ZERO		67080	
1	2	1	266	7	1	11	020					ZERO	ZERO		67090	
1	2	1	267	17	1	11	057					CLA	HJNB2		67100	
1	2	1	270	13	1	11	004		511136620		HJNB2	HPC	JNB2		67110	
1	2	1	271	17	1	11	013		000017776			STO	404		67120	
1	2	1	272	5	1	11	121					CLA	=000001776		67130	
1	2	1	273	5	1	11	121					C10	121	COMPARE	67140	
1	2	1	274	10	1	11	131				JNK1	C10	121	NO COMPARE -- INT 5	67150	
1	2	1	275	13	1	11	137				JNB2	TRA	JLJ5		67160	
1	2	1	276	13	1	11	076					STO	TEMP		67170	
1	2	1	277	17	1	11	032					CLA	K1		67180	
1	2	1	300	5	1	11	126					C10	126	INH Z CHAN SUBTRACT	67190	
1	2	1	301	5	1	11	030					C10	030	RESET INT 5	67200	
1	2	1	302	5	1	11	110					C10	110	RESET MAIN INT LATCH	67210	
1	2	1	303	17	1	11	137					CLA	777		67220	
1	2	1	304	13	1	11	073					STO	V4		67230	
1	2	1	305	15	1	11	060					HPC	HJNK1		67240	
1	2	1	306	4	1	11	132		511136220		HJNK1	XOR	JNK1	CORRECT ENTRY LOCATION	67250	
1	2	1	307	17	1	11	076					TNZ	JL83		67260	
1	2	1	310	15	1	11	012		000017764			CLA	TEMP		67270	
1	2	1	311	4	1	11	131					XOR	=0000017764		67280	
1	2	1	312	17	1	11	061					TNZ	JLJ5	Z CHAN STEP FROM I1 TO I0	67290	
1	2	1	313	13	1	11	061					CLA	HJNB3		67300	
1	2	1	314	17	1	11	004		\$11150220		HJNB3	HPC	JNB3		67310	
1	2	1	315	5	1	11	121					STO	404		67320	
1	2	1	316	5	1	11	121					CLA	=0000017764		67330	
1	2	1	317	10	1	11	131					C10	121	COMPARE	67340	
1	2	1	320	13	1	11	137				JNJ2	C10	121	NO COMPARE -- INT 5	67350	
1	2	1	321	13	1	11	076				JNB3	TRA	JLJ5		67360	
1	2	1	322	5	1	11	030					STU	777		67370	
1	2	1	323	5	1	11	110					STU	TEMP		67380	
1	2	1	324	17	1	11	137					C10	030	RESET INT 5	67390	
1	2	1	325	13	1	11	073					C10	110	RESET MAIN INT LATCH	67400	
1	2	1	326	15	1	11	062					CLA	777		67410	
1	2	1	327	4	1	11	132					STO	V4		67420	
1	2	1	330	17	1	11	076		511147620		HJNJ2	XOR	HJNJ2	CORRECT ENTRY LOCATION	67430	
1	2	1	331	15	1	11	011					HPC	JNJ2		67440	
1	2	1	332	4	1	11	131					TNZ	JL83		67450	
1	2	1	333	17	1	11	063		000012764			CLA	TEMP		67460	
1	2	1	334	13	1	11	004					XOR	=0000012764		67470	
1	2	1	335	17	1	11	011					CLA	JLJ5	X CHAN STEP FROM I1 TO I0	67480	
1	2	1	336	5	1	11	121					TNZ	JLJ5		67490	
1	2	1	337	5	1	11	121					CLA	HJNB4		67500	
1	2	1	340	10	1	11	131		511160620		HJNB4	HPC	JNB4		67510	
1	2	1	341	13	1	11	004					STO	404		67520	
1	2	1	342	5	1	11	121		000012764			CLA	=0000012764		67530	
1	2	1	343	5	1	11	121					C10	121	COMPARE	67540	
1	2	1	344	10	1	11	131				JNJ3	TRA	JLJ5	NO COMPARE -- INT 5	67550	
1	2	1	345	10	1	11	131					TRA			67560	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 133)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ
1	2	1	341	13	1	11	1	377			JMB4	STO	777		67570
1	2	1	342	13	1	11	1	076				STO	TEMP		67580
1	2	1	343	5	1	11	030					CIO	030	RESET INT 5	67590
1	2	1	344	5	1	11	110					CIO	110	RESET MAIN INT LATCH	67600
1	2	1	345	17	1	11	1	377				CLA	777		67610
1	2	1	346	13	1	11	1	073				STO	V4	CORRECT ENTRY LOCATION	67620
1	2	1	347	15	1	11	064					XOR	HJNJ3		67630
1	2	1	350	4	1	11	1	132	511160220		HJNJ3	HPC	JNJ3		67640
1	2	1	351	17	1	11	1	076				TNZ	JLB3		67650
1	2	1	352	15	1	11	006					CLA	TEMP		67660
1	2	1	353	4	1	11	1	131	000012524		XOR	-000012524	Y CHAN STEP FROM 11 TO 10	67670	
1	2	1	354	17	1	11	1	033				TNZ	JLJ5		67680
1	2	1	355	5	1	11	1	126				CLA	K77		67690
1	2	1	356	00	1	11	016		5111010030		TRA*	JP81	SET SUBTRACT INHIBIT	67700	
1	3	0	20	17	1	11	65				ORC	1,3,0,20,1,11,		67710	
											•	CHECK	MINUS STEP FROM Q=1,R=0	67720	
1	3	0	20	17	1	11	065				CLA	HJQB1		67730	
1	3	0	21	13	1	11	1	376			STO	776		67740	
1	3	0	22	13	1	11	1	071	511054030		HJQB1	JOB1		67750	
1	3	0	23	17	1	11	1	030				V2		67760	
1	3	0	24	13	1	11	1	004				CLA	HJAJ5		67770
1	3	0	25	17	1	11	006				STO	404		67780	
1	3	0	26	5	1	11	052		000012524		CLA	052		67790	
1	3	0	27	5	1	11	121				CLA	121	LOAD OPT REG Q=1,R=0	67800	
1	3	0	28	17	1	11	014				CLA	146	CHECK OPT REG LOAD	67810	
1	3	0	31	5	1	11	146		000340000		CIO	146	LOAD Z CHAN CTR	67820	
1	3	0	32	17	1	11	015		002540064		CLA	-0002540064		67830	
1	3	0	33	5	1	11	142				CLA	142		67840	
1	3	0	34	5	1	11	136				CIO	136	LOAD Y CHAN CTR	67850	
1	3	0	35	17	1	11	020				CLA	ZERO	LOAD X CHAN CTR	67860	
1	3	0	36	5	1	11	126				CIO	126		67870	
1	3	0	37	7	1	11	020				ADD	ZERO	RESET SUBTRACT INHIBIT	67880	
1	3	0	40	7	1	11	020				ADD	ZERO		67890	
1	3	0	41	7	1	11	020				ADD	ZERO		67900	
1	3	0	42	17	1	11	066				CLA	HJP82		67910	
1	3	0	43	13	1	11	004		511024030		HJP82	HPC		67920	
1	3	0	44	17	1	11	006				CLA	404		67930	
1	3	0	45	5	1	11	121		000012524		CLA	-0000012524	COMPARE	67940	
1	3	0	46	5	1	11	121				CIO	121	NO COMPARE - INT 5	67950	
1	3	0	47	00	1	11	017				CIO	121		67960	
1	3	0	50	13	1	11	1	377	511054620		TRA*	JLJ5		67970	
1	3	0	51	13	1	11	1	076			STO	777		67980	
1	3	0	52	17	1	11	032				CLA	TEMP		67990	
1	3	0	53	5	1	11	126				CLA	K1		68000	
1	3	0	54	5	1	11	030				CIO	030	INT Z CHAN SUBTRACT	68010	
1	3	0	55	5	1	11	110				CIO	110	RESET INT 5	68020	
1	3	0	56	17	1	11	1	377			CLA	777	RESET MAIN INT LATCH	68030	
1	3	0	57	13	1	11	1	073			STO	V4		68040	
1	3	0	60	15	1	11	067				XOR	HJPK1	CORRECT ENTRY LOCATION	68050	
1	3	0	61	4	1	11	356		511023430		HJPK1	HPC		68060	
1	3	0	62	17	1	11	1	076			TNZ	JPJ5		68070	
1	3	0	63	15	1	11	005				CLA	TEMP		68080	
1	3	0	64	4	1	11	355		000012500		XOR	-0000012500	Z CHAN STEP FROM 10 TO 00	68090	
											TNZ	JPJ4		68100	
															68110
															68120
															68130

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 134)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	0	65	17	1	11	1	070			HJPB3	CLA	HJPB3		68140	
1	3	0	66	13	1	11	1	004	511035430		HJPB3	HPC	JPB3		68150	
1	3	0	67	17	1	11	1	005	000012500			STU	404		68160	
1	3	0	70	5	1	11	1	121				CLA	=0000012500		68170	
1	3	0	71	5	1	11	1	121				CIO	121		68180	
1	3	0	72	00	1	11	1	121				TRA*	JLJ5		68190	
1	3	0	73	13	1	11	1	377	511054620		JPJ2	STU	777		68200	
1	3	0	74	13	1	11	1	076			JPB3	STU	TEMP		68210	
1	3	0	75	5	1	11	1	030				CIO	030		68220	
1	3	0	76	5	1	11	1	110				CIO	110		68230	
1	3	0	77	17	1	11	1	377				CLA	777		68240	
1	3	0	100	13	1	11	1	073				STU	V4		68250	
1	3	0	101	15	1	11	1	071				XOR	HJPJ2		68260	
1	3	0	102	4	1	11	1	356	511035030		HJPJ2	HPC	JPJ2		68270	
1	3	0	103	17	1	11	1	076				TNZ	JPJ5		68280	
1	3	0	104	15	1	11	1	020	000000500			CLA	TEMP		68290	
1	3	0	105	4	1	11	1	355				XOR	=000000500		68300	
1	3	0	106	17	1	11	1	072				TNZ	JPJ4		68310	
1	3	0	107	13	1	11	1	004	511046030		HJPB4	CLA	HJPB4		68320	
1	3	0	110	17	1	11	1	020	000000500			HPC	JPB4		68330	
1	3	0	111	5	1	11	1	121				CLA	404		68340	
1	3	0	112	5	1	11	1	121				CIO	121		68350	
1	3	0	113	00	1	11	1	017				CIO	121		68360	
1	3	0	114	13	1	11	1	377	511054620		JPJ3	TRA*	JLJ5		68370	
1	3	0	115	13	1	11	1	076			JPB4	STU	777		68380	
1	3	0	116	5	1	11	1	030				STU	TEMP		68390	
1	3	0	117	5	1	11	1	110				CIO	030		68400	
1	3	0	120	17	1	11	1	377				CIO	110		68410	
1	3	0	121	13	1	11	1	073				CLA	777		68420	
1	3	0	122	15	1	11	1	073				STU	V4		68430	
1	3	0	123	4	1	11	1	356	511045430		HJPJ3	XOR	HJPJ3		68440	
1	3	0	124	17	1	11	1	076				HPC	JPJ3		68460	
1	3	0	125	4	1	11	1	355				TNZ	JPJ5		68470	
1	3	0	126	17	1	11	1	033				CLA	TEMP		68480	
1	3	0	127	5	1	11	1	126				TNZ	JPJ4		68490	
1	3	0	130	13	1	11	1	376				CLA	K77		68500	
1	3	0	131	17	1	11	1	074				CIO	K77		68510	
1	3	0	132	13	1	11	1	071				CIO	L26		68520	
1	3	0	133	17	1	11	1	030				STU	V4		68530	
1	3	0	134	13	1	11	1	004				CHECK	PLUS STEP FROM Q+R=1		68540	
1	3	0	135	17	1	11	1	000				STU	776		68550	
1	3	0	136	5	1	11	1	132			JQ81	CLA	HJRH1		68560	
1	3	0	137	17	1	11	1	013				HPC	JR81		68570	
1	3	0	140	5	1	11	1	052	511121030		HJR81	STU	V2		68580	
1	3	0	141	5	1	11	1	121				STU	HJAJ5		68590	
1	3	0	142	17	1	11	1	001				CLA	404		68600	
1	3	0	143	5	1	11	1	136	777777776			CLA	=077777776		68610	
1	3	0	144	5	1	11	1	146				CIO	132		68620	
1	3	0	145	17	1	11	1	002	000017776			CLA	=0000017776		68630	
1	3	0	146	5	1	11	1	142				CIO	052		68640	
1	3	0	147	5	1	11	1	126	001500016			CLA	=001500016		68650	
1	3	0	148	5	1	11	1	146				CIO	136		68660	
1	3	0	149	17	1	11	1	002	002540000			CLA	=002540000		68670	
1	3	0	150	5	1	11	1	142				CIO	142		68680	
1	3	0	151	5	1	11	1	126				CIO	126		68690	
1	3	0	152	5	1	11	1	126				CIO	126		68700	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 135)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	3	0	150	7	1	11	1	020				ADD	ZER0		68710	
1	3	0	151	7	1	11	1	020				ADD	ZER0		68720	
1	3	0	152	7	1	11	1	020				ADD	ZER0		68730	
1	3	0	153	17	1	11	1	075			HJQ82	CLA	HJQ82		68740	
1	3	0	154	13	1	11	1	004	511070430			HPC	JQ82		68750	
1	3	0	155	17	1	11	1	013	000017776			STO	404		68760	
1	3	0	156	5	1	11	1	121				CLA	121		68770	
1	3	0	157	5	1	11	1	121				CIO	121		68780	
1	3	0	160	00	1	11	1	017	511054620		JQK1	TRA*	JLJ5		68800	
1	3	0	161	13	1	11	1	377			JQ82	STO	777		68810	
1	3	0	162	13	1	11	1	076				STO	TEMP		68820	
1	3	0	163	17	1	11	1	021				CLA	88		68830	
1	3	0	164	5	1	11	1	126				CIO	126		68840	
1	3	0	165	5	1	11	1	030				CIO	030		68850	
1	3	0	166	5	1	11	1	110				CIO	110		68860	
1	3	0	167	17	1	11	1	377				CLA	777		68870	
1	3	0	170	13	1	11	1	073				STO	V4		68880	
1	3	0	171	15	1	11	1	076	511070030		HJQK1	XOR	HJQK1		68890	
1	3	0	172	4	1	11	1	356				HPC	JQK1		68900	
1	3	0	173	17	1	11	1	076				TNZ	JPJ5		68910	
1	3	0	174	15	1	11	1	021				CLA	TEMP		68920	
1	3	0	175	4	1	11	1	355	000005776			XOR	-0000005776		68930	
1	3	0	176	17	1	11	1	077				TNZ	JPJ4		68940	
1	3	0	177	13	1	11	1	004	5110202030		HJQ83	CLA	HJQ83		68950	
1	3	0	200	17	1	11	1	021				HPC	JQ83		68960	
1	3	0	201	5	1	11	1	121	000005776			STO	404		68970	
1	3	0	202	5	1	11	1	121				CLA	-0000005776		68980	
1	3	0	203	00	1	11	1	121				CIO	121		68990	
1	3	0	204	13	1	11	1	377	511054620		JQJ2	TRA*	JLJ5		69000	
1	3	0	205	13	1	11	1	076			JQ83	STO	777		69010	
1	3	0	206	5	1	11	1	030				STO	TEMP		69020	
1	3	0	207	5	1	11	1	110				CIO	030		69030	
1	3	0	210	17	1	11	1	377				CIO	110		69040	
1	3	0	211	13	1	11	1	073				CLA	777		69050	
1	3	0	212	15	1	11	1	100	51101430		HJQJ2	STO	V4		69060	
1	3	0	213	4	1	11	1	356				XOR	HJQJ2		69070	
1	3	0	214	17	1	11	1	076				HPC	JQJ2		69080	
1	3	0	215	15	1	11	1	022	000005752			TNZ	JPJ5		69090	
1	3	0	216	4	1	11	1	355				CLA	TEMP		69100	
1	3	0	217	17	1	11	1	101				XOR	-0000005752		69110	
1	3	0	220	13	1	11	1	004	511012430		HJQ84	HPC	JQ84		69120	
1	3	0	221	17	1	11	1	022				CLA	404		69130	
1	3	0	222	5	1	11	1	121	000005752			CLA	-0000005752		69140	
1	3	0	223	5	1	11	1	121				TNZ	JPJ4		69150	
1	3	0	224	00	1	11	1	017	511054620		JQJ3	TRA*	JLJ5		69160	
1	3	0	225	13	1	11	1	377			JQ84	STO	777		69170	
1	3	0	226	13	1	11	1	076				STO	TEMP		69180	
1	3	0	227	5	1	11	1	030				CIO	121		69190	
1	3	0	230	5	1	11	1	110				CIO	030		69200	
1	3	0	231	17	1	11	1	377				CIO	110		69210	
1	3	0	232	13	1	11	1	073				CLA	777		69220	
1	3	0	233	15	1	11	1	102				STO	V4		69230	
1	3	0	233	15	1	11	1	102				XOR	HJQJ3		69240	
															69250	
															69260	
															69270	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 136)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	0	234	4	1	11	102		511112030		HJQJ3	HPC	JUJ3		69280	
1	3	0	235	17	1	11	103					TNZ	JPJ5		69290	
1	3	0	236	15	1	11	076		000005252		CLA	XOR	TEMP		69300	
1	3	0	237	4	1	11	355					TNZ	JPJ4	Y CHAN STEP FROM 11 TO 01	69310	
1	3	0	240	17	1	11	033					CLA	K77		69320	
1	3	0	241	5	1	11	126					CIG	L26	SET SUBTRACT INHIBIT	69330	
1	3	0	242	13	1	11	376				*	CHECK MINUS STEP FROM Q=0,R=1		69340		
1	3	0	243	17	1	11	103				JR81	STU	776		69350	
1	3	0	244	13	1	11	071		511010230		HJSB1	CLA	HJSB1		69360	
1	3	0	245	17	1	11	030				HJSB1	HPC	JSB1		69370	
1	3	0	246	13	1	11	004					V2			69380	
1	3	0	247	17	1	11	020					CLA	HJAJ5		69390	
1	3	0	250	5	1	11	132					STO	404		69400	
1	3	0	251	17	1	11	023		000005252			CLA	ZERO		69410	
1	3	0	252	5	1	11	052					CIO	L32	SET ACCEL SIGNS MINUS	69420	
1	3	0	253	5	1	11	121					CIO	052	LOAD OPT REG Q=0,R=1	69430	
1	3	0	254	17	1	11	024		000340126			CIO	121	CHECK OPT REG LOAD	69440	
1	3	0	255	5	1	11	142					CLA	-0000340126		69450	
1	3	0	256	5	1	11	136					CIO	L42	LOAD Y CHAN CTR	69460	
1	3	0	257	17	1	11	025		001500000			CLA	L36	LOAD X CHAN CTR	69470	
1	3	0	260	5	1	11	146					CIO	166	LOAD Z CHAN CTR	69480	
1	3	0	261	5	1	11	126					CIO	L26	RESET SUBTRACT INHIBIT	69490	
1	3	0	262	7	1	11	020				ADD	ZERO			69500	
1	3	0	263	7	1	11	020				ADD	ZERO			69510	
1	3	0	264	7	1	11	020				ADD	ZERO			69520	
1	3	0	265	17	1	11	104					CLA	HJR82		69530	
1	3	0	266	13	1	11	104		511135430		HJR82	HPC	JR62		69540	
1	3	0	267	17	1	11	023					STO	404		69550	
1	3	0	270	5	1	11	121		000005252			CLA	-0000000000		69560	
1	3	0	271	5	1	11	121					CIO	L21	COMPARE	69570	
1	3	0	272	00	1	11	017		511054620		JR81	TRA*	JLJ5	NO COMPARE - INT 5	69580	
1	3	0	273	13	1	11	377				JR82	STU	777		69590	
1	3	0	274	13	1	11	076					STO	TEMP		69600	
1	3	0	275	17	1	11	010		000000004			CLA	-0000000004		69610	
1	3	0	276	5	1	11	126					CIO	L26	INH Y CHAN SUBTRACT	69620	
1	3	0	277	5	1	11	030					CIO	030	RESET INT 5	69630	
1	3	0	300	5	1	11	110					CIO	L10	RESET MAIN INT LATCH	69640	
1	3	0	301	17	1	11	377					CLA	777		69650	
1	3	0	302	13	1	11	073					STO	V4		69660	
1	3	0	303	15	1	11	105		511135030		HJRK1	XOR	HJRK1	CORRECT ENTRY LOCATION	69670	
1	3	0	304	4	1	11	356					HPC	JRK1		69700	
1	3	0	305	17	1	11	076					TNZ	JPJ5		69710	
1	3	0	306	15	1	11	022		000005752			CLA	TEMP		69720	
1	3	0	307	4	1	11	355					XOR			69730	
1	3	0	310	17	1	11	106					TNZ	JPJ4	Y CHAN STEP FROM 01 TO 11	69740	
1	3	0	311	13	1	11	004		511147030		HJR83	HPC	HJR83		69750	
1	3	0	312	17	1	11	022					CLA	404		69760	
1	3	0	313	5	1	11	121		000005752			CLA	-00000005752		69770	
1	3	0	314	5	1	11	121					CIO	L21		69780	
1	3	0	315	00	1	11	017		511054620		JR2	TRA*	JLJ5	COMPARE	69790	
1	3	0	316	13	1	11	377				**83	STO	777	NO COMPARE - INT 5	69800	
															69810	
															69820	
															69830	
															69840	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 137)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	0	317	13	1	11	1	076				STO	TEMP		69850	
1	3	0	320	5	1	11	1	030				CIO	030	RESET INT 5	69860	
1	3	0	321	5	1	11	1	110				CIO	110	RESET MAIN INT LATCH	69870	
1	3	0	322	17	1	11	1	377				CLA	777		69880	
1	3	0	323	13	1	11	1	073				STO	V4		69890	
1	3	0	324	15	1	11	1	107				XOR	HJRJ2	CORRECT ENTRY LOCATION	69900	
1	3	0	325	4	1	11	1	356	511146430		HJRJ2	HPC	JRJ2		69910	
1	3	0	326	17	1	11	1	076				CLA	TEMP		69920	
1	3	0	327	15	1	11	1	021	000005776		XOR	TRA*	JPJ5	Z CHAN STEP FROM 01 TO 11	69930	
1	3	0	330	4	1	11	1	355			TNZ	TRJ4	-0000005776		69940	
1	3	0	331	17	1	11	1	110	511157430		HJRJ4	HPC	JRJ4		69950	
1	3	0	332	13	1	11	1	004				STO	04		69960	
1	3	0	333	17	1	11	1	021	000005776		CLA	04	-0000005776		69970	
1	3	0	334	5	1	11	1	121				CIO	121	COMPARE	69980	
1	3	0	335	5	1	11	1	121				CIO	121	NO COMPARE - INT 5	70000	
1	3	0	336	00	1	11	1	121	511054620		TRA*	JLJ5		70010		
1	3	0	337	13	1	11	1	377			JRJ3	STO	JLJ5		70020	
1	3	0	340	13	1	11	1	076			JRJ4	STO	TEMP		70030	
1	3	0	341	5	1	11	1	030				CIO	030	RESET INT 5	70040	
1	3	0	342	5	1	11	1	110				CIO	110	RESET MAIN INT LATCH	70050	
1	3	0	343	17	1	11	1	377				CLA	110		70060	
1	3	0	344	13	1	11	1	073				CLA	777		70070	
1	3	0	345	15	1	11	1	111				STO	V4		70080	
1	3	0	346	4	1	11	1	356	511157030		HJRJ3	XOR	HJRJ3	CORRECT ENTRY LOCATION	70090	
1	3	0	347	17	1	11	1	076				HPC	JRJ3		70100	
1	3	0	350	15	1	11	1	013	000017776		CLA	TEMP			70110	
1	3	0	351	4	1	11	1	355				XOR	JPJ5	X CHAN STEP FROM 01 TO 11	70120	
1	3	0	352	17	1	11	1	033				TNZ	JPJ4		70130	
1	3	0	353	5	1	11	1	126				CLA	K77		70140	
1	3	0	354	10	1	11	1	020				CIO	126	SET SUBTRACT INHIBIT	70150	
1	3	0	355	13	1	11	1	076				TRA	JSB1		70160	
1	3	0	356	0	1	11	1	031				STO	TEMP		70170	
1	3	1	20	1	1	11	1	112				HOP	HJAJ58		70180	
												ORC	1,3,1,20,1,11,		70190	
												CHECK	PLUS STEP FROM Q=0,R=1		70200	
1	3	1	20	17	1	11	1	112				CLA	HJTBI		70210	
1	3	1	21	13	1	11	1	376				STO	776		70220	
1	3	1	22	13	1	11	1	112				HPC	JTBI		70230	
1	3	1	23	17	1	11	1	030	511054630		STO	V2			70240	
1	3	1	24	13	1	11	1	004				CLA	HJAJ5		70250	
1	3	1	25	17	1	11	1	000				CLA	404		70260	
1	3	1	26	5	1	11	1	132	777777776		CLA	-077777776		70270		
1	3	1	27	17	1	11	1	023				CIO	132		70280	
1	3	1	30	5	1	11	1	052	000005252		CLA	-0000005252	SET ACCEL SIGNS PLUS	70290		
1	3	1	31	5	1	11	1	121				CIO	052	LOAD OPT REG Q=0,R=1	70300	
1	3	1	32	17	1	11	1	026				CLA	-0002540016	CHECK OPT REG LOAD	70310	
1	3	1	33	5	1	11	1	146	002540016		CIO	146	LOAD Z CHAN CTR	70320		
1	3	1	34	5	1	11	1	136				CIO	136	LOAD X CHAN CTR	70330	
1	3	1	35	17	1	11	1	025	001500000		CLA	-0001500000	LOAD Y CHAN CTR	70340		
1	3	1	36	5	1	11	1	142				CIO	142	RESET SUBTRACT INHIBIT	70350	
1	3	1	37	5	1	11	1	126				CIO	126		70360	
1	3	1	40	7	1	11	1	020				ADD	ZERO		70370	
1	3	1	41	7	1	11	1	020				ADD	ZERO		70380	
1	3	1	42	7	1	11	1	020				ADD	ZERO		70390	
1	3	1	42	7	1	11	1	020				ADD	ZERO		70400	
1	3	1	42	7	1	11	1	020				ADD	ZERO		70410	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 138)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	1	43	17	1	11	113				HJSB2	CLA	HJSB2		70420	
1	3	1	44	13	1	11	113	511024630			HJSB2	HPC	J5B2		70430	
1	3	1	45	17	1	11	004					CLA	404		70440	
1	3	1	46	5	1	11	121	000005252				CLA	=0000005252		70450	
1	3	1	47	5	1	11	121					CIO	121		70460	
1	3	1	50	00	1	11	017	511054620			J5K1	TRA*	JLJ5		70470	
1	3	1	51	13	1	11	1076				J5B2	STO	777		70480	
1	3	1	52	13	1	11	1076					STO	TEMP		70490	
1	3	1	53	17	1	11	021					CLA	68		70500	
1	3	1	54	5	1	11	126					CIO	126		70510	
1	3	1	55	5	1	11	030					CIO	030		70520	
1	3	1	56	5	1	11	110					CIO	110		70530	
1	3	1	57	17	1	11	1076					CLA	110		70540	
1	3	1	58	17	1	11	1076					CLA	777		70550	
1	3	1	60	13	1	11	073					STO	V4		70560	
1	3	1	61	15	1	11	114					XOR	HJSK1		70570	
1	3	1	62	4	1	11	114	511024230			HJSK1	HPC	J5K1		70580	
1	3	1	63	17	1	11	356					TNZ	JPJ5		70590	
1	3	1	64	15	1	11	027					CLA	TEMP		70600	
1	3	1	65	4	1	11	355	000000252				XOR	=0000000252		70610	
1	3	1	66	4	1	11	355					TNZ	JPJ4		70620	
1	3	1	67	13	1	11	115	511036230			HJSB3	CLA	HJSB3		70630	
1	3	1	68	13	1	11	1004					HPC	J5B3		70640	
1	3	1	70	17	1	11	027					CLA	404		70650	
1	3	1	71	5	1	11	121	000000252				CLA	=0000000252		70660	
1	3	1	72	5	1	11	121					CIO	121		70670	
1	3	1	73	00	1	11	017	511054620			J5J2	TRA*	JLJ5		70680	
1	3	1	74	13	1	11	1076				J5B3	STO	777		70690	
1	3	1	75	13	1	11	1076					STO	TEMP		70700	
1	3	1	76	5	1	11	030					CIO	030		70710	
1	3	1	77	5	1	11	110					CIO	110		70720	
1	3	1	100	17	1	11	1073					CLA	777		70730	
1	3	1	101	13	1	11	1073					STO	V4		70740	
1	3	1	102	15	1	11	116					CLA	V4		70750	
1	3	1	103	4	1	11	356	511035630			HJSJ2	XOR	HJSJ2		70760	
1	3	1	104	17	1	11	076					HPC	J5J2		70770	
1	3	1	105	15	1	11	030					TNZ	JPJ5		70780	
1	3	1	106	4	1	11	355	000000012				CLA	TEMP		70790	
1	3	1	107	17	1	11	117					CLA	=0000000012		70800	
1	3	1	108	17	1	11	117					CLA	JPJ4		70810	
1	3	1	109	17	1	11	117					CLA	HJSB4		70820	
1	3	1	110	13	1	11	1004	511046630			HJSB4	MPC	J5B4		70830	
1	3	1	111	13	1	11	004					STU	J5B4		70840	
1	3	1	112	17	1	11	030	000000012				CLA	404		70850	
1	3	1	113	5	1	11	121					CLA	=0000000012		70860	
1	3	1	114	00	1	11	017	511054620			J5J3	CIO	121		70870	
1	3	1	115	13	1	11	1076				J5B4	TRA*	JLJ5		70880	
1	3	1	116	13	1	11	1076					STO	777		70890	
1	3	1	117	5	1	11	030					STU	TEMP		70900	
1	3	1	120	5	1	11	110					CIO	030		70910	
1	3	1	121	17	1	11	1073					CIO	110		70920	
1	3	1	122	13	1	11	1073					CLA	777		70930	
1	3	1	123	15	1	11	120					STO	V4		70940	
1	3	1	124	4	1	11	356	511046230			HJSJ3	XOR	HJSJ3		70950	
1	3	1	125	17	1	11	1076					HPC	J5J3		70960	
1	3	1	125	17	1	11	1076					TNZ	JPJ5		70970	
1	3	1	125	17	1	11	1076					CLA	TEMP		70980	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 139)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	1	126	4	1	11	1	355				TNZ	JPJ4	Z CHAN STEP FROM 01 TO 00	70990	
1	3	1	127	17	1	11	1	033				CLA	K77		71000	
1	3	1	130	5	1	11	1	126				C10	L26	SET SUBTRACT INHIBIT	71010	
											JT81	STO	776	CHECK MINUS STEP FROM Q+R=0	71020	
1	3	1	131	13	1	11	1	376				STO	HJUB1		71030	
1	3	1	132	17	1	11	1	127				CLA	V2		71040	
1	3	1	133	13	1	11	1	071				STO	HJAJ5		71050	
1	3	1	134	17	1	11	1	030				CLA	404		71060	
1	3	1	135	13	1	11	1	004				STO	ZERO		71070	
1	3	1	136	17	1	11	1	020				CLA	ZERO	SET ACCEL SIGNS MINUS	71080	
1	3	1	137	5	1	11	1	132				C10	L32	LOAD OPT REG Q+R=0	71090	
1	3	1	140	17	1	11	1	020				CLA	ZERO	CHECK OPT REG LOAD	71100	
1	3	1	141	5	1	11	1	052				C10	052		71110	
1	3	1	142	5	1	11	1	121				C10	L21		71120	
1	3	1	143	17	1	11	1	031	001500126			CLA	=0001500126		71130	
1	3	1	144	5	1	11	1	142				C10	L42	LOAD Y CHAN CTR	71140	
1	3	1	145	5	1	11	1	136				C10	L36	LOAD X CHAN CTR	71150	
1	3	1	146	17	1	11	1	014	000340000			CLA	=000340000		71160	
1	3	1	147	5	1	11	1	146				C10	L46	LOAD Z CHAN CTR	71170	
1	3	1	150	5	1	11	1	126				C10	L26	RESET SUBTRACT INHIBIT	71180	
1	3	1	151	7	1	11	1	020				ADD	ZERO		71190	
1	3	1	152	7	1	11	1	020				ADD	ZERO		71200	
1	3	1	153	7	1	11	1	020				ADD	ZERO		71210	
1	3	1	154	17	1	11	1	121				CLA	HJT82		71220	
									511071230		HJT82	HPC	JT82		71230	
1	3	1	155	13	1	11	1	004				STO	404		71240	
1	3	1	156	17	1	11	1	020				CLA	ZERO		71250	
1	3	1	157	5	1	11	1	121				C10	L21	COMPARE	71260	
1	3	1	160	5	1	11	1	121				C10	L21	NO COMPARE - INT 5	71270	
1	3	1	161	00	1	11	1	017				TRA*	JLJ5		71280	
1	3	1	162	13	1	11	1	377				STO	777		71290	
1	3	1	163	13	1	11	1	076				STO	TEMP		71300	
1	3	1	164	17	1	11	1	032				CLA	K1		71310	
1	3	1	165	5	1	11	1	126				C10	L26	INH Z CHAN SUBTRACT	71320	
1	3	1	166	5	1	11	1	030				C10	030	RESET INT 5	71330	
1	3	1	167	5	1	11	1	110				C10	L10	RESET MAIN INT LATCH	71340	
1	3	1	170	17	1	11	1	377				CLA	777		71350	
1	3	1	171	13	1	11	1	073				STO	V4		71360	
1	3	1	172	15	1	11	1	122				XOR	HJTK1	CORRECT ENTRY LOCATION	71370	
									511070630		HJTK1	HPC	JTK1		71380	
1	3	1	173	4	1	11	1	356				TNZ	JPJ5		71390	
1	3	1	174	17	1	11	1	076				CLA	TEMP		71400	
1	3	1	175	15	1	11	1	030	000000012			XOR	=0000000012	Z CHAN STEP FROM 00 TO 01	71410	
1	3	1	176	4	1	11	1	355				TNZ	JPJ4		71420	
1	3	1	177	17	1	11	1	123				CLA	HJT83		71430	
									511102630		HJT83	HPC	JT83		71440	
1	3	1	200	13	1	11	1	004				STO	404		71450	
1	3	1	201	17	1	11	1	030				CLA	=0000000012		71460	
1	3	1	202	5	1	11	1	121				C10	L21	COMPARE	71470	
1	3	1	203	5	1	11	1	121				C10	L21	NO COMPARE - INT 5	71480	
1	3	1	204	00	1	11	1	017				TRA*	JLJ5		71490	
1	3	1	205	13	1	11	1	377				STO	777		71500	
1	3	1	206	13	1	11	1	076				STO	TEMP		71510	
1	3	1	207	5	1	11	1	030				C10	030	RESET INT 5	71520	
1	3	1	210	5	1	11	1	110				C10	L10	RESET MAIN INT LATCH	71530	
1	3	1	211	17	1	11	1	377				CLA	777		71540	
1	3	1	212	13	1	11	1	073				STO	V4		71550	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 140)

IM	IS	S	LUC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	3	1	213	15	1	11	124				HJTJ2	XOR	HJTJ2	CORRECT ENTRY LOCATION	71560	
1	3	1	214	4	1	11	124	511102230			HJTJ2	HPC	JTJ2		71570	
1	3	1	215	17	1	11	356					TNZ	JPJ5		71580	
1	3	1	216	15	1	11	076					CLA	TEMP		71590	
1	3	1	217	4	1	11	027	000C00252				XOR	=000000252	Y CHAN STEP FROM 00 TO 01	71600	
1	3	1	218	4	1	11	355					TNZ	JPJ4		71610	
1	3	1	220	17	1	11	125					CLA	HJT84		71620	
1	3	1	221	13	1	11	125	511113230			HJT84	HPC	JTH4		71630	
1	3	1	222	17	1	11	027					STU	404		71640	
1	3	1	223	5	1	11	121	000000252				CLA	=000000252		71650	
1	3	1	224	5	1	11	121					CIC	L21		71660	
1	3	1	225	00	1	11	121					CIC	L21		71670	
1	3	1	226	13	1	11	377	511054620			JTJ3	TRA*	JLJ5		71680	
1	3	1	227	13	1	11	076				JTR4	STG	777		71690	
1	3	1	230	5	1	11	030					STU	TEMP		71700	
1	3	1	231	5	1	11	110					CIC	03C	RESEI INT 5	71710	
1	3	1	232	17	1	11	377					CIC	L10	RESEI MAIN INT LATCH	71720	
1	3	1	233	13	1	11	073					CLA	777		71730	
1	3	1	234	15	1	11	126					STU	V4		71740	
1	3	1	235	4	1	11	126	511112630			HJTJ3	XOR	HJTJ3	CORRECT ENTRY LOCATION	71750	
1	3	1	236	17	1	11	076					HPC	JTJ3		71760	
1	3	1	237	15	1	11	023					TNZ	JPJ5		71770	
1	3	1	240	4	1	11	355	000005252				CLA	TEMP		71780	
1	3	1	241	17	1	11	033					XOR	=000005252	X CHAN STEP FROM 00 TO 01	71790	
1	3	1	242	5	1	11	126					TNZ	JPJ4		71800	
1	3	1	243	00	1	11	032					CLA	K77		71810	
1	4	0	20	17	1	11	127	511010040				CIC	L26	SET SUBTRACT INHIBIT	71820	
1	4	0	20	17	1	11	127					TRA*	JUG1		71830	
1	4	0	21	13	1	11	376					ORG	1,4,0,20,1,11,		71840	
1	4	0	22	13	1	11	127					CLA	HJUB1		71850	
1	4	0	23	17	1	11	070					STU	776		71860	
1	4	0	24	13	1	11	130	511010040			HJUB1	HPC	JUB1		71870	
1	4	0	25	17	1	11	071					STU	776		71880	
1	4	0	26	13	1	11	004					HPC	JUB1		71890	
1	4	0	27	17	1	11	033					CLA	HJVH1A		71900	
1	4	0	30	5	1	11	136					HPC	JVH1		71910	
1	4	0	31	17	1	11	034					STU	V2		71920	
1	4	0	32	5	1	11	126					CLA	HJAJ5		71930	
1	4	0	33	17	1	11	020					CLA	404		71940	
1	4	0	34	5	1	11	052					STU	404		71950	
1	4	0	35	5	1	11	121					CLA	=000000044	LOAD X CHAN CTR	71960	
1	4	0	36	17	1	11	035	000000044				CLA	=000000044		71970	
1	4	0	37	5	1	11	142					CIC	L36		71980	
1	4	0	38	5	1	11	126	000000006				CLA	=000000006	RESEI X CHAN SUBTRACT INHIBIT	71990	
1	4	0	39	17	1	11	020					CLA	ZERU		72000	
1	4	0	40	5	1	11	126					CIC	052	LOAD OPT REG Q+R=0	72010	
1	4	0	41	7	1	11	020					CIC	L21	CHECK OPT REG LOAD	72020	
1	4	0	42	17	1	11	020					CLA	ZERU		72030	
1	4	0	43	5	1	11	066					CIC	066	LOAD Y CHAN CTR	72040	
1	4	0	44	17	1	11	036	001100002				CLA	=000110002	RESEI Y CHAN SUBTRACT INHIBIT	72050	
1	4	0	45	5	1	11	146					CIC	L46		72060	
1	4	0	46	5	1	11	126					CIC	L26	RESEI COMPARE	72070	
1	4	0	47	17	1	11	030					CLA	=000110000	LOAD Z CHAN CTR	72080	
1	4	0	48	5	1	11	146	000000012				CIC	L46	RESEI Z CHAN SUBTRACT INHIBIT	72090	
1	4	0	49	17	1	11	030					CLA	=000000012		72100	
1	4	0	50	5	1	11	132					CIC	L32	ACCEL SIGNS X=PLUS,Y=MINUS,Z=PLUS	72110	
1	4	0	50	5	1	11	132					CIC	L32		72120	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 141)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	4	0	51	7	1	11	1	020			JUG1	ADD	ZEKO		72130	
1	4	0	52	13	1	11	1	377			JUG1	STO	777		72140	
1	4	0	53	17	1	11	1	377			JUG1	CLA	777		72150	
1	4	0	54	13	1	11	1	073			JUG1	STU	V4		72160	
1	4	0	55	15	1	11	1	121			JUG1	CIC	121		72170	
1	4	0	56	15	1	11	1	004	000012000		JUG1	XOR	=0000012000	X STEP FROM 00 TO 10	72180	
1	4	0	57	4	1	11	1	164			JUG1	TNZ	JUJ2		72190	
1	4	0	60	13	1	11	1	377			JUG1	STC	777		72200	
1	4	0	61	17	1	11	1	377			JUG1	CLA	777		72210	
1	4	0	62	13	1	11	1	073			JUG1	V4			72220	
1	4	0	63	5	1	11	1	121			JUG1	CIU	121		72230	
1	4	0	64	15	1	11	1	135	000012240		JUG1	XOR	=0000012240	Y STEP FROM 00 TO 01	72240	
1	4	0	65	4	1	11	1	164			JUG1	TNZ	JUJ2		72250	
1	4	0	66	13	1	11	1	377			JUG1	STO	777		72260	
1	4	0	67	17	1	11	1	377			JUG1	CLA	777		72270	
1	4	0	70	13	1	11	1	073			JUG1	STU	V4		72280	
1	4	0	71	5	1	11	1	121			JUG1	CIU	121		72290	
1	4	0	72	15	1	11	1	201	000012264		JUG1	XOR	=0000012264	Z STEP FROM 00 TO 10	72300	
1	4	0	73	4	1	11	1	164			JUG1	TNZ	JUJ2		72310	
1	4	0	74	13	1	11	1	377			JUG1	STU	777		72320	
1	4	0	75	17	1	11	1	377			JUG1	CLA	777		72330	
1	4	0	76	13	1	11	1	073			JUG1	STU	V4		72340	
1	4	0	77	5	1	11	1	121			JUG1	CIU	121		72350	
1	4	0	100	15	1	11	1	202	000017264		JUG1	XOR	=0000017264	X STEP FROM 10 TO 11	72360	
1	4	0	101	4	1	11	1	164			JUG1	TNZ	JUJ2		72370	
1	4	0	102	13	1	11	1	377			JUG1	STO	777		72380	
1	4	0	103	17	1	11	1	377			JUG1	CLA	777		72390	
1	4	0	104	13	1	11	1	073			JUG1	STU	V4		72400	
1	4	0	105	5	1	11	1	121			JUG1	CIU	121		72410	
1	4	0	106	15	1	11	1	012	000017764		JUG1	XOR	=0000017764	Y STEP FROM 01 TO 11	72420	
1	4	0	107	4	1	11	1	164			JUG1	TNZ	JUJ2		72430	
1	4	0	110	13	1	11	1	377			JUG1	STO	777		72440	
1	4	0	111	17	1	11	1	377			JUG1	CLA	777		72450	
1	4	0	112	13	1	11	1	073			JUG1	STC	V4		72460	
1	4	0	113	5	1	11	1	121			JUG1	CIC	121		72470	
1	4	0	114	15	1	11	1	013	000017776		JUG1	XOR	=0000017776	Z STEP FROM 10 TO 11	72480	
1	4	0	115	4	1	11	1	164			JUG1	TNZ	JUJ2		72490	
1	4	0	116	13	1	11	1	377			JUG1	STU	777		72500	
1	4	0	117	17	1	11	1	377			JUG1	CLA	777		72510	
1	4	0	120	13	1	11	1	073			JUG1	STO	V4		72520	
1	4	0	121	5	1	11	1	121			JUG1	CIC	121		72530	
1	4	0	122	15	1	11	1	021	000005776		JUG1	XOR	=000005776	X STEP FROM 11 TO 01	72540	
1	4	0	123	4	1	11	1	164			JUG1	TNZ	JUJ2		72550	
1	4	0	124	13	1	11	1	377			JUG1	STU	777		72560	
1	4	0	125	17	1	11	1	377			JUG1	CLA	777		72570	
1	4	0	126	13	1	11	1	073			JUG1	STC	V4		72580	
1	4	0	127	5	1	11	1	121			JUG1	CIC	121		72590	
1	4	0	130	15	1	11	1	203	000005536		JUG1	XOR	=000005536	Y STEP FROM 11 TO 10	72600	
1	4	0	131	4	1	11	1	164			JUG1	TNZ	JUJ2		72610	
1	4	0	132	13	1	11	1	377			JUG1	STC	777		72620	
1	4	0	133	17	1	11	1	377			JUG1	CLA	777		72630	
1	4	0	134	13	1	11	1	073			JUG1	STU	V4		72640	
1	4	0	135	5	1	11	1	121			JUG1	CIC	121		72650	
1	4	0	136	15	1	11	1	204	000005512		JUG1	XOR	=000005512	Z STEP FROM 11 TO 01	72660	
1	4	0	137	4	1	11	1	164			JUG1	TNZ	JUJ2		72670	
1	4	0	140	13	1	11	1	377			JUG1	STU	777		72680	
1	4	0	141	17	1	11	1	377			JUG1	CLA	777		72690	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 142)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	4	0	142	13	1	11	1	073				STC	V4		72700	
1	4	0	143	5	1	11	121					CIU	121		72710	
1	4	0	144	15	1	11	205		000000512			XOK	=00C0000512	X STEP FROM 01 TO 00	72720	
1	4	0	145	4	1	11	164				JUG5	TNZ	JUJ2		72730	
1	4	0	146	13	1	11	377					STU	777		72740	
1	4	0	147	17	1	11	1377					CLA	777		72750	
1	4	0	150	13	1	11	073					STO	V4		72760	
1	4	0	151	5	1	11	121					CIU	121		72770	
1	4	0	152	15	1	11	030		000000012			XOR	=0000000012	Y STEP FROM 10 TO 00	72780	
1	4	0	153	4	1	11	164				JUJ5	TNZ	JUJ2		72790	
1	4	0	154	13	1	11	1377					STO	777		72800	
1	4	0	155	17	1	11	1377					CLA	777		72810	
1	4	0	156	13	1	11	073					STU	V4		72820	
1	4	0	157	5	1	11	121					CIU	121		72830	
1	4	0	160	4	1	11	164				JUJ2	TNZ	JUJ2	Z STEP FROM 01 TO 00	72840	
1	4	0	161	17	1	11	033					CLA	K77		72850	
1	4	0	162	5	1	11	126					CIU	126	SET SUBTRACT INHIBIT	72860	
1	4	0	163	10	1	11	020				JUJ2	TRA	JV81		72870	
1	4	0	164	10	1	11	1243					TRA	JV81		72880	
1	4	1	20	1	1	11	131				ORG	ORG	1,4,1,20,1,11,		72890	
CHECK REGISTER RATE REGEN 2																
1	4	1	20	17	1	11	131				JV81	CLA	HJV81		72910	
1	4	1	21	13	1	11	131				HJV81	STU	776		72920	
1	4	1	22	13	1	11	131		511010240			HPC	JV81		72930	
1	4	1	23	17	1	11	070					STU	V1		72940	
1	4	1	24	13	1	11	132		511124240			CLA	HJV81		72950	
1	4	1	25	13	1	11	071					HPC	JV81		72960	
1	4	1	26	13	1	11	030					CLA	V2		72970	
1	4	1	27	17	1	11	004					CLA	HJAJ5		72980	
1	4	1	28	17	1	11	033					CLA	404		72990	
1	4	1	30	5	1	11	066		001100000			CIU	K77	SET COMPARE	73000	
1	4	1	31	17	1	11	036					CLA	066		73010	
1	4	1	32	5	1	11	146		000000014			CIU	146	LOAD Z CHAN CTR	73020	
1	4	1	33	17	1	11	206					CLA	=00C0000014		73040	
1	4	1	34	5	1	11	126		000017776			CIU	126	RESET Z CHAN SUBTRACT INHIBIT	73050	
1	4	1	35	17	1	11	013					CLA	=0000017776		73060	
1	4	1	36	5	1	11	052		001100010			CIU	052	LOAD OPT NEG Q-R=1	73070	
1	4	1	37	5	1	11	121					CIU	121	CHECK OPT REG. LOAD	73080	
1	4	1	40	17	1	11	207					CLA	=0001100010		73090	
1	4	1	41	5	1	11	142					CIU	142	LOAD Y CHAN CTR	73100	
1	4	1	42	5	1	11	126					CIU	126	RESET Y CHAN SUBTRACT INHIBIT	73110	
1	4	1	43	17	1	11	020					CLA	ZERU		73120	
1	4	1	44	5	1	11	066		000000044			CIU	066	RESET COMPARE	73130	
1	4	1	45	17	1	11	033					CLA	=0000000044		73140	
1	4	1	46	5	1	11	136					CIU	136	LOAD X CHAN CTR	73150	
1	4	1	47	17	1	11	020					CLA	ZERU		73160	
1	4	1	50	5	1	11	126		000000004			CIU	126	RESET X CHAN SUBTRACT INHIBIT	73170	
1	4	1	51	17	1	11	010					CLA	=00C0000004		73180	
1	4	1	52	5	1	11	132					CIU	132	ACCEL. SIGNS X=MINUS, Y=PLUS, Z=MINUS	73190	
1	4	1	53	7	1	11	020					ADD	ZERU		73200	
1	4	1	54	13	1	11	1377				JV81	STU	777		73210	
1	4	1	55	17	1	11	1377					CLA	777		73220	
1	4	1	56	13	1	11	073					STU	V4		73230	
1	4	1	57	5	1	11	121					CIU	121		73240	
1	4	1	60	15	1	11	012		000017764			XOR	=0000017764	Z STEP FROM 11 TO 10	73250	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 143)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	4	1	61	4	1	11	1	243			JVJ1	TNZ	JVJ2		73270	
1	4	1	62	13	1	11	1	377				CLA	777		73280	
1	4	1	63	17	1	11	1	377				CLA	777		73290	
1	4	1	64	13	1	11	1	073				STC	V4		73300	
1	4	1	65	5	1	11	1	121				C10	121		73310	
1	4	1	66	15	1	11	1	202	000017264			X04	=0000017264	Y STEP FROM 11 TO 01	73320	
1	4	1	67	4	1	11	1	243			JVA3	TNZ	JVJ2		73330	
1	4	1	71	17	1	11	1	377				CLA	777		73340	
1	4	1	72	13	1	11	1	073				STC	V4		73350	
1	4	1	73	5	1	11	1	121				C10	121		73360	
1	4	1	74	15	1	11	1	201	000012264			X04	=0000012264	X STEP FROM 11 TO 10	73370	
1	4	1	75	4	1	11	1	243			JVC3	TNZ	JVJ2		73380	
1	4	1	76	13	1	11	1	377				CLA	777		73390	
1	4	1	77	17	1	11	1	377				CLA	777		73400	
1	4	1	100	13	1	11	1	073				STC	V4		73420	
1	4	1	101	5	1	11	1	121				C10	121		73430	
1	4	1	102	15	1	11	1	135	000012240			X04	=0000012240	Z STEP FROM 10 TO 00	73440	
1	4	1	103	4	1	11	1	243			JVE3	TNZ	JVJ2		73450	
1	4	1	104	13	1	11	1	377				STC	777		73460	
1	4	1	105	17	1	11	1	377				CLA	777		73470	
1	4	1	106	13	1	11	1	073				STC	V4		73480	
1	4	1	107	5	1	11	1	121				C10	121		73490	
1	4	1	110	15	1	11	1	004	000012000			X04	=0000012000	Y STEP FROM 01 TO 00	73500	
1	4	1	111	4	1	11	1	243			JVG3	TNZ	JVJ2		73510	
1	4	1	112	13	1	11	1	377				STC	777		73520	
1	4	1	113	17	1	11	1	377				CLA	777		73530	
1	4	1	114	13	1	11	1	073				STC	V4		73540	
1	4	1	115	5	1	11	1	121				C10	121		73550	
1	4	1	116	7	1	11	1	020				ADD	ZER0		73560	
1	4	1	117	4	1	11	1	243			JVJ3	TNZ	JVJ2	X STEP FROM 10 TO 00	73570	
1	4	1	120	13	1	11	1	377				STC	777		73580	
1	4	1	121	17	1	11	1	377				CLA	777		73590	
1	4	1	122	13	1	11	1	073				STC	V4		73600	
1	4	1	123	5	1	11	1	121				C10	121		73610	
1	4	1	124	15	1	11	1	030	000000012			X04	=0000000012	Z STEP FROM 00 TO 01	73620	
1	4	1	125	4	1	11	1	243			JVA5	TNZ	JVJ2		73630	
1	4	1	126	13	1	11	1	377				STC	777		73640	
1	4	1	127	17	1	11	1	377				CLA	777		73650	
1	4	1	130	13	1	11	1	073				STC	V4		73660	
1	4	1	131	5	1	11	1	121				C10	121		73670	
1	4	1	132	15	1	11	1	205	000000512			X04	=00000000512	Y STEP FROM 00 TO 10	73680	
1	4	1	133	4	1	11	1	243			JVC5	TNZ	JVJ2		73690	
1	4	1	134	13	1	11	1	377				STC	777		73700	
1	4	1	135	17	1	11	1	377				CLA	777		73710	
1	4	1	136	13	1	11	1	073				STC	V4		73720	
1	4	1	137	5	1	11	1	121				C10	121		73730	
1	4	1	140	15	1	11	1	204	000005512			X04	=0000005512	X STEP FROM 00 TO 01	73740	
1	4	1	141	4	1	11	1	243			JVE5	TNZ	JVJ2		73750	
1	4	1	142	13	1	11	1	377				STC	777		73760	
1	4	1	143	17	1	11	1	377				CLA	777		73770	
1	4	1	144	13	1	11	1	073				STC	V4		73780	
1	4	1	145	5	1	11	1	121				C10	121		73790	
1	4	1	146	15	1	11	1	203	000005516			X04	=000005516	Z STEP FROM 01 TO 11	73800	
1	4	1	147	4	1	11	1	243			JVG5	TNZ	JVJ2		73810	
1	4	1	150	13	1	11	1	377				STC	777		73820	
1	4	1	151	17	1	11	1	377				CLA	777		73830	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 144)

IM	IS	S	LOC	UP	OM	DS	9	AOR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	4	1	152	13	1	11	1	073				STU	V4		73840	
1	4	1	153	5	1	11	121				CIC	L21			73850	
1	4	1	154	15	1	11	021		000005776		XOR	=00CC005776		Y STEP FROM I0 TO I1	73860	
1	4	1	155	4	1	11	1243			JVJ5	FNZ	JVJ2			73870	
1	4	1	156	13	1	11	1377				STC	777			73880	
1	4	1	157	17	1	11	1377				CLA	777			73890	
1	4	1	160	13	1	11	1073				STU	V4			73900	
1	4	1	161	15	1	11	013		000017776		XOR	=000017776		X STEP FROM O1 TO I1	73910	
1	4	1	163	4	1	11	1243				FNZ	JVJ2			73920	
1	4	1	164	17	1	11	1020				CLA	ZEHU			73930	
1	4	1	165	13	1	11	1073				STU	V4			73940	
1	4	1	166	5	1	11	066		311120		* *	CIC		CHECK LVDA POWER SUPPLY LINES AND A/D CONVERTERS	73970	
1	4	1	167	13	1	11	1376		320340		K35A	OC1	000311120	SET DA POWER SUPPLY SWITCH TO POSITION 1	73980	
1	4	1	170	5	1	11	233			JXCI	OC1	000320340		DISABLE COMPARE	73990	
1	4	1	171	5	1	11	025				CIC	066			74000	
1	4	1	172	13	1	11	1076				STU	776			74010	
1	4	1	173	2	1	11	1333				CIC	233		SEL LVDA +28A	74020	
1	4	1	174	14	1	11	1274				CIC	025		READ A/D CONVERTER	74030	
1	4	1	175	13	1	11	1376				STU	TEMP			74040	
1	4	1	176	17	1	11	134				SUB	K35A		LESS THAN 27.5	74050	
1	4	1	177	2	1	11	1076				STU	776			74060	
1	4	1	200	14	1	11	1274			JXFI	GLA	K35B		GREATER THAN 28.5	74070	
1	4	1	201	13	1	11	1376				SUB	TEMP			74080	
1	4	1	202	5	1	11	243				STC	776			74090	
1	4	1	203	5	1	11	025				CIC	243		LVDA + 28B	74100	
1	4	1	204	13	1	11	1076				CIC	025		READ A/D CONVERTER	74110	
1	4	1	205	2	1	11	1333				STU	TEMP			74120	
1	4	1	206	14	1	11	1274				SUB	K35A		LESS THAN 27.5	74130	
1	4	1	207	13	1	11	134				STU	776			74140	
1	4	1	210	17	1	11	134				GLA	K35B		GREATER THAN 28.5	74150	
1	4	1	211	2	1	11	1076			JXJI	STU	776			74160	
1	4	1	212	14	1	11	1274				SUB	TEMP			74170	
1	4	1	213	13	1	11	1376				STC	776			74180	
1	4	1	214	5	1	11	253				CIC	253		GREATER THAN 28.5	74190	
1	4	1	215	5	1	11	025				CIC	025		SEL LVDA + 28C	74200	
1	4	1	216	13	1	11	1076				STU	TEMP		RLAU A/D CONVERTER	74210	
1	4	1	217	2	1	11	1333				SUB	K35A			74220	
1	4	1	220	14	1	11	1274				STU	776		LESS THAN 27.5	74230	
1	4	1	221	13	1	11	1376				STU	776			74240	
1	4	1	222	17	1	11	134				CLA	K35D			74250	
1	4	1	223	2	1	11	1076			JXK2	SUB	TEMP		GREATER THAN 28.5	74260	
1	4	1	224	14	1	11	1274				STU	776			74270	
1	4	1	225	13	1	11	1376				STC	776			74280	
1	4	1	226	5	1	11	263				CIC	263		GREATER THAN 28.5	74290	
1	4	1	227	5	1	11	025				CIC	025		SEL LVDA + 28D	74300	
1	4	1	230	13	1	11	1076				STU	TEMP		READ A/D CONVERTER	74310	
1	4	1	231	2	1	11	1333				SUB	K35A			74320	
1	4	1	232	14	1	11	1274				STU	776			74330	
1	4	1	233	13	1	11	1376				STU	776		LESS THAN 27.5	74340	
1	4	1	234	17	1	11	134				CLA	K35B			74350	
1	4	1	235	2	1	11	1076				SUB	TEMP			74360	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 145)

IM	IS	S	LOC	UP	DM	OS	9	ADR	UCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	4	1	236	14	1	11	1	274				TM1	JVJ5		74410	
1	4	1	237	5	1	11	1	220				C1U	220	GREATER THAN 28.5	74420	
1	4	1	240	6	1	11	1	210	100000000			ANL	=010000000	READ 8 SWITCHES	74430	
1	4	1	241	4	1	11	1	250				TNZ	JY81	B2	74440	
1	4	1	242	10	1	11	1	263				TRA	JY81		74450	
1	4	1	243	13	1	11	1	076				STU	TEMP		74460	
1	4	1	244	17	1	11	1	211	000000400		JVJZ	CLA	=000000C400		74470	
1	4	1	245	5	1	11	1	203				C1U	603	SET LTE ERROR LAMP	74480	
1	4	1	246	17	1	11	1	076				CLA	TEMP		74490	
1	4	1	247	0	1	11	1	027				HOP	H95P7		74500	
1	4	1	250	13	1	11	1	376						SET AND RESET TE1H LATCH	74560	
1	4	1	251	17	1	11	1	033			JY81	STU	TE1H UP FOR TWO WORD TIMES	74570		
1	4	1	252	5	1	11	1	000				CLA	K77		74580	
1	4	1	253	17	1	11	1	212	000040000			C1U	000	SET INT INHIBIT	74590	
1	4	1	254	5	1	11	1	213				CLA	=0000040000		74610	
1	4	1	255	17	1	11	1	213	000020000			C1U	613		74620	
1	4	1	256	5	1	11	1	223				CLA	=0000020000		74630	
1	4	1	257	5	1	11	1	154				C1C	623		74640	
1	4	1	260	15	1	11	1	213	000020000			C1C	154		74650	
1	4	1	261	4	1	11	1	274				XDR	=0000020000		74660	
1	4	1	262	5	1	11	1	074				TNZ	JVJ5		74670	
1	4	1	263	5	1	11	1	106				C1U	074	RST INT 14	74680	
1	4	1	264	5	1	11	1	112				C1U	106		74690	
1	4	1	265	5	1	11	1	116				C1C	112		74700	
1	4	1	266	5	1	11	1	122				C1C	122		74710	
1	4	1	267	17	1	11	1	033				CLA	K77		74720	
1	4	1	270	5	1	11	1	000				C1C	000		74730	
1	4	1	271	0	1	11	1	023				HOP	H9P3		74740	
1	4	1	272	5	1	11	1	110				C1C	110		74750	
1	4	1	273	00	1	11	1	214	511010050			C1C	110		74760	
1	4	1	274	13	1	11	1	377				STO*	MAB1	INHIBIT ALL INTERRUPTS	74770	
1	4	1	275	00	1	11	1	215	501047600			TRA*	JAJ5A	RST INT REG	74780	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 146)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	UPC	VARIABLE	COMMENT	SEC	NO
1	5	0	20		1	11		135			MABI	ORG	1,5,0,20,1,11,		74860	
1	5	0	20	17	1	11	1	065				CLA	LCKIG		74880	
1	5	0	21	14	1	11	025					TMI	MACI		74890	
1	5	0	22	4	1	11	024					TNZ	MAHIA		74900	
1	5	0	23	0	1	11	1	022				HOP	I-2PI		74910	
1	5	0	24	00	1	11	216		531054270		MABIA	TRA*	MADZ		74920	
1	5	0	25	17	1	11	1	020			MACI	CLA	ZENK	EXERCISE TELEMETRY POWER SUPPLY SENSE INDICATORS	74930	
1	5	0	26	13	1	11	217				STU	STU	MCTR		74940	
1	5	0	27	5	1	11	066				CIC	CIC	O66		74950	
1	5	0	30	16	1	5	225				CCS	CCS	1,5		74960	
1	5	0	31	17	1	5	046				CLA	CLA	MAEI		74970	
1	5	0	32	6	1	5	1	047			ANC	ANC	KX8		74980	
1	5	0	33	13	1	5	1	076			STC	STC	TEMP	REMOVE ADDRESS	74990	
1	5	0	34	17	1	5	1	072			CLA	CLA	KMAEI		75000	
1	5	0	35	6	1	5	1	046			ANC	ANC	KX7	KEEP ADDRESS	75010	
1	5	0	36	15	1	5	1	076			XOR	XOR	TEMP		75020	
1	5	0	37	13	1	5	046				STU	STU	MAEI		75030	
1	5	0	41	17	1	11	231				CCS	CCS	1,11		75040	
1	5	0	42	5	1	11	220		000100000		CLA	CLA	=0000100000	RESET TEL P.S. SENSE	75050	
1	5	0	43	17	1	11	223		000040000		CIC	CIC	623	RESET INDICATOR	75070	
1	5	0	44	5	1	11	223				TRA	TRA	MAHI		75080	
1	5	0	45	10	1	11	101				CLA	CLA	MADATA		75090	
1	5	0	46	17	1	11	136				CIC	CIC	O22		75100	
1	5	0	47	5	1	11	022		000100000		CLA	CLA	=0000100000	LOAD DIN REG	75110	
1	5	0	51	10	1	11	213				TRA	TRA	MAJI	ENABLE TEL. P.S. SENSE	75120	
1	5	0	52	10	1	11	061				CIC	CIC	613		75130	
1	5	0	53	10	1	11	061				TRA	TRA	MAJI		75140	
1	5	0	54	13	1	11	377				MAJI	MAJI	777		75150	
1	5	0	55	17	1	11	221		000025234		STU	STU	777		75160	
1	5	0	56	2	1	11	032				CLA	CLA	=0000025234	DELAY 494 MSEC.	75170	
1	5	0	57	4	1	11	056				SUP	SUP	K1		75180	
1	5	0	60	0	1	11	377				TNZ	TNZ	*-1		75190	
1	5	0	61	17	1	11	220				HOP	HOP	777		75200	
1	5	0	62	5	1	11	223		000100000		CLA	CLA	=0000100000	DISABLE TEL P.S. SENSE	75210	
1	5	0	63	10	1	11	101				CIC	CIC	623		75220	
1	5	0	64	17	1	11	217				TRA	TRA	MAHI	DELAY	75230	
1	5	0	65	7	1	11	036				CLA	CLA	MCTN		75240	
1	5	0	66	13	1	11	217				ADD	ADD	KSI		75250	
1	5	0	67	2	1	11	222				STC	STC	MCTR		75260	
1	5	0	70	4	1	11	073		060000000		SUM	SUM	=0060000000	-24	75270	
1	5	0	71	10	1	11	106				TNZ	TNZ	MAGI		75280	
1	5	0	72	17	1	11	136				TRA	TRA	JXCI		75290	
1	5	0	73	16	1	5	225				CLA	CLA	MADATA		75300	
1	5	0	74	17	1	5	046				CCS	CCS	1,5		75310	
1	5	0	75	7	1	5	1	037			CLA	CLA	MAEI		75320	
1	5	0	76	13	1	5	046				ADD	ADD	KS2		75330	
1	5	0	77	16	1	11	231				STC	STC	MAEI	INCREMENT ADDRESS	75340	
1	5	0	100	10	1	11	043				CCS	CCS	1,11		75350	
1	5	0	101	13	1	11	377				TRA	TRA	MADI		75360	
1	5	0	102	17	1	11	223				STU	STU	777		75370	
1	5	0	103	2	1	11	1	032	000000360		PAHI	PAHI	=0000000360	DELAY 20 MSEC.	75380	
1	5	0	104	4	1	11	103				SUB	SUB	K1		75390	
1	5	0	105	0	1	11	377				TNZ	TNZ	*-1		75410	
1	5	0	105	4	1	11	377				HOP	HOP	777		75420	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 147)

IM	IS	LOC	OP	DM	DS	9	ADR	DCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	1	1	1	1	1	1	136	16524		MCATA	OC1	COC016524		75430	
1	1	1	1	1	1	1	137	12524			OC1	000012524		75440	
1	1	1	1	1	1	1	140	2524			OC1	000002524		75450	
1	1	1	1	1	1	1	141	6524			OC1	000006524		75460	
1	1	1	1	1	1	1	142	7524			OC1	000007524		75470	
1	1	1	1	1	1	1	143	6524			OC1	000006524		75480	
1	1	1	1	1	1	1	144	4524			OC1	000004524		75490	
1	1	1	1	1	1	1	145	5524			OC1	000005524		75500	
1	1	1	1	1	1	1	146	5724			OC1	000005724		75510	
1	1	1	1	1	1	1	147	5524			OC1	000005524		75520	
1	1	1	1	1	1	1	150	5124			OC1	C00005124		75530	
1	1	1	1	1	1	1	151	5324			OC1	000005324		75540	
1	1	1	1	1	1	1	152	5364			OC1	000005364		75550	
1	1	1	1	1	1	1	153	5324			OC1	000005324		75560	
1	1	1	1	1	1	1	154	5224			OC1	000005224		75570	
1	1	1	1	1	1	1	155	5264			OC1	000005264		75580	
1	1	1	1	1	1	1	156	5274			OC1	000005274		75590	
1	1	1	1	1	1	1	157	5264			OC1	000005264		75600	
1	1	1	1	1	1	1	160	5244			OC1	000005244		75610	
1	1	1	1	1	1	1	161	5254			OC1	000005254		75620	
1	1	1	1	1	1	1	162	5256			OC1	000005256		75630	
1	1	1	1	1	1	1	163	5254			OC1	000005254		75640	
1	1	1	1	1	1	1	164	5250			OC1	000005250		75650	
1	1	1	1	1	1	1	165	5252			OC1	000005252		75660	
1	1	1	1	1	1	1	166	6540		K100A	OC1	000006540	2-612 VDC	75670	
1	1	1	1	1	1	1	167	10520		K100B	OC1	000010520	3-381 VDC	75680	
1	1	1	1	1	1	1	170	6100		K100C	OC1	000006100	2-392 VDC	75690	
1	1	1	1	1	1	1	171	11160		K100D	OC1	000011160	3-601 VDC	75700	
1	1	1	1	1	1	1	172	106320		K100E	OC1	000106320	27-50 VDC	75710	
1	1	1	1	1	1	1	173	110740		K100F	OC1	000110740	28-49 VDC	75720	
1	1	1	1	1	1	1	174	51760		K100G	OC1	000051760	16-39 VDC	75730	
1	1	1	1	1	1	1	175	47740		K100H	OC1	000047740	15-6C VDC	75740	
1	1	1	1	1	1	1	176	25200		K100J	OC1	000025200	8-30 VDC	75750	
1	1	1	1	1	1	1	177	23560		K100K	OC1	000023560	7-70 VDC	75760	
1	5	0	106	17	1	1	212	000040000		JXG1	CLA	=0000040000	BIT 12	75780	
1	5	0	107	5	1	1	223			C10	C10	623		75790	
1	5	0	110	13	1	1	376			JXF2	STO	776	CHECK TELEMETRY CHANNELS A/D	75810	
1	5	0	111	17	1	1	224	000012070		CLA	CLA	=0000012070		75820	
1	5	0	112	5	1	1	022			C10	C10	022	LOAD DIN REG	75830	
1	5	0	113	17	1	1	220	000100000		CLA	CLA	=0000100000	BIT 11	75840	
1	5	0	114	5	1	1	213			C1C	C1C	613		75850	
1	5	0	115	10	1	1	101			TRA	TRA	MAHI	DELAY	75860	
1	5	0	116	5	1	1	303			C10	C10	303	SEL + 20 VDC TEL CHANNEL	75880	
1	5	0	117	5	1	1	025			C1C	C1C	025	READ A/D CONVERTER	75890	
1	5	0	120	13	1	1	076			STC	STC	TEMP		75900	
1	5	0	121	2	1	1	166			SUB	SUB	K100A		75910	
1	5	0	122	14	1	1	307			TMI	TMI	JXJ5		75920	
1	5	0	123	13	1	1	376			STC	STC	776		75930	
1	5	0	124	17	1	1	167			CLA	CLA	K100B		75940	
1	5	0	125	2	1	1	076			SUB	SUB	TEMP		75950	
1	5	0	126	14	1	1	307			TMI	TMI	JXJ5		75960	
1	5	0	127	13	1	1	376			STC	STC	776		75970	
1	5	0	130	5	1	1	313			C10	C10	313	SEL + 12 VDC TEL CHL	75980	
1	5	0	131	5	1	1	025			C10	C10	025	READ A/D CONVERTER	75990	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 148)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	5	0	132	13	1	11	1	076				STL	TEMP		76000	
1	5	0	133	2	1	11	1	166				SUB	K100A		76010	
1	5	0	134	14	1	11	1	307				TMI	JXJ5		76020	
1	5	0	135	13	1	11	1	376				STU	776		76030	
1	5	0	136	17	1	11	1	167				CLA	K100H		76040	
1	5	0	137	2	1	11	1	076				SUP	TEMP		76050	
1	5	0	140	14	1	11	1	307			JXJ3	TMI	JXJ5	SEL + 6 VDC TEL CHL	76060	
1	5	0	141	13	1	11	1	376				STU	776	READ A/D CONVERTER	76070	
1	5	0	142	5	1	11	1	323				CIC	323		76080	
1	5	0	143	5	1	11	1	025				CIC	025		76090	
1	5	0	144	2	1	11	1	170				SUB	K100C		76100	
1	5	0	145	14	1	11	1	147				TMI	**2		76110	
1	5	0	146	10	1	11	1	307			JXJ3	TRA	JXJ5		76120	
1	5	0	147	13	1	11	1	376				STU	776		76130	
1	5	0	150	5	1	11	1	333				CIC	333		76140	
1	5	0	151	5	1	11	1	025				CIC	025		76150	
1	5	0	152	13	1	11	1	076				STC	TEMP		76160	
1	5	0	153	2	1	11	1	166				SUB	K100A		76170	
1	5	0	154	14	1	11	1	307				TMI	JXJ5		76180	
1	5	0	155	13	1	11	1	376				STC	776		76190	
1	5	0	156	17	1	11	1	167				CLA	K100B		76200	
1	5	0	157	2	1	11	1	076				SUP	TEMP		76210	
1	5	0	160	14	1	11	1	307			JXJ3	TMI	JXJ5		76220	
1	5	0	161	13	1	11	1	376				STU	776		76230	
1	5	0	162	5	1	11	1	343				CIC	343		76240	
1	5	0	163	5	1	11	1	025				CIC	025		76250	
1	5	0	164	2	1	11	1	171				SUP	K100C		76260	
1	5	0	165	14	1	11	1	307			JXJ3	TMI	JXJ5		76270	
1	5	0	166	13	1	11	1	376				STC	776		76280	
1	5	0	167	5	1	11	1	353				CIC	353		76290	
1	5	0	170	5	1	11	1	025				CIC	025		76300	
1	5	0	171	2	1	11	1	170				SUB	K100C		76310	
1	5	0	172	14	1	11	1	174			JXJ3	TRA	JXJ5		76320	
1	5	0	173	10	1	11	1	307				STC	776		76330	
1	5	0	174	13	1	11	1	376		000100000		CLA	=0000100000		76340	
1	5	0	175	17	1	11	1	220				CIC	623		76350	
1	5	0	176	5	1	11	1	223		000040000		CLA	=0000040000		76360	
1	5	0	177	17	1	11	1	212				CIC	623		76370	
1	5	0	200	5	1	11	1	223		000005322		CLA	=000005322		76380	
1	5	0	201	17	1	11	1	225				CIC	022		76390	
1	5	0	202	5	1	11	1	022		000100000		CLA	=0000100000		76400	
1	5	0	203	17	1	11	1	220				CIC	613		76410	
1	5	0	204	5	1	11	1	213			JXJ3	TRA	MAF1		76420	
1	5	0	205	10	1	11	1	101				CIC	303		76430	
1	5	0	206	5	1	11	1	025				CIC	025		76440	
1	5	0	207	13	1	11	1	076				STU	TEMP		76450	
1	5	0	210	13	1	11	1	166				SUB	K100A		76460	
1	5	0	211	2	1	11	1	166				TMI	JXJ5		76470	
1	5	0	212	14	1	11	1	307				STU	776		76480	
1	5	0	213	13	1	11	1	376			JXJ3	CLA	K100R		76490	
1	5	0	214	17	1	11	1	167				SUB	TEMP		76500	
1	5	0	215	2	1	11	1	076				TMI	JXJ5		76510	
1	5	0	216	14	1	11	1	307				STU	776		76520	
1	5	0	217	13	1	11	1	376				CIC	313		76530	
1	5	0	220	5	1	11	1	313				CIC	025		76540	
1	5	0	221	5	1	11	1	025				STU	TEMP		76550	
1	5	0	222	13	1	11	1	076				STU	TEMP		76560	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 149)

IM	IS	S	LOC	OP	OM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	5	0	223	2	1	11	1	166				SUB	K100A		76570	
1	5	0	224	14	1	11	1	307				TMI	JXJ5		76580	
1	5	0	225	13	1	11	1	376				STO	776		76590	
1	5	0	226	17	1	11	1	167				CLA	K100B		76600	
1	5	0	227	2	1	11	1	076				SUB	TEMP		76610	
1	5	0	230	14	1	11	1	307				TMI	JXJ5		76620	
1	5	0	231	13	1	11	1	376			JZAI	STO	776	SEL + 6 VDC TEL CHL	76630	
1	5	0	232	5	1	11	1	025				CIC	323	READ A/D CONVERTER	76640	
1	5	0	233	5	1	11	1	025				CIC	025		76650	
1	5	0	234	13	1	11	1	076				STC	TEMP		76660	
1	5	0	235	2	1	11	1	166				SUB	K100A		76670	
1	5	0	236	14	1	11	1	307				TMI	JXJ5		76680	
1	5	0	237	13	1	11	1	376				STC	776		76690	
1	5	0	240	17	1	11	1	167				CLA	K100B		76700	
1	5	0	241	2	1	11	1	076				SUB	TEMP		76710	
1	5	0	242	14	1	11	1	307				TMI	JXJ5		76720	
1	5	0	243	13	1	11	1	376			JZCI	STC	776	SEL + 6 VDC SIG TEL CHL	76730	
1	5	0	244	5	1	11	1	333				CIC	333	READ A/D CONVERTER	76740	
1	5	0	245	5	1	11	1	025				CIC	025		76750	
1	5	0	246	13	1	11	1	076				STC	TEMP		76760	
1	5	0	247	2	1	11	1	166				SUB	K100A		76770	
1	5	0	250	14	1	11	1	307				TMI	JXJ5		76780	
1	5	0	251	13	1	11	1	376				STO	776		76790	
1	5	0	252	17	1	11	1	167				CLA	K100B		76800	
1	5	0	253	2	1	11	1	076				SUB	TEMP		76810	
1	5	0	254	14	1	11	1	307			JZEI	TMI	JXJ5	SEL - 6 VDC TEL CHL	76820	
1	5	0	255	13	1	11	1	376				STC	776	READ A/D CONVERTER	76830	
1	5	0	256	5	1	11	1	343				CIC	343		76840	
1	5	0	257	5	1	11	1	025				CIC	025		76850	
1	5	0	260	13	1	11	1	076				STO	TEMP		76860	
1	5	0	261	2	1	11	1	166				SUB	K100A		76870	
1	5	0	262	14	1	11	1	307				TMI	JXJ5		76880	
1	5	0	263	13	1	11	1	376				STC	776		76890	
1	5	0	264	17	1	11	1	167				CLA	K100B		76900	
1	5	0	265	14	1	11	1	076				SUB	TEMP		76910	
1	5	0	266	2	1	11	1	307				TMI	JXJ5		76920	
1	5	0	267	13	1	11	1	376			JZGI	STO	776	SEL - 20 VDC TEL CHL	76930	
1	5	0	270	5	1	11	1	353				CIC	353	READ A/D CONVERTER	76940	
1	5	0	271	5	1	11	1	025				CIC	025		76950	
1	5	0	272	13	1	11	1	076				STO	TEMP		76960	
1	5	0	273	2	1	11	1	166				SUB	K100A		76970	
1	5	0	274	14	1	11	1	307				TMI	JXJ5		76980	
1	5	0	275	13	1	11	1	376				STO	776		76990	
1	5	0	276	17	1	11	1	167				CLA	K100B		77000	
1	5	0	277	2	1	11	1	076				SUB	TEMP		77010	
1	5	0	300	14	1	11	1	307				TMI	JXJ5		77020	
1	5	0	301	10	1	11	1	020				TRA	JZJ1		77030	
1	5	1	20	17	1	11	1	200			JZJ1	ORG	1,5,1,20,1,11,	BIT 11	77040	
1	5	1	20	17	1	11	1	220	000100000			CLA	=00001		77050	
1	5	1	21	13	1	11	1	376				STO	776		77060	
1	5	1	22	5	1	11	1	223				CIC	623		77070	
1	5	1	23	17	1	11	1	212	000040000			CLA	=0000G40000	BIT 12	77080	
1	5	1	24	5	1	11	1	223				CIC	623		77090	
1	5	1	25	17	1	11	1	226	000003416			CLA	=000003416	LOAD DIN REC	77100	
1	5	1	26	5	1	11	1	022				CIC	022		77110	
1	5	1	27	17	1	11	1	220	000100000			CLA	=0000100000	BIT 11	77120	
1	5	1	30	5	1	11	1	213				CIC	613		77130	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 150)

IM	IS	S	LOC	OP	DP	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NC
1	5	1	31	10	1	11		101				TRA	MAH1	DELAY	77140	
1	5	1	32	5	1	11		303				CJC	303	SEL + 20 VDC TEL CHANNEL	77150	
1	5	1	33	5	1	11		025				CIU	025	READ A/D CONVERTER	77160	
1	5	1	34	2	1	11		170				SUB	K100C		77170	
1	5	1	35	14	1	11		037				TMI	**2		77180	
1	5	1	36	10	1	11		307				TRA	JXJ5		77190	
1	5	1	37	13	1	11		376				STC	776		77200	
1	5	1	40	5	1	11		313				CIU	313	SEL + 12 VDC TEL CHL	77210	
1	5	1	41	5	1	11		025				SUB	K100C	READ A/D CONVERTER	77220	
1	5	1	42	2	1	11		171				TMI	JXJ5		77230	
1	5	1	43	14	1	11		307				STC	776		77240	
1	5	1	44	13	1	11		376				CIU	025	SEL + 6 VDC TEL CHL	77250	
1	5	1	45	5	1	11		323				CJC	025	READ A/D CONVERTER	77260	
1	5	1	47	13	1	11		076				STC	TEMP		77270	
1	5	1	50	2	1	11		166				SUB	K100A		77280	
1	5	1	51	14	1	11		307				TMI	JXJ5		77290	
1	5	1	52	13	1	11		376				STC	776		77300	
1	5	1	53	17	1	11		167				CLA	K100H		77310	
1	5	1	54	2	1	11		076				SUB	TEMP		77320	
1	5	1	55	14	1	11		307				TMI	JXJ5		77330	
1	5	1	56	13	1	11		376				STC	776		77340	
1	5	1	57	5	1	11		333				CIU	333	SEL + 6 VDC SIG TEL CHL	77350	
1	5	1	61	2	1	11		170				CIU	025	READ A/D CONVERTER	77360	
1	5	1	62	14	1	11		064				SUB	K100C		77370	
1	5	1	63	10	1	11		307				TRA	**2		77380	
1	5	1	64	13	1	11		376				STC	JXJ5		77390	
1	5	1	65	5	1	11		343				CJC	343		77400	
1	5	1	66	5	1	11		025				CJC	025	SEL - 6 VDC TEL CHL	77410	
1	5	1	67	13	1	11		076				STC	TEMP	READ A/D CONVERTER	77420	
1	5	1	70	2	1	11		166				SUB	K100A		77430	
1	5	1	71	14	1	11		307				TMI	JXJ5		77440	
1	5	1	72	13	1	11		376				STC	776		77450	
1	5	1	73	17	1	11		167				CLA	K100R		77460	
1	5	1	74	2	1	11		076				SUB	TEMP		77470	
1	5	1	75	14	1	11		307				TMI	JXJ5		77480	
1	5	1	76	13	1	11		376				STC	776		77490	
1	5	1	77	5	1	11		353				CIU	353	SEL -20 VDC TEL CHL	77500	
1	5	1	100	5	1	11		025				CIU	025	READ A/D CONVERTER	77510	
1	5	1	101	2	1	11		171				SUB	K100D		77520	
1	5	1	102	14	1	11		307				TMI	JXJ5		77530	
1	5	1	103	13	1	11		376				STC	776		77540	
1	5	1	104	17	1	11		220	000100000			CLA	=0000100000		77550	
1	5	1	105	5	1	11		223				CIU	623	BIT 11	77560	
1	5	1	106	17	1	11		212	0000040000			CLA	=0000040000		77570	
1	5	1	107	5	1	11		223				CIU	623	BIT 12	77580	
1	5	1	110	17	1	11		227	000014744			CLA	=0000014744		77590	
1	5	1	111	5	1	11		022				CIU	022	LOAD DIN REG	77600	
1	5	1	112	17	1	11		220	000100000			CLA	=0000100000		77610	
1	5	1	113	5	1	11		213				CJC	613	BIT 11	77620	
1	5	1	114	10	1	11		101				TRA	MAH1		77630	
1	5	1	115	5	1	11		303				CJC	303	DELAY	77640	
1	5	1	116	5	1	11		025				CJC	025	SEL + 20 VDC TEL CHANNEL	77650	
1	5	1	117	2	1	11		171				SUB	K100C	READ A/D CONVERTER	77660	
1	5	1	120	14	1	11		307				TMI	JXJ5		77670	
1	5	1	121	13	1	11		376				STC	776		77680	
1	5	1	121	13	1	11		376				STC	776		77700	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 151)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ NO
1	5	1	122	5	1	11		313				C10	313	SEL + 12 VDC TEL CHL	77710
1	5	1	123	5	1	11		025				C10	025	READ A/D CONVERTER	77720
1	5	1	124	2	1	11		170				SUB	K100C		77730
1	5	1	125	14	1	11		127				TMI	**2		77740
1	5	1	126	10	1	11		307				TRA	JXJ5		77750
1	5	1	127	13	1	11		376				STO	776		77760
1	5	1	130	5	1	11		323		JZB3		C10	323	SEL + 6 VDC TEL CHL	77770
1	5	1	131	5	1	11		025				C10	025	READ A/D CONVERTER	77780
1	5	1	132	2	1	11		171				SUB	K100D		77790
1	5	1	133	14	1	11		307				TMI	JXJ5		77800
1	5	1	134	13	1	11		376				STO	776		77810
1	5	1	135	5	1	11		333				C10	333		77820
1	5	1	136	5	1	11		025				C10	025		77830
1	5	1	137	2	1	11		171				SUB	K100D		77840
1	5	1	140	14	1	11		307				TMI	JXJ5		77850
1	5	1	141	13	1	11		376		JZC3		STO	776		77860
1	5	1	142	5	1	11		343				C10	343		77870
1	5	1	143	5	1	11		025				C10	025		77880
1	5	1	144	2	1	11		170				SUB	K100C		77890
1	5	1	145	14	1	11		147				TMI	**2		77900
1	5	1	146	10	1	11		307				TRA	JXJ5		77910
1	5	1	147	13	1	11		376				STO	776		77920
1	5	1	150	5	1	11		353				C10	353		77930
1	5	1	151	5	1	11		025				C10	025		77940
1	5	1	152	13	1	11		076				STO	TEMP		77950
1	5	1	153	2	1	11		166				SUB	K100A		77960
1	5	1	154	14	1	11		307				TMI	JXJ5		77970
1	5	1	155	13	1	11		376				STO	776		77980
1	5	1	156	17	1	11		167				CLA	K100H		77990
1	5	1	157	2	1	11		076				SUB	TEMP		78000
1	5	1	160	14	1	11		307				TMI	JXJ5		78010
* CHECK VOLTAGE SWITCHING ON + 28 SIG															
1	5	1	161	13	1	11		376				STC	776		78030
1	5	1	162	17	1	11		220				CLA	=00C01CC00C	BIT 11	78040
1	5	1	163	5	1	11		223		000100000	JZF3	C10	623		78050
1	5	1	164	17	1	11		212		000040000		CLA	=0000040000	BIT 12	78060
1	5	1	165	5	1	11		223		000040000		C10	623		78070
1	5	1	166	17	1	11		006		000012524		CLA	=00C0012524		78080
1	5	1	167	5	1	11		022		000012524		C10	022	LOAD DIN REG	78090
1	5	1	170	17	1	11		220		000100000		CLA	=0000100000	BIT 11	78100
1	5	1	171	5	1	11		213		000100000		C10	613		78110
1	5	1	172	17	1	11		211		000000400		CLA	=0C00CC0400	BIT 18	78120
1	5	1	173	5	1	11		223		000000400		C10	623		78130
1	5	1	174	17	1	11		230		000001000		CLA	=0000001000	BIT 17	78140
1	5	1	175	5	1	11		223		000001000		C10	623		78150
1	5	1	176	10	1	11		054				TRA	MAJ1	DELAY	78160
1	5	1	177	10	1	11		054				TRA	MAJ1	DELAY	78170
1	5	1	200	5	1	11		053				C10	453	SEL + 28 SIG	78180
1	5	1	201	5	1	11		025				C10	025	READ A/D CONVERTER	78190
1	5	1	202	13	1	11		076				STC	TEMP		78200
1	5	1	203	2	1	11		172				SUB	K100E		78210
1	5	1	204	14	1	11		307				TMI	JXJ5		78220
1	5	1	205	13	1	11		376				STC	776		78230
1	5	1	206	17	1	11		173				CLA	K100F		78240
1	5	1	207	2	1	11		076				SUB	TEMP		78250
1	5	1	210	14	1	11		307				TMI	JXJ5	LESS THAN 27.5	78260
1	5	1	210	14	1	11		307				TMI	JXJ5		78270

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 152)

IM	IS	S	LOC	OP	CM	OS	9	ADR	UCT	VAL	LHS	GPC	VAR	TABLE	COMMENT	SEQ	NO
1	5	1	211	13	1	11	1	376			JZJ3	STC	776			78280	
1	5	1	212	17	1	11	1	032				CLA	K1			78290	
1	5	1	213	5	1	11	1	213				CIC	613			78300	
1	5	1	214	13	1	11	1	376			JZK3	STC	776			78310	
1	5	1	215	10	1	11	1	054				TRA	MAJ1			78320	
1	5	1	216	10	1	11	1	054				TRA	MAJ1		DELAY	78330	
1	5	1	217	5	1	11	1	053				CIC	453		DELAY	78340	
1	5	1	220	5	1	11	1	025				CIC	025		SEL + 28 SIG	78350	
1	5	1	221	13	1	11	1	076				STU	TEMP		READ A/D CONVERTER	78360	
1	5	1	222	2	1	11	1	175				SUP	K100H			78370	
1	5	1	223	14	1	11	1	307				TMI	JXJ5			78380	
1	5	1	224	13	1	11	1	376				STC	776			78390	
1	5	1	225	17	1	11	1	174				CLA	K1COG			78400	
1	5	1	226	2	1	11	1	076				SUB	TEMP			78410	
1	5	1	227	14	1	11	1	307				TMI	JXJ5			78420	
1	5	1	230	13	1	11	1	376			JZB4	STU	776			78430	
1	5	1	231	17	1	11	1	211		000000400		CLA	=0C000000400		BIT 18	78440	
1	5	1	232	5	1	11	1	223				CIC	623			78450	
1	5	1	233	10	1	11	1	054				TRA	MAJ1		DELAY	78460	
1	5	1	234	10	1	11	1	054				TRA	MAJ1		DELAY	78470	
1	5	1	235	5	1	11	1	053				CIC	453		SEL + 28 SIG	78480	
1	5	1	236	5	1	11	1	025				CIC	025		READ A/D CONVERTER	78490	
1	5	1	237	13	1	11	1	076				STC	TEMP			78500	
1	5	1	240	2	1	11	1	172				SUB	K1COE			78510	
1	5	1	241	14	1	11	1	307				TMI	JXJ5			78520	
1	5	1	242	13	1	11	1	376				STU	776			78530	
1	5	1	243	17	1	11	1	173				CLA	K100F			78540	
1	5	1	244	2	1	11	1	076				SUP	TEMP			78550	
1	5	1	245	14	1	11	1	307			JZC4	TMI	JXJ5			78560	
1	5	1	246	13	1	11	1	376		000000004		STU	776		BIT 24	78570	
1	5	1	247	17	1	11	1	010				CLA	=0C000000004			78580	
1	5	1	250	5	1	11	1	213				CIC	613			78590	
1	5	1	251	10	1	11	1	054				TRA	MAJ1		DELAY	78600	
1	5	1	252	10	1	11	1	054				TRA	MAJ1		DELAY	78610	
1	5	1	253	5	1	11	1	053				CIC	453		SEL + 28 SIG	78620	
1	5	1	254	5	1	11	1	025				CIC	025		READ A/D CONVERTER	78630	
1	5	1	255	13	1	11	1	076				STU	TEMP			78640	
1	5	1	256	2	1	11	1	177				SUP	K100K			78650	
1	5	1	257	14	1	11	1	307				TMI	JXJ5			78660	
1	5	1	260	13	1	11	1	376				STO	776			78670	
1	5	1	261	17	1	11	1	176				CLA	K100J			78680	
1	5	1	262	2	1	11	1	076				SUP	TEMP			78690	
1	5	1	263	14	1	11	1	307				TMI	JXJ5			78700	
1	5	1	264	13	1	11	1	376			JZD4	STC	776		BIT 17	78710	
1	5	1	265	17	1	11	1	230		000001000		CLA	=0C000001000			78720	
1	5	1	266	5	1	11	1	223				CIC	623			78730	
1	5	1	270	10	1	11	1	054				TRA	MAJ1		DELAY	78740	
1	5	1	271	5	1	11	1	053				TRA	MAJ1		DELAY	78750	
1	5	1	272	5	1	11	1	025				CIC	453		SEL + 28 SIG	78760	
1	5	1	273	13	1	11	1	076				CIC	025		READ A/D CONVERTER	78770	
1	5	1	274	2	1	11	1	172				SUB	TEMP			78780	
1	5	1	275	14	1	11	1	307				TMI	K100E			78790	
1	5	1	276	13	1	11	1	376				STC	JXJ5			78800	
1	5	1	277	17	1	11	1	173				CLA	776			78810	
1	5	1	300	2	1	11	1	076				SUB	K100F			78820	
1	5	1	301	14	1	11	1	307				TMI	JXJ5			78830	
1	5	1	301	14	1	11	1	307				TMI	JXJ5			78840	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 153)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NC
1	5	1	302	17	1	11	1	220	000100000			CLA	=0000100000	BIT 11	78850	
1	5	1	303	5	1	11	1	223				CIG	623		78860	
1	5	1	304	17	1	11	1	212	000040000			CLA	=0000040000	BIT 12	78870	
1	5	1	305	5	1	11	1	223				CIO	623		78880	
1	5	1	306	0	1	11	1	022				MOP	P2PI		78890	
1	5	1	307	13	1	11	1	377			JKJS	STC	777		78900	
1	5	1	310	00	1	11	1	215	501047600		TRA*	JAJ5A			78910	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 154)

IM	IS	S	LCC	OP	DM	DS	9	ADR	CCT	VAL	LMS	GPC	VARIABLE	COMMENT	SEQ	NO
1	7	1	40	17	1	13	1	2				ORG	1,7,1,40,1,13,2		18930	
1	7	1	40	17	1	13	1	2				ROUTINE II			18940	
1	7	1	41	14	1	13	1	056				CHANNEL SWITCHING TEST LVDA-ME			18950	
1	7	1	42	17	1	13	1	054				SEE PROCEDURE FOR PROPER VISUAL PATTERN			18960	
1	7	1	43	14	1	13	1	046			NAH1	TRA			18970	
1	7	1	44	13	1	13	1	054				CLA	LCR11		18980	
1	7	1	44	13	1	13	1	054				CLA	LCR		18990	
1	7	1	45	00	1	13	1	003			NAHIC	TRA			19000	
1	7	1	46	17	1	13	1	067	501004000			STU	NAHIC		19010	
1	7	1	47	17	1	13	1	034			NAHIA	TRA			19020	
1	7	1	50	5	1	13	1	223	000007200			CLA	=000002200	TO RTN 9 AND 10	19030	
1	7	1	51	17	1	13	1	020				CIC	623	RESET TFL AND PWR TEST	19040	
1	7	1	52	5	1	13	1	022				CLA	ZERU		19050	
1	7	1	53	5	1	13	1	042				CIO	022		19060	
1	7	1	54	5	1	13	1	036				CIO	042		19070	
1	7	1	55	10	1	13	1	044				CIC	036		19080	
1	7	1	56	17	1	13	1	000				TRA	NAHIC		19090	
1	7	1	57	7	1	13	1	261			NAH1	CLA	TIME		19100	
1	7	1	60	13	1	13	1	000	000000002			ADC	=000000002		19110	
1	7	1	61	2	1	13	1	262				STC	TIME		19120	
1	7	1	62	4	1	13	1	045	000000024			SUB	=000000024	TEN	19130	
1	7	1	63	13	1	13	1	000				TNZ	NAHIA		19140	
1	7	1	64	13	1	13	1	054				STC	TIME	SET EQUAL TO ZERO	19150	
1	7	1	65	10	1	13	1	067				STC	LCR		19160	
1	7	1	66	10	1	13	1	100				TRA	NAH1		19170	
1	7	1	67	13	1	13	1	377			NAH1	TRA	NAHIA		19180	
1	7	1	70	17	1	13	1	263				STU	777		19190	
1	7	1	71	5	1	13	1	223	000004000			CLA	=000004000	CAL POINT NR 26	19200	
1	7	1	72	17	1	13	1	264				CIC	623	RESET S.1.	19210	
1	7	1	73	5	1	13	1	203	000000012		NAH1	CLA	=000000012	HITS 23,25	19220	
1	7	1	74	17	1	13	1	265				CIC	603	SET TMR	19230	
1	7	1	75	5	1	13	1	223	000010000			CLA	=000010000	RIT 14	19240	
1	7	1	76	5	1	13	1	066				CIC	623	RESET DD ERRORS	19250	
1	7	1	77	0	1	13	1	377				CIC	066		19260	
1	7	1	100	17	1	13	1	266				HOP	777		19270	
1	7	1	101	5	1	13	1	000	000100000		NAHIA	CLA	=000100000	SET INT 15 INHIBIT	19280	
1	7	1	102	13	1	13	1	376				CIO	000		19290	
1	7	1	103	17	1	13	1	267			NAH1	STC	776		19300	
1	7	1	104	5	1	13	1	233	000000040			CLA	=000000040		19310	
1	7	1	105	17	1	13	1	270				CIO	633	BIT 21	19320	
1	7	1	106	2	1	13	1	032	000001622			CLA	=000001622	FULL SEQUENCE	19330	
1	7	1	107	4	1	13	1	106				SUB	K1	DELAY 75 PSEC.	19340	
1	7	1	110	5	1	13	1	154			*-1	TNZ	K1		19350	
1	7	1	111	6	1	13	1	265				CIC	154		19360	
1	7	1	112	4	1	13	1	126	000010000			ANC	=000010000		19370	
1	7	1	113	13	1	13	1	376				TNZ	NAJ5		19380	
1	7	1	114	17	1	13	1	271				CLA	776		19390	
1	7	1	115	2	1	13	1	032	00000266		NAHIA	SUP	K1	DELAY 15 MSEC.	19400	
1	7	1	116	4	1	13	1	115				TNZ	NAHIA		19410	
1	7	1	117	5	1	13	1	154				CIO	154	SHOULD GET INT 15 BEFORE END OF COUNT	19420	
1	7	1	120	6	1	13	1	265	000010000			ANC	=000010000		19430	
1	7	1	121	4	1	13	1	123				TNZ	NAK1		19440	
1	7	1	122	10	1	13	1	126				TRA	NAJ5		19450	
1	7	1	122	10	1	13	1	126				TRA	NAJ5		19460	
1	7	1	122	10	1	13	1	126				TRA	NAJ5		19470	
1	7	1	122	10	1	13	1	126				TRA	NAJ5		19480	
1	7	1	122	10	1	13	1	126				TRA	NAJ5		19490	

Figure 7-18. PTC ADAPT Self-Test Program (Sheet 155)

IM	IS	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NO
1	7	1123	5	1	13	100				NAK1	CIO	100		79500
1	7	1124	5	1	13	110					CIO	110		79510
1	7	1125	10	1	13	1045				NAJ5	TRA	NABIA	TO JABI	79520
1	7	1126	13	1	13	1377					STU	777		79530
1	7	1127	00	1	13	272		501047600			TRA*	JAJ5A		79540
1	7	1130	17	1	13	1066				NAB2	CLA	LCR11		79550
1	7	1131	14	1	13	1135					PMI	NAC2		79560
1	7	1132	4	1	13	1134					TNZ	PABIA		79570
1	7	1133	0	1	13	1022				NAB2A	HOP	H2PI		79580
1	7	1134	00	1	13	273		501014260		PABIA	TRA*	PABI		79590
1	7	1135	17	1	13	000				NAC2	CLA	TIME		79600
1	7	1136	4	1	13	1133					TNZ	NAB2A		79610
1	7	1137	13	1	13	1376				NAC2	STC	776		79620
1	7	1140	17	1	13	266		000100000			CLA	=00001C0000	SET INT 15 INHIBIT	79630
1	7	1141	5	1	13	000					CIO	000		79640
1	7	1142	17	1	13	274		000000100			CLA	=0000000100	BIT 2C	79650
1	7	1143	5	1	13	1233					CIC	633	HALF SEQUENCE	79660
1	7	1144	17	1	13	275		000000074			CLA	=0000000074	DELAY 5 MSEC.	79670
1	7	1145	2	1	13	1032					SUB	K1		79680
1	7	1146	4	1	13	1145					TNZ	*-1		79690
1	7	1147	5	1	13	1154					CIC	154		79700
1	7	1150	6	1	13	265		000010000			ANC	=0000001C000		79710
1	7	1151	4	1	13	1126					TNZ	NAJ5		79720
1	7	1152	13	1	13	1376					STU	776		79730
1	7	1153	17	1	13	275		000000074		NAD2A	CLA	=0000000074	DELAY 5 MSEC.	79740
1	7	1154	2	1	13	1032					SUB	K1		79750
1	7	1155	4	1	13	1154					TNZ	NAD2A		79760
1	7	1156	5	1	13	154					CIO	154	SHOULD GET INT 15 BEFORE END OF COUNT	79770
1	7	1157	6	1	13	265		000010000			ANC	=000001C000		79780
1	7	1160	4	1	13	1162					TNZ	NAF2		79790
1	7	1161	10	1	13	1126					TRA	NAJ5		79800
1	7	1162	5	1	13	100				NAF2	CIC	100		79810
1	7	1163	5	1	13	110					CIO	110		79820
1	7	1164	17	1	13	1030					CLA	HJAJ5		79830
1	7	1165	13	1	13	1004		400000000			STU	404		79840
1	7	1166	17	1	13	276					CLA	=0400000000		79850
1	7	1167	5	1	13	066					CIO	066	ENABLE COMPARE	79860
1	7	1170	13	1	13	1054					STO	LCB	CHANNEL SWITCHING IN PROGRESS	79870
1	7	1171	17	1	13	001					CLA	CSCTR		79880
1	7	1172	4	1	13	1213					TNZ	NAB3		79900
1	7	1173	16	1	7	227					CDS	1,7	CAL POINT NR 27	79910
1	7	1174	17	1	7	213					CLA	NAB3		79920
1	7	1175	6	1	7	1040					ANC	KX1	REMOVE ADDRESS	79930
1	7	1176	13	1	7	1076					STU	TEMP		79940
1	7	1177	17	1	7	250					CLA	KNAB3		79950
1	7	1200	6	1	7	1045					ANC	KX6	KEEP ADDRESS	79960
1	7	1201	15	1	7	1076					XOR	TEMP		79970
1	7	1202	13	1	7	213					STC	NAB3		79980
1	7	1203	17	1	7	220					CLA	NAC3		79990
1	7	1204	6	1	7	1040					ANC	KX1	REMOVE ADDRESS	80000
1	7	1205	13	1	7	1076					STU	TEMP		80010
1	7	1206	17	1	7	251					CLA	KNAC3		80020
1	7	1207	6	1	7	1045					AND	KX6	KEEP ADDRESS	80030
1	7	1210	15	1	7	1076					XOR	TEMP		80040
1	7	1211	13	1	7	220					STO	NAC3		80050
1	7	1211	13	1	7	220					STO	NAC3		80060

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 156)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
1	7	1	212	16	1	13		233			NAB3	CDS	1,13		80070	
1	7	1	213	17	1	13		005				CLA	KDI		80080	
1	7	1	214	13	1	13	1	074				STU	VAK5	ERROR INFO	80090	
1	7	1	215	5	1	13		022				CIO	022	LOAD DIN REG	80100	
1	7	1	216	5	1	13		071				CIC	071	READ DIN REG	80110	
1	7	1	217	16	1	12		232				CDS	1,12		80120	
1	7	1	220	17	1	12		000				CLA	KEM1		80130	
1	7	1	221	13	1	12	1	073				STU	VAK4	ERROR INFO	80140	
1	7	1	222	5	1	12		042				CIO	042	LOAD EM REG	80150	
1	7	1	223	5	1	12		111				CIO	111	READ EM REG	80160	
1	7	1	224	16	1	7		227				CDS	1,7		80170	
1	7	1	225	17	1	7		213				CLA	NAB3		80180	
1	7	1	226	7	1	7		036				ACC	KSI		80190	
1	7	1	227	13	1	7		213				STU	NAB3	INCREMENT ADDRESS	80200	
1	7	1	230	17	1	7		220				CLA	NAC3		80210	
1	7	1	231	7	1	7		036				ACC	KSI		80220	
1	7	1	232	13	1	7		220				STU	NAC3	INCREMENT ADDRESS	80230	
1	7	1	233	16	1	13		233				CDS	1,13		80240	
1	7	1	234	17	1	13		001				CLA	CSCTR		80250	
1	7	1	235	7	1	13		032				ACC	KI		80260	
1	7	1	236	13	1	13		001				STU	CSCTR	INCREMENT CTR	80270	
1	7	1	237	2	1	13		277	000000406			SUB	-000000406	=131 DEC.	80280	
1	7	1	240	14	1	13		122				TMI	NAF3		80290	
1	7	1	241	17	1	13		300	000030000			CLA	-0000030000	BITS 13,14	80300	
1	7	1	242	5	1	13		213				CIO	613		80310	
1	7	1	243	17	1	13		001				CLA	CSCTR		80320	
1	7	1	244	2	1	13		301	000000530			SUB	=000000530	=172 DEC.	80330	
1	7	1	245	4	1	13		304				TNZ	NAB5		80340	
1	7	1	246	13	1	13		001				STU	CSCTR	=0	80350	
1	7	1	247	10	1	13		304				TRA	NAH5		80360	
1	7	1	250	17	1	13		005				CLA	NAH5		80370	
1	7	1	251	17	1	12		000				DOG	1,12,0		80380	
1	7	1	251	17	1	13		3				CLA	KEM1		80390	
1	7	1	252	17	1	13		001				DOG	1,13		80400	
1	7	1	253	2	1	13		302	000000262			CLA	CSCTR		80410	
1	7	1	254	14	1	13		1260				SUB	-000000262	=49 DEC.	80420	
1	7	1	255	17	1	13		303				TMI	NAG3	LESS THAN 47	80430	
1	7	1	256	5	1	13		213	000024000			CLA	=0000024000	BITS 13,15	80440	
1	7	1	257	10	1	13		1304				CIC	613		80450	
1	7	1	260	17	1	13		001				TRA	NAH5		80460	
1	7	1	261	2	1	13		304	000000136			CLA	CSCTR		80470	
1	7	1	262	14	1	13		1266				SUB	-000000136	=47 DEC.	80480	
1	7	1	263	17	1	13		305	000022000			TMI	NAH3	LESS THAN 47	80490	
1	7	1	264	5	1	13		213				CLA	=0000022000	BITS 13,16	80500	
1	7	1	265	10	1	13		1304				CIC	613	SET CHZ	80510	
1	7	1	266	17	1	13		001				TRA	NAH5		80520	
1	7	1	267	2	1	13		264	000000012			CLA	CSCTR		80530	
1	7	1	270	14	1	13		1274				SUB	-000000012	=5	80540	
1	7	1	271	17	1	13		306	000021000			TMI	NAJ3	LESS THAN 5	80550	
1	7	1	272	5	1	13		1213				CLA	-0000021000	BITS 13,17	80560	
1	7	1	273	10	1	13		1304				CIO	613		80570	
1	7	1	274	17	1	13		001				TRA	NAB5		80580	
1	7	1	275	2	1	13		307	000000004			CLA	CSCTR		80590	
1	7	1	276	14	1	13		1271				SUB	=000000004		80600	
1	7	1	277	4	1	13		1301				TMI	NAH4		80610	
1	7	1	300	10	1	13		1283				TNZ	**2		80620	
1	7	1	300	10	1	13		1283				TRA	NAG4		80630	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 157)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	7	1	301	2	1	13	1	032				SUB	K1	=1	80640	
1	7	1	302	4	1	13	1	241				TNZ	NAB4		80650	
1	7	1	303	10	1	13	1	255				TRA	NAF4		80660	
1	7	1	304	13	1	13	1	376			NAB5	STC	776		80670	
1	7	1	305	17	1	13	1	310	000000360			CLA	=000000360		80680	
1	7	1	306	2	1	13	1	032			NAB5A	SUB	K1		80690	
1	7	1	307	4	1	13	1	306				TNZ	NAB5A		80700	
1	7	1	310	5	1	13	1	154				CIC	154		80710	
1	7	1	311	6	1	13	1	265	000010000			AND	=000010000		80720	
1	7	1	312	4	1	13	1	126				TNZ	NAJ5		80730	
1	7	1	313	13	1	13	1	376			NAC5	STU	776		80740	
1	7	1	314	17	1	13	1	275	000000074			CLA	=000000074		80750	
1	7	1	315	2	1	13	1	032				SUB	K1		80760	
1	7	1	316	4	1	13	1	315				TNZ	*-1		80770	
1	7	1	317	5	1	13	1	154				CIC	154		80780	
1	7	1	320	6	1	13	1	265	000010000			AND	=000010000		80790	
1	7	1	321	4	1	13	1	323				TNZ	NAD5A		80800	
1	7	1	322	0	1	13	1	030				HOP	HJAJ5		80810	
1	7	1	323	5	1	13	1	100			NAC5A	CIC	100		80820	
1	7	1	324	10	1	13	1	040				TRA	NRA1		80830	
1	7	0	40								*	TEST DISAGREEMENT DETECTORS AND CHANNEL		80840		
1	7	0	40								*	ERROR INDICATORS		80850		
1	7	0	41	17	1	13	1	002			NBA1	CLA	1,2,0,40,1,13,	80860		
1	7	0	42	13	1	13	1	032				DCCTR		80870		
1	7	0	43	2	1	13	1	307				STU		80880		
1	7	0	44	14	1	13	1	076	000000004			SUB	=000000004	80890		
1	7	0	45	2	1	13	1	032				TMI	NBC2	DDCTR = 1	80900	
1	7	0	46	14	1	13	1	114				SUB	K1	DDCTR = 2	80910	
1	7	0	47	2	1	13	1	032				TMI	NBC2	DDCTR = 3	80920	
1	7	0	50	14	1	13	1	132				TMI	NRE2	DDCTR = 4	80930	
1	7	0	51	2	1	13	1	032				SUB	K1	DDCTR = 5	80940	
1	7	0	52	14	1	13	1	152				TMI	NBF2	DDCTR=6	80950	
1	7	0	53	2	1	13	1	032				SUB	K1		80960	
1	7	0	54	14	1	13	1	170				TMI	NBG2		80970	
1	7	0	55	13	1	13	1	002			NBH1	STO	DCCTR		80980	
1	7	0	56	13	1	13	1	376			NBH2	STU	776		80990	
1	7	0	57	17	1	13	1	311	000002000			CLA	=000002000		81000	
1	7	0	60	5	1	13	1	223				CIC	623		81010	
1	7	0	61	17	1	13	1	267	000000040			CLA	=000000040		81020	
1	7	0	62	5	1	13	1	203				CIC	603		81030	
1	7	0	63	17	1	13	1	312	222000000			CLA	=022200000		81040	
1	7	0	64	5	1	13	1	036				CIC	036		81050	
1	7	0	65	5	1	13	1	105				CIC	105		81060	
1	7	0	66	17	1	13	1	265	000010000			CLA	=000010000		81070	
1	7	0	67	5	1	13	1	223				CIC	623		81080	
1	7	0	70	17	1	13	1	313	000000014			CLA	=000000014		81090	
1	7	0	71	5	1	13	1	203				CIC	603		81100	
1	7	0	72	17	1	13	1	314	000000200			CLA	=000000200		81110	
1	7	0	73	5	1	13	1	223				CIC	623		81120	
1	7	0	74	12	1	13	1	002				PIC	402		81130	
1	7	0	75	10	1	13	1	223				TRA	NBG4		81140	
1	7	0	76	13	1	13	1	376				STC	776		81150	
1	7	0	77	17	1	13	1	274	000000100			CLA	=000000100		81160	
1	7	0	100	5	1	13	1	203				CIC	603		81170	
1	7	0	101	17	1	13	1	315	333000000			CLA	=033300000		81180	
1	7	0	102												81190	
1	7	0	103												81200	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 158)

IM	IS	S	LQC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	7	0	102	5	1	13	036					CIC	036		81210	
1	7	0	103	5	1	13	105					CJU	105		81220	
1	7	0	104	17	1	13	265	000010000				CLA	=000010000	LOAD DDAS	81230	
1	7	0	105	5	1	13	273					CIC	623	READ DDAS	81240	
1	7	0	106	17	1	13	262	000000024				CLA	=000000024		81250	
1	7	0	107	5	1	13	203					CIC	603	SET CHL 1	81260	
1	7	0	110	17	1	13	316	000000050				CLA	=000000050	SET PWR TEST 1 AND TEL +8 IND	81270	
1	7	0	111	5	1	13	213					CIC	613		81280	
1	7	0	112	12	1	13	002					PIC	402		81290	
1	7	0	113	10	1	13	205					TRA	N8C4		81300	
1	7	0	114	13	1	13	376					STC	776		81310	
1	7	0	115	17	1	13	274	000000100				CLA	=000000100	INACTIVE CHL = 0	81320	
1	7	0	116	5	1	13	203					CIC	603		81330	
1	7	0	117	17	1	13	317	266400000				CLA	=026640000		81340	
1	7	0	120	5	1	13	036					CIC	036	DDAS	81350	
1	7	0	121	5	1	13	105					CIC	105		81360	
1	7	0	122	17	1	13	265	000010000				CLA	=000010000		81370	
1	7	0	123	5	1	13	223					CLA	=000000022		81380	
1	7	0	124	17	1	13	320	000000022				CLA	=000000022		81390	
1	7	0	125	5	1	13	203					CIC	603	SET CHL 2	81400	
1	7	0	126	17	1	13	274	000000100				CLA	=000000100	SET PWR TEST 2	81410	
1	7	0	127	5	1	13	213					CIC	613		81420	
1	7	0	130	12	1	13	002					PIU	402		81430	
1	7	0	131	10	1	13	205					TRA	N8C4		81440	
1	7	0	132	13	1	13	376					STU	776		81450	
1	7	0	133	17	1	13	311	000007000				CLA	=000007000		81460	
1	7	0	134	5	1	13	223					CIC	623		81470	
1	7	0	135	17	1	13	274	000000100				CLA	=000000100		81480	
1	7	0	136	5	1	13	203					CIC	603		81490	
1	7	0	137	17	1	13	321	155400000				CLA	=015400000	INACTIVE CHL = 0	81500	
1	7	0	140	5	1	13	036					CIC	036		81510	
1	7	0	141	5	1	13	105					CIC	105		81520	
1	7	0	142	17	1	13	265	000010000				CLA	=000010000		81530	
1	7	0	143	5	1	13	223					CIC	623		81540	
1	7	0	144	17	1	13	313	000000014				CLA	=000000014	SET CHL 3	81550	
1	7	0	145	5	1	13	203					CIC	603		81560	
1	7	0	146	17	1	13	314	000000200				CLA	=000000200	SET PWR TEST 3	81570	
1	7	0	147	5	1	13	213					CIC	613		81580	
1	7	0	150	12	1	13	002					PIU	402		81590	
1	7	0	151	10	1	13	205					TRA	N8C4		81600	
1	7	0	152	13	1	13	376					STU	776		81610	
1	7	0	153	17	1	13	267	000000040				CLA	=000000040	INACTIVE CHL = 1	81620	
1	7	0	154	5	1	13	203					CIC	603		81630	
1	7	0	155	17	1	13	322	044400000				CLA	=004400000		81640	
1	7	0	156	5	1	13	036					CIC	036		81650	
1	7	0	157	5	1	13	105					CIC	105		81660	
1	7	0	160	17	1	13	265	000010000				CLA	=000010000		81670	
1	7	0	161	5	1	13	223					CIC	623		81680	
1	7	0	162	17	1	13	262	000000024				CLA	=000000024	SET CHL 1	81690	
1	7	0	163	5	1	13	203					CIC	603		81700	
1	7	0	164	17	1	13	323	000000420				CLA	=000000420	SET PWR TEST 4 AND TEL -8 IND	81710	
1	7	0	165	5	1	13	213					CIC	613		81720	
1	7	0	166	12	1	13	002					PIU	402		81730	
1	7	0	167	10	1	13	205					TRA	N8C4		81740	
1	7	0	170	13	1	13	376					STC	776		81750	
1	7	0	171	17	1	13	267	000000040				CLA	=000000040	INACTIVE CHL = 1	81760	
1	7	0	172	5	1	13	203					CIC	603		81770	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 159)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	7	0	173	17	1	13		324	111000000			CLA	=0111C0CC00		81780	
1	7	0	174	5	1	13		036				CIC	036		81790	
1	7	0	175	5	1	13		105				CIO	105		81800	
1	7	0	176	17	1	13		265	000010000			CLA	=0000010000		81810	
1	7	0	177	5	1	13		223				CIC	623		81820	
1	7	0	200	17	1	13		320	000000022			CLA	=00CCCC0022	SET CHL 2	81830	
1	7	0	201	5	1	13		203				CIO	603		81840	
1	7	0	202	17	1	13		267	000000040			CLA	=0000000040	SET PMR TEST 1	81850	
1	7	0	203	5	1	13		213				CIC	613		81860	
1	7	0	204	12	1	13		002				PIO	402		81870	
1	7	0	205	13	1	13		376				STO	776		81880	
1	7	0	206	17	1	13		310	000000360		NBC4	CLA	=0000000360	DELAY 20 MSEC.	81890	
1	7	0	207	2	1	13		032				SUB	K1		81900	
1	7	0	210	4	1	13		207				TNZ	*-1		81910	
1	7	0	211	5	1	13		154				CIO	154		81920	
1	7	0	212	6	1	13		265	000010000			ANC	=0000010000		81930	
1	7	0	213	4	1	13		126				TNZ	NAJ5		81940	
1	7	0	214	17	1	13		275	000000074		NBE4	CLA	=00C0CC0074	DELAY 5 MSEC.	81950	
1	7	0	215	2	1	13		032				SUR	K1		81960	
1	7	0	216	4	1	13		215				TNZ	*-1		81970	
1	7	0	217	5	1	13		154				CIC	154		81980	
1	7	0	220	6	1	13		265	000010000			ANU	=00C00010000		81990	
1	7	0	221	4	1	13		223				NBG4			82000	
1	7	0	222	0	1	13		030				TNZ	HJAJ5		82010	
1	7	0	223	5	1	13		100				HOP	100		82020	
1	7	0	224	5	1	13		110				CIC	100		82030	
1	7	0	225	0	1	13		022			NBG4	CIO	110		82040	
1	7	0	225	0	1	12		0				HOP	H2P1		82050	
1	7	0	225	0	1	12		0				00G	1,12,0		82060	
1	7	0	225	1	12	1		0	774014000		KEM1	CCT	774014000		82070	
1	7	0	225	1	12	2		0	777760000		KEM2	OC1	777760000		82080	
1	7	0	225	1	12	3		0	777760000		KEM3	OC1	777760000		82090	
1	7	0	225	1	12	4		0	777774000		KEM4	OC1	777774000		82100	
1	7	0	225	1	12	5		0	774014000		KEM5	OC1	774014000		82110	
1	7	0	225	1	12	6		0	774014000		KEM6	OC1	774014000		82120	
1	7	0	225	1	12	7		0	774014000		KEM7	OC1	774014000		82130	
1	7	0	225	1	12	8		0	774014000		KEM8	OC1	774014000		82140	
1	7	0	225	1	12	9		0	774014000		KEM9	OC1	774014000		82150	
1	7	0	225	1	12	10		0	774014000		KEM10	OC1	774014000		82160	
1	7	0	225	1	12	11		0	774004000		KEM11	OC1	774004000		82170	
1	7	0	225	1	12	12		0	774014000		KEM12	OC1	774014000		82180	
1	7	0	225	1	12	13		0	774014000		KEM13	OC1	774014000		82190	
1	7	0	225	1	12	14		0	774014000		KEM14	OC1	774014000		82200	
1	7	0	225	1	12	15		0	774014000		KEM15	OC1	774014000		82210	
1	7	0	225	1	12	16		0	774014000		KEM16	OC1	774014000		82220	
1	7	0	225	1	12	17		0	774014000		KEM17	OC1	774014000		82230	
1	7	0	225	1	12	20		0	774014000		KEM18	OC1	774014000		82240	
1	7	0	225	1	12	21		0	774014000		KEM19	OC1	774014000		82250	
1	7	0	225	1	12	22		0	774034000		KEM20	OC1	774034000		82260	
1	7	0	225	1	12	23		0	774054000		KEM21	OC1	774054000		82270	
1	7	0	225	1	12	24		0	774114000		KEM22	OC1	774114000		82280	
1	7	0	225	1	12	25		0	774214000		KEM23	OC1	774214000		82290	
1	7	0	225	1	12	26		0	774414000		KEM24	OC1	774414000		82300	
1	7	0	225	1	12	27		0	775014000		KEM25	OC1	775014000		82310	
1	7	0	225	1	12	30		0	776014000		KEM26	OC1	776014000		82320	
1	7	0	225	1	12	31		0	774014000		KEM27	OC1	774014000		82330	
1	7	0	225	1	12	32		0	774014000		KEM28	OC1	774014000		82340	
1	7	0	225	1	12	33		0	774014000		KEM29	OC1	774014000		82350	
1	7	0	225	1	12	34		0	774014000		KEM29	OC1	774014000		82360	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 160)

IM	ES	S	LOC	OP	DP	DS	9	ADR	CCF	VAL	LHS	CPC	VARIABLE	COMMENT	SEC	NO
1	12	35	774014000	KEM30	OC1	774014000	OC1	774014000							82350	
1	12	36	774014000	KEM31	OC1	774014000	OC1	774014000							82360	
1	12	37	774014000	KEM32	OC1	774014000	OC1	774014000							82370	
1	12	40	770014000	KEM33	OC1	770014000	OC1	770014000							82380	
1	12	41	764014000	KEM34	OC1	764014000	OC1	764014000							82390	
1	12	42	754014000	KEM35	OC1	754014000	OC1	754014000							82400	
1	12	43	734014000	KEM36	OC1	734014000	OC1	734014000							82410	
1	12	44	674014000	KEM37	OC1	674014000	OC1	674014000							82420	
1	12	45	574014000	KEM38	OC1	574014000	OC1	574014000							82430	
1	12	46	374014000	KEM39	OC1	374014000	OC1	374014000							82440	
1	12	47	774014000	KEM40	OC1	774014000	OC1	774014000							82450	
1	12	50	774014000	KEM41	OC1	774014000	OC1	774014000							82460	
1	12	51	774014000	KEM42	OC1	774014000	OC1	774014000							82470	
1	12	52	774014000	KEM43	OC1	774014000	OC1	774014000							82480	
1	12	53	774014000	KEM44	OC1	774014000	OC1	774014000							82490	
1	12	54	774014000	KEM45	OC1	774014000	OC1	774014000							82510	
1	12	55	774014000	KEM46	OC1	774014000	OC1	774014000							82520	
1	12	56	777760000	KEM47	OC1	777760000	OC1	777760000							82540	
1	12	57	777760000	KEM48	OC1	777760000	OC1	777760000							82550	
1	12	60	777760000	KEM49	OC1	777760000	OC1	777760000							82570	
1	12	61	777760000	KEM50	OC1	777760000	OC1	777760000							82580	
1	12	62	777760000	KEM51	OC1	777760000	OC1	777760000							82590	
1	12	63	777764000	KEM52	OC1	777764000	OC1	777764000							82610	
1	12	64	777770000	KEM53	OC1	777770000	OC1	777770000							82620	
1	12	65	777760000	KEM54	OC1	777760000	OC1	777760000							82630	
1	12	66	777760000	KEM55	OC1	777760000	OC1	777760000							82640	
1	12	67	777760000	KEM56	OC1	777760000	OC1	777760000							82650	
1	12	70	777760000	KEM57	OC1	777760000	OC1	777760000							82670	
1	12	71	777760000	KEM58	OC1	777760000	OC1	777760000							82680	
1	12	72	777760000	KEM59	OC1	777760000	OC1	777760000							82690	
1	12	73	777760000	KEM60	OC1	777760000	OC1	777760000							82710	
1	12	74	777740000	KEM61	OC1	777740000	OC1	777740000							82720	
1	12	75	777720000	KEM62	OC1	777720000	OC1	777720000							82730	
1	12	76	777660000	KEM63	OC1	777660000	OC1	777660000							82740	
1	12	77	777560000	KEM64	OC1	777560000	OC1	777560000							82750	
1	12	100	777360000	KEM65	OC1	777360000	OC1	777360000							82760	
1	12	101	776760000	KEM66	OC1	776760000	OC1	776760000							82770	
1	12	102	775760000	KEM67	OC1	775760000	OC1	775760000							82780	
1	12	103	777760000	KEM68	OC1	777760000	OC1	777760000							82790	
1	12	104	777760000	KEM69	OC1	777760000	OC1	777760000							82800	
1	12	105	777760000	KEM70	OC1	777760000	OC1	777760000							82810	
1	12	106	777760000	KEM71	OC1	777760000	OC1	777760000							82820	
1	12	107	777760000	KEM72	OC1	777760000	OC1	777760000							82830	
1	12	110	777760000	KEM73	OC1	777760000	OC1	777760000							82840	
1	12	111	777760000	KEM74	OC1	777760000	OC1	777760000							82850	
1	12	112	773760000	KEM75	OC1	773760000	OC1	773760000							82860	
1	12	113	767760000	KEM76	OC1	767760000	OC1	767760000							82870	
1	12	114	757760000	KEM77	OC1	757760000	OC1	757760000							82880	
1	12	115	737760000	KEM78	OC1	737760000	OC1	737760000							82890	
1	12	116	677760000	KEM79	OC1	677760000	OC1	677760000							82900	
1	12	117	577760000	KEM80	OC1	577760000	OC1	577760000							82910	
1	12	120	377760000	KEM81	OC1	377760000	OC1	377760000								
1	12	121	777760000	KEM82	OC1	777760000	OC1	777760000								
1	12	122	777760000	KEM83	OC1	777760000	OC1	777760000								
1	12	123	777760000	KEM84	OC1	777760000	OC1	777760000								
1	12	124	777760000	KEM85	OC1	777760000	OC1	777760000								
1	12	125	777760000	KEM86	OC1	777760000	OC1	777760000								

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 161)

IM	IS	S	LOC	OP	DR	DS	9	ADR	DCI	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	12	126							777760000	KEP87	DCI	777760000		82920		
1	12	127							777760000	KEP88	DCI	777760000		82930		
1	12	130							777760000	KEP89	DCI	777760000		82940		
1	12	131							777760000	KEP90	DCI	777760000		82950		
1	12	132							777760000	KEP91	DCI	777760000		82960		
1	12	133							777760000	KEP92	DCI	777760000		82970		
1	12	134							777760000	KEP93	DCI	777760000		82980		
1	12	135							777764000	KEP94	DCI	777764000		82990		
1	12	136							777770000	KEP95	DCI	777770000		83000		
1	12	137							777760000	KEP96	DCI	777760000		83010		
1	12	140							777760000	KEP97	DCI	777760000		83020		
1	12	141							777760000	KEP98	DCI	777760000		83030		
1	12	142							777760000	KEP99	DCI	777760000		83040		
1	12	143							777760000	KEP100	DCI	777760000		83050		
1	12	144							777760000	KEP101	DCI	777760000		83060		
1	12	145							777760000	KEP102	DCI	777760000		83070		
1	12	146							777740000	KEP103	DCI	777740000		83080		
1	12	147							777720000	KEP104	DCI	777720000		83090		
1	12	150							777660000	KEP105	DCI	777660000		83100		
1	12	151							777560000	KEP106	DCI	777560000		83110		
1	12	152							777360000	KEP107	DCI	777360000		83120		
1	12	153							776760000	KEP108	DCI	776760000		83130		
1	12	154							775760000	KEP109	DCI	775760000		83140		
1	12	155							777760000	KEP110	DCI	777760000		83150		
1	12	156							777760000	KEP111	DCI	777760000		83160		
1	12	157							777760000	KEP112	DCI	777760000		83170		
1	12	160							777760000	KEP113	DCI	777760000		83180		
1	12	161							777760000	KEP114	DCI	777760000		83190		
1	12	162							777760000	KEP115	DCI	777760000		83200		
1	12	163							777760000	KEP116	DCI	777760000		83210		
1	12	164							773760000	KEP117	DCI	773760000		83220		
1	12	165							767760000	KEP118	DCI	767760000		83230		
1	12	166							757760000	KEP119	DCI	757760000		83240		
1	12	167							737760000	KEP120	DCI	737760000		83250		
1	12	170							677760000	KEP121	DCI	677760000		83260		
1	12	171							577760000	KEP122	DCI	577760000		83270		
1	12	172							377760000	KEP123	DCI	377760000		83280		
1	12	173							777760000	KEP124	DCI	777760000		83290		
1	12	174							777760000	KEP125	DCI	777760000		83300		
1	12	175							777760000	KEP126	DCI	777760000		83310		
1	12	176							777760000	KEP127	DCI	777760000		83320		
1	12	177							777760000	KEP128	DCI	777760000		83330		
1	12	200							777760000	KEP129	DCI	777760000		83340		
1	12	201							777760000	KEP130	DCI	777760000		83350		
1	12	202							777774000	KEP131	DCI	777774000		83360		
1	12	203							777774000	KEP132	DCI	777774000		83370		
1	12	204							777774000	KEP133	DCI	777774000		83380		
1	12	205							777774000	KEP134	DCI	777774000		83390		
1	12	206							777774000	KEP135	DCI	777774000		83400		
1	12	207							777770000	KEP136	DCI	777770000		83410		
1	12	210							777764000	KEP137	DCI	777764000		83420		
1	12	211							777774000	KEP138	DCI	777774000		83430		
1	17	212							777774000	KEP139	DCI	777774000		83440		
1	12	213							777774000	KEP140	DCI	777774000		83450		
1	12	214							777774000	KEP141	DCI	777774000		83460		
1	12	215							777774000	KEP142	DCI	777774000		83470		
1	12	216							777774000	KEP143	DCI	777774000		83480		

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 162)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NO
1	12	217	77774000	KEM144	OCI	77774000									83490	
1	12	220	777754000	KEM145	OCI	777754000									83500	
1	12	221	777734000	KEM146	OCI	777734000									83510	
1	12	222	777674000	KEM147	OCI	777674000									83520	
1	12	223	777574000	KEM148	OCI	777574000									83530	
1	12	224	777374000	KEM149	OCI	777374000									83540	
1	12	225	776774000	KEM150	OCI	776774000									83550	
1	12	226	775774000	KEM151	OCI	775774000									83560	
1	12	227	77774000	KEM152	OCI	77774000									83570	
1	12	230	77774000	KEM153	OCI	77774000									83580	
1	12	231	77774000	KEM154	OCI	77774000									83590	
1	12	232	77774000	KEM155	OCI	77774000									83600	
1	12	233	77774000	KEM156	OCI	77774000									83610	
1	12	234	77774000	KEM157	OCI	77774000									83620	
1	12	235	77774000	KEM158	OCI	77774000									83630	
1	12	236	773774000	KEM159	OCI	773774000									83640	
1	12	237	767774000	KEM160	OCI	767774000									83650	
1	12	240	757774000	KEM161	OCI	757774000									83660	
1	12	241	737774000	KEM162	OCI	737774000									83670	
1	12	242	677774000	KEM163	OCI	677774000									83680	
1	12	243	577774000	KEM164	OCI	577774000									83690	
1	12	244	377774000	KEM165	OCI	377774000									83700	
1	12	245	77774000	KEM166	OCI	77774000									83710	
1	12	246	77774000	KEM167	OCI	77774000									83720	
1	12	247	77774000	KEM168	OCI	77774000									83730	
1	12	250	77774000	KEM169	OCI	77774000									83740	
1	12	251	77774000	KEM170	OCI	77774000									83750	
1	12	252	77774000	KEM171	OCI	77774000									83760	
1	12	253	77774000	KEM172	OCI	77774000									83770	
1	13	5	740177776	K01	OCI	740177776									83780	
1	13	6	177774	K02	OCI	177774									83790	
1	13	7	37600774	K03	OCI	37600774									83800	
1	13	10	777777776	K04	OCI	777777776									83810	
1	13	11	700177776	K05	OCI	700177776									83820	
1	13	12	640177776	K06	OCI	640177776									83830	
1	13	13	540177776	K07	OCI	540177776									83840	
1	13	14	340177776	K08	OCI	340177776									83850	
1	13	15	740177774	K09	OCI	740177774									83860	
1	13	16	740177776	K010	OCI	740177776									83870	
1	13	17	740177776	K011	OCI	740177776									83880	
1	13	20	740177772	K012	OCI	740177772									83890	
1	13	21	740177766	K013	OCI	740177766									83900	
1	13	22	740177756	K014	OCI	740177756									83910	
1	13	23	740177736	K015	OCI	740177736									83920	
1	13	24	740177676	K016	OCI	740177676									83930	
1	13	25	740177576	K017	OCI	740177576									83940	
1	13	26	740177376	K018	OCI	740177376									83950	
1	13	27	740177776	K019	OCI	740177776									83960	
1	13	30	740177776	K020	OCI	740177776									83970	
1	13	31	740177776	K021	OCI	740177776									83980	
1	13	32	740177776	K022	OCI	740177776									83990	
1	13	33	740177776	K023	OCI	740177776									84000	
1	13	34	740177776	K024	OCI	740177776									84010	
1	13	35	740177776	K025	OCI	740177776									84020	
1	13	36	740176776	K026	OCI	740176776									84030	
1	13	37	740175776	K027	OCI	740175776									84040	
1	13			K027	OCI										84050	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 163)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT VAL	LHS	OPC	VARIABLE	COMMENT	SEC NO
1	13							40	740173776	KD28	OC1	740173776		84060
1	13							41	740167776	KD29	OC1	740167776		84070
1	13							42	740157776	KD30	OC1	740157776		84080
1	13							43	740137776	KD31	OC1	740137776		84090
1	13							44	740077776	KD32	OC1	740077776		84100
1	13							45	740177776	KD33	OC1	740177776		84110
1	13							46	740177776	KD34	OC1	740177776		84120
1	13							47	740177776	KD35	OC1	740177776		84130
1	13							51	740177776	KD37	OC1	740177776		84140
1	13							52	740177776	KD38	OC1	740177776		84150
1	13							53	740177776	KD39	OC1	740177776		84160
1	13							54	740377776	KD40	OC1	740377776		84170
1	13							55	740577776	KD41	OC1	740577776		84180
1	13							56	741177776	KD42	OC1	741177776		84190
1	13							57	742177776	KD43	OC1	742177776		84200
1	13							60	744177776	KD44	OC1	744177776		84210
1	13							61	750177776	KD45	OC1	750177776		84220
1	13							62	760177776	KD46	OC1	760177776		84230
1	13							63	401777776	KD47	OC1	040177776		84240
1	13							64	100177776	KD48	OC1	100177776		84250
1	13							65	200177776	KD49	OC1	200177776		84260
1	13							66	400177776	KD50	OC1	400177776		84270
1	13							70	177776	KD52	OC1	000177776		84280
1	13							71	177776	KD53	OC1	000177776		84300
1	13							72	177770	KD54	OC1	000177770		84310
1	13							73	177764	KD55	OC1	000177764		84320
1	13							74	177754	KD56	OC1	000177754		84330
1	13							75	177734	KD57	OC1	000177734		84340
1	13							76	177674	KD58	OC1	000177674		84350
1	13							77	177574	KD59	OC1	000177574		84360
1	13							100	177374	KD60	OC1	000177374		84370
1	13							101	177774	KD61	OC1	000177774		84380
1	13							102	177774	KD62	OC1	000177774		84390
1	13							103	177774	KD63	OC1	000177774		84400
1	13							104	177774	KD64	OC1	000177774		84410
1	13							105	177774	KD65	OC1	000177774		84420
1	13							106	177774	KD66	OC1	000177774		84430
1	13							107	177774	KD67	OC1	000177774		84440
1	13							110	176774	KD68	OC1	000176774		84450
1	13							111	175774	KD69	OC1	000175774		84460
1	13							112	173774	KD70	OC1	000173774		84470
1	13							113	167774	KD71	OC1	000167774		84480
1	13							114	157774	KD72	OC1	000157774		84490
1	13							115	137774	KD73	OC1	000137774		84500
1	13							116	77774	KD74	OC1	000077774		84510
1	13							117	177774	KD75	OC1	000177774		84520
1	13							120	177774	KD76	OC1	000177774		84530
1	13							121	177774	KD77	OC1	000177774		84540
1	13							122	177774	KD78	OC1	000177774		84550
1	13							123	177774	KD79	OC1	000177774		84560
1	13							124	177774	KD80	OC1	000177774		84570
1	13							125	177774	KD81	OC1	000177774		84580
1	13							126	377774	KD82	OC1	000377774		84590
1	13							127	577774	KD83	OC1	000577774		84600
1	13							130	1177774	KD84	OC1	001177774		84620

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 164)

IM	IS	S	LUC	UP	DM	US	9	ADR	OCT VAL	LHS	OPC	VARIABLE	COMMENT	SEQ NC
1	13	131						2177774	K085	OCI	00217774		84630	
1	13	132					4177774	K086	OCI	00417774			84640	
1	13	133					1017774	K087	OCI	01017774			84650	
1	13	134					2017774	K088	OCI	02017774			84660	
1	13	135					7760074	K089	OCI	07760074			84670	
1	13	136					13760074	K090	OCI	13760074			84680	
1	13	137					23760074	K091	OCI	23760074			84690	
1	13	140					43760074	K092	OCI	43760074			84700	
1	13	141					3760076	K093	OCI	03760076			84710	
1	13	142					3760074	K094	OCI	03760074			84720	
1	13	143					3760074	K095	OCI	03760074			84730	
1	13	144					3760074	K096	OCI	03760074			84740	
1	13	145					3760076	K097	OCI	03760076			84750	
1	13	146					37600754	K098	OCI	037600754			84760	
1	13	147					37600734	K099	OCI	037600734			84770	
1	13	150					37600674	K100	OCI	037600674			84780	
1	13	151					37600374	K101	OCI	037600374			84790	
1	13	152					37600374	K102	OCI	037600374			84800	
1	13	153					37600774	K103	OCI	037600774			84810	
1	13	154					37600774	K104	OCI	037600774			84820	
1	13	155					37600774	K105	OCI	037600774			84830	
1	13	156					37600774	K106	OCI	037600774			84840	
1	13	157					37600774	K107	OCI	037600774			84850	
1	13	160					37600774	K108	OCI	037600774			84860	
1	13	161					37600774	K109	OCI	037600774			84870	
1	13	162					37601774	K110	OCI	037601774			84880	
1	13	163					37602774	K111	OCI	037602774			84890	
1	13	164					37604774	K112	OCI	037604774			84900	
1	13	165					37610774	K113	OCI	037610774			84910	
1	13	166					37620774	K114	OCI	037620774			84920	
1	13	167					37640774	K115	OCI	037640774			84930	
1	13	170					37700774	K116	OCI	037700774			84940	
1	13	171					37600774	K117	OCI	037600774			84950	
1	13	172					37600774	K118	OCI	037600774			84960	
1	13	173					37600774	K119	OCI	037600774			84970	
1	13	174					37600774	K120	OCI	037600774			84980	
1	13	175					37600774	K121	OCI	037600774			84990	
1	13	176					37600774	K122	OCI	037600774			85000	
1	13	177					37600774	K123	OCI	037600774			85010	
1	13	201					37200774	K124	OCI	037200774			85020	
1	13	202					36600774	K125	OCI	036600774			85030	
1	13	203					36600774	K126	OCI	036600774			85040	
1	13	204					36600774	K127	OCI	036600774			85050	
1	13	205					27600774	K128	OCI	027600774			85060	
1	13	206					17600774	K129	OCI	017600774			85070	
1	13	207					73777776	K130	OCI	07377776			85080	
1	13	210					67777776	K131	OCI	06777776			85090	
1	13	211					57777776	K132	OCI	05777776			85100	
1	13	212					77777776	K133	OCI	07777776			85110	
1	13	213					77777776	K134	OCI	07777776			85120	
1	13	214					77777776	K135	OCI	07777776			85130	
1	13	215					77777776	K136	OCI	07777776			85140	
1	13	215					77777776	K137	OCI	07777776			85150	
1	13	216					77777776	K138	OCI	07777776			85160	
1	13	217					77777776	K139	OCI	07777776			85170	
1	13	220					77777776	K140	OCI	07777776			85180	
1	13	221					77777776	K141	OCI	07777776			85190	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 165)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	1	30	17	1	10	1	101	77777776	K0142	OCT	77777776			85200	
1	6	1	30	17	1	10	1	067	777777576	K0143	OCT	777777576			85210	
1	6	1	31	14	1	10	1	033	777777376	K0144	UCI	777777376			85220	
1	6	1	32	0	1	10	1	022	777777776	K0145	OCT	777777776			85230	
1	6	1	33	17	1	10	1	020	777777776	K0146	OCT	777777776			85240	
1	6	1	34	13	1	10	1	101	777777776	K0147	OCT	777777776			85250	
1	6	1	35	5	1	10	204		777777776	K0148	OCT	777777776			85260	
1	6	1	36	5	1	10	210		777777776	K0149	OCT	777777776			85270	
1	6	1	37	13	1	10	251		777777776	K0150	OCT	777777776			85280	
1	6	1	40	13	1	10	252		777777776	K0151	OCT	777777776			85290	
1	6	1	41	13	1	10	253		777777776	K0152	OCT	777777776			85300	
1	6	1	42	13	1	10	254		777777776	K0153	OCT	777777776			85310	
1	6	1	43	13	1	10	255		777777776	K0154	OCT	777777776			85320	
1	6	1	44	13	1	10	100		777777776	K0155	OCT	777777776			85330	
1	6	1	45	17	1	10	033		777777776	K0156	OCT	777777776			85340	
1	6	1	46	13	1	10	256		777777776	K0157	OCT	777777776			85350	
1	6	1	47	17	1	10	101		777777776	K0158	OCT	777777776			85360	
1	6	1	50	13	1	10	257		777777776	K0159	OCT	777777776			85370	
1	6	1	51	16	1	6	226		777777776	K0160	OCT	777777776			85380	
1	6	1	52	17	1	6	173		777777776	K0161	OCT	777777776			85390	
1	6	1	53	6	1	6	1045		777777776	K0162	OCT	777777776			85400	
1	6	1	54	13	1	6	1076		777777776	K0163	OCT	777777776			85410	
										K0164	OCT	777777776			85420	
										K0165	OCT	777777776			85430	
										K0166	OCT	777777776			85440	
										K0167	OCT	777777776			85450	
										K0168	OCT	777777776			85460	
										K0169	OCT	777777776			85470	
										K0170	OCT	777777776			85480	
										K0171	OCT	777777776			85490	
										K0172	OCT	777777776			85500	
															85510	
															85520	
															85530	
															85540	
															85550	
															85560	
															85570	
															85580	
															85590	
															85600	
															85610	
															85620	
															85630	
															85640	
															85650	
															85660	
															85670	
															85680	
															85690	
															85700	
															85710	
															85720	
															85730	
															85740	
															85750	
															85760	

ROUTINE 12
CHECK GOD SIMULATION UNDER MANUAL CONTROL
ORG 1,6,1,30,1,10,101
CLA LCR12
TMI PAC1
HOP H2P1
INITIALIZE
GLA ZER0
STC CTR
CIC 204
CIU 210
STO QUAD1
STO QUAD2
STO QUAD3
STO QUAC4
STC MAG
STC STOP
GLA K77
STC PATH
CLA Y1
STO YN
OCT 001C0C000
CDS L*6
GLA KPAF1
AND K*6
STC TEMP

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 166)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	1	55	17	1	6	1	103				CLA	PAF1		85770	
1	6	1	56	6	1	6	1	040				ANC	KX1		85780	
1	6	1	57	15	1	6	1	076				XOR	TEMP		85790	
1	6	1	60	13	1	6	1	103				STU	PAF1		85800	
1	6	1	61	17	1	6	1	110				CLA	PAH1		85810	
1	6	1	62	6	1	6	1	040				ANC	KX1		85820	
1	6	1	63	15	1	6	1	076				XOR	TEMP		85830	
1	6	1	64	13	1	6	1	110				STU	PAH1		85840	
1	6	1	65	17	1	6	1	121				CLA	PAD2		85850	
1	6	1	66	6	1	6	1	040				ANC	KX1		85860	
1	6	1	67	15	1	6	1	076				XOR	TEMP		85870	
1	6	1	70	13	1	6	1	121				STU	PAF2		85880	
1	6	1	71	17	1	6	1	125				CLA	PAF2		85890	
1	6	1	72	6	1	6	1	040				ANC	KX1		85900	
1	6	1	73	15	1	6	1	076				XOR	TEMP		85910	
1	6	1	74	13	1	6	1	125				STU	PAF2		85920	
1	6	1	75	16	1	10	230					CCS	L.10		85930	
1	6	1	76	17	1	10	257					CLA	YN	SELECT PATH YN	85940	
1	6	1	77	5	1	10	007				PAD1	CU	007		85950	
1	6	1	100	17	1	10	260		000000652		PAE1	CLA	=0C00000652	DELAY 35 MSEC.	85960	
1	6	1	101	2	1	10	1.032				SUB	K1	**1		85970	
1	6	1	102	4	1	10	1.101				TNZ	**1			85980	
1	6	1	103	17	1	10	105					LOAD	RATIOTRAN A=XN		85990	
1	6	1	104	5	1	10	017				PAF1	CU	XI		86000	
1	6	1	105	17	1	10	260		000000652		CU	U17			86010	
1	6	1	106	2	1	10	1.032				SUB	K1	=0C00C00652	DELAY 35 MSEC.	86020	
1	6	1	107	4	1	10	1.106				TNZ	**1			86030	
1	6	1	110	17	1	10	105					LOAD	RATIOTRAN B=XN		86040	
1	6	1	111	5	1	10	017				PAH1	CU	XI		86050	
1	6	1	112	17	1	10	256				CU	U17			86060	
1	6	1	113	14	1	10	1.174				CU	U17			86070	
1	6	1	114	5	1	10	114				TMI	PHF2			86080	
											CU	U14		SET SINGLE STEP	86090	
												MANUAL	OPERATION		86100	
												READ	RATIOTRAN		86120	
												SET	SWITCH B3 ON IF TEST IS TO BE REPEATED		86130	
												DEPRESS	ADVANCE		86140	
												TRA	PCM1		86150	
									040000000		PAC2	CU	220	IS REPEAT SWITCH ON	86160	
											ANC	=004CCCC000		YES	86170	
											TNZ	PAE1			86180	
												LOAD	RATIOTRAN=XN		86190	
											PAD2	CU	XI		86200	
											CU	U17		SINGLE STEP	86210	
											CU	U14			86220	
												MANUAL	OPERATION		86230	
												READ	RATIOTRAN		86240	
												SET	SWITCH B3 ON IF TEST IS TO BE REPEATED		86250	
												DEPRESS	ADVANCE		86260	
												TRA	PCM1		86270	
											PAF2	CU	XI	LOAD RATIOTRAN B	86280	
											CU	U17			86290	
									040000000		PAG2	CU	220	IS REPEAT SWITCH ON	86300	
											ANC	=0C400000000			86310	
											TNZ	PAE1		INCREMENT PATH SELECT	86320	
											PAH2	CU	YN		86330	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 167)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	1	133	16	1	10	101					SHR	1		86340	
1	6	1	134	13	1	10	257					STC	YN		86350	
1	6	1	135	17	1	10	256				PAJ2	CLA	PATH		86360	
1	6	1	136	14	1	10	142					TMI	PRA1		86370	
1	6	1	137	17	1	10	101					CLA	Y1		86380	
1	6	1	140	13	1	10	257					STO	YN		86390	
1	6	1	141	10	1	10	154					TRA	PBD1		86400	
1	6	1	142	17	1	10	257				PBA1	CLA	YN	IS PATH TEST COMPLETE	86410	
1	6	1	143	4	1	10	076					TNZ	PAO1		86420	
1	6	1	144	13	1	10	256				PBB1	STO	PATH		86430	
1	6	1	145	17	1	10	1033					CLA	K77		86440	
1	6	1	146	13	1	10	251					STC	QUAD1		86450	
1	6	1	147	17	1	10	101					CLA	Y1	SELECT PATH Y1	86460	
1	6	1	150	5	1	10	007					C10	C07	DELAY 35 MSEC.	86470	
1	6	1	151	17	1	10	260		000000652			CLA	=0000000652		86480	
1	6	1	152	2	1	10	032					SUB	K1		86490	
1	6	1	153	4	1	10	157				PBD1	TNZ	*-1		86500	
1	6	1	154	17	1	10	251					CLA	QUAD1		86510	
1	6	1	155	14	1	10	157					TMI	PBF1		86520	
1	6	1	156	10	1	10	1204					TRA	PBB3		86530	
1	6	1	157	17	1	10	105				PBF1	CLA	X1	QUADRANT 1 TESTS	86540	
1	6	1	160	5	1	10	177					C10	177	LOAD RATIO TRANS-XN	86550	
1	6	1	161	17	1	10	260		000000652			CLA	=0000000652	TRY TO SET MINUS WITH BIT S=0,I=0	86560	
1	6	1	162	2	1	10	032					SUB	K1		86570	
1	6	1	163	4	1	10	162					TNZ	*-1		86580	
1	6	1	164	17	1	10	105					CLA	X1		86590	
1	6	1	165	5	1	10	177					C10	177		86600	
1	6	1	166	17	1	10	020					CLA	ZERO	TRY TO SET MINUS WITH BIT S=0,I=0	86610	
1	6	1	167	13	1	10	251					STO	QUAD1		86620	
1	6	1	170	17	1	10	033					CLA	K77		86640	
1	6	1	171	13	1	10	252					STC	QUAD2		86650	
1	6	1	172	10	1	10	100					TRA	PAE1		86660	
1	6	1	173	17	1	10	105				KPAF1	CLA	X1		86670	
									577777776		CA	OCT	577777776		86680	
									777777776		CB	OCT	777777776		86690	
									377777776		CC	OCT	377777776		86700	
1	6	1	174	17	1	10	102				PBF2	CLA	CA	SELECTS QUAD 2	86710	
1	6	1	175	5	1	10	077					C10	077		86720	
1	6	1	176	5	1	10	114					C10	114	SINGLE STEP	86730	
														MANUAL OPERATION	86740	
														CHECK FOR 10 VRMS ON CORRECT PATH	86750	
														SET SWITCH B3 ON IF TEST IS TO BE REPEATED	86760	
														DEPRESS ADVANCE	86770	
														TRA	PCH1	86780
1	6	1	177	10	1	10	353					C10	220		86790	
1	6	1	200	5	1	10	220					ANC	=0040000000		86800	
1	6	1	201	6	1	10	231					TNZ	PAJ2		86810	
1	6	1	202	4	1	10	135					TRA	PAH2		86820	
1	6	1	203	10	1	10	132		0400000000			CLA	QUAD2		86830	
1	6	1	204	17	1	10	252				PBB3	CLA	QUAD2		86840	
1	6	1	205	14	1	10	244					TMI	PCE1		86850	
1	6	1	206	17	1	10	253					CLA	QUAD3		86860	
1	6	1	207	14	1	10	273					TMI	PCE1		86870	
1	6	1	210	17	1	10	254					CLA	QUAD4		86880	
1	6	1	211	14	1	10	322					TMI	PCR2		86890	
1	6	1	212	17	1	10	255					CLA	MAG		86900	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 168)

IM	IS	S	LCC	OP	UP	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEQ	NO
1	6	1	213	14	1	10	1	215					PBF3		86900	
1	6	1	214	0	1	0	1	022					H2P1		86910	
1	6	1	215	17	1	10	1	261	000000030	PBF3		CLA	=0000000030	RESET COD SINA, SINB	86920	
1	6	1	216	5	1	10	1	223				C1U	623		86930	
1	6	1	217	16	1	6	1	036				CDS	1*6		86940	
1	6	1	220	17	1	6	1	036				ACC	KSI		86950	
1	6	1	221	7	1	6	1	036				STU	PAF1		86960	
1	6	1	222	13	1	6	1	036				CLA	PAF1		86980	
1	6	1	223	17	1	6	1	110				ADC	PAH1		86990	
1	6	1	224	17	1	6	1	036				ADC	KSI		87000	
1	6	1	225	13	1	6	1	110				STC	PAF2		87020	
1	6	1	226	17	1	6	1	121				CLA	PAC2		87030	
1	6	1	227	7	1	6	1	036				ACC	KSI		87040	
1	6	1	230	13	1	6	1	121				STC	PAD2		87050	
1	6	1	231	17	1	6	1	125				CLA	PAF2		87060	
1	6	1	232	7	1	6	1	036				ADC	KSI		87070	
1	6	1	233	13	1	6	1	125				STU	PAF2		87080	
1	6	1	234	16	1	10	1	230				CDS	1*10		87090	
1	6	1	235	17	1	10	1	100				CLA	STOP		87100	
1	6	1	236	17	1	10	1	036				ADC	KSI		87110	
1	6	1	237	13	1	10	1	100	072000000			STU	STOP		87120	
1	6	1	240	2	1	10	1	262				SUP	=0072000000		87130	
1	6	1	241	4	1	10	1	100				TNZ	PAE1		87140	
1	6	1	242	13	1	10	1	255				STU	MAG		87150	
1	6	1	243	10	1	10	1	100				TRA	PAE1		87160	
1	6	1	244	17	1	10	1	104			PCH1	CLA	CC	QUADRANT 2 TESTS	87170	
1	6	1	245	5	1	10	1	117				C1U	C10	LOADS RATIO TRAN=H	87180	
1	6	1	246	5	1	10	1	114				C1U	C10	READ B	87190	
1	6	1	247	10	1	10	1	353				TRA	PAE1		87200	
1	6	1	250	17	1	10	1	104				CLA	CC	LOADS RATIO TRAN=A	87210	
1	6	1	251	5	1	10	1	117				C1U	C10	READ A	87220	
1	6	1	252	5	1	10	1	114				C1U	C10	LOADS RATIO TRAN=A	87230	
1	6	1	253	10	1	10	1	353				TRA	PCH1	RESETS COSA AND COSB	87240	
1	6	1	254	17	1	10	1	240	000000100			CLA	=0000000300		87250	
1	6	1	255	5	1	10	1	223				C1U	623	SETS COSB MINUS	87260	
1	6	1	256	17	1	10	1	102				CLA	CA	LOAD RATIO TRAN=B	87270	
1	6	1	257	5	1	10	1	057				C1U	O57		87280	
1	6	1	260	5	1	10	1	114				C1U	C10		87290	
1	6	1	261	10	1	10	1	353				TRA	PCH1	SETS COSA MINUS	87300	
1	6	1	262	17	1	10	1	102				CLA	CA	LOAD RATIO TRAN=A	87310	
1	6	1	263	5	1	10	1	037				C1U	O37		87320	
1	6	1	264	5	1	10	1	114				C1U	C10		87330	
1	6	1	265	10	1	10	1	353				TRA	PCH1		87340	
1	6	1	266	17	1	10	1	033				CLA	K77		87350	
1	6	1	267	13	1	10	1	253				STC	JUAD3		87360	
1	6	1	270	17	1	10	1	020				CLA	ZERO		87370	
1	6	1	271	13	1	10	1	252				STC	JUAD2		87380	
1	6	1	272	10	1	10	1	350				TRA	PCF1		87390	
1	6	1	273	17	1	10	1	103				CLA	CB	QUADRANT 3 TESTS	87400	
1	6	1	274	5	1	10	1	117				C1U	C10	LOADS RATIO TRAN=B	87410	
1	6	1	275	5	1	10	1	114				C1U	C10	READ B	87420	
1	6	1	276	10	1	10	1	353				TRA	PCH1		87430	
1	6	1	277	17	1	10	1	103			PCE1	CLA	CB	LOADS RATIO TRAN=A	87440	
1	6	1	300	5	1	10	1	117				C1U	C10	READ A	87450	
1	6	1	301	5	1	10	1	114				C1U	C10		87460	
1	6	1	302	10	1	10	1	353				TRA	PCH1	RESETS SINA COSA, SINB COSB	87470	
1	6	1	303	17	1	10	1	263	000000170			CLA	=0000000170		87480	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 169)

IM	IS	S	LOC	OP	DM	DS	9	ADR	OCT	VAL	LMS	OPC	VARIABLE	COMMENT	SEC	NO
1	6	1	304	5	1	10	1	223				CIU	623		87470	
1	6	1	305	17	1	10	1	303				CLA	CB	SET SINA AND COSB MINUS	87480	
1	6	1	306	5	1	10	0	057				CIC	057	LOAD RATIOTRAN=B	87490	
1	6	1	307	5	1	10	1	114				CIU	114		87500	
1	6	1	310	10	1	10	1	353				TRA	PCH1		87510	
1	6	1	311	17	1	10	1	103				CLA	CB	SET SINA AND COSA MINUS	87520	
1	6	1	312	5	1	10	0	037				CIC	037	LOAD RATIOTRAN=A	87530	
1	6	1	313	5	1	10	1	114				CIC	114		87540	
1	6	1	314	10	1	10	1	353				TRA	PCH1		87550	
1	6	1	315	17	1	10	1	033				CLA	K77		87560	
1	6	1	316	13	1	10	1	254				STC	QUAD4		87570	
1	6	1	317	17	1	10	1	020				CLA	ZERO		87580	
1	6	1	320	13	1	10	1	253				STC	QUAD3		87590	
1	6	1	321	10	1	10	1	350				TRA	PCF1		87600	
1	6	1	322	17	1	10	1	102			PCB2	CLA	CA	QUADRANT 4 TESTS	87610	
1	6	1	323	5	1	10	1	117				CIU	117	LOADS RATIOTRAN=B	87620	
1	6	1	324	5	1	10	1	114				CIU	114	READ B	87630	
1	6	1	325	10	1	10	1	353				TRA	PCH1		87640	
1	6	1	326	17	1	10	1	102				CLA	CA		87650	
1	6	1	327	5	1	10	1	117				CIU	117	LOADS RATIOTRAN=A	87660	
1	6	1	330	5	1	10	1	114				CIU	114	READ A	87670	
1	6	1	331	10	1	10	1	353				TRA	PCH1		87680	
1	6	1	332	17	1	10	1	261		000000030		CLA	=0000000030	RESETS SINA AND SINB	87690	
1	6	1	333	5	1	10	1	223				CIC	623		87700	
1	6	1	334	17	1	10	1	104				CLA	CC		87710	
1	6	1	335	5	1	10	0	057				CIC	057	SETS SINB MINUS	87720	
1	6	1	336	5	1	10	1	114				CIU	114	LOADS RATIOTRAN=B	87730	
1	6	1	337	10	1	10	1	353				TRA	PCH1		87740	
1	6	1	340	17	1	10	1	104				CLA	CC		87750	
1	6	1	341	5	1	10	0	037				CIC	037		87760	
1	6	1	342	5	1	10	1	114				CIU	114		87770	
1	6	1	343	10	1	10	1	353				TRA	PCH1		87780	
1	6	1	344	17	1	10	1	033				CLA	K77		87790	
1	6	1	345	13	1	10	2	555				STC	MAG		87800	
1	6	1	346	17	1	10	1	020				CLA	ZERO		87810	
1	6	1	347	13	1	10	1	254				STC	QUAD4		87820	
1	6	1	350	17	1	10	1	263		000000170	PCF1	CLA	=0000000170		87830	
1	6	1	351	5	1	10	1	223				CIC	623		87840	
1	6	1	352	10	1	10	1	204				TRA	PB03		87850	
1	6	1	353	13	1	10	1	376			PCH1	STC	776		87860	
1	6	1	354	17	1	10	1	101				CLA	CTR		87870	
1	6	1	355	7	1	10	1	032				ACC	K1		87880	
1	6	1	356	13	1	10	1	101				STC	CTR		87890	
1	6	1	357	5	1	10	1	204		000000176		CIC	204		87900	
1	6	1	360	6	1	10	1	264				AND	=0000000176		87910	
1	6	1	361	4	1	10	1	364				TNZ	**3		87920	
1	6	1	362	17	1	10	1	032				CLA	K1		87930	
1	6	1	363	5	1	10	1	210				CIU	210		87940	
1	6	1	364	0	1	10	1	376				HOP	776		87950	
1	6	1	364	0	1	10	1	105		177777774	X1	OCT	177777774		87960	
								106		160016		OCT	000160016		87970	
								107		140014		OCT	000140014		87980	
								110		120012		OCT	000120012		87990	
								111		100010		OCT	000100010		88000	
								112		60006		OCT	000060006		88010	
								113		40004		OCT	000040004		88020	
								114		20002		OCT	000020002		88030	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 170)

IM	IS	S	LOC	UP	DM	DS	9	ADR	OCT	VAL	LHS	OPC	VARIABLE	COMMENT	SEC	NC
1	10							115	1600160			OCT	001600160		88040	
1	10							116	1400140			CCF	001400140		88050	
1	10							117	1200120			OCT	001200120		88060	
1	10							120	1000100			OCT	001000100		88070	
1	10							121	600060			CCF	000600060		88080	
1	10							122	400040			OCT	000400040		88090	
1	10							123	200020			OCT	000200020		88100	
1	10							124	1600160			OCT	016001600		88110	
1	10							125	1400140			OCT	014001400		88120	
1	10							126	12001200			OCT	012001200		88130	
1	10							127	10001000			OCT	010001000		88140	
1	10							130	6000600			OCT	006000600		88150	
1	10							131	4000400			OCT	004000400		88160	
1	10							132	2000200			OCT	002000200		88170	
1	10							133	160016000			OCT	160016000		88180	
1	10							134	140014000			OCT	140014000		88190	
1	10							135	120012000			OCT	120012000		88200	
1	10							136	100010000			OCT	100010000		88210	
1	10							137	60006000			OCT	060006000		88220	
1	10							140	40004000			OCT	040004000		88230	
1	10							141	20002000			OCT	020002000		88240	
1	10							142	0			OCT	000000000		88250	
												END			88260	

Figure 7-13. PTC ADAPT Self-Test Program (Sheet 171)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.14.0.142 M10P24	21940
0.14.0.143 M10P25	22060
0.14.0.144 M10P26	22230
0.14.0.145 M10P27	22410
0.14.0.146 M10P28	22550
0.14.0.147 M10P29	22630
0.14.0.114 M10P2	20180
0.14.0.150 M10P30	22800
0.14.0.151 M10P31	22870
0.14.0.152 M10P33	22940
0.14.0.153 M10P34	23050
0.14.0.154 M10P35	23110
0.14.0.155 M10P36	23160
0.14.0.156 M10P37	23220
0.14.0.157 M10P38	23270
0.14.0.160 M10P39	23460
0.14.0.115 M10P3	20230
0.14.0.161 M10P40	23550
0.14.0.162 M10P41	23640
0.14.0.163 M10P42	23730
0.14.0.164 M10P43	23820
0.14.0.165 M10P44	23910
0.14.0.166 M10P45	24000
0.14.0.116 M10P4	20280
0.14.0.117 M10P5	20380
0.14.0.120 M10P6	20450
0.14.0.121 M10P7	20520
0.14.0.122 M10P8	20590
0.14.0.123 M10P9	20660
0.14.0.201 M10P10	25470
0.14.0.202 M10P11	25560
0.14.0.203 M10P12	25660
0.14.0.204 M10P13	25760
0.14.0.205 M10P14	25860
0.14.0.207 M10P18	26030
0.14.0.210 M10P19	26080
0.14.0.170 M10P1	24090
0.14.0.211 M10P20	26140
0.14.0.212 M10P21	26210
0.14.0.213 M10P22	26280
0.14.0.214 M10P23	26350
0.14.0.215 M10P24	26420
0.14.0.216 M10P25	26490
0.14.0.217 M10P26	26560
0.14.0.220 M10P27	26630
0.14.0.171 M10P2	24680
0.14.0.172 M10P3	24720
0.14.0.173 M10P4	24790
0.14.0.174 M10P5	24880
0.14.0.175 M10P6	25090
0.14.0.176 M10P7	25180
0.14.0.177 M10P8	25270
0.14.0.200 M10P9	25360
0.15.0.017 M12P1	27770
0.15.0.020 M12P2	27790
	24620
	30950

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 2)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.15.0.000 H12P3	28240
0.15.0.021 H12P4	27810
0.15.0.001 H12P5	28390
0.15.0.022 H12P6	27830
0.15.0.002 H13P1	28540
0.15.0.023 H13P2	27850
0.15.0.003 H13P3	28690
0.15.0.024 H13P4	27870
0.15.0.004 H13P5	28840
0.15.0.025 H13P6	27890
0.15.0.005 H14P1	28990
0.15.0.026 H14P2	27910
0.15.0.006 H14P3	29140
0.15.0.027 H14P4	27930
0.15.0.007 H14P5	29290
0.15.0.030 H14P6	27950
0.15.0.010 H15P1	29440
0.15.0.031 H15P2	27970
0.15.0.011 H15P3	29590
0.15.0.032 H15P4	27990
0.15.0.012 H15P5	29740
0.15.0.033 H15P6	28010
0.15.0.013 H16P1	29890
0.15.0.034 H16P2	28030
0.15.0.014 H16P3	30040
0.15.0.035 H16P4	28050
0.15.0.015 H16P5	30190
0.15.0.036 H16P6	28070
0.15.0.016 H17P1	
0.17.0.017 H17P2	
0.12.0.131 H20P2	31790
0.12.0.132 H20P3	31810
0.12.0.133 H20P4	32070
0.12.0.134 H21P1	32120
0.12.0.135 H21P2	32180
0.12.0.136 H21P3	32270
0.12.0.137 H22P4	32690
0.12.0.140 H23P1	32720
0.12.0.141 H23P2	32820
0.12.0.142 H23P3	32880
0.12.0.143 H23P5	32740
0.12.0.144 H24P1	33000
0.12.0.145 H24P3	33100
0.12.0.146 H24P4	33160
0.12.0.147 H24P5	33220
0.12.0.150 H25P1	33340
0.12.0.151 H25P2	33520
0.12.0.152 H25P3	33650
0.12.0.153 H26P1	33710
0.12.0.154 H27P1	33950
0.12.0.155 H27P2	34040
0.12.0.156 H27P3	34090
0.12.0.157 H28P1	34160
0.12.0.160 H28P2	34220
0.12.0.161 H29P2	35900
0.15.0.055 H29P3	36170
0.15.0.000 H12P3	28240
0.15.0.021 H12P4	27810
0.15.0.001 H12P5	28390
0.15.0.022 H12P6	27830
0.15.0.002 H13P1	28540
0.15.0.023 H13P2	27850
0.15.0.003 H13P3	28690
0.15.0.024 H13P4	27870
0.15.0.004 H13P5	28840
0.15.0.025 H13P6	27890
0.15.0.005 H14P1	28990
0.15.0.026 H14P2	27910
0.15.0.006 H14P3	29140
0.15.0.027 H14P4	27930
0.15.0.007 H14P5	29290
0.15.0.030 H14P6	27950
0.15.0.010 H15P1	29440
0.15.0.031 H15P2	27970
0.15.0.011 H15P3	29590
0.15.0.032 H15P4	27990
0.15.0.012 H15P5	29740
0.15.0.033 H15P6	28010
0.15.0.013 H16P1	29890
0.15.0.034 H16P2	28030
0.15.0.014 H16P3	30040
0.15.0.035 H16P4	28050
0.15.0.015 H16P5	30190
0.15.0.036 H16P6	28070
0.15.0.016 H17P1	
0.17.0.017 H17P2	
0.12.0.131 H20P2	31790
0.12.0.132 H20P3	31810
0.12.0.133 H20P4	32070
0.12.0.134 H21P1	32120
0.12.0.135 H21P2	32180
0.12.0.136 H21P3	32270
0.12.0.137 H22P4	32690
0.12.0.140 H23P1	32720
0.12.0.141 H23P2	32820
0.12.0.142 H23P3	32880
0.12.0.143 H23P5	32740
0.12.0.144 H24P1	33000
0.12.0.145 H24P3	33100
0.12.0.146 H24P4	33160
0.12.0.147 H24P5	33220
0.12.0.150 H25P1	33340
0.12.0.151 H25P2	33520
0.12.0.152 H25P3	33650
0.12.0.153 H26P1	33710
0.12.0.154 H27P1	33950
0.12.0.155 H27P2	34040
0.12.0.156 H27P3	34090
0.12.0.157 H28P1	34160
0.12.0.160 H28P2	34220
0.12.0.161 H29P2	35900
0.15.0.055 H29P3	36170
0.15.0.000 H12P3	28240
0.15.0.021 H12P4	27810
0.15.0.001 H12P5	28390
0.15.0.022 H12P6	27830
0.15.0.002 H13P1	28540
0.15.0.023 H13P2	27850
0.15.0.003 H13P3	28690
0.15.0.024 H13P4	27870
0.15.0.004 H13P5	28840
0.15.0.025 H13P6	27890
0.15.0.005 H14P1	28990
0.15.0.026 H14P2	27910
0.15.0.006 H14P3	29140
0.15.0.027 H14P4	27930
0.15.0.007 H14P5	29290
0.15.0.030 H14P6	27950
0.15.0.010 H15P1	29440
0.15.0.031 H15P2	27970
0.15.0.011 H15P3	29590
0.15.0.032 H15P4	27990
0.15.0.012 H15P5	29740
0.15.0.033 H15P6	28010
0.15.0.013 H16P1	29890
0.15.0.034 H16P2	28030
0.15.0.014 H16P3	30040
0.15.0.035 H16P4	28050
0.15.0.015 H16P5	30190
0.15.0.036 H16P6	28070
0.15.0.016 H17P1	
0.17.0.017 H17P2	
0.12.0.131 H20P2	31790
0.12.0.132 H20P3	31810
0.12.0.133 H20P4	32070
0.12.0.134 H21P1	32120
0.12.0.135 H21P2	32180
0.12.0.136 H21P3	32270
0.12.0.137 H22P4	32690
0.12.0.140 H23P1	32720
0.12.0.141 H23P2	32820
0.12.0.142 H23P3	32880
0.12.0.143 H23P5	32740
0.12.0.144 H24P1	33000
0.12.0.145 H24P3	33100
0.12.0.146 H24P4	33160
0.12.0.147 H24P5	33220
0.12.0.150 H25P1	33340
0.12.0.151 H25P2	33520
0.12.0.152 H25P3	33650
0.12.0.153 H26P1	33710
0.12.0.154 H27P1	33950
0.12.0.155 H27P2	34040
0.12.0.156 H27P3	34090
0.12.0.157 H28P1	34160
0.12.0.160 H28P2	34220
0.12.0.161 H29P2	35900
0.15.0.055 H29P3	36170

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 3)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.15.0.056 H29P4	35990	36270								
0.17.0.022 H2P1	49770	53010								86910
0.15.0.057 H30P1	36290	36360								85560
0.17.0.321 H30P2A	36500									82040
0.15.0.060 H30P2	36380									79580
0.15.0.061 H31P3	36580									78890
0.15.0.062 H31P4	36560									74910
0.15.0.041 H32P1	36850									36480
0.15.0.063 H32P2	36910									
0.15.0.064 H32P3	36990									
0.15.0.065 H32P4	37080									
0.15.0.066 H33P1	37170									
0.15.0.067 H33P2	37250									
0.15.0.070 H33P3	37320									
0.15.0.071 H34P4	37590									
0.15.0.072 H34P5	37570									
0.15.0.073 H34P6	37930									
0.15.0.074 H34P7	38000									
0.15.0.075 H34P8	38080									
0.15.0.076 H34P9	38170									
0.15.0.053 H36P1	38400									
0.15.0.052 H36P2	38370									
0.15.0.077 H37P4	38870									
0.15.0.100 H37P5	38850									
0.15.0.101 H38P4	39360									
0.15.0.102 H39P1	39470									
0.15.0.103 H39P2	39560									
0.15.0.104 H39P3	39640									
0.15.0.105 H39P4	39690									
0.15.0.106 H40P1	39780									
0.15.0.107 H40P2	39910									
0.15.0.110 H40P3	39990									
0.15.0.111 H41P1	40070									
0.15.0.112 H41P2	40140									
0.15.0.113 H41P3	40310									
0.15.0.114 H42P1	40380									
0.15.0.115 H42P2	40500									
0.17.0.024 H43P2	50390									
0.15.0.264 H45P2	42520									
0.15.0.275 H47P1	43460									
0.15.0.276 H47P2	43490									
0.15.0.265 H50P1	42540									
0.13.0.000 H5P3	5150									
0.13.0.001 H5P4	5170									5230
0.13.0.002 H5P5	5250									5310
0.13.0.003 H5P6	5330									5400
0.13.0.004 H5P7	5420									
0.13.0.016 H6P10	6320									6380
0.13.0.017 H6P11	6400									6480
0.13.0.020 H6P12	6500									6560
0.13.0.021 H6P13	6580									6660
0.13.0.022 H6P14	6680									6740
0.13.0.023 H6P15	6760									6820
0.13.0.024 H6P16	6840									6910
0.13.0.025 H6P17	6930									6990
0.13.0.026 H6P18	7010									7080

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 4)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.13.0.027 H6P19	7100	7160
0.13.0.005 H6P1		
0.13.C.030 H6P20	7180	7240
0.13.C.031 H6P21	7260	7330
0.13.0.032 H6P22	7350	7410
0.13.0.033 H6P23	7430	7490
0.13.0.006 H6P2	5580	
0.13.0.007 H6P3	5600	5730
0.13.0.010 H6P4	5750	5840
0.13.C.011 H6P5	5860	5950
0.13.0.012 H6P6	5970	6040
0.13.C.013 H6P7	6060	6120
0.13.0.014 H6P8	6140	6210
0.13.0.015 H6P9	6230	6300
0.13.0.045 H7P10	8260	8330
0.13.0.046 H7P11	8350	8420
0.13.0.047 H7P12	8440	8510
0.13.0.050 H7P13	8530	8600
0.13.0.051 H7P14	8620	8690
0.13.0.052 H7P15	8710	8780
0.13.0.053 H7P16	8800	8860
0.13.0.054 H7P17	8880	8940
0.13.0.055 H7P18	8960	9030
0.13.0.056 H7P19	9050	9140
0.13.0.034 H7P1	7510	7580
0.13.0.057 H7P20	9160	9220
0.13.0.060 H7P21	9240	9300
0.13.C.061 H7P22	9320	9390
0.13.0.062 H7P23	9410	9500
0.13.0.063 H7P24	9520	9590
0.13.0.064 H7P25	9610	9680
0.13.0.065 H7P26	9700	9776
0.13.0.066 H7P27	9790	9860
0.13.0.067 H7P28	9880	9940
0.13.C.070 H7P29	9960	10030
0.13.0.035 H7P2	7600	7660
0.13.0.071 H7P30	10050	10120
0.13.0.072 H7P31	10140	10210
0.13.0.073 H7P32	10230	10300
0.13.0.074 H7P33	10320	10390
0.13.0.075 H7P34	10410	10480
0.13.0.076 H7P35	10500	10570
0.13.0.077 H7P36	10590	10660
0.13.C.100 H7P37	10680	10740
0.13.0.101 H7P38	10760	10820
0.13.0.102 H7P39	10840	10910
0.13.0.036 H7P3	7680	7740
0.13.0.103 H7P40	10930	11000
0.13.0.104 H7P41	11020	11090
0.13.0.105 H7P42	11110	11220
0.13.0.106 H7P43	11240	11310
0.13.0.107 H7P44	11330	11400
0.13.0.110 H7P45	11420	11480
0.13.0.111 H7P46	11500	11560
0.13.0.112 H7P47	11580	11650
0.13.0.113 H7P48	11670	11740

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 5)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.13.0.114 H7P49	11760	11830
0.13.0.037 H7P4	7760	7820
0.13.0.115 H7P50	11850	11920
0.13.0.116 H7P51	11940	12010
0.13.0.117 H7P52	12030	12100
0.13.0.120 H7P53	12120	12210
0.13.0.122 H7P548	12560	
0.13.0.121 H7P54	12230	
0.13.0.140 H7P558	12640	12540
1.17.0.101 H7P55	12680	
0.13.0.040 H7P5	7840	7900
0.13.0.041 H7P6	7920	7980
0.13.0.042 H7P7	8000	8080
0.13.0.043 H7P8	8100	8160
0.13.0.044 H7P9	8180	8240
0.17.0.025 H8P1A	12610	12700
0.13.0.123 H8P1	12840	
0.13.0.124 H8P2	12860	12930
0.13.0.125 H8P3	12950	13020
0.13.0.126 H8P4	13040	13110
0.13.0.127 H8P5	13130	13200
0.13.0.130 H8P6	13220	13290
1.17.0.100 H95P1A	12750	
0.17.0.026 H95P1	5210	5290
0.17.0.026 H95P1	34430	38920
0.17.0.027 H95P7	56740	74500
0.14.0.007 H9P10	15330	
0.14.0.010 H9P11	15400	
0.14.0.011 H9P12	15470	
0.14.0.012 H9P13	15520	
0.14.0.013 H9P14	15590	
0.14.0.014 H9P15	15660	
0.14.0.015 H9P16	15730	
0.14.0.016 H9P17	15800	
0.14.0.017 H9P18	15870	
0.14.0.020 H9P19	15940	
0.13.0.141 H9P1	13310	13490
0.14.0.021 H9P20	16010	
0.14.0.022 H9P21	16080	
0.14.0.023 H9P22	16150	
0.14.0.024 H9P23	16220	
0.14.0.025 H9P24	16290	
0.14.0.026 H9P25	16360	
0.14.0.031 H9P26	16430	
0.14.0.032 H9P27	16500	
0.14.0.033 H9P28	16570	
0.14.0.034 H9P29	16640	
0.14.0.000 H9P2	14710	
0.14.0.035 H9P30	16710	
0.14.0.036 H9P31	16780	
0.14.0.037 H9P32	16850	
0.14.0.040 H9P33	16920	
0.14.0.041 H9P34	16990	
0.14.0.042 H9P35	17060	
0.14.0.043 H9P36	17130	
0.14.0.044 H9P37	17200	

30980

27150

25060

19880

12650

5470

5380

42930

13080

13070

12780

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 6)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1,11,0,042 HJLKI	65590
1,11,0,040 HJMBI	65220
1,11,0,050 HJMB2	66270
1,11,0,052 HJMB3	66480
1,11,0,054 HJMB4	66670
1,11,0,053 HJMJ2	66610
1,11,0,055 HJMJ3	66800
1,11,0,051 HJMK1	66420
1,11,0,047 HJNB1	66100
1,11,0,057 HJNH2	67100
1,11,0,061 HJNB3	67310
1,11,0,063 HJNB4	67500
1,11,0,062 HJNJ2	67440
1,11,0,064 HJNJ3	67630
1,11,0,060 HJNK1	67250
1,11,0,056 HJPB1	66900
1,11,0,066 HJPB2	67930
1,11,0,070 HJPB3	68140
1,11,0,072 HJPB4	68330
1,11,0,071 HJPJ2	68270
1,11,0,073 HJPJ3	68460
1,11,0,067 HJPK1	68080
1,11,0,065 HJOB1	67740
1,11,0,075 HJOB2	68740
1,11,0,077 HJOB3	68950
1,11,0,101 HJOB4	69140
1,11,0,100 HJOJ2	69080
1,11,0,102 HJOJ3	69270
1,11,0,076 HJOK1	68890
1,11,0,074 HJRB1	68550
1,11,0,104 HJRB2	69560
1,11,0,106 HJRB3	69770
1,11,0,110 HJRB4	69960
1,11,0,107 HJRJ2	69900
1,11,0,111 HJRJ3	70090
1,11,0,105 HJSB1	69710
1,11,0,103 HJSB2	69370
1,11,0,113 HJSB3	70420
1,11,0,115 HJSB4	70630
1,11,0,117 HJSB5	70820
1,11,0,116 HJSJ2	70760
1,11,0,120 HJSJ3	70950
1,11,0,114 HJSK1	70570
1,11,0,112 HJTB1	70220
1,11,0,121 HJTB2	71220
1,11,0,123 HJTB3	71430
1,11,0,125 HJTB4	71620
1,11,0,124 HJTJ2	71560
1,11,0,126 HJTJ3	71750
1,11,0,122 HJTK1	71370
1,11,0,127 HJUB1	71040
1,11,0,130 HJV81A	71900
1,11,0,131 HJV81	72920
1,10,0,034 HJME3	54950
1,10,0,033 HJMK1	54850
1,11,0,132 HJV81	72960
	71860

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 8)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.16.0.370 HP10	4140
0.16.0.371 HP11	4180
0.16.0.372 HP12	4220
0.16.0.373 HP13	4260
0.16.0.374 HP14	4300
0.16.0.376 HP15	4340
0.16.0.377 HP16	4380
1.00.0.001 HP17	4430
1.01.0.002 HP18	4470
1.02.0.003 HP19	4510
1.03.0.131 HP1	3780
1.03.0.004 HP20	4550
1.04.0.005 HP21	4590
1.05.0.006 HP22	4630
1.06.0.007 HP23	4670
1.07.0.017 HP24	4710
1.10.0.027 HP25	4750
1.11.0.037 HP26	4790
1.12.0.377 HP27	4830
1.13.0.377 HP28	4870
1.14.0.377 HP29	4910
0.01.0.001 HP2	3820
1.15.0.177 HP30	4950
1.16.0.100 HP31	4990
1.17.0.077 HP32	5030
0.02.0.001 HP3	3860
0.03.0.001 HP4	3900
0.04.0.001 HP5	3940
0.05.0.010 HP6	3980
0.16.0.365 HP7	4020
0.16.0.366 HP8	4060
0.16.0.367 HP9	4100
0.17.0.103 HRTRN	42090
0.17.0.075 INTIND	2570
1.00.0.121 JAA2	
1.00.0.010 JAB1	
1.00.0.015 JAC1	
1.00.0.133 JAC2A	
1.00.0.130 JAC2	
1.00.0.255 JAC3	
1.00.1.030 JAC4	
1.00.1.067 JAC5	
1.00.0.134 JAD2	
1.00.0.264 JAD3	
1.00.1.034 JAD4	
1.00.1.073 JAD5	
1.00.0.301 JAE3	
1.00.1.040 JAE4	
1.00.1.077 JAE5	
1.00.0.055 JAF1	
1.00.0.150 JAF2	
1.00.0.306 JAF3	
1.00.1.044 JAF4	
1.00.1.103 JAF5	
1.00.0.064 JAG1	
1.00.0.233 JAG2	
	53340
	55980
	53700
	42330
	31080
	51180
	51370

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 9)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.00,0.313 JAG3	55370								
1.00,1.047 JAG4									
1.00,1.107 JAG5									
1.00,0.071 JAH1									
1.00,0.236 JAH2									
1.00,0.320 JAH3									
1.00,1.053 JAH4									
1.00,0.102 JAJ1									
1.00,0.243 JAJ2									
1.00,0.325 JAJ3									
1.00,1.057 JAJ4									
1.00,1.117 JAJ5A									
1.00,1.124 JAJ5B									
1.00,1.116 JAJ5	53820	53880	53980	54140	54280	54370	54440	54910	
1.00,1.116 JAJ5	55030	55510	56940						
1.00,0.110 JAK1									
1.00,0.250 JAK2									
1.00,1.010 JAK3	55840								
1.00,1.063 JAK4									
1.00,1.131 J8A1	56630								
1.00,1.220 J8A2	56620								
1.00,1.135 J8B1									
1.00,1.224 J8B2									
1.00,0.100 J8B3									
1.00,0.125 J8B4									
1.00,0.137 J8B5									
1.00,1.141 J8C1									
1.00,1.230 J8C2									
1.00,0.103 J8C3									
1.00,0.130 J8C4									
1.00,0.142 J8C5									
1.00,1.155 J8D1									
1.00,1.234 J8D2									
1.00,0.106 J8D3									
1.00,0.145 J8D5									
1.00,1.161 J8E1									
1.00,1.240 J8E2									
1.00,0.111 J8E3									
1.00,0.150 J8E5									
1.00,1.165 J8F1									
1.00,1.244 J8F2									
1.00,0.114 J8F3									
1.00,0.153 J8F5									
1.00,1.210 J8G1	57100								
1.00,1.250 J8G2									
1.00,0.117 J8G3									
1.00,0.133 J8G4									
1.00,0.156 J8G5									
1.00,1.214 J8H1									
1.00,1.254 J8H2									
1.00,0.122 J8H3									
1.00,0.161 J8H5									
1.00,1.261 J8J2									
1.00,1.267 J8K2									
1.00,0.070 J8M2									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 10)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.06.0.164 JCB1
 1.06.0.176 JCB2
 1.06.0.211 JCB4
 1.06.0.254 JCB5
 1.06.0.167 JCC1
 1.06.0.201 JCC2
 1.06.0.257 JCC5
 1.06.0.204 JCD2
 1.06.0.262 JCD5
 1.06.0.207 JCE2
 1.06.0.235 JCE4
 1.06.0.265 JCF5
 1.06.0.212 JCF2
 1.06.0.240 JCF4
 1.06.0.215 JCG2
 1.06.0.243 JCG4
 1.06.0.172 JCH1
 1.06.0.220 JCH7
 1.06.0.246 JCH4
 1.06.0.223 JCJ2
 1.06.0.251 JCJ4
 1.06.0.226 JCK2
 1.01.0.012 JDB1
 1.01.0.035 JDB2
 1.01.0.051 JDB3
 1.01.0.074 JDB4
 1.01.0.040 JDC2
 1.01.0.077 JDC4
 1.01.0.043 JDD2
 1.01.0.102 JDD4
 1.01.0.016 JDE1
 1.01.0.046 JDE2
 1.01.0.055 JDE3
 1.01.0.105 JDE4
 1.01.0.021 JDF1
 1.01.0.060 JDF1
 1.01.0.024 JDG1
 1.01.0.063 JDG3
 1.01.0.027 JDH1
 1.01.0.066 JDH3
 1.01.0.032 JDJ1
 1.01.0.071 JDJ3
 1.01.0.133 JEA2
 1.01.0.110 JEB1
 1.01.0.135 JEB7
 1.01.0.161 JEB3
 1.01.0.205 JER4
 1.01.0.236 JEB5
 1.00.1.301 JEC1A
 1.01.0.113 JEC1
 1.01.0.137 JEC2
 1.01.0.206 JEC4
 1.01.0.242 JEC5
 1.01.0.167 JED3
 1.01.0.212 JED4
 1.01.0.246 JED5

60000

57730

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 11)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.01, 1.022 JRLA	64200								
1.02, C, 1.155 JRI1	61020								
1.02, O, 2.17 JJI1	64270	64750							
1.02, O, 2.27 JRI1	65160								
1.02, C, 2.63 JRI1									
1.02, 1.014 JRI1									
1.02, 1.047 JRI1									
1.02, 1.132 JRI1									
1.02, 1.072 JRI1	65610	67800	65990	66440	66630	66820	67270	67460	67650
1.02, 1.113 JRI1									
1.02, 1.071 JRI1									
1.02, 1.117 JRI1									
1.02, 1.131 JRI1	65500	65640	65710	65830	65900	66020	66330	66470	66540
1.02, 1.131 JRI1	66660	66730	66850	67100	67300	67370	67490	67560	67680
1.02, 1.131 JRI1									
1.02, 1.046 JRI1	66050								
1.02, 1.133 JRI1									
1.02, 1.162 JRI1									
1.02, 1.205 JRI1									
1.02, 1.226 JRI1									
1.02, 1.204 JRI1									
1.02, 1.225 JRI1									
1.02, 1.161 JRI1									
1.02, 1.275 JRI1									
1.02, 1.243 JRI1									
1.02, 1.320 JRI1									
1.02, 1.341 JRI1									
1.02, 1.317 JRI1									
1.02, 1.340 JRI1									
1.02, 1.274 JRI1									
1.03, 0.020 JRI1									
1.03, 0.050 JRI1									
1.03, 0.073 JRI1									
1.03, 0.114 JRI1									
1.03, 0.072 JRI1									
1.03, 0.113 JRI1									
1.03, C, 3.55 JRI1	68130	68320	68500	68940	69130	69320	69760	69950	70140
1.03, 0.355 JRI1	70620	70810	70990	71420	71610	71800	71800	71800	71800
1.03, 0.356 JRI1	68100	68290	68480	68910	69100	69290	69730	69920	70110
1.03, 0.356 JRI1	70590	70780	70970	71390	71580	71770			
1.03, 0.047 JRI1									
1.03, 0.130 JRI1									
1.03, 0.161 JRI1									
1.03, 0.204 JRI1									
1.03, 0.225 JRI1									
1.03, 0.203 JRI1									
1.03, 0.224 JRI1									
1.03, 0.160 JRI1									
1.03, 0.242 JRI1									
1.03, 0.273 JRI1									
1.03, 0.316 JRI1									
1.03, C, 3.37 JRI1									
1.03, 0.315 JRI1									
1.03, 0.336 JRI1									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 13)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.03,0.272 JRK1									
1.03,1.020 JSB1	70170								
1.03,1.051 JSR2									
1.03,1.074 JSB3									
1.03,1.115 JSB4									
1.03,1.073 JSJ2									
1.03,1.114 JSJ3									
1.03,1.050 JSK1									
1.03,1.131 JTB1									
1.03,1.162 JTB2									
1.03,1.205 JTB3									
1.03,1.226 JTB4									
1.03,1.204 JTB2									
1.03,1.225 JTB3									
1.03,1.161 JTK1									
1.04,0.066 JUA3									
1.04,0.124 JUA5									
1.04,0.020 JUB1									
1.04,0.074 JUC3									
1.04,0.132 JUC5									
1.04,0.140 JUE3									
1.04,0.140 JUE5									
1.04,0.052 JUG1									
1.04,0.110 JUG3									
1.04,0.146 JUG5									
1.04,0.060 JUI1									
1.04,0.164 JUJ2									
1.04,0.164 JUJ2									
1.04,0.116 JUJ3									
1.04,0.154 JUJ5									
1.04,1.070 JVA3									
1.04,1.126 JVA5									
1.04,1.020 JWB1									
1.04,1.076 JVC3									
1.04,1.134 JVC5									
1.04,1.104 JVE3									
1.04,1.142 JVE5									
1.04,1.054 JVG1									
1.04,1.112 JVG3									
1.04,1.150 JVG5									
1.04,1.062 JVJ1									
1.04,1.243 JVJ2									
1.04,1.120 JVJ3									
1.04,1.156 JVJ5									
1.00,0.171 JWB1									
1.00,0.217 JWB3									
1.00,0.175 JWB1									
1.00,0.227 JWF3									
1.00,0.202 JWF1									
1.00,0.207 JWH1									
1.00,0.215 JWK1									
1.05,0.141 JXA3									
1.05,1.225 JXB2									
1.05,0.147 JXB3									
1.04,1.166 JXC1									
72190	72250	72310	72370	72430	72490	72550	72610	72670	
72730	72790	72840	72880	72940	72990	73050	73110	73170	
72870									
72880	73270	73330	73390	73450	73510	73570	73630	73690	
73750	73810	73870	73930						
54570									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 14)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.17,0.032 K1	2780	32410	34110	36140	36240	36340	36680	37190	37220
0.17,0.032 K1	37300	48560	38580	39030	39110	39440	39510	39670	40170
0.17,0.032 K1	40220	42570	43270	43430	43580	43750	43890	43950	44220
0.17,0.032 K1	44260	44360	44410	44460	45570	45850	45930	46080	46300
0.17,0.032 K1	46450	46600	46840	47580	47920	48990	49440	50150	50220
0.17,0.032 K1	50630	50690	51100	51320	52610	52700	53160	53280	64360
0.17,0.032 K1	64410	64470	64520	64570	64630	64790	64840	64900	64950
0.17,0.032 K1	65000	65060	67190	68020	71310	75190	75400	78290	79360
0.17,0.032 K1	79430	79680	79750	80260	80640	80690	80760	80880	80920
0.17,0.032 K1	80940	80960	80980	81900	81960	85970	86030	86490	86580
0.17,0.032 K1	87880	87930	42730	42770	42860	43370	43530	43670	43700
0.15,0.270 K2	42610	42700	44040	44100	44190	44510			
0.15,0.270 K2	43830	43990							
0.10,0.370 K31P1	42110								
0.10,0.371 K31P2	42160								
0.17,0.035 K324	44290								
0.10,0.372 K34P2	37410								
0.10,0.373 K34P3	37480								
1.11,0.133 K35A	74060	74160	74260	74360					
1.11,0.134 K35H	74090	74190	74290	74390					
0.11,0.344 K35P4	42220								
0.10,1.241 K37P3	42280								
0.04,1.255 K61P3A	47250								
0.17,0.033 K77	13440								
0.17,0.033 K77	69330	31840	49030	5350	54780	66030	66860	67690	68510
0.17,0.033 K77	86440	70150	71000	71810	72850	73010	74590	74780	85680
0.16,1.167 K90P3	52300	86640	87330	87560	87790				
0.05,1.244 K90P4A	52370								
0.16,1.170 K90P5	52790								
0.16,1.171 K90P6	52950								
0.16,0.142 K95P1	49520								
0.16,0.143 K95P2	49570								
0.16,0.144 K95P3	49310								
0.16,0.145 K95P4	49670								
0.16,0.146 K95P5	49720								
0.16,0.147 K97P3	50460								
0.16,1.110 K97P4A	50360								
0.16,0.151 K97P5A	50870								
0.16,0.150 K97P5	50770								
0.05,0.012 KA	46620								
0.05,0.033 KB	47440	47430							
0.05,0.054 KC	47450								
1.13,0.150 KD100									
1.13,0.151 KD101									
1.13,0.152 KD102									
1.13,0.153 KD103									
1.13,0.154 KD104									
1.13,0.155 KD105									
1.13,0.156 KD106									
1.13,0.157 KD107									
1.13,0.160 KD108									
1.13,0.161 KD109									
1.13,0.016 KD10*									
1.13,0.162 KD110									
1.13,0.163 KD111									
1.13,0.164 KD112									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 16)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.13.C.165 KD114
1.13.C.166 KD114
1.13.C.167 KD115
1.13.C.170 KD116
1.13.C.171 KD117
1.13.C.172 KD118
1.13.C.173 KD119
1.13.C.174 KD120
1.13.C.175 KD121
1.13.C.176 KD122
1.13.C.177 KD123
1.13.C.200 KD124
1.13.C.201 KD125
1.13.C.202 KD126
1.13.C.203 KD127
1.13.C.204 KD128
1.13.C.205 KD129
1.13.C.220 KD12
1.13.C.206 KD130
1.13.C.207 KD131
1.13.C.210 KD132
1.13.C.211 KD133
1.13.C.212 KD134
1.13.C.213 KD135
1.13.C.214 KD136
1.13.C.215 KD137
1.13.C.216 KD138
1.13.C.217 KD139
1.13.C.221 KD13
1.13.C.220 KD14C
1.13.C.221 KD141
1.13.C.222 KD142
1.13.C.223 KD143
1.13.C.224 KD144
1.13.C.225 KD145
1.13.C.226 KD146
1.13.C.227 KD147
1.13.C.230 KD148
1.13.C.231 KD149
1.13.C.232 KD14
1.13.C.232 KD15C
1.13.C.233 KD151
1.13.C.234 KD152
1.13.C.235 KD153
1.13.C.236 KD154
1.13.C.237 KD155
1.13.C.240 KD156
1.13.C.241 KD157
1.13.C.242 KD158
1.13.C.243 KD159
1.13.C.223 KD15
1.13.C.244 KD160
1.13.C.245 KD161
1.13.C.246 KD162
1.13.C.247 KD163

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 17)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

- 1.13.0.250 K0164
- 1.13.C.251 K0165
- 1.13.0.252 K0166
- 1.13.0.253 K0167
- 1.13.0.254 K0168
- 1.13.0.255 K0169
- 1.13.0.024 K016
- 1.13.0.256 K017C
- 1.13.0.257 K0171
- 1.13.0.260 K0172
- 1.13.0.025 K017
- 1.13.0.026 K018
- 1.13.0.027 K019
- 1.13.C.005 K01
- 1.13.0.030 K020
- 1.13.0.031 K021
- 1.13.0.032 K022
- 1.13.C.033 K023
- 1.13.0.034 K024
- 1.13.0.035 K025
- 1.13.0.036 K026
- 1.13.0.037 K027
- 1.13.0.040 K028
- 1.13.0.041 K029
- 1.13.0.006 K02
- 1.13.0.042 K030
- 1.13.0.043 K031
- 1.13.0.044 K032
- 1.13.0.045 K033
- 1.13.0.046 K034
- 1.13.0.047 K035
- 1.13.0.050 K036
- 1.13.0.051 K037
- 1.13.0.052 K038
- 1.13.0.053 K039
- 1.13.0.007 K03
- 1.13.C.054 K040
- 1.13.0.055 K041
- 1.13.0.056 K042
- 1.13.0.057 K043
- 1.13.C.060 K044
- 1.13.0.061 K045
- 1.13.0.062 K046
- 1.13.0.063 K047
- 1.13.0.064 K048
- 1.13.0.065 K049
- 1.13.0.010 K04
- 1.13.0.066 K050
- 1.13.C.067 K051
- 1.13.0.070 K052
- 1.13.0.071 K053
- 1.13.0.072 K054
- 1.13.0.073 K055
- 1.13.0.074 K056
- 1.13.0.075 K057
- 1.13.0.076 K058
- 1.13.0.077 K059

80080 RO370

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 18)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.13.0.077 KD59
 1.13.C.011 KD5
 1.13.0.100 KP60
 1.13.0.101 KU61
 1.13.0.102 KD62
 1.13.0.103 K063
 1.13.0.104 KD64
 1.13.0.105 K065
 1.13.0.106 K066
 1.13.C.107 K067
 1.13.0.110 KU68
 1.13.0.111 K069
 1.13.C.012 K06
 1.13.0.112 KD70
 1.13.0.113 KU71
 1.13.0.114 KD72
 1.13.0.115 K073
 1.13.0.116 K074
 1.13.0.117 K075
 1.13.0.120 K076
 1.13.0.121 K077
 1.13.0.122 K078
 1.13.0.123 K079
 1.13.0.013 K07
 1.13.0.124 K080
 1.13.0.125 K081
 1.13.0.126 K082
 1.13.0.127 K083
 1.13.0.130 K084
 1.13.C.131 K085
 1.13.0.132 K086
 1.13.0.133 K087
 1.13.0.134 K088
 1.13.0.135 K089
 1.13.0.014 K08
 1.13.0.136 K090
 1.13.0.137 KU91
 1.13.0.140 K092
 1.13.0.141 K093
 1.13.0.142 K094
 1.13.0.143 K095
 1.13.C.144 K096
 1.13.0.145 K097
 1.13.0.146 K098
 1.13.0.147 K099
 1.13.C.015 K09
 0.05.0.075 KD
 1.12.0.143 KEM100
 1.12.0.144 KEM101
 1.12.0.145 KEM102
 1.12.0.146 KEM103
 1.12.0.147 KEM104
 1.12.0.150 KEM105
 1.12.0.151 KEM106
 1.12.0.152 KEM107
 1.12.0.153 KLM108

47460

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 19)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

- 1.12.0.154 KEM109
- 1.12.0.011 KEM10
- 1.12.0.155 KEM10
- 1.12.0.156 KEM11
- 1.12.0.157 KEM12
- 1.12.0.160 KEM13
- 1.12.0.161 KEM14
- 1.12.0.162 KEM15
- 1.12.0.163 KEM16
- 1.12.0.164 KEM17
- 1.12.0.165 KEM18
- 1.12.0.166 KEM19
- 1.12.0.012 KEM11
- 1.12.0.167 KEM120
- 1.12.0.170 KEM121
- 1.12.0.171 KEM122
- 1.12.0.172 KEM123
- 1.12.0.173 KEM124
- 1.12.0.174 KEM125
- 1.12.0.175 KEM126
- 1.12.0.176 KEM127
- 1.12.0.177 KEM128
- 1.12.0.200 KEM129
- 1.12.0.013 KEM12
- 1.12.0.201 KEM130
- 1.12.0.202 KEM131
- 1.12.0.203 KEM132
- 1.12.0.204 KEM133
- 1.12.0.205 KEM134
- 1.12.0.206 KEM135
- 1.12.0.207 KEM136
- 1.12.0.210 KEM137
- 1.12.0.211 KEM138
- 1.12.0.212 KEM139
- 1.12.0.014 KEM13
- 1.12.0.213 KEM140
- 1.12.0.214 KEM141
- 1.12.0.215 KEM142
- 1.12.0.216 KEM143
- 1.12.0.217 KEM144
- 1.12.0.220 KEM145
- 1.12.0.221 KEM146
- 1.12.0.222 KEM147
- 1.12.0.223 KEM148
- 1.12.0.224 KEM149
- 1.12.0.015 KEM14
- 1.12.0.225 KEM150
- 1.12.0.226 KEM151
- 1.12.0.227 KEM152
- 1.12.0.230 KEM153
- 1.12.0.231 KEM154
- 1.12.0.232 KEM155
- 1.12.0.233 KEM156
- 1.12.0.234 KEM157
- 1.12.0.235 KEM158
- 1.12.0.236 KEM159

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 20)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.12.0.016	KEM15	
1.12.0.237	KEM160	
1.12.0.240	KEM161	
1.12.0.241	KEM167	
1.12.0.242	KEM163	
1.12.0.243	KEM164	
1.12.0.244	KEM165	
1.12.0.245	KEM166	
1.12.0.246	KEM167	
1.12.0.247	KEM168	
1.12.0.250	KEM169	
1.12.0.017	KEM16	
1.12.0.251	KEM17C	
1.12.0.252	KEM171	
1.12.0.253	KEM172	
1.12.0.020	KEM17	
1.12.0.021	KEM18	
1.12.0.022	KEM19	
1.12.0.000	KEM1	80130
1.12.0.023	KEM20	80390
1.12.0.024	KEM21	
1.12.0.025	KEM22	
1.12.0.026	KEM23	
1.12.0.027	KEM24	
1.12.0.030	KEM27	
1.12.0.031	KEM26	
1.12.0.032	KEM27	
1.12.0.033	KEM28	
1.12.0.034	KEM29	
1.12.0.001	KEM2	
1.12.0.035	KEM10	
1.12.0.036	KEM11	
1.12.0.037	KEM12	
1.12.0.040	KEM15	
1.12.0.041	KEM34	
1.12.0.042	KEM15	
1.12.0.043	KEM36	
1.12.0.044	KEM37	
1.12.0.045	KEM38	
1.12.0.046	KEM39	
1.12.0.002	KEM3	
1.12.0.047	KEM40	
1.12.0.050	KEM41	
1.12.0.051	KEM42	
1.12.0.052	KEM43	
1.12.0.053	KEM44	
1.12.0.054	KEM45	
1.12.0.055	KEM46	
1.12.0.056	KEM47	
1.12.0.057	KEM48	
1.12.0.060	KEM49	
1.12.0.003	KEM4	
1.12.0.061	KEM50	
1.12.0.062	KEM51	
1.12.0.063	KEM52	
1.12.0.064	KEM53	

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 21)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.12.0.065	KEM54	
1.12.0.066	KEM55	
1.12.0.067	KEM56	
1.12.0.070	KEM57	
1.12.0.071	KEM58	
1.12.0.072	KEM59	
1.12.0.004	KEM5	
1.12.0.073	KEM60	
1.12.0.074	KEM61	
1.12.0.075	KEM62	
1.12.0.076	KEM63	
1.12.0.077	KEM64	
1.12.0.100	KEM65	
1.12.0.101	KEM66	
1.12.0.102	KEM67	
1.12.0.103	KEM68	
1.12.0.104	KEM69	
1.12.0.005	KEM6	
1.12.0.105	KEM70	
1.12.0.106	KEM71	
1.12.0.107	KEM72	
1.12.0.110	KEM73	
1.12.0.111	KEM74	
1.12.0.112	KEM75	
1.12.0.113	KEM76	
1.12.0.114	KEM77	
1.12.0.115	KEM78	
1.12.0.116	KEM79	
1.12.0.006	KEM7	
1.12.0.117	KEM80	
1.12.0.120	KEM81	
1.12.0.121	KEM82	
1.12.0.122	KEM83	
1.12.0.123	KEM84	
1.12.0.124	KEM85	
1.12.0.125	KEM86	
1.12.0.126	KEM87	
1.12.0.127	KEM88	
1.12.0.130	KEM89	
1.12.0.007	KEM8	
1.12.0.131	KEM90	
1.12.0.132	KEM91	
1.12.0.133	KEM92	
1.12.0.134	KEM93	
1.12.0.135	KEM94	
1.12.0.136	KEM95	
1.12.0.137	KEM96	
1.12.0.140	KEM97	
1.12.0.141	KEM98	
1.12.0.142	KEM99	
1.12.0.010	KEM9	
0.05.0.116	KF	47470
0.05.0.137	KF	47480
0.05.0.160	KG	47490
0.16.0.314	KHDG1	49930
0.16.0.323	KHDG2	49940
		51590
		51600

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 22)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0+16+0+276 KHUO	49920	51580							
0+15+0+274 KHP	43010	43050							
0+15+0+273 KHP	42980	43320	43550						
0+05+0+201 KH	47500								
0+05+0+222 KJ	47700	47720	47780	47800	47820	47840	47860		
0+05+0+224 KJ	47880								
0+05+0+234 KK	45950	45960	45970	45980	46010	46020	46030		
0+05+0+236 KK									
0+11+0+004 KLI	44800								
0+11+0+005 NL2	44870								
0+11+0+006 KL3	44940								
0+11+0+007 KL4	45030								
0+11+0+010 KLS	45100								
0+11+0+011 KL6	45190								
0+05+0+245 KL	46100	46110							
1+07+0+072 KCAF1	75010								
1+07+0+375 KKA	12270								
0+15+0+266 KMAXPA	42640								
0+15+0+267 KMAXM	43100	43150	43220						
0+15+0+271 KMAXPA	42790								
0+15+0+272 KMAXP	42950	43120	43180						
0+10+0+375 KKH	12330								
0+02+0+375 KMC									
0+03+0+375 KMD									
0+04+0+375 KMF									
0+05+0+375 KMG									
0+06+0+375 KMH									
0+11+0+375 KHM									
0+12+0+375 KMJ									
0+13+0+375 KMK									
0+14+0+375 KML									
0+15+0+375 KMM									
0+16+0+375 KMN									
0+17+0+375 KMO									
0+01+0+375 KMP									
0+07+0+375 KMJ									
0+00+0+375 KMR									
1+07+1+250 KNAH3	12420								
1+07+1+251 KNAC3	79960								
1+06+1+173 KPAF1	80030								
0+17+0+036 KSI	85740								
0+17+0+036 KSI	32340	32370	37690	39180	46640	46720	46870	47160	87020
0+17+0+036 KSI	50600	52570	53220	73260	80220	86960	86990		
0+17+0+036 KSI	87050	87090							
0+17+0+037 KS2	36720	36750	37130	37760	38670	75340	50190	47370	
0+17+0+040 K41	32650	33400	33880	34470	34540	42360	47300		
0+17+0+040 K41	52410	53100	79940	80010	85780	85860	85900		
0+17+0+041 K42	32660								
0+17+0+042 K43	33410								
0+17+0+043 K44	33890								
0+17+0+044 K45	34550								
0+17+0+045 K46	34500								
0+17+0+045 K46	85750								
0+17+0+046 K47	31190								
0+17+0+047 K48	31220								
0+03+0+152 LIOP10									
0+03+0+161 LIOP11									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 23)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0,03,0,166	L10P12	
0,03,0,173	L10P13	
0,03,0,202	L10P14	
0,03,0,210	L10P15	
0,03,0,216	L10P16	
0,03,0,224	L10P17	
0,03,0,232	L10P18	
0,03,0,243	L10P19	
0,03,0,031	L10P1	
0,03,0,752	L10P20	
0,03,0,264	L10P21	
0,03,0,302	L10P22	
0,03,0,323	L10P23	
0,03,0,340	L10P24	
0,03,1,002	L10P25	
0,03,1,023	L10P26	
0,03,1,045	L10P27	
0,03,1,063	L10P28	
0,03,1,073	L10P29	
0,03,0,063	L10P2	
0,03,1,114	L10P30	
0,03,1,123	L10P31	
0,03,1,132	L10P33	
0,03,1,145	L10P34	
0,03,1,153	L10P35	
0,03,1,160	L10P36	
0,03,1,166	L10P37	
0,03,1,173	L10P38	
0,03,1,215	L10P39	
0,03,0,070	L10P3	
0,03,1,225	L10P40	
0,03,1,235	L10P41	
0,03,1,245	L10P42	
0,03,1,255	L10P43	
0,03,1,265	L10P44	
0,03,1,275	L10P45	
0,03,0,075	L10P4	
0,03,0,107	L10P5	
0,03,0,116	L10P6	
0,03,0,125	L10P7	
0,03,0,134	L10P8	
0,03,0,143	L10P9	
0,04,0,053	L11P10	25450
0,04,0,064	L11P11	
0,04,0,076	L11P12	
0,04,0,110	L11P13	
0,04,0,122	L11P14	
0,04,0,133	L11P15	
0,04,0,141	L11P18	
0,04,0,146	L11P19	
0,03,1,315	L11P1	25980
0,04,0,154	L11P20	
0,04,0,163	L11P21	
0,04,0,172	L11P22	
0,04,0,201	L11P23	
0,04,0,710	L11P24	24070

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 24)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.04.0.217 LL1P25								
0.04.0.226 LL1P26								
0.04.0.235 LL1P27								
0.04.0.305 LL1P28	26070	26130	26200	26270	26340	26410	26480	26550
0.04.0.305 LL1P28	26690							26620
0.04.0.245 LL1P29								
0.03.1.323 LL1P2								
0.04.0.255 LL1P10								
0.04.0.263 LL1P31								
0.04.0.273 LL1P32								
0.04.0.307 LL1P33								
0.03.1.327 LL1P3	26790	26850	26940	27020				
0.03.1.336 LL1P4								
0.03.1.347 LL1P5								
0.04.0.002 LL1P6								
0.04.0.013 LL1P7								
0.04.0.024 LL1P8								
0.04.0.035 LL1P9								
0.04.0.124 LL1PA								
0.06.0.001 LL2P1								
0.06.0.366 LL2P2								
0.06.0.046 LL2P3								
0.06.0.370 LL2P4								
0.06.0.064 LL2P5								
0.06.1.000 LL2P6								
0.06.0.102 LL3P1								
0.06.1.010 LL3P2								
0.06.0.120 LL3P3								
0.06.1.012 LL3P4								
0.06.0.136 LL3P5								
0.06.1.014 LL3P6								
0.06.0.154 LL4P1								
0.06.1.016 LL4P2								
0.06.0.172 LL4P3								
0.06.1.020 LL4P4								
0.06.0.210 LL4P5								
0.06.1.022 LL4P6								
0.01.0.234 LL5P1J	10190	10280	10370	10460	10550	10640	11720	11810
0.01.0.234 LL5P1H	11940	12080	12170	12450	12470	12490		11900
0.01.0.234 LL5P1M	9570	9660	9750	9840	9920	10000	10100	10800
0.01.0.234 LL5P1J	10890	10980	11070	11160	11290	11380	11460	11630
0.01.0.234 LL5P1J								
0.00.1.173 LL5P1K	5710	5810	5910	5930	6020	6100	6180	6360
0.00.1.173 LL5P1K	6450	6540	6620	6720	6800	6890	6970	7140
0.00.1.173 LL5P1K	7220	7310	7390	7470	7550	7640	7720	7880
0.00.1.173 LL5P1K	7960	8040	8140	8220	8310	8400	8490	8670
0.00.1.173 LL5P1K	8760	8840	8920	9010	9100	9200	9280	9460
0.00.1.173 LL5P1K								
0.00.0.227 LL5P1L	5360	5450						
1.17.1.363 LL5P1M	12770							
0.01.1.136 LL5P1M	12910							
0.02.1.356 LL5P1P	15000	13090	13180	13190	13270	13370	15380	15450
0.02.1.356 LL5P1P	15570	15070	15120	15180	15240	15310	15990	15510
0.02.1.356 LL5P1P	16200	15640	15710	15780	15850	15920	16060	16130
0.02.1.356 LL5P1P	16830	16270	16340	16410	16480	16550	16620	16690
0.02.1.356 LL5P1P	16830	16900	16970	17040	17110	17180	17250	17320
0.02.1.356 LL5P1P	17480	17550	17620	17690	17760	17830	17900	18040

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 25)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0,03,1,305	L15P1Q	18110	18180	18250	18320	18390	18460	18530	18600	18670
0,03,1,305	L15P1Q	18740	18810	18880	18950	19020	19090	19160	19230	19300
0,03,1,305	L15P1Q	19370	19440	19510	19580	19650	19720	19790	19860	19930
0,03,1,305	L15P1Q	20130	20200	20270	20340	20410	20480	20550	20620	20690
0,03,1,305	L15P1Q	21200	21270	21340	21410	21480	21550	21620	21690	21760
0,03,1,305	L15P1Q	22030	22100	22170	22240	22310	22380	22450	22520	22590
0,03,1,305	L15P1Q	23040	23110	23180	23250	23320	23390	23460	23530	23600
0,03,1,305	L15P1Q	23810	23880	23950	24020	24090	24160	24230	24300	24370
0,03,1,361	L15P1R	24670	24740	24810	24880	24950	25020	25090	25160	25230
0,06,0,226	L15P1	30720	30790	30860	30930	31000	31070	31140	31210	31280
0,06,1,040	L15P1S	28230	28300	28370	28440	28510	28580	28650	28720	28790
0,06,1,040	L15P1S	29580	29650	29720	29790	29860	29930	30000	30070	30140
0,01,1,015	L15P1T	12290	12350	12410	12470	12530	12590	12650	12710	12770
0,06,1,024	L15P2	30750	30810	30870	30930	30990	31050	31110	31170	31230
0,06,0,244	L15P3	30780	30840	30900	30960	31020	31080	31140	31200	31260
0,06,1,026	L15P4	30810	30870	30930	30990	31050	31110	31170	31230	31290
0,06,0,262	L15P5	30840	30900	30960	31020	31080	31140	31200	31260	31320
0,06,1,030	L15P6	30870	30930	30990	31050	31110	31170	31230	31290	31350
0,06,0,300	L16P1	30810	30870	30930	30990	31050	31110	31170	31230	31290
0,06,1,032	L16P2	30840	30900	30960	31020	31080	31140	31200	31260	31320
0,06,0,316	L16P3	30870	30930	30990	31050	31110	31170	31230	31290	31350
0,06,1,034	L16P4	30810	30870	30930	30990	31050	31110	31170	31230	31290
0,06,0,334	L16P5	30840	30900	30960	31020	31080	31140	31200	31260	31320
0,06,1,036	L16P6	30870	30930	30990	31050	31110	31170	31230	31290	31350
0,06,0,352	L17P1	30900	30960	31020	31080	31140	31200	31260	31320	31380
0,13,0,310	L17P2	31400	31460	31520	31580	31640	31700	31760	31820	31880
0,13,0,320	L17P3A	31210	31270	31330	31390	31450	31510	31570	31630	31690
0,13,0,350	L17P3B	31210	31270	31330	31390	31450	31510	31570	31630	31690
0,13,0,331	L17P3C	31290	31350	31410	31470	31530	31590	31650	31710	31770
0,13,0,324	L17P3	31120	31180	31240	31300	31360	31420	31480	31540	31600
0,16,0,060	L1P1A1	2670	2730	2790	2850	2910	2970	3030	3090	3150
0,00,0,015	L1P1A	49330	49390	49450	49510	49570	49630	49690	49750	49810
0,16,0,070	L1P1K	49330	49390	49450	49510	49570	49630	49690	49750	49810
0,16,0,000	L1P1C	49340	49400	49460	49520	49580	49640	49700	49760	49820
0,00,0,000	L1P1	14670	14730	14790	14850	14910	14970	15030	15090	15150
0,01,1,143	L20P1A	30380	30440	30500	30560	30620	30680	30740	30800	30860
0,06,1,060	L20P1	32900	32960	33020	33080	33140	33200	33260	33320	33380
0,07,1,000	L20P2A	31970	32030	32090	32150	32210	32270	32330	32390	32450
0,07,1,002	L20P2B	31740	31800	31860	31920	31980	32040	32100	32160	32220
0,06,1,065	L20P2	32330	32390	32450	32510	32570	32630	32690	32750	32810
0,07,1,005	L20P3	32640	32700	32760	32820	32880	32940	33000	33060	33120
0,07,1,012	L20P4	32330	32390	32450	32510	32570	32630	32690	32750	32810
0,07,1,013	L20P5	32640	32700	32760	32820	32880	32940	33000	33060	33120
0,07,1,020	L20P6	32360	32420	32480	32540	32600	32660	32720	32780	32840
0,07,1,022	L21P1	32990	33050	33110	33170	33230	33290	33350	33410	33470
0,07,1,030	L21P2	32160	32220	32280	32340	32400	32460	32520	32580	32640
0,07,1,041	L21P3	32160	32220	32280	32340	32400	32460	32520	32580	32640
0,07,1,046	L21P4	32470	32530	32590	32650	32710	32770	32830	32890	32950
0,07,1,063	L21P5	32510	32570	32630	32690	32750	32810	32870	32930	32990
0,07,1,067	L22P1	32550	32610	32670	32730	32790	32850	32910	32970	33030
0,07,1,073	L22P2	32470	32530	32590	32650	32710	32770	32830	32890	32950
0,07,1,077	L22P3	32470	32530	32590	32650	32710	32770	32830	32890	32950
0,07,1,102	L22P4	32480	32540	32600	32660	32720	32780	32840	32900	32960
0,07,1,116	L23P1	32480	32540	32600	32660	32720	32780	32840	32900	32960
0,07,1,130	L23P2	32480	32540	32600	32660	32720	32780	32840	32900	32960

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 26)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0,07,1,136 L23P3	32860								
0,07,1,144 L23P4									
0,10,0,032 L23P5									
0,07,1,152 L24P1	32520								
0,07,1,176 L24P2									
0,07,1,164 L24P3									
0,07,1,172 L24P4									
0,07,1,200 L24P5	33140								
0,07,1,212 L25P1									
0,07,1,234 L25P2									
0,07,1,251 L25P3									
0,07,1,257 L26P1	33690								
0,07,1,270 L26P2	32560								
0,07,1,304 L27P1	32590								
0,07,1,315 L27P2	34020								
0,07,1,322 L27P3									
0,07,1,331 L28P1									
0,07,1,337 L28P2	34200								
0,10,0,006 L28P3									
0,07,1,352 L28P4	34490								
0,07,1,353 L28P5	34600								
0,10,0,000 L28P6A									
0,10,0,001 L28P6B									
0,07,1,354 L28P6	32110	32170	32260	32310	32810	32930	33090	33150	
0,07,1,354 L28P6	33210	33310	33500	33640	33700	34030	34080	34150	
0,07,1,354 L28P6	34210	34280							
0,06,1,064 L29P1A	31750								
0,10,0,034 L29P1	35860								
0,10,0,041 L29P2	36150								
0,10,0,066 L29P3	36250								
0,10,0,100 L29P4	2680	3390	5560						
0,00,0,016 L2P1	3100								
0,00,0,070 L2P2									
0,10,0,111 L30P1									
0,10,0,133 L30P2A									
0,10,0,124 L30P2									
0,10,0,140 L31P1	36710	36730	36910	42130	42150				
0,10,0,143 L31P2	36740	36760	42180	42200					
0,10,0,145 L31P3	36600								
0,10,0,160 L31P4									
0,10,0,164 L32P1									
0,10,0,173 L32P2									
0,10,0,203 L32P3									
0,10,0,213 L32P4									
0,10,0,224 L33P1	37230								
0,10,0,234 L33P2									
0,10,0,243 L33P3									
0,10,0,250 L34P1	37440	37470	37720	37740	37820				
0,10,0,301 L34P2	37510	37540	37750	37770					
0,10,0,304 L34P3									
0,10,0,306 L34P4									
0,10,0,321 L34P5									
0,10,0,325 L34P6									
0,10,0,334 L34P7									
0,10,0,344 L34P8									
0,10,0,354 L34P9									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 27)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.11.0.260 L35+2						
0.11.0.272 L35P3	38730	38830				
0.11.0.276 L35P4	38660	38680				
0.11.0.300 L36P1			42240	42260		
0.11.0.317 L36P2						
0.11.0.323 L36+3						
0.11.0.326 L36+4						
0.10.1.000 L37P1A						
0.11.0.334 L37P1	38760					
0.10.1.004 L37P2	39240					
0.10.1.014 L37P3	39170	39190	42300	42320		
0.10.1.016 L37P4						
0.10.1.031 L37P5						
0.10.1.032 L38P1						
0.10.1.035 L38+2						
0.10.1.040 L38P3						
0.10.1.046 L38P4	39270					
0.10.1.060 L39P1	39450					
0.10.1.101 L39P2A						
0.10.1.071 L39P2						
0.10.1.104 L39P3A						
0.10.1.103 L39P3						
0.10.1.110 L39P4						
0.00.0.071 L3P1	3110					
0.10.1.117 L40P1						
0.10.1.134 L40P2						
0.10.1.144 L40P3						
0.10.1.154 L41P1						
0.10.1.161 L41P2						
0.10.1.202 L41P3						
0.10.1.207 L42P1						
0.10.1.223 L42P2						
0.10.1.232 L42P3						
0.10.1.232 L42P3						
0.10.1.232 L42P3						
0.11.0.343 L42P4A						
0.10.1.240 L42P4	36350	36470	36900	37060	37160	37240
0.10.1.242 L43P1	37990	38070	38150	38260	39460	37310
0.10.1.275 L43P2	39800	39980	40060	40110	39630	39680
0.10.1.275 L43P2	38540				40350	40540
0.10.1.242 L43P1	36160	36260	36540	36660	37670	39090
0.10.1.275 L43P2	42310	40550				
0.10.0.040 L45P1A	35870					
0.11.1.000 L45P1						
0.11.1.005 L45P2	42470					
0.11.1.043 L45P3A	42620					
0.11.1.051 L45P3B	42870					
0.11.1.026 L45P3						
0.11.1.052 L45P4						
0.11.1.055 L45P5						
0.11.1.062 L46P1						
0.11.1.067 L46P2						
0.11.1.074 L46P3						
0.11.1.077 L46P4						
0.11.1.103 L46P5						
0.11.1.110 L46P6						
0.11.1.115 L46P7						
0.11.1.130 L47P1A	43440					
0.11.1.126 L47P1B	42590	42750	43390			

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 28)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.11.1.133 L47PIC	43400								
0.11.1.122 L47P1									
0.11.1.162 L47P2									
0.11.1.260 L47P3A	44370								
0.11.1.264 L47P3	42680								
0.11.1.273 L47P4A	44420								
0.11.1.271 L47P4	42970								
0.11.1.300 L47P5A	44470								
0.11.1.276 L47P5	43040								
0.11.1.303 L48P1	43060								
0.11.1.303 L48P1	44030								
0.11.1.155 L48P2	43970								
0.11.1.222 L48P3	44240								
0.00.0.153 L4CP1	3340								
0.00.0.156 L4CP2	3360								
0.00.0.161 L4CP3	3380								
0.00.0.123 L4P1	3180								
0.00.0.126 L4P2	3200								
0.00.0.131 L4P3	3220								
0.00.0.134 L4P4	3240								
0.00.0.137 L4P5	3260								
0.00.0.142 L4P6	3280								
0.00.0.145 L4P7	3300								
0.00.0.150 L4P8	3320								
0.11.1.004 L50P1A	42480								
0.11.0.000 L50P1	44590								
0.11.0.017 L50P2									
0.11.0.025 L50P3									
0.11.0.034 L50P4									
0.11.0.043 L51P1									
0.11.0.052 L51P2									
0.11.0.063 L51P3									
0.11.0.107 L52P1									
0.11.0.122 L52P2A									
0.00.0.164 L5P1									
1.12.0.376 L5P2AA									
0.01.0.062 L5P2A									
1.13.0.376 L5P2AH									
0.02.1.000 L5P2B									
1.14.0.177 L5P2CC									
0.03.0.376 L5P2C									
1.15.0.007 L5P2D0									
0.04.0.052 L5P2D									
1.16.1.000 L5P2EE									
0.05.0.003 L5P2E									
1.17.1.375 L5P2FF									
0.06.0.006 L5P2F									
0.07.0.177 L5P25									
0.10.1.077 L5P2H									
0.11.1.257 L5P2I									
0.12.0.000 L5P2J									
0.13.1.376 L5P2K									
0.14.0.030 L5P2L									
0.15.0.376 L5P2M									
0.16.0.000 L5P2N									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 29)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.00.0.234	L6P1A	5550
0.00.0.230	L6P1	3750
0.00.1.063	L6P20	5480
0.00.1.073	L6P21	
0.00.1.102	L6P22	
0.00.1.111	L6P23	
0.00.0.251	L6P2A	5680
0.00.0.235	L6P2	1450
0.00.0.253	L6P3	
0.00.0.264	L6P4	
0.00.0.276	L6P5	
0.00.0.306	L6P6	
0.00.0.315	L6P7	
0.00.0.325	L6P8	6190
0.00.0.335	L6P9	6270
0.00.1.222	L7P10	
0.00.1.242	L7P11	
0.00.1.242	L7P12	
0.00.1.252	L7P13	
0.00.1.262	L7P14	
0.00.1.272	L7P15	
0.00.1.301	L7P16	
0.00.1.310	L7P17	
0.00.1.320	L7P18	
0.00.1.330	L7P19	
0.00.1.120	L7P1	
0.00.1.337	L7P20	
0.00.1.346	L7P21	
0.00.1.356	L7P22	
0.01.0.003	L7P23	
0.01.0.013	L7P24	
0.01.0.023	L7P25	
0.01.0.033	L7P26	
0.01.0.043	L7P27	
0.01.0.052	L7P28	
0.01.0.061	L7P29	
0.00.1.177	L7P2	
0.01.0.075	L7P30	
0.01.0.105	L7P31	
0.01.0.115	L7P32	
0.01.0.125	L7P33	
0.01.0.135	L7P34	
0.01.0.145	L7P35	
0.01.0.155	L7P36	
0.01.0.164	L7P37	
0.01.0.173	L7P38	
0.01.0.203	L7P39	
0.00.1.136	L7P3	
0.01.0.213	L7P40	
0.01.0.223	L7P41	
0.01.0.235	L7P42	
0.01.0.245	L7P43	
0.01.0.255	L7P44	
0.01.0.264	L7P45	
0.01.0.273	L7P46	
0.01.0.307	L7P47	
		11170

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 31)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.01.0.317 L7P48					
0.01.0.327 L7P49					
0.00.1.145 L7P4					
0.01.0.337 L7P50					
0.01.0.347 L7P51					
0.01.0.357 L7P52					
0.01.1.002 L7P53					
0.03.0.023 L7P54A					
0.03.0.027 L7P54B					
0.03.0.017 L7P54					
1.17.1.356 L7P55A					
1.17.1.352 L7P55					
0.00.1.154 L7P5					
0.00.1.163 L7P6					
0.00.1.174 L7P7					
0.00.1.203 L7P8					
0.00.1.212 L7P9					
0.01.1.040 L8P1					
0.01.1.050 L8P2					
0.01.1.060 L8P3					
0.01.1.070 L8P4					
0.01.1.100 L8P5					
0.01.1.110 L8P6					
0.01.1.120 L8P7					
0.01.1.126 L8P8					
0.01.1.134 L8P9					
0.16.1.012 L90P1A	13410	13430			
0.06.1.120 L90P1					
0.06.1.126 L90P2					
0.06.1.132 L90P3					
0.06.1.164 L90P4A					
0.06.1.155 L90P4					
0.06.1.230 L90P6					
0.06.1.245 L94P1					
0.06.1.256 L94P2					
0.06.1.272 L94P3					
0.03.0.030 L95P1A					
0.16.0.001 L95P1					
0.16.0.004 L95P2					
0.16.0.006 L95P3					
0.16.0.010 L95P4					
0.16.0.012 L95P5					
0.16.0.026 L95P6					
0.16.0.002 L95P7					
0.16.0.033 L96P1					
0.16.0.054 L96P2					
0.16.0.057 L96P3					
0.16.1.007 L97P1					
0.16.1.013 L97P2					
0.16.1.023 L97P3					
0.16.1.041 L97P4A					
0.16.1.035 L97P4					
0.16.1.060 L97P5					
0.16.1.113 L98P1A					
0.16.1.111 L98P1					
0.16.1.133 L98P2A					
12180					
8050					
13510					
13390					
50340					
52400	52430	52560	52580	52630	
52720					
52310	52800	52960	52980	53250	
53090	53120	53210	53230	53250	
52170	52190	52230	52330	52650	
12630					
49150	49170	49590	49610		
49180	49200	49640	49660		
49210	49230	49690	49710		
49240	49260	49740	49760		
49020					
49120	49140	49540	49560		
49070					
49110					
49280					
50290	50950				
50380	50400	50590	50610	50650	
50710					
51120					
50430	50540	50740	50840		
51340					
					52890
					52850
					52680
					52650
					51360

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 32)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.16.1.125 L98P2	50580	50800	50900	50910
0.16.0.163 L98P3A	49390	50020	50180	50200
0.16.0.165 L98P3B	50090	50170		
0.16.0.161 L98P3C	50240			
0.16.0.152 L98P3	50470	50780	50880	
0.16.1.151 L98P4	50350	50480	50660	
0.16.1.160 L98P5	50470	50670	50820	50920
0.10.1.304 L99P1	52130			
0.02.0.042 L9P10				
0.02.0.051 L9P11				
0.02.0.060 L9P12				
0.02.0.066 L9P13				
0.02.0.074 L9P14				
0.02.0.103 L9P15				
0.02.0.112 L9P16				
0.02.0.121 L9P17				
0.02.0.130 L9P18				
0.02.0.137 L9P19				
0.01.1.137 L9P1				
0.02.0.146 L9P20				
0.02.0.155 L9P21				
0.02.0.164 L9P22				
0.02.0.173 L9P23				
0.02.0.202 L9P24				
0.02.0.211 L9P25				
0.02.0.220 L9P26				
0.02.0.227 L9P27				
0.02.0.236 L9P28				
0.02.0.245 L9P29				
0.01.1.144 L9P2	14660			
0.02.0.254 L9P30				
0.02.0.263 L9P31				
0.02.0.272 L9P32				
0.02.0.301 L9P33				
0.02.0.310 L9P34				
0.02.0.317 L9P35				
0.02.0.326 L9P36				
0.02.0.335 L9P37				
0.02.0.344 L9P38				
0.02.0.353 L9P39				
0.01.1.154 L9P3	14770			
0.02.1.002 L9P40	17400			
0.02.1.011 L9P41				
0.02.1.020 L9P42				
0.02.1.027 L9P43				
0.02.1.036 L9P44				
0.02.1.045 L9P45				
0.02.1.054 L9P46				
0.02.1.063 L9P47				
0.02.1.072 L9P48				
0.02.1.101 L9P49				
0.02.0.002 L9P4				
0.02.1.110 L9P50				
0.02.1.117 L9P51				
0.02.1.126 L9P52				
0.02.1.135 L9P53				

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 33)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.02.1.144 L9P54	47330	49000	49480	50790	52820
0.02.1.153 L9P55	3040	49490			
0.02.1.162 L9P56	3060	50890			
0.02.1.171 L9P57	3080	52980			
0.02.1.200 L9P58	48940	53360			
0.02.1.207 L9P59	49060	78390			
0.02.0.004 L9P5	49090				
0.02.1.216 L9P60	2600				
0.02.1.225 L9P61	61010				
0.02.1.234 L9P62	48970				
0.02.1.243 L9P63	2980				
0.02.1.252 L9P64	3350				
0.02.1.261 L9P65	3370				
0.02.1.270 L9P66	3020				
0.02.1.277 L9P67	2800				
0.02.1.306 L9P68	2820				
0.02.1.315 L9P69	2840				
0.02.0.012 L9P6	2860				
0.02.1.324 L9P70	2880				
0.02.1.333 L9P71	2900				
0.02.1.342 L9P72	2920				
0.02.0.017 L9P7	2940				
0.02.0.025 L9P8	2960				
0.02.0.033 L9P9	2980				
0.04.1.256 LA	3000				
0.13.0.135 LC1	3020				
0.17.0.050 LC2	3040				
0.17.0.031 LC3	3060				
0.17.0.052 LC5	3080				
0.16.0.274 LC6	3100				
0.17.0.033 LC7	3120				
0.17.0.034 LC8	3140				
0.16.0.210 LC9	3160				
0.17.0.065 LCR10	3180				
0.17.0.066 LCR11	3200				
0.17.0.067 LCR12	3220				
0.13.0.134 LCR1	3240				
0.17.0.035 LCR2	3260				
0.17.0.036 LCR3	3280				
0.17.0.037 LCR4	3300				
0.17.0.060 LCR5	3320				
0.17.0.061 LCR6	3340				
0.17.0.062 LCR7	3360				
0.17.0.063 LCR8	3380				
0.17.0.064 LCR9	3400				
0.17.0.234 LINE1	3420				
0.17.0.244 LINE2	3440				
0.17.0.254 LINE3	3460				
0.17.0.266 LINE4	3480				
0.17.0.306 LINE5A	3500				
0.17.0.300 LINE5	3520				
0.17.0.317 LINE6A	3540				
0.17.0.320 LINE6B	3560				
0.17.0.307 LINE6	3580				
0.02.1.357 LPPA	3600				
	3620				
	3650				
	3680				
	49000				
	49490				
	50890				
	52980				
	53360				
	78390				
	74880				
	78970				
	3350				
	3370				
	3020				
	2800				
	2820				
	2840				
	2860				
	2880				
	2900				
	2920				
	2940				
	2960				
	44650				
	44660				
	44670				
	44680				
	45120				
	44690				
	45280				
	45300				
	44700				
	49080				
	49480				
	50790				
	52820				
	49000				
	49490				
	50890				
	52980				
	53360				
	78390				
	74880				
	78970				
	3350				
	3370				
	3020				
	2800				
	2820				
	2840				
	2860				
	2880				
	2900				
	2920				
	2940				
	2960				
	44650				
	44660				
	44670				
	44680				
	45120				
	44690				
	45280				
	45300				
	44700				
	49080				
	49480				
	50790				
	52820				
	59990				
	60860				
	56610				
	79880				
	55970				
	79170				
	21680				
	14650				
	21570				
	22660				
	31730				
	35850				
	5530				
	13400				
	13380				
	13420				
	42460				
	44580				
	45640				
	53330				

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 34)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.03,1.362 LPR	25170	25260	25350	25440	25550	25650	25750	25850	25940
0.04,0.137 LPR	74900								
0.04,0.137 LPR	53350								
1.05,0.024 MABIA									
1.05,0.014 MABIA									
1.05,0.020 MAB1									
1.05,0.025 MAC1									
1.05,0.043 MAB1									
1.05,0.046 MAE1									
1.05,0.061 MAF1									
1.05,0.073 MAG1									
1.10,0.255 MAG									
1.05,0.101 MAH1									
1.05,0.054 MAJ1									
1.05,0.054 MAJ1									
1.11,0.217 MCTR									
1.11,0.136 MDATA									
1.07,1.045 MABIA									
0.11,0.143 MABIA									
1.07,1.046 MABIC									
1.07,1.044 MAB10									
1.07,1.040 MAB1									
1.07,1.133 MAB2A									
1.07,1.130 MAB2									
1.07,1.213 MAB3									
1.07,1.241 MAB4									
1.07,1.306 MAB5A									
1.07,1.304 MAB5									
1.07,1.056 MAB1									
1.07,1.135 MAB2									
1.07,1.220 MAB3									
1.07,1.154 MAB2A									
1.07,1.137 MAB2									
1.07,1.246 MAB4									
1.07,1.323 MAB5A									
1.07,1.313 MAB5									
1.07,1.234 MAB3									
1.07,1.067 MAF1									
1.07,1.162 MAF2									
1.07,1.252 MAF3									
1.07,1.255 MAF4									
1.07,1.100 MABIA									
1.07,1.072 MAB1									
1.07,1.260 MAB3									
1.07,1.263 MAB4									
1.07,1.115 MABIA									
1.07,1.102 MAB1									
1.07,1.266 MAB3									
1.07,1.271 MAB4									
1.07,1.274 MAB3									
1.07,1.126 MAB5									
1.07,1.123 MAB1									
1.07,0.040 MAB1									
1.07,0.076 MAB2									
1.07,0.205 MAB4									
1.07,0.114 MAB2									

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 35)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.07,0.132 NBE2	80950								
1.07,0.214 NBE4									
1.07,0.152 NBF2	80970								
1.07,0.170 NRG2	80990								
1.07,0.223 NRG4	81160	82000							
1.07,0.055 NBH1									
1.07,0.056 NBH2									
0.16,0.354 NINE	51200	51310	51330						
0.16,0.351 N	51030	51090	51110						
0.12,0.056 P45	32920								
1.07,1.134 PARI1	79570								
1.06,1.030 PARI									
1.06,1.033 PAC1	85550								
1.06,1.116 PAC2									
1.06,1.076 PAD1	86420								
1.06,1.121 PAD2	85850	85880	87030						
1.06,1.100 PAE1	86180	86320	87120	87140					
1.06,1.103 PAF1	85770	85800	86970						
1.06,1.125 PAF2	85890	85920	87040						
1.06,1.127 PAG2									
1.06,1.110 PAH1	85810	85840	86980						
1.06,1.132 PAH2	86820								
1.06,1.135 PAJ2	86810								
1.10,0.256 PATH	85690	86080	86360						
0.15,0.116 PATN1	36460	36650	38300						
0.15,0.226 PATN2	38530	38930							
0.15,0.245 PATN3	39080	40650							
0.15,0.216 PATN4	37660	38320							
0.12,0.001 PATN	32100	34340							
1.06,1.142 PBA1	86370								
1.06,1.144 PBA1									
1.06,1.204 PBA3	86530	87850							
1.06,1.154 PBD1	86400								
1.06,1.157 PBF1	86520								
1.06,1.174 PBF2	86090								
1.06,1.215 PBF3	86900								
1.06,1.244 PCB1	86840								
1.06,1.322 PCB2	86880								
1.06,1.273 PCE1	86860								
1.06,1.350 PCF1	87370	87600	87180	87220	87320	87410	87450		
1.06,1.353 PCH1	86150	86270	87680	87740	87780	87820	87880		
1.06,1.353 PCH1	87510	87550	87640	87740	87780	87820	87880		
0.05,0.001 PGNR	45760	45810	45830	46120	46350	46370	46470		
0.05,0.001 PGNR	47070	47510	47610	47940					
0.15,0.042 PKSC	37630	38310							
1.10,0.251 QUAD1	85620	86450	86510	86430					
1.10,0.252 QUAD2	85630	86650	86830	87360					
1.10,0.253 QUAD3	85640	86850	87340	87590					
1.10,0.254 QUAD4	85650	86870	87570	87820					
0.13,0.237 SAVE	31050	31150							
0.17,0.100 STOP	2580	31900	32430	32490	32570	32620	32960		
0.17,0.100 STOP	33370	33850	36090	38460	38740	38800	38970		
0.17,0.100 STOP	39230	39520	39300	44860	44930	45020	45180		
0.17,0.100 STOP	45480	45560	45580	45920	46070	46070	49430		
0.17,0.100 STOP	49450	50210	50230	50760	50860	50860	52460		
0.17,0.100 STOP	52710	52780	52940	53170	53170	53170	52690		

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 36)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.17,0.077 IEMP1	5670	5180	5800	40590	40630	42370	42400	49810
0.17,0.077 IEMP1	49840	50940	50160	50560	50420	50640		
0.17,0.077 IEMP2	31100	31330						
0.17,0.077 IEMP3	31200	31280						
0.17,0.076 IEMP	19700	24080	31310	24990	25050	27080	27140	28180
0.17,0.075 IEMP	28210	28330	24140	28510	28630	28660	28780	28810
0.17,0.076 IEMP	28930	28960	24480	29230	29260	29380	29410	29530
0.17,0.076 IEMP	29560	29690	29110	29660	29980	30010	30130	30160
0.17,0.076 IEMP	30280	30310	29830	29860	34420	34480	34510	34590
0.17,0.076 IEMP	36620	37460	30970	37530	38490	38620	38640	38640
0.17,0.076 IEMP	38820	39000	37500	39150	39320	42120	42170	42230
0.17,0.076 IEMP	42290	42360	39130	45460	45520	45550	46250	46520
0.17,0.076 IEMP	47280	47350	47380	49320	49530	49580	49630	49680
0.17,0.076 IEMP	49730	49980	50010	50060	50130	50370	50370	52390
0.17,0.076 IEMP	52420	52490	52620	53070	53110	56650	56730	56520
0.17,0.076 IEMP	65623	66730	65810	66000	66060	66350	66450	66560
0.17,0.076 IEMP	66640	66750	65920	67280	67390	67470	67580	67660
0.17,0.075 IEMP	68010	68110	67180	68410	68490	68820	68970	69030
0.17,0.076 IEMP	69110	69220	68300	69740	69850	69930	70040	70120
0.17,0.076 IEMP	70180	70500	70600	70710	70900	70980	71300	71400
0.17,0.076 IEMP	71510	71590	71700	74090	74100	74150	74200	74250
0.17,0.076 IEMP	74300	74350	74400	74490	75000	75030	75900	75950
0.17,0.076 IEMP	76000	76050	76160	76460	76510	76560	76610	76660
0.17,0.076 IEMP	76710	76760	76810	76910	76960	77010	77280	77330
0.17,0.076 IEMP	77440	77490	78000	78210	78260	78360	78410	78500
0.17,0.076 IEMP	78540	78590	78780	78830	79950	79980	80020	80050
0.17,0.076 IEMP	85760	85790	85830	85910				
1.13,0.000 TIME	2620	79130	79160	79600				
0.17,0.070 V1	35910	36180	36280	36490	36570	36860	36920	37000
0.17,0.070 V1	37090	37180	37260	37580	37940	38010	38090	38180
0.17,0.070 V1	38370	38860	39370	39570	39700	39790	39920	40000
0.17,0.070 V1	40090	40150	40320	40510	41690	42950		
0.17,0.071 V2	36000	36300	36390	36590	37600	38420	38840	65250
0.17,0.071 V2	66120	56920	57770	69390	70250	71050	71920	72980
0.17,0.072 V3								
0.17,0.073 V4	39580	39620	42630	53740	53860	53920	54020	54080
0.17,0.073 V4	54180	55150	55210	55330	55410	55490	55620	55660
0.17,0.073 V4	55680	55740	55800	63440	63530	63600	63730	63800
0.17,0.073 V4	63730	63990	64090	64230	65580	65770	65960	66410
0.17,0.073 V4	66600	66790	67240	67620	68070	68260	68450	68880
0.17,0.073 V4	69070	69260	69700	70080	70560	70750	70940	71360
0.17,0.073 V4	71550	71740	72160	72260	72340	72400	72460	72520
0.17,0.073 V4	72580	72640	72700	72820	73240	73300	73360	73420
0.17,0.073 V4	73480	73540	73600	73720	73740	73840	73900	73950
0.17,0.074 V5	36420	36630	36640	37030	37130	37640	39010	
0.17,0.070 VARI	5160	5240	5320	5590	5740	5850	5960	6050
0.17,0.070 VARI	6130	6220	6310	6490	6570	6670	6750	6830
0.17,0.070 VARI	6920	7000	7090	7250	7340	7420	7500	7590
0.17,0.070 VARI	7670	7750	7830	7990	8090	8170	8250	8340
0.17,0.070 VARI	8430	8520	8610	8790	8870	8950	9040	9150
0.17,0.070 VARI	9230	9310	9400	9600	9690	9780	9870	9950
0.17,0.070 VARI	10040	10130	10220	10400	10490	10580	10670	10750
0.17,0.070 VARI	10830	10920	11010	11200	11370	11410	11490	11570
0.17,0.070 VARI	11660	11750	11840	12020	12110	12220	12350	12690

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 37)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0,17,0,071 VAR2	12850	17940	13030	13120	13210	13300	13390	19830	24120
0,17,0,071 VAR2	25010	27120	30960	31820	32750	32980	33030	33750	33830
0,17,0,071 VAR2	33970	42330	43480	48860	49300	56690	5670	5980	6070
0,17,0,071 VAR2	5180	5760	5340	5430	5610	5760	5870	6770	6850
0,17,0,071 VAR2	6150	6240	6330	6410	6510	6590	6690	7520	7610
0,17,0,071 VAR2	6940	7020	7110	7190	7270	7360	7440	8270	8360
0,17,0,071 VAR2	7620	7770	7850	7930	8010	8110	8190	9060	9170
0,17,0,071 VAR2	8450	8540	8630	8720	8810	8890	8970	9890	9970
0,17,0,071 VAR2	9250	9330	9420	9510	9620	9710	9800	10690	10770
0,17,0,071 VAR2	10060	10150	10240	10330	10420	10510	10600	11510	11590
0,17,0,071 VAR2	10850	10940	11030	11120	11250	11340	11430	12580	12720
0,17,0,071 VAR2	11680	11770	11860	11950	12040	12130	12240	25030	27100
0,17,0,071 VAR2	12870	12960	13050	13140	13230	13320	13410	15340	15410
0,17,0,071 VAR2	30940	34410	40610	42560	43510	49290	49470	15950	16020
0,17,0,072 VAR3	2700	2720	48880	48960	49050	49470	15270	16580	16650
0,17,0,073 VAR4	2750	14720	15030	15090	15140	15200	15880	17210	17280
0,17,0,073 VAR4	15480	15530	15600	15670	15740	15810	16510	17860	17930
0,17,0,073 VAR4	16090	16160	16230	16300	16370	16440	17140	18490	18560
0,17,0,073 VAR4	16720	16790	16860	16930	17000	17070	17790	19120	19190
0,17,0,073 VAR4	17350	17440	17510	17580	17650	17720	18420	19820	19850
0,17,0,073 VAR4	18000	18070	18140	18210	18280	18350	19050	20600	20670
0,17,0,073 VAR4	18630	18700	18770	18840	18910	18980	21160	22240	22320
0,17,0,073 VAR4	19260	19330	19400	19470	19540	19610	21040	23170	23250
0,17,0,073 VAR4	19940	20190	20240	20290	20390	20460	20530	24010	24630
0,17,0,073 VAR4	20740	20810	20860	20910	20980	21040	21160	25280	25370
0,17,0,073 VAR4	21330	21400	21500	21640	21820	21950	22070	26090	26150
0,17,0,073 VAR4	22560	22640	22810	22840	22950	23060	23120	26740	27780
0,17,0,073 VAR4	23280	23470	23560	23650	23740	23830	23920	29300	29450
0,17,0,073 VAR4	24690	24730	24800	24890	25000	25100	25190	32080	32130
0,17,0,073 VAR4	25480	25570	25670	25770	25870	25960	26040	33110	33170
0,17,0,073 VAR4	26220	26290	26360	26430	26500	26570	26640	34000	34170
0,17,0,073 VAR4	28250	28400	28550	28700	28850	29000	29150	28950	29100
0,17,0,073 VAR4	29600	29750	29900	30050	30200	30490	31800	30300	32060
0,17,0,073 VAR4	32190	32280	32700	32730	32890	32890	33010	48920	48920
0,17,0,073 VAR4	33230	33350	33530	33660	33720	33960	34050	28800	29100
0,17,0,074 VAR5	34230	34290	34970	48900	63360	80140	28800	30300	32060
0,17,0,074 VAR5	2760	14760	28200	28350	28500	30000	30150	39390	80090
0,17,0,074 VAR5	29250	29400	29550	29700	29850	30000	30150	34100	34170
0,17,0,074 VAR5	32780	33060	33460	33610	34300	38500	39390	28950	29100
0,16,0,341 WURD	50050	51160	51240	51270	53140	86600	86670	28950	29100
1,10,0,105 X1	86000	86060	86200	86280	86550	86600	86670	30300	32060
1,10,0,101 Y1	85700	86380	86460	86460	86390	86410	3550	30300	32060
1,10,0,257 YN	85710	85940	86330	86350	86390	86410	3550	30300	32060
0,17,0,020 ZERO	2560	2740	3400	3430	3460	3490	3520	21980	22170
0,17,0,020 ZERO	3610	3640	3670	3700	13460	14750	15150	19840	20200
0,17,0,020 ZERO	20540	20610	20680	20750	20820	21240	21740	21980	22170
0,17,0,020 ZERO	22360	22490	22570	22750	22980	23070	23130	24020	24650
0,17,0,020 ZERO	26730	26900	26980	31860	32010	32270	33260	33560	34240
0,17,0,020 ZERO	36020	36190	36310	37110	37270	37380	37960	38040	38120
0,17,0,020 ZERO	38230	38430	38600	39030	39270	39380	39490	39590	39710
0,17,0,020 ZERO	39950	40010	40240	39030	39030	39380	39490	42340	43340
0,17,0,020 ZERO	43720	43800	45730	40270	40270	40860	42830	43240	43340
0,17,0,020 ZERO	47750	47770	47790	47810	47830	46060	47130	47710	47730
0,17,0,020 ZERO	52240	52250	52260	52500	52510	52520	52740	47890	49380
0,17,0,070 ZERO	52830	52900	52910	52920	52990	53420	53790	52750	52760
0,17,0,070 ZERO								53950	54110

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 38)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0,05,0,006	=00000020	46040						
0,16,0,353	=00000022	51190						
1,13,0,320	=00000022	81390						
0,12,0,174	=00000024	32980						
0,11,0,354	=00000024	44920						
0,05,0,005	=00000024	4890						
0,16,0,211	=00000024	79140						
1,13,0,262	=00000024	81250						
0,15,0,347	=00000030	38450						
1,10,0,261	=00000030	87690						
0,16,0,344	=00000034	52280						
0,14,0,313	=00000040	23840						
0,15,0,305	=00000040	36110						
1,10,0,005	=00000040	53510						
1,11,0,003	=00000040	65410						
1,13,0,267	=00000040	79330						
1,11,0,033	=00000044	71950						
0,12,0,177	=00000046	32500						
1,13,0,316	=00000050	81270						
1,13,0,275	=00000074	79670						
0,13,0,244	=00000076	31340						
0,14,0,315	=00000100	23710						
0,15,0,307	=00000100	28890						
0,16,0,333	=00000100	49410						
1,10,0,016	=00000100	54720						
1,13,0,274	=00000100	79650						
0,15,0,352	=00000110	39400						
0,12,0,163	=00000112	31890						
1,13,0,304	=00000136	80480						
0,16,0,332	=00000144	49360						
1,10,0,236	=00000146	64050						
1,10,0,263	=00000170	87460						
0,14,0,305	=00000176	22730						
1,10,0,264	=00000176	87910						
0,14,0,316	=00000200	23800						
0,15,0,311	=00000200	29040						
1,13,0,314	=00000200	81130						
0,11,0,355	=00000240	44960						
1,10,0,036	=00000252	56540						
1,11,0,027	=00000252	70610						
1,13,0,302	=00000262	80420						
1,13,0,271	=00000266	79420						
1,10,0,240	=00000300	64190						
1,10,0,244	=00000334	64510						
1,11,0,223	=00000360	75390						
1,13,0,310	=00000360	80680						
0,14,0,317	=00000400	23890						
0,15,0,313	=00000400	29190						
1,10,0,040	=00000400	56700						
1,11,0,211	=00000400	74470						
1,13,0,277	=00000406	80280						
1,13,0,323	=00000420	81710						
0,16,0,275	=00000500	49130						
1,11,0,020	=00000500	68310						
1,11,0,205	=00000512	72720						
1,10,0,233	=00000520	63630						
50510		50530	50730	50830	52450			
81830								
33840								
50420		50510						
81250		81690						
38450		39260						
87690								
52280								
23840								
36110								
81040		81760	81850					
73150								
32950								
79740		81950						
23930								
81180		81320	81410	81480				
32460								
87830								
23400								
36080								
81570								
63690		71650						
70660								
87230								
64940								
81690								
78130		78440						
49160		49220	49250					
68360								
73680								

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 40)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.10.0.035 =0000C524	56500				
1.13.0.301 =0000C330	80330				
1.10.0.234 =0000C0630	63890				
1.10.0.260 =0000C0630	85960				
0.17.0.334 =0000C0770	37020				
1.10.0.037 =0C000C776	56580				
0.14.0.420 =000001000	23980				
0.15.0.315 =0000C01000	29340				
0.05.0.004 =000001000	46480				
1.11.0.230 =000001000	78150				
1.10.0.232 =000001240	63630				
1.10.0.177 =000001252	59910				
1.10.0.235 =000001460	64020				
1.13.0.270 =00001622	79350				
0.14.0.262 =00001760	21290				
0.14.0.262 =0C0001760	23880				
1.10.0.230 =000001760	63460				
1.10.0.176 =00001774	59870				
0.15.0.317 =000002000	29490				
0.13.0.240 =000002000	31060				
0.05.0.254 =000002000	46530				
1.13.0.311 =000002000	81020				
0.12.0.166 =000002040	31950				
1.13.0.004 =000002200	79040				
0.15.0.367 =000002260	43600				
0.15.0.370 =000002400	43620				
0.15.0.366 =000002466	43420				
1.11.0.226 =000003416	77100				
1.10.0.214 =000003776	60800				
0.15.0.321 =000004000	29640				
0.16.0.347 =000004000	50940				
1.13.0.263 =000004000	79220				
1.16.0.052 =000005252	57280				
1.11.0.023 =000005252	69310				
1.11.0.225 =000005322	76390				
1.11.0.204 =000005512	72660				
1.11.0.203 =000005546	72600				
1.11.0.022 =000005752	69120				
1.11.0.021 =000005776	68930				
0.14.0.236 =000010000	16960				
0.15.0.323 =000010000	29790				
1.13.0.265 =000010000	79260				
1.13.0.265 =000010000	81230				
0.05.0.007 =000012000	46130				
1.11.0.004 =000012000	65630				
1.11.0.224 =000012070	75830				
1.11.0.135 =000012240	72240				
1.11.0.201 =000012264	73380				
1.11.0.005 =000012500	65820				
1.10.0.051 =000012524	57240				
1.11.0.006 =000012524	66010				
1.11.0.011 =000012764	66460				
0.05.0.251 =000013000	46230				
1.11.0.227 =000014744	77610				
1.11.0.202 =000017264	72360				
59950	63490				
86020	86480	86570			
46480					
78150					
63630					
59910					
64020					
79350					
21290					
23880					
63460					
59870					
29490					
31060					
46530					
81020					
31950					
79040					
43600					
43620					
43420					
77100					
60800					
29640					
50940					
79220					
57280					
69310					
76390					
72660					
72600					
69120					
68930					
16960					
29790					
79260					
81230					
46130					
65630					
75830					
72240					
73380					
65820					
57240					
66010					
66460					
46230					
77610					
72360					
23430	23090				
64010	24050				
64010	63420				
81460					
30320	30880				
69440	69590	7030C			
73740					
73800					
69170					
68980					
17310					
30170					
79390					
81370					
46190					
65680					
73440					
73380					
65870					
66150					
66510					
47520					
73320					
23430	23520	23610	23700	23790	
64010	64180				
7030C	70450	71790			
6980C					
6999C	73860				
7971C	79790	80720	80790	81090	
81670	81810	81930	81990		
4638C	46400	47970			
73500					
68170					
67670	67960				
67530					
66300					
67480					
47950					
78090					

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 41)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.11,0.012 =000017764	66650	67290	67340	72420	73260		
1.10,0.053 =000017776	57320						
1.11,0.013 =000017776	66840	67130	68620	68770	70130	72480	73070
1.11,0.013 =000017776	73920						
0.14,0.235 =000020000	16820	19290	19500				
0.15,0.325 =000020000	29940	30820					
0.12,0.204 =000020000	34070						
1.10,0.004 =000020000	53490						
1.11,0.213 =000020000	74640						
1.13,0.306 =000021000	80560						
1.13,0.305 =000022000	80500						
0.05,0.011 =000024000	66160						
1.13,0.303 =000024000	80440						
0.05,0.261 =000025000	47080						
1.11,0.221 =000025234	75180						
0.15,0.377 =000026202	44450						
1.13,0.300 =000030000	80300						
0.16,0.335 =000037740	49830						
0.16,0.336 =000037776	49970						
0.14,0.234 =000040000	16680	17610	19220				
0.15,0.324 =000040000	29870	30790					
1.10,0.225 =000040000	62860						
1.11,0.212 =000040000	74610	75780	76370	77080	77590	78070	78870
1.11,0.212 =000040000							
0.15,0.374 =000054602	44400						
0.15,0.333 =000070000	36940						
0.14,0.233 =000100000	16540	18940	19150	19430			
0.15,0.322 =000100000	29720	30760					
0.05,0.253 =000100000	46410						
1.10,0.224 =000100000	62780						
1.11,0.220 =000100000	75060	75220	75850	76350	76410	77050	77120
1.11,0.220 =000100000	77570	77630	78110	78850			
0.15,0.373 =000131002	44350						
1.10,0.003 =000152204	53470						
0.14,0.232 =000200000	16400	17470	18800	19080			
0.15,0.320 =000200000	29570						
0.05,0.250 =000200000	46200						
1.10,0.223 =000200000	62700						
0.14,0.345 =000201000	25810						
1.11,0.014 =000340000	67830	71160					
1.11,0.007 =000340064	67000						
1.11,0.024 =000340126	69470						
0.14,0.231 =000400000	16260	17240	18660	19010			
0.15,0.316 =000400000	29420						
1.10,0.222 =000400000	62260	62400	62470				
0.14,0.343 =000404400	25710						
0.14,0.230 =001000000	16120						
0.15,0.314 =001000000	29270	17100	18520	18870	26680		
1.10,0.221 =001000000	61780						
0.14,0.341 =001010200	25610	61920	61990				
0.15,0.356 =001020000	39890						
1.11,0.036 =001100000	72080						
1.11,0.035 =001100002	72020						
1.11,0.207 =001100010	73100						
1.10,0.021 =001240000	56090						

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 42)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.10.0.022 =001250000	56260			
1.11.0.025 =001500000	69500	70360		
1.11.0.001 =001500016	68350	68650		
1.11.0.031 =001500176	71130			
1.10.0.174 =001770000	59710			
1.10.0.213 =001774006	60720			
1.14.0.227 =002600000	15980	18380	18730	26610
1.15.0.312 =002600000	29120	30640		
1.10.0.017 =002600000	54780	61590		
1.10.0.015 =002600002	54700	55000		
0.13.0.230 =002610042	11980			
0.14.0.337 =002620100	25510			
1.10.0.020 =002620000	56050	56720		
1.13.0.231 =002525252	12070			
1.11.0.002 =002640000	65480	66710		
1.11.0.026 =002640016	70330			
1.11.0.015 =002640064	67020	67650		
1.10.0.023 =003770000	56300	59680		
0.14.0.226 =004000000	15840	16190		
1.15.0.310 =004000000	28970	30610	18240	18590
1.10.0.247 =004000000	65150			
1.13.0.210 =004020102	10430			
0.15.0.336 =004040000	25400	25430		
0.13.0.226 =004040004	11690			
0.15.0.335 =004000000	37150			
0.15.0.357 =005120000	39970			
0.07.0.260 =005000000	47020			
0.14.0.302 =007000000	22530	22610		
0.12.0.331 =007000000	36630			
1.10.0.210 =007000000	60370			
1.10.0.173 =007777740	59550			
1.10.0.207 =007777776	60340			
0.14.0.225 =010000000	15700	16050	18100	18450
0.15.0.306 =010000000	28620	30580		
0.11.0.364 =010000000	45400			
0.05.0.267 =010000000	48000			
1.10.0.217 =010000000	61130	61200	18450	20470
0.14.0.335 =010000000	25310	64740		
0.13.0.206 =010101012	10340			
0.14.0.301 =010220000	22390			
0.13.0.224 =010504102	11800			
0.14.0.340 =012020000	25540			
0.05.0.257 =016000000	46890			
1.10.0.152 =017600000	59020			
1.10.0.172 =017700000	59620			
0.14.0.224 =020000000	15260	15920	18310	26470
0.15.0.304 =020000000	28070	17960		
0.13.0.242 =020000000	51110	30550		
0.05.0.263 =020000000	47180			
0.16.0.356 =020000000	51450			
0.14.0.333 =020000040	25220			
0.13.0.204 =020410206	10250			
0.14.0.342 =021010000	25640			
0.13.0.222 =021042104	11710			
0.14.0.334 =024000000	25250			
1.10.0.202 =036000000	60190			

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 43)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.10,0.212 =036074170	60640				
1.10,0.201 =036077776	60160				
1.10,0.151 =037417036	58990				
1.10,0.171 =037750000	59590				
0.14,0.222 =040000000	15370	17820	18170	22820	26330
0.15,0.302 =040000000	28520				
0.16,0.357 =040000000	51550				
1.10,0.231 =040000000	63560				
0.14,0.331 =040000020	25130				
0.14,0.332 =042000000	25160				
0.13,0.202 =042104212	10160				
1.13,0.322 =044400000	81640				
0.13,0.166 =046453224	7030				
0.13,0.146 =050001240	3630				
0.11,0.365 =050001240	45680				
1.10,0.055 =052500000	57410				
0.13,0.220 =052525252	11150				
0.14,0.275 =056000000	22020				
0.14,0.300 =060000000	22320				
1.11,0.222 =060000000	75280				
0.12,0.206 =076000500	34360				
0.12,0.162 =070003100	31830				
1.10,0.262 =072000000	87110				
0.05,0.256 =074000000	46790				
0.14,0.277 =076000000	22210				
1.10,0.150 =077030000	58960				
1.10,0.175 =077774000	59740				
0.14,0.167 =100000000	15230	15630	17680	18030	20920
0.15,0.300 =100000000	28370	30420			26260
0.11,0.362 =100000000	45240	63760			
1.10,0.226 =100000000	62920				
1.11,0.210 =100000000	74430				
0.14,0.326 =106000010	24920				
0.14,0.346 =100200000	25840				
0.14,0.327 =101000000	24950				
0.13,0.162 =107301660	6430				
0.14,0.245 =110000000	20400				
0.15,0.365 =110000110	42500				
0.13,0.145 =110005110	3600	44320			
1.13,0.324 =111000000	81780				
0.13,0.167 =114722350	7040				
0.14,0.266 =120000000	21520				
0.13,0.236 =126000270	13500				
0.14,0.271 =120000270	21710				
0.12,0.164 =120000270	31910				
0.12,0.165 =120002670	31920				
0.15,0.330 =120016100	31770				
0.12,0.205 =120016100	34320				
0.13,0.143 =120020500	3540				
0.15,0.341 =122222222	38030	12900			
0.13,0.234 =123456702	12880				
0.14,0.273 =124010000	21780				
1.10,0.054 =125200000	57370				
1.10,0.060 =125202524	57610				
1.10,0.067 =125250000	58380				
0.13,0.217 =125252524	11060				

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 44)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.14.0.334	=130000000	22710
0.03.0.252	=130000000	46320
0.10.0.350	=130000000	50960
0.13.0.200	=130001410	9470
0.14.0.027	=130007000	14680
0.15.0.327	=130007000	31760
0.12.0.210	=130007000	35880
0.11.0.346	=130007000	44610
1.10.0.000	=130007000	53360
0.13.0.233	=130007430	12510
0.10.0.374	=130116010	12320
0.16.0.303	=132100000	22580
0.14.0.306	=137300000	22780
0.14.0.307	=137300000	22920
0.14.0.310	=137300000	23030
0.00.0.264	=140000000	47550
1.10.0.237	=140000000	64120
0.14.0.112	=140001020	14780
0.14.0.130	=140001040	24970
0.14.0.237	=140014430	19170
0.13.0.156	=140057610	5570
0.13.0.137	=140062210	3460
0.15.0.326	=140066210	30370
0.12.0.171	=140066210	32030
0.14.0.355	=140167620	27060
0.14.0.350	=140171230	26000
1.10.0.211	=146314630	60560
1.10.0.077	=147460000	58730
0.15.0.351	=150000300	38910
0.12.0.211	=150000310	35690
0.15.0.363	=150000310	40560
0.14.0.354	=150000460	27060
0.13.0.144	=150002710	3570
0.14.0.110	=150030260	14690
0.13.0.142	=150032660	3510
0.12.0.207	=150032660	34680
0.15.0.346	=150110110	38280
1.13.0.321	=153400000	81500
0.10.0.376	=160000360	42140
0.11.0.345	=160000360	42250
0.13.0.155	=160000560	5490
1.17.0.000	=160000760	12810
0.14.0.321	=160000560	24150
0.15.0.364	=160000560	40640
0.13.0.136	=160003760	3120
0.13.0.132	=160030160	2080
0.11.0.356	=160044760	44960
0.16.0.343	=160050260	50310
0.11.0.361	=160052760	45130
0.11.0.347	=160064760	44710
0.11.0.352	=160065160	44810
0.11.0.353	=160070360	44830
0.16.0.342	=160142300	50300
0.15.0.343	=160300000	38140
0.15.0.140	=170300000	37980
1.10.0.073	=171440000	58610

42490	8060	11180	13520
45670	5690		
22850			
23750			
33290	33580		
42170	5640		
5640			
45270			
44820	44890	45140	45320
44880	44950	45110	45200
44900	45060		
45050			
45040			
45150			

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 45)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.15.0.345	=174300000	38250						
1.10.0.147	=176050000	58930						
1.10.0.160	=177400000	59210						
1.10.0.056	=177700000	57450						
0.14.0.242	=177700000	20260						
1.10.0.170	=177700000	59530						
0.13.0.160	=200600000	6250						
0.14.0.223	=200000000	15440						
0.15.0.054	=200000000	28220						
0.12.0.177	=200000000	33080						
0.11.0.350	=200000000	44760						
1.10.0.220	=200000000	61350						
0.14.0.324	=200000004	24830						
0.14.0.325	=200400000	24860						
0.13.0.227	=201004220	11960						
0.13.0.225	=202702020	11870						
0.15.0.360	=203320000	40050						
0.13.0.221	=210421042	11690						
1.10.0.013	=212320000	54420						
0.13.0.223	=214102040	11780						
1.13.0.312	=222000000	81060						
0.15.0.342	=244444444	38110						
1.10.0.025	=252000000	56390						
1.10.0.042	=252400000	56810						
1.10.0.066	=252500000	58290						
1.10.0.057	=252505252	57550						
1.10.0.010	=252520000	54040						
1.10.0.045	=252524000	57030						
0.13.0.212	=252525200	10540						
0.13.0.176	=252525250	9360						
0.14.0.353	=252525250	26840						
0.13.0.165	=252525252	6780						
0.13.0.165	=252525252	9540						
0.14.0.351	=252525252	26750						
1.10.0.047	=252525252	57130						
0.13.0.161	=252642550	6420						
1.10.0.014	=253500000	54640						
0.13.0.174	=263026500	9080						
1.13.0.317	=266400000	81340						
1.10.0.243	=277777776	64380						
0.14.0.276	=300000000	22130						
0.14.0.264	=300000040	21420						
1.10.0.076	=317140000	58700						
0.13.0.173	=331033100	9070						
1.13.0.315	=333000000	81200						
0.13.0.163	=362144430	6440						
1.10.0.143	=363146314	58760						
1.10.0.164	=363770000	59360						
0.12.0.200	=371000000	33200						
1.10.0.154	=374170360	59080						
0.12.0.202	=377000000	33770						
1.10.0.157	=377001774	59180						
1.10.0.061	=377707776	57660						
0.14.0.741	=377770000	20160						
1.10.0.167	=377776000	59500						
211770	22200	22200	22010	22200	19640	23200	25930	26190
6260	9260	17540	17890	19640	23200	25930	26190	
30390	38200							
33630								
60130								
54090	54130	55100	58000	58060	58230	58410		
9650								
27010	7130	7200	8200	8210	8470	8550		
6790	10520	11040	11130	12050				
9630								
26880								
57880	58120	58160	58350	60100	60480			
64490	64650	65110						

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 46)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

0.13.0.171 =37777776	7860	7870					
0.13.0.153 =40000000	5190	6340					9180
0.13.0.153 =40000000	10090	11600				7790	
0.14.0.221 =40000000	15300	17340				23180	26120
0.14.0.221 =40000000							
0.12.0.176 =40000000	32000						
0.15.0.336 =40000000	37610						
0.16.0.352 =40000000	51170						
1.10.0.011 =40000000	24190	56920					
1.13.0.276 =40000000	79860						
0.14.0.322 =40000000	24740						
0.15.0.377 =40000004	43860						
0.15.0.371 =40000010	43740						
0.14.0.260 =40001000	21130						
0.14.0.237 =40003000	21070						
0.14.0.235 =40007000	21010						
0.14.0.235 =40017000	20950						
0.14.0.323 =40020000	24770						
0.14.0.254 =40037000	20880						
0.14.0.253 =40077000	20780						
0.14.0.222 =40177000	20710						
0.13.0.211 =40201020	10430						
0.14.0.251 =40377000	20640						
0.13.0.207 =40404000	10360						
0.14.0.250 =40770000	20570						
0.16.0.360 =41000000	52330	52860					
0.13.0.205 =41020410	10270						
0.15.0.337 =41111114	37950						
0.15.0.344 =41111114	38220						
0.14.0.247 =41777000	20500						
0.13.0.203 =42104210	10180						
0.14.0.246 =43777000	20430						
0.14.0.344 =46640000	25740						
0.14.0.270 =46600000	21660						
0.14.0.243 =47000000	20310	20330					
1.10.0.074 =47463000	58640						
1.10.0.166 =47760030	59420						
0.14.0.244 =47777000	20360						
0.13.0.152 =50000000	5110						
0.13.0.147 =50100400	3660						
1.13.0.003 =50100400	79020						
1.10.0.155 =501005010	59100						
1.10.0.227 =501006020	63300						
1.13.0.273 =501014260	79590						
1.10.0.063 =501034060	57740						
1.10.0.064 =501045410	57750						
1.10.0.215 =501047600	60920						
1.11.0.215 =501047600	74840						
1.13.0.272 =501047600	74540						
1.10.0.216 =501066420	61040						
0.14.0.274 =51000000	21900						
0.12.0.201 =51100000	33490						
1.10.0.250 =511006220	65170						
1.11.0.016 =511010030	67710						
1.11.0.032 =511010040	71830						
0.13.0.150 =511010050	3690						

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 47)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.10.0.001 =311010050	53370						
1.11.0.214 =311010050	74820						
1.11.0.017 =311054620	67990						
1.11.0.017 =311054620	70020						
1.10.0.024 =524000000	56350						
1.10.0.041 =525000000	56770						
1.10.0.200 =525200000	60070						
1.10.0.007 =525240000	53970	55220	58090				
1.10.0.044 =525250000	57910	57970					
1.13.0.213 =525252400	10630						
0.13.0.177 =525252520	9450						
0.13.0.164 =525252524	6700	7120	7210	8120	8130	8460	8560
0.13.0.164 =525252524	9340	9430	16610	10860	10950	12140	
0.14.0.352 =525252524	26780	26810	26960				
1.10.0.050 =525252524	57190	57840	58030	58440	60040	60440	
0.15.0.362 =525300000	40480						
0.13.0.151 =531020270	3720						
0.11.0.366 =531020270	45690						
0.05.0.266 =531020270	47990						
1.11.0.216 =531054270	74220						
1.10.0.245 =537777776	64680	64810	64920	65080			
0.14.0.265 =600000000	21470						
0.05.0.255 =600000000	46550						
0.14.0.267 =600010000	21550						
1.10.0.153 =607700000	59050						
0.05.0.265 =610000000	47650						
0.15.0.353 =612020000	39540	39620					
1.10.0.070 =631463146	58480	60520					
1.10.0.075 =636314630	58670						
1.10.0.161 =637700000	59270						
1.10.0.012 =652520000	54260						
0.13.0.215 =652525252	10880						
0.14.0.263 =660000176	21340						
1.10.0.241 =677777776	64330	64430	64540				
1.10.0.071 =714631462	58520						
1.10.0.162 =717740000	59300						
0.13.0.216 =725252524	10970						
0.15.0.361 =725300000	40290						
0.13.0.170 =731530654	7050						
0.13.0.175 =731773400	9090						
1.10.0.246 =737777776	64760	64860	64970				
0.05.0.262 =740000000	47100						
1.10.0.204 =741700000	60250						
1.10.0.144 =741703606	58800	60600					
1.10.0.203 =741777776	60220						
1.10.0.072 =746310000	58550						
1.10.0.163 =74760036	59330						
1.10.0.145 =760741702	58840						
0.13.0.235 =765432106	12970	12990					
1.10.0.206 =770000000	60310						
1.10.0.205 =77007776	60280						
1.10.0.146 =770360000	58870						
1.10.0.165 =77170000	59390						
0.15.0.332 =774300000	16690	36970	37050				
0.13.0.232 =775252524	12160						
1.10.0.026 =776000000	56430						

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 48)

LEFT HAND SYMBOLS AND THEIR POINTS OF REFERENCE

1.10.0.156 = 776003770	59130	60680							
1.10.0.043 = 777400000	56850								
0.16.0.537 = 777400000	50000								
0.16.0.534 = 77740036	49800								
1.10.0.006 = 777760000	53810	56130	57500						
0.14.0.240 = 777700000	20120								
1.10.0.046 = 777740000	57070	59460	60760						
0.13.0.201 = 77777770	9830								
0.13.0.172 = 777777774	8020								
0.13.0.157 = 777777776	5620	8030	8650	9740					
0.13.0.157 = 777777776	6880	7280	7290	5920	5990	6010	6080	6170	
0.13.0.157 = 777777776	8280	8300	8340	7300	7450	7540	7620	7630	
0.13.0.157 = 777777776	8750	8820	8630	8390	8480	8570	8640	8660	
0.13.0.157 = 777777776	11350	8820	8630	8980	9720	9810	11260	11280	
0.13.0.157 = 777777776	13340	11370	11620	13060	13150	13170	13240	13260	
0.14.0.111 = 777777776	14730								
0.15.0.037 = 777777776	28090	28260	28410	28560	28710	28860	29010	29160	
0.15.0.037 = 777777776	29310	29460	29610	29760	29910	30060	30210	30340	
0.15.0.037 = 777777776	53450		55890	55590	59770	60390	60990	64590	
1.10.0.002 = 777777776	65020								
1.11.0.000 = 777777776	65260	53710	55890	55590	59770	60390	60990		
		68600	70280						

Figure 7-14. PTC ADAPT Self-Test Program Symbolic Table (Sheet 49)

	MODULE 0	SFC/FUK	C
0	042742076003	151547566003	044750065003
		163550166003	350745466003
		163550166003	350123334003
		163550166003	36720026003
		163550166003	044740176003
10	161540226003	04676134003	163561412003
		357741530003	352101620003
		357741530003	367213200003
		357741530003	046747276003
		357741530003	16155316003
20	050747266003	163560412003	330742076003
		266107366003	336107456003
		266107366003	367221412003
		266107366003	050741256003
		266107366003	161540134003
30	052753476003	163540134003	330100134003
		330742266003	367205666003
		330742266003	052740134003
		330742266003	161545766003
		330742266003	054740134003
40	163540066003	154740134003	356100166003
		356100166003	367204266003
		356100166003	054740134003
		356100166003	161546366003
		356100166003	056740134003
50	163546466003	350740134003	352306566003
		352306566003	367200134003
		352306566003	060740134003
		352306566003	060740134003
		352306566003	060740134003
60	35275526003	350300134003	367205066003
		367205066003	060740134003
		367205066003	161545166003
		367205066003	163547030003
		367205066003	336747120003
70	33631360003	336113536003	367207430003
		367207430003	062756420003
		367207430003	161553416003
		367207430003	163545576003
		367207430003	330752630003
100	330305676003	367213130003	064745776003
		064745776003	161553430003
		064745776003	066746076003
		064745776003	163553730003
		064745776003	336746176003
110	367206276003	066754530003	161546376003
		161546376003	07075030003
		161546376003	330755330003
		161546376003	336306576003
		161546376003	367215630003
120	070746676003	161556130003	072741620003
		072741620003	163542076003
		072741620003	336745566003
		072741620003	367202076003
		072741620003	072745666003
130	16154520003	074742076003	163545766003
		163545766003	330753700003
		163545766003	330642076003
		163545766003	367206066003
		163545766003	074754200003
140	076740166003	163554300003	326742076003
		326742076003	326646266003
		326742076003	367214400003
		326742076003	076742076003
		326742076003	161546366003
150	163546076003	362746466003	362656000003
		362656000003	367202076003
		362656000003	161554700003
		362656000003	102742076003
		362656000003	163546666003
160	26675000003	266642076003	367208766003
		367208766003	102751000003
		367208766003	161553436003
		367208766003	104756730003
		367208766003	163563020003
170	364640036003	367207066003	371400136003
		367207066003	332007166003
		367207066003	10475336003
		367207066003	161557730003
		367207066003	106742640003
		367207066003	163540136003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 1 of 64)

	MODULE 0	SECTOR 0	
200	350747066003	350640236003	367207166003
200	106753336003	161560610003	110742640003
200	163540236003	163540236003	163540236003
210	352640336003	367207166003	110755436003
210	161562730003	112761620003	163542640003
210	336740336003	336740336003	336740336003
220	336100436003	367207166003	112755436003
220	161562710003	114777360003	163542640003
220	336763030003	336763030003	336763030003
230	336105576003	367223330003	114763410003
230	161541620003	116755600003	163540636003
230	352640736003	352640736003	352640736003
240	336107166003	367215736003	116764410003
240	161555500003	170747766003	163555436003
240	350665110003	350665110003	350665110003
250	336115500003	367213316003	120757350003
250	161540736003	122747066003	163541036003
250	364155436003	364155436003	364155436003
260	336107766003	367215736003	122747776003
260	161557350003	124741036003	163547066003
260	330147166003	330147166003	330147166003
270	336115436003	367215716003	124767410003
270	161557360003	126755704003	163557350003
270	336147066003	336147066003	336147066003
300	367201236003	126747166003	130755416003
300	16355704003	16355704003	16355704003
300	367207066003	367207066003	367207066003
310	130741336003	161547166003	132755736003
310	163553316003	163553316003	163553316003
310	266107066003	266107066003	266107066003
320	132747166003	161553336003	134755716003
320	163557350003	163557350003	163557350003
320	372107066003	372107066003	372107066003
330	134747166003	161556036003	136756016003
330	16357360003	16357360003	16357360003
330	136741636003	136741636003	136741636003
340	161547166003	140753336003	163555316003
340	004701636003	004701636003	004701636003
340	161547166003	161547166003	161547166003
350	142756136003	163556216003	350755304003
350	002717350003	002717350003	002717350003
350	142742036003	142742036003	142742036003
360	144755346003	16355304003	350757350003
360	004702036003	004702036003	004702036003
360	000013336001	000013336001	000013336001
370	000013304001	000017450001	000017420001
370	324762620003	444400060003	444400060003
370	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 2)

	MODULE 0	SECTUR 1	
0	0000000000	02000072000	24074010000
10	77274013400	47071640400	03362341000
20	03340023400	06471760400	03162341000
30	42670013400	00471720400	47067341000
40	24674023400	16156010400	16156010400
50	25074013400	16156341000	25274673600
60	25276341000	161544703600	25474706600
70	25474403400	16154403400	25674013400
100	25674716600	16156023600	26074043400
110	26074716600	16156043600	30274103400
120	13774716600	27162063600	13574203400
130	04174716600	42026103600	04700403400
140	31160716600	30721653600	05600403400
150	04174716600	17155643600	33140403400
160	05024716600	06025333600	07025013400
170	15026143600	16075023400	17026341000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 3)

MODULE 0 SECTOR 1

200	000010134001	000021504001	000023410001	000010236001	000007066001	000010336001	000007166001	000016436001
210	000010234001	000021604001	000023410001	000010336001	000007066001	000010436001	000007166001	000016536001
220	000010134001	000021704001	000023410001	000010436001	000007066001	000010536001	000007166001	000016636001
230	000010234001	000022004001	000023410001	000023520001	000015500001	000010536001	000007066001	000010636001
240	000007166001	000015736001	000010134001	000015704001	000023410001	000010636001	000007066001	000010736001
250	000007166001	000015736001	000010234001	000015704001	000023410001	000010736001	000007066001	000011036001
260	000007166001	000015436001	000010134001	000023410001	000011036001	000007066001	000011136001	000007166001
270	000015436001	000010234001	000023410001	000011136001	000007066001	000011236001	000007166001	000015336001
300	000014034001	000014034001	000014034001	000014034001	000010134001	000015704001	000023410001	000011236001
310	000007066001	000011336001	000007166001	000022136001	000010434001	000022232001	000023410001	000011336001
320	000007066001	000011436001	000007166001	000022336001	000011034001	000022432001	000023410001	000011436001
330	000007066001	000011536001	000007166001	000022536001	000012034001	000022632001	000023410001	000011536001
340	000007066001	000011536001	000007166001	000022736001	000014034001	000023032001	000023410001	000011636001
350	000007066001	000011736001	000007166001	000016536001	000014034001	000023104001	000023410001	000011736001
360	000007066001	000012036001	000007166001	000016436001	000014034001	000023204001	000023410001	000000260001
370	000000000000	000000000000	000000000000	000000000000	000000000000	470000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 4)

	MODULE 0		SECTUR 2					
0	00200000002	030177030003	020255412003	116775650003	167540236003	174247366003	330251136003	464640012003
10	735215412003	140275650003	12074036003	167547366003	202240312003	330255412003	446675650003	735200436003
20	030247366003	122742076003	167540412003	204255412003	330275650003	470640536003	735207366003	160240112003
30	124755412003	167556732003	212275650003	330242017003	356640636003	735207366003	040240212003	126755412003
40	167562132003	214275650003	330241012003	442640736003	735207366003	020240512003	130755412003	167562232003
50	222275650003	330242412003	444641036003	735207366003	050240612003	132755412003	167562332003	224275650003
60	330241412003	446641136003	735207366003	030240712003	134755412003	167575650003	232241236003	330247366003
70	450641112003	735215412003	060262432003	136775650003	167543012003	234241336003	330247366003	356641212003
100	735215412003	040256732003	140775650003	167542012003	242241436003	330247366003	452641512003	735215412003
110	070262532003	142775650003	167543412003	244241536003	330247366003	444641612003	735215412003	050262232003
120	144775650003	167542412003	252241636003	330247366003	454642112003	735215412003	100262632003	146775650003
130	167544012003	254241736003	330247366003	450642212003	735215412003	060262432003	150775650003	167543012003
140	262242036003	330247366003	456642512003	735215412003	110262732003	152775650003	167544412003	264242136003
150	330247366003	452642612003	735215412003	070262532003	154775650003	167543412003	272242236003	330247366003
160	460643112003	735215412003	120263032003	156775650003	167545012003	274242336003	330247366003	454643212003
170	735215412003	100262632003	160775650003	167544012003	302242436003	330247366003	462643512003	735215412003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 5)

MODULE 0 SECTOR 2

200	130263132003	162775650003	167545412003	304242536003	330247366003	456643612003	735215412003	110262732003
210	164775650003	167544412003	312242636003	330247366003	464644112003	735215412003	140263232003	166775650003
220	167546012003	314243136003	330247366003	460644212003	735215412003	120263032003	170775650003	167545012003
230	322243236003	330247366003	466644512003	735215412003	150263332003	172775650003	167546412003	324243336003
240	330247366003	462644612003	735215412003	130263132003	174775650003	167545412003	334243436003	330247366003
250	464645112003	735215412003	140263432003	176775650003	167547012003	344243536003	330247366003	466645212003
260	735215412003	150263232003	200775650003	167546012003	354243636003	330247366003	470645512003	735215412003
270	160263532003	202775650003	167547412003	364243736003	330247366003	472645612003	735215412003	170263332003
300	204775650003	167546412003	374244036003	330247366003	474646112003	735215412003	200263632003	206775650003
310	167550012003	404244136003	330247366003	466646212003	735215412003	150263432003	210775650003	167547012003
320	414244236003	330247366003	472646512003	735215412003	170263032003	212775650003	167545012003	424244336003
330	330247366003	442646612003	735215412003	020263532003	214775650003	167547412003	434244436003	330247366003
340	446647112003	735215412003	030263132003	216775650003	167545412003	332244536003	342247366003	352247212003
350	362255412003	312263632003	735235650003	330250012003	735204636003	476CC7366003	777547512003	175555412003
360	777762132003	163575650003	167740260003	161540000002	041740000002	167540000002	047000000002	175740000002
370	055000000002	000000000000	000000000000	000000000000	000000000000	410000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 6)

	MODULE 0	SECTOR 3											
0	0000000000	040025040003	306740000002	167540000002	040240000002	050240000002	100240000002	110240000002					
10	044240000002	574740000002	260240000002	564740000002	420240000002	041740000002	420240000002	330277666003					
20	504312136004	576647066003	613212236003	310747166003	167577676003	020242572003	030243010003	040254000003					
30	050242640003	060261434003	100251336003	110247366003	60740212003	270240612003	564741212003	420241612003					
40	041742212003	420242612003	330243212003	602643612003	613204212003	312744612003	167545212003	070245612003					
50	140246212003	170246612003	064247212003	074240012003	104255412003	041764032003	300270550003	310241012003					
60	330255412003	604664132003	613230550003	314751436003	167547366003	041742076003	320241412003	613230550003					
70	33025136003	604647366003	613215412003	316764232003	167570550003	124251636003	141747366003	207600212003					
100	606764336003	450242012003	231424332003	610770550003	340255412003	612764432003	420270550003	041751736003					
110	420247366003	330264536003	614642412003	613215412003	320764632003	167570550003	444752036003	350247366003					
120	330262536003	614643012003	613215412003	322764732003	167570550003	144252136003	360247366003	330242076003					
130	616643412003	613215412003	324765032003	167570550003	154252236003	164247366003	041742076003	370244012003					
140	542755412003	400265132003	330270550003	620652336003	613207366003	326742076003	167544412003	041755412003					
150	430265232003	544330550003	613212436003	330747366003	167542076003	041745012003	410255412003	613225332003					
160	332770550003	167552536003	442747366003	440242076003	446645412003	613230550003	334752636003	167547366003					
170	330255412003	620665432003	613230550003	336752736003	167547366003	040256736003	060246012003	070255412003					

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 7)

	MODULE 0	SECTOR 3	
200	100265532003	11027055C003	120253036003
			140247366003
			150246412003
			160255412003
			170265632003
			200270550003
210	612753136003	420507366003	430247012003
			544315412003
			613225732003
			340770550003
			167553236003
			622747366003
220	420247412003	430255412003	544326032003
			624670550003
			613213336003
			342747366003
			167550012003
			564755412003
230	420262132003	430270550003	544313436003
			626647366003
			613202076003
			344761012003
			167570550003
			630766136003
240	420261412003	430266214003	544330550003
			632653536003
			613207366003
			346766336003
			167551012003
			624755412003
250	420262132003	430270550003	544313636003
			634647366003
			613200612003
			350766436003
			167561412003
			626766214003
260	420270550003	430255412003	544326532003
			636670550003
			613213736003
			352747366003
			167547212003
			632766636003
270	420250412003	430255412003	544326732003
			640670550003
			613205776003
			354770230003
			167541012003
			041741412003
300	420250012003	430244560003	544314036003
			613207366003
			633401212003
			175567036003
			360752012003
			163545576003
310	226771230003	16157132C003	047027100003
			175767236003
			642021012003
			360742076003
			167561012003
			047015412003
320	041764214003	450267332003	743230550003
			362754136003
			167547366003
			330241012003
			743202012003
			364743012003
330	167544012003	644745012003	450250012003
			330241612003
			646667436003
			743212412003
			366767432003
			167570550003
340	020254236003	140247366003	650767236003
			450261012003
			330242076003
			652661012003
			743215412003
			370764214003
350	167567532003	030270550003	130240260003
			654740000002
			450240000002
			330240000002
			656640000002
			743200000002
360	660000000002	777540000002	175540000002
			167740000002
			161540000002
			777740000002
			163540000002
			047000000002
370	175740000002	055000000002	000000000000
			000000000000
			404000000000
			000001000001
			000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 8)

	MODULE 0										SECTOR 4									
0	0000000000	050001450003	275757536003	340247366003	041742012003	000545012003	205573136003	002562412003												
10	467415412003	041773232003	203553710003	004557636003	002747366003	010342412003	002544412003	430273336003												
20	065322412003	037215412003	360273432003	012753710003	201557736003	041047366003	201743012003	065104012003												
30	051233336003	470062412003	472055412003	474073532003	476053710003	500060036003	502047366003	504043412003												
40	506046412003	510073636003	014762412003	201555412003	041073632003	201753710003	065105320003	107200000002												
50	512040000002	514040000002	002740100003	016120136003	203607366003	002744012003	022107012003	207633736003												
60	145222412003	016755412003	520674032003	773053710003	002760236003	522107366003	223604412003	175547412003												
70	016103412003	247634136003	771062412003	430255412003	065334232003	167213710003	524760336003	340247366003												
100	267403012003	002745012003	147410012003	002774336003	016122412003	217215412003	016774432003	526653710003												
110	147420436003	771047366003	430241012003	065302412003	225205412003	002774536003	010362412003	100715412003												
120	100734632003	340253710003	267420536003	175747366003	530342012003	100706012003	100734736003	532662412003												
130	340255412003	771062332003	267413710003	430260636003	065307366003	267201412003	024054120003	004777766003												
140	075375000003	004560736003	410707366003	274740024003	075355412003	274570510003	412721036003	203747366003												
150	075340124003	203555412003	303122132003	335230510003	203561136003	467407366003	004741012003	534100224003												
160	267215412003	004562332003	771070510003	430261236003	065307366003	347201412003	00740424003	075355412003												
170	000556732003	536130510003	373621336003	443207366003	427402012003	000741024003	275315412003	413222232003												

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 9)

	MODULE 0	SECTOR	4
200	000770510003	004721436003	331647366003
		340242412003	267402024003
		340242412003	000755412003
		340242412003	540122432003
		340242412003	004730510003
210	323661536003	340247366003	267403012003
		002744024003	542115412003
		002744024003	267222532003
		002744024003	544770510003
		002744024003	340261636003
220	267407366003	041743412003	000550024003
		205755412003	075362632003
		205755412003	205570510003
		205755412003	546121736003
		205755412003	463207366003
230	205544012003	467420024003	555415412003
		775562732003	410730510003
		775562732003	532762036003
		775562732003	113307366003
		775562732003	205344412003
240	175540064003	512755412003	101323032003
		175670510003	512545012003
		175670510003	534777666003
		175670510003	113302076003
		175670510003	175547366003
250	274775136003	101323412003	175640112003
		274575232003	775030710003
		274575232003	534777666003
		274575232003	024075236003
		274575232003	066063412003
260	130040112003	172075332003	234070710003
		276077666003	340075136003
		276077666003	402040366003
		276077666003	002742076003
		276077666003	522123012003
270	615600364003	601235232003	550770710003
		340277666003	430275236003
		340277666003	065300366003
		340277666003	571202076003
		340277666003	615423012003
300	002740364003	542135332003	611230710003
		615402340003	552775400003
		615402340003	340277766003
		615402340003	350275500003
		615402340003	444077766003
310	041347666003	446077766003	041347166003
		450077676003	041347066003
		450077676003	452042340003
		450077676003	0413447676003
		450077676003	454042640003
320	041340000002	456040000002	041340000002
		460040000002	041340000002
		460040000002	462040000002
		460040000002	041340000002
		460040000002	464040000002
330	041340000002	466040000002	041340000002
		771040000002	430240000002
		771040000002	065300000002
		771040000002	671200000002
		771040000002	002740000002
340	522100000002	713600000002	016100000002
		023200000002	554000000002
		023200000002	556740000002
		023200000002	340240000002
		023200000002	023400000002
350	000000000000	000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
360	000000000000	000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
		000000000000	000000000000
370	000000000000	000000000000	000000000000
		000000000000	000000000000
		000000000000	402000000000
		000000000000	000000000000
		000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 10)

	MODULE 0	SECTOR 5	
0	0000C0C00003	000000000003	000001000001 000001000003 000000024003 000000020003 000012000003
10	160000060003	000024000003	141516170003 323536370003 52556570003 727576770003 132040530003 336021340003
20	745473000003	616263640003	714142430003 656667700003 444546470003 505122230003 242526270003 303112010003
30	020304050003	060710110003	111415160003 000000000003 173235360003 375255560003 577275760003 771320400003
40	533360210003	347454730003	006162630003 646566670003 707141420003 434445460003 475051220003 232425260003
50	273031120003	010203040003	050607100003 000000000003 101114150003 161732350003 363752550003 565772750003
60	767713200003	405333600003	213474540003 730061620003 636465660003 677071410003 424344450003 464750510003
70	222224250003	262730310003	120102030003 040506070003 000000000003 071011140003 151617320003 353637520003
100	555657720003	757677130003	204053330003 602134740003 547300610003 626364650003 666770710003 414243440003
110	454647500003	512223240003	252627300003 311201020003 030405060003 000000000003 060710110003 141516170003
120	323536370003	525556570003	727576770003 132040530003 336021340003 745473000003 616263640003 656667700003
130	714142430003	444546470003	505122230003 242526270003 303112010003 020304050003 000000000003 050607100003
140	111415160003	173235360003	375255560003 577275760003 771320400003 533360210003 347454730003 006162630003
150	646566670003	707141420003	434445460003 475051220003 232425260003 273031120003 010203040003 000000000003
160	040506070003	101114150003	161732350003 363752550003 565772750003 767713200003 405333600003 213474540003
170	730061620003	636465660003	677071410003 424344450003 464750510003 222324250003 262730310003 120102030003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 11)

MODULE 0 SECTOR 5

200	C00000000003	0J0405060003	071011140003	151617320003	353637520003	555657720003	757677130003	204053330003
210	602134740003	547300610003	626364650003	666770710003	414243440003	454647500003	512223240003	252627300003
220	311201020003	0000CC000003	012345670003	123456700003	234567012003	345670122003	456701234003	567012344003
230	670123456003	701234566003	012345670003	123456700003	514624230003	714565000003	100000000003	652765510003
240	637122650003	000104040003	030047510003	714523650003	510000000003	476167650003	004551000003	000000000003
250	002000000003	000013000003	130000000003	000100000003	000002000003	60CC00000003	074000000003	016000000003
260	006000000003	000025000003	740000000003	020000000003	140000000003	610000000003	531020270003	010000000003
270	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
300	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
310	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
320	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
330	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
340	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
350	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
360	C00000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 12)

	MODULE 0	SECTOR 6							
0	77757650003	044741736003	167547366003	777742036003	004640066003	101202136003	604740166003	204402236003	
10	610740266003	240402336003	614740366003	274402436003	620740466003	330402536003	624740566003	364402636003	
20	630740666003	420402736003	634740766003	454403036003	640741066003	510403136003	644741166003	544403236003	
30	650741266003	600403336003	652741366003	634403436003	646741466003	67C403536003	642741566003	724403636003	
40	777541666003	175543736003	777762412003	163551012003	036744036003	161540412003	175777766003	055007666003	
50	00003776001	000007466001	000007676001	000005432001	000004050001	000000036001	000007366001	0000003736001	
60	137740012003	133611012003	151227736003	656000412003	660037766003	424707666003	262777776003	167547466003	
70	264747676003	161570032003	344004050003	067740136003	000247366003	C41743736003	260240012003	203551012003	
100	346770136003	201540412003	350037766003	352007666003	000037776001	000007466001	000007676001	0000030232001	
110	00004050001	00000236001	000007366001	000003736001	000000012001	000011012001	0000030336001	0000000412001	
120	565437766003	771047666003	565437776003	275747466003	340247676003	360270432003	565404050003	041040336003	
130	041047366003	041043736003	710740012003	201551012003	356770536003	513400412003	771077766003	565407666003	
140	74077776003	340247466003	414707676003	510770632003	113304050003	175540436003	350747366003	101303736003	
150	175640012003	350551012003	434730736003	422740412003	201577766003	360247666003	71277776003	175547466003	
160	041047676003	041071032003	041044050003	350240536003	424047366003	414703736003	350740012003	075351012003	
170	350571136003	434700412003	175777766003	065107666003	175577776003	351207466003	771047676003	565431232003	

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 13)

	MODULE 0	SECTOR 6	
200	740744050003 340240636003 565407366003 201743736003 065100012003 201551012003 333231336003 360240412003		
210	041077766003 041047666003 041077766003 714747466003 201547676003 360771432003 513404050003 350240736003		
220	125047366003 041343736003 771040012003 565411012003 740771536003 340240412003 360277766003 565407666003		
230	041077766003 041047466003 041047676003 714771632003 201544050003 362741036003 513407366003 350243736003		
240	127040012003 041351012003 771071736003 045000412003 424077766003 775547666003 113337776003 175547466003		
250	414707676003 534772032003 101304050003 175641136003 534547366003 434703736003 702040012003 201751012003		
260	065132136003 201540412003 551237766003 775007666003 414737776003 534747666003 075347676003 534572232003		
270	434704050003 534401236003 775547366003 430243736003 065300012003 567211012003 7750322336003 000000412001		
300	C0C0J7766001 0C0C7666001 000037776001 00007466001 000007676001 000032432001 000004050001 000001336001		
310	00007366001 00003736001 000000012001 000011012001 000032536001 000000412001 000037766001 000007666001		
320	C0C0J7766001 00007466001 000007676001 000032436001 000004050001 00000436001 00C007366001 000003736001		
330	000000012001 000011012001 000032436001 000000412001 000037766001 000007666001 000037766001 000007466001		
340	000007676001 00003232001 000004050001 000001536001 000007366001 000003736001 000000012001 000011012001		
350	000032236001 000000412001 000037766001 000007666001 000037766001 000007466001 000007676001 000032132001		
360	000004050001 000003736001 000000012001 000011012001 000032600001 000006060001 000005436001 000004620001		
370	C000J0036001 000006420001 000000000000 000000000000 000000000000 40C4C0000003 000000000000 000000000000		

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 14)

	MODULE 0	SECTOR 7	
0	775540000002	354740000002	356100000002
			095200000002
			775000000002
			360740000002
			420740000002
			041740000002
10	420240000002	362000000002	211740000002
			240240000002
			171540000002
			266740000002
			167540000002
			330240000002
20	002640000002	731200000002	270740000002
			167540000002
			430740000002
			043300000002
			061700000002
			731400000002
30	272740000002	167540000002	360740000002
			420240000002
			041740000002
			420240000002
			047000000002
			330240000002
40	731200000002	274740000002	167540000002
			430240000002
			043300000002
			731200000002
			416700000002
			024740000002
50	075340000002	024540000002	040740000002
			075340000002
			040540000002
			424700000002
			203740000002
			065340000002
60	203540000002	201100000002	025200000002
			201740000002
			346100000002
			157200000002
			235400000002
			201740000002
70	364100000002	167200000002	325400000002
			201740000002
			366100000002
			177200000002
			561400000002
			201740000002
100	370100000002	611200000002	203540000002
			372740000002
			201540000002
			416700000002
			026740000002
			101300000002
110	103640000002	026540000002	424700000002
			276740000002
			167540000002
			025400000002
			300740000002
			167540000002
120	306740000002	161540000002	343740000002
			240240000002
			171540000002
			374640000002
			731200000002
130	302740000002	167540000002	430240000002
			043300000002
			731400000002
			304740000002
			167540000002
140	001400000002	330240000002	134640000002
			731200000002
			203540000002
			364740000002
			201540000002
			264740000002
150	161540000002	045400000002	310740000002
			167540000002
			306740000002
			161540000002
			211740000002
			240240000002
160	171540000002	330240000002	376640000002
			731200000002
			312740000002
			167540000002
			430240000002
			043300000002
170	365200000002	731400000002	314740000002
			167540000002
			001400000002
			330240000002
			400640000002
			731236600002

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 15)

MODULE 0 SECTOR 7

200	316740000002	167540000002	366740000002	420240000002	041740000002	426240000002	362000000002	430240000002
210	043330000002	731200000002	203540000002	320740000002	167540000002	366740000002	201540000002	416700000002
220	026740000002	101300000002	105640000002	026540000002	424700000002	401740000002	240240000002	171540000002
230	001400000002	330240000002	402640000002	731200000002	322740000002	167540000002	360740000002	420240000002
240	041740000002	420240000002	362000000002	411740000002	260240000002	171540000002	330240000002	376640000002
250	731200000002	324740000002	167540000002	430240000002	043300000002	537200000002	731400000002	326740000002
260	167540000002	001400000002	264740000002	161540000002	330240000002	404640000002	731200000002	045400000002
270	203540000002	264740000002	161540000002	370740000002	201540000002	416700000002	026740000002	101300000002
300	107640000002	026540000002	424700000002	025400000002	330740000002	167540000002	161540000002	406740000002
310	420240000002	430240000002	043300000002	633200000002	731400000002	332740000002	167540000002	330240000002
320	410640000002	731200000002	334740000002	167540000002	065740000002	420240000002	170240000002	330240000002
330	731200000002	336740000002	167540000002	430240000002	043300000002	677200000002	731400000002	340740000002
340	167540000002	041740000002	420240000002	430240000002	043300000002	731200000002	167540000002	171540000002
350	344000000002	412000000002	211740000002	002640000002	775540000002	414000000002	000000000000	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	400001000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 16)

	MODULE 0	SECTION 10	
200	742655412003	465233232003	226763250003
			161546436003
			047007066003
			330242340003
			465233402003
			230747466003
210	161555412003	576773232003	420263250003
			550246536003
			041747066003
			420242340003
			773042076003
			041377442003
220	330247466003	744655412003	465233532003
			232763250003
			161546636003
			047007066003
			33024276003
			465221012003
230	505421412003	746003254003	775563410003
			17756326003
			775746736003
			163547066003
			047002076003
			177761012003
240	750021412003	512643254003	775563250003
			775747036003
			207547066003
			420702340003
			760755412003
			175563250003
250	300742076003	774010166003	300561034003
			762772236003
			175544654003
			306747666003
			774030136003
			306544754003
260	42270762003	710770126003	175577336003
			574744654003
			712007666003
			574570436003
			420704754003
			502747672003
270	175570426003	030761534003	573416412003
			030547236003
			207007066003
			775547136003
			101307166003
			177573636003
300	175765012003	113304202003	177647466003
			775015412003
			230261632003
			424764050003
			426750176003
			430743656003
310	432750166003	434761034003	436770136003
			440743756003
			442770126003
			444770436003
			446743756003
			450770426003
320	452761534003	454742340003	456750176003
			460753744003
			462770110003
			464747336003
			466747066003
			470773702003
330	472742056003	474755412003	476774032003
			500763250003
			502747436003
			504747066003
			506742340003
			510774102003
340	512742056003	514755412003	516743472003
			520763250003
			522747536003
			524747066003
			526742340003
			530774202003
350	532742056003	534755412003	536774332003
			540763250003
			542747636003
			544747066003
			546742340003
			550745436003
360	552765012003	554774402003	556742056003
			560755412003
			562774532003
			564763250003
			566742340003
			611434600003
370	000010447001	000011632001	000004202001
			000021632001
			130116010003
			500000000003
			160000360003
			000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 17)

	MODULE 0	SECTGR 10	
0	7167766003	20194766003	211777676003 175547166003 175747676003 171547640003 340277666003 065741236003
10	420244054003	041747666003	420275236003 330244554003 512647672003 501201226003 203741336003 065344054003
20	203544472003	175741326003	275342036003 175544054003 420707666003 C30775336003 075344554003 030547672003
30	432702026003	047037640003	203756200003 201120700003 011206076003 201744130003 716104010003 115221000003
40	203561100003	720756136003	201547066003 325761534003 175545636003 011407166003 202764260003 161542076003
50	041757012003	171577542003	724756412003 420277542003 430250166003 065331136003 141210066003 465402340003
60	204770536003	161561012003	041761412003 420243254003 420243254003 065746610003 420245536003 726647066003
70	465202076003	206761012003	161570336003 167561012003 041761412003 420243254003 420243254003 756024060003
100	330245636003	726547066003	465205736003 210747166003 167542076003 430261012003 065321412003 465203254003
110	212763250003	161545736003	041747066003 167546036003 047007166003 330257012003 465210476003 214747466003
120	161577542003	360255412003	602751632003 420263250003 730746036003 420247066003 732772176003 420247166003
130	550242340003	330255412003	734664050003 465206236003 216747066003 161546136003 602747166003 420254520003
140	04105042003	330247466003	330247466003 736655412003 465211632003 220764050003 161550176003 041743256003 420250166003
150	773061034003	330254036003	740643766003 465214026003 222754336003 161543756003 047014326003 330261534003
160	465202340003	224750176003	161550044003 350254010003 065773102003 420247466003 720744136003 420247066003
170	550255412003	065773232003	420263250003 041746336003 420247066003 773042340003 041373302003 330247466003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 18)

	MODULE 0	SECTOR 11	
0	143746276003	0136C1230003	011213610003 656034600003 752023476003 550764476003 161565476003 552766676003
10	163570076003	065770776003	320274700003 255410720003 430261412003 560302154003 107201410003 167575036003
20	554753412003	310275136003	551410066003 430240436003 560335200003 107234700003 560775300003 320250720003
30	255435136003	430250066003	430250066003 107235200003 562774700003 300275300003 041750720003 310275436003
40	430250066003	56030636003	123235200003 775575536003 175575600003 775750720003 167575736003 175750066003
50	055000736003	551435200003	564774700003 310275300003 563410720003 566776036003 300250066003 570741036003
60	310275200003	575430676003	570776100003 300274700003 570775300003 310250720003 575435736003 556750066003
70	300241136003	564775200003	310261412003 563402154003 556747210003 310276236003 563413412003 564776336003
100	300275600003	310271776003	563411620003 556772076003 300251620003 041774700003 310253620003 563437666003
110	065761412003	320242154003	570751010003 310276436003 575413412003 566777640003 300277666003 041747666003
120	310276036003	575410066003	560761412003 320242154003 255412210003 267407676003 777552412003 754741034003
130	065107666003	261210076003	777003244003 572750066003 161552210003 574777640003 163546376003 430254230003
140	560314310003	107234600003	570776500003 310276600003 575400000002 065740000002 320240000002 756740000002
150	300240000002	760740000002	310240000002 730740000002 203540000002 607400000002 560740000002 320240000002
160	607400000002	560740000002	300240000002 041740000002 310240000002 607400000002 065740000002 320240000002
170	607400000002	762740000002	300240000002 041740000002 310240000002 607400000002 560740000002 320240000002

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 19)

MODULE 0 SECTOR 11

200	60740000002	76474000002	31024000002	60740000002	06574000002	32024000002	60740000002	60740000002	04374000002
210	31024000002	20374000002	06510000002	20354000002	33320000002	60740000002	56074000002	56074000002	32024000002
220	73074000002	20354000002	60740000002	56074000002	30024000002	31024000002	60740000002	60740000002	76474000002
230	30024000002	56074000002	31024000002	60740000002	76474000002	30024000002	31024000002	31024000002	60740000002
240	76474000002	30024000002	56074000002	31024000002	20374000002	06510000002	20354000002	20354000002	44520000002
250	60740000002	06574000002	32024000002	60740000002	07374000002	31024000002	54140000002	54140000002	76000000002
260	60740523603	75200706603	00000533601	00000716601	77554207603	76675016603	06513473603	06513473603	55521006603
270	77501367603	77554766603	77074767603	06510746603	567216012003	775015412003	775562632003	775562632003	776774310003
300	06511017603	60120325603	77501016603	77554327603	430261012003	56030207603	611221012003	611221012003	775007676003
310	00001365601	00000766601	000021134001	000027636001	000003756001	000027626001	000021534001	000021534001	000002340001
320	00001017601	000010044001	000027210001	000010076001	000034704001	000033410001	000010166001	000010166001	000035036001
330	00001006601	000011576001	000007666001	000027220001	000010036001	000007066001	000007736001	000007736001	000007166001
340	00000207601	000010166001	000035100001	000002640001	000022632001	160000360003	130007000003	130007000003	160064760003
350	20000000003	00000020003	160065160003	160070360003	000000024003	000000240003	160044760003	160044760003	000000016003
360	000000014003	160052760003	100000000003	000000006003	010000000003	050001240003	531020270003	531020270003	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	400200000003	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 20)

	MODULE 0	SECTOR 12	
0	000037100001	1710C0000003	061000000003 070000000003 1210000C0003 1300C0C00003 020000000003 031000000003
10	111000C00003	10C000000003	174000000003 064000000003 075000000003 124C00000003 135000000003 025000000003
20	034000000003	1140C0000003	105000000003 062000000003 073000000003 122C00000003 133C00000003 023000000003
30	032000000003	1120C0000003	103000000003 177000000003 067000000003 0760C0000003 127000000003 136000000003
40	0260C0000003	037CC0000003	117000000003 106000000003 016C00C00003 0070C0000003 163000C00003 172000000003
50	002000C00003	145000000003	004000000003 160000000003 001000000003 000010000003 517000000003 106000000003
60	016000000003	007CC0000003	032000000003 112000000003 103000000003 1630C0C00003 002000000003 034000000003
70	1140C0000003	1050C0000003	165000000003 004000000003 031000000003 111000000003 100000000003 160000000003
100	0010C0000003	177CC0000003	067000000003 076000000003 127000000003 136C00C00003 02600C000003 037000000003
110	016000C00003	1770C0000003	067000000003 076000000003 1270000C0003 136000000003 026000000003 037000000003
120	117000000003	106000000003	016000000003 000010000003 000400000003 000200000003 000100000003
130	000040000003	150032660003	120002670003 120005270003 120011270003 120014270003 120020670003 120041270003
140	120047270003	1200427C003	120047270003 120015100003 120065270003 12007227C003 120075270003 120100270003
150	120105270003	12011627C003	120124670003 120127670003 120142270003 120146670003 120151270003 120154670003
160	120157670003	120020500003	070003100003 000000132003 120000270003 120002670003 000002040003 000000002003
170	000000004003	140066210003	000000046003 000000020003 000000024003 000000014003 400000000003 200000000003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 21)

MODULE 0 SECTOR 12

```

200 371000000003 511000000003 377000000003 00000010003 000020000003 12C01610C003 .07000500003 150032660003
210 1300C7C00003 150000310003 000000000000 000000000000 000000000000 000000000000 0C0000000000 000000000000
220 C0CC00000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
230 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
240 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
250 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
260 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
270 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
300 C0CC00000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
310 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
320 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
330 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
340 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
350 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
360 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
370 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 4001000000003 000000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 22)

	MODULE 0	SECTOR 13	
0	13007400003	13007740003	13010300003
			13010700003
			13011400003
			13011640003
10	13013200003	13013700003	13014640003
			13015240003
			13015640003
			13016200003
20	13017140003	13000200003	13000360003
			13000720003
			13001320003
			13001660003
30	13003160003	13003560003	13004120003
			13004460003
			13005020003
			13005360003
40	13006620003	13007160003	13010160003
			13010520003
			13011120003
			13011520003
50	13012520003	13013120003	13013520003
			13014060003
			13014420003
			13015020003
60	13016320003	13016720003	13000141003
			13000541003
			13001141003
			13001541003
70	13003041003	13003641003	13004241003
			13004641003
			13005241003
			13005641003
100	13007201003	13007541003	13010141003
			13010541003
			13011141003
			13011641003
110	13013201003	13013541003	13014741003
			13015341003
			13015741003
			13016341003
120	13000121003	13000743003	13002021003
			13002421003
			13003021003
130	13004421003	01000101003	00000000003
			00000000003
140	57116537003	14005761003	15003266003
			12002050003
			11000511003
			05000124003
150	51101005003	53102027003	50000000003
			40000000003
			16000560003
			14005761003
160	20000000003	25264255003	10730166003
			36214443003
			525252524003
			252525252003
170	731530654003	37777777603	77777774003
			33103310003
			26502650003
			7337340003
			25252525003
			52525252003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 23)

MODULE 0 SECTOR 13

200	130001410003	777777770003	042104212003	421042120003	020410206003	410204140003	010101012003	404040500003
210	004020102003	402010200003	252525200003	525252400003	000000004003	652525252003	725252524003	125252524003
220	052525252003	210421042003	021042104003	214102040003	010604102003	202020200003	004040404003	201004220003
230	002010042003	002525252003	775252524003	130007430003	123456702003	765432106003	120000270003	000000000003
240	000020000003	000000000003	020000000003	000000000003	000000076003	000000000000	000000000000	000000000000
250	000000000003	400000000003	200000000003	100000000003	040000000003	020000000003	010000000003	004000000003
260	002000000003	001000000003	000400000003	000200000003	000100000003	000040000003	000020000003	000010000003
270	000040000003	000020000003	000001000003	000000400003	000000200003	000000100003	000000040003	000000020003
300	000000100003	000000004003	000000002003	000000000000	000000000000	000000000000	000000000000	000000000000
310	000037766001	000023726001	000024036001	000007566001	000022012001	000024126001	000024214001	000032410001
320	000010412001	000011012001	000023736001	000037740001	000035336001	00004654001	000024326001	000035036001
330	00004754001	000024332001	000035026001	000024136001	000010134001	00004654001	000024326001	000035136001
340	00004754001	000024332001	000035126001	000024136001	000024414001	00002034001	000035016001	000035026001
350	000025036001	000000012001	000032020001	000025036001	000000000000	000000000000	000000000000	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 24)

	MODULE 0	SECTOR 14	
0	14006221C003	140001C2C003	140002070003
10	140024420003	140030020003	140033020003
20	140057420003	140063020003	140066420003
30	000037300001	140110020003	140113420003
40	140140420003	140144020003	140147420003
50	14004620003	140010220003	140013620003
60	140040620003	140044220003	140047620003
70	140074620003	14010220003	140103620003
100	140130620003	140134220003	140137620003
110	150030260003	77777776003	140001070003
120	140047030003	140052430003	140056030003
130	140101030003	140104030003	140107030003
140	140141030003	140151430003	140160030003
150	140046230003	140051630003	140055230003
160	140106630003	140112630003	140116630003
170	140146630003	140151630003	140157630003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 25)

MODULE 0 SECTOR 14

200 140016440003 140025440003 140032040003 140037040003 140044040003 140051040003 140055440003 140060440003
210 140063040003 140066040003 140071440003 140075040003 1401C0440003 140104040003 140107440003 140113040003
220 140116440003 400000000003 040000000003 200000000003 000000000003 010000000003 004000000003 002000000003
230 001000000003 004000000003 000200000003 000100000003 000040000003 000020000003 000010000003 140014430003
240 77777C000003 37777C000003 177770000003 470000000003 477770000003 110000000003 437770000003 417770000003
250 40777C000003 403770000003 401770000003 400770000003 400370000003 400170000003 400070000003 400030000003
260 400100000003 000000000003 000001760003 660000176003 300000040003 600000000003 120000000003 600010000003
270 460000000003 12000270003 000000004003 175010000003 510000000003 656000000003 300000000003 076000000003
300 060000000003 010220000003 007000000003 132100000003 130000000003 137300000003 137340000003
310 137370000003 00000002003 000000000003 000000040003 00000010003 000000200003 00000400003
320 00001000003 16000560003 400000002003 400200000003 20000004003 200400000003 10000010003 101000000003
330 140001040003 04000020003 042000000003 020000040003 024000000003 0100000003 004040000003 002020100003
340 012020000003 00101020003 021010000003 000404400003 440400000003 000200000003 100000000003 000002000003
350 140171230003 25252522003 525252524003 252525250003 150000460003 14016762003 000000000003 000000000003
360 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003
370 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 26)

	MODULE 0		SECTOR 15						
0	150023060003	150032060003	150041060003	150050060003	150066060003	150075060003	150084060003	150093060003	150102060003
10	150113060003	150122060003	150131060003	150140060003	150147060003	150156060003	150165060003	150174060003	150183060003
20	150173060003	150174060003	150002600003	150004260003	150005260003	150006260003	150007260003	150008260003	150009260003
30	15011260003	150012260003	150013260003	150014260003	150015260003	150016260003	150017260003	150018260003	150019260003
40	00000002003	150072100003	000000000003	111111112003	222222222003	333333332003	444444444003	555555554003	666666666003
50	666666666003	777777774003	150147510003	150140110003	200000000003	150033100003	150040100003	15004700003	150054000003
60	150052100003	150062500003	150070100003	150075500003	150101500003	150105500003	150112100003	150116100003	15012100003
70	150121500003	150143100003	150150500003	150152500003	150156100003	150162100003	150166100003	1501700003	150173000003
100	15014700003	150023300003	150030300003	150034700003	150041700003	150044300003	150047700003	150050700003	150053300003
110	150062300003	150066300003	150070700003	150101300003	150103700003	150111700003	150117000003	150123000003	150129000003
120	634300000003	644300000003	654300000003	664300000003	674300000003	704300000003	714300000003	744300000003	754300000003
130	424300000003	434300000003	444300000003	454300000003	464300000003	474300000003	504300000003	514300000003	544300000003
140	224300000003	234300000003	244300000003	254300000003	264300000003	274300000003	304300000003	310300000003	340300000003
150	014300000003	024300000003	034300000003	044300000003	054300000003	064300000003	074300000003	104300000003	114300000003
160	114300000003	124300000003	134300000003	204300000003	214300000003	334300000003	404300000003	534300000003	644300000003
170	604300000003	734300000003	004300000003	144300000003	154300000003	164300000003	174300000003	204300000003	214300000003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 27)

MODULE 0 SECTOR 15

200	344300C00003	3543C000C003	364300000003	374300000003	524300000003	544300000003	554300000003	564300000003
210	5743C0C00003	724300000003	744300000003	754300000003	764300000003	7743C0C00003	124300000003	130300000003
220	120300C00003	1343C0000003	160300000003	174300000003	164300000003	170300000003	012100000003	022100000003
230	0361C0000003	0421C0000003	056100000003	066100000003	072100000003	102100000003	116100000003	126100000003
240	132100C00003	1461C0000003	416100000003	426100000003	432100000003	612100000003	622100000003	636100000003
250	642100000003	6561C0000003	666100000003	672100000003	702100000003	716100000003	726100000003	732100000003
260	7461C0000003	216100000003	226100000003	232100000003	150002710003	110000110003	4C0003774003	400001774003
270	000C0C004003	000C03774003	000001774003	00000776003	400000776003	150051310003	150061310003	000000004003
300	100000000003	00000010003	040000000003	00000020003	0200000C0003	00000040003	010000000003	000001000003
310	004000000003	00000200003	002000000003	00000400003	001000000003	000010000003	000400000003	000020000003
320	000200000003	000040000003	000100000003	000010000003	000040000003	000200000003	140066210003	130007000003
330	120016100003	0077C0000003	774300000003	000077000003	000000770003	0047C00C0003	400000000003	411111114003
340	170300C00003	122222222C03	2444444444003	160300000003	4111111140003	1743000C0003	15013011C003	000000030003
350	00000006003	150000300003	000000110003	612020000003	000000014003	00000016003	001020000003	005320000003
360	205320C00003	725300000003	525300000003	150000310003	160000560003	11C000110003	000002466003	000002260003
370	000002400003	400C0010003	400000004003	000131002003	000054402003	400010000003	000037400001	000026202003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 28)

	MODULE 0		SECTOR 16					
0	77557760003	67C324012003	177561426003	175747076003	672321326003	177647276003	775021226003	123747376003
10	027621526003	7040C7476003	706021626003	440245276003	025602010003	323407276003	220761026003	175545276003
20	102743256003	051CC5266003	102561104003	422742610003	223403376003	71C767426003	201547276003	316761032003
30	324403310003	323405276003	341405366003	422767436003	203545430003	422740736003	223427516003	712740226003
40	177540436003	424767516003	253400426003	102740636003	075367516003	102540626003	177741036003	065127516003
50	177541C26003	1032C1236003	323427516003	341401226003	203745076003	065105736003	203547140003	073207040003
60	422754436003	2234C7666003	714747036003	201540660003	320747026003	324433236003	125750066003	253402076003
70	323421226003	3414C7C36003	422773316003	223407026003	714750076003	201543244003	322750066003	324406710003
100	127747266003	2534C5266003	323427426003	341405366003	430761012003	716314236003	027207666003	720000236003
110	42474CC60003	775540226003	72254336003	430247666003	043300436003	227200660003	724740426003	270254436003
120	72274766003	0651C0636003	722540060003	227200626003	775014536003	775547666003	702541036003	775740060003
130	207541026003	726754636003	730547666003	430241236003	043300060003	267201226003	702742240003	260240000002
140	0107C0000002	702540000002	730761476003	065121326003	730561226003	267221526003	732761626003	223427636003
150	207C31436003	775572336003	430277666003	043333614003	3252C7666003	734756336003	270273714003	775007672003
160	775556326003	430274036003	043307766003	343234136003	736747666003	270261412003	775002154003	574056510003
170	63004766003	646052012003	000004034001	000007666001	00000776001	000003244001	00000776001	000016510001

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 29)

MODULE 0 SECTION 16

```

200 C0CC16336C01 C0CC0C3756001 000016326001 000010076001 000003244C01 C0CC1C666C01 0C0016110001 000037640001
210 00CC0C0CC0C03 0C0C0024C03 000000000003 000000000003 000000000003 C0CC0C0C0C03 0C0C0C0C0C03 C00000000003
220 C00000000003 C0C0C0C0C0C03 000000000003 000000000003 00CC00000003 C0CC0C0C0C03 0C0C0C0C0C03 C00000000003
230 00CCCC000003 C0CC0C0C0C03 000000000003 000000000003 000000000003 00CC0C0C0C03 0C0C0C0C0C03 000000000003
240 C0CC0C0C0C03 0C0C0C0C0C03 000000000003 000000000003 0C0C0C0C0C03 C0CC0C0C0C03 000000000003 000000000003
250 00CCCC000003 0C0C0C0C0C03 000000000003 000000000003 0C0000000003 C0C0C0C0C0C03 000000000003 000000000003
260 C0CC0C0C0C03 C0C0C0C0C0C03 000000000003 000000000003 000000000003 C0CC0C0C0C03 0C0C0C0C0C03 000000000003
270 0C0C0C0C0C03 0C0C0C0C0C03 000000000003 000000000003 000000000003 C0C0005C0003 004761220003 220045510003
300 C0C0C0C0C003 43466361C03 237146450003 000000000003 000000610003 63632444C03 000C0C0C0003 000025610003
310 5104C0C00003 C0C0C0C0C003 000025610003 510500000003 23462361C003 43006551C003 514651C0C003 63462445C003
320 230C0C0C0003 00C0C0C0C003 000000000003 655151460C03 51006346C0C3 2445230C0C03 667151220C03 230047610003
330 2222C0C0C03 C0C0C0C0C003 000000144003 000000100003 777740036003 C0CC3774C003 0C0C37776003 777740000003
340 C0CC00010003 0C0C0C0C0C03 160142300003 160050260003 000000034003 C0CC0C012003 0C0C00014003 000004000003
350 130C0C0C0003 0C0C0C0C0C03 400000000003 000000022003 000C0C0C0C03 C0C0C0006003 020000C0C003 04000000C003
360 4100C0C0C003 0C0C0C0C0C03 000000000000 000000000000 000000000000 16C07747C003 160037700C03 160127710003
370 16C0C012C003 16017733C003 160014140003 160177150003 1600C0160003 4C0C040C0003 160151370003 401000000003

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 30)

MODULE 0 SECTOR 17

```

0 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
10 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
20 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
30 50104720003 50105220003 00000000000 77777776003 130300000003 00000000000 002000000003 000000100003
40 00077776003 27000000003 26000000003 250000000003 240000000003 777000000003 00037740003 777740036003
50 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003
60 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003
70 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003
100 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003 00000000003
110 65000000003 66000000003 67000000003 70000000003 71000000003 41000000003 42000000003 43000000003
120 44000000003 45000000003 46000000003 47000000003 50000000003 51000000003 22000000003 23000000003
130 24000000003 25000000003 26000000003 27000000003 30000000003 31001010003 01000000003 02000000003
140 03000000003 04000000003 05000000003 06000000003 07000000003 10000000003 11000000003 12000000003
150 13000000003 20000000003 21000000003 33000000003 40000000003 53000000003 60000000003 73000000003
160 00000000003 14000000003 15000000003 16000000003 17000000003 32000000003 34000000003 35000000003
170 36000000003 37000000003 52000000003 54000000003 55000000003 56000000003 57000000003 72000000003

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 31)

MODULE 0 SECTOR 17

200 740000000003 750000000003 760000000003 770000000003 110000000003 210000000003 310000000003 410000000003
 210 510000000003 610000000003 710000000003 050000000003 050000000003 110000000003 150000000003 210000000003
 220 250000000003 310000000003 350000000003 410000000003 450000000003 510000000003 400000000003 010000000003
 230 020000000003 040000000003 100000000003 200000000003 514624230003 714565000003 073300650003 276551630003
 240 712265000003 233047650003 265171230003 655100000003 733047650003 006143430003 006143470003 706145240003
 250 446591710003 630071450003 006243610003 634200000003 616263640003 656667700003 714142430003 444546470003
 260 505122230003 242526270003 303133010003 020304050003 060710110003 120000000003 141516170003 323435360003
 270 372052210003 565772740003 757677130003 543355400003 536073000003 000000000003 000000000003 645400000002
 300 233047650003 004663230003 614300630003 706151610003 632365510003 270000000003 012345670003 233047650003
 310 006465630003 714461430003 007145230003 656765510003 220071450003 005165640003 000000000003 044321260003
 320 361150000003 150055300003 776000000002 000000000003 000000000003 000000000003 000000000003 000000000000
 330 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000000
 340 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000000
 350 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000000
 360 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000000
 370 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000003 000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 32)

	MODULE 1	SECTOR 0	
0	00C000100001	4110C0610003	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
10	041746476003	167541530003	004741410003 024240000003 0542401C0003 064242076003 114277666003 124246612003
20	134240236003	014240012003	131740336003 061622352003 004740436003 044261352C03 074240536003 104243012003
30	775540412003	040751012003	034243376003 152252612003 775540612003 042741212003 034242612003 152243212003
40	77553612003	014754212003	034254612003 152244612003 775545212003 041745612003 142277764003 775545476003
50	040745530003	014240236003	132242212003 775543612003 044744212003 014277766C03 13227776003 775547366003
60	046742076003	014246112003	132240632003 775551650003 050777766003 05427776003 172247366003 775546512003
70	052751650003	054277766003	17227776003 775547366003 054740736003 054241212003 172242076003 775546112003
100	072740732003	064251650003	20227776003 77557776003 074747366003 064246512003 202241032003 775551650003
110	076777766003	06427776003	202247366003 131741036003 441601212003 263402076003 777546112003 175541032003
120	777751650003	163577666003	775742076003 161547366003 100741136003 407246612003 047003036003 175740466003
130	057037666003	775541236003	102746112003 074251660003 212277666003 775543012C03 104751012C03 074277676003
140	212243132003	775551650003	106777666003 074243236003 212240466003 041341336C03 775546112C03 330251660003
150	022303076003	3272C0466003	235403012003 020251012003 220242076003 775540612003 110742612003 104243212003
160	222244612003	775545212003	112745612003 104245476003 222257130003 775542076003 114742212003 104243612003
170	222244212003	421437666003	000001436001 000006612001 000006112001 00C037666001 00C001536001 000037366001

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 33)

MODULE 1 SECTOR 0

200	000001636001	000037364001	000037666001	000003376001	000006612001	000001536001	000037364001	000037666001
210	116743336003	775540466003	044242076003	162277364003	775551660003	120743012003	044251012003	162277666003
220	775543436003	122740466003	124241736003	242277366003	775541536003	124777364003	124251660003	242243076003
230	775540466003	126743012003	124251012003	242277666003	775541036003	130746112003	114277766003	232277776003
240	775547366003	132742076003	114245512003	232277766003	775577766003	134747366003	114240736003	232246512003
250	775577766003	014777766003	024247366003	142242076003	775547512003	136777766003	134277766003	262247366003
260	302242076003	775550112003	144245476003	140771330003	134277766003	262277766003	302247366003	775542076003
270	142750512003	134242056003	262242340003	302277766003	144777766003	447247366003	131755412003	603611650003
300	14602056003	150037766003	000037766001	000007366001	000002076001	000011112001	000037766001	000037766001
310	00007366001	000002076001	000007112001	000037766001	000037766001	000007366001	000002076001	000012112001
320	000037766001	000037766001	000007366001	000002076001	000011512001	000037766001	000037766001	00007366001
330	000002076001	000013112001	000014112001	000001060001	000000000000	000000000000	000000000000	000000000000
340	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
350	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 34)

	MODULE 1	SECTOR 1																							
0	0000000000	0040CC000002	421001020003	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
10	0000000000	000000000000	047015636003	041777666003	154242212003	C04747112C03	00277666003	131755736003																	
20	045600512003	047437666003	434016036003	775541112003	330277666003	554206536003	775541512003	020537666003																	
30	041356136003	330242112003	436677666003	554216236003	775543112003	070277666003	002516336003	041343512003																	
40	330277666003	436656436003	554204112003	775577666003	070256536003	C14504512C03	576537666003	000256636003																	
50	041345112003	330277666003	554204636003	775542212003	074507112003	C41377666C03	330256736003	440640512003																	
60	554237666003	775557036C03	030241112003	076537666003	070502076003	C64501512C03	054537666003	034517136003																	
70	174502112003	274537666003	131757236003	175603112003	041777666003	074257336C03	070243512C03	330277666003																	
100	554202336003	775544112003	276537666003	041357436003	330244512003	036677666003	554217536003	775545112003																	
110	110240236003	272502212003	266507112003	256537666003	236500024003	376502076003	2762252512003	070277666003																	
120	330277664003	554217636003	7755252512003	446537666003	041352564003	330257736003	442652512003	554237666003																	
130	775565224003	120243536003	456512512003	041345476C03	330260530003	442642076003	554206612003	775577666003																	
140	120245036003	726513724003	041351112003	330260032003	442666610003	554237666003	775544736003	120253724003																	
150	746511112003	041346632003	330266610003	442677666003	554220136003	775553724003	120251112003	444520232003																	
160	442526610003	446277666C03	606520336003	626513724C03	636511112003	526520432C03	546526610003	766537666003																	
170	736520536003	646513724003	756511112003	406520632C03	426526610003	C70277666003	330260736003	554213724003																	

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 35)

	MODULE 1	SECTOR 1	
200	775551112003	506521032003	041366610003 330240236003 444644212003 554206612003 775577666003 130245036003
210	706500366003	041340364003	330277666003 444644736003 554200366003 775540364003 130277666003 466507036003
220	041340366003	330240364003	444677666003 554221136003 775540366003 130240364003 666537666003 041354436003
230	330240366003	444640364003	554237666003 775561236003 130240366003 516500364003 716537666003 476515636003
240	566500366003	700500364003	676537666003 106521336003 070240366003 330240364003 554237666003 775544636003
250	176500366003	041340364003	330277666003 446661436003 554200366003 775540364003 140242076003 136500366003
260	041343212003	330245476003	450641270003 554202076003 775543612003 150241260003 046537766003 041361500003
270	330240000002	452640000002	554200000002 775540000002 160240000002 440240000002 454300000002 613200000002
300	156500000002	041340000002	330240000002 010640000002 554200000002 775540000002 170240000002 166500000002
310	172500000002	336500000002	536500000002 116500000002 036500000002 126500000002 134500000002 246500000002
320	006500000002	146500000002	066500000002 042500000002 044500000002 056500000002 356500000002 556500000002
330	116500000002	056500000002	154500000002 152500000002 146500000002 070240000002 046240000002 041340000002
340	330240000002	554200000002	456000000002 000000000000 000000000000 000000000000 000000000000 000000000000
350	000000000000	000000000000	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
360	000000000000	000000000000	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
370	000000000000	000000000000	000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 36)

MODULE 1										SECTOR 2														
0	0000000000	0000000000	0000000000	0000000000	0000000000	0000000000	431001430003	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
10	0000000000	0000000000	0000000000	0000000000	0000000000	0000000000	000000000000	000000000000	100742076003	775577666003	163543212003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003	000777766003
20	15427776003	264247366003	254242056003	061755412003	011555310003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003	041777766003
30	002761412003	274263014003	304255310003	004777666003	314243336003	254243212003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003	006777766003
40	041347366003	102742056003	011555412003	041763132003	242255310003	242277766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003	263437766003
50	175561412003	043763014003	25426322003	060255310003	220277666003	77742076003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003	167543212003
60	265203636003	175743212003	010677766003	263237766003	106747366003	011542056003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003	010755412003
70	242255310003	263437766003	777577766003	175547366003	060261412003	220263014003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003	777763332003
100	110677666003	265202076003	175743212003	012642012003	263223436003	112743212003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003	011577766003
110	242247366003	242242056003	263415412003	777555310003	175577766003	060277766003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003	220247366003
120	167563014003	114663532003	265215310003	175777666003	014663636003	263203212003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003	067777666003
130	267407366003	175542056003	063015412003	775563732003	116755310003	16357766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003	061777766003
140	014761412003	124263014003	242264032003	016755310003	274242076003	304243212003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003	004747366003
150	254242412003	041351012003	04135520003	04137766003	120761500003	011564136003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003	014747212003
160	242243244003	263416010003	777564336003	175547212003	020764236003	254243244003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003	060256510003
170	777747212003	167550212003	122664236003	265203244003	175757310003	022664336003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003	263207212003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 37)

MODULE 1 SECTOR 2

200	011543244003	022760010003	242264136003	242247212003	263424236003	777543244003	175560510003	060240236003
210	220247212003	777746236003	167547612003	126643244003	265221310003	175764336003	024647212003	263202056003
220	130764536003	011547612003	024742056003	242242056003	242262012003	263421714003	77755510003	175564636003
230	060247612003	220264236003	777743244003	167563210003	132664536003	265207612003	175764236003	026643244003
240	263223710003	067764636003	254247612003	775550212003	134764236003	163543244003	061764510003	011564536003
250	041747612003	264264436003	026743244003	124265210003	242264636003	030747612003	314264236003	032743244003
260	304265710003	274240236003	041747612003	254246236003	041347212003	041343244003	041366510003	136764536003
270	011547612003	026742056003	242264336003	242247212003	263422012003	777564714003	175562710003	065765000003
300	254240000002	060240000002	220240000002	777740000002	167540000002	140640000002	265200000002	175740000002
310	024640000002	263200000002	142740000002	011540000002	024740000002	242240000002	242240000002	263400000002
320	777540000002	175540000002	060240000002	220240000002	777740000002	167540000002	144640000002	265200000002
330	175740000002	022640000002	263200000002	146740000002	011540000002	022740000002	242240000002	242240000002
340	263400000002	777540000002	175540000002	060240000002	220240000002	777740000002	167540000002	150640000002
350	265200000002	175740000002	014640000002	263200000002	067740000002	254240000002	034000000002	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 38)

	MODULE 1			SECTOR 3				
0	CCCCCCCC00	0000000000	0000000000	000000400001	441002040003	CCCC00000000	CCCC00000000	000000000000
10	CCCCCCCC00	0000000000	0000000000	000000000000	000000000000	CCCC00000000	000000000000	000000000000
20	224746536003	775577666003	163547166003	061743076003	011540466003	C0C740636003	264245212003	046752112003
30	124241436003	242254612003	054741536003	314254212003	274253612003	C52742076003	304252612003	254242056003
40	041342056003	041342056003	041346636003	226740466003	011540636003	046752112003	242252112003	242241700003
50	036037766003	777547666003	175543276003	043752612003	254243012003	060251012003	22027776003	777747366003
60	167546732003	230675610003	734207676003	175740532003	056675510003	732207036003	232740466003	011540536003
70	056752112003	242252112003	242241700003	036037766003	777547666003	175543012003	060251012003	22027776003
100	777747366003	167547132003	234675610003	734207676003	175742032003	C60675510003	732207236003	236740466003
110	011542036003	060752112003	242252112003	242241700003	036037766003	777547666003	175543012003	060251012003
120	22027776003	777747366003	167547332003	240675610003	734207676003	175775510003	732203376003	067752612003
130	254277666003	775547436003	256747166003	163543076003	061740466003	011540036003	041753212003	264241336003
140	041745212003	124252112003	242240136003	062753612003	304254612003	274240236003	030754212003	314252612003
150	254242056003	041342056003	041342056003	041347536003	242740466003	C11541336003	041752112003	242252112003
160	242241700003	036037766003	777547666003	175542176003	065752612003	254243012003	060251012003	22027776003
170	777747366003	167547632003	244675610003	734207676003	175742132003	C60675510003	732207736003	246740466003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 39)

MODULE 1 SECTOR 3

200	011542136003	060752112003	242252112003	242241700003	036037766003	777547666003	175543012003	060251012003
210	22027776003	777747366003	167550032003	250675610003	734207676003	175742232003	056675510003	732210136003
220	252740466003	011542236003	056752112003	242252112003	242241700003	036037766003	777547666003	175543012003
230	060251012003	22027776003	777747366003	167550232003	254675610003	734207676003	175742332003	046675510003
240	732203376003	067752612003	254277666003	064010336003	000007166001	000003076001	000000466001	000002076001
250	00013212001	000002336001	000005212001	000012112001	000002436001	000014212001	000013612001	000002536001
260	00014612001	000012612001	000002056001	000002056001	000002056001	000010436001	000000466001	000002336001
270	00012112001	000012112001	000001700001	000037766001	000007666001	000010366001	000012612001	000003012001
300	00011012001	000037766001	000007366001	000010532001	000035610001	000007676001	000002232001	000035510001
310	00010636001	00000466001	000002236001	000012112001	000012112001	00001700001	000037766001	000007666001
320	00003012001	000011012001	000037766001	000007366001	000010732001	000035610001	000007676001	000002132001
330	000035510001	000011036001	000000466001	000002136001	000012112001	000012112001	000001700001	000037766001
340	00007666001	000003012001	000011012001	000037766001	000007366001	00001132001	000035610001	000007676001
350	000000000000	000000000000	000000000000	000012612001	000002060001	000007666001	000003140001	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 40)

	MODULE 1		SECTOR 4	
0	0000000000	0000000000	0000000000	0000000000
10	0000000000	0000000000	0000000000	0000000000
20	262752736003	775577666003	161547066003	264753036003
30	154253612003	074743436003	314252612003	414742076003
40	416752612003	304242056003	254242076003	041746612003
50	254253212003	020742056003	26427766003	04137776003
60	024677766003	50723776003	777547366003	777752112003
70	777547366003	77752112003	167560132003	242256410003
80	167560232003	242256410003	27267766003	50723776003
90	010677766003	50723776003	777547366003	777752112003
100	777547366003	777752112003	167542132003	242256410003
110	167560332003	242256410003	41267766003	50723776003
120	410677766003	50723776003	777547366003	777752112003
130	777547366003	777752112003	167543032003	242256410003
140	167560332003	242256410003	41267766003	50723776003
150	410677766003	50723776003	777547366003	777752112003
160	777547366003	777752112003	167543032003	242256410003
170	167560332003	242256410003	41267766003	50723776003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 41)

MODULE 1 SECTOR 4

```

200 57160000002 77554000002 50624000002 05224000002 17554000002 26610000002 57160000002 77554000002
210 27074000002 17510000002 57160000002 77554000002 52624000002 05224000002 17554000002 26610000002
220 57160000002 77554000002 27074000002 17510000002 57160000002 77554000002 54624000002 05224000002
230 17554000002 26610000002 57160000002 77554000002 27074000002 17510000002 57160000002 44024000002
240 42030000002 52120000002 54740000002 17554000002 42274000002 40724000002 17574000002 05700000002
250 77554000002 06774000002 00024000002 42474000002 42724000002 42674000002 44724000002 33024000002
260 42664000002 57120000002 17024000002 21424000002 22424000002 23424000002 24424000002 06774000002
270 00024000002 04700000002 22024000002 43000000002 77754000002 43200000002 00000000000 00000000000
300 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
310 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
320 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
330 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
340 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
350 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
360 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
370 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 42)

MODULE 1 SECTOR 5

0	C0C0C0C0C0C0C0	0000C000C0C0C0	00000000000000	000000000000	000000000000	0140C000000002	461030060003	000000000000
10	00C0C0C0C0C0C0	0000C0C0C0C0C0	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
20	44C746576C03	77554253C003	447242410003	424742240003	4472616C0003	454742076003	044261726003	440746612003
30	427262534003	2024C4636003	606244754003	052247666003	360107236003	C77604654C03	617407672003	775544626003
40	626263134003	0522620360C3	3621222352003	617621236003	775562352003	64625012C003	052253636003	175542212003
50	354122036003	617621352003	775545420003	356746120C03	1751377660C3	6176221360C3	775543244003	666245610003
60	05227740C03	360122036C03	151622352003	617410120C03	7755617360C3	7062436560C3	052261726003	175562204003
70	354107310003	61761062C0C3	775553636003	356762534003	175104636003	617603756003	775544626003	726263134003
100	052244320003	362137766003	617622336003	775543244003	44075031C003	44727774C003	424761236003	447262352003
110	456777666003	044262436003	440742212003	427262036003	702421352003	60625012C0C3	052270312003	362102512003
120	6176C7666003	775556604003	626270770003	052277666003	360116736003	257607644003	617430770003	775577666003
130	646271312003	052242512C03	362107666003	617616604003	775570770003	666277666003	052256736003	362107644003
140	617630770003	775577666C03	706272312003	052242512003	3601170C4003	31761473C003	617430760003	775577666003
150	726273312003	052242512003	175547666003	354116604003	6176307700C3	775577666C03	356756736C03	175107644003
160	61763C770003	775577666003	440774312003	447242512003	424757104003	44727077C003	014777666003	044275312003
170	440742512003	427257004003	422757430003	447270760003	46C777666003	447262036003	130422352003	130421236003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 43)

MODULE 1 SECTOR 5

200	127262352003	052262536003	175542212003	364122036003	617621352003	775550120003	366770312003	175102512003
210	6176C7666003	775556604003	065770770003	427277666003	775556736003	130407644003	130430770003	127277666003
220	052271312003	175542512003	372107666003	617616604003	775570770003	370777666003	175116736003	617607644003
230	775570770003	422777666003	447272312003	130402512003	130407666003	127256604003	052270770003	175577666003
240	364116736003	6176C7644003	775570770003	366777666003	175133312003	617602512003	775547666003	020756604003
250	427270770003	130437666003	130416736003	127247644003	052270770003	175577666003	376134312003	617602512003
260	775547666003	374756604003	175130770003	617637666003	775556736003	460747644003	447270770003	130437666003
270	130435312003	127242512003	052247666003	175556604003	364130770003	617637666003	775556736003	366747644003
300	175130770003	6176C2660003	440740000002	447240000002	424740000002	447240000002	045000000002	777540000002
310	432000000002	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
320	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
330	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
340	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
350	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
360	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000
370	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000	000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 44)

	MODULE 1	SECTOR 6	
0	000000000000	000000000000	000000000000 471017470003
10	000000000000	000000000000	000000000000 000000000000
20	000000000000	000000000000	000000000000 000000000000
30	15774000002	04500000002	04174000002 20354000002 41024000002 42024000002 52254000002
40	52454000002	53054000002	53254000002 20154000002 06774000002 53454000002 20274000002
50	53654000002	45470000002	36674000002 11330000002 17554000002 20674000002 10130000002 17564000002
60	20654070003	22074000002	10130000002 17564000002 22054000002 24274000002 10130000002 17564000002
70	24254207603	25277666003	101302212003 175647112003 252577666003 460705036003 536742212003 016247112003
100	54077666003	065104736003	203200512003 21277666003 036244436003 540741112003 065137666003 215202076003
110	212741512003	036277666003	534744436003 371602112003 230277666003 727401036003 440243112003 462337666003
120	201205036003	212743512003	036277666003 230241036003 727404112003 21277666003 036244436003 440244512003
130	462337666003	201204736003	536745112003 202737666003 536544736003 534742212003 305607112003 20277666003
140	536545036003	331400512003	53677666003 175201036003 534541112003 06777666003 522546536003 202741512003
150	016277666003	540746636003	065102112003 325237666003 522744436003 337603112003 411437666003 212744736003
160	376243512003	54077666003	065106736003 345204112003 21277666003 376241036003 041744512003 522577666003
170	067745036003	524545112003	201437666003 212747036003 204742212003 176247112003 230277666003 727407136003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 45)

MODULE 1 SECTOR 6

200 440240512003 462337666003 273207236003 265401112003 524777666003 511602076003 526741512003 567637666003

210 530747336003 645602112003 532777666003 433607436003 045003112003 542777666003 447247536003 454703512003

220 206777666003 075347636003 206544112003 220777666003 075347736003 220544512003 242777666003 075354336003

230 242545112003 252777666003 075354436003 252542212003 460707112003 201777666003 075354536003 201540512003

240 544137666003 201214636003 532541112003 201437666003 210742076003 236241512003 230277666003 727414736003

250 210742112003 236277666003 230255036003 727403112003 500777666003 447255136003 204743512003 136277666003

260 230255236003 727404112003 204777666003 076255336003 230244512003 727437666003 067755436003 526545112003

270 041759500003 524540000002 721400000002 206740000002 236240000002 230240000002 727400000002 206740000002

300 236240000002 230240000002 727400000002 546740000002 447240000002 206740000002 136240000002 230240000002

310 727400000002 206740000002 076240000002 230240000002 727400000002 067740000002 530540000002 041740000002

320 526540000002 721400000002 204740000002 236240000002 230240000002 727400000002 204740000002 236240000002

330 230240000002 727400000002 542740000002 447240000002 210740000002 136240000002 230240000002 727400000002

340 210740000002 076240000002 230240000002 727400000002 067740000002 532540000002 041740000002 530540000002

350 546740000002 447240000002 411400000002 775540000002 203740000002 065340000002 203540000002 410240000002

360 550300000002 751200000002 065740000002 420240000002 775000000002 000000000000 000000000000 000000000000

370 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 46)

	MODULE 1		SECTOR 7		
0	0000000000	0000000000	0000000000	0000000000	0000000000
10	0000000000	0000000000	0000000000	0000000000	501040100003
20	0000000000	0000000000	0000000000	0000000000	0000000000
30	0000000000	0000000000	0000000000	0000000000	00001700001
40	155740236003	1356C3256003	131740226003	115630704003	157411430003
50	447253230003	041743244003	044255230003	104243244003	00777666003
60	000562352003	544126736003	113220352003	000571236003	201426536003
70	546771336003	447260352003	550771436003	407262352003	154277666003
100	554760352003	C00271536003	775543612003	556750512003	065126236003
110	330271636003	552321352003	255200264003	775560520003	233220352003
120	552303612003	247210512003	255426536003	200262352003	777567436003
130	155740264003	273620520003	271237666003	045031136003	267220352003
140	554743612003	000250512003	570766536003	467262352003	313231436003
150	552300264003	255220520003	775577666003	572766736003	330261352003
160	345226536003	255422352003	200266236003	220260352003	552310512003
170	131577666003	002766736003	427220352003	456732436003	154260520003
					175566536003
					520762352003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 47)

MODULE 1 SECTOR 7

200 113332036003 175660352003 426566736003 440761352003 101300264003 175577666003 522771036003 113303244003
210 175660710003 440555412003 466726514003 012752650003 171567536003 C44243244003 162261510003 464715412003
220 000766514003 167562310003 104243040003 222250012003 456711012003 426742240003 075340000002 426540000002
230 440740000002 075340000002 440540000002 466700000002 002740000002 065340000002 002540000002 576100000002
240 525600000002 600740000002 427240000002 002740000002 602100000002 611200000002 002540000002 611400000002
250 012740000002 000740000002 002740000002 604100000002 541600000002 606740000002 427240000002 611400000002
260 002740000002 610100000002 555600000002 612740000002 427240000002 611400000002 002740000002 550100000002
270 571600000002 614740000002 427240000002 611400000002 002740000002 616100000002 563600000002 603200000002
300 547400000002 065100000002 503200000002 533400000002 775540000002 620740000002 065100000002 615200000002
310 330240000002 552300000002 255200000002 775540000002 572740000002 065100000002 633200000002 330240000002
320 552300000002 647200000002 061000000002 200240000002 100400000002 C00000000000 000000000000 C00000000000
330 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
340 C00000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
350 C00000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
360 C00000000000 C00000000000 000000000000 000000000000 000000000000 000000000000 C00000000000 000000000000
370 000000000000 000000000000 000000000000 000000000000 000000000000 - 000000000000 200000000000 000000000000

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 48)

	MODULE 1	SECTOR 10	
0	13CC0700003	511C10050003	777777776003
		000152204003	000020CC0003
			00CC0040003
			77776CC0003
			525240000003
10	25252000003	4CC00000003	65252000003
		212520000003	253500C00003
			C02CC002003
			0C0CC010003
			002000000003
20	00252000003	00124C000003	001250000003
		003770000003	524C00000003
			252CC0000003
			776000C0003
			511100110003
30	501056CC0003	501055400003	501064000003
		501106400003	5011134C0003
			CC0000524003
			000000252003
			C00000776003
40	C0000040003	525CC0000003	252400000003
		777400000003	525250C00003
			252524CC0003
			777774CC0003
			252525252003
50	525252524003	0C0012524003	000005252003
		000017776003	125200000003
			052500000003
			177700000003
			252505252003
60	125202524003	3777C7776003	00000004003
		501034060003	501045410003
			00C00002003
			25250C000003
			125250000003
70	631463146003	714631462003	746310000003
		171440000003	474630C00003
			63631463003
			317140C00003
			147460000003
100	C0000270001	001CC0000003	577777776003
		777777776003	377777776003
			17777774003
			000160016003
			000140014003
110	000120012003	0001CC010003	000060006003
		000040004003	000020002003
			001600160003
			001400140003
			001200120003
120	C010C01CC003	000600060003	000400040003
		000200020003	016001600003
			C14001400003
			012001200003
			010001000003
130	C06000600003	0040C0400003	002000200003
		160016000003	140014000003
			12C0120C0003
			100010CC0003
			060006000003
140	04CC04C00003	020CC2000003	000000000003
		363146314003	741703606003
			760741702003
			77036CC00003
			17605000C0003
150	077030000003	037417036003	017600000003
		607700000003	374170360003
			501005010003
			776003770003
			377001774003
160	1774CC000003	637700000003	717740000003
		747760036003	36377CC00003
			77177CC00003
			477600376003
			377776000003
170	177770000003	037750000003	017770000003
		007777740003	001770000003
			C7777740003
			C00001774003
			0C0001252003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 49)

MODULE 1 SECTOR 10

```

200 52520C000003 036077776003 036000000003 741777776003 74170C0C0003 770077776003 770000000003 007777776003
210 0077CC000003 146314630003 036074170003 001774006003 000003776003 501047600003 501066420003 01000000000003
220 20000C000003 0010C000C003 000400000003 000200000003 000100000003 000C40C0C003 100C000C0003 501006020003
230 C00C01760003 0400C000C003 000001240003 00000520003 000000630003 00000146C003 0CC000146003 14000000000003
240 00C000300003 677777776003 000000014003 277777776003 000000334003 537777776003 737777776003 00400000000003
250 511006220003 0000C000C003 000000000003 000000000003 000000000003 0C0C0C00C003 0CC0C0000003 00000000000003
260 C00000652003 0000C030003 072000000003 000000170003 000000176003 000C0000C000 000000CC0000 00000000000000
270 00C000000000 0000C0000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000000000
300 000000000000 0000C0000000 000000000000 000000000000 000000000000 000C00000000 000000000000 00000000000000
310 000000000000 0000C0000000 000000000000 000000000000 000000000000 00CC0C000000 000000000000 00000000000000
320 000000000000 0000C000C000 000000000000 000000000000 000000000000 00CC00000000 000000000000 00000000000000
330 C000C0C00000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000000000
340 00C0C0C00000 00C0C0000000 000000000000 000000000000 000C0C0C0C00 00C0C000C0C0 00C0C000C0C0 00000000000000
350 C0C0C0C0C000 00C0C0000000 000000000000 000000000000 000000000000 00C0C0C0C0C0 00C0C0C0C0C0 00000000000000
360 C0C0C0C00000 00C0C0000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000000000
370 C0C0C0C00000 0000C0000000 000000000000 000000000000 000000000000 000000000000 000000000000 00000000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 50)

	MCCULE 1	SECTOR 11	
0	77777776003	0015C0016003	002540000003 000000040003 0000120C0003 C0001250C003 000012524003 000340064003
10	00C00004003	000012764003	000017764003 00001776003 000340000003 002540064003 511010030003 511054620003
20	CC000500003	000005776003	000005752003 000005252003 000340126003 C015C0000003 002540016003 000000252003
30	00C00012003	0015C0126003	511010040003 000000040003 000000006003 C011C0002003 001100C00003 521177120003
40	511055620003	511023620003	511023220003 511035220003 511034620003 511045620003 511045220003 511121620003
50	511071220003	511070620003	511102620003 511102220003 51111322C003 51111262CC03 511010030003 511136620003
60	511136220003	51115022C003	511147620003 511160620003 51116022C003 51105403CC03 511024030003 511023430003
70	511035430003	511035030003	511046030003 511045430003 511121030003 511070430003 511070030003 511102030003
100	511101430003	511112430003	511112030003 5111010230003 511135430003 511135030003 511147030003 511146430003
110	511157430003	511157030003	511054630003 511024630003 511024230003 511C36230003 511035630003 511046630003
120	511046230003	511071230003	511070630003 511102630003 511102230003 511113230003 511112630003 511010040003
130	511010240003	511010240003	511112440003 000311120003 000320340003 C0G012240003 000016524003 000012524003
140	000002524003	00C006524003	000007524003 000006524003 000004524003 C00005524003 000005724003 000005524003
150	000005124003	000005324003	000005364003 000005324003 000005224003 C00005264003 000005274003 000005264003
160	000005244003	000005254003	000005256003 000005254003 000005250003 C00005252003 00000654003 000010520003
170	00C006100003	000011160003	000106320003 000110740003 000051760003 000047740003 000025200003 000023560003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 51)

MODULE 1 SECTOR 11

```

200 000003700001 00012264003 000017264003 00005536003 00005512003 00000512003 00000014003 001100010003
210 100000000003 000004000003 000040000003 000020000003 511010050003 501047600003 531054270003 000000000003
220 000100000003 000025234003 060000000003 000003600003 000017070003 00000322003 00003416003 000014744003
230 000001000003 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
240 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
250 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
260 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
270 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
300 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
310 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
320 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
330 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
340 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
350 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
360 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
370 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 52)

MODULE 1 SECTOR 12

0	774014C00003	777760C00003	777760000003	777774000003	774014C00003	774C140C0003	774014C00003	774014C00003	774014000003
10	774014C00003	77401C000003	774004000003	774014000003	774014C00003	774014C00003	774014C00003	774014C00003	774014000003
20	774C14C00003	774C14000003	774034000003	774054000003	774114000003	7742140C0003	774414000003	774014000003	775014000003
30	776014C00003	774C14000003	774014000003	774014000003	774014000003	774C14000003	774014C00003	774014C00003	774014000003
40	770014C00003	764014000003	754014000003	734014000003	674014000003	574C14C00003	374C14000003	774014000003	774014000003
50	774014C00003	774014C00003	774014000003	774014000003	774014000003	774C14000003	777760000003	777760000003	777760000003
60	777760C00003	777760C00003	777760000003	777764000003	777770000003	777760000003	777760000003	777760000003	777760000003
70	777760000003	777760000003	777760000003	777760000003	777740000003	77772CC00003	77766CC00003	777760000003	777560000003
100	777360000003	776760000003	775760000003	777760000003	77776C000003	77776C000003	77776C000003	77776C000003	777760000003
110	777760000003	777760000003	773760000003	767760000003	757760000003	737760000003	677760000003	577760000003	577760000003
120	377760C00003	77776CC00003	777760000003	777760000003	777760000003	777760000003	777760000003	777760000003	777760000003
130	777760C00003	777760000003	777760000003	777760000003	777760000003	777764000003	777770000003	777760000003	777760000003
140	77776C000003	77776C000003	777760000003	777760000003	777760C00003	77776C000003	777740000003	777720000003	777720000003
150	77766C000003	777560000003	777360000003	776760000003	775760000003	77776C000003	77776C000003	777760000003	777760000003
160	77776C000003	77776C000003	777760000003	777760000003	773760000003	76776C000003	757760000003	737760000003	737760000003
170	677760C00003	577760000003	377760000003	777760000003	77776C000003	77776C000003	77776C000003	777760000003	777760000003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 53)

MODULE 1 SECTOR 12

```

200 77776000003 77776000003 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003
210 77776400003 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003
220 77775400003 77773400003 77767400003 77767400003 77737400003 77677400003 77577400003 77777400003 77777400003
230 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003 77377400003 77777400003 76777400003
240 75777400003 73777400003 67777400003 57777400003 37777400003 77777400003 77777400003 77777400003 77777400003
250 77777400003 77777400003 77777400003 77777400003 77777400003 77777400003 00000000000 00000000000 00000000000
260 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
270 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
300 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
310 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
320 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
330 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
340 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
350 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
360 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000
370 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 54)

	MODULE 1	SECTOR 13	
0	00000000003	00000000003	00000000003
10	77777776003	70017776003	74017776003
20	74017772003	74017776003	74017776003
30	74017776003	74017776003	74017776003
40	74017776003	74017776003	74017776003
50	74017776003	74017776003	74017776003
60	74417776003	75017776003	76017776003
70	00017774003	00017774003	00017774003
100	00017734003	00017774003	00017774003
110	00017674003	00017574003	00017374003
120	00017774003	00017774003	00017774003
130	00117774003	00217774003	00417774003
140	43760074003	03760076003	037600774003
150	037600674003	037600574003	037600374003
160	03760074003	037600774003	037601774003
170	03770074003	037600774003	037600774003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 55)

MODULE 1 SECTOR 13

```

200 037400774003 037200774003 036600774003 035600774003 033600774003 C27600774003 017600774003 737777776003
210 677777776003 577777776003 377777776003 777777774003 777777776003 777777776003 777777772003 777777776003
220 777777756003 777777736003 777777676003 77777756003 777777376003 777777776003 777777776003 777777776003
230 777777776003 777777776003 777777776003 777777776003 777777676003 7777775776003 7777773776003 777777776003
240 777777776003 777777776003 777677776003 777777776003 777777776003 777777776003 777777776003 777777776003
250 777777776003 777777776003 777577776003 777377776003 776777776003 775777776003 773777776003 767777776003
260 757777776003 00000002003 000000024003 000004000003 000000012003 000100000003 000100000003 000000040003
270 000001622003 00000266003 50104760003 50101426003 000000100003 000000074003 400000000003 000000406003
300 00003000003 00000530003 000000262003 000024000003 000000136003 000220000003 000021000003 000000040003
310 00000360003 00000200003 22200000003 04440000003 00000014003 000000200003 000000050003 266400000003
320 00000022003 15400000003 00000000003 000000420003 111000000003 000000000000 000000000000 000000000000
330 00000000000 00000000000 00000000000 00000000000 00000000000 000000000000 000000000000 000000000000
340 00000000000 00000000000 00000000000 00000000000 00000000000 000000000000 000000000000 000000000000
350 00000000000 00000000000 00000000000 00000000000 00000000000 000000000000 000000000000 000000000000
360 00000000000 00000000000 00000000000 00000000000 00000000000 000000000000 000000000000 000000000000
370 00000000000 00000000000 00000000000 00000000000 00000000000 000000000000 000000000000 000000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 56)

MODULE 1 SECTOR 14

```

0  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
10  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
20  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
30  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
40  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
50  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
60  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
70  CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
100 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
110 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
120 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
130 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
140 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
150 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
160 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
170 CCCCCCCCCC 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0003770001

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 57)

MODULE 1 SECTOR 14

200 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

210 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

220 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

230 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

240 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

250 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

260 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

270 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

300 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

310 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

320 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

330 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

340 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

350 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

360 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

370 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 551003550003

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 58)

MODULE 1 SECTOR 15

```

 0  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 000017700001
10  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
20  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
30  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
40  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
50  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
60  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
70  0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
100 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
110 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
120 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
130 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
140 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
150 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
160 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000
170 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 00000000000000 561000360003

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 59)

MODULE 1 SECTOR 16

```

200 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
210 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
220 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
230 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
240 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
250 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
260 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
270 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
300 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
310 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
320 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
330 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
340 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
350 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
360 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
370 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 62)

MODULE 1 SECTOR 17

```
0 1600056003 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
10 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
20 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
30 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
40 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
50 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
60 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
70 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 130074000003  
100 130014c3003 57116537003 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
110 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
120 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
130 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
140 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
150 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
160 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000  
170 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 63)

MODULE 1 SECTOR 17

```

200 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
210 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
220 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
230 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
240 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
250 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
260 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
270 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
300 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
310 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
320 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
330 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
340 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
350 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
360 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000
370 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000 000000000000

```

Figure 7-15. PTC ADAPT Self-Test Program Memory Location Contents (Sheet 64)

Column	Column Heading	Definition of Column Data
1	IM	Instruction Module
2	IS	Instruction Sector
3	S	Syllable
4	LOC	Location (memory)
5	OP	Operation Code (octal)
6	DM	Data Module
7	DS	Data Sector
8	9	A9 Bit (0 or 1)
9	ADR	Operand Address
10	OCT VAL	Octal Value (constant)
11	LHS	Left Hand Side (symbolic code)
12	OPC	Operation Code (alphabetic)
13	VARIABLE	Data or Operand
14	COMMENT	Description of Operation
15	SEQ NO	Sequence Number of punched card in program listing.

Figure 7-16. PTC ADAPT Test Program Column Information

SECTION VIII

TROUBLE ISOLATION

8-1. SCOPE.

8-2. This section describes the basic operations involved in isolating troubles in the PTC. (General trouble isolating procedures keyed to the calibration procedures will be supplied in changes to this manual.)

8-3. BASIC TROUBLE SHOOTING PROCEDURE.

8-4. ANALYSIS.

8-5. When a PTC malfunction is discovered, the pertinent calibration procedures in Section VII should be performed to localize the malfunction to a particular functional unit of the PTC.

8-6. When the malfunctioning unit has been determined, analyze its circuits with the aid of the Second Level Logic and Electrical Schematic Diagrams in Section X and the circuit descriptions in Section II. Reference is made from the Second Level Logic Diagrams to the Automated Logic Diagrams (ALD's) by the "LN" numbers of the ALD sheets. The ALD's show the point to point wiring of the gate assemblies; circuit points for testing signal levels can be determined from these diagrams. Reference is also made between the ALD's and the Electrical Schematic Diagrams by "LN" numbers.

NOTE

Descriptions of the format and contents of these types of diagrams are given in Section X. The format of the "LN" numbers is also explained in Section X.

8-7. PROBING GATE ASSEMBLIES.

8-8. Signal levels in the gate assembly circuits can be observed by probing the pins of the SMS card receptacles. (The logic blocks on the ALD's specify the pins used for logic signals and the locations of the cards (and receptacles) in the gate assemblies.)

CAUTION

To prevent damage to the equipment, take care to locate the correct pins while probing a gate assembly.

8-9. Figure 8-1 shows the SMS card receptacle pin arrangement on the wiring side of a gate assembly; the gate assembly is shown in its extended or open position.

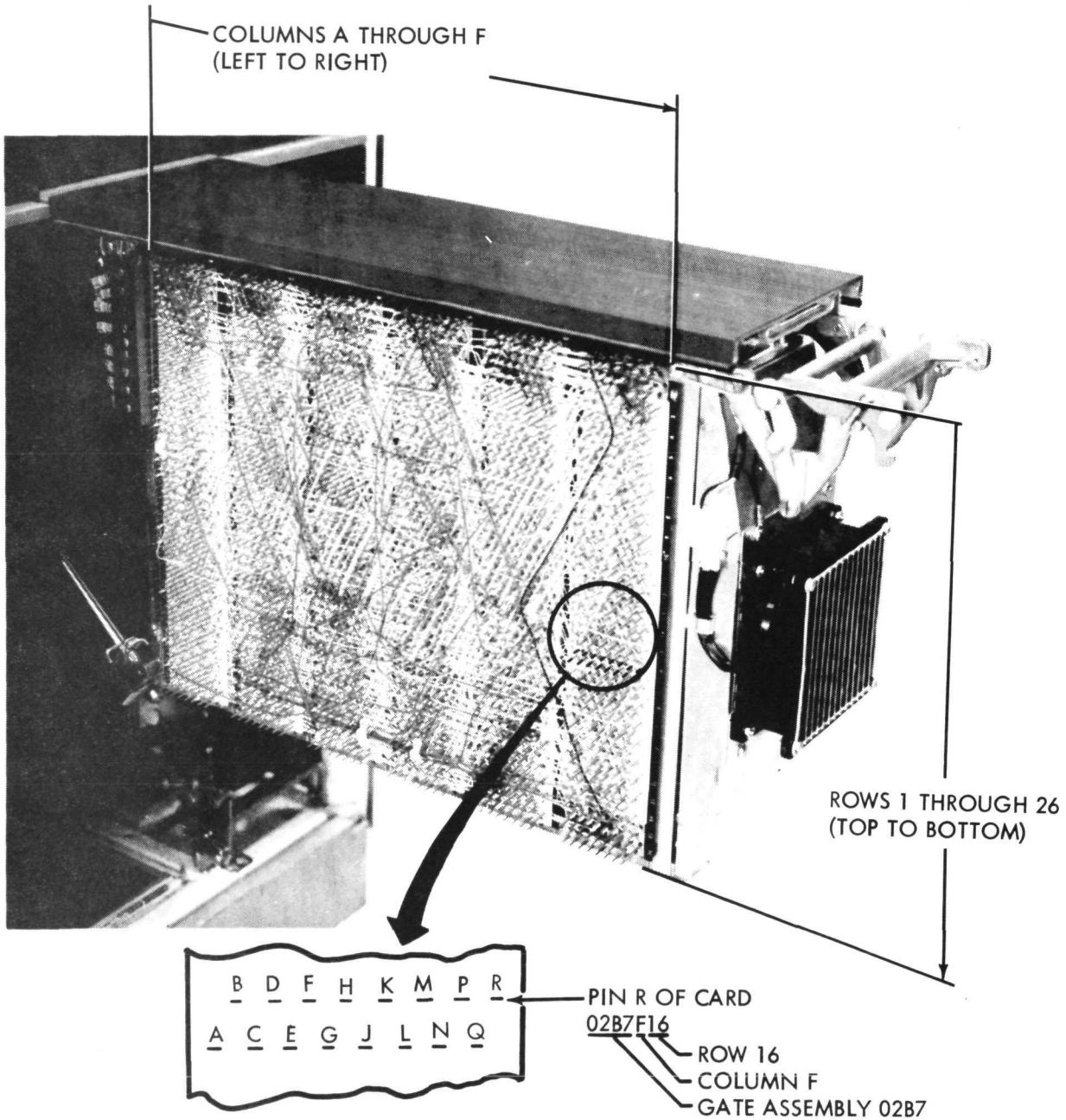


Figure 8-1. SMS Card Location and Pin Arrangement in Gate Assemblies

8-10. TROUBLE SHOOTING SMS CARDS.

8-11. Except for the special printed circuit board assemblies (figure 9-2), SMS cards are considered nonreparable and should be replaced by a new card when a failure occurs. If a special printed circuit board assembly (card) is determined to be faulty, the card should be checked to determine the faulty component. To check the card circuits:

- a. Turn off PTC power.
- b. Pull the card from its receptacle (use SMS Card Puller, IBM part number 6072429, shown on figure 4-4, part A).
- c. Insert Card Extender (IBM part number 6072431, shown on figure 4-3, part C) into the card receptacle.
- d. Insert the card into the Card Extender, and apply power to the PTC.

With the aid of the special card schematic diagrams (figures 10-38 and 10-39) the defective card component can be determined; the card should then be repaired as described in Section IX.

SECTION IX

REPAIR

9-1. SCOPE.

9-2. This section contains (1) lists of replaceable PTC assemblies and parts; (2) descriptions of recommended methods of replacement and repair of these assemblies and parts; (3) a list of materials required to refurbish the PTC exterior surfaces; and (4) a description of recommended methods for refurbishing these surfaces.

WARNING

Hazards to service personnel exist in the following PTC assemblies:

1. Interlock and Filter Box Assembly (01B5) - Line voltage is present when PTC power is off.
2. Memory Arrays (02A4 and 02A5) - The memory unit is not connected to the equipment ground when connector J1 is disconnected; potentials of +30 VDC and -28 VDC are present when J1 is disconnected.
3. Tape Reader and Tape Spooler Assemblies (03A2 and 03A3) - when the assemblies are pulled forward, the motor shafts and belts are exposed.

9-3. REPLACEABLE ASSEMBLIES AND PARTS.

9-4. Figure 9-1 lists the replaceable PTC assemblies. Figures 9-2 through 9-11 list the recommended replaceable parts to be supplied by the International Business Machines Corporation. Figure 9-12 identifies the vendors and their codes as contained in the Federal Supply Code for Manufacturers, Cataloging Handbook H4-1. Reference should be made to the assembly drawings (figures 10-29 through 10-37) when replacing assemblies.

9-5. REPAIR TECHNIQUES.

9-6. The following paragraphs discuss repair techniques applicable to the PTC. Many of the special tools listed and illustrated in Section IV are referenced in these discussions.

9-7. PUSHBUTTON SWITCH ASSEMBLIES.

9-8. As shown on figure 9-13, a pushbutton switch assembly consists of four basic parts: switch, switch housing, light module, and screen. All of these parts and the lamp bulbs within the light modules are replaceable parts, as indicated on figures 9-8 through 9-11.

WARNING

Remove main power from PTC before dismantling any switch assemblies on the control panels.

9-9. The screen of any PTC pushbutton switch can be removed from the switch housing by inserting the arms of the Switch Assembly Extractor (IBM part number 6900020) into the spaces between the sides of the screen and the switch housing until the arms of the extractor engage the openings in the frame which supports the screen; the screen (and its frame) can then be pulled out of the switch housing. When the screen has been removed, the light module can be removed in the same manner. The switch can be removed from its housing by using the Switch Assembly Wrench (IBM part number 6900017) to loosen the nut which holds the switch to its housing.

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
01A1	Plotter Assembly	6900170	14668
01B1	Gate Assembly	Refer to figure 10-2	
01B2	Gate Assembly	Refer to figure 10-2	
01B3	Gate Assembly	Refer to figure 10-2	
01B4	Power Supply Assembly	Refer to figure 9-3	
01B5	Interlock and Filter Box Assembly	Refer to figure 9-4	
01B6	Resonator Supply Assembly	Refer to figure 9-5	
01B7	Power Supply Assembly	Refer to figure 9-6	
01B8	Power Supply Assembly	Refer to figure 9-7	
02A1	Memory Load and Data Display Panel Assembly	Refer to figure 9-8	
02A2	Processor Panel Assembly	Refer to figure 9-9	
02A4	Memory Array	6900634	03640
0245	Memory Array	6900633	03640
02B1	Gate Assembly	Refer to figure 10-2	
02B2	Gate Assembly	Refer to figure 10-2	
02B3	Gate Assembly	Refer to figure 10-2	
02B4	Gate Assembly	Refer to figure 10-2	
02B5	Gate Assembly	Refer to figure 10-2	
02B6	Unused		
02B7	Unused		
02B8	Unused		
03A1	Tape Reader Control Panel Assembly	Refer to figure 9-10	
03A2	Tape Reader Assembly	Model RR-1002B-333	16550

Figure 9-1. PTC Replaceable Assemblies (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
03A3	Tape Spooler Assembly	Model RS-500A	16550
03A4	C. E. Panel Assembly	Refer to figure 9-11	
03A5	Gate Assembly	Refer to figure 10-2	
03A6	Power Supply	Model M36-5-0V	09206
03A7	Power Supply	Model M36-5-0V	09206
03A8	Power Supply	Model M15-10-0V	09206
03A9	Power Supply	Model M15-10-0V	09206
03A10	Power Supply	Model M36-10A-0V	09206
03A11	Power Supply	Model M15-30A-0V	09206
03B1	Cable Entry, AC Outlets	(Not Available)	
03B2	Gate Assembly	Refer to figure 10-2	
03B3	Gate Assembly	Refer to figure 10-2	
03B4	Gate Assembly	Refer to figure 10-2	
03B5	Gate Assembly	Refer to figure 10-2	
03B6	Gate Assembly	Refer to figure 10-2	
03B7	Gate Assembly	Refer to figure 10-2	
03B8	Gate Assembly	Refer to figure 10-2	

Figure 9-1. PTC Replaceable Assemblies (Sheet 2)

Vendor Code	Part Number	Nomenclature	Description
03640	6900227	Inhibit Current Control	See figure 10-38

Figure 9-2. Repairable Printed Circuit Board (SMS Card) Assemblies.

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
F1	Fan	480991	88360
Note: Refer to figure 10-29 when replacing parts.			

Figure 9-3. Power Supply Assembly (01B4) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CB1	Circuit Breaker	6080248	03640
CB2	Circuit Breaker	6081594	
CB3	Circuit Breaker	6080356	
F1 1 thru F1 4	Filter	6076162	
K1	Relay	6080429	
K2	Contactoer	6050355	
T1	Transformer	6077905	
XK1	Relay Socket	6080442	
Note: Refer to figure 10-30 when replacing parts.			

Figure 9-4. Interlock and Filter Box Assembly (01B5) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
NA	Differential Card	370612	88360
NA	Over-Voltage Card	370575	88360
Note: Refer to figure 10-31 when replacing parts.			

Figure 9-5. Resonator Supply Assembly (01B6) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
F1	Fan	480991	88360
NA	Differential Card	370612	 —
NA	Differential Card	370613	
NA	Differential Card	370576	
Note: Refer to figure 10-32 when replacing parts.			

Figure 9-6. Power Supply Assembly (01B7) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
F1	Fan	480991	88360
NA	Differential Card	370608	 —
NA	Differential Card	370613	
NA	Over-Voltage Card	370576	
NA	Over-Voltage Card	370578	
Note: Refer to figure 10-33 when replacing parts.			

Figure 9-7. Power Supply Assembly (01B8) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR4	Diode	492543	88360
DS1 thru DS76	Lamp	6078990	03640
S1 thru S4	Switch (Light module 6079720)	6078534	
S5 and S6	Switch (Light module 6078420)	6078534	
S7 thru S14	Switch (Light module 6079720)	6078534	
S15	Switch (Light module 6078420)	6078534	
S16 thru S32	Switch (Light module 6079720)	6078534	
S33	Switch (Light module 6079721)	6078534	
S34 thru S59	Switch (Light module 6079722)	6078534	
S60 thru S62	Switch (Light module 6079732)	6078534	
S63	Switch (Light module 6079719)	6078534	
S64	Switch (Light module 6079732)	6078534	
S65	Switch (Light module 6079719)	6078529	
S66	Switch	6035426	
S67	Switch	6035429	
XDS20	Light Module	6079731	
XDS34	Light Module	6079732	
XDS35 and XDS36	Light Module	6079725	
XDS68	Light Module	6079730	

Figure 9-8. Memory Load and Data Display Panel Assembly (02A1) Replaceable Parts (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
XDS70 thru XDS73	Light Module	6079718	
XDS74	Light Module	6079727	
XDS75	Light Module	6079718	03640
XDS77	Light Module	6079732	03640

Notes: Use switch housing part number 6078422 and screen 6078943 for all switches except S66 and S67.

Refer to figure 10-34 when replacing parts.

Figure 9-8. Memory Load and Data Display Panel Assembly (02A1) Replaceable Parts (Sheet 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR7	Diode	492543	88360
DS1 thru DS74	Lamp	6078990	03640
S1 and S2	Switch (Light module 6079732)	6078529	
S3	Switch (Light module 6080638)	6078529	
S4	Switch (Light module 6079732)	6078534	
S5 thru S7	Switch (Light module 6079732)	6078529	
S8 thru S15	Switch (Light module 6080637)	6078534	
S16	Switch (Light module 6079732)	6078529	
S17	Switch (Light module 6079732)	6078534	
S18 thru S24	Switch (Light module 6080637)	6078534	
S25 and S26	Switch (Light module 6079733)	6078534	
S27	Switch (Light module 6079732)	6078534	
S28	Switch (Light module 6079732)	6078529	
S29 thru S80	Switch	6900674	
S81	Switch	6900229	
S82	Switch (Light module 6079732)	6078534	
S83	Switch (Light module 6079733)	6078534	
S84	Switch (Light module 6079732)	6078534	
S85	Switch (Light module 6079733)	6078534	

Figure 9-9. Processor Panel Assembly (02A2) Replaceable Parts (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
S86	Switch (Light module 6079730)	6078534	03640
XDS1 thru XDS17	Light Module	6079733	
XDS20	Light Module	6079733	
XDS25 thru XDS33	Light Module	6079731	
XDS34 and XDS35	Light Module	6079725	
XDS36 thru XDS40	Light Module	6080637	
XDS41	Light Module	6079733	
XDS62 thru XDS67	Light Module	6079724	
<p>Notes: Use switch housing part number 6078422 and screen 6078943 for all switches except S29 through S81.</p> <p>Refer to figure 10-35 when replacing parts.</p>			

Figure 9-9. Processor Panel Assembly (02A2) Replaceable Parts (Sheet 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR4	Diode	492543	88360
DS1 thru DS22	Lamp	6078990	03640
S1	Switch (Light module 6078918)	6078534	
S2	Switch (Light module 6079719)	6078534	
S3	Switch (Light module 6079719)	6078529	
S4 thru S7	Switch (Light module 6078417)	6078534	
S8	Switch (Light module 6081684)	6078534	
S10	Switch (Light module 6079730)	6078534	
S11	Switch (Light module 6079719)	6078529	
S12 and S13	Switch (Light module 6079732)	6078529	
S14	Switch (Light module 6079730)	6078534	
S15	Switch (Light module (6079733)	6078534	
S16	Switch (Light module 6079732)	6078529	
S17	Switch (Light module 6079732)	6078534	
S18	Switch (Light module 6079719)	6078534	
S19	Switch (Light module 6079723)	6078529	
S20	Switch (Light module 6079730)	6078529	
S21	Switch (Light module 6079732)	6078529	
<p>Notes: Use switch housing part number 6078422 and screen 6078943 for all switches.</p> <p>Refer to figure 10-36 when replacing parts.</p>			

Figure 9-10. Tape Reader Control Panel Assembly (03A1) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR18	Diode	492543	88360
DS1 thru DS54	Lamp	6078990	03640
S2 thru S14	Switch (Light module 6080637)	6078529	
S15	Switch (Light module 6079730)	6078534	
S16	Switch (Light module 6079733)	6078534	
S17	Switch (Light module 6080637)	6078529	
S18	Switch (Light module 6079733)	6078529	
S19	Switch (Light module 6079732)	6078534	
S20 and S21	Switch	6900198	
S22	Switch	6900199	
S23	Switch	6900198	
S24	Switch	6080558	
XDS1 thru XDS33	Light Module	6080636	
XDS51 thru XDS53	Light Module	6079733	
XDS55 thru XDS61	Light Module	6080636	

Notes: Use switch housing part number 6078422 and screen 6078943 for all switches except S20 through S24.

Refer to figure 10-37 when replacing parts.

Figure 9-11. C. E. Panel Assembly (03A4) Replaceable Parts

Vendor Code	Name	Address
03640	International Business Machines Corp.	Owego, N. Y.
09206	Trygon Electronics, Inc.	Roosevelt, N. Y.
14668	California Computer Products, Inc.	Anaheim, California
16550	Rheem Electronics Corp.	Los Angeles, California
88360	International Business Machines Corp.	Endicott, N. Y.

Figure 9-12. Vendor Code Cross-Reference

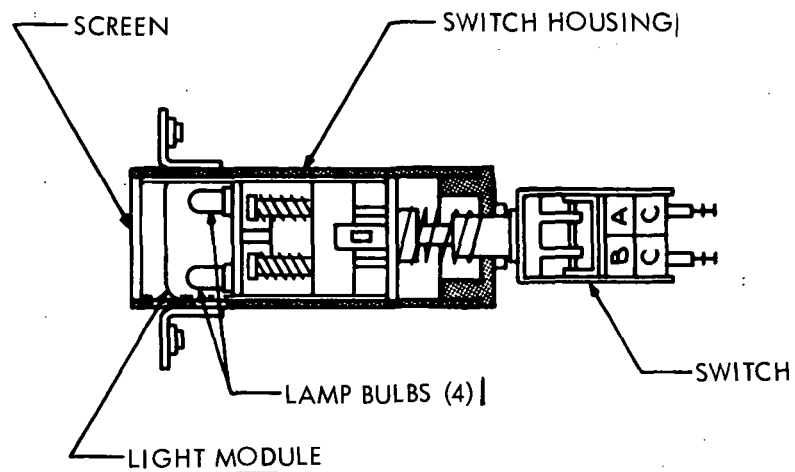


Figure 9-13. Pushbutton Switch Assembly

9-10. WRAPPED CONNECTIONS.

9-11. The wire wrapped connection is a precision pressure junction. A special wrapping tool wraps the stripped end of a wire tightly around the stationary terminal on a gate assembly. The resulting connection is a highly reliable permanent connection because of the high local residual stresses produced in the wire and terminal. Figure 9-14 illustrates a typical wrapped connection. The following paragraphs discuss the processes for using manual tools to wrap and unwrap connections. Recommended tools for wrapped connections are listed on figure 9-15.

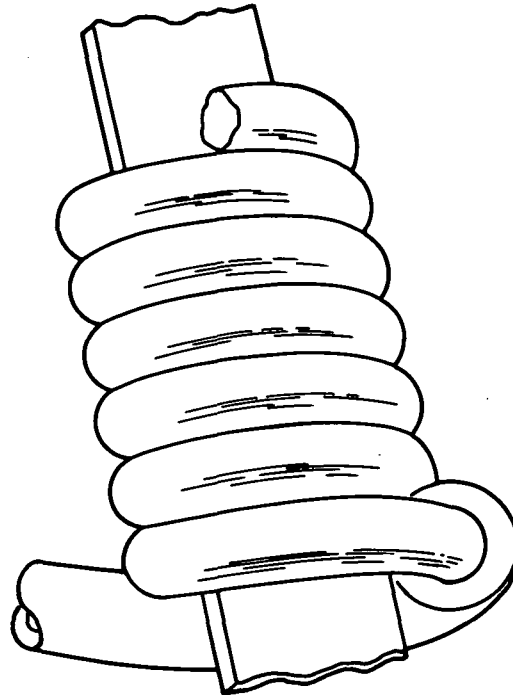


Figure 9-14. Wrapped Connection

Tool	Vendor/Part Number	Description
Hand Unwrap Tool	IBM 6072437	See figure 4-3, part O
Hand Wire Wrap Tool	IBM 6072438	See figure 4-3, part G
Wrapping Bit (No. 20)	Keller A-18633	See figure 4-3, part H
Wrapping Bit (No. 22)	Keller A-18632	
Wrapping Bit (No. 24)	Keller A-26232	
Wrapping Bit (No. 26)	Keller A-27611	
Sleeve (No. 20)	Keller A-18285	See figure 4-3, part I
Sleeve (No. 22, 24)	Keller A-18840	
Sleeve (No. 26)	Keller A-17611-2	

Figure 9-15. Recommended Wrapping Tools
V-9-14

CAUTION

Only nylon-jacketed or semi-rigid PVC (polyvinyl chloride-insulated) wire should be used for re-wiring back panels. Teflon-insulated wire, used in panels produced by automation, is unsuitable for re-wiring in the field due to the difficulty in stripping without damaging the conductor.

9-12. WRAPPING. The following procedure indicates the necessary steps in making a wrapped connection.

- a. Select the bit and sleeve for the wire size to be used.

<u>Wire Size AWG</u>	<u>Wrapping Bit</u>	<u>Sleeve</u>
26	Keller, A-27611	Keller, A-17611-2
24	Keller, A-26232	Keller, A-18840
22	Keller, A-18632	Keller, A-18840
20	Keller, A-18633	Keller, A-18285

- b. Install bit and sleeve in the nose assembly of the wrapping tool (figure 9-16):

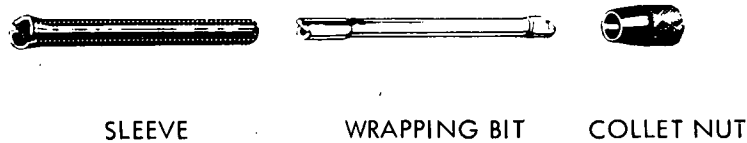


Figure 9-16. Wrapping Tool Assembly

1. Loosen the collet nut on the nose assembly.
 2. Insert the wrapping bit into the collet. Rotate the bit while applying slight pressure against the end until it seats itself. (To remove the bit, reverse this process.)
 3. Place the sleeve over the bit and into the collet. Rotate until sleeve is seated and positioned. Apply slight pressure to the end of the sleeve and tighten collet nut.
- c. Strip 1-3/8 to 1-1/2 inch of insulation from the end of the wire to be wrapped. This will result in about six wraps around the terminal. The completed terminal must have at least five turns of bare wire.

CAUTION

Do not nick or scrape the wire. A nicked wire is subject to breaks that are difficult to detect. Areas where plating is removed will oxidize, causing an unreliable connection.

d. Insert the stripped wire into the small hole of the wrapping bit (figure 9-17, part A) taking care to insert the wire up to the insulation. Do not bend the bare end of the wire; it may be difficult to slide into the bit. If the wire is not inserted in the wrapping bit up to the insulation, a "shiner" (bare wire between insulation and terminal) may result. There should be $1/4$ turn to $3/4$ turn of insulation at the beginning of each wrap, except for coaxial cable. Coaxial cable insulation should not be wrapped, but it must end no more than $1/16$ inch from the terminal.

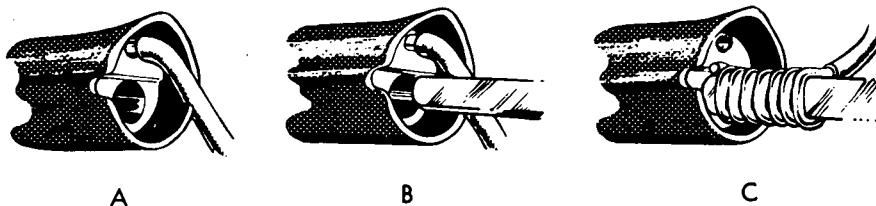


Figure 9-17. Wrapping Procedure

e. Hold the wire with the fingers and bend the insulated portion of the lead into the retaining notch in the sleeve (figure 9-17, part B). Use the right or left notch as determined by the direction of the approach (or exit) of the lead. Place the wrapping bit on the terminal. Be sure the terminal is inserted into the bit as far as it will go. Hold the tool in line with the terminal.

f. Hold the tool on the terminal and squeeze the trigger to wrap the wire on the terminal. The tool will automatically recede as the wire coils on the terminals. Release trigger and remove tool from terminal. The wrapped connection is complete (figure 9-17, part C).

NOTE

If too much pressure is used to push the tool on the terminal, a turn of wire will wrap over a previous turn. If too little pressure is exerted, the adjacent wraps of wire may not touch each other. Maximum separation between individual turns on the terminal must not exceed 0.005 inch, excluding the first and last wrap (figure 9-18).

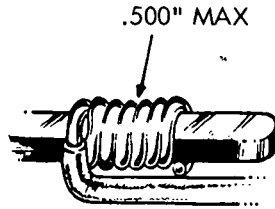


Figure 9-18. Wrap Spacing

9-13. UNWRAPPING. Wires can be removed from a terminal by using the hand unwrap tool illustrated on figure 9-19. This tool can unwrap both right and left-hand wraps.

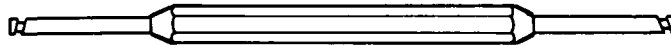


Figure 9-19. Unwrap Tool

9-14. Unwrapping is accomplished by catching the tail of the wire with the unwrap point and turning the tool in a direction opposite to that of the wrap. In some cases, it may be necessary to lift the wire tail away from the pin before the wire can be unwrapped. Apply only enough pressure to loosen turns.

CAUTION

An unwrapped wire must never be rewrapped.
A new wire must be used as a replacement.

Never slide a termination on a pin because this rounds the sharp corner of the pin and makes subsequent connections unreliable. As you unwrap a wire, see that the first coil does not break off and drop into the panel. This breakage is often caused by the lip of the tool not engaging the tail of the wire. Terminals may be wrapped ten times before replacement is necessary.

9-15. **WRAPPED CONNECTION QUALITY.** Because the connection is destroyed if a wrap is disturbed in any manner, it is difficult to determine if a good quality junction has been made. The most common factors causing poor quality wraps are:

1. Incorrect wrapping bit for the wire size in use.
2. Worn or damaged wrapping bit.
3. Dirty wrapping bit.

9-16. A defective wrapped connection may be either too tight or too loose. If the wrap is made too tight, the wire is deformed to such an extent that it becomes brittle. The wire may then break under vibration and handling. A loose wrap will not have sufficient pressure to bond the wire to the terminal.

9-17. SMS back panel wires are frequently routed around, but not attached to, an intermediate terminal. If a wire is pulled too tight or excessive pressure is exerted at the point of contact with the intermediate terminal, insulation damage may result, allowing the wire to short to the terminal. This short may be intermittent. When wiring back panels; do not pull wires tightly around intermediate terminals, or allow a wire to rub along a terminal pin.

9-18. CRIMPED CONNECTIONS.

9-19. A crimped connection is a union of two electrical conductors formed by pressure. A crimped connection is usually made with a terminal that has a barrel or trough to accept a short length of wire. The wire is inserted in the terminal, which is then formed to compress and restrict the wire inside the terminal barrel as indicated on figure 9-20. If the correct pressure is applied during the forming process, a homogeneous mass will result in the crimped area.

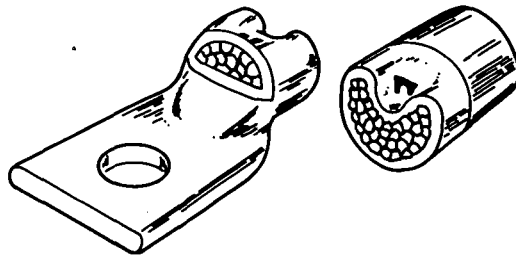


Figure 9-20. Crimped Connection, Cross Section

9-20. The critical factor in making a crimped connection is the extent to which the terminal and conductor are formed. Pressure produced in the process must be high enough to cause a bond between the terminal and conductor materials, yet low enough to prevent embrittlement of the formed parts.

9-21. **RECOMMENDED CRIMPING TOOLS.** Recommended crimping tools and their intended applications are listed in figure 9-21.

9-22. AMP tool 59501 is a ratchet crimping tool to be used with 22-24 AWG solid or stranded wire only. The die-set is not replaceable, and no adjustments are provided on the tool.

Crimping Tool	Application	Description
AMP 59501	Used to crimp AWG 22-24 solid or stranded wire.	See figure 4-3, part Q.
Berg HT-3-20	Used to crimp AWG 20 solid or stranded wire to a slip-on terminal.	See figure 4-3, part R.
Berg HT-3-22	Used to crimp AWG 22 solid or stranded wire to a slip-on terminal.	
Berg HT-3-24	Used to crimp AWG 24 solid or stranded wire to a slip-on terminal.	
Bendix 11-7295	Used to crimp size 12, 16, and 20 type connector contacts.	See figure 4-3, part K.

Figure 9-21. Recommended Crimping Tools

9-23. Terminals used with the AMP ratchet tool have a two-section crimping barrel as illustrated in figure 9-22. The tool crimps one section on the conductor and the other section on the insulation. Make certain to insert terminals into the die so that the larger die opening crimps the insulation.

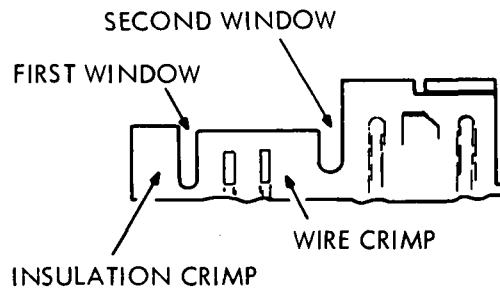


Figure 9-22. Slip-on Connector Terminal

9-24. **CRIMPED CONNECTION QUALITY.** The quality of a crimped connection depends largely on the correct combination of wire, terminal, and tool for each application. The following procedure is recommended for determining the quality of crimped connections:

- a. Visually inspect all completed connections for the following:

CAUTION

Do not use a connection that does not meet these criteria.

1. Stripped portion of the wire centrally located under the crimp.
2. No deformation of the terminal outside of the crimp area.
3. No fractures of the terminal or wire.

- b. Test completed connections having no visual defects as follows:

1. Grip the wire between the thumb and forefinger of one hand and the terminal between the thumb and forefinger of the other hand.
2. Pull the wire, exerting only enough pressure to make the wire taut. Check for any movement of the wire within the terminal barrel.

NOTE

Wire movement in the terminal barrel can often be heard, but not seen. Such a connection is called a clicker and must not be used.

3. Bend the wire about 30 from center and repeat step 2. Bend the wire in the opposite direction about 30 from center and repeat step 2.

9-25. SOLDERED CONNECTIONS

9-26. The soldering process involves six steps: selection of materials, preparing the soldering iron and tip, preparing the work, heating the work, applying the flux and solder, and cooling.

9-27. **SELECTION OF MATERIALS.** Recommended soldering tools are listed in figure 9-23.

CAUTION

Do not use acid-core solder.

Tool	Vendor/Part No.	Description
Soldering Handle	Hexacon P25	See figure 4-3, part E.
Soldering Tip	Hexacon HT248D	See figure 4-3, part F.

Figure 9-23. Recommended Soldering Tools

9-28. Rosin cored wire solder (conforming to Federal Specification QQ-S-571) is similar to a piece of spaghetti; the hollow center is filled with flux that flows over the work when heated to a moderate temperature (about 300° F). This temperature is below the melting point of the solder (about 360° F). The flux becomes active upon further heating, but prolonged exposure to heat causes it to decompose.

9-29. **PREPARING THE SOLDERING IRON AND TIP.** The soldering iron is used only to transmit heat to the work. Before using the iron, heat it to operating temperature and tin it: wip the tip with a clean cloth or canvas; then apply flux and solder, giving the tip a clean, shiny coat of solder. Tinning is done to insure good heat transfer and to keep the connection area free of contamination. Subsequent accumulation of flux residue and solder dross can be removed in the same manner.

9-30. **PREPARING THE WORK.** The work must be clean. No grease, wax, paint, dust or other foreign material should be present on the surfaces to be soldered. These surfaces should be pretinned. Pretinning is the application of a tin layer of solder over the surfaces of the metals to be joined, using the same process as for tinning the soldering iron tip.

9-31. Use extreme care when stripping insulation from wire. The stripping tools should be adjusted so that no metal is removed from the wire during the stripping operation. Cutting the strands in stranded wire reduces the cross-sectional area, which decreases current carrying capacity and presents a mechanically weak spot; a nick in solid wire has much the same effect.

9-32. Unless otherwise specified, insulation should be stripped so that not more than 1/8 inch nor less than 1/16 inch of wire will be exposed between the soldered terminal and the insulation (figure 9-24). Leads of an axial lead component should not be formed closer than 1/16 inch from the component body (figure 9-25).

9-33. **HEATING THE WORK.** The joint must be thoroughly heated before applying solder. Efficient heat transfer from the iron to the work depends on the cleanliness of the surfaces and the size of the contact area. A small amount of clean solder on the iron tip will insure effective heat transfer.

9-34. Poor solder connections are often the result of insufficient heat. Protect components, but remember that a destroyed component is less expensive than a cold soldered joint that causes intermittent failures.

9-35. **APPLYING THE FLUX AND SOLDER.** The solder should be applied to the work, not to the iron. If the surfaces are clean and are at the correct temperature, flux and solder will flow freely over the surfaces and wet the metal. This wetting action is the basic solder bond. After the solder solidifies, it will remain adhered to the surface and will provide electrical continuity.

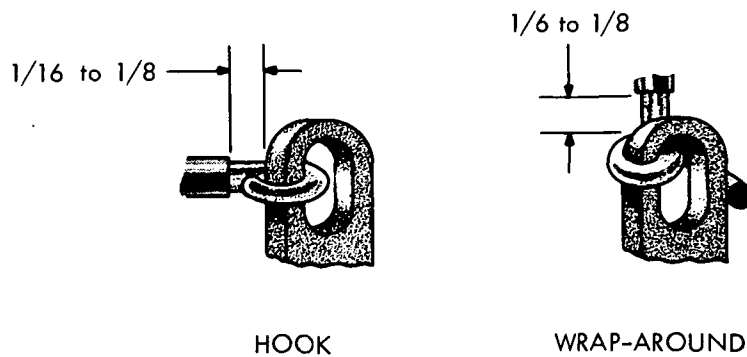


Figure 9-24. Terminal Connections

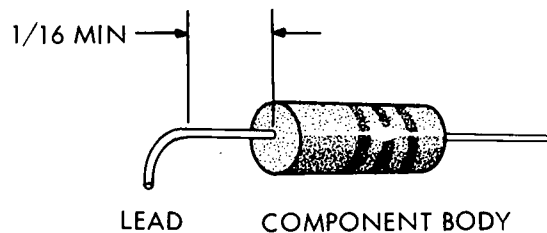


Figure 9-25. Axial Lead Connection

9-36. The proper amount of solder is important. The solder bond occurs on the metal surfaces and excessive solder does not improve the joint but can introduce undesirable side effects. Use enough solder to cover the parts to be joined, but leave the outlines visible.

9-37. **COOLING.** Once the solder has been applied, withdraw the soldering iron and allow the joint to cool. Solidification of solder is not instantaneous, and any movement during this time may cause a solder bond of unacceptable quality. Keep the parts perfectly still until the solder is frozen.

9-38. **VISUAL INSPECTION.** A good soldered connection is bright and smooth. The solder feathers out to a thin edge from the main body of solder in the joint. It also approximately outlines the wire and terminal. Figure 9-26 illustrates good soldered connections.

9-39. Figure 9-27 illustrates defective soldered connections.

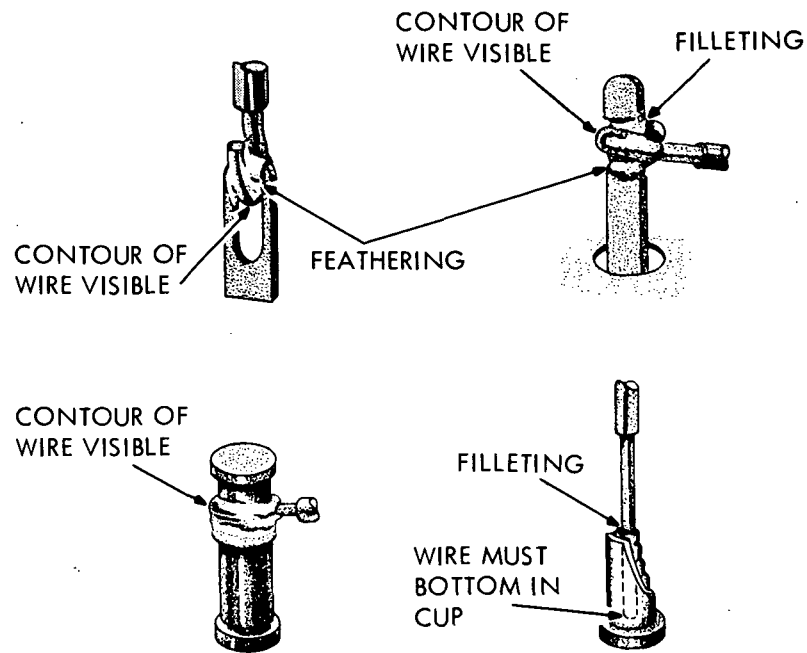


Figure 9-26. Good Soldered Connections

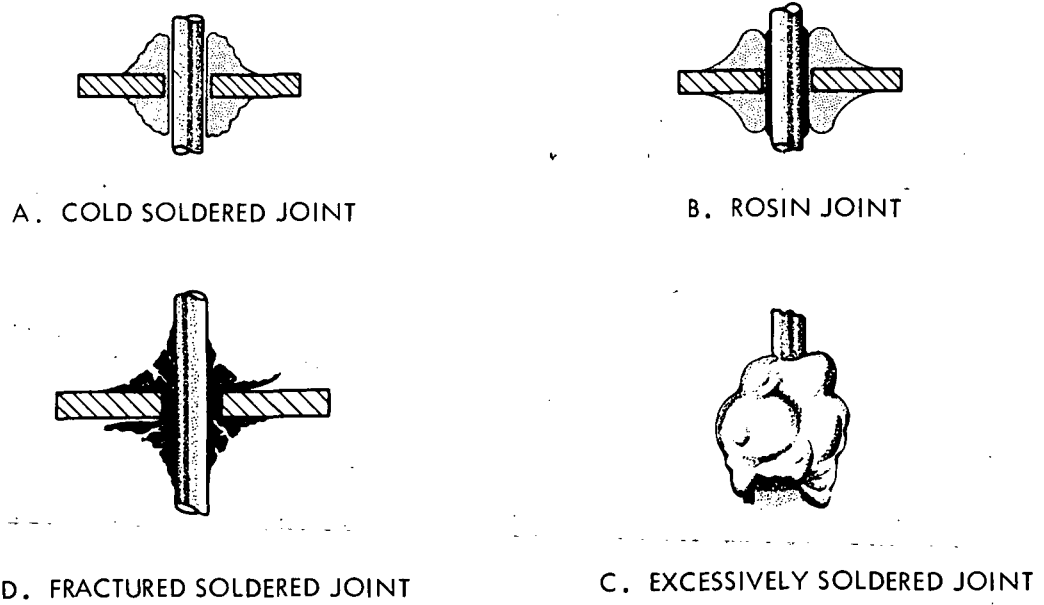


Figure 9-27. Defective Soldered Connections

9-40. The Cold Soldered Joint (figure 9-27, part A) has a dull, granular appearance. It is caused by insufficient heating, or movement of the work during cooling.

9-41. The Rosin Joint (figure 9-27, part B) has a rosin inclusion. Rosin joints can be due to insufficient heat to permit the rosin to be displaced by the solder, or insufficient heat to permit adequate melting of the flux.

9-42. The Excessively Soldered Joint (figure 9-27, part C) hides the outline of the joint components with an excessive amount of solder.

9-43. The Fractured Soldered Joint (figure 9-27, part D) is one in which small cracks are present. This condition can be due to stress applied before the solder is completely solidified.

9-44. SMS CARD REPLACEMENT.

9-45. The SMS card puller (IBM 6072429) facilitates insertion or removal of SMS cards from their sockets. Use of this tool reduces the probability of dropping cards and other handling damage. This tool is illustrated on figure 4-3, part A.

9-46. In operation, the card puller fits over the edges of an SMS card. When the tool is properly positioned, a tooth on the spring-loaded latch seats in a hole in the card. The card is released by depressing the latch.

CAUTION

Before removing an SMS card, insert IBM punched cards or similar material between the card to be removed and adjacent SMS cards. Damage to SMS cards or components may be eliminated in this manner.

Oil or moisture from the fingers can critically decrease the insulation resistance on the land pattern side of the card. Cards should be carefully handled by the edges only.

9-47. When an SMS card is removed from its socket, the card contacts should be cleaned and lubricated before the card is reinstalled if either of the following conditions exists:

1. The card contacts are visibly contaminated.
2. The card contacts have been handled. If there is any doubt about the contamination of the contacts, clean and relubricate them.

9-48. The following cleaning and lubricating procedure insures low contact resistance and reduces wear of the gold-plated contact surfaces. The procedure may be performed any number of times without affecting contact reliability. To clean and lubricate the contacts:

- a. Apply lubricant (IBM part number 6072430) either directly to the contacts or indirectly with a saturated, clean, lint-free cloth or tissue.
- b. Wipe the contacts toward the component section of the card with a cloth or tissue moistened with the lubricant.

CAUTION

Do not allow the lubricant to contact the clear plastic coating on the component portion of the card. The solvents in the lubricant can dissolve the plastic coating, which will act as an insulator if rubbed on the contacts.

- c. Rub the contacts with a clean, dry piece of cloth or tissue until there is no visible trace of the lubricant. The cloth or tissue will darken if further cleaning is necessary. Repeat the procedure from step a if further cleaning is needed.

9-49. SMS CARD REPAIR.

9-50. Repair of printed circuit cards primarily consists of soldering and unsoldering operations. The specific jobs involved are:

1. Removal of defective components.
2. Installation of replacement components.
3. Joining broken printed conductors.

9-51. Care must be taken to avoid damage to the card assembly during the repair process. The card assembly is easily damaged in two ways:

1. Heat damage to the card or to components on the card.
2. Physical damage.

9-52. The card is made of an insulating material that will withstand a dipsolder temperature of about 515° F for 30 seconds. This compares with a minimum solder melting temperature of 361° F and an average soldering iron temperature of 750° F. This means that the soldering iron must contact the card for only a short interval of time. Excessive heat may damage a card in two ways by:

1. Destroying the bond between the insulated board and a printed conductor, resulting in a raised conductor;
2. Scorching or burning the board.

9-53. Excessive heat may also damage components on the card. Semiconductors are especially sensitive to heat. Use of the soldering tools recommended under **SOLDERED CONNECTIONS** will help avoid heat damage.

9-54. Physical damage in the form of a raised conductor is easily inflicted if stress is applied in a direction that tends to separate the conductor from the board (figure 9-28).

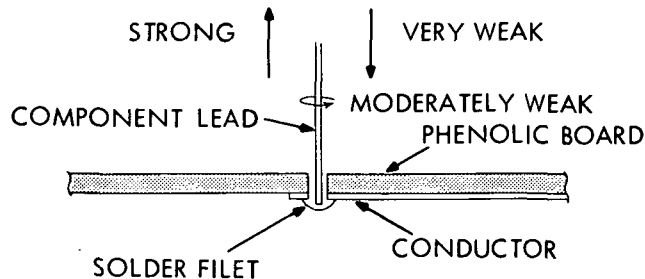


Figure 9-28. Stress Applied to Component Leads

9-55. **COMPONENT REMOVAL.** When the leads of the defective component must be saved, use the following procedure to remove the component:

a. Straighten the component leads that are bent over on the wiring side of the board. Figure 9-29 illustrates a method of using the soldering iron tip as a wedge to prevent pulling the land away from the board. A pair of long-nose pliers may be used on the component side of the card to prevent downward movement of the lead.

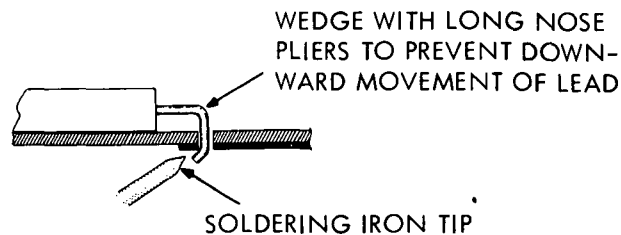


Figure 9-29. Component Removal

b. Heat the component leads and pull them through the holes from the component side of the board.

9-56. If the leads of the defective component may be destroyed, use the following removal procedure:

a. Cut the leads of the defective component as close as possible to the board on the component side of the card. Do not damage the board or adjacent components.

- b. Hold the card in your hand and use a clean, tinned soldering iron to heat the solder connection between the remaining portion of the leads and the conductor pattern.
- c. When the solder starts to flow, rap the hand holding the card on the work surface.
- d. Repeat steps b and c if the solder and piece of lead do not leave the hole.

9-57. **COMPONENT INSTALLATION.** Use the following procedure for installing components on SMS cards.

- a. Insert component leads through the holes in the board. Cut the leads so that about 1/16 inch remains to bend over on the conductor pattern. Bend the leads parallel to the component body and toward each other. Axial lead components, such as resistors, are mounted flush against the surface of the board.

CAUTION

Do not bend leads close to components (see **SOLDERED CONNECTIONS** for technique). The leads on tantalum capacitors are particularly subject to damage.

- b. Solder the component leads to the conductor pattern. Avoid excessive heat and solder, particularly with transistors and diodes. It is not desirable to fill the hole in the board with solder.
- c. Wash the general area of repair using a typewriter cleaning brush and IBM cleaning fluid (IBM part number 450608). Dry the affected area by wiping with a clean piece of cloth or tissue.

9-58. **PRINTED CONDUCTOR REPAIR.** Two printed conductor defects may be found: broken conductor, or delaminated conductor (raised land).

9-59. To repair a broken conductor, solder a 24 AWG solid wire jumper across the break. The wire should overlap the printed conductor at least 1/16 inch on each end. If the break is long, and the possibility of a short exists, use insulated wire stripped on each end.

9-60. To repair a delaminated conductor, cut both ends of the loose section at a point where the bond is not broken. After the loose section is removed, repair the conductor using the same method used for a broken conductor.

9-61. **EXTERIOR SURFACE COATINGS.**

9-62. Figure 9-30 lists the solvents, reducers, primers and paints needed to refurbish PTC coatings that become chipped, discolored, or otherwise defective.

NOTE

The dark gray, white, and black paints listed in figure 9-30 for the functional areas and panel markings are actually vinyl inks, originally applied by silk screen processes.

9-63. REPAINTING TECHNIQUES.

9-64. The following paragraphs indicate the recommended consistencies for the paints and other fluids needed to repair the exterior coatings of the PTC. A fine brush should be used to retouch defective panel markings and any small scratches on the PTC. For repainting areas greater than 1 in. square, the paint should be applied by spraying.

9-65. SOLVENTS. The surface to be repainted should be thoroughly cleaned by wiping it with the solvent indicated in figure 9-30. The surface should then be allowed to dry for at least 30 minutes.

9-66. PRIMERS. If the coating has been marred so that the metal surface is exposed, a primer coating should be applied before the paint is applied. The primer need not be diluted for brush application; however, for spray application the primer should be diluted with one part reducer to two parts primer. The primer coating should be air dried for at least three minutes before paint is applied.

9-67. PAINTS. The paints need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to four parts paint. Four or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. For a non-textured finish, these applications are the finish coat; however, for a textured finish these applications are only the first finish coat.

NOTE

The number of paint coats required to adequately repair the defective surface depends on the depth of the defect and the thickness of the original coatings.

9-68. If the final surface is to be textured, a second finish coat of paint should be applied after the first finish coat has been air dried. The paint for this second finish coat need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to eight parts paint. Five or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. (See note in preceding paragraph.)

9-69. TEXTURING AGENT. The texturing agent should not be diluted before being sprayed as a fine mist coat over the second finish coat.

Surface	Solvent	Reducer*	Primer*	Paint (Vinyl)*	Notes*
Frame Covers	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903	Charcoal-John L. Armitage Co., P-318	Deep Charcoal-John L. Armitage Co., U-211.	Use texturing agent, John L. Armitage Co., M-411.
Feature Strips Control Panels Background Functional Areas		John L. Armitage Co., A-903 or M-130.	Blue-Gray, John L. Armitage Co., P-350.	Light Gray-John L. Armitage Co., U-662S.	
Panel Markings				Dark Gray-John L. Armitage Co., M-1085.	
				White-John L. Armitage Co., M-1027.	Used on Dark Gray functional areas.
				Black-John L. Armitage Co., M-1035.	Used on Light Gray areas.
Name Plate	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903, or M-130.	Yellow-John L. Armitage Co., P-321.	Yellow-John L. Armitage Co., U-396.	
			Blue-John L. Armitage Co., P-300.	Sky Blue-John L. Armitage Co., U-333.	
				White-John L. Armitage Co., M-1027.	Used as a filler for engraving.
*Equivalent materials may be used.					

Figure 9-30. Recommended Repainting Materials

SECTION X

DIAGRAMS

10-1. SCOPE.

10-2. This section contains three types of Engineering drawings required for maintenance of the PTC (Electrical Schematic Diagrams, Second Level Logic Diagrams, and Assembly Drawings) as follows:

- Figure 10-7. Filter and Interlock Box Assembly (01B5) Electrical Schematic Diagram (LN 00. 03. 10. 0)
- Figure 10-8. Relay Gate Assembly (03A5) Electrical Schematic Diagram (LN 00. 03. 20. 0 and LN 00. 03. 20. 1)
- Figure 10-9. AC Power Distribution (01 Frame) Diagram (LN 00. 03. 30. 0)
- Figure 10-10. AC Power Distribution (02 and 03 Frames) Diagram (LN 00. 03. 40. 0)
- Figure 10-11. DC Power Distribution (01 Frame) Diagram (LN 00. 03. 50. 0)
- Figure 10-12. DC Power Distribution (02 and 03 Frames) Diagram (LN 00. 03. 60. 0, LN 00. 03. 60. 1, LN 00. 03. 60. 2 and LN 00. 03. 60. 3)
- Figure 10-13. 115 VAC System Flow Diagram (LN 00. 03. 70. 0, LN 00. 03. 70. 1, LN 00. 03. 70. 2 and LN 00. 03. 70. 3)
- Figure 10-14. AC Power Control Signal Flow Diagram (LN 00. 03. 70. 4)
- Figure 10-15. Chassis Ground System Flow Diagram (LN 00. 03. 71. 0)
- Figure 10-16. Bus Bar System Flow Diagram (LN 00. 03. 72. 0)
- Figure 10-17. +30 VDC System Flow Diagram (LN 00. 03. 73. 0)
- Figure 10-18. +12 VDC System Flow Diagram (LN 00. 03. 74. 0)
- Figure 10-19. -12 VDC System Flow Diagram (LN 00. 03. 75. 0)
- Figure 10-20. -28 VDC System Flow Diagram (LN 00. 03. 76. 0)
- Figure 10-21. -48, -20, and -6 VDC System Flow Diagram (LN 00. 03. 77. 0)
- Figure 10-22. Relay Cross Reference List
- Figure 10-23. Tape Reader Control Panel Assembly (03A1) Electrical Schematic Diagram (LN 00. 04. 01. 0 and LN 00. 04. 01. 1)
- Figure 10-24. C. E. Panel Assembly (03A4) Electrical Schematic Diagram (LN 00. 04. 05. 0, LN 00. 04. 05. 1 and LN 00. 04. 05. 2)

- Figure 10-25. Memory Load and Data Display Panel Assembly (02A1) Electrical Schematic Diagram (LN 00. 04. 10. 0, LN 00. 04. 10. 1, LN 00. 04. 10. 2 and LN 00. 04. 10. 3)
- Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4)
- Figure 10-27. Memory AC-DC Power Diagram (LN 00. 04. 20. 1 and 00. 04. 20. 0)
- Figure 10-28. PTC Second Level Logic Diagrams
- Figure 10-29. Power Supply Assembly (01B4) Assembly Drawing
- Figure 10-30. Filter and Interlock Box Assembly (01B5) Assembly Drawing
- Figure 10-31. Resonator Supply Assembly (01B6) Assembly Drawing
- Figure 10-32. Power Supply Assembly (01B7) Assembly Drawing
- Figure 10-33. Power Supply Assembly (01B8) Assembly Drawing
- Figure 10-34. Memory Load and Data Display Panel Assembly (02A1) Assembly Drawing
- Figure 10-35. Processor Display Panel Assembly (02A2) Assembly Drawing
- Figure 10-36. Tape Reader Control Panel Assembly (03A1) Assembly Drawing
- Figure 10-37. C. E. Panel Assembly (03A4) Assembly Drawing
- Figure 10-38. Inhibit Current Control Printed Circuit Board Assembly (6900227)
- Figure 10-39. SDTDL 2. 048 MC Oscillator Printed Circuit Board Assembly (6901352)

10-3. Automated Logic Diagrams (ALD's), Circuit Card Location Charts, and Edge Connector Lists are not included in this manual; they are supplied in a set of five volumes entitled SATURN V LTE - Programmable Test Controller Automated Logic Diagrams. However, the ALD page format and the contents of the Circuit Card Location Charts and Edge Connector Lists are explained in this section.

10-4. DRAWING REFERENCES.

10-5. References are made between and within the Electrical Schematic Diagrams, ALD's, Circuit Card Location Charts, and Edge Connector Lists by an "LN" seven digit number (XX. XX. XX. X) assigned to each page (or sheet). The LN number indicates the type of drawing as follows:

1. Electrical Schematic Diagrams - LN 00. 03. XX. X or LN 00. 04. XX. X
2. Signal Interface List - 04. XX. XX. X
3. ALD's, Circuit Card Location Charts and Edge Connector Lists - LN 05. XX. XX. X

The digit positions filled here by X's specify the page number sequence.

10-6. Figure 10-1 lists the PTC ALD's by logic page (LN) number and page part number. The page part number is used for ordering a specific page. Figure 10-2 lists the Circuit Card Location Charts and figure 10-3 lists the Edge Connector Lists in alpha numeric order by PTC gate assembly. The page part number, page (LN) number and the number of sheets for each gate assembly are given for ordering a specific page or series of pages.

10-7. When tracing signals from page-to-page of the ALD's or from pages of the ALD's to the panel assembly electrical schematic diagrams, the LN number is used to locate the origin or destination of the signals. Reference from one page of the ALD's to another page is designated by a 05. XX. XX. X LN number. However when tracing signals between the ALD pages and the panel assembly electrical schematic diagrams, a 04. XX. XX. X LN number is used. This LN number (04. XX. XX. X) references a sheet of the Signal Interface List, figure 10-4. The Signal Interface List gives the origins and destinations of the interface signals. Sheet 1 of figure 10-4 is the table of contents for the remaining sheets and may be used for locating interface signals between assemblies of the PTC.

10-8. SECOND LEVEL LOGIC DIAGRAMS.

10-9. Second level logic diagrams are so called because they do not contain the degree of detail found on the automated or "first level" logic diagrams. Second level logic diagrams do not contain such details as pin connection designations, voltage levels, SMS card types, or location of SMS cards in the gate assemblies; all these details are included on the automated logic diagrams.

10-10. The second level logic diagrams (figure 10-28) are provided to aid in the logical analysis of the PTC. These diagrams are arranged by PTC functions. Included with these diagrams is the chart of logic symbol definitions (figure 10-28, sheets 1 and 2) which define the logic symbols used in these diagrams. A block diagram (figure 10-28, sheet 3) showing the relationship of the PTC functions is also included.

NOTE

The Logic Symbols listing (located at the end of this Volume) also defines each second level logic symbol and the corresponding ALD symbol.

10-11. In the lower left corner of each second level logic diagram except sheets 1, 2, and 3 is a table which lists (by LN number) the ALD pages that are represented on the diagram.

10-12. In the upper left corner of each second level diagram except sheets 1, 2, and 3 are tables that list (by sheet number) the origins of the input signals to the sheet and the destinations of the outputs from the sheet; however, common timing signals and signals whose origin or destination is on the Electrical Schematic Diagrams are not listed in these tables.

Logic Page Number	Page Part Number	Logic Page Number	Page Part Number	Logic Page Number	Page Part Number
05.02.01.1	6903405	05.03.26.1	6903458	05.06.04.1	6903203
05.02.02.1	6903406	05.03.27.1	6903459	05.06.05.1	6903204
05.03.03.1	6903407	05.03.28.1	6903460	05.06.06.1	6903205
05.02.04.1	6903408	05.04.01.1	6903746	05.06.06.2	6903372
05.02.05.1	6903409	05.04.02.1	6903747	05.06.07.1	6903206
05.02.06.1	6903410	05.04.03.1	6903748	05.06.07.2	6903373
05.02.07.1	6903411	05.04.04.1	6903749	05.06.08.1	6903207
05.02.08.1	6903412	05.04.05.1	6903750	05.06.09.1	6903208
05.02.09.1	6903413	05.04.06.1	6903751	05.06.11.1	6903210
05.02.10.1	6903414	05.04.07.1	6903752	05.06.12.1	6903211
05.02.11.1	6903415	05.04.08.1	6903753	05.06.13.1	6903212
05.02.12.1	6903416	05.04.09.1	6903754	05.06.14.1	6903213
05.02.13.1	6903417	05.04.10.1	6903755	05.06.15.1	6903214
05.02.14.1	6903418	05.04.11.1	6903756	05.06.16.1	6903215
05.02.15.1	6903419	05.04.12.1	6903757	05.06.17.1	6903216
05.02.16.1	6903420	05.04.12.2	None	05.06.18.1	6903217
50.02.17.1	6903421	05.04.12.3	None	05.06.19.1	6903218
05.02.18.1	6903422	05.04.13.1	6903758	05.06.20.1	6903219
05.02.19.1	6903423	05.04.14.1	6903759	05.06.21.1	6903220
05.02.20.1	6903424	05.04.15.1	6903760	05.06.22.1	6903221
05.02.21.1	6903425	05.04.16.1	6903761	05.06.23.1	6903222
05.02.22.1	6903426	05.05.01.1	6900300	05.06.24.1	6903223
05.02.23.1	6903427	05.05.02.1	6900301	05.06.25.1	6903224
05.03.01.1	6903433	05.05.03.1	6900302	05.06.26.1	6903225
05.03.02.1	6903434	05.05.04.1	6900303	05.06.27.1	6903226
05.03.03.1	6903435	05.05.05.1	6900304	05.06.28.1	6903227
05.03.04.1	6903436	05.05.06.1	6900305	05.06.29.1	6903228
05.03.05.1	6903437	05.05.07.1	6900306	05.06.30.1	6903229
05.03.06.1	6903438	05.05.08.1	6900307	05.06.31.1	6903230
05.03.07.1	6903439	05.05.09.1	6900308	05.06.32.1	6903231
05.03.08.1	6903440	05.05.10.1	6900309	05.07.01.1	6903150
05.03.09.1	6903441	05.05.11.1	6900310	05.07.02.1	6903151
05.03.10.1	6903442	05.05.12.1	6900311	05.07.03.1	6903152
05.03.11.1	6903443	05.05.13.1	6900312	05.07.04.1	6903153
05.03.12.1	6903444	05.05.14.1	6900313	05.07.05.1	6903154
05.03.13.1	6903445	05.05.15.1	6900314	05.07.06.1	6903155
05.03.14.1	6903446	05.05.16.1	6900315	05.07.07.1	6903156
05.03.15.1	6903447	05.05.17.1	6900316	05.07.08.1	6903157
05.03.16.1	6903448	05.05.18.1	6900317	05.07.09.1	6903158
05.03.17.1	6903449	05.05.19.1	6900318	05.07.10.1	6903159
05.03.18.1	6903450	05.05.20.1	6900319	05.07.11.1	6903160
05.03.19.1	6903451	05.05.21.1	6900320	05.07.12.1	6903161
05.03.20.1	6903452	05.05.22.1	6900321	05.07.13.1	6903162
05.03.21.1	6903453	05.05.23.1	6900322	05.07.14.1	6903163
05.03.22.1	6903454	05.05.24.1	7900323	05.07.15.1	6903164
05.03.23.1	6903455	05.05.25.1	6900324	05.07.16.1	6903165
05.03.24.1	6903456	05.05.26.1	6900325	05.07.17.1	6903166
05.03.25.1	6903457	05.05.27.1	6900326	05.07.18.1	6903167

Figure 10-1. PTC Automated Logic Diagrams (Sheet 1 of 3)

Logic Page Number	Page Part Number	Logic Page Number	Page Part Number	Logic Page Number	Page Part Number
05. 07. 19. 1	6903168	05. 09. 15. 1	6903344	05. 13. 16. 1	6903192
05. 07. 20. 1	6903169	05. 09. 16. 1	6903345	05. 13. 17. 1	6903193
05. 07. 21. 1	6903170	05. 09. 17. 1	6903346	05. 13. 18. 1	6903194
05. 07. 22. 1	6903171	05. 09. 18. 1	6903347	05. 13. 19. 1	6903195
05. 07. 23. 1	6903172	05. 10. 01. 1	6903463	05. 13. 20. 1	6903196
05. 07. 24. 1	6903173	05. 10. 02. 1	6903464	05. 13. 21. 1	6903197
05. 07. 25. 1	6903174	05. 10. 03. 1	6903465	05. 13. 22. 1	6903198
05. 07. 26. 1	6903175	05. 10. 04. 1	6903466	05. 14. 01. 1	6903375
05. 07. 27. 1	6903233	05. 10. 05. 1	6903467	05. 14. 02. 1	6903376
05. 08. 01. 1	6903475	05. 10. 06. 1	6903468	05. 14. 03. 1	6903377
05. 08. 02. 1	6903476	05. 10. 07. 1	6903469	05. 14. 04. 1	6903378
05. 08. 02. 2	6903477	05. 10. 08. 1	6903470	05. 14. 05. 1	6903379
05. 08. 03. 1	6903478	05. 10. 09. 1	6903471	05. 14. 06. 1	6903380
05. 08. 04. 1	6903479	05. 10. 10. 1	6903472	05. 14. 07. 1	6903381
05. 08. 05. 1	6903480	05. 10. 11. 1	6903473	05. 14. 08. 1	6903382
05. 08. 06. 1	6903481	05. 10. 12. 1	6903474	05. 14. 09. 1	6903383
05. 08. 07. 1	6903482	05. 11. 01. 1	6903725	05. 14. 10. 1	6903384
05. 08. 08. 1	6903483	05. 11. 02. 1	6903726	05. 14. 11. 1	6903385
05. 08. 09. 1	6903484	05. 11. 03. 1	6903727	05. 14. 12. 1	6903386
05. 08. 10. 1	6903485	05. 11. 04. 1	6903728	05. 13. 13. 1	6903387
05. 08. 11. 1	6903486	05. 11. 05. 1	6903729	05. 14. 14. 1	6903388
05. 08. 12. 1	6903487	05. 11. 06. 1	6903730	05. 14. 15. 1	6903389
05. 08. 13. 1	6903488	05. 11. 07. 1	6903731	05. 14. 16. 1	6903390
05. 08. 14. 1	6903489	05. 11. 08. 1	6903732	05. 14. 17. 1	6903391
05. 08. 15. 1	6903490	05. 11. 09. 1	6903733	05. 14. 18. 1	6903392
05. 08. 16. 1	6903491	05. 11. 10. 1	6903734	05. 14. 19. 1	6903393
05. 08. 17. 1	6903492	05. 11. 11. 1	6903735	05. 14. 20. 1	6903394
05. 08. 18. 1	6903493	05. 11. 12. 1	6903736	05. 14. 21. 1	6903395
05. 08. 19. 1	6903494	05. 11. 13. 1	6903737	05. 14. 22. 1	6903396
05. 08. 20. 1	6903495	05. 11. 14. 1	6903738	05. 14. 23. 1	6903397
05. 08. 21. 1	6903496	05. 11. 15. 1	6903739	05. 15. 01. 1	6903350
05. 08. 22. 1	6903497	05. 11. 16. 1	6903740	05. 15. 02. 1	6903351
05. 08. 23. 1	6903498	05. 11. 17. 1	6903741	05. 15. 03. 1	6903352
05. 08. 24. 1	6903499	05. 13. 01. 1	6903177	05. 15. 04. 1	6903353
05. 09. 01. 1	6903330	05. 13. 02. 1	6903178	05. 15. 05. 1	6903354
05. 09. 02. 1	6903331	05. 13. 03. 1	6903179	05. 15. 06. 1	6903355
05. 09. 03. 1	6903332	05. 13. 04. 1	6903180	05. 15. 07. 1	6903356
05. 09. 04. 1	6903333	05. 13. 05. 1	6903181	05. 15. 08. 1	6903357
05. 09. 05. 1	6903334	05. 13. 06. 1	6903182	05. 15. 09. 1	6903358
05. 09. 06. 1	6903335	05. 13. 07. 1	6903183	05. 15. 10. 1	6903359
05. 09. 07. 1	6903336	05. 13. 08. 1	6903184	05. 15. 11. 1	6903360
05. 09. 08. 1	6903337	05. 13. 09. 1	6903185	05. 15. 12. 1	6903361
05. 09. 09. 1	6903338	05. 13. 10. 1	6903186	05. 15. 13. 1	6903362
05. 09. 10. 1	6903339	05. 13. 11. 1	6903187	05. 15. 14. 1	6903363
05. 09. 11. 1	6903340	05. 13. 12. 1	6903188	05. 15. 15. 1	6903364
05. 09. 12. 1	6903341	05. 13. 13. 1	6903189	05. 15. 16. 1	6903365
05. 09. 13. 1	6903342	05. 13. 14. 1	6903190	05. 15. 17. 1	6903366
05. 09. 14. 1	6903343	05. 13. 15. 1	6903191	05. 15. 18. 1	6903367

Figure 10-1. PTC Automated Logic Diagrams (Sheet 2)

Logic Page Number	Page Part Number	Logic Page Number	Page Part Number	Logic Page Number	Page Part Number
05. 15. 19. 1	6903368	05. 20. 04. 1	6900353	05. 26. 06. 1	6903283
05. 15. 20. 1	6903369	05. 20. 05. 1	6900354	05. 26. 07. 1	6903284
05. 15. 21. 1	6903370	05. 20. 06. 1	6900355	05. 26. 08. 1	6903285
05. 15. 22. 1	6903371	05. 20. 07. 1	6900356	05. 26. 09. 1	6903286
05. 16. 01. 1	6903245	05. 20. 08. 1	6900357	05. 27. 01. 1	6903287
05. 16. 02. 1	6903246	05. 20. 09. 1	6900358	05. 27. 02. 1	6903288
05. 16. 03. 1	6903247	05. 20. 10. 1	6900359	05. 27. 03. 1	6903289
05. 16. 04. 1	6903248	05. 20. 11. 1	6900360	05. 27. 04. 1	6903290
05. 16. 05. 1	6903249	05. 20. 12. 1	6900361	05. 27. 05. 1	6903291
05. 16. 06. 1	6903250	05. 20. 13. 1	6900362	05. 27. 06. 1	6903292
05. 16. 07. 1	6903251	05. 20. 14. 1	6900363	05. 27. 07. 1	6903293
05. 16. 08. 1	6903252	05. 20. 15. 1	6900364	05. 27. 08. 1	6903294
05. 16. 09. 1	6903253	05. 20. 16. 1	6900365	05. 27. 09. 1	6903295
05. 16. 10. 1	6903254	05. 20. 17. 1	6900366	05. 27. 10. 1	6903296
05. 16. 11. 1	6903255	05. 20. 18. 1	6900367	05. 27. 11. 1	6903297
05. 16. 12. 1	6903256	05. 20. 19. 1	6900368	05. 27. 12. 1	6903298
05. 16. 13. 1	6903257	05. 20. 20. 1	6900369	05. 27. 13. 1	6903299
05. 16. 14. 1	6903258	05. 20. 21. 1	6900370	05. 27. 14. 1	6903300
05. 16. 15. 1	6903259	05. 20. 22. 1	6900371	05. 27. 15. 1	6903301
05. 16. 16. 1	6903260	05. 20. 23. 1	6900372	05. 27. 16. 1	6903302
05. 16. 17. 1	6903261	05. 20. 24. 1	6900373	05. 27. 17. 1	6903303
05. 16. 18. 1	6903262	05. 26. 01. 1	6903278	05. 28. 01. 1	6903274
05. 16. 19. 1	6903263	05. 26. 02. 1	6903279	05. 28. 02. 1	6903275
05. 20. 01. 1	6900350	05. 26. 03. 1	6903280	05. 28. 03. 1	6903276
05. 20. 02. 1	6900351	05. 26. 04. 1	6903281	05. 28. 04. 1	6903277
05. 20. 03. 1	6900352	05. 26. 05. 1	6903282		

Figure 10-1. PTC Automated Logic Diagrams (Sheet 3)

Gate Assembly	Page Part Number	"LN" Number	Number of Sheets
01B1	6900328	05. 09. 00. 1	3
01B2	6900329	05. 10. 00. 1	2
01B3	6900330	05. 11. 00. 1	3
02A4	6903310	05. 26. 00. 1	2
02A5	6903311	05. 27. 00. 1	2
02A6	6903312	05. 28. 00. 1	2
02B1	6900331	05. 05. 00. 1	4
02B2	6900332	05. 06. 00. 1	3
02B3	6900333	05. 07. 00. 1	3
02B4	6900334	05. 08. 00. 1	2
02B5	6900335	05. 20. 00. 1	3
03B2	6900339	05. 02. 00. 1	2
03B3	6900340	05. 03. 00. 1	2
03B4	6900341	05. 04. 00. 1	2
03B5	6900342	05. 16. 00. 1	3
03B6	6900343	05. 15. 00. 1	2
03B7	6900344	05. 14. 00. 1	3
03B8	6900345	05. 13. 00. 1	1

Figure 10-2. PTC Circuit Card Location Charts

Gate Assembly	Page Part Number	"LN" Number	Number of Sheets
01B1	6900375	05. 09. 00. 2	3
01B2	6900376	05. 10. 00. 2	1
01B3	6900377	05. 11. 00. 2	2
02A4	6903313	05. 26. 00. 2	4
02A5	6903314	05. 27. 00. 2	3
02A6	6903315	05. 28. 00. 2	1
02B1	6900378	05. 05. 00. 2	4
02B2	6900379	05. 06. 00. 2	4
02B3	6900380	05. 07. 00. 2	4
02B4	6900381	05. 08. 00. 2	4
02B5	6900382	05. 20. 00. 2	3
03B2	6900386	05. 02. 00. 2	3
03B3	6900387	05. 03. 00. 2	5
03B4	6900388	05. 04. 00. 2	4
03B5	6900389	05. 16. 00. 2	4
03B6	6900390	05. 15. 00. 2	3
03B7	6900391	05. 14. 00. 2	4
03B8	6900392	05. 13. 00. 2	4

Figure 10-3. PTC Edge Connector Lists

10-13. AUTOMATED LOGIC DIAGRAMS (ALD's).

10-14. PAGE LAYOUT. Each ALD page contains page identification, edge information, logic blocks, connecting lines, and an area for comments. Figure 10-5 shows a typical logic page. Each page has a possible logic format of five blocks wide and nine blocks long, so logic blocks can occupy any of 45 possible positions.

10-15. PAGE IDENTIFICATION. As shown on figure 10-5, the following information appears at the top of each logic diagram page:

- a. Page part number (1), used for ordering a specific page or series of pages.
- b. Title (2), a description of the logic contained on the page.
- c. Equipment name or code number (3).
- d. Logic page (LN) number (4), a seven-digit number (05. xx. xx. x) assigned to the page. (Refer to paragraph 10-5 for the explanation of the seven digits in the LN number.)

10-16. SIGNAL LINES. All lines entering or leaving a logic page are labeled to correspond to the labeling on the logic page to which they interconnect. Lines enter on the left side of the page and leave on the right side of the page. If a line leaves a page and goes to several locations on another page, the line is usually distributed on the destination page and not the origin page. If a line leaves a page and goes to several other pages, it is shown as a branched line on the origin page.

10-17. EDGE INFORMATION. Data shown at the extreme left and extreme right of each page are called edge information. Edge information includes names of input and output signals, and numbers of the logic pages on which these signals also appear. The first line (and second line, if necessary) contains the signal name. The last line lists the number of the logic page on which the signal appears again. The logic page number is directly opposite the signal line.

10-18. EDGE CONNECTORS. When a signal or service wire enters or leaves a gate assembly, it may be routed through an edge connector. An edge connector is a modified SMS card whose contacts lead to an inter-chassis cable instead of to a printed circuit. An edge connector plugs into an SMS card receptacle exactly like a standard SMS card. An edge connector is so called because it is usually plugged into a receptacle near one edge of a gate assembly.

10-19. On ALD pages, a signal line connected to an edge connector is indicated by an asterisk or lozenger and a number or letter combination (for example, *2, *C, □ ⊥, □F, ⊥ □, etc) located on the entry or exit line. This notation refers to an entry in the table of edge connector locations and pin letters near the bottom of the ALD page.

10-20. Edge connector locations and pin letters are given in the standard SMS card location code. (See figure 10-5.) For example, *⊥ -- 0⊥A8A25A indicates that the signal line designated *⊥ (in the upper left corner of figure 10-5) is routed through the edge connector in frame 0⊥, gate assembly A8, column A, position 25, via pin A, of this edge connector.

h. Logic Block Location. Each ALD page is composed on a grid containing seven columns (designated 1 through 7, left to right) and nine rows A through H and J, top to bottom). A logic block may occupy any of the 45 locations in columns 2 through 6 (columns 1 and 7 are reserved for edge information); each location is designated by a two-character code designating the column and row.

10-22. COMMENTS. An area (5 on figure 10-5) at the bottom of each ALD page is reserved for comments. These comments usually indicate the designer(s) and the dates and numbers of the revisions that have been made to this ALD page.

10-23. CIRCUIT CARD LOCATION CHARTS.

10-24. The circuit card location charts (included with the ALD's) designate the SMS card (by type and IBM part number) used in each card location on the gate assemblies. These charts also indicate the total number of block configurations for that card and the ALD page(s) on which a logic block representing a circuit on that card is shown; each page entry indicates one logic block printed on that page.

10-25. EDGE CONNECTOR LISTS.

10-26. The edge connector lists (included with the ALD's) list the edge connectors for each SMS gate assembly, the signal present on each edge connector pin, and the ALD page (by LN number) on which the edge connector pin and signal are shown.

10-27. ASSEMBLY DRAWINGS.

10-28. The assembly drawings are provided to aid in the location of replaceable parts. Only the assembly drawings that are required for part replacement are included in this section.

NOTE

Many assembly drawings contain notes referring to IBM specifications; these notes are for manufacturing purposes only and should be disregarded for maintenance purposes.

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SIGNAL INTERFACE, PTC

LOGIC SHEET	TITLE	PAGE
04.00.01.0	CE PANEL to MEMORY	2
04.02.01.0	ML & DD PANEL to 03B2	3
04.03.01.0	ML & DD PANEL to 03B3	4
04.03.02.0	ML & DD PANEL to 03B3, TR PANEL to 03B3	5
04.04.01.0	03B4 to I/O and PROCESSOR PANEL	6
04.04.02.0	03B4 to CE PANEL	7
04.05.01.0	01 to 02 FRAME	8
04.05.02.0	01B1 to 02A4	9
04.06.01.0	02 FRAME to 01 FRAME and ADAPT I/O	10
04.07.01.0	01 to 02 FRAME and CE PANEL	11
04.07.02.0	02B3 to MEMORY	12
04.08.01.0	ADAPT I/O to 02B4	13
04.08.02.0	ADAPT I/O to 02B4	14
04.08.03.0	ADAPT I/O to 02B4	15
04.08.04.0	ADAPT I/O to 02B4	16
04.08.05.0	01 to 02 FRAME	17
04.09.01.0	TYPEWRITER to 01B1	18
04.09.02.0	CPU to 01B1	19
04.09.03.0	01B1 to SLFCK CONN	20
04.09.04.0	01B1 to SLFCK CONN	21
04.09.05.0	01B1 to SLFCK CONN	22
04.09.06.0	01B1 to SLFCK CONN	23
04.09.07.0	01B1 to SLFCK CONN	24
04.10.01.0	PLOTTER to 01B2	25
04.10.02.0	CPU to 01B2	26
04.11.01.0	01B3 to 1443 PRINTER	27
04.11.02.0	01 to 02 FRAME	28
04.13.01.0	CE PANEL to 03B8	29
04.13.03.0	PROC. PANEL to 03B8	30
04.13.04.0	PROC. PANEL to 03B8	31
04.13.05.0	03B8 to ADAPT I/O	32
04.13.06.0	01 to 02 FRAME	33
04.14.01.0	ML & DD, CE, TR PANELS to 03B7	34
04.15.01.0	ML & DD PANEL to 03B6, TR PANEL to 03B6	35
04.15.02.0	03B6 to CE PANEL	36
04.16.01.0	03B5 to ML & DD PANEL	37
04.16.02.0	03B5 to ML & DD PANEL	38
04.20.01.0	PROC. PANEL to 02B5	39
04.20.02.0	PROC. PANEL to 02B5	40
04.20.03.0	ADAPT I/O to 02B5	41
04.26.01.0	02A4 to MEMORY DIODE BD	42
04.26.02.0	02A4 to MEMORY DIODE BD	43
04.26.03.0	02A4 to MEMORY DIODE BD	44
04.26.04.0	02A4 to MEMORY DIODE BD	45
04.26.05.0	02A4 to 02B1	46
04.27.01.0	02A3 to 02A5	47
04.27.02.0	02A5 to 02A3	48
04.27.03.0	02A5 to CE PANEL	49
04.27.04.0	02A5 to 02B3	50
04.28.01.0	02A6 to 02A3	51
04.28.02.0	02A6 to MEMORY	52

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Figure 10-4. Signal Interface List (Sheet 1 of 52)

FROM			SIGNAL NAME		TO		REFERENCE
PLUG	MATE	LOGIC SHEET			PLUG	MATE	LOGIC SHEET
03P18-b	J2-b	00.04.05.1	MBR SW	1	02P10-j	02A3J2-j	05.27.05.1
	Z			2		k	05.27.05.1
	X			3		m	05.27.06.1
	V			4		n	05.27.06.1
	T			5		p	05.27.07.1
	R			6		q	05.27.07.1
	N			7		r	05.27.08.1
	L			8		s	05.27.08.1
	J			9		t	05.27.09.1
	G			10		u	05.27.09.1
	E			11		v	05.27.10.1
	C			12		w	05.27.10.1
	A			13		x	05.27.11.1
	d			PAR		y	05.27.11.1
	j		SPARE			EE	EE
	k					FF	FF
	m					GG	GG
	n					HH	HH

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Figure 10-4. Signal Interface List (Sheet 2)

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FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B2D01-A B C D E F G H	05.02.01.1 05.02.02.1 05.02.03.1 05.02.04.1 05.02.05.1 	CETRS IND CEHOPC1 IND CESS MBR IND CESER IND CEAI3 IND CESS MSC IND CEDOAC IND CEBR14 IND	02J6-t w y v u x z AA	00.04.10.0 	P3 t w y v u x z AA
03B2D01-K L M N P Q R	05.02.06.1 05.02.23.1 	TRCP ERR IND SS MDR SYLO IND SS MDR SYL1 IND SS MDR IS1 IND SS MDR IS2 IND SS MDR IS3 SS MDR IS4 IND	02J6-s A B C D E F	00.04.10.0 00.04.10.3 	P3 s A B C D E F
03B2E01-A B C D E F G H J K L M N P Q R	05.02.22.1 	DTDR SIGN IND B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15	02J6-PP R S T U V W X Y Z a b c d e f	00.04.10.1 	P3 PP R S T U V W X Y Z a b c d e f
03B2E02-A B C D E F G H J K L M N P Q R	05.02.22.1 	DTDR B16 IND B17 B18 B19 B20 B21 B22 B23 B24 B25 SSMDR DS1 IND DS2 DS3 DS4 IA IM0 IND IA IM1 IND	02J6-g h i j k m n p q r J K L M G H	00.04.10.1 00.04.10.2 00.04.10.3 00.04.10.3 	P3 g h i j k m n p q r J K L M G H
03B2F01-A B C D E F G H	05.02.23.1 05.02.14.1 05.02.06.1 05.02.05.1 	SSMDR DA DM0 IND SSMDR DA DM1 IND SW A13 IA SW A13 DATA SW TRS INV ERR 1 IND INV ERR 2 IND SW LAMP TEST 2	02J6-N P FF EE DD BB CC GG	00.04.10.2 00.04.10.2 00.04.10.0 	P3 N P FF EE DD BB CC GG

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LN 04.02.01.0

Figure 10-4. Signal Interface List (Sheet 3)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B3D01-A B C D E F G H J K L M	05.03.08.1 05.03.19.1 	IA A1 IND IA A2 IND IA A3 IND IA A4 IND IA A5 IND IA A6 IND IA A7 IND IA A8 IND SW OP1 SW OP2 SW OP3 SW OP4	02J7-R S T U V W X Y d c b a	00.04.10.3 00.04.10.2 	P4-R S T U V W X Y d c b a
03B3E01-A B C D E F G H J K L M N P Q R	04.03.08.1 05.03.16.1 05.03.18.1 05.03.08.1 	INS OA1 IND INS OA2 IND INS OA3 IND INS OA4 IND INS OA5 IND INS OA6 IND INS OA7 IND INS OA8 IND INS OA9 IND SW CD RST NOT SYL O BR IND SYL 1 BR IND INS OP1 IND INS OP2 IND INS OP3 IND INS OP4 IND	02J8-C D E F G H J K L y u v M N P R	00.04.10.2 00.04.10.0 00.04.10.2 	P5-C D E F G H J K L y w v M N P R
03B3E02-A B C D E F G H J K L M N P	05.03.19.1 05.03.20.1 05.03.19.1 	SW DS4 DS3 DS2 DS1 OA1 OA2 OA3 OA4 OA5 OA6 OA7 OA8 OA9 DA MM	02J7-p q r s h m k j i h g f e z	00.04.10.2 	P4-p q r s h m k j i h g f e z
03B3F01-A B C D E F G H J K L M N P	05.03.22.1 	SW SYL IS4 IS3 IS2 IS1 A8 A7 A6 A5 A4 A3 A2 A1 IA MM	02J7-P N M L K B C D E F G H J A	00.04.10.3 	P4-P N M L K B C D E F G H J A

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Figure 10-4. Signal Interface List (Sheet 4)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B3F02-A	05.03.20.1	SW B1	02J8-s	00.04.10.1	P5-s
B		R2	r		r
C		B3	q		q
D		B4	p		p
E		B5	n		n
F		B6	m		m
G		B7	k		k
H		B8	j		j
J		B9	i		i
K		B10	h		h
L		B11	g		g
M		B12	f		f
N		B13	e		e
P		B14	d		d
Q		B15	c		c
R	05.03.21.1	B16	b		b
03B3F03-A		B17	a		a
B		B18	Z		Z
C		B19	Y		Y
D		B20	X		X
E		B21	W		W
F		B22	V		V
G		B23	U		U
H		B24	T		T
J		B25	S		S
K	05.03.19.1	SIGN	t		t
L	05.03.15.1	SW CD RST	x	00.04.10.0	x
N	05.03.14.1	SW RPT PRG CYC	z		z
P		SW SING STEP MODE	AA		AA
Q		SW ADR HOLD MODE	BB		BB
R	05.03.18.1	SW SINGLE DIS	CC		CC
03B3F04-A	05.03.21.1	SW TAA DR1	03J10-FF	00.04.01.1	P2-FF
R		SW TAA DR2	b		b
C		SW TAA DR3	d		d
D		SW TAA DR4	f		f
E		SW TAA DR5	h		h
03B3E03-A	05.03.18.1	INS BR PB IND 1	02J8-A	00.04.10.2	P5-A
B	05.03.18.1	INS BR PB IND 2	02J8-B	00.04.10.2	B
C					
D					
E					
F					
G					
H					
J					
K					
L					
M	05.03.08.1	SW LAMP TEST 2	02J4-w	00.04.10.0	P5-w
N					
P					
Q					
R					

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Figure 10-4. Signal Interface List (Sheet 5)

FROM		SIGNAL NAME	VIA	TO	
EDGE CONN.	LOGIC SHEET			LOGIC SHEET	PLUG
03B4A01-A	05.04.10.1	DISCR OUT 1 SIG RET	Twisted Pair	00.04.52.0	9009J3-H
B	┌	DISCR OUT 2 SIG RET	┌	┌	J
C	05.04.09.1	DISCR OUT 3 SIG RET	┌	┌	K
D	┌	DISCR OUT 4 SIG RET	┌	┌	L
E	┌	DISCR OUT 5 SIG RET	┌	┌	M
F	┌	DISCR OUT 6 SIG RET	┌	┌	N
J	See Note				P
03B4D04-C	05.04.01.1	PBN SIG RET			R
D	05.04.02.1	W SIG RET	┌	┌	S
G	05.04.14.1	ACGACISS SIG RET	┌	00.04.53.0	T
E	05.04.04.1	CLDIS CLDISG	┌	┌	U
03W1A16	00.03.60.1				V
03TB2-3	00.03.40.0	EOSTV			Y
03TB2-6		EOSTVR			Z
03W1A-17	00.03.60.1	TESPG			a
03W1A-18		TESPG			b
02TB01-01	00.03.40.0	EOSW			
02TB01-02	┌	FOSWN			9009J4-b
02TB01-03	┌	EOHI			c
02TB02-06	┌	EO RET			Z
03TB04-14	┌	CHASSIS			a
					A
					B
					q
					r
					s
					t
					u
					v
					9009J4-PH
03B4C04-A	05.04.07.1	P40 IND	02J19- s	00.04.15.2	P4-s
B		P20	┌	┌	u
C		P10	┌	┌	w
D	05.04.08.1	P4	┌	┌	y
E		P2	┌	┌	AA
F		P1	┌	┌	CC
G	05.04.09.1	D6	┌	┌	CC
H		D5	┌	┌	r
J		D4	┌	┌	t
K		D3	┌	┌	v
L	05.04.10.1	D2	┌	┌	x
M		D1	┌	┌	z
N	05.04.12.1	CST SW	┌	┌	BB
P	05.04.11.1	HALT SW ON	┌	┌	i
Q		HALT SW OFF	┌	┌	p
R	05.04.12.1	ERROR HOLD SW	┌	00.04.15.1	q
					m
03B4D01-D	05.04.01.1	MACH RST SW	02J19- n	00.04.15.2	P4-n
03B4A02-B		MACH RST RLY	08T73-17	00.03.60.0	03P13-J
03B4A04-A	05.04.13.1	PR ADV ON	02J19- k	00.04.15.2	P4-k
B	┌	PR ADV OFF	┌	┌	EE
					EE

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Figure 10-4. Signal Interface List (Sheet 6)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B4B04-A	05.04.05.1	SW BG 1	03P19-p	00.04.05.2	J3-p
B		2	n		n
C		3	m		m
D		4	k		k
E		5	j		j
F		6	i		i
G		7	h		h
H		8	g		g
J		9	f		f
K		10	e		e
L		11	d		d
M		12	c		c
N		13	b		b
P		14	a		a
Q	05.04.06.1	SW ALL PHASE	q		q
R		SW ALL BG			
03B4B03-A	05.04.06.1	SW PA	03P19-t	00.04.05.2	J3-t
B		PB	s		s
C		PC	r		r
D		CCW	w		w
E		CCX	x		x
F		CCY	y		y
G		CCZ	z		z
H		SCOPE SYNC	BB		BB
J		SW ALL CLOCKS	v		v
K	05.04.13.1	CE ADV ON	DD		DD
L		CE ADV OFF	CC		CC
M		REM ADV ON	Z		Z
N		REM ADV OFF	Y		Y
P		SINGLE PHASE SW	V		V
Q		SINGLE BIT SW	W		W
R		NORMAL MODE	X		X
03B4B02-A	05.04.16.1	BG 1 IND	03P19-E	00.04.05.1	J3-E
B		2	G		G
C		3	J		J
D		4	L		L
E		5	N		N
F		6	R		R
G		7	T		T
H		8	D		D
J		9	F		F
K		10	H		H
L		11	K		K
M		12	M		M
N		13	P		P
P		14	S		S
Q		LAMP TEST CE 1	AA		AA
R					
03B4A03-A	05.04.16.1	PA IND	03P19-A	00.04.05.1	J3-A
B		PB IND	B		B
C		PC IND	C		C
D	05.04.13.1	SINGLE INST SW	U		U

			JACK	MATE	REFERENCE LOGIC SHEET
03B4A02-A	05.04.01.1	-Y MACH RST	02J12-q	01P15-q	05.11.07.1
03B4E03-A	05.04.12.1	-Y MACH RST	02J13-N	01P16-N	05.09.07.1
03B4E03-B	05.04.01.1	CIO 224	02J13-J	01P16	05.09.13.1

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Figure 10-4. Signal Interface List (Sheet 7)

FROM		SIGNAL NAME	TO		REFERENCE LOGIC SHEET
EDGE CONN.	LOGIC SHEET		JACK	MATE	
02B1A04-A B C D E	05.05.25.1 05.05.26.1 05.05.26.1	BG8 BG9 BG10 SPARE SPARE	02J12- n p m u v	01P15- n p m u v	05.11.06.1
02B1D03-A B C D E	05.05.24.1 05.05.24.1 05.05.24.1	BG1 BG2 BG3 SPARE SPARE	02J13- C D E b c	01P16- C D E b c	05.09.01.1 05.09.01.1 05.09.02.1
02B1D04-A B C D	05.05.25.1 05.05.26.1	BG6 BG12 SPARE SPARE	02J13- W Y h i	01P16- W Y h i	05.10.01.1 05.10.01.1

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Figure 10-4. Signal Interface List (Sheet 8)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	PLUG	MATE	LOGIC SHEET
02B1E03-A	05.05.15.1	RD DLY 2.25 A	02P13-C	02A3J4-C	05.27.03.1
B	05.03.15.1	RD DLY 1.75 A	K	K	┆
C	05.05.14.1	INHIBIT GATE A	E	E	┆
D	05.05.16.1	RD & WR DLY 0.75 A	A	A	05.27.01.1
E	05.05.16.1	RD & WR DLY 2.75 A	D	D	┆
F	05.05.15.1	PTC READ GATE A	H	H	┆
G	05.05.15.1	PTC WRITE GATE A	J	J	┆
H	05.05.16.1	RD & WR DLY 12.5 A	B	B	┆
J	05.05.05.1	SYL 1	02P10-f	02A3J2-f	05.27.01.1 05.27.02.1
K	05.05.20.1	MAR 5 READ	b	b	┆
L	05.05.20.1	MAR 5 NOT READ	c	c	┆
M	05.05.01.1	STROBE A INH	02P13-N	02A3J4-N	05.27.03.1
N		SPARE	02P10-d	02A3J2-d	
Q			02P13-R	02A3J4-R	
R			02P13-S	02A3J4-S	
02B1E04-A	05.05.19.1	RD DLY 2.25 B	02P14-C	02A3J5-C	05.27.04.1
B	05.05.19.1	RD DLY 1.75 B	K	K	┆
C	05.05.17.1	INHIBIT GATE B	E	E	┆
D	05.05.18.1	RD & WR DLY 0.75 B	A	A	05.27.02.1
E	05.05.18.1	RD & WR DLY 2.75 B	D	D	┆
F	05.05.19.1	PTC READ GATE B	H	H	┆
G	05.05.19.1	PTC WRITE GATE B	J	J	┆
H	05.05.18.1	RD & WR DLY 1.25 B	B	B	┆
J		SPARE	P	P	┆
K	05.05.01.1	STROBE B INH	N	N	05.27.04.1
L		SPARE	R	R	
M		SPARE	S	S	
02B1F02-A	05.05.09.1	MAR 1	02P10-A	02A3J2-A	05.26.02.1 05.26.06.1
B	05.05.09.1	1 NOT	N	N	┆
C	05.05.10.1	3 NOT	R	R	┆
D		2 NOT	P	P	┆
E		2	B	B	┆
F		3	C	C	┆
G		4 NOT	S	S	05.26.03.1 05.26.07.1
H		5 NOT	T	T	┆
J	05.05.11.1	6 NOT	U	U	┆
K	05.05.10.1	4	D	D	┆
L	05.05.10.1	5	E	E	┆
M	05.05.11.1	6	F	F	┆
N		7 NOT	V	V	05.26.04.1 05.26.08.1
P		8 NOT	W	W	┆
Q	05.05.08.1	9 NOT	X	X	┆
R	05.05.11.1	7	G	G	┆
02B1F03-A	05.05.11.1	MAR 8	02P10-H	02A3J2-H	05.26.04.1 05.26.08.1
B	05.05.08.1	9	J	J	┆
C	05.05.08.1	10 NOT	Y	Y	05.26.05.1 05.26.09.1
D	05.05.06.1	11 NOT	Z	Z	┆
E	05.05.07.1	10	K	K	┆
F	05.05.06.1	12 NOT	a	a	┆
G	05.05.07.1	11	L	L	┆
H	05.05.07.1	12	M	M	┆

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Figure 10-4. Signal Interface List (Sheet 9)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
02B2A01-A 02B2A01-B	05.06.32.1	PTC - AI3 SIG RET	Twisted Pair	00.04.52.0	9009J3- e J3- f
02B2D02-A	05.06.08.1	PCB	JACK 02J13- X	MATE 01P16- X	REFERENCE LOGIC SHEET 05.10.01.1
02B2E01-A B C E	05.06.08.1 05.06.08.1 05.06.05.1	PA-A PB-A CPZ-B SPARE	02J13- A B F a	01P16- A B F a	05.09.01.1 05.09.01.1 05.09.02.1

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Figure 10-4. Signal Interface List (Sheet 10)

V-10-20

FROM		TO			
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
02B3D04-A B C D E F G H J K L M N P Q	05.07.27.1 	BIT 1 IND 2 3 4 5 6 7 8 9 10 11 12 13 14 LAMP TEST CE 2	03P18-c a Y W U S P M K H F D B e r	00.04.05.1 	J2-c a Y W U S P M K H F D B e r
02B3C01-A 	05.07.24.1 	MEM LOAD SW	03P18-f 	00.04.05.1 	J2-f
02B3F05-A B C	05.07.03.1 05.07.04.1 05.07.16.1	CIO DATA SIG RET PIO DATA SIG RET PTRS SIG RET	Twisted Pair 	00.04.52.0 00.04.52.0 00.04.55.0 00.04.55.0 00.04.54.0 00.04.54.0	9009J3-c 9009J3-d 9009J6-P 9009J6-R 9009J5-F 9009J5-G
		TO		REFERENCE LOGIC	
02B3A02-A 		CIO	JACK 02J13-M 	MATE 01P16-M 	05.09.01.1
02B3F01-A B C D		PRS SPARE 	02J12-h w x y 	01P15-h w x y 	05.11.01.1

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Figure 10-4. Signal Interface List (Sheet 11)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	PLUG	MATE	LOGIC SHEET
02B3E04-A	05.07.24.1	NT MBR 1	02P12- P	02A3J3- P	05.27.05.1
B	05.07.26.1	MBR 1	A	A	
C	05.07.26.1	MBR 2	B	B	
D	05.07.24.1	NT MBR 2	R	R	
E	05.07.24.1	NT MBR 3	S	S	05.27.06.1
F	05.07.26.1	MBR 3	C	C	
G	05.07.26.1	MBR 4	D	D	
H	05.07.24.1	NT MBR 4	T	T	
J	05.07.24.1	NT MBR 5	U	U	05.27.07.1
K	05.07.26.1	MBR 5	E	E	
L	05.07.26.1	MBR 6	F	F	
M	05.07.24.1	NT MBR 6	V	V	
N	05.07.25.1	NT MBR 7	W	W	05.27.08.1
P	05.07.26.1	MBR 7	G	G	
Q	05.07.26.1	MBR 8	H	H	
R	05.07.25.1	NT MBR 8	X	X	
02B3F04-A	05.07.25.1	NT MBR 9	02P12- Y	02A3J3- Y	05.27.09.1
E	05.07.26.1	MBR 9	J	J	
C	05.07.26.1	MBR 10	K	K	
D	05.07.25.1	NT MBR 10	Z	Z	
E	05.07.25.1	NT MBR 11	a	a	05.27.10.1
F	05.07.26.1	MBR 11	!	L	
F	05.07.26.1	MBR 12	M	M	
H	05.07.25.1	NT MBR 12	b	b	
J	05.07.25.1	NT MBR 13	c	c	05.27.11.1
K	05.07.26.1	MBR 13	N	N	
L	05.07.26.1	MBR 14	d	d	
M	05.07.25.1	NT MBR 14	e	e	
N	05.07.08.1	CBR 1	02P10- h	02A3J2- h	05.27.05.1 05.27.06.1
P	05.07.08.1	CBR 2	i	i	05.27.07.1 05.27.08.1
Q	05.07.24.1	SET MBR 1	z	z	05.27.09.1 05.27.10.1
R	05.07.24.1	SET MBR 2	AA	AA	05.27.11.1

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Figure 10-4. Signal Interface List (Sheet 12)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
02B4A04-A	05.08.14.1	CIO 001	Twisted Pair	00.04.50.0	9009J1-K
B	05.08.10.1	SIG RET			L
C	05.08.14.1	CIO 002			M
D	05.08.10.1	SIG RET			N
E	05.08.14.1	CIO 005			P
F	05.08.10.1	SIG RET			R
G	05.08.14.1	CIO 006			S
H	05.08.10.1	SIG RET			T
J	See Note I.	CIO 011			U
K	05.08.14.1	SIG RET			V
L	05.08.10.1	CIO 012			W
M	05.08.14.1	SIG RET			X
N	05.08.10.1	CIO 015			Y
P	05.08.14.1	SIG RET			Z
Q	05.08.10.1	CIO 016			a
R	05.08.14.1	SIG RET			b
02B4B04-A	05.08.10.1	CIO 021	Twisted Pair	00.04.50.0	c
B	05.08.14.1	SIG RET			d
C	05.08.10.1	CIO 022			e
D	05.08.15.1	SIG RET			f
E	05.08.11.1	CIO 025			g
F	05.08.15.1	SIG RET			h
G	05.08.11.1	CIO 026			i
H	05.08.15.1	SIG RET			j
J	See Note I.	CIO 031			k
K	05.08.11.1	SIG RET			m
L	05.08.15.1	CIO 032			n
		SIG RET			p
		CIO 035			q
		SIG RET			r
		CIO 036			s
		SIG RET			t
		CIO 041	u		
		SIG RET	v		
		CIO 042	w		
		SIG RET	x		
		CIO 045	y		
		SIG RET	z		
		CIO 046	AA		
		SIG RET	BB		
		CIO 051	CC		
		SIG RET	DD		
		CIO 052	EE		
		SIG RET	FF		
		CIO 055	GG		
		SIG RET	HH		
		CIO 056	JJ		
		SIG RET	KK		
		CIO 061	LL		
		SIG RET	MM		
		BLANK	NN		
		CHASSIS	PP		
03TB04-13	00.03.60.0				

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Figure 10-4. Signal Interface List (Sheet 13)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
02B4C04-A	05.08.11.1	CIO 062	Twisted Pair	00.04.51.0	9009J2- F
B	05.08.15.1	SIG RET CIO 065			G
C	05.08.11.1	SIG RET CIO 066			H
D	05.08.15.1	SIG RET CIO 071			J
E	05.08.11.1	SIG RET CIO 072			K
F	05.08.15.1	SIG RET CIO 075			L
G	05.08.11.1	SIG RET CIO 076			M
H	05.08.15.1	SIG RET CIO 101			N
J	See Note I	SIG RET			P
K	05.08.11.1	CIO 102			R
L	05.08.15.1	SIG RET CIO 105			
M	05.08.11.1	SIG RET CIO 106			Y
N	05.08.16.1	SIG RET CIO 111			Z
P	05.08.12.1	SIG RET CIO 112			a
Q	05.08.16.1	SIG RET CIO 115			b
R	05.08.12.1	SIG RET CIO 116			c
02B4D04-A	05.08.16.1	SIG RET CIO 121			d
B	05.08.12.1	SIG RET CIO 122	e		
C	05.08.16.1	SIG RET CIO 125	f		
D	05.08.12.1	SIG RET CIO 126	g		
E	05.08.16.1	SIG RET CIO 131	h		
F	05.08.12.1	SIG RET CIO 132	i		
G	05.08.16.1	SIG RET CIO 135	j		
H	05.08.12.1	SIG RET CIO 136	k		
J	See Note I	SIG RET	l		
K	05.08.16.1	CIO 141	m		
L	05.08.12.1	SIG RET CIO 142	n		
M	05.08.16.1	SIG RET CIO 145	p		
N	05.08.16.1	SIG RET CIO 146	q		
03TB04- 13	00.03.60.0	BLANK	r		
03W1A- 14	00.03.60.3	CHASSIS	s		
03W1A- 15	00.03.60.3	TESPG	t		
			u		
			v		
			w		
			x		
			y		
			z		
			AA		
			BB		
			CC		
			DD		
			EE		
			FF		
			GG		
			HH		
			JJ		
			KK		
			LL		
			MM		
			NN		
			PP		
			D		
			E		

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Figure 10-4. Signal Interface List (Sheet 14)

FROM				TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG	
02B4E04-A	05.08.12.1	CIO 146	Twisted Pair	00.04.55.0	9009J6-S	
B	┌	SIG RET				T
C	05.08.13.1	CIO 152				U
D	┌	SIG RET				V
E	┌	CIO 156				W
F	┌	SIG RET				X
G	┌	CIO 162				Y
H	┌	SIG RET				Z
J	See Note	CIO 166				a
K	05.08.13.1	SIG RET				b
L	┌	CIO 172	c			
M	┌	SIG RET	d			
N	05.08.17.1	CIO 176	e			
P	┌	SIG RET	f			
Q	┌	CIO 202	g			
R	┌	SIG RET	h			
02B4F04-A	05.08.17.1	CIO 206	Twisted Pair	00.04.55.0	9009J6-y	
B	┌	SIG RET				z
C	┌	A5 PTC				AA
D	┌	SIG RET				BB
E	┌	A6 PTC				CC
F	┌	SIG RET				DD
G	┌	A7 PTC				EE
J	See Note	SIG RET				FF
		A8 PTC				GG
		SIG RET				HH
		A9 PTC	JJ			
		CIO PTC	KK			
		SIG RET	LL			
		P10 PTC	MM			
		SIG RET				
02B4A03-A	05.08.17.1	ACNCST	Twisted Pair	00.04.53.0	9009J4-g	
B	┌	SIG RET				h
C	┌	PTC CST				LL
J	See Note	SIG RET	MM			
		ACNCCST	e			
		SIG RET	f			
03TB04-15	00.03.60.0	BLANK CHASSIS			NN PP	

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Figure 10-4. Signal Interface List (Sheet 15)

FROM			TO				
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG		
02B4F03-A	05.08.18.1	ACC BIT SIGN SIG RET	Twisted Pair	00.04.54.0	9009J5- H		
B		ACC BIT 1 SIG RET			J		
C		ACC BIT 2 SIG RET			K		
D		ACC BIT 3 SIG RET			L		
E	05.08.19.1	ACC BIT 4 SIG RET			M		
F		ACC BIT 5 SIG RET			N		
G		ACC BIT 6 SIG RET			P		
H		ACC BIT 7 SIG RET			R		
J	See Note						
K	05.08.20.1	ACC BIT 8 SIG RET				a	
L		ACC BIT 9 SIG RET				b	
M		ACC BIT 10 SIG RET				c	
N		ACC BIT 11 SIG RET				d	
P						e	
Q						f	
R						g	
02B4D03-A	05.08.21.1	ACC BIT 12 SIG RET			Twisted Pair	00.04.54.0	9009J5- i
B		ACC BIT 13 SIG RET					j
C		ACC BIT 14 SIG RET					k
D		ACC BIT 15 SIG RET					m
E	05.08.22.1	ACC BIT 16 SIG RET	n				
F		ACC BIT 17 SIG RET	p				
G		ACC BIT 18 SIG RET	q				
H		ACC BIT 19 SIG RET	r				
J	See Note		s				
K	05.08.23.1	ACC BIT 20 SIG RET	t				
L		ACC BIT 21 SIG RET	u				
M		ACC BIT 22 SIG RET	v				
N		ACC BIT 23 SIG RET	w				
P	05.08.24.1	ACC BIT 24 SIG RET	x				
Q		ACC BIT 25 SIG RET	y				
03TB04-14	00.03.60.0	CHASSIS					z
							AA
							BB
							CC
							DD
					EE		
					FF		
					GG		
					HH		
					JJ		
					KK		
					LL		
					MM		
					PP		

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Figure 10-4. Signal Interface List (Sheet 16)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	JACK	MATE	LOGIC SHEET
02B4A02-A B C D E	05.08.06.1 	CODE 140 144 150 SPARE SPARE	02J13- T U V f g	01P16- T U V f g	05.10.01.1
02B4C01-A B C D E F	05.08.06.1 	CODE 120 124 130 134 SPARE SPARE	02J13- G H K L d e	01P16- G H K L d e	05.09.01.1
02B4E02-A B C D E F G H	05.08.07.1 05.08.02.2 05.08.02.2 	CODE 164 170 160 -Y CODE 774 SPARE +Y CODE 774 SPARE SPARE	02J12- e f g i j k z AA	01P15- e f g i j k z AA	05.11.01.1 05.11.01.1

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Figure 10-4. Signal Interface List (Sheet 17)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
01B1D01-A	05.09.10.1	A	01P13-a		01A2J1-a
B		B	b		b
C		C	c		c
D		D	e		e
E		E	f		f
F		F	Y		Y
G	05.09.06.1	UC SHIFT MAG	S		S
H	05.09.06.1	LC SHIFT MAG	T		T
J	05.09.10.1	TYPE RET	d		d
K	05.09.10.1	Z	Z		Z
L	05.09.09.1	SPACE MAG	M		M
M	05.09.11.1	CHECK MAG	B		B
N		SPARE	m		m
P		SPARE	n		n
Q		SPARE	r		r
R		SPARE	j		i
01B1A01-A		SPARE	01P13-K		01A2J1-K
B		SPARE	N		N
C	05.09.08.1	R1	E		E
D		R2	F		F
E		R2-A	D		D
F		R5	H		H
G	05.09.09.1	T1	C		C
H		T2	A		A
J		TAB MAG	L		L
K		INDEX MAG	R		R
L		RED MAG	U		U
M		BLK MAG	V		V
N		CARR RET MAG	P		P
P		SPARE	W		W
Q		SPARE	h		h
R		SPARE	k		k

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Figure 10-4. Signal Interface List (Sheet 18)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	PLUG	MATES	LOGIC SHEET
01B1A02-A	05.09.01.1	PA A	01P16- A	02J13- A	05.06.08.1
B	┆	PB A	B	B	05.06.08.1
C	┆	BG 1	C	C	05.05.24.1
D	┆	BG 2	D	D	┆
E	05.09.02.1	BG 3	E	E	┆
F	05.09.02.1	CPZ B	F	F	05.06.05.1
G	05.09.01.1	CODE 120	G	G	05.08.06.1
H	┆	124	H	H	┆
K	┆	130	K	K	┆
L	┆	134	L	L	┆
M	┆	CIO	M	M	05.07.21.1
N	05.09.07.1	MACH RST	N	N	05.04.01.1
P	05.09.07.1	TYPR READY	P	P	00.04.15.3
Q	05.09.04.1	PLOTTER READY	R	R	00.04.15.3
R	05.09.06.1	10 CPS MV	S	S	05.15.07.1

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Figure 10-4. Signal Interface List (Sheet 19)

FROM				TO			
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG		
01B1D02-A	05.09.14.1	SLFCK 1A * ACC SIGN SIG RET	Twisted Pair	00.04.54.0	01J6-H		
B	05.09.14.1	SLFCK 2A * ACC 1 SIG RET			J		
C	05.09.14.1	SLFCK 3A * ACC 2 SIG RET			K		
D	05.09.15.1	SLFCK 4A * ACC 3 SIG RET			L		
E	05.09.15.1	SLFCK 5A * ACC 4 SIG RET			M		
F	05.09.15.1	SLFCK 6A * ACC 5 SIG RET			N		
G	05.09.16.1	SLFCK 7A * ACC 6 SIG RET			P		
H	05.09.16.1	SLGCK 8A * ACC 7 SIG RET			R		
J	See Note				S		
K	05.09.16.1	SLFCK 9A * ACC 8 SIG RET			T		
L	05.09.17.1	SLFCK 10A * ACC 9 SIG RET			U		
M	05.09.17.1	SLFCK 11A * ACC 10 SIG RET			V		
N	05.09.17.1	SLFCK 12A * ACC 11 SIG RET			W		
P	05.09.18.1	SLFCK 13A * ACC 12 SIG RET			X		
Q	05.09.18.1	SLFCK 14A * ACC 13 SIG RET			Y		
R	05.09.18.1	SLFCK 15A * ACC 14 SIG RET			Z		
01B01D03-A	05.09.14.1	SLFCK 1A * ACC 15 SIG RET					a
B	05.09.14.1	SLFCK 2A * ACC 16 SIG RET					b
C	05.09.14.1	SLFCK 3A * ACC 17 SIG RET					c
D	05.09.15.1	SLFCK 4A * ACC 18 SIG RET					d
E	05.09.15.1	SLFCK 5A * ACC 19 SIG RET					e
F	05.09.15.1	SLFCK 6A * ACC 20 SIG RET					f
G	05.09.16.1	SLFCK 7A * ACC 21 SIG RET					g
H	05.09.16.1	SLFCK 8A * ACC 22 SIG RET					h
J	See Note						i
K	05.09.16.1	SLFCK 9A * ACC 23 SIG RET					j
L	05.09.16.1	SLFCK 10A * ACC 24 SIG RET			k		
M	05.09.16.1	SLFCK 11A * ACC 25 SIG RET			m		
N	05.09.14.1	A1 PTC SLFCK SIG RET		00.04.55.0	n		
P	05.09.14.1	A2 PTC SLFCK SIG RET			p		
Q	05.09.14.1	A3 PTC SLFCK SIG RET			q		
R	05.09.15.1	A4 PTC SLFCK SIG RET			r		
					s		
					t		
					u		
					v		
					w		
					x		
					z		
					AA		
					BB		
					CC		
					DD		
					EE		
					FF		
					GG		
					HH		
					JJ		
					KK		
					LL		
					MM		
					01J7-q		
					r		
					s		
					t		
					u		
					v		
					w		
					x		

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Figure 10-4. Signal Interface List (Sheet 20)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
01B03-A	05.09.16.1	SLFCK 8 * CODE 025 SIG RET	Twisted Pair	00.04.50.0	01J08- g h
D	05.09.16.1	SLFCK 8 * CODE 131 SIG RET		00.04.51.0	01J09- w x
C	05.09.16.1	SLFCK 9 * CODE 042 SIG RET		00.04.50.0	01J08- w x
D	05.09.16.1	SLFCK 9 * CODE 146 SIG RET		00.04.55.0	01J07- S T
E	05.09.16.1	SLFCK 9 * CODE 031 SIG RET		00.04.50.0	01J08- k m
F	05.09.16.1	SLFCK 9 * CODE 135 SIG RET		00.04.51.0	01J09- AA BB
G	05.09.17.1	SLFCK 10 * CODE 071 SIG RET		00.04.51.0	01J09- M N
H	05.09.17.1	SLFCK 10 * CODE 048 SIG RET		00.04.50.0	01J08- AA BB
J	See Note				
K	05.09.17.1	SLFCK 10 * CODE 152 SIG RET		00.04.55.0	01J07- U V
L	05.09.17.1	SLFCK 10 * CODE 035 SIG RET		00.04.50.0	01J08- q r
M	05.09.17.1	SLFCK 10 * CODE 141 SIG RET		00.04.51.0	01J09- EE FF
N	05.09.17.1	SLFCK 11 * CODE 052 SIG RET		00.04.50.0	01J08- EE FF
P	05.09.17.1	SLFCK 11 * CODE 156 SIG RET		00.04.55.0	01J07- W S
Q	05.09.17.1	SLFCK 11 * CODE 041 SIG RET		00.04.50.0	01J08- u v
R	05.09.17.1	SLFCK 11 * CODE 145 SIG RET		00.04.51.0	01J09- JJ KK
01B04- A	05.09.17.1	SLFCK 12 * CODE 056 SIG RET		00.04.50.0	01J08- JJ KK
B	05.09.17.1	SLFCK 12 * CODE 162 SIG RET		00.04.55.0	01J07- Y Z
C	05.09.17.1	SLFCK 12 * CODE 045 SIG RET		00.04.50.0	01J08- y z
D	05.09.17.1	SLFCK 12 * CODE 151 SIG RET		00.04.51.0	01J09- LL MM
E	05.09.18.1	SLFCK 13 * CODE 062 SIG RET		00.04.51.0	01J09- F G
F	05.09.18.1	SLFCK 13 * CODE 166 SIG RET		00.04.55.0	01J07- a b
G	05.09.18.1	SLFCK 13 * CODE 051 SIG RET		00.04.50.0	01J08- CC DD
H	05.09.18.1	SLFCK 13 * CODE 102 SIG RET		00.04.51.0	01J09- Y Z
J	See Note				
K	05.09.18.1	SLFCK 14 * CODE 066 SIG RET		00.04.51.0	01J09- K L
L	05.09.18.1	SLFCK 14 * CODE 208 SIG RET	00.04.55.0	01J07- i j	
M	05.09.18.1	SLFCK 14 * CODE 172 SIG RET	00.04.55.0	01J07- c d	
N	05.09.18.1	SLFCK 14 * CODE 055 SIG RET	00.04.50.0	01J08- GG HH	
P	05.09.18.1	SLFCK 15 * CODE 072 SIG RET	00.04.51.0	01J09- P R	
Q	05.09.18.1	SLFCK 15 * CODE 176 SIG RET	00.04.55.0	01J07- e f	
R	05.09.18.1	SLFCK 15 * CODE 061 SIG RET	00.04.50.0	01J08- LL MM	

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Figure 10-4. Signal Interface List (Sheet 21)

FROM		SIGNAL NAME	Twisted Pair	TO			
EDGE CONN.	LOGIC SHEET			LOGIC SHEET	PLUG		
01B1B01-A	05.09.14.1	SLFCK 1 * CODE 002 SIG RET	Twisted Pair	00.04.50.0	01J08- M ┆ N		
B	┆	SLFCK 1 * CODE 106 SIG RET		00.04.51.0	01J09- c ┆ d		
C		SLFCK 1 * CODE 212 SIG RET		00.04.55.0	01J07- k ┆ m		
D		SLFCK 1 * CODE 075 SIG RET		00.04.51.0	01J09- S ┆ T		
E		SLFCK 2 * CODE 006 SIG RET		00.04.50.0	01J08- S ┆ T		
F		SLFCK 2 * CODE 112 SIG RET		00.04.51.0	01J09- g ┆ h		
G		SLFCK 2 * CODE 216 SIG RET		00.04.55.0	01J07- n ┆ p		
H		SLFCK 2 * CODE 101 SIG RET		00.04.51.0	01J09- W ┆ X		
J		See Note					
K		05.09.14.1		SLFCK 3 * CODE 012 SIG RET	00.04.50.0	01J08- W ┆ X	
L		┆		SLFCK 3 * CODE 116 SIG RET	00.04.51.0	01J09- k ┆ l	
M	SLFCK 3 * CODE 001 SIG RET			00.04.50.0	01J08- K ┆ L		
N	┆	SLFCK 3 * CODE 105 SIG RET		00.04.51.0	01J09- a ┆ b		
P		05.09.15.1		SLFCK 4 * CODE 016 SIG RET	00.04.50.0	01J08- a ┆ b	
Q	┆	SLFCK 4 * CODE 122 SIG RET		00.04.51.0	01J09- q ┆ r		
R		SLFCK 4 * CODE 005 SIG RET		00.04.50.0	01J08- P ┆ R		
01B1B02-A	05.09.15.1	SLFCK 4 * CODE 111 SIG RET		Twisted Pair	00.04.51.0	01J09- e ┆ f	
B	┆	SLFCK 5 * CODE 022 SIG RET			00.04.50.0	01J08- e ┆ f	
C		SLFCK 5 * CODE 126 SIG RET			00.04.51.0	01J09- u ┆ v	
D		SLFCK 5 * CODE 011 SIG RET			00.04.50.0	01J08- U ┆ V	
E		SLFCK 5 * CODE 115 SIG RET			00.04.51.0	01J09- i ┆ j	
F		SLFCK 6 * CODE 026 SIG RET			00.04.50.0	01J08- i ┆ j	
G		SLFCK 6 * CODE 132 SIG RET			00.04.51.0	01J09- y ┆ z	
H		SLFCK 6 * CODE 015 SIG RET			00.04.50.0	01J08- Y	
J		See Note					
K		05.09.15.1			SLFCK 6 * CODE 121 SIG RET	00.04.51.0	01J09- n ┆ p
L		05.09.16.1	SLFCK 7 * CODE 032 SIG RET		00.04.50.0	01J08- n ┆ p	
M	┆	SLFCK 7 * CODE 136 SIG RET	00.04.51.0		01J09- MM ┆ NN		
N		SLFCK 7 * CODE 021 SIG RET	00.04.50.0		01J08- c ┆ d		
P	┆	SLFCK 7 * CODE 125 SIG RET	00.04.51.0		01J09- s ┆ t		
Q		SLFCK 8 * CODE 036 SIG RET	00.04.50.0		01J08- s ┆ t		
R	┆	SLFCK 8 * CODE 142 SIG RET	00.04.51.0		01J09- GG ┆ HH		

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Figure 10-4. Signal Interface List (Sheet 22)

FROM				TO			
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG		
01B1A04-A	05.09.16.1	SLFCK 8 * INTERRUPT 8 SIG RET	Twisted Pair	00.04.52.0	01J10- w x y z AA BB CC DD EE FF GG HH LL MM		
B	┌	SLFCK 9 * INTERRUPT 9 SIG RET					
C	05.09.17.1	SLFCK 10 * INTERRUPT 10 SIG RET					
D	┌	SLFCK 11 * INTERRUPT 11 SIG RET					
E	┌	SLFCK 12 * INTERRUPT 12 SIG RET					
F	05.09.18.1	SLFCK 13 * INTERRUPT 13 SIG RET					
G	┌	SLFCK 14 * INTERRUPT 14 SIG RET					
H	┌	SLFCK 15 * INTERRUPT 15 SIG RET					
J	See Note						
K	05.09.13.1	PTC PIO SLFCK SIG RET			00.04.55.0	01J07- LL MM	
L	05.09.12.1	SLFCK □A			04.09.01.0	01J13- a	
01B1C01-A	05.09.17.1	SLFCK 11 * CODE 076 SIG RET		Twisted Pair	00.04.51.0	01J09- U V W X Y Z AA BB CC DD EE FF GG HH	
B	┌	SLFCK 12 * CODE 202 SIG RET				00.04.55.0	01J07- k h
C	05.09.16.1	SLFCK 9 * CODE 065 SIG RET				00.04.51.0	01J09- H J
D	05.09.12.1	SLFCK DISC OUT 1 SIG RET				00.04.52.0	01J10- H J K L M N P R S T
E	┌	SLFCK DISC OUT 2 SIG RET					
F	┌	SLFCK DISC OUT 3 SIG RET					
G	┌	SLFCK DISC OUT 4 SIG RET					
H	┌	SLFCK DISC OUT 5 SIG RET					
J	See Note						
K	05.09.12.1	SLFCK DISC OUT 6 SIG RET			00.04.52.0	01J11- U V W X Y Z AA BB CC DD EE FF GG HH	
L	┌	SLFCK DISC IN 1 SIG RET					
M	┌	SLFCK DISC IN 2 SIG RET					
N	┌	SLFCK DISC IN 3 SIG RET					
P	┌	SLFCK DISC IN 4 SIG RET					
Q	┌	SLFCK DISC IN 5 SIG RET					
R	┌	SLFCK DISC IN 6 SIG RET					
01B1D04-A	05.09.15.1	A5 PTC SLFCK SIG RET		00.04.55.0	01J07- y z AA BB CC DD EE FF GG HH		
B	┌	A6 PTC SLFCK SIG RET					
C	05.09.16.1	A7 PTC SLFCK SIG RET					
D	┌	A8 PTC SLFCK SIG RET					
E	┌	A9 PTC SLFCK SIG RET					
J	See Note						

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Figure 10-4. Signal Interface List (Sheet 23)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	LOGIC SHEET	PLUG	
01B1C02-A	05.09.14.1	DATA B SLFCK	04.11.01.0	01J12-	n
B	┆	DATA A SLFCK	┆	┆	p
C	┆	DATA 8 SLFCK	┆	┆	q
D	05.09.15.1	DATA 4 SLFCK	┆	┆	r
E	┆	DATA 2 SLFCK	┆	┆	s
F	┆	DATA 1 SLFCK	┆	┆	t
G	05.09.16.1	DATA C SLFCK	┆	┆	u
H	05.09.14.1	UC SHIFT MAGSLFCK	04.09.01.0	01J13-	S
J	See Note		┆	┆	
K	05.09.14.1	LC SHIFT MAGSLFCK	┆	┆	T
L	┆	R1 SLFCK	┆	┆	E
M	05.09.15.1	R2 SLFCK	┆	┆	F
N	┆	R2A SLFCK	┆	┆	D
P	┆	R5 SLFCK	┆	┆	H
Q	05.09.16.1	T1 SLFCK	┆	┆	C
R	┆	CARR CTRL SLFCK	┆	01J12-	v
01B1C02-A	05.09.16.1	T2 SLFCK	┆	01J13-	A
B	┆	PR CHECK RST SLFCK	04.11.01.0	01J12-	B
C	┆	CK MAG SLFCK	04.09.01.0	01J13-	B
D	05.09.17.1	BLOCK DATA SLFCK	04.11.01.0	01J12-	D
E	┆	TAB MAG SLFCK	04.09.01.0	01J13-	L
F	┆	PRINT INSTR SLFCK	04.11.01.1	01J12-	K
G	┆	INDEX MAG SLFCK	04.09.01.0	01J13-	R
H	┆	PROCESS -D. CYCLE SC	04.11.01.0	01J12-	F
J	See Note		┆	┆	
K	05.09.17.1	RED MAG SLFCK	04.09.01.0	01J13-	U
L	05.09.18.1	BLK MAG SLFCK	┆	01J13-	V
M	┆	CARR RET MAG SLCK	┆	01J13-	P
N	┆	SPACE MAG SLFCK	┆	01J13-	M
P	05.09.12.1	SLFCK PROC RELEASE	04.11.01.0	01J12-	D
Q	┆	SLFCK Y	04.09.01.0	01J13-	Y
R	┆	SLFCK <input type="checkbox"/> C	┆	01J13-	c
01B1C04-A	05.09.12.1	SLFCK PARITY CHECK	04.11.01.0	01J12-	A
B	┆	<input type="checkbox"/> D	04.09.01.0	01J12-	b
C	┆	CARR BUSY	┆	01J12-	BB
D	┆	<input type="checkbox"/> E	┆	01J13-	e
E	┆	<input type="checkbox"/> F	┆	┆	f
F	┆	PRINT READY	04.11.01.0	01J12-	E
G	┆	RUN LATCH	04.11.01.0	┆	y
H	┆	CHAN 12	┆	┆	DD
J	see Note		┆	┆	
K	05.09.14.1	SLFCK 1 * INTERRUPT 1	Twisted 00.04.52.0	01J10-	g
L	┆	SIG RET	┆	┆	h
M	┆	SLFCK 2 * INTERRUPT 2	┆	┆	i
N	05.09.15.1	SIG RET	┆	┆	j
P	┆	SLFCK 3 * INTERRUPT 3	┆	┆	k
Q	┆	SIG RET	┆	┆	m
R	05.09.16.1	SLFCK 4 * INTERRUPT 4	┆	┆	n
	┆	SIG RET	┆	┆	p
	┆	SLFCK 5 * INTERRUPT 5	┆	┆	q
	┆	SIG RET	┆	┆	r
	┆	SLFCK 6 * INTERRUPT 6	┆	┆	s
	┆	SIG RET	┆	┆	t
	┆	SLFCK 7 * INTERRUPT 7	┆	┆	u
	┆	SIG RET	┆	┆	v
01TB02- 12	00.03.30.0	EOSW	00.04.53.0	01J11-	s
01J11- u	00.04.53.0	EOSWN	00.04.53.0	┆	l
01TB02- 13	00.03.30.0	EOSET	00.04.53.0	┆	v

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Figure 10-4. Signal Interface List (Sheet 24)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
0112C01-A	05.10.05.1	PEN UP	01P17-9		01A1P5-9
B		PEN DOWN	10	REFER TO	10
C		DRUM UP PLOT	1	INSTRUCTION	1
D		DRUM DOWN PLOT	2	MANUAL FOR	2
E		CARR RIGHT PLOT	4	CALCOMP	4
F		CARR LEFT PLOT	3	DIGITAL	3
G		SPARE	11	INCREMENTAL	11
H		SPARE	12	PLOTTER	12
J	05.10.05.1	EXT GND	15	MODEL	15
K		SPARE	7	565	7
L			8		8
M			6		6
N			5		5
P		CHASSIS	14		14
Q		SPARE	13		13
R		SPARE	16		16

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Figure 10-4. Signal Interface List (Sheet 25)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	PLUG	MATE	LOGIC SHEET
01B2B01-A	05.10.01.1	CODE 140	01P16-T	02J13-T	05.08.08.1
B		CODE 144	U	U	
C		CODE 150	V	V	
D		BG 6	W	W	05.05.25.1
E		PC B	X	X	05.06.08.1
F		BG 12	Y	Y	05.05.26.1
G	05.10.04.1	FREE RUN SS	Z	Z	05.15.03.1
H		SPARE	a	a	
J			b	b	
K			c	c	
L			d	d	
M			e	e	
N			f	f	
P			g	g	
Q			h	h	
R			i	i	

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Figure 10-4. Signal Interface List (Sheet 26)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
01B3C01-A B C D E F G H K L M N P Q R	05.11.13.1	DATA 1	01J05-t		P5-t
	05.11.13.1	2	s		s
	05.11.14.1	4	r		r
	⊥	8	q		q
		A	p		p
	05.11.15.1	B	n		n
	05.11.16.1	C	u		u
	05.11.08.1	TIME 015-030	G		G
		060-090	H		H
	⊥	090-000	d		d
		105-000	c		c
	05.11.17.1	PRINT READY	E		E
	05.11.02.1	PROC RELEASE	D		D
	05.11.07.1	PARITY CHECK	A		A
	05.11.15.1	CARR BUSY	BB		BB
01B3C02-A B C D E F G H K L M N P Q R	05.11.16.1	BLOCK DATA	01J05-R		P5-R
	05.11.15.1	CARR CH 12	DD		DD
	05.11.06.1	SP SUPP MOD	M		M
	05.11.17.1	RUN LATCH	y		y
	05.11.02.1	DT OFF	z		z
		START RST	S		S
	⊥	POWER ON RST	x		x
		PR CHECK RESET	B		B
	05.11.01.1	CARR CONTROL	v		v
	05.11.01.1	PRINT INSTR	K		K
	05.11.02.1	PROC +D CYCLE	F		F
		SPARE	AA		AA
		SPARE	CC		CC
	05.11.17.1	I/O CHK STP SW ON	C		C
		SPARE	L		L

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Figure 10-4. Signal Interface List (Sheet 27)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	PLUG	MATE	LOGIC SHEET
01B3A02-A B C D E F G H J K L M N P Q R	05.11.03.1 05.11.04.1	DATA BIT SIGN 1 2 3 4 5 6 7 SPARE DATA BIT 8 9 10 11 12 13 14	01P15-A B C D E F G H J K L M N P R S	02J12-A B C D E F G H J K L M N P R S	05.13.10.1 05.13.11.1
01B3A03-A B C D E F G H J K L M N P Q R	05.11.04.1 05.11.05.1 05.11.05.1 05.11.06.1 05.11.06.1 05.11.01.1	DATA BIT 15 16 17 18 19 20 21 22 SPARE DATA BIT 23 24 25 CODE 164 170 160 PRS	01P15-T U V W X Y Z a AA b c d e f g h	02J12-T U V W X Y Z a AA b c d e f g h	05.13.11.1 05.13.12.1 05.13.12.1 05.08.07.1 05.07.03.1
01B3A04-A B C D E F G H J K L M	05.11.01.1 05.11.06.1 05.11.01.1 05.11.07.1 05.11.07.1 05.11.17.1 05.11.17.1	-Y CODE 774 SPARE SPARE BG 10 BG 8 BG 9 +Y CODE 774 MACH RST 500 CPS MV PRNTR READY FREE RUN SS NT SPARE	01P15-i j J m n p k q r s t u	02J12-i j J m n p k q r s t u	05.08.02.2 05.05.26.1 05.05.25.1 05.05.26.1 05.08.02.2 05.04.01.1 05.15.03.1 00.04.15.3 05.15.03.1
EDGE CONN. 01B3D01-A	LOGIC SHEET 05.11.02.1	SIGNAL NAME VIA PRNTR HAMMER 01B02-14 HOLD	PLUG 01P11-P	MATE 02J2-P	REFERENCE LOGIC SHEET 00.03.50.0

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Figure 10-4. Signal Interface List (Sheet 28)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B8B01-A	05.13.10.1	A/S IND	03P17-B	00.04.05.0	J1-B
B	↓	DLA 2	D	↓	D
C	05.13.09.1	3	F	↓	F
D	05.13.10.1	4	H	↓	H
E	↓	5	K	↓	K
F	↓	6	M	↓	M
G	05.13.09.1	7	P	↓	P
H	05.13.10.1	8	S	↓	S
J	↓	9	U	↓	U
K	↓	10	W	↓	W
L	05.13.09.1	11	Y	↓	Y
M	05.13.10.1	12	a	↓	a
N	05.13.11.1	13	c	↓	c
P	↓	14	C	↓	C
Q	05.13.09.1	15	C	↓	C
R	05.13.11.1	16	E	↓	E
03B8D02-A	05.13.11.1	DLA 17 IND	03P17-G	00.04.05.0	J1-G
B	↓	18	J	↓	J
C	05.13.09.1	19	L	↓	L
D	05.13.11.1	20	N	↓	N
E	↓	21	R	↓	R
F	↓	22	T	↓	T
G	05.13.09.1	23	V	↓	V
H	05.13.11.1	24	X	↓	X
J	05.13.12.1	25	Z	↓	Z
K	↓	26	b	↓	b
L	05.13.09.1	27	e	↓	e
M	05.13.12.1	28	g	↓	g
N	↓	29	i	↓	i
P	↓	30	k	↓	k
Q	05.13.08.1	ACCO IND	n	↓	n
R	05.13.12.1	ACC1 IND	q	↓	q
03B8D03-A	05.13.08.1	DLB 1 IND	03P17-a	00.04.05.0	J1-a
B	05.13.12.1	2	u	↓	u
C	↓	3	w	↓	w
D	05.13.08.1	4	y	↓	y
E	↓	5	AA	↓	AA
F	↓	6	CC	↓	CC
G	↓	7	EE	↓	EE
H	↓	8	d	↓	d
J	↓	9	f	↓	f
K	↓	10	h	↓	h
L	↓	11	j	↓	j
M	↓	12	m	↓	m
N	↓	13	p	↓	p
P	↓	14	r	↓	r
Q	↓	15	t	↓	t
R	↓	16	v	↓	v
03B8H04-A	05.13.09.1	DLB 17 IND	03P17-x	00.04.05.0	J1-x
B	↓	18	z	↓	z
C	↓	19	BB	↓	BB
D	↓	20	DD	↓	DD
E	↓	21	FF	↓	FF
F	↓	AI 0 IND	GG	↓	GG
G	↓	1	HH	↓	HH
H	05.13.08.1	2	JJ	↓	JJ
J	↓	3	KK	↓	KK
K	↓	4	LL	↓	LL
L	↓	LAMP TEST CE 3	MM	↓	MM

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Figure 10-4. Signal Interface List (Sheet 29)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B8D01-A	05.13.02.1	DATA 1 IND 1	02J16-B	00.04.15.0	P1-B
B		DATA 1 IND 2	A		A
C		DATA 2 IND 1	D		D
D		DATA 2 IND 2	C		C
E		DATA 3 IND 1	F		F
F		DATA 3 IND 2	E		E
G		DATA 4 IND 1	H		H
H		DATA 4 IND 2	G		G
J	05.13.03.1	DATA 5 IND 1	K		K
K		DATA 5 IND 2	J		J
L		DATA 6 IND 1	M		M
M		DATA 6 IND 2	L		L
N		DATA 7 IND 1	P		P
P		DATA 7 IND 2	N		N
Q		DATA 8 IND 1	S		S
R		DATA 8 IND 2	R		R
03B8D02-A	05.13.04.1	DATA 9 IND 1	02J16-U	00.04.15.0	P1-U
B		DATA 9 IND 2	T		T
C		DATA 10 IND 1	W		W
D		DATA 10 IND 2	V		V
E		DATA 11 IND 1	Y		Y
F		DATA 11 IND 2	X		X
G		DATA 12 IND 1	a		a
H		DATA 12 IND 2	Z		Z
J	05.13.05.1	DATA 13 IND 1	c		c
K		DATA 13 IND 2	n		n
L	05.13.14.1	DISCR IN 1 SW	02J18-e	00.04.15.3	P3-e
M		DISCR IN 2 SW	e		e
N		DISCR IN 3 SW	a		a
P		DISCR IN 4 SW	Y		Y
Q		DISCR IN 5 SW	W		W
R		DISCR IN 6 SW	U		U
03B8D03-A	05.13.07.1	OP1 IND 1	02J16-e	00.04.15.0	P1-e
B		OP1 IND 2	d		d
C		OP2 IND 1	g		g
D		OP2 IND 2	f		f
E		OP3 IND 1	i		i
F		OP3 IND 2	h		h
G		OP4 IND 1	k		k
H		OP4 IND 2	j		j
J	05.13.01.1	MEM REG SW	02J19-U	00.04.15.2	P4-U
K		TR REG SW	V		V
L		ERROR RST SW	02J17-FF	00.04.15.1	P2-FF
M		CST IND 1	02J19-h	00.04.15.2	P4-h
N		CST IND 2	j		P4-j
P	05.13.05.1	MEM BUFF PAR IND 1	02J17-U	00.04.15.1	P2-U
Q		MEM BUFF PAR IND 2	T		P2-T
R					

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Figure 10-4. Signal Interface List (Sheet 30)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B8D04-A	05.13.16.1	SW PREG A 1	02J18-B	00.04.15.3	P3-B
B		B 1			P
C		A 2	C		C
D		B 2	q		q
E	05.13.17.1	A 3	D		D
F		B 3	r		r
G		A 4	E		E
H		B 4	s		s
J		A 5	F		F
K		B 5	t		t
L	05.13.18.1	A 6	G		G
M		B 6	u		u
N		A 7	H		H
P		B 7	v		v
Q		A 8	J		J
R		B 8	w		w
03B8E04-A	05.13.20.1	SW PREG A 9	02J16-K	00.04.15.3	P3-K
B		B 9	x		x
C		A 10	L		L
D		B 10	v		v
E	05.13.19.1	A 11	M		M
F		B 11	z		z
G		A 12	N		N
H		B 12	AA		AA
J		A 13	P		P
K		B 13	BB		BB
L	05.13.22.1	A 14	R		R
M		B 14	CC		CC
N	05.13.20.1	A 15	S		S
P		B 15	DD		DD
Q	05.13.21.1	A 16	T		T
R		B 16	EE		EE
03B8E05-A	05.13.21.1	SW PREG A 17	02J18-V	00.04.15.3	P3-V
B		B 17	FF		FF
C		A 18	X		X
D		B 18	GG		GG
E		A 19	Z		Z
F		B 19	HH		HH
G	05.13.14.1	A 20	h		h
H		B 20	JJ		JJ
J		A 21	d		d
K		B 21	KK		KK
L	05.13.15.1	A 22	i		i
M		B 22	LL		LL
N		A 23	k		k
P		B 23	MM		MM
Q		A 24	j		j
R		B 24	NN		NN
03B8F05-A	05.13.15.1	SW PREG A 25	02J18-m	00.04.15.3	P3-m
B		B 25	PP		PP
C	05.13.16.1	A SGN	A		A
D		B SGN	m		m
E	05.13.01.1	PAR ERROR IND	02J17-W	00.04.15.1	P2-W

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Figure 10-4. Signal Interface List (Sheet 31)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
03BR-D05-A	05.13.14.1	DISCR IN 1 SIG RET	Twisted Pair	00.04.53.0	9009J4- w x y z AA BB CC DD EE FF GG HH
B		DISCR IN 2 SIG RET			
C		DISCR IN 3 SIG RET			
D		DISCR IN 4 SIG RET			
E		DISCR IN 5 SIG RET			
F		DISCR IN 6 SIG RET			

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Figure 10-4. Signal Interface List (Sheet 32)

FROM			TO		REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	JACK	MATE	LOGIC SHEET
03B8F02-A	04.13.10.1	DATA BIT SIGN	02J12-	01P15-	05.11.03.1
B		1	A	A	
C		2	B	B	
D		3	C	C	
E		4	D	D	
F		5	E	E	
G		6	F	F	
H		7	G	G	
J		8	H	H	
K	04.13.11.1	9	K	K	05.11.04.1
L		10	L	L	
M		11	M	M	
N		12	N	N	
P		13	P	P	
Q		14	R	R	
R		15	S	S	
			T	T	
03B8F03-A	04.13.11.1	DATA BIT 16	02J12-	01P15-	05.11.05.1
B	04.13.11.1	17	U	U	
C	04.13.12.1	18	V	V	
D		19	W	W	
E		20	X	X	
F		21	Y	Y	
G		22	Z	Z	
H		23	a	a	
J		24	b	b	05.11.06.1
K		25	c	c	05.11.06.1
L		SPARE	d	d	
			J	J	

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Figure 10-4. Signal Interface List (Sheet 33)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B7B01-A	05.14.06.1	SW ERR RST	02J9- c	00.04.10.0	P6-c
B	05.14.21.1	SW SGDTC NOT	h		h
C	05.14.21.1	SW SGDTC	i		i
D	05.14.23.1	SW RPT	g		g
E	05.14.23.1	SW RPT NOT	f		f
F	05.14.01.1	TPE IND	d		d
G	05.14.07.1	TR SYL 1 PB IND	b	00.04.10.1	b
H	05.14.08.1	TR SYL 0 PB IND	a		a
J	05.14.10.1	SER PB IND 1	n	00.04.10.0	n
K	05.14.10.1	SER PB IND 2	p		p
L	05.14.17.1	SPE IND	e		e
M	05.14.23.1	DTRPT IND	k		k
N	05.14.23.1	DTRPT NOT IND	m		m
P	05.14.07.1	SW LAMP TEST 2	K		K
03B7A01-A	05.14.02.1	TRACK 1	03P16- 1	Reference RHEEM 03A2J1-1	
B		2	2	TAPE READER	2
C	05.14.03.1	3	3	MAINTENANCE	3
D		4	4	MANUAL	4
E	05.14.04.1	5	5	MODEL RR-1002B. L, R	5
F		6	6		6
G	05.14.06.1	7	7		7
H		8	8		8
03B7B02-A	05.14.02.1	CHANL 1 NOT	03P15- A	00.04.05.2	J4- A
B		2	C		C
C	05.14.03.1	3	E		E
D		4	G		G
E	05.14.04.1	5	J		J
F		6	L		L
G	05.14.06.1	SEQ INT NOT	D		D
H		TAPB NOT	F		F
03B7C03-A	05.14.05.1	SW TRCH 1 - 01	03J10- a	00.04.01.1	P2-a
B		SW TRCH 2 - 01	c		c
C		SW TRCH 3 - 01	e		e
D		SW TRCH 4 - 01	g		g
E		SW TRCH 5 - 01	i		i
03B7C01-A	05.14.05.1	SW TRCH 1 - 02	02J9- L	00.04.10.2	P6-L
B		SW TRCH 2 - 02	K		K
C		SW TRCH 3 - 02	J		J
D		SW TRCH 4 - 02	H		H
E		SW TRCH 5 - 02	G		G
F		SW TRCH 6 - 02	F		F
03B7C03- F	05.14.15.1	2 to SEVEN IND	03J10- U	00.04.01.1	P2-U
G		2 to EIGHT IND	q		q
H		2 to NINE IND	r		r
J		2 to TEN IND	s		s
K		2 to ELEVEN IND	t		t

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Figure 10-4. Signal Interface List (Sheet 34)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B6C01-A	05.15.01.1	SW ML	03J10-A	00.04.01.1	P2-A
B	05.15.01.1	SW DD	B		B
C	05.15.17.1	START	C		C
D		START NOT	D		D
E		ADV NOT	E		E
F		ADV	F		F
G	05.15.01.1	MAN	G		G
H	05.15.01.1	AUTO	H		H
J	05.15.18.1	STOP	J		J
K	05.15.16.1	TA PWR	L		L
L	05.15.21.1	PWR RLY GRD	N		N
M	05.15.20.1	LAMP TEST 1A	P		P
N	05.15.03.1	FR SS NOT	S		S
P	05.15.14.1	FRTR	X		X
Q	05.15.15.1	DIR	V		V
R	05.15.15.1	DIR NOT	W		W
03B6C02-A	05.15.17.1	FRTR NOT	Y		Y
B	05.15.19.1	VER ONLY NOT	Z		Z
C	05.15.19.1	VER ONLY	AA		AA
D	05.15.05.1	SEL ADR	BB		BB
E	05.15.02.1	FRR TEST	DD		DD
F	05.15.02.1	ERR TEST NOT	EE		EE
G	05.15.13.1	RESET 2	HH		HH
H	05.15.01.1	LAMP TEST 1	T		T
K	05.15.13.1	TRGB9	GG		GG
03B6B01-A	05.15.20.1	DD IND	03J9-A	00.04.01.0	P1-A
B	05.15.01.1	ML IND	B		B
C	05.15.16.1	START IND 2	C		C
D	05.15.16.1	START IND 1	D		D
E	05.15.15.1	ADV IND 2	E		E
F	05.15.17.1	ADV IND 1	F		F
G	05.15.20.1	MAN IND	G		G
H	05.15.01.1	AUTO IND	H		H
J	05.15.16.1	STOP IND 2	J		J
K	05.15.16.1	STOP IND 1	K		K
L	05.15.15.1	RVS IND	N		N
M	05.15.15.1	FWD IND	P		P
N	05.15.19.1	VER ONLY IND B	R		R
P	05.15.19.1	VER ONLY IND A	S		S
Q	05.15.05.1	SEL ADR IND	T		T
03B6B02-A	05.15.02.1	SW IA	02J9-r	00.04.10.0	P6-r
B	05.15.02.1	SW IA NOT	q	00.04.10.0	q
C	05.15.03.1	SW RESET 1	M	00.04.10.2	M
D	05.15.03.1	SW START SS	A	00.04.10.3	A
E	05.15.21.1	SW LAMP TEST 2A	v	00.04.10.0	v
L	05.15.20.1	SW TR RST	j		j
M	05.15.21.1	IA COMP IND	t		t
N	05.15.21.1	DA COMP IND	s		s
P	05.15.22.1	SE1 IND	LL		LL
Q	05.15.22.1	SE2 IND	MM		MM

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Figure 10-4. Signal Interface List (Sheet 35)

FROM			TO			
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG	
03B6D03-A B C D E F G H J K L M N P Q R	05.15.03.1	500 CPS MV	03P15-K	00.04.05.2	03A4J4-K	
	05.15.04.1	TRCP 1 A	N		N	
	05.15.04.1	2 A	R		R	
	05.15.05.1	3 A	T		T	
	05.15.05.1	4 A	U		U	
	05.15.07.1	10 CPS MV	M		M	
	05.15.11.1	TRCB 1 A	V		V	
	05.15.11.1	2 A	W		W	
	05.15.12.1	3 A	X		X	
			4 A	Y		Y
			5 A	Z		Z
			6 A	a		a
	05.15.13.1	7 A	b			b
			8 A	c		c
		9 A	H		H	
		SPARE	B		K	
03B6C03-A B	05.15.07.1	TRCP ERR DLY SPARE	03P15-S	00.04.05.2	03A4J4-S P	
03B6B03-A B C	05.15.03.1	FEED TRACK	03P16-9	00.04.05.2	03A2J1-9	
	05.15.14.1	DRIVE LEFT	11	Reference RHEEM	11	
	05.15.14.1	DRIVE RIGHT	10	Tape Reader Maintenance Manual Model RR-1002-2B, L, R	10	
03B6A01-A B C D E F G H K L M N P Q R	05.15.11.1	SW TRCB1	02J9-E	00.04.10.2	02A1P6-E	
	05.15.11.1	TRCB2	D		D	
	05.15.12.1	TRCB3	C		C	
		TRCB4	B		B	
		TRCB5	S	00.04.10.1	S	
		TRCB6	R		R	
	05.15.13.1	TRCB7	P		P	
	05.15.13.1	TRCB8	N		N	
		SPARE	T		T	
			U		U	
			V		V	
			W		W	
			X		X	
			Y		Y	
		Z		Z		
			REFERENCE			
03B6A03-A B C D	05.15.03.1	500 CPS MV	JACK	MATE	LOGIC SHEET	
	05.15.03.1	FREE RUN SS NT	02J12-r	01P15-r	05.11.07.1	
	05.15.17.1	10 CPS MV	02J12-t	01P15-t	05.11.17.1	
	05.15.03.1	FREE RUN SS	02J13-S	01P16-S	05.09.06.1	
			02J13-Z	01P16-Z	05.10.04.1	

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Figure 10-4. Signal Interface List (Sheet 36)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B5B02-A	05.16.14.1	SECK IND	03J9-U	00.04.01.0	03P1-U
B	05.16.09.1	2 to ZERO	a		a
C	05.16.13.1	TAADR1	V		V
D		TAADR2	W		W
E		TAADR3	X		X
F	05.16.14.1	TAADR4	Y		Y
G	05.16.14.1	TAADR5	Z		Z
H	05.16.09.1	2 TO ONE	g		g
J	05.16.09.1	2 TO TWO	h		h
K	05.16.07.1	2 TO THREE	q		q
L	05.16.14.1	SEL_CNTR	r		r
03B5C03-A	05.16.16.1	TRIS1 IND	02J4-C	00.04.10.3	02P1-C
B		TRIS2	D		D
C		TRIS3	E		E
D		TRIS4	F		F
E	05.16.17.1	TRA 1	G		G
F		TRA 2	H		H
J		TRA 3	J		J
H		TRA 4	K		K
J	05.16.18.1	TRA 5	L		L
K		TRA 6	M		M
L		TRA 7	N		N
M		TRA 8	P		P
03B5E02-A	05.16.12.1	TRDS 1 IND	02J4-W	00.04.10.2	P1-W
B		TRDS 2	X		X
C		TRDS 3	Y		Y
D		TRDS 4	Z		Z
E	05.16.19.1	TRSYL 0	A	00.04.10.3	A
F	05.16.19.1	TRSYL 1	B	00.04.10.3	B
G	05.16.15.1	TRDM 1	q	00.04.10.2	q
H	05.16.15.1	TRDM 0	p	00.04.10.2	p
J	05.16.19.1	TRIM0 1A	R	00.04.10.3	R
K	05.16.19.1	TRIM1 1A	S	00.04.10.3	S

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Figure 10-4. Signal Interface List (Sheet 37)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
03B5A01-A	05.16.01.1	TR SIGN IND	02.15-A	00.04.10.1	02P2-A
B		TRB1	B		B
C		TRB2	C		C
D		TRB3	D		D
E	05.16.02.1	TRB4	E		E
F		TRB5	F		F
G		TRB6	G		G
H		TRB7	H		H
J	05.16.03.1	TRB8	J		J
K		TRB9	K		K
L		TRB10	L		L
M		TRB11	M		M
N	05.16.04.1	TRB12	N		N
P		TRB13	P		P
Q		TRB14	R		R
R		TRB15	S		S
03B5A04-A	05.16.05.1	TRB16 IND	02.15-T	00.04.10.1	02P2-T
B		TRB17	U		U
C		TRB18	V		V
D		TRB19	W		W
E	05.16.06.1	TRB20	X		X
F		TRB21	Y		Y
G		TRB22	Z		Z
H		TRB23	a		a
J	05.16.07.1	TRB24	b		b
K	05.16.07.1	TRB25	c		c
L	05.16.01.1	SW LAMP TEST 2	d		d
03B5B01-A	05.16.08.1	TROA1 IND	02.14-a	00.04.10.2	02P1-a
B		TROA2	b		b
C		TROA3	c		c
D		TROA4	d		d
E	05.16.09.1	TROA5	e		e
F		TROA6	f		f
G		TROA7	g		g
H	05.16.10.1	TROA8	h		h
J	05.16.10.1	TROA9	i		i
K	05.16.11.1	TROP1	j		j
L		TROP2	k		k
M		TROP3	m		m
N		TROP4	n		n

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Figure 10-4. Signal Interface List (Sheet 38)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	VIA	LOGIC SHEET	PLUG
02B5C04-A B C D E F G H J K L M N P Q R	05.20.13.1 05.20.14.1 	A1 IND 2 A1 IND 1 A2 IND 2 A2 IND 1 A3 IND 2 A3 IND 1 A4 IND 2 A4 IND 1 A5 IND 2 A5 IND 1 A6 IND 2 A6 IND 1 A7 IND 2 A7 IND 1 A8 IND 2 A8 IND 1	02J16-m n p q r s t u v w x y z AA BF CC	00.04.15.0 	P1-m n p q r s t u v w x y z AA BB CC
02B5C03-A B	05.20.18.1 	A9 IND 2 A9 IND 1	02J16-DD EE	00.04.15.0 	P1-DD EE
02B5D04-A B C D F G H J K L M N P Q R	05.20.17.1 05.20.16.1 05.20.15.1 05.20.16.1 05.20.15.1 05.20.16.1 05.20.15.1 05.20.16.1 05.20.18.1	IM 1 IND IM 0 IND DM 1 IND DM 0 IND DS 1 IND IS 1 IND DS 2 IND IS 2 IND DS 3 IND IS 3 IND DS 4 IND IS 4 IND SYL 1 IND 2 SYL 1 IND 1 SYL 0 IND 2 SYL 0 IND 1	02J17-A B C D E F G H J K L M N P R S	00.04.15.1 	P2-A B C D E F G H J K L M N P R S
02B5D03-A B C D E F G H J K L M N P Q R	05.20.12.1 05.20.11.1 05.20.10.1 05.20.09.1	IND B 1 IND I 1 B 2 I 2 B 3 I 3 B 4 I 4 B 5 I 5 B 6 I 6 B 7 I 7 B 8 I 8	02J17-X Y Z a b c d e f g h i j k m n	00.04.15.1 	P2-X Y Z a b c d e f g h i j k m n

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Figure 10-4. Signal Interface List (Sheet 39)

FROM			VIA	TO	
EDGE CON.N.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG
02B5E04-A B C D E F G H J K L M N P Q R	05.20.08.1 ┆ 05.20.07.1 ┆ 05.20.06.1 ┆ 05.20.05.1 ┆	IND B 9 I 9 B 10 I 10 B 11 I 11 B 12 I 12 B 13 I 13 B 14 I 14 B 15 I 15 INT 16 IND 2 INT 16 IND 1	02J17-p q r s t u v w x y z AA BB CC DD EE	00.04.15.2 ┆	P2-p q r s t u v w x y z AA BB CC DD EE
02B5E03-A B C D E F G H J K L M N P Q R	05.20.12.1 ┆ 05.20.11.1 ┆ 05.20.10.1 ┆ 05.20.09.1 ┆ 05.20.08.1 ┆ 05.20.07.1 ┆ 05.20.06.1 ┆ 05.20.05.1 ┆ 05.20.24.1	INH SW 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 INT 16 SW OFF	02J19-A B C D E F G H J K L M N P R S	00.04.15.1 ┆ 00.04.15.2 ┆	P4-A B C D E F G H J K L M N P R S
02B5F04-A B C D E F G	05.20.15.1 ┆ 05.20.02.1 ┆ 05.20.18.1 ┆ 05.20.24.1 ┆ 05.20.02.1	MEM ADD SW HOPSAVE SW INH CTRL OFF LAMP TEST INT 16 SW ON INH CTRL ON	02J19-Y a d DD b c	00.04.15.2 ┆	P4-Y a d DD b c

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Figure 10-4. Signal Interface List (Sheet 40)

FROM				TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PLUG	
02H5A04-A	05.20.01.1	INTRPT 1 SIG RET	Twisted Pair	00.04.52.0	9009J3-g h i j k m n p q r s t u v w x	
B		INTRPT 2 SIG RET				
C		INTRPT 3 SIG RET				
D		INTRPT 4 SIG RET				
E		INTRPT 5 SIG RET				
F		INTRPT 6 SIG RET				
G		INTRPT 7 SIG RET				
H		INTRPT 8 SIG RET				
J		See Note				
K		05.20.01.1				INTRPT 9 SIG RET
L						INTRPT 10 SIG RET
M						INTRPT 11 SIG RET
N						INTRPT 12 SIG RET
P						INTRPT 13 SIG RET
Q						INTRPT 14 SIG RET
R			INTRPT 15 SIG RET			
03TB4 - 14	00.03.60.0		CHASSIS			PP
03W1A- 19			TESPG			F
03W1A- 20			TESPG			G

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Figure 10-4. Signal Interface List (Sheet 41)

FROM				TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PIN
02A4 E01-A	05.26.02.1	X UNITS 0 DR A	Twisted Pair	01.01.01.0	02A03MBADB-R
E02-A		0 RET A			J
E01-B		1 DR A			S
E02-B		1 RET A			K
E01-C		2 DR A			T
E02-C		2 RET A			L
E01-D		3 DR A			U
E02-D		3 RET A			M
E01-E		4 DR A			V
E02-E		4 RET A			N
E01-F		5 DR A			W
E02-F		5 RET A			O
E01-G		6 DR A			X
E02-G		6 RET A			P
E01-H		7 DR A			Y
E02-H		7 RET A			Q
E01-J	05.26.03.1	X EIGHTS 0 DR A			A
E02-J		0 RET A			E
E01-K		1 DR A			B
E02-K		1 RET A			F
E01-L		2 DR A			C
E02-L		2 RET A			G
E01-M		3 DR A			D
E02-M		3 RET A			H
E01-N		4 DR A			A
E02-N		4 RET A		02A03MBADB-	E
E01-P		5 DR A			B
E02-P		5 RET A			F
E01-Q		6 DR A			C
E02-Q		6 RET A			G
E01-R		7 DR A			D
E02-R		7 RET A			H
E03-A	05.26.02.1	X UNITS 0 DR A			R
E04-A		0 RET A			J
E03-B		1 DR A			S
E04-B		1 RET A			K
E03-C		2 DR A			T
E04-C		2 RET A			L
E03-D		3 DR A			U
E04-D		3 RET A			M
E03-E		4 DR A			V
E04-E		4 RET A			N
E03-F		5 DR A			W
E04-F		5 RET A			O
E03-G		6 DR A			X
E04-G		6 RET A			P
E03-H		7 DR A			Y
E04-H		7 RET A			Q

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Figure 10-4. Signal Interface List (Sheet 42)

EDGE CONN.	FROM				TO		
	LOGIC SHEET	SIGNAL NAME	LOGIC SHEET		PIN		
02A4 E05-A	05.26.04.1	Y UNITS	0 DR A	Twisted Pair	01.01.01.0	02A3MBBDB-	R
E06-A			0 RET A				J
E05-B			1 DR A				S
E06-B			1 RET A				K
E05-C			2 DR A				T
E06-C			2 RET A				L
E05-D			3 DR A				U
E06-D			3 RET A				M
E05-E			4 DR A				V
E06-E			4 RET A				N
E05-F			5 DR A				W
E06-F			5 RET A				O
E05-G			6 DR A				X
E06-G			6 RET A				P
E05-H	7 DR A	7					
E06-H	7 RET A	7					
E05-I	05.26.05.1	Y EIGHTS	0 DR A			02A3MBBDB-	Q
E06-I			0 RET A				A
E05-K			1 DR A				B
E06-K			1 RET A				F
E05-L			2 DR A				C
E06-L			2 RET A				G
E05-M			3 DR A				D
E06-M			3 RET A				H
E05-N			4 DR A				A
E06-N			4 RET A				E
E05-P			5 DR A				B
E06-P			5 RET A				F
E05-Q			6 DR A				C
E06-Q			6 RET A				G
E05-R	7 DR A	D					
E06-R	7 RET A	H					
E07-A	05.26.04.1	Y UNITS	0 DR A				R
E08-A			0 RET A				J
E07-B			1 DR A				S
E08-B			1 RET A				K
E07-C			2 DR A				T
E08-C			2 RET A				L
E07-D			3 DR A				U
E08-D			3 RET A				M
E07-E	4 DR A	V					
E08-E	4 RET A	N					
E07-F	5 DR A	W					
E08-F	5 RET A	O					
E07-G	6 DR A	X					
E08-G	6 RET A	P					
E07-H	7 DR A	7					
E08-H	7 RET A	7					
							Q

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Figure 10.4. Signal Interface List (Sheet 43)

FROM				TO		
EDGE CONN	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PIN	
02A4 E09-A	05.26.06.1	X UNITS	0 DR B	01.01.01.0	02A3MBADB-	R
E10-A			0 RET B			J
E09-B			1 DR B			S
E10-B			1 RET B			K
E09-C			2 DR B			T
E10-C			2 RET B			L
E09-D			3 DR B			U
E10-D			3 RET B			M
E09-E			4 DR B			V
E10-E			4 RET B			N
E09-F			5 DR B			W
E10-F			5 RET B			O
E09-G			6 DR B			X
E10-G			6 RET B			P
E09-H			7 DR B			Y
E10-H			7 RET B			Q
E11-J	05.26.07.1	X EIGHTS	0 DR B			A
E12-J			0 RET B			E
E11-K			1 DR B			B
E12-K			1 RET B			F
E11-L			2 DR B			C
E12-L			2 RET B			G
E11-M			3 DR B			D
E12-M			3 RET B			H
E11-N			4 DR B			A
E12-N			4 RET B			E
E11-P			5 DR B			B
E12-P			5 RET B			F
E11-Q			6 DR B			C
E12-Q			6 RET B			G
E11-R			7 DR B			D
E12-R			7 RET B			H
E11-A	05.26.06.1	X UNITS	0 DR B			R
E12-A			0 RET B			J
E11-B			1 DR B			S
E12-B			1 RET B			K
E11-C			2 DR B			T
E12-C			2 RET B			L
E11-D			3 DR B			U
E12-D			3 RET B			M
E11-E			4 DR B			V
E12-E			4 RET B			N
E11-F			5 DR B			W
E12-F			5 RET B			O
E11-G			6 DR B			X
E12-G			6 RET B			P
E11-H			7 DR B			Y
E12-H			7 RET B			Q

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Figure 10-4. Signal Interface List (Sheet 44)

FROM					TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME			LOGIC SHEET	PIN	
02A4 E13-A	05.26.08.1	Y UNITS	0 DR B	Twisted Pair	01.01.01.0	02A03MADDB-R	
E14-A			0 RET B				J
E13-B			1 DR B				S
E14-B			1 RET B				K
E13-C			2 DR B				T
E14-C			2 RET B				L
E13-D			3 DR B				U
E14-D			3 RET B				M
E13-E			4 DR B				V
E14-E			4 RET B				N
E13-F			5 DR B				W
E14-F			5 RET B				O
E13-G			05.26.09.1				Y EIGHTS
E14-G	6 RET B	X					
E13-H	7 DR B	P					
E14-H	7 RET B	Y					
E13-J	0 DR B	Q					
E14-J	0 RET B	A					
E13-K	1 DR B	E					
E14-K	1 RET B	B					
E13-L	05.26.08.1	Y UNITS	2 DR B				
E14-L			2 RET B				C
E13-M			3 DR B				G
E14-M			3 RET B				D
E13-N			4 DR B				H
E14-N			4 RET B				A
E13-P			5 DR B				B
E14-P			5 RET B				F
E13-Q			6 DR B				C
E14-Q			6 RET B				G
E13-R	05.26.08.1	Y UNITS	7 DR B				
E14-R			7 RET B				D
E15-A			0 DR B				R
E16-A			0 RET B				J
E15-B			1 DR B				S
E16-B			1 RET B				K
E15-C			2 DR B				T
E16-C			2 RET B				L
E15-D			3 DR B				U
E16-D			3 RET B				M
E15-E			4 DR B				V
E16-E			4 RET B				N
E15-F			5 DR B				W
E16-F			5 RET B				O
E15-G			6 DR B				X
E16-G			6 RET B				P
E15-H	7 DR B	Y					
E16-H	7 RET B	Q					

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Figure 10-4. Signal Interface List (Sheet 45)

FROM		TO			REFERENCE
EDGE CONN.	LOGIC SHEET	SIGNAL NAME	JACK	MATE	LOGIC SHEET
02A4D07- A	05.26.04.1 05.26.08.1	MAR 8	J2- H	02P10- H	05.05.11.1
B	05.26.04.1 05.26.08.1	9	J	J	05.05.08.1
C	05.26.05.1 05.26.09.1	10 NOT	Y	Y	05.05.08.1
D	05.26.05.1 05.26.09.1	11 NOT	Z	Z	05.05.06.1
E	05.26.05.1 05.26.09.1	10	K	K	05.05.07.1
F	05.26.05.1 05.26.09.1	12 NOT	a	a	05.05.06.1
G	05.26.05.1 05.26.09.1	11	L	L	05.05.07.1
H	05.26.05.1 05.26.09.1	12	M	M	05.05.07.1
02A4D08- A	05.26.02.1 05.26.06.1	MAR 1	J2- A	02P10- A	05.05.09.1
B	05.26.02.1 05.26.06.1	1 NOT	N	N	05.05.09.1
C	05.26.02.1 05.26.06.1	3 NOT	R	R	05.05.10.1
D	05.26.02.1 05.26.06.1	2	P	P	
E	05.26.02.1 05.26.06.1	2	B	B	
F	05.26.02.1 05.26.06.1	3	C	C	
G	05.26.03.1 05.26.07.1	4 NOT	S	S	
H	05.26.03.1 05.26.07.1	5	T	T	
J	05.26.03.1 05.26.07.1	6	U	U	05.05.11.1
K	05.26.03.1 05.26.07.1	4	D	D	05.05.10.1
L	05.26.03.1 05.26.07.1	5	E	E	05.05.10.1
M	05.26.03.1 05.26.07.1	6	F	F	05.05.11.1
N	05.26.04.1 05.26.08.1	7 NOT	V	V	05.05.11.1
P	05.26.04.1 05.26.08.1	8	W	W	05.05.11.1
Q	05.26.04.1 05.26.08.1	9	X	X	05.05.09.1
R	05.26.04.1	7	G	C	05.05.11.1
02A4D18- E	05.26.01.1	22 DEGREES CENT A	02A-3	000A- C	
F		29 DEGREES CENT A		D	
R		35 DEGREES CENT A		E	
02A4D21- E	05.26.01.1	22 DEGREES CENT B		000B- C	
F		29 DEGREES CENT B		D	
R		35 DEGREES CENT B		E	

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Figure 10-4. Signal Interface List (Sheet 46)

FROM			TO		
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PIN
02A5E03-	B 05.27. 12.1	INH A 0 MB1 RET	Twisted Pair	01.01.04.0	02A3MABP1-2
	A 16.1	MB1			3
	D 12.1	MB2 RET			68
	C 16.1	MB2			69
	F 12.1	1 MB2 RET			70
	H 16.1	MB2			71
	G 12.1	MB1 RET			136
	J 16.1	MB1			137
	K 12.1	0 MB3 RET			02A3MABP2-2
	L 16.1	MB3			3
	M 12.1	MB4 RET			68
	N 16.1	MB4			69
	P 12.1	1 MB4 RET			70
	Q 16.1	MB4			71
	R 12.1	MB3 RET			136
	02A5E04-	MB3			137
	B 12.1	INH A 0 MB5 RET			02A3MABP3-2
	A 16.1	MB5			3
	D 13.1	MB6 RET			68
	C 16.1	MB6			69
	F 13.1	1 MB6 RET			70
	E 16.1	MB6			71
	H 13.1	MB5 RET			136
	G 16.1	MB5			137
	J 13.1	0 MB7 RET		02A3MABP4-2	
	K 16.1	MB7		3	
	L 13.1	MB8 RET		68	
	M 16.1	MB8		69	
	N 13.1	MB8 RET		70	
	P 16.1	MB8		71	
	Q 13.1	MB7 RET		136	
	R 16.1	MB7		137	
	02A5E05-	INH A 0 MB9 RET		02A3MABP5-2	
	B 14.1	MB9		3	
	A 16.1	MB9		68	
	D 14.1	MB10 RET		69	
	C 16.1	MB10		70	
	F 14.1	1 MB10 RET		71	
	E 16.1	MB10		136	
	H 14.1	MB9 RET		137	
	G 16.1	MB9		02A3MABP6-2	
	J 14.1	0 MB11 RET		3	
	K 16.1	MB11		68	
	L 14.1	MB12 RET		69	
	M 16.1	MB12		70	
	N 14.1	1 MB12 RET		71	
	P 16.1	MB12		136	
	Q 14.1	MB11 RET		137	
	R 16.1	MB11		02A3MABP7-2	
	02A5E06-	INH A 0 MB13 RET		3	
	B 15.1	MB13		68	
	A 16.1	PAR RET		69	
	D 15.1	PAR		70	
	C 16.1	PAR RET		71	
	F 15.1	PAR		136	
	E 16.1	PAR		137	
	H 15.1	MB13 RET			
	G 16.1	MB13			

6900505-REL (66118KR)

LN 04.27.01.0

Figure 10-4. Signal Interface List (Sheet 47)

FROM					TO	
EDGE CONN.	LOGIC SHEET	SIGNAL NAME		LOGIC SHEET	PIN	
02A5 E11-B	05.27.12.1	INH B 0 MB1 RET	Twisted Pair	01.01.04.1	02A3MBBP1-2	
A	17.1	0 MB1		3		
D	12.1	0 MB2 RET			68	
C	17.1	0 MB2			69	
F	12.1	1 MB2 RET			70	
E	17.1	1 MB2			71	
H	12.1	1 MB1 RET			136	
G	17.1	1 MB1			137	
J	12.1	0 MB3 RET			02A3MBBP2-2	
K	17.1	0 MB3			3	
L	12.1	0 MB4 RET			68	
M	17.1	0 MB4			69	
N	12.1	1 MB4 RET			70	
P	17.1	1 MB4			71	
Q	12.1	1 MB3 RET			136	
R	17.1	1 MB3			137	
E12-B	13.1	0 MB5 RET			02A3MBBP3-2	
A	17.1	0 MB5			3	
D	13.1	0 MB6 RET			68	
C	17.1	0 MB6			69	
F	13.1	1 MB6 RET			70	
E	17.1	1 MB6			71	
H	13.1	1 MB5 RET			136	
G	17.1	1 MB5			137	
J	13.1	0 MB7 RET			02A3MBBP4-2	
K	17.1	0 MB7			3	
L	13.1	0 MB8 RET			68	
M	17.1	0 MB8			69	
N	13.1	1 MB8 RET			70	
P	17.1	1 MB8			71	
Q	13.1	1 MB7 RET			136	
R	17.1	1 MB7			137	
E13-B	14.1	0 MB9 RET			02A3MBBP5-2	
A	17.1	0 MB9			3	
D	14.1	0 MB10 RET			68	
C	17.1	0 MB10			69	
F	14.1	1 MB10 RET			70	
E	17.1	1 MB10			71	
H	14.1	1 MB9 RET			136	
G	17.1	1 MB9			137	
J	14.1	0 MB11 RET			02A3MBBP6-2	
K	17.1	0 MB11			3	
L	14.1	0 MB12 RET			68	
M	17.1	0 MB12			69	
N	14.1	1 MB12 RET			70	
P	17.1	1 MB12			71	
Q	14.1	1 MB11 RET			136	
R	17.1	1 MB11			137	
E14-B	15.1	0 MB13 RET			02A3MBBP7-2	
A	17.1	0 MB13			3	
D	15.1	0 PAR RET			68	
C	17.1	0 PAR			69	
F	15.1	1 PAR RET			70	
E	17.1	1 PAR			71	
H	15.1	1 MB13 RET			136	
G	17.1	1 MB13			137	

LN 04.27.02.0

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Figure 10-4. Signal Interface List (Sheet 48)

FROM		SIGNAL NAME	TO		REFERENCE LOGIC SHEET
EDGE CONN.	LOGIC SHEET		JACK	MATE	
02A5E20-A	05.27.03.1	MAR 5 NOT READ	02A3J2- c	02P10- c	05.05.20.1
B	05.27.03.1	MAR 5 READ	b	b	05.05.20.1
C	05.27.03.1	FORCE WR 1	g	g	FOR TEST ONLY
D	05.27.04.1	MBR SW 1	j	j	00.04.05.1
E	05.27.05.1	2	k	k	
F	05.27.06.1	3	m	m	
G	05.27.06.1	4	n	n	
H	05.27.07.1	5	p	p	
J	05.27.07.1	6	q	q	
K	05.27.08.1	7	r	r	
L	05.27.08.1	8	s	s	
M	05.27.09.1	9	t	t	
N	05.27.09.1	10	u	u	
P	05.27.10.1	11	v	v	
Q	05.27.10.1	12	w	w	
02A5E10-A	05.27.11.1	MBR SW 13	02A3J2- x	02P10- x	00.04.05.1
B	05.27.11.1	MBR SW PAR	y	y	00.04.05.1
C	05.27.05.1	SET MBR 1	z	z	05.07.24.1
	05.27.06.1				
	05.27.07.1				
	05.27.08.1				
02A5E10-D	05.27.09.1	SET MBR 2	02A3J2- AA	02P10- AA	05.07.24.1
	05.27.10.1				
	05.27.11.1				
02A5E10-E	05.27.05.1	CBR 1	02A3J2- h	02P10- h	05.07.08.1
	05.27.06.1				
	05.27.07.1				
	05.27.08.1				
02A5E10-F	05.27.09.1	CBR 2	02A3J2- i	02P10- i	05.07.08.1
	05.27.10.1				
	05.27.11.1				
02A5E10-G	05.27.01.1	SYL 1	02A3J2- f	02P10- f	05.05.01.1
	05.27.02.1	SYL 1			
02A5E10-H	05.27.03.1	STROBE A INH	02A3J4- N	02P13- N	05.05.01.1
02A5E10-I	05.27.04.1	STROBE B INH	02A3J5- J	02P14- J	05.05.01.1
02A5E19-A	05.27.03.1	RD DLY 2.25 A	02A3J4- C	02P13- C	05.05.15.1
B		RD DLY 1.75 A	K	K	05.05.15.1
C		INHIBIT GATE A	E	E	05.05.14.1
D	05.27.01.1	RD & WR DLY 0.75 A	A	A	05.05.16.1
E		RD & WR DLY 2.75 A	D	D	05.05.16.1
F		PTC READ GATE A	H	H	05.05.15.1
G		PTC WRITE GATE A	J	J	05.05.15.1
H		RD & WR DLY 1.25 A	B	B	05.05.16.1
02A5E18-A	05.27.04.1	RD DLY 2.25 B	02A3J5- C	02P14- C	05.05.19.1
B		RD DLY 1.75 B	K	K	05.05.19.1
C		INHIBIT GATE B	E	E	05.05.17.1
D	05.27.02.1	RD & WR DLY 0.75 B	A	A	05.05.18.1
E		RD & WR DLY 2.75 B	D	D	05.05.18.1
F		PTC READ GATE B	H	H	05.05.19.1
G		PTC WRITE GATE B	J	J	05.05.19.1
H		RD & WR DLY 1.75 B	B	B	05.05.18.1

6900505-REL (66118KR)

LN 04.27.03.0

Figure 10-4. Signal Interface List (Sheet 49)

FROM		SIGNAL NAME	TO		REFERENCE
EDGE CONN.	LOGIC SHEET		JACK	MATE	LOGIC SHEET
02A5E15- A	05.27.09.1	NT MBR9	02A3J3- Y	02P12- Y	05.07.25.1
B		MBR 9	J	J	05.07.26.1
C		MBR 10	K	K	05.07.26.1
D		NT MBR 10	Z	Z	05.07.25.1
E	05.27.10.1	NT MBR 11	a	a	05.07.25.1
F		MBR 11	L	L	05.07.26.1
G		MBR 12	M	M	05.07.26.1
H		NT MBR 12	b	b	05.07.25.1
J	05.27.11.1	NT MBR 13	c	c	05.07.25.1
K		MBR 13	N	N	05.07.26.1
L		MBR 14	d	d	05.07.26.1
M		NT MBR 14	e	e	05.07.25.1
02A5E16- A	05.27.05.1	NT MBR 1	02A3J3- P	02P12- P	05.07.24.1
B		MBR 1	A	A	05.07.26.1
C		MBR 2	B	B	05.07.26.1
D		NT MBR 2	R	R	05.07.24.1
E	05.27.06.1	NT MBR 3	S	S	05.07.24.1
F		MBR 3	C	C	05.07.26.1
G		MBR 4	D	D	05.07.26.1
H		NT MBR 4	T	T	05.07.24.1
J	05.27.07.1	NT MBR 5	U	U	05.07.24.1
K		MBR 5	F	F	05.07.26.1
L		MBR 6	F	F	05.07.26.1
M		NT MBR 6	V	V	05.07.24.1
N	05.27.08.1	NT MBR 7	W	W	05.07.25.1
P		MBR 7	G	G	05.07.26.1
Q		MBR 8	H	H	05.07.26.1
R		NT MBR 8	X	X	05.07.25.1

LN 04.27.04.0

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Figure 10-4. Signal Interface List (Sheet 50)

V-10-60

FROM		SIGNAL NAME	Twisted Pair	TO	
EDGE CONN.	LOGIC SHEET			LOGIC SHEET	PIN
02A06A14-D	05.28.01.1	SENSE A MB1A SEG1		01.01.04.1	02A3MACP1- 1
E		TW SENSE A MB1A SEG1			2
G		SENSE A MB1B SEG2			68
F		TW SENSE A MB1B SEG2			69
A15-G		SENSE A MB2B SEG2			70
F		TW SENSE A MB2B SEG2			71
D		SENSE A MB2A SEG1			137
E		TW SENSE A MB2A SEG1			138
A16-D		SENSE A MB3A SEG1			02A3MACP2- 1
E		TW SENSE A MB3A SEG1			2
G		SENSE A MB3B SEG2			68
F		TW SENSE A MB3B SEG2			69
A17-G		SENSE A MB4B SEG2			70
F		TW SENSE A MB4B SEG2			71
D		SENSE A MB4A SEG1			137
E		TW SENSE A MB4A SEG1			138
A18-D		SENSE A MB5A SEG1			02A3MACP3- 1
E		TW SENSE A MB5A SEG1			2
G		SENSE A MB5B SEG2			68
F		TW SENSE A MB5B SEG2			69
A19-G		SENSE A MB6B SEG2			70
F		TW SENSE A MB6B SEG2			71
D		SENSE A MB6A SEG1			137
E		TW SENSE A MB6A SEG1			138
A13-D	05.28.02.1	SENSE A MB7A SEG1			02A3MACP4- 1
E		TW SENSE A MB7A SEG1			2
G		SENSE A MB7B SEG2			68
F		TW SENSE A MB7B SEG2			69
B13-F		SENSE A MB8E SEG2			70
E		TW SENSE A MB8B SEG2			71
D		SENSE A MB8A SEG1			137
C		TW SENSE A MB8A SEG1			138
B14-D		SENSE A MB9A SEG1			02A3MACP5- 1
C		TW SENSE A MB9B SEG1			2
F		SENSE A MB9B SEG2			68
E		TW SENSE A MB9B SEG2			69
B15-F		SENSE A MB10B SEG2			70
E		TW SENSE A MB10B SEG2			71
D		SENSE A MB10A SEG1			137
C		TW SENSE A MB10A SEG1			138
B16-D		SENSE A MB11A SEG1			02A3MACP6- 1
C		TW SENSE A MB11A SEG1			2
F		SENSE A MB11B SEG2			63
E		TW SENSE A MB11B SEG2			69
B17-F		SENSE A MB12B SEG2			70
E		TW SENSE A MB12B SEG2			71
C		SENSE A MB12A SEG1			137
D		TW SENSE A MB12A SEG1			138
B18-D		SENSE A MB13A SEG1			02A3MACP7- 1
C		TW SENSE A MB13A SEG1			2
F		SENSE A MB13B SEG2			68
E		TW SENSE A MB13B SEG2			69
B19-F		SENSE A PARB SEG2			70
E		TW SENSE A PARB SEG2			71
C		SENSE A PARA SEG1			137
D		TW SENSE A PARA SEG1			138

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LN 04.28.01.0

Figure 10-4. Signal Interface List (Sheet 51)

FROM		SIGNAL NAME	TO	
EDGE CONN.	LOGIC SHEET		LOGIC SHEET	PIN
02A00A97-D	05.28.03.1	SENSE B MB1A SEG1	01.01.05.0	02A03MBCP1- 1
E		TW SENSE B MB1A SEG1		2
G		SENSE B MB1B SEG2		68
F		TW SENSE B MB1B SEG2		69
A08-G		SENSE B MB2B SEG2		70
F		TW SENSE B MB2B SEG2		71
D		SENSE B MB2A SEG1		137
E		TW SENSE B MB2A SEG1		138
A09-D		SENSE B MB3A SEG1		02A03MBCP2- 1
E		TW SENSE B MB3A SEG1		2
G		SENSE B MB3B SEG2		68
F		TW SENSE B MB3B SEG2		69
A10-G		SENSE B MB4B SEG2		70
F		TW SENSE B MB4B SEG2		71
D		SENSE B MB4A SEG1		137
E		TW SENSE B MB4A SEG1		138
A11-D		SENSE B MB5A SEG1		02A03MBCP3- 1
E		TW SENSE B MB5A SEG1		2
G		SENSE B MB5B SFG2		68
F		TW SENSE B MB5B SEG2		69
A12-G		SENSE B MB6B SEG2		70
F		TW SENSE B MB6B SEG2		71
D		SENSE B MB6A SEG1		137
E		TW SENSE B MB6A SEG1		138
A06-D	05.28.04.1	SENSE B MB7A SEG1		02A3MBCP4- 1
E		TW SENSE B MB7A SEG1		2
G		SENSE B MB7B SEG2		68
F		TW SENSE B MB7B SEG2		69
B06-F		SENSE B MB8B SEG2		70
E		TW SENSE B MB8B SEG2		71
D		SENSE B MB8A SEG1		137
C		TW SENSE B MB8A SEG1		138
B07-D		SENSE B MB9A SEG1		02A03MBCP5- 1
C		TW SENSE B MB9A SEG1		2
F		SENSE B MB9B SEG2		68
E		TW SENSE B MB9B SEG2		69
B08-F		SENSE B MB10B SEG2		70
F		TW SENSE B MB10B SEG2		71
D		SENSE B MB10A SFG2		137
C		TW SENSE B MB10A SEG2		138
B09-D		SENSE B MB11A SEG2		02A03MBCP6- 1
C		TW SENSE B MB11A SEG2		2
F		SENSE B MB11B SEG2		68
E		TW SENSE B MB11B SEG2		69
B10-F		SENSE B MB12B SEG2		70
E		TW SENSE B MB12B SEG2		71
D		SENSE B MB12A SEG1		137
C		TW SENSE B MB12A SEG1		138
B11-D		SENSE B MB13A SEG1		02A03MBCP7- 1
C		TW SENSE B MB13A SEG1		2
F		SENSE B MB13B SEG2		68
E		TW SENSE B MB13B SEG2		69
B12-F		SENSE B PAR B SEG2		70
E		TW SENSE B PAR B SEG2		71
D		SENSE B PAR A SEG1		137
C		TW SENSE B PAR A SEG1		138

LN 04.28.02.0

6900505-REL (66118KR)

Figure 10-4. Signal Interface List (Sheet 52)

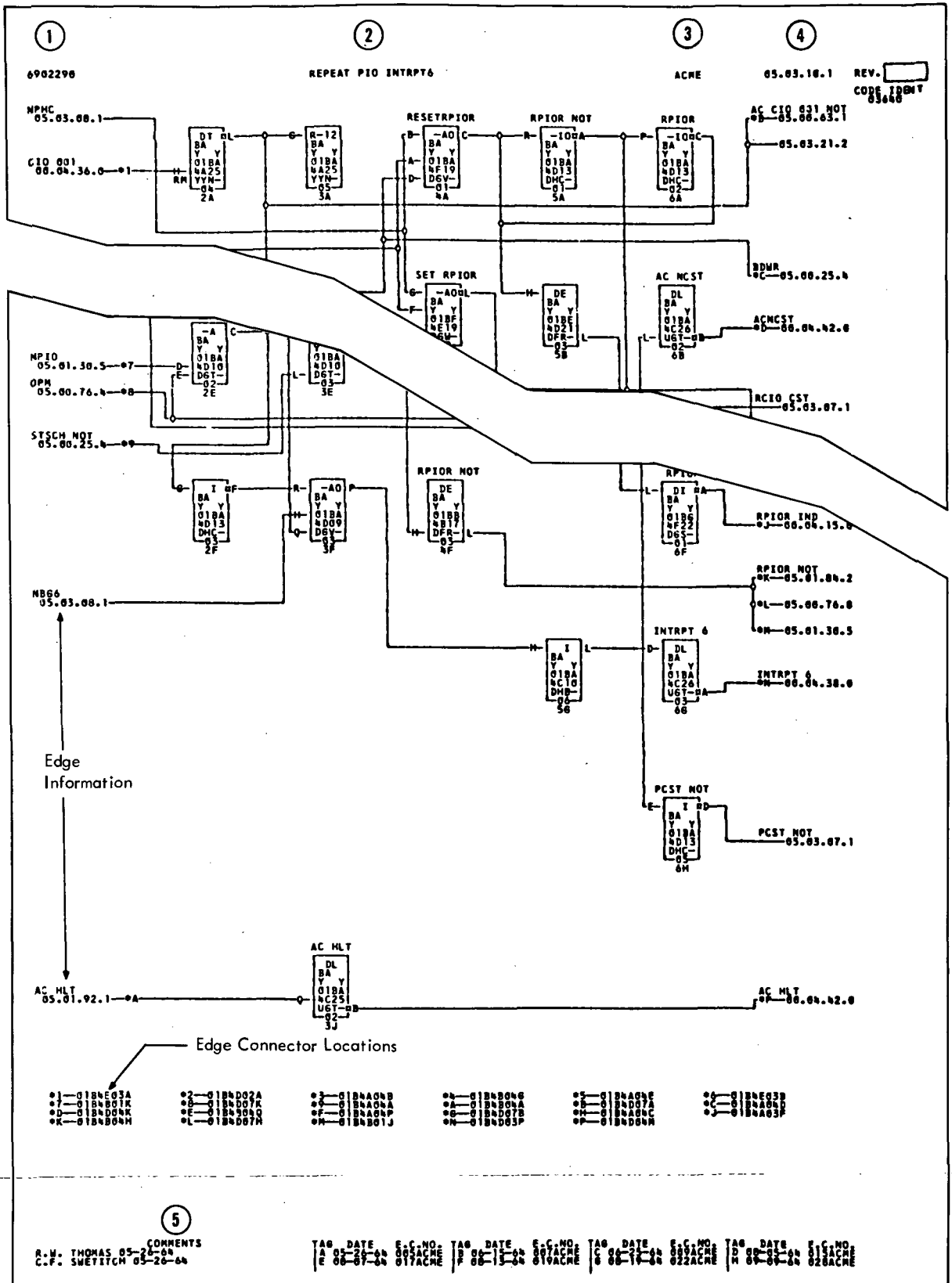
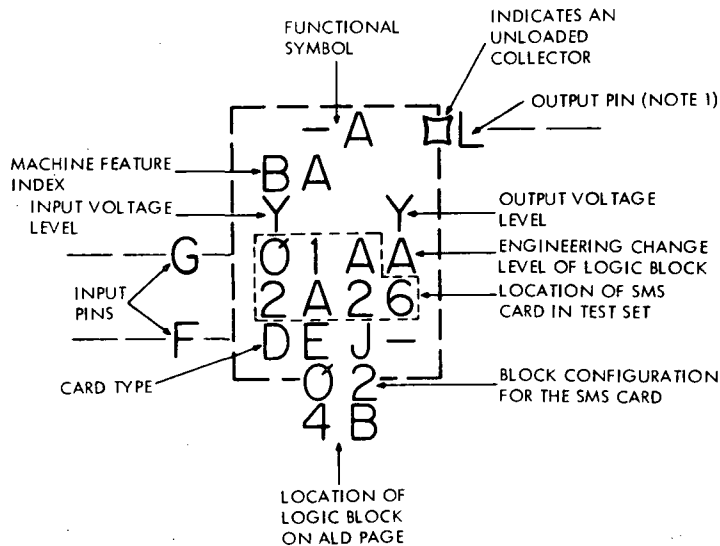


Figure 10-5. Typical Logic Page

10-21. **LOGIC BLOCKS.** The logic blocks represent the SMS card circuits. A basic logic function is usually represented by a single block, but some functions may require more than one block. In the case of multiple circuits on one SMS card, each circuit is represented by a separate logic block. The standard format of the logic block is shown on figure 10-6; salient features are as follows:

- a. **Timing.** The timings of special circuits, such as single shots, oscillators, and delays, are printed above the logic blocks.
- b. **Functional Symbol.** This symbol consists of a sign (when used) and letter(s) that indicate the type of circuit.
- c. **Machine Feature Index.** This code indicates the configuration of the equipment. BA indicates the basic configuration.
- d. **Voltage Levels.** These two code letters indicate the nominal levels of input and output voltage. The Y symbol indicates "0" = 0 vdc and "1" = -6 vdc.
- e. **Card Location.** The location of an SMS card in the gate assemblies is indicated by a seven-character code; for example, 02B3F22 indicates that a card is located in frame 02, gate assembly B3, column F, position 22.
- f. **Card Type.** The type of SMS card is indicated by a four character alphanumeric code.
- g. **Block Configuration Code.** Most SMS cards contain more than one circuit. The circuit used for a particular logic function is indicated by the two-digit block configuration code.



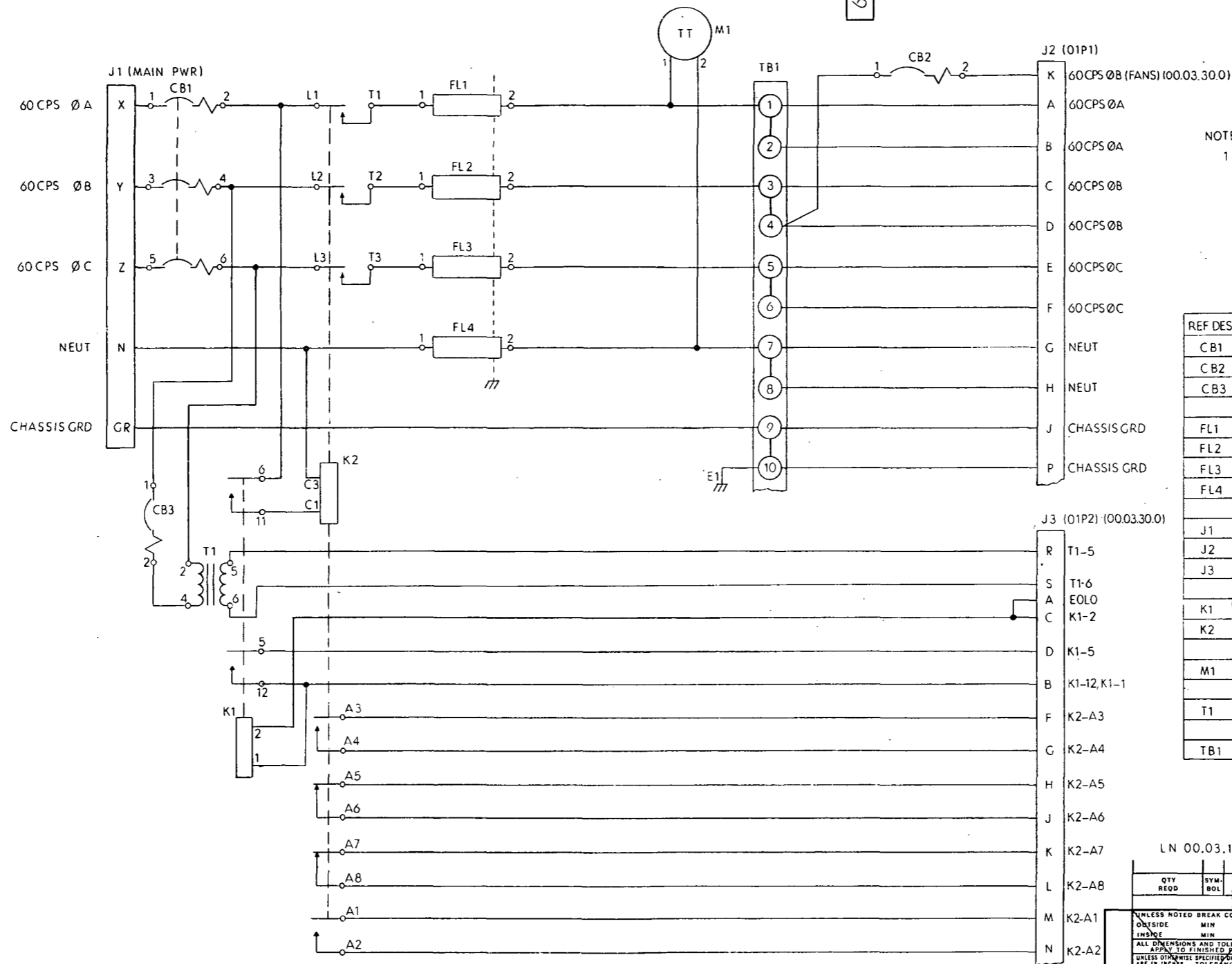
NOTES:

1. IF THE OUTPUT PIN IS SHOWN IN THE TOP HALF OF THE LOGIC BLOCK, THE OUTPUT IS OUT OF PHASE WITH THE INPUT(S). IF THE OUTPUT PIN IS SHOWN IN THE BOTTOM HALF OF THE LOGIC BLOCK, THE OUTPUT IS IN PHASE WITH THE INPUT(S).
2. ADJACENT PIN LETTERS (ON EITHER SIDE OF THE BLOCK) INDICATE THAT THESE PINS ARE JUMPED TOGETHER.

Figure 10-6. Typical Logic Block

6900544

REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	66118-CK	RELEASE	R/1.9.4	
A	66118-DK	SEE ENGRG NOTICE	4/27/64	H.P.
B	66118-GH	SEE ENGRG NOTICE	R/230.64	
C	66118-KZ	SEE ENGRG NOTICE	R/28.64	



NOTES
1 REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATION WITH 01B5

REF DES	PART NUMBER	DESCRIPTION	VALUE	TOL ± %	RATING
CB1	6080248	CIRCUIT BREAKER, 3PH	115VAC		20 A
CB2	6078936		.1PH		2.5A
CB3	6080356		.1PH		0.5A
FL1	6076162	FILTER			
FL2					
FL3					
FL4					
J1	6072145	CONNECTOR (HUBBELL)			
J2	MS3100A28-205				
J3	MS3100A28-165				
K1	608C429	RELAY			
K2	6080355	CONTACTOR			
M1	6018105	INDICATOR, ELAPSE TIME			
T1	6077905	TRANSFORMER			
TB1	6078992	TERMINAL STRIP			

REFERENCE DRAWING

LN 00.03.10.0

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 580 MADISON AVE. NEW YORK 22, N. Y.							
TITLE EL SCHEMATIC FILTER & INTERLOCK BOX (01B5), P.T.C.							
DRAWN GLOTZ			DATE 4/27/64		CODE IDENT NO. 03640		
DESIGN APPROVAL W.S. Kim			DATE 4/28/64		SIZE D 6900544		
SCALE NONE			SHEET				

Figure 10-7. Filter and Interlock Box Assembly (01B5) Electrical Schematic Diagram (LN 00. 03. 10. 0)

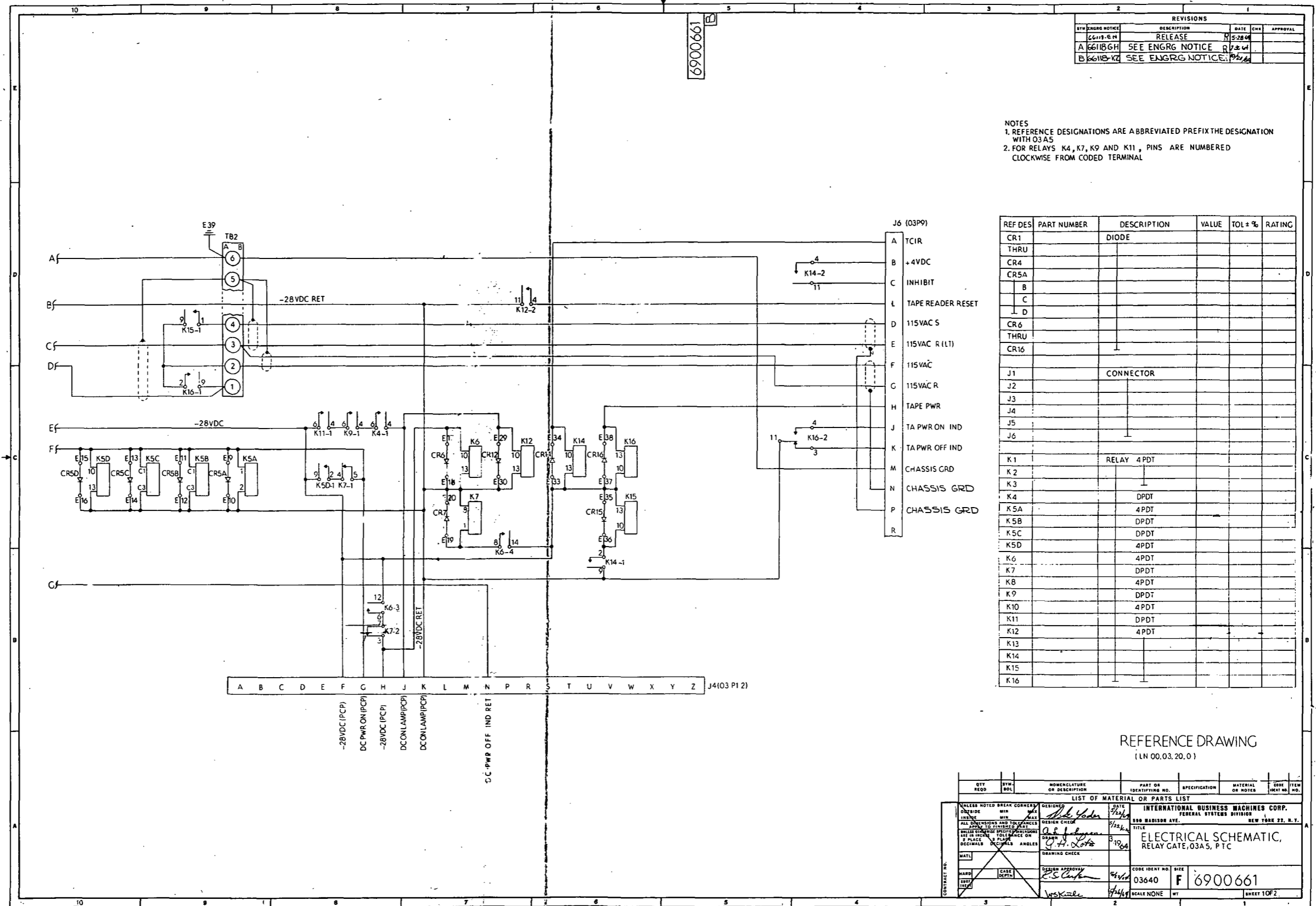


Figure 10-8. Relay Gate Assembly (03A5)
 Electrical Schematic Diagram (LN 00.03.20.0
 and LN 00.03.20.1) (Sheet 1 of 2)

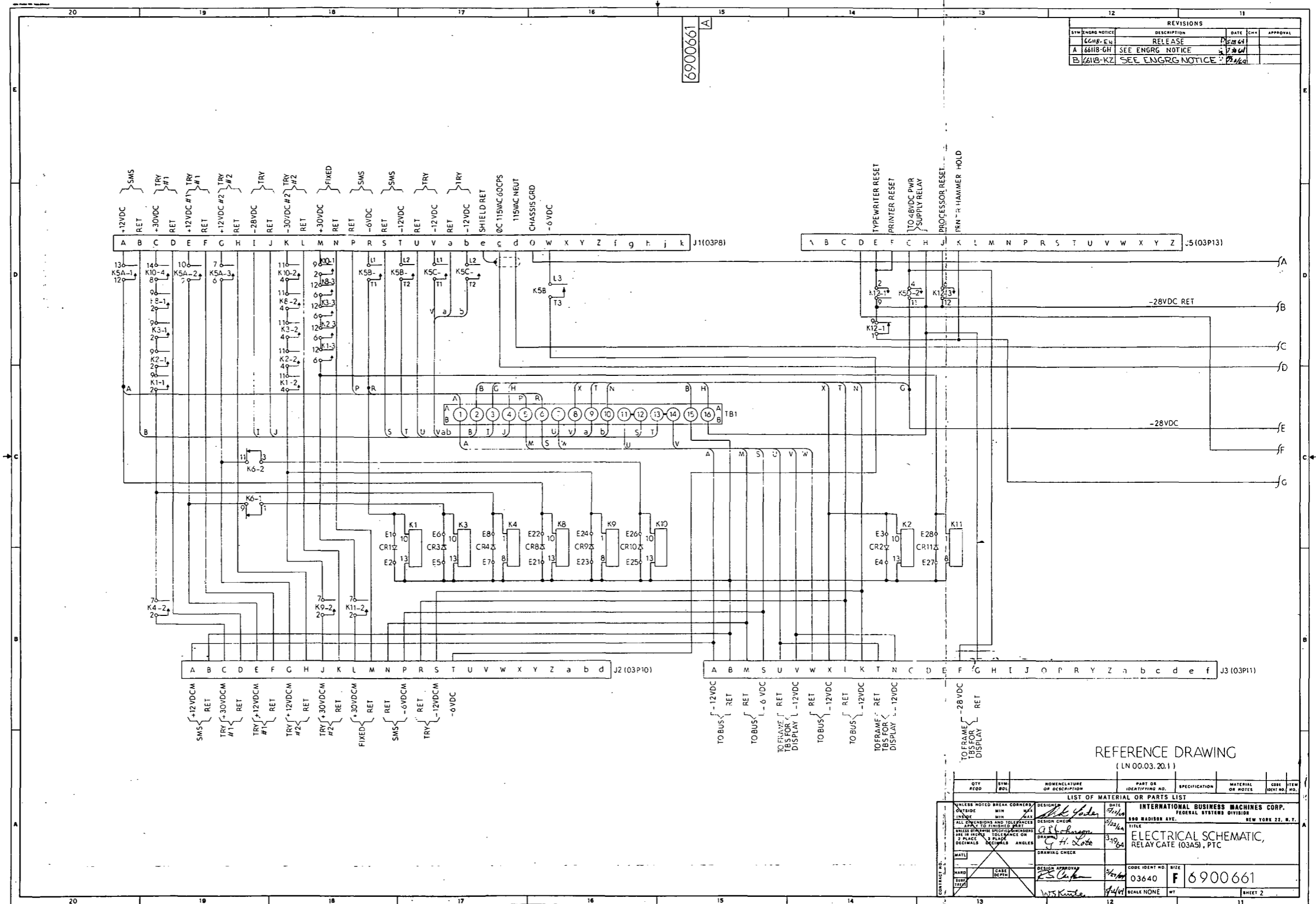


Figure 10-8. Relay Gate Assembly (03A5) Electrical Schematic Diagram (LN 00.03.20.0 and LN 00.03.20.1) (Sheet 2)

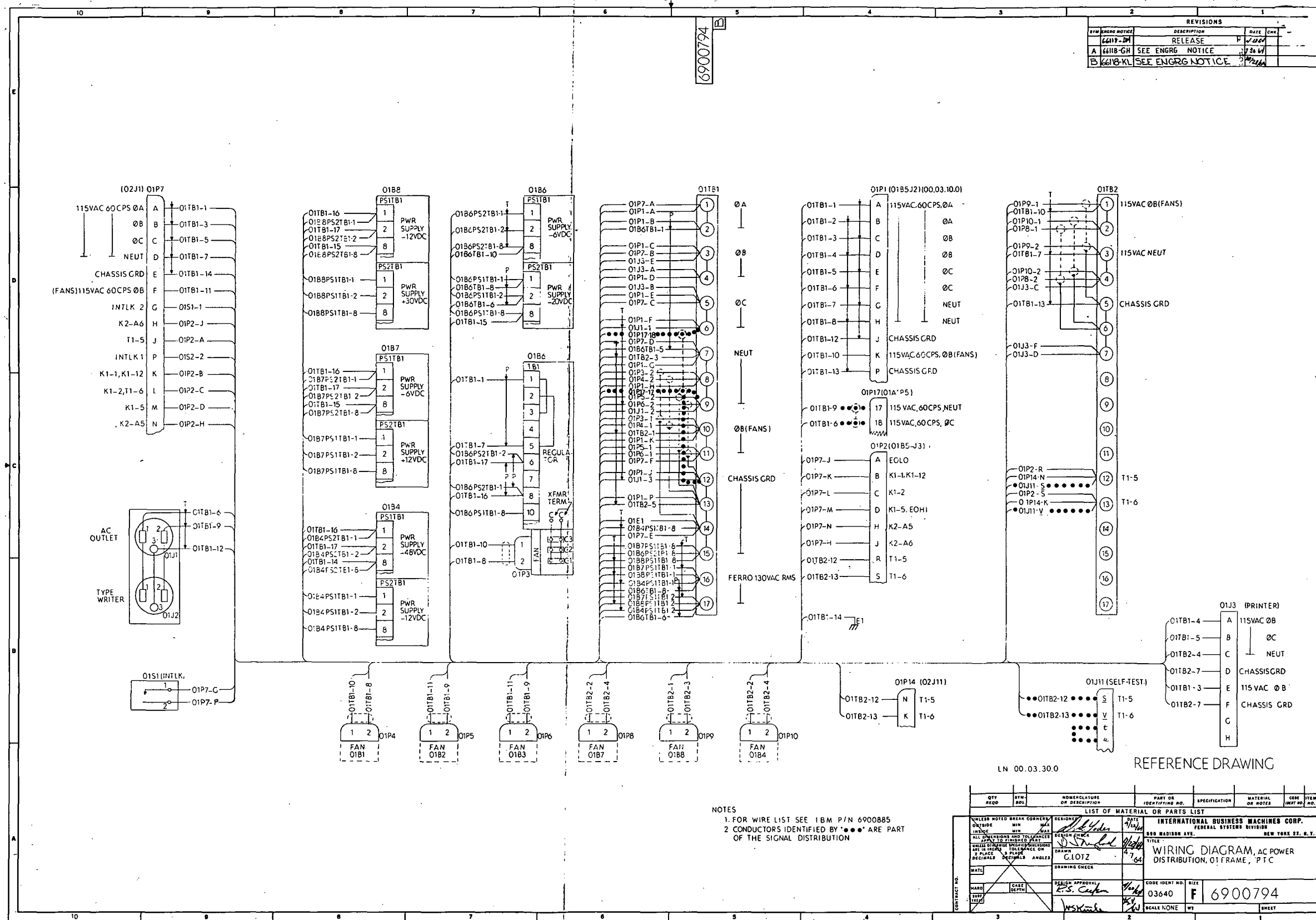


Figure 10-9. AC Power Distribution (01 Frame) Diagram (LN 00. 03. 30. 0)

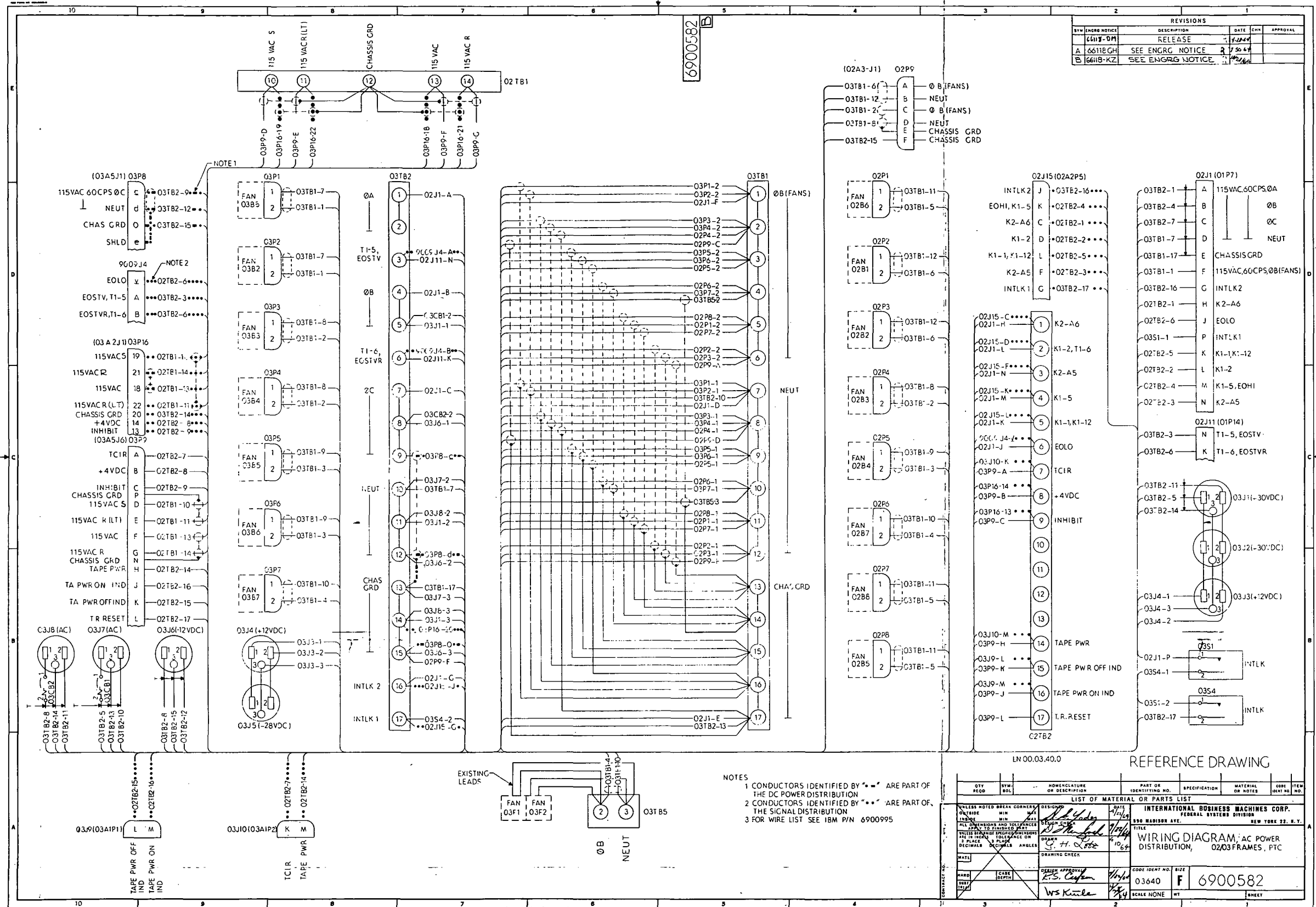
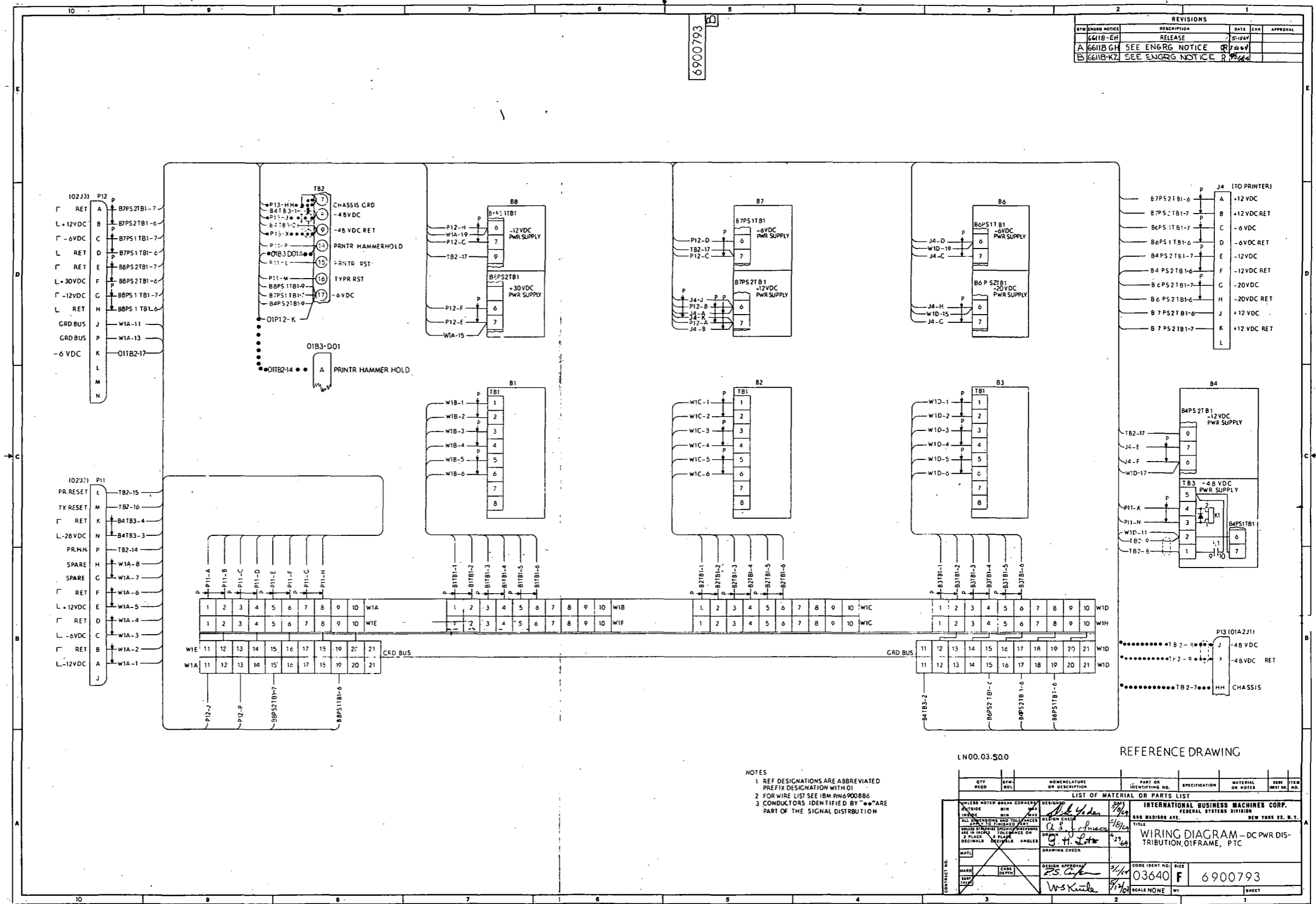


Figure 10-10. AC Power Distribution (02 and 03 Frames) Diagram (LN 00.03.40.0)



6900793

REVISIONS				
BY	ENGRG NOTICE	DESCRIPTION	DATE	CHK
A	6611B-EH	RELEASE	5-1967	
A	6611B-GH	SEE ENGRG NOTICE	8-17-67	
B	6611B-KZ	SEE ENGRG NOTICE	8-17-67	

(02J3) P12

RET	A	B7PS2TB1-7
L +12VDC	B	B7PS1TB1-6
-6VDC	C	B7PS1TB1-7
RET	D	B7PS1TB1-6
RET	E	BBPS2TB1-7
L +30VDC	F	BBPS2TB1-6
-12VDC	G	BBPS1TB1-7
RET	H	BBPS1TB1-6
GRD BUS	J	W1A-11
GRD BUS	P	W1A-13
-6VDC	K	O1TB2-17
	L	
	M	
	N	

(02J3) P11

PR.RESET	L	TB2-15
TY.RESET	M	TB2-16
RET	K	B4TB3-4
L -28VDC	N	B4TB3-3
PR.HH	P	TB2-14
SPARE	H	W1A-8
SPARE	C	W1A-7
RET	F	W1A-6
L +12VDC	E	W1A-5
RET	D	W1A-4
L -6VDC	C	W1A-3
RET	B	W1A-2
L -12VDC	A	W1A-1
	J	

- NOTES
- REF DESIGNATIONS ARE ABBREVIATED PREFIX DESIGNATION WITH 01
 - FOR WIRE LIST SEE IBM PING900886
 - CONDUCTORS IDENTIFIED BY "0" ARE PART OF THE SIGNAL DISTRIBUTION

LN00.03.50.0

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CONTRACT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION NEW YORK 22, N.Y.							
TITLE: WIRING DIAGRAM - DC PWR DISTRIBUTION, O1FRAME, PTC							
DRAWN: G. H. Lutz							
DESIGN APPROVAL: W. S. Kuehl							
CONTRACT NO. 03640							
SHEET 1 OF 1							

Figure 10-11. DC Power Distribution (01 Frame) Diagram (LN 00.03.50.0)

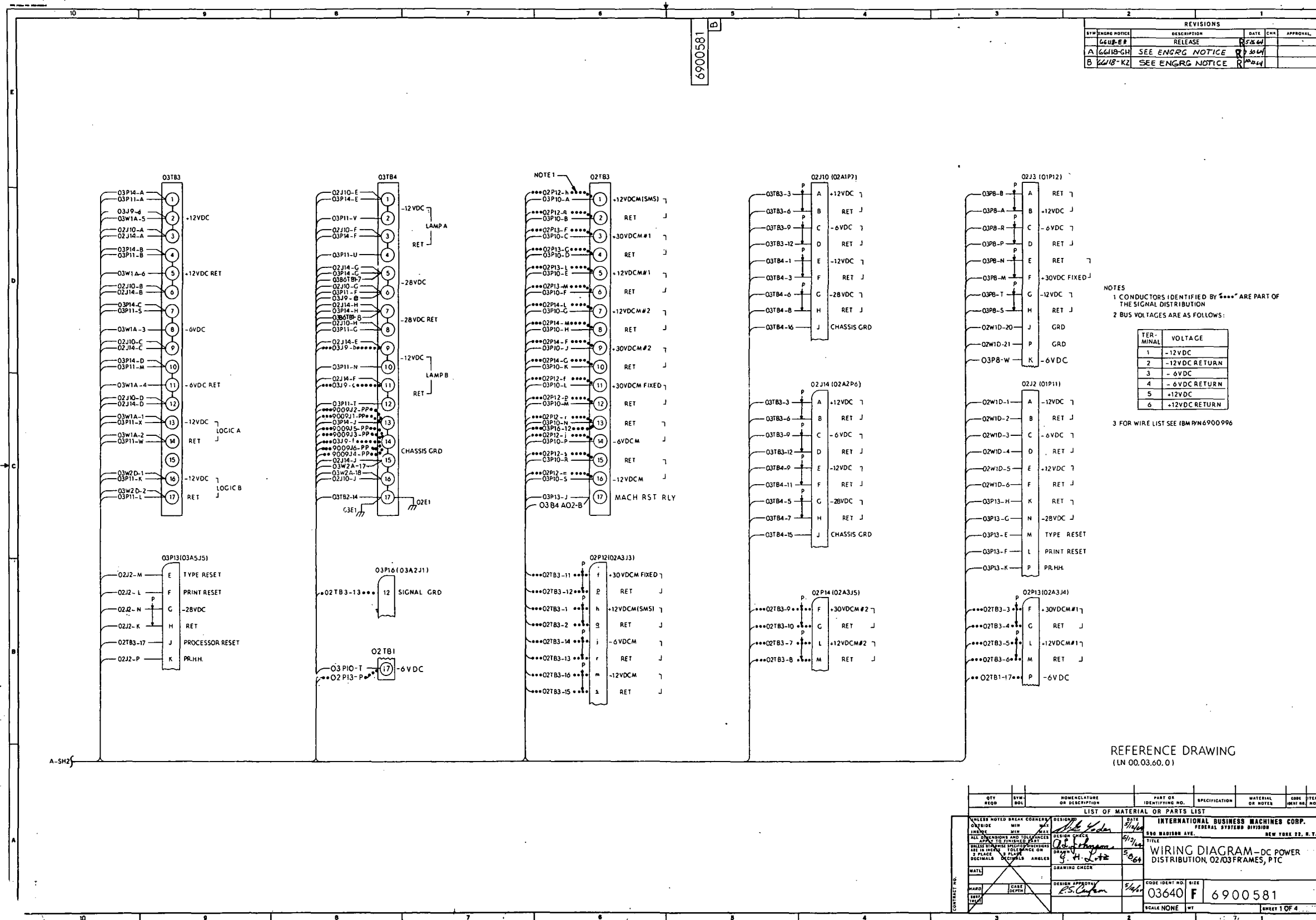
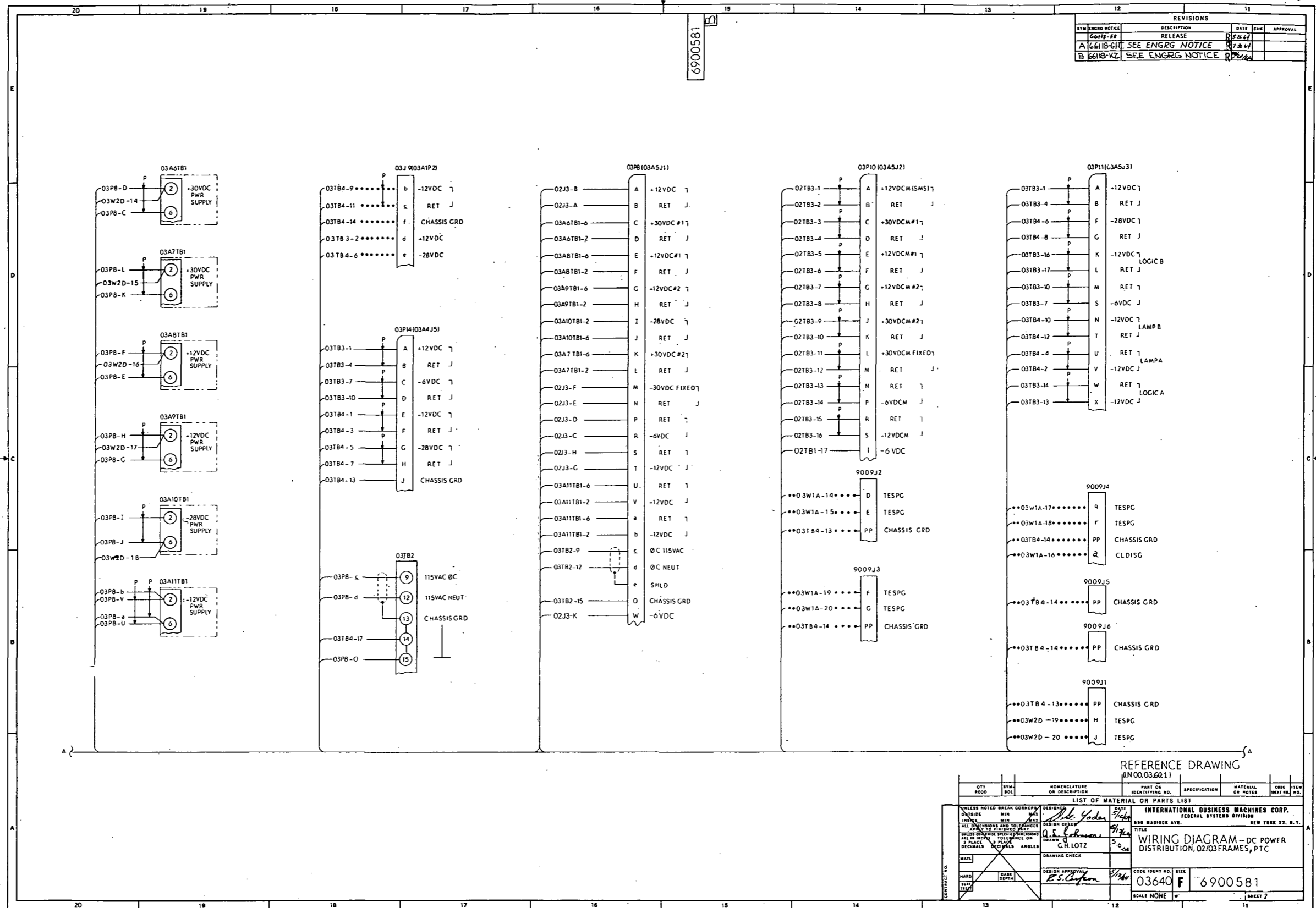


Figure 10-12. DC Power Distribution (O2 and O3 Frames) Diagram (LN 00. 03. 60. 0, LN 00. 03. 60. 1, LN 00. 03. 60. 2 and LN 00. 03. 60. 3) (Sheet 1 of 4)



6900581

REVISIONS			
SYM	ENGRG NOTICE	DESCRIPTION	DATE
	6618-KZ	RELEASE	8/28/67
A	6618-GH	SEE ENGRG NOTICE	7/28/67
B	6618-KZ	SEE ENGRG NOTICE	8/28/67

REFERENCE DRAWING
(LN 00.03.60.1)

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM
		LIST OF MATERIAL OR PARTS LIST					
		UNLESS NOTED BREAK CORNERS TO BE ROUNDED OFF TO MATCH DIMENSIONS AND TOLERANCES ARE IN INCHES TOLERANCE ON 3 PLACES DECIMALS ON OTHERS ANGLES TO BE SHOWN					
		DESIGNER: <i>D. Yoda</i> DATE: <i>7/4/67</i>					
		DRAWN: <i>G.H. Lotz</i> DATE: <i>5/5/64</i>					
		DRAWING CHECK: _____					
		DESIGN APPROVAL: <i>B.S. Clifton</i> DATE: <i>1/1/68</i>					
		CODE IDENT NO: 03640 SIZE: F					
		SCALE: NONE					

Figure 10-12. DC Power Distribution (02 and 03 Frames) Diagram (LN 00.03.60.0, LN 00.03.60.1, LN 00.03.60.2 and LN 00.03.60.3) (Sheet 2)
V-10-72.

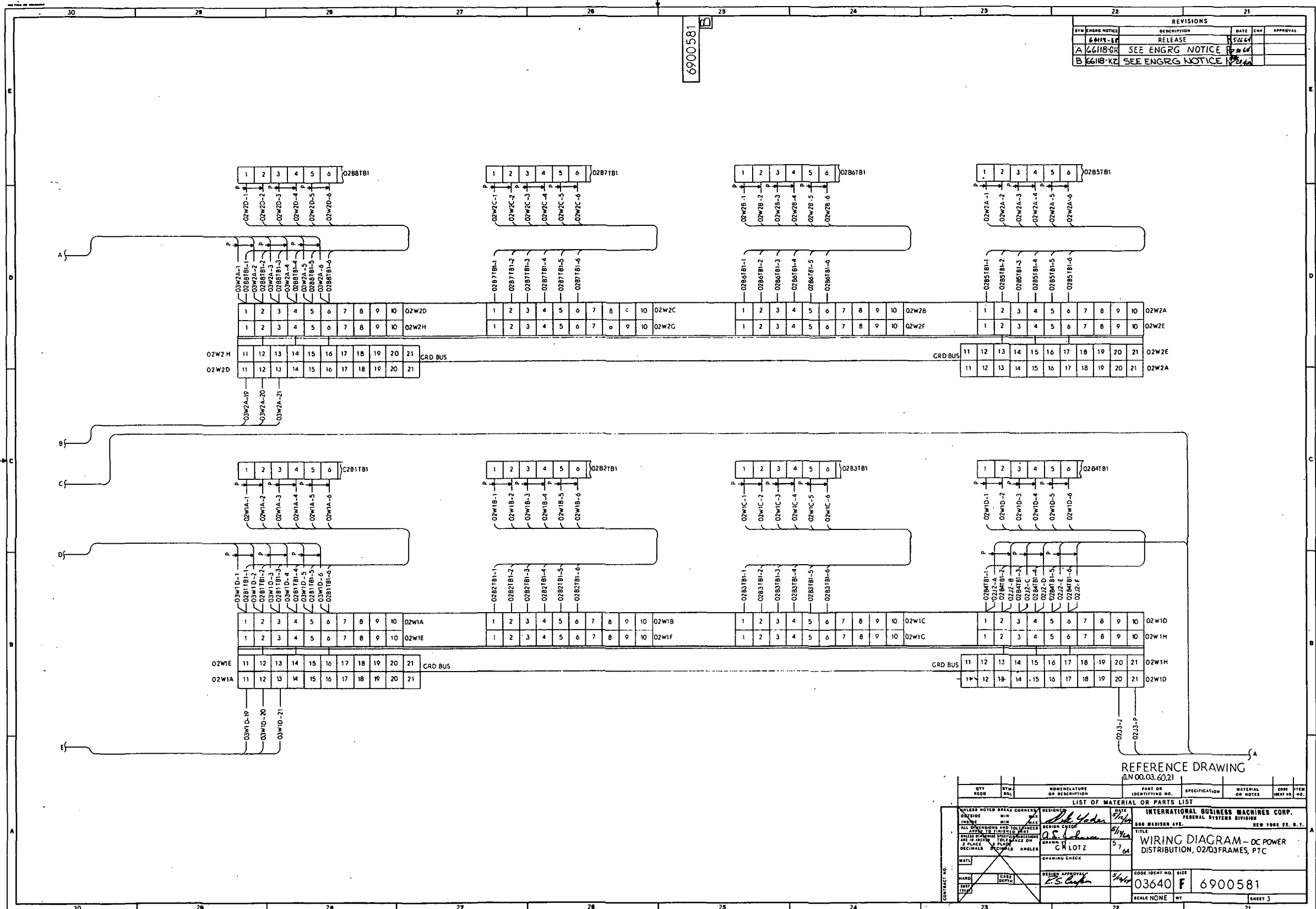
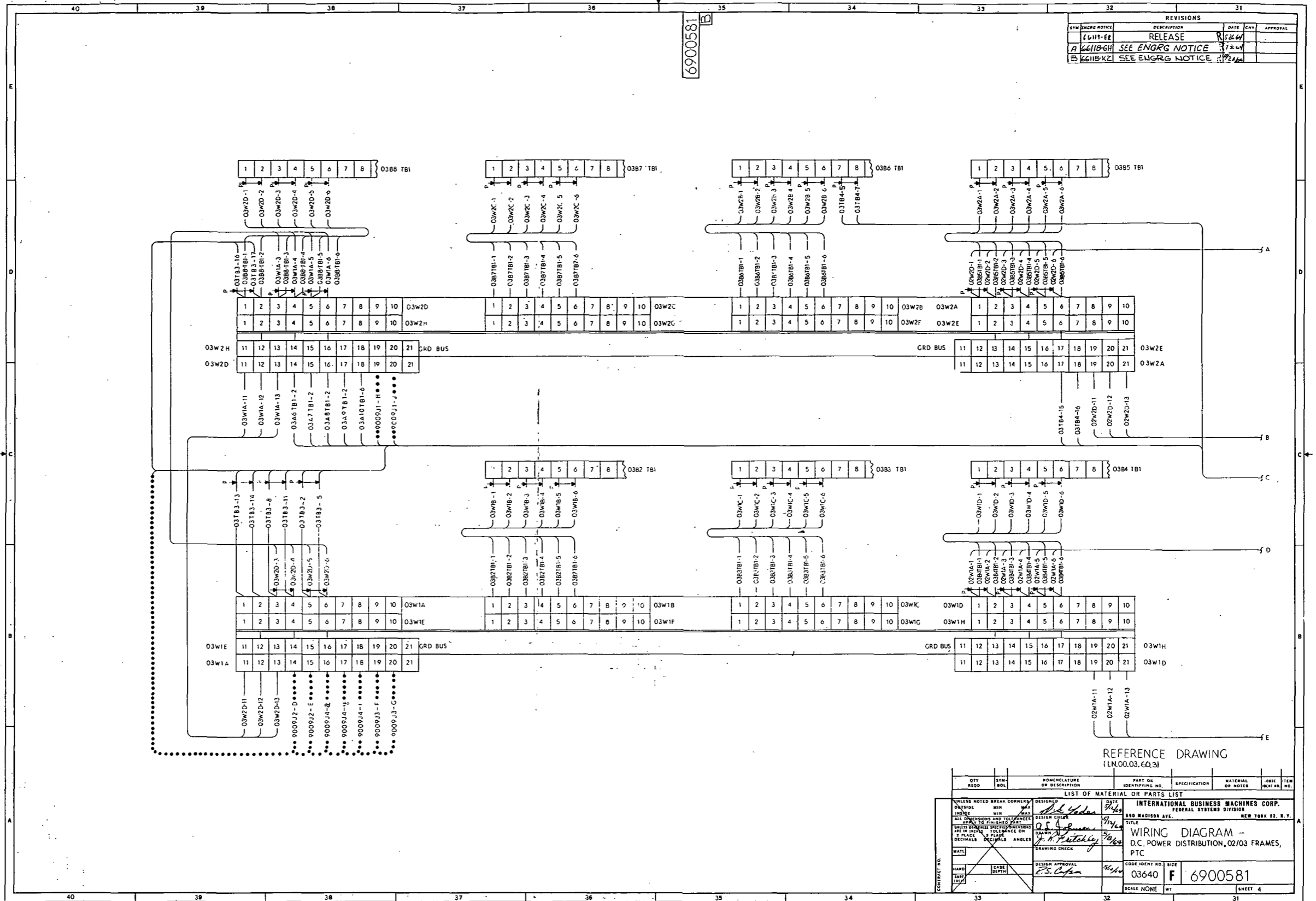


Figure 10-12. DC Power Distribution (O2 and O3 Frames) Diagram (LN 00. 03. 60. 0, LN 00. 03. 60. 1, LN 00. 03. 60. 2 and LN 00. 03. 60. 3) (Sheet 3)



6900581

REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
		RELEASE	1/26/64	
A	6611B-GH	SEE ENGRG NOTICE	1/26/64	
B	6611B-KZ	SEE ENGRG NOTICE	1/26/64	

REFERENCE DRAWING
(LN00.03.60.3)

QTY REQD	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM IDENT NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS: DESIGNER: <i>Ed. Cohen</i> INSIDE MIN MAX ALL DIMENSIONS AND TOLERANCES: DESIGN CHECK: <i>W. J. ...</i> SHOWN TO FINEST POINT UNLESS OTHERWISE SPECIFIED: DRAWN BY: <i>H. H. Patchley</i> ALL DIMENSIONS TO UNLESS OTHERWISE SPECIFIED: DECIMALS ANGLES DRAWING CHECK: <i>H. H. Patchley</i> MATERIAL: HARDNESS: DESIGN APPROVAL: <i>E. S. Cohen</i> CODE IDENT NO: F 6900581 SCALE: NONE WT. SHEET 4							

Figure 10-12. DC Power Distribution (02 and 03 Frames) Diagram (LN 00. 03. 60. 0, LN 00. 03. 60. 1, LN 00. 03. 60. 2 and LN 00. 03. 60. 3) (Sheet 4)

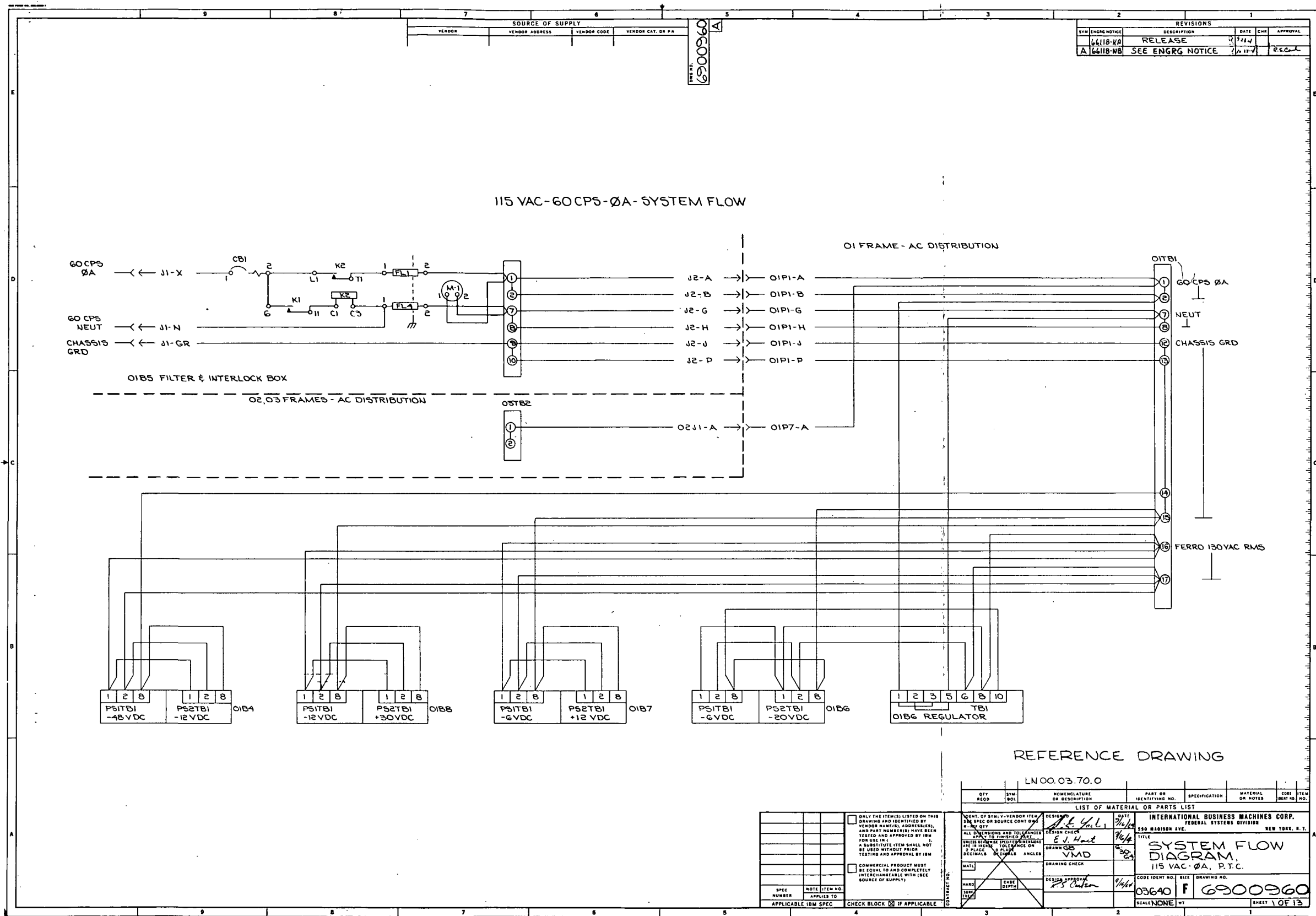


Figure 10-13. 115 VAC System Flow Diagram (LN 00. 03. 70. 0, LN 00. 03. 70. 1, LN 00. 03. 70. 2 and LN 00. 03. 70. 3) (Sheet 1 of 4)

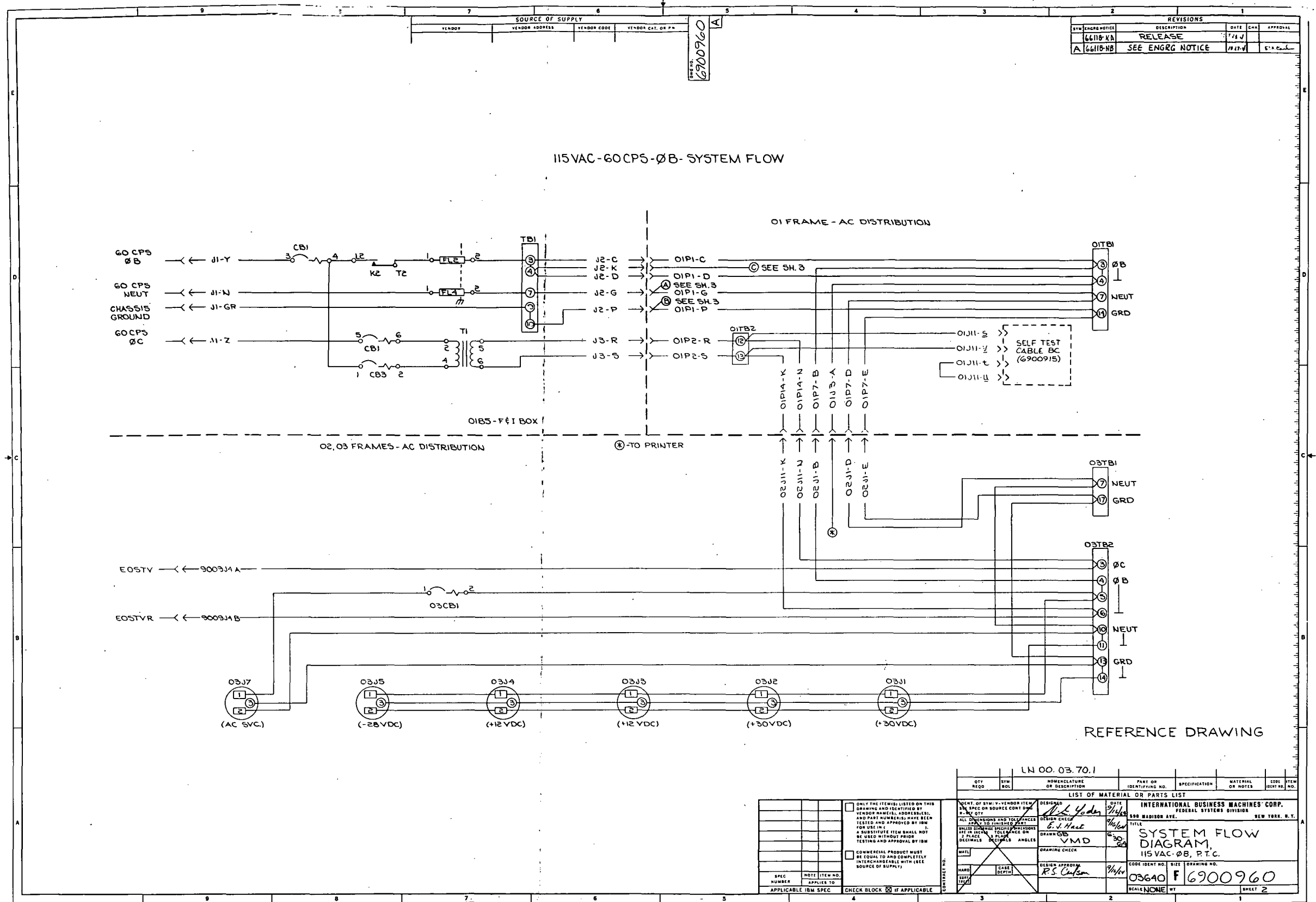


Figure 10-13. 115 VAC System Flow Diagram (LN 00. 03. 70. 0, LN 00. 03. 70. 1, LN 00. 03. 70. 2 and LN 00. 03. 70. 3) (Sheet 2)

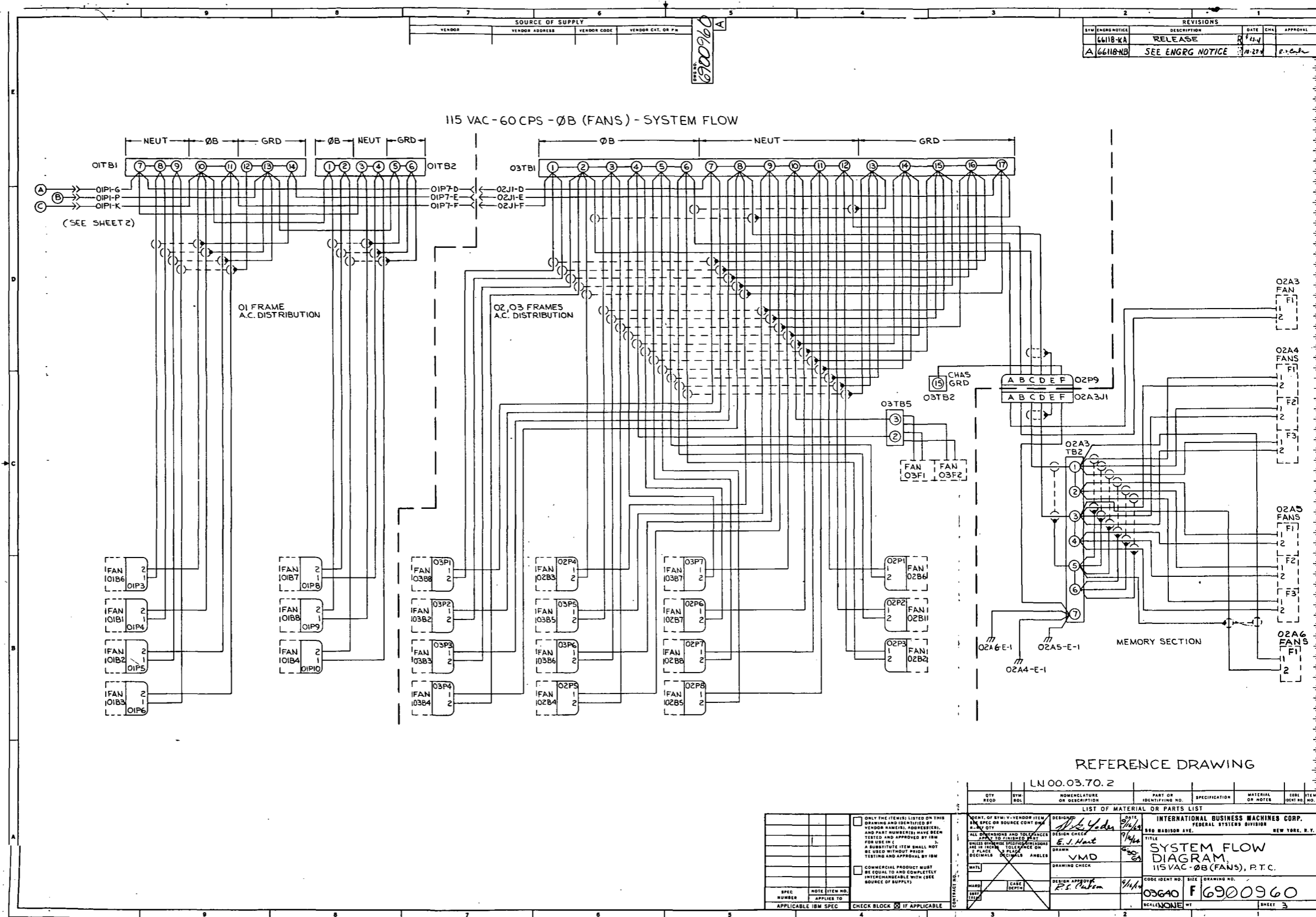


Figure 10-13. 115 VAC System Flow Diagram (LN 00.03.70.0, LN 00.03.70.1, LN 00.03.70.2 and LN 00.03.70.3) (Sheet 3)

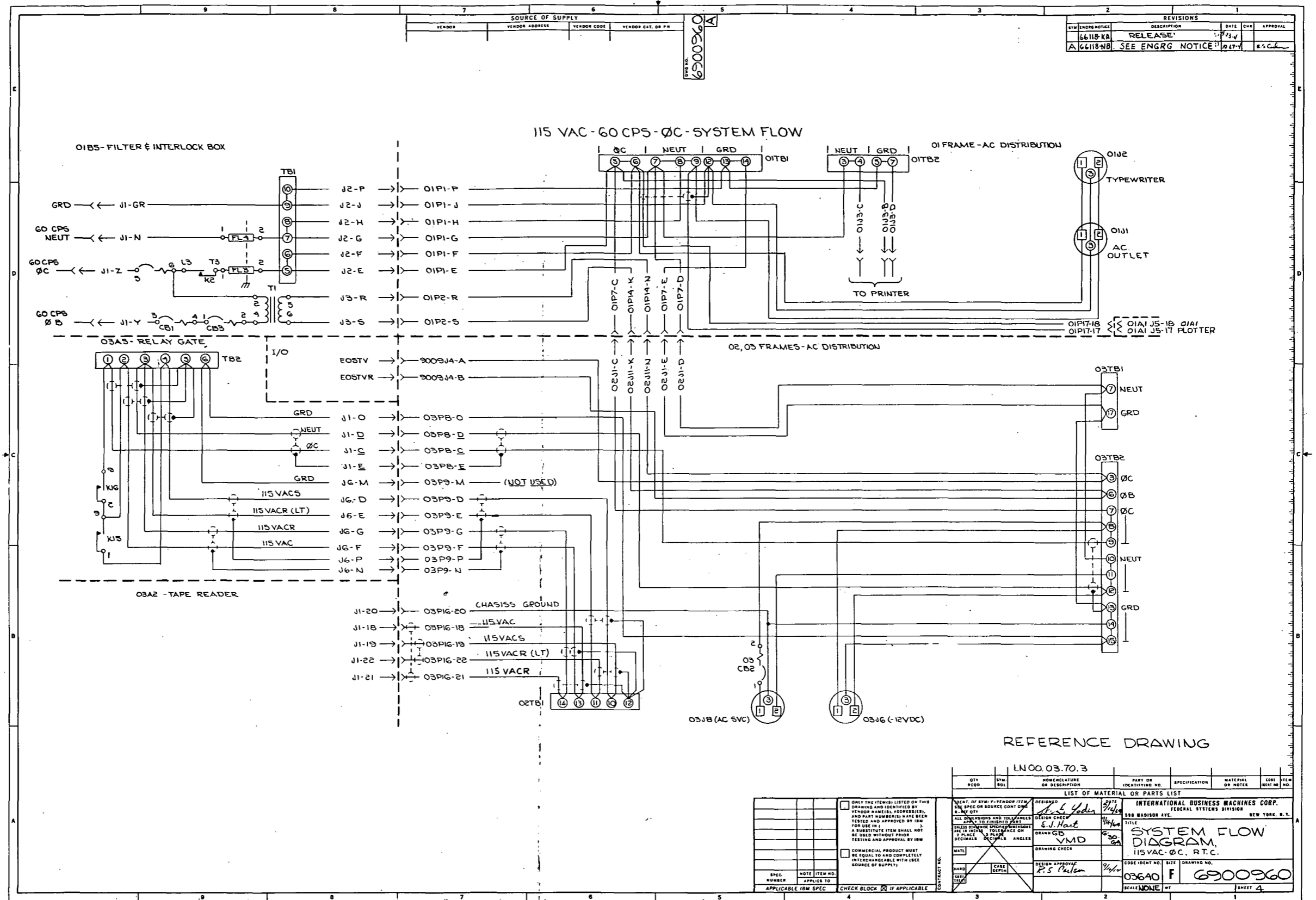
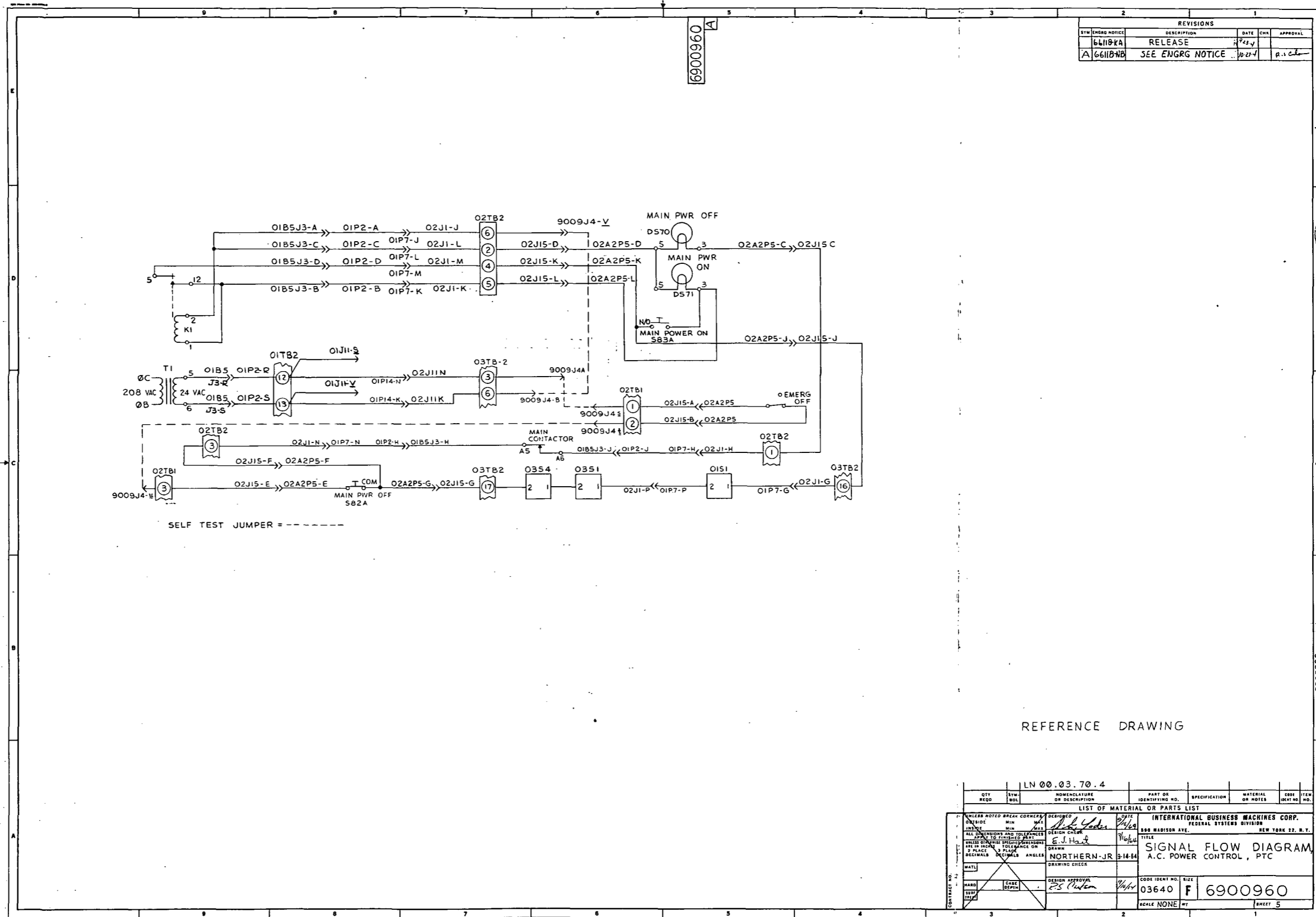


Figure 10-13. 115 VAC System Flow Diagram (LN 00. 03. 70. 0, LN 00. 03. 70. 1, LN 00. 03. 70. 2 and LN 00. 03. 70. 3) (Sheet 4)

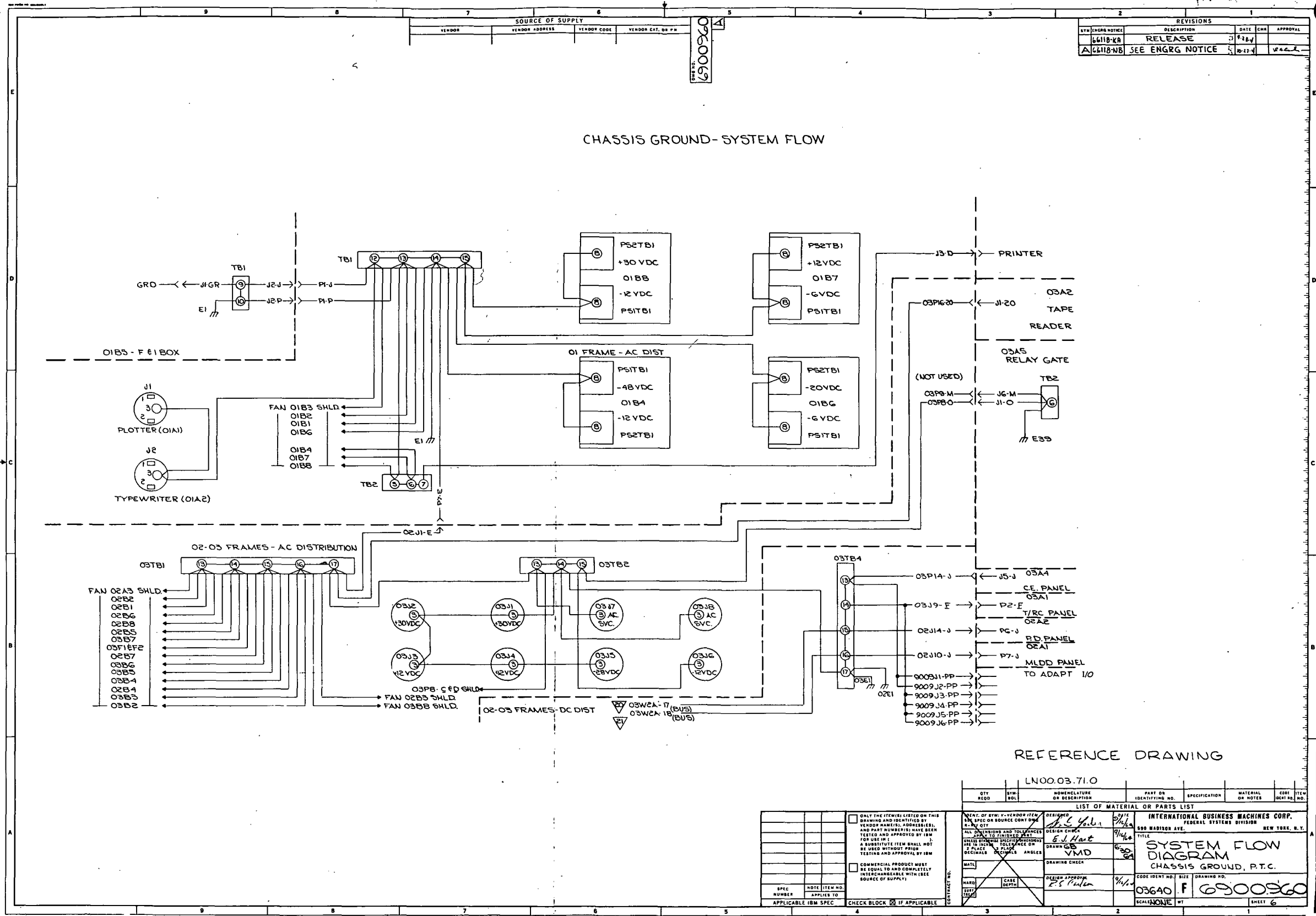


REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	6418KA	RELEASE	7-23-64	
A	6618WB	SEE ENGRG NOTICE	10-27-64	P. J. C.

REFERENCE DRAWING

LN 00.03.70.4				
QTY	SYM	NOMENCLATURE	PART OR IDENTIFYING NO.	SPECIFICATION
LIST OF MATERIAL OR PARTS LIST				
UNLESS NOTED BREAK CORNERS		DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP.
DRAWING		MIN	MAX	FEDERAL SYSTEMS DIVISION
ALL DIMENSIONS AND TOLERANCES		DESIGN CHECK		880 MADISON AVE.
GOVERN TO THIS DRAWING				NEW YORK 22, N.Y.
UNLESS OTHERWISE SPECIFIED DIMENSIONS		DRWING		TITLE
IN PLACE TELEPHONE OR				SIGNAL FLOW DIAGRAM
30 PLACE TELEPHONE OR				A.C. POWER CONTROL, PTC
DIMENSIONS				
DRAWING CHECK				
MATERIAL				
HARD COPY		DESIGN APPROVAL	DATE	CODE IDENT NO. SIZE
DEPTH				03640 F 6900960
				SCALE NONE
				SHEET 5

Figure 10-14. AC Power Control Signal Flow Diagram (LN 00.03.70.4)



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
66118-KR		RELEASE	12-24-64	
A66118-NB		SEE ENGRG NOTICE	10-27-64	

REFERENCE DRAWING

LN00.03.71.0

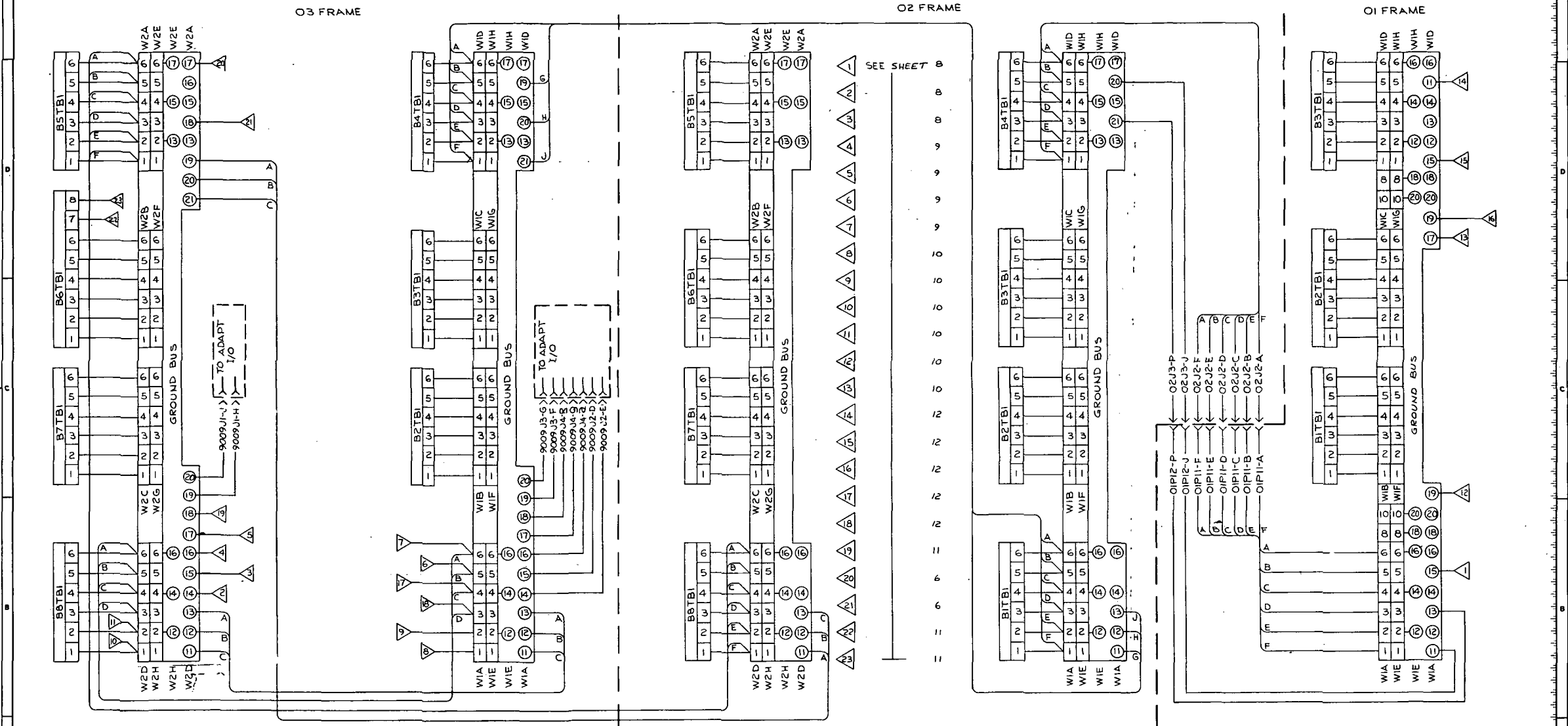
QTY	SYM	HOMECENTRE	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM IDENT NO.
LIST OF MATERIAL OR PARTS LIST							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION NEW YORK, N.Y.							
TITLE: SYSTEM FLOW DIAGRAM CHASSIS GROUND, P.T.C.							
CODE IDENT NO.: 03640 F DRAWING NO.: 6900960							
SCALE: NONE							

Figure 10-15. Chassis Ground System Flow Diagram (LN 00.03.71.0)

SOURCE OF SUPPLY			
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.
			6900960

REVISIONS				
BY	ENGR NOTICE	DESCRIPTION	DATE	APPROVAL
66118-KA		RELEASE	11/23/64	
A 66118-WB		SEE ENGR NOTICE	11/23/64	E.S.C.

BUS BAR SYSTEM - (D.C. DISTRIBUTION - SIGNAL GROUND - CHASSIS GROUND)



REFERENCE DRAWING

LN 00.03.72.0

QTY REQD	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM
		LIST OF MATERIAL OR PARTS LIST					
		INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 800 MARSHALL AVE. NEW YORK, N.Y.					
		DESIGNED BY: <i>John Yoder</i> DATE: <i>11/23/64</i>					
		DRAWN BY: <i>G.J. Hoad</i> DATE: <i>11/23/64</i>					
		CHECKED BY: <i>WMD</i> DATE: <i>11/23/64</i>					
		DESIGN APPROVAL BY: <i>R.S. Carter</i> DATE: <i>11/23/64</i>					
		CODE IDENT. NO. SIZE DRAWING NO. 03640 F 6900960					
		SCALE: NONE					

Figure 10-16. Bus Bar System Flow Diagram (LN 00.03.72.0)

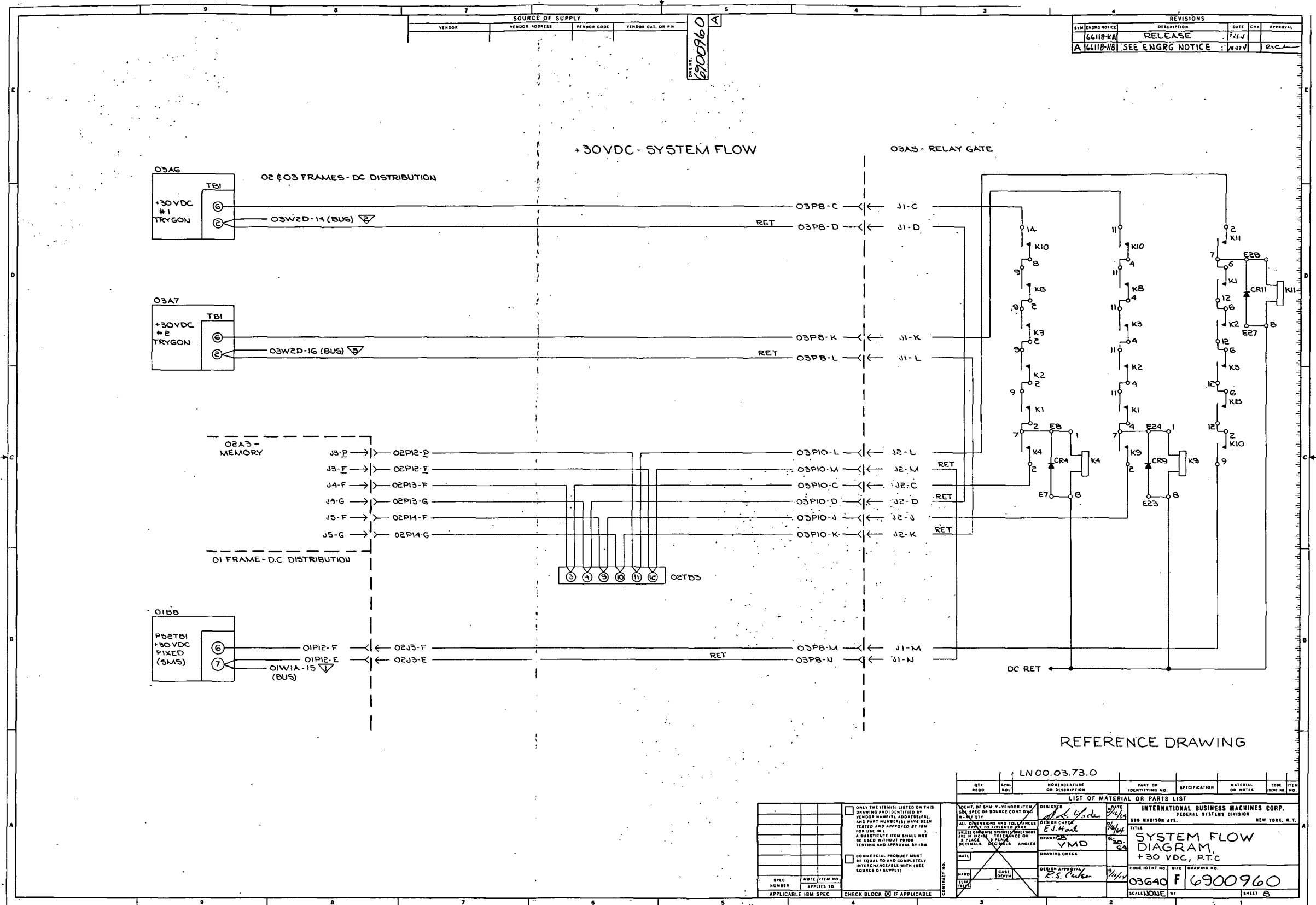


Figure 10-17. +30 VDC System Flow Diagram (LN 00. 03. 73. 0)

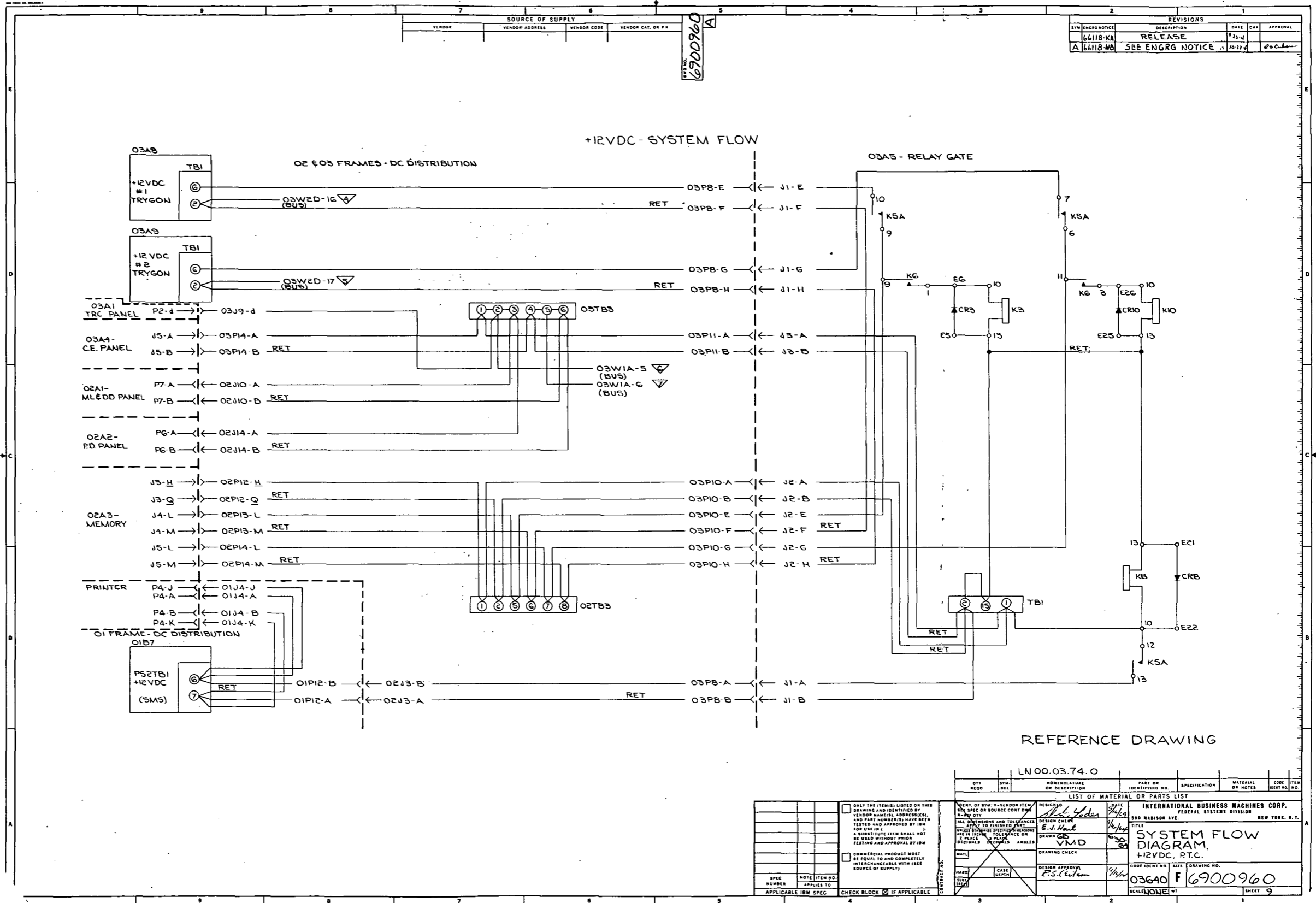


Figure 10-18. +12 VDC System Flow Diagram (LN 00. 03. 74. 0)

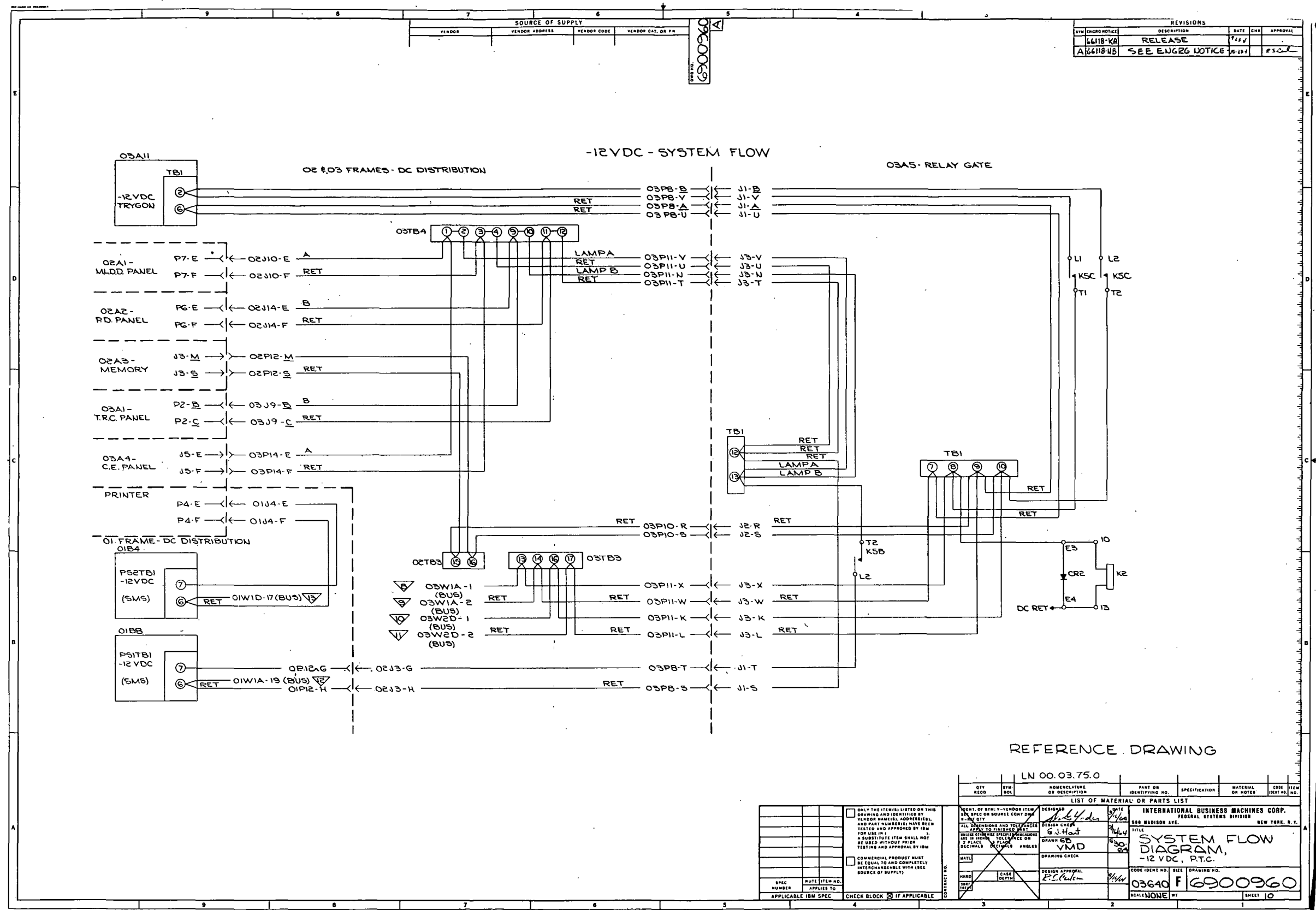


Figure 10-19. -12 VDC System Flow Diagram (LN 00.03.75.0)

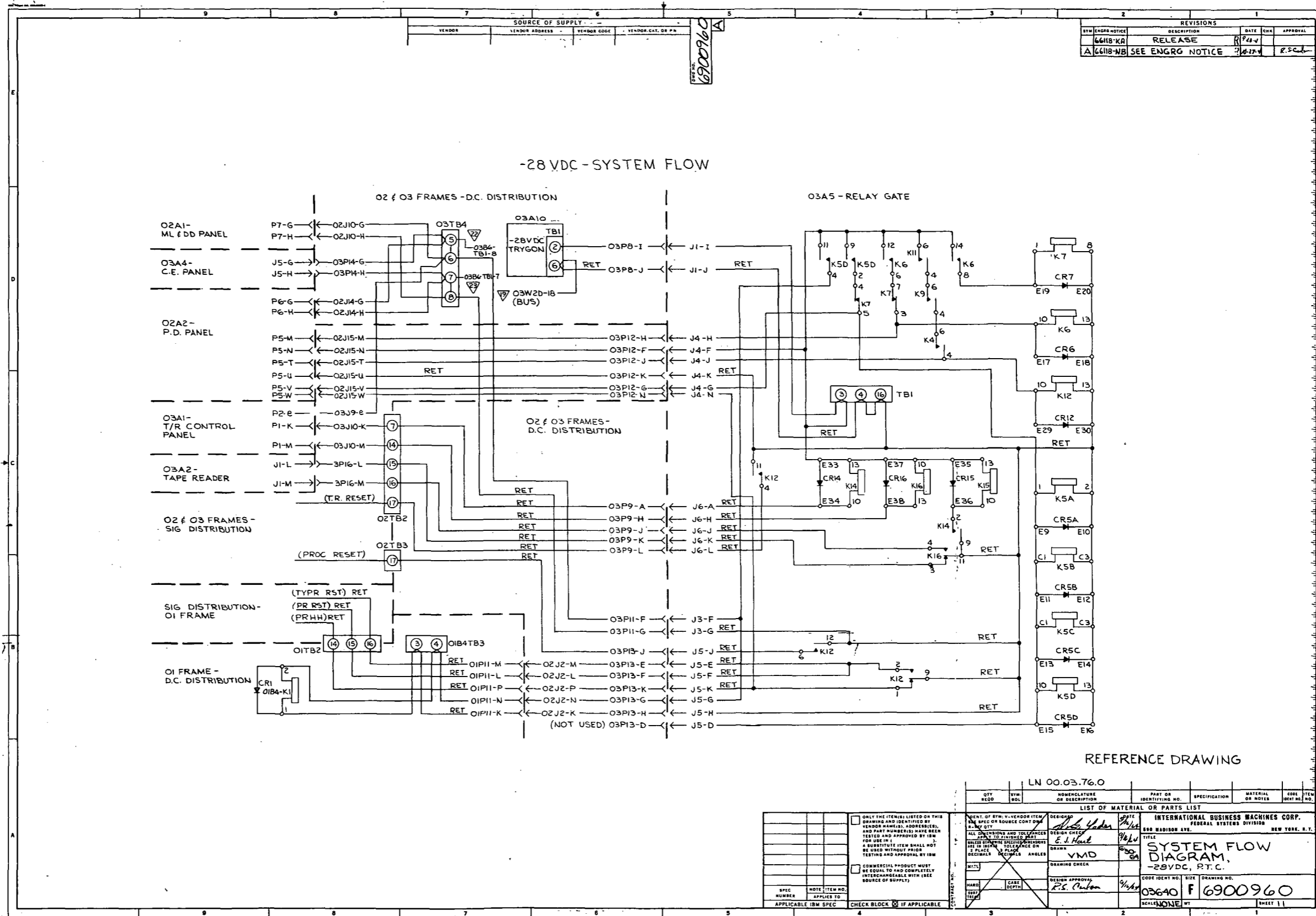


Figure 10-20. -28 VDC System Flow Diagram (LN 00.03.76.0)

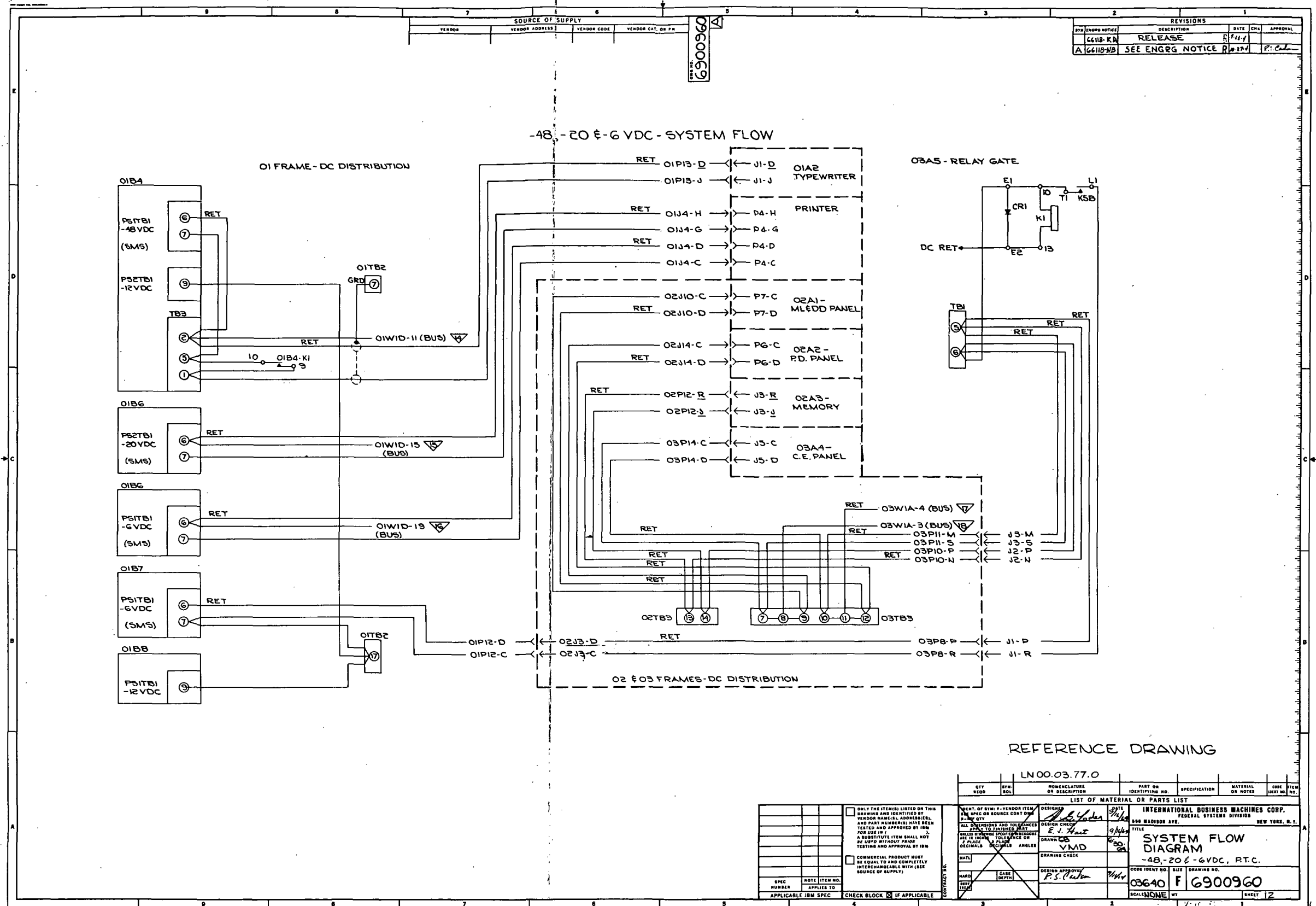


Figure 10-21. -48, -20, and -6 VDC System Flow Diagram (LN 00. 03. 77. 0)

6900960
A

REVISIONS				
REV	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
66118-K8		RELEASE	9-23-54	
A 66118-W8		SEE ENGRG NOTICE	10-27-54	

RELAY	IBM NO.	MANUFACT. NO.	CONTACTS	LOCATION		
				LOGIC NUMBER	ZONE	DRAWING
03A5K1	6080407	MHUO-12D 6VDC ALLIED CONTROL	COIL 10-13	00.03.77.0	3D	6900960-12
			2-9	00.03.73.0	3D	-8
			4-11	00.03.73.0	2D	-8
03A5K2	6080408	MHUO-12D 12 VDC ALLIED CONTROL	COIL 10-13	00.03.75.0	2B	-10
			2-9	00.03.73.0	3D	-8
			4-11	00.03.73.0	2D	-8
03A5K3	6080408	MHUO-12D 12 VDC ALLIED CONTROL	COIL 10-13	00.03.74.0	3D	6900960-9
			2-9	00.03.73.0	3D	-8
			4-11	00.03.73.0	2D	-8
03A5K4	6080405	MTRH-4-26.5 C3 ALLIED CONTROL	COIL 1-8	00.03.73.0	2C	6900960-8
			2-7	00.03.73.0	3C	-8
			4-6	00.03.76.0	3D	-11
03A5K5A	6080409	MHYO-12D 26.5 VDC ALLIED CONTROL	COIL 1-2	00.03.76.0	2C	6900960-1
			9-10	00.03.74.0	4D	-9
			6-7	00.03.74.0	2D	-9
03A5K5B	6080410	CAT B230C ROWAN CONTROL	C1-C3	00.03.76.0	2C	6900960-11
			T2-L2	00.03.75.0	4B	-10
			T1-L1	00.03.77.0	2D	-12
03A5K5C	6080420	CAT B220C ROWAN CONTROL	COIL C1-C3	00.03.76.0	2B	-11
			T1-L1	00.03.75.0	2D	-10
			T2-L2	00.03.75.0	2D	-10
03A5K5D	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	COIL 10-13	00.03.76.0	2B	-11
			2-9	00.03.76.0	4D	-11
			4-11	00.03.76.0	4D	-11
03A5K6	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	COIL 10-13	00.03.76.0	2D	6900960-11
			1-9	00.03.74.0	4D	-9
			3-11	00.03.74.0	2D	-9
03A5K7	6080405	MTRH-4-26.5 C3 BRANSON	1-8	00.03.76.0	2D	-11
			4-5	00.03.76.0	4D	-11
			3-7	00.03.76.0	4D	-11
03A5K8	6080408	MHUO-12D 12 VDC ALLIED CONTROL	10-13	00.03.74.0	2B	-9
			2-9	00.03.73.0	3D	-8
			4-11	00.03.73.0	2D	-8
			6-12	00.03.73.0	1D	-8

RELAY	IBM NO.	MANUFACT. NO.	CONTACTS	LOCATION		
				LOGIC NUMBER	ZONE	DRAWING
03A5K9	6080405	MTRH-4-26.5 C3 BRANSON	1-8	00.03.73.0	2C	6900960-8
			2-7	00.03.73.0	2C	-8
			4-6	00.03.76.0	3D	-11
03A5K10	6080408	MHUO-12D 12 VDC ALLIED CONTROL	COIL 10-13	00.03.74.0	2D	-9
			8-14	00.03.73.0	3C	-8
			4-11	00.03.73.0	2C	-8
03A5K11	6080405	MTRH-4-26.5 C3 BRANSON	COIL 1-8	00.03.73.0	1D	6900960-8
			2-7	00.03.73.0	1D	-8
			6-4	00.03.76.0	4D	-11
03A5K12	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	10-13	00.03.76.0	2D	-11
			6-12	00.03.76.0	4B	-11
			1-9-2	00.03.76.0	4B	-11
			4-11	00.03.76.0	5C	-11
03A5K14	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	COIL 10-13	00.03.76.0	4C	6900960-11
			2-9	00.03.76.0	3C	6900960-11
03A5K15	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	COIL 10-13	00.03.76.0	3C	6900960-11
			2-9	00.03.70.0	9C	6900960-4
03A5K16	6080406	MHUO-12D 26.5 VDC ALLIED CONTROL	COIL 10-13	00.03.76.0	4C	6900960-11
			2-9	00.03.70.0	9C	-4
			3-4-11	00.03.76.0	3B	-11
01B5K1	6080429	PBHG-12A 24 VAC ALLIED CONTROL	COIL 1-2	00.03.70.4	9D	6900960-5
			6-11	00.03.70.0	8D	-1
			5-12	00.03.70.4	9D	-5
01B5K2	6080355	CAT B330 22C ROWAN CONTROL	C1-C3	00.03.70.0	8D	6900960-1
			T1-L1	00.03.70.0	8D	-1
			T2-L2	00.03.70.1	8D	-2
			T3-L3	00.03.70.3	9D	-4
01B4K1	6080409	MHYO-12D 26.5 VDC ALLIED CONTROL	9-10	00.03.77.0	8D	6900960-12
			COIL 1-2	00.03.76.0	8B	6900960-11

LN 00.03.78.0

QTY	SYM	NOMENCLATURE	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM
REQD	BOL	OR DESCRIPTION				IDENT	NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS:		DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE	MIN	MIN	9/14/54	FEDERAL SYSTEMS DIVISION			
INSIDE	MIN	MAX		300 MADISON AVE. NEW YORK 22, N. Y.			
ALL DIMENSIONS AND TOLERANCES		DESIGN CHECK		TITLE			
ARE TO BE SHOWN UNLESS				RELAY, CROSS REFERENCE LIST			
OTHERWISE SPECIFIED		DRAWN	9-11-54	NORTHERN			
SEE IN PLACE		DRAWING CHECK		SCALE NONE			
DECIMALS DECIMALS ANGLES		DESIGN APPROVAL		CODE IDENT NO. SIZE			
				03640 F 6900960			
				SHEET 13			

Figure 10-22. Relay Cross Reference List

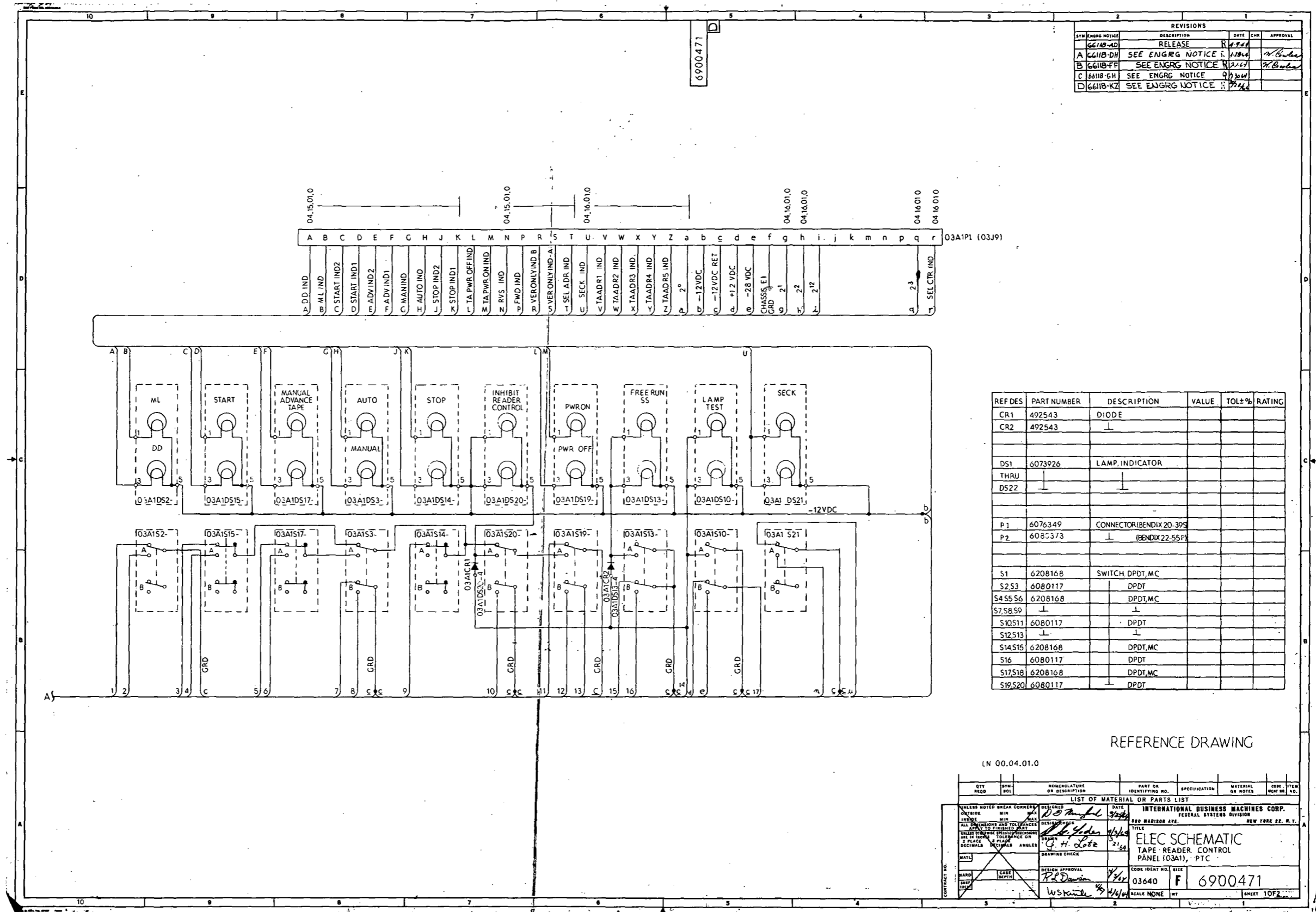


Figure 10-23. Tape Reader Control Panel Assembly (03A1) Electrical Schematic Diagram (LN 00.04.01.0 and LN 00.04.01.1) (Sheet 1 of 2)
V-10-88

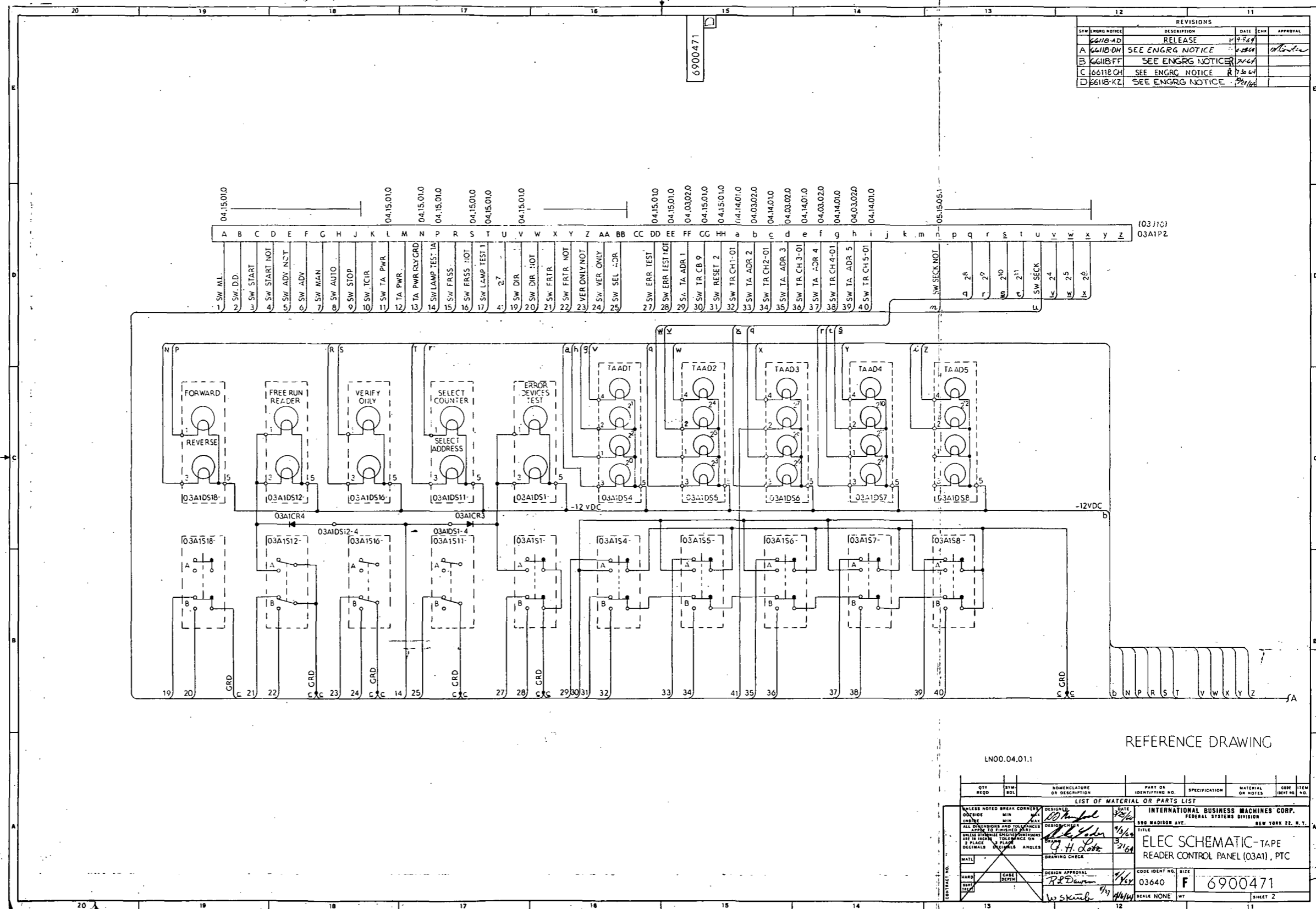
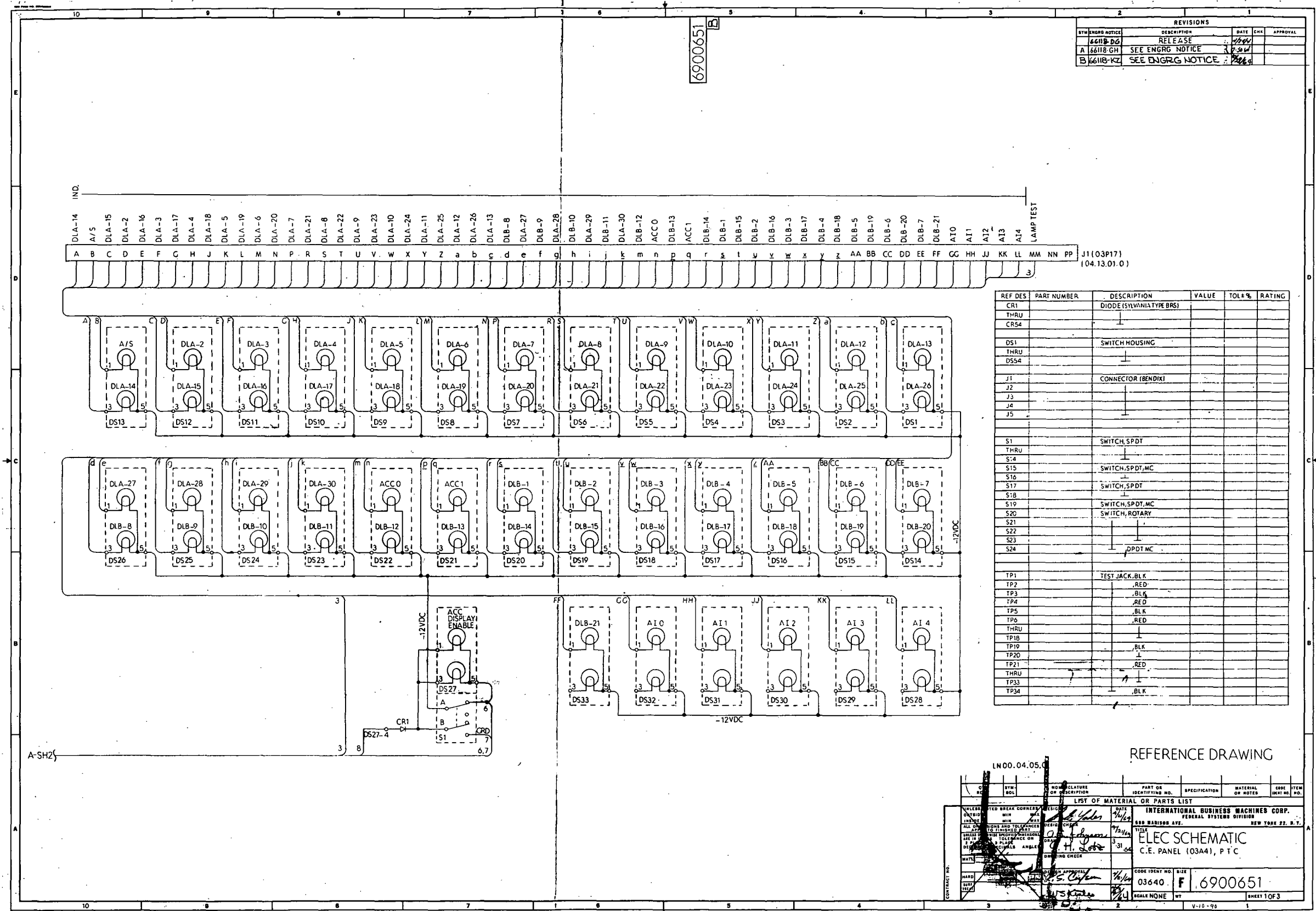


Figure 10-23. Tape Reader Control Panel Assembly (03A1) Electrical Schematic Diagram (LN 00. 04. 01. 0 and LN 00. 04. 01.1) (Sheet 2)



REVISIONS				
REV	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
A	66118-DG	RELEASE	1/24/64	
B	66118-GH	SEE ENGRG NOTICE	3/25/64	
C	66118-KZ	SEE ENGRG NOTICE	7/26/64	

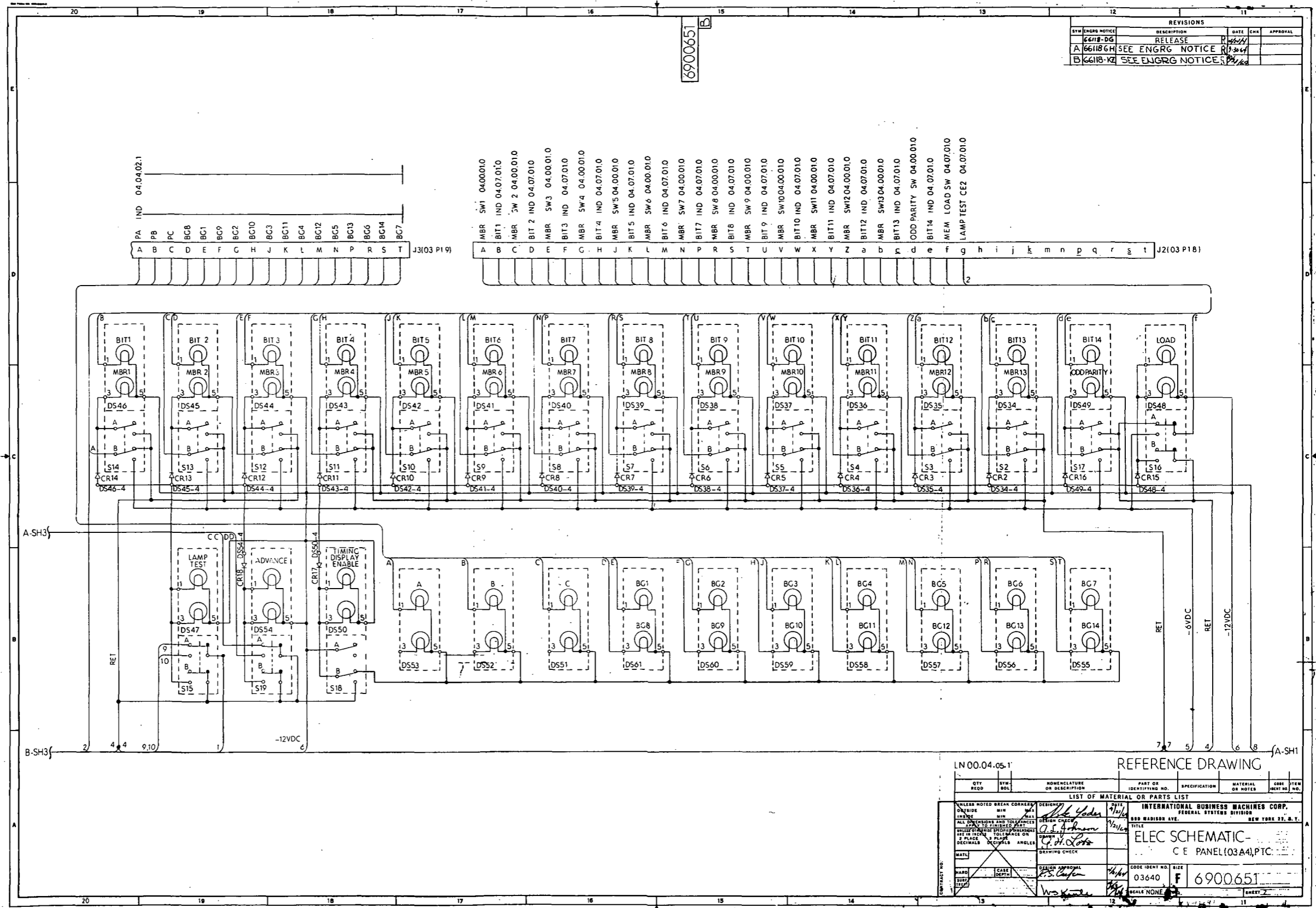
REF DES	PART NUMBER	DESCRIPTION	VALUE	TOL%	RATING
CR1		DIODE (SYLVANIA TYPE BRS)			
THRU					
CR54					
DS1		SWITCH HOUSING			
THRU					
DS54					
J1		CONNECTOR (BENDIX)			
J2					
J3					
J4					
J5					
S1		SWITCH, SPDT			
THRU					
S14					
S15		SWITCH, SPDT, MC			
S16					
S17		SWITCH, SPDT			
S18					
S19		SWITCH, SPDT, MC			
S20		SWITCH, ROTARY			
S21					
S22					
S23					
S24		DPDT MC			
TP1		TEST JACK, BLK			
TP2		RED			
TP3		BLK			
TP4		RED			
TP5		BLK			
TP6		RED			
THRU					
TP18					
TP19		BLK			
TP20					
TP21		RED			
THRU					
TP33					
TP34		BLK			

LN00.04.05.0

REFERENCE DRAWING

QTY	SYM	NO. RELATIVE OR DESCRIPTION	PART OR IDENTIFYING NO.	APPROXIMATION	MATERIAL OR NOTES	USE ITEM OR PART NO.
LIST OF MATERIAL OR PARTS LIST						
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION NEW YORK 22, N. Y.						
ELEC SCHEMATIC C.E. PANEL (03A4), P T C						
HARD COPY NO. 03640			SIZE F		6900651	
SCALE NONE			V-10-90		SHEET 1 OF 3	

Figure 10-24. C. E. Panel Assembly (03A4) Electrical Schematic Diagram (LN 00.04.05.0, LN 00.04.05.1 and LN 00.04.05.2) (Sheet 1 of 3)
V-10-90



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
66118-DG		RELEASE	11/24/64	
A	66118-GH	SEE ENGRG NOTICE R 11/24/64		
B	66118-KZ	SEE ENGRG NOTICE R 11/24/64		

6900651

LN 00.04.05.1 REFERENCE DRAWING

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS: DESIGNER: <i>John Yoder</i> DATE: <i>11/24/64</i>							
ON-SIDE MIN MAX: <i>1/16" 1/8" 1/4"</i> DESIGN CHECK: <i>W.S. Cooper</i>							
ALL DIMENSIONS AND TOLERANCES ARE IN INCHES UNLESS OTHERWISE SPECIFIED. DIMENSIONS TO BE PLACED ON ORIGINALS IN FULL ANGLES. DRAWING CHECK: <i>W.S. Cooper</i>							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 880 MADISON AVE. NEW YORK 27, N. Y.							
TITLE: ELEC SCHEMATIC - C E PANEL (03A4), PTC							
DRAWN BY: <i>W.S. Cooper</i> CODE IDENT NO: 03640 SIZE: F							
CHECKED BY: <i>W.S. Cooper</i> SCALE: NONE SHEET: 2							

Figure 10-24. C. E. Panel Assembly (03A4) Electrical Schematic Diagram (LN 00. 04. 05. 0, LN 00. 04. 05. 1 and LN 00. 04. 05. 2) (Sheet 2)

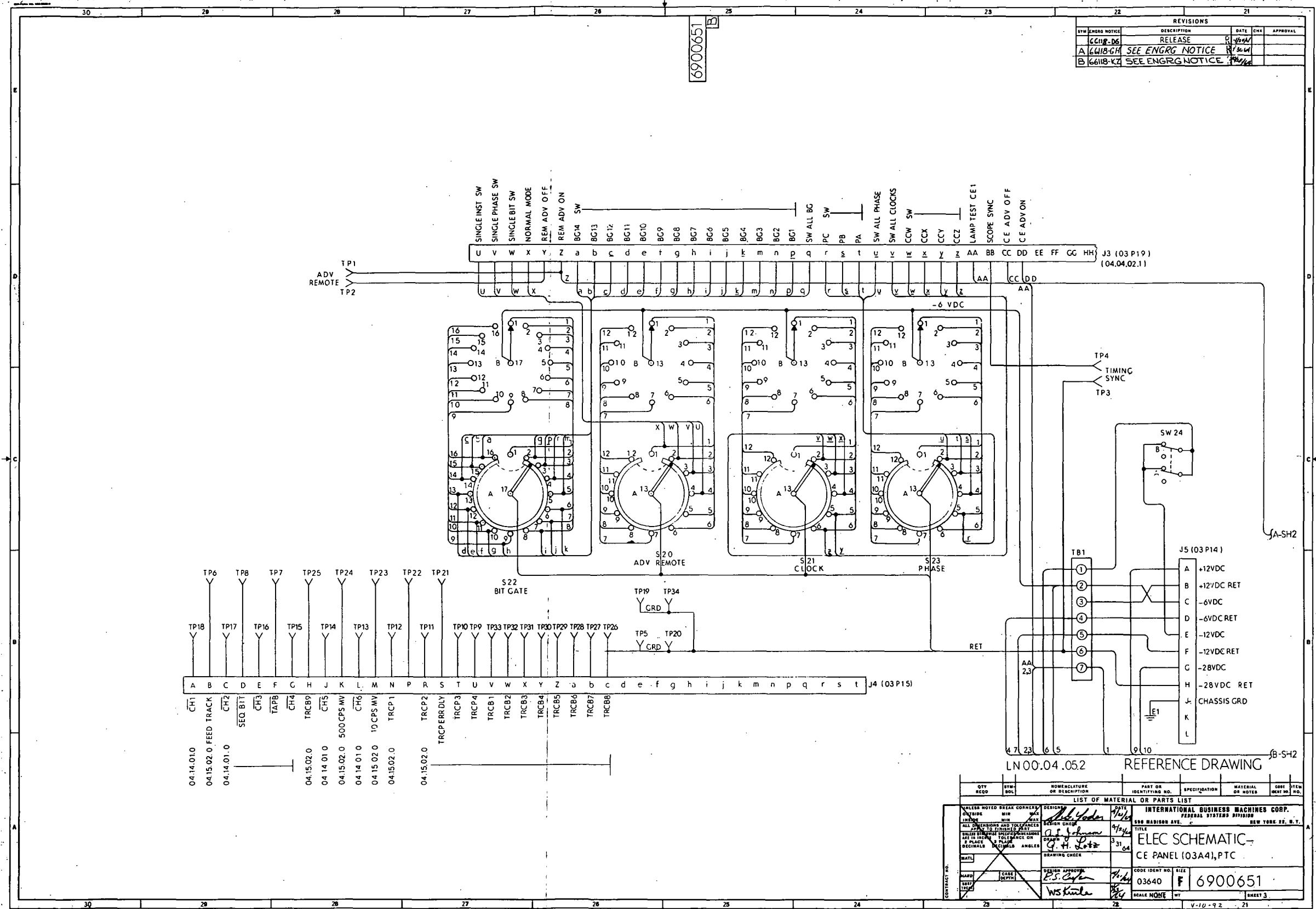
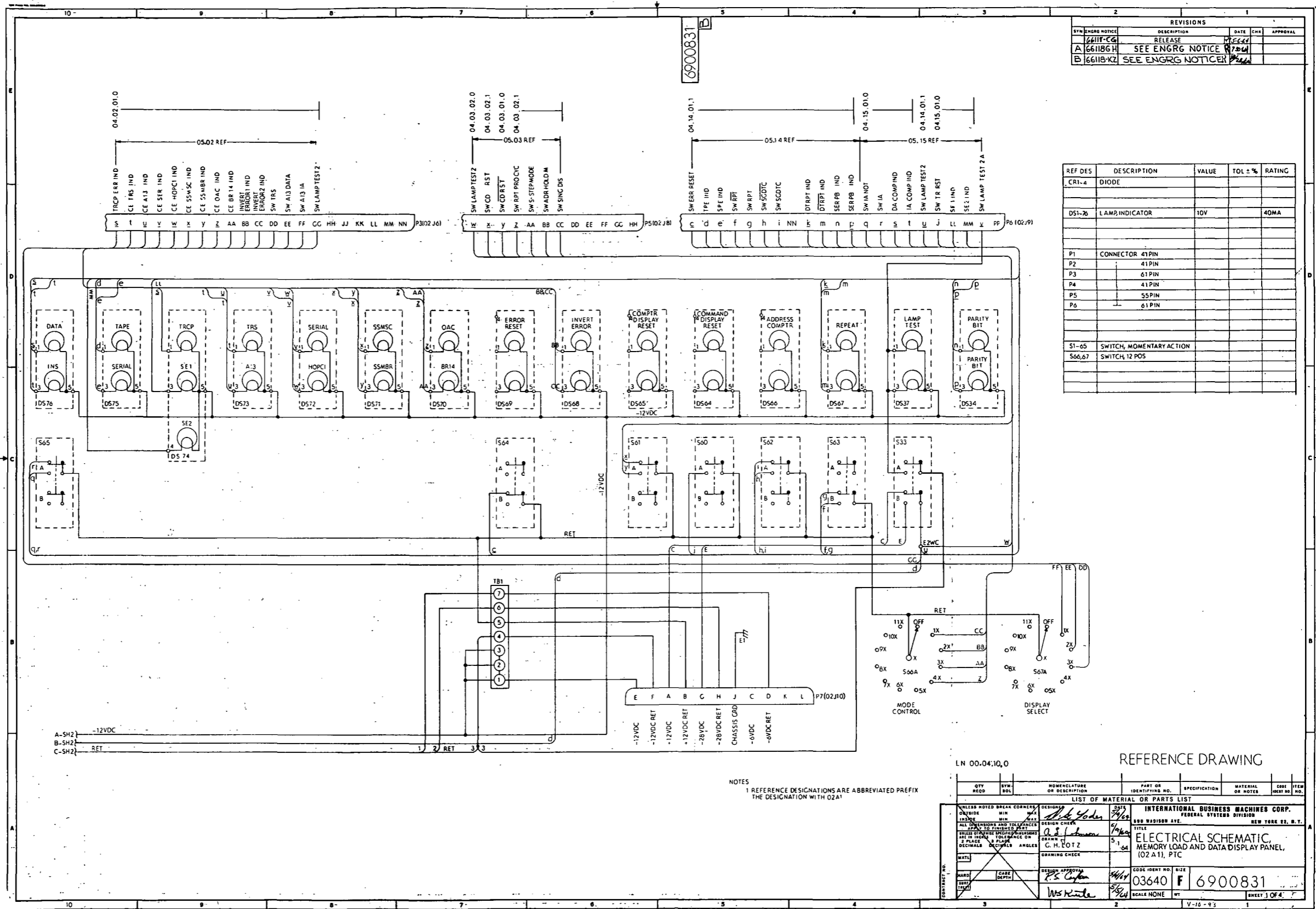


Figure 10-24. C. E. Panel Assembly (03A4) Electrical Schematic Diagram (LN 00. 04. 05. 0, LN 00. 04. 05. 1 and LN 00. 04. 05. 2) (Sheet 3)
V-10-92



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPVAL
A	66118-CG	RELEASE	7/20/64	
B	66118B-H	SEE ENGRG NOTICE	7/20/64	
B	66118-KZ	SEE ENGRG NOTICE	7/20/64	

REF DES	DESCRIPTION	VALUE	TOL ± %	RATING
CR1-4	DIODE			
DS1-26	LAMP INDICATOR	10V		40MA
P1	CONNECTOR	41 PIN		
P2		41 PIN		
P3		61 PIN		
P4		41 PIN		
P5		55 PIN		
P6		61 PIN		
S1-65	SWITCH, MOMENTARY ACTION			
S66,67	SWITCH, 12 POS			

LN 00.04.10.0

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	COND. IDENT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 350 MADISON AVE. NEW YORK 22, N.Y.							
TITLE: ELECTRICAL SCHEMATIC, MEMORY LOAD AND DATA DISPLAY PANEL, (02A1), PTC							
CODE IDENT NO. SIZE: 03640 F 6900831							
SCALE: NONE							

Figure 10-25. Memory Load and Data Display Panel Assembly (02A1) Electrical Schematic Diagram (LN 00.04.10.0, LN 00.04.10.1, LN 00.04.10.2 and LN 00.04.10.3) (Sheet 1 of 4)

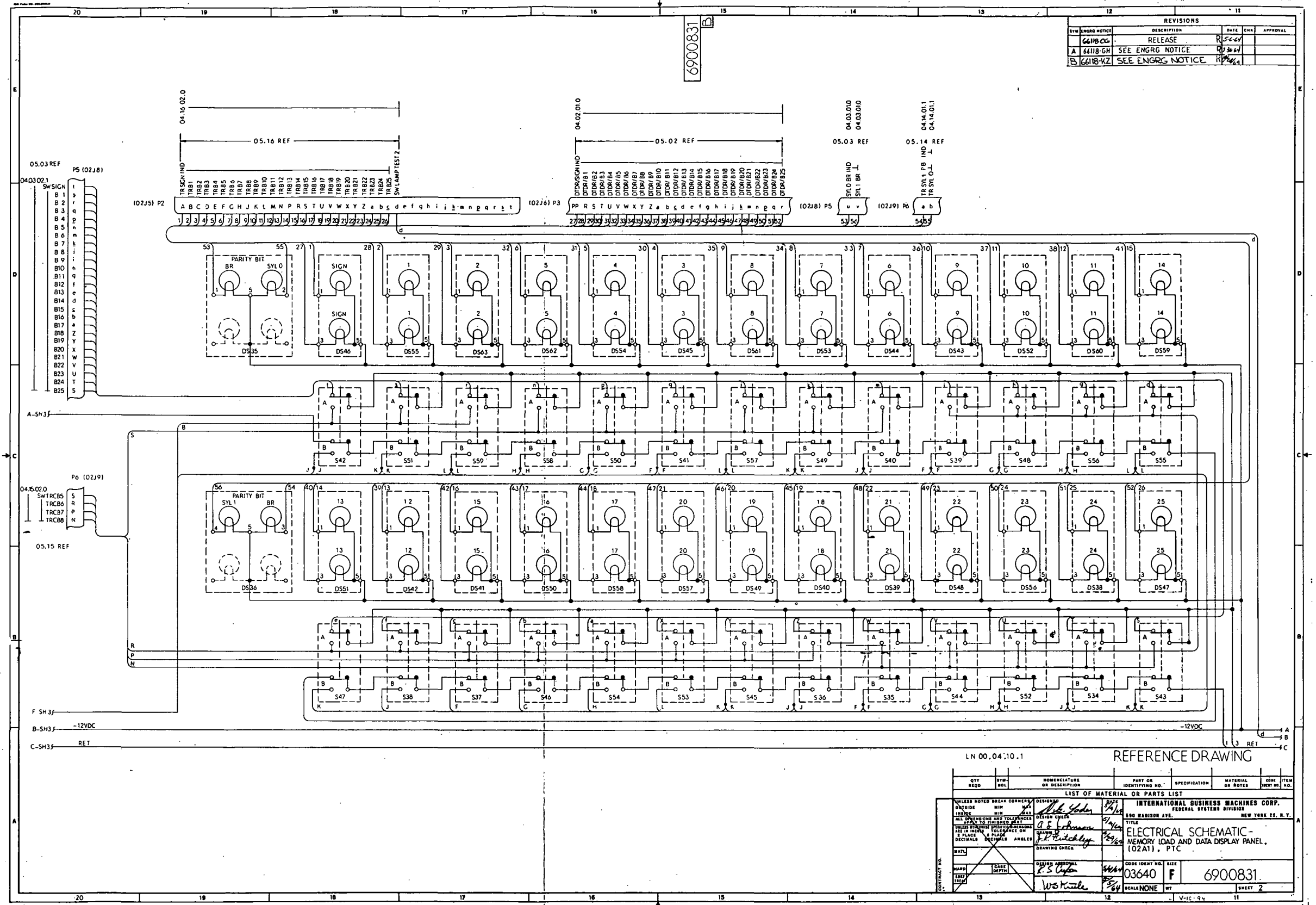
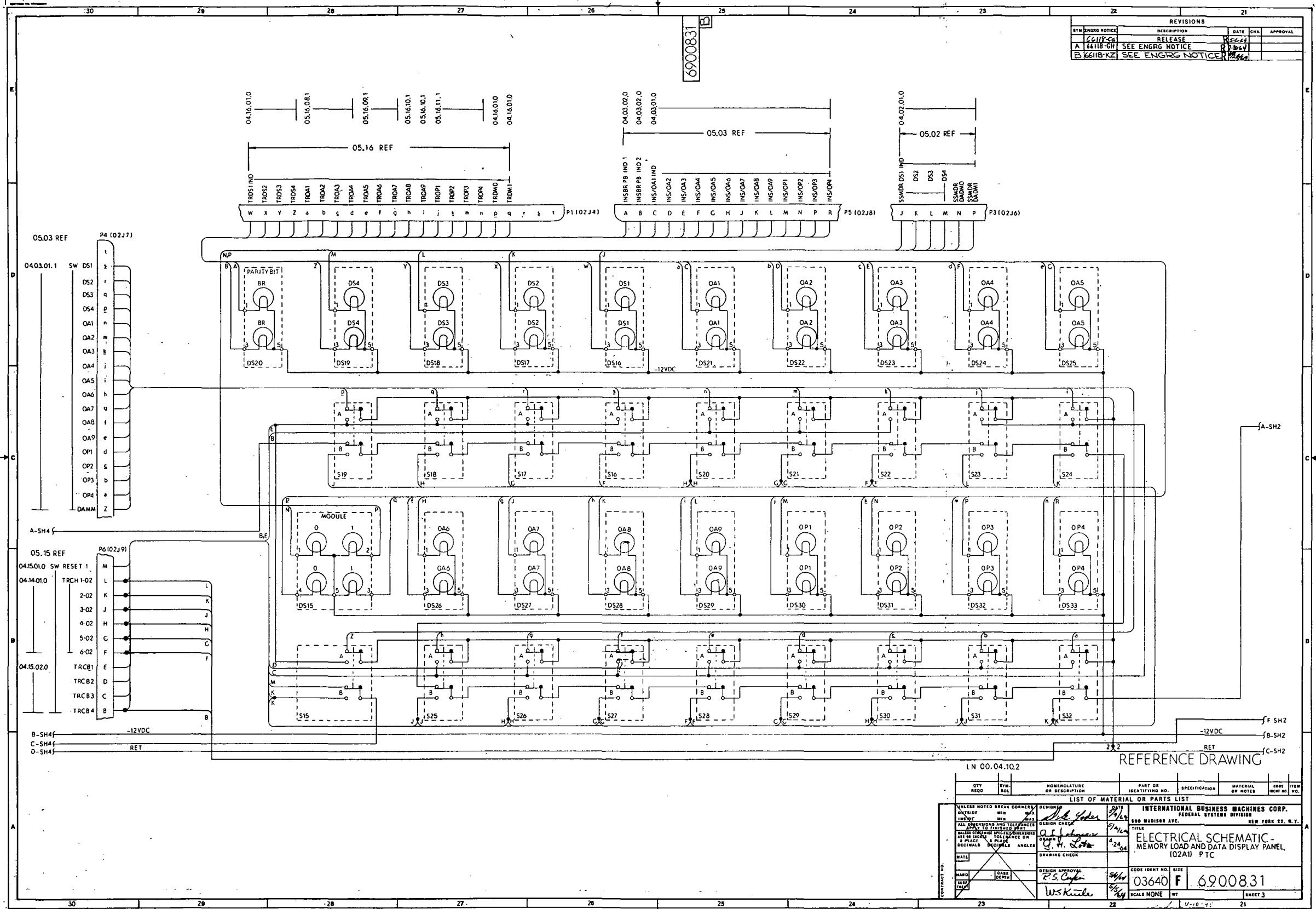


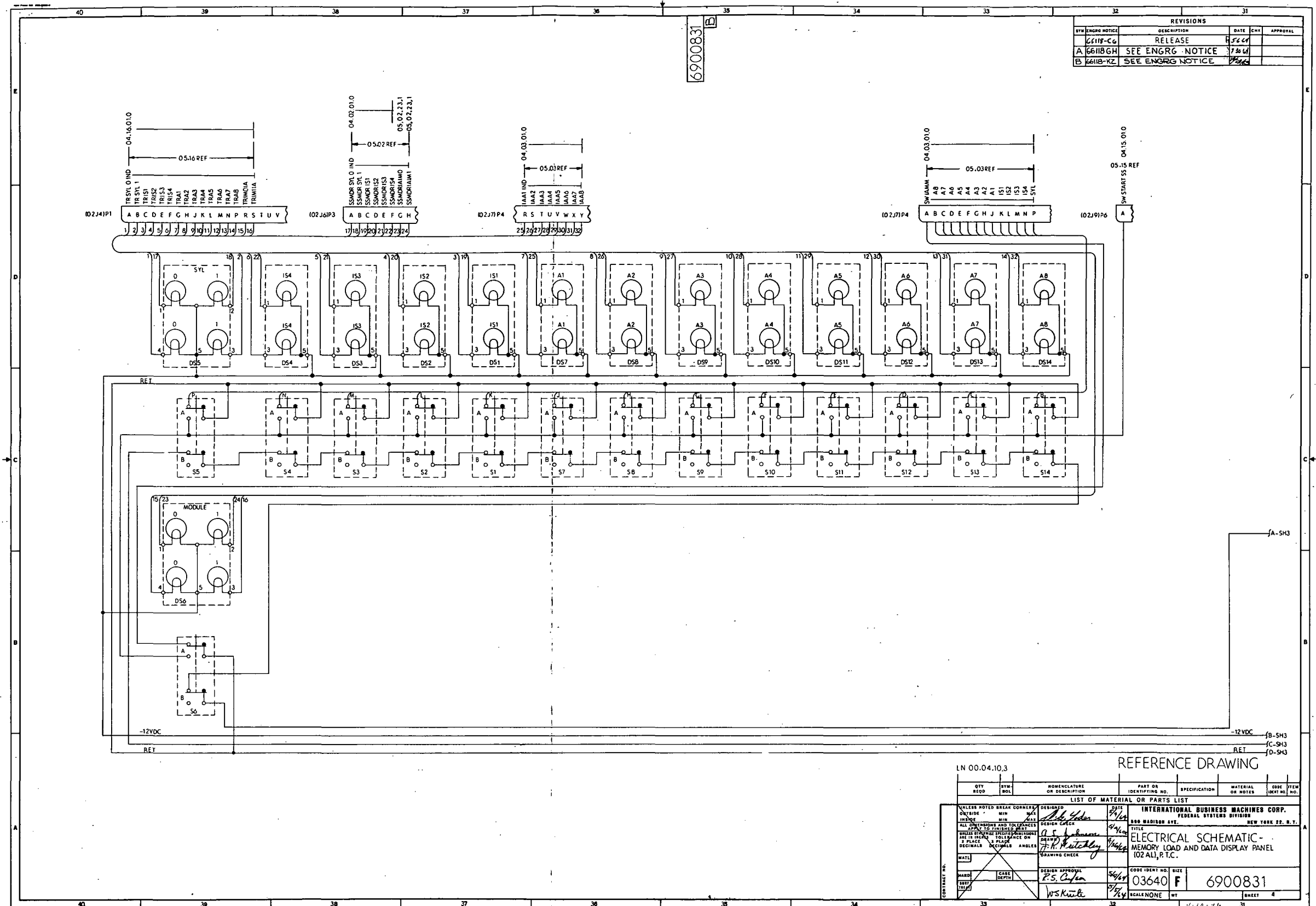
Figure 10-25. Memory Load Data Display Panel Assembly (02A1) Electrical Schematic Diagram (LN 00. 04. 10. 0, LN 00. 04. 10. 1, LN 00. 04. 10. 2 and LN 00. 04. 10. 3) (Sheet 2)
V-10-94



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK
A	6611B-SH	SEE ENGRG NOTICE	12-24-64	
B	6611B-KZ	SEE ENGRG NOTICE	12-24-64	

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	ENGR	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
DESIGNED BY		DESIGN CHECK		INTERNATIONAL BUSINESS MACHINES CORP.			
DRAWN BY		CHECKED BY		FEDERAL SYSTEMS DIVISION			
DATE		DATE		580 MADISON AVE. NEW YORK 22, N.Y.			
SCALE		SCALE		TITLE			
				ELECTRICAL SCHEMATIC -			
				MEMORY LOAD AND DATA DISPLAY PANEL			
				(02A1) PTC			
DRAWING APPROVAL		DESIGN APPROVAL		CODE IDENT NO.		SIZE	
WS Kuebler		R.S. Cooper		03640		F 6200831	
				SCALE NONE		SHEET 3	

Figure 10-25. Memory Load Data Display Panel Assembly (02A1) Electrical Schematic Diagram (LN 00. 04. 10. 0, LN 00. 04. 10. 1, LN 00. 04. 10. 2 and LN 00. 04. 10. 3) (Sheet 3)



REVISIONS			
BY	ENGRG NOTICE	DESCRIPTION	DATE
	66118-C6	RELEASE	7/26/66
A	66118-BGH	SEE ENGRG NOTICE	7/26/66
B	66118-KZ	SEE ENGRG NOTICE	7/26/66

LN 00.04.10.3 REFERENCE DRAWING

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM LIST NO.
LIST OF MATERIAL OR PARTS LIST							
<small>UNLESS NOTED BREAK CORNERS TO BE SHOWN ON THIS DRAWING</small> <small>ALL DIMENSIONS AND TOLERANCES ARE TO UNFINISHED PARTS</small> <small>FRACE & HEAD DECIMALS ANGLES</small>							
DESIGNED BY: <i>W.S. Knize</i>		CHECKED BY: <i>W.S. Knize</i>		DRAWN BY: <i>W.S. Knize</i>		DATE: <i>7/26/66</i>	
DESIGN APPROVAL: <i>E.S. Carter</i>		DRAWING CHECK: <i>W.S. Knize</i>		INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 350 MADISON AVE. NEW YORK 22, N.Y.		TITLE: ELECTRICAL SCHEMATIC - MEMORY LOAD AND DATA DISPLAY PANEL (02 AL), P.T.C.	
MATERIAL:		SCALE: NONE		CODE IDENT NO: 03640		SIZE: F	
CONTRACT NO.:		DRAWING NO.:		6900831		SHEET 4	

Figure 10-25. Memory Load Data Display Panel Assembly (02A1) Electrical Schematic Diagram (LN 00.04.10.0, LN 00.04.10.1, LN 00.04.10.2 and LN 00.04.10.3) (Sheet 4)
V-10-96

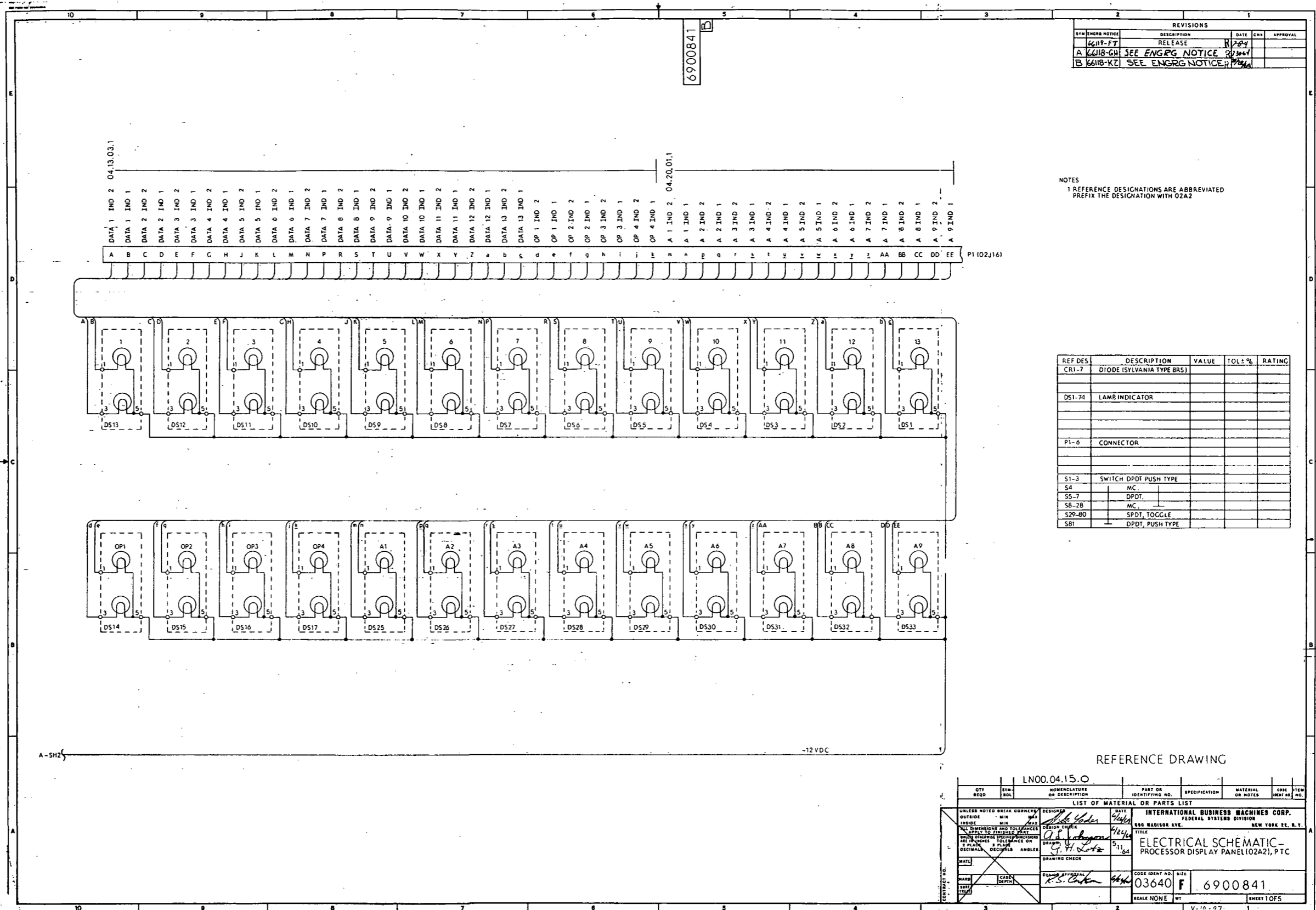


Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4) (Sheet 1 of 5)

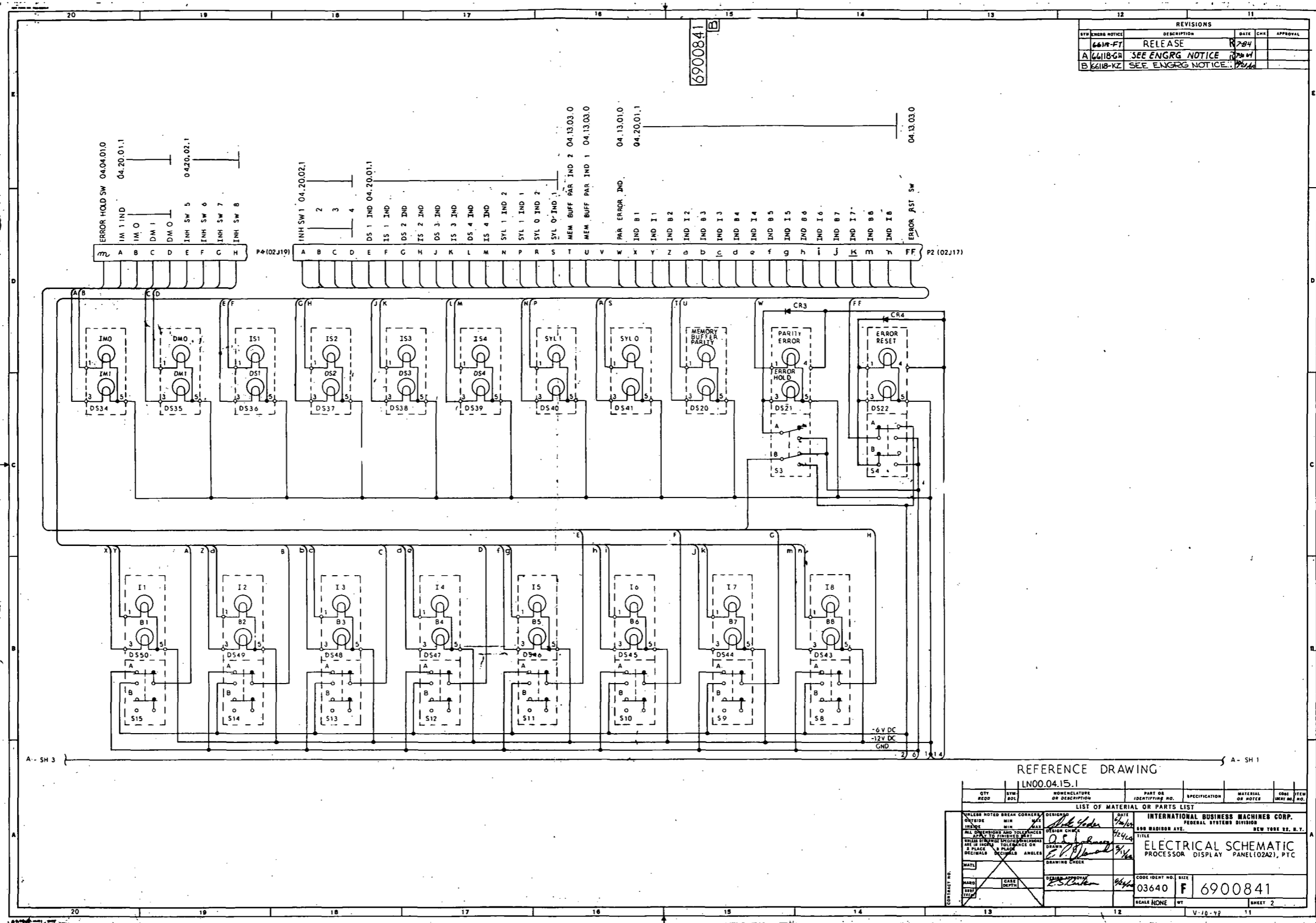
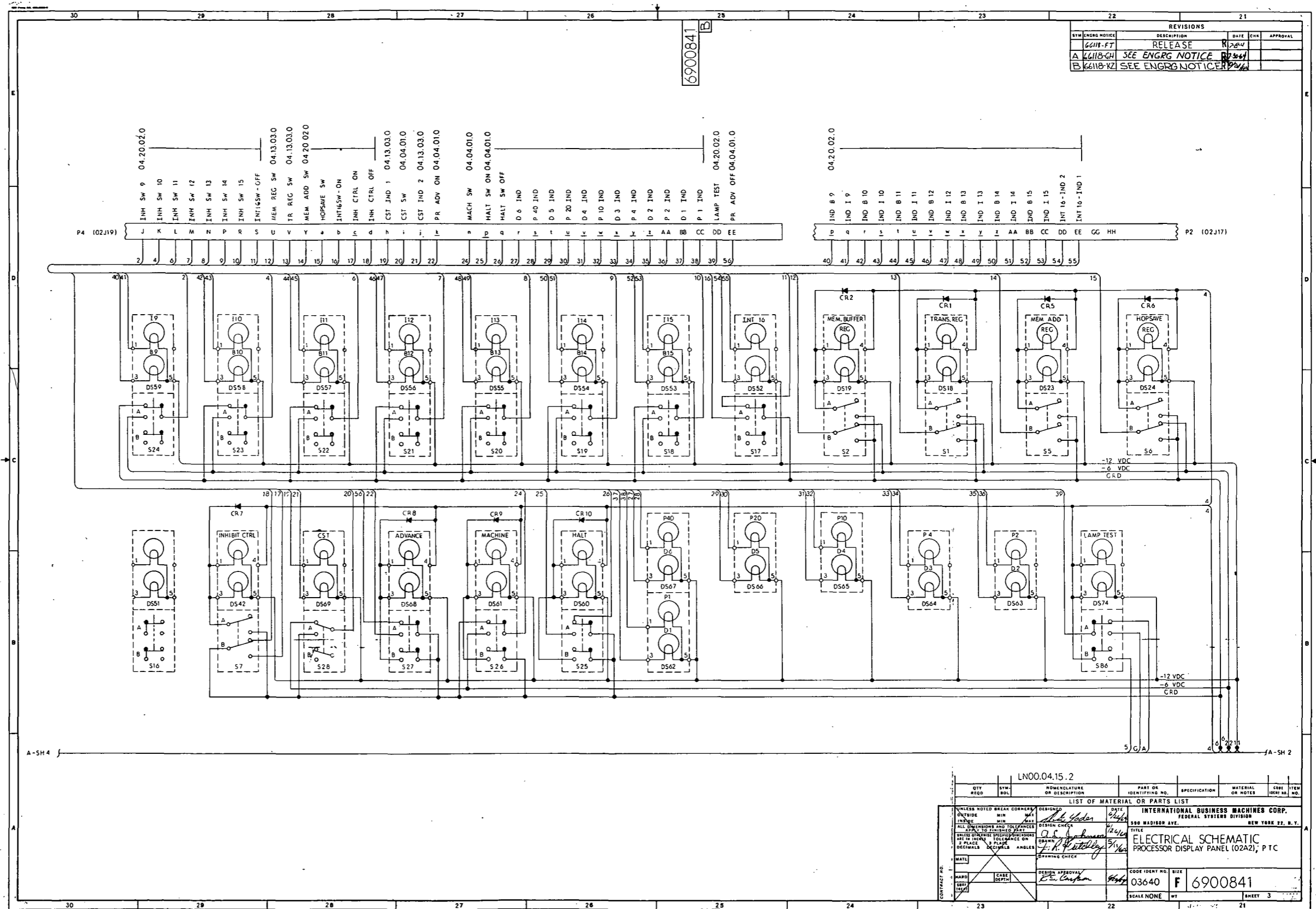


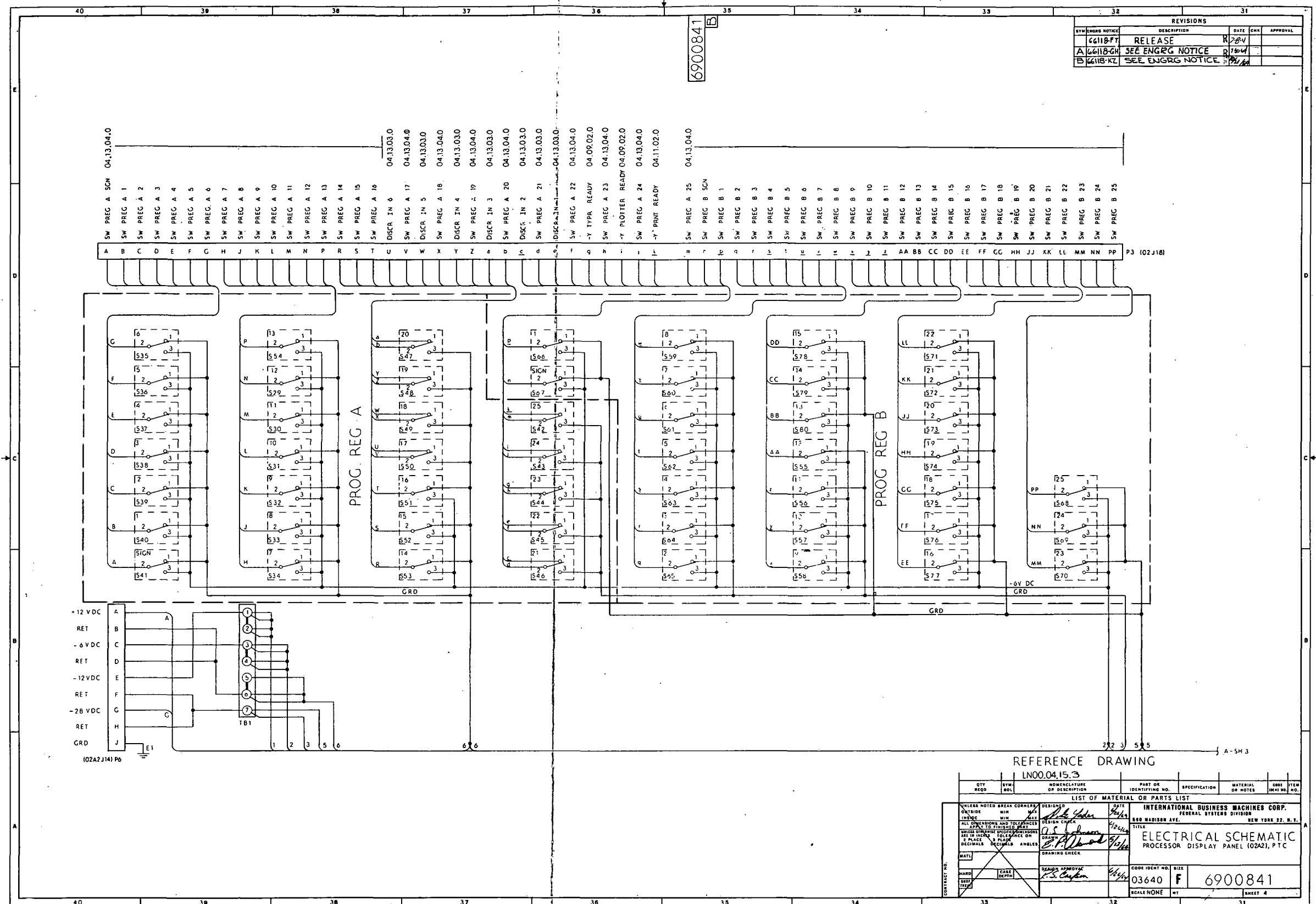
Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4) (Sheet 2)
V-10-98



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	66118-FT	RELEASE	1/28/64	
A	66118-GH	SEE ENGRG NOTICE	2/24/64	
B	66118-KZ	SEE ENGRG NOTICE	2/24/64	

LN00.04.15.2									
QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM	NO.	
LIST OF MATERIAL OR PARTS LIST									
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION NEW YORK 27, N. Y.									
ELECTRICAL SCHEMATIC PROCESSOR DISPLAY PANEL (02A2); PTC									
DESIGNED BY: <i>John J. Guder</i>		DATE: <i>2/24/64</i>		DESIGN CHECK: <i>John J. Guder</i>		CODE IDENT NO.:		SIZE:	
DRAWN BY: <i>L. R. G. [Signature]</i>		DATE: <i>2/24/64</i>		DRAWING CHECK: <i>[Signature]</i>		03640		F 6900841	
SCALE: NONE		SHEET: 3		SCALE: NONE		WT:		SHEET: 3	

Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4) (Sheet 3)



REVISIONS			
SYMBOL	DESCRIPTION	DATE	APPROVAL
66118-FT	RELEASE	R/284	
A 66118-GH	SEE ENGRG NOTICE	R/1604	
B 66118-KZ	SEE ENGRG NOTICE	R/1604	

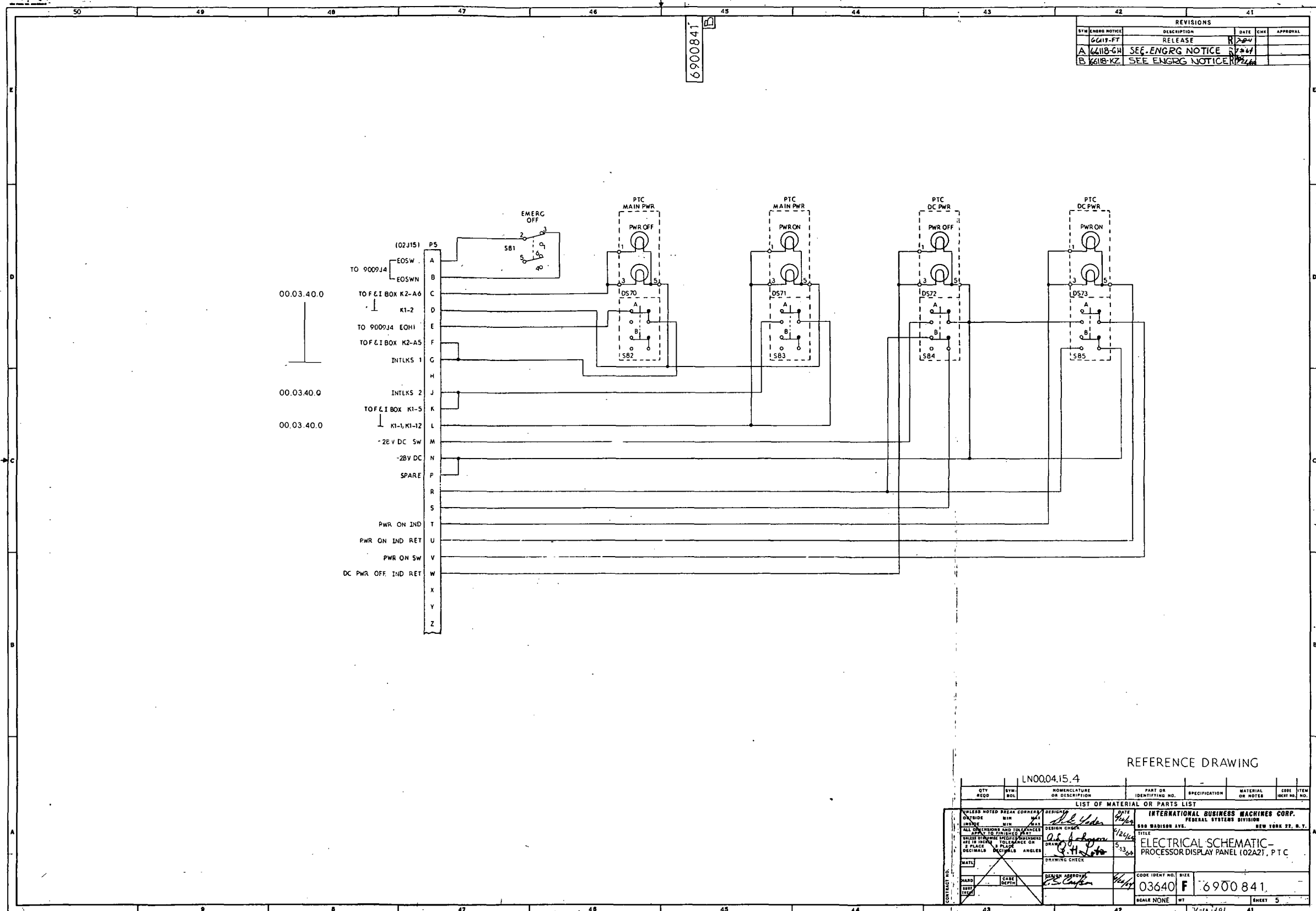
REFERENCE DRAWING
LN00.04.15.3

QTY	SYM	NOMENCLATURE	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL	CODE	ITEM

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP.
OUTSIDE MIN MAX	<i>John</i>	<i>4/24/64</i>	FEDERAL SYSTEMS DIVISION
ALL DIMENSIONS AND TOLERANCES TO BE TO UNLESS OTHERWISE SPECIFIED	DESIGN CHECK		800 MADISON AVE. NEW YORK 22, N. Y.
SALES ENGINEER SPECIFICATIONS TO BE TO UNLESS OTHERWISE SPECIFIED	<i>A.S. Brown</i>	<i>4/24/64</i>	TITLE
1 PLACE 2 PLACE 3 PLACE 4 PLACE 5 PLACE 6 PLACE 7 PLACE 8 PLACE 9 PLACE 10 PLACE	DRAWN	<i>A.S. Brown</i>	ELECTRICAL SCHEMATIC
DECIMALS ANGLES	DRAWING CHECK	<i>A.S. Brown</i>	PROCESSOR DISPLAY PANEL (02A2), PTC
MATL	DESIGN APPROVAL	<i>F.S. Clayton</i>	CODE IDENT NO. SIZE
	CASE DEPTH	<i>F.S. Clayton</i>	03640 F
			6900841
			SCALE NONE WT
			SHEET 4

Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4) (Sheet 4)
V-10-100



REVISIONS				
REV	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
6	6411-FT	RELEASE	11/20/64	
A	6411B-GH	SEE ENGRG NOTICE	11/20/64	
B	6411B-KZ	SEE ENGRG NOTICE	11/20/64	

REFERENCE DRAWING

LN0004.15.4

QTY	SYM	NOMENCLATURE	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS	DESIGN	DATE	INTERNATIONAL BUSINESS MACHINES CORP.
OUTSIDE	MIN	MAX	FEDERAL SYSTEMS DIVISION
INDUCE	MIN	MAX	500 MADISON AVE. NEW YORK 27, N.Y.
ALL DIMENSIONS AND TOLERANCES	DESIGN CHECK		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATE		
3 PLACE DECIMALS	13	06	
DECIMALS	ANGLES		
	DRAWING CHECK		
	DESIGN APPROV		
	CHECK		
	DATE		

CODE IDENT NO.	SIZE	
03640	F	6900841
SCALE NONE	WT	SHEET 5

Figure 10-26. Processor Display Panel Assembly (02A2) Electrical Schematic Diagram (LN 00. 04. 15. 0 through LN 00. 04. 15. 4) (Sheet 5)

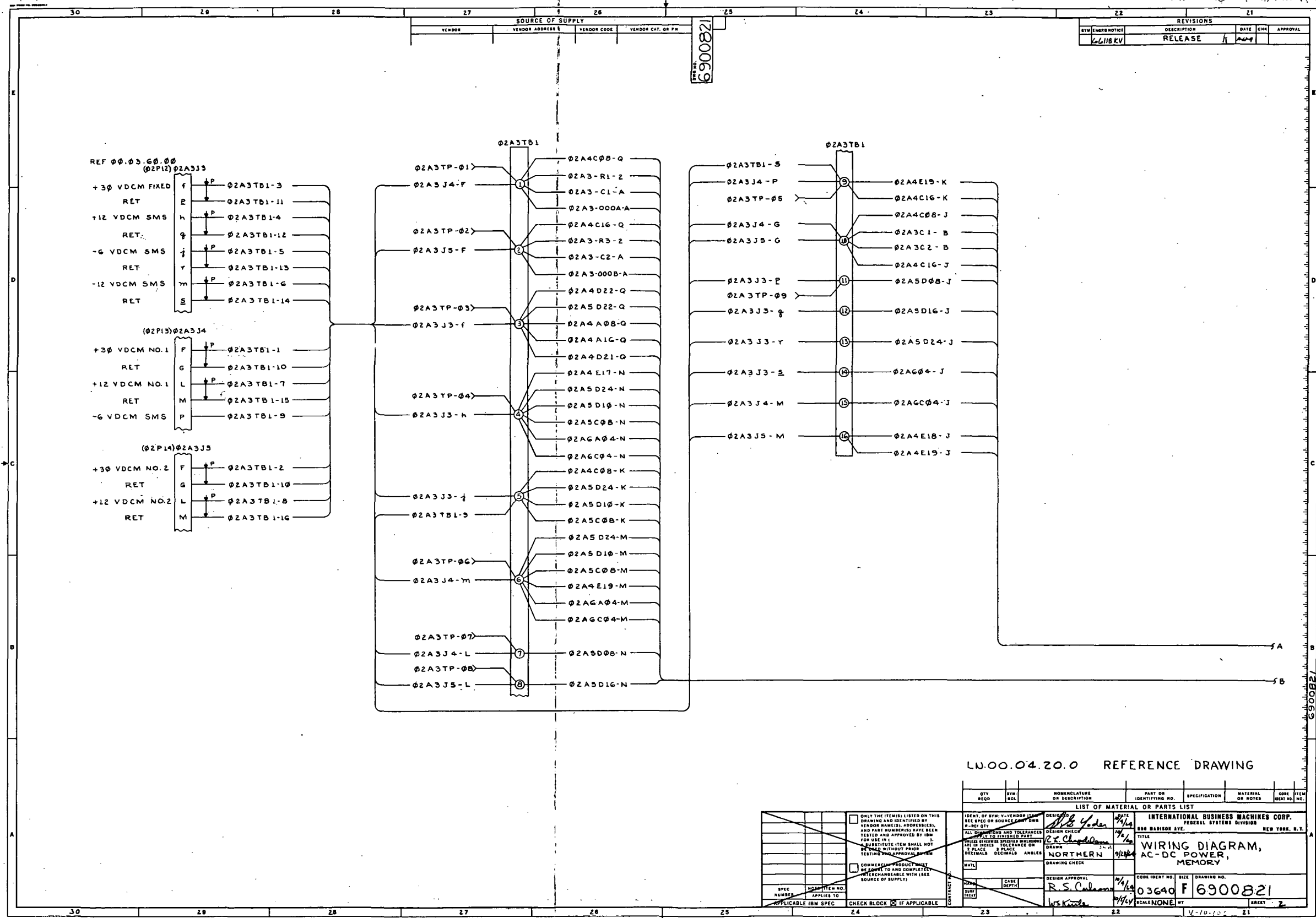
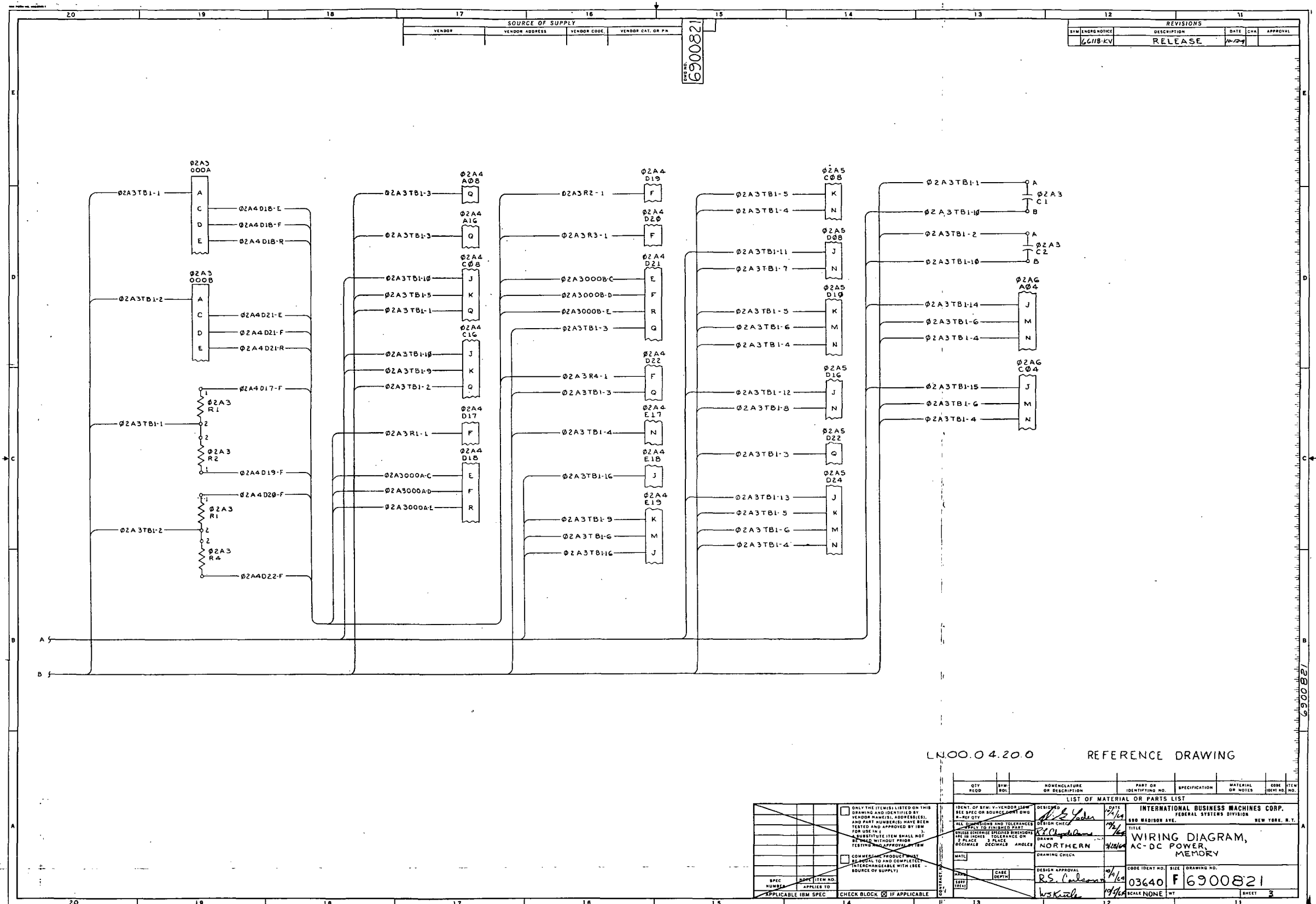


Figure 10-27. Memory AC-DC Power Diagram (LN 00. 04. 20. 1 and 00. 04. 20. 0) (Sheet 1 of 3)



SOURCE OF SUPPLY			
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

REVISIONS				
SYM	ENGINE/NOTICE	DESCRIPTION	DATE	APPROVAL
66118-KV		RELEASE	10/27	

LN00.04.20.0 REFERENCE DRAWING

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
<input type="checkbox"/> ONLY THE ITEMS LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN A... <input type="checkbox"/> CONSUMER PRODUCTS... <input type="checkbox"/> IBM... <input type="checkbox"/> IBM...							
DESIGNED BY		DESIGN CHECK		DRAWN		DRAWING CHECK	
DATE		DATE		DATE		DATE	
BY		BY		BY		BY	
APPROVAL		APPROVAL		APPROVAL		APPROVAL	
DATE		DATE		DATE		DATE	
BY		BY		BY		BY	
APPLICABLE IBM SPEC		CHECK BLOCK		IF APPLICABLE			
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 800 MADISON AVE. NEW YORK, N. Y.				TITLE WIRING DIAGRAM, AC-DC POWER, MEMORY			
CODE IDENT NO.		SIZE		DRAWING NO.			
03640		F		6900821			
SCALE		NONE		SHEET		3	

Figure 10-27. Memory AC-DC Power Diagram (LN 00.04.20.1 and 00.04.20.0) (Sheet 2)

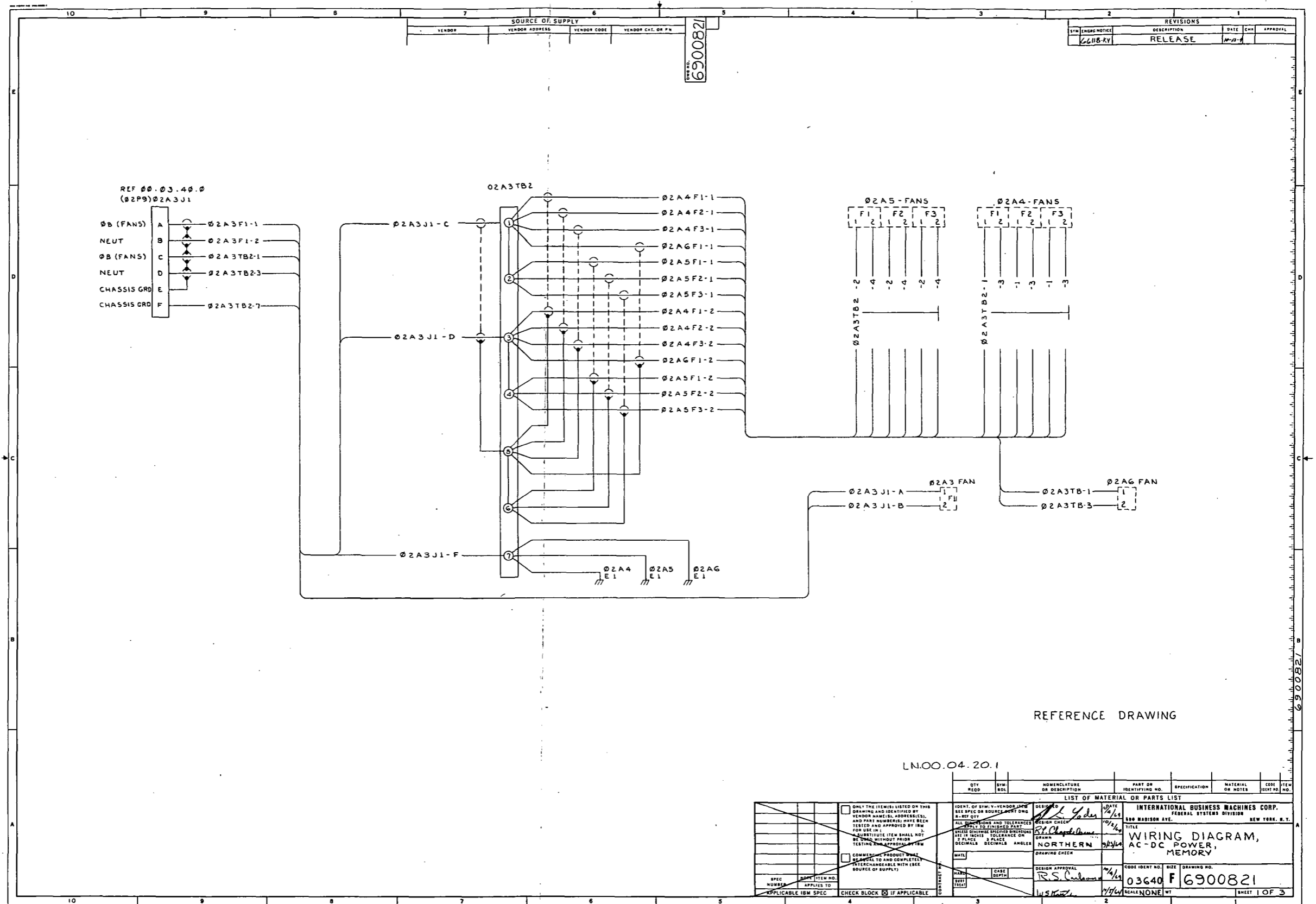


Figure 10-27. Memory AC-DC Power Diagram (LN 00.04.20.1 and 00.04.20.0) (Sheet 3)

6900906

REVISIONS				
REV	DESCRIPTION	DATE	CHK	APPROVAL
1	RELEASE	1:11		
A	661187			YCDER

- SYMBOL INDEX**
- | | | |
|------------------|---------------------|------------------------------|
| 1. AND | 11. LATCH 4 | 21. RELAY |
| 2. AND-INVERT | 12. LATCH 5 | 22. RELAY DRIVER |
| 3. AND-OR-INVERT | 13. LATCH 6 | 23. RESISTOR NETWORK |
| 4. DELAY | 14. LATCH 7 | 24. SENSE AMPLIFIER |
| 5. INVERTER | 15. LINE DRIVER | 25. SENSE AMPLIFIER DETECTOR |
| 6. INVERTER-OR | 16. LINE TERMINATOR | 26. SINGLE SHOT |
| 7. LAMP DRIVER | 17. OR | 27. STROBE DRIVER |
| 8. LATCH 1 | 18. OR-INVERT | 28. TRATCH |
| 9. LATCH 2 | 19. OSCILLATOR | 29. TRIGGER 1 |
| 10. LATCH 3 | 20. POWER DRIVER | 30. TRIGGER 2 |

SYMBOL DEFINITIONS
NOTE
A logic "one" is a -6VDC for -12VDC level and a logic "zero" is a 0VDC level unless otherwise noted.

INDEX NO.	SYMBOL	NAME	DESCRIPTION
1.		AND	When all inputs are "1", the output is a "1". If any input is a "0", the output is a "0".
2.		AND-INVERT	When all inputs are "1", the output is a "0". If any input is a "0", the output is a "1".
3.		AND-OR-INVERT	Inputs - outputs are the same as an And-Invert. The output transistor allows the outputs of several And-Or-Inverts to be connected (OR'd) together. A "0" output of any AO of an "OR'd" group of AO's will form a "0" output from the group.
4.		DELAY	The Delay circuit delays the input signal for the nominal duration shown above the symbol.
5.		INVERTER	A "1" input causes a "0" output and vice-versa.
6.		INVERTER-OR	Input - output same as Inverter. The output transistor allows the outputs of several Inverter-Ors to be connected (OR'd) together; a "0" output of any IO of an "OR'd" group of IO's will force a "0" output from the group.
7.		LAMP DRIVER	A "1" input causes the Lamp Driver to turn on its associated indicator lamp; a "0" input causes the Lamp Driver to turn off its associated indicator lamp.
8.		LATCH 1	 The set and reset outputs are complementary. A "0" at the "0" set input causes the set output to become a "1" and the reset output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed. Similarly, a "0" at the "0" reset input causes the reset output to become a "1" and the set output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed. An asterisk (*) immediately following a signal at a "0" set or "0" reset input indicates that this signal enters the latch through an Isolation diode.

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
9.		LATCH 2	 Same as Latch 1. "1" at the "1" set input causes the set output to become a "1" and the reset output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed. Similarly, a "1" at the "1" reset input or a "1" at the "1" reset input causes the reset output to become a "1" and the set output to become a "0"; the output will remain in this condition even after the input conditioning level is removed.
10.		LATCH 3	
11.		LATCH 4	See LATCH 1.
12.		LATCH 5	See LATCH 1.
13.		LATCH 6	See LATCH 1 and LATCH 2.

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
14.		LATCH 7	 See LATCH 2.
15.		LINE DRIVER	Signal driver and low impedance matching device.
16.		LINE TERMINATOR	The Line Terminator is a gated inverter used to terminate a transmission line in its proper impedance match and reference voltage. The omission of the gate input indicates that the gate input is a "1" at all times.
17.		OR	When all inputs are "1", the output is a "1". If any input is a "0", the output is a "0".
18.		OR-INVERT	When all inputs are "0", the output is a "1". If any input is a "1", the output is a "0". The outputs of several Or-Inverts can be OR'd together.
19.		OSCILLATOR	Generates a square wave signal (0VDC to -6VDC) at a 2.048 MC frequency.
20.		POWER DRIVER	Signal shaper and driver - a "1" input causes a "1" output; a "0" input causes a "0" output.
21.		RELAY	 RELAY COIL NORMALLY OPEN NORMALLY CLOSED ARMATURE RELAY COIL

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS	DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION				
OUTSIDE	MIN	MAX	800 MADISON AVE. NEW YORK 22, N. Y.				
INSIDE	MIN	MAX	TITLE				
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART			LOGIC DIAGRAM, PROGRAMMABLE TEST CONTROLLER (PTC)-SYMBOL DEFINITIONS				
BRIEF DIMENSIONS SPECIFY DIMENSIONS IN INCHES TOLERANCE ON DECIMALS PLACE			DRAWING CHECK				
DECIMALS DECIMALS ANGLES			DESIGN APPROVAL				
SCALE			CODE IDENT NO.		SIZE		
SCALE			F		6900906		
SCALE			SCALE		SHEET 1 of 72		

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 1 of 72)

6900906

REVISIONS				
REV	DATE	DESCRIPTION	BY	APPROVAL
1		RELEASE		
2		REDRAWN WITH CHANGE: 1/45		

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION						
22.		RELAY DRIVER	<table border="0"> <tr> <td>Input</td> <td>Output</td> </tr> <tr> <td>"1"</td> <td>0VDC</td> </tr> <tr> <td>"0"</td> <td>-26.5VDC</td> </tr> </table>	Input	Output	"1"	0VDC	"0"	-26.5VDC
Input	Output								
"1"	0VDC								
"0"	-26.5VDC								
23.		RESISTOR NETWORK	Resistors in this network are shunted across the memory current supply to control the drive current applied to the memory core array. An increase in memory ambient temperature requires a decrease in memory drive current.						
24.		SENSE AMPLIFIER	The Sense Amplifier is a gated differential amplifier that senses "1"s from the memory array at inputs A and B; the Sense Amplifier is enabled when input C (the gate input) is a "1". When a "1" is sensed at inputs A and B, the signal is amplified, rectified and sent to a Sense Amplifier Detector.						
25.		SENSE AMPLIFIER DETECTOR	The Sense Amplifier Detector is a strobed Schmitt trigger that produces a "1" output only when one of its associated Sense Amplifiers senses a "1" and the strobe input is a "0".						
26.		SINGLE SHOT	Any or all three inputs may be connected. An unconnected input (indicated by the absence of an input) is effectively a "1" input. All inputs must equal "1" to trigger the single shot. The negative going transition of the last input to become a "1" triggers the single shot. The duration of the negative square wave output is shown above the symbol.						
27.		STROBE DRIVER	The Strobe Driver provides the signal to strobe the 14 Sense Amplifier Detectors in each memory. The Strobe Driver inverts and amplifies its input signal.						
28.		TRATCH	A "0" input causes the corresponding output to become a "0" and the other two outputs to become "1"s.						
29.		TRIGGER 1	The set output becomes a "1" when input A is a "0" and input B goes from a "1" to a "0". The reset output becomes a "1" when input D is a "0" and input C goes from a "1" to "0". (The omission of input "1" set and "1" reset inputs indicates that these lines are grounded.)						
30.		TRIGGER 2	The set output becomes a "1" when input A is a "0" and input B goes from a "1" to a "0". The reset output becomes a "1" when input C is a "0" and input B goes from a "1" to a "0". (The omission of input "1" set and "1" reset indicates that these lines are grounded.)						

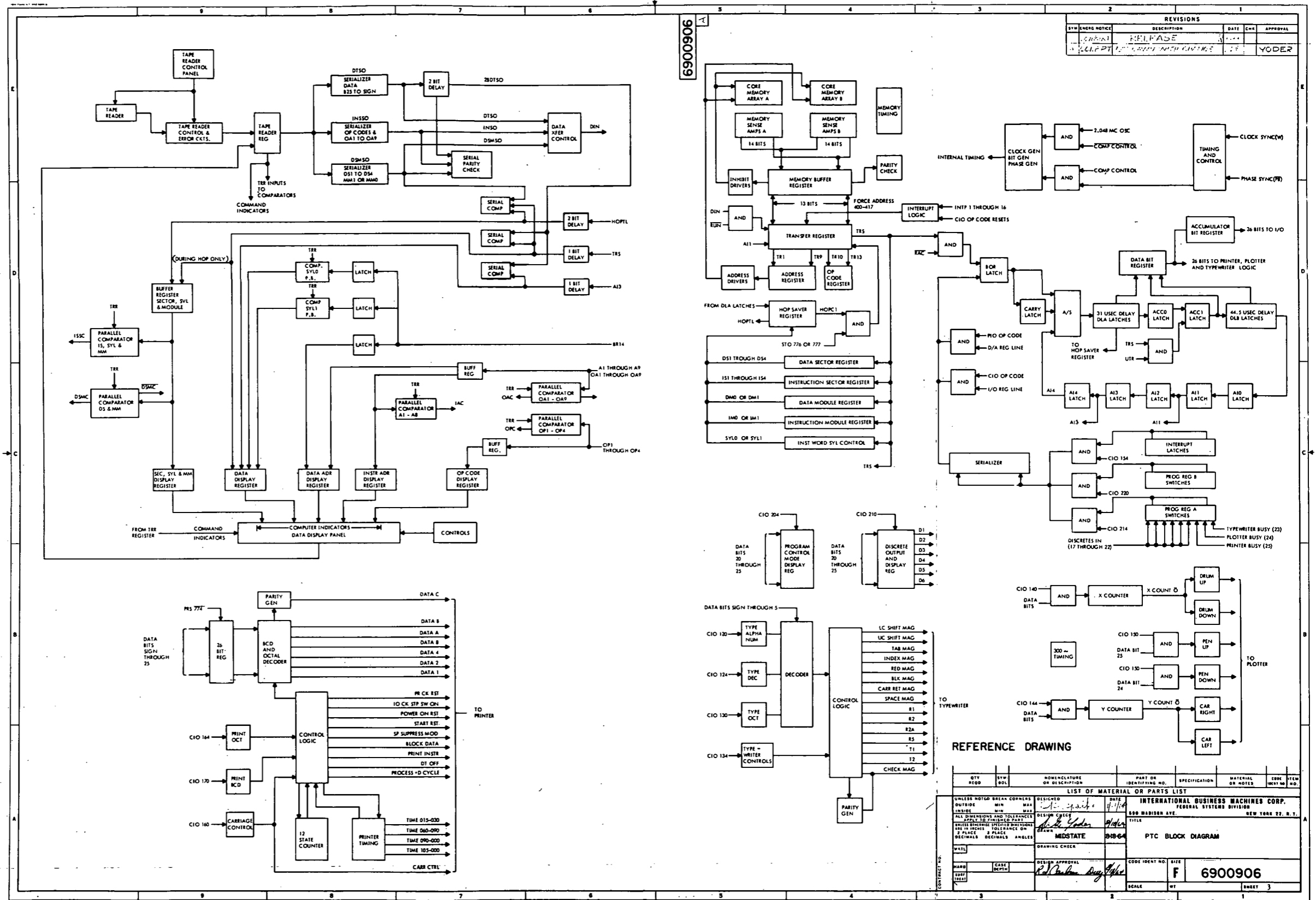
NOTES:

- Abbreviations of signal names are defined in 6900910, Symbol Definitions and Signal Abbreviations for the PTC. Listing of additional abbreviations are:
 - MSEC millisecond
 - USEC microsecond
 - NSEC nanosecond
 - MC megacycles
- The numbers listed in tabular INPUTS and OUTPUTS columns are sheet number locations of signal origin and destinations.
- All logic blocks are defined on sheets 1 and 2.

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CON	ITEM
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE		WIS	WAS	FEDERAL SYSTEMS DIVISION			
INSIDE		WIS	WAS	300 MADISON AVE. NEW YORK 27, N. Y.			
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART		DESIGNED BY	DATE	TITLE			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 3 PLACE DECIMALS DECIMALS ANGLES		WIS	WAS	SYMBOL DEFINITIONS			
DRAWING CHECK		DESIGN APPROVAL	DATE	CODE IDENT NO.	SIZE	6900906	
MATERIAL		WIS	WAS	SCALE	WT	SHEET 2	

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 2)



REFERENCE DRAWING

QTY	REV	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	DATE	BY
1	1	PTC BLOCK DIAGRAM	6900906				

LIST OF MATERIAL OR PARTS LIST

QTY	REV	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	DATE	BY
1	1	PTC BLOCK DIAGRAM	6900906				

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
500 MADISON AVE. NEW YORK 22, N.Y.

PTC BLOCK DIAGRAM

DRAWING NO. 6900906
SCALE: 1:1
SHEET 3

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 3)

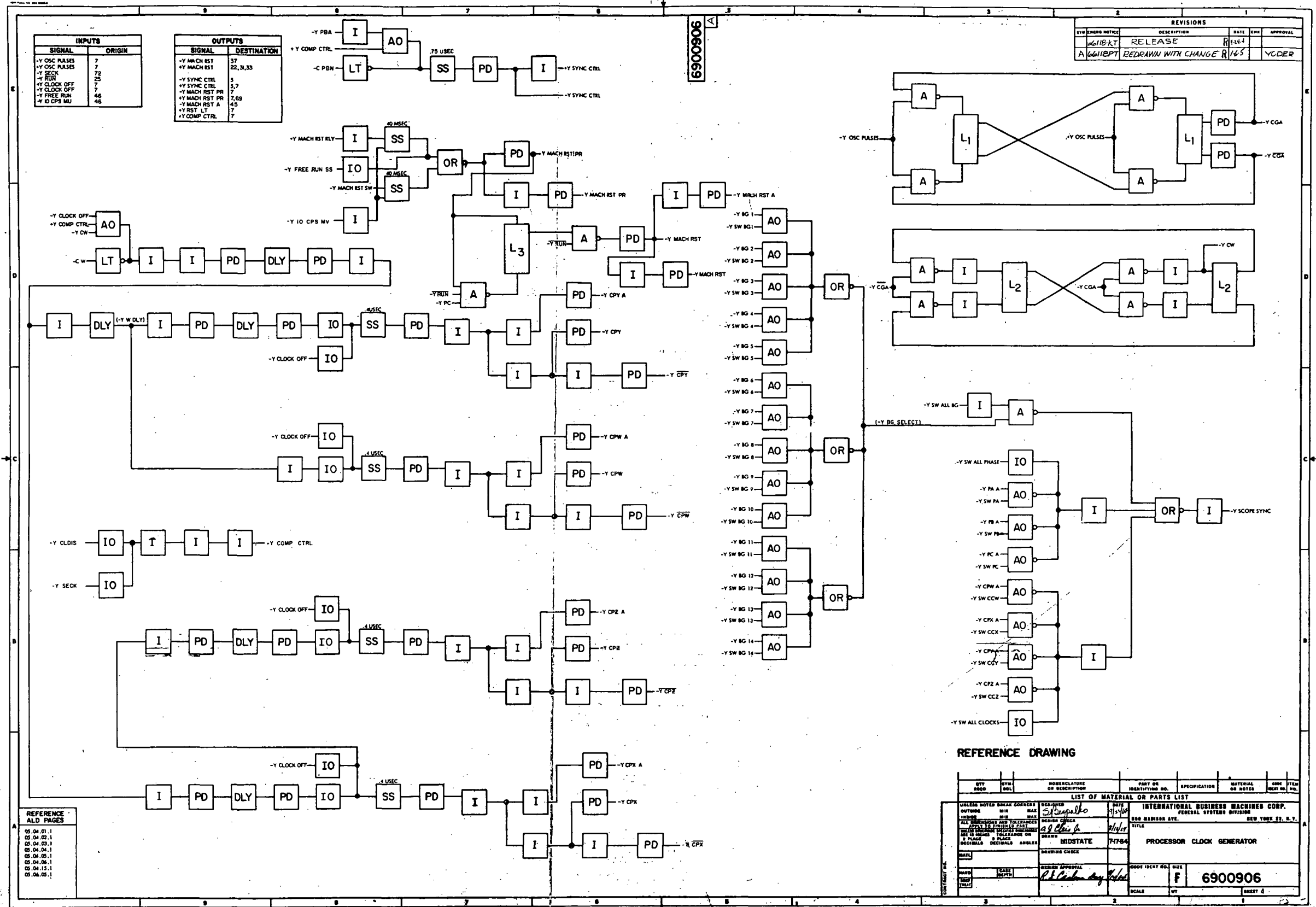


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 4)

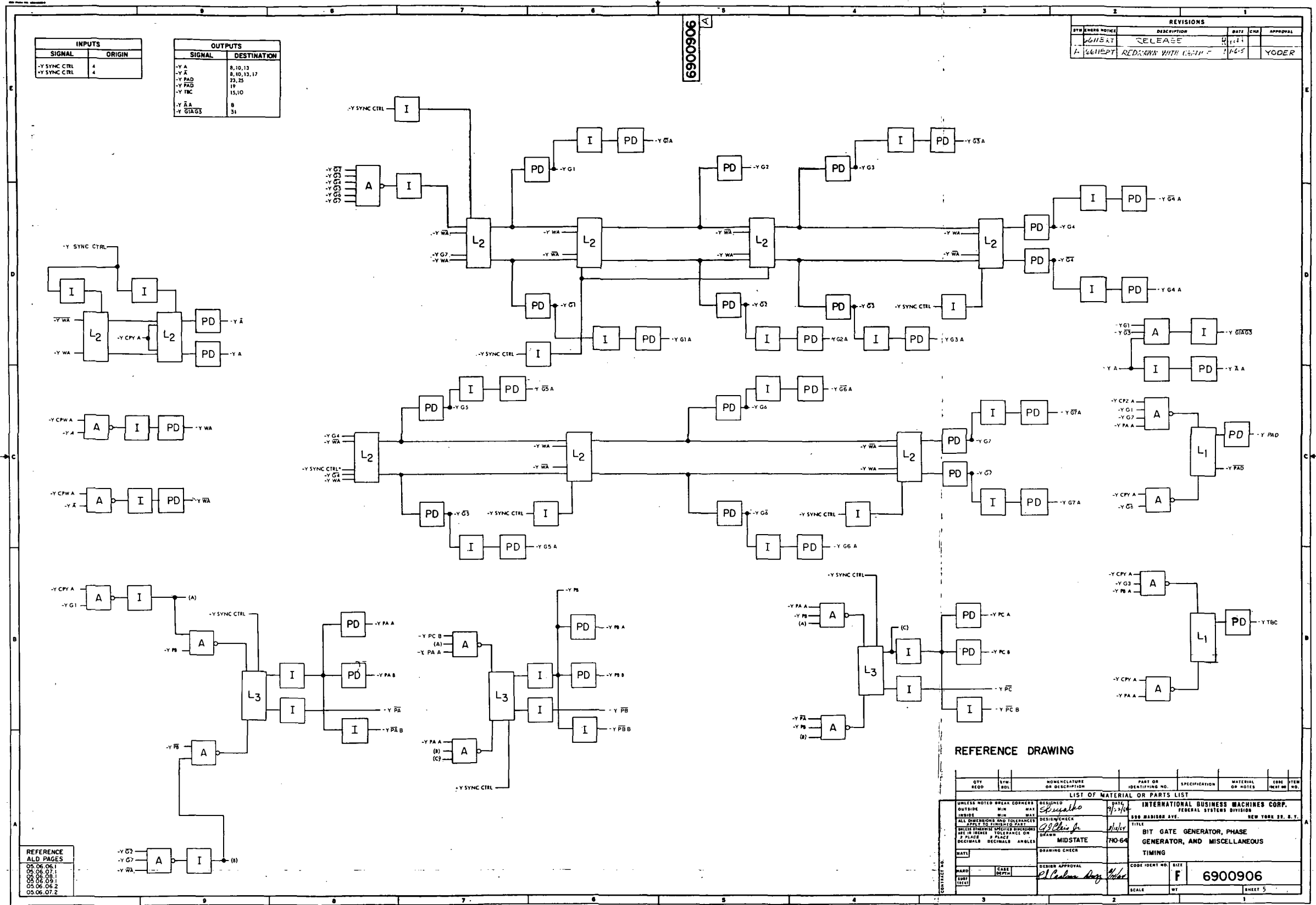


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 5)

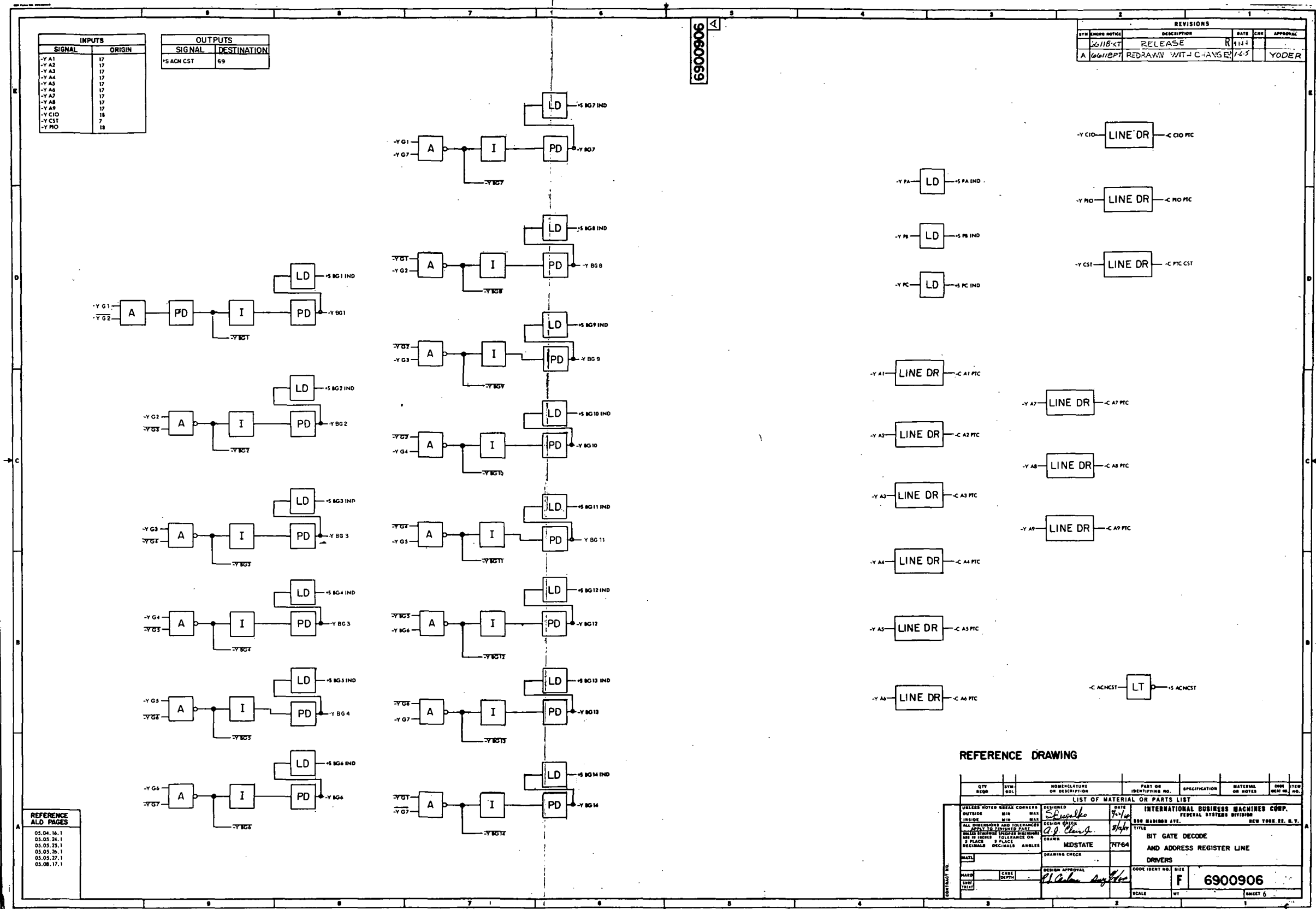


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 6)

V-10-110

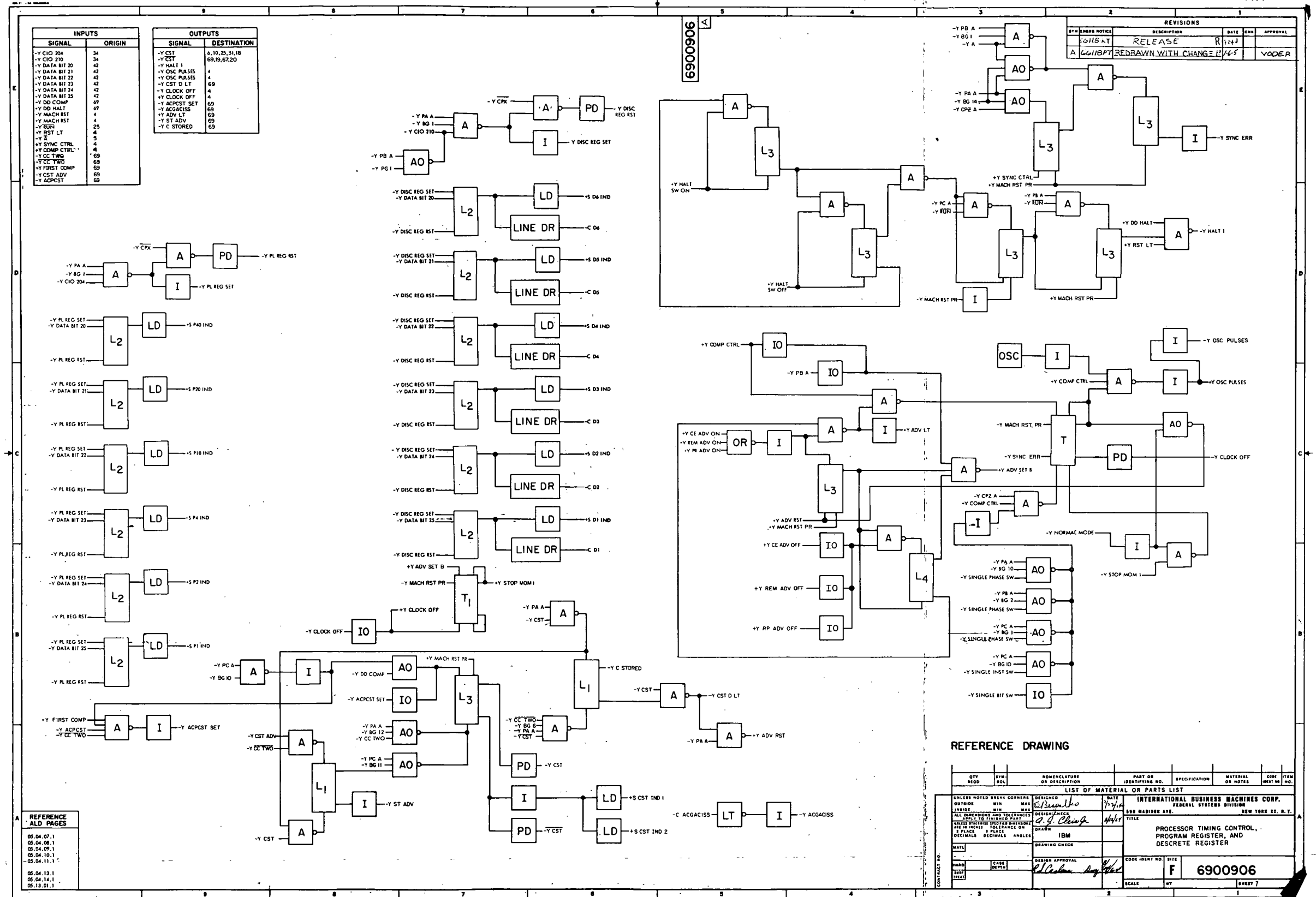


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 7)

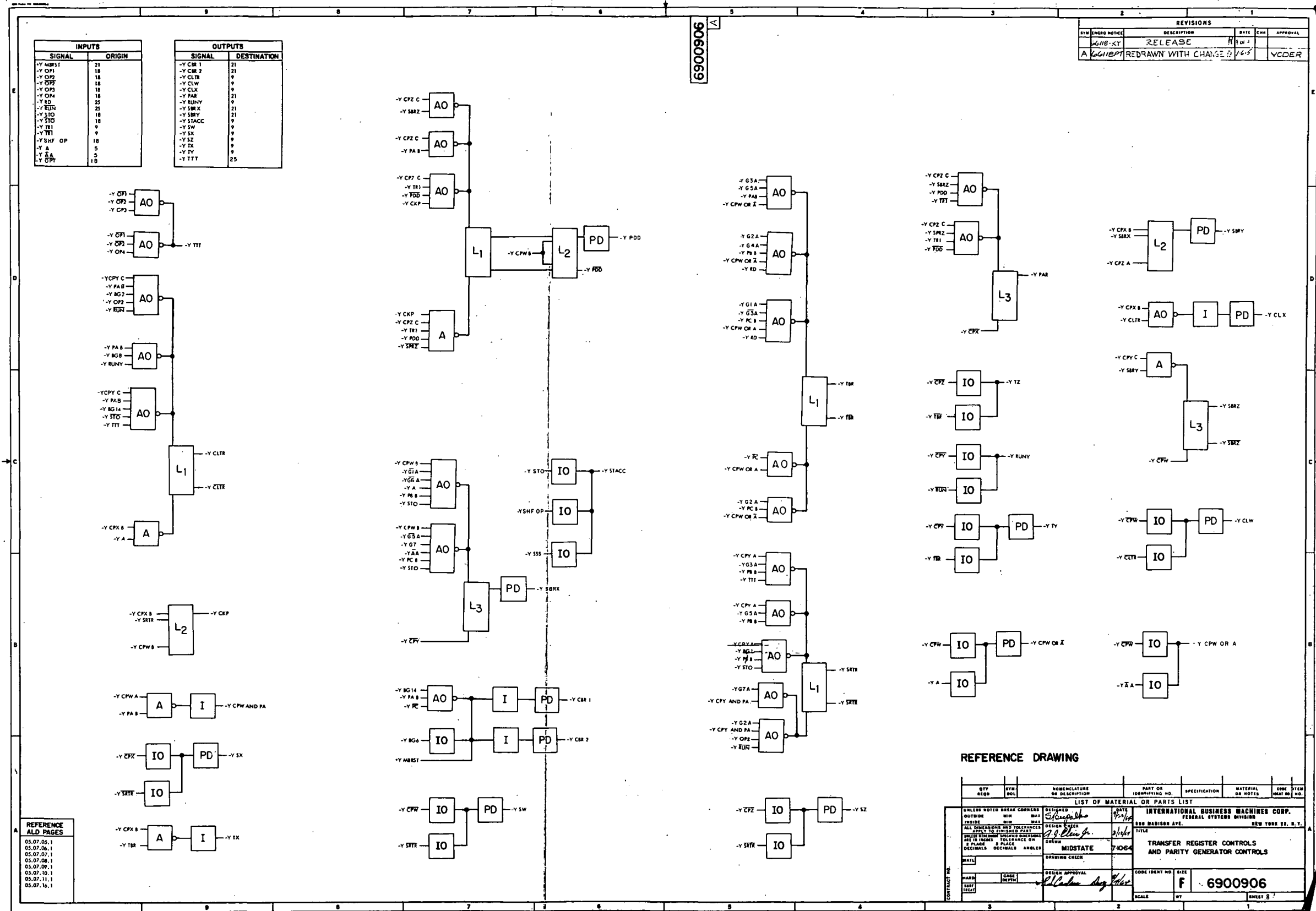


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 8)

V-10-112

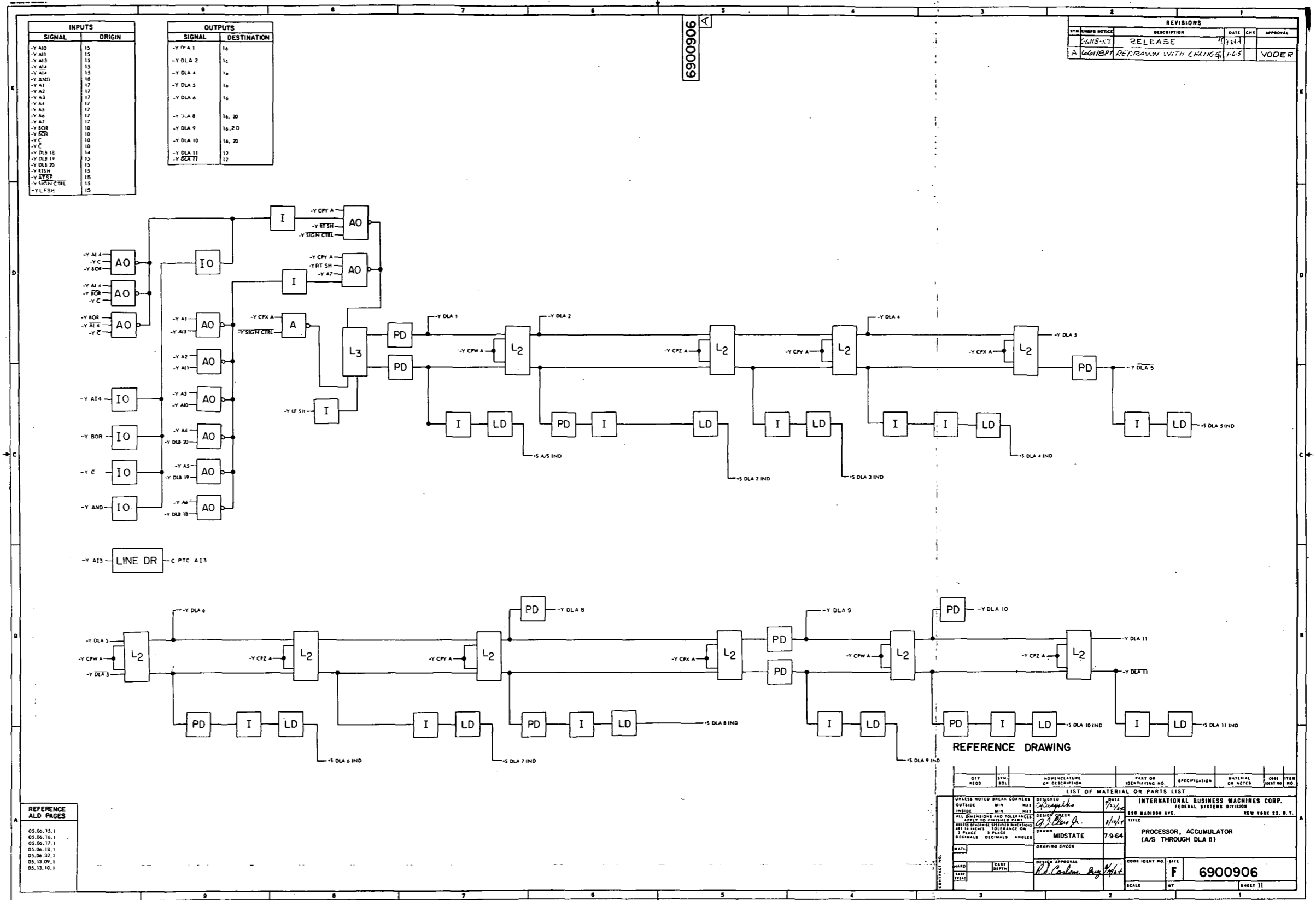
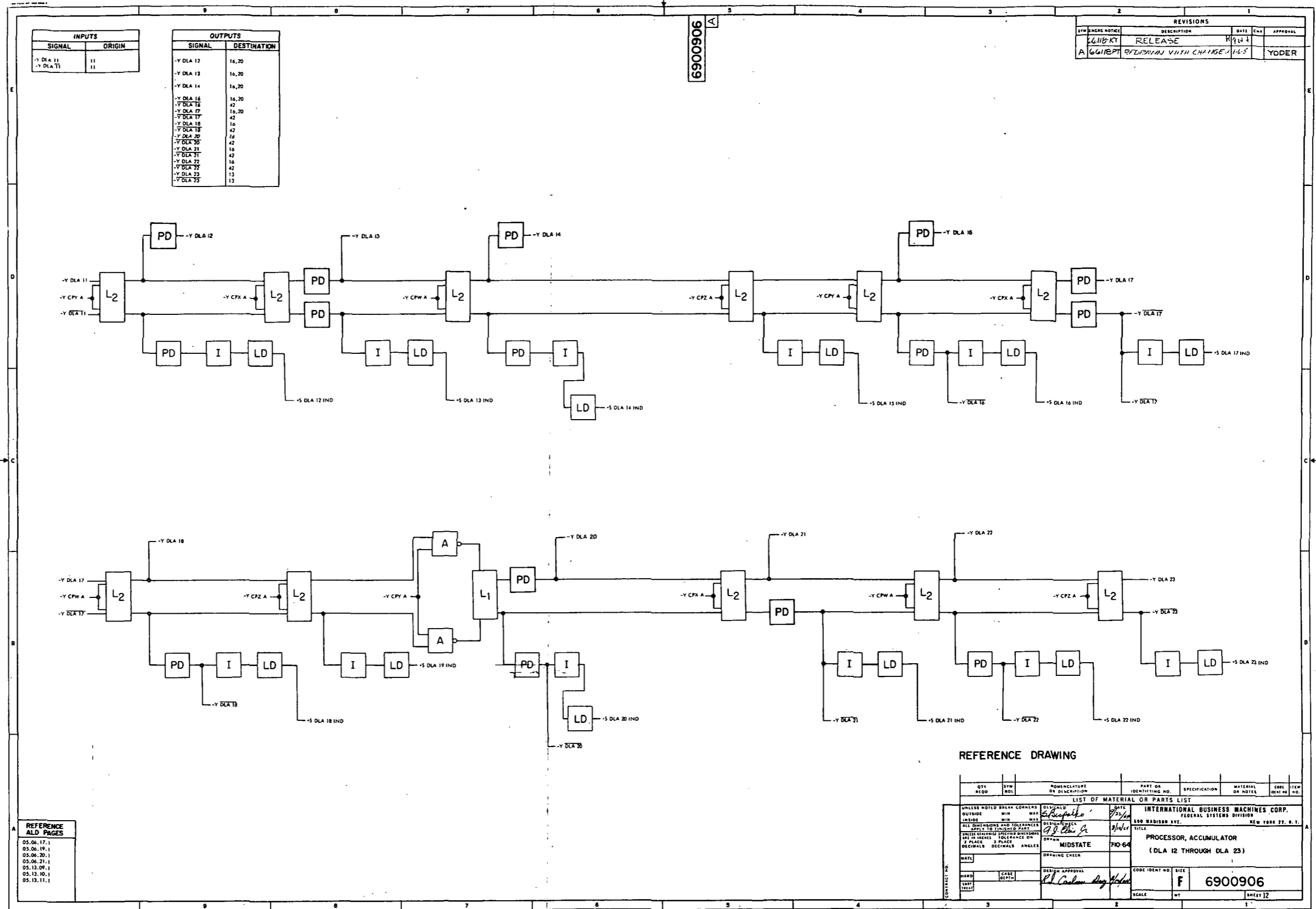


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 11)



REFERENCE A.L.D. PAGES
05.06.17.1
05.06.19.1
05.06.20.1
05.06.21.1
05.13.09.1
05.13.10.1
05.13.11.1

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS							
OUTSIDE	MIN	MAX	DESIGNED BY: <i>E. J. ...</i>				
INSIDE	MIN	MAX	DRAWN BY: <i>J. J. ...</i>				
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART							
UNLESS OTHERWISE SPECIFIED							
FINISH IS BRASS							
TOLERANCE ON 3 PLACES .5 PLACE							
DECIMALS DECIMALS ANGLES							
MATERIAL: MIDSTATE 70-64							
DRAWING CHECK: <i>[Signature]</i>							
DESIGN APPROVAL: <i>[Signature]</i>							
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION							
350 MADISON AVE. NEW YORK 22, N. Y.							
TITLE: PROCESSOR, ACCUMULATOR (DLA 12 THROUGH DLA 23)							
CODE IDENTIFYING NO. F 6900906							
SCALE: WT SHEET 12							

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 12)

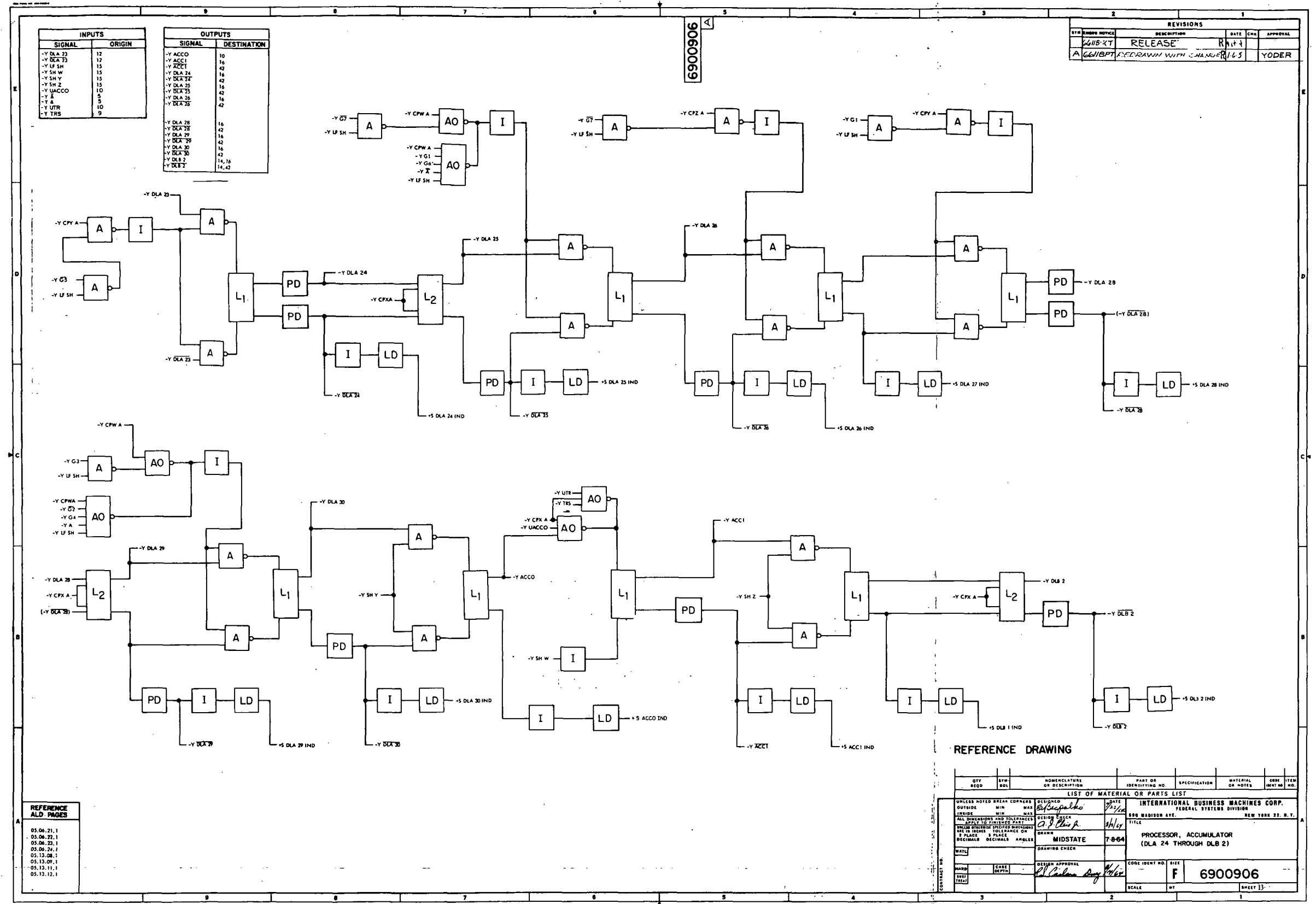
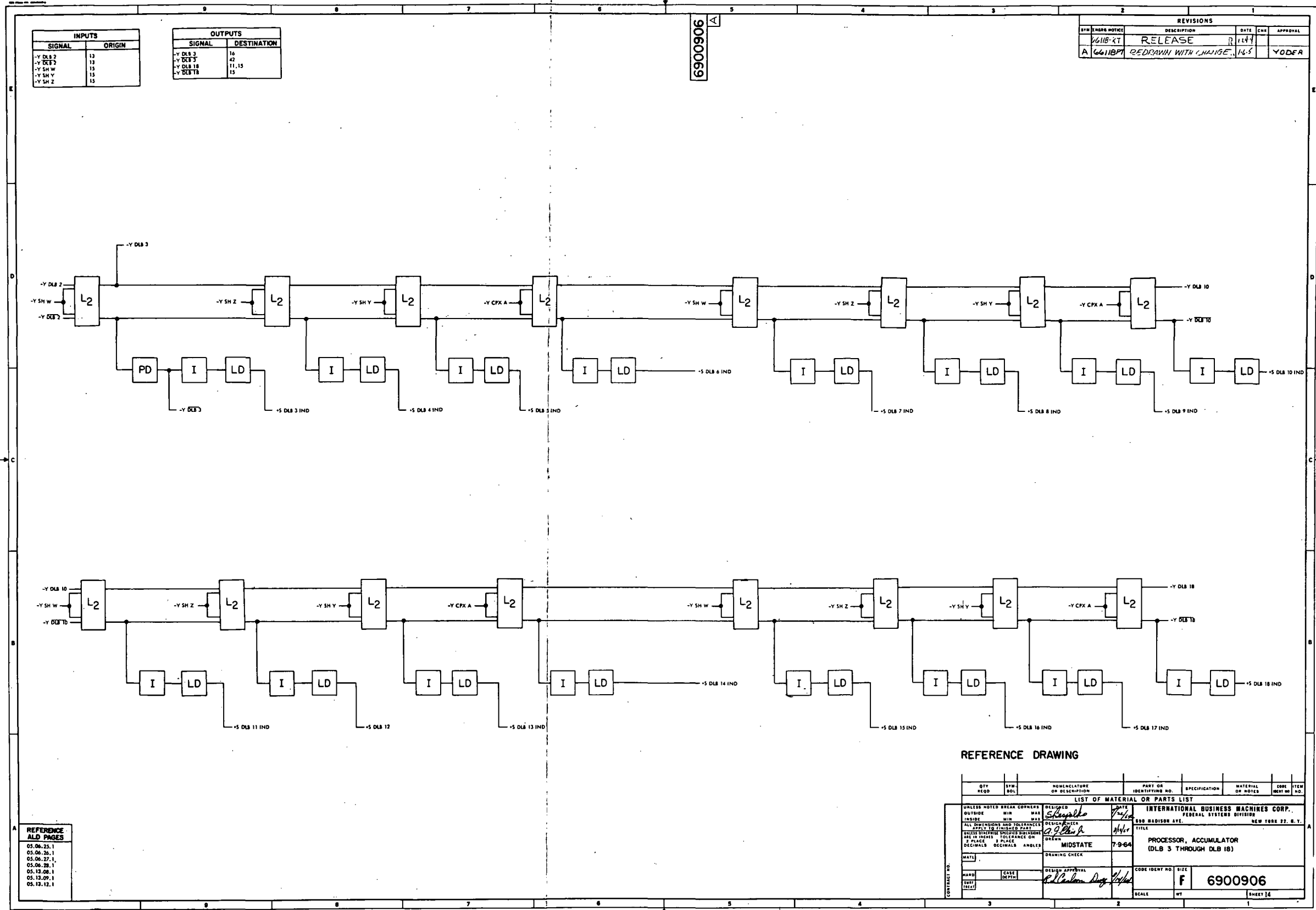


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 13)



INPUTS	
SIGNAL	ORIGIN
-Y DLB 2	13
-Y DLB 7	13
-Y SH W	15
-Y SH Y	15
-Y SH Z	15

OUTPUTS	
SIGNAL	DESTINATION
-Y DLB 3	16
-Y DLB 7	42
-Y DLB 18	11, 15
-Y DLB 7B	15

REVISIONS				
REV	REVISION	DATE	CHK	APPROVAL
1	RELEASE	11/17		
A	REDRAWN WITH CHANGE	11-5		YODFA

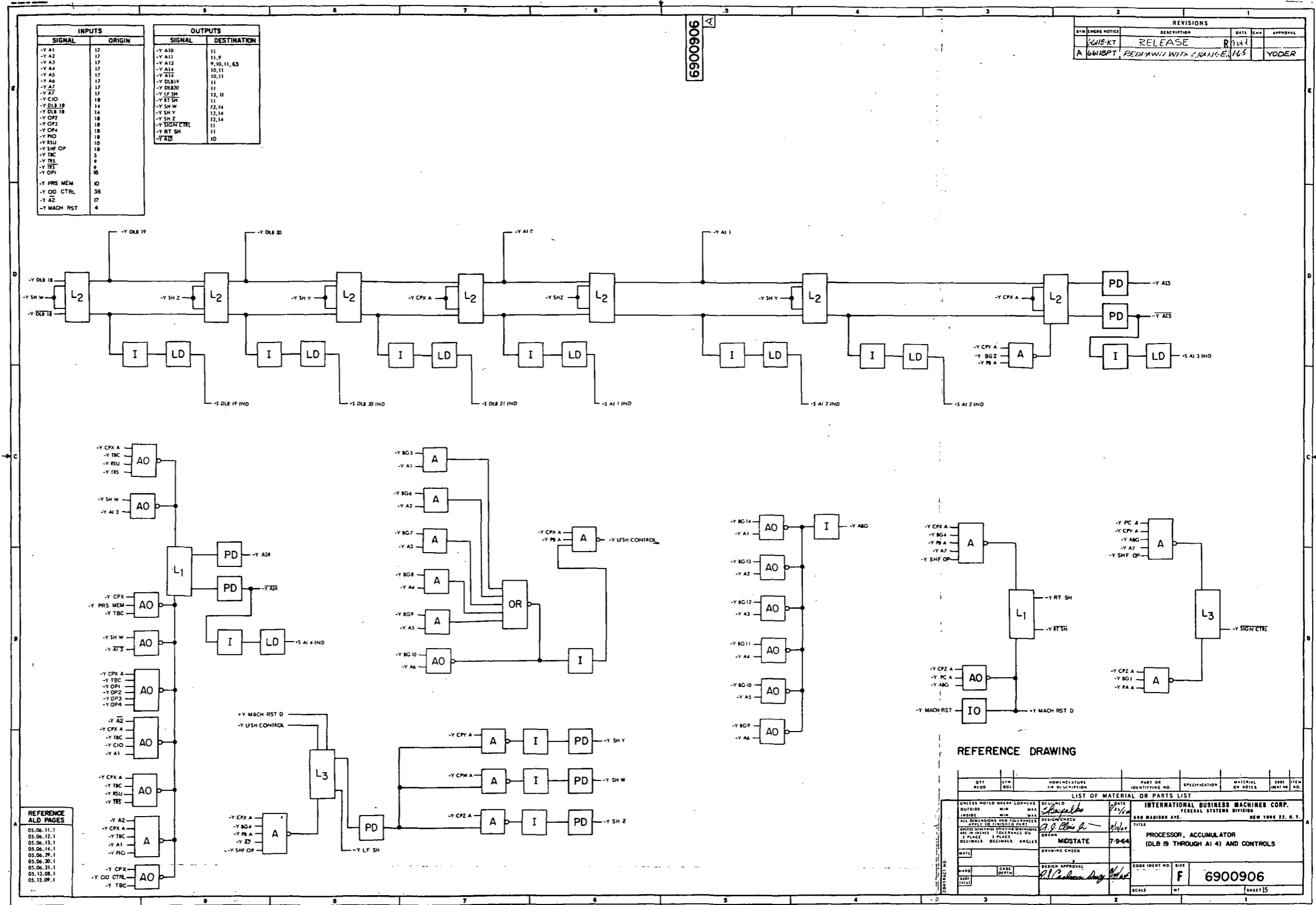
REFERENCE AID PAGES
03.06.25.1
03.06.26.1
03.06.27.1
03.06.28.1
03.12.08.1
03.12.09.1
03.12.12.1

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED	DATE		INTERNATIONAL BUSINESS MACHINES CORP.		
OUTSIDE	MIN	MAX	7/9/64		FEDERAL SYSTEMS DIVISION		
INSIDE	MIN	MAX	7/9/64		800 MADISON AVE. NEW YORK 22, N. Y.		
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART		DESIGNED BY	TITLE		PROCESSOR, ACCUMULATOR		
SMALL DIMENSIONS SHOULD BE OBSERVED		2. J. Blum	MIDSTATE		(DLB 3 THROUGH DLB 18)		
SEE IN INCHES TOLERANCE ON 3 PLACE DECIMALS DECIMALS ANGLES		DRAWN BY	7-9-64		DRAWING CHECK		
MATERIAL		DESIGN APPROVAL		CODE IDENT NO.		SIZE	
HAND		K. L. Cantor		F		6900906	
TEMP		DATE		SCALE		WT	
TEST						SHEET 14	

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 14)

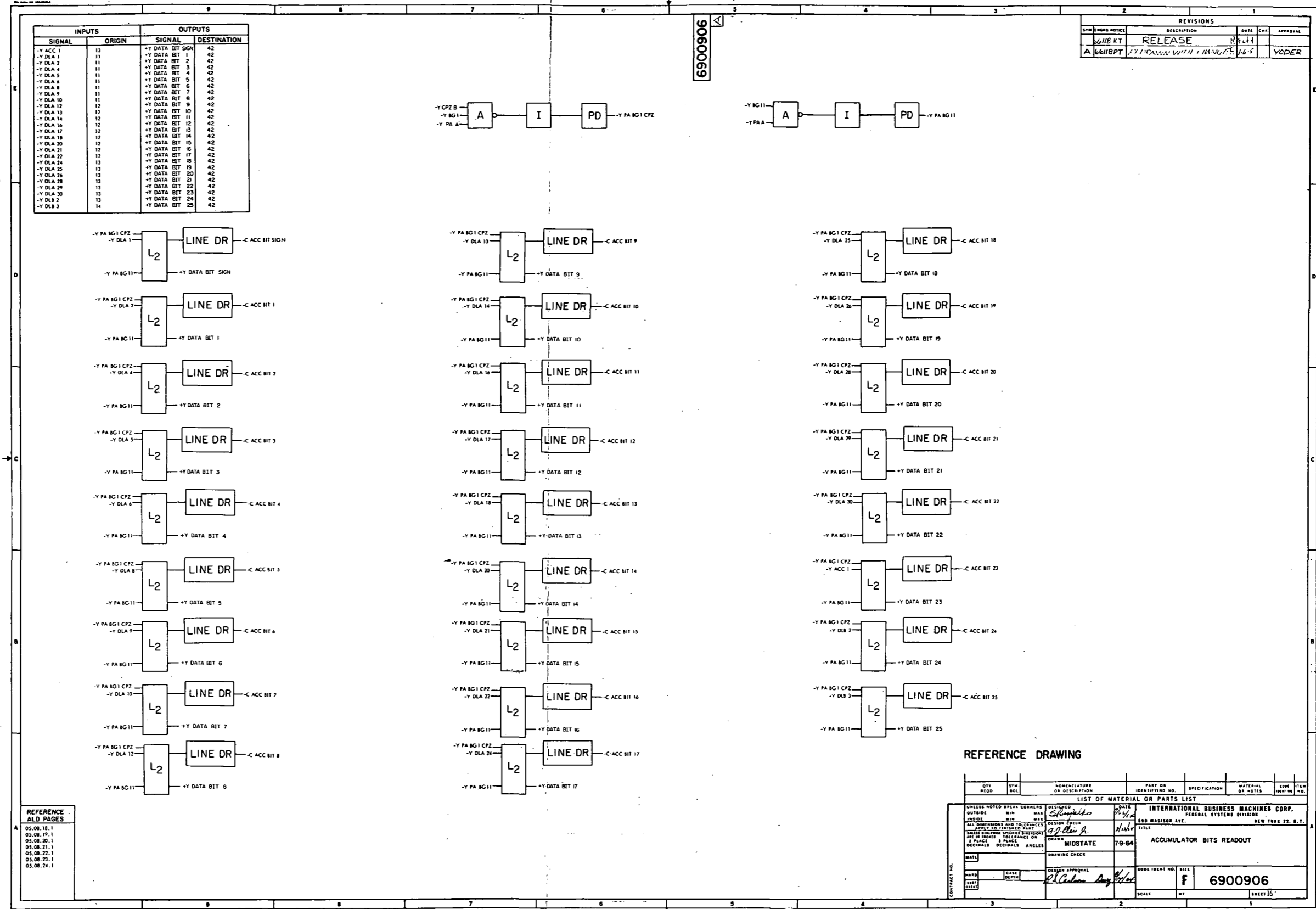
V-10-118



REFERENCE DRAWING

QTY	REV	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL	UNIT	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED WHEN LOANED TO OUTSIDE				INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION			
ALL DIMENSIONS AND TOLERANCES SHALL BE IN INCHES UNLESS OTHERWISE SPECIFIED				350 MADISON AVE. NEW YORK 22, N. Y.			
FRACTIONS SHALL BE IN INCHES UNLESS OTHERWISE SPECIFIED				TITLE: PROCESSOR, ACCUMULATOR (DLB 19 THROUGH A1 4) AND CONTROLS			
DECIMALS SHALL BE IN INCHES UNLESS OTHERWISE SPECIFIED				DRAWING NO. 7-964			
MATERIAL				DRAWING CHECK			
HARD COPY				DESIGN APPROVAL			
SCALE				CODE IDENT NO. B16			
				F 6900906			
				SHEET 15			

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 15)



6900906

REVISIONS				
SYM	ENG/GR	NOTICE	DESCRIPTION	DATE
			RELEASE	8/11
A	66118BPT		17110000 WITH 11/11/64	11/65
				YODER

REFERENCE - AID PAGES	
A	05.08.18.1
	05.08.19.1
	05.08.20.1
	05.08.21.1
	05.08.22.1
	05.08.23.1
	05.08.24.1

REFERENCE DRAWING

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.
LIST OF MATERIAL OR PARTS LIST						
UNLESS NOTED BY** CORNERS		DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP.		
OUTSIDE	MIN	MAX	8/11/64	FEDERAL SYSTEMS DIVISION		
INSIDE	MIN	MAX		500 MADISON AVE. NEW YORK 22, N. Y.		
ALL DIMENSIONS AND TOLERANCES		DESIGN CHECK		TITLE		
PER THE DIMENSIONAL SYSTEM		9/1/64		ACCUMULATOR BITS READOUT		
SMALL DIMENSIONS UNLESS OTHERWISE SPECIFIED		DRAWN	7-9-64	MIDSTATE		
1/8 PLACE 3 PLACE DECIMALS		DRAWING CHECK		SCALE		
DECIMALS ANGLES		DESIGN APPROVAL		CODE IDENT NO. SIZE		
		R. J. ...		F 6900906		
				SCALE WT. SHEET 16		

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 16)

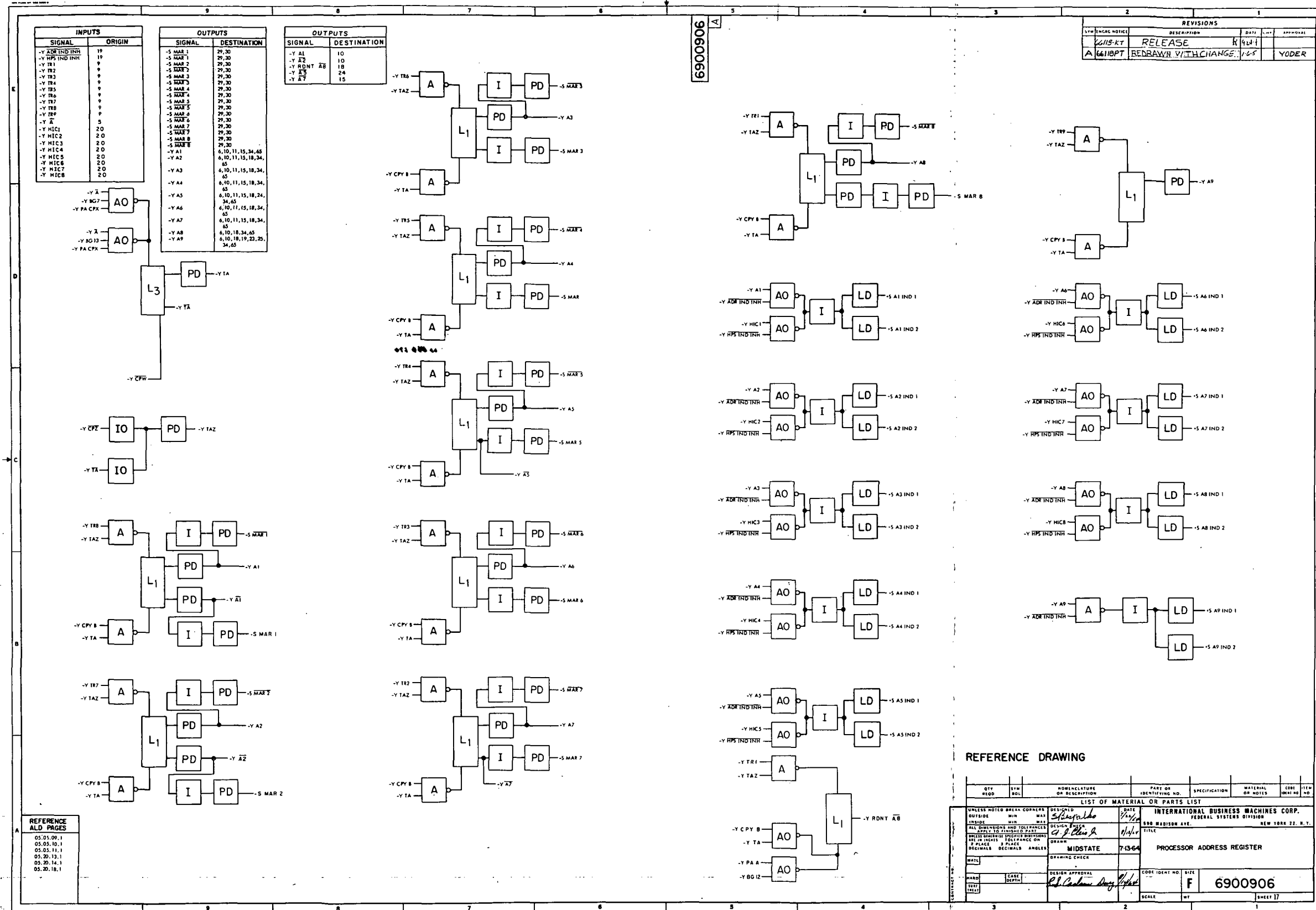


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 17)

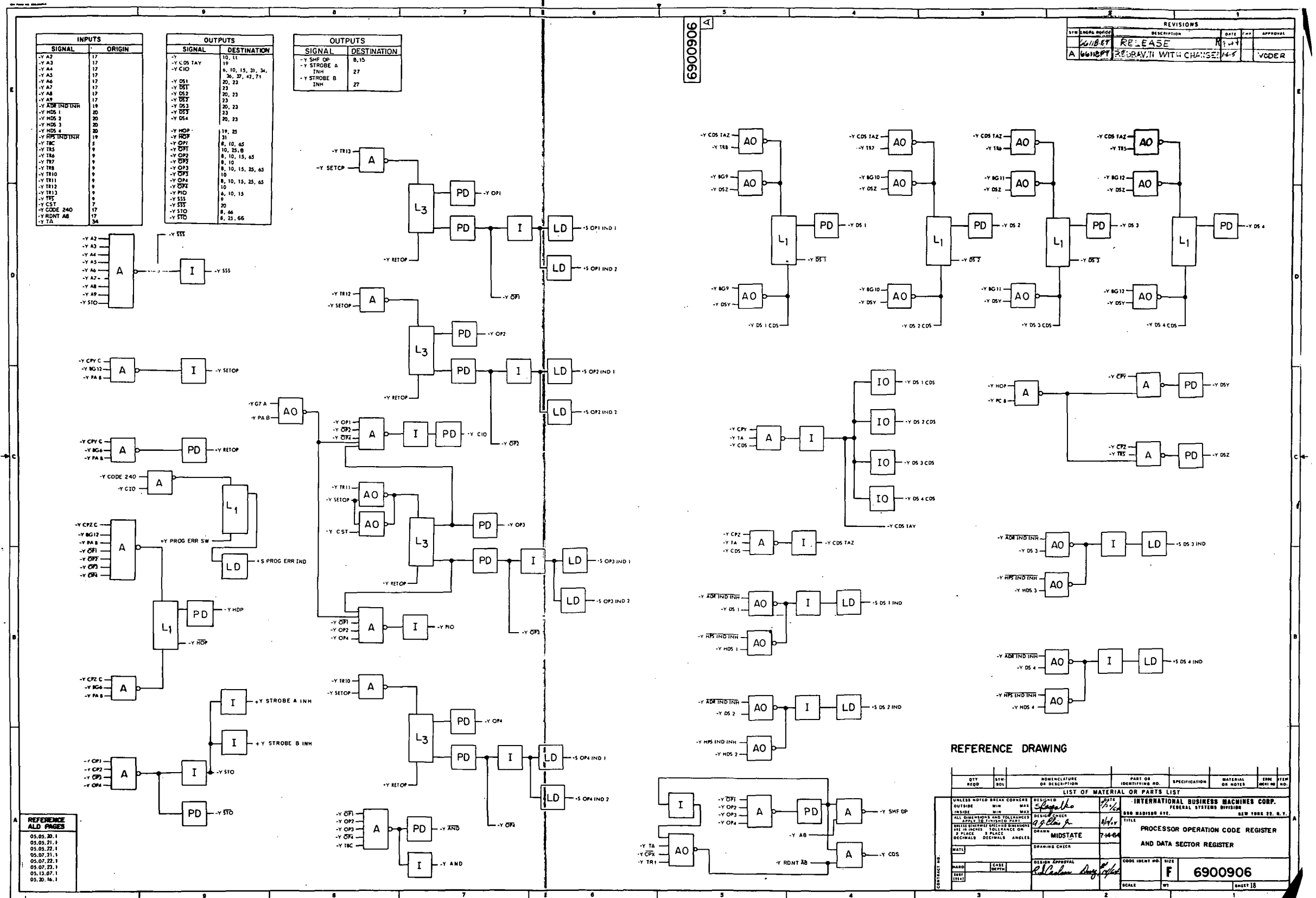


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 18)

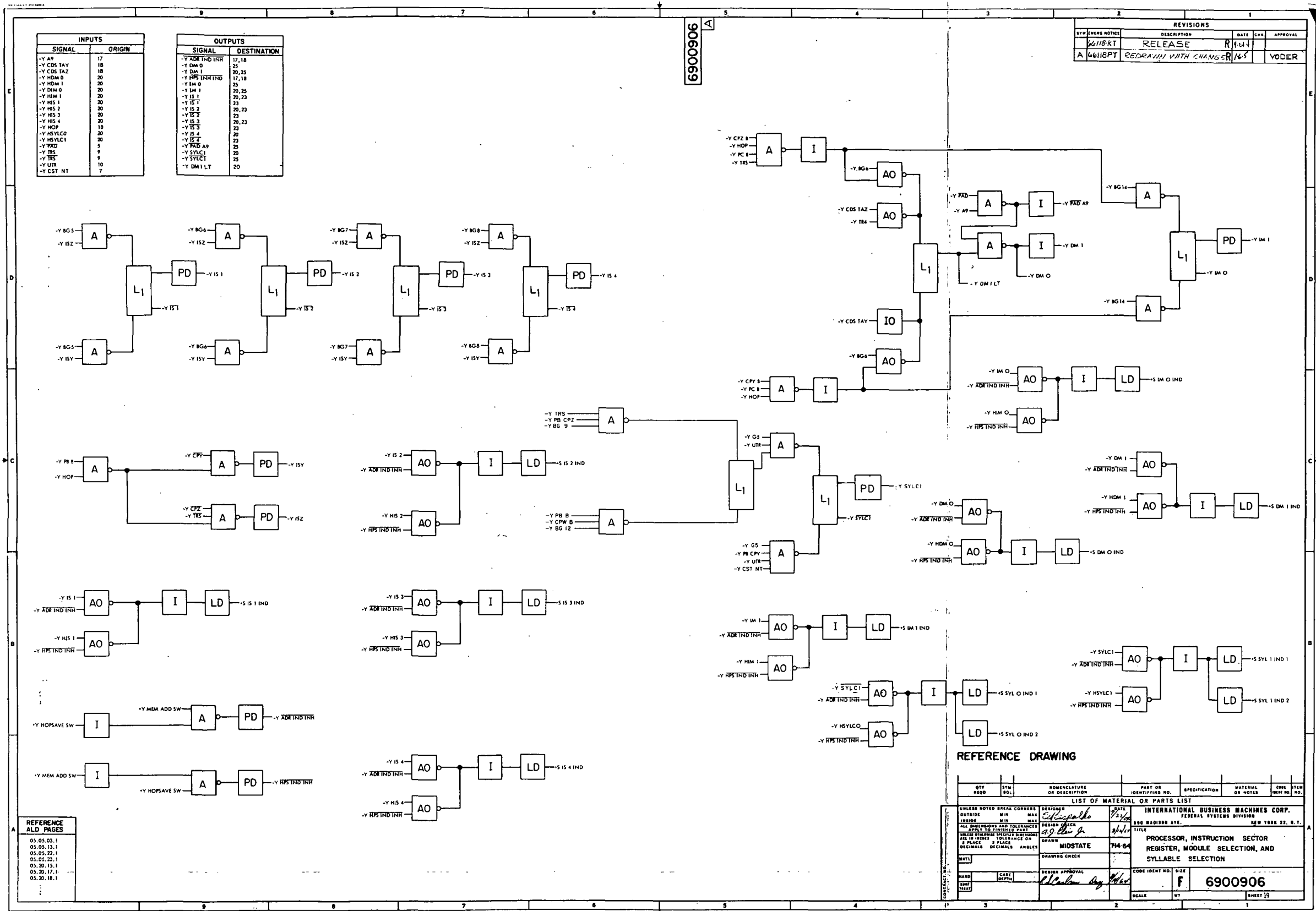


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 19)

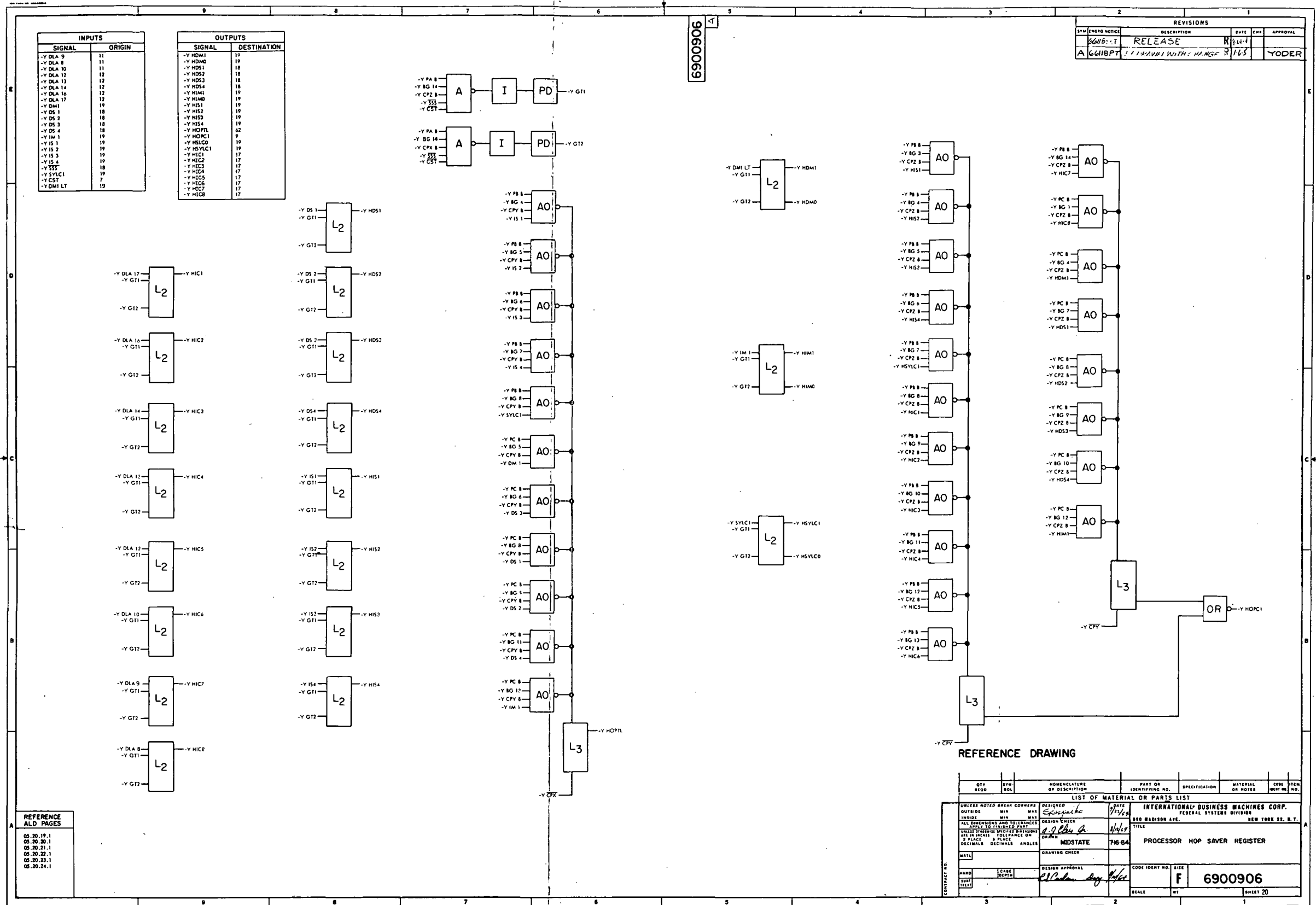


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 20)

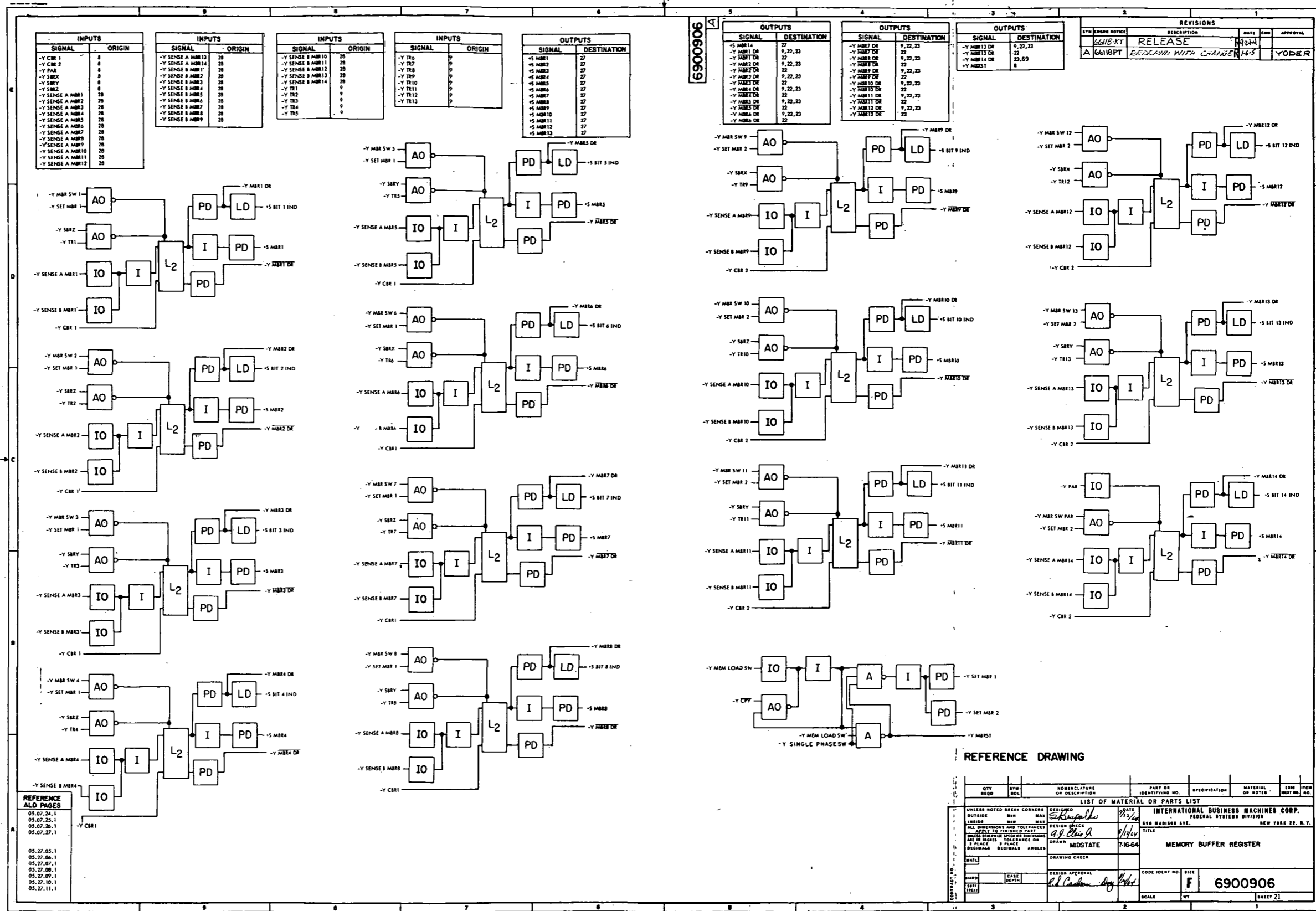


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 21)

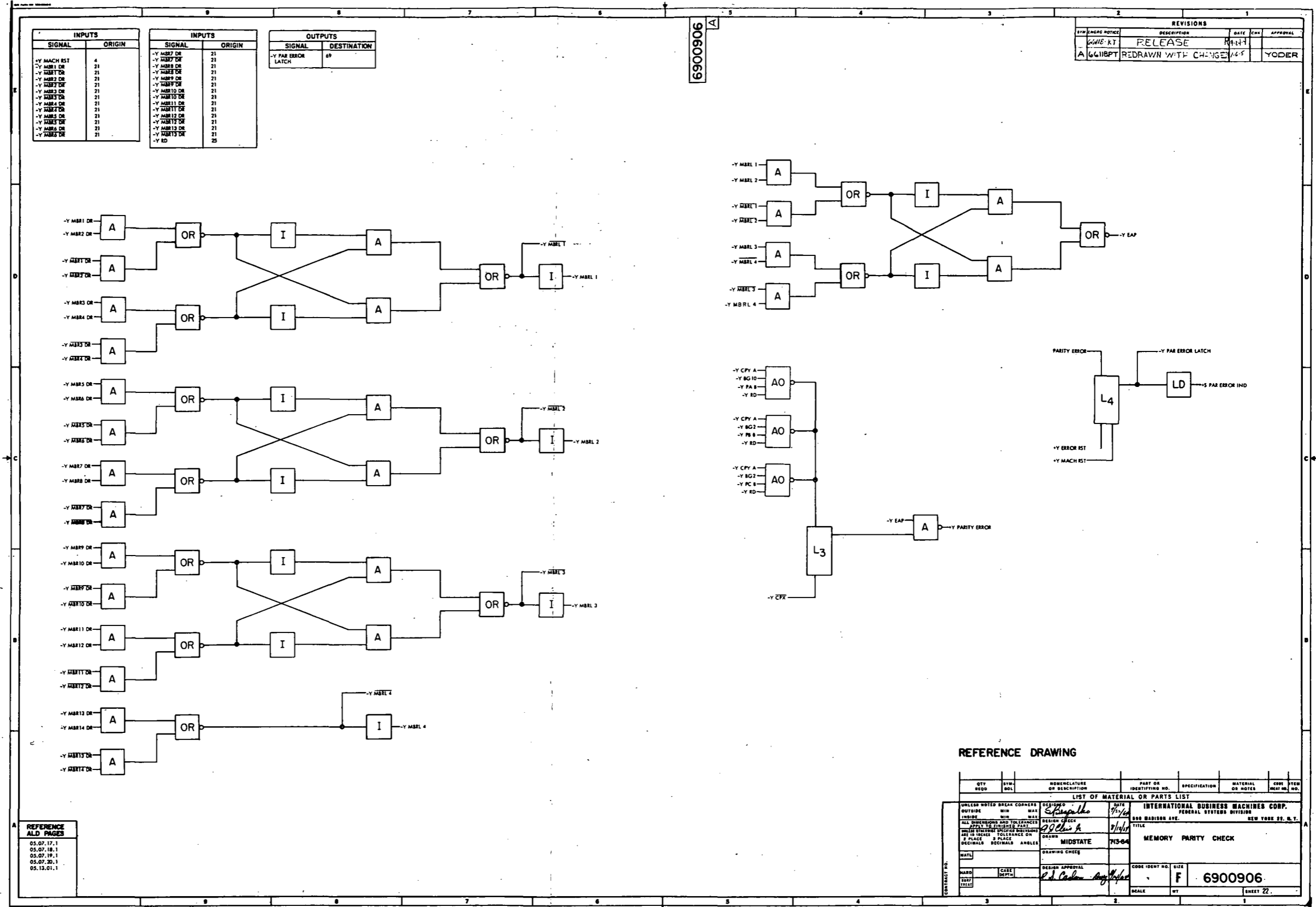


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 22)

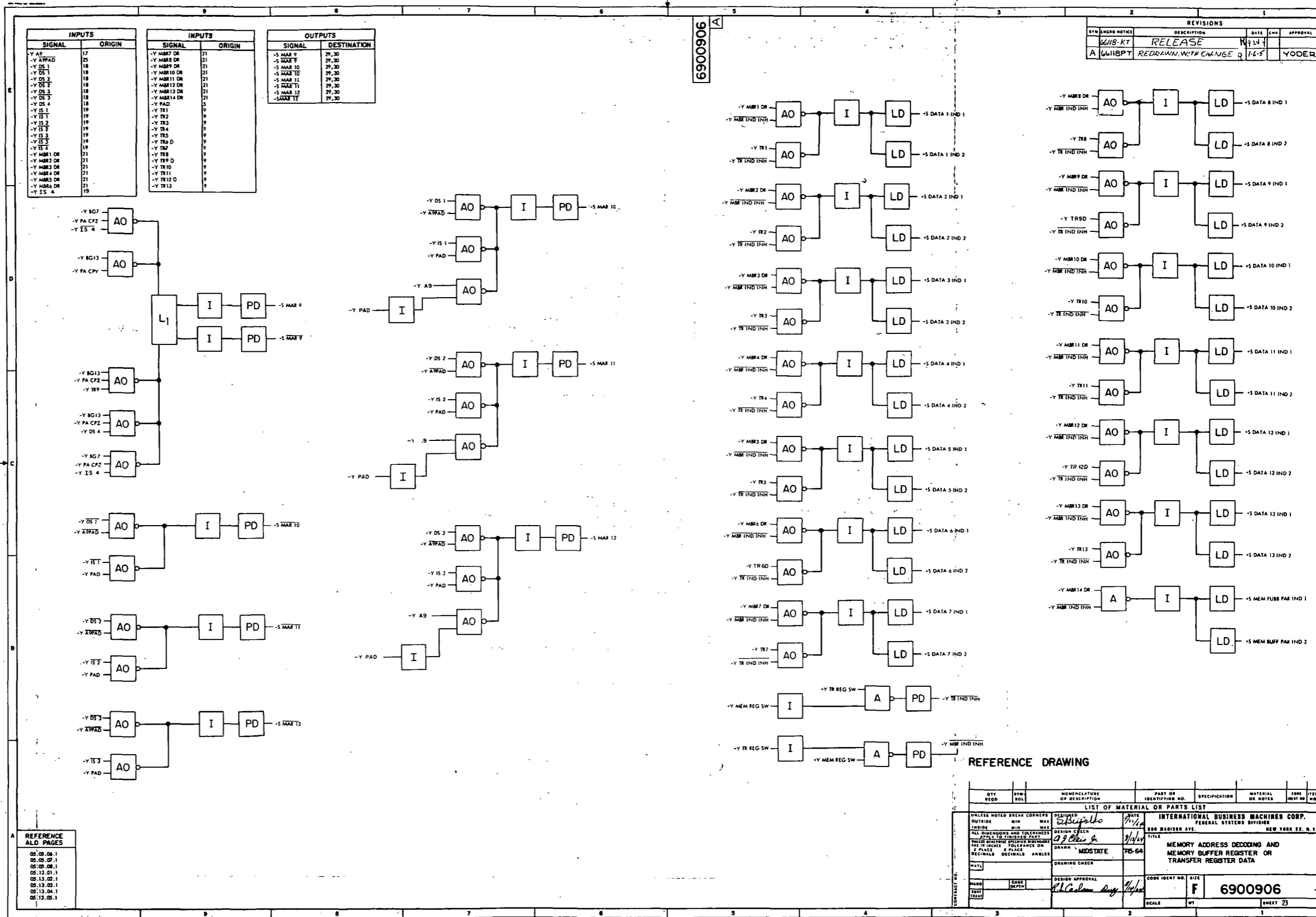


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 23)

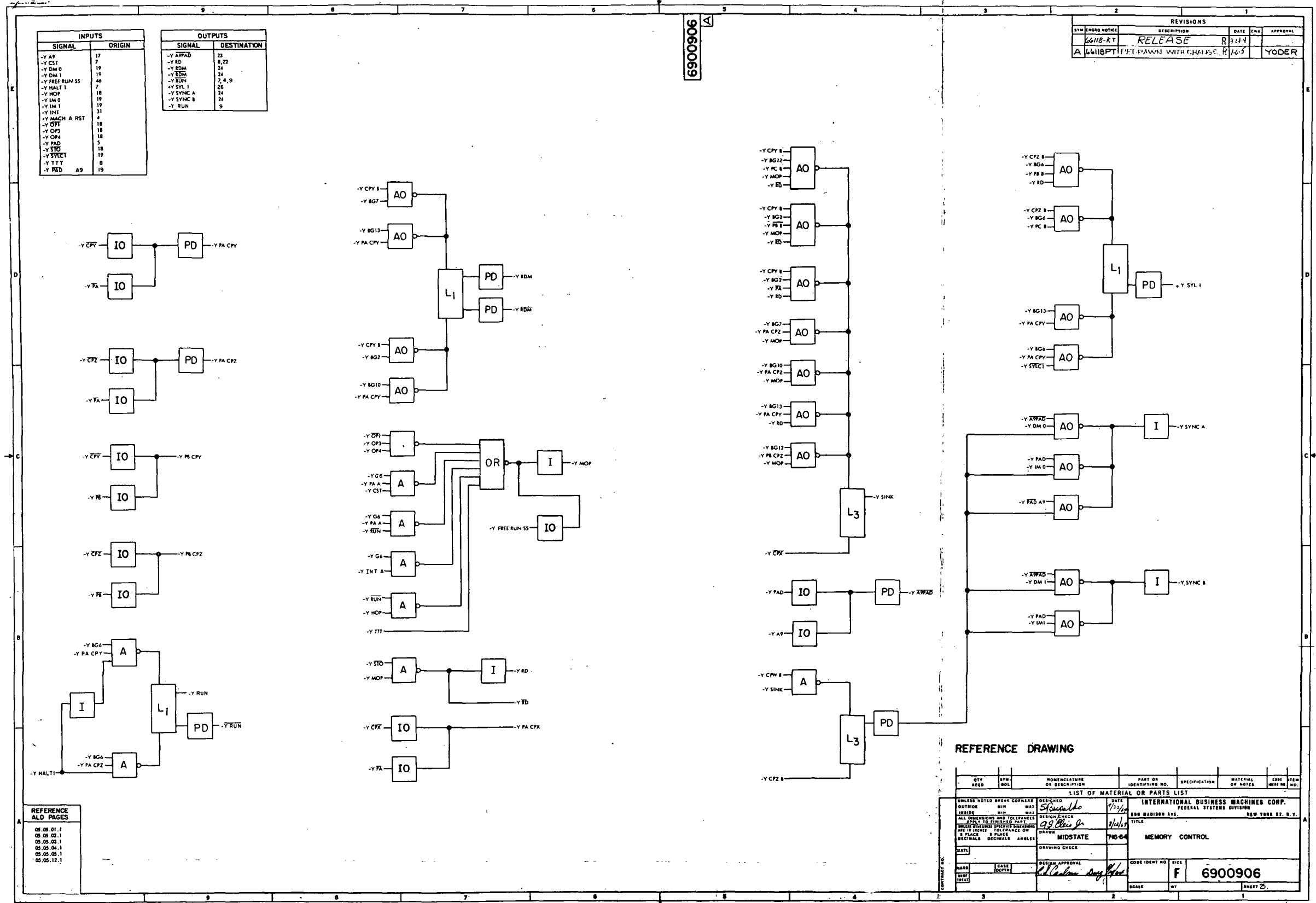


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 25)

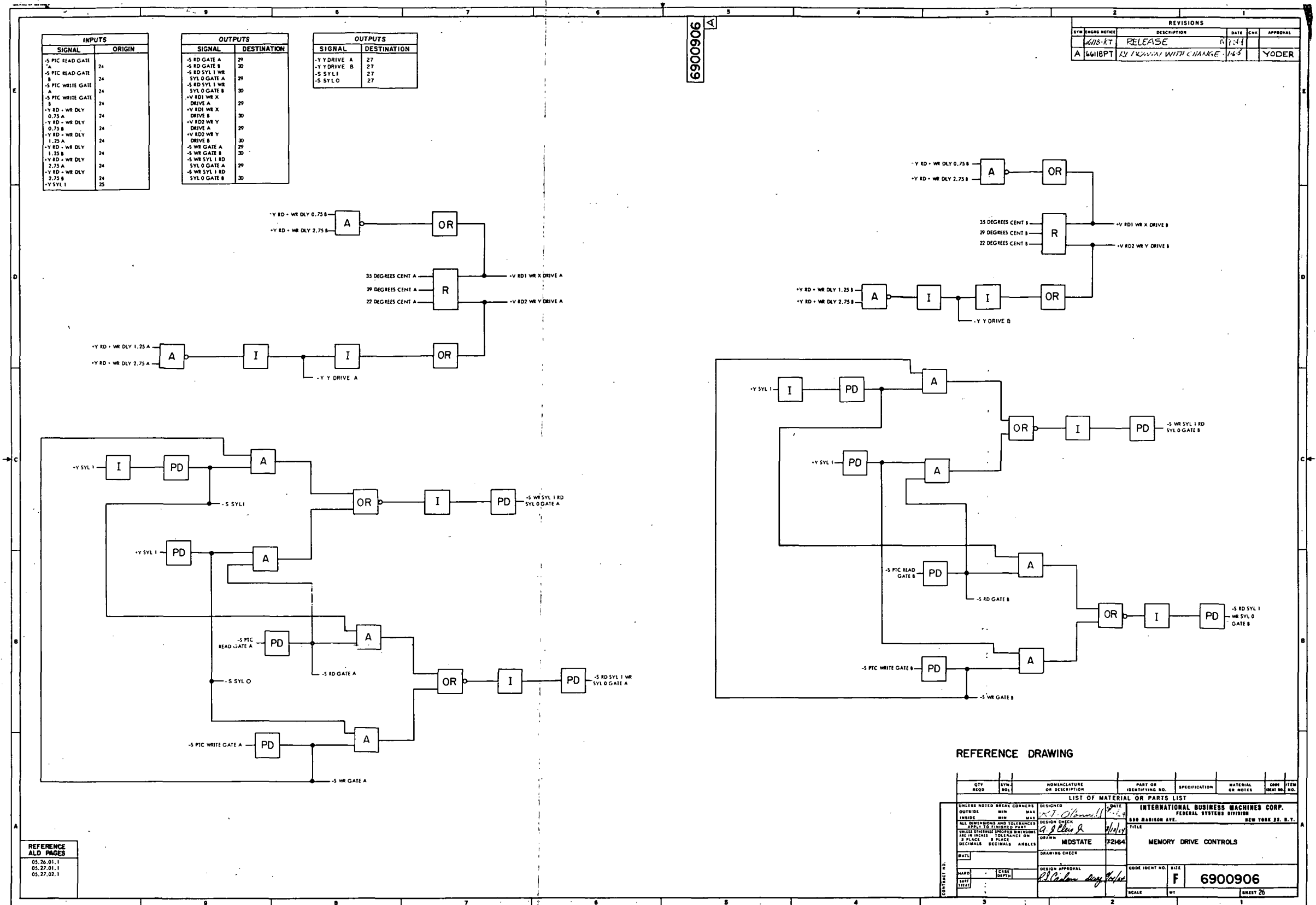


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 26)

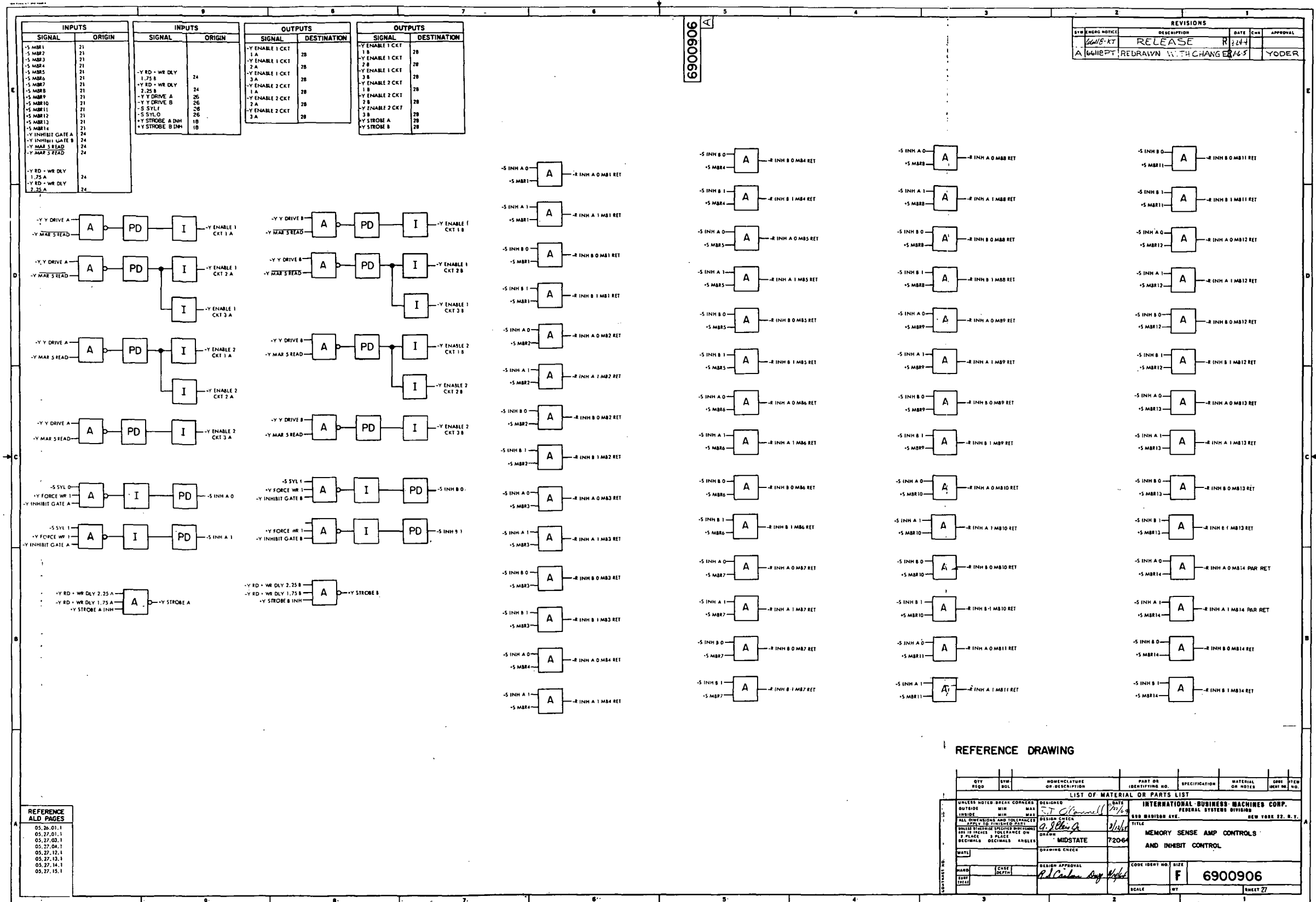


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 27)

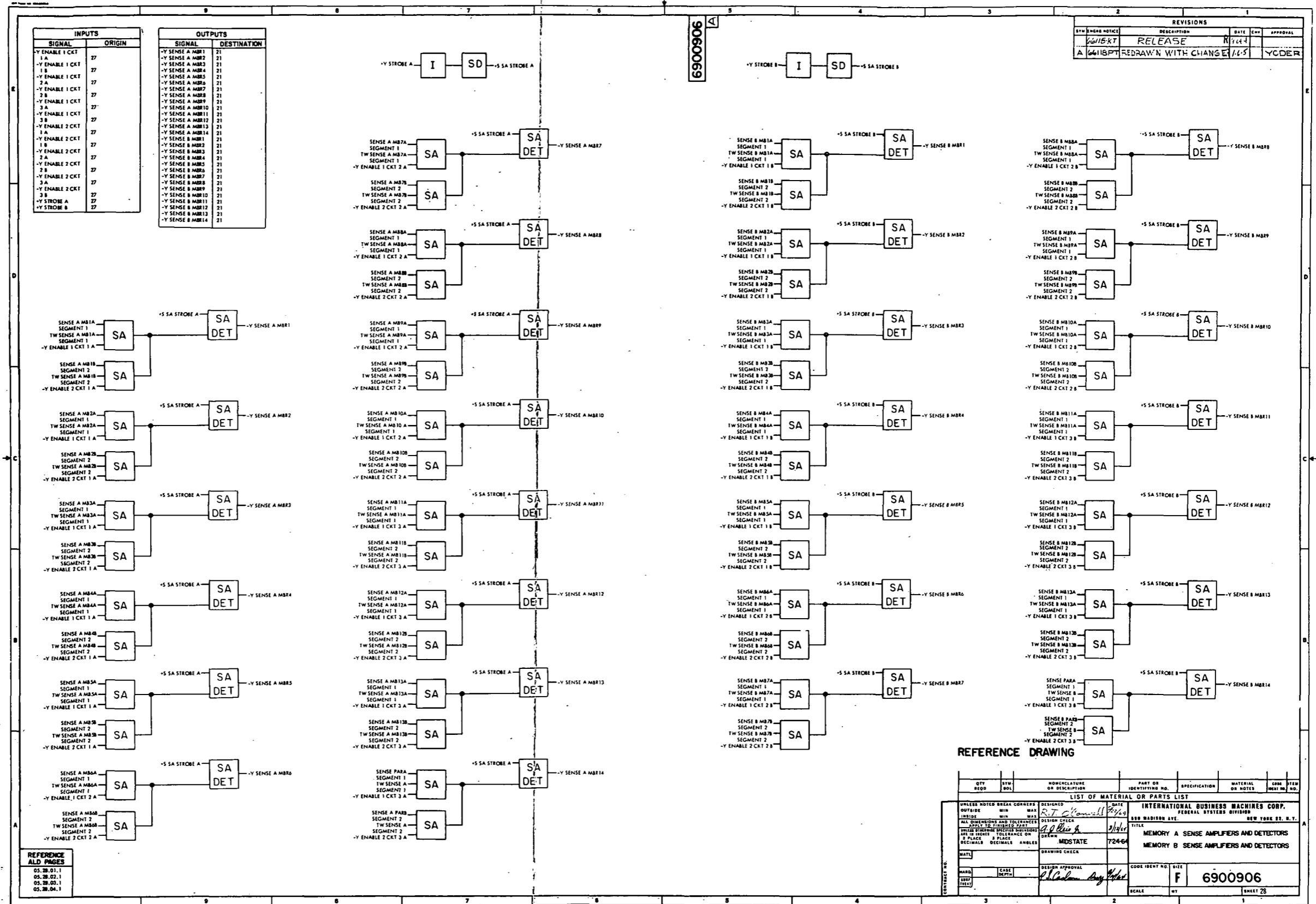


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 28)

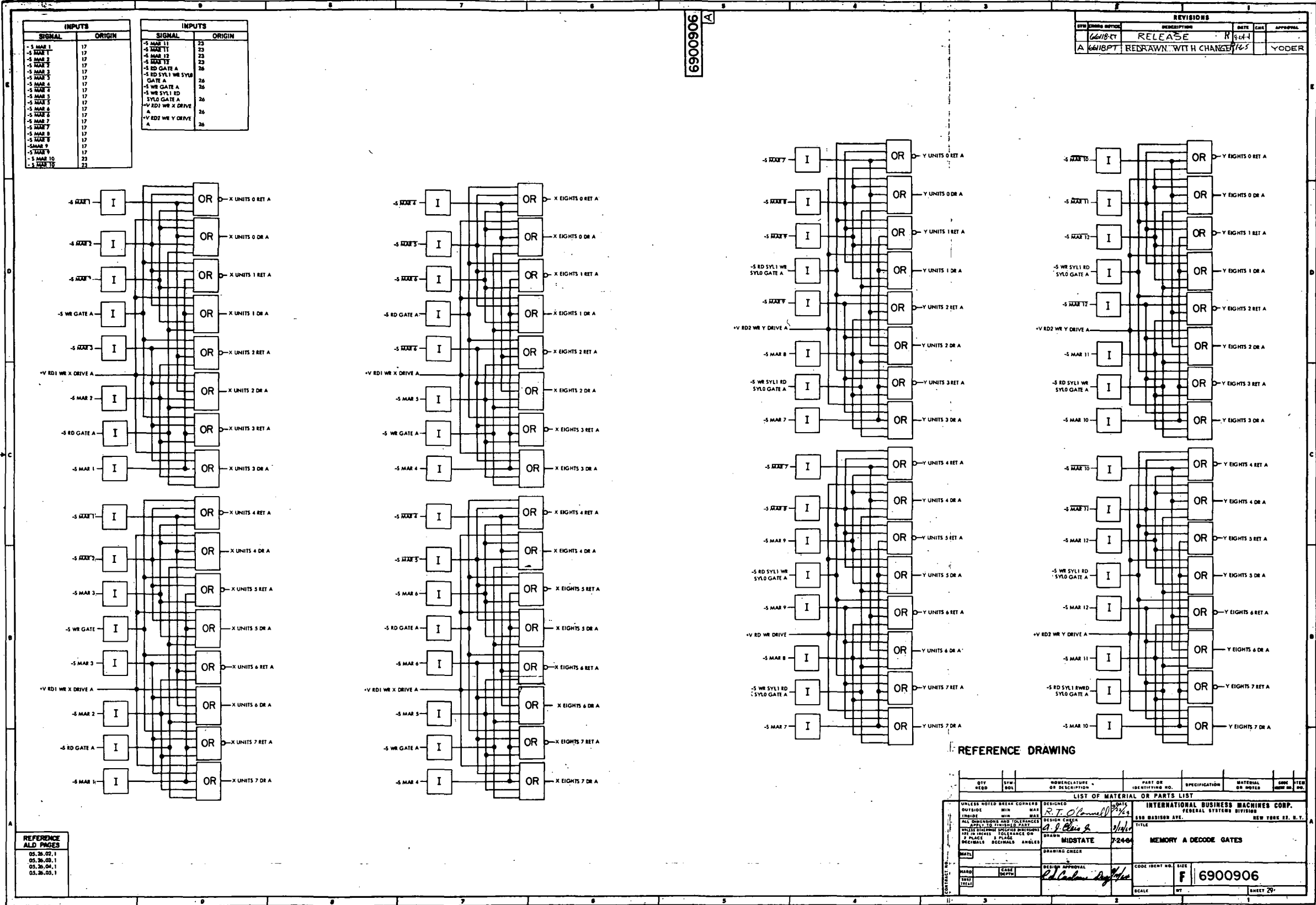


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 29)

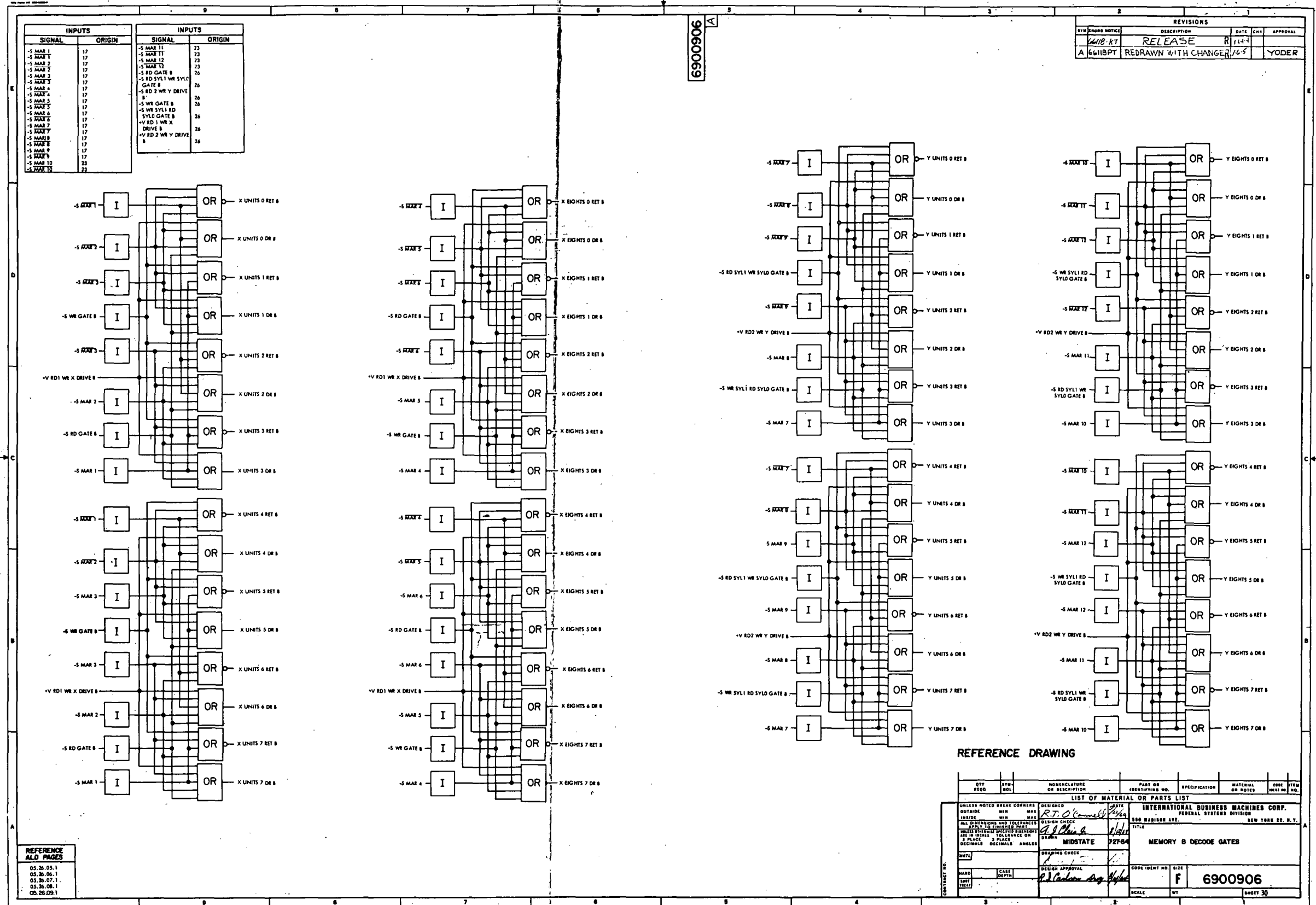


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 30)

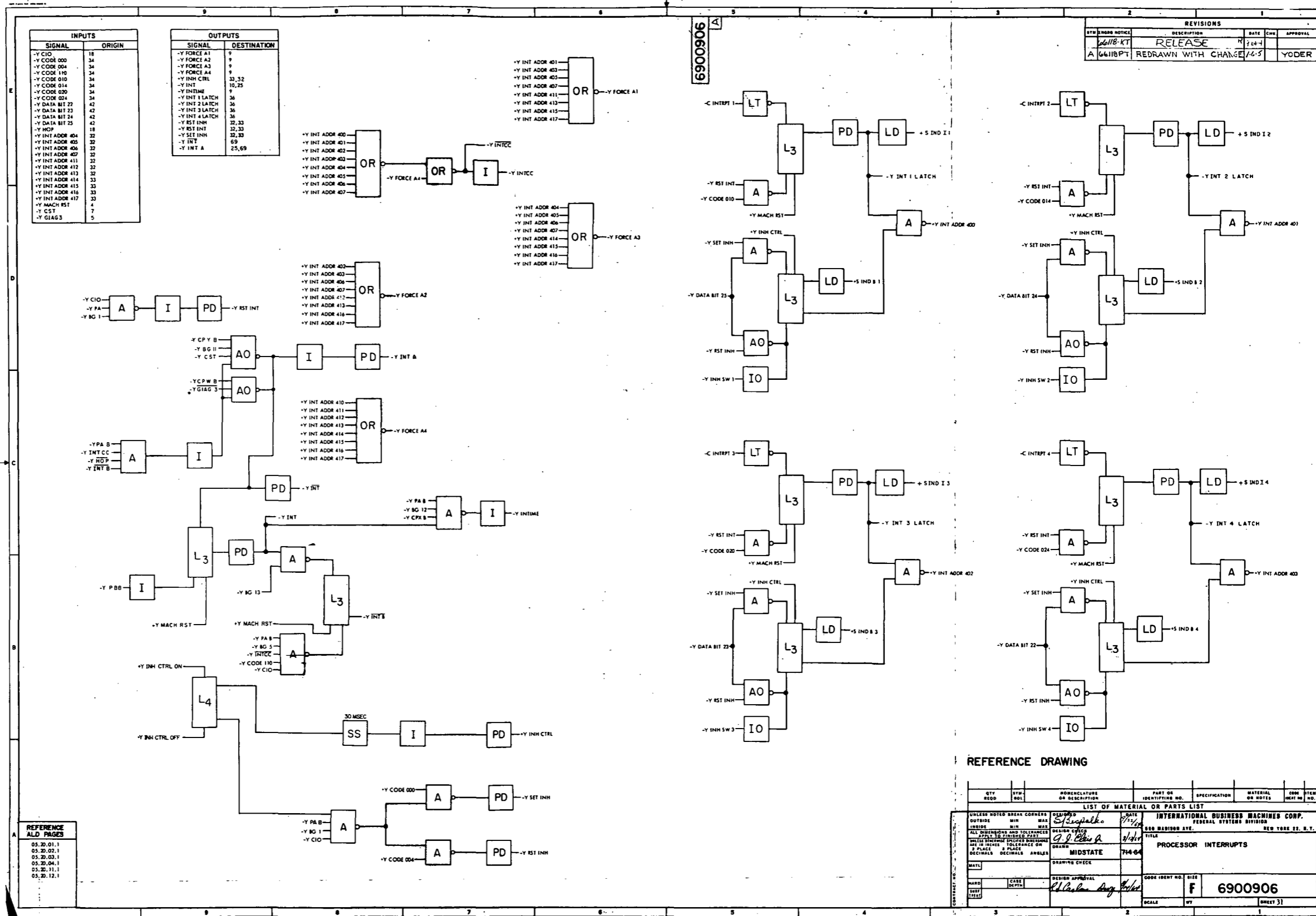


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 31)

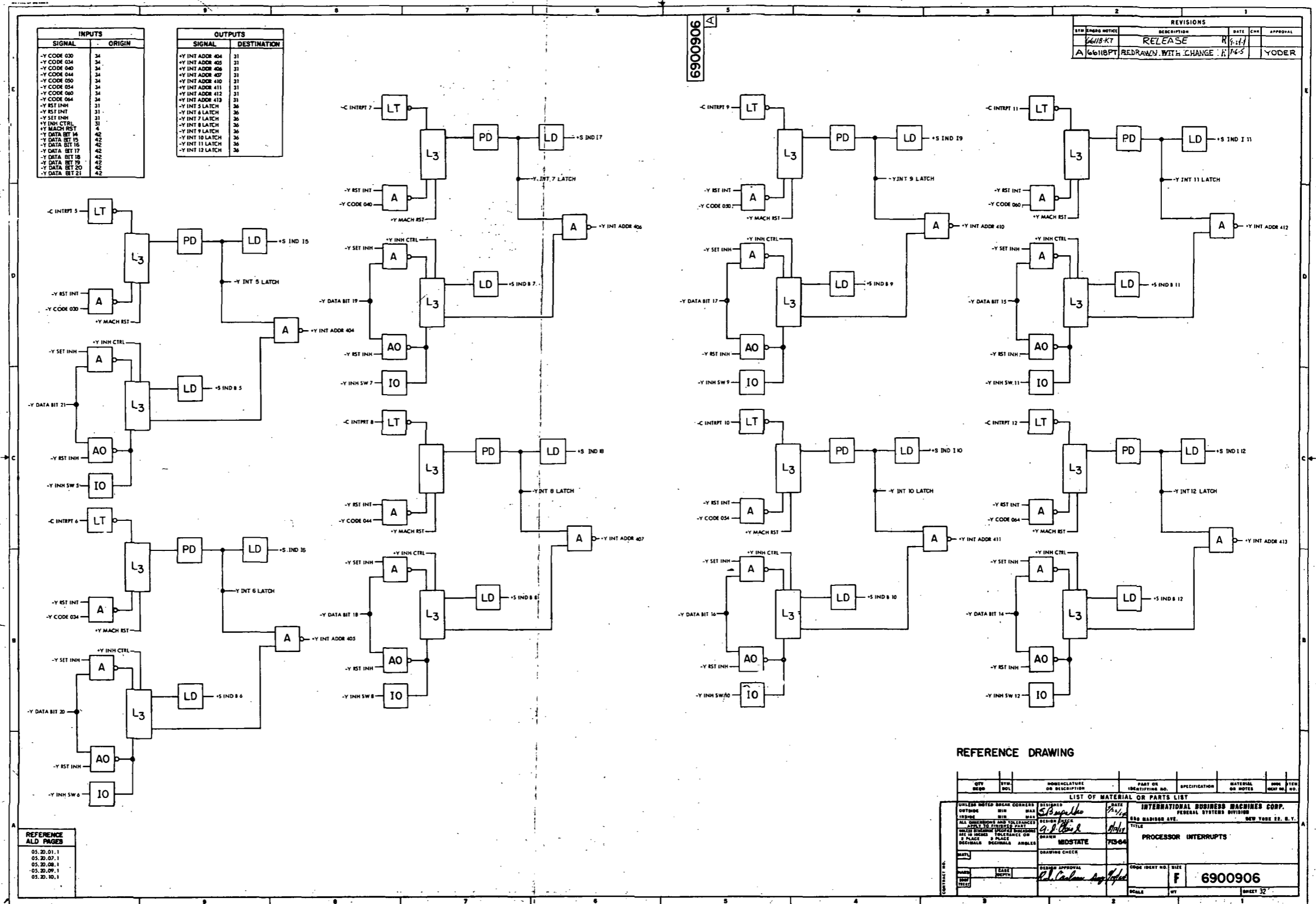
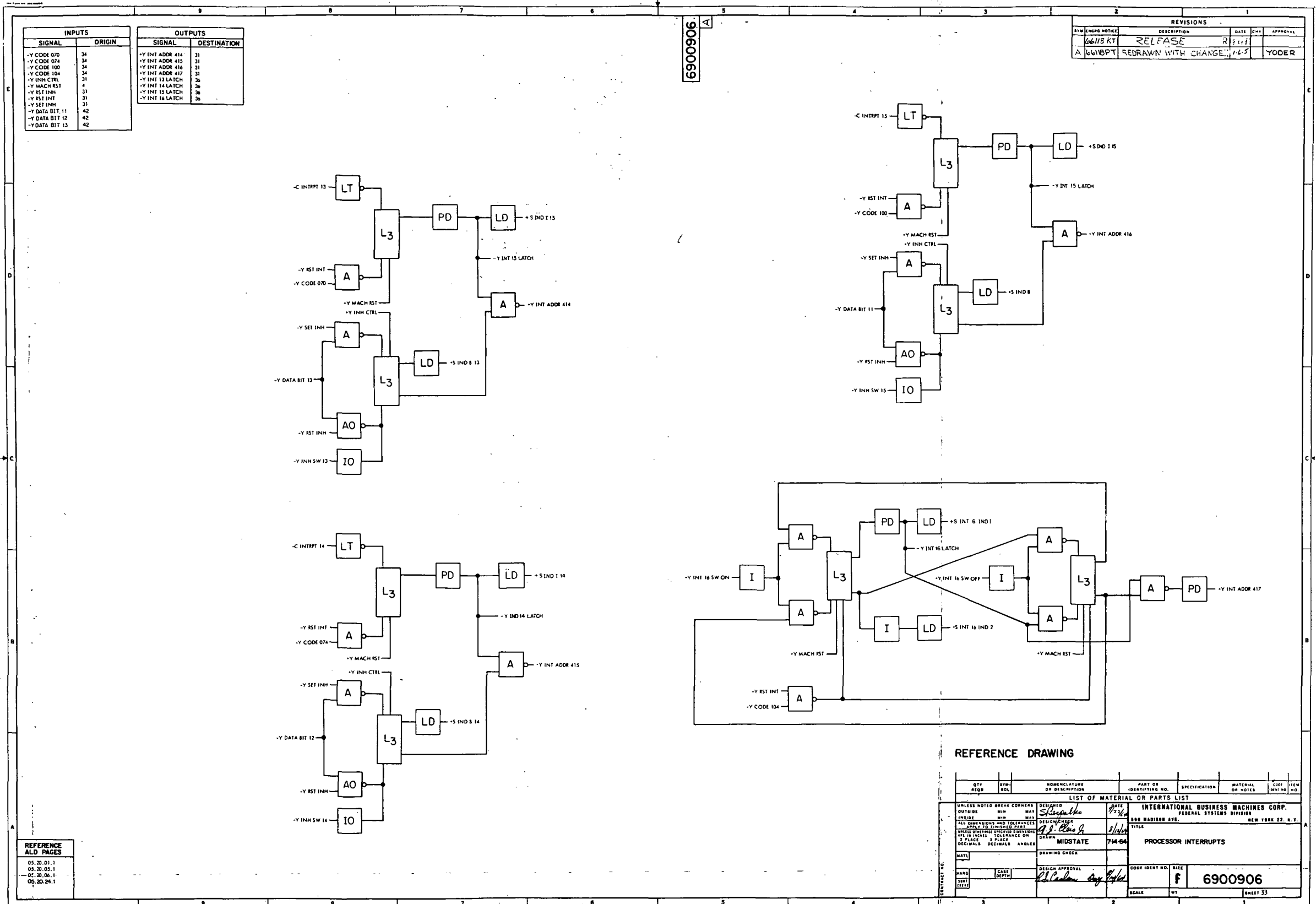


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 32)



INPUTS		OUTPUTS	
SIGNAL	ORIGIN	SIGNAL	DESTINATION
-Y CODE 070	34	-Y INT ADDR 414	31
-Y CODE 074	34	-Y INT ADDR 415	31
-Y CODE 100	34	-Y INT ADDR 416	31
-Y CODE 104	34	-Y INT ADDR 417	31
-Y INH CTRL	31	-Y INT 13 LATCH	36
-Y MACH RST	4	-Y INT 14 LATCH	36
-Y RST INH	31	-Y INT 15 LATCH	36
-Y RST INT	31	-Y INT 16 LATCH	36
-Y SET INH	31	-Y INT 13 LATCH	36
-Y DATA BIT 11	42	-Y INT 14 LATCH	36
-Y DATA BIT 12	42		
-Y DATA BIT 13	42		

REVISIONS				
BY	DATE	DESCRIPTION	CHK	APPROVAL
66118 KT	12/11/63	RELEASE		
A 66118 PPT		REDRAWN WITH CHANGE...		YODER

DATE	DESCRIPTION
05.20.01.1	
05.20.05.1	
02.20.06.1	
05.20.24.1	

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX							
INSIDE MIN MAX							
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART							
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 3 PLACES DECIMALS DECIMALS ANGLES							
DRAWN MIDSTATE 7/14-64							
PROCESSOR INTERRUPTS							
DRAWING CHECK							
DESIGN APPROVAL							
CODE IDENT NO. SIZE F 6900906							
SCALE 1"=1"							
SHEET 33							

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 33)

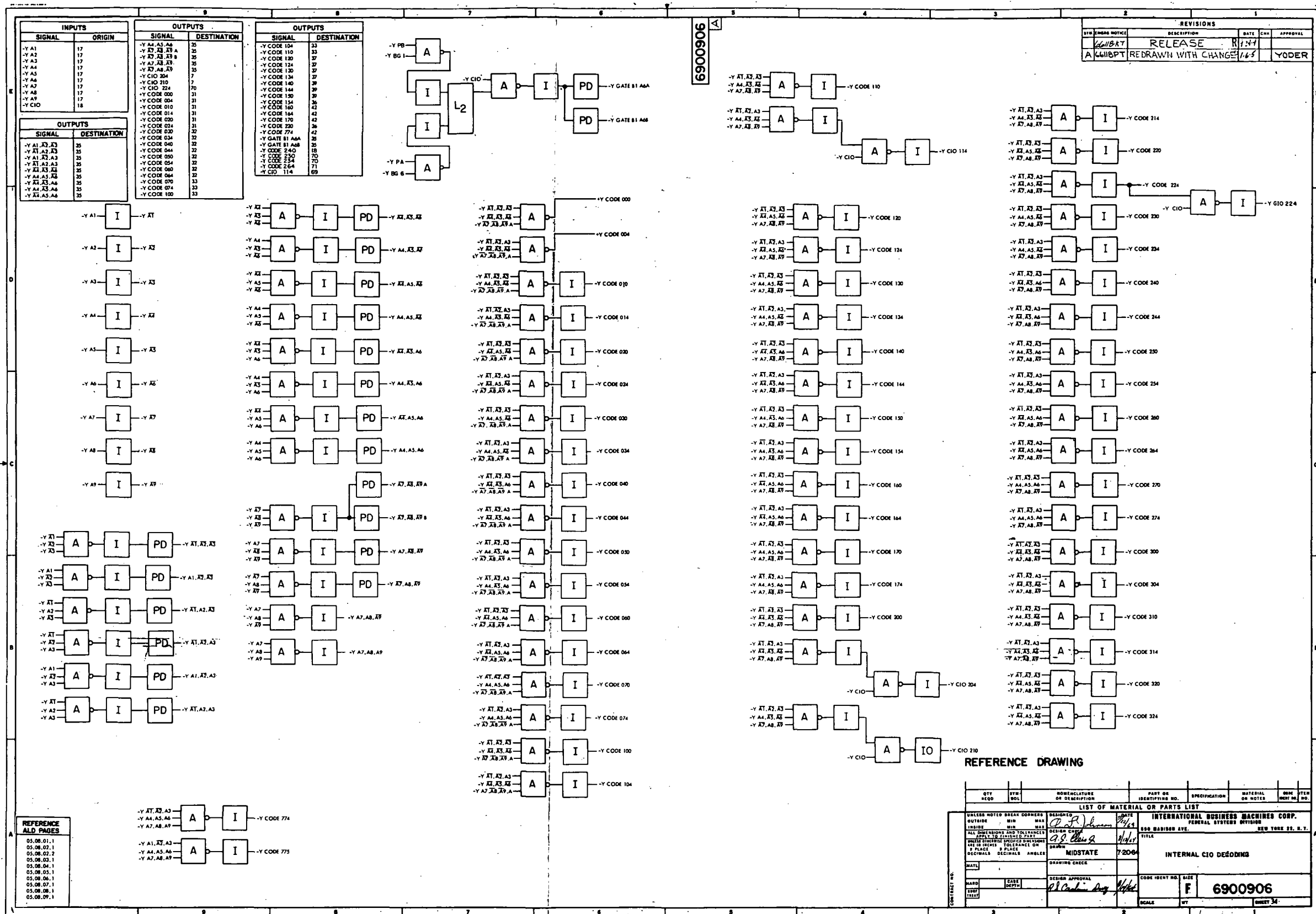


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 34)

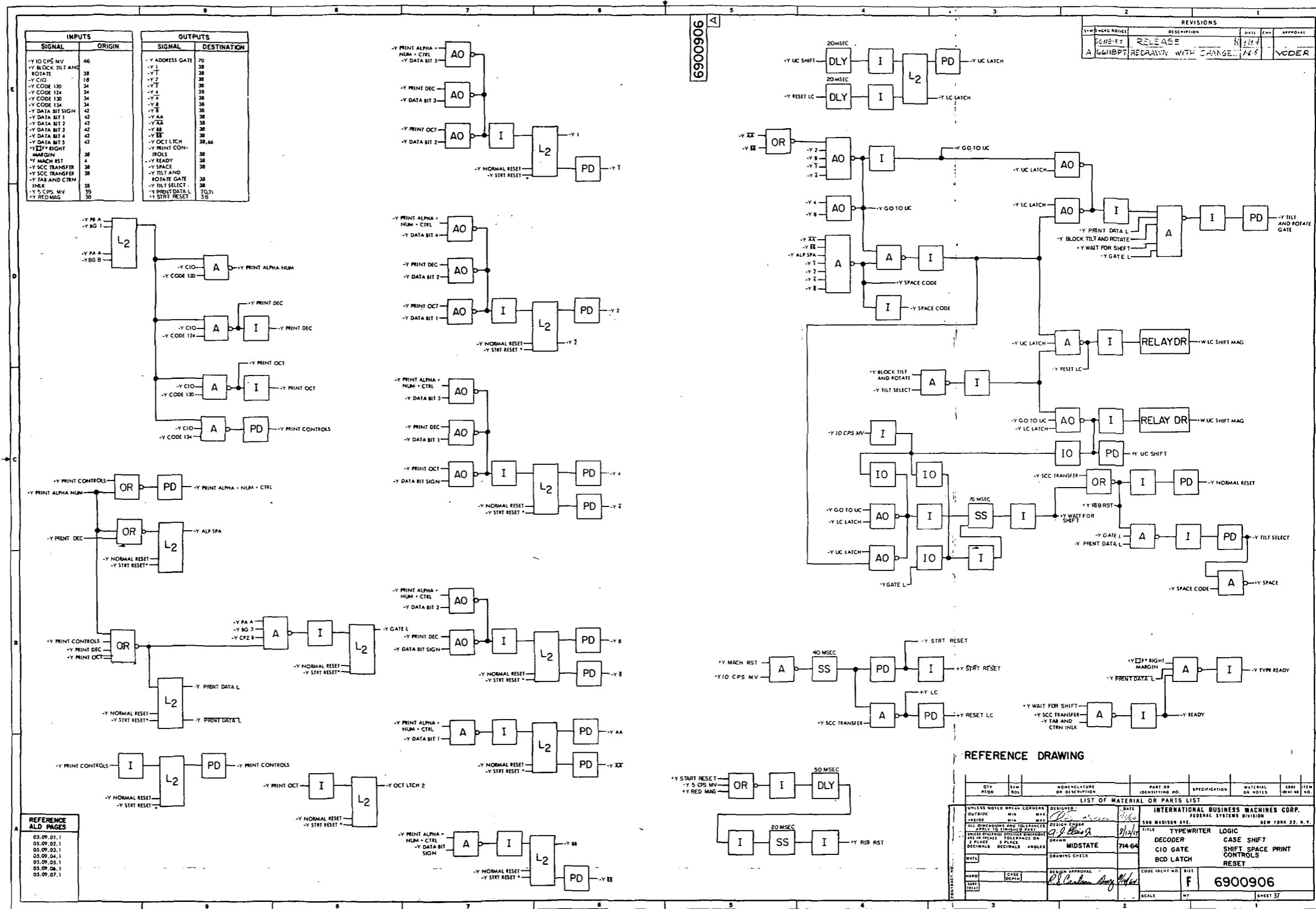


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 37)

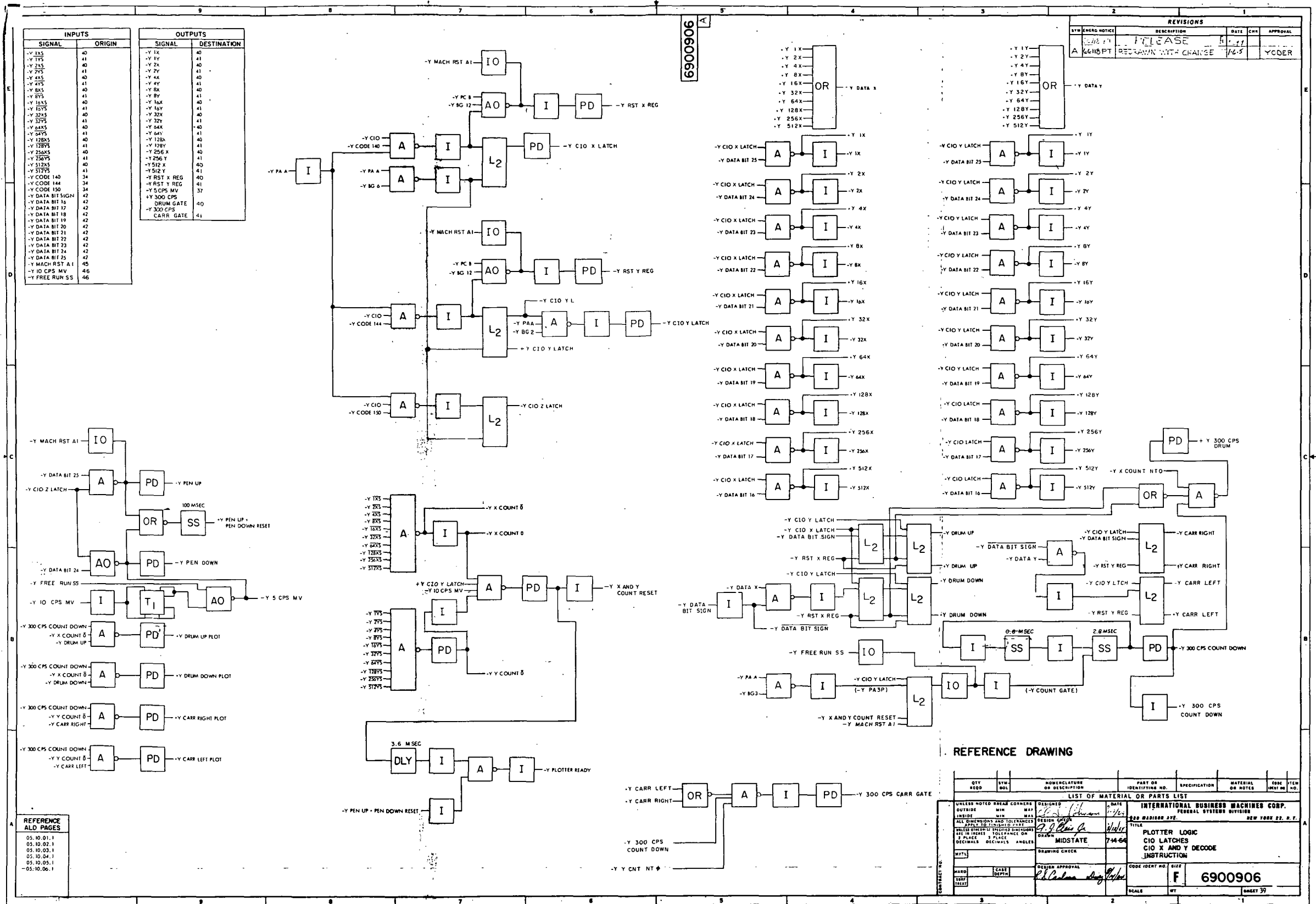


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 39)

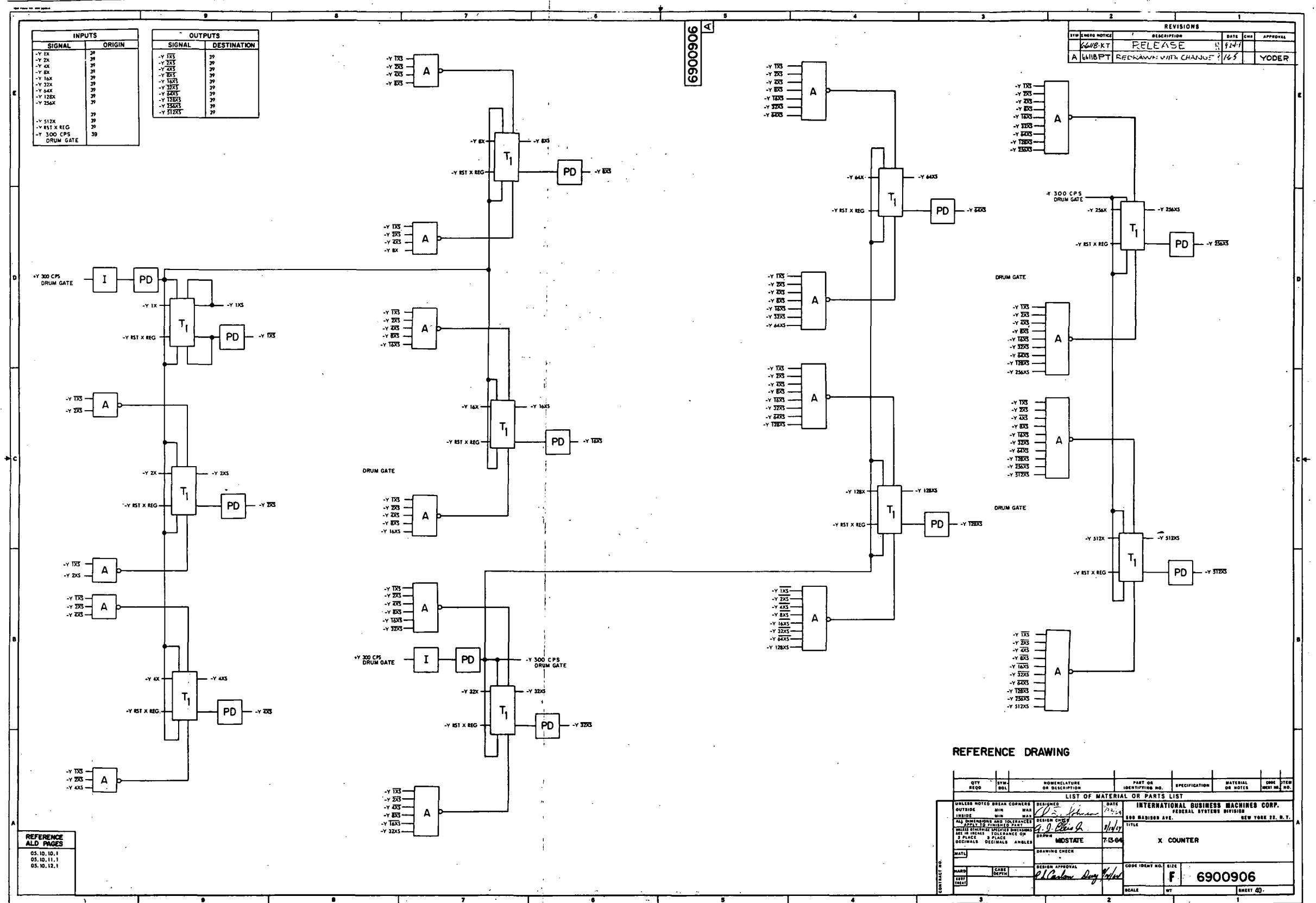


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 40)

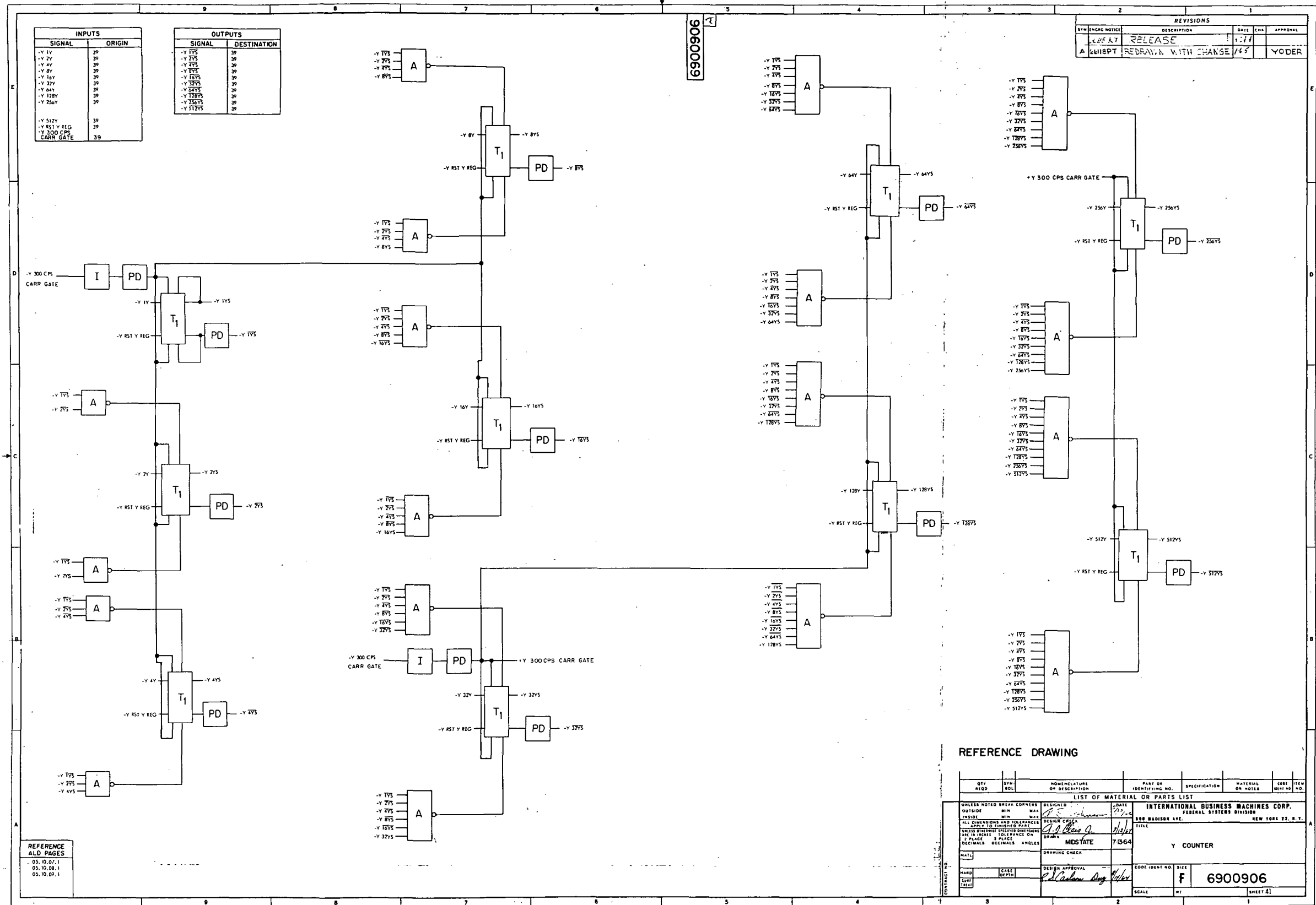


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 41)

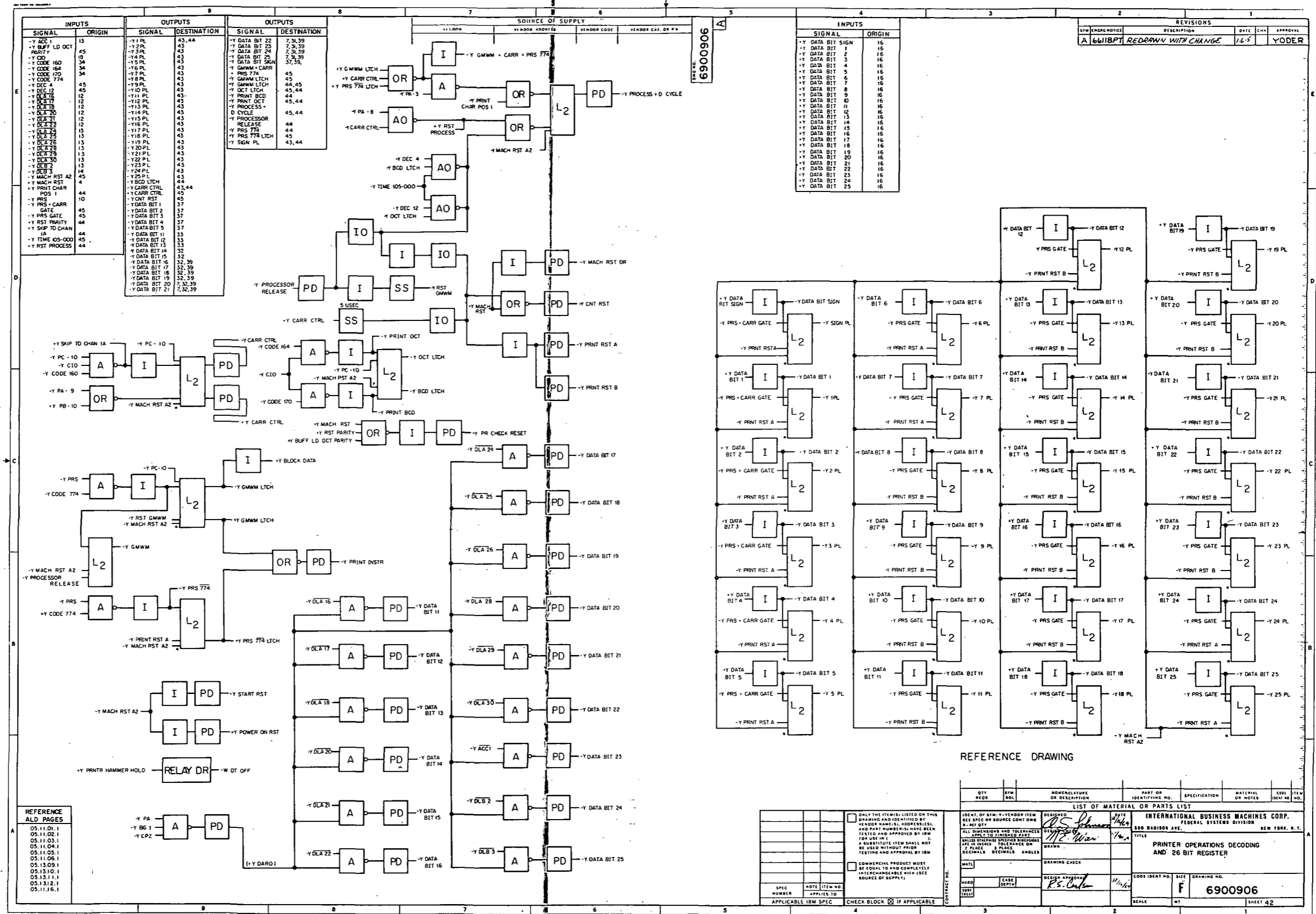
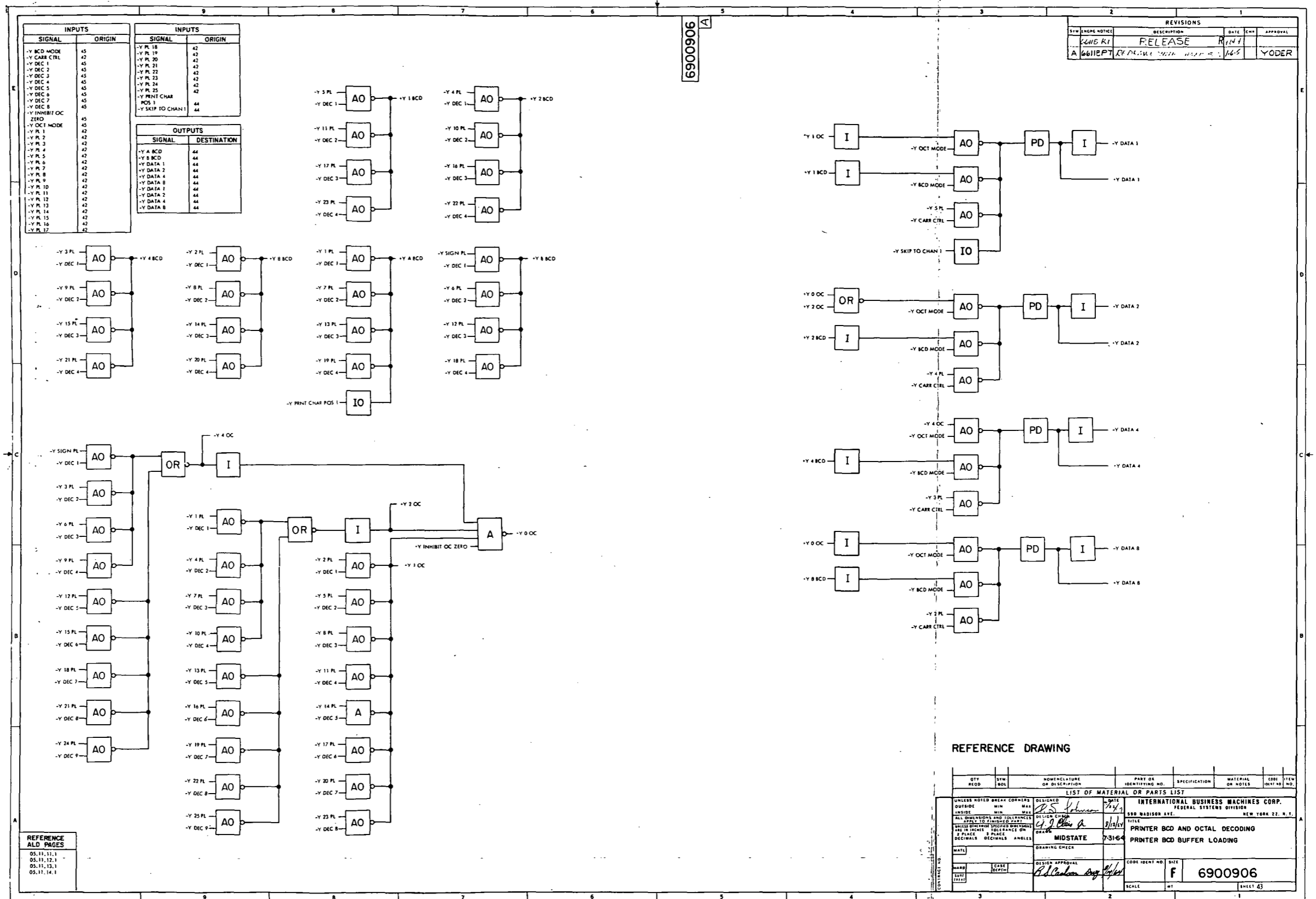


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 42)



6900906

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
1	RELEASE	11/11	
2	REVISED	11/15	YODER

REFERENCE DRAWING

QTY	REV	NOMENCLATURE	PART OR	SPECIFICATION	MATERIAL	CODE	ITEM
REQD	BOL	OR DESCRIPTION	IDENTIFYING NO.		OR NOTES		NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK COPYRE		DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE		MIN	MAX	FEDERAL SYSTEMS DIVISION			
MAX DIMENSIONS AND TOLERANCES		DESIGN CHECK		350 MADISON AVE. NEW YORK 22, N. Y.			
APPLY TO FINISHED PART		C. J. Blum		TITLE			
LIMIT DIMENSION DECIMALS		11/15/64		PRINTER BCD AND OCTAL DECODING			
1/2 PLACE		DRAWN		DECIMALS			
3 PLACE		MIDSTATE		7-31-64			
DECIMALS		DRAWING CHECK		PRINTER BCD BUFFER LOADING			
ANGLES		DESIGN APPROVAL		CODE IDENT NO			
		R. L. Carlson		F			
		SCALE		6900906			
		HT		SHEET 43			

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 43)

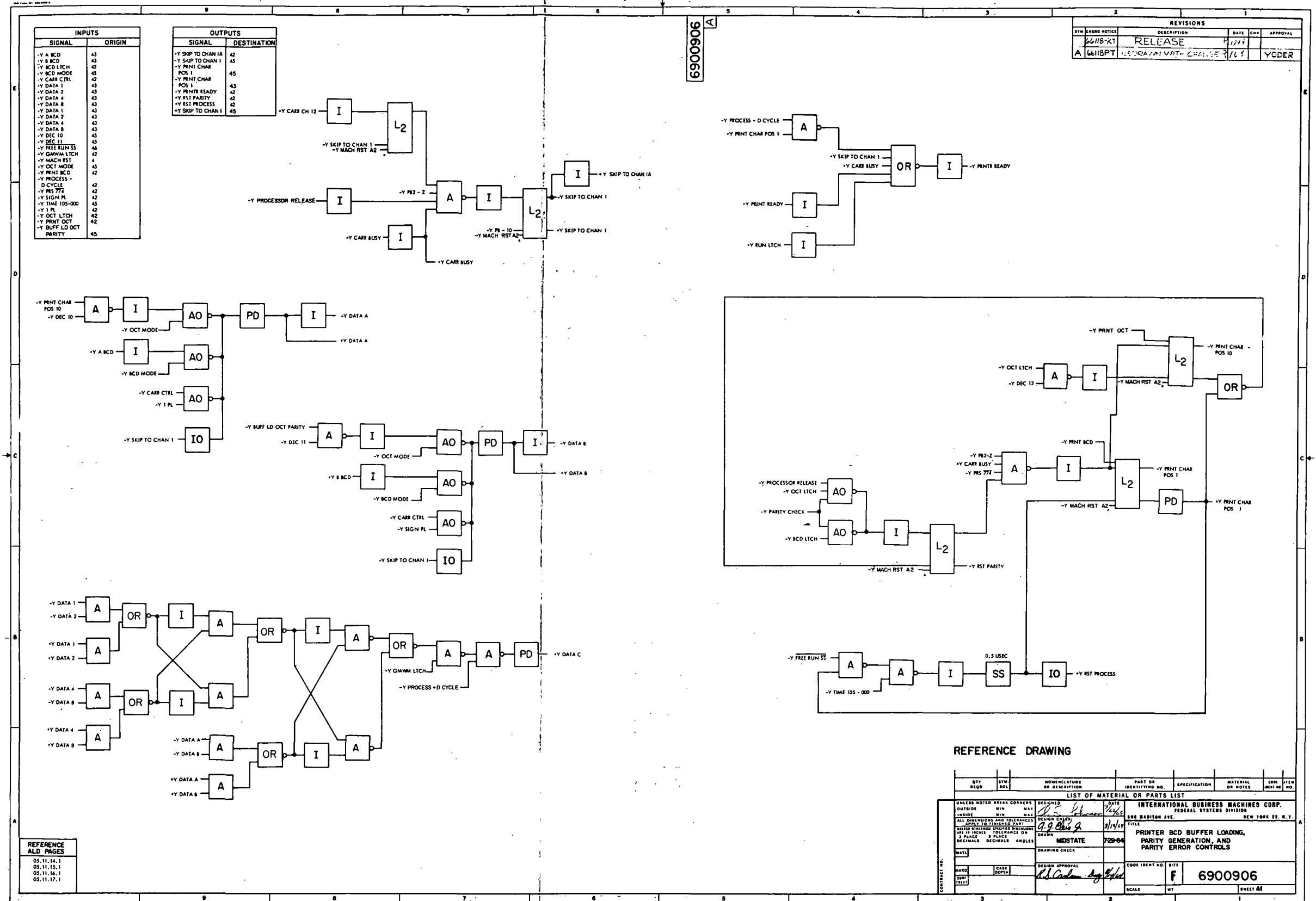


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 44)

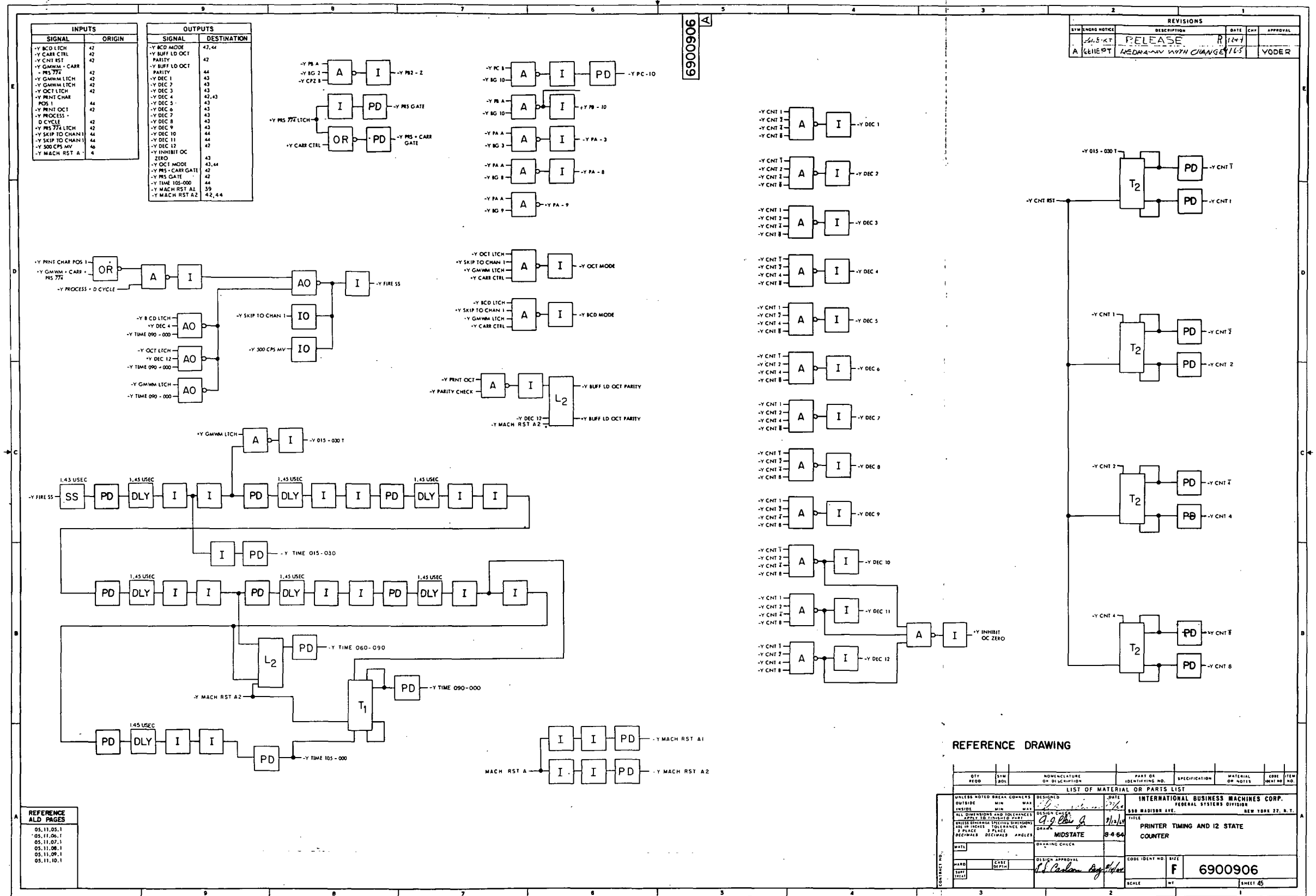


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 45)

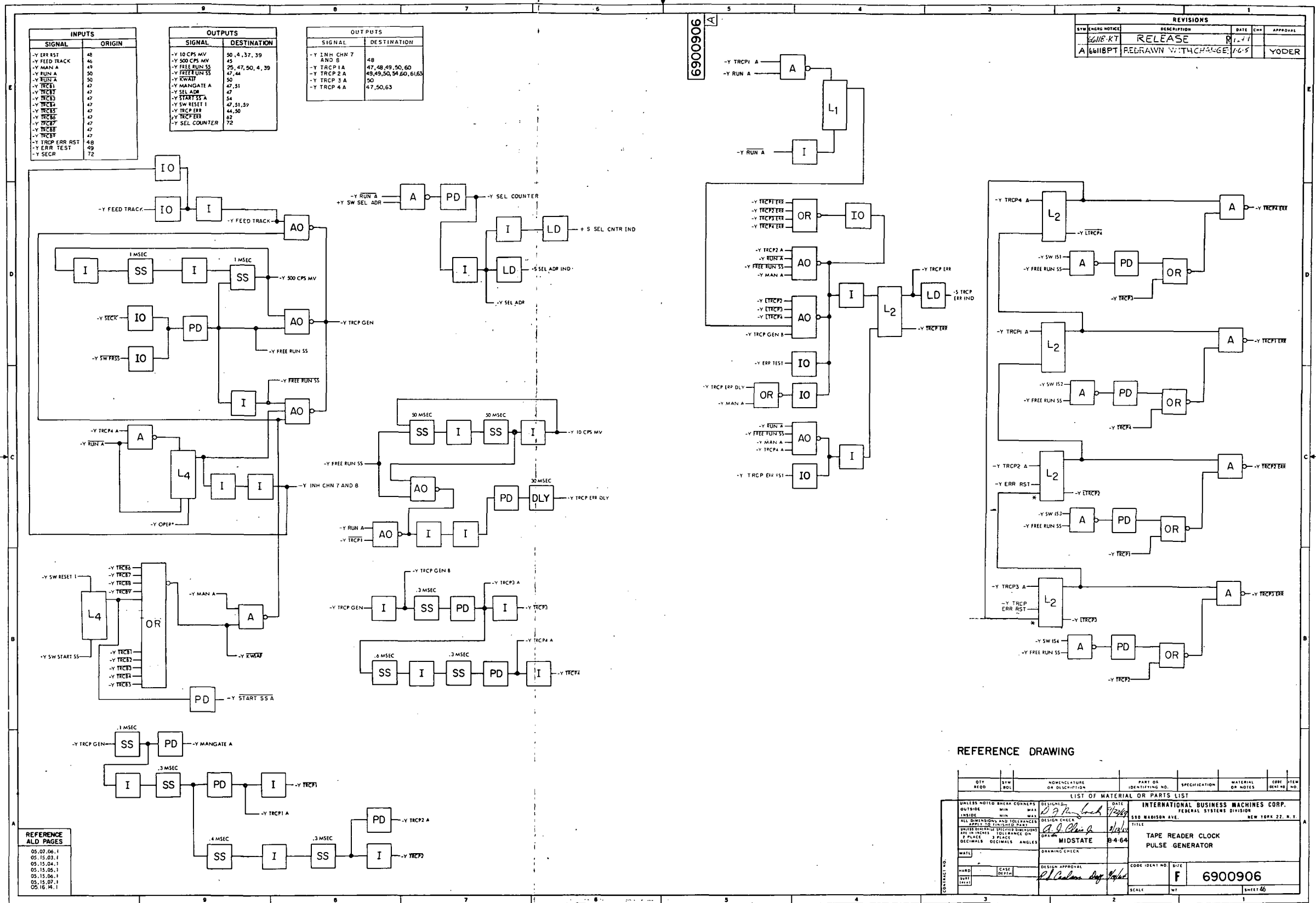


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 46)

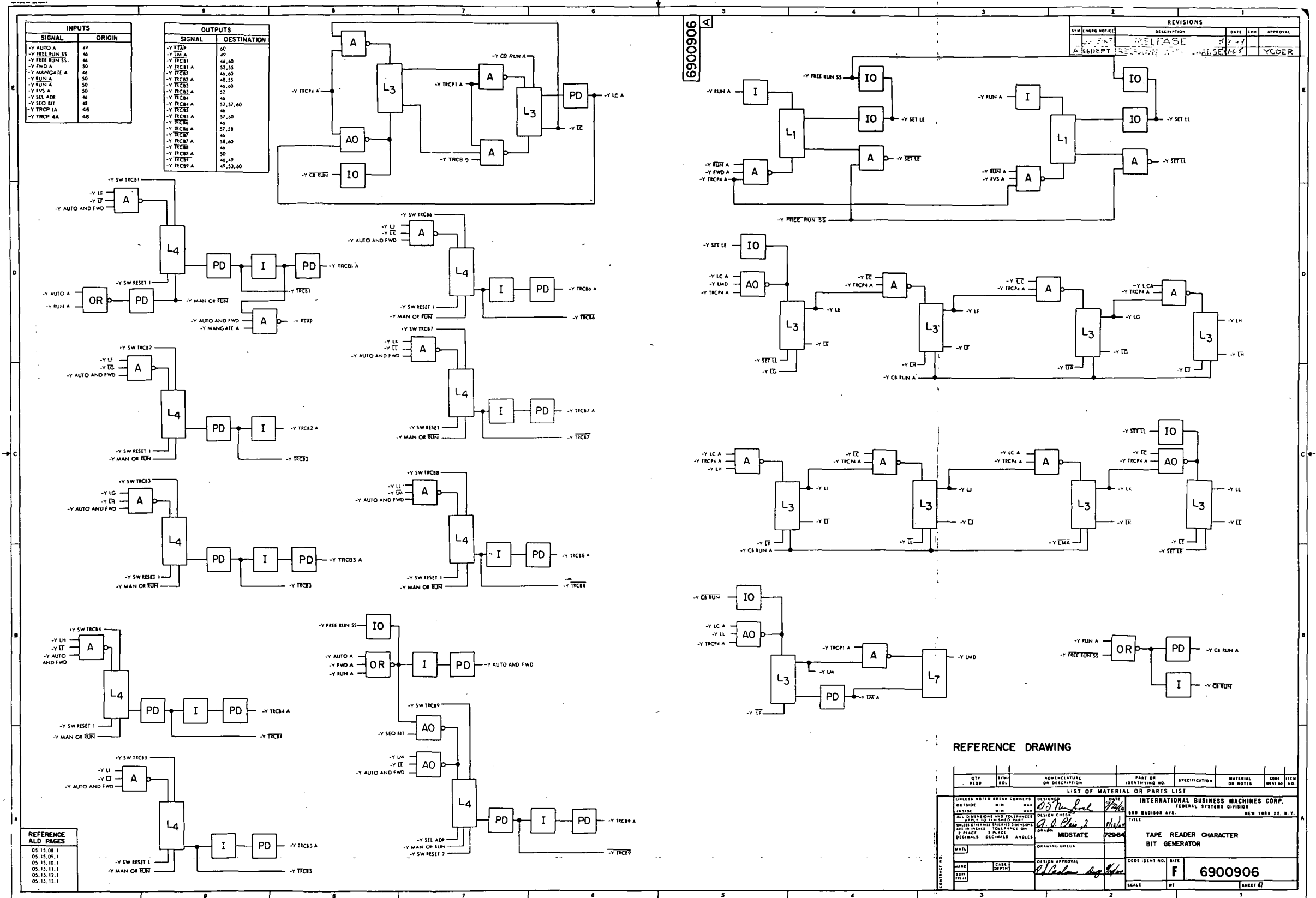


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 47)

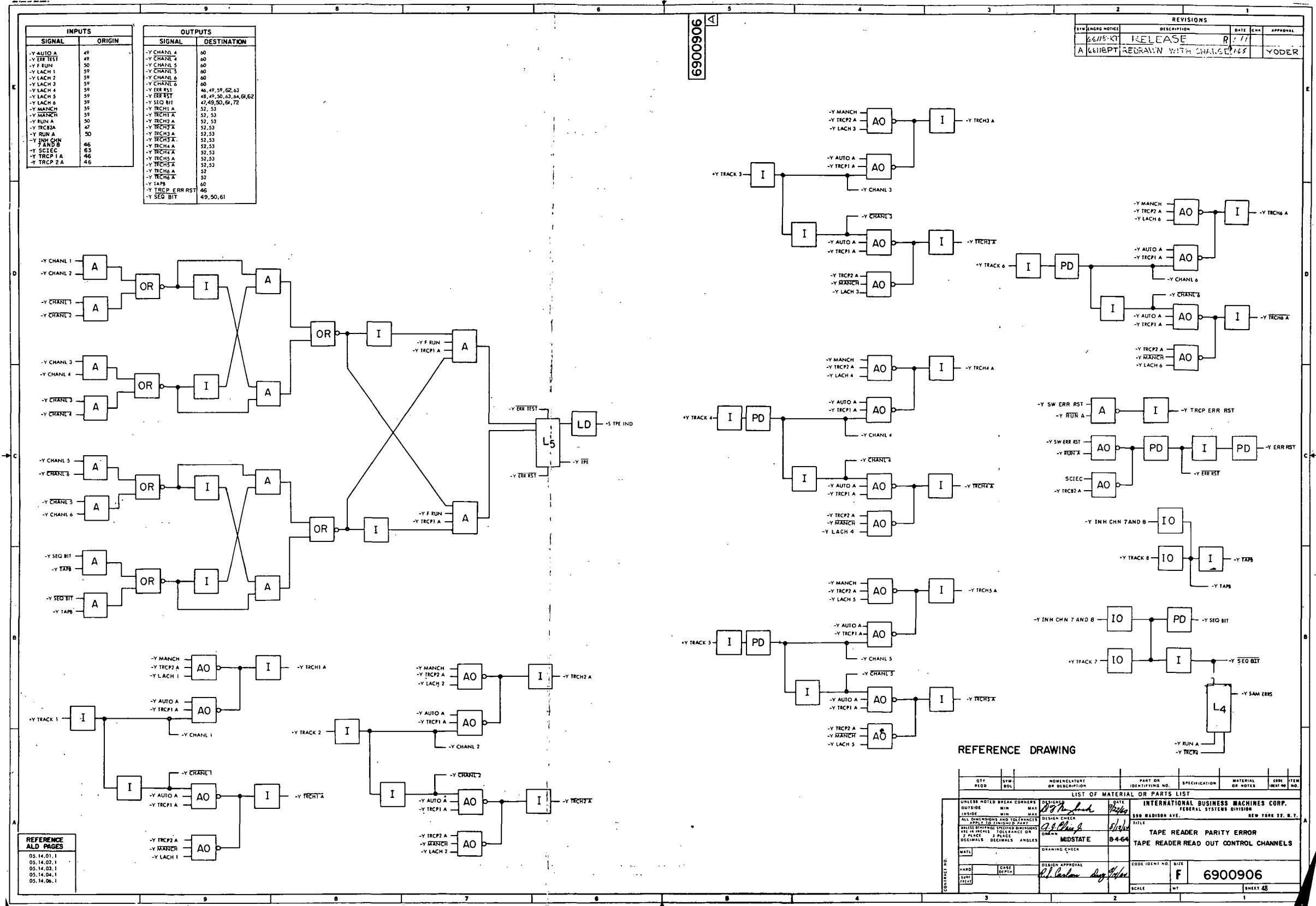
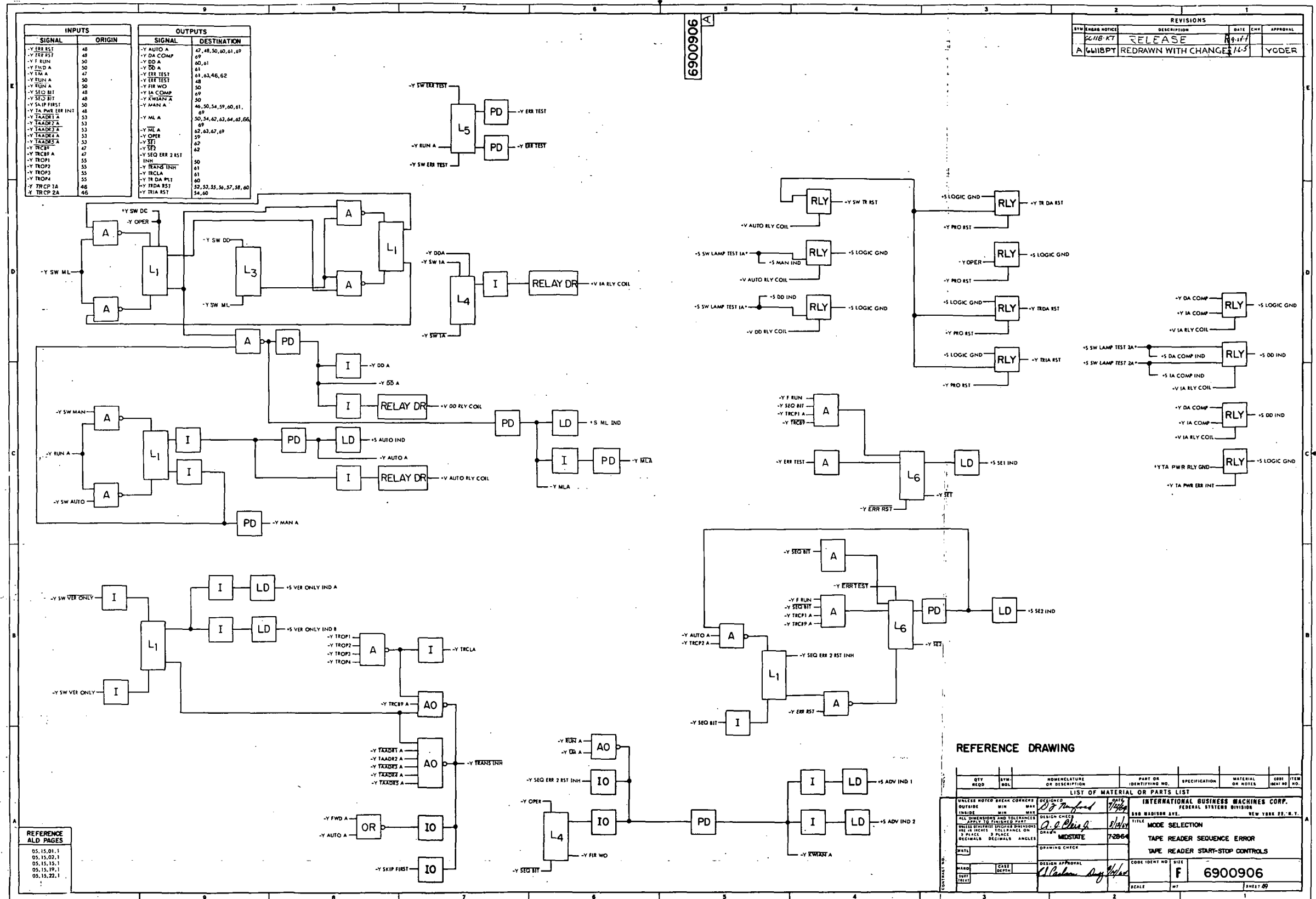


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 48)



REVISIONS				
REV	REASON	DATE	CHK	APPROVAL
1	RELEASE	8-9-57		
2	REDRAWN WITH CHANGES	11-3		YODER

REFERENCE DRAWING

QTY	SYM	HOMENCLATURE	PART OR	SPECIFICATION	MATERIAL	GRN	ITEM
REQD	MBOL	OR DESCRIPTION	IDENTIFYING NO.		OR NOTES		NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE	MIN	BY		FEDERAL SYSTEMS DIVISION			
INSIDE	MAX	WJM	7/28/57	540 MADISON AVE. NEW YORK 22, N.Y.			
ALL DIMENSIONS AND TOLERANCES		DESIGN CHECK		TITLE			
TO BE SHOWN UNLESS NOTED OTHERWISE		D. P. BLAIR	8/24/57	MODE SELECTION			
3 PLACE	3 PLACE	DRN	MIDSTATE	TAPE READER SEQUENCE ERROR			
DECIMALS	ANGLES			TAPE READER START-STOP CONTROLS			
DRAWING CHECK				CODE IDENT NO.	SIZE	SCALE	
DESIGN APPROVAL					F	6900906	
DATE						SHEET 49	

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 49)

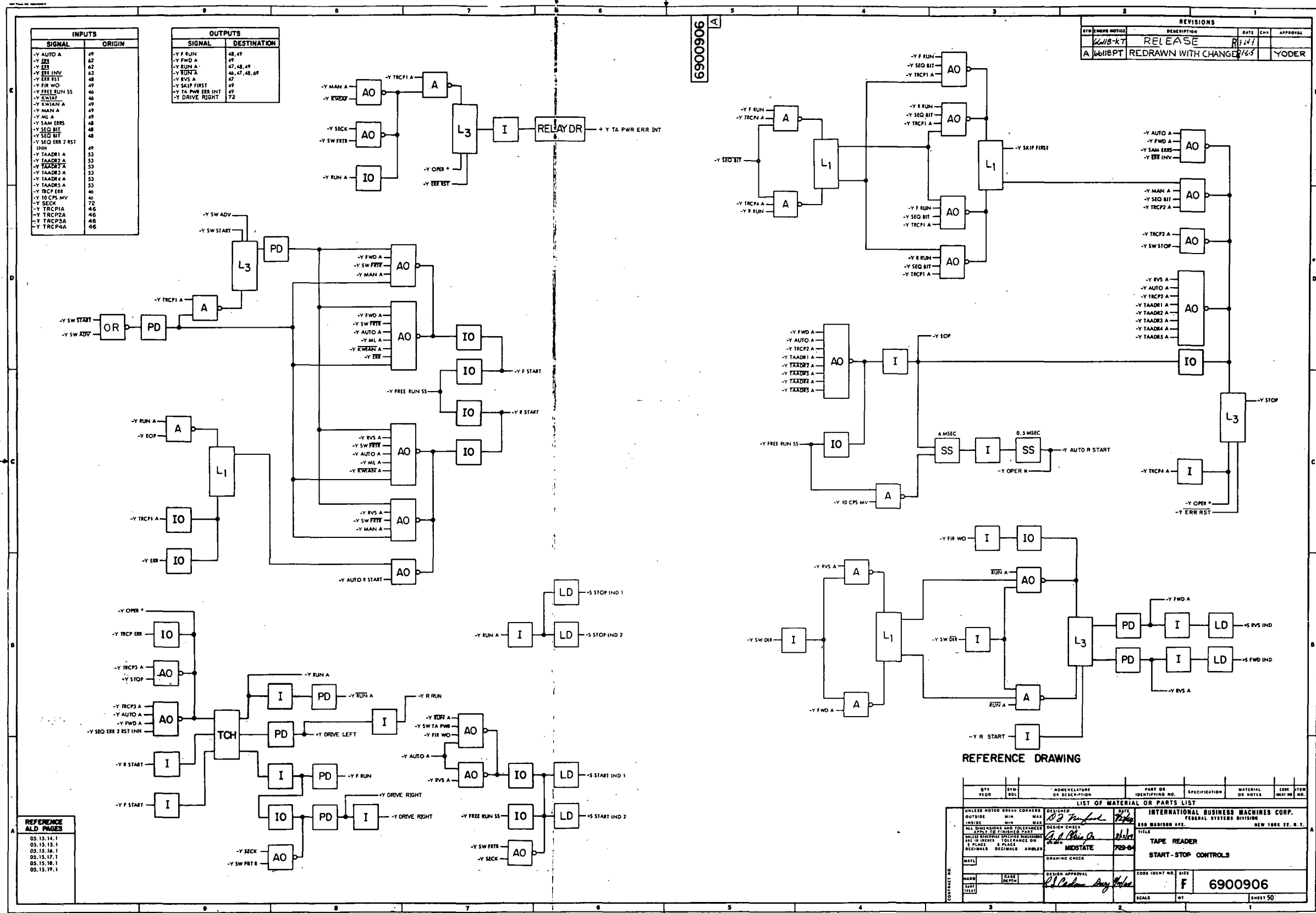


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 50)

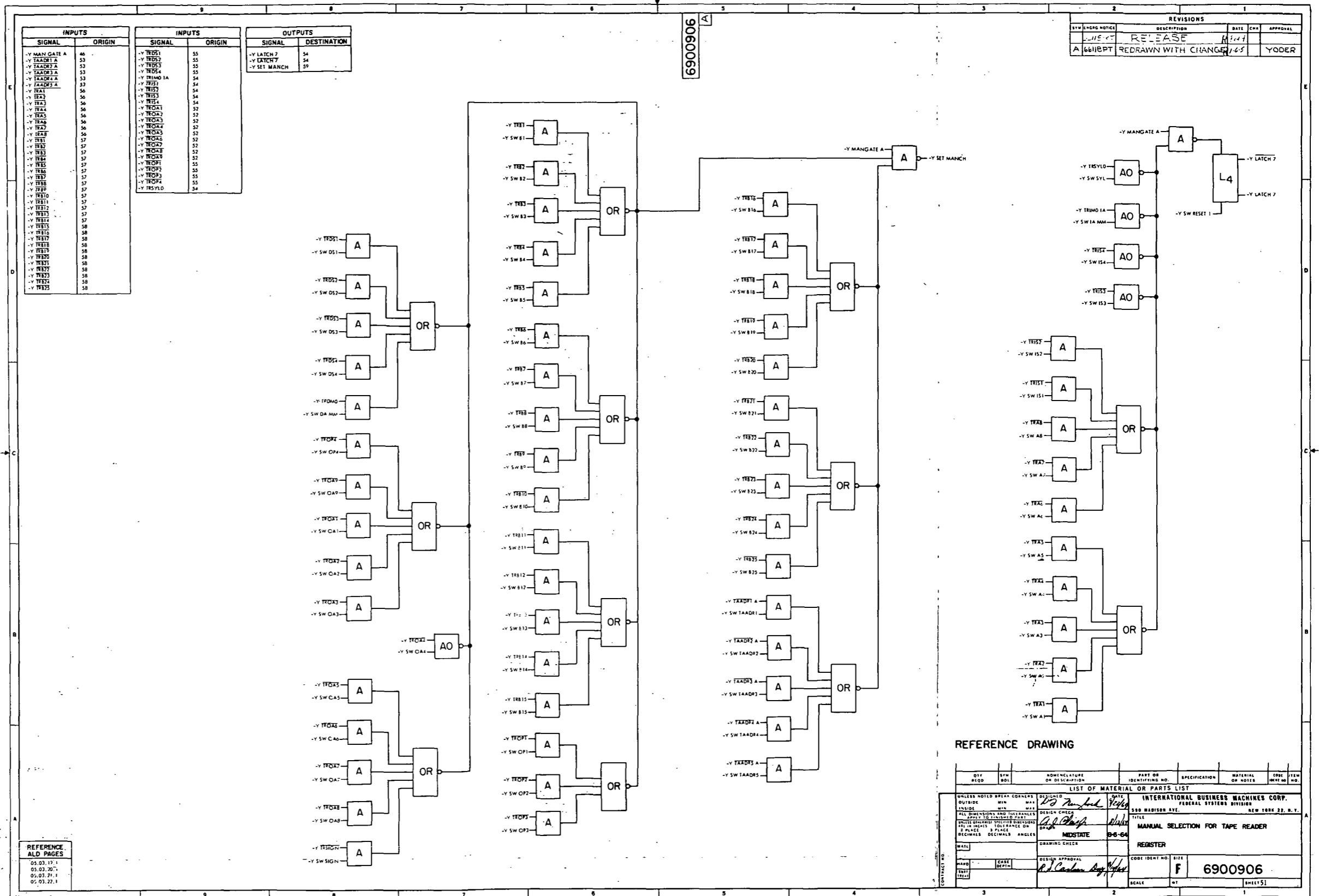


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 51)

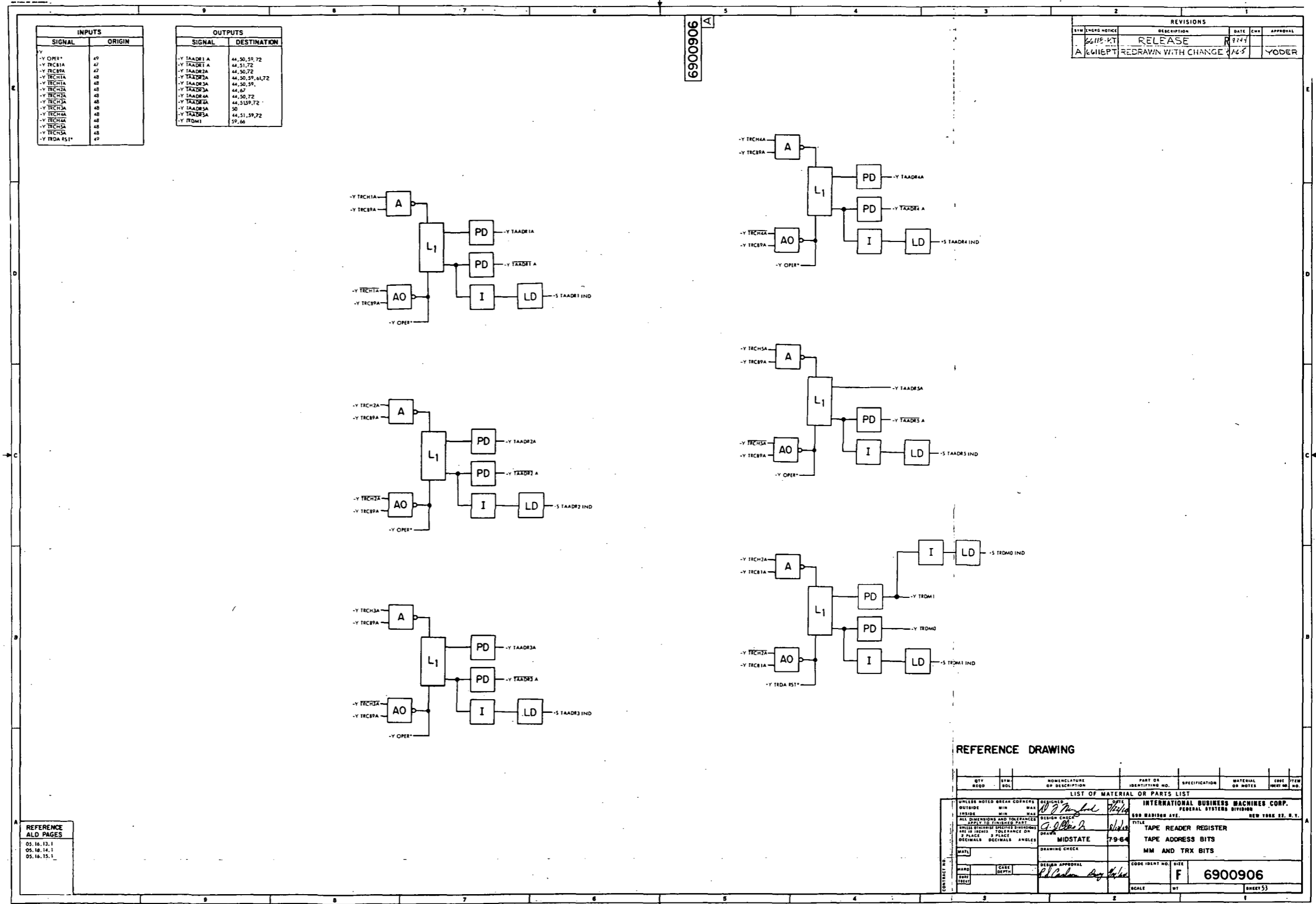
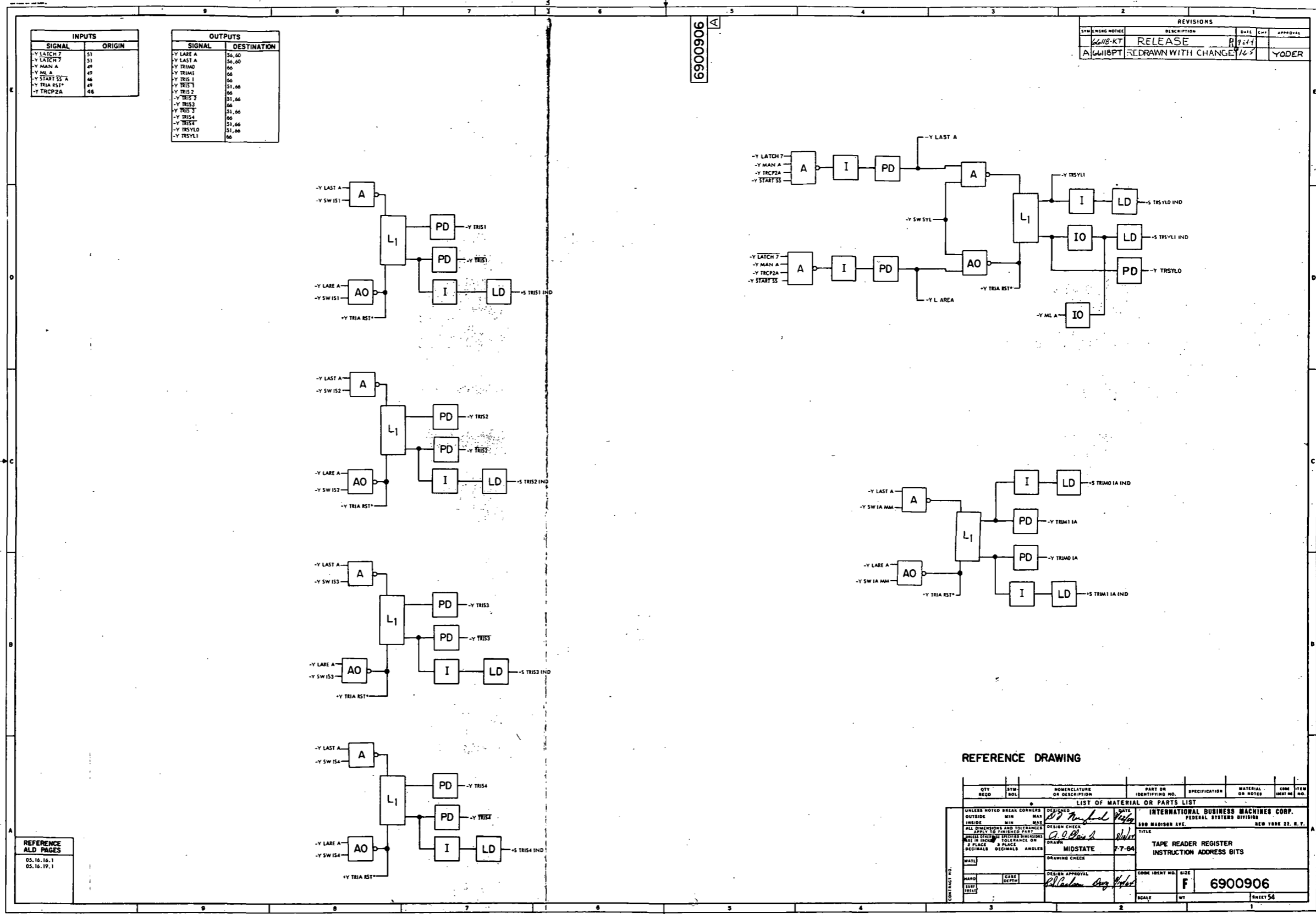


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 53)



REVISIONS				
NO.	DESCRIPTION	DATE	BY	APPROVAL
1	RELEASE	8/24		
2	REDRAWN WITH CHANGE	1/65		YODER

6900906
A

REFERENCE
AID PAGES
05, 16, 16.1
05, 16, 19.1

REFERENCE DRAWING

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 550 MADISON AVE. NEW YORK 22, N. Y.			
OUTSIDE	MIN	MAX	DESIGN CHECK	TITLE			
INSIDE	MIN	MAX	DESIGN CHECK	TAPE READER REGISTER INSTRUCTION ADDRESS BITS			
F PLACE DECIMALS		DRAWN		MIDSTATE 7-7-64			
DECIMALS		DRAWING CHECK		SCALE			
ANGLES		DESIGN APPROVAL		CODE IDENT NO.		SIZE	
		DRAWN		F		6900906	
		CHECK		SCALE		SHEET 54	
		DEPT.					
		DATE					

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 54)

V-10-158

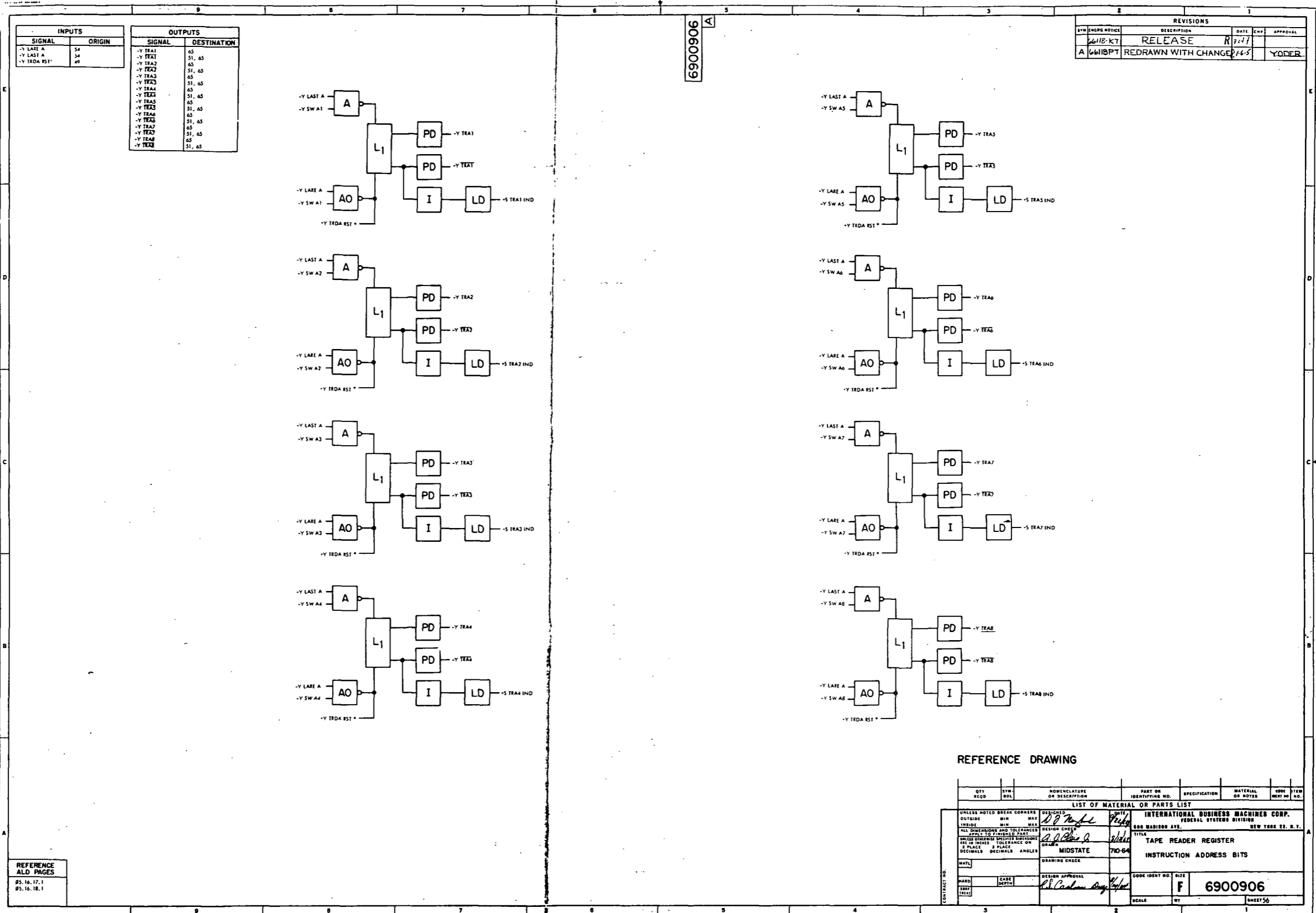


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 56)

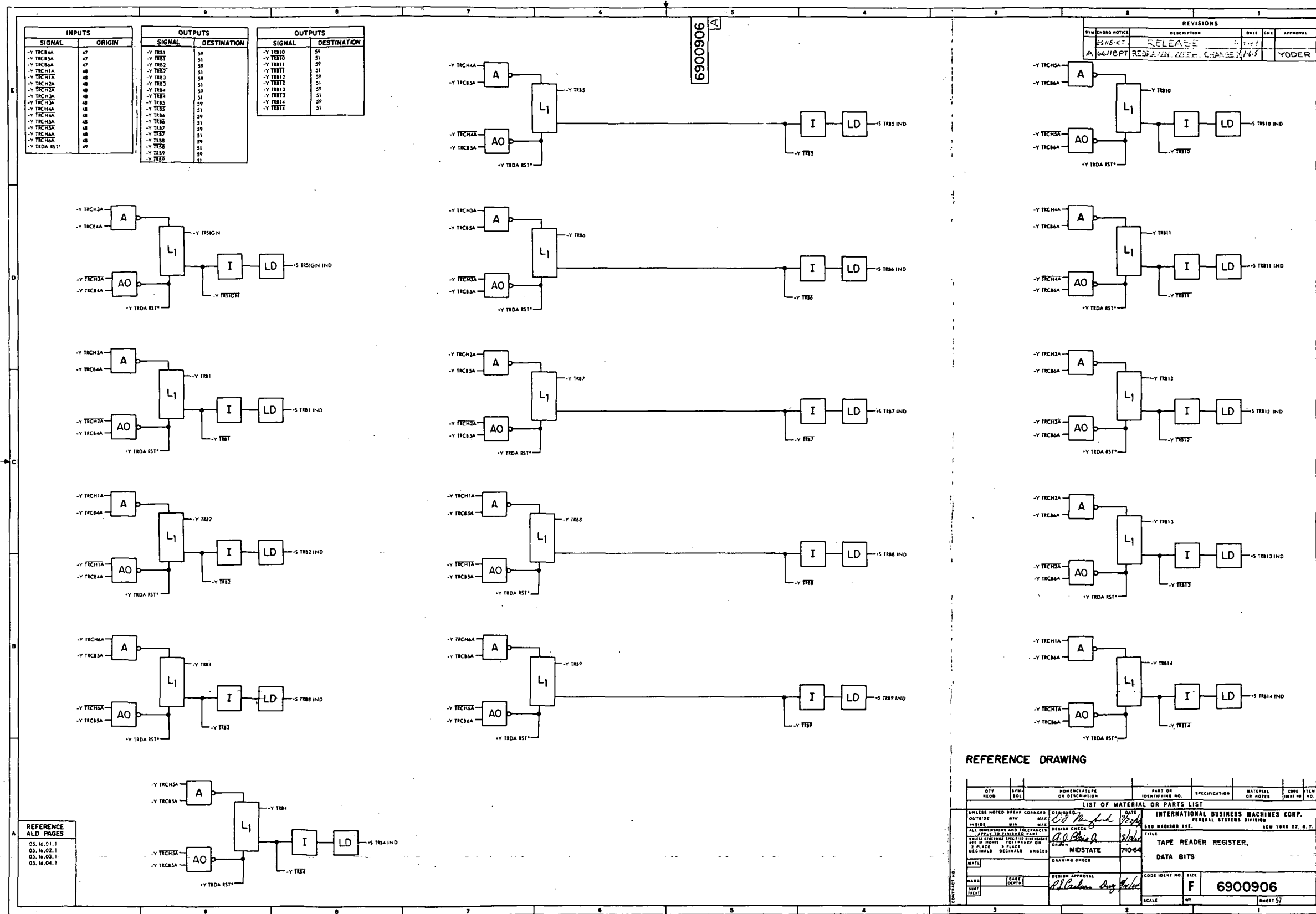
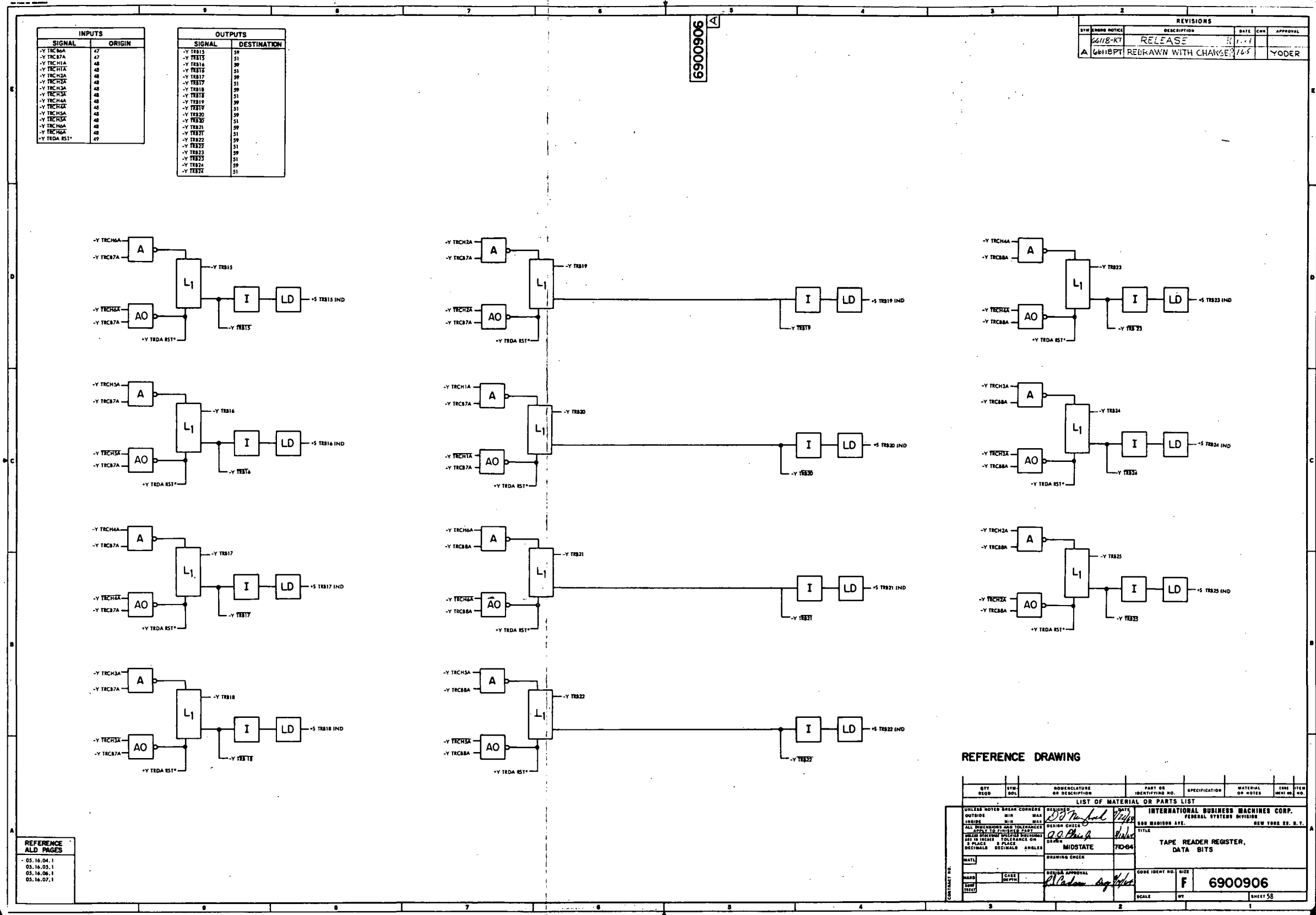


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 57)



INPUTS		OUTPUTS	
SIGNAL	ORIGIN	SIGNAL	DESTINATION
-Y TRCH2A	47	-Y TRB15	51
-Y TRCH7A	48	-Y TRB16	51
-Y TRCH2A	48	-Y TRB17	51
-Y TRCH7A	48	-Y TRB18	51
-Y TRCH3A	48	-Y TRB19	51
-Y TRCH8A	48	-Y TRB20	51
-Y TRCH3A	48	-Y TRB21	51
-Y TRCH8A	48	-Y TRB22	51
-Y TRCH2A	48	-Y TRB23	51
-Y TRCH7A	48	-Y TRB24	51
-Y TRCH3A	48	-Y TRB25	51
-Y TRCH8A	48	-Y TRB26	51
-Y TRDA RST*	49		

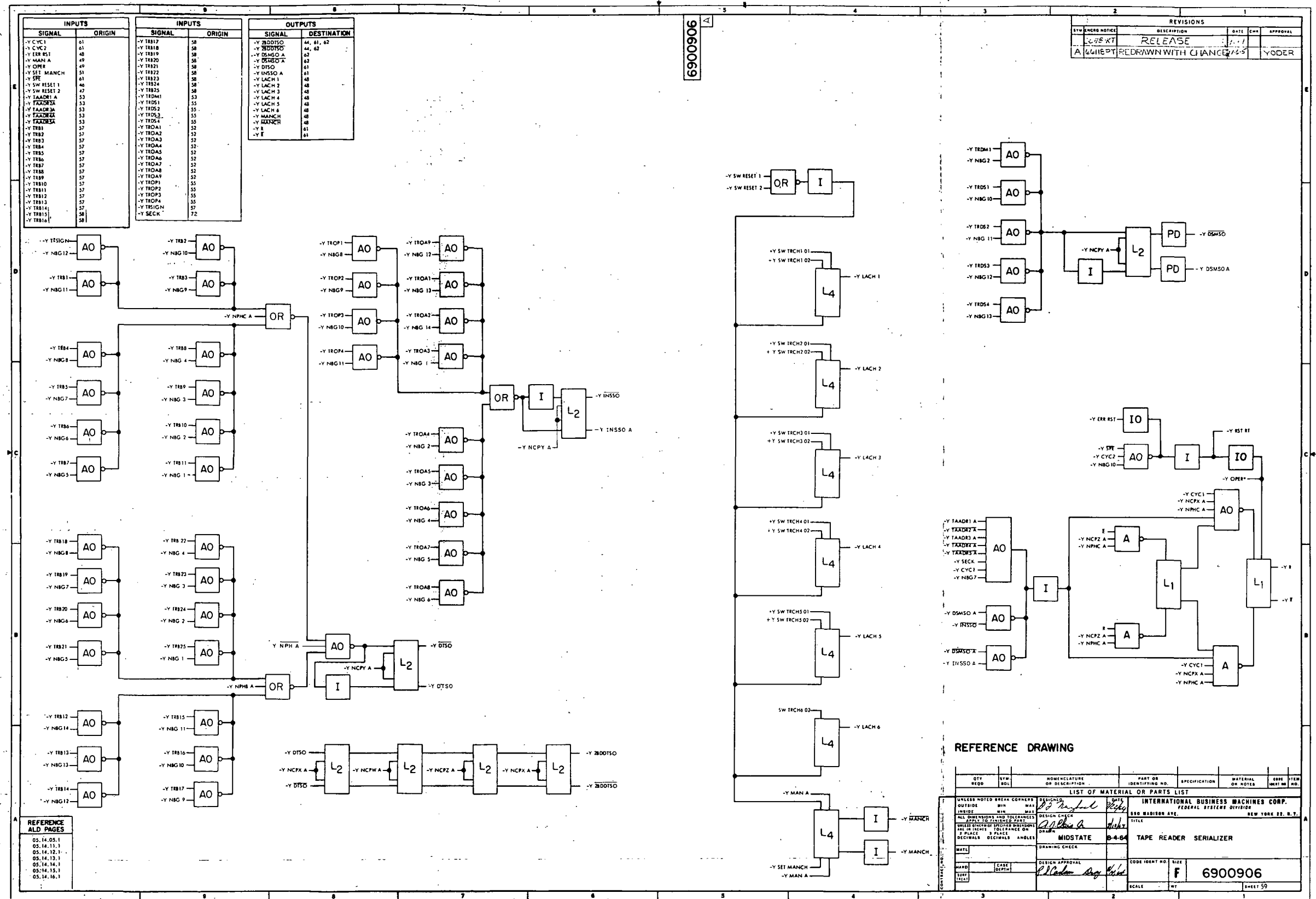
REVISIONS			
REV	DATE	DESCRIPTION	APPROVAL
1	11-1	RELEASE	
2	1-1	REDRAWN WITH CHANGES	YODER

DATE	DESCRIPTION
05.16.04.1	
05.16.05.1	
05.16.06.1	
05.16.07.1	

REFERENCE DRAWING

QTY	SYMBOL	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	DATE	BY
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE DIMENSIONS		DESIGNED BY	DATE	FEDERAL SYSTEMS DIVISION			
ALL DIMENSIONS AND TOLERANCES		DESIGNED BY	DATE	800 MADISON AVE. NEW YORK 22, N.Y.			
SHOWN TO DIMENSIONS UNLESS		DESIGNED BY	DATE	TITLE			
OTHERWISE SPECIFIED OTHERWISE		DESIGNED BY	DATE	TAPE READER REGISTER,			
DIMENSIONS TO BE PLACED ON		DESIGNED BY	DATE	DATA BITS			
DIMENSIONS TO BE PLACED ON		DESIGNED BY	DATE	DRAWING NO. 70-64			
DIMENSIONS TO BE PLACED ON		DESIGNED BY	DATE	SCALE			
DIMENSIONS TO BE PLACED ON		DESIGNED BY	DATE	SHEET 58			

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 58)



REFERENCE DRAWING

QTY	REQD	SYM	HOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

QTY	REQD	SYM	HOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO.

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX DIMENSIONS AND TOLERANCES APPLY TO FINISHED PARTS. ALL DIMENSIONS UNLESS OTHERWISE SPECIFIED ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS DECIMALS ANGLES.

DESIGNER: *P. J. ...*
 DESIGN CHECK: *A. ...*
 DRAWING CHECK: *P. ...*
 MIDDLE STATE 8-4-64
 TITLE: TAPE READER SERIALIZER
 CODE IDENT NO: **F**
 SIZE: **6900906**
 SCALE: **1:1**
 SHEET: **59**

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 59)

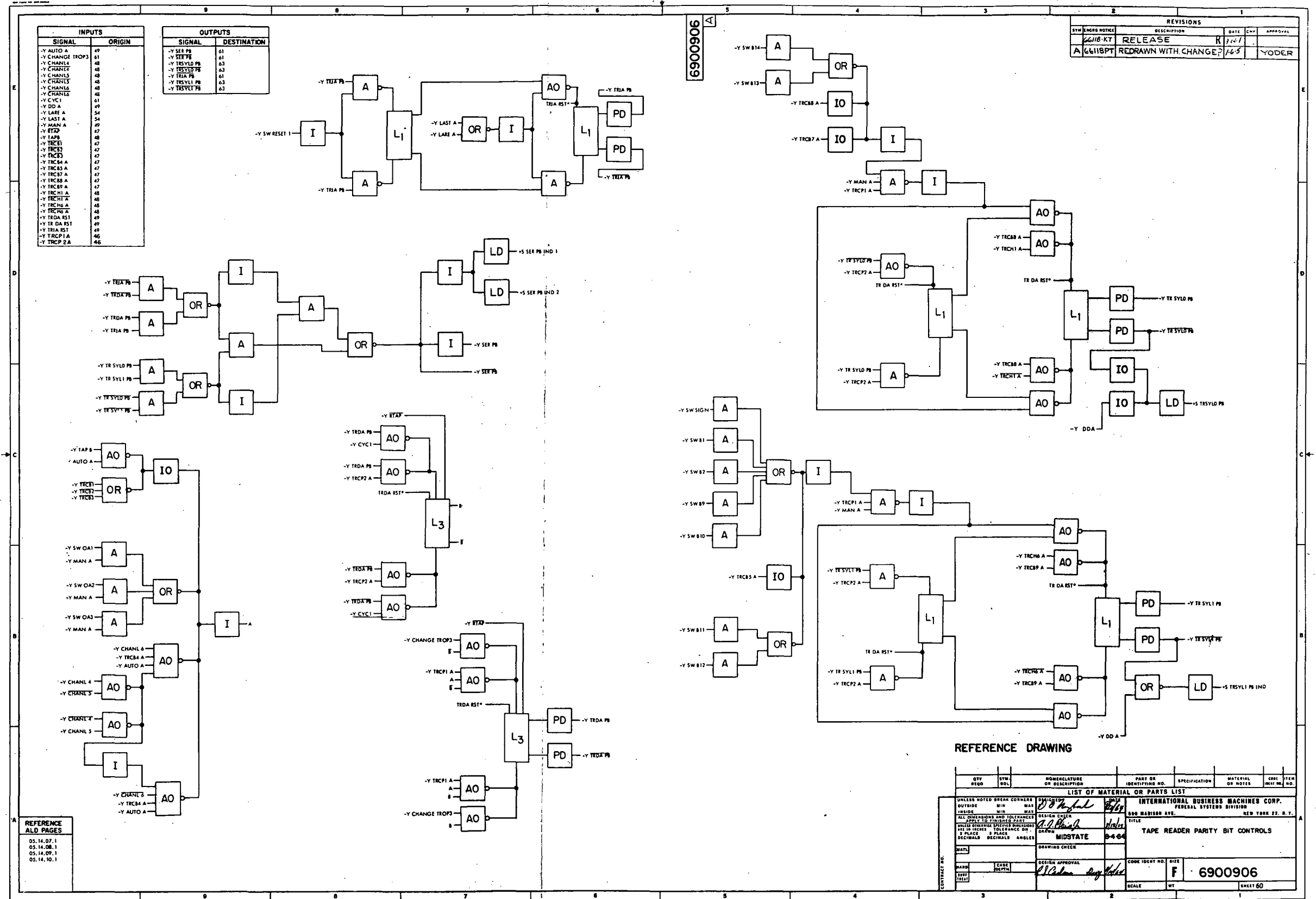


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 60)

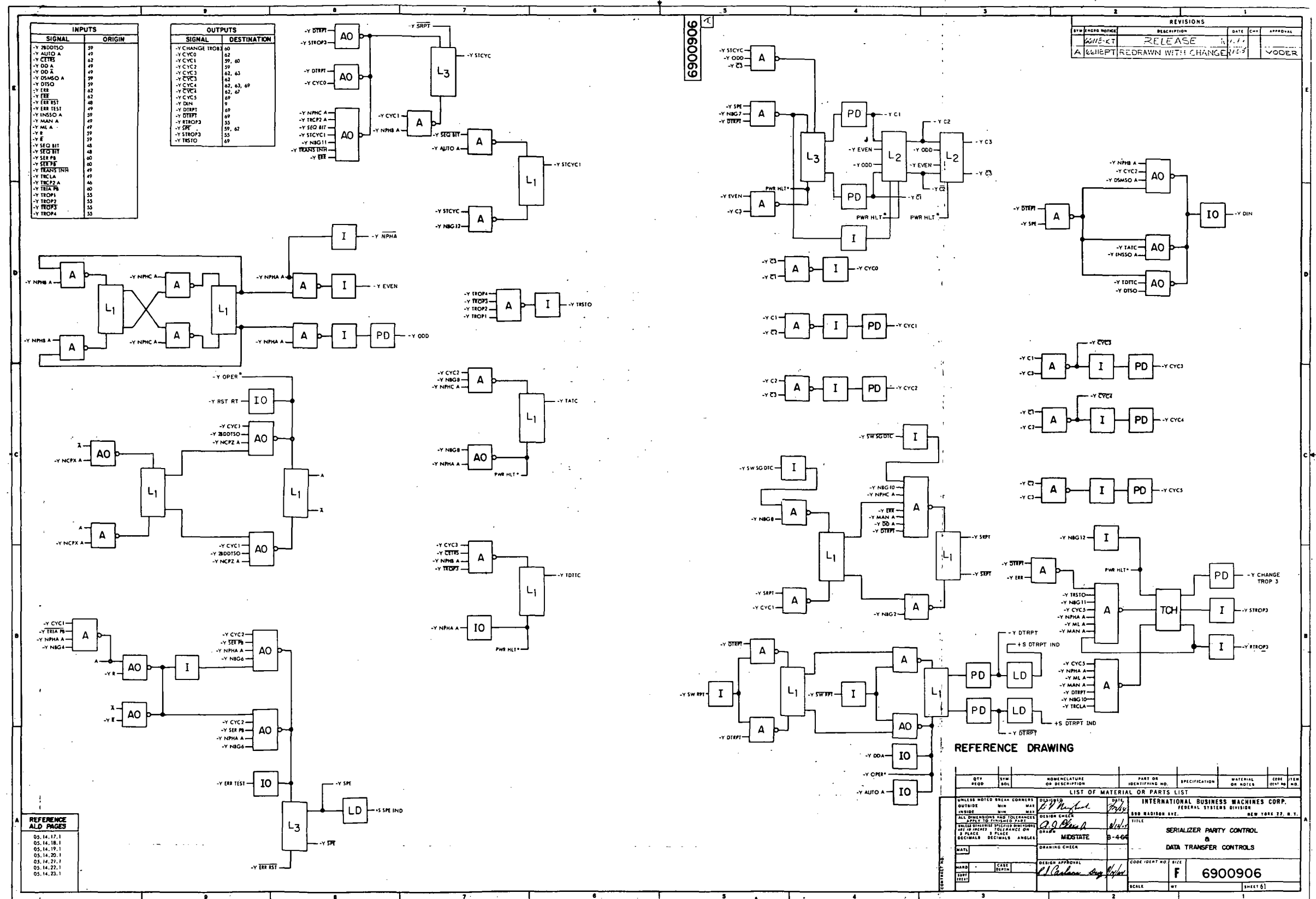


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 61)

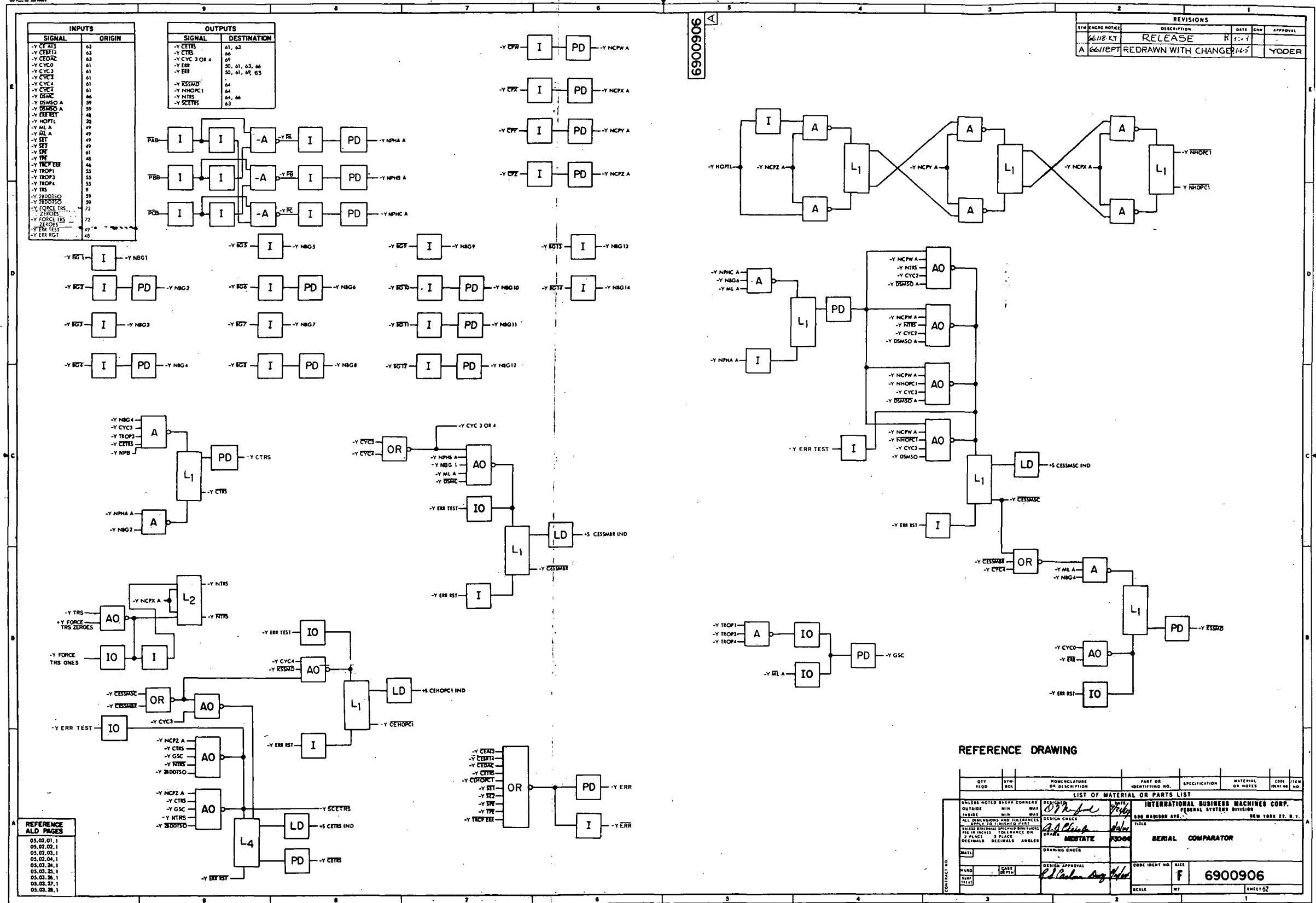


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 62)

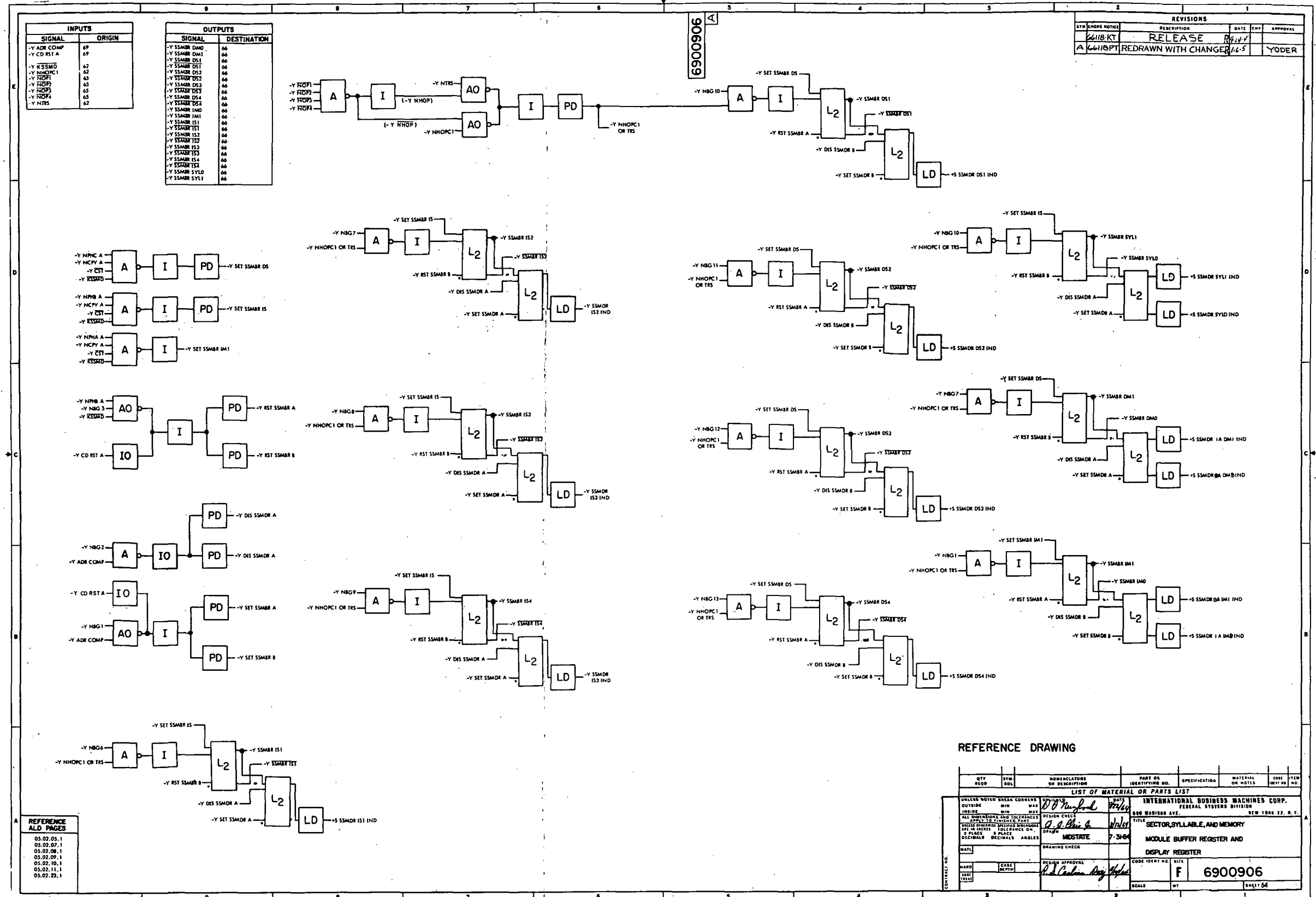


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 64)

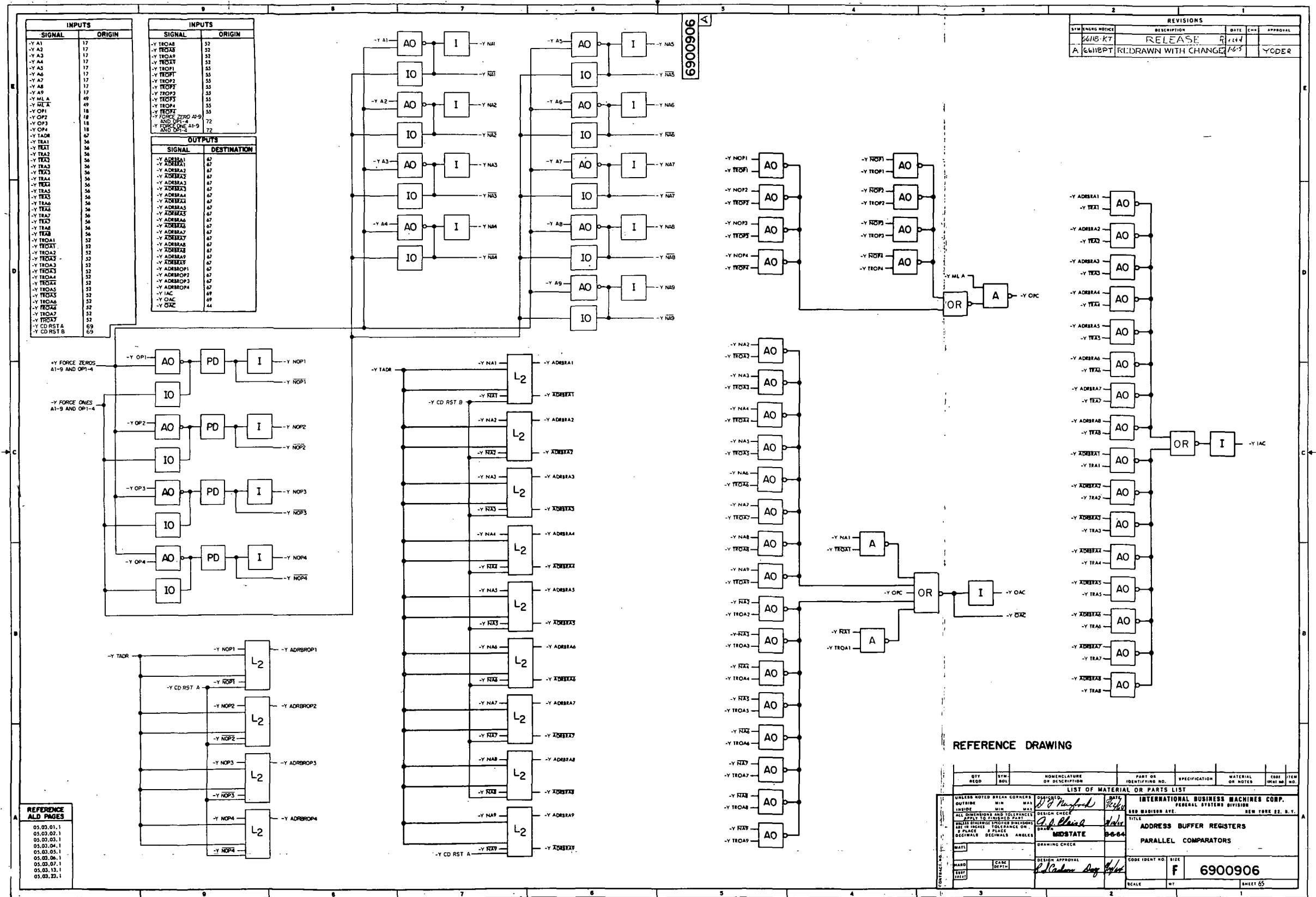


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 65)

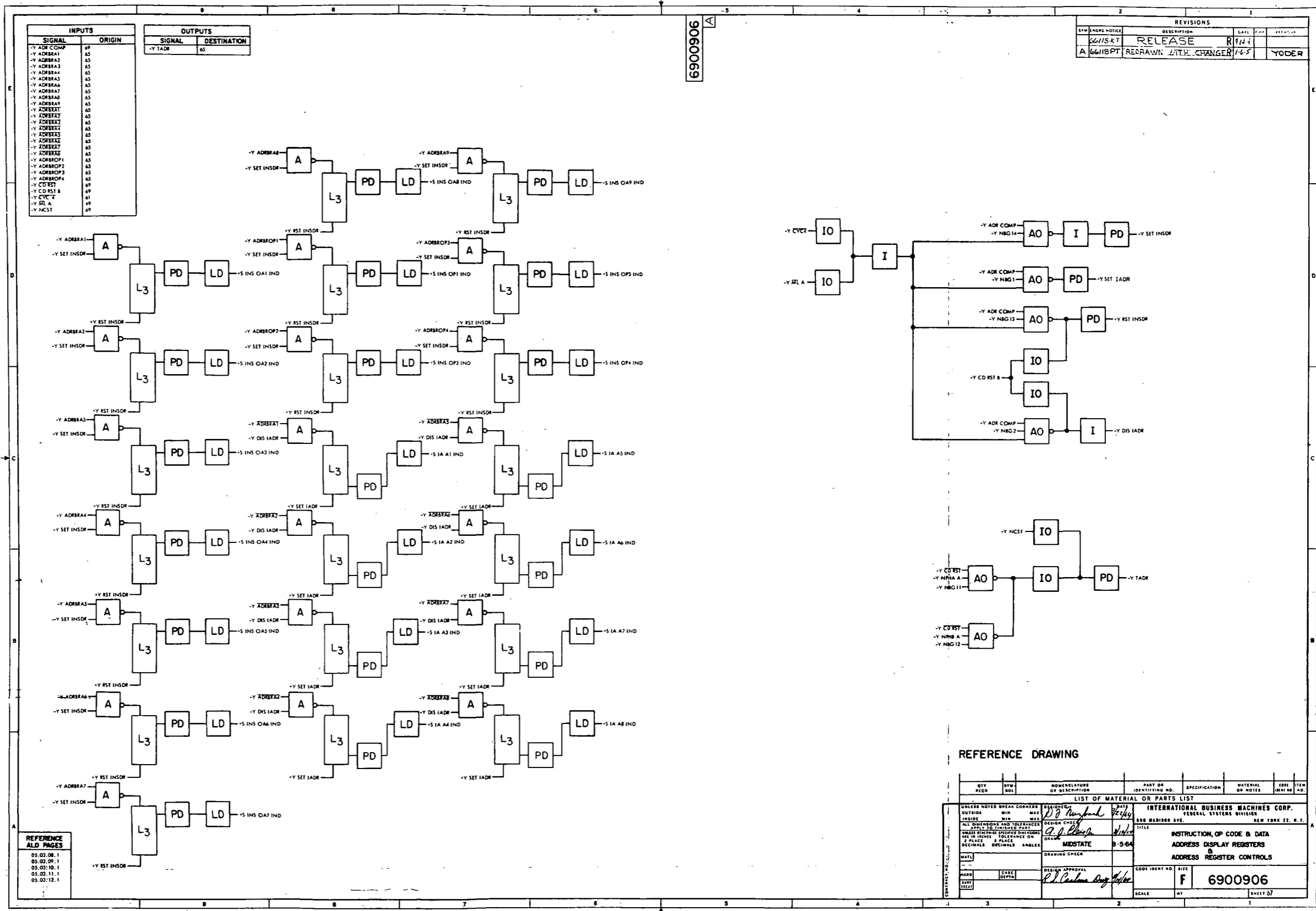
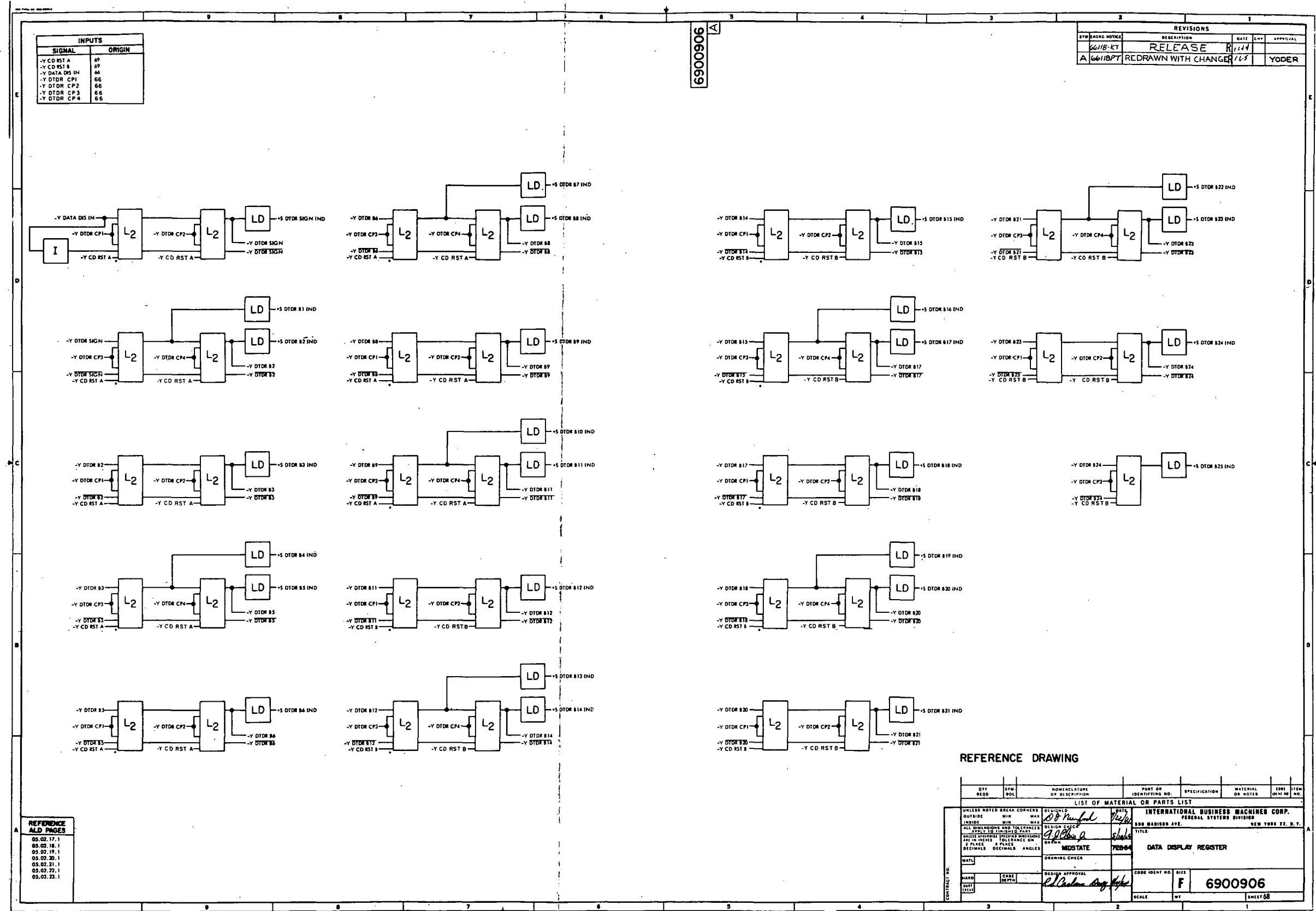


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 67)



INPUTS	
SIGNAL	ORIGIN
-Y CD RST A	69
-Y CD RST B	69
-Y DATA DIS IN	60
-Y DTDOR CP1	66
-Y DTDOR CP2	66
-Y DTDOR CP3	66
-Y DTDOR CP4	66

REVISIONS			
SYMBOL	REVISION	DATE	APPROVAL
66118-KT	RELEASE	11/14	
A 66118-BPT	REDRAWN WITH CHANGE	7/13	YODER

6900906

DATE	DESCRIPTION
05.02.17.1	
05.02.18.1	
05.02.19.1	
05.02.20.1	
05.02.21.1	
05.02.22.1	
05.02.23.1	

REFERENCE DRAWING

QTY	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CON	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED	PARTS		INTERNATIONAL BUSINESS MACHINES CORP.		
OUTSIDE	MIN	MAX	7/2/64		FEDERAL SYSTEMS DIVISION		
INSIDE	MIN	MAX	7/2/64		300 MADISON AVE.		
ALL DIMENSIONS AND TOLERANCES		DESIGN CHECK	7/2/64		NEW YORK 22, N. Y.		
APPLY TO UNLESS NOTED		DRAWN	7/2/64		TITLE		
DRILL DIMENSIONS SPECIFY DRILLINGS		MIDSTATE		DATA DISPLAY REGISTER			
2 PLACE DECIMALS		722-04		DRAWING CHECK			
3 PLACE DECIMALS		722-04		DESIGN APPROVAL			
ANGLES		722-04		CASE			
		722-04		DEPTH			
		722-04		DATE			
		722-04		SCALE			
		722-04		CODE IDENT NO.			
		722-04		F			
		722-04		6900906			
		722-04		SHEET 68			

Figure 10-28. PTC Second Level Logic Diagrams (Sheet 68)

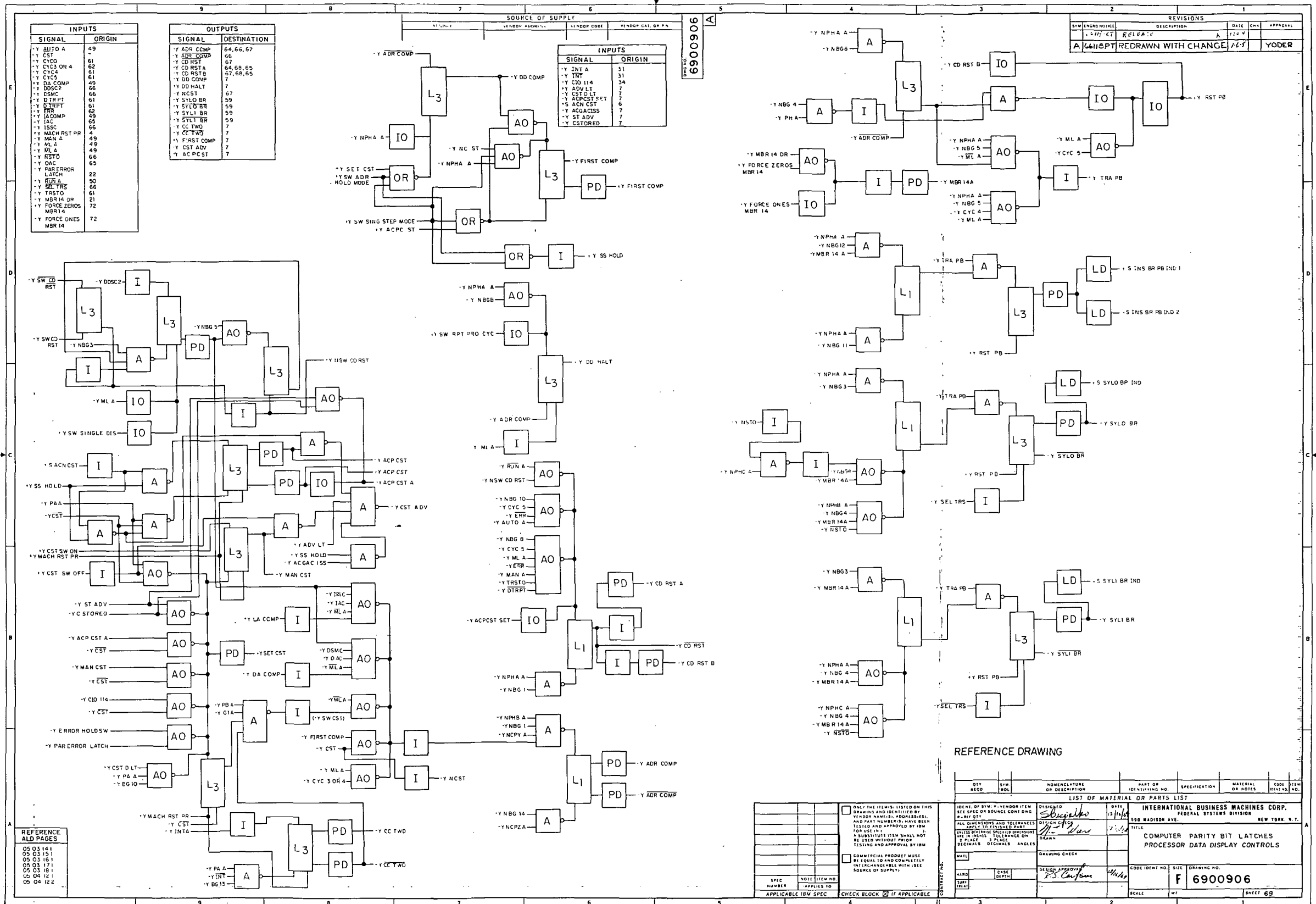


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 69)

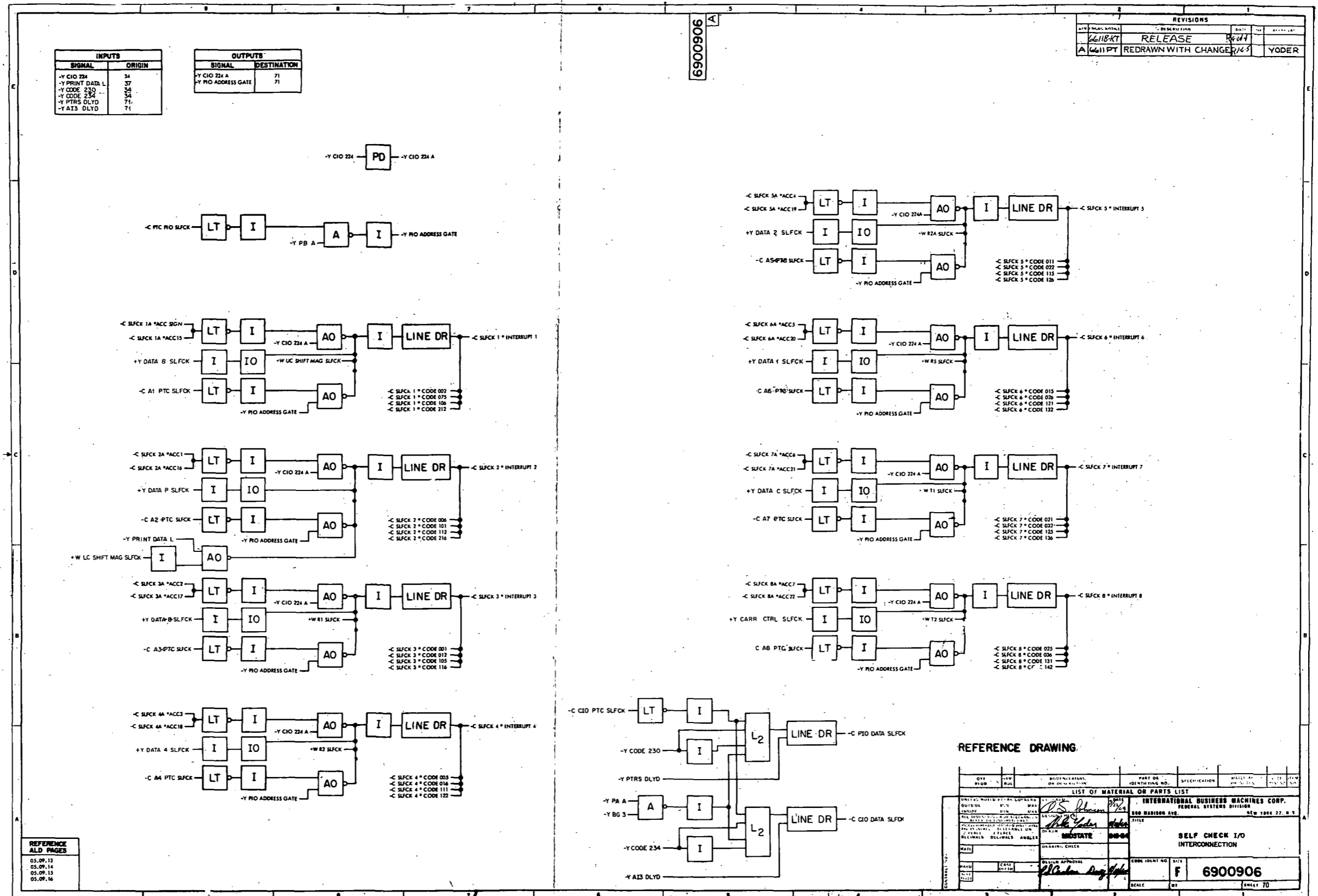


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 70)

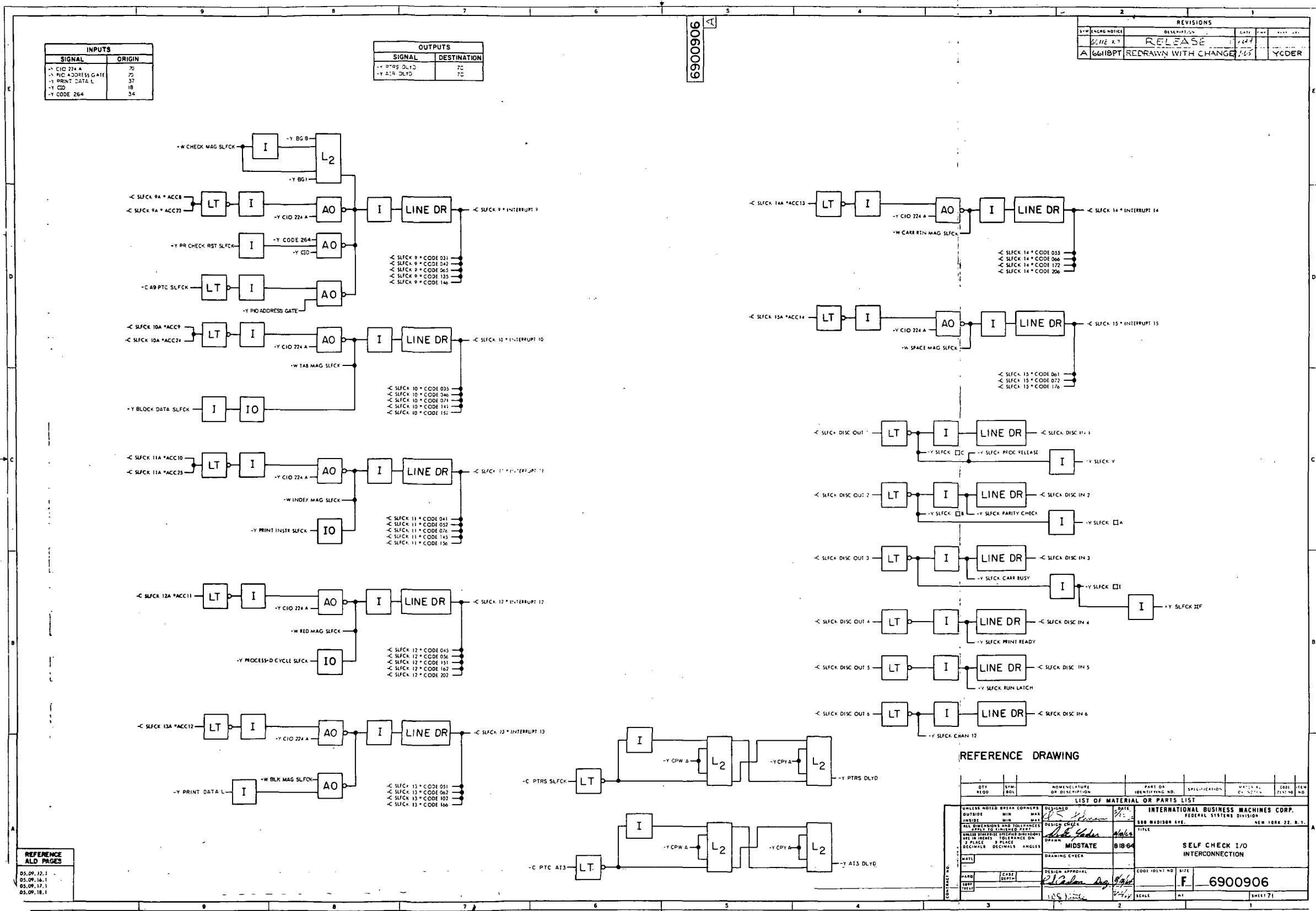


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 71)

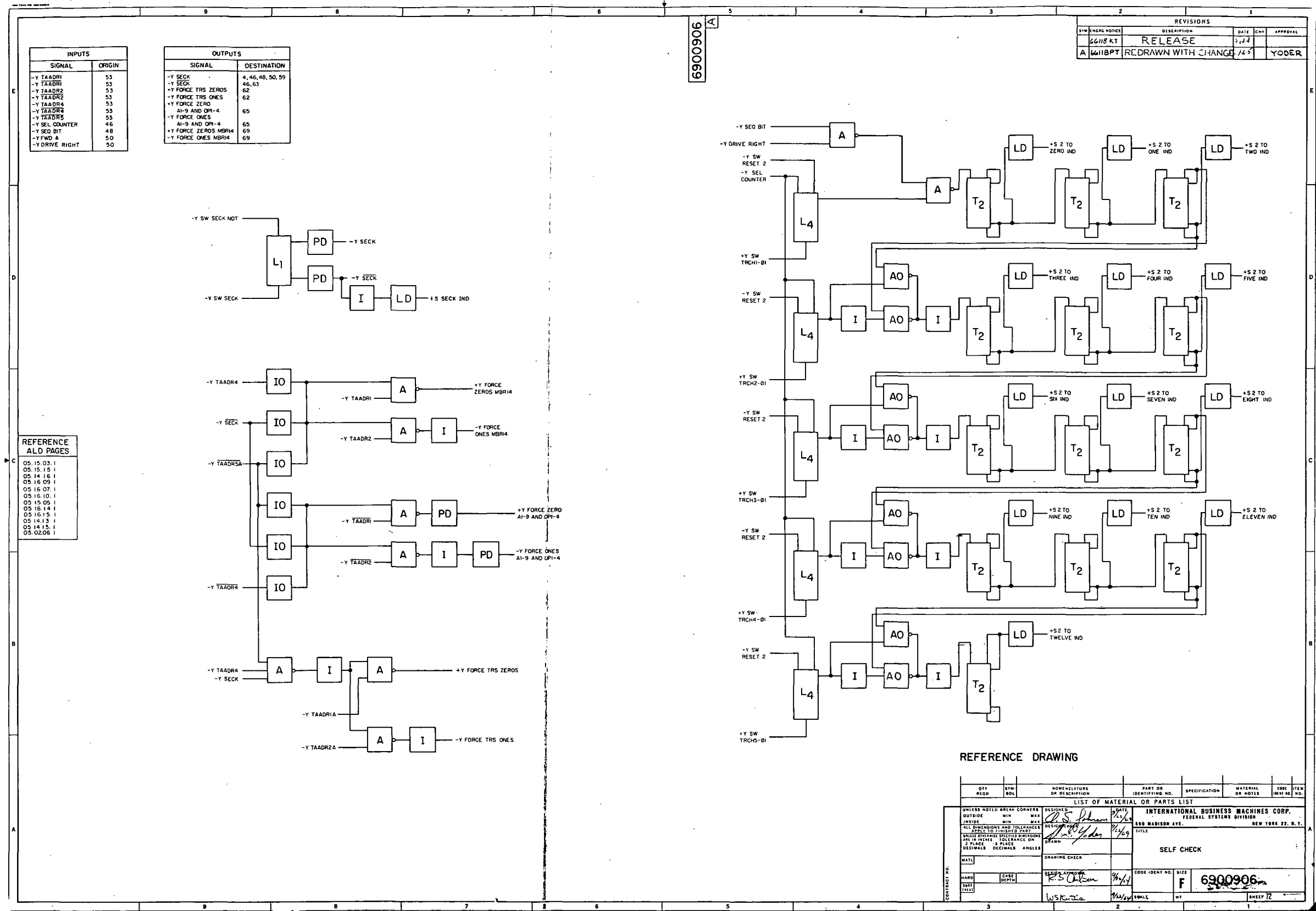
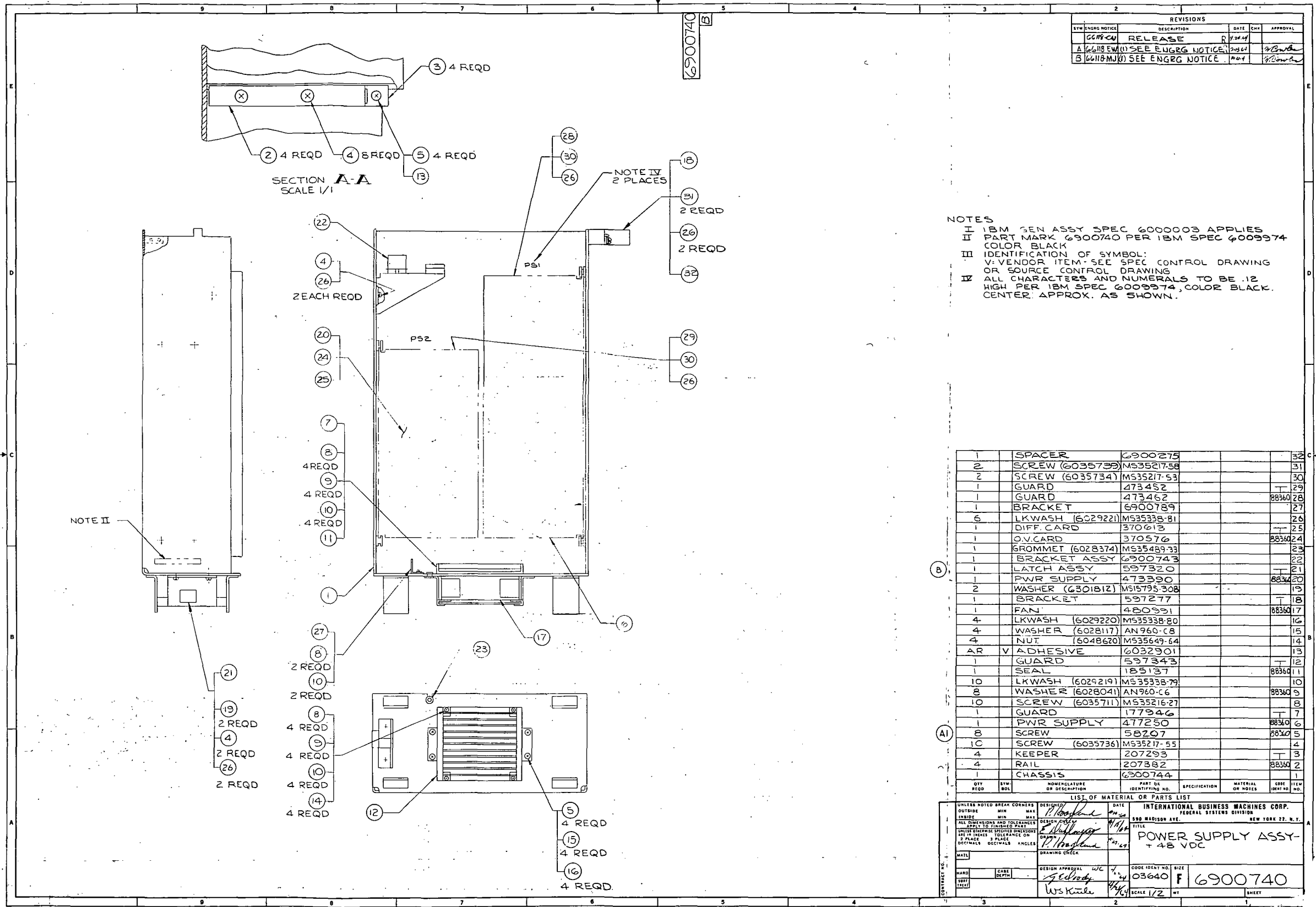


Figure 10-28. PTC Second Level Logic Diagrams (Sheet 72)



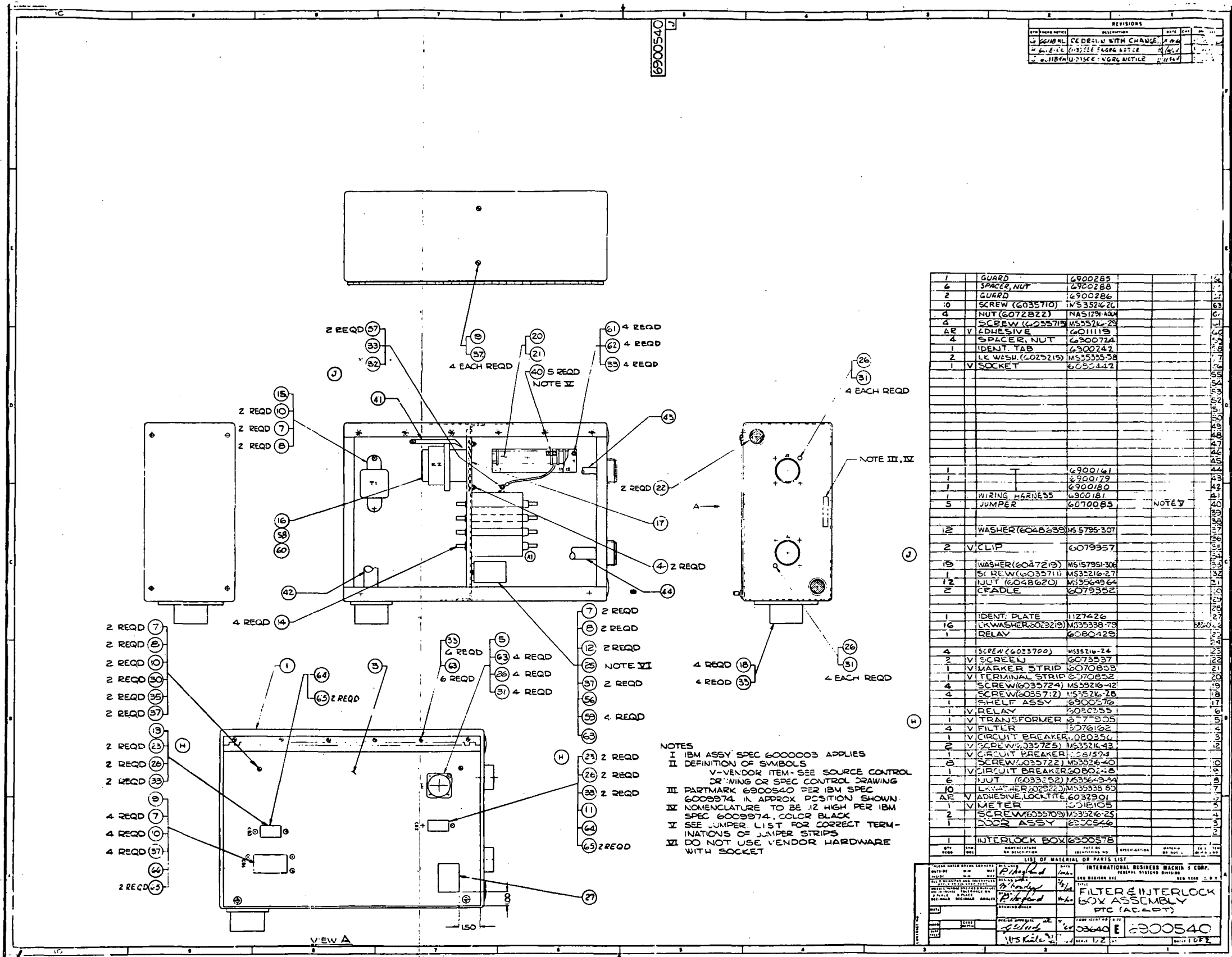
REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	66118CW	RELEASE	1/24/64	
A	66118EW	(1) SEE ENGRG NOTICE	2/25/64	
B	66118MJ	(1) SEE ENGRG NOTICE	1/24/64	

NOTES
 I IBM GEN ASSY SPEC 6000003 APPLIES
 II PART MARK 6900740 PER IBM SPEC 6009974
 COLOR BLACK
 III IDENTIFICATION OF SYMBOL:
 V: VENDOR ITEM - SEE SPEC CONTROL DRAWING
 OR SOURCE CONTROL DRAWING
 IV ALL CHARACTERS AND NUMERALS TO BE .12
 HIGH PER IBM SPEC 6009974, COLOR BLACK.
 CENTER APPROX. AS SHOWN.

QTY REQD	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
1		SPACER	6900275				32
2		SCREW (6035739)	MS35217-58				31
2		SCREW (6035734)	MS35217-53				30
1		GUARD	473452				29
1		GUARD	473462			88360	28
1		BRACKET	6900789				27
6		LKWASH (602922)	MS35338-81				26
1		DIFF CARD	370613				25
1		O.V. CARD	370576			88360	24
1		GROMMET (6028374)	MS35489-33				23
1		BRACKET ASSY	6900743				22
1		LATCH ASSY	597320				21
1		PWR SUPPLY	473390			88360	20
2		WASHER (6301812)	MS15795-308				19
1		BRACKET	597277				18
1		FAN	480991			88360	17
4		LKWASH (602922)	MS35338-80				16
4		WASHER (6028117)	AN960-C8				15
4		NUT (6048620)	MS35649-64				14
AR		V ADHESIVE	6032901				13
1		GUARD	597343				12
1		SEAL	185137			88360	11
10		LKWASH (6029219)	MS35338-79				10
8		WASHER (6028041)	AN960-C6			88360	9
10		SCREW (6035711)	MS35216-27				8
1		GUARD	177946				7
1		PWR SUPPLY	477250			88360	6
8		SCREW	58207			88360	5
10		SCREW (6035736)	MS35217-55				4
4		KEEPER	207293				3
4		RAIL	207382			88360	2
1		CHASSIS	6900744				1

UNLESS NOTED BREAK CORNERS		DATE		INTERNATIONAL BUSINESS MACHINES CORP.	
OUTSIDE	MIN	MAX	DESIGNED BY	DATE	FEDERAL SYSTEMS DIVISION
			<i>[Signature]</i>	1/24/64	550 MADISON AVE. NEW YORK 22, N.Y.
APPLY TO FINISHED PART		DESIGN CHECKED BY		TITLE	
		<i>[Signature]</i>		POWER SUPPLY ASSY -	
UNLESS OTHERWISE SPECIFIED CORNERS		DRAWN BY		+ 48 VDC	
ARE IN INCHES TOLERANCE ON		<i>[Signature]</i>			
2 PLACES DECIMALS ANGLES		DRAWING CHECKED			
		<i>[Signature]</i>			
		DESIGN APPROVAL		CODE IDENT NO. SIZE	
		<i>[Signature]</i>		F 6900740	
		SCALE 1/2		SHEET	
		<i>[Signature]</i>			

Figure 10-29. Power Supply Assembly (01B4) Assembly Drawing



REV	DESCRIPTION	DATE	BY
1	GENERAL FEDERAL WITH CHANGE	1/1/64	
2	ADDED 1-10-64	1/10/64	
3	ADDED 1-10-64	1/10/64	

QTY	DESCRIPTION	PART NO.	UNIT	REMARKS
1	GUARD	6900285		
4	SPACER, NUT	6900288		
2	GUARD	6900286		
10	SCREW (6035710)	MS3526-26		
4	NUT (6072822)	MS179-4004		
4	SCREW (6035719)	MS5526-25		
AR	V ADHESIVE	601119		
4	SPACER, NUT	6900724		
1	IDENT. TAB	6900742		
2	LK WASH (6029215)	MS3535-38		
1	V SOCKET	6900442		
1		6900141		
1		6900179		
1		6900180		
1	WIRING HARNESS	6900181		
5	JUMPER	6070085		NOTE 7
12	WASHER (6048639)	MS5795-307		
2	V CLIP	6079357		
15	WASHER (6047219)	MS5795-306		
1	SCREW (6035711)	MS3526-27		
12	NUT (6048620)	MS35649-64		
2	CFADLE	6079352		
1	IDENT. PLATE	1127426		
16	LK WASHER (603219)	MS3538-79		
1	RELAY	6060429		
4	SCREW (6035700)	MS5526-24		
2	V SCREEN	6075537		
1	V MARKER STRIP	6070853		
1	V TERMINAL STRIP	6070852		
4	SCREW (6035724)	MS3526-42		
4	SCREW (6035712)	MS5526-26		
1	SHELF ASSY	6900376		
1	V RELAY	6050355		
1	V TRANSFORMER	6075335		
4	V FILTER	6076162		
1	V CIRCUIT BREAKER	603252		
2	V SCREW (6035725)	MS3526-43		
1	V CIRCUIT BREAKER	603254		
2	SCREW (6035722)	MS3526-40		
6	NUT (603252)	MS35649-44		
10	LK WASHER (602822)	MS3538-80		
AR	V ADHESIVE, LOCKTITE	6032901		
1	V METER	6018105		
2	SCREW (6035709)	MS3526-25		
1	DOOR ASSY	6900546		

NOTES
 I IBM ASSY SPEC 6000003 APPLIES
 II DEFINITION OF SYMBOLS
 V-VENDOR ITEM-SEE SOURCE CONTROL
 OR WIRING OR SPEC CONTROL DRAWING
 6008974 IN APPROX POSITION SHOWN
 III PARTMARK 6900540 PER IBM SPEC
 6008974 IN APPROX POSITION SHOWN
 IV NOMENCLATURE TO BE .12 HIGH PER IBM
 SPEC 6008974, COLOR BLACK
 V SEE JUMPER LIST FOR CORRECT TERM-
 INATIONS OF JUMPER STRIPS
 VI DO NOT USE VENDOR HARDWARE
 WITH SOCKET

LIST OF MATERIAL OR PARTS LIST

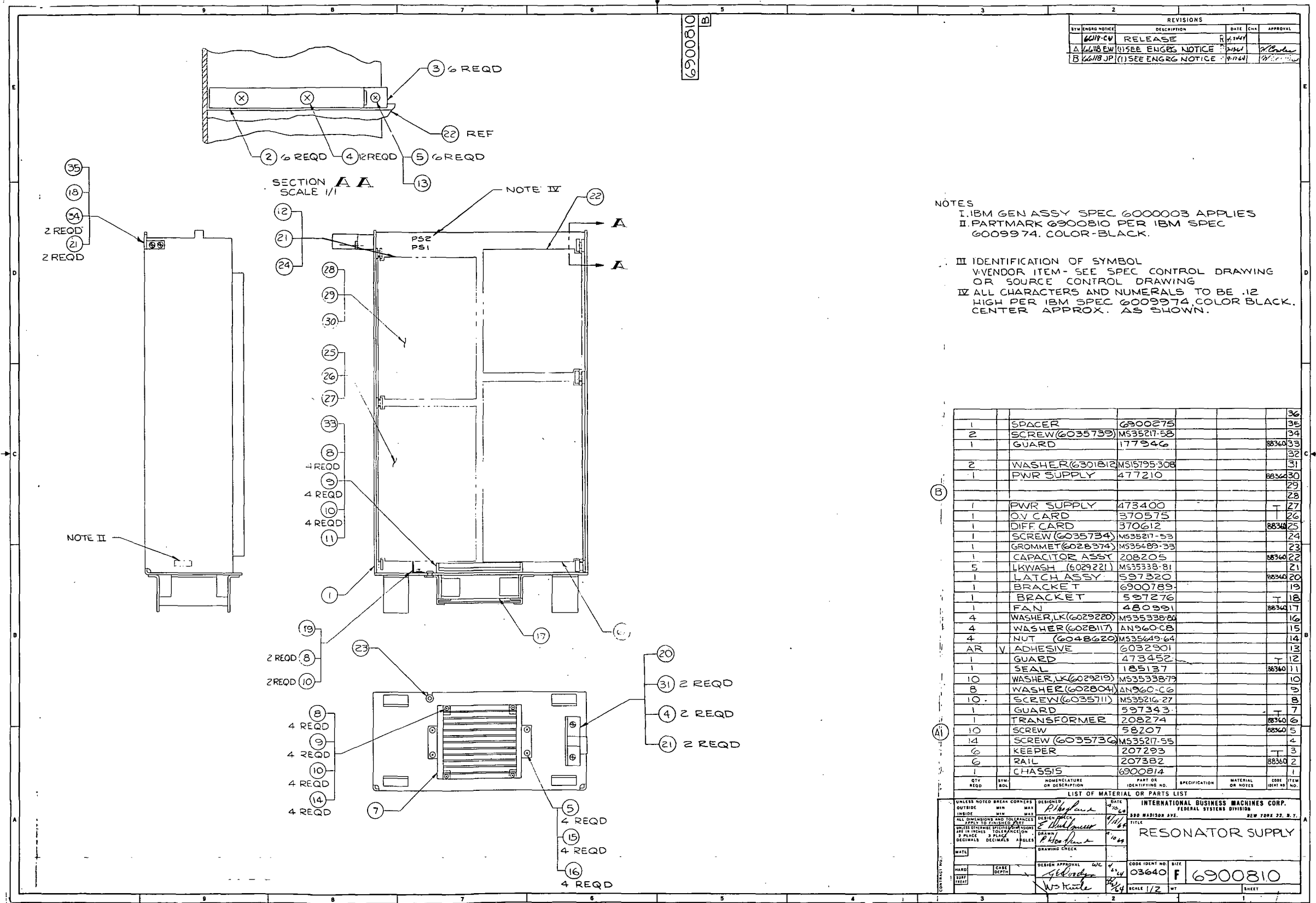
INTERNATIONAL BUSINESS MACHINES CORP.
 FEDERAL SYSTEMS DIVISION

DATE: 1/1/64
 BY: [Signature]
 CHECKED: [Signature]
 APPROVED: [Signature]

PROJECT: FILTER & INTERLOCK BOX ASSEMBLY
 PTC (ADAPT)

FORM 100-100-1
 1-64
 6900540

Figure 10-30. Filter and Interlock Box Assembly (01B5) Assembly Drawing



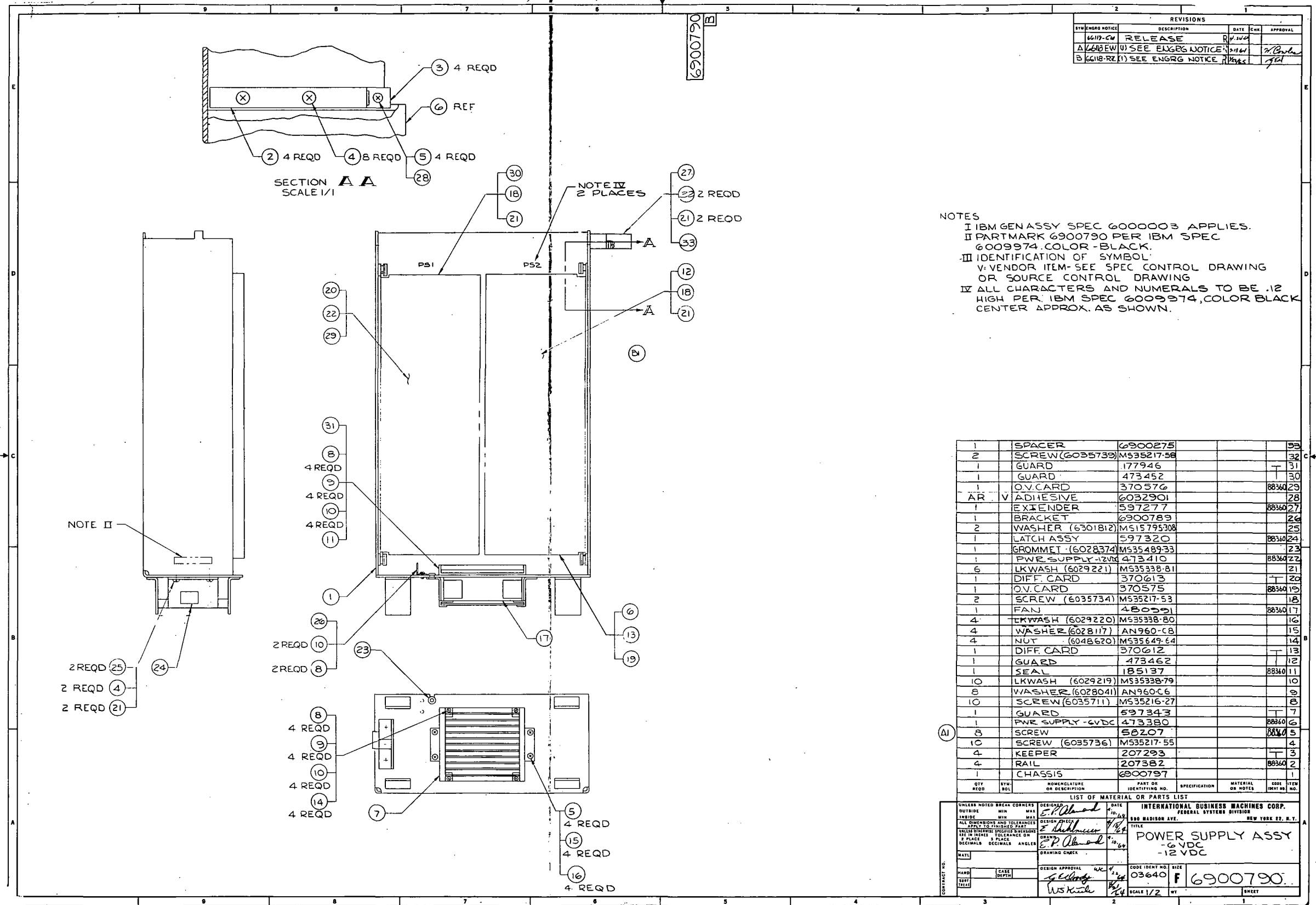
REVISIONS				
REV	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
6018 CV		RELEASE	11/14/64	
A 6618 EW	(1) SEE ENGRG NOTICE		9-11-64	
B 6618 JP	(1) SEE ENGRG NOTICE		9-11-64	

NOTES
 I. IBM GEN ASSY SPEC 6000003 APPLIES
 II. PARTMARK 6900810 PER IBM SPEC 6009974. COLOR-BLACK.
 III. IDENTIFICATION OF SYMBOL
 VENDOR ITEM- SEE SPEC CONTROL DRAWING OR SOURCE CONTROL DRAWING
 IV. ALL CHARACTERS AND NUMERALS TO BE .12 HIGH PER IBM SPEC 6009974. COLOR BLACK. CENTER APPROX. AS SHOWN.

QTY REQD	SYM	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
1		SPACER	6900275				36
2		SCREW (6035739)	M535217-58				34
1		GUARD	177946			88360	33
2		WASHER (6301812)	MS15795308				31
1		PWR SUPPLY	477210			88360	30
1		PWR SUPPLY	473400				28
1		O.V. CARD	370575				27
1		DIFF CARD	370612			88360	26
1		SCREW (6035734)	M535217-53				25
1		GROMMET (6028374)	M535489-33				24
1		CAPACITOR ASSY	208205			88360	23
5		LKWASH (6029221)	M535338-81				22
1		LATCH ASSY	597320			88360	21
1		BRACKET	6900789				20
1		BRACKET	597276				19
1		FAN	480991			88360	18
4		WASHER LK (6029220)	M535338-80				17
4		WASHER (6028117)	AN960-C8				16
4		NUT (6048620)	M535649-64				15
AR	V	ADHESIVE	6032901				14
1		GUARD	473452				13
1		SEAL	185137			88360	12
10		WASHER LK (6029219)	M535338-79				11
8		WASHER (602804)	AN960-C6				10
10		SCREW (6035711)	M535216-27				9
1		GUARD	597343				8
1		TRANSFORMER	208274			88360	7
10		SCREW	58207			88360	6
14		SCREW (6035736)	M535217-55				5
6		KEEPER	207293				4
6		RAIL	207382			88360	3
1		CHASSIS	6900814				2

UNLESS NOTED BREAK CORRESPONDING TO DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED
 UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON 2 PLACE 3 PLACE DECIMALS DECIMALS ANGLES
 DATE: 11/14/64
 DESIGNED BY: P. H. ...
 DRAWN BY: P. H. ...
 CHECKED BY: ...
 INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION NEW YORK 22, N. Y.
 TITLE: RESONATOR SUPPLY
 CODE IDENT NO: 03640 F 6900810
 SCALE: 1/2
 SHEET: 1

Figure 10-31. Resonator Supply Assembly (01B6) Assembly Drawing



REVISIONS				
REV	DESCRIPTION	DATE	CHK	APPROVAL
6619-CW	RELEASE			
A 6618-EW	(1) SEE EXGRG NOTICE	1/14/64		
B 6618-RZ	(1) SEE ENGRG NOTICE	1/14/64		

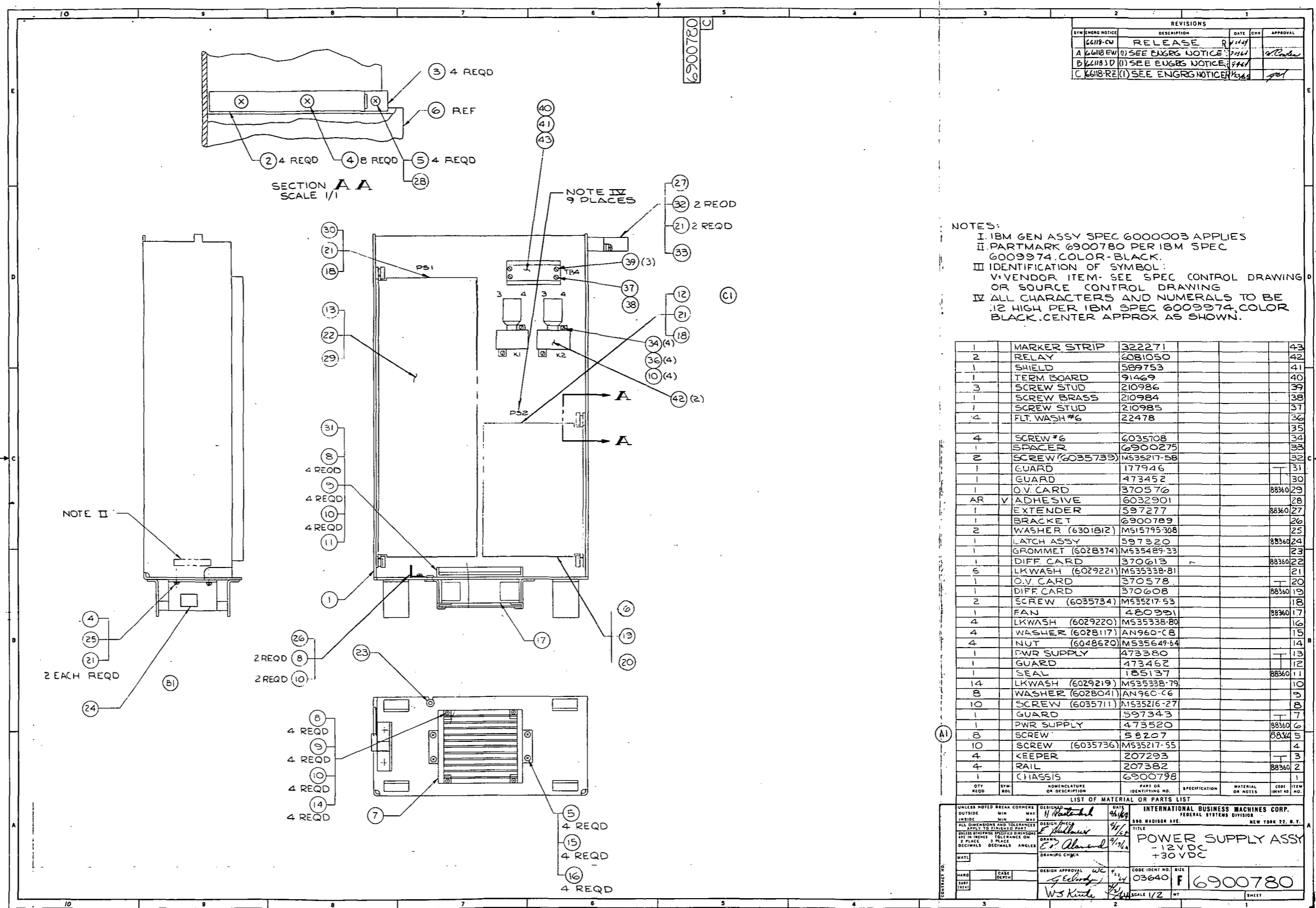
NOTES
 I IBM GENASSY SPEC 6000003 APPLIES.
 II PARTMARK 6900790 PER IBM SPEC 6009974. COLOR -BLACK.
 III IDENTIFICATION OF SYMBOL:
 V-VENDOR ITEM-SEE SPEC CONTROL DRAWING OR SOURCE CONTROL DRAWING
 IV ALL CHARACTERS AND NUMERALS TO BE .12 HIGH PER IBM SPEC 6009974. COLOR BLACK CENTER APPROX. AS SHOWN.

QTY REQD	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.
1		SPACER	6900275			99
2		SCREW (6035739)	M535217-58			32
1		GUARD	177946			31
1		GUARD	473452			30
1		O.V. CARD	370576			29
1		V ADHESIVE	6032901			28
1		EXIENDER	597277			27
1		BRACKET	6900789			26
2		WASHER (6301812)	M515795308			25
1		LATCH ASSY	597320			24
1		GROMMET (6028374)	M53548933			23
1		PWR SUPPLY -12VDC	473410			22
6		LKWASH (6029221)	M535338-81			21
1		DIFF. CARD	370613			20
1		O.V. CARD	370575			19
2		SCREW (6035734)	M535217-53			18
1		FAN	480951			17
4		LKWASH (6029220)	M535338-80			16
4		WASHER (6028117)	AN960-C8			15
4		NUT (60486620)	M535649-64			14
1		DIFF. CARD	370612			13
1		GUARD	473462			12
1		SEAL	185137			11
10		LKWASH (6029219)	M535338-79			10
6		WASHER (6028041)	AN960C6			9
10		SCREW (6035711)	M535216-27			8
1		GUARD	597343			7
1		PWR SUPPLY -6VDC	473380			6
8		SCREW	58207			5
10		SCREW (6035736)	M535217-55			4
4		KEEPER	207293			3
4		RAIL	207382			2
1		CHASSIS	6900797			1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS	DESIGNED BY	DATE	INTERNATIONAL BUSINESS MACHINES CORP.
OUTSIDE	E. P. Oberholser	10-24-63	FEDERAL SYSTEMS DIVISION
INSIDE			380 MADISON AVE. NEW YORK 22, N.Y.
ALL DIMENSIONS AND TOLERANCES UNLESS OTHERWISE SPECIFIED	DESIGN CHECKED		TITLE
PER PLACE DECIMALS ANGLES	E. P. Oberholser	10-24-63	POWER SUPPLY ASSY
	DRIVING CHECK		-6 VDC
			-12 VDC
WATL	DESIGN APPROVAL	DATE	CODE IDENT NO.
	G. Kelly	11-24-63	03640 F
HARD	DATE	SCALE	6900790
SURF	11-24-63	1/2	
TEXT	W. Schickel	BY	SHEET

Figure 10-32. Power Supply Assembly (01B7) Assembly Drawing



REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	6619-CW	RELEASE	9/14/69	
A	6618-BW	(1) SEE ENGRG NOTICE	7/14/69	J. R. ...
B	6618-BD	(1) SEE ENGRG NOTICE	7/14/69	J. R. ...
C	6618-BE	(1) SEE ENGRG NOTICE	7/14/69	J. R. ...

NOTES:
 I. IBM GEN ASSY SPEC 6000003 APPLIES
 II. PARTMARK 6900780 PER IBM SPEC 6009974, COLOR-BLACK.
 III. IDENTIFICATION OF SYMBOL:
 V-VENDOR ITEM-SEE SPEC CONTROL DRAWING OR SOURCE CONTROL DRAWING
 IV. ALL CHARACTERS AND NUMERALS TO BE .12 HIGH PER IBM SPEC 6009974, COLOR BLACK, CENTER APPROX AS SHOWN.

QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.	QTY	SYM	DESCRIPTION	PART OR IDENTIFYING NO.
1		MARKER STRIP	322271				
2		RELAY	6081050				
1		SHIELD	589753				
1		TERM BOARD	91469				
3		SCREW STUD	210986				
1		SCREW BRASS	210984				
1		SCREW STUD	210985				
4		FLT. WASH #6	22478				
4		SCREW #6	6035708				
1		SPACER	6900275				
2		SCREW (6035739)	M535217-58				
1		GUARD	177946				
1		GUARD	473452				
1		O.V. CARD	370576				
AR	V	ADHESIVE	6032901				
1		EXTENDER	597277				
1		BRACKET	6900789				
2		WASHER (6301812)	M515795-308				
1		LATCH ASSY	597320				
1		GROMMET (6028374)	M535489-33				
1		DIFF. CARD	370613				
6		LKWASH (6029221)	M535338-81				
1		O.V. CARD	370578				
1		DIFF. CARD	370608				
2		SCREW (6035734)	M535217-53				
1		FAN	480991				
4		LKWASH (6029220)	M535338-80				
4		WASHER (6028117)	AN960-C8				
4		NUT (6048620)	M535649-64				
1		PWR SUPPLY	473380				
1		GUARD	473462				
1		SEAL	185137				
14		LKWASH (6029219)	M535338-79				
8		WASHER (6028041)	AN960-C6				
10		SCREW (6035711)	M535216-27				
1		GUARD	597343				
1		PWR SUPPLY	473520				
8		SCREW	59207				
10		SCREW (6035736)	M535217-55				
4		KEEPER	207293				
4		RAIL	207382				
1		CHASSIS	6900798				

UNLESS NOTED BREAK CORNERS
 OUTSIDE MIN MAX
 INSIDE MIN MAX
 ALL DIMENSIONS AND TOLERANCES
 APPLICABLE TO FINISHED PART
 UNLESS OTHERWISE SPECIFIED DIMENSIONS
 IN PLACE DECIMALS TOLERANCES ON
 DECIMALS ANGLES

DESIGNED BY: H. R. ...
 DATE: 9/16/69
 CHECKED BY: E. J. ...
 DATE: 9/16/69
 DRAWING CHECKED BY: W. S. ...
 DATE: 9/16/69

INTERNATIONAL BUSINESS MACHINES CORP.
 FEDERAL SYSTEMS DIVISION
 550 MADISON AVE.
 NEW YORK 22, N. Y.

TITLE: POWER SUPPLY ASSY
 -12VDC
 +30VDC

CODE IDENT NO.: F 6900780
 SCALE: 1/2
 SHEET: 1

Figure 10-33. Power Supply Assembly (01B8) Assembly Drawing

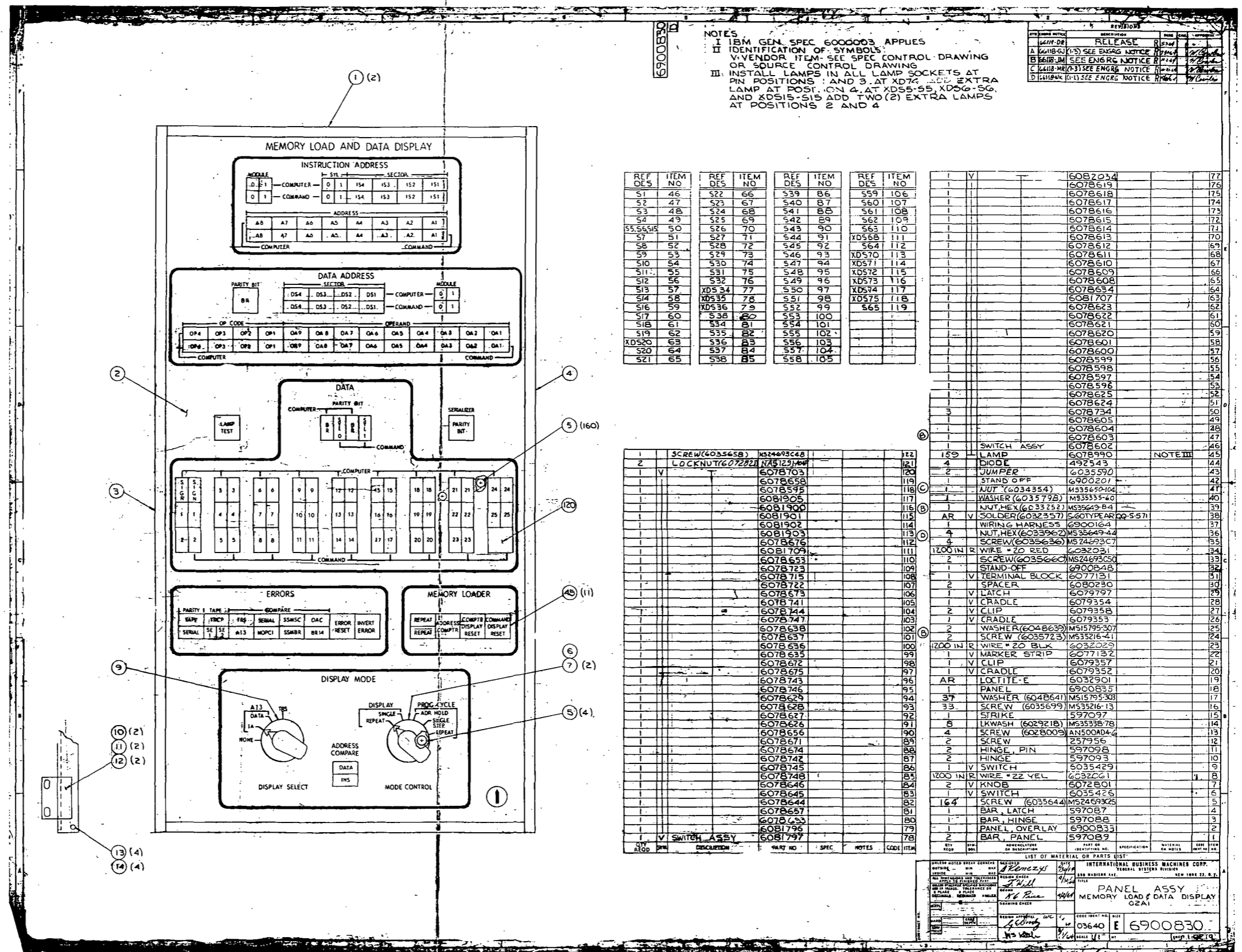
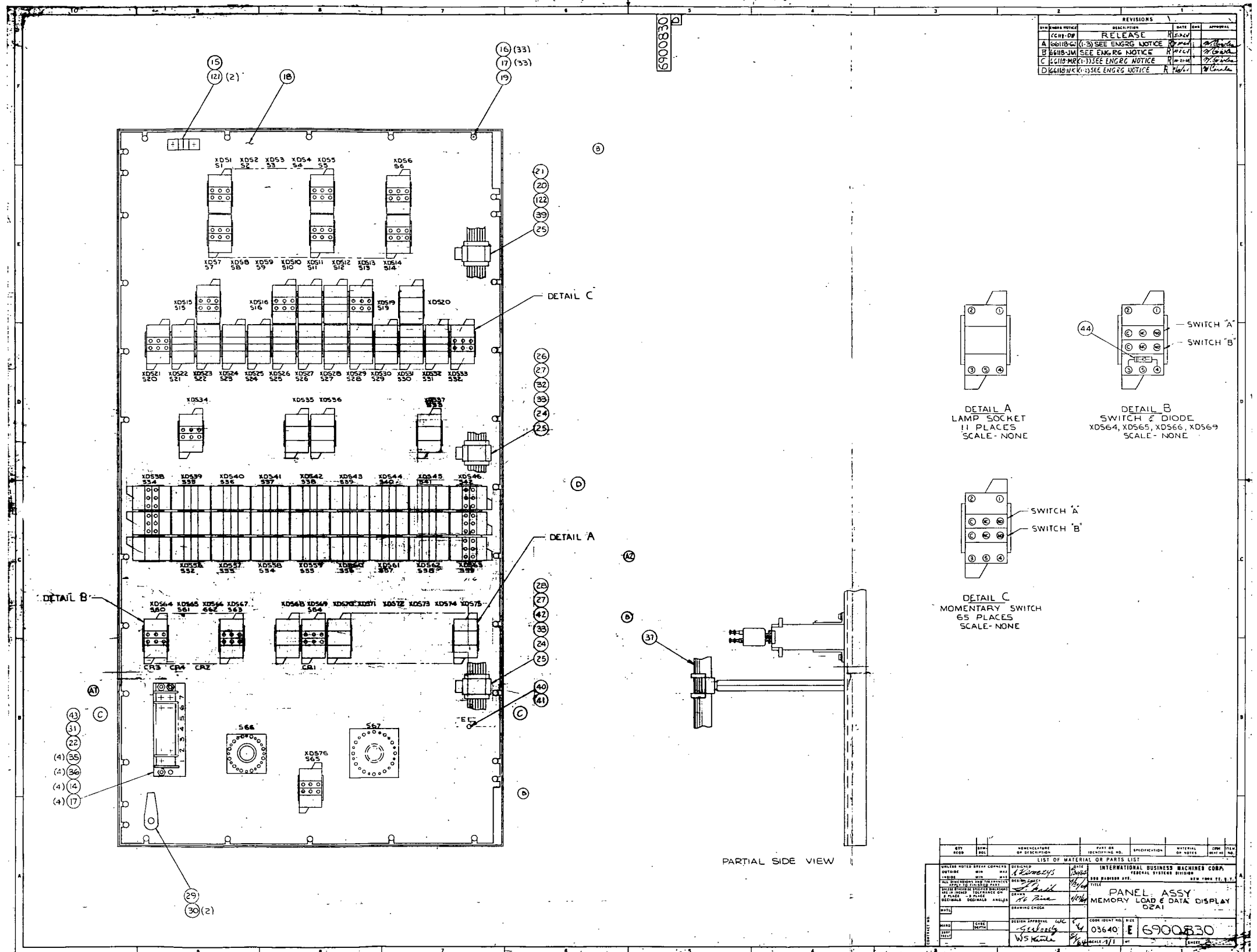
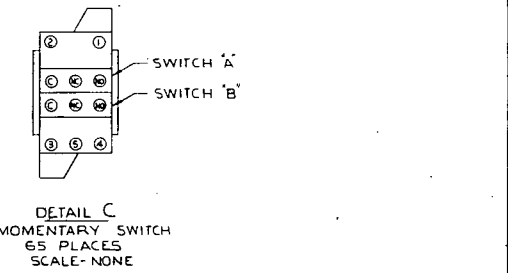
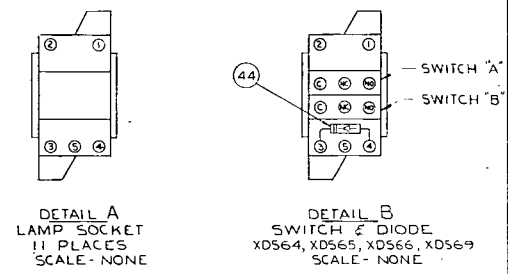


Figure 10-34. Memory Load and Data Display Panel Assembly (02A1) Assembly Drawing (Sheet 1 of 2)



REV	DESCRIPTION	DATE	BY	APP
1	RELEASE			
A	(1-3) SEE ENGRG NOTICE			
B	SEE ENGRG NOTICE			
C	SEE ENGRG NOTICE			
D	SEE ENGRG NOTICE			



PARTIAL SIDE VIEW

QTY	SYM	MANUFACTURE	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL	COM	VIEW
LIST OF MATERIAL OR PARTS LIST							
1	02A1	INTERNATIONAL BUSINESS MACHINES CORP.	03640				
PANEL ASSY MEMORY LOAD & DATA DISPLAY 02A1							
03640 E 6900830							

Figure 10-34. Memory Load and Data Display Panel Assembly (02A1) Assembly Drawing (Sheet 2)

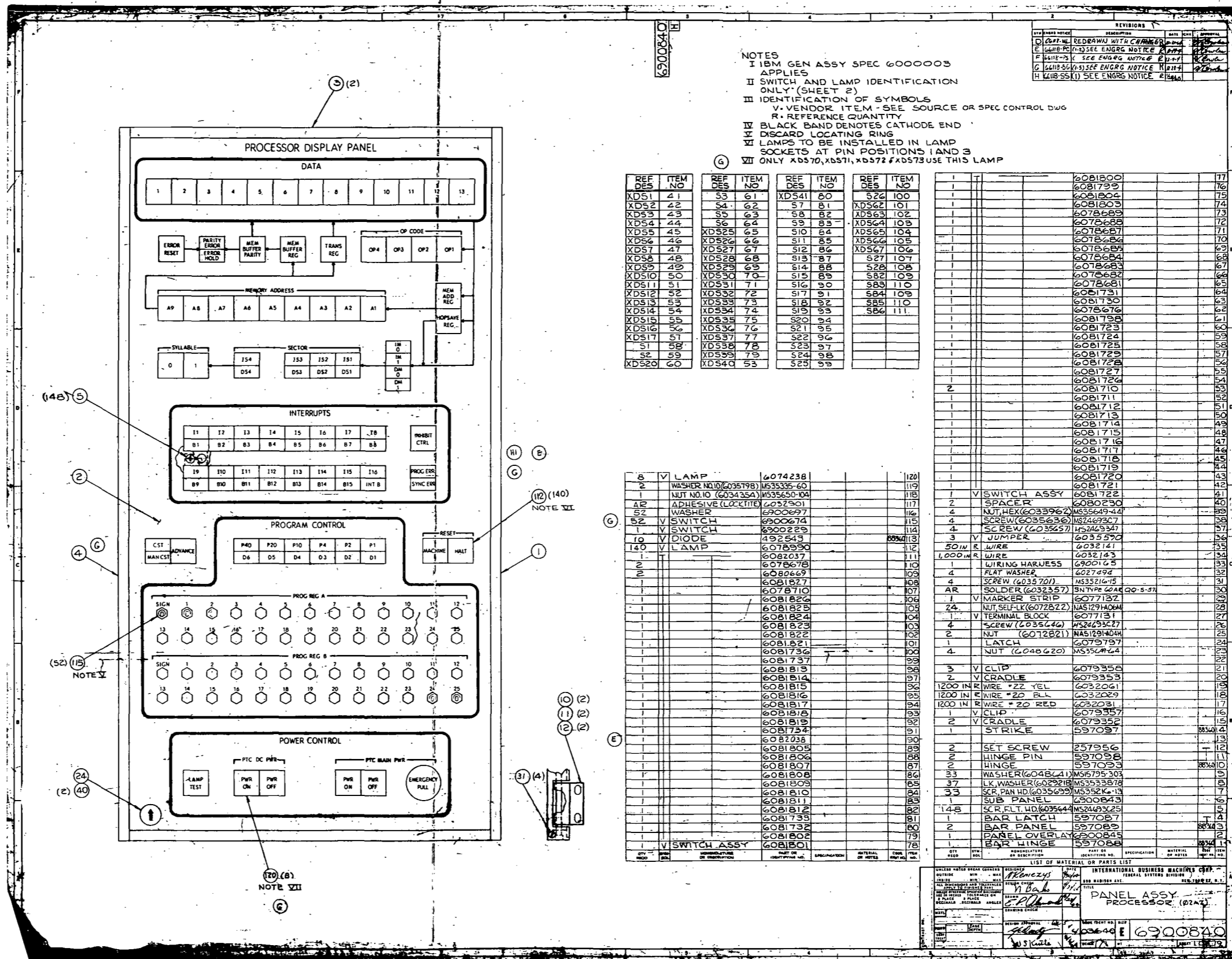
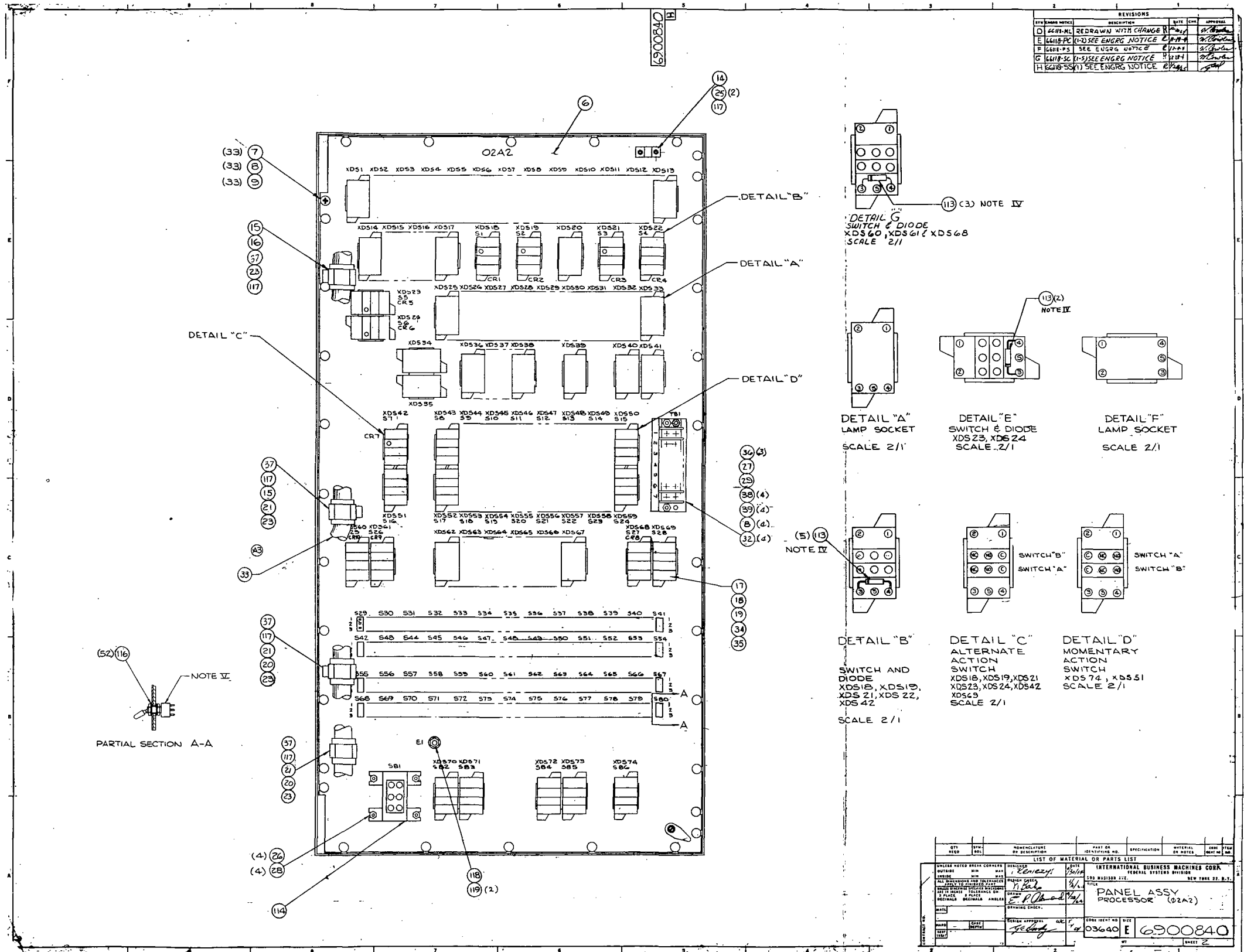


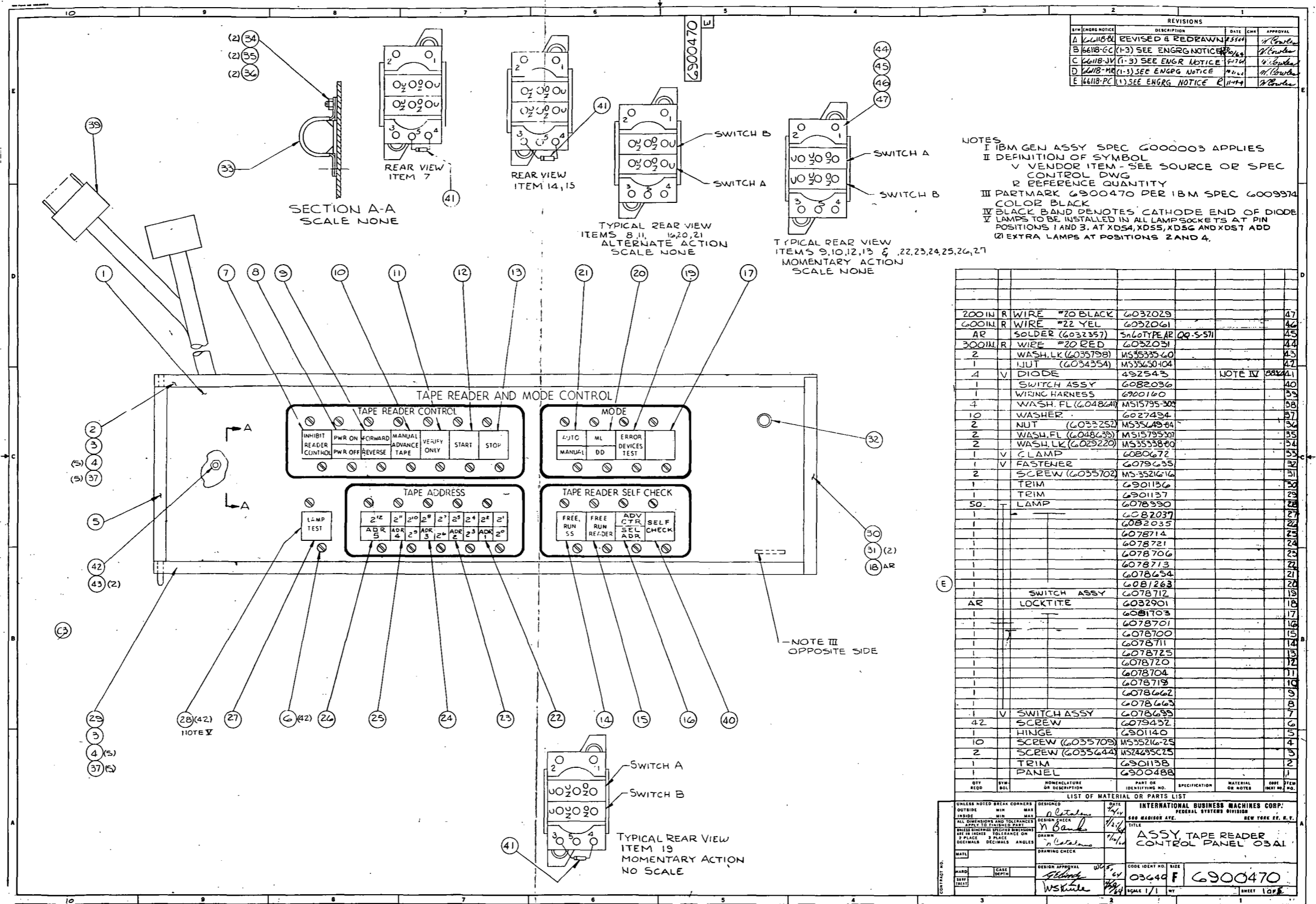
Figure 10-35. Processor Display Panel Assembly (02A2) Assembly Drawing (Sheet 1 of 2) V-10-184



REVISIONS				
REV	DATE	DESCRIPTION	BY	APP
D	6/21/61	REDRAWN WITH CHANGE	W. J.
E	6/21/61	ADD ENG. NOTICE	W. J.
F	6/21/61	SEE ENG. NOTICE	W. J.
G	6/21/61	ADD ENG. NOTICE	W. J.
H	6/21/61	SEE ENG. NOTICE	W. J.

QTY	UNIT	MANUFACTURE	PART OR	APPROXIMATE	DIFFERENTIAL	FORM	ITEM
REQ	NO.	BY DESCRIPTION	IDENTIFYING NO.	OR MODEL	OR MODEL	NO.	NO.
UNLESS NOTED OTHERWISE DISASSEMBLE DATE INTERNATIONAL BUSINESS MACHINES CORP.							
OUTSIDE MIN MAX 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61							
LINE: MIN MAX 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61 1/2/61							
ALL DIMENSIONS AND TOLERANCES UNLESS OTHERWISE SPECIFIED ARE IN INCHES							
TOLERANCES: FRACTIONS DECIMALS ANGLES							
MATERIALS: E. P. ...							
PARTS: ...							
DRAWN BY: ...							
CHECKED BY: ...							
DATE: 6/21/61							
SCALE: 2/1							
PART NO: 03640							
REV: E							
DRAWING NO: 6900840							
SHEET 2							

Figure 10-35. Processor Display Panel Assembly (02A2) Assembly Drawing (Sheet 2)



REVISIONS				
REV	ENGR NOTICE	DESCRIPTION	DATE	APPROVAL
A	66118-BL	REVISED & REDRAWN	11/24/66	W. C. ...
B	66118-CC (1-3)	SEE ENGR NOTICE	11/24/66	W. C. ...
C	66118-JV (1-3)	SEE ENGR NOTICE	11/24/66	W. C. ...
D	66118-MR (1-3)	SEE ENGR NOTICE	11/24/66	W. C. ...
E	66118-PC (1)	SEE ENGR NOTICE	11/24/66	W. C. ...

NOTES
 I IBM GEN ASSY SPEC 6000003 APPLIES
 II DEFINITION OF SYMBOL
 V VENDOR ITEM - SEE SOURCE OR SPEC
 CONTROL DWG
 R REFERENCE QUANTITY
 III PARTMARK 6900470 PER IBM SPEC 6009974
 COLOR BLACK
 IV BLACK BAND DENOTES CATHODE END OF DIODE
 V LAMPS TO BE INSTALLED IN ALL LAMP SOCKETS AT PIN POSITIONS 1 AND 3. AT XDS4, XDS5, XDS6 AND XDS7 ADD (2) EXTRA LAMPS AT POSITIONS 2 AND 4.

QTY	REV	DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	DATE	BY
200		IN R WIRE #20 BLACK	6032029				47
600		IN R WIRE #22 YEL	6032061				47
AR		SOLDER (6032357)	Sn60TYPEAR	QQ-5-571			45
300		IN R WIRE #20 RED	6032031				44
2		WASH. LK (6035798)	MS35355-60				43
1		NUT (6034354)	MS35650-104				42
4		V DIODE	482543		NOTE IV	08/21	
1		SWITCH ASSY	6082036				40
1		WIRING HARNESS	6901160				39
4		WASH. FL (6048641)	MS15795-308				38
10		WASHER	6027494				37
2		NUT (6033252)	MS35649-64				36
2		WASH. FL (6048638)	MS15795-307				35
2		WASH. LK (6029220)	MS35358-60				34
1		V CLAMP	6080672				33
1		V FASTENER	6079635				32
2		SCREW (6035702)	MS-3521616				31
1		TRIM	6901136				30
1		TRIM	6901137				29
50		LAMP	6078930				28
1			6082037				27
1			6082035				26
1			6078714				25
1			6078721				24
1			6078706				23
1			6078713				22
1			6078654				21
1			6081263				20
1		SWITCH ASSY	6078712				19
AR		LOCKTITE	6032901				18
1			6081703				17
1			6078701				16
1			6078700				15
1			6078711				14
1			6078725				13
1			6078720				12
1			6078704				11
1			6078719				10
1			6078662				9
1			6078663				8
1		V SWITCH ASSY	6078699				7
42		SCREW	6079452				6
1		HINGE	6901140				5
10		SCREW (6035709)	MS35216-25				4
2		SCREW (6035644)	MS24655-25				3
1		TRIM	6901138				2
1		PANEL	6900488				1

Figure 10-36. Tape Reader Control Panel Assembly (03A1) Assembly Drawing

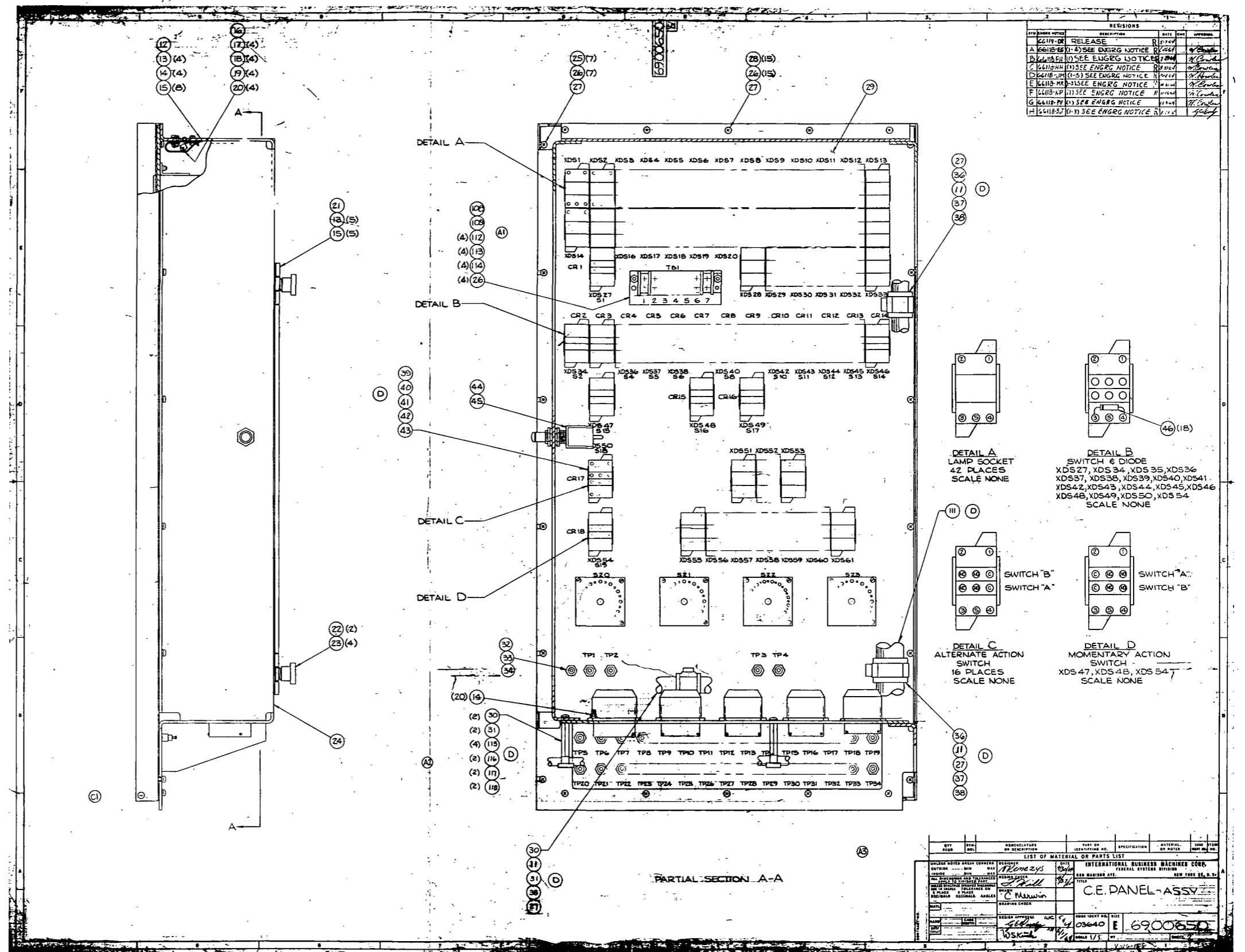


Figure 10-37. C. E. Panel Assembly
(03A4) Assembly Drawing (Sheet 2)

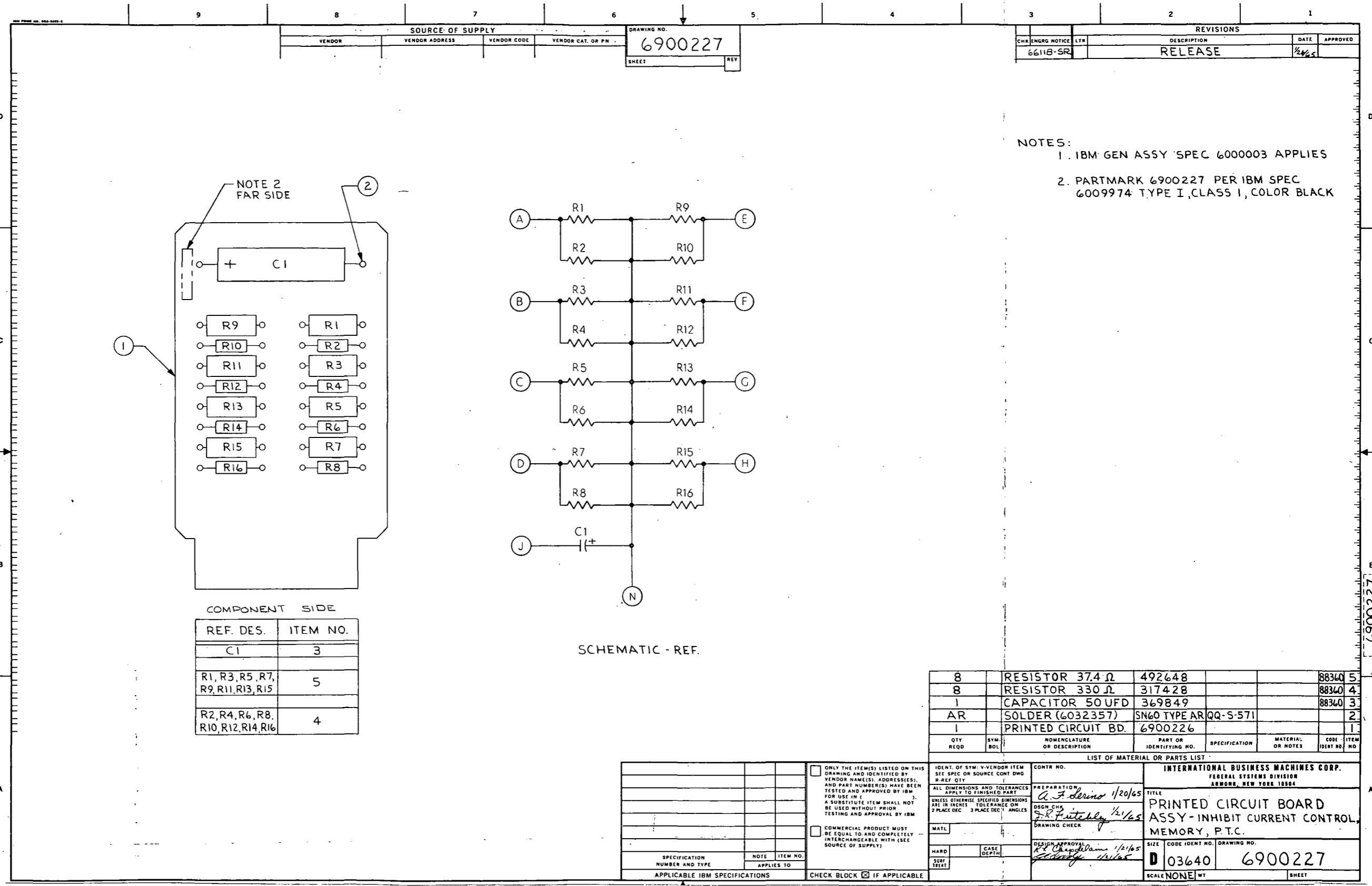
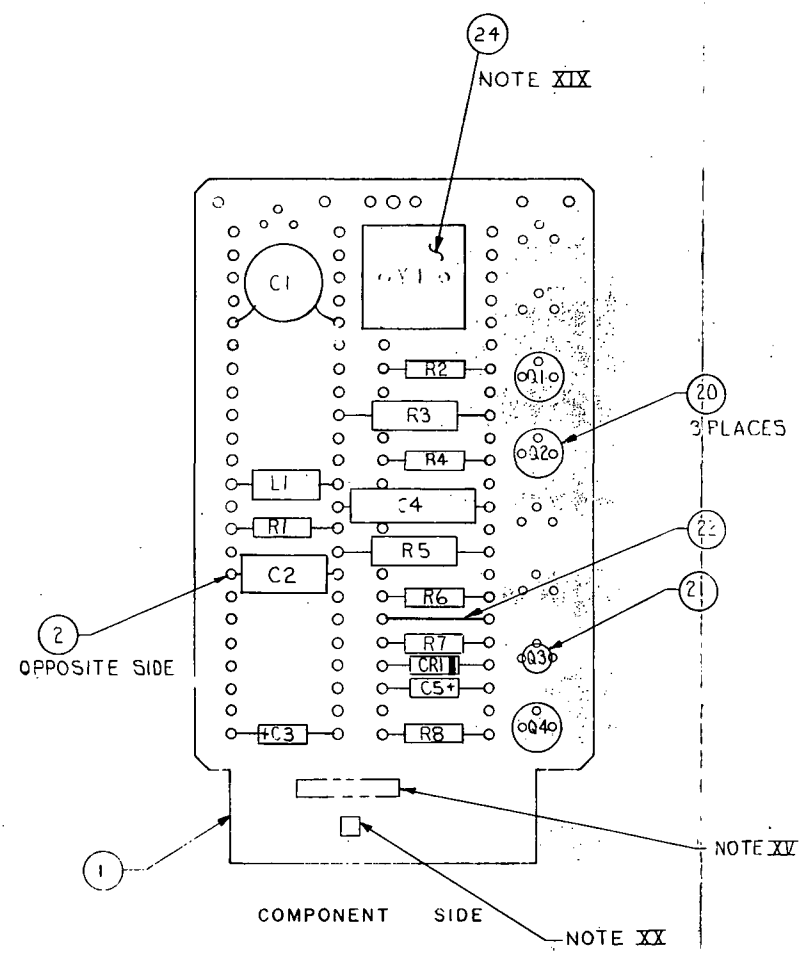


Figure 10-38. Inhibit Current Control Printed Circuit Board Assembly (6900227)

6901352 A

REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	661128N	RELEASE		
A	66115KG	(1-2) ADDED NOTES XIX AND XX AND ITEM 24 R	9264	J.E. WOOD



- NOTES
- X IBM GEN ASSY SPEC 6000003 APPLIES
 - XI MIN ELECTRICAL CLEARANCE TO BE .018
 - XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
 - XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
 - XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
 - XV PARTMARK 6901352 ASSY PER IBM SPEC 6009974, COLOR BLACK
 - XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
 - XVII BLACK BAND DENOTES CATHODE END OF DIODE
 - XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R- REFERENCE QUANTITY
 - XIX UPPER HALF OF CRYSTAL CAN SHALL BE INSULATED WITH SEALANT INDICATED PER IBM SPEC 6009341. CRYSTAL SHOULD NOT BE SUBJECTED TO TEMP OVER 150°F IN CURING

XX MARK CHANGE LEVEL TYPE I CLASS I COLOR BLACK PER SPEC 6009974

C2	23
Y1	19
Q4	18
Q3	17
Q1-Q2	16
R8	15
R7	14
R6	13
R5	12
R4	11
R3	10
R2	9
R1	8
L1	7
CRI	6
C4	5
C3, C5	4
C1	3
REF DES	ITEM NO.

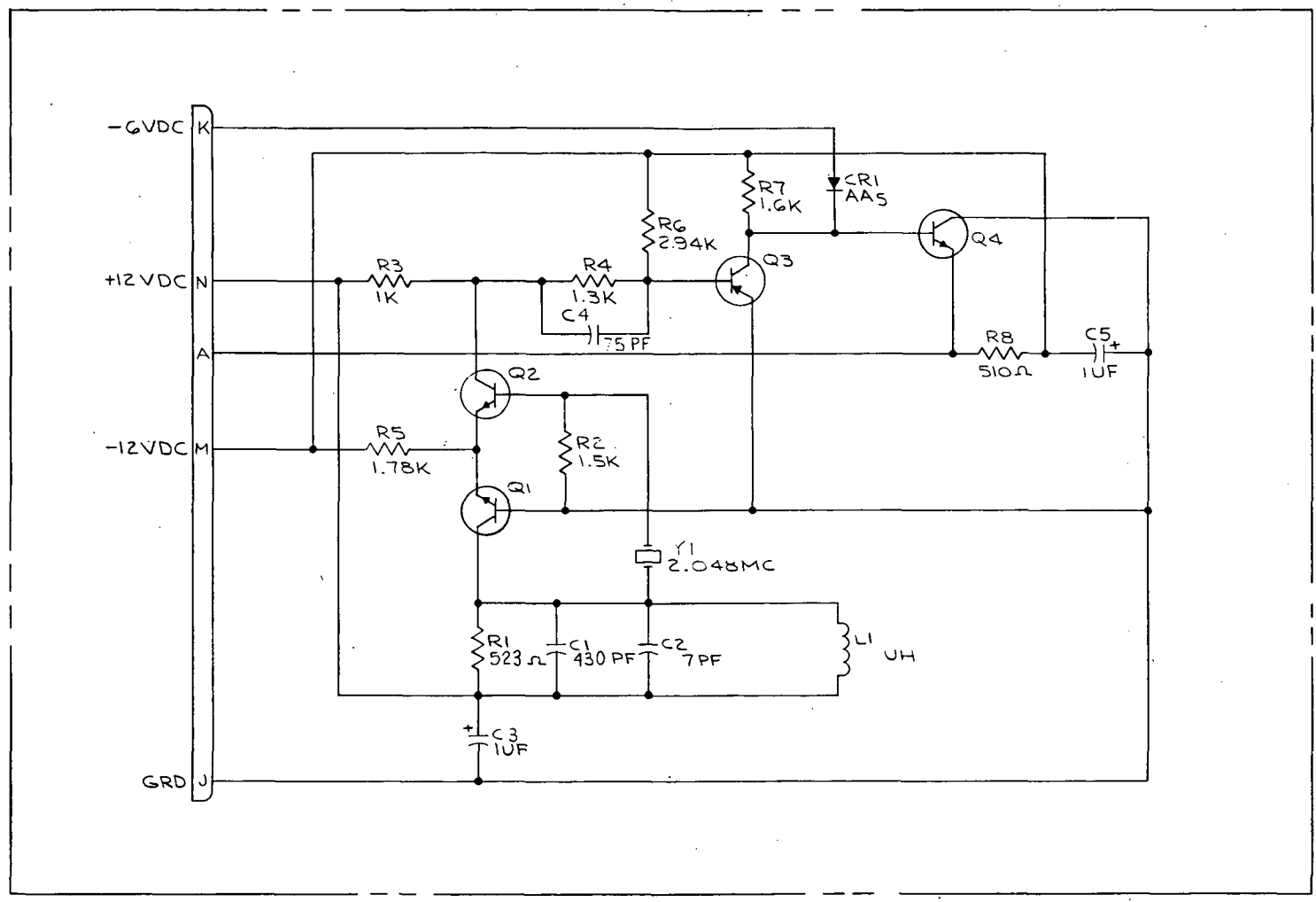
AR	V	SEALANT	6075477		24
1		CAPACITOR 7PF±5%500V	492515		88360 23
3	IN	WIRE #22AWG, YELLOW	6036152		22
1		SPACER	483070		21
3		SPACER	491299		88360 20
1	V	CRYSTAL 2.048 MC	6079504		19
1			318325		18
1			369177		17
2		TRANSISTOR	526798		16
1		510Ω ±5% 1/2W	317012		15
1		1.6K ±5% 1/2W	317018		14
1		2.94K ±1% 1/8W	479127		13
1		1.78K ±1% 1/4W	479226		12
1		1.3K ±1% 1/8W	550093		11
1		1.0K ±1% 1/4W	491010		10
1		1.5K ±5% 1/2W	317017		9
1		RESISTOR 523Ω ±1% 1/8W	491238		8
1		INDUCTOR 12 UH ±5%	217136		7
1		DIODE	491008		6
1		75PF	492464		5
2		1UF	124582		4
1		CAPACITOR 430PF±5% .00V	483309		88360 3
AR		SOLDER (6032357) Sn 60 AR	QQ-S-571		2
1		SMS CARD	6901353		1

LIST OF MATERIAL OR PARTS LIST			
UNLESS NOTED BREAK CORNERS OUTSIDE	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 500 MADISON AVE. NEW YORK 22, N.Y.
MIN	<i>J.E. Wood</i>	<i>10-27-63</i>	TITLE
MAX			PRINTED CIRCUIT BOARD ASSY - 2.048 MC. OSCILLATOR, SdTDL
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	DESIGN CHECK		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON	<i>J.E. Wood</i>	<i>10-27-63</i>	
2 PLACE DECIMALS			
3 PLACE DECIMALS			
ANGLES			
MATL	DRAWING CHECK		
HARD	DESIGN APPROVAL	<i>E. Wood</i>	CODE IDENT NO. 03640
DRY TREAT	<i>E. Wood</i>	<i>10-27-63</i>	SIZE D
			6901352
			SCALE 2/1
			SHEET 1 OF 2

Figure 10-39. SdTDL 2.048 MC Oscillator Printed Circuit Board Assembly (6901352) (Sheet 1 of 2) V-10-190

6901352 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	661128U	RELEASE	8-22-64		
A	66115K6	(1-2) ADDED NOTES XIX AND XX AND ITEM 24 R	9-26-64		J.E. WOOD



QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							
UNLESS NOTED BREAK CORNERS		DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP.			
OUTSIDE	MIN	MAX	4/1/63	FEDERAL SYSTEMS DIVISION			
INSIDE	MIN	MAX	1/16/63	590 MADISON AVE. NEW YORK 22, N. Y.			
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART		DESIGN CHECK	1/16/63	TITLE			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON		DRAWN	CC	PRINTED CIRCUIT BOARD			
2-PLACE	3-PLACE	MDEE	10/28/63	ASSY- 2.048 MC OSCILLATOR			
DECIMALS	DECIMALS	DRAWING CHECK					
MATERIAL		DESIGN APPROVAL	1/23	CODE IDENT NO.	SIZE	6901352	
HARD	CASE DEPTH	E. McLean	1-3	03640	D		
SUFF TREAT			64	SCALE	WT	SHEET 2	

Figure 10-39. SDTD 2.048 MC Oscillator Printed Circuit Board Assembly (6901352) (Sheet 2)

LOGIC SYMBOLS

In the list that follows, each type of logic symbol on the PTC ALD's is described. Each typical ALD symbol is shown with the corresponding symbol (if any) used in the simplified logic diagrams on figure 10-28; some of the circuits indicated on the ALD's (such as resistive loads and diode clamps) are not indicated on figure 10-28 because they perform no logic function.

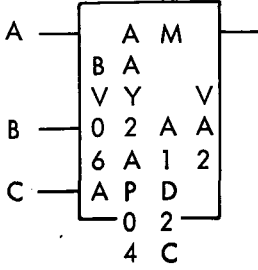
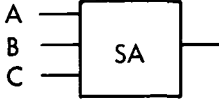
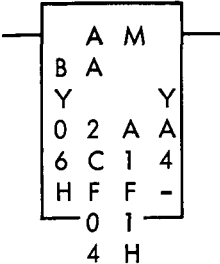

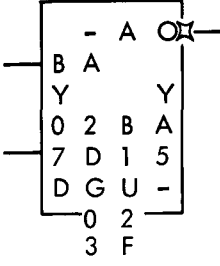

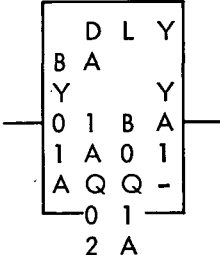
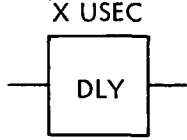
The two letters on the third line down from the top of each ALD symbol (see figure 10-6) indicate the nominal levels of input and output voltage for that circuit. The levels represented by these letters are shown in the following table.

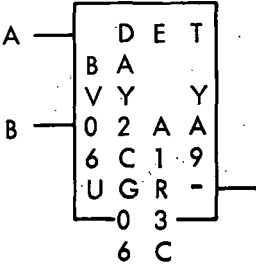
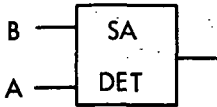
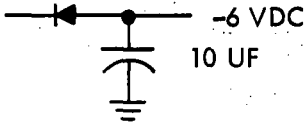
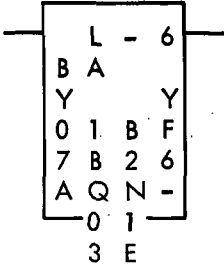
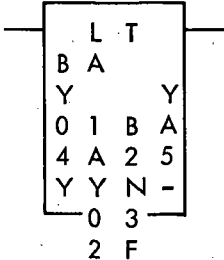
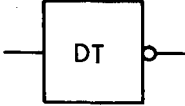
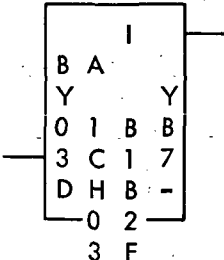

Symbol	Voltage Levels (Nominal)	
	Up Level	Down Level
C	+ 1.30 VDC	-1.25 VDC
R	+12.0 VDC	0 VDC
S	0 VDC	-12 VDC
V	Special	Special
W	0 VDC	-48 VDC
Y	0 VDC	-6 VDC

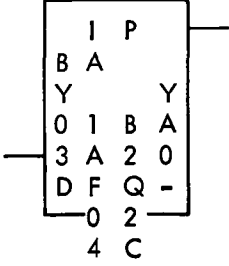
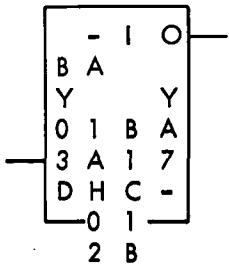
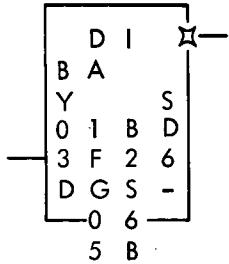
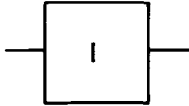
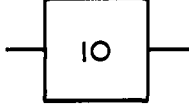
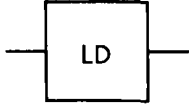
Note: The "Special" levels indicated by V are explained in the description of the logic circuits to which it applies.

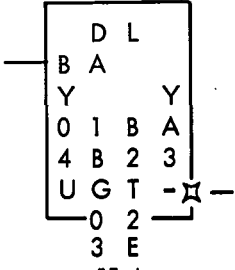

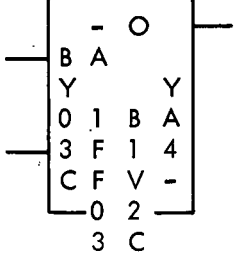
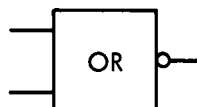
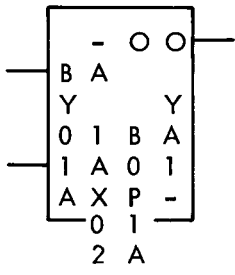
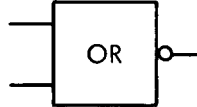
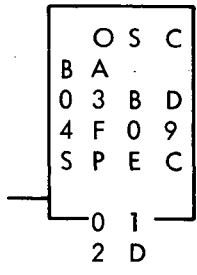
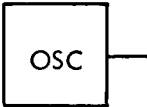
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>1. AND. The output of an AND circuit is the logical AND of its inputs. When all inputs are "1's", the output is a "1"; if any input is a "0", the output is a "0". The AND circuit may have two or more inputs.</p>		
<p>2. AND-INVERTER. This circuit performs the logical AND and INVERT functions. When all inputs are "1's", the output is a "0"; if any input is a "0", the output is a "1". The AND-INVERTER circuit may have two or more inputs.</p>		

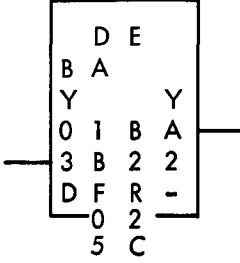

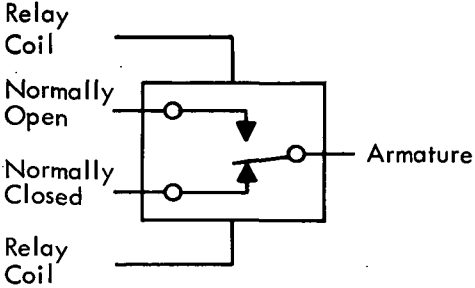
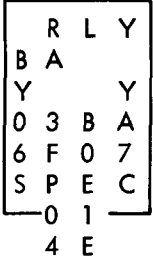
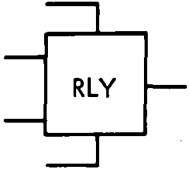
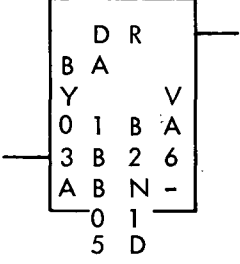

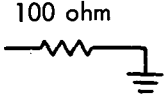
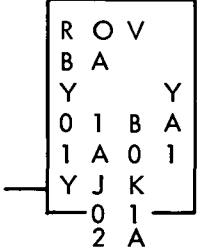
Note: The functional symbol "+O" may be substituted for "-A".

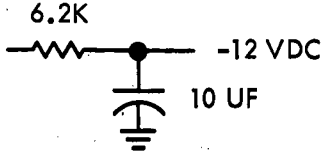
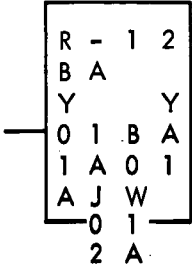
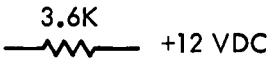
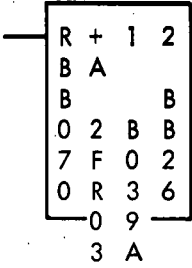
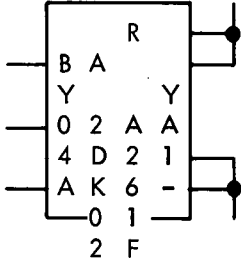
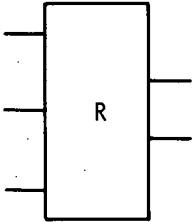
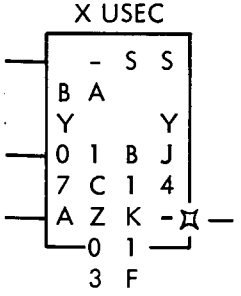
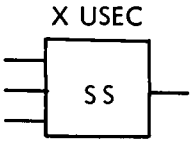
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>3. SENSE AMPLIFIER. The sense amplifier is a gated differential amplifier that senses "1's" at inputs A and B. The amplifier is enabled when input C is a "1". When a "1" is sensed at inputs A and B, the signal is amplified, rectified and sent to a detector.</p>		
<p>4. STROBE DRIVER. The strobe driver provides a signal to strobe the detectors. The strobe driver inverts and amplifies its input signal.</p>		
<p>5. AND-OR-INVERTER. This circuit performs the logical AND, OR, and INVERT functions. The relation between the inputs and outputs is the same as the AND-INVERTER circuit. However the output transistor of this circuit allows the outputs of several AND-OR-INVERTER circuits to be connected (OR'd) together. A "0" output from any AND-OR-INVERTER circuit of an "OR'd" group of circuits will force a "0" output from the group. The AND-OR-INVERTER circuit may have two or more inputs.</p>	 <p>Note The functional symbol "+O O" may be substituted for "-AO".</p>	
<p>6. DELAY. This circuit delays only the positive transition of its input; a delay occurs only when the input changes from a "1" (-6 VDC) to a "0" (0 VDC). The nominal delay duration is indicated above the symbol. A "1" input causes a "1" output.</p>	<p>X USEC</p> 	<p>X USEC</p> 

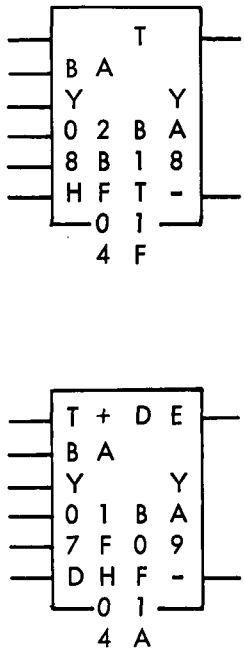
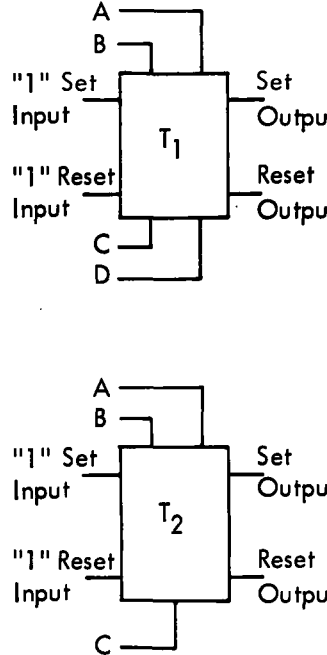
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>7. DETECTOR. This circuit is a strobed Schmitt trigger that produces a "1" output only when one of its associated sense amplifiers senses a "1" and the strobe input is a "0".</p>	 <p>Note</p> <p>The "A" input is the input from the sense amplifier and the "B" input is the strobe input.</p>	
<p>8. DIODE. This circuit is a diode clamped to -6 VDC.</p> 		<p>None</p>
<p>9. DRIVER TERMINATOR. This circuit is a signal shaper, inverter, and low impedance matching device.</p>		
<p>10. INVERTER. The output of this circuit is the inverse of its input; a "1" input results in a "0" output and vice versa.</p>		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)						
<p>11. INVERTER (POWER). This circuit performs signal inversion and amplification; a "1" input results in a "0" output and vice versa.</p> <p>12. INVERTER-OR. This circuit performs signal inversion; a "1" input results in a "0" output and vice versa. The output transistor of this circuit allows several INVERTER-OR circuits to be connected ("OR'd") together. A "0" output from any INVERTER-OR circuit of an "OR'd" group of circuits will force a "0" output from the group.</p> <p>13. LAMP DRIVER. A "1" input causes the LAMP DRIVER to turn on its associated indicator lamp; a "0" input causes the LAMP DRIVER to turn off its associated indicator lamp. The input-output levels are as follows:</p> <table border="1" data-bbox="162 1323 568 1449"> <thead> <tr> <th>Input</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>"1" (-6 VDC)</td> <td>0 VDC</td> </tr> <tr> <td>"0" (0 VDC)</td> <td>-12 VDC</td> </tr> </tbody> </table> <p>Note</p> <p>One side of the indicator lamp is connected to -12 VDC; the other side is connected to the output of the LAMP DRIVER. When the output of the LAMP DRIVER is 0 VDC, the potential difference of volts across the lamp lights the lamp.</p>	Input	Output	"1" (-6 VDC)	0 VDC	"0" (0 VDC)	-12 VDC	<div style="text-align: center;">  </div> <div style="text-align: center; margin-top: 20px;">  </div> <div style="text-align: center; margin-top: 20px;">  </div> <p style="text-align: center;">Note</p> <p>The "DI" functional symbol represents "Driver, Indicator".</p>	<div style="text-align: center; margin-top: 100px;">  </div> <div style="text-align: center; margin-top: 100px;">  </div> <div style="text-align: center; margin-top: 100px;">  </div>
Input	Output							
"1" (-6 VDC)	0 VDC							
"0" (0 VDC)	-12 VDC							

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>14. LINE DRIVER. This circuit functions as a signal driver and low impedance matching device.</p>	 <p>Note</p> <p>The "DL" functional symbol represents "Driver, Line".</p>	
<p>15. OR-INVERTER. This circuit performs the logical OR and INVERT functions. When all inputs are "0's", the output is a "1"; if any input is a "1", the output is a "0". This circuit may have two or more inputs.</p>	 <p>Note: The functional symbol "+A" may be substituted for "-O".</p>	
<p>16. OR-INVERTER-OR. This circuit functions in the same manner as the OR-INVERTER. The outputs of many OR-INVERTER-OR's may be connected (OR'd) together. A "0" output from any OR-INVERTER-OR circuit of an "OR'd" group of circuits will force a "0" output from the group. This circuit may have two or more inputs.</p>		
<p>17. OSCILLATOR. This circuit generates a square wave signal (0 VDC to -6 VDC) at a 2.048 MC frequency.</p>		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>18. POWER DRIVER. This circuit provides circuit matching and power amplification. A "1" input causes a "1" output; a "0" input causes a "0" output.</p>	 <p>Note</p> <p>The "DE" functional symbol represents "Driver, Emitter". The output portion of this circuit is an emitter follower.</p>	
<p>19. RELAY</p> 		
<p>20. RELAY DRIVER. This circuit functions as a level shifter to enable a "1" to energize a relay coil.</p>	 <p>Note: The "DR" functional symbol represents "Driver, Relay".</p>	
<p>21. RESISTOR. This circuit is a 100 ohm resistor connected to ground.</p> 		<p>None</p>

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>22. RESISTOR. This circuit is a 6.2K resistor connected to -12 VDC.</p> 		<p>None</p>
<p>23. RESISTOR. This circuit is a 3.6K resistor connected to +12 VDC.</p> 		<p>None</p>
<p>24. THERMAL RESISTOR NETWORK. Resistors in this network are shunted across the memory current supply to control the drive current supplied to the memory core array.</p>		
<p>25. SINGLE SHOT. Any or all of the inputs may be connected; an unconnected input (indicated by the absence of that input) is effectively a "1" input. All inputs must be "1's" to trigger the SINGLE SHOT. The negative-going transition of the last input to become a "1" triggers the single shot, forcing it to produce a negative output pulse whose negative transition is coincident with the triggering transition of its input. The nominal duration of the pulse is shown above the symbol.</p>		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-28)
<p>26. TRIGGER 1. This circuit is a bistable device that becomes set (1) if the "1" Set Input becomes a "1" or, (2) if input A is a "0" and input B changes from a "1" to a "0". Similarly, the circuit becomes reset (1) if the "1" Reset Input becomes a "1" or, (2) if input D is a "0" and input C changes from a "1" to a "0".</p> <p>27. TRIGGER 2. This circuit is very similar to the TRIGGER 1. The basic difference is that the circuit becomes reset when input C is a "0" and input B changes from a "1" to a "0". This circuit also provides power amplification.</p>	 <p>Note</p> <p>The functional symbol "T + DE" represents "Trigger and Driver, Emitter".</p>	

GLOSSARY

In the list that follows, each signal name used on the PTC Second Level Logic (figure 10-28) and the ALD's is listed and described. The signal names are listed in numerical-alphabetical order in the "Symbol" column. The second column, titled "Figure 10-28 Sheet Number," lists the sheet of the Second Level Logic Diagrams on which each signal originates. The third column, titled "ALD and/or Figure 10-4 LN Number and Symbol Definition," lists the sheet of ALD's and/or the Signal Interface List (figure 10-4) or which signal originates, and the definition of the symbol.

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

10CPS MV	046	05 15 07 1	10CPS MULTIVIBRATOR
10 CPS MV NT	046	INVERSE 10 CPS MV	
15 30 T	045	05 11 08 1 015 TO 030	TIME PRINTER CLOCK
16 PL THRU 23 PL	042	05 11 05 1	PRINT LATCHES 16 THRU 23
1 2 4 R A B BCD	043	05 11 11 1	BINARY DECODER OUTPUTS
1 2 4 8	037	05 09 03 1	ONE OUTPUTS BINARY CODE DECIMAL LATCHES 1 2 4 8
1 2 4 DC	043	05 11 12 1	OCTAL DECODER OUTPUT
1 PL THRU 7 PL	042	05 11 03 1	PRINT LATCHES 1 THRU 7
1X THRU 32X	039	05 10 03 1	DECODED DATA BITS 20 TO 25 CONVERTED TO OCTAL 1 THRU 32
1Y THRU 256Y	039	05 10 02 1	DECODED DATA BITS 17 TO 25 CONVERTED TO OCTAL 1 THRU 256
22 DEGREES CENT A	026	04 26 05 0 - 05 26 01 1	TEMPERATURE VERSUS CURRENT CONTROL
22 DEGREES CENT B	026	04 26 05 0 - 05 26 01 0	TEMPERATURE VERSUS CURRENT CONTROL
24 PL THRU 25 PL	042	05 11 06 1	PRINT LATCHES 24 AND 25
29 DEGREES CENT A	026	04 26 05 0 - 05 26 01 1	TEMPERATURE VERSUS CURRENT CONTROL

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

29 DEGREES CENT B	026	04 26 05 0 - 05 26 01 0	TEMPERATURE VERSUS CURRENT CONTROL
2800T50 NOT	059	05 14 13 1	INVERSE 2800T50
2800T50	059	05 14 13 1	TWO BIT DELAY DATA SERIAL OUT
300 CPS COUNT DOWN	039	05 10 06 1	300 CPS GATED OUTPUT PLOTTER COUNTERS COUNT DOWN
35 DEGREES CENT A	026	04 26 05 0 - 05 26 01 1	TEMPERATURE VERSUS CURRENT CONTROL
35 DEGREES CENT B	026	04 26 05 0 - 05 26 01 0	TEMPERATURE VERSUS CURRENT CONTROL
500CPS MV	046	05 15 03 1	500CPS MULTIVIBRATOR SINGLE SHOT
512Y	039	05 10 03 1	DECODED DATA BIT 16 CONVERTED TO OCTAL 512
64X THRU 512	039	05 10 04 1	DECODED DATA BITS 16 THRU 19 CONVERTED TO OCTAL 64 THRU 512
8 PL THRU 15 PL	042	05 11 04 1	PRINT LATCHES 8 THRU 15
A1 A3 NT A2	034	05 08 01 1 A1 A3	INVERSE A2 ANDED LEVEL ADDRESS BITS 10 DECODE
A1 NOT A2 A3	034	05 08 01 1 A1	INVERSE A2 A3 ANDED LEVEL ADDRESS BITS 10 DECODE
A1 NOT	017	05 05 09 1	INVERSE A1
A1	017	05 05 09 1	ONE OUTPUT ADDRESS REGISTER LATCH 1
A1 THRU A4 IND 1 2	017	05 20 13 1	ADDRESS BITS 1 THRU 4 INDICATOR DRIVERS 1 AND 2
A1 THRU A9 PTC	006	05 09 17 1	ADDRESS BITS 1 THRU 9 OUTPUT FROM PTC
A2 A3 A4 A5 NOT	017	05 05 10 1	INVERSE A2 A3 A4 A5
A2 A3 A4 A5	017	05 05 10 1	ONE OUTPUT ADDRESS REGISTER LATCHES 2 3 4 5

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
A2 A3 NT A1	034	05 08 01 1 A2 A3 INVERSE A1 ANDED LEVEL ADDRESS BITS IO DECODE
A2 NOT A1 A3	034	05 08 01 1 A2 INVERSE A1 A3 ANDED LEVEL ADDRESS BITS IO DECODE
A3 NOT A1 A2	034	05 08 01 1 A3 INVERSE A1 A2 ANDED LEVEL ADDRESS BITS IO DECODE
A4 A5 A6	017	05 08 02 1 A4 A5 A6 ANDED LEVEL ADDRESS BITS IO DECODE
A4 A5 NT A6	034	05 08 02 1 A4 A5 INVERSE A6 ANDED LEVEL ADDRESS BITS IO DECODE
A4 A6 NT A5	034	05 08 02 1 A4 A6 INVERSE A5 ANDED LEVEL ADDRESS BITS IO DECODE
A4 NT A5 A6	034	05 08 02 1 A4 INVERSE A5 A6 ANDED LEVEL ADDRESS BITS IO DECODE
A5 A6 NT A4	034	05 08 02 1 A5 A6 INVERSE A4 ANDED LEVEL ADDRESS BITS IO DECODE
A5 NT A4 A6	034	05 08 02 1 A5 INVERSE A4 A6 ANDED LEVEL ADDRESS BITS IO DECODE
A5 THRU A8 IND 1 2	017	05 20 14 1 ADDRESS BITS 5 THRU 8 INDICATOR DRIVERS 1 AND 2
A6 A7 A8 A9 NOT	017	05 05 11 1 INVERSE A6 A7 A8 A9
A6 A7 A8 A9	017	05 05 11 1 ONE OUTPUT FROM ADDRESS REGISTER LATCHES 6 7 8 9
A6 NT A4 A5	034	05 08 02 1 A6 INVERSE A4 A6 ANDED LEVEL ADDRESS BITS IO DECODE
A7 A8 A9	034	05 08 03 1 A7 A8 A9 ANDED LEVEL ADDRESS BITS IO DECODE
A7 A8 NT A9	034	05 08 03 1 A7 A8 INVERSE A9 ANDED LEVEL ADDRESS BITS IO DECODE

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

A7 NT A8 A9	034	05 08 03 1 A7 INVERSE A8 A9 ANDED LEVEL ADDRESS BITS 10 UECODE
A8 NT A7 A9	034	05 08 03 1 A8 INVERSE A8 A9 ANDED LEVEL ADDRESS BITS 10 DECODE
A9PAD NOT	025	05 05 12 1 ADDRESS 9 PHASE A DELAYED INVERSE
A9 IND 1 2	017	05 20 18 1 ADDRESS BIT 9 INDICATOR DRIVER
AA 88	037	05 09 04 1 ONE OUTPUT BINARY CODE DECIMAL LATCHES AA 88
ABC	015	05 06 13 1 ADDRESS BIT GATE
ACCO	013	05 06 24 1 ONE OUTPUT ACCUMULATOR 0 LATCH AT END OF 3LA, DELAY A LATCHES 1 THRU 30
ACCI	013	05 06 24 1 ONE OUTPUT ACCUMULATOR 1 LATCH AT INPUT TO DELAY B LATCHES 1 THRU 21
ACC BIT 12 THRU 15	016	05 08 21 1 ACCUMULATOR BITS 12 THRU 15 PTC OUTPUT
ACC BIT 16 THRU 19	016	05 08 22 1 ACCUMULATOR BITS 16 THRU 19 PTC OUTPUT
ACC BIT 1 2 3	016	05 08 18 1 ACCUMULATOR BITS 1 THRU 3 PTC OUTPUTS
ACC BIT 20 THRU 23	016	05 08 23 1 ACCUMULATOR BITS 20 THRU 23 PTC OUTPUT
ACC BIT 24 25	016	05 08 24 1 ACCUMULATOR BITS 24 AND 25 PTC OUTPUT
ACC BIT 4 THRU 7	016	05 08 19 1 ACCUMULATOR BITS 4 THRU 7 PTC OUTPUTS
ACC BIT 8 THRU 11	016	05 08 20 1 ACCUMULATOR BITS 8 THRU 11 PTC OUTPUT
ACC BIT SIGN	016	05 08 18 1 ACCUMULATOR SIGN BIT PTC OUTPUT
ACMCSY	006	05 08 17 1 ACME COMPUTER SINGLE STEP FEED THRU PTC
ADD SUB	011	05 07 52 1 OUTPUT LEVEL OF THE ADDER CIRCUIT

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

ADDRR A1-A4 NOT	065	05 03 01 1	INVERSE ADDR R A1-A4
ADDRR A1-A4	065	05 03 01 1	ADDRESS BUFFER REG BITS A1 THRU A4
ADDRR A5-A8 NOT	065	05 03 02 1	INVERSE ADDR R A5-A8
ADDRR A5-A8	065	05 03 02 1	ADDRESS BUFFER REG BITS A5 THRU A8
ADDRR A9 NOT	065	05 03 03 1	INVERSE ADDR R A9
ADDRR A9	065	05 03 03 1	ADDRESS BUFFER REG BIT A9
ADDRR OPI-OP4 NOT	065	05 03 04 1	INVERSE ADDR R OPI-OP4
ADDRR OPI-OP4	065	05 03 04 1	ADDRESS BUFFER REG BITS OPI THRU OP4
ADR COMP NOT	069	05 03 16 1	INVERSE ADR COMP
ADR COMP	069	05 03 16 1	ADDRESS COMPARE
ADR IND IMM NOT	019	05 20 15 1	ADDRESS INDICATOR INHIBIT INVERSED
ADV IND 2	049	05 15 15 1	ADVANCE INDICATOR 2
ADV IND	049	05 15 15 1	ADVANCE INDICATOR DRIVER
ADV RST	007	05 04 14 1	ADVANCE RESET TIMING CONTROL LEVEL
ADV SET B	007	05 04 13 1	ADVANCE SET B INVERSE LEVEL
A10 IND	015	05 13 08 1	ACCUMULATOR INSTRUCTION CHANNEL LATCH 0
A10	015	05 06 29 1	ONE OUTPUT LATCH 0 AT END OF ACCUMULATOR
A11 3	015	05 06 30 1	ONE OUTPUT LATCHES 1 AND 3 AT END OF ACCUMULATOR INSTRUCTION CHANNEL DLB LATCHES
A12-A13 IND	015	05 13 08 1	ACCUMULATOR INSTRUCTION CHANNEL LATCHES 2 AND 3 INDICATOR DRIVERS

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

A14	015	05 06 31 1 ONE OUTPUT LATCH 4 AT END OF ACCUMULATOR INSTRUCTION CHANNEL 018 LATCHES INDICATOR DRIVER INSTRUCTION CHANNEL 018 LATCHES
A1 0 01 1 IND	015	05 13 09 1 ACCUMULATOR INSTRUCTION CHANNEL LATCHES 0 AND 1 INDICATOR DRIVERS
ALP SPA	037	05 09 02 1 ALPHA SPACE
AND NOT	018	05 07 22 1 INVERSE LEVEL OF DECODED LOGICAL AND OPERATION
A NT	005	05 06 07 1 BIT GENERATOR LATCH A ZERO OUTPUT
A	005	05 06 07 1 BIT GENERATOR LATCH A ONE OUTPUT
AUTO AND FWD	047	05 15 13 1 AUTOMATIC AND FOWARD
AUTO A	049	05 15 01 1 AUTOMATIC FROM DRIVE SOURCE A
AUTO IND	049	05 15 01 1 AUTOMATIC INDICATOR DRIVER OUTPUT
AUTO RLY COIL	049	05 15 01 1 AUTOMATIC RELAY COIL DRIVER OUTPUT
AUTO R START	050	05 15 19 1 AUTOMATIC RESTART
BCD LATCH	042	05 11 01 1 BINARY CODED DECIMEL LATCH
BCD MODE	045	05 11 07 1 BINARY CODED DECIMEL MODE
0G13 14 NT	006	05 05 27 1 INVERSE 0G13 14
0G13 14	006	05 05 27 1 BIT GATES 13 14
0G1 2 3 4 NT	006	05 05 24 1 INVERSE 0G1 2 3 4
0G1 2 3 4	006	05 05 24 1 BIT GATES 1 2 3 4
0G5 6 7 8 NT	006	05 05 25 1 INVERSE 0G5 6 7 8

Figure 10-28
 ALD and/or Figure 10-4 LN Number
 and Symbol Definition

Figure 10-28
 Sheet Number

Symbol

BG5 6 7 8	006	05 05 25 1 BIT GATES 5 6 7 8
BG9 10 11 12 NT	006	05 05 26 1 BG9 10 11 12 INVERSE
BG9 10 11 12	006	05 05 26 1 BIT GATES 9 10 11 12
BG SELECT	004	05 04 05 1 BIT GATE SELECT GENERATE SCOPE SYNC ON CE PANEL
BLACK MAG	038	05 09 09 1 BLACK MAGNET DRIVER OUTPUT
BLOCK DATA	042	05 11 16 1 BLOCK TRANSFER OF DATA TO PRINTER
BLOCK TILT ROTATE	038	05 09 09 1 DEGATE LEVEL PRINT CONTROLS
BOR NOT	010	05 07 03 1 INVERSE BOR
BOR	010	05 07 03 1 OUTPUT 8 LATCH TO ADD SUB UNIT
BUFF LD OCT PARITY	045	05 11 07 1 BUFFER LOAD OCTAL PARITY ONE OUTPUT OF A LATCH
BUFF LD OCT PAR NT	045	05 11 07 1 BUFFER LOAD OCTAL PARITY ZER LATCH OUTPUT
C1-C3 NOT	061	05 14 19 1 INVERSE C1-C3
C1-C3	061	05 14 19 1 CONTROL LEVELS 1 2 AND 3
CA13 NOT	063	05 02 03 1 INVERSE CA13
CARR BUSY NT	044	05 11 15 1 PRINTER CARRIAGE BUSY INVERSE LEVEL
CARR BUSY	044	04 11 01 0 - 05 11 15 1 TYPEBAR IN MOTION
CARR CH 12	044	04 11 01 0 - 05 11 15 1 CARRIAGE AT A PUNCH IN CHANNEL 12 OF CARRIAGE CONTROL TAPE
CARR CTRL LATCH NT	042	05 11 01 1 CARRIAGE CONTROL LATCH ZERO OUTPUT
CARR CTRL LATCH	042	05 11 01 1 CARRIAGE CONTROL LATCH ONE OUTPUT
CARR LEFT PLOT	039	05 10 05 1 CARRIAGE LEFT PLOTTER

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

CARR LEFT	039	05 10 03 1	CARRIAGE LEFT LATCH ONE OUTPUT DATA SIGN INPUT
CARR RET MAG	038	05 09 09 1	CARRIAGE RETURN MAGNET DRIVER OUTPUT
CARR RIGHT PLOT	039	05 10 05 1	CARRIAGE RIGHT PLOTTER
CARR RIGHT	039	05 10 03 1	CARRIAGE RIGHT LATCH ZERO OUTPUT DATA SIGN INPUT
CBR 1 2	008	05 07 08 1	CLEAR BUFFER REGISTER 1 2
CB RUN A	047	05 15 08 1	CHARACTER COUNTER BIT RUN FROM DRIVER SOURCE A
CB RUN NOT	047	05 15 08 1	INVERSE CB RUN A
CD RST NOT	069	05 03 15 1	INVERSE CD RST
CD RST	069	05 03 15 1	COMPUTER DISPLAY RESET
CDS	018	05 07 22 1	CHANGE DATA SECTOR OPERATION
CDS TAY	018	05 05 20 1	CHANGE DATA SECTOR TIME PHASE A CLOCK PULSE Y
CDS TAZ	018	05 05 20 1	CHANGE DATA SECTOR TIME PHASE A CLOCK PULSE Z
CEA13 IND	063	05 02 03 1	COMPARE ERROR OUTPUT FROM 3RD DELAY LATCH AT END OF ACCUMULATOR, INSTRUCTION CHANNEL. INDICATOR DRIVER
CEA13 NOT	063	05 02 03 1	INVERSE OF CEA13
CEB14 IND	063	05 02 05 1	COMPARE ERROR BUFFER REGISTER 14 INDICATOR DRIVER
CEB14 NOT	063	05 02 05 1	COMPARE ERROR BUFFER REGISTER 14 INVERSE
CEOAC NOT	063	05 02 05 1	COMPARE ERROR OPERAND ADDRESS COMPARE INVERSE
CEOAC	063	05 02 05 1	COMPARE ERROR OPERAND ADDRESS INDICATOR DRIVER
CE ADV OFF	007	04 04 02 0 - 05 04 13 1	ADVANCE OFF CE PANEL

Figure 10-28
 Sheet Number
 ALD and/or Figure 10-4 LN Number
 and Symbol Definition

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
CE ADV ON	007	04 04 02 0 - 05 04 13 1 ADVANCE SWITCH ON CE PANEL
CE HOPCI IND	062	05 02 01 1 COMPARE ERROR HOP CONSTANT FOR STORAGE DURNING INTERRUPT OPERATION. INDICATOR DRIVER
CE HOPCI NOT	062	05 02 01 1 COMPARE ERROR HOP CONSTANT FOR STORAGE DURNING INTERRUPT OPERATION. INVERSE LEVEL
CESSER IND	063	05 02 03 1 COMPARE ERROR SERIAL INDICATOR OUTPUT
CESSMR IND	062	05 02 02 1 COMPARE ERROR SECTOR SYLLABLE MODULE BUFFER REGISTER INDICATOR DRIVER
CESSMR NOT	062	05 02 02 1 COMPARE ERROR SECTOR SYLLABLE MODULE BUFFER REGISTER INVERSE LEVEL
CESSMSC IND	062	05 02 04 1 INDICATOR DRIVER CESSMSC
CESSMSC NOT	062	05 02 04 1 COMPARE ERROR SECTOR SYLLABLE MODULE SELF CHECK LATCH INVERSE OUTPUT
CETRS IND	062	05 02 01 1 COMPARE ERROR TRANSFER REGISTER INDICATOR DRIVER
CETRS NOT	062	05 02 01 1 COMPARE ERROR TRANSFER REGISTER SERIAL INVERSED
CGA NOT	004	05 04 03 1 INVERSE CGA
CGA	004	05 04 03 1 CLOCK GATE A PTC CLOCK PULSE GENERATOR
CHANGE TROP3	061	05 14 22 1 CHANGE TAPE READER OPERATION BIT 3
CHANL 1 NOT	048	05 14 02 1 INVERSE CHANL 1
CHANL 1	048	05 14 02 1 CHANNEL 1
CHANL 2 NOT	048	05 14 02 1 INVERSE CHANL2
CHANL 2	048	05 14 02 1 CHANNEL 2
CHANL 3-4 NOT	048	05 14 03 1 INVERSE CHANL 3-4

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

CHAML 3-4	048	05 14 03 1	CHANNEL 3-4
CHAML 5-6 NOT	048	05 14 04 1	INVERSE CHAML 5-6
CHAML 5-6	048	05 14 04 1	CHANNEL 5-6
CHECK MAG	038	05 09 11 1	CHECK MAGNET DRIVER OUTPUT
CIO 001	035	05 08 14 1	UNASSIGNED
CIO 002	035	05 08 10 1	CIO CODE 002 UNASSIGNED
CIO 005	035	05 08 14 1	CIO CODE 005 READ RCA 110 (BRD)
CIO 006	035	05 08 10 1	CIO CODE 006 LOAD SWITCH SELECTION REGISTER SSFB
CIO 011	035	05 08 14 1	CIO CODE 011 READ RCA 110 (MODR RTR YAGR)
CIO 012	035	05 08 10 1	CIO CODE 012 LOAD RCR REGISTER (CC)
CIO 015	035	05 08 14 1	CIO CODE 015 READ OCY
CIO 016	035	05 08 10 1	CIO CODE 016 LOAD COMM REC (CR)
CIO 021	035	05 08 14 1	CIO CODE 021 READ DISCRETE (DOR)
CIO 022	035	05 08 10 1	CIO CODE 022 LOAD DIS INPUT (DIN)
CIO 025	035	05 08 14 1	CIO CODE 025 READ AD CONVERTER
CIO 026	035	05 08 10 1	CIO CODE 026 LOAD DIS INPUT (DIS)
CIO 031	035	05 08 14 1	CIO CODE 031 READ SWITCH SEL (SSR)
CIO 032	035	05 08 10 1	CIO CODE 032 LOAD NASA DISCRETES
CIO 035	035	05 08 14 1	CIO CODE 035 READ TELEMETRY A (BRD)
CIO 036	035	05 08 10 1	CIO CODE 036 LOAD DDAS REG (TS)

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition
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Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
C10 041	035	05 08 14 1 C10 CODE 041 READ TELEMETRY 8 (0R0)
C10 042	035	05 08 10 1 C10 CODE 042 LOAD ERROR REG
C10 045	035	05 08 15 1 C10 CODE 045 READ DDAS (0R0)
C10 046	035	05 08 11 1 C10 CODE LOAD INTERRUPT REG
C10 051	035	05 08 15 1 C10 CODE 051 READ NASA SIM INPUTS
C10 052	035	05 08 11 1 C10 CODE LOAD OPTISYN REG
C10 055	035	05 08 15 1 C10 CODE 055 READ IO REG SW SEL (SSF0)
C10 056	035	05 08 11 1 C10 CODE LOAD COD SHIFT REG
C10 061	035	05 08 15 1 C10 CODE 061 READ IO REG RCA (GC)
C10 062	035	05 08 11 1 C10 CODE LOAD ENABLE COD SHIFT REG
C10 065	035	05 08 15 1 C10 CODE 065 READ IO REG COMM REC (CR)
C10 066	035	05 08 11 1 C10 CODE LOAD ENABLE COMPARE
C10 071	035	05 08 15 1 C10 CODE 071 READ IO REG DISCRETES (DIN)
C10 072	035	05 08 11 1 C10 CODE TELEMETRY SAMPLE
C10 075	035	05 08 15 1 C10 CODE 075 READ IO REG DISCRETES (DIS)
C10 076	035	05 08 11 1 C10 CODE RCA 110 SAMPLE
C10 101	035	05 08 15 1 C10 CODE 101 READ IO REG NASA DISCRETES
C10 102	035	05 08 11 1 C10 CODE SAMPLE RESET
C10 105	035	05 08 15 1 C10 CODE 105 READ IO REG DDAS (TS)
C10 106	035	05 08 11 1 C10 CODE SET DA DST LATCH

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

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Symbol

CIO 111	035	05 08 16 1	CIO CODE 111	READ IO REG ERRORS
CIO 112	035	05 08 12 1	CIO CODE 112	RESET DA DST LATCH
CIO 114	035	05 08 06 1	PTC CONTROL	SINGLE STEP
CIO 115	035	05 08 16 1	CIO CODE 115	READ IO REG INTERRUPT
CIO 116	035	05 08 12 1	CIO CODE 116	SET DA WALT LATCH
CIO 121	035	05 08 16 1	CIO CODE 121	READ IO REG OPTISYN
CIO 122	035	05 08 12 1	CIO CODE 122	RESET DA WALT LATCH
CIO 125	035	05 08 16 1	CIO CODE 125	READ ADDRESS REG (AZTEC)
CIO 126	035	05 08 12 1	CIO CODE 126	INHIBIT ACCEL SUB
CIO 131	035	05 08 16 1	CIO CODE 131	UNASSIGNED
CIO 132	035	05 08 12 1	CIO CODE 132	SET ACCEL PLUS OR MINUS
CIO 135	035	05 08 16 1	CIO CODE 135	LYDCHE REAL TIME COUNTER AZTEC
CIO 136	035	05 08 12 1	LOAD ACCEL	DELAY LINE
CIO 141 THRU 151	035	05 08 16 1	CIO CODES 141 145 151	UNASSIGNED
CIO 142 THRU 152	035	05 08 12 1	CIO SPARES	
CIO 154A	036	05 13 13 1	CONTROL INPUT	OUTPUT CODE 154 PHASE A
CIO 154B	036	05 13 13 1	CONTROL INPUT	OUTPUT CODE 154 PHASE B
CIO 154C	036	05 13 13 1	CONTROL INPUT	OUTPUT CODE 154 PHASE C
CIO 154 NOT	036	05 13 01 1	INVERSE CIO	154
CIO 154	036	05 13 01 1	CONTROL INPUT	OUTPUT CODE 154

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

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Symbol

CIO 156 THRU 216	035	05 08 13 1 CIO SPARES
CIO 204	035	05 08 07 1 PROGRAM LOOP LIGHTS
CIO 210	035	05 08 07 1 DISCRETE OUTPUTS
CIO 214A	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 214 PHASE A
CIO 214B	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 214 PHASE B
CIO 214C	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 214 PHASE C
CIO 214 NOT	036	05 13 01 1 INVERSE CIO 214
CIO 214	036	05 13 01 1 CONTROL INPUT OUTPUT CODE 214
CIO 220A	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 220 PHASE A
CIO 220B	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 220 PHASE B
CIO 220C	036	05 13 13 1 CONTROL INPUT OUTPUT CODE 220 PHASE C
CIO 220 NOT	036	05 13 01 1 INVERSE CIO 220
CIO 220	036	05 13 01 1 CONTROL INPUT OUTPUT CODE 220
CIO CTRL	036	05 13 14 1 CONTROL INPUT OUTPUT CONTROL
CIO DATA C	010	04 07 01 0 - 05 07 03 1 CONTROL INPUT OUTPUT DATA IO LINE TERMINATOR TERMINATOR OUTPUT TO BOR LATCH
CIO PTC	006	05 08 17 1 CONTROL INPUT OUTPUT OPERATION CODE OUTPUT PTC
CIO	018	05 07 21 1 CODED INPUT OUTPUT INSTRUCTION
CIO X LATCH	039	05 10 01 1 CONTROL INPUT OUTPUT X LATCH PLOTTER DRUM MOTION
CIO Y LATCH	039	05 10 01 1 CONTROL INPUT OUTPUT Y LATCH PLOTTER CARRIAGE MOTION

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol	Sheet Number	ALD and/or Figure 10-4 LN Number	Symbol Definition
CIO Y	039	05 10 01 1	CONTROL INPUT OUTPUT Y GENERATION OF COUNT GATE
CIO Z LATCH	039	05 10 01 1	CONTROL INPUT OUTPUT Z LATCH PLOTTER PEN MOTION
CKP	008	05 07 06 1	CHECK PARITY
CLOCK OFF	007	05 04 13 1	CLOCK OFF
CLTR MOT	008	05 07 10 1	INVERSE CLTR
CLTR	008	05 07 10 1	CLEAR TRANSFER REGISTER
CLW	008	05 07 16 1	CLEAR TRANSFER REGISTER AND W CLOCK TIME
CLX	008	05 07 05 1	CLEAR X CLOCK TIME
CNT 1 2 4 8 NT	045	05 11 09 1	INVERSE CNT 1 2 4 8
CNT 1 2 4 8	045	05 11 09 1	OCTAL OUTPUTS 12 STATE COUNTER
CNT RSY	042	05 11 02 1	COUNTER RESET
CODE 000	034	05 08 04 1	CIO CODE 000 SET INTERRUPT INHIBIT REGISTER
CODE 004	034	05 08 04 1	CIO CODE 004 RESET INTERRUPT INHIBIT REGISTER
CODE 010	034	05 08 04 1	CIO CODE 010 RESET INTERRUPT -1
CODE 014	034	05 08 04 1	CIO CODE 014 RESET INTERRUPT -2
CODE 020	034	05 08 04 1	CIO CODE 020 RESET INTERRUPT -3
CODE 024	034	05 08 04 1	CIO CODE 024 RESET INTERRUPT -4
CODE 030	034	05 08 04 1	CIO CODE 030 RESET INTERRUPT -5
CODE 034	034	05 08 04 1	CIO CODE 034 RESET INTERRUPT -6
CODE 040	034	05 08 04 1	CIO CODE 040 RESET INTERRUPT -7

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

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CODE 044	034	05 08 05 1 C10 CODE 044	RESET INTERRUPT -8
CODE 050	034	05 08 05 1 C10 CODE 050	RESET INTERRUPT -9
CODE 054	034	05 08 05 1 C10 CODE 054	RESET INTERRUPT -10
CODE 060	034	05 08 05 1 C10 CODE 060	RESET INTERRUPT -11
CODE 064	034	05 08 05 1 C10 CODE 064	RESET INTERRUPT -12
CODE 070	034	05 08 05 1 C10 CODE 070	RESET INTERRUPT -13
CODE 074	034	05 08 05 1 C10 CODE 074	RESET INTERRUPT -14
CODE 100	034	05 08 05 1 C10 CODE 100	RESET INTERRUPT -15
CODE 104	034	05 08 05 1 C10 CODE 104	RESET INTERRUPT -16
CODE 110	034	05 08 06 1 C10 CODE 110	RESET INTERRUPT LATCH
CODE 114	034	05 08 06 1 C10 CODE 114	SET PTC CONTROL SINGLE STEP LATCH
CODE 120	034	05 08 06 1 C10 CODE 120	TYPE ALPHANUMERIC
CODE 124	034	05 08 06 1 C10 CODE 124	TYPE DECIMAL
CODE 130	034	05 08 06 1 C10 CODE 130	TYPE OCTAL
CODE 134	034	05 08 06 1 C10 CODE 134	TYPEWRITER CONTROL
CODE 140	034	05 08 06 1 C10 CODE 140	PLOTTER X
CODE 144	034	05 08 06 1 C10 CODE 144	PLOTTER Y
CODE 150	034	05 08 06 1 C10 CODE 150	PLOTTER Z
CODE 154	034	05 08 07 1 C10 CODE 154	SCAN INTERRUPT
CODE 160	034	05 08 07 1 C10 CODE 160	PRINT

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
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Symbol

CODE 164	034	05 08 07 1 C10 CODE 164 PRINT OCTAL
CODE 170	034	05 08 07 1 C10 CODE 170 PRINT BCD
CJDE 174	034	05 08 07 1 C10 CODE 174 UNASSIGNED
CODE 200	034	05 08 07 1 C10 CODE 200 UNASSIGNED
CODE 204	034	05 08 07 1 C10 CODE 204 PROGRAM LOOP LIGHTS
CODE 210	034	05 08 07 1 C10 CODE 210 DISCRETE OUTPUT
CODE 214	034	05 08 07 1 C10 CODE 214 READ DISCRETE REGISTER A
CODE 220	034	05 08 08 1 C10 CODE 220 READ DISCRETE REGISTER B
CODE 224 THRU 260	034	05 0A 08 1 C10 CODES 224 THRU 260 UNASSIGNED
CODE 264 THRU 324	034	05 08 09 1 C10 CODES 264 THRU 324 UNASSIGNED
CODE 774	034	05 08 02 2 C10 CODE 774 LINE PRINT
CODE 775	034	05 08 02 2 C10 CODE 775 PRINT ACCUMULATOR
COMP CTRL NOT	007	05 04 04 1 INVERSE CTRL
COMP CTRL	007	05 04 04 1 COMPUTER CONTROL FROM EXTERNAL INPUT
COUNT GATE	039	05 10 04 1 GATES 300CPS COUNT DOWN
CP CABLE	007	04 04 01 0 - 05 04 01 1 EXTERNAL COMPUTER CABLING PRESENT GENERATE COMPUTER CONTROL TIMING
CPM B	004	05 06 05 1 CLOCK PULSE M FROM DRIVE SOURCE B
CPM X Y Z A	004	05 04 15 1 CLOCK PULSES M X Y AND Z FROM DRIVE SOURCE A
CPM X Y Z NOT	004	05 04 15 1 INVERSE LEVELS CPM X Y AND Z

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

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Symbol

CPW X Y Z	004	05 04 15 1	CLOCK PULSES M X Y AND Z
CPX B	004	05 06 05 1	CLOCK PULSE X FROM DRIVE SOURCE B
CPY B	004	05 06 05 1	CLOCK PULSE Y FROM DRIVE SOURCE B
CPZ B	004	05 06 05 1	CLOCK PULSE Z FROM DRIVE SOURCE B
C	010	05 07 01	CARRY
C M	004	05 04 02 1	CLOCK M FROM EXTERNAL SOURCE
CST IND 1	007	05 13 01 1	COMPUTER SINGLE STEP INDICATOR DRIVER
CST IND 2	007	05 13 01 1	COMPUTER SINGLE STEP INDICATOR DRIVER
CST NT	007	05 04 14 1	INVERSE CST
CST	007	05 04 14 1	COMPUTER SINGLE STEP
CST SM	069	04 04 01 0 - 05 04 12 1	COMPUTER SINGLE STEP
CTRS NOT	062	05 02 01 1	COMPARE TRANSFER REG SERIAL INVERSED
CW CY CY CZ	004	05 04 04 1	PTC CLOCK PULSES M X Y Z
CW OR W	004	04 04 01 0 - 05 04 01 1	CLOCK PULSE W EXTERNAL SOURCE
CYC3 NOT CYC4 NOT	061	05 14 20 1	INVERSE CYC0, CYC4
CYC0 - CYC5	061	05 14 20 1	CYCLE 0 THRU CYCLE 5 LEVELS
D1 D2 IND	007	05 04 10 1	DISCRETE REGISTER INDICATOR DRIVERS
D1 D2	007	05 04 10 1	DISCRETE REGISTER OUTPUTS TO IO
D3 D4 D5 D6 IND	007	05 04 09 1	DISCRETE REGISTER INDICATOR DRIVERS
D3 D4 D5 D6	007	05 04 09 1	DISCRETE REGISTER OUTPUTS TO IO

Figure 10-28
 Sheet Number

Symbol

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
DARO	042	05 13 09 1 DATA READ OUT
CA COMP IND	049	05 15 21 1 DATA ADDRESS COMPARE INDICATOR DRIVER
DA COMP	049	05 15 21 1 DATA ADDRESS COMPARE
DATA 13 IND 1 2	023	05 13 05 1 DATA BIT 13 INDICATOR DRIVERS 1 AND 2
DATA 1 2	043	05 11 13 1 DATA BITS 1 AND 2 BCD BUFFER LOAD
DATA 1 4 IND 1 2	023	05 13 02 1 DATA BITS 1 THRU 4 INDICATOR DRIVERS 1 AND 2
DATA 4 8 A	043	05 11 14 1 DATA BITS 4 8 AND A BCD BUFFER LOAD
DATA 5 8 IND 1 2	023	05 13 03 1 DATA BITS 5 THRU 8 INDICATOR DRIVERS 1 AND 2
DATA 9 12 IND 1 2	023	05 13 04 1 DATA BITS 9 THRU 12 INDICATOR DRIVERS 1 AND 2
DATA BIT 1 THRU 8	042	05 13 10 1 DATA BIT 1 THRU 8
DATA BIT 9 THRU 17	042	05 13 11 1 DATA BITS 9 THRU 17
DATA BIT SIGN	042	05 13 10 1 DATA BIT SIGN
DATA BITS 18 TO 25	042	05 13 12 1 DATA BITS 18 THRU 25
DATA B	044	05 11 15 1 DATA BIT B BUFFER LOAD
DATA C NT	044	05 11 16 1 DATA BIT C BUFFER LOAD
DATA DIS IM	066	05 02 16 1 DATA DISPLAY INPUT
DC CST	069	04 04 01 0 - 05 04 12 1 DIRECT COMPUTER COMPUTER SINGLE STEP
DD A	049	05 15 01 1 DATA DISPLAY FROM DRIVE SOURCE A
DD COMP	069	05 03 14 1 DATA DISPLAY COMPARE
DD MALT	069	05 03 14 1 DATA DISPLAY MALT

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

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Symbol

DD IND	049	05 15 20 1 DATA DISPLAY INDICATOR DRIVER
DD NOT A	049	05 15 01 1 INVERSE DD A
DD RELAY COIL	049	05 15 01 1 DATA DISPLAY RELAY COIL DRIVER OUTPUT
DDSC1	066	05 02 15 1 DATA DISPLAY SHIFT REGISTER CONTROL 1
DDSC2 NOT	066	05 02 15 1 INVERSE DDSC2
DDSC2	066	05 02 15 1 DATA DISPLAY SHIFT REGISTER CONTROL 2
DEC 1 THRU 5	045	05 11 09 1 DECIMAL OUTPUTS 12 STATE COUNTER
DEC 6 THRU 12	045	05 11 10 1 DECIMAL OUTPUTS 12 STATE COUNTER
DET REF VOLT A 15	028	05 28 01 1 DETECTOR REFERENCE VOLTAGE MEMORY A
DET REF VOLT B	028	05 28 03 1 DETECTOR REFERENCE VOLTAGE MEMORY B
DIN	061	05 14 23 1 SERIALIZED DATA INPUT TO COMPUTER
DISCR IN 1 THRU 6	036	04 13 05 0 - 05 13 14 1 DISCRETE INPUTS 1 THRU 6 FROM IO
DISCR IN 1 TO 6 SW	036	05 13 14 1 DISCRETE INPUTS 1 THRU 6 SWITCHES
DISC REG RST	007	05 04 08 1 DISCRETE REGISTER RESET
DISC REG SET	007	05 04 08 1 DISCRETE REGISTER SET
DIS A13	066	05 02 14 1 DISPLAY 3RD LATCH ACCUMULATOR INSTRUCTION CHANNEL
DIS IADR	067	05 03 12 1 DISPLAY INSTRUCTION ADDRESS DISPLAY REGISTER
DIS SSMOR A	064	05 02 07 1 DISPLAY SECTOR SYLLABLE MODULE DISPLAY REGISTER FROM SOURCE A
DIS SSMOR B	064	05 02 07 1 DISPLAY SECTOR SYLLABLE MODULE DISPLAY REGISTER FROM SOURCE B

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
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Symbol

DLA 10 12 13	011	05 06 17 1	ACCUMULATOR DELAY A LATCHES 10 12 13 ONE OUTPUTS
DLA 12 IND	012	05 13 10 1	ACCUMULATOR DELAY LINE A LATCH INDICATOR DRIVER
DLA 13 14 IND	012	05 13 11 1	ACCUMULATOR DELAY LINE A LATCHES 13 AND 14 INDICATOR DRIVERS
DLA 14 16 17	012	05 06 19 1	ACCUMULATOR DELAY A LATCHES 14 16 17 ONE OUTPUTS
DLA 16 17 IND	012	05 13 11 1	ACCUMULATOR DELAY LINE A LATCHES 16 AND 17 INDICATOR DRIVERS
DLA 18 20 21	012	05 06 20 1	ACCUMULATOR DELAY A LATCHES 18 20 21 ONE OUTPUTS
DLA 18 20 IND	012	05 13 11 1	ACCUMULATOR DELAY LINE A LATCHES 18 AND 20 INDICATOR DRIVERS
DLA 1 2 IND	011	05 13 10 1	ACCUMULATOR DELAY LINE A LATCHES 1 AND 2 INDICATOR DRIVERS
DLA 1	011	05 06 18 1	ACCUMULATOR DELAY A LATCH 1 ONE OUTPUT
DLA 21 22 24 IND	013	05 13 11 1	ACCUMULATOR DELAY LINE A LATCHES 21 22 AND 24 INDICATOR DRIVERS
DLA 22 24 25	013	05 06 21 1	ACCUMULATOR DELAY A LATCHES 22 24 25 ONE OUTPUTS
DLA 23 27 IND	013	05 13 09 1	ACCUMULATOR DELAY LINE A LATCHES 23 AND 27 INDICATOR DRIVERS
DLA 25 26 IND	013	05 13 12 1	ACCUMULATOR DELAY LINE A LATCHES 25 AND 26 INDICATOR DRIVERS
DLA 26 27	013	05 06 22 1	ACCUMULATOR DELAY LATCHES 26 27 ONE OUTPUTS
DLA 28 29 30 IND	013	05 13 12 1	ACCUMULATOR DELAY LINE A LATCHES 28 29 AND 30 INDICATOR DRIVERS
DLA 28 29 30	013	05 06 23 1	ACCUMULATOR DELAY A LATCHES 28 29 30 ONE OUTPUTS

ALD and/or Figure 10-4 LN Number
and Symbol Definition

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Symbol

DLA 2 4 5	011	05 06 15 1	ACCUMULATOR DELAY A LATCHES 2 4 AND 5 ONE OUTPUTS
DLA 3 IND	011	05 13 09 1	ACCUMULATOR DELAY LINE A LATCH 3 INDICATOR DRIVER
DLA 4 5 IND	011	05 13 10 1	ACCUMULATOR DELAY LINE A LATCHES 4 AND 5 INDICATOR DRIVERS
DLA 6 7 8 9	011	05 06 16 1	ACCUMULATOR DELAY A LATCHES 6 THRU 9 ONE OUTPUTS
DLA 6 8 IND	011	05 13 10 1	ACCUMULATOR DELAY LINE A LATCHES 6 AND 8 INDICATOR DRIVERS
DLA 7 11 15 19 IND	011	05 13 09 1	ACCUMULATOR DELAY LINE A LATCHES 7 11 15 19 INDICATOR DRIVERS
DLA 9 10 IND	011	05 13 10 1	ACCUMULATOR DELAY LINE A LATCHES 9 AND 10 INDICATOR DRIVERS
DLB 10	014	05 06 26 1	ACCUMULATOR DELAY B LATCH 10 ONE OUTPUT
DLB 14	014	05 06 27 1	ACCUMULATOR DELAY B LATCH 14 ONE OUTPUT
DLB 17 THRU 21 IND	014	05 13 09 1	ACCUMULATOR DELAY LINE B LATCHES 17 THRU 21 INDICATOR DRIVERS
DLB 18	014	05 06 28 1	ACCUMULATOR DELAY B LATCH 18 ONE OUTPUT
DLB 19 20	015	05 06 29 1	ACCUMULATOR DELAY B LATCHES 19 20 ONE OUTPUT
DLB 1 IND	013	05 13 08 1	ACCUMULATOR DELAY LINE B LATCH 1 INDICATOR DRIVER
DLB 2 3 IND	013	05 13 12 1	ACCUMULATOR DELAY LINE B LATCHES 2 AND 3 INDICATOR DRIVERS
DLR 2	013	05 06 24 1	ACCUMULATOR DELAY B LATCH 1 ONE OUTPUT
DLB 3 6	014	05 06 25 1	ACCUMULATOR DELAY B LATCHES 3 AND 6 ONE OUTPUTS
DLB 4 THRU 16 IND	014	05 13 08 1	ACCUMULATOR DELAY LINE B LATCHES 4 THRU 16

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

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Symbol

Symbol	Figure 10-28 Sheet Number	Figure 10-4 LN Number	Symbol Definition
DLY A	024	05 05 16 1	INDICATOR DRIVERS DELAY MEMORY A
DM 0 1 IND	019	05 20 17 1	INDICATOR DRIVERS DATA MODULE 0 1
DM 0	019	05 05 13 1	DATA MODULE 0
DM 1	019	05 05 13 1	DATA MODULE 1
DRIVE LEFT	050	05 15 14 1	DRIVE LEFT
DRIVE RIGHT	050	05 15 14 1	DRIVE RIGHT
DRUM DOWN PLOT	039	05 10 05 1	DRUM DOWN PLOTTER
DRUM DOWN	039	05 10 04 1	DRUM DOWN ONE OUTPUT OF LATCH DATA SIGN INPUT
DRUM UP PLOT	039	05 10 05 1	DRUM UP PLOTTER
DRUM UP	039	05 10 04 1	DRUM DOWN ZERO OUTPUT OF LATCH DATA SIGN INPUT
DSMC	066	05 02 12 1	DATA SECTOR MODULE COMPARE
DSMSO A	059	05 14 15 1	DATA SECTOR MODULE SERIAL CUT FROM SOURCE A
DSMSO NOT	059	05 14 15 1	INVERSE DSMSO
DS 1 2 3 4 IND	018	05 20 16 1	DATA SECTOR 1 2 3 4 INDICATOR DRIVERS
DS 1 2 3 NOT	018	05 05 21 1	INVERSE DS 1 2 3
DS 1 2 3	018	05 05 21 1	DATA SECTOR 1 2 3
DS 1 - 4 CDS	018	05 05 20 1	DATA SECTOR BITS 1 THRU 4 CHANGE DATA SECTOR
DS 4	018	05 05 22 1	DATA SECTOR 4
DSY	018	05 05 21 1	DATA SECTOR Y TIMING LEVEL

ALD and/or Figure 10-4 LN Number
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Symbol

DSZ	018	05 05 21 1 DATA SECTOR Z TIMING LEVEL
DTDRCP1-4	066	05 02 16 1 DATA DISPLAY REGISTER CLOCK PULSES 1 THRU 4
DTDR 810	068	05 02 18 1 DATA DISPLAY REGISTER BIT 10
DTDR 811 NOT	068	05 02 18 1 INVERSE DTDR 811
DTDR 811	068	05 02 18 1 DATA DISPLAY REGISTER BIT 11
DTDR 812 NOT	068	05 02 19 1 INVERSE DTDR 812
DTDR 812	068	05 02 19 1 DATA DISPLAY REGISTER BIT 12
DTDR 813	068	05 02 20 1 DATA DISPLAY REGISTER BIT 13
DTDR 814 NOT	068	05 02 20 1 INVERSE DTDR 814
DTDR 814	068	05 02 20 1 DATA DISPLAY REGISTER BIT 14
DTDR 815 NOT	068	05 02 19 1 INVERSE DTDR 815
DTDR 815	068	05 02 19 1 DATA DISPLAY REGISTER BIT 15
DTDR 816	068	05 02 20 1 DATA DISPLAY REGISTER BIT 16
DTDR 817 NOT	068	05 02 20 1 INVERSE DTDR 817
DTDR 817	068	05 02 20 1 DATA DISPLAY REGISTER BIT 17
DTDR 818 NOT	068	05 02 19 1 INVERSE DTDR 818
DTDR 818	068	05 02 19 1 DATA DISPLAY REGISTER BIT 18
DTDR 81	068	05 02 18 1 DATA DISPLAY REGISTER BIT 1
DTDR 820-825	068	05 02 23 1 DATA DISPLAY REGISTER DRIVER INDICATORS BIT 20 THRU BIT 25
DTDR 820 NOT	068	05 02 20 1 INVERSE DTDR 820

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

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Symbol

DTDR 820	059	05 02 20 1	DATA DISPLAY REGISTER BIT 20
DTDR 821 NOT	068	05 02 19 1	INVERSE DTDR 821
DTDR 821	068	05 02 19 1	DATA DISPLAY REGISTER BIT 21
DTDR 822 NOT	069	05 02 20 1	INVERSE DTDR 822
DTDR 822	068	05 02 20 1	DATA DISPLAY REGISTER BIT 22
DTDR 823 NOT	068	05 02 20 1	INVERSE DTDR 823
DTDR 823	068	05 02 20 1	DATA DISPLAY REGISTER BIT 23
DTDR 824	068	05 02 21 1	DATA DISPLAY REGISTER BIT 24
DTDR 825	068	05 02 21 1	DATA DISPLAY REGISTER BIT 25
DTDR 82 NOT	068	05 02 18 1	INVERSE DTDR 82
DTDR 82	068	05 02 18 1	DATA DISPLAY REGISTER BIT 2
DTDR 83 NOT	068	05 02 17 1	INVERSE DTDR 83
DTDR 83	068	05 02 17 1	DATA DISPLAY REGISTER BIT 3
DTDR 84	068	05 02 18 1	DATA DISPLAY REGISTER BIT 4
DTDR 85 NOT	068	05 02 18 1	INVERSE DTDR 85
DTDR 85	068	05 02 18 1	DATA DISPLAY REGISTER BIT 5
DTDR 86 NOT	068	05 02 17 1	INVERSE DTDR 86
DTDR 86	068	05 02 17 1	DATA DISPLAY REGISTER BIT 6
DTDR 87	068	05 02 19 1	DATA DISPLAY REGISTER BIT 7
DTDR 88 NOT	068	05 02 18 1	INVERSE DTDR 8

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DTDR 08	068	05 02 16 1	DATA DISPLAY REGISTER BIT 8
DTDR 09 NOT	068	05 02 17 1	INVERSE DTDR 09
DTDR 09	068	05 02 17 1	DATA DISPLAY REGISTER BIT 9
DTDR SIGN-019 IND	068	05 02 22 1	DATA DISPLAY REGISTER DRIVER INDICATORS SIGN THRU BIT 19
DTDR SIGN NOT	068	05 02 17 1	INVERSE DTDR SIGN
DTDR SIGN	068	05 02 17 1	DATA DISPLAY REGISTER SIGN
DTDRPT IND	061	05 14 23 1	DATA REPEAT DRIVER INDICATOR
DTDRPT NOT IND	061	05 14 23 1	INVERSE DTDRPT INDICATOR DRIVER
DTDRPT NOT	061	05 14 23 1	INVERSE DTDRPT
DTDRPT	061	05 14 23 1	DATA REPEAT
DTISO 012 THRU 025	059	05 14 11 1	DATA SERIAL OUT BITS 12 THRU 25
DTISO NOT	059	05 14 12 1	INVERSE DTISO
DTISO	059	05 14 12 1	DATA SERIAL OUT LATCH OUTPUT
£AP	022	05 07 19 1	ERROR A BUFFER REGISTER PARITY
ENABLE 1 CKT 1-3 A	027	05 27 03 1	ENABLE SENSE AMPS SEGMENT 1 CIRCUITS 1-3 MEMORY A
ENABLE 1 CKT 1-3 B	027	05 27 04 1	ENABLE SENSE AMPS SEGMENT 1 CIRCUITS 1-3 MEMORY B
ENABLE 2 CKT 1-3 A	027	05 27 03 1	ENABLE SENSE AMPS SEGMENT 2 CIRCUITS 1-3 MEMORY A
ENABLE 2 CKT 1-3 B	027	05 27 04 1	ENABLE SENSE AMPS SEGMENT 2 CIRCUITS 1-3 MEMORY B
EOP	050	05 15 19 1	END OF PROGRAM BIT

ALD and/or Figure 10-4 LN Number
and Symbol Definition

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Symbol

ERROR HOLD SW	069	04 04 01 0 - 05 04 12 1	ERROR HOLD SWITCH
ERROR RST SW	022	04 13 03 0 - 05 13 01 1	ERROR RESET SWITCH
ERR NOT INV	062	05 02 06 1	ERROR NOT INVERSE
ERR NOT	062	05 02 02 1	INVERSED ERROR LEVEL
ERR RST NOT	048	05 14 06 1	INVERSE ERR RST
ERR RST	048	05 14 06 1	ERROR RESET
ERR TEST NOT	049	05 15 02 1	INVERSE ERR TEST
ERR TEST	049	05 15 02 1	ERROR TEST
EVEN	061	05 14 18 1	EVEN DATA TRANSFER LEVEL
EXT GND	039	05 10 05 1	SIGNAL GROUND TO PLOTTER
FEED TRACK	046	04 15 02 0 - 05 15 03 1	TAPE FEED MOLES
FIRE SS	045	05 11 07 1	FIRE SINGLE SHOT
FIR MO	049	05 15 15 1	FIRST WORD
FIRST COMP	069	05 03 14 1	FIRST COMPARE
FORCE A1	031	05 20 03 1	SETS TRANSFER REGISTER BIT 8
FORCE A2	031	05 20 01 1	SETS TRANSFER REGISTER BIT 7
FORCE A3	031	05 20 03 1	SETS TRANSFER REGISTER BIT 6
FORCE A4	031	05 20 03 1	SETS TRANSFER REGISTER BIT 5
FREE RUN SS NOT	046	05 15 03 1	INVERSE FREE RUN SS
FREE RUN SS	046	05 15 03 1	FREE RUN SINGLE SHOT

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

FRSS 10	046	05 15 19 1	FREE RUN SINGLE SPOT AND IOCPS MULTIVIBRATOR
F RUN	050	05 15 14 1	FORWARD RUN TAPE READER
F START	050	05 15 17 1	FORWARD START
FWD A	050	05 15 15 1	FORWARD LEVEL FROM DRIVE SOURCE A TAPE READER
FWD IND	050	05 15 15 1	FORWARD INDICATOR DRIVER
G1 G2 G3 G4 NT	005	05 06 06 1	BIT GATE GENERATOR LATCHES 1 THRU 4 ZERO OUTPUT
G1 G2 G3 G4	005	05 06 06 1	BIT GATE GENERATOR LATCHES 1 THRU 4 ONE OUTPUTS
G5 G6 G7 NT	005	05 06 07 1	BIT GATE GENERATOR LATCHES 5 THRU 7 ZERO OUTPUT
G5 G6 G7	005	05 06 07 1	BIT GATE GENERATOR LATCHES 5 THRU 7 ONE OUTPUTS
GACISS	006	05 08 17 1	GATE ADVANCE COMPUTER ONE INSTRUCTION DURING SINGLE STEP
GATE B1 A6A	034	05 08 01 1	CIO GATE OUT CODES FROM DRIVE SOURCE A
GATE B1 A6B	034	05 08 01 1	CIO GATE OUT CODES FROM DRIVE SOURCE B
GATE B1 A6	034	05 08 01 1	GATE PHASE B BIT GATE 1 TO PHASE A BIT GATE 6
GATE L	037	05 09 02 1	LEVEL USED IN GENERATION OF SPACE OR TILT SELECT
G6W	004	05 04 01 1	CLOCK W FROM EXTERNAL SOURCE DELAYED CW
G6X	004	05 04 02 1	CLOCK X FROM EXTERNAL SOURCE DELAYED CW
G6Y	004	05 04 02 1	CLOCK Y FROM EXTERNAL SOURCE DELAYED CW
G6Z	004	05 04 02 1	CLOCK Z FROM EXTERNAL SOURCE DELAYED CW
GMMW CARR PRS775	042	05 11 02 1	GROUP MARK WORD MARK CARRIAGE PRINT STORAGE OR PRINT ACCUMULATOR

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition
Sheet Number

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number	Symbol Definition
GNM LATCH MT	042	05 11 01 1	ZERO OUTPUT GNM LATCH
GNM LATCH	042	05 11 01 1	GROUP MARK WORD MARK LATCH ONE OUTPUT SET BY CIO CODE 774
GO TO UC MT	037	05 09 05 1	GO TO UPPER CASE INVERSE LEVEL
GO TO UC	037	05 09 05 1	GO TO UPPER CASE
GSC	062	05 02 03 1	GATE SERIAL COMPARE
GTI	020	05 20 19 1	GATE TIME 1
GTZ	020	05 20 19 1	GATE TIME 2
HALT 1	007	05 04 11 1	HALT 1
HALT SW OFF	007	04 04 01 0 - 05 04 11 1	HALT SWITCH OFF
HALT SW ON	007	04 04 01 0 - 05 04 06 1	HALT SWITCH ON
HDRO 1	020	05 20 24 1	HOP SAVER REGISTER DATA MODULE 0 1
HDSA 2 3	020	05 20 23 1	HOP SAVER REGISTER DATA SECTORS 1 2 3
HDS4	020	05 20 24 1	HOP SAVER REGISTER DATA SECTOR 4
HICI 2 3	020	05 20 22 1	HOP SAVER REGISTER OLA OUTPUT 17 16 14
HIC 4 5 6 7 8	020	05 20 23 1	HOP SAVER REGISTER OLA OUTPUTS 12 13 10 7 6
HIMO 1	020	05 20 24 1	HOP SAVER REGISTER INSTRUCTION MODULE 0 1
HISI 2 3 4	020	05 20 22 1	HOP SAVER REGISTER INSTRUCTION SECTOR BITS 1 TO 4
HOPCI	020	05 20 21 1	HOP CONTANT LEVEL 1 GENERATE HOP CONSTANT
HOP	018	05 07 23 1	HOP OPERATION
HOPSAVE SW	019	04 20 02 0 - 05 20 15 1	HOP SAVE SWITCH

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

HOP TL	020	05 20 19 1	MOP TAPE LOAD
MPS IND IMM NOT	019	05 20 15 1	MOPSAVE INDICATOR INHIBIT INVERSED
MSYLC1 MSYLC0	020	05 20 22 1	SYLLABLE CONTROL LATCH STATUS MOP SAVER REGISTER
IAC NOT	065	05 03 07 1	INVERSE IAC
IAC	065	05 03 07 1	INSTRUCTION ADDRESS COMPARE
IADR A1-A8 NOT	067	05 03 11 1	INVERSE IADR A1-A8
IADR A1-A8	067	05 03 11 1	INSTRUCTION ADDRESS DISPLAY REG BITS 1 THRU 8
IA A1-A8 IND	067	05 03 08 1	INSTRUCTION ADDRESS BITS 1 THRU 8 INDICATOR DRIVE
IA COMP IND	049	05 15 21 1	INSTRUCTION ADDRESS COMPARE INDICATOR DRIVER
IA COMP	049	05 15 21 1	INSTRUCTION ADDRESS COMPARE
IA RLY COIL	049	05 15 02 1	INSTRUCTION ADDRESS RELAY COIL DRIVER OUTPUT
IM 0 1 IND	019	05 20 17 1	INSTRUCTION MODULE 0 1 INDICATOR DRIVERS
IM 0	019	05 05 13 1	INSTRUCTION MODULE 0
IM 1	019	05 05 13 1	INSTRUCTION MODULE 1
INDEX MAG	038	05 09 09 1	INDEX MAGNET DRIVER OUTPUT
IND 8 11 12	031	05 20 07 1	BLOCK INTERRUPT 11 12 INDICATOR DRIVERS
IND 8 13 14	031	05 20 06 1	BLOCK INTERRUPTS 13 14 INDICATOR DRIVERS
IND 8 15	031	05 20 05 1	BLOCK INTERRUPT 15 INDICATOR DRIVER
IND 8 16	031	05 20 05 1	BLOCK INTERRUPT 16 INDICATOR DRIVER
IND 8 1 2	031	05 20 12 1	BLOCK INTERRUPT 1 2 INDICATOR DRIVERS

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

IND B 3 4	031	05 20 11 1	BLOCK INTERRUPT 3 4 INDICATOR DRIVERS
IND B 5 6	031	05 20 10 1	BLOCK INTERRUPT 5 6 INDICATOR DRIVERS
IND B 8 9	031	05 20 09 1	BLOCK INTERRUPT 8 9 INDICATOR DRIVERS
IND B 9 10	031	05 20 08 1	BLOCK INTERRUPT 9 10 INDICATOR DRIVERS
IND I 11 12	031	05 20 07 1	INTERRUPT 11 12 INDICATOR DRIVERS
IND I 13 14	031	05 20 06 1	INTERRUPT INDICATOR DRIVERS 13 AND 14
IND I 15	031	05 20 05 1	INTERRUPT 15 INDICATOR DRIVER
IND I 1 2	031	05 20 12 1	INTERRUPT 1 2 INDICATOR DRIVERS
IND I 3 4	031	05 20 11 1	INTERRUPT 3 4 INDICATOR DRIVERS
IND I 5 6	031	05 20 10 1	INTERRUPT 5 6 INDICATOR DRIVERS
IND I 7 8	031	05 20 09 1	INTERRUPT 7 8 INDICATOR DRIVERS
IND I 9 10	031	05 20 08 1	INTERRUPT 9 10
INHIBIT GATE A	024	05 05 14 1	INHIBIT GATE MEMORY A
INHIBIT GATE B	024	05 05 17 1	INHIBIT GATE B
INHIBIT OC ZERO	045	05 11 10 1	INHIBIT OCTAL ZERO
INW A 0 MB13-14 RET	027	05 27 15 1 - 04 27 01 0	INHIBIT MEMORY A BUFFER BITS 13 AND 14 RETURNS SYLLABLE 0
INW A 0 MB1-14	027	04 27 01 0 - 05 27 16 1	INHIBIT MEMORY A SYLLABLE 0 BITS 1 THRU 14 DRIVE RESISTORS
INH A 0 MB9-12 RET	027	05 27 14 1 - 04 27 01 0	INHIBIT MEMORY A BUFFER BITS 9 THRU 12 RETURNS SYLLABLE 0

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

INH A 0 MB 1-4 RET	027	05 27 12 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 1 THRU 4 RETURNS SYLLABLE 0
INH A 0 MB 5-8 RET	027	05 27 13 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 5 THRU 8 RETURNS SYLLABLE 0
INH A 0	027	05 27 03 1 INHIBIT MEMORY A SYLLABLE 0
INH A 1 MB13-14 RET	027	05 27 15 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 13 AND 14 RETURNS SYLLABLE 1
INH A 1 MB1-14	027	04 27 01 0 - 05 27 16 1 INHIBIT MEMORY A SYLLABLE 1 BITS 1 THRU 14 DRIVE RESISTORS
INH A 1 MB9-12 RET	027	05 27 14 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 9 THRU 12 RETURNS SYLLABLE 1
INH A 1 MB 1-4 RET	027	05 27 12 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 1 THRU 4 RETURNS SYLLABLE 1
INH A 1 MB 5-8 RET	027	05 27 13 1 - 04 27 01 0 INHIBIT MEMORY A BUFFER BITS 5 THRU 8 RETURNS SYLLABLE 1
INH A 1	027	05 27 03 1 INHIBIT MEMORY A SYLLABLE 1
INH B 0 MB13-14 RET	027	05 27 15 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 13 AND 14 RETURNS SYLLABLE 0
INH B 0 MB1-14	027	04 27 02 0 - 05 27 17 1 INHIBIT MEMORY A SYLLABLE 0 BITS 1 THRU 14 DRIVE RESISTORS
INH B 0 MB9-12 RET	027	05 27 14 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 9 THRU 12 RETURNS SYLLABLE 0
INH B 0 MB 1-4 RET	027	05 27 12 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 1 THRU 4 RETURNS SYLLABLE 0
INH B 0 MB 5-8 RET	027	05 27 13 1 - 04 27 02 1 INHIBIT MEMORY B BUFFER BITS 5 THRU 8 RETURNS SYLLABLE 0

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

INH B 0	027	05 27 04 1 INHIBIT MEMORY B SYLLABLE 0
INH B 1 MB13-14 RET	027	05 27 15 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 13 AND 14 RETURNS SYLLABLE 1
INH B 1 MB1-14	027	04 27 02 0 - 05 27 17 1 INHIBIT MEMORY B SYLLABLE 1 BITS 1 THRU 14 DRIVE RESISTORS
INH B 1 MB9-12 RET	027	05 27 14 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 9 THRU 12 RETURNS SYLLABLE 1
INH B 1 MB 1-4 RET	027	05 27 12 1 - 04 27 02 0 INHIBIT MEMORY B BUFFER BITS 1 THRU 4 RETURNS SYLLABLE 1
INH B 1 MB 5-8 RET	027	05 27 13 1 - 04 27 02 1 INHIBIT MEMORY B BUFFER BITS 5 THRU 8 RETURNS SYLLABLE 1
INH B 1	027	05 27 04 1 INHIBIT MEMORY B SYLLABLE 1
INH CTRL OFF	031	04 20 02 0 - 05 20 02 1 INHIBIT CONTROL OFF SWITCH
INH CTRL ON	031	04 20 02 0 - 05 20 02 1 INHIBIT CONTROL ON SWITCH
INH CTRL	031	05 20 02 1 INHIBIT CONTROL
INH SW 11 12	031	04 20 02 0 - 05 20 07 1 INHIBIT SWITCHES 11 AND 12
INH SW 13 14	031	04 20 02 0 - 05 20 06 1 INHIBIT SWITCHES 13 AND 14
INH SW 15	031	04 20 02 0 - 05 20 05 1 INHIBIT SWITCH 15
INH SW 15		04 20 02 0 - 05 20 05 1 INHIBIT SWITCH 15
INH SW 1 2	031	04 20 02 0 - 05 20 12 1 INHIBIT SWITCHES 1 AND 2
INH SW 3 4	031	04 20 02 0 - 05 20 11 1 INHIBIT SWITCHES 3 AND 4
INH SW 5 6	031	04 20 02 0 - 05 20 10 1 INHIBIT SWITCHES 5 AND 6
INH SW 7 8	031	04 20 02 0 - 05 20 09 1 INHIBIT SWITCHES 7 AND 8

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

INH SW 9 10	031	04 20 02 0 - 05 20 08 1 INHIBIT SWITCHES 9 AND 10
INS OR P8 IND	069	05 03 18 1 INSTRUCTION BUFFER REGISTER PARITY BIT INDICATOR DRIVER
INS DROPI-OP4	067	05 03 10 1 INSTRUCTION DISPLAY REGISTER OPERATION BITS 1 THRU 4
INS DRO A1-A9	067	05 03 09 1 INSTRUCTION DISPLAY REGISTER OPERAND ADDRESS BITS 1 THRU 9
INS OAI-OA9 IND	067	05 03 08 1 INSTRUCTION OPERAND ADDRESS BITS 1 THRU 9 INDICATOR DRIVERS
INS OPI-OP4 IND	067	05 03 08 1 INSTRUCTION OPERATION BITS 1 TO 4 INDICATOR DRIVE
INSSO A	059	05 14 14 1 INSTRUCTION SERIAL OUT FROM SOURCEA
INSSO NOT	059	05 14 14 1 INVERSE INSSO A
INTCC	031	05 20 03 1 INTERRUPT COMPUTER CONTROL
INTIME	031	05 20 02 1 INTERRUPT TIME
INTAPT 1 THRU 15	031	04 20 03 0 - 05 20 01 1 INTERRUPTS 1 THRU 15 INPUTS FROM EXTERNAL SOURCE
INT 11 12 LATCH	032	05 20 07 1 INTERRUPT 11 12 LATCH OUTPUTS
INT 13 14 LATCH	033	05 20 06 1 INTERRUPT 13 AND 14 LATCH OUTPUTS
INT 15 LATCH	033	05 20 05 1 INTERRUPT 15 LATCH OUTPUT
INT 1 2 LATCH	031	05 20 11 1 INTERRUPT 1 2 LATCH OUTPUTS
INT 1 THRU 15	031	05 20 01 1 INTERRUPT 1 THRU 15 OUTPUT OF LINE TERMINATORS
INT 3 4 LATCH	031	05 20 11 1 INTERRUPT 3 4 LATCH OUTPUTS

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Symbol
Sheet Number

INT 5 6 LATCH	032	05 20 10 1 INTERRUPT 5 6 LATCH OUTPUTS
INT 7 8 LATCH	032	05 20 09 1 INTERRUPT 7 8 LATCH OUTPUTS
INT 9 10 LATCH	032	05 20 08 1 INTERRUPT 9 10 LATCH OUTPUTS
INT ADDR 400 401	031	05 20 12 1 INTERRUPT ADDRESS 400 401
INT ADDR 402 403	031	05 20 11 1 INTERRUPT ADDRESS 402 403
INT ADDR 404 405	031	05 20 10 1 INTERRUPT ADDRESS 404 405
INT ADDR 406 407	031	05 20 09 1 INTERRUPT ADDRESS 406 407
INT ADDR 410 411	031	05 20 08 1 INTERRUPT ADDRESS 410 411
INT ADDR 412 413	031	05 20 07 1 INTERRUPT ADDRESS 412 413
INT ADDR 416	031	05 20 05 1 INTERRUPT ADDRESS 416
INT ADDR 417	031	05 20 05 1 INTERRUPT ADDRESS 417
INT ADR 414 415	031	05 20 06 1 INTERRUPT ADDRESSES 414 AND 415
INT	031	05 20 04 1 INTERRUPT
INT SW 16 OFF	031	04 20 02 0 -- 05 20 24 1 INTERRUPT SWITCH 16 OFF
INT SW 16 ON	031	04 20 02 0 - 05 20 24 1 INTERRUPT SWITCH 16 ON
INVERSE		DEFINITION ZERO OUTPUT OF A LATCH
INV ERR IND	063	05 02 06 1 INVERT ERROR INDICATOR DRIVER
INV ERR NOT	063	05 02 06 1 INVERT ERROR INVERSE
INV ERR	063	05 02 06 1 INVERT ERROR
IO CHK STOP SW ON	044	05 11 17 1 INPUT OUTPUT STOP ON ERROR SWITCH CN TIED OFF

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

IS 1 2 3 IND	019	05 20 15 1 INSTRUCTION SECTOR 1 2 3 INDICATOR DRIVERS
IS 1 IS 2	019	05 05 22 1 INVERSE IS 1 IS 2
IS 1 IS 2	019	05 05 22 1 INSTRUCTION SECTOR 1 2
IS 3 IS 4 NOT	019	05 05 23 1 INVERSE IS 3 IS 4
IS 3 IS 4	019	05 05 23 1 INSTRUCTION SECTOR 3 4
IS 4 IND	019	05 20 18 1 INSTRUCTION SECTOR 4 INDICATOR DRIVER
ISSC NOT	066	05 02 13 1 INVERSE ISSC
ISSC	066	05 02 13 1 INSTRUCTION SECTOR SYLLABLE COMPARE
ISY	019	05 05 22 1 INSTRUCTION SECTOR Y TIMING LEVEL
ISZ	019	05 05 22 1 INSTRUCTION SECTOR Z TIMING LEVEL
KSSRD NOT	062	05 02 04 1 KEEP SECTOR SYLLABLE MODULE DISPLAY INVERSED
KWIAF NOT	046	05 15 03 1 RESULTS FROM THE PRESENTS OF START SS LEVEL OR ANY OF THE TAPE READER CHARACTER COUNTER BITS. IT GUARANTEES A FULL COMPLEMENT OF TAPE CHARACTERS, AND ALLOWS CLOCK PULSE 3 AND 4 WHILE IN MANUAL MODE.
KWIAN NOT A	049	05 15 15 1 FIRST WORD RECOGNITION TO GENERATE START TAPE READER
LACH 1-4	059	05 14 05 1 LATCHES 1 THRU 4
LACH 5 6	059	05 14 05 1 LATCHES 5 AND 6
LARE A	054	05 16 19 1 LATCH RESET FROM DRIVE SOURCE A
LAST A	054	05 16 19 1 LATCH SET FROM DRIVE SOURCE A
LATCH 7 NOT	051	05 03 22 1 INVERSE LATCH 7

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

Symbol	Sheet Number	ALD and/or Figure 10-4 LN Number	Symbol Definition
LATCH Y	051	05 03 22 1	CONTROLS MANUAL SELECTION OF TAPE READER REGISTER
LC A	047	05 15 08 1	LATCH C FROM DRIVE SOURCE A
LC LATCH	037	05 09 05 1	LOWER CASE LATCH ONE OUTPUT
LC NOT	047	05 15 08 1	INVERSE LC A
LC SHIFT MAG	037	05 09 06 1	LOWER CASE SHIFT MAGNET DRIVER OUTPUT
LE LM NOT	047	05 15 09 1	INVERSE LE THRU LM
LE LM	047	05 15 09 1	LATCHES E THRU M
LF SM	015	05 06 12 1	LEFT SHIFT ACCUMULATOR
LFSH CONTROL	015	05 06 11 1	LEFT SHIFT ACCUMULATOR CONTROL LINE
LJ LK NOT	047	05 15 10 1	INVERSE LJ THRU LK
LJ LK	047	05 15 10 1	LATCHES I THRU K
LMD	047	05 15 11 1	LATCH MD
LM NOT A	047	05 15 11 1	LATCH M INVERSE
LM	047	05 15 11 1	LATCH M
LOGIC GND	049	00 00 00 0 - 05 15 20 1	LOGIC GROUND
LTRCP 2 3 4 NOT	046	05 15 06 1	INVERSE LATCH OUTPUT TAPE READER CLOCK PULSES 2 3 AND 4
MACH RST NT	031	05 04 01 1	INVERSE MACH RST
MACH RST NT		04 20 02 0 - 05 20 04 1	MACHINE RESET INVERSE LEVEL
MACH RST RLY	004	04 04 01 0 - 05 04 01 1	MACHINE RESET RELAY
MACH RST	004	05 04 01 1	MACHINE RESET

Figure 10-28 ALD and/or Figure 10-4 LN Number
Sheet Number and Symbol Definition

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number	Symbol Definition
MACH RST SM	004	04 04 01 0 - 05 04 01 1	MACHINE RESET SWITCH
MANCH NOT	059	05 14 05 1	INVERSE MANCH
MANCH	059	05 14 05 1	MANUAL CHANNEL
MAN A	049	05 15 01 1	MANUAL FROM DRIVE SOURCE A
MAN CH SET	051	05 03 19 1	MANUAL CHANNEL SET
MAN GATE A	046	05 15 04 1	MANUAL GATE DRIVE SOURCE A
MAN IND	049	05 15 20 1	MANUAL INDICATOR DRIVER
MAN OR RUM NOT	047	05 15 11 1	MANUAL OR INVERSE RUM LEVEL
MAR 10 11 12	023	05 05 07 1	MEMORY ADDRESS REGISTER 10 11 AND 12 DECODER OUTPUT LEVELS
MAR 11 NOT	023	05 05 06 1	MEMORY ADDRESS REGISTER 11 INVERSE DECODER OUTPUT LEVEL
MAR 12 NOT	023	05 05 06 1	MEMORY ADDRESS REGISTER 12 INVERSE DECODER OUTPUT LEVEL
MAR 1 NOT	017	05 05 09 1	INVERSE MAR 1
MAR 1	017	05 05 09 1	MEMORY ADDRESS REGISTER 1
MAR 2 3 4 5 NOT	017	05 05 10 1	INVERSE MAR 2 3 4 5
MAR 2 3 4 5	017	05 05 10 1	MEMORY ADDRESS REGISTER 2 3 4 5
MAR 5 NOT READ	024	05 05 20 1	INVERSE MAR 5
MAR 5 READ	024	05 05 20 1	MEMORY ADDRESS REGISTER 5 READ
MAR 6 7 8	017	05 05 11 1	MEMORY ADDRESS REGISTER 6 7 8

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
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Symbol

MAR 9 10 NJT	023	05 05 08 1 INVERSE MAR 9 MAR 10
MAR 9	023	05 05 08 1 MEMORY ADDRESS REGISTER 9 DECODER OUTPUT LEVEL
MBR1-14	021	05 07 26 1 MEMORY BUFFER REGISTER BITS 1 THRU 14 DRIVERS
MBR1-6 NOT DR	021	05 07 24 1 MEMORY BUFFER REGISTER 1 THRU 6 NOT DRIVE PARITY DRIVE
MBR7-14 NOT DR	021	05 07 25 1 MEMORY BUFFER REGISTER 7 THRU 14 NOT DRIVE PARITY DRIVE
MBRL 1 2 NOT	022	05 07 17 1 INVERSE MBRL 1 2
MBRL 1 2	022	05 07 17 1 MEMORY BUFFER REGISTER LEVELS 1 AND 2 PARITY CHECKING
MBRL 3 4	022	05 07 18 1 MEMORY BUFFER REGISTER LEVELS 3 AND 4 PARITY CHECKING
MBR 11 12	021	05 27 10 1 MEMORY BUFFER BITS 11 AND 12
MBR 11 12 S	021	05 27 10 1 MEMORY BUFFER BITS 11 AND 12 GENERATE INHIBIT
MBR 13 14	021	05 27 11 1 MEMORY BUFFER BITS 13 AND 14
MBR 13 14 S	021	05 27 11 1 MEMORY BUFFER BITS 13 AND 14 GENERATE INHIBIT
MBR 1 2	021	05 27 05 1 MEMORY BUFFER BITS 1 2
MBR 1 2 S	021	05 27 05 1 MEMORY BUFFER BITS 1 2 GENERATE INHIBIT
MBR 1 THRU 14 DR	021	05 07 26 1 MEMORY BUFFER REGISTER BITS 1 THRU 14 DRIVERS
MBR 1 THRU 14	021	04 07 01 1 - 05 07 26 1 MEMORY BUFFER REGISTER BIT 1 THRU 14
MBR 1 THRU 5 IND	021	05 13 05 1 MEMORY BUFFER REGISTER BITS 1 THRU 5 INDICATOR DRIVERS
MBR 3 4	021	05 27 06 1 MEMORY BUFFER BITS 3 4

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
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Symbol

MBR 3 4 S	021	05 27 06 1	MEMORY BUFFER BITS GENERATE INHIBIT
MBR 5 6	021	05 27 07 1	MEMORY BUFFER BIT 5 5 AND 6
MBR 5 6 S	021	05 27 07 1	MEMORY BUFFER BITS 5 AND 6 GENERATE INHIBIT
MBR 6 THRU 13 IND	021	05 13 06 1	MEMORY BUFFER REGISTER BITS 6 THRU 13 INDICATOR DRIVERS
MBR 7 8	021	05 27 08 1	MEMORY BUFFER BITS 7 AND 8
MBR 7 8 S	021	05 27 08 1	MEMORY BUFFER BITS 7 AND 8 GENERATE INHIBIT
MBR 9 10	021	05 27 09 1	MEMORY BUFFER BITS 9 AND 10
MBR 9 10 S	021	05 27 09 1	MEMORY BUFFER BITS 9 10 GENERATE INHIBITS
MBR IND IMM NOT	023	05 13 01 1	MEMORY BUFFER REGISTER INDICATOR INHIBIT INVERSED
MBR SW 11 12	021	04 27 03 0 - 05 27 10 1	MEMORY BUFFER SWITCH INPUT 11 AND 12
MBR SW 13 14	021	04 27 03 0 - 05 27 11 1	MEMORY BUFFER SWITCH INPUT 13 AND 14
MBR SW 1 2	021	04 27 03 0 - 05 27 05 1	MEMORY BUFFER SWITCH INPUTS 1 AND 2
MBR SW 3 4	021	04 27 03 0 - 05 27 06 1	MEMORY BUFFER SWITCH INPUTS 3 AND 4
MBR SW 5 6	021	04 27 03 0 - 05 27 07 1	MEMORY BUFFER SWITCH INPUTS 5 AND 6
MBR SW 7 8	021	04 27 08 0 - 05 27 08 1	MEMORY BUFFER SWITCH INPUTS 7 AND 8
MBR SW 9 10	021	04 27 03 0 - 05 27 09 1	MEMORY BUFFER SWITCH INPUTS 9 AND 10
MBRST	021	05 07 24 1	MEMORY BUFFER REGISTER START
MEM ADD SW	019	04 20 02 0 - 05 20 15 1	MEMORY ADDRESS SWITCH
MEM BUFF PAR IND 1	023	05 13 05 1	MEMORY BUFFER PARITY INDICATOR DRIVER 1

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
MEM BUFF PAR IND 2	023	05 13 05 1 MEMORY BUFFER PARITY INDICATOR DRIVER 2
MEM LOAD SW	021	04 07 01 0 - 05 07 24 1 MEMORY LOAD SWITCH
MEM REG SW	023	04 13 03 0 - 05 13 01 1 MEMORY BUFFER REGISTER SWITCH
ML A	049	05 15 01 1 MEMORY LOAD FROM DRIVE SOURCE A
ML ERR	066	05 02 14 1 MEMORY LOADER ERROR
ML IND	049	05 15 01 1 MEMORY LOAD INDICATOR DRIVER OUTPUT
ML NOT A	049	05 15 01 1 INVERSE ML
MIRC	066	05 02 12 1 MEMORY MODULE COMPARE
MOP	025	05 05 03 1 MEMORY OPERATE
MA1 THRU MA9 NOT	065	05 03 13 1 INVERSE MA1 THRU MA9
MA1 THRU MA9	065	05 03 13 1 NAND ADDRESS BITS A1 THRU A9
MA13	063	05 02 03 1 NAND, OUTPUT OF 3RD DELAY LATCH AT END OF ACCUMULATOR INSTRUCTION CHANNEL
NBG10 THRU NBG14	062	05 03 26 1 NAND BIT GATE 10 THRU BIT GATE 14
NBG1 THRU NBG4	062	05 03 24 1 NAND BIT GATE 1 THRU BIT GATE 4
NBG5 THRU NBG9	062	05 03 25 1 NAND BIT GATE 5 THRU BIT GATE 9
NCPW THRU NCPZ A	062	05 03 28 1 NAND CLOCK PULSES W X Y AND Z FROM SOURCE A
NHOPC1 NOT	062	05 02 02 1 INVERSE NHOPC1
NHOPC1 OR TRS	064	05 02 07 1 NAND HOPC1 OR TRANSFER REGISTER SERIAL
NHOPC1	062	05 02 02 1 NAND LATCH OUTPUT WHICH GENERATES MOP CONSTANT FOR STORAGE DURNING INTERRUPT OPERATION

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

NHOP NOT	062	05 02 05 1 INVERSE NHOP
NHOP	062	05 02 05 1 NAND HOP OPERATION
NOP1 THRU NOP4 NOT	065	05 03 23 1 INVERSE NOP1 THRU NOP4
NOP1 THRU NOP4	065	05 03 23 1 NAND OPERATION CODE BITS 1 THRU 4
NORMAL RESET	037	05 09 06 1 RESET BCD LATCHES
NPMA TO NPMC A	062	05 03 27 1 NAND PHASES A B AND C FROM DRIVE SOURCE A
NTRS NOT	062	05 02 01 1 NAND, TRANSFER REG SERIAL INVERSED
NTRS	062	05 20 01 1 NAND TRANSFER REGISTER SERIAL
NT 1 2 4 8 16 YS	041	05 10 07 1 INVERSE OCTAL Y COUNTER OUTPUTS
NT 1 2 4 8 16XS	040	05 10 10 1 INVERSE OCTAL X COUNTER OUTPUTS
NT 1 2 4 8	037	05 09 03 1 INVERSE OUTPUT 1 2 4 8
NT 256 512XS	040	05 10 12 1 INVERSE OCTAL X COUNTER OUTPUTS
NT 256 512YS	041	05 10 09 1 INVERSE OCTAL Y COUNTER OUTPUTS
NT 32 64 128XS	040	05 10 11 1 INVERSE OCTAL X COUNTER OUTPUTS
NT 32 64 128YS	041	05 10 08 1 INVERSE OCTAL Y COUNTER OUTPUTS
NT A1 A2 A3	034	05 08 01 1 INVERSE ANDED LEVEL A1 A2 A3 ADDRESS BITS 10 DECODE
NT A4 A5 A6	034	05 08 02 1 INVERSE A4 A5 A6 ANDED LEVEL ADDRESS BITS 10 DECODE
NT A7 A8 A9 A	034	05 08 03 1 INVERSE A7 A8 A9 ANDED LEVEL ADDRESS BITS 10 DECODE FROM DRIVE SOURCE A
NT A7 A8 A9 B	034	05 08 03 1 INVERSE A7 A8 A9 ANDED LEVEL ADDRESS BITS 10

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Symbol Figure 10-28 Sheet Number

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
NT AA 88	037	DECODE FROM DRIVE SOURCE B
NT ACCO	013	05 09 04 1 INVERSE AA 88
NT AIO	015	05 06 24 1 INVERSE ACCO
NT AII 2 3	015	05 06 29 1 INVERSE AIO
NT A14	015	05 06 30 1 ZERO OUTPUT LATCHES 1 2 AND 3 AT END OF ACCUMULATOR INSTRUCTION CHANNEL DLB LATCHES
NT CIO CTRL	036	05 06 31 1 INVERSE A14
NT DLA 10 11 12 13	011	05 13 14 1 INVERSE CIO CTRL
NT DLA 14 15 16 17	012	05 06 17 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 10 TO 13
NT DLA 18 19 20 21	012	05 06 19 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 14 TO 17
NT DLA 1	011	05 06 20 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 18 TO 21
NT DLA 22 23 24 25	013	05 06 18 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCH 1
NT DLA 26 27	013	05 06 21 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 22 TO 25
NT DLA 28 29 30	013	05 06 22 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 26 27
NT DLA 2 THRU 4	011	05 06 23 1 ZERO OUTPUT ACCUMULATOR DELAY A LATCHES 28 TO 30
NT DLA 6 7 8 9	011	05 06 15 1 ZERO OUTPUTS ACCUMULATOR DELAY A LATCHES 2 THRU 4
NT DLB 11 12 13 14	014	05 06 16 1 INVERSE DLA 6 7 8 9
NT DLB 15 16 17 18	014	05 06 27 1 ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 11 TO 14
NT DLB 19 20 21	015	05 06 28 1 ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 15 TO 18
NT DLB 1 2	013	05 06 29 1 ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 19 TO 21
		05 06 24 1 ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 1 AND 2

Figure 10-28
 Sheet Number

ALD and/or Figure 10-4 LN Number
 and Symbol Definition

Symbol

NT DLB 3 4 5 6	014	05 06 25 1	ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 3 THRU 6
NT DLB 7 8 9 10	014	05 06 26 1	ZERO OUTPUT ACCUMULATOR DELAY B LATCHES 7 TO 10
NT HOPCA	020	05 20 20 1	INVERSE HOP CONSTANT LEVEL A FROM HOP SAVER 2
NT HOP	010	05 07 23 1	INVERSE HOP
NT INTCC	031	05 20 03 1	INVERSE INTCC
NT INT B	031	05 20 02 1	INVERSE INTERRUPT B LATCH OUTPUT
NT MBR 11 12	021	05 27 10 1	INVERSE MBR 11 12
NT MBR 13 14	021	05 27 11 1	INVERSE MBR 13 14
NT MBR 1 2	021	05 27 05 1	INVERSE MBR 1 2
NT MBR 1 THRU 6	021	04 07 01 0 - 05 07 24 1	SWITCH INPUTS 1 THRU 6 MEMORY BUFFER REGISTER
NT MBR 3 4	021	05 27 06 1	INVERSE MBR 3 4
NT MBR 5 6	021	05 27 07 1	INVERSE MBR 5 6
NT MBR 7 8	021	05 27 08 1	INVERSE MBR 7 8
NT MBR 7 THRU 14	021	04 07 01 0 - 05 07 25 1	SWITCH INPUTS 7 THRU 14 MEMORY BUFFER REGISTER
NT MBR 9 10	021	05 27 09 1	INVERSE MBR 9 10
NT R1	038	05 09 08 1	INVERSE R1
NT R2A	038	05 09 08 1	INVERSE R2A
NT R2	038	05 09 09 1	INVERSE R2
NT R5	038	05 09 08 1	INVERSE R5

Figure 10-28
 ALD and/or Figure 10-4 LN Number
 and Symbol Definition

Figure 10-28
 Sheet Number

Symbol

NT RT SH	015	05 06 13 1	INVERSE RIGHT SHIFT LEVEL
NT SBRZ	008	05 07 09 1	INVERSE SBRZ
NT SIGN CTRL	015	05 06 14 1	INVERSE SIGN CONTROL LEVEL
NT SSS	018	05 07 23 1	INVERSE SSS
NT T1	038	05 09 09 1	INVERSE T1
NT T2	038	05 09 09 1	INVERSE T2
DAC NOT	065	05 03 05 1	INVERSE DAC
DAC	065	05 03 05 1	OPERAND ADDRESS COMPARE
OCT LATCH	042	05 11 01 1	OCTAL LATCH
OCT LTRCH	037	05 09 02 1	OCTAL LATCH
OCT MODE	045	05 11 07 1	OCTAL MODE
ODD PARITY IND	021	05 15 06 1	ODD PARITY INDICATOR DRIVER
UDD	061	05 14 18 1	ODD DATA TRANSFER LEVEL
OPI 3 NOT	018	05 07 21 1	INVERSE OPI 3
OPI 3	018	05 07 21 1	OPERATION BITS 1 3
OPI 4 IND 1 2	018	05 13 07 1	OPERATION BITS 1 THRU 4 INDICATOR DRIVERS 1 AND 2
OP2 4 NOT	018	05 07 22 1	INVERSE OP2 4
OP2 4	018	05 07 22 1	OPERATION 2 4 BITS
OPC	065	05 03 06 1	OPERATION CODE COMPARE
OPER	049	05 15 20 1	OPERATE

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

OSC PULSES NT	007	05 04 13 1	INVERSE OSC PULSES
OSC PULSES	007	05 04 13 1	OSCILLATOR PULSES
P10 IND	007	05 04 07 1	PROGRAM CONTROL REGISTER BIT 10 INDICATOR DRIVER
P20 IND	007	05 04 07 1	PROGRAM CONTROL REGISTER BIT 20 INDICATOR DRIVER
P40 IND	007	05 04 07 1	PROGRAM CONTROL REGISTER BIT 40 INDICATOR DRIVER
P4 P2 P1 IND	007	05 04 08 1	PROGRAM CONTROL REGISTER BITS 1 2 4 INDICATOR DRIVERS
PA3P	039	05 10 01 1	PHASE A BIT GATE 3 PLOTTER
PAD NOT A9	019	05 05 13 1	INVERSE PHASE A DELAYED ADDRESS 9
PAD NOT	005	05 06 09 1	PHASE A DELAYED LATCH ZERO OUTPUT
PAD	005	05 06 09 1	PHASE A DELAYED LATCH ONE OUTPUT
PARITY CHECK	044	04 11 01 0 - 05 11 17 1	PARITY IN PRINTER
PARITY ERROR	022	05 07 20 1	PARITY ERROR
PAR ERROR IND	022	05 13 01 1	PARITY ERROR INDICATOR DRIVER
PAR ERROR LATCH	022	05 13 01 1	PARITY ERROR LATCH
PAR	008	05 07 09 1	PARITY GENERATES FINAL PARITY
PA 3	045	05 11 06 1	PHASE A BIT GATE 3
PA 8	045	05 11 06 1	PHASE A BIT GATE 8
PA 9	045	05 11 06 1	PHASE A BIT GATE 9
PA A THRU PC A	005	05 06 08 1	PHASE A THRU PHASE C FROM DRIVE SOURCE A

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

P. BG11	016	05 08 25 1	PHASE A BIT GATE 11
PA BG1 CP2	016	05 08 24 1	PHASE A BIT GATE 1 CLOCK PULSE Z
PA B YTHRU PC B	005	05 06 08 1	PHASE A THRU PHASE C FROM DRIVE SOURCE B
PA CPY	025	05 05 01 1	PHASE A CLOCK PULSE Y
PA CPZ	025	05 05 01 1	PHASE A CLOCK PULSE Z
PA THRU PC NOT	005	05 06 08 1	INVERSE PA THRU PC
PN NOT	004	04 04 01 0 -	05 04 01 1 ZERO OUTPUT PHASE GENERATOR LATCH 0
PB 10	045	05 11 06 1	PHASE B BIT GATE 10
PB CPY	025	05 05 01 1	PHASE B CLOCK PULSE Y
PB CPZ	025	05 05 01 1	PHASE B CLOCK PULSE Z
PC 10	045	05 11 06 1	PHASE C BIT GATE 10
PDD NOT	008	05 07 06 1	INVERSE PDD
PDD	008	05 07 06 1	PARITY DELAY
PEN DOWN	039	05 10 05 1	PLOTTER PEN DOWN
PEN UP PEN DOWN RESET	039	05 10 05 1	PLOTTER PEN UP OR DOWN RESET
PEN UP	039	05 10 05 1	PEN UP PLOTTER
PHA BGB	066	03 02 14 1	PHASE A BIT GATE B
PIO DATA C	010	05 07 04 1	PROCESS INPUT OUTPUT DATA INPUT TO LINE TERMINATOR
PIO DATA Y	010	05 07 04 1	PROCESS INPUT OUTPUT DATA OUTPUT LINE TERMINATOR
PIO	018	05 07 21 1	PROCESS INPUT OUTPUT INSTRUCTION

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

PLOTTER READY	039	05 10 06 1	PLOTTER READY
PL REG RST	007	05 04 07 1	PROGRAM LOOP RESET
PL REG SET	007	05 04 07 1	PROGRAM LOOP SET CIO 204
POD NOT	008	05 07 10 1	INVERSE POD
POD	008	05 07 10 1	PARITY OUT DELAY
PRINT ALPHANUM CTRL	037	05 09 02 1	CONTROLS DATA INPUT TO 8CD LATCHES
PRINT ALPHA NUM	037	05 09 01 1	PRINT ALPHABETIC NUMERIC TYPERWRITER
PRINT BCD	042	05 11 01 1	PRINT BINARY CODED DECIMAL
PRINT CHECK RST	042	05 11 02 1	PRINT CHECK RESET
PRINT CONTROLS NT	037	05 09 01 1	GENERATED BY CODE 134 TYPERWRITER CONTROL
PRINT CONTROLS	037	05 09 02 1	LEVEL USED TO GENERATE TYPERWRITER OPERATIONS
PRINT DEC NT	037	05 09 01 1	INVERSE PRINT DEC
PRINT DEC	037	05 09 01 1	PRINT DECIMAL TYPERWRITE CONTROL LEVEL
PRINT INSTR	042	05 11 01 1	PRINT INSTRUCTION
PRINT OCT NT	037	05 09 01 1	INVERSE PRINT OCT
PRINT OCT	037	05 09 01 1	PRINT OCTAL TYPERWRITER CONTROL LEVEL
PRINT READ	044	05 11 17 1	PRINTER READY
PRINT RLADY	044	04 11 01 0 - 05 11 17 1	INITIATES TRANSFER OF DATA
PRNT OCT	042	05 11 01 1	PRINT OCTAL
PRNT RST	042	05 11 02 1	PRINT RESET

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition
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PROCESSOR RELEASE	042	04 11 01 0 - 05 11 02 1	RELEASE PROCESSOR FROM PRINT INSTRUCTION
PROCESS LTCH NT	042	05 11 02 1	ZERO OUTPUT PROCESS LATCH
PRUCSS	042	05 11 02 1	ONE OUTPUT PROCESS LATCH
PRU RST	049	00 00 00 0 - 05 15 20 1	PROCESS RESET
PR DATA L	037	05 09 02 1	LEVEL USED IN GENERATION OF SPACE OR TILT SELECT
PR ADV OFF	007	04 04 02 0 - 05 04 13 1	PROCESS ADVANCE OFF
PR ADV ON	007	04 04 02 0 - 05 04 13 1	PROCESS ADVANCE SWITCH ON
PRS CARR GATE	045	05 11 06 1	PRINT CARRIAGE GATE
PRS GATE	045	05 11 06 1	PRINT GATE
PRS MEM NT	010	05 07 03 1	PRINT MEMORY INVERSE
PRS PRS775 LTCH NT	042	05 11 01 1	INVERSE PRS PRS775 LTCH
PRS PRS775 LTCH	042	05 11 01 1	ONE OUTPUT LATCH PRINT STORAGE OR PRINT ACCUMULATOR
PRS PRS775	042	05 11 01 1	PRINT STORAGE OR PRINT ACCUMULATOR
PRS	010	05 07 03 1	PRINT OPERATION
PRT CHAR POS 10	044	05 11 17 1	PRINT CHARACTER POSITION 10 PARITY ERROR INDICATOR
PRT CHAR POS 1 NT	044	05 11 17 1	INVERSE PRT CHAR POS1
PRT CHAR POS 1	044	05 11 17 1	PRINT CHARACTER POSITION 1 PARITY ERROR INDICATOR
PTC CST	006	05 08 17 1	COMPUTER SINGLE STEP OUTPUT FROM PTC

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

PTRS C	009	05 07 16 1	TRANSFER REGISTER SERIAL OUTPUT OF LINE DRIVER
R1	038	05 09 08 1	ROTATE 1
R1 W	038	05 09 08 1	ROTATE 1 PRINT DRIVER OUTPUT
R2A	038	05 09 08 1	ROTATE 2A
R2A W	038	05 09 08 1	ROTATE 2A PRINT DRIVER OUTPUT
R2	038	05 09 08 1	ROTATE 2
R2 W	038	05 09 08 1	ROTATE 2 PRINT DRIVER OUTPUT
R5	038	05 09 08 1	ROTATE 5
R5 W	038	05 09 08 1	ROTATE 5 PRINT DRIVER OUTPUT
RAC NOT	010	05 07 02 1	RECIRCULATE ACCUMULATOR INVERSE
RD1 WR X DRIVE A	026	05 26 01 1	READ 1 TIME WRITE X DRIVE MEMORY A
RD1 WR X DRIVE B	026	05 26 01 1	READ 1 TIME WRITE X DRIVE MEMORY B
RD2 WR Y DRIVE A	026	05 26 01 1	READ 2 TIME WRITE Y DRIVE MEMORY A
RD2 WR Y DRIVE B	026	05 26 01 1	READ 2 TIME WRITE Y DRIVE MEMORY B
ROM NOT	025	05 05 02 1	INVERSE ROM
ROM	025	05 05 02 1	READ MEMORY CONTROL READ FROM MEMORY OPERATION
RD GATE A	024	05 05 15 1	READ GATE MEMORY A
RD GATE A		05 27 01 1	READ GATE MEMORY A
RD GATE B	024	05 05 19 1	READ GATE B
RD GATE B		05 27 02 1	READ GATE MEMORY B

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

RD NOT	025	05 05 03 1	INVERSE RD
RD	025	05 05 03 1	READ READ MEMORY OPERATION
RD SYL1 WR SYLO GTA	026	05 27 01 1	READ SYLLABLE 1 WRITE SYLLABLE 0 GATE MEMORY A
RD SYL1 WR SYLO GTB	026	05 27 02 1	READ SYLLABLE 1 WRITE SYLLABLE 0 GATE MEMORY B
RD WR A	024	05 05 14 1	READ WRITE MEMORY A
RD WR B	024	05 05 17 1	READ WRITE MEMORY B
RD WR DLY 0.75 A	024	05 05 16 1	READ WRITE DELAY 0.75US MEMORY A
RD WR DLY 0.75 B	024	05 05 18 1	READ WRITE DELAY 0.75US MEMORY B
RD WR DLY 1.25 A	024	05 05 16 1	READ WRITE DELAY 1.25US MEMORY A
RD WR DLY 1.25 B	024	05 05 18 1	READ WRITE DELAY 1.25US MEMORY B
RD WR DLY 1.75 A	024	05 05 15 1	READ WRITE DELAY 1.75US MEMORY A
RD WR DLY 1.75 B	024	05 05 15 1	READ WRITE DELAY 1.75US MEMORY B
RD WR DLY 2.25 A	024	05 05 15 1	READ WRITE DELAY 2.25US MEMORY A
RD WR DLY 2.25 B	024	05 05 19 1	READ WRITE DELAY 2.25US MEMORY B
RD WR DLY 2.75 A	024	05 05 16 1	READ WRITE DELAY 2.75US MEMORY A
RD WR DLY 2.75 B	024	05 05 18 1	READ WRITE DELAY 2.75US MEMORY B
RD WR NOT A	024	05 05 14 1	READ WRITE INVERSE MEMORY A
RD WR NOT B	024	05 05 17 1	READ WRITE INVERSE MEMORY B
READY	037	05 09 07 1	TYPEWRITER READY
RED MAG	038	05 09 09 1	RED MAGNET DRIVER OUTPUT

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

REM ADV OFF	007	04 04 02 0 - 05 04 13 1	REMOTE ADVANCE OFF
REM ADV ON	007	04 04 02 0 - 05 04 13 1	REMOTE ADVANCE SWITCH ON
RESET LC NT	037	05 09 07 1	RESET LOWER CASE
RETOP	018	05 07 23 1	RESET OPERATION
RIGHT MARGIN NT	038	05 09 10 1	INVERSE RIGHT MARGIN
RIGHT MARGIN	038	05 09 10 1	RIGHT MARGIN TYPWR WRITER FEED BACK
R NOT	059	05 14 16 1	INVERSE R
R RUN	050	05 15 14 1	REVERSE RUN TAPE READER
R	059	05 14 16 1	LEVEL USED IN SERIALIZER PARITY CHECKING
R START	050	05 15 17 1	REVERSE START
RST ERROR LTCH	044	05 11 17 1	RESET ERROR LATCH
RST GMMH	042	05 11 02 1	RESET GROUP MARK WORD MARK
RST INH	031	05 20 02 1	RESET INHIBIT
RST INSDR	067	05 03 12 1	RESET INSTRUCTION DISPLAY REGISTER
RST INT	031	05 20 04 1	RESET INTERRUPT
RST PARITY	044	05 11 17 1	RESET PARITY
RST PB	069	05 03 17 1	RESET PARITY BIT
RST PROCESS	044	05 11 17 1	RESET PROCESS
RST RT	059	05 14 16 1	RESET SERIALIZER PARITY BIT LATCHES
RST SSMBRA	064	05 02 07 1	RESET SECTOR SYLLABLE MODULE BUFFER REGISTER FROM SOURCE A

Figure 10-28 ALD and/or Figure 10-4 LN Number
Sheet Number and Symbol Definition

Symbol	Figure 10-28 Sheet Number	Figure 10-4 LN Number	Symbol Definition
RST SSMR8B	064	05 02 07 1	RESET SECTOR SYLLABLE MODULE BUFFER REGISTER FROM SOURCE B
RST X REG	039	05 10 01 1	RESET X REGISTER
RST Y REG	039	05 10 01 1	RESET Y REGISTER
RSU	010	05 07 02 1	REVERSE SUBTRACT
RTAP NOT	047	05 15 11 1	RESET TAPE PARITY INVERSE
RTROP3	061	05 14 22 1	RESET TAPE READER OPERATION BIT 3
RUN A	050	05 15 14 1	RUN LEVEL FROM DRIVE SOURCE A
RUN LATCH	044	04 11 01 0 - 05 11 17 1	PRINTER IN RUN CONDITION
RUN NOT A	050	05 15 14 1	INVERSE RUN A
RUN NOT	025	05 05 02 1	INVERSE RUN LEVEL
RUNY	008	05 07 11 1	RUN Y CLOCK TIME
RVS A	050	05 15 15 1	REVERSE LEVEL FROM DRIVE SOURCE A TAPE READER
RVS IND	050	05 15 15 1	REVERSE INDICATOR DRIVER
SAM ERRS	048	05 14 06 1	SAMPLE ERRORS
SA STROBE A	028	05 28 01 1	SENSE AMPLIFIER STROBE MEMORY A
SA STROBE B	028	05 28 03 1	SENSE AMPLIFIER STROBE MEMORY B
SBRX	008	05 07 08 1	SET BUFFER REGISTER X CLOCK PULSE
SBRV	008	05 07 06 1	SET BUFFER REGISTER Y CLOCK TIME
SBRZ	008	05 07 09 1	SET BUFFER REGISTER Z CLOCK TIME

Figure 10-28 ALD and/or Figure 10-4 LN Number
 and Symbol Definition
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Symbol

SCC TRANSFER NT	038	05 09 10 1 INVERSE SCC TRANSFER
SCC TRANSFER	038	05 09 10 1 DEGATE LEVEL PRINT CONTROLS TYPewriter FEEDBACK
SCETRS NOT	062	05 02 01 1 SERIAL COMPARE ERROR TRANSFER REGISTER SERIAL INVERSE LEVEL
SCOPE SYNC	004	05 04 06 1 ANDED OUTPUTS OF SELECTED BIT GATE PHASE AND CLOCK PULSE AVAILABLE ON CE TEST PANEL
SCRS NT	036	05 13 22 1 INVERSE SCRS
SCRS	036	05 13 22 1 LOAD ACCUMULATOR FROM A OR B SWITCHES CONTROLLED BY A CIO
SC BC BITS	036	05 13 19 1 SCREEN BITS PROGRAM SWITCH REGISTERS A OR B
SC B BITS	036	05 13 14 1 SCREEN BITS PROGRAM SWITCH REGISTERS A OR B
SC C BITS	036	05 13 16 1 SCREEN BITS PROGRAM SWITCH REGISTERS A OR B
SEL IND	049	05 15 22 1 SEQUENCE ERROR 1 INDICATOR DRIVER
SEL NOT	049	05 15 22 1 SEQUENCE ERROR 1 INVERSE
SE2 IND	049	05 15 22 1 SEQUENCE ERROR 2 INDICATOR DRIVER
SE2 NOT	049	05 15 22 1 SEQUENCE ERROR 2 INVERSE
SECK NOT		00 00 00 0 - 05 02 06 1 INVERSE SELF CHECK LEVEL
SECK NOT		00 00 00 0 - 05 15 03 1 SELF CHECK INVERSE LEVEL
SECK		00 00 00 0 - 05 15 14 1 SELF CHECK
SEL ADR IND	046	05 15 05 1 SELECT ADDRESS INDICATOR DRIVER
SEL ADR	046	05 15 05 1 SELECT ADDRESS
SEL A13 DATA	066	05 02 14 1 SELECT DATA 3RD LATCH ACCUMULATOR INSTRUCTION

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

Symbol	Sheet Number	Channel	Definition
SEL A13 IA	066	05 02 14 1	SELECT INSTRUCTION ADDRESS 3RD LATCH ACCUMULATOR INSTRUCTION CHANNEL
SEL A13	066	05 02 14 1	SELECT 3RD LATCH ACCUMULATOR INSTRUCTION CHANNEL
SEL TRS	066	05 02 14 1	SELECT TRANSFER REGISTER SERIAL
SEN B MB9 SEG 2	028	04 28 02 0 - 05 28 04 1	SENSE MEMORY B BIT 9 SEGMENT 2
SENSE A MB10 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 10 SEGMENT 1
SENSE A MB10 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 10 SEGMENT 2
SENSE A MB11 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 11 SEGMENT 1
SENSE A MB11 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 11 SEGMENT 2
SENSE A MB12 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 12 SEGMENT 1
SENSE A MB12 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 12 SEGMENT 2
SENSE A MB13 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 13 SEGMENT 1
SENSE A MB13 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 13 SEGMENT 2
SENSE A MB1 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 1 SEGMENT 1
SENSE A MB1 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 1 SEGMENT 2
SENSE A MB2 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 2 SEGMENT 1
SENSE A MB2 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 2 SEGMENT 2
SENSE A MB3 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 3 SEGMENT 1
SENSE A MB3 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 3 SEGMENT 2
SENSE A MB4 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 4 SEGMENT 1

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SENSE A MB4 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 4 SEGMENT 2
SENSE A MB5 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 5 SEGMENT 1
SENSE A MB5 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 5 SEGMENT 2
SENSE A MB6 SEG 1	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 6 SEGMENT 1
SENSE A MB6 SEG 2	028	04 28 01 0 - 05 28 01 1	SENSE MEMORY A BIT 6 SEGMENT 2
SENSE A MB7 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 7 SEGMENT 1
SENSE A MB7 SEG 2	028	04 25 01 0 - 05 28 02 1	SENSE MEMORY A BIT 7 SEGMENT 2
SENSE A MB8 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 8 SEGMENT 1
SENSE A MB8 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 8 SEGMENT 2
SENSE A MB9 SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 9 SEGMENT 1
SENSE A MB9 SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A BIT 9 SEGMENT 2
SENSE A MB11-6	028	05 28 01 1	MEMORY A SENSE AMP DETECTOR OUTPUTS TO MEMORY BUFFER BITS 1 T:RU 6
SENSE A MB17-14	028	05 28 02 1	SENSE MEMORY A MEMORY BUFFER REGISTER BITS 7 - 14
SENSE A PAR SEG 1	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A PARITY BIT SEGMENT 1
SENSE A PAR SEG 2	028	04 28 01 0 - 05 28 02 1	SENSE MEMORY A PARITY BIT SEGMENT 2
SENSE B MB10 SEG 1	028	04 28 02 0 - 05 28 04 1	SENSE MEMORY B BIT 10 SEGMENT 1
SENSE B MB10 SEG 2	028	04 28 02 0 - 05 28 04 1	SENSE MEMORY B BIT 10 SEGMENT 2
SENSE B MB11 SEG 1	028	04 28 02 0 - 05 28 04 1	SENSE MEMORY B BIT 11 SEGMENT 1
SENSE B MB11 SEG 2	028	04 28 02 0 - 05 28 04 1	SENSE MEMORY B BIT 11 SEGMENT 2

ALD and/or Figure 10-4 LN Number
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Symbol

SENSE 0 MB12 SEG 1	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 12	SEGMENT 1
SENSE 0 MB12 SEG 2	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 12	SEGMENT 2
SENSE 0 MB13 SEG 1	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 13	SEGMENT 1
SENSE 0 MB13 SEG 2	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 13	SEGMENT 2
SENSE 0 MB1 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 1	SEGMENT 1
SENSE 0 MB1 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 1	SEGMENT 2
SENSE 0 MB2 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 2	SEGMENT 1
SENSE 0 MB2 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 2	SEGMENT 2
SENSE 0 MB3 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 3	SEGMENT 1
SENSE 0 MB3 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 3	SEGMENT 2
SENSE 0 MB4 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 4	SEGMENT 1
SENSE 0 MB4 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 4	SEGMENT 2
SENSE 0 MB5 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 5	SEGMENT 1
SENSE 0 MB5 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 5	SEGMENT 2
SENSE 0 MB6 SEG 1	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 6	SEGMENT 1
SENSE 0 MB6 SEG 2	020	04 20 02 0 - 05 20 03 1	SENSE MEMORY 0 BIT 6	SEGMENT 2
SENSE 0 MB7 SEG 1	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 7	SEGMENT 1
SENSE 0 MB7 SEG 2	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 7	SEGMENT 2
SENSE 0 MB8 SEG 1	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 8	SEGMENT 1
SENSE 0 MB8 SEG 2	020	04 20 02 0 - 05 20 04 1	SENSE MEMORY 0 BIT 8	SEGMENT 2

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ALD and/or Figure 10-4 LN Number
and Symbol Definition

Symbol

SENSE B MB9 SEG 1	020	04 20 02 0 - 05 20 04 1 SENSE MEMORY 0 BIT 9 SEGMENT 1
SENSE B MB9 SEG 2	020	04 20 02 0 - 05 20 03 1 SENSE MEMORY 0 BIT 9 SEGMENT 2
SENSE B MBRI-6	020	05 20 03 1 SENSE MEMORY 0 MEMORY BUFFER REGISTER BITS 1 - 6
SENSE B MBR7 THRU 14	020	05 20 04 1 SENSE MEMORY 0 BITS 7 TO 14 TO BUFFER REGISTER
SENSE B PAR SEG 1	020	04 20 02 0 - 05 20 04 1 SENSE MEMORY 0 PARITY BIT SEGMENT 1
SENSE B PAR SEG 2	020	04 20 02 0 - 05 20 04 1 SENSE MEMORY 0 PARITY BIT SEGMENT 2
SEQ BIT NOT	040	05 14 06 1 INVERSE SEQ BIT
SEQ BIT	040	05 14 06 1 SEQUENCE BIT
SEQ ERR 2 RST IMM	049	05 15 22 1 SEQUENCE ERROR 2 RESET INHIBIT
SER PB ID 2	060	05 14 10 1 SERIAL PARITY BIT INDICATOR 2 DRIVER OUTPUT
SER PB IND 1	060	05 14 10 1 SERIAL PARITY BIT INDICATOR 1 DRIVER OUTPUT
SER PB	060	05 14 10 1 SERIAL PARITY BIT
SETOP	018	05 07 23 1 SET OPERATION
SET IADR	067	05 03 12 1 SET INSTRUCTION ADDRESS DISPLAY REGISTER
SET IMM	031	05 20 02 1 SET INHIBIT
SET INSR	067	05 03 12 1 SET INSTRUCTION DISPLAY REGISTER
SET LE NOT	047	05 15 08 1 INVERSE SET LE
SET LE	047	05 15 08 1 SET LATCH E
SET LL NOT	047	05 15 08 1 INVERSE SET LL
SET LL	047	05 15 08 1 SET LATCH L

Figure 10-28
 AID and/or Figure 10-4 LN Number
 and Symbol Definition

Figure 10-28
 Sheet Number

Symbol

SET MAN CM	051	05 03 21 1 SET MANUAL CHANNEL
SET MBR 1	021	05 07 24 1 SET MEMORY BUFFER REGISTER POSITIONS 1 THRU 7
SET MBR 1		04 27 03 0 - 05 27 05-08 1 SET MEMORY BUFFER REGISTER CIRCUIT 1
SET MBR 2	021	05 07 24 1 SET MEMORY BUFFER REGISTER POSITIONS 8 THRU 14
SET MBR 2		04 27 03 0 - 05 27 09-11 1 SET MEMORY BUFFER REGISTER CIRCUIT 2
SET SSMR DS	064	05 02 07 1 SET SECTOR SYLLABLE MODULE BUFFER REGISTER DATA SECTOR
SET SSMR IM1	064	05 02 07 1 SET SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION MODULE 1
SET SSMR IS	064	05 02 07 1 SET SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR
SET SSMR A	064	05 02 07 1 SET SECTOR SYLLABLE MODULE DISPLAY REGISTER FROM SOURCE A
SET SSMR B	064	05 02 07 1 SET SECTOR SYLLABLE MODULE DISPLAY REGISTER FROM SOURCE B
SHF OP	018	05 07 22 1 SHIFT OPERATION
SH DATA	015	05 07 32 1 SHIFTED DATA OUTPUT DLB TO DLA LATCHES
SH W	015	05 06 12 1 SHIFT CLOCK PULSE W
SH Y	015	05 06 12 1 SHIFT CLOCK PULSE Y
SH Z	015	05 06 12 1 SHIFT CLOCK PULSE Z
SIGN PL	042	05 11 03 1 SIGN PRINT LATCH
SINGLE BIT SW	007	04 04 02 0 - 05 04 13 1 SINGLE BIT SWITCH

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SINGLE INST SW	007	04 07 01 0 - 05 07 24 1 SINGLE INSTRUCTION SWITCH
SINGLE PHASE SW	007	04 04 02 0 - 05 04 13 1 SINGLE PHASE SWITCH
SINK	025	05 05 04 1 LEVEL USED IN GENERATION OF MEMORY SYNC LEVELS A
SKIP FIRST NOT	050	05 15 16 1 INVERSE SKIP
SKIP FIRST	050	05 15 16 1 SKIP FIRST SEQUENCE BIT
SKIP TO CHAN 1 MT	044	05 11 15 1 INVERSE SKIP TO CHAN 1 OF THE PRINTER CARRIAGE TAPE
SKIP TO CHAN 1		05 11 15 1 MOVES PRINTER FORMS UNTIL A HOLE IS SENSED IN CHANNEL 1 OF THE CARRIAGE TAPE
SPACE CODE NT	037	05 09 05 1 INVERSE SPACE CODE LEVEL
SPACE CODE	037	05 09 05 1 SPACE CODE DECODED OUTPUT
SPACE MAG	038	05 09 09 1 SPACE MAGNET DRIVER OUTPUT
SPACE NT	037	05 09 06 1 INVERSE SPACE LEVEL
SPE IND	061	05 14 17 1 SERIALIZER PARITY ERROR INDICATOR DRIVER
SPE NOT	061	05 14 17 1 INVERSE SPE
SPE	061	05 14 17 1 SERIALIZER PARITY ERROR
SRPT NOT	061	05 14 21 1 SET REPEAT INVERSED
SRTR NOT	008	05 07 06 1 INVERSE SHIFT RIGHT TRANSFER REGISTER
SSMBR DM0	064	05 02 09 1 SECTOR SYLLABLE MODULE BUFFER REGISTER DATA MODULE 0
SSMBR DM1	064	05 02 09 1 SECTOR SYLLABLE MODULE BUFFER REGISTER DATA MODULE 1

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number and Symbol Definition
SSMBR DS1-3 NOT	064	05 02 10 1 INVERSE SSMBR DS1-3
SSMBR DS1-3	064	05 02 10 1 SECTOR SYLLABLE MODULE BUFFER REGISTER DATA SECTORS 1 2 AND 3
SSMBR DS4	064	05 02 11 1 SECTOR SYLLABLE MODULE BUFFER REGISTER DATA SECTOR 4
SSMBR IMO-1	064	05 02 11 1 SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION MODULES 0 AND 1
SSMBR IS1	064	05 02 08 1 SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR 1
SSMBR IS 1 NOT	064	05 02 08 1 INVERSE SSMBR IS 1
SSMBR IS 2 NOT	064	05 02 08 1 INVERSE SSMBR IS 2
SSMBR IS 2	064	05 02 08 1 SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR 2
SSMBR IS 3 NOT	064	05 02 08 1 INVERSE SSMBR IS 3
SSMBR IS 3	064	05 07 08 1 SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR 3
SSMBR IS 4 NOT	064	05 02 09 1 INVERSE SSMBR IS 4
SSMBR IS 4	064	05 02 09 1 SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR 4
SSMBR SYL 1 NOT	064	05 02 09 1 INVERSE SSMBR SYL 1
SSMBR SYL 1	064	05 02 09 1 SECTOR SYLLABLE MODULE BUFFER REGISTER SYLLABLE 1
SSHDR DA DMO IND	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA ADDRESS DATA MODULE 0 INDICATOR DRIVER
SSHDR DA DMI IND	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA

ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SSMDR DM0	064	ADDRESS DATA MODULE 1 INDICATOR DRIVER
SSMDR DM1	064	05 02 09 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA MODULE 0
SSMDR DS1-3	064	05 02 09 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA MODULE 1
SSMDR DS1-4 IMD	064	05 02 10 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA SECTORS 1 2 AND 3
SSMDR DS1-4 IMD	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA SECTORS 1 THRU 4 INDICATOR DRIVERS
SSMDR DS4	064	05 02 11 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER DATA SECTOR 4
SSMDR IA IMD IMD	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION ADDRESS INSTRUCTION MODULE 0 INDICATOR DRIVER
SSMDR IA IMI IMD	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION ADDRESS INSTRUCTION MODULE 1 INDICATOR DRIVER
SSMDR IMO-1	064	05 02 11 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION MODULES 0 AND 1
SSMDR IS1-4 IMD	064	05 02 23 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION SECTORS 1 THRU 4 INDICATOR DRIVERS
SSMDR IS1	064	05 02 08 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION SECTOR 1
SSMDR IS 2	064	05 02 08 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION SECTOR 2
SSMDR IS 3	064	05 02 08 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION SECTOR 3
SSMDR IS 4	064	05 02 09 1 SECTOR SYLLABLE MODULE DISPLAY REGISTER INSTRUCTION SECTOR 4

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Symbol
Figure 10-28
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SSMDR SYL1	064	05 02 09 1	SECTOR SYLLABLE MODULE DISPLAY REGISTER SYLLABLE 1
SSMDR SYL 0-1 IND	064	05 02 23 1	SECTOR SYLLABLE MODULE DISPLAY REGISTER SYLLABLES 0 AND 1 INDICATOR DRIVERS
SSMDR SYL 1 NOT	064	05 02 09 1	INVERSE SSMDR SYL 1
SSS	018	05 07 23 1	GENERATES STORE ACCUMULATOR
STACC	008	05 07 16 1	STORE ACCUMULATOR
START IND 1 2	050	05 15 16 1	START INDICATOR 1 2 DRIVERS
START \$\$ NOT A	046	05 15 03 1	INVERSE START SINGLE SMGT DRIVE SOURCE A
STCYC1	061	05 14 19 1	START CYCLE 1
STCYC	061	05 14 18 1	START CYCLE
STOP IND 1 2	050	05 15 16 1	STOP INDICATOR 1 2 DRIVERS
STOP MOM 1	007	05 04 14 1	NEGATING TO CLOCK CONTROL
STOP NOT	050	05 15 18 1	INVERSE STOP
STOP	050	05 15 18 1	STOP
STO NOT	018	05 07 22 1	INVERSE STO
STO	018	05 07 22 1	STORE INSTRUCTION
STROBE A INH	027	05 07 22 1	STROBE A INHIBIT PREVENTS BUFFER LOAD FROM SENSE AMPLIFIERS A
STROBE A	027	05 27 03 1	STROBE MEMORY A
STROBE B INH	027	05 07 22 1	STROBE B INHIBIT PREVENTS BUFFER LOAD FROM SENSE AMPLIFIERS B

Figure 10-28 ALD and/or Figure 10-4 LN Number
 Sheet Number and Symbol Definition

SYSTORE B	027	05 27 04 1 STROBE MEMORY B
STROP3	061	05 14 22 1 SET TAPE READER OPERATION BIT 3
STRT RESET	037	05 09 07 1 START RESET TYPewriter
SW A1 THRU A8	051	04 03 01 0 - 05 03 22 1 SWITCH INSTRUCTION ADDRESS BITS 1 THRU 8
SW ADR HOLD	069	04 03 02 0 - 05 03 14 1 SWITCH ADDRESS HOLD
SW ADV NOT	050	04 15 01 0 - 05 15 17 1 INVERSE SW ADV
SW ADV	050	04 15 01 0 - 05 15 17 1 SWITCH ADVANCE
SW A13 DATA	066	04 02 01 0 - 05 02 14 1 SWITCH LATCH 3 AT END OF ACCUMULATOR INSTRUCTION CHANNEL DATA
SW A13 IA	066	04 02 01 0 - 05 02 14 1 SWITCH LATCH 3 AT END OF ACCUMULATOR INSTRUCTION CHANNEL INSTRUCTION ADDRESS
SW ALL RC	004	04 04 02 0 - 05 04 06 1 SWITCH ALL BIT GATES SCOPE SYNC
SW ALL CLOCKS	004	04 04 02 0 - 05 04 06 1 SWITCH ALL CLOCK PULSES SCOPE SYNC
SW ALL PHASE	004	04 04 02 0 - 05 04 06 1 SWITCH ALL PHASES SCOPE SYNC
SW AUTO	049	04 15 01 0 - 05 15 01 1 SWITCH AUTO
SW B16 THRU B25	051	04 03 02 0 - 05 03 21 1 SWITCH BITS 16 THRU 25
SW B1 THRU B15	051	04 03 02 0 - 05 03 20 1 SWITCH BITS 1 THRU 15
SW B61 THRU 14	004	04 04 02 0 - 05 04 05 1 SWITCH BIT GATES 1 THRU 14 SYNC SELECT GENERATION
SW CCM X Y Z	004	04 04 02 0 - 05 04 06 1 SWITCH CLOCK PULSES W X Y Z SYNC
SW CD RST NOT	069	04 03 01 0 - 05 03 16 1 INVERSE SW CD RST

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

Figure 10-28 Sheet Number

Symbol

SW CD RST	069	04 03 01 0 - 05 03 15 1 SWITCH COMPUTER DISPLAY RESET
SW CST	069	05 04 12 1 SWITCH COMPUTER SINGLE STEP
SW DA MM	051	04 03 01 0 - 05 03 19 1 SWITCH DATA ADDRESS MEMORY MODULE
SW DU	049	04 15 01 0 - 05 15 01 1 SWITCH DATA DISPLAY
SW DIR NOT	050	04 15 01 0 - 05 15 15 1 INVERSE SW DIR
SW DIR	050	04 15 01 0 - 05 15 15 1 SWITCH DIRECTION
SW DSL THRU ↕	051	04 03 01 0 - 05 03 19 1 SWITCH DATA SECTORS 1 THRU ↕
SW ERR RST	048	04 14 01 0 - 05 14 06 1 SWITCH ERROR RESET
SW ERR TEST NOT	049	04 15 01 0 - 05 15 02 1 INVERSE SW ERR TEST
SW ERR TEST	049	04 15 01 0 - 05 15 02 1 SWITCH ERROR TEST
SW FRSS NOT	046	04 15 01 0 - 05 15 03 1 SWITCH FREE RUN SINGLE SHOT INVERSE
SW FRTR NOT	050	04 15 01 0 - 05 15 17 1 INVERSE SW FRTR
SW FRTR	050	05 15 14 1 SWITCH FREE RUN TAPE READER
SW FRTR		04 15 01 0 - 05 15 14 1 SWITCH FREE RUN TAPE READER
SW IA MM	051	04 03 01 0 - 05 03 22 1 SWITCH INSTRUCTION ADDRESS MEMORY MODULE
SW IA NOT	049	04 15 01 0 - 05 15 02 1 INVERSE SW IA
SW IA	049	04 15 01 0 - 05 15 02 1 SWITCH INSTRUCTION ADDRESS
SW ISI THRU ↕	051	04 03 01 0 - 05 03 22 1 SWITCH INSTRUCTION SECTORS 1 THRU ↕
SW LAMP TEST IA	049	04 15 01 0 - 05 15 20 1 SWITCH LAMP TEST CIRCUIT IA

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SW LAMP TEST 1	049	04 15 01 0 - 05 15 01 1 LAMP TEST PANEL 1
SW LAMP TEST 2A	049	04 15 01 0 - 05 15 21 1 SWITCH LAMP TEST CIRCUIT 2A
SW LAMP TEST 2	057	04 03 02 0 - 05 03 08 1 SWITCH LAMP TEST 2
SW LAMP TEST 2		04 16 04 0 - 05 16 01 1 SWITCH LAMP TEST CIRCUIT 2
SW MAN	049	04 15 01 0 - 05 15 01 1 SWITCH MANUAL
SW ML	049	04 15 01 0 - 05 15 01 1 SWITCH MEMORY LOAD
SW OAL THRU OAS	051	04 03 01 0 - 05 03 19 1 SWITCH OPERAND ADDRESS BITS 1 THRU 3
SW OAA	051	04 03 02 0 - 05 03 20 1 SWITCH OPERAND ADDRESS BIT 4
SW OAS THRU OAP	051	04 03 01 0 - 05 03 19 1 SWITCH OPERAND ADDRESS BITS 5 THRU 9
SW OPI THRU OP4	051	04 03 02 1 - 05 03 19 1 SWITCH OPERATION BITS 1 THRU 4
SW PA PB PC	004	04 04 02 0 - 05 04 06 1 SWITCH PHASE A B AND C SCOPE SYNC
SW PREG A 11 - 13	036	04 13 04 0 - 05 13 20 1 PROGRAM REGISTER A SWITCHES 11 - 13
SW PREG A 14	036	04 13 04 0 - 05 13 22 1 PROGRAM REGISTER A SWITCH 14
SW PREG A 15	036	04 13 04 0 - 05 13 19 1 PROGRAM REGISTER A SWITCH 15
SW PREG A 16 - 19	036	04 13 04 0 - 05 13 21 1 PROGRAM REGISTER A SWITCHES 16 - 19
SW PREG A 20 21	036	04 13 04 0 - 05 13 14 1 PROGRAM REGISTER A SWITCHES 20 21
SW PREG A 22 - 25	036	04 13 04 0 - 05 13 15 1 PROGRAM REGISTER A SWITCHES 22 - 25
SW PREG A 1 2	036	04 13 04 0 - 05 13 16 1 PROGRAM REGISTER A SWITCHES 1 2
SW PREG A 3 TO 5	036	04 13 04 0 - 05 13 17 1 PROGRAM REGISTER A SWITCHES 3 TO 5
SW PREG A 6 TO 8	036	04 13 04 0 - 05 13 18 1 PROGRAM REGISTER A SWITCHES 6 TO 8

ALD and/or Figure 10-4 LN Number
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Figure 10-28
Sheet Number

Symbol

SW PREG A 9 - 10	036	04 13 04 0 - 05 13 19 1	PROGRAM REGISTER A SWITCHES 9 TO 10
SW PREG A SGM	036	04 13 04 0 - 05 13 16 1	PROGRAM REGISTER A SWITCH SIGN
SW PREG B 11 - 13	036	04 13 04 0 - 05 13 20 1	PROGRAM REGISTER B SWITCHES 11 - 13
SW PREG B 15	036	04 13 04 0 - 05 13 19 1	PROGRAM REGISTER B SWITCH 15
SW PREG B 15		04 13 04 0 - 05 13 22 1	PROGRAM REGISTER B SWITCH 14
SW PREG B 16 - 19	036	04 13 04 0 - 05 13 21 1	PROGRAM REGISTER B SWITCHES 16 - 19
SW PREG B 20 21	036	04 13 04 0 - 05 13 14 1	PROGRAM REGISTER B SWITCHES 20 21
SW PREG B 22 - 25	036	04 13 04 0 - 05 13 15 1	PROGRAM REGISTER B SWITCHES 22 - 25
SW PREG B 1 2	036	04 13 04 0 - 05 13 16 1	PROGRAM REGISTER B SWITCHES 1 2
SW PREG B 3 TO 5	036	04 13 04 0 - 05 13 17 1	PROGRAM REGISTER B SWITCHES 3 TO 5
SW PREG B 6 TO 8	036	04 13 04 0 - 05 13 18 1	PROGRAM REGISTER B SWITCHES 6 TO 8
SW PREG B 9 - 10	036	04 13 04 0 - 05 13 19 1	PROGRAM REGISTER B SWITCHES 9 TO 10
SW PREG B SGM	036	04 13 04 0 - 05 13 16 1	PROGRAM REGISTER B SWITCH SIGN
SW RESET 1	046	04 15 01 0 - 05 15 03 1	SWITCH RESET CIRCUIT 1
SW RESET 2	047	04 15 01 0 - 05 15 13 1	SWITCH RESET CIRCUIT 2
SW RPT NOT	061	04 14 01 0 - 05 14 23 1	INVERSE SW RPT
SW RPT PRG CYC	069	04 03 02 0 - 05 03 14 1	SWITCH REPEAT PROCESS CYCLE
SW RPT	061	04 14 01 0 - 05 14 23 1	SWITCH REPEAT
SW	008	05 07 11 1	SHIFT W CLOCK TIME
SW SEL ADR	046	04 15 02 0 - 05 15 05 1	SWITCH SELECT ADDRESS

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SW SCDTC NOF	061	04 14 01 0 - 05 14 21 1	ADDRESS COMPUTER INVERSE LEVEL
SW SCDTC	061	04 14 01 0 - 05 14 21 1	ADDRESS COMPUTER
SW SIGM	051	04 03 02 0 - 05 03 19 1	SWITCH SIGN
SW SINGLE DIS	069	04 03 02 0 - 05 03 16 1	SWITCH SINGLE DISPLAY
SW SING STEP MODE	069	04 03 02 0 - 05 03 14 1	SWITCH SINGLE STEP
SW START NOF	050	04 15 01 0 - 05 15 17 1	INVERSE SW START
SW START	050	04 15 01 0 - 05 15 17 1	SWITCH START
SW START SS	046	05 15 03 1	SWITCH START SINGLE SHOT
SW START SS	050	04 15 01 0 - 05 15 03 1	SWITCH START SINGLE SHOT
SW STOP	050	04 15 01 0 - 05 15 16 1	SWITCH STOP
SW SYL	051	04 03 01 0 - 05 03 22 1	SWITCH SYL INSTRUCTION TAPE
SW TAAORI-5	051	04 03 02 0 - 05 03 21 1	SWITCH TAPE ADDRESS BITS 1 THRU 5
SW TA PWR	050	04 15 01 1 - 05 15 16 1	SWITCH TAPE POWER
SW TACB1 2	047	04 15 02 0 - 05 15 11 1	SWITCH TAPE READER CHARACTER BIT 1 2
SW TACB3 THRU 6	047	04 15 02 0 - 05 15 12 1	SWITCH TAPE READER CHARACTER BITS 3 THRU 6
SW TACB7 THRU 9	047	04 15 02 0 - 05 15 13 1	SWITCH TAPE READER CHARACTER BIT 7 THRU 9
SW TACHI-5 01	059	04 14 01 0 - 05 14 05 1	SWITCH TAPE READER CHANNEL 1 THRU 5 FROM PANEL 1
SW TACHI-6 02	059	04 14 01 0 - 05 14 05 1	SWITCH TAPE READER CHANNEL 1 THRU 6 FROM PANEL 2

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

SW TR RST	049	04 15 01 0 - 05 15 20 1	SWITCH TAPE READER RESET
SW TRS	066	04 02 01 0 - 05 02 14 1	SWITCH TRANSFER REGISTER SERIAL
SW VER ONLY NOT	049	04 15 01 0 - 05 15 19 1	INVERSE SW VER ONLY
SW VER ONLY	049	04 15 01 0 - 05 15 19 1	SWITCH VERIFY ONLY
SK	008	05 07 11 1	SHIFT X CLOCK TIME
SYLO DR IND	069	05 03 18 1	SYLLABLE 0 BUFFER REGISTER INDICATOR DRIVER
SYLO RR NOT	069	05 03 18 1	INVERSE SYLO RR
SYLO BR	069	05 03 18 1	SYLLABLE 0 BUFFER REGISTER
SYLI BR IND	069	05 03 18 1	SYLLABLE 0 BUFFER REG INDICATOR DRIVER
SYLI BR NOT	069	05 03 18 1	INVERSE SYLI BR
SYLI BR	069	05 03 18 1	SYLLABLE 1 BUFFER REGISTER
SYL 0 1 IND 1 2	019	05 20 18 1	SYLLABLE 0 1 INDICATOR DRIVERS 1 2
SYL 0	025	05 05 05 1	SYLLABLE 0 CONTROLS MEMORY READ WRITE SYLLABLE 0
SYL 0 SYL 1	027	05 27 01 1	SYLLABLE 0, SYLLABLE 1, MEMORY CONTROL LEVELS
SYL 1	025	05 05 05 1	SYLLABEE 1 CONTROLS MEMORY READ WRITE SYLLABLE 1
SYL C1 NOT	019	05 05 03 1	INVERSE SYL C1
SYL C1	019	05 05 03 1	SYLLABLE 1 CONTROL
SYNC A	025	05 05 12 1	SYNC A GENERATES MEMORY A TIMING
SYNC B	025	05 05 12 1	SYNC B GENERATES MEMORY B TIMING
SYNC CTRL NT	004	05 04 01 1	INVERSE SYNC CTRL

Figure 10-28
ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
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Symbol

SYNC CTRL	004	05 04 01 1	SYNC CONTROL FROM EXTERNAL SOURCE DELAYED PHASE B
SZ	008	05 07 11 1	SHIFT 2 CLOCK TIME
T1	038	05 09 09 1	TILT ONE
T1 W	038	05 09 09 1	TILT 1 PRINT DRIVER OUTPUT
T2	038	05 09 09 1	TILT TWO
T2 W	038	05 09 09 1	TILT 2 PRINT DRIVER OUTPUT
TAADRIA - TAADR3A	053	05 16 13 1	TAPE ADDRESS BITS 1 TO 3 FROM DRIVE SOURCE A
TAADR1-TAADR3 NOT A	053	05 16 13 1	INVERSE TAADRIA THRU 3A
TAADR1 -3 IND	053	05 16 13 1	TAADR1 -3 INDICATOR DRIVERS
TAADR4A - TAADR5A	053	05 16 14 1	TAPE ADDRESS BITS 4 THRU 5 FROM DRIVE SOURCE A
TAADR4-TAADR5 NOT A	053	05 16 14 1	INVERSE TAADR4A THRU 5A
TAADR4 - 5 IND	053	05 16 14 1	TAADR4 -5 INDICATOR DRIVERS
TAB CRTM IMLK	038	05 09 10 1	DEGATE LEVEL PRINT CONTROL TYPEWRITER FEEDBACK
TAB MAG	038	05 09 09 1	TABULATOR MAGNET DRIVER OUTPUT
TAOR	067	05 03 12 1	TRANSFER ADDRESS DISPLAY REGISTER
TAPB NOT	048	05 14 06 1	INVERSE TAPB
TAPB	048	05 14 06 1	TRACH PARITY BIT
TA PWR ERR INT	049	05 15 14 1	TAPE POWER ERROR INTERRUPT
TA PWR RLY CRD	049	05 15 21 1	TAPE POWER RELAY GROUND
TA	017	05 05 09 1	TRANSFER ADDRESS ONE OUTPUT FROM LATCH

Figure 10-28 ALD and/or Figure 10-4 LN Number
 Sheet Number and Symbol Definition

Symbol	Figure 10-28 Sheet Number	ALD and/or Figure 10-4 LN Number	Symbol Definition
TATC	061	05 14 21 1	TRANSFER ADDRESS TO COMPUTER
TAZ	017	05 05 09 1	TRANSFER ADDRESS ZERO OUTPUT FROM LATCH
TBC	005	05 06 09 1	ONE OUTPUT OF TIMING LATCH FROM BIT GATE 3 CLOCK Y PHASE B TO BIT GATE 1 CLOCK PULSE Y PHASE A
TBR NOT	008	05 07 07 1	INVERSE TBR
TBR	008	05 07 07 1	TRANSFER BUFFER REGISTER
TDTTC	061	05 14 21 1	TRANSFER DATA TO COMPUTER
TILT ROTATE GATE	037	05 09 06 1	GATES PRINT DRIVER OUTPUTS
TILT SELECT	037	05 09 06 1	GATES PRINT CONTROL DRIVER OUTPUTS
TIME 015 030	045	05 11 08 1	015 TO 030 TIME PRINTER CLOCK
TIME 060 090	045	05 11 08 1	060 TO 090 TIME PRINTER CLOCK
TIME 090 000	045	05 11 08 1	090 TO 000 TIME PRINTE CLOCK
TIME 105 000	045	05 11 08 1	105 TO 000 TIME PRINTER CLOCK
TPE IND	048	05 14 01 1	TAPE ERROR INDICATOR DRIVER
TPE	048	05 14 01 1	TAPE ERROR
TR10 11 12	009	05 07 15 1	TRANSFER REGISTER 10 11 12
TR120 NOT	009	05 07 15 1	INVERSE TR120
TR120	009	05 07 15 1	TRANSFER REGISTER 12 DELAYED
TR13 NOT	009	05 07 11 1	INVERSE TR13
TR13	009	05 07 11 1	TRANSFER REGISTER 13
TR10 NOT	009	05 07 13 1	INVERSE TR10

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Figure 10-28
Sheet Number

Symbol

TR1D	009	05 07 13 1	TRANSFER REGISTER 1 DELAYED
TR1 NOT	009	05 07 05 1	INVERSE TR1
TR1	009	05 07 05 1	TRANSFER REGISTER 1
TR2 3 4 NOT	009	05 07 12 1	INVERSE TR2 3 4
TR2 3 4	009	05 07 12 1	TRANSFER REGISTER 2 3 4
TR3D NOT	009	05 07 13 1	INVERSE TR3D
TR3D	009	05 07 13 1	TRANSFER REGISTER 3 DELAYED
TR5 6 7 NOT	009	05 07 14 1	INVERSE TR5 6 7
TR5 6 7	009	05 07 14 1	TRANSFER REGISTER 5 6 7
TR6D	009	05 07 13 1	TRANSFER REGISTER 6 DELAYED
TR8 NOT	009	05 07 13 1	INVERSE TR8
TR8	009	05 07 13 1	TRANSFER REGISTER 8
TR9D NOT	009	05 07 16 1	INVERSE TR9D
TR9D	009	05 07 16 1	TRANSFER REGISTER 9 DELAYED
TR9	009	05 07 16 1	TRANSFER REGISTER 9
TRAI THRU 4 IND	056	05 16 17 1	TAPE READER ADDRESS BITS 1 THRU 4 INDICATOR DRIVERS
TRAI THRU 4 IND		05 16 17 1	TAPE READER ADDRESS BITS A1 THRU A4 INDICATOR DRIVERS
TRAI THRU 4 NOT	056	05 16 17 1	INVERSE TRAI THRU 4
TRAI THRU 4 NOT		05 16 17 1	INVERSE TRAI THRU A4

Figure 10-28 ALD and/or Figure 10-4 LN Number
and Symbol Definition

Symbol

TR1 THRU 4	056	05 16 17 1 TAPE READER ADDRESS BITS 1 THRU 4
TR1 THRU 4		05 16 17 1 TAPE READER ADDRESS BITS A1 THRU A4
TRAS THRU 8 IND	056	05 16 18 1 TAPE READER ADDRESS BITS 5 THRU 8 INDICATOR
TRAS THRU 8 IND		05 16 18 1 TAPE READER ADDRESS BITS A5 THRU A8 INDICATOR DRIVERS
TRAS THRU 8 NOT	056	05 16 18 1 INVERSE TRAS THRU 8
TRAS THRU 8 NOT		05 16 18 1 INVERSE TRAS THRU A8
TRAS THRU 8	056	05 16 18 1 TAPE READER ADDRESS BITS 5 THRU 8 DRIVERS
TRAS THRU 8		05 16 18 1 TAPE READER ADDRESS BITS A5 THRU A8
TRACK 1 TRACK 2	048	04 14 01 0 - 05 14 02 1 TAPE READER TRACKS 1 AND 2
TRACK 3 TRACK 4	048	04 14 01 0 - 05 14 03 1 TAPE READER TRACKS 3 AND 4
TRACK 5 TRACK 6	048	04 14 01 0 - 05 14 04 1 TAPE READER TRACKS 5 AND 6
TRACK 7 TRACK 8	048	04 14 01 0 - 05 14 06 1 TAPE READER TRACKS 7 AND 8
TRANS IMH NOT	049	05 15 19 1 INVERSE TRANSFER INHIBIT
TRA PB	069	05 03 17 1 TRANSFER PARITY BIT
TRB12 - TRB15 IND	057	05 16 04 1 TRB12 - TRB15 INDICATOR DRIVERS
TRB12 - TRB15 NOT	057	05 16 04 1 INVERSE TRB12 - TRB15
TRB12 - TRB15	057	05 16 04 1 TAPE READER BITS 12 TO 15
TRB16 - TRB19 IND	058	05 16 05 1 TRB16 - TRB19 INDICATOR DRIVERS
TRB16 - TRB19 NOT	058	05 16 05 1 INVERSE TRB16 - TRB19

ALD and/or Figure 10-4 LN Number
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Sheet Number

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TRB16 - TRB19	058	05 16 05 1	TAPE READER BITS 16 TO 19
TRB1 - TRB3 IND	057	05 16 01 1	TRB1 - TRB3 INDICATOR DRIVERS
TRB1 - TRB3 NOT	057	05 16 01 1	INVERSE TRB1 - TRB3
TRB1 - TRB3	057	05 16 01 1	TAPE READER BITS 1 THRU 3
TRB20 - TRB23 IND	058	05 16 06 1	TRB20 - TRB23 INDICATOR DRIVERS
TRB20 - TRB23 NOT	058	05 16 06 1	INVERSE TRB20 - TRB23
TRB20 - TRB23	058	05 16 06 1	TAPE READER BITS 20 TO 23
TRB24 - TRB25 IND	058	05 16 07 1	TRB24 - TRB25 INDICATOR DRIVERS
TRB24 - TRB25 NOT	058	05 16 07 1	INVERSE TRB24 - TRB25
TRB24 - TRB25	058	05 16 07 1	TAPE READER BITS 24 AND 25
TRB4 - TRB7 IND	057	05 16 02 1	TRB4 - TRB7 INDICATOR DRIVERS
TRB4 - TRB7 NOT	057	05 16 02 1	INVERSE TRB4 - TRB7
TRB4 - TRB7	057	05 16 02 1	TAPE READER BITS 4 TO 7
TRB8 - TRB11 IND	057	05 16 03 1	TRB8 - TRB11 INDICATOR DRIVERS
TRB8 - TRB11 NOT	057	05 16 03 1	INVERSE TRB8 - TRB11
TRB8 - TRB11	057	05 16 03 1	TAPE READER BITS 8 TO 11
TRC81A 2A	047	05 15 11 1	TAPE READER CHARACTER COUNTER BITS 1 AND 2 FROM DRIVE SOURCE A
TRC81 TRC82 NOT	047	05 15 11 1	INVERSE TRC81 TRC82
TRC83A-6A	047	05 15 12 1	TAPE READER CHARACTER COUNTER BITS 3 THRU 6 FROM DRIVE SOURCE A

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TRCB3	TRCB6 NOT	047	05 15 12 1	INVERSE TRCB3 THRU TRCB6
TRCB7A-9A		047	05 15 13 1	TAPE READER CHARACTER COUNTER BITS 7 THRU 9 FROM DRIVE SOURCE A
TRCB7	TRCB9 NOT	047	05 15 13 1	INVERSE TRCB7 THRU TRCB 9
TRCH 1A NOT		048	05 14 02 1	INVERSE TRCH 1A
TRCH 1A		048	05 14 02 1	TAPE READER CHANNEL 1 FROM DRIVE SOURCE A
TRCH 2A NOT		048	05 14 02 1	INVERSE TRCH 2A
TRCH 2A		048	05 14 02 1	TAPE READER CHANNEL 2 FROM DRIVE SOURCE A
TRCH 3A-4A NOT		048	05 14 03 1	INVERSE TRCH 3A-4A
TRCH 3A-4A		048	05 14 03 1	TAPE READER CHANNELS 3 AND 4 FROM DRIVE SOURCE A
TRCH 5A-6A NOT		048	05 14 04 1	INVERSE TRCH 5A-6A
TRCH 5A-6A		048	05 14 04 1	TAPE READER CHANNELS 5 AND 6 FROM DRIVE SOURCE A
TRCLA		049	05 15 19 1	TAPE READER CLEAR AND ADD
TRCP1 2 ERROR NOT		046	05 15 06 1	TAPE READER CLOCK PULSES 1 AND 2 ERROR LEVEL INVERSED
TRCP1 A		046	05 15 04 1	TAPE READER CLOCK PULSE 1 FROM DRIVE SOURCE A
TRCP1 NOT A		046	05 15 04 1	INVERSE TAPE READER CLOCK PULSE 1 A
TRCP2 A		046	05 15 04 1	TAPE READER CLOCK PULSE 1 FROM DRIVE SOURCE A
TRCP2 NOT A		046	05 15 04 1	INVERSE TAPE READER CLOCK PULSE 2 A
TRCP3 4 ERROR NOT		046	05 15 06 1	TAPE READER CLOCK PULSES 3 AND 4 ERROR LEVEL INVERSED

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TRCP3 A	046	05 15 05 1	TAPE READER CLOCK PULSE 3 FROM DRIVE SOURCE A
TRCP3 NOT A	046	05 15 05 1	INVERSE TRCP3 A
TRCP4 A	046	05 15 05 1	TAPE READER CLOCK PULSE 4 FROM DRIVE SOURCE A
TRCP4 NOT A	046	05 15 05 1	INVERSE TRCP4 A
TRCP ERR DLY	046	05 15 07 1	TAPE READER CLOCK PULSE ERROR DELAY
TRCP ERR IND	046	05 02 05 1	TAPE READER CLOCK PULSE ERROR INDICATOR DRIVER
TRCP ERR NOT	046	05 15 07 1	INVERSE TRCP ERR
TRCP ERR	046	05 15 07 1	TAPE READER CLOCK PULSE ERROR
TRCP GEN	046	05 15 03 1	TAPE READER CLOCK PULSE GENERATOR
TRDA PB NOT	060	05 14 09 1	INVERSE TRDA
TRDA PB	060	05 14 09 1	TAPE READER DATA PARITY BIT
TRDA RST	049	05 15 20 1	TAPE READER DATA RESET
TRDMO 1 IND	053	05 16 15 1	TAPE READER DATA MODULES 0 AND 1 INDICATOR DRIVER
TRDMO 1 IND		05 16 15 1	TAPE READER DATA MODULES 0 AND 1 INDICATOR DRIVERS
TRDMO 1	053	05 16 15 1	TAPE READER DATA MODULES 0 AND 1
TRDMO 1		05 16 15 1	TAPE READER DATA MODULES 0 AND 1
TRDS1 - TRDS4 IND	055	05 16 12 1	TRDS1 - TRDS4 INDICATOR DRIVERS
TRDS1 - TRDS4 NOT	055	05 16 12 1	INVERSE TRDS1 - TRDS4
TRDS1 - TRDS4	055	05 16 12 1	TAPE READER DATA SECTOR BITS 1 THRU 4
TRIA PB NOT	060	05 14 10 1	INVERSE TRIA PB

Figure 10-28
 AID and/or Figure 10-4 LN Number
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TRIA PB	060	05 14 10 1 TAPE READER INSTRUCTION ADDRESS PARITY BIT
TRIA RST	049	05 15 20 1 TAPE READER INSTRUCTION RESET
TRIMD 1 IA IND	054	05 16 19 1 TAPE READER INSTRUCTION MODULES 0 AND 1 INDICATOR DRIVERS
TRIMD 1 IA	054	05 16 19 1 TAPE READER INSTRUCTION MODULES 0 AND 1 INSTRUCTION ADDRESS
TRISI THRU 4 IND	054	05 16 16 1 TAPE READER INSTRUCTION SECTOR 1 THRU 4 INDICATOR DRIVERS
TRISI THRU 4 IND		05 16 16 1 TAPE READER INSTRUCTION SECTOR 1 THRU 4 INDICATOR DRIVERS
TRISI THRU 4 NOT	054	05 16 16 1 INVERSE TRISI THRU 4
TRISI THRU 4 NOT		05 16 16 1 INVERSE TRISI THRU 4
TRISI THRU 4	054	05 16 16 1 TAPE READER INSTRUCTION SECTOR 1 THRU 4
TRISI THRU 4		05 16 16 1 TAPE READER INSTRUCTION SECTOR 1 THRU 4
TROA1 - TROA4 IND	052	05 16 08 1 TROA1 - TROA4 INDICATOR DRIVERS
TROA1 - TROA4 NOT	052	05 16 08 1 TROA1 - TROA4 INVERSED
TROA1 - TROA4	052	05 16 08 1 TAPE READER OPERAND ADDRESS BITS 1 TO 4
TROA5 - TROA7 IND	052	05 16 09 1 TROA5 - TROA7 INDICATOR DRIVERS
TROA5 - TROA7 NOT	052	05 16 09 1 INVERSE TROA5 - TROA7
TROA5 - TROA7	052	05 16 09 1 TAPE READER OPERAND ADDRESS BITS 5 TO 7
TROA8 - TROA9 IND	052	05 16 10 1 TROA8 - TROA9 INDICATOR DRIVERS
TROA8 - TROA9 NOT	052	05 16 10 1 INVERSED TROA8 - TROA9

Figure 10-28 ALD and/or Figure 10-4 LN Number
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TRDAB - TRDA9	052	05 16 10 1	TAPE READER OPERAND ADDRESS BITS 0 AND 9
TROP1 - TROP4 IMD	055	05 16 11 1	TRCP1 - TROP4 INDICATOR DRIVERS
TROP1 - TRUP4 NOT	055	05 16 11 1	INVERSE TROP1 - TROP4
TROP1 - TROP4	055	05 16 11 1	TAPE READER OPERATION BITS 1 THRU 4
TR DA RST	049	05 15 20 1	TAPE READER DATA RESET
TR IMD INH NOT	023	05 13 01 1	TRANSFER REGISTER INDICATOR INHIBIT INVERSED
TR REG SW	023	04 13 03 0 - 05 13 01 1	TRANSFER REGISTER SWITCH
TR SYL 0 PB IMD	060	05 14 08 1	TAPE READER SYLLABLE 0 PARITY BIT INDICATOR DRIVE
TR SYL 0 PB NOT	060	05 14 08 1	INVERSE TR SYL 0 PB
TR SYL 0 PB	060	05 14 08 1	TAPE READER SYLLABLE 0 PARITY BIT
TR SYL 1 PB IMD	060	05 14 07 1	TAPE READER SYLLABLE 1 INDICATOR DRIVER OUTPUT
TR SYL 1 PB NOT	060	05 14 07 1	INVERSE TR SYL 1 PB
TR SYL 1 PB	060	05 14 07 1	TAPE READER SYLLABLE 1 PARITY BIT
TRSIGN IMD	057	05 16 01 1	TAPE READER SIGN INDICATOR DRIVER
TRSIGN NOT	057	05 16 01 1	INVERSE TRSIGN
TRSIGN	057	05 16 01 1	TAPE READER SIGN
TRS NOT	009	05 07 16 1	INVERSE TRS
TRS	009	05 07 16 1	TRANSFER REGISTER SERIAL
TRSTO	061	05 14 21 1	TAPE READER STORE OPERATION DECODED
TRSYLO 1 IMD	054	05 16 19 1	TAPE READER SYLLABLES 0 AND 1 INDICATOR DRIVERS

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TRSYLO 1 IND		05 16 19 1	TAPE READER SYLLABLES 0 AND 1
TRSYLO 1	054	05 16 19 1	TAPE READER SYLLABLES 0 AND 1
TRSYLO 1		05 16 19 1	TAPE READER SYLLABLES 0 AND 1
T D OFF	042	05 11 02 1	TIME DELAY HAMMER RESTORE POWER OFF
TTT	008	05 07 09 1	INDICATES NO TRANSFER OPERATION
TW SENA MB9 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB9 SEG 2
TW SEN A MB10 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB10 SEG 1
TW SEN A MB10 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB10 SEG 2
TW SEN A MB11 SLG2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB11 SEG 2
TW SEN A MB11 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB11 SEG 1
TW SEN A MB12 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB12 SEG 1
TW SEN A MB12 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB12 SEG 2
TW SEN A MB13 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB12 SEG 1
TW SEN A MB13 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A MB13 SEG 2
TW SEN A MB1 SEG 1	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A MB1 SEG 1
TW SEN A MB1 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A MB1 SEG 2
TW SEN A MB2 SEG 1	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A MB2 SEG 1
TW SEN A MB2 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A MB2 SEG 2
TW SEN A MB3 SEG 1	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A MB3 SEG 1
TW SEN A MB3 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A SEGMENT 2

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TM SEN A MB4 SEG 1	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A	MB4 SEGMENT 1
TM SEN A MB4 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A	MB4 SEG 2
TM SEN A MB5 SEG 1	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A	MB5 SEG 1
TM SEN A MB5 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A	MB5 SEG 2
TM SEN A MB6 SEG 1	028	04 28 01 0 - 05 26 01 1	TWISTED WIRE SENSE A	MB6 SEG 1
TM SEN A MB6 SEG 2	028	04 28 01 0 - 05 28 01 1	TWISTED WIRE SENSE A	MB6 SEG 2
TM SEN A MB7 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB7 SEG 1
TM SEN A MB7 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB7 SEG 2
TM SEN A MB8 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB8 SEG 1
TM SEN A MB8 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB8 SEG 2
TM SEN A MB9 SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB9 SEG 1
TM SEN A MB9 SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	MB9 SEG 2
TM SEN A PAR SEG 1	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	PAR SEG 1
TM SEN A PAR SEG 2	028	04 28 01 0 - 05 28 02 1	TWISTED WIRE SENSE A	PAR SEG 2
TM SEN B MB10 SEG 1	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB10 SEG 1
TM SEN B MB10 SEG 2	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB10 SEG 2
TM SEN B MB11 SEG 1	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB11 SEG 1
TM SEN B MB11 SEG 2	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB11 SEG 2
TM SEN B MB12 SEG 1	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB12 SEG 1
TM SEN B MB12 SEG 2	028	04 28 02 0 - 05 28 04 1	TWISTED WIRE SENSE B	MB12 SEG 2

Figure 10-28 ALD and/or Figure 10-4 LN Number
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TW SEN B MB13 SEG 1	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB13 SEG 1
TW SEN B MB13 SEG 2	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB13 SEG 2
TW SEN B MB1 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB1 SEG 1
TW SEN B MB1 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB1 SEG 2
TW SEN B MB2 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB2 SEG 1
TW SEN B MB2 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB2 SEG 2
TW SEN B MB3 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB3 SEG 1
TW SEN B MB3 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB3 SEG 2
TW SEN B MB4 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB4 SEG 1
TW SEN B MB4 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB4 SEG 2
TW SEN B MB5 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB5 SEG 1
TW SEN B MB5 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB5 SEG 2
TW SEN B MB6 SEG 1	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB6 SEG 1
TW SEN B MB6 SEG 2	028	04 28 02 0 - 05 28 03 1 TWISTED WIRE SENSE B MB6 SEG 2
TW SEN B MB7 SEG 1	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB7 SEG 1
TW SEN B MB7 SEG 2	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB7 SEG 2
TW SEN B MB8 SEG 1	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB8 SEG 1
TW SEN B MB8 SEG 2	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB8 SEG 2
TW SEN B MB9 SEG 1	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB9 SEG 1
TW SEN B MB9 SEG 2	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B MB9 SEG 2

Figure 10-28
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TM SEN B PAR SEG 1	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B PAR SEG 1
TM SEN B PAR SEG 2	028	04 28 02 0 - 05 28 04 1 TWISTED WIRE SENSE B PAR SEG 2
TX	008	05 07 05 1 TRANSFER X CLOCK TIME
TYPR READY	027	05 09 07 1 TYPERWRITER READY SENSE BY C10 214
TY	008	05 07 11 1 TRANSFER Y CLOCK TIME
TZ	008	05 07 08 1 TRANSFER BUFFER REGISTER AND 2 CLOCK TIME
UACCU	010	05 07 04 1 SPECIFIES USE OF INSTRUCTION
UC LATCH	037	05 09 05 1 UPPER CASE LATCH ONE OUTPUT
UC SHIFT MAG	037	05 09 06 1 UPPER CASE SHIFT MAGNET DRIVER OUTPUT
UC SHIFT NT	037	05 09 06 1 UPPER CASE SHIFT RESETS UC LATCH DELAYED 30MS
UTR	010	05 07 04 1 SPECIFIES USE OF OPERAND ADDRESS TO REPLACED INSTRUCTION COUNTER ADDRESS DURNING TRANSFER OR MOP OPERATION
VER ONLY IND A B	049	05 15 19 1 VERIFY ONLY INDICATOR DRIVERS A B
WAIT FOR SHIFT NT	037	05 09 07 1 DEGATE TYPERWRITER READY
WR GATE A	024	05 05 15 1 WRITE GATE MEMORY A
WR GATE A		05 27 01 1 WRITE GATE MEMORY A
WR GATE B	024	05 05 19 1 WRITE GATE B
WR GATE B		05 27 02 1 WRITE GATE MEMORY B
WR GATE NOT A	024	05 05 15 1 INVERSE WR GATE A
WR GATE NOT B	024	05 05 19 1 INVERSE WR GATE B

Figure 10-28 ALD and/or Figure 10-4 LN Number and Symbol Definition

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WR SYL1 RD SYLO GTA	026	05 27 01 1	WRITE SYLLABLE 1	READ SYLLABLE 0	GATE MEMORY A
WR SYL1 RD SYLO GTB	026	05 27 02 1	WRITE SYLLABLE 1	READ SYLLABLE 0	GATE MEMORY B
W A NOT	005	05 04 06 1	CLOCK PULSE W	AND WITH BIT GATE	LATCH A ZERO
W A	005	05 05 06 1	CLOCK PULSE W	AND WITH BIT GATE	LATCH A ONE
W DLY	004	05 04 02 1	CLOCK W	FROM EXTERNAL	SOURCE DELAYED CW
W OR CW	004	04 04 01 0 -	05 04 01 1	CLOCK PULSE W	EXTERNAL SOURCE
X AND Y COUNT RESET	039	05 10 06 1	X AND Y	COUNTER RFSET	
X COUNT 0	039	05 10 06 1	X	COUNTER	EQUAL TO ZERO
X COUNT NT 0	039	05 10 06 1	X	COUNTER	NOT ZERO
X EIGHTS 0-7 DR B	030	05 26 07 1 -	04 26 03 0	EIGHTS X C	THRU 7 DRIVES MEMORY B
X EIGHTS 0-7 RET B	030	05 26 07 1 -	04 26 03 0	EIGHTS X 0	THRU 7 RETURNS MEMORY B
X EIGHTS 0 - 7 DR A	029	05 26 03 1 -	04 26 01 0	X EIGHTS 0	THRU 7 DRIVES MEMORY A
X EIGHTS 0 - 7 RT A	029	05 26 03 1 -	04 26 01 0	X EIGHTS 0	THRU 7 RETURNS MEMORY A
X UNITS 0-7 DR B	030	05 26 06 1 -	04 26 03 0	UNITS X 0	THRU 7 DRIVES MEMORY B
X UNITS 0-7 RET B	030	05 26 06 1 -	04 26 03 0	UNITS X 0	THRU 7 RETURNS MEMORY B
X UNITS 0 TO 7 DR A	029	05 26 02 1 -	04 26 01 0	X UNITS 0	THRU 7 DRIVES MEMORY A
X UNITS 0 TO 7 RT A	029	05 26 02 1 -	04 26 01 0	X UNITS 0	THRU 7 RETURNS MEMORY A
Y COUNT NT 0	039	05 10 06 1	Y	COUNTER	NOT ZERO
Y DRIVE A	027	05 26 01 1	Y	DRIVE	MEMORY A
Y DRIVE B	027	05 26 01 1	Y	DRIVE	MEMORY B

Figure 10-28 ALD and/or Figure 10-4 LN Number
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Y EIGHTS 0-7 DR A	029	05 26 05 1 - 04 26 02 0 EIGHTS Y DRIVES 0 THRU 7 MEMORY A
Y EIGHTS 0-7 DR B	030	05 26 09 1 - 04 26 04 0 EIGHTS Y 0 THRU 7 DRIVES MEMORY B
Y EIGHTS 0-7 RET A	029	05 26 05 1 - 04 26 02 0 EIGHTS 0 THRU 7 Y RETURNS MEMORY A
Y EIGHTS 0-7 RET B	030	05 26 09 1 - 04 26 04 0 EIGHTS Y 0 THRU 7 RETURNS MEMORY B
Y JA	038	04 09 01 1 CARRIAGE OPERATION TYPEWRITER FEEDBACK
Y JB	038	04 09 01 1 CARRIAGE RETURN INDEX TYPEWRITER FEEDBACK
Y JC	038	04 09 01 1 TAB INTERLOCK TYPEWRITER FEEDBACK
Y JE	038	04 09 01 1 END OF LINE INTERLOCK TYPEWRITER FEEDBACK
Y JF	038	04 09 01 0 END OF LINE TYPEWRITER
Y JY	038	04 09 01 1 TAB INTERLOCK
Y UNITS 0-7 DR A	029	05 26 04 1 - 04 26 02 0 Y UNITS 0 THRU 7 DRIVES MEMORY A
Y UNITS 0-7 DR B	030	05 26 04 1 UNITS Y 0-7 DRIVES MEMORY A
Y UNITS 0-7 DR B	030	05 26 08 1 - 04 26 04 0 UNITS Y 0 THRU 7 DRIVES MEMORY B
Y UNITS 0-7 RET B	030	05 26 08 1 - 04 26 04 0 UNITS Y 0 THRU 7 RETURNS MEMORY B
Y UNITS 0 TO 7 RT A	029	05 26 04 1 - 04 26 02 0 Y UNITS 0 THRU 7 RETURNS MEMORY A
Y Z	038	04 09 01 0 - 05 09 10 1 PRINT FEEDBACK
ZER NOT	010	05 07 02 1 ZERO INVERSE LEVEL

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