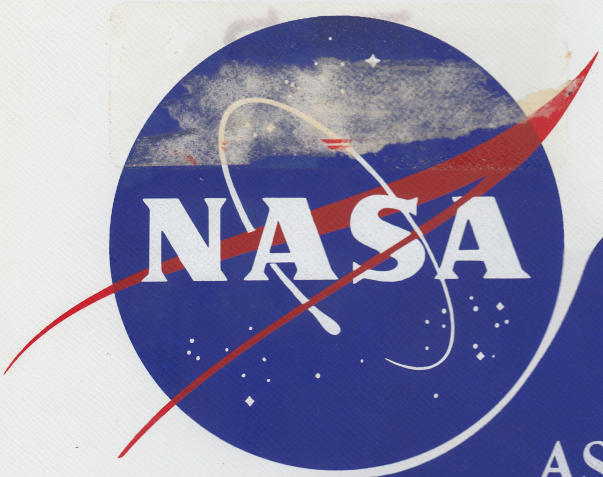

ASTRIONICS SYSTEM HANDBOOK

Saturn
Launch Vehicle

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

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ASTRIONICS SYSTEM HANDBOOK

SATURN LAUNCH VEHICLES

1 November 1968

Changed 15 November 1969

PREFACE

This second revised edition of the Astrionics System Handbook has been developed under the direction and overall supervision of Dr. Rudolf Decher of the Astrionics Systems Engineering Office.

This description of the Saturn Astrionics System has been generated by personnel of the Astrionics Laboratory, the staff of the Astrionics Systems Engineering Office, and by personnel of the International Business Machines Corporation working under Contract NAS8-14000.

The handbook will be updated and expanded as it becomes necessary due to changes or refinements in the system concept and hardware. Sections not contained in the first release of this document will be made available within three months.

Ludie G. Richard

LUDIE G. RICHARD
Chief,
Systems Engineering Office
Astrionics Laboratory

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CHAPTER 1
INTRODUCTION

SECTION 1.1
PURPOSE OF THE ASTRIONICS SYSTEM HANDBOOK

The Astrionics System consists of all electrical and electronic equipment aboard the Saturn Launch Vehicle — this Handbook describes the components which make up the Astrionics System.* Presented in fundamental terms, the descriptions are intended to explain the general operation of the components on a system level and to avoid detailed descriptions of the components themselves, if possible. However, when the operation of a component is sufficiently important to the system operation, more detailed descriptions of the component have been provided.

Primary attention has been given to the flight components of the Instrument Unit because they perform the most critical functions of the Astrionics System. Signal flow to other stages is followed only as required to provide an overall understanding of the system operation.

Secondary attention has been given to ground systems which operate with the Astrionics System to provide tracking, data processing, and other support activities for the Saturn Launch Vehicles and the Apollo Mission. The degree of detail to which these ground systems are explained is in accordance with their importance to the Astrionics System.

General mission requirements and system capabilities are briefly discussed in Chapter 1 to provide a basic understanding of the Astrionics System. Subsequent chapters present functional descriptions of the various subsystems and hardware involved.

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* Both Saturn IB and Saturn V Astrionics Systems are described in the Handbook. Because these Systems are very similar, the discussion is centered about the Saturn V Astrionics System. Specific differences between the Saturn IB and Saturn V Astrionics Systems are indicated in diagrams in Section 1.4, as well as throughout the text.

SECTION 1.2
SATURN LAUNCH VEHICLES

Figures 1.2-1 and 1.2-2 illustrate the Saturn IB Vehicle and Saturn V Vehicle, respectively, and include some characteristic vehicle data. Both vehicles have the same upper stage (the S-IVB Stage), which is propelled by a restartable engine. The Instrument Unit is mounted on top of the S-IVB Stage and is very similar for Saturn IB and Saturn V.

The primary mission of Saturn IB is to serve as a launch vehicle for the Apollo Spacecraft earth orbital flight tests. These earth orbital flights will simulate certain phases of the lunar landing mission and will provide flight tests for the spacecraft and the S-IVB/IU Stage. Saturn V is the launch vehicle for the actual Apollo lunar landing missions. The typical profile of a lunar landing mission is described in Section 1.3.

The primary objective of the Saturn Vehicles is the successful accomplishment of the Apollo mission. In addition, the Saturn Vehicles are capable of performing other types of missions which can be generally classified as the insertion of heavy payloads into earth orbits and translunar trajectories. These other missions may include:

- Transfer between earth orbits
- Rendezvous in earth orbit
- Direct ascent and injection into translunar trajectory
- Injection into translunar trajectory following extended earth-orbit phases
- Extended missions beyond injection

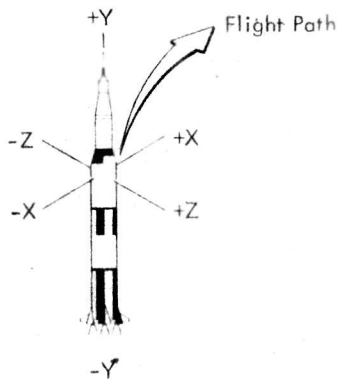
Saturn Vehicles are numbered consecutively, beginning with 201 for the first Saturn IB Flight Vehicle and 501 for the first Saturn V Flight Vehicle. The first few vehicles of each series are considered research and development vehicles.

NOTICE

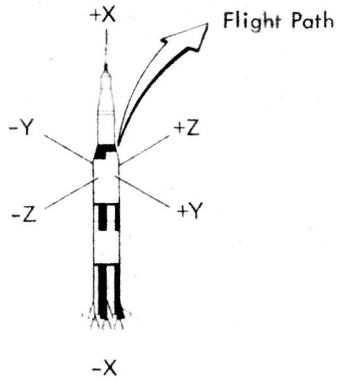
SATURN/APOLLO COORDINATE CHANGES

The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). Under these standards, the XYZ axes are defined as: the X axis is vertical through the launch site, the Z axis is parallel to the aiming azimuth, and the Y axis completes the right-handed system. Vehicle axes for roll, pitch and yaw are also defined as X, Y, and Z, respectively.

Because of Instrument Unit and vehicle configuration changes, this coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). The conversion from the old system to the new is as follows:



OLD		NEW
X	to	Z
Y	to	X
Z	to	Y



A detailed explanation of the coordinate systems can be found in Chapter 2.

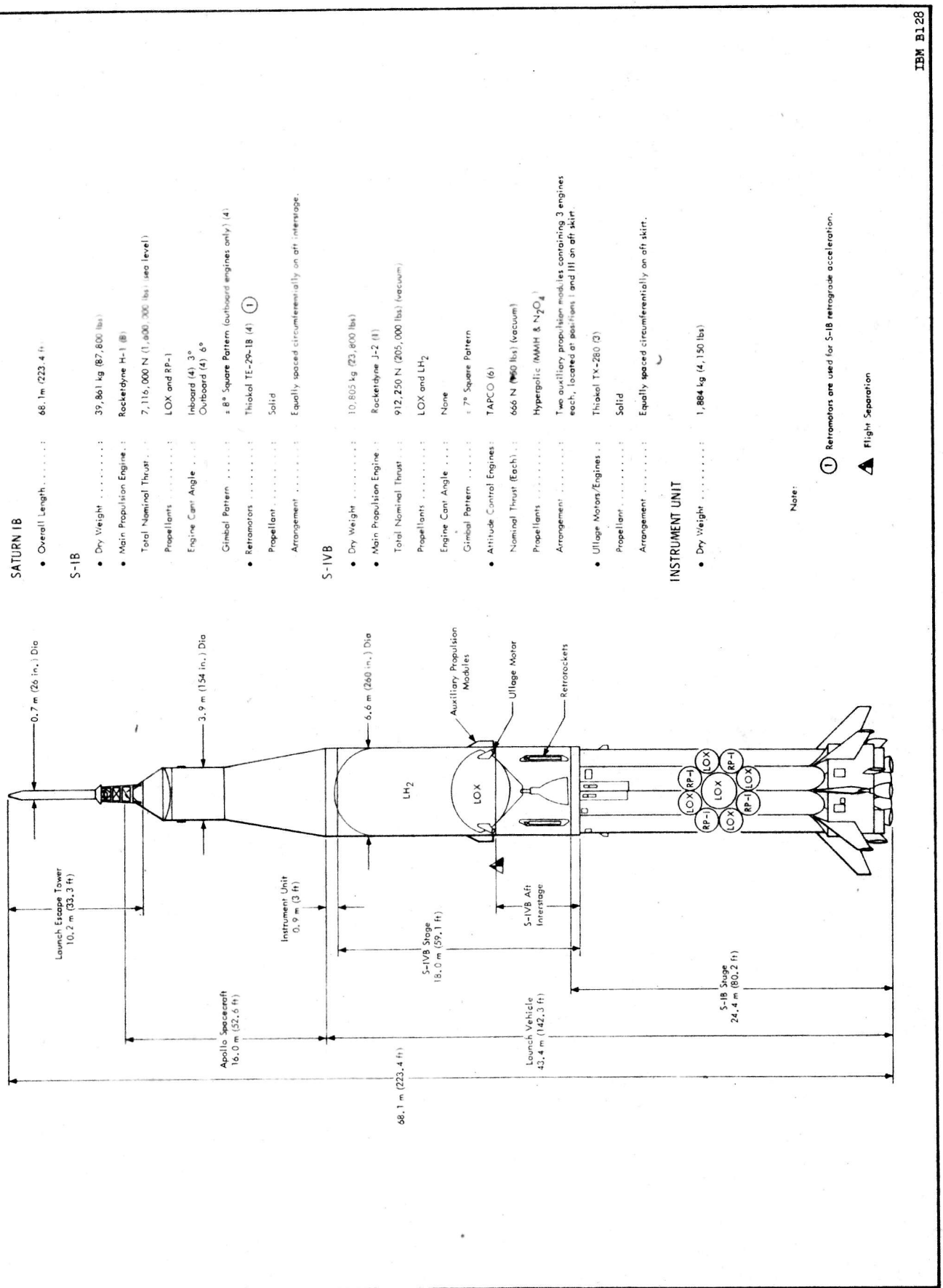
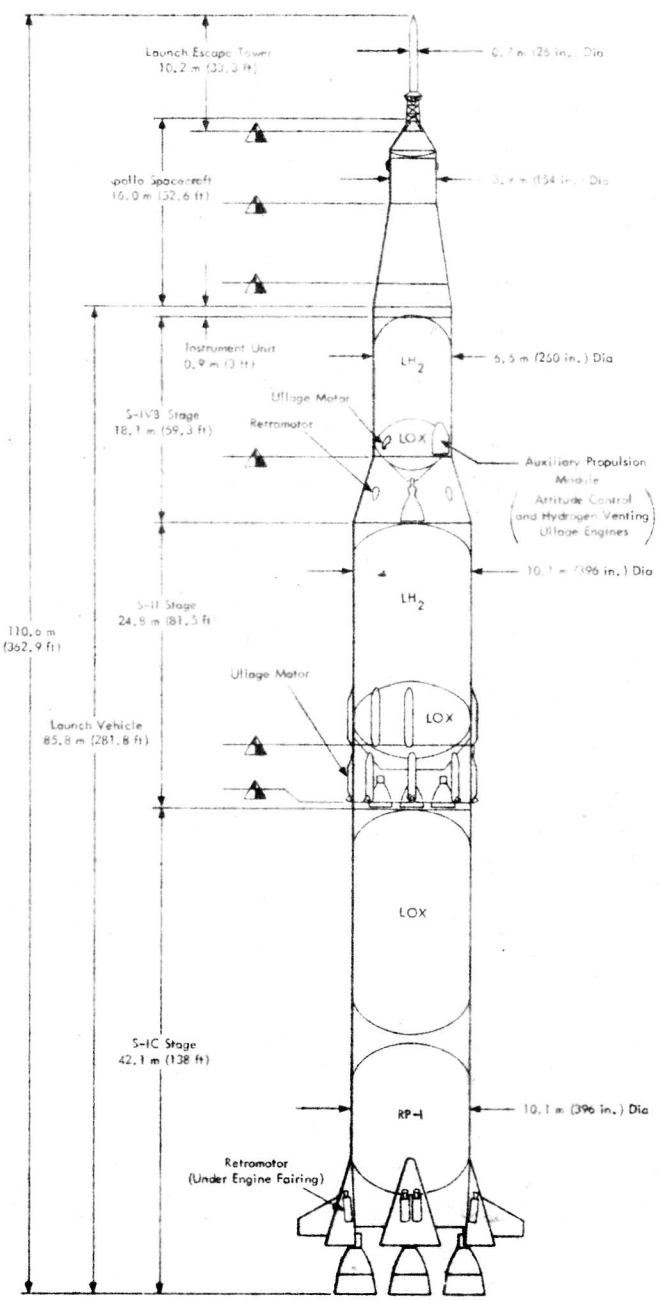


Figure 1.2-1 Saturn IB Launch Vehicle Characteristic Data



SATURN V

- Overall Length . . . . . : 110.6m (362.9 ft)

S-IC

- Dry Weight . . . . . : 136,200 Kg (300,000 lbs)
- Main Propulsion Engines : Rocketdyne F-1 (5)
  - Total Nominal Thrust . . : 33,864,500 N (7,610,000 lbs)
  - Propellants . . . . . : LOX and RP-1
  - Engine Cant Angle . . . . : Outboard Engines (4) Are Electrically Canted to 2°.
  - Gimbal Pattern . . . . . : ± 5° 9° Square Pattern (Outboard Engines (4)
- Retromotors . . . . . : 8
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Two in each F-1 engine fairing

S-II

- Dry Weight . . . . . : 37,183 kg (81,900 lbs)
- Mainstage Propellant Capacity . . . . . : 440,380 kg (970,000 lbs)
- Main Propulsion Engines : Rocketdyne J-2 (5)
  - Total Nominal Thrust . . : 4,561,250 N (1,025,000 lbs)
  - Propellants . . . . . : LOX and LH_2
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : ± 7° Square Pattern (Outboard Engines) (4)
- Ullage Motors/Engines . : RS-U-501 (8)
  - Nominal Thrust (Each) . : 101,900 N (22,900 lbs) (vacuum)
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Equally spaced around S-IC/S-II Interstage, in line with S-IC fins and positions I, II, III, & IV.

S-IVB

- Dry Weight . . . . . : 12,440 kg (27,400 lbs)
- Mainstage Propellant Capacity . . . . . : 104,420 kg (230,000 lbs)
- Main Propulsion Engine : Rocketdyne J-2 (1)
  - Total Nominal Thrust . . : 912,250 N (205,000 lbs)
  - Propellants . . . . . : LOX and LH_2
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : 7° Square Pattern
- Attitude Control Engines : TAPCO (6)
  - Nominal Thrust (Each) . : 670 N (150 lbs) (vacuum)
  - Propellants . . . . . : Hypergolic (MMH & N_2O_4)
  - Arrangement . . . . . : Two auxiliary propulsion modules containing 3 engines each, located at positions I and III on aft skirt.
- Ullage Motors/Engines . : Thiokol TX-260 (2)
  - Nominal Thrust (Each) . : 15,560 N (3,500 lbs) (vacuum)
  - Propellant . . . . . : Solid
  - Arrangement . . . . . : Equally spaced circumferentially on aft skirt.
- Hydrogen Venting Ullage Engines . . . . . : Gemini OAMS (2)
  - Nominal Thrust (Each) . : 320 N (72 lbs) (vacuum)
  - Propellants . . . . . : Hypergolic (MMH & N_2O_4)
  - Arrangement . . . . . : One in each of two auxiliary propulsion modules located at positions I and III on aft skirt.
- Retromotors . . . . . : TE-29-18 (4) (1)
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Positions I, II, III, and IV S-II/S-IVB Interstage.

INSTRUMENT UNIT

- Dry Weight . . . . . : 1,884 kg (4,150 lbs)

Note:

(1) Retromotors are used for S-II retrograde acceleration

▲ Flight Separation

IBM B129

Figure 1.2-2 Saturn V Launch Vehicle Characteristic Data

SECTION 1.3
SATURN V MISSION PROFILE

The profile of the Saturn V Launch Vehicle Mission is illustrated in Figure 1.3-1. Beginning with prelaunch checkout of the Astrionics System, the mission is divided into seven operational phases, which are referenced to specific vehicle events. These phases and their approximate time durations are shown in Table 1.3-1. The following paragraphs describe these phases in detail.

PRELAUNCH AND LIFT-OFF

The prelaunch phase includes a complete Astrionics System checkout, prelaunch program and component activity (countdown), and the actual vehicle liftoff. The prelaunch phase begins several weeks before launch and continues until the moment the vehicle leaves the launch pad.

During system checkout, all components are thoroughly tested by a complex of ground support equipment. The testing activities include stage and system checkout while the vehicle is still in the Vertical Assembly Building (VAB) and final checkout on the launch pad. These test activities are sometimes referred to as "pre-rollout" (VAB) and "post-rollout" (pad) tests.

Table 1.3-1 Saturn V Operational Phases

Phase	Approximate Duration
Prelaunch	24 hours
S-IC Burn	160 seconds
S-II Burn	385 seconds
S-IVB First Burn	150 seconds
Orbital Coast	4.5 hours
S-IVB Second Burn	355 seconds
Translunar Coast	2 hours

Preparation for launch is the next step in the prelaunch phase. During this operation, the Inertial Platform is aligned to the launch azimuth, the final launch and flight constants are loaded into the LVDC, and all final preparations are completed.

The final step in the prelaunch phase is the countdown and actual liftoff. After ignition of the five F-1 engines, complete vehicle control is transferred from the ground to the IU. The vehicle is held down for a few seconds after ignition to allow the engines to develop full thrust. The holddown arms then permit a "soft" release as the vehicle begins its vertical travel.

S-IC BURN

The second phase of the Astrionics System operation occurs during S-IC burn. During this phase, the vehicle lifts from the pad and is propelled through the denser portion of the atmosphere. This burn time will normally continue for approximately 160 seconds and terminate when the fuel supply is depleted.

Boost navigation calculations are initiated in the final seconds before liftoff and continue until the vehicle reaches earth orbit. The boost navigation routine of the flight program calculates position, thrust acceleration, and velocity in a space-fixed, inertial coordinate system. These quantities provide the necessary inputs to the guidance routines of the flight program.

Guidance of the vehicle throughout the first-stage burn is achieved through a preset time-tilt (pitch) program. Steering commands are generated as functions of time to guide the vehicle on a pre-calculated course toward the orbital objective. The vehicle is rolled into correct alignment with the flight azimuth and tilted into the correct flight attitude.

Attitude control during first-stage burn is accomplished by swivelling the four outer propulsion engines to change the direction of thrust and thereby change vehicle attitude. Thrust directions are oriented about the roll, pitch, and yaw axes of the

vehicle. The rate at which the vehicle can change its attitude or direction is controlled by programming throughout the flight to prevent structural damage to the vehicle.

Vehicle events are initiated and monitored by the LVDC in an operation called "sequencing". Generally, these sequence commands are used to initiate or terminate a particular vehicle operation (e.g., inboard engine cutoff or retromotor ignition). A detailed flight sequence can be found in Section 4.3.

Final sequencing is often referred to as "staging" and is defined as the series of events leading to stage separation. The main staging events of the S-IC Stage are: inboard engine cutoff, outboard engine cutoff, ignition of the S-II ullage motors, firing of the separation device, and ignition of the S-IC retromotors. After separation, the S-IC Stage falls to earth in a ballistic flight path.

S-II BURN

S-II Stage ignition occurs almost simultaneously with separation of the S-IC Stage. This phase of the flight is designed to continue until fuel depletion (385 seconds after S-IC separation).

Near the beginning of this operational phase, the guidance system scheme changes from a standard time-tilt mode to a path adaptive mode. This path adaptive mode is designed to guide the vehicle toward its orbital goal with greater accuracy and fuel economy. Path adaptive guidance is used for the remainder of the boost flight. Navigation and attitude control operations are a continuation of the scheme used in the S-IC phase.

The launch escape tower is jettisoned and second plane separation occurs early in this phase as part of the normal sequence. Fuel depletion sensors provide a signal to start staging operations. The five J-2 propulsion engines are shutdown simultaneously as the S-II and S-IVB Stages are prepared for staging. Basically, the staging sequence is as follows: sense low-fuel level, cutoff all 5 engines, fire the S-IVB ullage motors, fire the separation device, and fire the S-II retromotors. After separation, the S-II Stage falls to earth in a ballistic flight path.

S-IVB FIRST BURN (ORBITAL INJECTION)

The first burn of the S-IVB Stage is designed to give the vehicle its final boost into earth orbit. The burn time of the S-IVB Stage's single J-2 engine is approximately 150 seconds. Engine cutoff occurs at the instant the vehicle reaches a predetermined velocity. After cutoff, the engine is prepared for a second burn period which will occur later in the flight.

Boost navigation calculations, used in the two previous stages, are continued throughout the S-IVB first burn. These calculated quantities provide the necessary inputs to the guidance computations which become more exacting as the vehicle approaches orbital insertion and cutoff velocity. The path adaptive guidance scheme continues throughout this flight phase.

Attitude control for the S-IVB burn phase differs from the control of the other 2 stages because of the single-engine configuration. Since the single engine can only control pitch and yaw movements, an auxiliary propulsion system is utilized to control the roll functions. This system consists of ON-OFF thrust nozzles which are mounted on the aft portion of the S-IVB structure. The lateral and opposing thrust of these nozzles positions the vehicle about its roll axis as commanded by the guidance and control system.

Third-stage sequencing begins at S-II engine cutoff and continues for the remainder of the S-IVB/IU flight. Initial sequencing involves the preparation and ignition of the J-2 engine and jettisoning of the S-IVB ullage rockets. Engine cutoff at orbital insertion is commanded by the guidance system. Thereafter, the engine is purged for several minutes in preparation for a later restart when S-IVB second burn is commanded.

ORBITAL COAST

The orbital coast (earth orbit) phase of the Saturn Mission follows cutoff of the S-IVB engine. The vehicle, which is now reduced to the S-IVB/IU Stage and Apollo Spacecraft, will orbit the earth at an approximate altitude of 185 kilometers (100 nautical miles).

The orbital coast phase is scheduled to continue for a maximum of 3 orbits. During this flight period, the flight program/Astrionics System performs seven major functions: navigation, guidance, attitude control, event sequencing, data management (telemetry), ground command processing, and equipment evaluation and checkout. When all systems are checked and determined ready and the vehicle is positioned in the lunar insertion window, J-2 engine is restarted for injection into the translunar trajectory.

Orbital navigation includes computations to solve for position and for velocity based on insertion conditions. The computations are carried out by

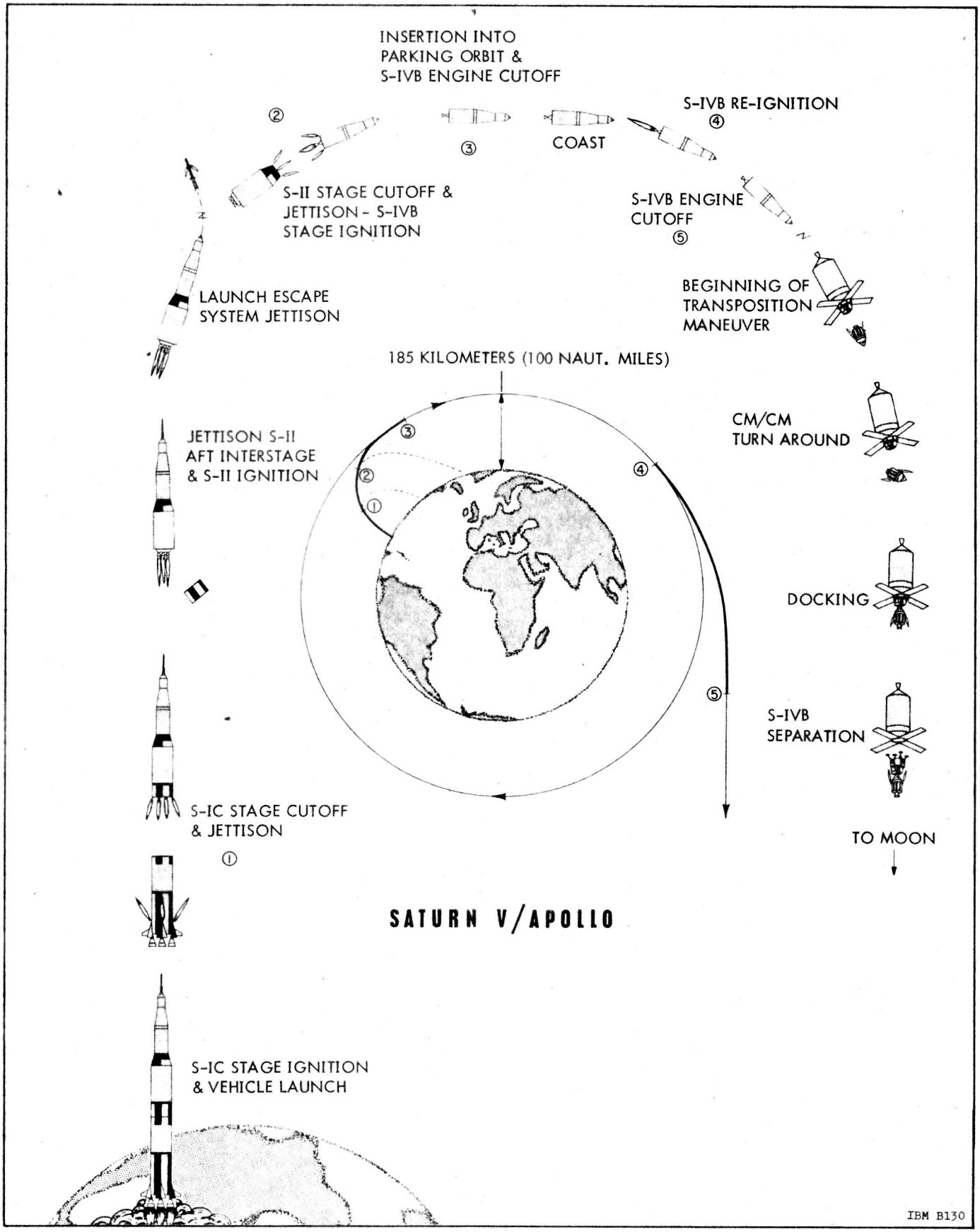


Figure 1.3-1 Saturn V Mission Profile

utilizing mathematical models of the earth and its atmosphere to approximate the effects of the physical world on the vehicle. The orbital guidance function is computed by using navigational inputs, time, and vehicle attitude. Generally, the vehicle attitude will be maintained at 90 degrees to the local vertical. Since the J-2 propulsion engine is cutoff, the auxiliary propulsion system is used for all attitude maneuvers.

Sequencing in orbital coast flight primarily involves purging the J-2 engine after cutoff and then preparing it for a later restart.

S-IVB SECOND BURN (TRANSLUNAR INJECTION)

The second-burn flight of the S-IVB Stage is used to "break away" from earth orbit and thus inject the launch vehicle/spacecraft into a translunar trajectory. During this burn period, the velocity is considerably increased (approximately 40 percent) to enable the vehicle to escape the earth's gravitational pull. Shutdown of the J-2 engine will occur when the correct velocity has been achieved.

TRANSLUNAR COAST

The final operational phase for the Saturn Launch Vehicle is the translunar coast phase. During this phase, the primary function of the vehicle is to maintain a steady attitude while transposition and docking maneuvers are performed. These maneuvers consist of:

- Spacecraft LM adapter deployment
- CSM separation from the LM/IU/S-IVB configuration and CSM turn-around
- CSM docking to the LM/IU-S-IVB configuration.

Soon after this point in time, the mission of the Saturn Launch Vehicle is considered completed, and the S-IVB/IU Stage is separated from the LM/CSM configuration.

SECTION 1.4
ASTRIONICS SYSTEMS

The overall Astrionics Systems of the Saturn IB and V Launch Vehicles are shown in simplified block diagrams in Figures 1.4-1 and 1.4-2, respectively. The major portion of the Astrionics equipment is located in the IU. During flight, the Astrionics System performs, or is involved in, the following main functions:

- Navigation, guidance, and control of the vehicle
- Measurement of vehicle parameters
- Data transmission between vehicle and ground stations (up and down)
- Tracking of the launch vehicle
- Checkout and monitoring of vehicle functions in orbit
- Detection of emergency situations
- Generation of electrical power for system operation

The operational lifetime of the S-IVB/IU Astrionics System is 4-1/2 hours for Saturn IB and 7 hours for Saturn V. The operational lifetime is limited by the capacity of the power supply (batteries) and the water and gas supply of the environmental control system which is sufficient to complete the presently defined launch vehicle missions. With increased electrical system and environmental control system capability, the operational lifetime of the Astrionics System can be extended for longer duration missions if required.

NAVIGATION, GUIDANCE, AND CONTROL

The Saturn Astrionics System provides navigation, guidance, and control of the launch vehicle from liftoff until separation of the S-IVB/IU from the spacecraft. The components involved in these functions are the ST-124M Inertial Platform Assembly, the LVDC/LVDA, the Flight Control Computer, the Control-EDS Rate Gyros, the Control Accelerometers (Saturn IB only), and finally the propulsion engine actuators and the auxiliary propulsion system. The data stored in the memory of the LVDC can be updated by data transmission from ground stations through the IU command system. The Inertial Platform Assembly carries three integrating accelerometers which measure the thrust acceleration in a space-fixed reference frame. In addition, the platform gimbal angles indicate the attitude of the vehicle in the platform reference frame. The LVDA serves as the input/output device for the LVDC and also performs necessary data processing.

The LVDC performs computations for navigation, guidance, and control functions. The position and velocity of the vehicle is obtained by combining accelerometer measurements with computed gravitational acceleration. This information is the input to the guidance computations which determine the required thrust vector orientation and engine cutoff time according to the guidance scheme stored in the memory of the LVDC.

Attitude control during powered flight is accomplished through swivelling of propulsion engines by means of hydraulic actuators to obtain the proper thrust vector orientation. The actuator commands are generated in the Flight Control Computer. The Flight Control Computer combines attitude error signals from the LVDA and angular rate signals from Rate Gyros to provide stable attitude control of the vehicle. The attitude error signal is generated in the LVDC by comparing the required thrust vector orientation (from guidance computations) with the actual vehicle attitude (obtained from platform gimbal angles).

During orbital coast periods, attitude control is achieved by the auxiliary propulsion system. This system consists of 6 nozzles arranged in 2 modules and mounted on the aft end of the S-IVB Stage. The auxiliary propulsion system is controlled by the Flight Control Computer located in the IU.

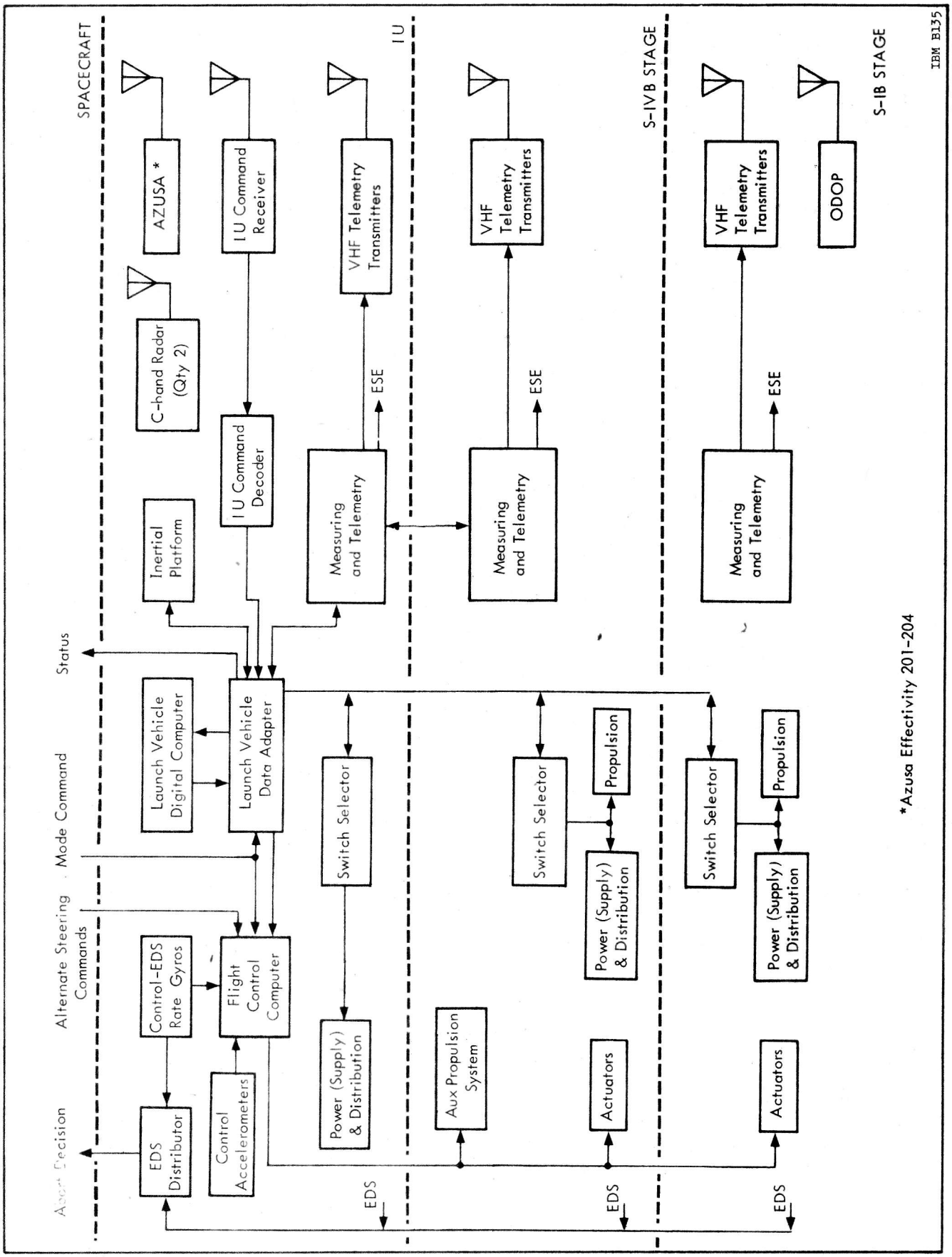


Figure 1.4-1 Saturn IB Astrionics System (Operational Vehicle)

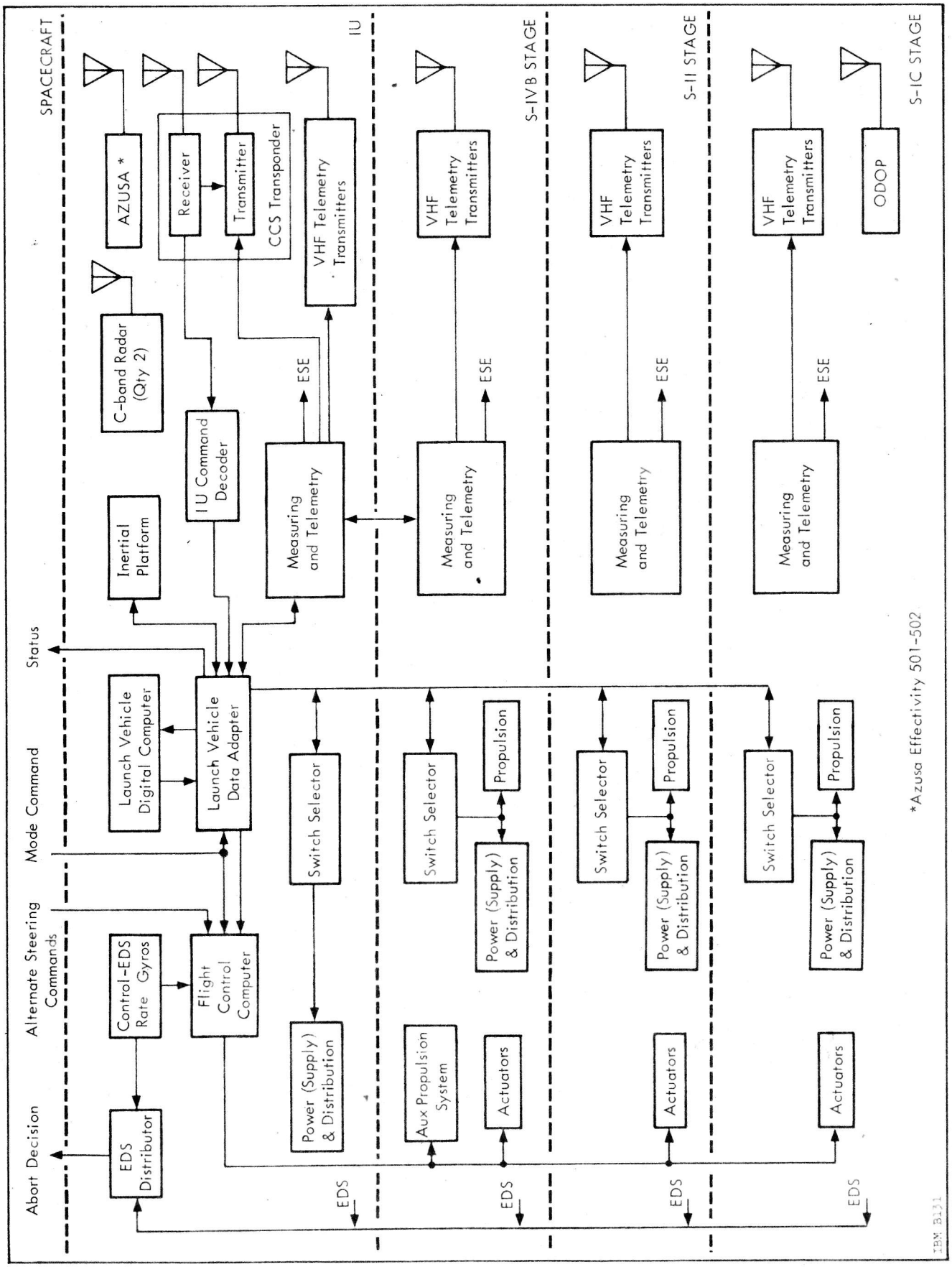


Figure 1.4-2 Saturn V Astrionics System (Operational Vehicle)

Flight sequence control (e.g., vehicle staging, engine ignition and cutoff) is performed by the LVDC. The flight program, stored in the LVDC memory, generates the necessary flight sequence commands, which are transmitted through the LVDA and Switch Selector to the proper circuit in the particular vehicle stage.

MEASUREMENTS AND DATA TRANSMISSION

Each vehicle stage is equipped with a measuring and telemetry system, including RF transmitters and antennas. For efficient utilization of available bandwidth and to obtain the required accuracy, three different modulation techniques are used in each stage telemetry system. These three techniques are FM/FM, PCM/FM, and SS/FM. (The SS/FM is employed in research and development vehicles only).

In Saturn IB vehicles, telemetry data is radiated from the vehicle to ground stations in the VHF band (225-260 MHz). The PCM/FM systems of the S-IVB Stage and the IU are interconnected to provide a redundant transmission path and to make S-IVB measurements available to the LVDA. All flight control data is transmitted through the PCM/FM system.

In Saturn V Vehicles, the PCM/FM telemetry data of the S-IVB and IU is transmitted in the VHF band (225-260 MHz) and, in some vehicles, in the UHF band (2200-2300 MHz). The UHF-band transmission is provided primarily for transmission over the longer ranges after the vehicle has left earth orbit. In addition, the PCM/FM data can be transmitted through the UHF communication and command system transponder. This arrangement provides high reliability through redundancy in transmission paths.

The telemetry system of each stage has a separate output via coaxial cable to the electrical support equipment, which is used with the digital data acquisition system for vehicle checkout before launch.

The IU command system permits data transmission from ground stations to the IU for insertion into the LVDC.

TRACKING

The Saturn Vehicles carry several tracking transponders. The ODOP Transponder is located in the first stage of Saturn IB and V Launch Vehicles. The IU is equipped with two C-band Radar Transponders, an AZUSA Transponder, and the CCS Transponder (S-band tracking).

EMERGENCY DETECTION

A vehicle emergency detection system collects special measurements from each stage of the launch vehicle. Based on these measurements, critical states of the vehicle which may require mission abort are detected, and the information is sent to the Spacecraft for display and/or initiation of an automatic abort.

SPACECRAFT INTERFACE

Several lines cross the IU/Spacecraft interface for exchange of signals. Alternate steering commands from the spacecraft navigation and guidance system may be used to control the launch vehicle during S-II and S-IVB powered flight phases. This type of operation is considered as backup in case of a failure of the IU navigation and guidance system. To indicate the state of the launch vehicle, certain measurements are sent to the Spacecraft and displayed for the crew.

Before launch, automatic checkout of the vehicle system is controlled by the launch computer complex and the electrical support equipment. This equipment also includes the digital data acquisition system.

SECTION 1.5
SYSTEM RELIABILITY CONSIDERATIONS

From the overall reliability goal of 0.85 assigned to the Saturn Launch Vehicles, a goal of 0.992 was apportioned to the Instrument Unit which contains the majority of the Astrionics System identified in Section 1.4. This goal is applied only to the components required to accomplish and support the guidance, control, and sequencing functions during the Saturn IB earth orbital mission (4.7 hours) and the flight portion of the Saturn V lunar mission (6.8 hours).

The Instrument Unit design concept requires a digital/inertial guidance scheme and an attitude error/attitude rate control scheme. A non-redundant system implementation of these design concepts would have a reliability of approximately 0.98 which is not commensurate with the 0.992 goal. In order to achieve reliability which is commensurate with the IU goal, six forms of redundancy are utilized within the IU:

- Triple modular redundancy with majority voting
- Dual redundancy
- Pair and spare redundancy
- Quad redundancy
- Backup redundancy at the functional level
- LVDC program backup redundancy

TRIPLE MODULAR REDUNDANCY

Triple Modular Redundancy (TMR) is employed extensively throughout the Launch Vehicle Digital Computer (LVDC) and Launch Vehicle Data Adapter (LVDA). The binary logic required to perform a given function is triplicated, and the outputs of the 3 channels thus formed are fed to a majority voter. The output of the voter coincides with the majority of the inputs to the voter (i.e., three logical "1's" or two "1's" and a "0" produce a "1" output; two "0's" and a "1" or three "0's" produce a "0" output). The effects of all single component part failures are negated by this scheme and significant reliability enhancement results.

DUAL REDUNDANCY

The LVDC and LVDA utilize dual redundancy in the computer memory and power supply areas. Normally, the output from one of the dual memories (memory A) is utilized. However, if an error is detected in memory A (by either parity checking or half-select current monitoring), output is switched to memory B.

The power supplies which furnish excitation for the LVDC and LVDA circuits are designed so that the predominant mode of failure is no output. Two supplies, each capable of supplying the required current, are actively "OR'ed" by diodes. Thus, failure of any one supply can be tolerated.

PAIR AND SPARE REDUNDANCY

"Pair and Spare" is the term applied to the IU control system redundancy scheme. This circuitry, which is used in the Control Signal Processor and Flight Control Computer, processes slowly varying dc voltage levels. Once again, the required circuitry is triplicated. The three channels are the "active" or "command" channel, the "standby" or "spare" channel, and the "reference" channel. Output is normally from the active channel. A differential amplifier is used to compare the active channel output with the reference channel output. If a difference in level occurs, output is switched to the standby channel. All single failures are detected and negated by this scheme.

A form of "pair and spare" redundancy is also utilized in the LVDA ladder output circuitry. As in the control system, an active channel is compared with a reference channel. A disagreement initiates a switchover which allows a standby channel to provide the output to the Flight Control Computer. Some of the hardware in the LVDA ladder circuitry is utilized for all three vehicle axes by a time sharing arrangement.

QUAD REDUNDANCY

Quad redundancy is employed in the Mod II Switch Selector. Individual transistors are replaced

by 4 transistors in a series-parallel configuration. Similarly, single diodes and resistors are replaced by groups of four.

BACKUP REDUNDANCY

The Emergency Detection System (EDS) constitutes backup redundancy at the functional level. The EDS cannot negate the mission effects of the failures which it detects. It does, however, provide for the crew's safe departure from a defunct vehicle. Thus, while the probability of the IU accomplishing the translunar injection is in the order of .99, the probability of not injuring the crew (in the case of a launch vehicle failure) is increased to 0.9999 by utilization of the EDS.

PROGRAM BACKUP REDUNDANCY

The logical decision-making capability of the LVDA/LVDC is used to achieve backup redundancy for various components.

The LVDC flight program compares the digital word present in the Switch Selector register with the word issued by the LVDA. If a disagreement is detected, the LVDA issues the binary complement of the original digital word to the Switch Selector. This complement word causes the Switch Selector to issue the same output that the original word would have generated. The effects of single failures in the Switch Selector register are negated by this scheme.

The LVDC flight program performs a reasonableness test on the inputs from the gimbal resolvers of the ST-124M Inertial Platform Assembly. An unreasonable input will cause switchover from the fine mode of resolver operation to the coarse mode (which is sufficient to allow mission success). If both fine and coarse resolver inputs are unreasonable, the LVDC/LVDA will cause the Launch Guidance Failure indication in the spacecraft to be affirmative. This failure indication is an EDS manual abort parameter. As opposed to mission success redundancy, this function of the LVDC flight program constitutes an EDS type of redundancy.

The flight program evaluates the Platform system inertial velocity outputs in a manner similar to that described for the gimbal resolvers. For each inertial axis, the velocity encoding and processing hardware has dual redundancy. Reasonableness tests are performed on the output of the initially selected channel. If an unreasonableness is detected, the program switches to the redundant channel. If the redundant channel is reasonable, its output will be utilized in the normal fashion. An unreasonable decision on the redundant channel will cause the LVDC flight program to use a modified navigation scheme and initiate the Launch Guidance Failure indication previously described. This arrangement provides mission redundancy for failures of the optisyns, Accelerometer Signal Conditioner, and associated LVDA hardware. EDS-type redundancy is provided for double failures of this hardware and single failures within the Inertial Platform accelerometers and associated servo loops.

CHAPTER 2
NAVIGATION AND GUIDANCE

SECTION 2.1
THE NAVIGATION, GUIDANCE, AND CONTROL SYSTEM

The problem of directing a space vehicle, to accomplish a given mission, is customarily discussed in terms of three separate functions: navigation, guidance, and control. The boundaries between these 3 areas are to some extent arbitrary and conventional. The 3 terms, navigation, guidance, and control, will be used in this text according to the following definitions:

- Navigation is the determination of position and velocity of the vehicle from measurements made onboard the vehicle.
- Guidance is the computation of maneuvers necessary to achieve the desired end conditions of a trajectory (e.g., an insertion into orbit).
- Control is the execution of maneuvers (determined from the guidance scheme).

A block diagram of the overall Saturn V navigation, guidance, and control system is shown in Figure 2.1-1. (This figure also applies for the Saturn IB Vehicle if the S-II Stage Switch Selector and engine actuator blocks are omitted.) The 3-gimbal, stabilized Inertial Platform Assembly (ST-124-M) provides a space-fixed coordinate reference system for navigation measurements (vehicle acceleration and velocity). Three integrating type accelerometers, mounted on the stabilized inner gimbal of the platform, measure the 3 components of vehicle velocity ($\dot{X}_I$, $\dot{Y}_I$, $\dot{Z}_I$) resulting from vehicle propulsion. The measurements are sent through the LVDA to the LVDC where they are used in calculating the vehicle's velocity and position in space in relation to the earth.

According to the guidance scheme (programmed into the computer), the maneuver required to achieve the desired end conditions is determined by the LVDC. The instantaneous position and velocity of the vehicle are used as inputs. The result is the required thrust direction (guidance command) and the time of engine cutoff.

Guidance information stored in the LVDC (e.g., position, velocity) can be updated through the IU command system by data transmission from ground stations. (The IU command system provides the general capability for inserting new information into the LVDC.)

The Flight Control Computer is the controlling element of the control system. It accepts basic signals from 2 sources:

- Vehicle attitude error signals (ψ) from the LVDC/LVDA.
- Vehicle attitude rate-of-change signals ($\dot{\phi}$) from the Control-EDS Rate Gyro Package.

The attitude correction commands are computed according to the guidance scheme in the LVDC. They are then issued through the LVDA to the Flight Control Computer. The Flight Control Computer then commands the engine actuators to move their respective engines to the desired angle. This gimballing action changes the direction of the thrust vector of the vehicle, thus moving the vehicle about its roll, pitch, or yaw axis. The Control-EDS Rate Gyro Package senses the angular rate of change of these attitude changes and movements of the vehicle. The signals thus generated are supplied as dynamic feedback to the Flight Control Computer. The Flight Control Computer sums the angular rate information from the rate gyros with the attitude error signals from the LVDC/LVDA to produce engine commands which conform to the prescribed vehicle limits.

Commands for flight sequence control are generated in the LVDC according to a stored program. These commands are transferred through the LVDA to the Switch Selector of the corresponding vehicle stage. Examples of flight sequence control are engine ignition, cutoff, and stage separation. The Switch Selector in the addressed stage activates the necessary circuitry to perform the commanded function.

Attitude and sequence control of the launch vehicle is described in Chapters 3 and 4, respectively. The Inertial Platform, LVDA and LVDC, which are involved in navigation, guidance, and control operations, are described in Chapters 14 and 15.

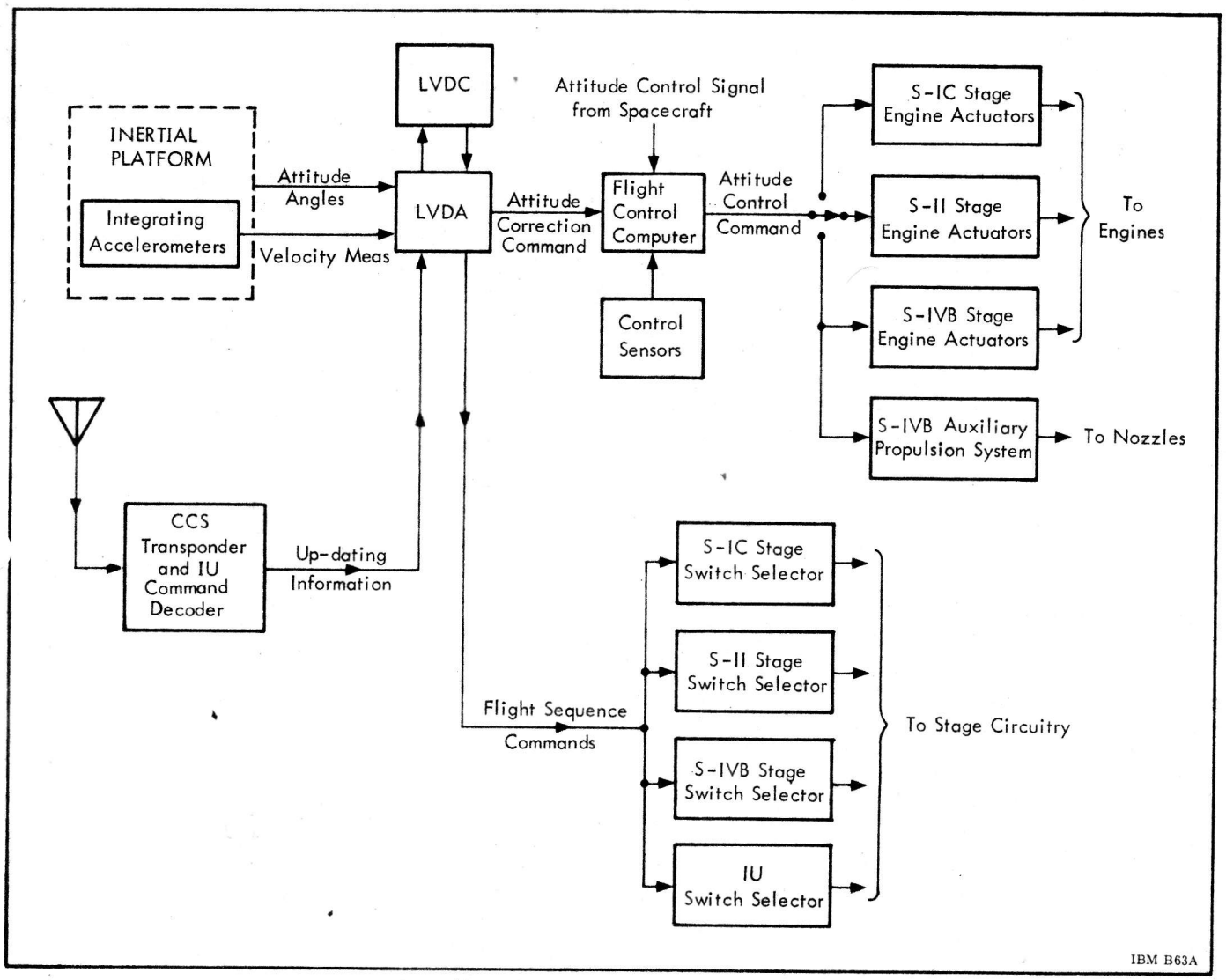


Figure 2.1-1 Block Diagram of Saturn V Navigation, Guidance, and Control System

SECTION 2.2
NAVIGATION

2.2.1 GENERAL DESCRIPTION

During powered flight, the Saturn IB/V Navigation System determines vehicle position, velocity, and acceleration from measurements made onboard the vehicle. The initial measurements are supplied by integrating accelerometers which are mounted on an inertial platform within the ST-124-M Inertial Platform Assembly*.

Three different coordinate reference systems (three-dimensional) are associated with the Saturn IB/V Navigation System. Using these coordinate systems and measurements from the Platform (velocity and attitude angle), the LVDC is programmed to compute the instantaneous vehicle velocity and position. These values are presented to the guidance system in terms of X Y Z coordinates.**

During orbital flight, vehicle position, velocity, and acceleration are computed from equations of motion which are based on the flight conditions at the time of orbital insertion. During this phase of the flight, data for navigation and guidance calculations can be updated from the ground stations via the IU command system.

2.2.2 NAVIGATION COORDINATE REFERENCE SYSTEMS

References for vehicle origin, position, and destination must be defined before a navigation scheme can function. The three primary coordinate systems used for Saturn navigation are:

- The gravitational coordinate system (X_G Y_G Z_G)
- The plumbline coordinate system (X_S Y_S Z_S)
- The body coordinate system (X_B Y_B Z_B)

The references for these coordinate systems are either earth fixed or space fixed. An earth-fixed reference vector will exist in a line from the earth's center through a point on the earth's surface (e.g., launch site). As the earth rotates, the vector will remain oriented between these 2 points and is therefore earth fixed. A space-fixed reference vector will be aimed at a point in space and is completely independent of the earth's revolution. After a quarter revolution of the earth, the earth-fixed vector will have rotated 90 degrees while the space-fixed vector will have remained pointed in its oritinal direction. The origin of both reference vectors remains fixed at the center of the earth.

GRAVITATIONAL COORDINATE SYSTEM

The gravitational (X_G, Y_G, Z_G) coordinate system is a nonrotating, rectangular coordinate system whose origin is fired at the center of the earth. See Figure 2.2-1. It is used in computing the effect that gravity has upon the Platform-mounted accelerometers. The Y_G axis is aligned with the earth's spin axis and points south. The X_G axis is in the equatorial plane and intersects the equator at the longitude of the launch site at launch time. The Z_G axis which is perpendicular to the Y_G and X_G axes completes the right-handed orthogonal system.

PLUMBLINE COORDINATE SYSTEM

The plumbline (X_S Y_S Z_S) coordinate system is used for navigation and guidance computations. Its origin is also at the center of the earth. See Figure 2.2-1. The system is earth fixed until Guidance Reference Release (GRR), a few seconds before liftoff. At that time, the X_S axis is established, and the system becomes permanently space fixed.

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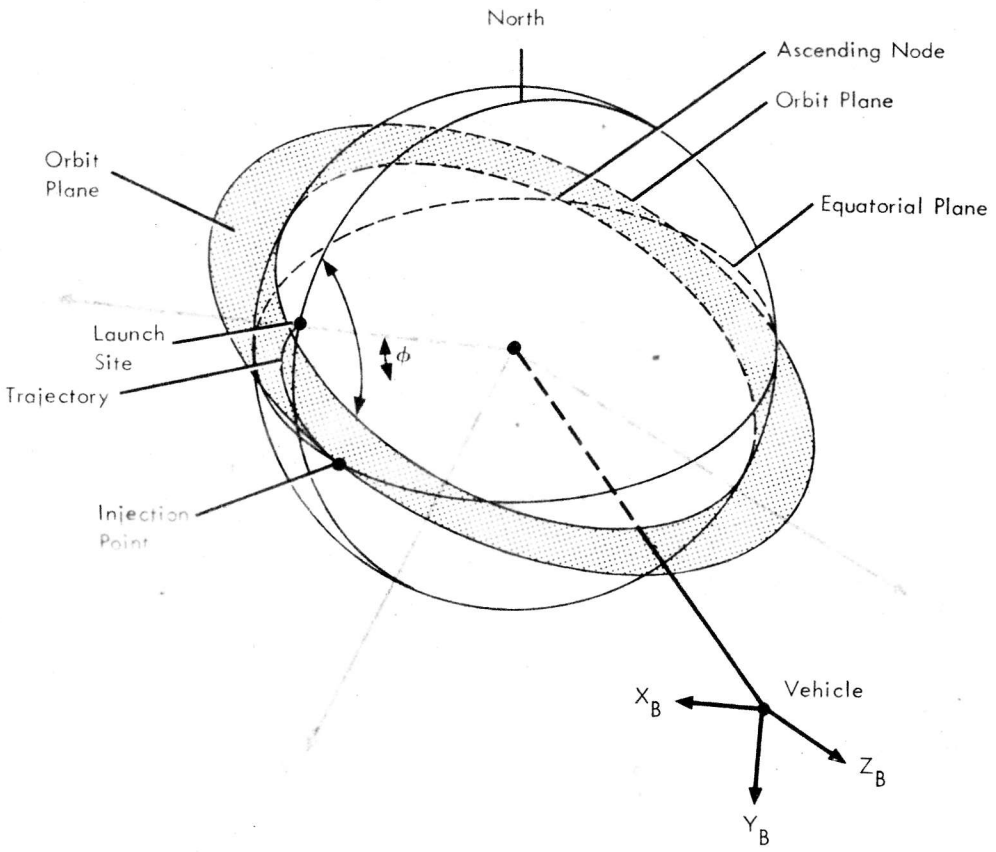
* For the Purpose of brevity, the ST-124-M Inertial Platform Assembly will hereafter be referred to as the Platform.

** The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.



Gravitational Coordinate System — A non-rotating, rectangular coordinate system. The Y_G axis is collinear with the earth's spin axis and points south. The X_G axis is perpendicular to the Y_G axis and oriented so that the $X_G Y_G$ plane contains the launch site at launch time. The Z_G axis completes a right-hand orthogonal system.

Navigational Coordinate System — A non-rotating, rectangular coordinate system. The X_S axis is collinear with the gravity vector at the launch site. The Z_S axis is parallel to the earth-fixed firing azimuth and is positive downrange. The Y_S axis completes a right-hand orthogonal system.

$X_B Y_B Z_B$ Body Coordinate System — A coordinate system which is parallel to the $X_S Y_S Z_S$ system and with its origin at the vehicle's Platform — sometimes written as $X_M Y_M Z_M$.

ϕ Geodetic latitude of the launch site.

Az Launch azimuth, measured in clockwise direction from north.

r Radius vector from the earth's center to the vehicle.

Figure 2.2-1 Navigation Coordinate Systems

BODY COORDINATE SYSTEM

The body (X_B Y_B Z_B) coordinate system is used for velocity measurements. Unlike the first two systems, the X_B Y_B Z_B system has its point of origin at the Platform (see Figure 2.2-1). The X_B Y_B Z_B coordinates are parallel with the X_S Y_S Z_S coordinates. Thus, any increment of velocity measured at the Platform is an indication of motion along the X_S Y_S Z_S axes. Before launch, both the plumbline and body coordinate systems are earth fixed, but at GRR, both systems become space fixed. The body coordinate system is sometimes referred to as the X_M Y_M Z_M system.

2.2.3 NAVIGATION CALCULATIONS

BOOST NAVIGATION

The velocity values, measured by the Platform integrating accelerometers, are processed within the LVDA and forwarded to the LVDC as increments of velocity. Velocity is integrated and used to determine position. The basic navigation scheme is shown in Figure 2.2-2.

Additional forces, such as gravity and initial velocity, must be considered, and the effect induced by these forces must be compensated for within the navigational computations. The gravitational acceleration, which is acting upon the accelerometers, is computed from the stored gravitational model of the earth. This gravitational acceleration varies in relation to position and distance from the earth. A nominal value is 9.8 meters/second/second (9.8 M/S^2) at the earth's surface and will decrease as vehicle altitude increases.

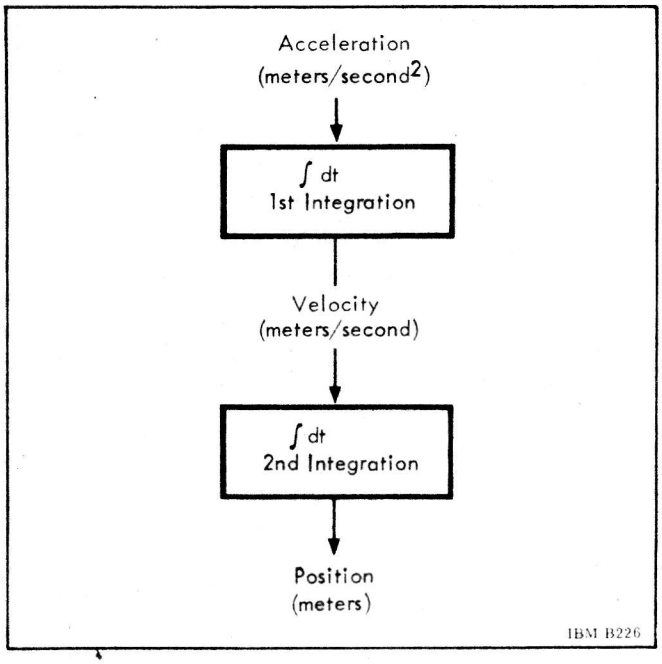


Figure 2.2-2 Basic Navigation Scheme

The quantities and equations required for boost navigational computations are listed in Table 2.2-1. A definition of the terms used in these and other navigation equations may be found in the List of Abbreviations, Signs, and Symbols at the rear of this handbook.

Figure 2.2-3 is a detailed flow diagram of the navigation scheme. Starting at the upper left of the figure, velocity measurements (integrated from the Platform's acceleration values) are obtained from the Platform via the LVDA. Within the LVDC, initial velocity (imparted by the spinning earth), gravitational velocity (caused by the effects of gravity), and the Platform velocity are algebraically summed. Their sum is inertial vehicle velocity in the space-fixed X_S Y_S Z_S coordinate system. This velocity is integrated and added to the initial position (distance from earth's center to the launch site) to determine vehicle position. The value of position is used in guidance computations and to compute the gravitational velocity which is "looped back" to the velocity readings. Values of Platform velocities are differentiated to obtain components of acceleration.

ORBITAL NAVIGATION

During orbital coast flight, the navigational program periodically computes the vehicle position, velocity, and acceleration from equations of motion which are based on vehicle conditions at the time of orbital insertion. In orbit, navigation and guidance information in the LVDC can be updated by digital data transmission through the IU command system

Orbital navigation includes the computations necessary to determine position, velocity, and total acceleration of the S-IVB and IU relative to the navigational coordinate system during earth orbit. These computations are carried out in an indirect fashion, making use of mathematical models of the earth, its atmosphere, and the vehicle to approximate the effects of the physical world on the vehicle. See Table 2.2-1.

Additional navigational computations are used in maintaining vehicle attitude during orbital coast flight. These computations establish a local vertical which is used as a reference for attitude control. Normally, the attitude of the vehicle roll axis will be maintained at 90 degrees with respect to this local vertical.

Table 2.2-1 Navigation Computations

Boost Navigation

The boost navigation routine combines calculated gravitational accelerations with measured Platform velocities to compute position and total velocity in an earth centered inertial coordinate frame.

The gravitational acceleration components, $\ddot{X}_g$, $\ddot{Y}_g$, and $\ddot{Z}_g$ are computed during boost as:

$$\ddot{X}_g = X_S\ S - P \sin \phi$$
$$\ddot{Y}_g = Y_S\ S + P \cos \phi \sin Az$$
$$\ddot{Z}_g = Z_S\ S - P \cos \phi \cos Az,$$

where S and P are computed from equations which characterize the gravitational model and include values of GM (universal gravitational constant), a_e (equatorial radius of the earth), ϕ (geodetic launch site latitude), Az (firing azimuth), and established constants*. These accelerations are then used to compute a change in position and velocity due only to the gravitational force. The gravitational position change is combined with the updated change in position due to thrust force to arrive at a new inertial position. The velocity change is added to the accumulated platform measurements to arrive at the current inertial velocity. The state quantities thus calculated provide the necessary navigational input to the guidance routines.

The computations in the LVDC are performed in the following order:

(1) Change in position from gravitation

$$\Delta X_g = | I_{gX\ PAST} + \ddot{X}_{g PAST}\ \Delta t/2 |\ \Delta t$$

(2) Change in position from acceleration

$$\Delta X_T = [\ \dot{X}_M + \dot{X}_{M\ PAST}\ |\ \Delta t/2$$

(3) New space-fixed position

$$X_S = X_{S\ PAST} + \Delta X_g + \Delta X_T + \dot{X}_o\ \Delta t$$

(4) Gravitation computations

$$\ddot{X}_g = g\ (X_S,\ Y_S,\ Z_S)$$

(5) Gravitational velocity

$$I_{gX} = I_{gX\ PAST} + \Delta t/2\ (\ddot{X}_g + \ddot{X}_{g\ PAST})$$

(6) Space-fixed velocity

$$\dot{X}_S = \dot{X}_M + I_{gX} + \dot{X}_o$$

(X_M represents measured values of velocity from the Platform.)

Corresponding notation also holds for the Y and Z directions.

The computational method described is adequate for all periods of flight other than cutoff. Because the navigational computations are performed only at intervals greater than 1 second, position and velocity must be extrapolated to provide proper values at S-IVB cutoff. A special routine is included in the terminal calculations to provide the necessary extrapolations, thus ensuring correct navigational quantities from which to initiate orbital navigation.

* The gravitational model used in current studies evaluates only the round earth and first oblateness terms during boost.

Table 2.2-1 Navigation Computations (Cont.)

Orbital Navigation

Orbital navigation includes the computations necessary to determine position, velocity, and total acceleration of the S-IVB and IU relative to the navigation coordinate system during orbital coast. These computations are carried out in an indirect fashion, making use of mathematical models of the earth, its atmosphere, and the vehicle to approximate the effects of the physical world on the vehicle. Certain simplifying assumptions were made with regard to the drag model and the rotation of the earth's atmosphere*. The equations characterizing the mathematical model are:

$$\ddot{X} = \ddot{X}_G + \ddot{X}_D + \ddot{X}_V$$

$$\ddot{Y} = \ddot{Y}_G + \ddot{Y}_D + \ddot{Y}_V$$

$$\ddot{Z} = \ddot{Z}_G + \ddot{Z}_D + \ddot{Y}_V$$

where for the first equation, $\ddot{X}$ is the total acceleration in the space-fixed X direction caused by gravitation ($\ddot{X}_G$), atmosphere drag ($\ddot{X}_D$), and venting accelerations ($\ddot{X}_V$). Corresponding notation also holds for the Y and Z directions. The system is then numerically integrated to yield position and velocity of the vehicle at any time.

* The gravitational model evaluates the round earth and the first three oblateness terms of the expansion.

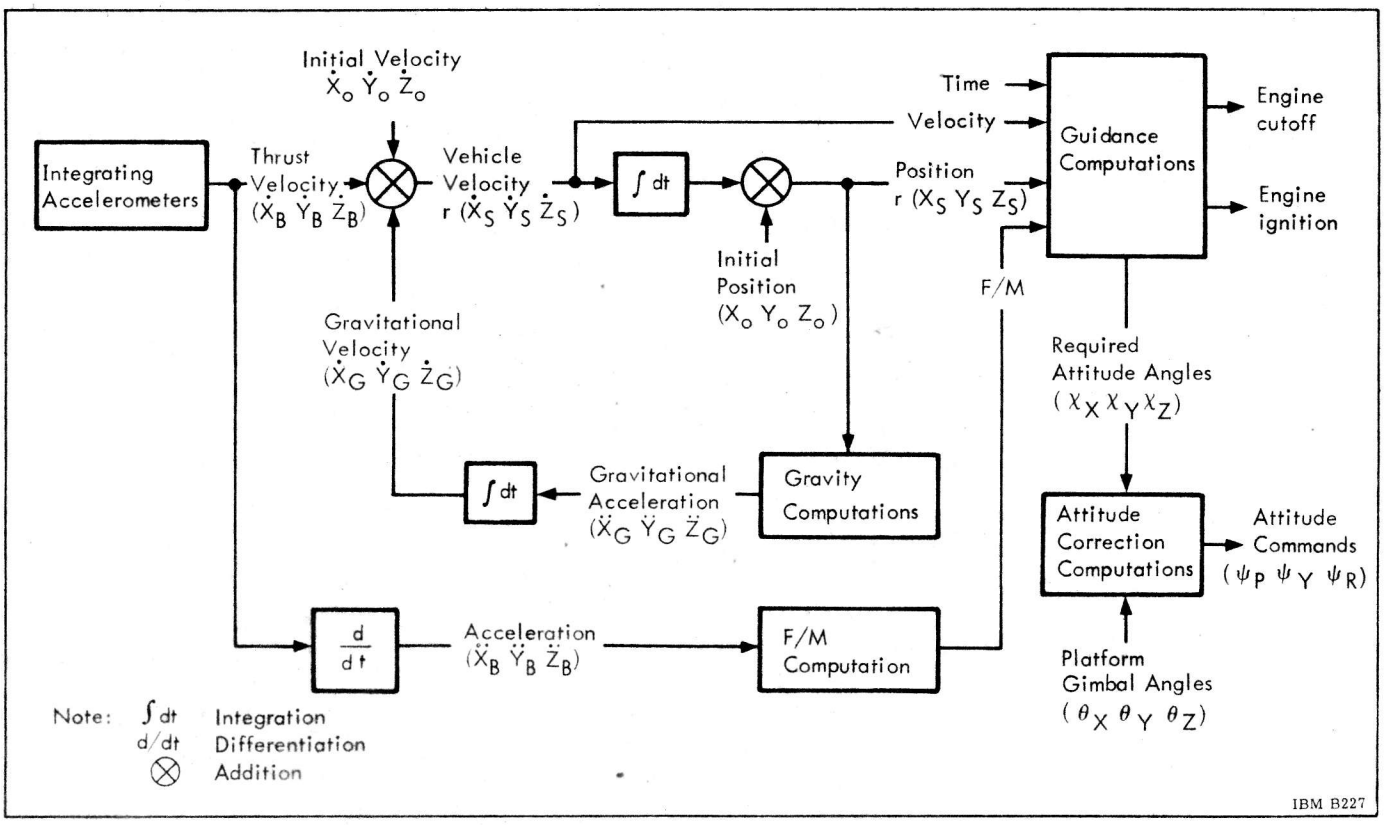


Figure 2.2-3 Navigation and Guidance Flow Diagram

SECTION 2.3
GUIDANCE

2.3.1 GENERAL CONSIDERATIONS

The guidance function of the launch vehicle is accomplished by computing the necessary flight maneuvers to meet the desired end conditions of the flight (e. g. , inserting the payload into earth orbit). Guidance computations are performed within the LVDC by programmed guidance equations which use navigation data and mission requirements as their inputs. Simply, the guidance program compares the launch vehicle's present position and heading with the predetermined "target in space", and the computed differences are issued to the attitude control equipment as maneuvering commands. The control system then alters the vehicle's thrust direction until the vehicle is on its newly computed heading.

Figure 2. 3-1 is a simplified flow diagram of the guidance computations within the LVDC. These computations are actually a logical progression of computed formulas which have a guidance command as their solution. After the desired attitude has been determined by the "best path" program, the guidance computations might be reduced into the following equation:

$$\psi = \chi - \theta$$

where: ψ is the attitude error command* (all measured in the $X_S\ Y_S\ Z_S$ system**)

χ is the desired attitude

θ is the vehicle attitude

Calculating these attitude error commands completes the guidance scheme.

Input data to the guidance computations are the state variables of the vehicle position, velocity, and acceleration (i. e. , the navigation measurements). The result of the guidance computations is the required thrust direction (guidance command) and the time of engine cutoff and re-ignition for the S-IVB Stage. The thrust direction is expressed as three Euler angles $\chi_X\ \chi_Y\ \chi_Z$ defining the thrust vector orientation in the space-fixed coordinate system $X_S\ Y_S\ Z_S$. One final computation, however, involves transforming the attitude commands into the vehicle reference frame from the Platform coordinate references ($\psi_X\ \psi_Y\ \psi_Z$ to $\psi_R\ \psi_P\ \psi_Y$). These values are then utilized by the control system to form the engine thrust angle commands.

PATH ADAPTIVE GUIDANCE

Overall system performance requires that the guidance scheme minimize propellant consumption for flight maneuvers and avoid excessive structural loads caused by such maneuvers. The guidance system must correct numerous flight perturbations, such as atmospheric perturbations from wind, unsymmetrical air flow because of vehicle dissymmetry, flight path deviations caused by nonstandard vehicle and engine characteristics and performance (this might even include engine-out cases), control inaccuracies, and emergency situations.

In addition, the required end conditions of the powered flight phase, at insertion into earth orbit and at injection into translunar trajectory, must be met with a high degree of accuracy to avoid additional propellant consuming maneuvers.

To meet this requirement, path adaptive guidance has been developed for Saturn Vehicles. The path adaptive guidance scheme does not constrain the vehicle to a standard trajectory, as with many ballistic missiles. Based on the instantaneous state of the vehicle, the path adaptive guidance scheme computes a new minimum propellant flight path to achieve the mission-determined end conditions. Thus, perturbations occurring during flight will be corrected in an optimum way.

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* Sometimes referred to as $\Delta\phi$ in other documentation.

** The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1. 2.

Several path adaptive guidance schemes have been developed for Saturn Vehicles. The polynomial guidance scheme and the iterative guidance mode have been successfully used in Saturn I flights. The iterative guidance mode will be used with Saturn IB and V and is described in Paragraph 2. 3. 2.

During first-stage flight (S-IB or S-IC Stage propulsion), the vehicle transverses the dense portion of the atmosphere where high aerodynamic pressure occurs. To avoid excessive structural loads caused by guidance maneuvers, no guidance constraints are applied during this flight phase. Open loop guidance, in the form of a time-tilt program, is used. Path adaptive guidance begins with the ignition of the second stage (S-II Stage for Saturn V and S-IVB Stage for Saturn IB).

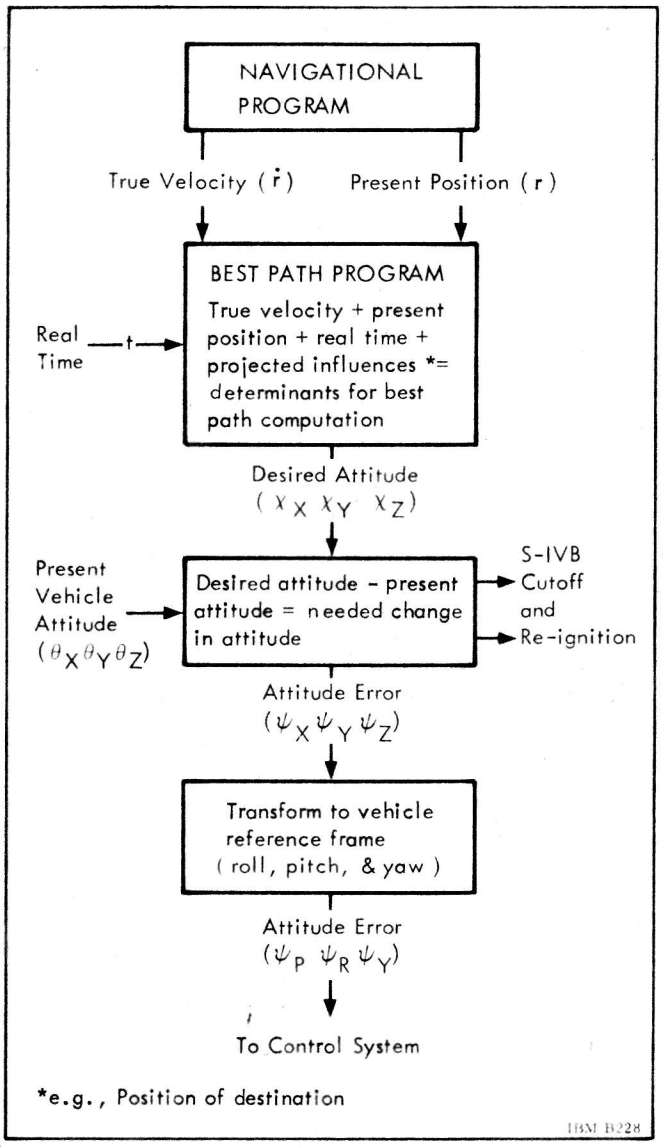


Figure 2. 3-1 LVDC Guidance Functions

TRAJECTORY CONSTRAINTS AND LAUNCH WINDOW

A large number of constraints apply to the trajectory of a launch vehicle. These constraints result from mission rules; environmental conditions such as the atmosphere and location of launch point; operational requirements such as safety restrictions of launch azimuth and tracking requirements; and hardware limitations such as structural load limits and available propulsion means. The dominating and most severe requirement applying to the choice of trajectories is optimal propellant utilization.

A combination of the various constraints generates a limited time period for launch; i. e., a launch window to meet mission requirements. There are 2 types of launch windows for the launch vehicle in the Saturn V/Apollo mission: the ground launch window for ascent into parking orbit and the orbital launch window for translunar injection.

The launch azimuth at the ground and the orientation (inclination and descending node) of the parking orbit are varying with time. A brief explanation of the reasons for time varient launch azimuth, inclination, and descending node seems advisable at this point. At any instant of time a plane can be defined which contains the launch site, the center of the earth, and the moon at the desired time of arrival. In order to maintain this plane, it is necessary to vary the launch azimuth on the ground continuously, since the launch site is moving with the rotating earth and the moon is moving. When range safety constraints are introduced, the launch azimuth will be limited to a certain band of values. For launches from Cape Kennedy, the band is approximately 72 to 108 degrees measured east of north and will be encountered twice each day. Within this band, a 26-degree range of azimuths will guarantee at least a 2-1/2 hour launch window. Normally, this variation will be applied to the portion of the band where launch azimuth varies linearly with the time of launch. Of the two daily launch periods, one will generally lead to a shorter coasting arc in orbit than the other. Since the geographic position of the launch site is fixed, it follows that one of the launch periods leads to time of coast in parking orbit such that ignition in orbit occurs within a range close to the launch site - sometimes referred to as the "Atlantic opportunity". The second launch period calls for coasting arcs of greater length - commonly referred to as "Pacific opportunities".

Since launch vehicle payload capability is degraded by powered plane changes, it is assumed

that in the nominal case there will be no such maneuvers. If it is desired to go into an orbit with an inclination to the earth's equator (greater than the latitude of the launch site), then it is possible to launch directly into the properly selected launch azimuth. There are other constraints which might be present which affect the launch window problem; e.g., launch during daylight, proper lighting of the launch site, and lighting of the return landing sites. These, however, do not affect the basic geometrical considerations.

2.3.2 ITERATIVE GUIDANCE MODE

The Iterative Guidance Mode (IGM) was developed to meet the mission flexibility requirement of large space vehicles with minimum propellant consumption. The scheme is based on optimizing techniques using calculus of variations to determine a minimum propellant flight path which satisfies the mission requirements. Experience with hundreds of minimum propellant trajectories for various orbital insertion missions has demonstrated that the optimum thrust direction, relative to the local vertical, is very nearly a linear function of time during vacuum flight. Moreover, the size of the angle between the optimum thrust direction and the local horizon is never very large. These observations show a remarkable agreement with the mathematical results obtained from the calculus of variations when a flat earth model having a constant gravitational field is used, and position and velocity constraints are imposed at cutoff. A closed solution can be obtained with this mathematical model and it yields an explicit equation for the optimum thrust direction. This equation has the form:

$$\chi_P = \arctan (A + Bt) \qquad (2.3\text{-}1)$$

where χ_P is the optimum thrust direction for minimum propellant consumption and t is the time. Constants A and B are determined by the specified cutoff velocity and position, the initial values of the state variables, the vehicle thrust acceleration, and the engine specific impulse. The comparison of this equation with the results of trajectory studies suggests the use of the first order expansion of (2.3-1) as an approximation:

$$\chi_P = A + Bt \qquad (2.3\text{-}2)$$

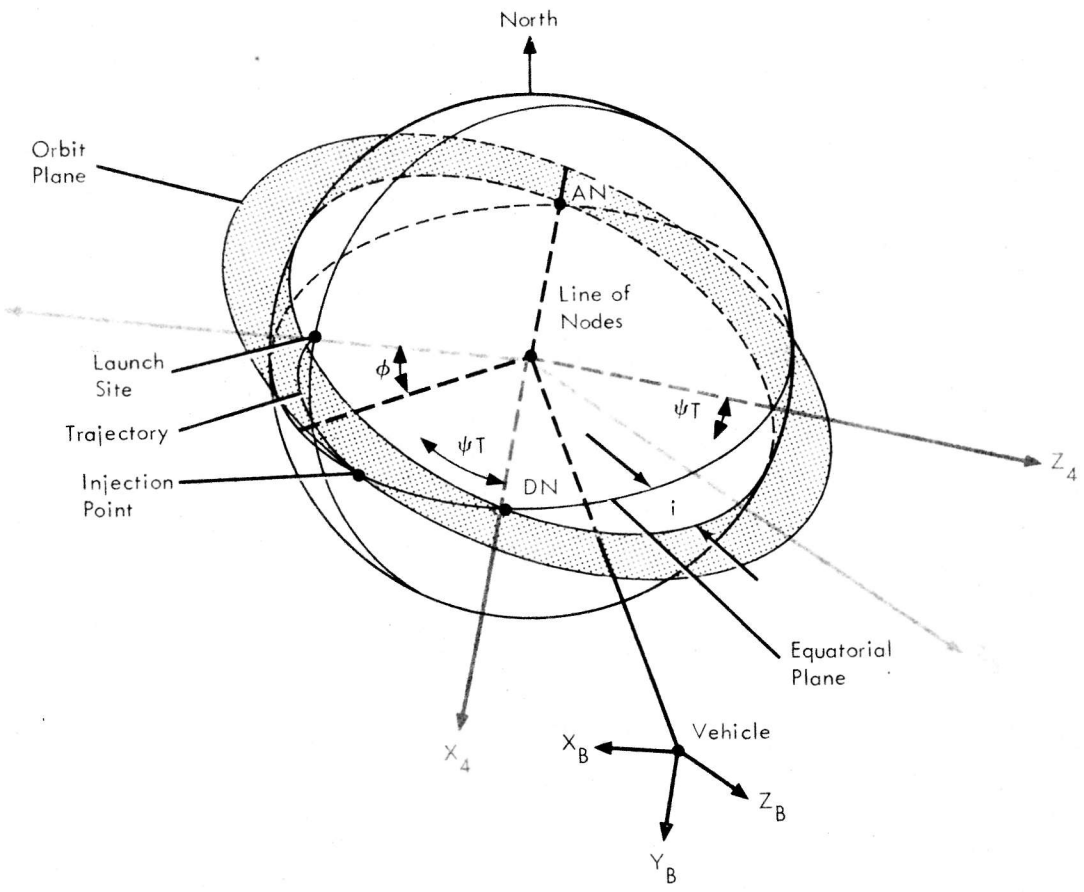
A rectangular injection coordinate system (X_V Y_V Z_V) (Figure 2.3-2) is established with the origin at the center of the earth and with the X_V axis lying along the vertical which intersects the calculated cutoff position. Simplified equations of motions are derived to approximate the motion over an oblate earth with a realistic gravitational field. These equations of motion are solved during flight to determine the instantaneous range angle to cutoff, the time-to-go to cutoff, and the gravitational effects occurring over the remaining flight time. This information is used to compute values for A and B continuously during flight. In practice, only the value of A need be calculated when computation rates on the order of one or more per second are used (except during the last few seconds before cutoff when both A and B are computed and held constant over the remaining flight time). This is necessary because the equation gives an indeterminate command angle at the cutoff point.

The iterative guidance scheme will be activated early in the S-II Stage burn period and will continue in operation until insertion into parking orbit. Subsequently, IGM will operate until lunar transit injection with the second burn of the S-IVB Stage. The guidance scheme generates commands for the pitch-yaw angle of the thrust direction and the cutoff velocity.

The inclination of the parking orbit cutoff plane, the descending node, and the launch azimuth are functions of time of launch. During the last few minutes prior to liftoff, these quantities will be computed in the launch ground computer and the results will be put into the LVDA. At the same time, the Platform will be aligned to the direction of the desired launch azimuth. Figure 2.3-3 shows how the quantities, dependent on time of launch, vary for a typical launch day. Very simple representations of these curves, as a function of time of launch, can be obtained.

Examination of the loop shown in Figure 2.3-4 between vehicle tracking and telemetry of the LVDC and Platform, along with transmission of data in real time to the MCC, the various possibilities of updating information to the computer, of overriding commands such as the ignition equation, and of performing an alternate mission can be seen. In the case of abort (e.g., failure somewhere in the S-II to the nominal mission), no change in input is required. The solution of time-to-go and other parameters in the iterative scheme settle out quite rapidly (after 2 or 3 cycles). This statement also holds for changes in desired terminal conditions which might be built into the computer. Neither the accuracy nor the near optimality of the scheme is degraded.

In summary, the effort has been directed toward generality of guidance equations with a minimum amount of input – both for the nominal mission and for abort and alternate missions. Since a minimum amount of "tampering" with the main program



Note: Y coordinates have been omitted for clarity

	Navigation coordinate system
$X_B Y_B Z_B$	Platform coordinate system — sometimes written as $X_M Y_M Z_M$
$X_4 Y_4 Z_4$	Target plane coordinate system
	Injection coordinate system

ϕ	Launch site latitude
ψ_T	Total range angle
i	Inclination of orbit
DN	Descending Node
AN	Ascending Node

Figure 2.3-2 Guidance Coordinate Systems

in the LVDC is necessary, efficiency is at a high level, and checkout is greatly simplified. A great deal of consideration was given to the question: Is it better to have one set of guidance equations with the extraneous computation of the quantities which are nulled for a special case, or to have separate equations for the ascent-into-orbit and the flight-out-of-orbit? Close coordination with personnel who would actually be involved with the flight program on the LVDC resolved the answer: Extraneous computation, with the minimum amount of change to the flight program, is more desirable. The time required for programming a computer from one flight to the next is reduced by this method. In fact, theoretically it is possible to program the computer, change the vehicle configuration, change the mission, and never perform another checkout of the LVDC. Practically, of course, a high-confidence level is necessary for crew safety and for accomplishing the desired mission – so checkouts are performed again but of a much more limited nature than if a completely new computer program were required.

The iterative guidance equations require more LVDC capacity than most of the other guidance schemes optimized for minimum propellant consumption, but considerable flexibility is gained. The same set of guidance command equations is applicable to almost all orbital missions and can be formulated for use with any number of high thrust stages. The small number of presettings that must be calculated for a flight represents physical quantities such as vehicle exhaust velocity, nominal cutoff time, and desired cutoff position and velocity. This is an important characteristic of the scheme since these presettings may be determined without resorting to time-consuming statistical methods. The accuracy and propellant economy with the scheme are excellent. The fuel required to attain the desired cutoff conditions (at orbit insertion) is within 5 kilograms (11.1 pounds) of that required using exact minimum propellant equations obtained with the calculus of variations. This economy is obtained even under severe perturbations such as an engine failure in the first stage of a two-stage, multi-engine vehicle.

2.3.3 GUIDANCE FUNCTIONS IN FLIGHT

The following is a brief summarizing description of guidance functions during the various phases of the Saturn Launch Vehicle Mission in the Apollo Program.

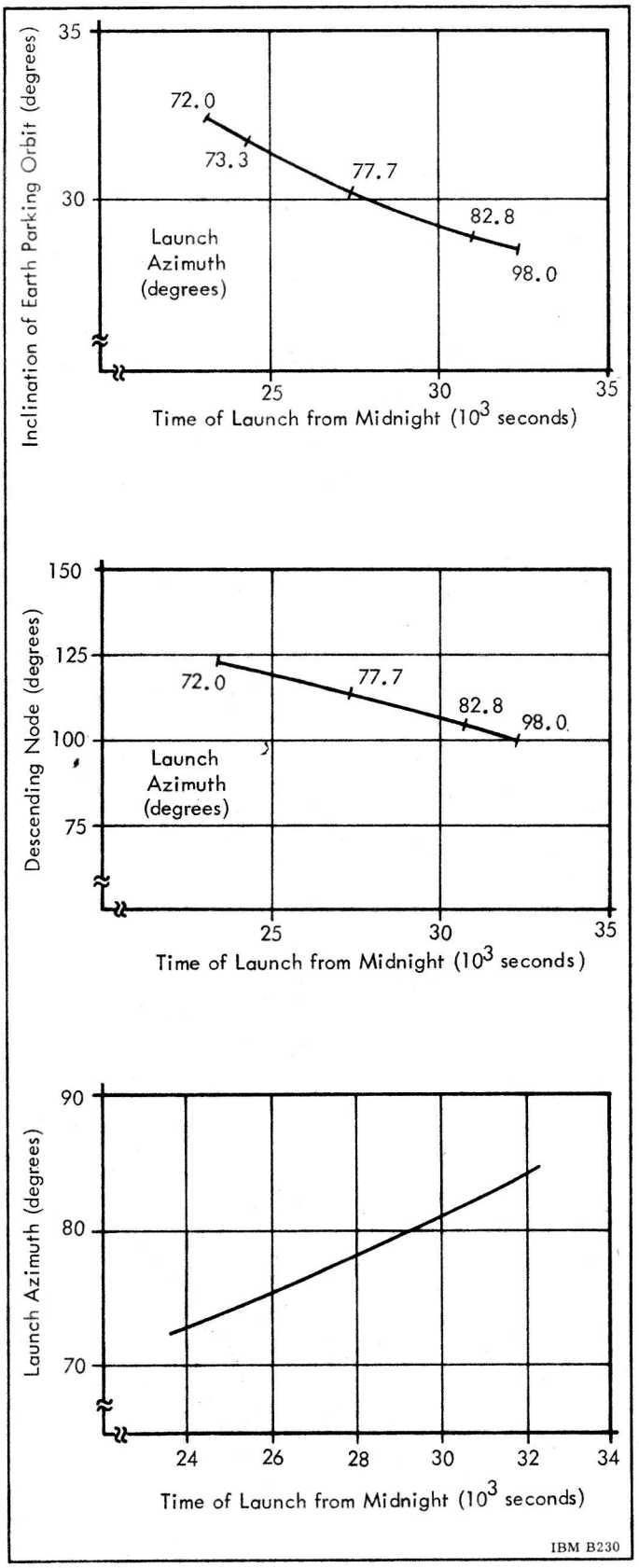


Figure 2.3-3 Launch Window Parameters

Before launch, the Platform is erected with the X_S axis vertical and Z_S axis pointing in the direction of the launch azimuth. Since the launch azimuth is varying with time, the Platform is torqued to maintain this orientation. Just prior to liftoff, the Platform is released and becomes space-fixed oriented. The Z_S axis now determines the flight azimuth.

FIRST-STAGE FLIGHT

The vehicle lifts off vertically from the launch pad and maintains its vertical orientation long enough (approximately 10 second) to clear the ground equipment. It then initiates a roll maneuver to align the vehicle with the flight azimuth direction. (On the launch pad, the vehicle always has a roll orientation fixed to the launching site.) This maneuver gives the vehicle control axes the correct alignment to the flight plane, thus simplifying the computations in the attitude control loop.

During first-stage propulsion, a time-tilt (pitch) program, stored in the LVDC, is applied simultaneously with the described roll maneuver. The pitch angle of the vehicle is commanded according to the tilt program, which is a function of time only and is independent of navigation measurements. However, navigation measurements and computations are performed throughout the flight, beginning at GRR. Cutoff of the first stage engines occurs when the fuel level in the tanks reaches a predetermined level. Thereafter, the first stage is separated from the launch vehicle.

SECOND- AND THIRD-STAGE FLIGHT

After ignition of the S-II Stage, adaptive guidance (i.e., the iterative guidance mode) is used during all propelled flight phases of the mission. The iterative guidance mode, described in paragraph 2.3.2, computes the pitch and yaw angles of the required thrust direction to guide the vehicle on a minimum propellant trajectory into the predetermined parking orbit.

S-II Stage engine cutoff is initiated when the propellant in the S-II tank is consumed to a predetermined level. Following separation of the S-II Stage, the S-IVB Stage engine is ignited.

By this time the vehicle has reached approximately the orbital altitude and the S-IVB propulsion provides the necessary velocity for the circular parking orbit. When the predetermined velocity has been obtained, the guidance computations command engine cutoff.

Acceleration, velocity, and aerodynamic pressure for a typical Saturn V powered flight trajectory into earth orbit are shown in Figure 2.3-5. The step in the F/M curve around 415 seconds is caused by a change of the propellant mixture ratio to increase the specific impulse which, however, reduces the thrust and therefore cannot be applied earlier.

ORBITAL FLIGHT

During orbital coast flight, the navigation program continually computes the vehicle position and

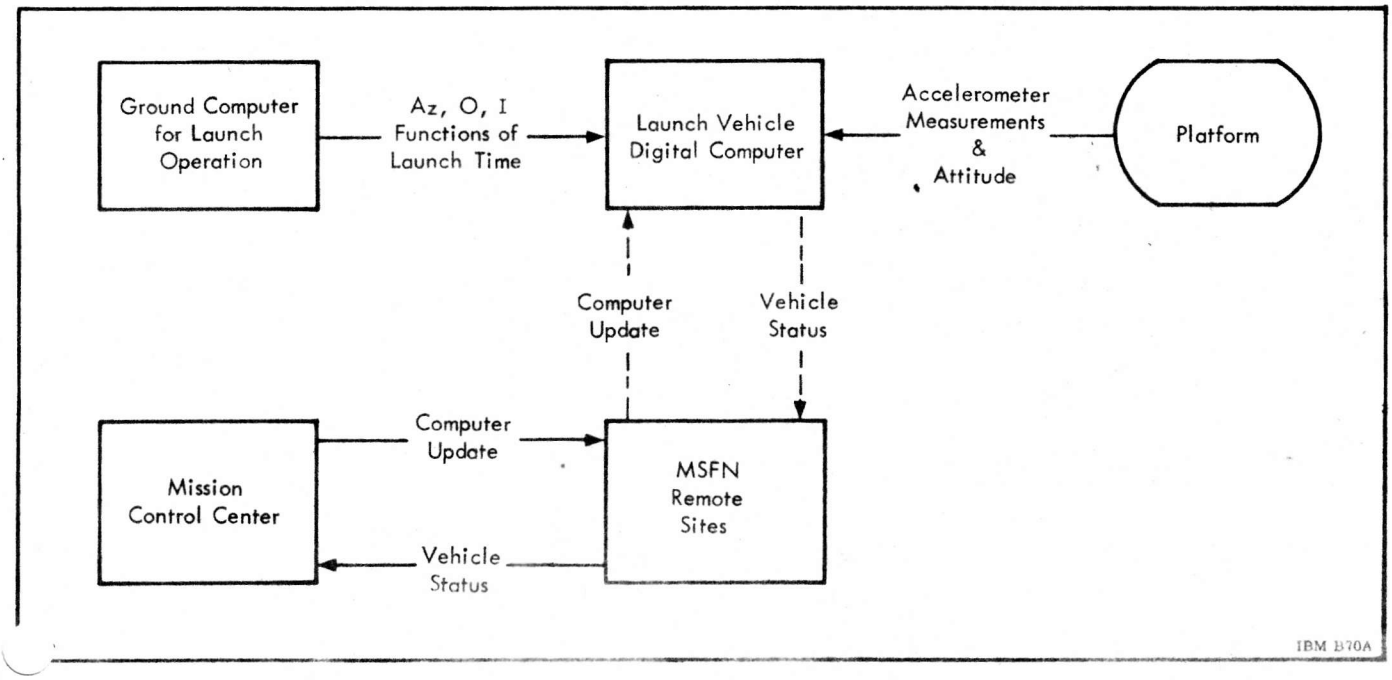


Figure 2.3-4 Linkage Between Vehicle and Ground

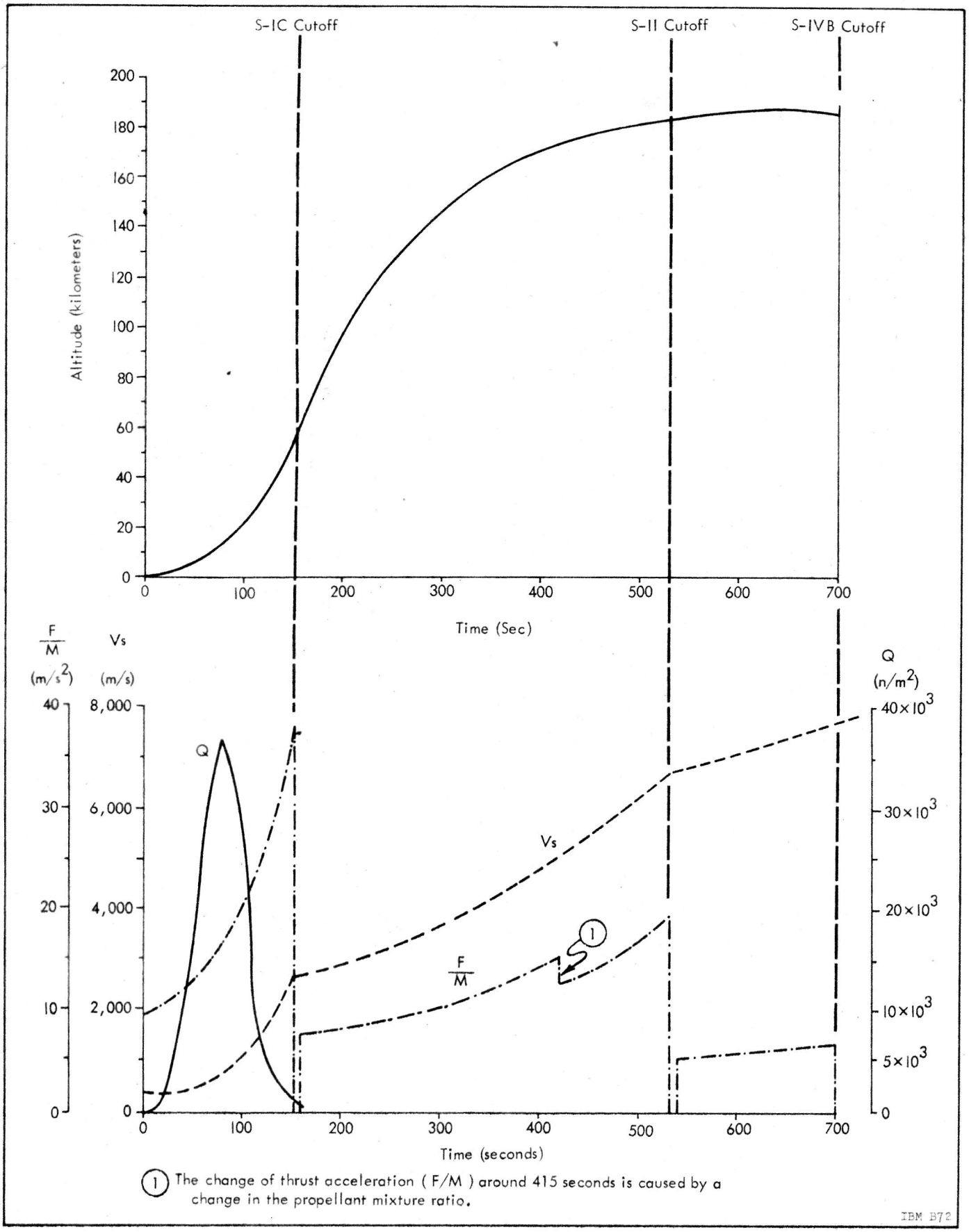


Figure 2.3-5 Altitude, Acceleration (F/M), Velocity (V_S), and Aerodynamic Pressure (Q) for a Typical Saturn Trajectory

velocity from the equations of motion based on insertion conditions. Attitude of the vehicle roll axis in orbit is normally maintained at 90 degrees with respect to the local vertical. The local vertical is determined from navigational computations. The time of re-ignition of the S-IVB engine and the required thrust orientation for powered flight-out-of-orbit are computed during each orbit.

In orbit, navigation and guidance information in the LVDC can be updated by data transmission from ground stations through the IU radio command system.

TRANSLUNAR INJECTION

When the computed time of re-ignition occurs, the S-IVB engine is ignited. The same guidance equations are used again for the translunar injection. The S-IVB propulsion is cutoff when the proper energy (velocity) for translunar injection is achieved.

In the following flight phase, up to and through the transposition maneuver, navigation and guidance computations continue.

CHAPTER 3
ATTITUDE CONTROL

SECTION 3.1
ATTITUDE CONTROL SYSTEM

3.1.1 GENERAL CONSIDERATIONS

The attitude control requirement of the Saturn Launch Vehicle can be divided into attitude control during powered flight and attitude control during coast flight. Attitude control and stabilization during powered flight are accomplished by swivelling of the propulsion engines to control thrust vector direction. During coast flight (in orbit and after translunar injection), attitude control is provided by the auxiliary propulsion system of the S-IVB Stage. This auxiliary propulsion system is used also during powered flight of the S-IVB Stage for roll control which cannot be achieved with the single engine of the S-IVB Stage.

Control of the launch vehicle during ascent into earth orbit can be divided into 2 phases. During first-stage powered flight, the vehicle traverses the dense portion of the atmosphere. Large side forces (resulting from aerodynamic flow and wind) can act on the vehicle. Maneuvers during this flight phase are limited because of structural constraints. Structural loads from aerodynamic forces are kept within a tolerable range by controlling the vehicle to achieve a minimum angle of attack. Aerodynamic pressure reaches a maximum at approximately 12 kilometers (7.4 miles) altitude 77 seconds after liftoff. For a typical Saturn V trajectory, see Figure 2.3-5.

From the viewpoint of vehicle control, maneuvers during vacuum flight are limited only to the extent that structural bending and propellant sloshing are not dangerously excited through the nature of the control command.

The objective of the attitude control system during propulsion of the vehicle is to appropriately orient the thrust vector, relative to the vehicle, such that the required attitude commands are performed in a satisfactorily damped mode of rotation.

The vehicle cannot be considered rigid but must be treated as distributed masses connected by an elastic structure. Forces acting on these masses, resulting from atmospheric perturbations or active control of the vehicle, excite the complex spring-mass system and cause body bending. Since the structure possesses low damping characteristics, oscillatory bending modes of considerable amplitude can be produced, to which control sensors may be subjected at their particular locations. Thus, incorrect information about the total vehicle behavior may cause self-excitation of the bending modes and instability of the vehicle control system.

The vehicle is aerodynamically unstable because the center of pressure is located forward of the center of gravity. As an example, Figure 3.1-1 is a plot of the center of pressure and the center of gravity for the first phase of the Saturn V flight and shows that the vehicle is unstable except for a short period of time around the 60th flight second.

Much of the vehicle characteristic data varies widely with time and the individual stages. In addition, some can be predetermined only to a certain degree, and tolerances must be imposed. Thus a wide operating range of the control system must be provided.

A typical frequency spectrum for the Saturn V Vehicle during powered flight can be seen in Figure 3.1-2. The frequency bands, rather than single frequencies, are the result of changing vehicle-state conditions because of propellant consumption as a function of flight time. The frequency band marked "engine-reaction-zero" represents the sinusoidal response where the inertial effects of the engine induce forces at the engine gimbal point equal and opposite to the side forces obtained by swivelling the thrust vector. The net effect is that the vehicle bending mode response to the engine deflection is zero at this frequency. This is sometimes known as the "tail-wags-dog" frequency.

The Saturn V control law for the thrust vector deflection angle (β) is:

$$\beta = a_0 \psi + a_1 \dot{\phi}$$

where a_0 and a_1 are gain factors, and ψ and $\dot{\phi}$ are attitude error angle and attitude angular rate, respectively. The attitude error angle (ψ) is obtained from the LVDC/LVDA, and the attitude angular rate ($\dot{\phi}$) is obtained from the rate gyros.

The Saturn IB control law for the thrust vector deflection angle (β) is:

$$\beta = a_0 \psi + a_1 \dot{\phi} + g_2 \ddot{y}$$

where $\ddot{y}$ is the lateral acceleration along the pitch or yaw axis as designated, and g_2 is the corresponding gain factor. The pitch and yaw $\ddot{y}$ values are measured by the Control Accelerometers whose sensitive axes are perpendicular to the vehicle longitudinal axis. The lateral acceleration control is used during S-IB Stage propulsion to reduce structural loads from aerodynamic forces and to provide minimum-drift control.

The acceleration measured by the body-mounted Control Accelerometers differs from that measured by the guidance accelerometers. The guidance accelerometers are mounted on the stable platform of the Inertial Platform Assembly and measure accelerations with respect to an inertial space coordinate system, while the Control Accelerometers are used to measure side or lateral acceleration with respect to the vehicle coordinates (acceleration along the yaw and pitch axes).

The choice of the control sensor (rate gyros and accelerometers) locations is very important for attitude stabilization of the vehicle. Stabilization of large launch vehicles, with respect to bending and torsion modes, is usually obtained by shaping networks in each of the three control sensor channels.

Elastic body stability may be attained either by phase stabilization or by attenuation of the bending frequencies. Each method has its advantages. Phase stabilization, especially of the lower bending modes, makes it possible to maintain adequate bandwidth at the control frequency. Also, a phase-stabilized bending mode will damp out faster after excitation than a mode that depends upon attenuation for stabilization. In contrast, stabilization by attenuation is preferable for the higher bending modes since these mode shapes are generally more difficult to define and because it is possible to compensate bending mode shapes and frequencies satisfactorily by attenuation. Thus for practical reasons, phase stabilization is applied to the lower frequencies and gain stabilization (stabilization by attenuation) to the higher frequency spectrum. In the case of large launch vehicles like Saturn V, some bending modes are so close to the control loop frequency that they are best phase stabilized. Thus, for Saturn V during first-stage operation, the first and second bending modes will be phase stabilized and higher modes will be attenuated. During the second-stage powered flight, only the first bending modes will be phase stabilized and higher modes will be attenuated. During the third-stage powered flight, the bending mode frequencies are higher than those for the other stages; therefore, all the bending modes of this stage will be stabilized by attenuation. All torsional modes are at a relatively high frequency and will be attenuated for all stages.

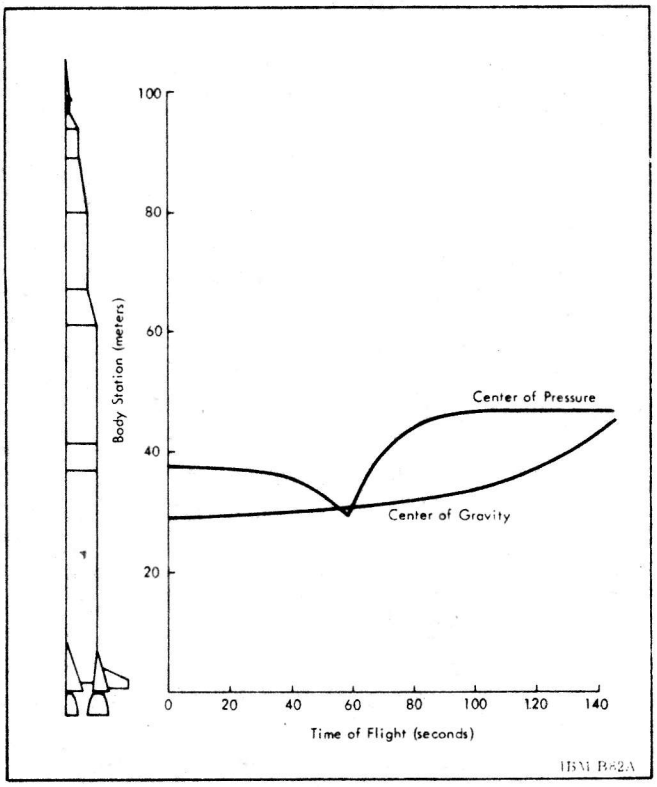


Figure 3.1-1 Variations of CP and CG During Flight

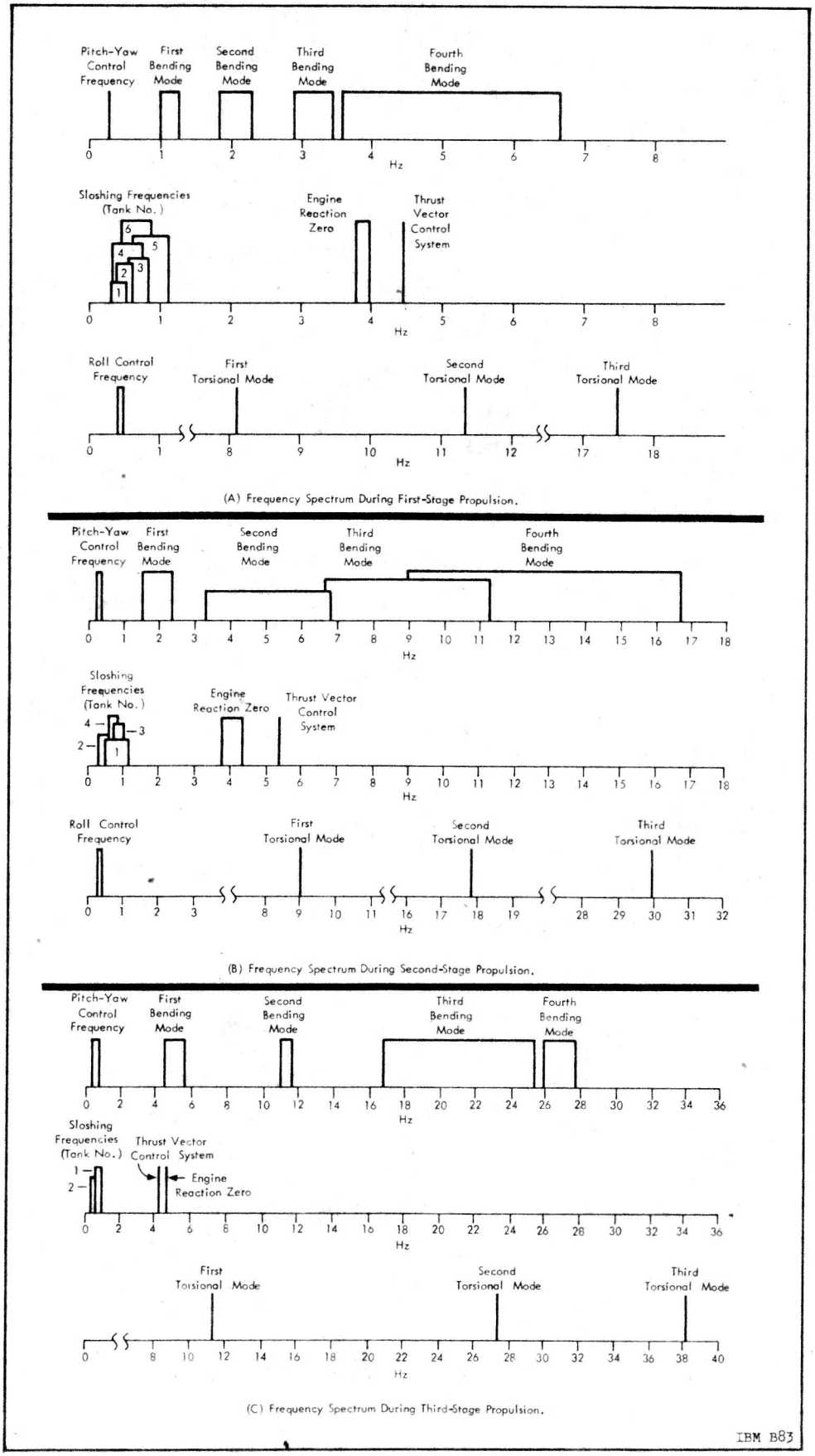


Figure 3.1-2 Typical Saturn V Frequency Spectrum

To provide the desired phase, it is necessary that the rate gyro be properly located on the vehicle. Figure 3.1-3 exhibits the Saturn configuration and the first two bending mode shapes.

The attitude gyros and rate gyros are both located in the Instrument Unit. Since the control loop gain at the bending mode frequencies is much less through the attitude loop than through the rate loop, the location of the attitude gyro is not as sensitive and is usually determined by other considerations - primarily the need to have one centrally located unit for all stages. The location of the body-mounted accelerometers (used only in the Saturn IB first-stage propulsion phase) is also in the Instrument Unit. However, should design changes dictate, the accelerometers could be located elsewhere on the vehicle.

3.1.2 ATTITUDE CONTROL FOR POWERED FLIGHT

Attitude control of the launch vehicle during powered flight is accomplished by swivelling of the main propulsion engines and thereby changing the orientation of the thrust vector.

The attitude control system of the Saturn V Launch Vehicle provides attitude control and stabilization from launch until separation of the S-IVB/IU Stage from the Apollo Spacecraft. For the second-burn phase of the S-IVB Stage, the Apollo navigation guidance and control system is available as a backup system and sends input signals to the Saturn Flight Control Computer. This backup capability for the S-II and S-IVB first-powered flight is under consideration.

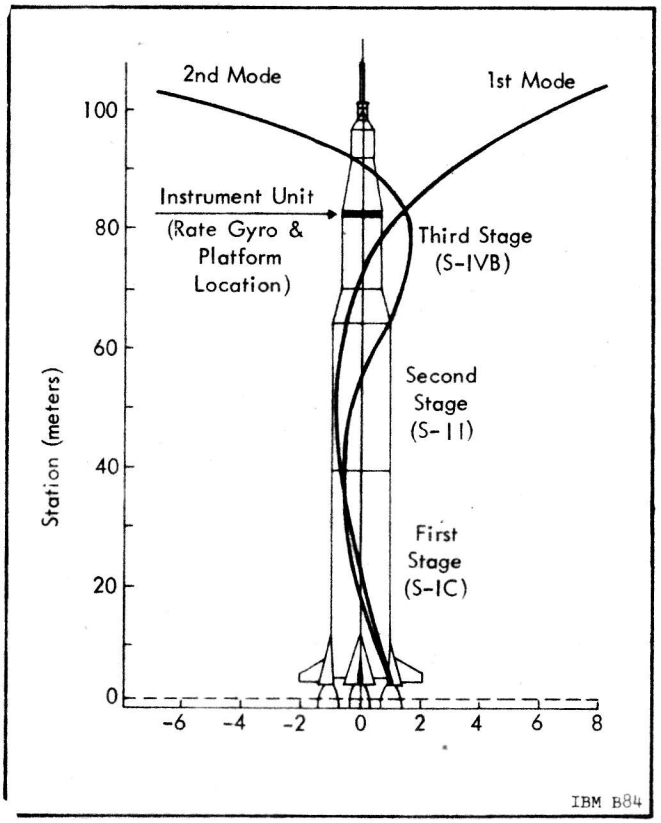


Figure 3.1-3 Shape of the First and Second Bending Modes (Saturn V)

The S-IB Stage has eight engines. The four outer engines are swivelled in pitch and yaw by two hydraulic actuators at each engine (see Figure 3.1-4). The S-IC and S-II Stages have five engines each. The four outer engines can be swivelled in pitch and yaw by two hydraulic actuators at each engine. The S-IVB Stage is propelled by a single engine which can be swivelled in pitch and yaw. In addition, the S-IVB Stage is equipped with an auxiliary propulsion system consisting of 6 nozzles (2 sets of 3 nozzles) mounted on the outside of the aft end of the S-IVB Stage. Four of the six nozzles are required for roll control of the S-IVB Stage, since roll control cannot be achieved with a single main propulsion engine. Figure 3.1-5 shows the layout of the engine actuators and nozzles for the stages of the Saturn V Vehicle. The polarity tables given in this figure indicate which actuators or nozzles are required to perform corrections for pitch, yaw, or roll error signals.

The main components of the Saturn attitude control system are shown in Figure 3.1-6. The platform gimbal angle readings ($\theta_X\ \theta_Y\ \theta_Z$)* indicate the orientation of the vehicle in the navigation coordinate system ($X_S\ Y_S\ Z_S$). The LVDC computes the required thrust vector orientation (i.e., the desired gimbal angles ($\chi_X\ \chi_Y\ \chi_Z$) according to the guidance scheme and generates the difference ($\psi = \chi - \theta$). From the attitude angle differences ($\psi_X \psi_Y \psi_Z$), attitude error signals ($\psi_R \psi_P \psi_Y$ – with respect to the body-fixed roll, pitch, and yaw axes) are generated and sent to the Flight Control Computer.

In addition to the attitude error signals, the Flight Control Computer receives signals from control sensors – attitude rate signals ($\dot{\phi}_P \dot{\phi}_Y \dot{\phi}_R$ – with respect to the vehicle's pitch, yaw, and roll axes) and lateral acceleration signals ** ($\ddot{y}_P$, $\ddot{y}_Y$ – along the pitch and yaw axes). All control signals fed into the Flight Control Computer are analog signals. The Flight Control Computer processes and combines these signals according to the control laws (Equations 3.1-1 and 3.1-2) to generate the control signals for the engine actuators and attitude control nozzles.

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

** Saturn IB only.

3.1.3 ATTITUDE CONTROL FOR COAST FLIGHT

During coast flight, attitude control of the vehicle is accomplished by means of the S-IVB Stage auxiliary propulsion system which contains six attitude control engines (thrust nozzles). When fired, the nozzles produce torques about the center of gravity of the vehicle. They are controlled in a pulse-type manner (full thrust or OFF) by the spatial amplifiers in the Flight Control Computer. The attitude control engines are turned ON when the input signal to the spatial amplifier exceeds certain limits and turned OFF when the input signal falls below a set threshold. The control scheme generates thrust pulses of variable duration at changing intervals which are controlled by the pseudo rate modulators in the spatial amplifier. Over a certain range of the input signal, the output of the modulator is pulse-width and frequency modulated and is a function of the input signal magnitude. Above this range, the output (thrust) is continuously ON; below this range, it is OFF.

A phase diagram (Figure 3.1-7) shows the angle and angular rate relationship for a limit cycle operation. When the vehicle is rotating in a positive direction with positive angle (corresponding to point A on the diagram), it will reach point B when the combination of ψ and $\dot{\phi}$ exceeds the upper side of the attitude deadband — thus firing the rocket motor. The angular rate of $\dot{\phi}$ decreases and changes to a negative quantity, placing the vehicle at point C on the diagram where the signal, still positive, falls below the level required to keep the motor ON, and the torque disappears. From this point, the vehicle drifts at a constant angular velocity toward condition D where the negative deadband limit is exceeded.

The attitude control engines of the S-IVB Stage auxiliary propulsion system are used to control the vehicle attitude in roll during S-IVB powered flight phases and in pitch, yaw, and roll during S-IVB coast flight phases. These engines are located in 2 modules 180 degrees apart on the aft end of the S-IVB Stage. One module is located over position I and the other over position III as shown in Figure 3.1-5. Each module has three hypergolic attitude control engines. One engine of each module is used to control the vehicle's attitude in pitch while the other two are used in yaw and roll control.

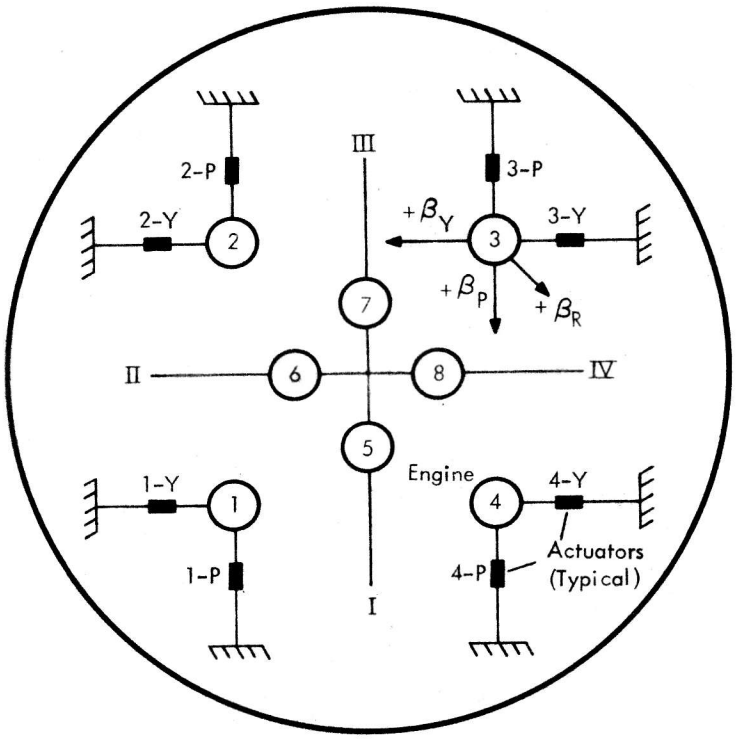
The attitude engine control signal is composed of an attitude error signal (ψ) and a vehicle turning rate signal ($\dot{\phi}$). The body mounted Control-EDS Rate Gyros, located in the Instrument Unit, supply the desired vehicle turning rate information. Attitude error signals (ψ) may come from 1 of 2 sources. When the Instrument Unit is controlling the vehicle, an attitude error signal is supplied by the LVDC through the LVDA as shown in Figure 3.1-8. When the Spacecraft is controlling the vehicle, an attitude error signal is obtained from the Spacecraft over Spacecraft/IU interface lines.

Limits are imposed by the LVDC for IU-generated attitude error signals and by the IU Flight Control Computer for Spacecraft-generated attitude error signals. It should be noted in the figure that attitude error limits of ±2.5 degrees in pitch and yaw and ±3.5 degrees in roll are imposed on the attitude error signals. These error signals are used only by the auxiliary propulsion system.

3.1.4 SPACECRAFT ATTITUDE CONTROL

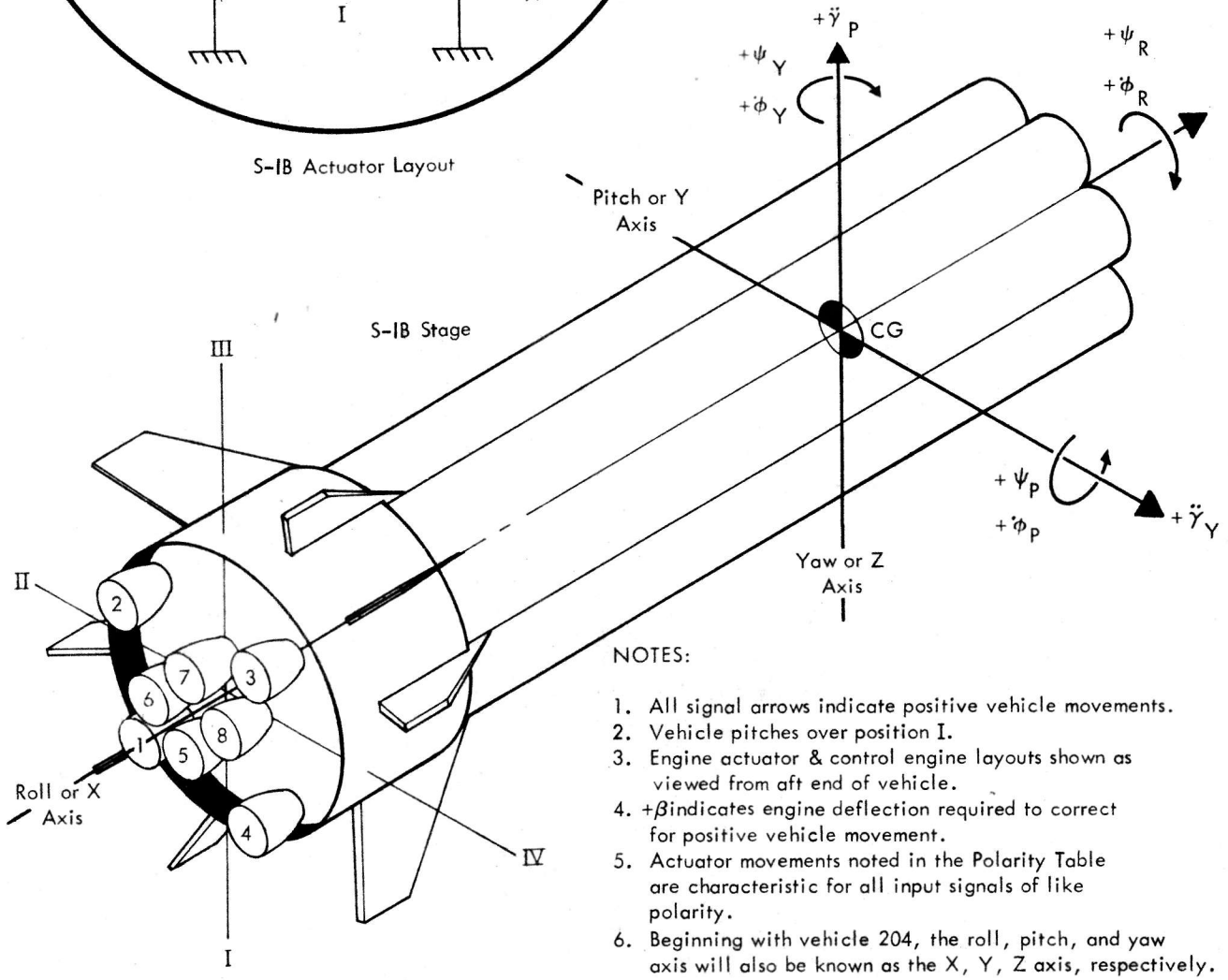
Spacecraft attitude control of Saturn IB/V Vehicles, by the Astronaut, exists as an optional means of controlling the vehicle during the orbital phases of flight. (The hardware for control during powered flight does exist, but its use is not planned for present missions.)

The attitude error signals from the Spacecraft may originate in the Apollo navigation, guidance, and control system or may be generated by the Astronaut through manual control. In any case, the limiters in the IU Flight Control Computer will limit the angular rate. These limits prevent excessive propellant



S-IB Actuator Layout

S-IB Control Signal Polarity Table			
Actuator No.	Signal & Actuator Movement		
	$+\psi_R$	$+\psi_Y$	$+\psi_P$
1-Y	RET	RET	
1-P	EXT		RET
2-Y	EXT	RET	
2-P	RET		EXT
3-Y	RET	EXT	
3-P	EXT		EXT
4-Y	EXT	EXT	
4-P	RET		RET



NOTES:

1. All signal arrows indicate positive vehicle movements.
2. Vehicle pitches over position I.
3. Engine actuator & control engine layouts shown as viewed from aft end of vehicle.
4. $+\beta$ indicates engine deflection required to correct for positive vehicle movement.
5. Actuator movements noted in the Polarity Table are characteristic for all input signals of like polarity.
6. Beginning with vehicle 204, the roll, pitch, and yaw axis will also be known as the X, Y, Z axis, respectively.

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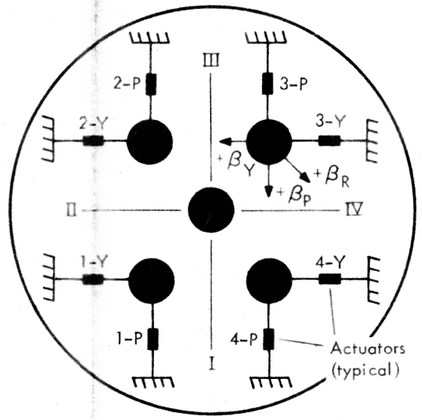
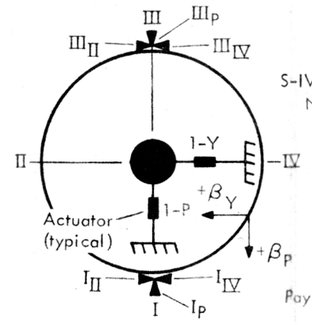
Figure 3.1-4 S-IB Stage Engine and Actuator Configuration

NOTES:

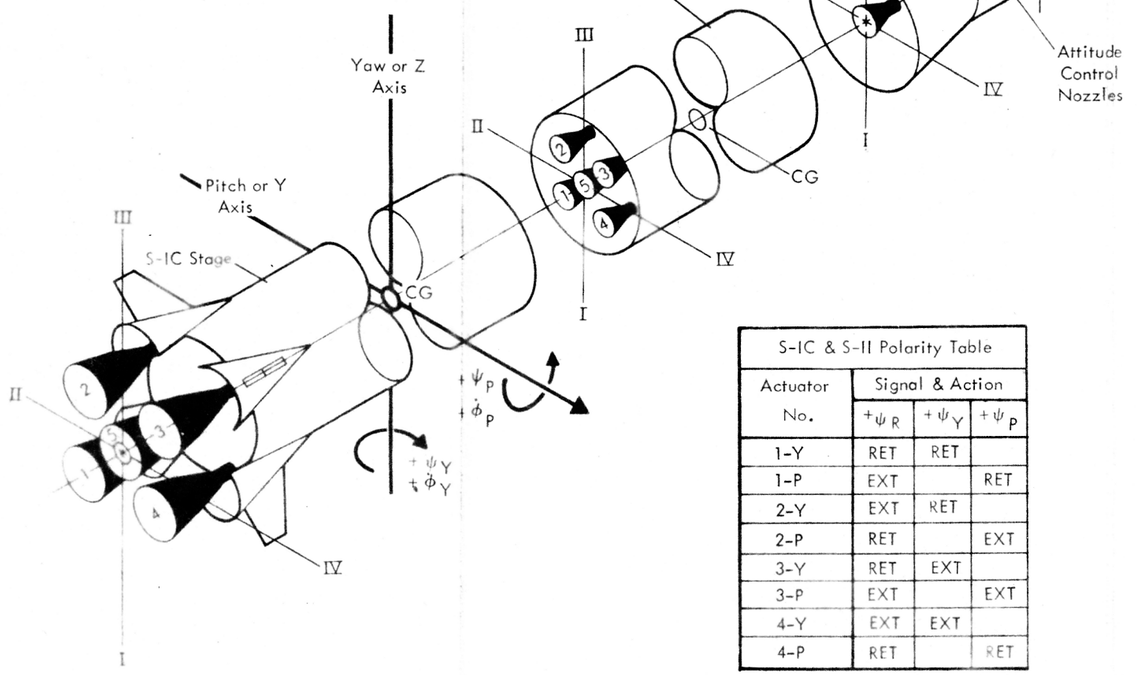
1. All signal arrows indicate positive vehicle movements.
2. Vehicle pitches over position I.
3. Engine actuator layouts shown as viewed from aft end of vehicle.
4. Directions and polarities shown are typical for all stages.
5. $+\beta$ indicates engine deflection required to correct for positive vehicle movement.
6. CG = Center of gravity
   F = Nozzles on
   EXT = Actuator extended
   RET = Actuator retracted
   β = Thrust vector angular deflection
7. Beginning with vehicle 502, the roll, pitch, and yaw axes will also be known as the X, Y, Z axes, respectively.



S-IC & S-II Actuator Layouts



S-IVB Actuator and Nozzle Layout



S-IC & S-II Polarity Table

Actuator No.	Signal & Action		
	$+\psi_R$	$+\psi_Y$	$+\psi_P$
1-Y	RET	RET	
1-P	EXT		RET
2-Y	EXT	RET	
2-P	RET		EXT
3-Y	RET	EXT	
3-P	EXT		EXT
4-Y	EXT	EXT	
4-P	RET		RET

S-IVB Polarity Table

Actuator No.	Signal & Action			
	$+\psi_R$	$-\psi_R$	$+\psi_Y$	$+\psi_P$
1-Y			EXT	
1-P				RET
Engine No.				
I_{IV}		F		
I_P				
I_{II}	F			
III_{II}		F		
III_P				
III_{IV}	F			

Conditions During Coast						
	$+\psi_R$	$-\psi_R$	$+\psi_Y$	$-\psi_Y$	$+\psi_P$	$-\psi_P$
I_{IV}		F		F		
I_P					F	
I_{II}	F		F			
III_{II}		F	F			
III_P						F
III_{IV}	F			F		

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Figure 3.1-5 Saturn V Engines, Actuators, and Nozzle Arrangement

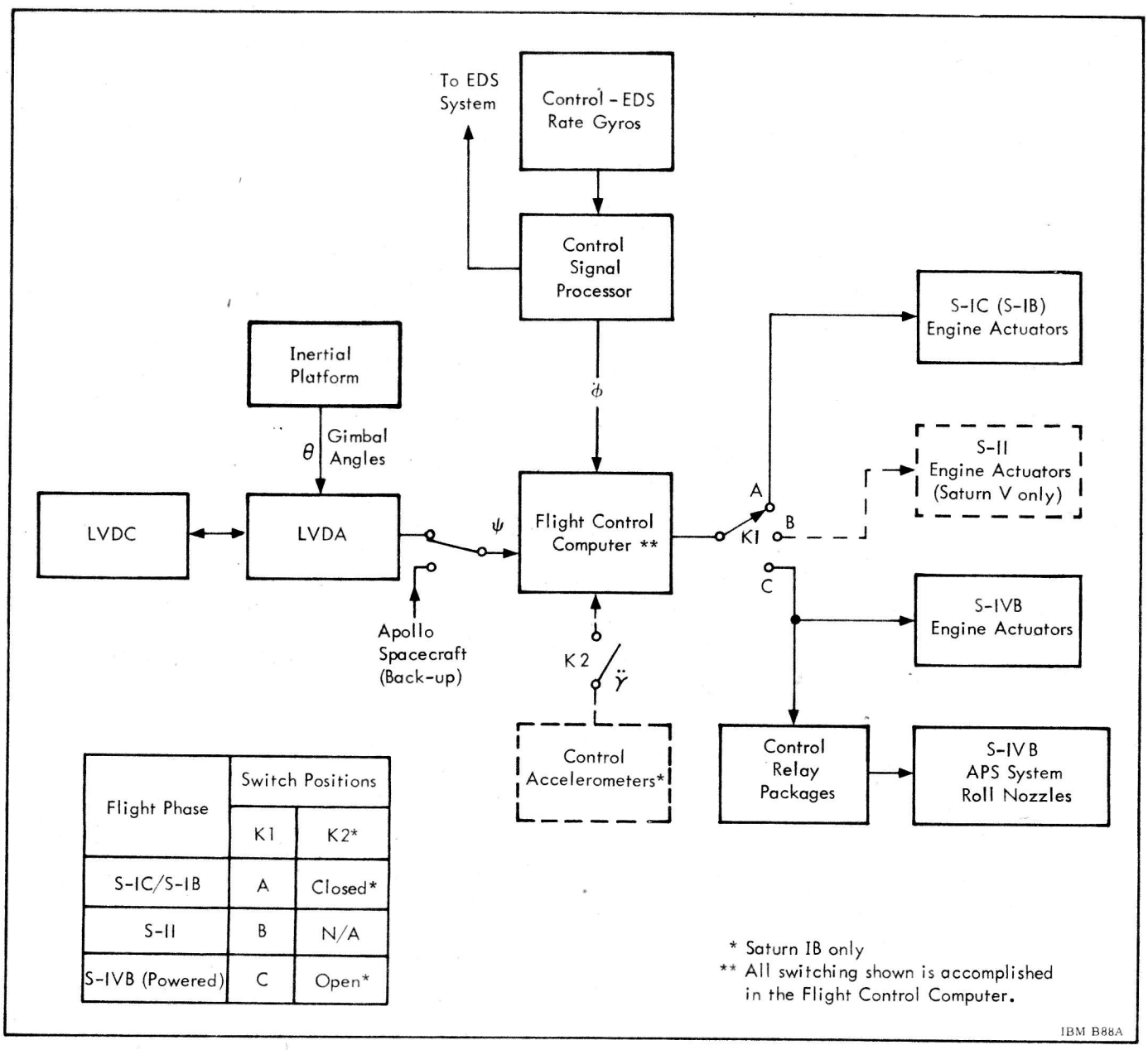


Figure 3.1-6 Saturn Control System Simplified Block Diagram (Powered Flight)

usage which would result from large angular rate commands while driving the vehicle to the desired attitude.

The Apollo Spacecraft attitude reference system can follow the instantaneous vehicle attitude. This is accomplished by driving the command display unit servo motor with an error signal which is formed by differencing the commanded and actual gimbal angles. When the Astronaut wishes to maintain a particular attitude orientation, he can use the computer to set the command display unit command resolver to the desired gimbal value. The difference between the commanded and actual gimbal angles results in an error signal which is resolved into vehicle coordinates and is given to the IU Flight Control Computer as an attitude error signal. The S-IVB attitude control system then operates in the limit-cycle mode about this command attitude.

3.1.5 ATTITUDE SIGNAL PROCESSING

The attitude control system is a closed-loop system in which various input control signals are

supplied by way of the Flight Control Computer (FCC) to the engine actuators. Signals, PSI (ψ) and Phi dot ($\dot{\phi}$), are generated for each of the three vehicle axes (roll, pitch, and yaw) and can be written as three equations for the Beta command.

$$\beta_r = A_0 \psi_r + A_1 \dot{\phi}_r$$

$$\beta_p = A_0 \psi_p + A_1 \dot{\phi}_p$$

$$\beta_y = A_0 \psi_y + A_1 \dot{\phi}_y$$

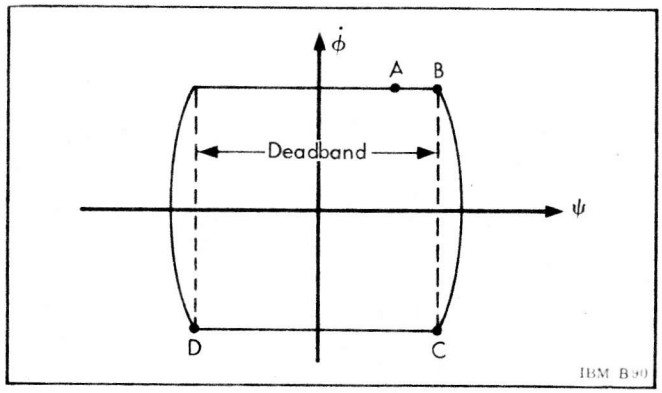


Figure 3.1-7 Limit Cycle Phase Diagram

Figure 3.1-9 illustrates a processing and flow diagram for attitude control signals during powered flight. Gimbal angles (θ_x, θ_y, θ_z) from the ST-124 Inertial Platform are received as electrical input signals in the LVDC and indicate the actual attitudes of the vehicle with respect to the space coordinate reference system. The Chi (χ_x, χ_y, χ_z) signals are generated in the LVDC and indicate the desired vehicle attitudes as determined by the guid-

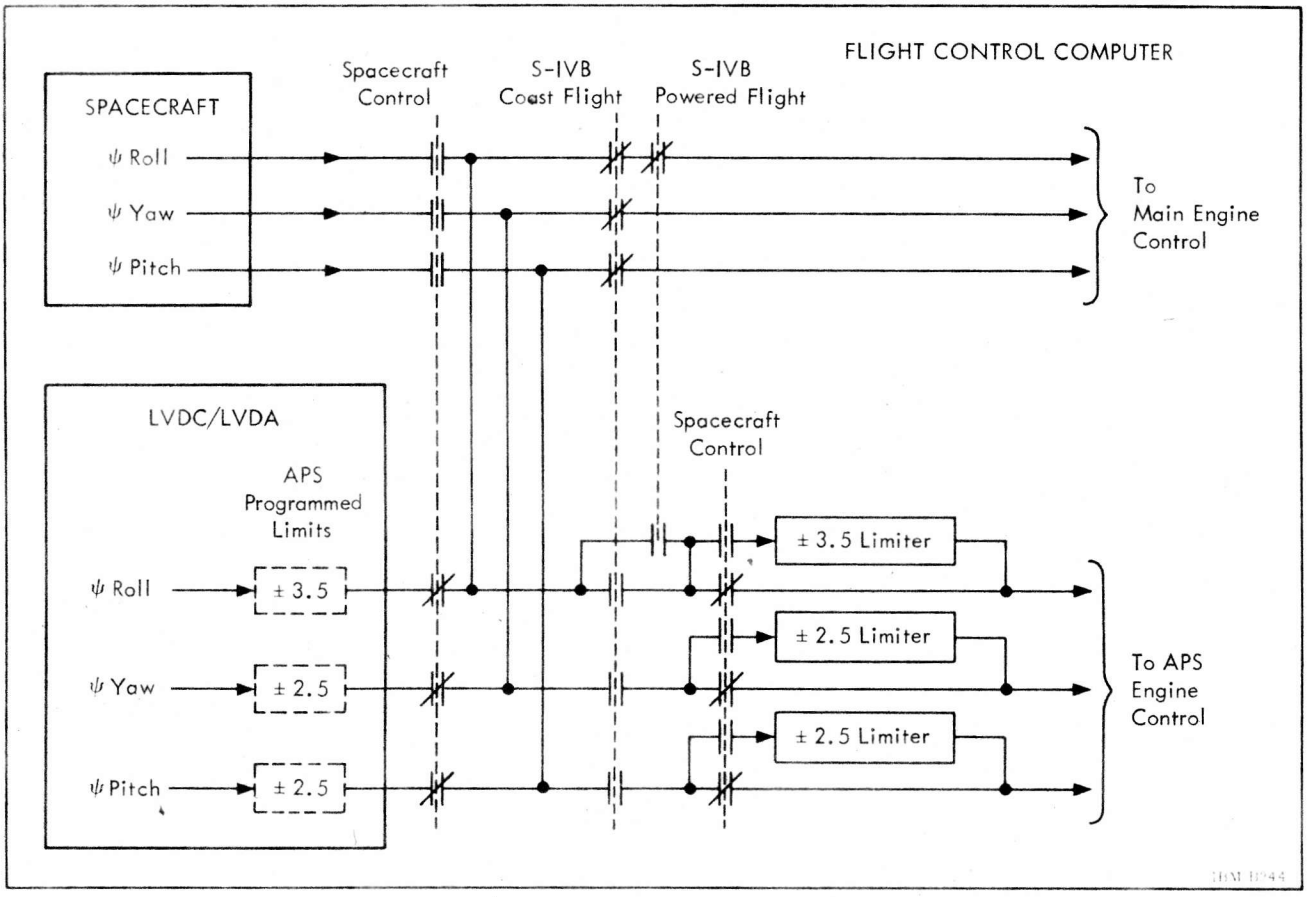


Figure 3.1-8 Attitude Error Signal Sources Functional Block Diagram

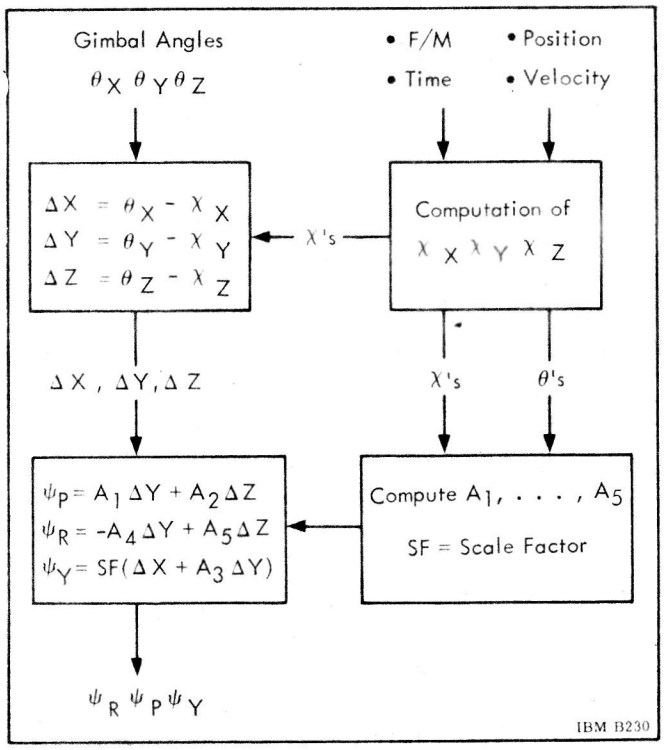


Figure 3.1-9 Attitude Signal Flow Diagram

ance scheme. The attitude error signals (Δ_x, Δ_y, Δ_z) are the differences between actual gimbal angles and the desired vehicle attitude angle and are measured in the platform reference frame. Since the attitude error commands must be provided in the vehicle reference frame, a coordinate transformation must be performed. The sine-cosine coefficients (A1, A2, A3, A4, A5, and scale factor) are computed during every minor loop support routine of the Flight Program and are utilized to transform the attitude error signals into vehicle oriented ladder commands (ψ_p, ψ_r, ψ_y). The coefficients A1 through A5 are calculated approximately once per second (the gain to be used in these equations is defined in Table 3.1-1).

The angular rate error signals ($\dot{\phi}_p$, $\dot{\phi}_r$, and $\dot{\phi}_y$) are supplied by the Control-EDS Rate Gyro Package through the Control Signal Processor. The outputs are provided as redundant signals and are the attitude angular rates of the vehicle about the vehicle's pitch, roll, and yaw axes. The purpose of the angular rate error signals is to control the rate of response of the vehicle to the Beta command and to eliminate overshoot at the end of the correction.

The generation of the attitude error commands (ψ) for roll, pitch, and yaw is performed in the LVDC by computing the difference between the actual vehicle attitude angles (θ) and the guidance command angles (χ), where the guidance command angles are the desired vehicle attitude angles. The method for obtaining the attitude error command as stated in the general equation ($\psi = \chi - \theta$) is illustrated in the flow diagram (Figure 3.1-9) and the angular difference (in Figure 3.1-9) indicates the correction that must be applied to the vehicle's engines to achieve required trajectory.

PLATFORM GIMBAL ANGLES

The ST-124M Inertial Platform gimbal angles provide an indication of the actual roll, pitch, and yaw attitude of the vehicle and are measured during minor loop operation in the Flight Program. The measurement of these angles occurs every 40 milliseconds during the boost mode and twice per second during orbit. The angles are provided as an electrical signal from the output of a dual resolver system in the ST-124M, (Refer to Section 14.4).

GIMBAL ANGLE REASONABLENESS TEST

To ensure that the gimbal angle readings are accurate, the Flight Program executes a test routine within the LVDC to check the validity of the gimbal angle readings. This test routine is called the Gimbal Angle Reasonableness Test and is not to be confused with the Accelerometer Reasonableness Test. Although the routine is termed Reasonableness Test, the actual gimbal angle processing consists of 3 tests:

Disagreement Test

Zero Test

Reasonable Change Test

DISAGREEMENT TEST

The output from the dual speed resolvers is sent to the LVDA as electrical signals (analog) where they are converted to digital form by the duplexed Crossover Detectors (COD) and temporarily stored in two 11-bit counters to form two gimbal angle readings, an "A" reading and a "B" reading (Refer to Figure 15.6-2). These readings are compared in the LVDA and, if the 2 readings disagree by more than +3 or -4 counts, a Disagreement Bit (DB) is set. The DB is part of the gimbal angle

Table 3.1-1 Typical Attitude Parameters for Saturn V

Flight Mode	Attitude Control Gain	Attitude Rate Limits			Limits on Magnitude of Attitude Commands		
		Yaw	Pitch	Roll	Yaw	Pitch	Roll
S-IC Burn	1	±12°/s	±12°/s	±12°/s	15°	15°	15°
S-II Burn	1	±12°/s	±12°/s	±12°/s	15°	15°	15°
S-IVB 1st Burn	1	±12°/s	±12°/s	±12°/s	15°	15°	3.5°
Coast	1	±2.4°/s	±2.4°/s	±2.4°/s	2.5°	2.5°	3.5°
S-IVB 2nd Burn	1	±12°/s	±12°/s	±12°/s	15°	15°	15°
Coast	1	±2.4°/s	±2.4°/s	±2.4°/s	2.5°	2.5°	2.5°

word placed in the accumulator and is telemetered as a measurement. A one in bit position D13 on mode code 24 indicates that a DB is present. Reading "A" is used if the DB is not set, but if it is set, the LVDC goes to a special subroutine in the Flight Program to evaluate the error source. This subroutine performs tests to determine whether the disagreement was caused by the COD counters, COD multiplexers, or the DB circuitry.

The disagreement in counter A and counter B arises from one of the following three error sources:

1. Counter A or counter B or both are defective.

2. DB circuitry defective.

3. A COD multiplexer circuit input to the counters is defective.

To determine whether either or both counters are defective, the counters are individually tested by permitting them to count a known frequency for a known time and comparing the count with a stored constant. If a reading is not within ±3 counts of the stored constant, the counter is presumed to have failed.

If neither counter is defective, no logical reason is found for the DB. Therefore, the computer logic assumes that the failure which set the DB was in the counter "B" reading. The counter A reading is selected and a failure count is implemented against counter B. If the counter A reading passes the reasonable change test, then it is assumed that the counter B reading was incorrect and caused the DB to be set. If the DB is set five times with both counters checking operational, and the A reading passes the reasonable change test all five times in one computation cycle, the counter B is assumed to have failed and the counter A is selected permanently.

If the A reading fails the reasonable change test after the DB is set and both counters check operational the assumption that the counter B reading caused the DB is proven incorrect. If the A reading fails the reasonable change test twice in one computation cycle after a DB is set and both counters check operational, the counter B is selected permanently.

If through the counter testing, the counter A or counter B is determined to be faulty, the respective counter keeping track of failures is updated and the other reading is used. Two failures of either A or B counter in a computation cycle causes the other counter to be permanently selected. If both counters fail, the last good attitude error command is used. At this time bit D14 will be set in conjunction with bit D13 on mode code 24. Also, the guidance failure discretes will be set indicating that the platform has failed and attitude reference has been lost. If both counters fail twice in one computation cycle, the program is modified such that further DB's cause the last good attitude error command to serve as the new attitude error command.

ZERO TEST

After the gimbal reading has been selected by the above process, the reading undergoes a zero test. This test is designed to determine whether the counter reading is zero when it should not be. A zero reading is one where each of the 11 bits in

the counter is zero. An unexpected zero reading is interpreted as an error and is included as part of the tine to detect a failure in the power source acting the dual-speed resolver system. If a zero reading occurs, the previous counter reading is examined to determine if it also was zero. If it was not zero, the single zero reading condition has no significance and is overlooked. The program then transfers control to perform the reasonable change test. If, however, the previous reading was zero, the last attitude error command is checked to determine whether its magnitude was less than the prestored value in the flight program's table of test constants. Refer to Table 3.1-2 (Zero Test column). If the attitude error command is less than the prestored value in the table, it indicates that the vehicle's attitude was not changed and the zero reading indicated by the counter is assumed to be valid. If however the attitude error command is greater than the prestored constant, the indication is such that the attitude of the vehicle had changed and the counter reading should indicate a reading greater than zero to show the vehicle change. In this latter condition, the zero reading is not valid and the gimbal reading is called unreasonable. When the zero test is unreasonable, the gimbal angle reasonable test failure counter is incremented by a count of one and the previous good attitude error command is reissued.

Table 3.1-2 Gimbal Angle Reasonableness Test Constants

Time Interval	Fine Resolver	Coarse Resolver (First)	Coarse Resolver (After First Use)	Zero Test
RR*** (Initial Reading Only)	1.4 **	-----	----	0.06
GRR*** to T_5 + 100	0.4	18.5	0.6	0.06
T_5 + 100 to T_6*	1.0	18.5	2.0	1.2
T_6 - 9 to T_7 + 15	0.4	18.5	0.6	0.06
T_7 + 15 to T_7 + 700	1.5	18.5	2.0	1.2
T_7 + 700 to End of Mission	1.0	18.5	2.0	1.2

* This change is made when switch over from orbital navigation to boost navigation occurs.

** Due to the fact that there can be a one degree misalignment of the vehicle on the launch pad and the possibility of additional gimbal angle offsets due to winds, the initial fine gimbal reasonableness test constants (RTC) at GRR only is specified as 1.4 .

*** Guidance Reference Release (GRR).

The zero test for the yaw axis is performed in the same manner as performed in the pitch or roll axis. Although the change in this axis is expected to be zero, the yaw gimbal angle output, providing successive zero counter readings, does not necessarily indicate an error. The last attitude error command is checked against the zero test constant and if less than the value of the test constant, the counter readings of zero are valid.

REASONABLE CHANGE TEST

If the selected gimbal angle reading passes the zero test, the reading is compared to the last reasonable reading. The difference between the two readings is compared to the Gimbal Angle Reasonableness Test constants which are prestored in the LVDC memory. If the magnitude of the difference is greater than the prestored values (Refer to Table 3.1-2 first three columns), the new reading is called unreasonable and the failure counter is incremented. The initial value for the fine resolver contains a launch pad misalignment factor of one degree and a possibility of additional offsets due to winds. The large initial value for the coarse resolver is purposely set to compensate for the large differences of accuracies between fine and coarse resolvers.

If the gimbal reading is unreasonable during either the zero test or the reasonable change test, the previous good attitude error command is reissued. If a particular (x, y, or z) channel is found to be unreasonable 3 times during one computation cycle in boost or 3 times during 5 seconds in orbit, the backup (2:1) resolver replaces the fine (64:1) resolver as a source of gimbal angle readings. The test for this condition occurs each time a gimbal angle reasonableness test failure counter is incremented. Unreasonable readings from the backup resolver at a rate of more than 15 per second during boost or more than 6 in 5 seconds during orbit causes the guidance reference failure discrete to be set. The test for this condition is made once per computation cycle in boost and once every 5 seconds in orbit in minor loop support.

The apparent rate of vehicle attitude change for conditions resulting from either the fine or coarse resolver failure can be determined from the values of the test constants contained in Table 3.1-2 and the fact that during boost the minor loop is processed 25 times per second and in orbit the minor loop is processed 10 times per second (gimbal angle only read twice per second).

Examples:

Boost:

$0.04 \times 25 = 10.0^{\circ}$/sec (fine resolver)
$0.06 \times 25 = 15.0^{\circ}$/sec (coarse resolver)

Orbit:

$1.0 \times 2 = 2.0$ /sec (fine resolver)
$2.0 \times 2 = 4.0$ /sec (coarse resolver)

Attitude Error Commands

The attitude error commands (ψ_R, ψ_P, ψ_Y) are the signals generated in the LVDC and used by the FCC to implement the change in direction of the thrust vector. These signals are generated 25 times per second during boost (powered flight) and 10 times per second in orbital flight. The computation is performed during the minor loop routine of the Flight Program. However, the evaluation of the signal is much more complicated than just described. Evaluation of the signal is described in the following paragraphs.

Major Loop Chi

During each computation cycle, the LVDC cycles through various routines. During the Iterative Guidance Mode (IGM) routine, the LVDC, via inputs such as time, velocity and position, computes the desired attitude of the vehicle required to meet orbital end conditions. This value of Chi (X) is calculated in the platform reference system for each of the vehicle's axes. The changes in trajectory that are required in the elapsed time period from one computation cycle to the next is the ΔChi and is defined as:

$$\Delta \text{Chi}\ (x, y, z) = \text{Chi (current)} - \text{Chi (past)}$$

This change is the change in the desired vehicle attitude that will provide an optimum trajectory to achieve desired end conditions.

Chi Increments

To provide a smooth and continuous change in vehicle attitude, when correcting for a change in desired vehicle attitude, ΔChi is incremented into smaller angles as a function of the duration of the computation cycle and the number of times the minor loop is performed. The process of incrementing ΔChi is an averaging process and is performed during the minor loop support routine (once every major loop during boost). The increments are termed DChi and are defined by:

$$\text{DCHI} = \frac{\Delta \text{Chi}\ (x, y, z) \cdot (0.04)}{\text{Time (comp cycle)}}$$

Limits are placed on DChi values so that the rate of change of the vehicle attitude is limited to one degree per second in boost. This limiting is performed in the minor loop support routine. During orbit, the rate limit is set to 0.4 and 0.6 degree per second for pitch/yaw and roll respectively. Refer to Table 3.1-3 for the attitude command rate limits.

MINOR LOOP CHI (MLCHI)

During each minor loop, the desired vehicle attitude is updated by increasing the previous value of MLChi by the incremental amount DChi. Under normal operating conditions the completion of each computation cycle should result in a value of the current MLChi being equal to the first value of MLChi initiated at the start of the computation plus ΔChi. However, if the commanded attitude change exceeds the rate of change limitation imposed on DChi, it may require two or more computation cycles to achieve the desired attitude change:

Incremental Update
MLChi (current) = MLChi (previous) + DChi

Major Loop Update (normal operation)
MLChi (current) = MLChi (initial) + ΔChi

Gimbal Angle Read

The gimbal angles (θx, θy, θz) are read during each minor loop routine in boost and twice per second in orbit. The angles are read in the Platform reference coordinate system.

Table 3.1-3 Attitude Constants

Flight Mode	Ladder Rate Limit (deg/minor loop)			Ladder Magnitude Limit (degrees)			Attitude Command Rate Limit (deg/sec)		
	Pitch	Roll	Yaw	Pitch	Roll	Yaw	Pitch	Roll	Yaw
S-IC Burn	0.48	0.48	0.48	15.3	15.3	15.3	1.0	1.0	1.0
S-II Burn	0.48	0.48	0.48	15.3	15.3	15.3	1.0	1.0	1.0
S-IVB 1st Burn	0.48	0.48	0.48	15.3	3.5	15.3	1.0	1.0	1.0
Coast	0.24	0.24	0.24	2.5	3.5	2.5	0.4	0.6	0.4
S-IVB 2nd Burn	0.48	0.48	0.48	15.3	15.3	15.3	1.0	1.0	1.0
Coast	0.24	0.24	0.24	2.5	3.5	2.5	0.4	0.6	0.4

Attitude Error Command

The updated value of the MLChi and the current gimbal angle reading are compared during each minor loop routine. Any difference between the desired vehicle attitude (X) and the actual vehicle attitude (θ) is called the attitude error command. These signal differences or attitude error commands are referenced to the Platform reference coordinate system. Since the signals required to correct the vehicle's attitude must be referenced to the vehicle's body reference coordinate system, the commands (Δx, Δy, Δz) must be rotated through a transformation matrix to obtain the commands ψR, ψP, and ψY. The trigonometric functions required to transform from Platform frames to the vehicle frame are computed in the minor loop support routine.

Limiting

The Attitude Error Commands are magnitude and rate limited using flight mode dependent constants. As shown in Table 3.1-3, these limitations are placed on the ladder outputs (ψR, ψP, and ψY) by the Flight Program to provide control and stability. Maximum ladder magnitude is 15.3 degrees and is a function of hardware design. The limit values as shown reflect an attitude control gain of 1.

ATTITUDE ERROR COMMAND PROCESSING

Figures 15.6-9 and 15.6-10 illustrate the attitude command processing within the LVDA. Although the attitude error commands are generated as digital data, the signals are converted to analog signal prior to being presented to the FCC. The development of the signals is performed in the LVDA and includes digital to analog conversion, error detection, signal amplification and scaling, telemetry buffering and storage. Digital data are alternately received from the LVDC and are temporarily stored in three 9-bit ladder registers. Two of the ladder registers in conjunction with two ladder decoders provide redundant processing of the commands. The third ladder register and ladder decoder act as a reference channel used in error detection.

The error detector compares the reference ladder decoder with both the ladder decoder A output and the output of the selected output multiplexer driver. If the comparisons are within designated tolerances, the error detector allows the normally selected channel A to remain selected. If either or both comparisons are out of the normal tolerance ($\approx$0.1 degree) the error detector will select channel B. Channel A is reselected by the LVDC in each minor loop unless channel A is known to have failed 3 times in a computation cycle. The output of the selected ladder is applied to 3 output multiplexer-drivers. Each driver, when enabled by the roll, pitch or yaw control signal, will sample and store its respective roll, pitch or yaw command. The "hold" capacitor in the driver stores the analog voltages for a limited time before the signal tends to decay. Constant update of the attitude commands is provided every 40 milliseconds during the boost phase of flight and every 100 milliseconds during the coast phase of flight.

SECTION 3.2
CONTROL SENSORS

3.2-1 RATE GYROS

Single degree of freedom rate gyros are used on the Saturn Vehicles to sense the angular rate of movement of the vehicles about the roll, yaw, and pitch axes.

This type of rate gyro is employed in the Control-EDS Rate Gyro Package in the IU of the Saturn IB/V Vehicles. It is used both for attitude control and for EDS operations.

The rate gyro (Figure 3.2-1) uses a microsyn differential transformer pickoff which is coupled to the gimbal. Angular rate about the input axis of the rate gyro will be translated to an ac voltage output signal from the microsyn. The amplitude of this signal has a definite relationship to the angular rate. This relationship, called the scale factor, is approximately 0.5656 Vp-p/degree/second. The rate gyro has the capability of sensing angular rates to 20 degrees/second in either counter-clockwise or clockwise direction.

Each rate gyro is equipped with self-test capabilities. A self contained electromagnetic coil can be remotely excited to cause the rate gyro gimbal to be deflected. This deflection provides an output from the microsyn without subjecting the gyro to a rate input. A built-in generator, integral with the gyro rotor,

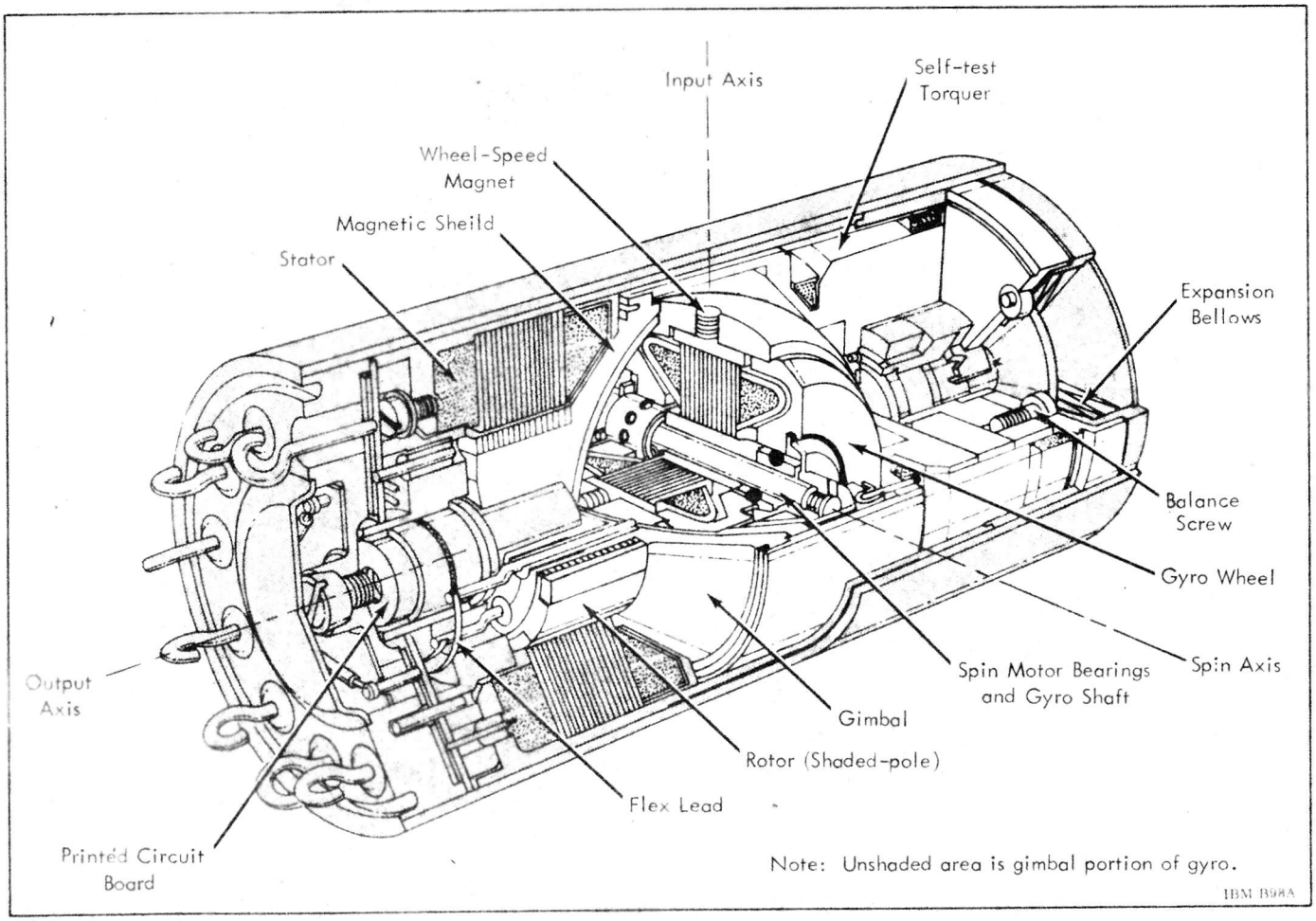


Figure 3.2-1 Cutaway View of a Self-Test Rate Gyro

provides ac pulses (the frequency is the indication of the gyro rotor speed).

The rate gyros are fluid-damped devices which maintain a nearly constant damping factor over the range of temperatures in which the damping fluid retains its fluid characteristics. When the gyros are employed in low-temperature environments which exceed the gyro ratings, the package must be supplied with heaters to ensure proper operation.

3.2.2 CONTROL-EDS RATE GYRO PACKAGE

The Control-EDS Rate Gyro Package (Figure 3.2-2) contains nine rate gyros arranged in a triple-redundant configuration (Figure 3.2-3). Each group of three rate gyros provides output signals for angular rate about the pitch axis ($\dot{\phi}_P$), yaw axis ($\dot{\phi}_Y$), and roll axis ($\dot{\phi}_R$). Each group of gyros is completely independent of the two other groups. Thus, there are nine separate output signals – one from each gyro. The comparison and selection of the output signals are accomplished in the Control Signal Processor.

Each of the gyro groups receives 400 Hz, single-phase power from a separate inverter. These inverters are located in the Control Signal Processor.

This triple redundant configuration increases the reliability for the Control-EDS Rate Gyro Package, which is used throughout the mission.

Since the Control-EDS Rate Gyro package is located on an IU cold plate, it will be maintained at a temperature which will not require the use of heaters within the package.

3.2.3 CONTROL SIGNAL PROCESSOR

The Control Signal Processor converts the ac rate gyro signals into dc signals required as inputs to the Flight Control Computer. It also compares and selects output signals from corresponding redundant rate gyros. A block diagram of the Control Signal Processor is given in Figure 3.2-4.

The 400 Hz output signal from each rate gyro is demodulated to generate a dc voltage which is proportional to the rate output of the gyro. A telemetry output from each demodulator is provided.

Two of the three demodulated outputs (of one channel) are compared within a comparison circuit,

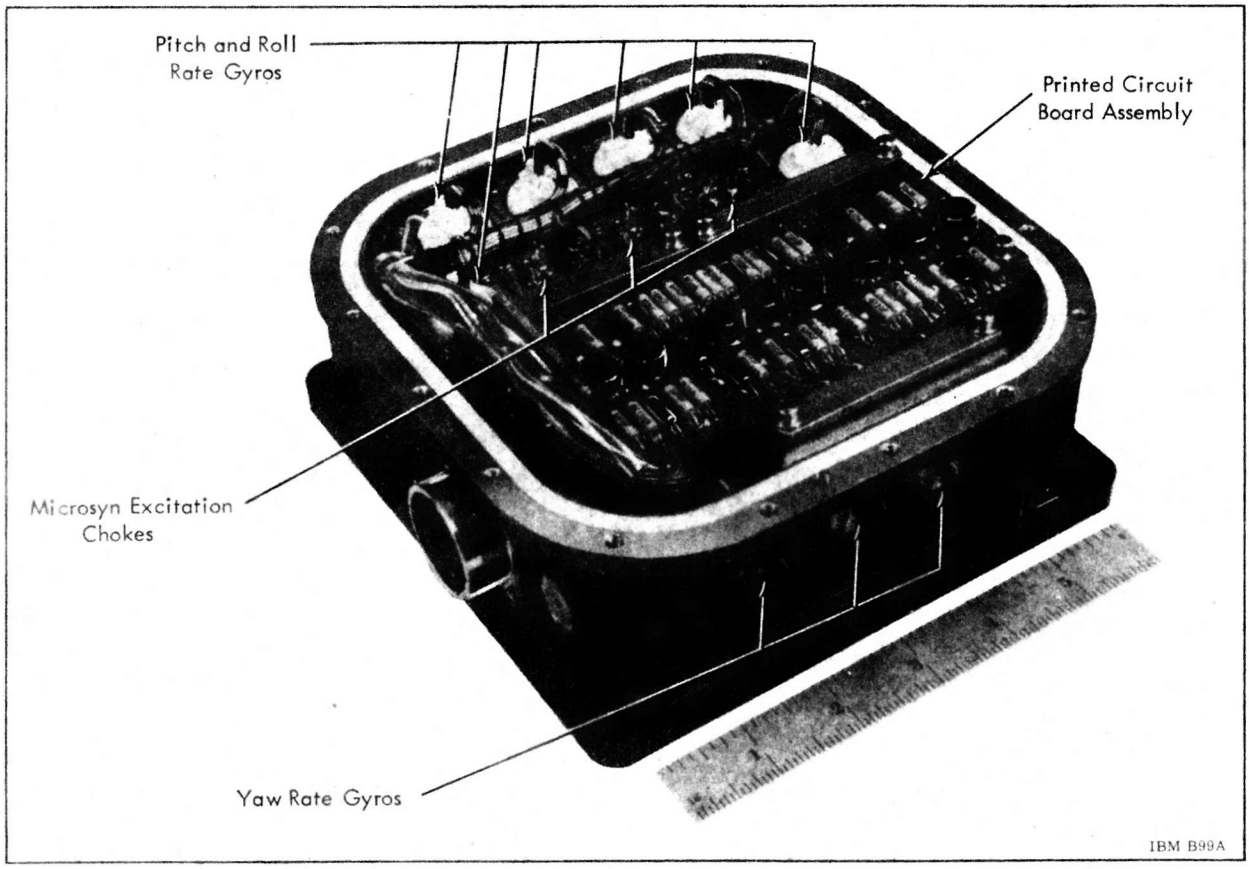


Figure 3.2-2 Control-EDS Rate Gyro Package with Covers Removed

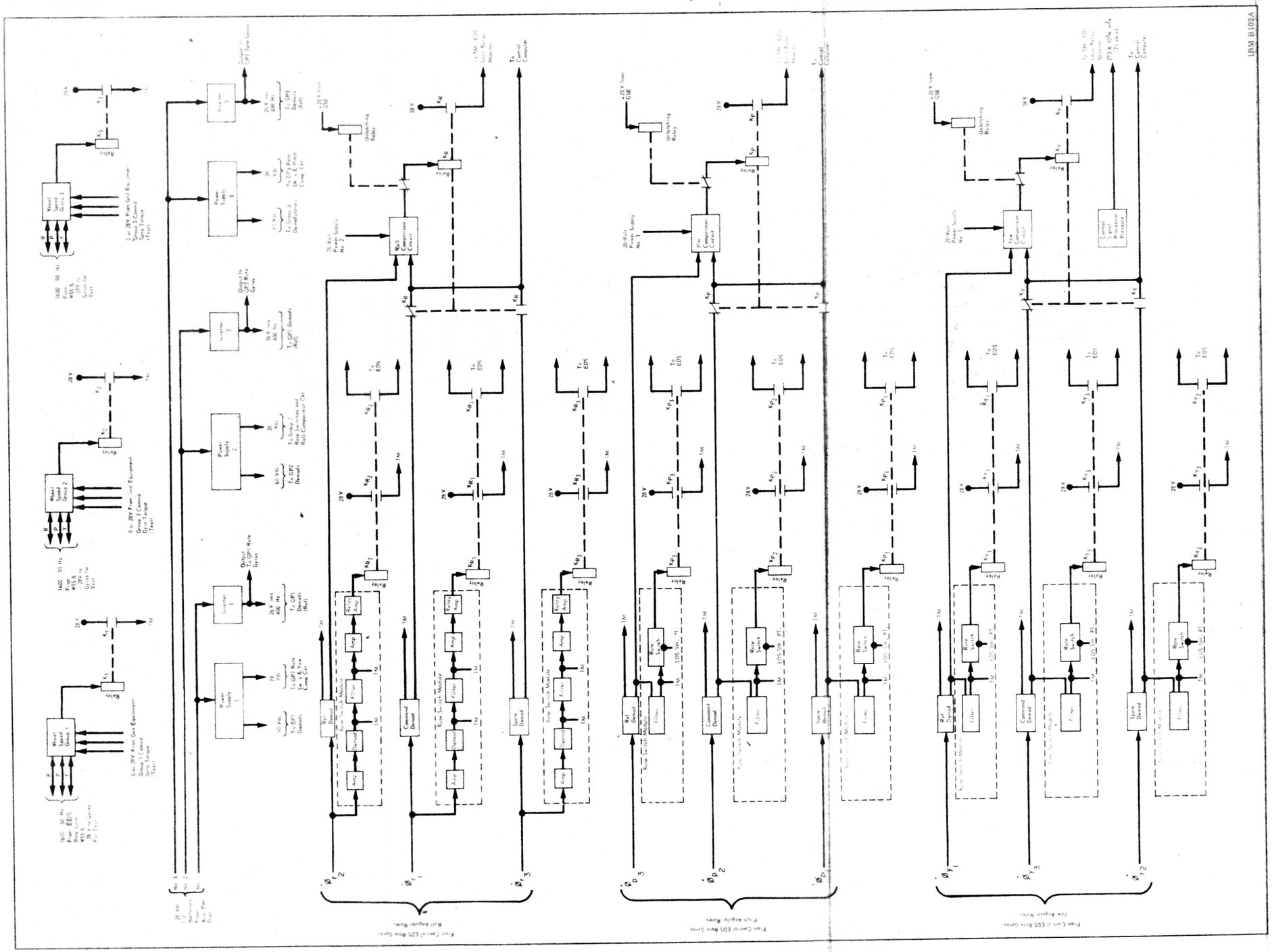


Figure 3.2-4 Control Signal Processor Block Diagram

and when the dc output of the two compared demodulators differs by a preset amount, a relay selects the output of the spare demodulator as the input to the Flight Control Computer. The relay remains in this position until reset by an external command signal. Closure of the relay is indicated by a telemetry output. The dc outputs (0 - 45 volts) of each channel are used as inputs to the Flight Control Computer.

Each rate switch receives the 400 Hz output signal from one gyro and energizes a relay when the amplitude of the signal exceeds the predetermined magnitude. This relay generates an EDS signal which is indicated by the telemetry.

The angular velocities of the gyro rotors are measured by wheel speed sensor circuits which provide outputs to telemetry for monitoring purposes. The input signals to each speed sensor are frequencies proportional to the angular velocity of the gyro rotors. If the frequency of any one input deviates more than ± 50 Hz, the wheel speed sensor will generate a discrete signal for telemetry indicating gyro overspeed or underspeed conditions.

The Control Signal Processor contains three power supplies operating from three separate 28-volt batteries. Each power supply provides 60 Vdc for one roll, yaw, and pitch demodulator, and 28 Vdc for the comparison circuit and one roll, yaw, and pitch rate switch.

Three static inverters, also located in the Control Signal Processor, operate from unregulated battery power to generate closely regulated 26 Vac (400 Hz) signals. Each inverter provides motor and microsyn power to one roll, yaw, and pitch rate gyro, and a reference excitation to one roll, yaw, and pitch demodulator.

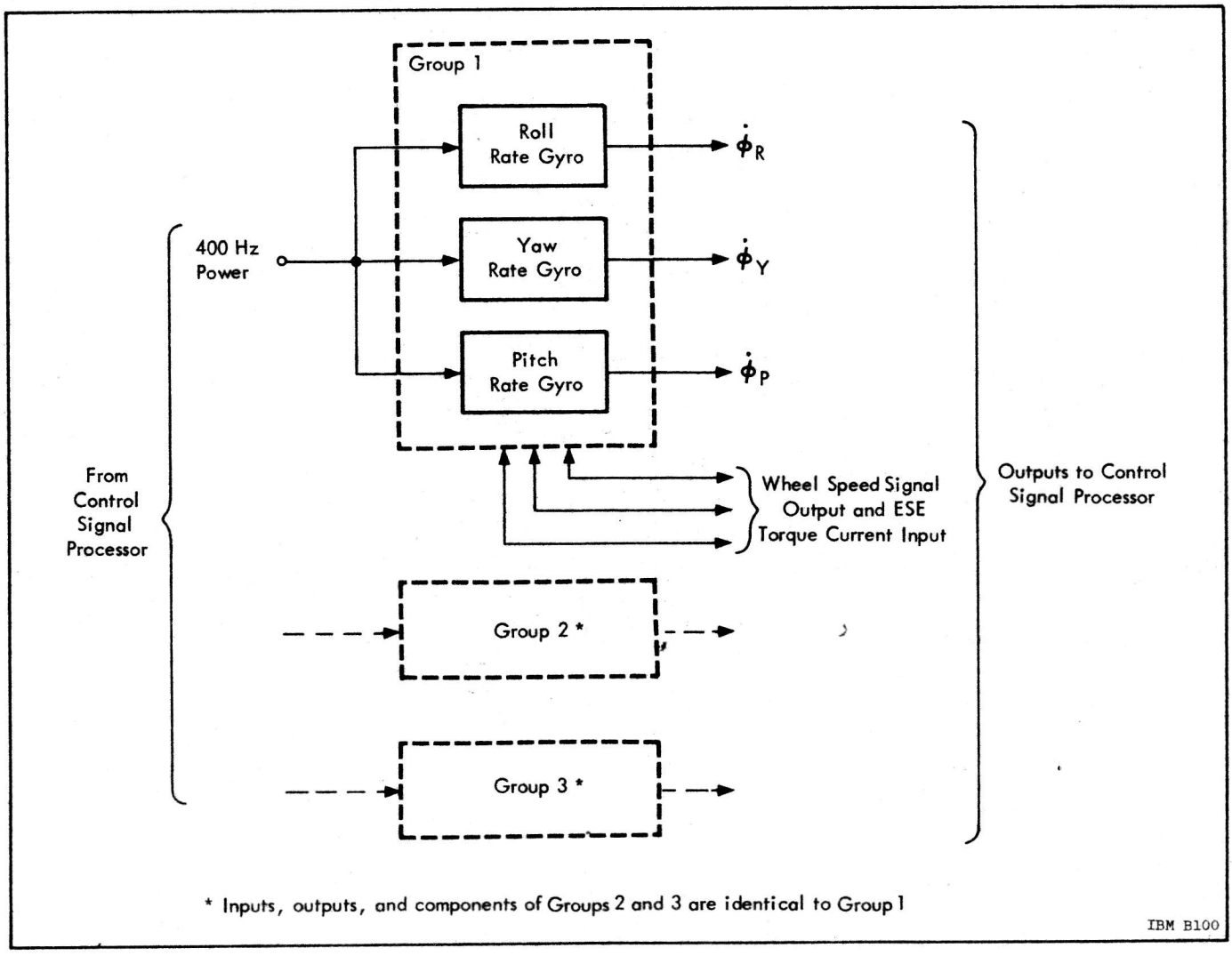


Figure 3.2-3 Control-EDS Rate Gyro Package Block Diagram

3.2.4 CONTROL ACCELEROMETER

Two Control Accelerometers are used during first stage burn on the Saturn IB Vehicles. They are used to sense the lateral acceleration of the vehicle (perpendicular to its longitudinal axis) in the pitch and yaw planes. The output of these instruments is used in the control system to reduce structural loading and to control vehicle deflection due to the lateral winds.

The Control Accelerometer is a linear, spring-mass, fluid damped system with an inductive pickoff. Its excitation is from a self-contained static inverter which converts the 28-volt dc input voltage to a 400-hertz ac voltage (see Figure 3.2-5). The ac output of the accelerometer sensor is proportional to the applied acceleration in its sensitive axis. This output signal is amplified and demodulated within the assembly to produce a dc output voltage proportional to acceleration. This output is fed to the Flight Control Computer.

The heart of the accelerometer is its spring-mass system. The seismic mass is supported and restrained by a non-pendulous spring suspension system. The springs constrain the mass to pure translational motion with practically no friction and provide extremely low cross-axis sensitivity at the same time.

The spring-mass system is fluid dampened with a silicone fluid. As the accelerometer is subjected to acceleration, the mass moves with respect to the case and causes a positive displacement of the fluid with a resultant damping action. In addition to this effect, the damping fluid provides resistance to shock and vibration. A change in fluid volume with any temperature change is compensated for by an internal bellows.

A special feature of these accelerometers is their self-checking capability. By exciting a separate electromagnetic coil (force coil), it is possible to deflect the seismic mass by a calibrated amount and thus check the electrical output of the instrument without subjecting it to acceleration. This provides a means of remotely checking the accelerometers after their installation on the vehicle to ensure proper operation before flight. Table 3.2-1 lists the accelerometer characteristics.

Table 3.2-1 Control Accelerometer Characteristics

Measuring range	0 to ±10 m/s^2
Natural frequency	8 ±1.5 Hz
Damping ratio	0.8 ±0.2 of critical
Cross axis sensitivity	0.002 g/g
Scale factor	1.0 Vdc/m/s^2
Power	15 watts maximum (not including heaters)

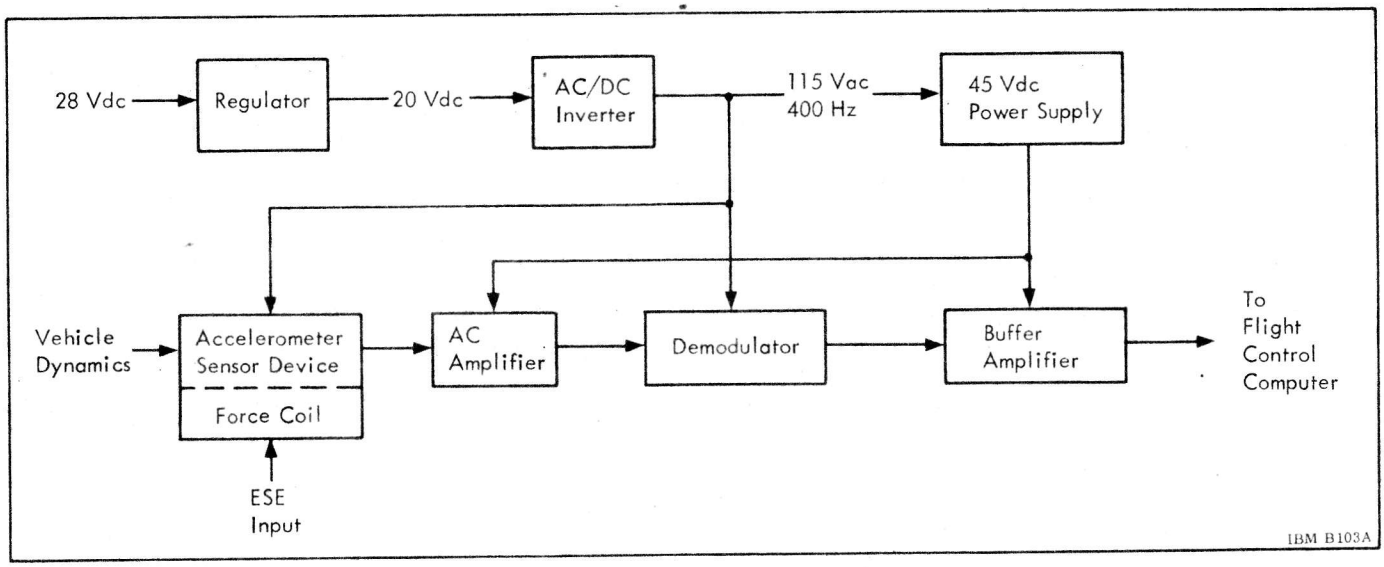


Figure 3.2-5 Control Accelerometer Block Diagram

SECTION 3.3
FLIGHT CONTROL COMPUTER

3.3.1 GENERAL

The Flight Control Computer is an analog device which generates the proper control commands for the engine actuators and the S-IVB auxiliary propulsion system. The computer accomplishes this by processing and combining the analog signals from the LVDA, control sensors, and Apollo Spacecraft.

The Flight Control Computer is equipped with eight input channels to accept eight different control signals listed in Table 3.3-1. The essential elements of the Flight Control Computer (for powered flight operation) are shown in the simplified block diagram, Figure 3.3-1. Signal line filters provide the proper time-variable adjustment of the a_0 and a_1 gain factors in the Saturn IB V control laws expressed in equations 3.1-1 and 3.1-2. The Control Attenuation Timer (CAT) is used in the Saturn IB Flight Control Computer to provide the required time-variable adjustment of the g_2 gain factor in the Saturn IB control law.

The signals processed are then summed and amplified by either servo or spatial amplifiers. These signals are the control signals for the engine servo actuators which control the thrust vector deflection angle.

The Flight Control Computer also generates the control signals for operation of the S-IVB auxiliary propulsion system which provides roll control during S-IVB powered flight and complete attitude control during coast flight. A simplified diagram of the Flight Control Computer configuration during coast flight is given in Figure 3.3-2. The attitude error signal (ψ) is provided by the LVDC/LVDA or the Apollo Spacecraft. Signals from the spacecraft are limited in the Flight Control Computer while the signals supplied by the LVDA have been limited in the LVDC/LVDA. Angular rate signals ($\dot{\phi}$) are obtained from the Control-EDS Rate Gyros in the IU. The spatial amplifiers generate the control signals (ON-OFF) for the auxiliary propulsion system attitude control engines.

The Saturn V and the Saturn IB Flight Control Computers are designed according to the same general scheme. The configurations of both computers, however, are somewhat different for the powered flight phases since the Saturn V is a 3-stage vehicle while Saturn IB is a 2-stage vehicle. See paragraph 3.3.2. Both types of computers have the same configuration for S-IVB powered flight attitude control and coast flight attitude control.

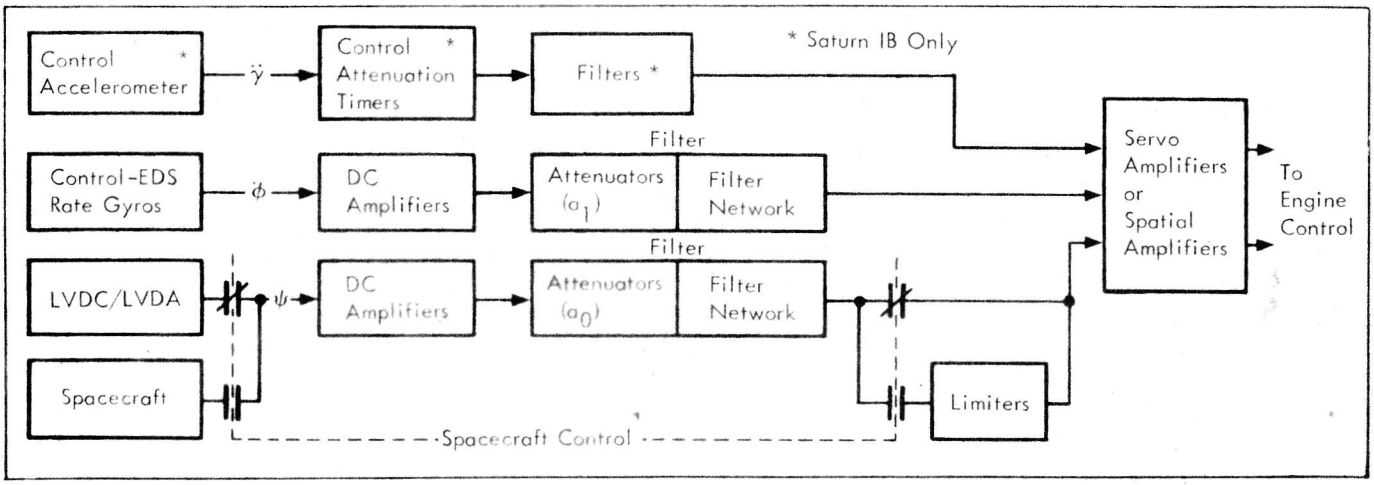


Figure 3.3-1 Simplified Diagram of the Flight Control Computer for Powered Flight

3.3.2 FLIGHT CONTROL COMPUTER OPERATION DURING POWERED FLIGHT

The Saturn IB Flight Control Computer differs from the Saturn V Flight Control Computer in several areas.

The Saturn IB Flight Control Computer contains a channel for Control Accelerometer signals (for first-stage powered flight). One type of servo amplifier is used to control the engine actuators of the S-IB Stage. Another type of servo amplifier (the same used in Saturn V) controls the S-IVB engine actuators. The engine actuator control loops for the S-IB Stage use electrical feedback. The computer contains amplifiers, filters, and the necessary switching devices for two vehicle stages.

The Saturn V Flight Control Computer has no channels for Control Accelerometer signals. The same type of servo amplifier is used to control the engine actuators in each stage (S-IC, S-II, and S-IVB). The computer contains amplifiers, filters, and the corresponding switching relays for three vehicle stages. The control loops for the engine actuators use mechanical feedback.

Table 3.3-1 Input Signals to the Flight Control Computer

Input Channel	Symbol	Gain* Factor	Signal Sources
Lateral Acceleration			
Pitch	$\ddot{\gamma}_P$	g_2	Saturn IB Control Accelerometers
Yaw	$\ddot{\gamma}_Y$		
Angular Rate			
Pitch	$\dot{\phi}_P$	a_1	Control-EDS Rate Gyros
Yaw	$\dot{\phi}_Y$		
Roll	$\dot{\phi}_R$		
Attitude Error			
Pitch	ψ_P	a_0	LVDA/LVDC or Spacecraft
Yaw	ψ_Y		
Roll	ψ_R		

* Time-varying functions that determine which of the three terms of the control equation will be dominant. The control equation is defined as: $\beta_c = a_0 \psi + a_1 \dot{\phi}$ ($+ g_2 \ddot{\gamma}$ for Saturn IB)

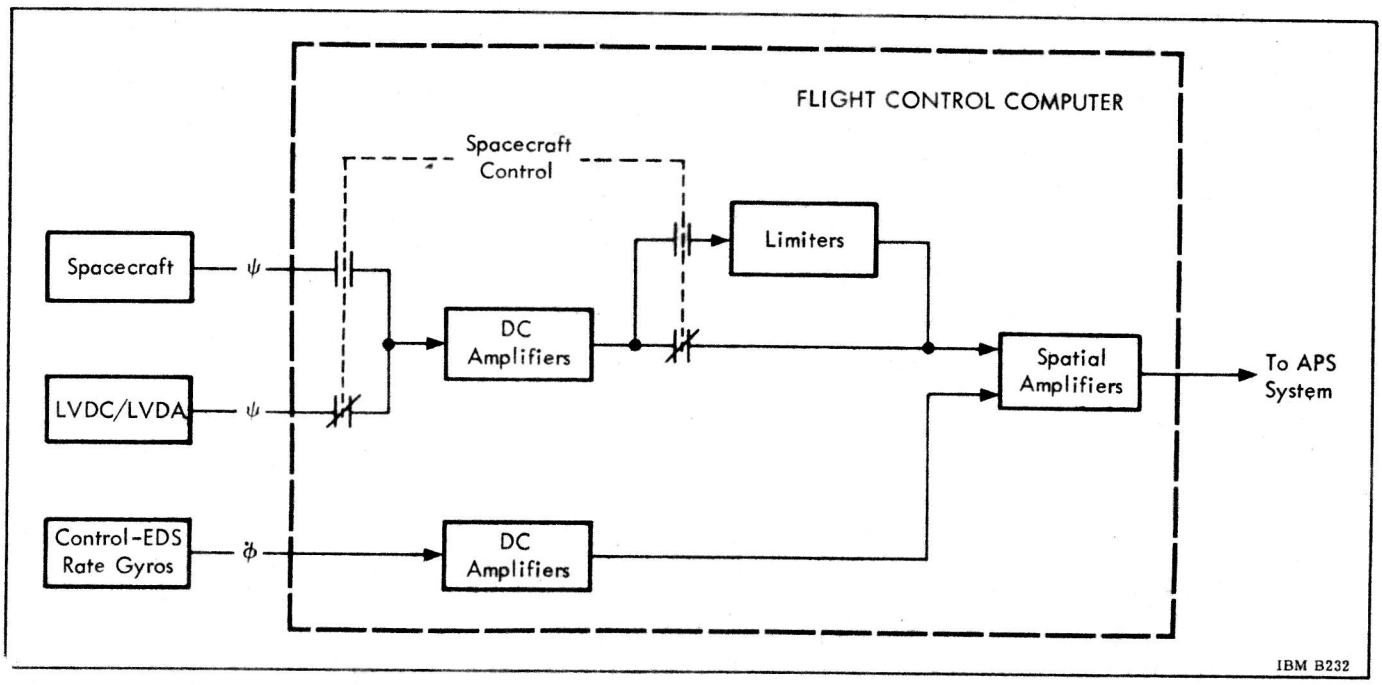


Figure 3.3-2 Simplified Diagram of the Flight Control Computer for Coast Flight

SATURN IB FLIGHT CONTROL COMPUTER

Figure 3.3-3 is a block diagram of the Saturn IB Flight Control Computer. During first-stage powered flight, each input signal to the computer passes through a dc amplifier and filter before it enters the servo amplifiers.

Attenuation (gain control) is accomplished by either of two methods: by motor-driven, cam-controlled potentiometers called Control Attenuation Timers (CAT's) or relay-switched, fixed-resistor networks. The CAT's provide attenuation that varies continuously as a function of time, while the relay-switched resistor networks change attenuation in discrete steps at predetermined time intervals. These relays are commanded by signals from the LVDC/LVDA via the IU Switch Selector and are often referred to as "switchpoints". Each filter block shown in the figure represents a relay-resistor (attenuator) network and its associated filter network. A different set of attenuators and filters is used during the S-IVB powered flight phases since the dynamic characteristic of the vehicle is changed after separation of the S-IB Stage and aerodynamic forces no longer exist. The required filters for each stage are selected by relays according to the flight program. No filters are used for operation of the S-IVB auxiliary propulsion system (during coast flight and for roll control during powered flight). The actual filter networks are passive RLC networks which provide gain and phase stabilization in the control loop to prevent undesirable signal frequencies from affecting the attitude control.

In the CAT device, a rocker arm drives two coupled potentiometers which are electrically connected to the appropriate channels. The outputs from the potentiometers are time-varying functions of the input signals; i.e., the $\ddot{\gamma}$ signal inputs to the attenuator appear at the attenuator output modified by g_2. The cam is driven by a 115V, 400-cycle, single-phase, synchronous motor. The cam speed is determined by a gear train arrangement.

A typical Saturn IB time program for a_0, a_1, and g_2 is shown in Figure 3.3-4. The gain factor (g_2) has a maximum value during the time period of high aerodynamic pressure, thus emphasizing the lateral acceleration control signals. These Control Accelerometer signals are used during the S-IB flight phase only. The gain coefficients (g_2) for Control Accelerometer signals are varied by CAT circuits. The other gain factors (a_0 and a_1) are changed by relay switching of resistors.

The Flight Control Computer contains eight servo amplifiers for the actuators of the S-IB Stage and six servo amplifiers for the actuators of the S-IVB Stage. The servo amplifiers are magnetic amplifiers which sum and amplify the filtered and scaled control signals to generate the control signals for the engine actuators. The output stage of the amplifier can provide up to 12 milliamperes (S-IB) or 50 milliamperes (S-IVB) of current to the torque motor-operated control valve of each hydraulic servo actuator. A portion of this output current is returned through a feedback network to provide required accuracy in gain and linearity.

There is one servo amplifier for each engine actuator in the S-IB Stage (i.e., four pitch servo amplifiers and four yaw servo amplifiers). The three yaw output control signals (ψ_Y $\dot{\phi}_Y$ $\ddot{\gamma}_Y$) to the Flight Control Computer are fed into each of the four yaw amplifiers. Correspondingly, the three pitch input channels are connected to each of the four pitch amplifiers. The two roll input signals (ψ_R and ϕ_R) are sent to all eight S-IB servo amplifiers since it is necessary to deflect the engines in pitch and yaw simultaneously for execution of a roll maneuver.

The six servo amplifiers for the S-IVB powered flight are used in a triple redundant configuration to control the two servo actuators of the single J-2 engine. The output signals of two yaw servo amplifiers are compared, and if they agree, one is used to control the yaw actuator. If those two signals disagree, the output of the third yaw servo amplifier is switched to the actuator. The same scheme applies to the pitch channel.

To achieve APS thruster synchronization of roll control during S-IVB powered flight, the output signal of the yaw-roll I spatial amplifier configuration feeds both control relay packages. Although not shown in Figure 3.3-3, the yaw-roll II signals are interrupted during this period and will not be used until the coast flight control operation.

SATURN V FLIGHT CONTROL COMPUTER

Figure 3.3-5 is a block diagram of the Saturn V Flight Control Computer. The attitude error sig-

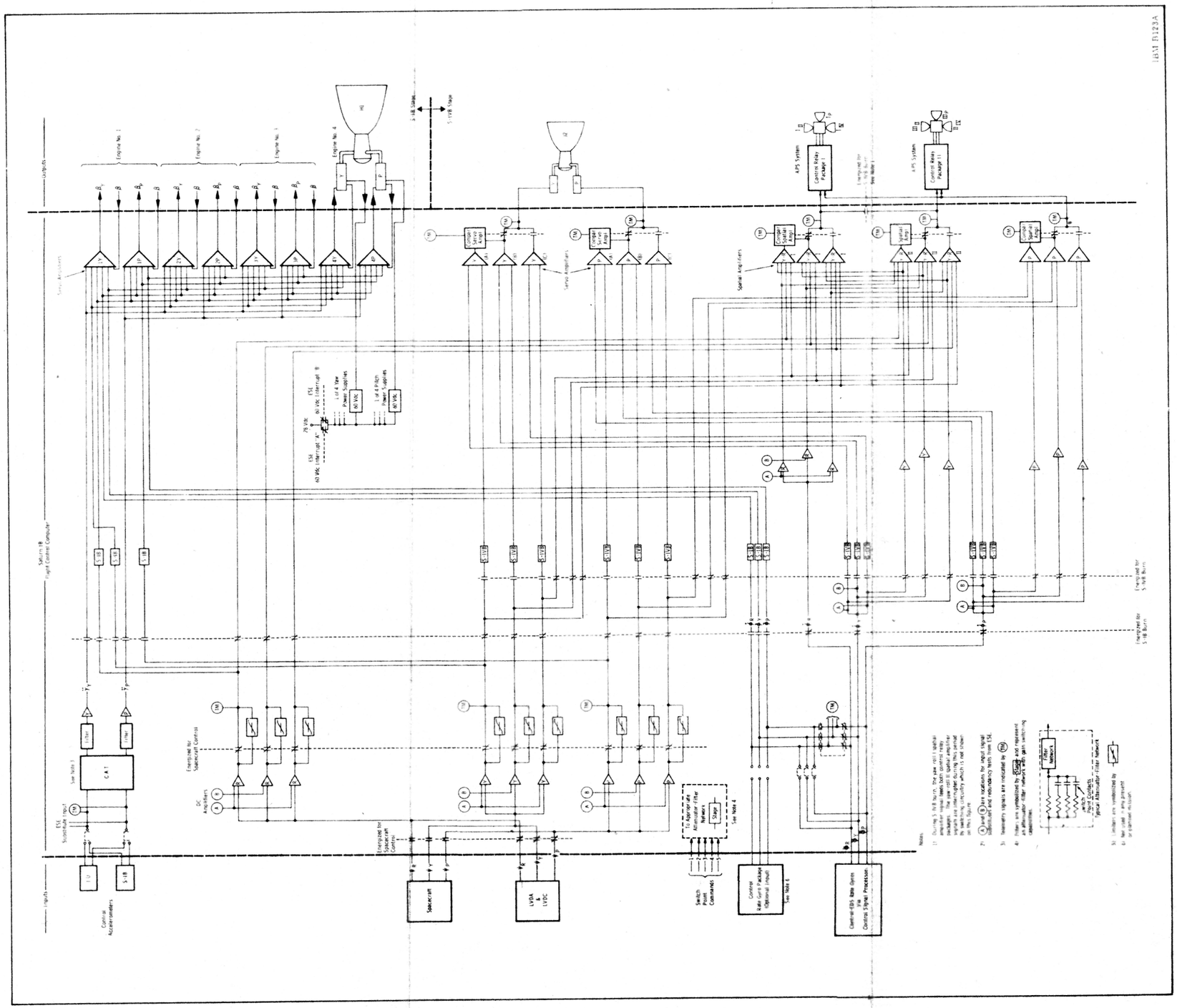


Figure 3.3-3 Saturn IB Flight Control Computer Block Diagram

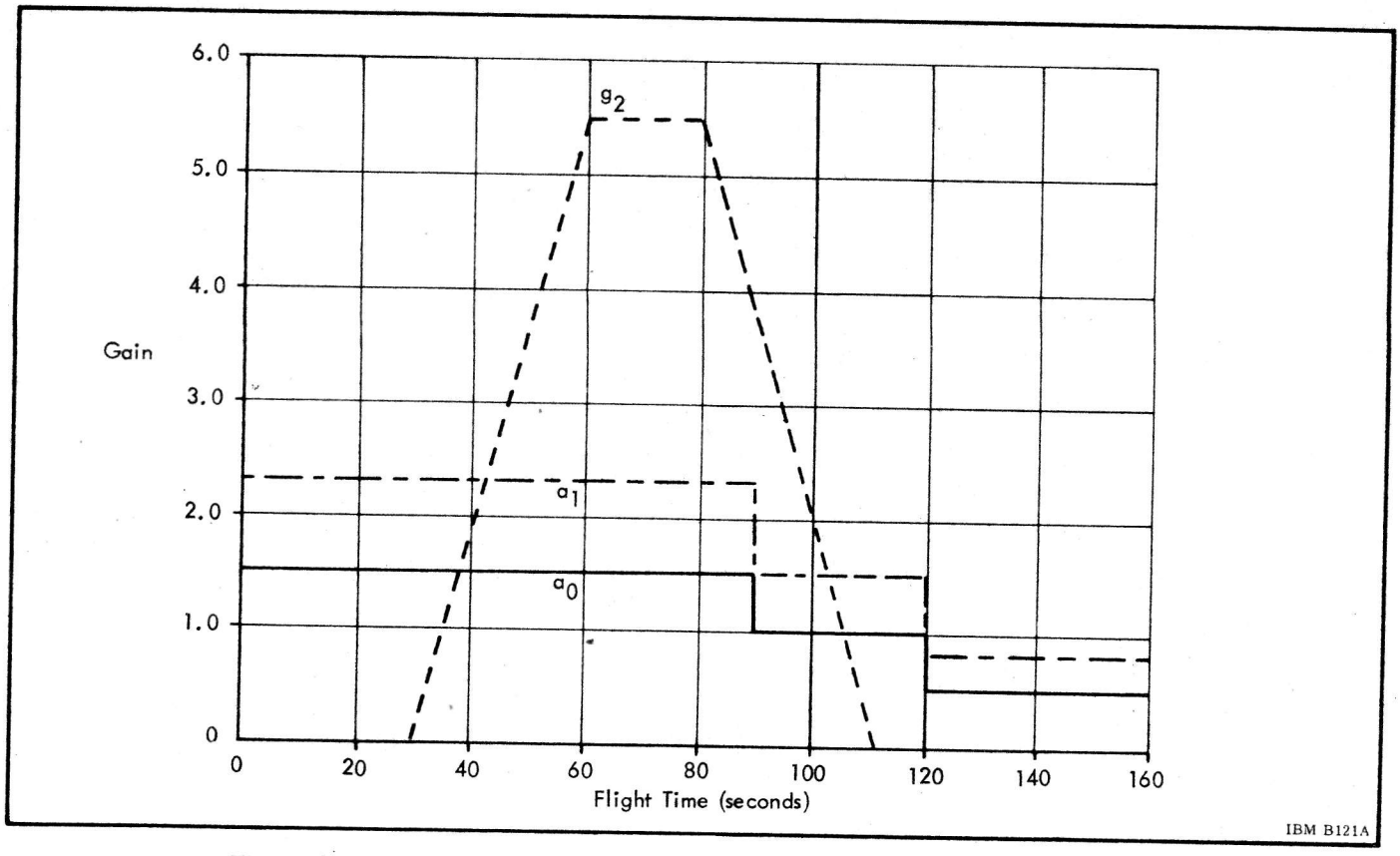


Figure 3.3-4 Typical Saturn IB Gain Program for a_0, a_1, g_2 Coefficients

nals (ψ), originating either from the LVDA or the spacecraft, are switched by a quad redundant relay configuration to three scaling amplifiers in each of the three channels (yaw, pitch, and roll). A different set of filters is switched in for each powered flight phase (S-IC, S-II, S-IVB). As in the Saturn IB Flight Control Computer, filters provide the proper adjustment of the gain coefficients a_0 and a_1.

The attitude error signals and angular rate signals from the filters are summed in the magnetic servo amplifiers and the resulting signal is used to generate the actuator control signals. The Flight Control Computer contains eight servo amplifiers of the same type. Each amplifier provides a maximum output current of 50 milliamperes to torque the motor-operated control valves of the actuators (see Figure 3.3-6). Each servo amplifier controls one of the eight engine actuators in the S-IC Stage or S-II Stage.

The roll signals (ψ_R and $\dot{\phi}_R$) are distributed to all eight servo amplifiers. The yaw signals (ψ_Y and $\dot{\phi}_Y$) are connected to all four yaw servo amplifiers and the pitch signals (ψ_P and $\dot{\phi}_P$) are connected to all four pitch servo amplifiers. The switching of input signals, filters, and servo amplifiers in the Flight Control Computer is controlled by the LVDC/LVDA through Switch Selector circuitry. See Section 4.2. Since the S-IVB Stage has only two engine actuators, it should be noted that six of the eight servo amplifiers are used in a triple redundant arrangement. The control configuration for third-stage burn is otherwise similar to that described for the S-IVB powered flight phase of Saturn IB Flight Control Computer.

3.3.3 FLIGHT CONTROL COMPUTER OPERATION DURING COAST FLIGHT

The Flight Control Computer configurations of the Saturn IB and Saturn V are identical for coast flight attitude control (Figures 3.3-3 and 3.3-5).

No filters are contained in the signal channels (ψ and $\dot{\phi}$) of the APS. Attitude error signals (ψ) from the spacecraft are limited in the Flight Control Computer between the dc amplifiers and the spatial amplifiers. The limiter circuits provide roll, pitch, and yaw signal limiting and are switched into the circuit only during the spacecraft control mode of operation.

IBM B126A

Figure 3.3-5 Saturn V Flight Control Computer Block Diagram

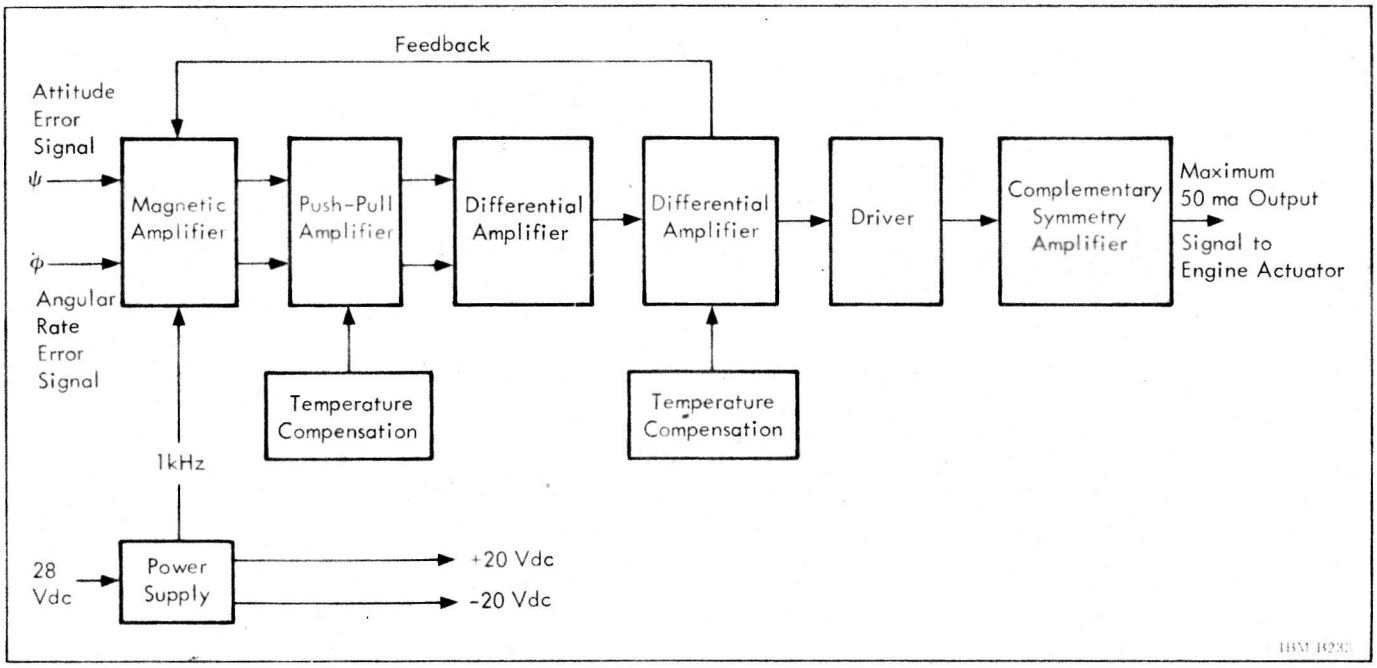


Figure 3.3-6 50-Milliampere Servo Amplifier Block Diagram

The signals from the dc amplifiers are sent directly to the spatial amplifiers. The spatial amplifiers sum the input signals (ψ and $\dot{\phi}$) and compare the resulting signal level with a predetermined threshold level. When the combined control signals exceed the limits set by the threshold, a switching amplifier energizes the relays in the control relay package, which in turn operates the valves of the proper attitude control engines.

The Flight Control Computer contains nine spatial amplifiers which are used in a triple redundant configuration (three spatial amplifiers for each pitch, yaw, and roll control). A comparator circuit selects 1 of 2 amplifiers out of the 3 triple-redundant amplifiers in each channel. The spatial amplifiers for pitch control switch either the (+) pitch or the (-) pitch nozzle ON. They require only the two input signals (ψ_P and $\dot{\phi}_P$). The remaining 2 groups of spatial amplifiers both control yaw and roll maneuvers. Each of these amplifiers receives roll and yaw input signals (ψ_R, ψ_Y, $\dot{\phi}_R$, $\dot{\phi}_Y$) since the same nozzles are used for yaw and roll control. The control relay package which operates the valve coils is discussed in Section 3.4.

The Saturn V Flight Control Computer includes a circuit designed to provide an outward engine cant of approximately 2 degrees for the four gimballed S-IC Stage engines. Since the stage is designed with no mechanical cant, an electrical substitute is provided. At approximately 20 seconds after lift-off, the IU Switch Selector issues a command to the Flight Control Computer via the IU Control Distributor. This signal is applied to a ramp generator which produces an output to the yaw and pitch servo amplifiers in order to cause each S-IC engine actuator to retract the amount necessary to produce the 2-degree cant.

3.3.4 REDUNDANCY IN THE FLIGHT CONTROL COMPUTER

The attitude rate signals ($\dot{\phi}$) and the attitude error signals (ψ) enter the Flight Control Computer via separate duplex lines. The duplex lines continue until they branch into the three scaling amplifiers as shown in Figure 3.3-7. (The switchover between attitude error signals from the LVDA or the spacecraft is accomplished by relays arranged in a quad redundant configuration.)

For the S-IVB powered flight and coast flight attitude control, the Flight Control Computer has a triple redundant configuration in each channel. For each of the six input control signals (ψ_P, ψ_Y, ψ_R, $\dot{\phi}_P$, $\dot{\phi}_Y$, $\dot{\phi}_R$), there are three redundant, completely independent channels. Each channel contains individual amplifiers, filters (if used), and relays. These triple redundant signal channels are connected to a triple redundant arrangement of servo amplifiers or spatial amplifiers. The outputs of two of the three triple redundant servo (or spatial) amplifiers are compared and, if they agree, one output is applied to the engine actuator (control relay package). If the compared signals do not agree, the output of the third servo (or spatial) amplifier is used.

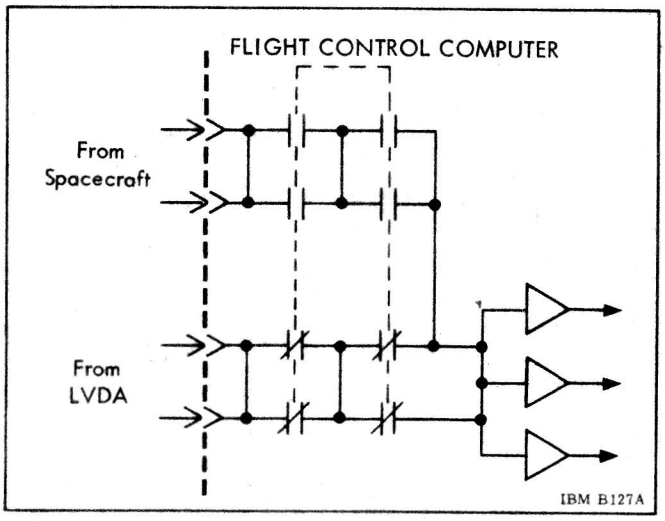


Figure 3.3-7 Redundant Cabling in the Flight Control Computer

SECTION 3.4
ENGINE CONTROLS

3.4.1 ENGINE SERVO ACTUATORS

The angular direction of the thrust vector of Saturn IB and V engines is controlled by swivelling the gimbal-mounted propulsion engines. This control is obtained by linear hydraulic servo-actuators in the pitch and yaw planes.

The actual arrangement of the actuators for the multi-engine stages and the single-engine S-IVB Stage of the Saturn Launch Vehicle is shown in Figure 3.4-1. Independent hydraulic systems for each gimbaled engine are used to provide the following advantages:

- Flight system can be qualified by single-engine test.
- One system can be verified at a time.
- Malfunction and replacement can be isolated to 1 system.
- Post flight performance comparisons are easily accomplished and problem areas are quickly isolated.
- Redundant capability.

For the multi-engine vehicle stages, the redundant capability is further increased by sizing the swivel range so that, despite the failure of one control engine, the remaining gimbaled engines can maintain satisfactory control. The failure modes may be:

- Loss of thrust (engine out).
- Loss of hydraulic pressure (hydraulic system failure).
- Any actuation malfunction caused by servo valve failure, failure in signal lines, or Flight Control Computer output stage.

During operation of the rocket engines in the S-IC and S-II Stages, the hydraulic power supply is provided by a hydraulic pump driven by the engine turbine and an accumulator-reservoir to cover peak loads. An auxiliary pump, driven by an electric motor, provides hydraulic pressure for static checkout of the hydraulic system.

For the first-stage engines, the hydraulic pressure is obtained directly from the fuel turbopump; as the fuel itself is used as the hydraulic fluid. The available low operating pressure requires a large servo valve and actuator piston area; however, the pressurization system is very simple and even the accumulator-reservoir can be omitted as a result of the almost unlimited availability of pressurized fuel.

The transformation of the electrical signal from the Flight Control Computer, which commands the angular deflection (β) of the engine into a linear displacement, is performed by servo actuator assemblies. The servo valves are four-way, flow-control devices, with internal dynamic pressure feedback and mechanical feedback of the actuator piston position. Figure 3.4-2 is a symbolic representation of the valve. The servo valve operates in the following manner. The error signal from the Flight Control Computer is applied to the torque motor coil which displaces the flapper valve and restricts the flow of hydraulic fluid in one branch (e.g., the left one in Figure 3.4-2). The increasing pressure in that branch drives the second stage power spool to the right, which in turn allows hydraulic pressure build up on the left side of the actuator piston, causing a linear displacement of the actuator to the right. The mechanical feedback linkage displacement places a counter torque on the flapper valve. When this feedback torque equals the applied torque from the servo valve torque motor, no further motion of the actuator can occur. The potentiometer measures the actuator position for telemetry purposes.

In the S-IB Stage servo actuators only, an electrical potentiometer is used as a feedback transducer. It applies a "β" feedback signal to the Flight Control Computer servo amplifier. The mechanical feedback provides higher reliability, which results primarily from the elimination of the feedback potentiometer and its associated wiring, connections, and power supply, and reduction in corresponding failure

modes. Further, the mechanical feedback has an important advantage in that the actuator goes to a null position ($\beta = 0$) if the "β" command signal from the Flight Control Computer fails in the zero level.

The characteristics of the hydraulic servo actuator systems are given in Table 3.4-1.

3.4.2 AUXILIARY PROPULSION SYSTEM

The APS system, shown in Figure 3.4-3, consists primarily of spatial amplifiers, control relay packages, and attitude control nozzles. The figure is not detailed since the APS system operation has been generally explained and illustrated in previous sections. The purpose of this section is to explain the design characteristics of the system and to examine component functions.

SPATIAL AMPLIFIERS

The Flight Control Computer contains 3 sets of triple-redundant spatial amplifiers. One set of amplifiers is used during S-IVB powered flight, and all three sets are used for coast flight control. For

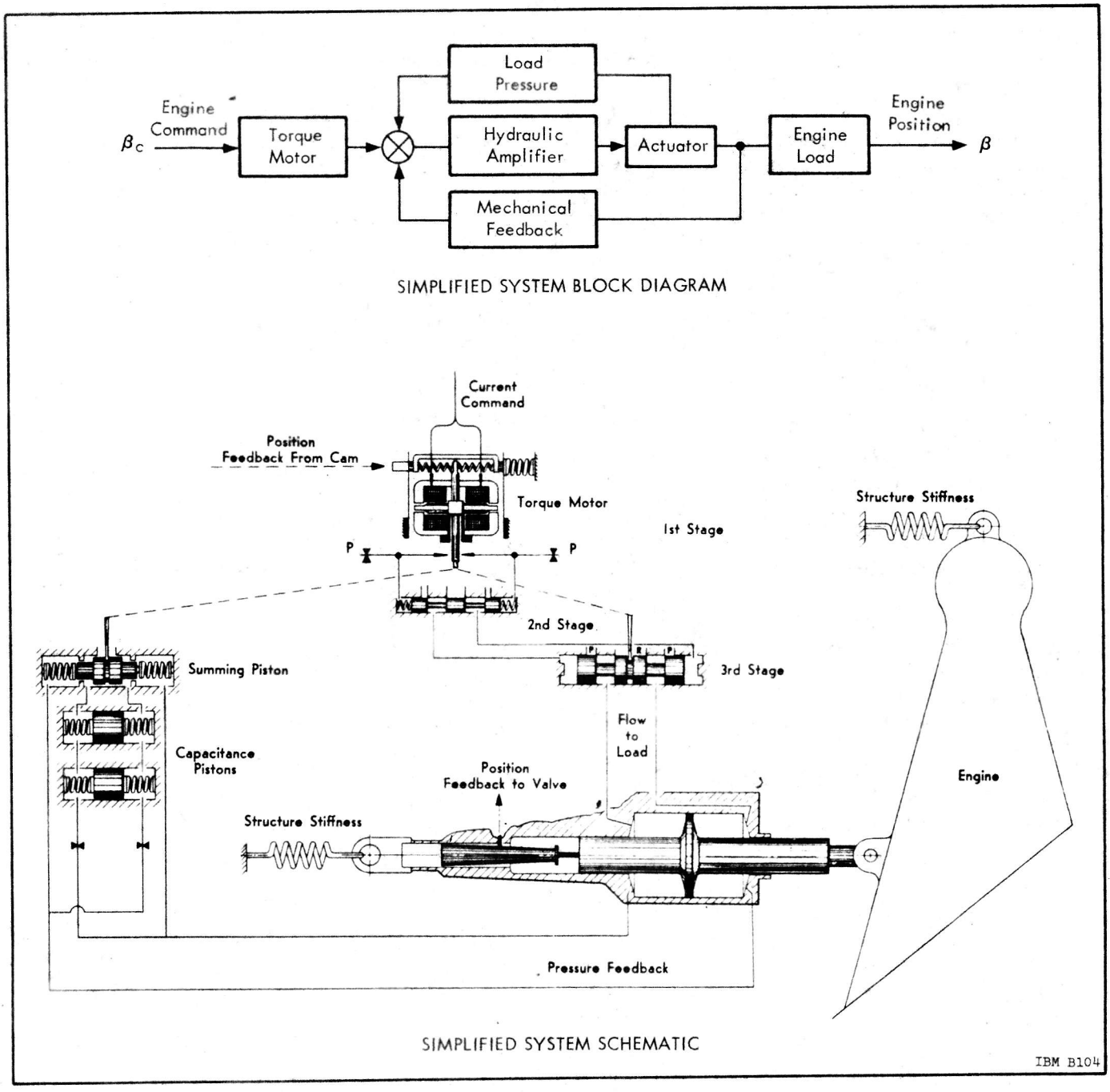


Figure 3.4-1 Hydraulic Actuator System

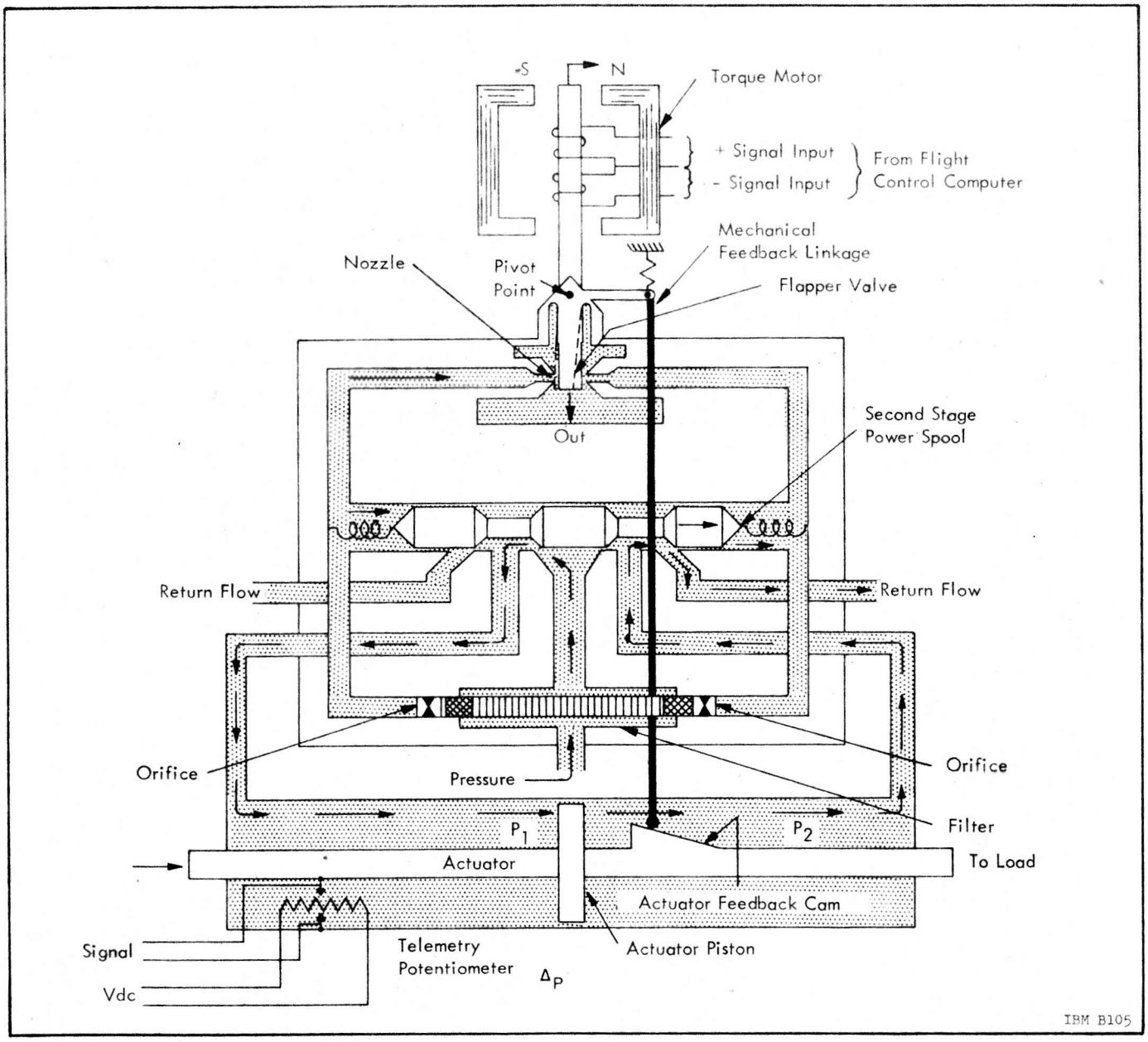


Figure 3.4-2 Flow-through Valve and Actuator with Mechanical Feedback

S-IVB powered flight, one set of spatial amplifiers (yaw-roll I) is used to feed both control relay packages. This scheme allows synchronized firing of the attitude control nozzles (thrusters) for roll attitude maneuvers during S-IVB powered flight. The signals for the other set of spatial amplifiers used in powered flight (yaw-roll II) are interrupted. The switching circuitry used to achieve this configuration is referred to as the "spatial synchronizer" and is located within the Flight Control Computer. During coast flight, the control relay packages operate independently so that yaw corrections can be made.

The purpose of these amplifiers is to develop ON-OFF control signals for the S-IVB thruster nozzles. The output signal is proportional (in duration) to the yaw, pitch, and roll error signals generated by the LVDC/LVDA or spacecraft. A block diagram of the spatial amplifier is shown in Figure 3.4-4.

Attitude and rate signals are applied to the magnetic amplifier where they are algebraically summed. The output signal of the magnetic amplifier is then amplified by 2 differential amplifier stages. Depending upon the amplitude and polarity of the signal, one of the two Schmitt triggers will change state. The triggered signal is then used to drive relays within the Control Relay Package in the S-IVB Stage. The relays transmit S-IVB Stage power to fuel and oxidizer solenoid valves of the commanded hypergolic engines.

Table 3.4-1 Servo Actuator Characteristics (Design Goals)

Parameter	S-IC F-1 Engine	S-II J-2 Engine	S-IVB J-2 Engine	S-IB H-1 Engine
Engine				
Moment Arm				
meters	1.620	0.301	0.295	0.699
inches	63.8	11.9	11.6	27.5
Moments of Inertia				
kg m^2	42,000	1,990	1,970	750
slug ft^2	56,760	2,690	2,660	1,015
Servo Actuator				
Piston Area cm^2	368	83.9	76	32.3
in^2	57	13	11.78	5
Stroke cm	29.2	7.7	7.4	9.7
inches	11.5	3.02	2.9	3.82
Supply Pressure				
N/cm^2	12.4×10^6 to 15.2×10^6	24.2×10^6	25.2×10^6	20.7×10^6
psig	1,800-2,200	3,500	3,650	3,000
Torque Motor Current				
ma	50	50	50	12
System				
Angular Deflection				
degrees	±5.15	±7	±7	±7.99
Angular Velocity				
deg/s	5	9.6	8.0	
Load Resonance	8.0	7.9	7.1	

The duration of the output control signal is determined by comparison of the input error signals (ψ and $\dot{\phi}$) and cutoff feedback signal. The greater the amplitude of the input signals, the longer time it will take the cutoff feedback signal to overcome the input error signals. This action results in proportionately longer duration output signals.

To this point, the discussion of the auxiliary propulsion system has been concerned with the pitch channel. The yaw and roll channels are similar in all details except that their combined error signals are mixed to ensure minimum fuel consumption. The yaw-roll mixing scheme is designed so that opposing engines will not fire simultaneously. The scheme also prevents one engine from adding to an error already existing in another channel.

Deadbands are introduced within the spatial amplifier circuit (and APS system in general) to conserve fuel and avoid "oversteering". In effect, a limiting tolerance is built into the system which will allow an attitude adjustment to be made by the APS system only if the adjustment is over a certain predetermined level. A typical roll deadband is shown in Figure 3.4-5.

The operation of the auxiliary propulsion system during coast phase is illustrated in Figure 3.4-6. The operation starts at point A, which represents a given attitude error (ψ) and attitude rate ($\dot{\phi}$) of the vehicle. The end state is the limit cycle within the deadband and about the commanded attitude angle.

CONTROL RELAY PACKAGE

Each control relay package consists of 12 miniature, double-pole, double-throw relays. Two such packages are used to control the S-IVB attitude control engine valve coils. These valve coils are an integral part of the engine and control the fuel and oxidizer poppet valves. The relays are driven in groups of eight from the three S-IVB attitude control

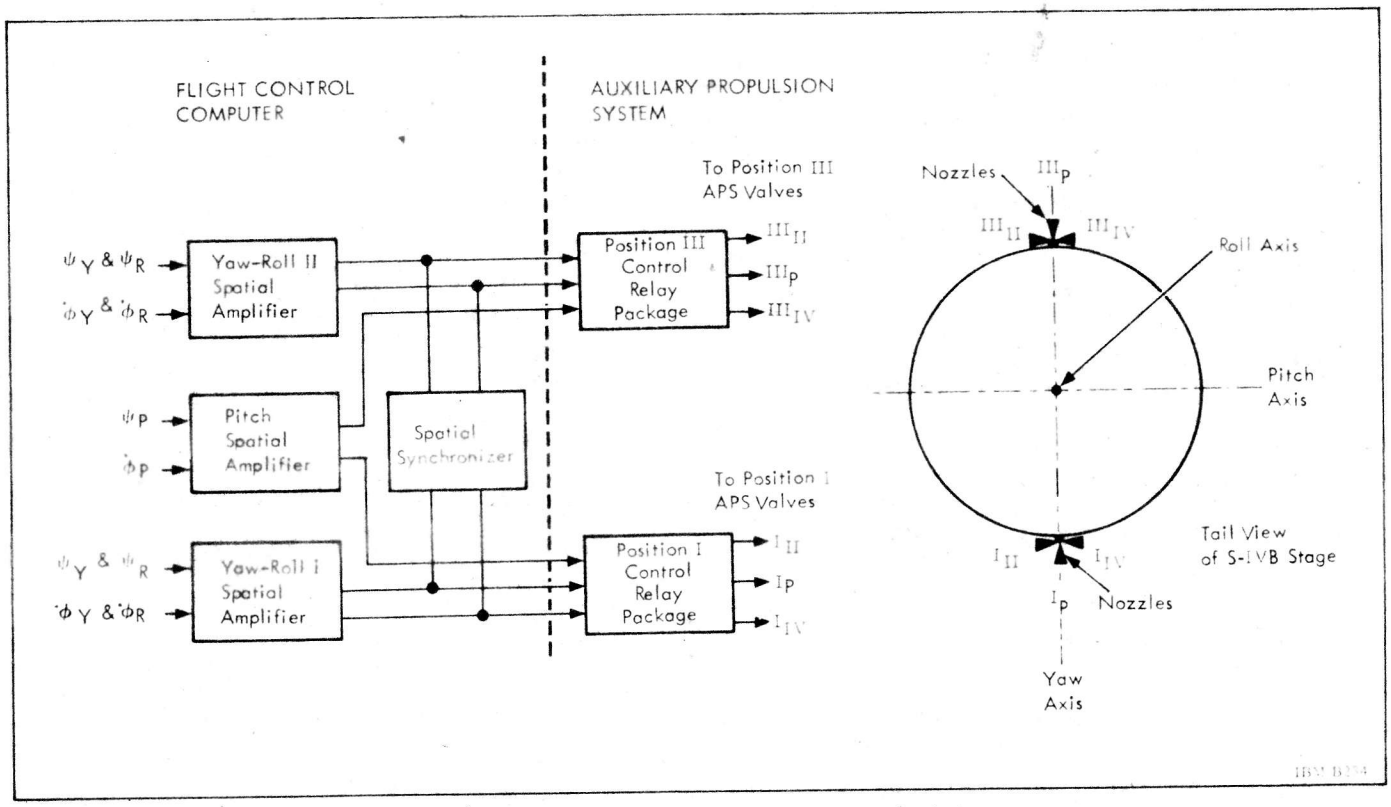


Figure 3.4-3 Auxiliary Propulsion System Block Diagram

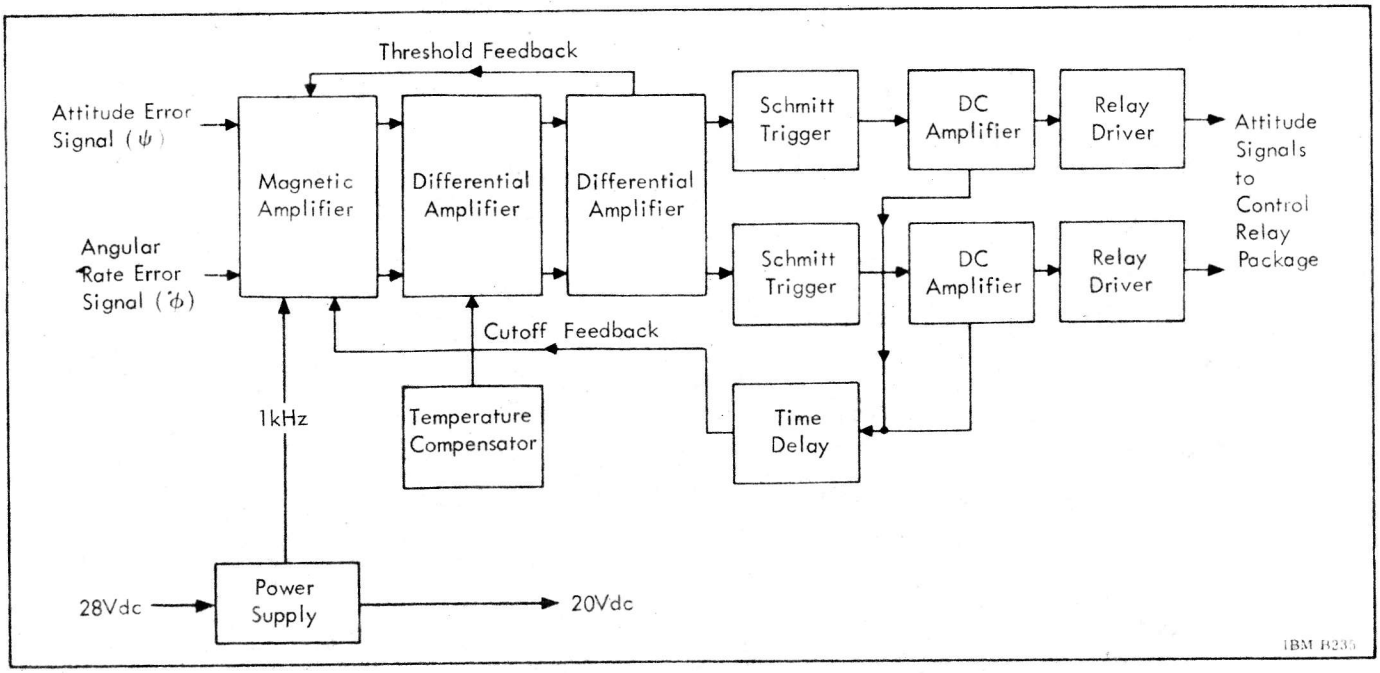


Figure 3.4-4 Spatial Amplifier Block Diagram

spatial amplifiers in the Flight Control Computer. Figure 3.4-7 shows the arrangement of the relays, valve coils, and fuel and oxidizer poppet valves associated with 1 amplifier in the pitch or yaw-roll axis.

As an example, if the attitude control signal requires that nozzle I_{II} be turned ON, the spatial amplifier energizes relay coils K1 through K4, which close the associated contacts (1, 1', etc.). Valve coils 1, 1', etc., are energized and open fuel valves 1, 2, 3, and 4 and oxidizer valves 1', 2', 3', and 4' in the quad valve network. This turns on nozzle I_{II}.

The control relay package was designed to take advantage of the redundant valve configuration by providing failure isolation from the predominant modes of relay failure (open-circuited coils, failure-to-make contacts, and welded contacts). This relay redundancy can be shown by considering relay 1 as an example. When relay coil K1 is energized, it closes contacts 1 and 1', which energize valve coils 1 and 1' and cause fuel valve 1 and oxidizer valve 1' to open. An open in coil K1 or a failure of contacts 1 and 1' to close results in no operation of fuel valve 1 and oxidizer valve 1'. However, this does not cause a failure

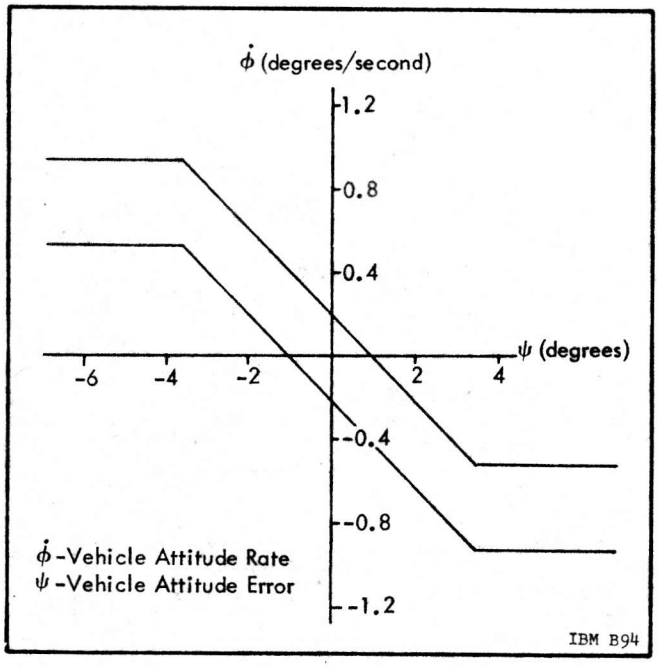


Figure 3.4-5 Typical Roll Deadband for S-IVB Auxiliary Propulsion System

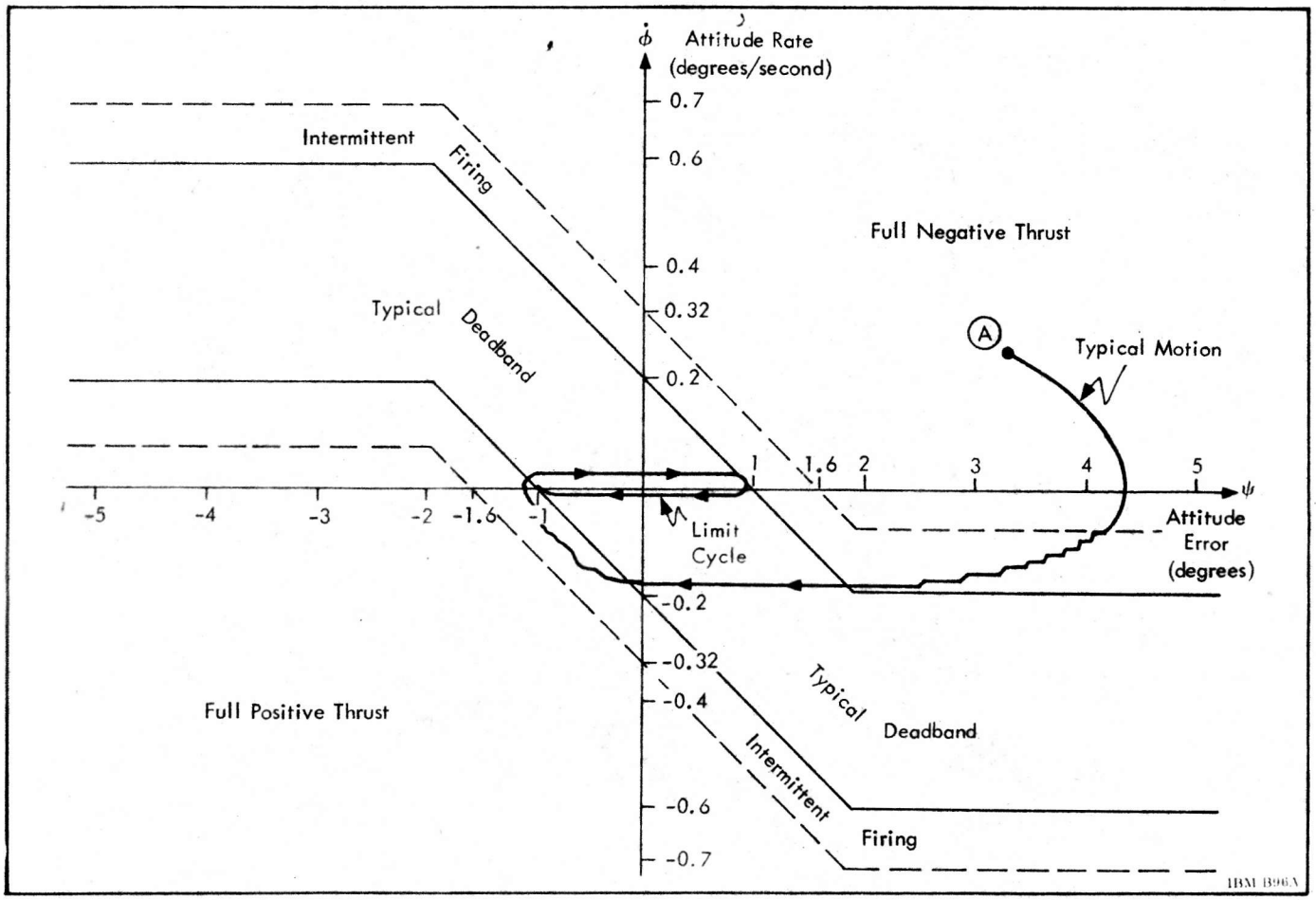


Figure 3.4-6 Typical Coast Phase APS Operation

of the attitude control system, since the redundant valves provide an operative flow path through valves 2-4 and 2'-4'. If, on the other hand, either or both sets of contacts of relay 1 should weld, or otherwise become permanently closed, fuel valve 1 and oxidizer valve 1' would be open. However, control of fuel and oxidizer would be maintained by valves 3 and 3', respectively.

Reliability predictions have shown that 85 percent of relay coil failures are due to an open coil, and 93 percent of contact failures are due to failure to close. The design of the control relay package isolates the control system from these predominate failures, as well as from welded-contact failures.

The control relay package was introduced into the design of the S-IVB Stage attitude control system to improve the interstage cabling design between the IU Flight Control Computer and the S-IVB Stage valve coils by reducing the current requirements from 12 amperes to 200 milliamperes. Therefore, the control relay package saves about 100 pounds of cabling and reduces the Flight Control Computer spatial amplifier's power requirements by switching the power to the valve coils in the S-IVB Stage.

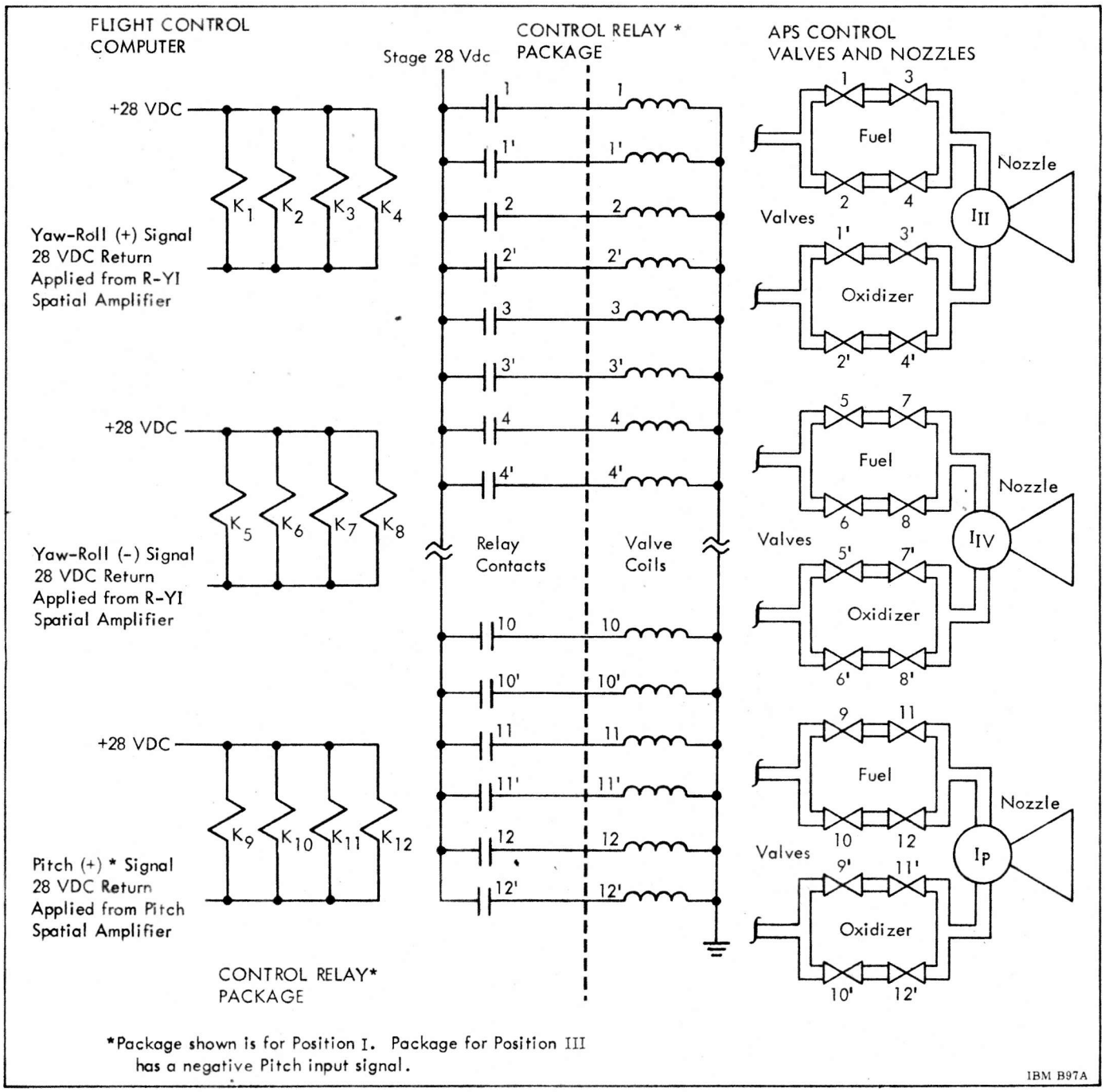


Figure 3.4-7 Control Relay Unit and Quad-Redundant Valves

CHAPTER 4
MODE AND SEQUENCE CONTROL

SECTION 4.1
INTRODUCTION

The terms mode and sequence control will be defined to explain their relationship with the Astrionics System. The LVDC memory contains a predetermined number of sets of instructions which, when initiated, induce the entire Astrionics System, or portions of the system, to operate in a particular mode. An example of a mode operation is the solving of guidance equations with interlaced attitude control and sequencing commands during the first stage flight. Each mode consists of a predetermined sequence of events. The computer also generates the appropriate control signals (e.g., engine cutoff and ignition, stage separation). Such a predetermined sequence of events is initiated by commanding the computer to operate in a particular mode.

Mode selection and initiation is accomplished through one of 3 actions: the successful completion of a previous mode, computer switching to a new mode based on real time, or an event occurrence. In addition to these internal mode selections which the system makes, mode switching is also accomplished by commands from the ground checkout equipment (before launch), the IU command system, or the Apollo Spacecraft. A built-in safeguard feature gives the system the capability of refusing conflicting commands or commands that would be detrimental to vehicle safety.

Examples of modes of operation that occur during flight in the Astrionics System are:

- First-stage guidance, control, and sequencing.
- Second-stage guidance, control, and sequencing.
- Third-stage guidance, control, and sequencing.
- Orbital operations —

  Vehicle attitude stabilization commanded by the IU.

  Spacecraft command of the vehicle attitude.

- Guidance, control, and sequencing of the third stage (second burn) into lunar trajectory —

  Using the IU navigation, guidance, and control system.

  Using the spacecraft navigation, guidance, and control system.

- Control of stage sequence functions from ground stations through the IU command system (emergency mode).
- Insertion of data into the LVDC through the IU command system.

The mode and sequence control scheme is very flexible since changes of modes and flight sequences are made by changing the instructions and programs in the LVDC memory, rather than by hardware modifications. The equipment involved in mode and sequence control of the launch vehicle is indicated in Figure 4.2-1. The LVDC issues flight sequence commands through the LVDA to the Switch Selector of the particular stage where the command must be executed. The Switch Selector of the addressed stage activates the appropriate circuit to perform the commanded function (e.g., engine cutoff, power ON or OFF). The Switch Selector operation is discussed in Section 4.2.

Mode commands from the spacecraft to the LVDA change the operational mode of the IU guidance and control system. When the Astronaut wants to control the attitude of the vehicle during coast flight, in

orbit, and after translunar injection, he initiates the proper mode command to the LVDA. The mode command is processed by the LVDA and LVDC, and the necessary sequence signals are generated to allow attitude control signals from the spacecraft to feed into the IU Flight Control Computer. Control is returned to the IU attitude control system when the Astronaut issues another mode command. In a similar manner, the back-up guidance mode may be selected. In this mode, the navigation and guidance system of the spacecraft guides the vehicle during powered flight.

During coast flight, the IU command system may be used to command mode changes from the ground.

Before launch, the ground checkout equipment exercises all operational modes of the Astrionics System. This includes simulated launch and orbit programs. The launch computer commands a particular mode of system operation by sending a coded command to the LVDA which "reads" it into the LVDC. The mode command is decoded, and the set of instructions or program, which is defined by the decoded mode command, is selected from the LVDC memory. The LVDC then begins to execute (within itself or elsewhere in the system) the instructions in that mode program.

Some events of the flight sequence are controlled by "discrete" signals generated by the LVDC according to a time program. Other events of the flight sequence are initiated when a particular event has occurred. For example, a signal is sent to the IU indicating S-IC engine cutoff – the LVDC then sends a signal to shutdown the S-II recirculation system.

A new time base for the time-controlled program is initiated during operation as a result of certain flight events (e.g., at lift-off, by the actuation of the first stage propellant level sensors, and S-IVB engine cutoff). A discrete signal is given to the LVDC as a reference for each time base.

SECTION 4.2
SWITCH SELECTOR

4.2.1 SYSTEM DESCRIPTION

Each stage, and the Instrument Unit, of the Saturn Launch Vehicle are equipped with a Switch Selector. The Switch Selector consists of electronic and electromechanical components which decode digital flight sequence commands from the LVDA/LVDC and activate the proper stage circuits to execute the commands.

Each Switch Selector can activate, one at a time, 112 different circuits in its stage. The selection of a particular stage Switch Selector is accomplished through the command code. Coding of flight sequence commands and decoding of the stage Switch Selectors reduces the number of interface lines between stages and increases the flexibility of the system with respect to timing and sequence. In the Saturn V Launch Vehicle, which contains 4 Switch Selectors, 448 different functions can be controlled using only 28 lines from the LVDA. (Two IU + 28-volt and two signal return lines from the Control Distributor are also used.) Flight sequence commands may be issued at time intervals of 100 milliseconds.

Figure 4.2-1 illustrates the Saturn V Switch Selector configuration. As shown, all Switch Selector control lines are connected through the Control Distributor in the IU to the LVDA and the electrical support equipment.

To maintain power isolation between vehicle stages, the Switch Selector is divided into two sections: the input section (relay circuits) of each Switch Selector receives its power from the IU; the output section (decoding circuitry and drivers) of each Switch Selector receives its power from the stage in which the Switch Selector is located. The input and output are coupled together through a diode matrix. This matrix decodes the 8-bit input code and activates a PNP output driver, thus producing a Switch Selector output.

Each Switch Selector is connected to the LVDA through 22 lines:

Stage select lines - 2
Read command lines - 2
Reset (forced) lines - 2
Bit register output lines - 8
Verification lines - 8

In addition, there are 2 lines for IU + 28 Vdc and 2 lines for signal return between the Control Distributor and the Switch Selectors.

The wire pairs for stage select, read command, forced reset, IU + 28 Vdc, and signal return are redundant. Only one of each pair is required for normal operation.

All connections between the LVDA and the Switch Selectors, with the exception of the stage select inputs, are connected in parallel as shown in Figure 4.2-2.

The output signals of the LVDA switch selector register, with the exception of the 8-bit command, are sampled at the Control Distributor in the IU and sent to IU PCM telemetry. Each Switch Selector also provides 3 outputs to the telemetry system within its stage.

The Switch Selector is designed to execute flight sequence commands given by the 8-bit code or by its complement. This feature increases reliability and permits operation of the system despite certain failures in the LVDA switch selector register, line drivers, interface cabling, or Switch Selector relays.

The flight sequence commands are stored in the LVDC memory and are issued according to the flight program. When a Programmed Input/Output (PIO) instruction is given, the LVDC loads the 15-bit switch selector register with the computer data. The LVDA switch selector register word format is shown in Figure 4.2-3.

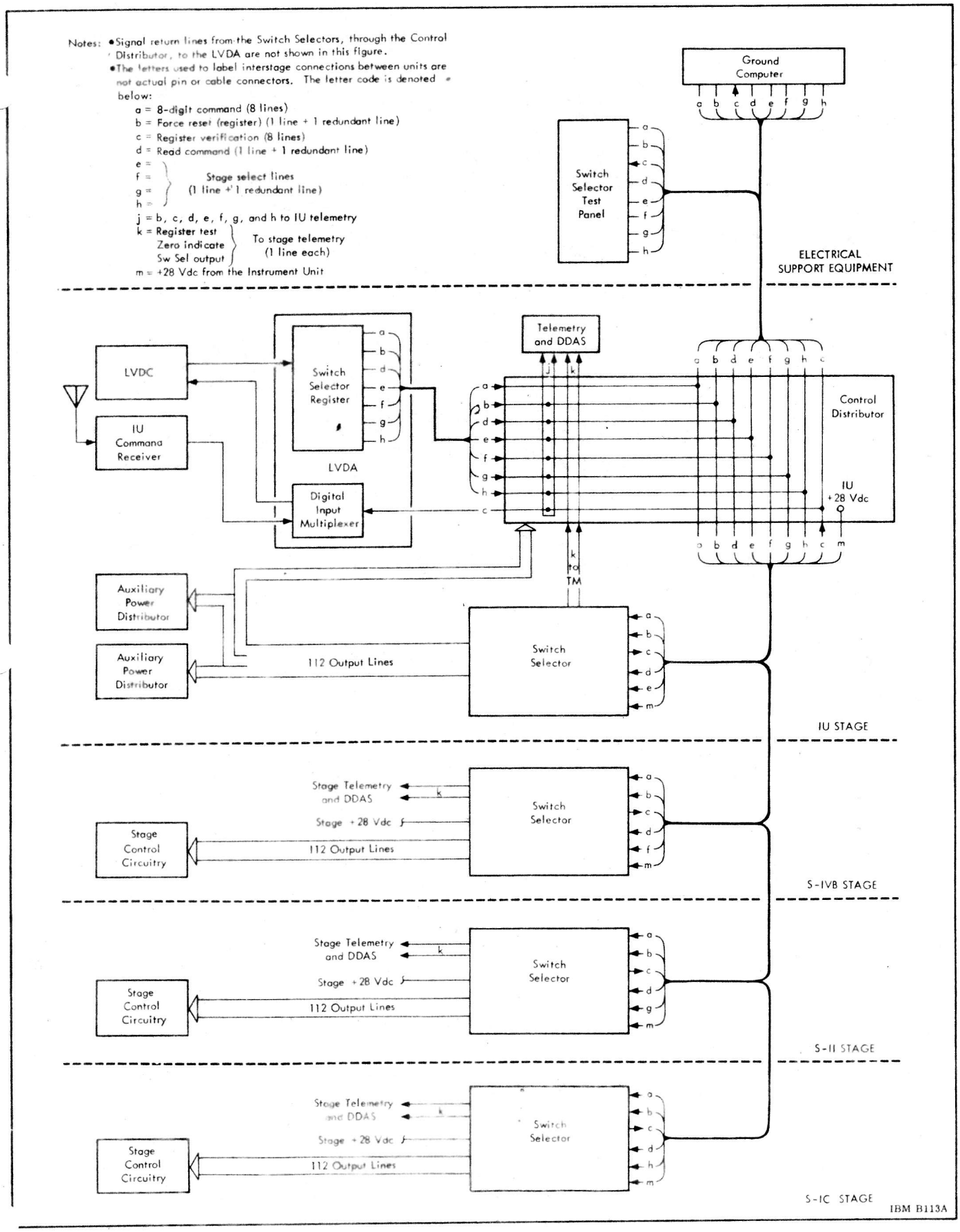


Figure 4.2-1 Saturn V Switch Selector Configuration

Switch Selector register bits 1 through 8 represent the flight sequence command. Bits 9 through 13 select the Switch Selector to be activated. Bit 14 resets all the relays in the Switch Selectors in the event data transfer is incorrect as indicated by faulty verification information received by the LVDA. Bit 15 activates the addressed Switch Selector for execution of the command. The LVDC loads the switch selector register in two passes: bits 1 through 13 are loaded during the first pass and, depending on the feedback code, either bit 14 or bit 15 is loaded during the second pass.

After the Switch Selector input relays have been "picked" by the 8-bit command, the complement of the received code is sent back to the LVDA/LVDC over eight parallel lines. The feedback (verification information) is returned to the digital

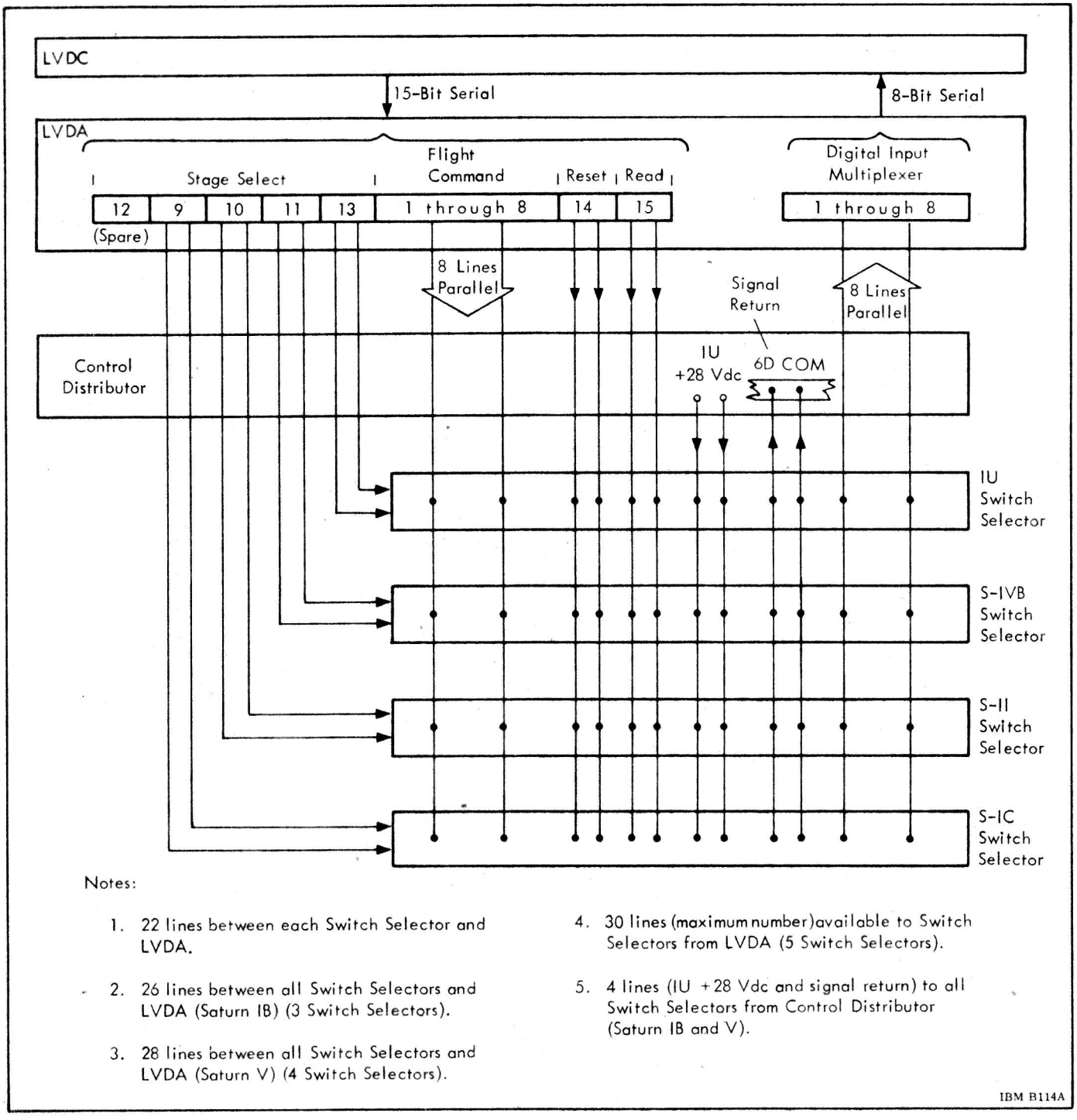


Figure 4.2-2 LVDC - Switch Selector Interconnection Diagram

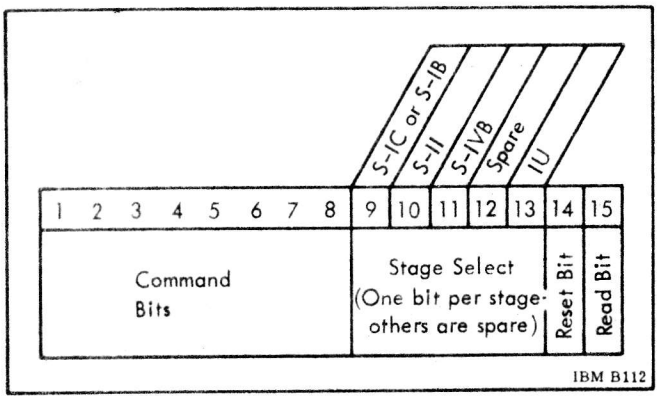


Figure 4.2-3 Switch Selector Register Word Format

input multiplexer of the LVDA and is subsequently compared with the original code in the LVDC. If the feedback agrees with the original code, a read command is given. If the feedback does not agree with the original code, a reset command is given (forced reset), and the LVDC/LVDA reissues the 8-bit command in complement form.

A typical operation cycle, to initiate a given function in a particular stage, is accomplished as follows:

- The 8 verify lines are sampled to ensure that all stage select relays have been reset, thereby ensuring an unwanted stage is not selected. Zero voltage on all lines indicates that this condition exists. The presence of IU + 28 Vdc on the verify lines indicates that the verify lines are enabled because a stage Switch Selector is not reset. Having detected this situation, the LVDC commands a "force reset" and then rechecks the verify lines.
- The LVDC inserts the 8-bit flight command into the LVDA switch selector register. At the same time, a stage select command is sent to the appropriate Switch Selector. Application of the stage select command completes the signal return path for the input relays and allows the 8-bit command to be stored in the Switch Selector input relays.
- The verification lines are sampled to determine if the command transfer was correct.
- If the verification is correct, the LVDC sends a read command to the Switch Selector; activating it, and causing the proper output to occur.
- If the verification is not correct, the LVDC initiates a reset command to prepare the Switch Selector to receive the complement of the original command.
- After the forced reset is completed, the LVDC loads the stage select command, and the complement of the previously sent command, into the LVDA switch selector register.
- Neglecting the verification information that occurs after the complement command is inserted, the LVDC initiates a read command which produces an output from the selected switch selector channel. The read command also energizes the automatic reset circuitry which returns the Switch Selector to the reset condition to prepare it for a new cycle.

4.2.2 COMPONENT DESCRIPTION

A description of Switch Selector operation is given in the following paragraphs (refer to the simplified schematic diagram and timing diagram shown in Figures 4.2-4 and 4.2-5, respectively) The circuit functions of the Switch Selector are as follows:

Stage select

Input relays

Verification

Reset (forced)

Read command

Reset (automatic)

Decoding matrix

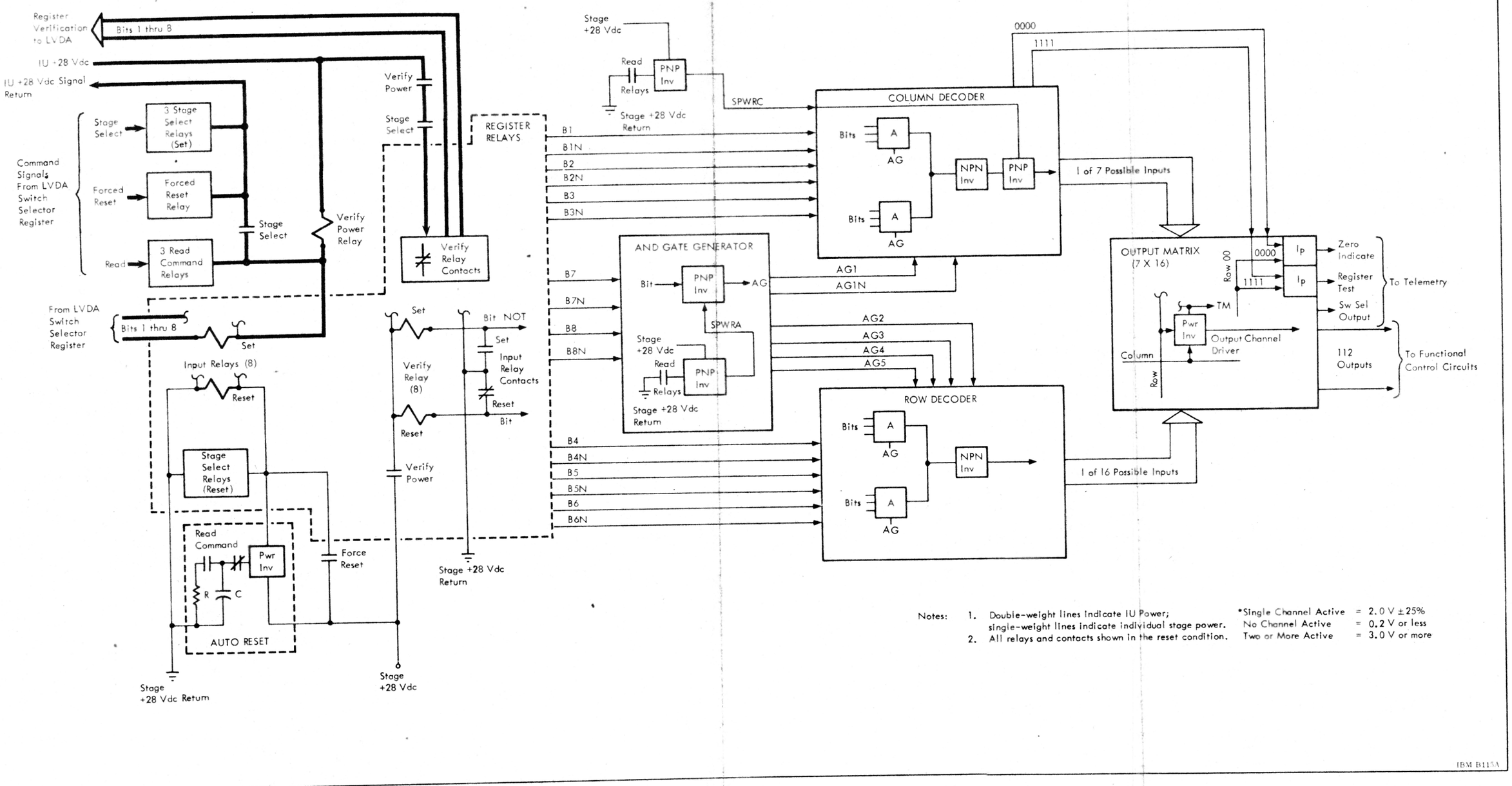
Output matrix and telemetry

Test outputs

The Switch Selector operates on positive logic (i.e., +28 Vdc for a binary "1" and 0 Vdc for a binary "0").

STAGE SELECT

The purpose of the stage select command is to enable the desired Switch Selector to receive the coded flight sequence command from the LVDA. The stage select command (1 bit) is transmitted individually on a separate line to each Switch Selector. Because of the danger of overloading the LVDA, no more than 2 Switch Selectors can be addressed simultaneously.



Notes:
1. Double-weight lines indicate IU Power; single-weight lines indicate individual stage power.
2. All relays and contacts shown in the reset condition.

*Single Channel Active = 2.0 V ±25%
No Channel Active = 0.2 V or less
Two or More Active = 3.0 V or more

IBM B115A

Figure 4.2-4 Switch Selector (Model II) Simplified Diagram

The stage select command sets three magnetic latch relays in the addressed Switch Selector. The setting of these relays completes a ground path for the read command relay, the set side of the input relays, and the verify power relay (see Figure 4.2-4). This action conditions the read and input relays to receive commands from the LVDA and energizes the verify power relay. When the verify power relay contacts close, IU + 28 Vdc power is applied through a set of stage select contacts to the verify relay contacts; and stage + 28 Vdc is applied to the verify relays. The Switch Selector can now accept the 8-bit command from the LVDA, store it in the input relays, and make verification information available to the LVDA

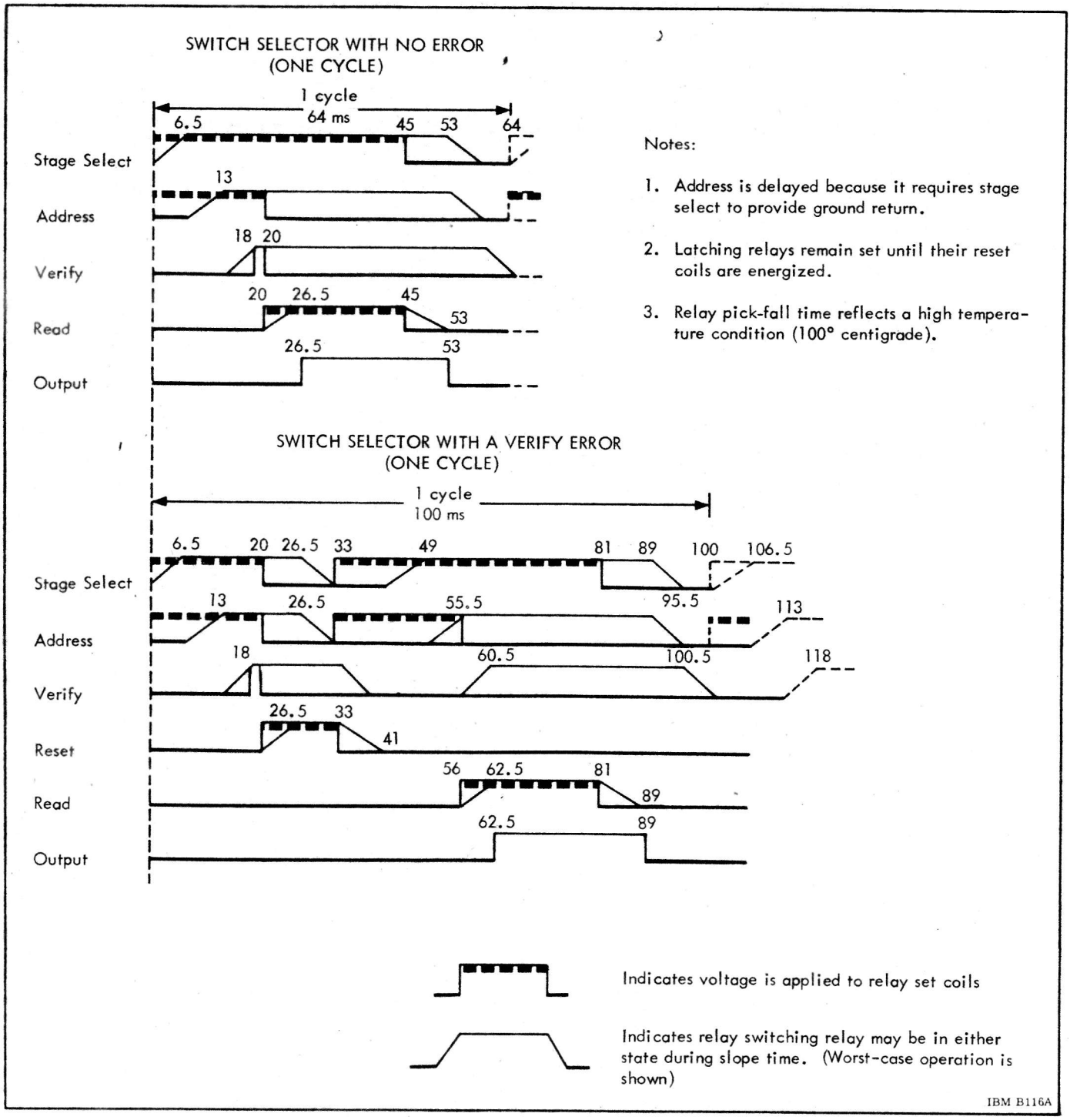


Figure 4.2-5 Typical Switch Selector Timing Diagram

INPUT RELAYS

The input register of the Switch Selector is made up of eight magnetic latch relays, controlled by the 8-bit coded command from the LVDA. The coded command (consisting of 8 bits in parallel) is available to the Switch Selector during the same period of time the stage select signal is present. As soon as the stage select relays are set, a signal return path is provided for the coded command through the input relay coils (See Figure 4.2-4). This allows the coded command to be stored in the input register.

Once the coded command is stored in the input register, binary information is available to the verification register, column decoder, row decoder, and the AND gate generator.

VERIFICATION

A feedback circuit is used to provide verification information back to the LVDC. This circuit consists of 8 relays, and is controlled by the input relay contacts. When a "1" is applied to the input relay set coil, stage ground is switched to the verify relay set coil causing the normally closed verify relay contact to open; indicating a "0" to the LVDC. When a "0" is applied to the input relay set coil, the input relay contacts remain in the reset condition. Stage ground remains applied to one side of the verify relay reset coil, causing the verify relay contact to remain in its normally closed position. Therefore, the verification output of a Switch Selector is the complement of the input command.

READ COMMAND

Immediately after verification of the original command, the read command is initiated. If verification of the original command proved to be false, the read command will not be initiated by the LVDC until the forced reset, stage select, and complemented command have been transmitted to the Switch Selector.

Three conventional (non-latching) relays are picked when the read command is received from the LVDA. One side of the coils of these relays is connected to the read command signal, the other side is connected to the IU signal return through the stage select relay contacts. Thus, a stage select signal must have been received before a read command relay can be energized. When the read relay contacts close, stage ground is applied to the switch power inverters (SPWRA and SPWRC) in the decoder matrix. These inverters generate voltages (SPWRA and SPWRC) which activate the AND gate generators and the column decoder circuitry allowing the coded command to be decoded and an output to occur.

RESET (FORCED)

A forced reset is initiated by the LVDC when the LVDC determines that the verification information is not the complement of the given command. The reset signal is applied to the forced reset relay coil causing the forced reset contacts to close. This action applies stage + 28 Vdc to the stage select and input relay reset coils forcing the Switch Selector into the reset condition shown in Figure 4.2-4. After the forced reset has been completed, the stage select command and the complement of the original flight sequence command are transmitted to the Switch Selector. The complement command is not verified by the LVDC before the read command is issued.

RESET (AUTOMATIC)

An automatic reset pulse is generated when stage power is initially applied to the Switch Selector and when the read command is issued. The automatic reset circuitry consists of a power inverter, an RC network, and a set of read command contacts.

Activation of the read command relay contacts is not required to produce the "Power ON" reset pulse. Prior to the application of stage power to the Switch Selector, the read command contacts are in the reset condition (as shown in Figure 4.2-6) and capacitor C is in a discharged state. When power is applied to the Switch Selector, stage 28 Vdc is applied to the emitter of the power inverter and capacitor C begins to charge through base resistor (R3) and thermistor (RT1). Under these conditions the power inverter turns on, producing an output of approximately 28 Vdc at the collector. This output is applied across the input relay reset coils and the stage select reset coils forcing the Switch Selector into a reset condition.

The duration of the reset pulse is determined by the charge time of capacitor C through base resistor R3 and thermistor RT1. When C charges sufficiently, the power inverter is turned off and the reset pulse is removed from the reset coils.

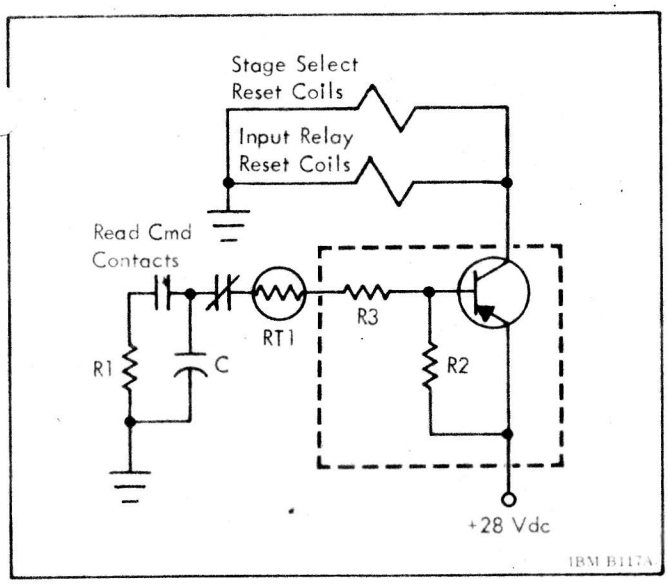


Figure 4.2-6 Automatic Reset Circuitry Simplified Diagram

The automatic reset pulse initiated by the read command is developed exactly the same as the "Power ON" reset pulse. When the read command is issued, the normally open read command relay contact closes, and the normally closed read command relay contact opens. This allows capacitor C to discharge through resistor R1. The power inverter remains turned off (due to lack of base drive) until the read command is removed. When the read command is removed, the read command relay contacts return to the reset condition. At this time, capacitor C begins to charge providing base drive for the power inverter. The power inverter turns on, producing an output of approximately 28 Vdc at the collector. The output is applied across the input relay and stage select relay reset coils forcing the Switch Selector into the reset condition as shown in Figure 4.2-4.

As previously stated, the duration of the reset pulse is determined by the charge time of capacitor C through base resistor R3 and thermistor RT1. When C is sufficiently charged. the power inverter is turned off and the reset pulse is removed from the reset coils.

DECODING MATRIX

The decoding matrix is comprised of PNP inverters, NPN inverters, and AND circuits arranged so that selection of a particular output channel can be made by either the true or complement input code.

This matrix can be divided into three sections as follows (see Figure 4.2-4):

- AND gate circuitry
- Row decoder
- Column decoder

The object of these circuits is to generate a particular column and row signal for each input code and to send these signals to the output matrix upon receipt of the read command signal.

The 8-bit coded command is transferred to the decoding matrix by operation of the input relay contacts. When a binary "1" is applied to an input relay set coil, the normally open input relay contact closes and the normally closed input relay contact opens.

This causes stage ground to be switched from the verify relay reset coil to the verify relay set coil. The bit NOT input to the decoding matrix is now tied to stage ground, while the bit input line to the decoding matrix is at stage + 28 Vdc. When a binary "0" is applied to an input relay set coil, the input relay contacts remain in the reset condition. With the input relay contacts in the reset condition, the bit NOT input to the decoding matrix is at stage + 28 Vdc and the bit input to the decoding matrix is a 0 Vdc.

The 8-bit command is sub-divided into groups for decoding and output driver selection. The least three significant bits (1, 2, and 3) are decoded to enable the column selection circuitry. The next three bits (4, 5, and 6) are decoded to enable the row selection circuitry. Bits 7 and 8 and SPWRA (controlled by read command relays) are applied to the AND gate generator where they are decoded to supply the appropriate AND gates to the column and row decoders. Bit 8 is applied to the AND gate generator where it is decoded to determine whether the coded command is a true or complement word. The listing below illustrates the Boolean expressions for decoding bits 7 and 8.

AG1 = B8 · Read Command

AG1N = B8N · Read Command

AG2 = AG1 · B7

AG3 = AG1 · B7N

AG4 = AG1N · B7N

AG5 = AG1N · B7

where: B8 = Bit 8 = Bit 8 is a binary "1".

B8N = Bit 8 NOT = Bit 8 is a binary "0".

When decoding a typical word (01010101) where bits 8 through 1 are arranged from left to right, the column is determined by bits 8, 3, 2 and 1, or 0101, or more completely by AG1N· B3· B2N· B1. Similarly, the row is determined by bits 8, 7, 6, 5, and 4, or 01010, or more completely AG5· B6N· B5· B4N. However, if the input register transfer circuitry shows a failure, the complement of the original word must select the same output channel in the output matrix. Therefore, the location defined by 01010101 must also be defined by 10101010. This complement code is decoded in the same manner as the original code. The column is determined by bits 8, 3, 2, and 1, or 1010, or more completely by AG1· B3N· B2· B1N. The row is determined by 8, 7, 6, 5, and 4, or 10101, or more completely by AG3· B6· B5N· B4. Therefore, the total expression to define this particular output channel is:

$$\begin{aligned}\text{Channel XY} &= \text{AG1N}\cdot\text{AG5}\cdot\text{B6N}\cdot\text{B5}\cdot\\ &\quad\ \text{B4N}\cdot\text{B3}\cdot\text{B2N}\cdot\text{B1}\\ &+ \text{AG1}\cdot\text{AG3}\cdot\text{B6}\cdot\text{B5N}\cdot\\ &\quad\ \text{B4}\cdot\text{B3N}\cdot\text{B2}\cdot\text{B1N}\end{aligned}$$

OUTPUT MATRIX AND TELEMETRY

The 112 output channels of the Switch Selector are arranged in a 7 by 16 matrix configuration (7 columns and 16 rows). The coordinate selection is similar to the X-Y coincidence method common to core memory technology. An output channel driver (PNP inverter) with the location X-Y in the matrix is activated when the row decoder circuitry (X) and the column decoder circuitry (Y) are turned ON by application of the read command. When activated, the output channel driver produces a + 28 Vdc output to the control circuitry of the selected function.

In addition to producing an output voltage, each output channel driver also produces a separate telemetry output. The 112 telemetry outputs are tied together to produce one switch selector telemetry output signal. This signal is transmitted via PCM and DDAS telemetry. The telemetry signal indicates whether none, one, or more than one output channel is ON at any given time. If one output channel is activated, the telemetry signal will have a magnitude of 2.0 Vdc ± 20 percent; if no output channel is active, the telemetry signal will have a magnitude of 0.2 Vdc or less; and if more than one output channel is activated, the telemetry signal will have a magnitude of 3.0 Vdc or more. When the Switch Selector is operating properly, only one output channel will be active at any given time.

TEST OUTPUTS

In addition to the telemetry output described, each Switch Selector has two telemetry outputs which are used to verify that the input selection relays can be set and reset properly. These signals (register test and zero indicate) are special outputs of the output matrix. The register test output is generated by an output driver when the input address selection is all ones and the read command has been issued. The zero indicate output is generated when the input address selection is all zeros (read command is not required). The zero indicate and register test signals are transmitted via PCM and DDAS telemetry.

SECTION 4.3
SATURN V OPERATION SEQUENCE

The Saturn V Operation sequence starts during the prelaunch phase at approximately 22 hours when the electrical power from the ground support equipment is applied to all stages of the launch vehicle. Figure 4.3-1 provides an overall view of the prelaunch sequence. During this time, the sequencing is controlled from the launch control center-launcher-umbilical tower complex, utilizing both manual and automatic control to checkout the functions of the entire Astrionics System. After the umbilical is disconnected, the sequencing is primarily controlled by the flight program within the LVDC.

Since flight sequencing is time related, the sequencing operation is divided into seven time periods. These time periods are referred to as time bases and progress from the first time base (T_0) through time base No. 8 (T_8). Each time base is related to a particular flight event. These time bases and their initiating events are as follows:

T_0	Guidance Reference Release
T_1	Lift-off
T_2	Inboard engine cutoff (S-IC)
T_3	Outboard engine cutoff (S-IC)
T_4	Engine cutoff (S-II)
T_5	Engine cutoff (S-IVB)
T_6	Begin restart preparations (S-IVB)
T_7	Engine cutoff (S-IVB)
T_8	DCS Command TD and E

The flight program (described in Chapter 11) uses these time bases in issuing sequential commands to the appropriate stages. The essential sequenced events, as they occur within each time base, are listed in Table 4.3-1.

Table 4.3-1 Typical Saturn V Flight Sequence, **Time Base 0 through 8**

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
——	Guidance Reference Release (T_0)		T_1 - 17.0
00:00:00.0	Liftoff – Start of Time Base No. 1 (T_1)		T_1 + 0.0
00:00:05.0	Sensor Bias On	IU	T_1 + 5.0
00:00:14.0	Multiple Engine Cutoff Enable	S-IC	T_1 + 14.0
00:00:19.8	S-IC Outboard Engines Cant On 'A'	IU	T_1 + 19.8
00:00:20.0	S-IC Outboard Engines Cant On 'B'	IU	T_1 + 20.0
00:00:20.2	S-IC Outboard Engines Cant On 'C'	IU	T_1 + 20.2
00:00:24.0	TM Calibrate On	S-IC	T_1 + 24.0
00:00:27.0	TM Calibrator In-flight Calibrate On	IU	T_1 + 27.0
00:00:29.0	TM Calibrate Off	S-IC	T_1 + 29.0
00:00:30.0	Launch Vehicle Engines EDS Cutoff Enable	IU	T_1 + 30.0
00:00:32.0	TM Calibrator In-flight Calibrate Off	IU	T_1 + 32.0
00:00:49.5	Fuel Pressurizing Valve No. 2 Open + Tape Recorder Record	S-IC	T_1 + 49.5
00:01:14.0	Start Data Recorders	S-II	T_1 + 74.0
00:01:15.0	Cooling System Electronic Assembly Power Off	IU	T_1 + 75.0
00:01:30.0	TM Calibrator In-flight Calibrate On	IU	T_1 + 90.0
00:01:35.0	TM Calibrator In-flight Calibrate Off	IU	T_1 + 95.0
00:01:35.3	Fuel Pressurizing Valve No. 3 Open	S-IC	T_1 + 95.3
00:01:45.0	Flight Control Computer Switch Point No. 1	IU	T_1 + 105.0
00:01:55.1	TM Calibrate On	S-IC	T_1 + 115.1
00:02:00.0	Flight Control Computer Switch Point No. 2	IU	T_1 + 120.0
00:02:00.1	TM Calibrate Off	S-IC	T_1 + 120.1
00:02:03.5	Fuel Pressurizing Valve No. 4 Open	S-IC	T_1 + 123.5
00:02:03.8	Tape Recorder Record On	IU	T_1 + 123.8
00:02:04.1	LOX Tank Strobe Lights Off	S-IC	T_1 + 124.1
00:02:04.3	S-IC Two Engines Out Auto-Abort Inhibit Enable	IU	T_1 + 124.3
00:02:04.5	S-IC Two Engines Out Auto-Abort Inhibit	IU	T_1 + 124.5
00:02:04.7	Excess Rate (P, Y, R)Auto-Abort Inhibit Enable	IU	T_1 + 124.7
00:02:04.9	Excess Rate (P, Y, R) Auto-Abort Inhibit and Switch Rate Gyros SC Indication A	IU	T_1 + 124.9
00:02:05.1	Two Adjacent Outboard Engines Out Cutoff Enable	S-IC	T_1 + 125.1

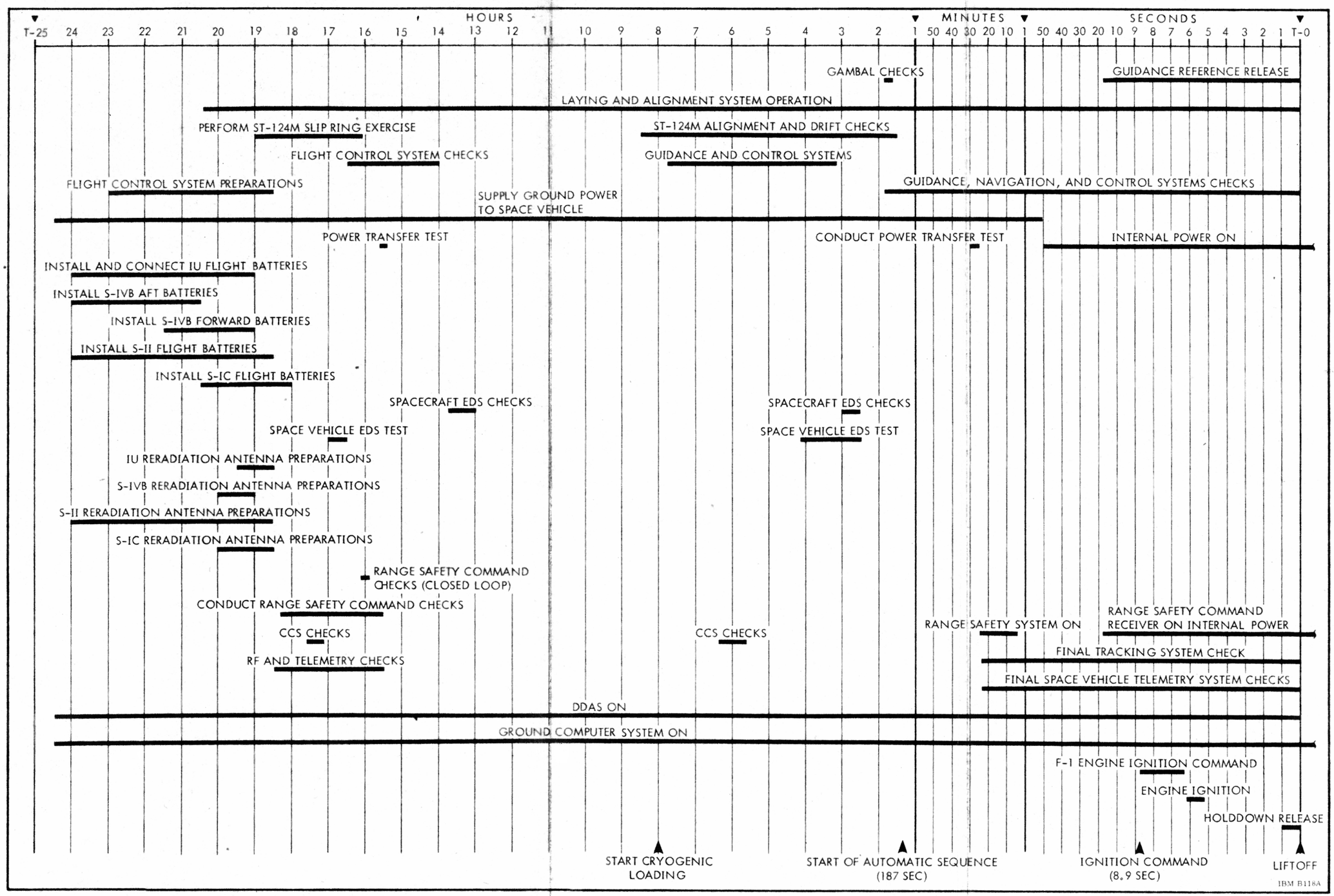


Figure 4.3-1 Typical Saturn V Astrionics System Prelaunch Sequence

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
00:02:05.2	Inboard Engine Cutoff – Start of Time Base No. 2 (T_2)	S-IC	T_2 + 0.0
00:02:05.4	Inboard Engine Cutoff Backup	S-IC	T_2 + 0.2
00:02:05.6	Start First PAM-FM/FM Calibration	S-II	T_2 + 0.4
00:02:05.8	Auto-Abort Enable Relays Reset	IU	T_2 + 0.6
00:02:06.0	Excess Rate (Roll) Auto-Abort Inhibit Enable	IU	T_2 + 0.8
00:02:06.2	Excess Rate (Roll) Auto-Abort Inhibit and Switch Rate Gyros SC Indication 'B'	IU	T_2 + 1.0
00:02:10.6	Stop First PAM-FM/FM Calibration	S-II	T_2 + 5.4
00:02:21.1	S-II Ordnance Arm	S-II	T_2 + 15.9
00:02:21.3	Separation and Retro No. 1 EBW Firing Units Arm	S-IC	T_2 + 16.1
00:02:21.5	Separation and Retro No. 2 EBW Firing Units Arm	S-IC	T_2 + 16.3
00:02:24.3	TM Measurement Switchover	S-IC	T_2 + 19.1
00:02:24.5	Separation Camera On	S-IC	T_2 + 19.3
00:02:24.6	Q-Ball Power Off	IU	T_2 + 19.4
00:02:24.7	Outboard Engines Cutoff Enable	S-IC	T_2 + 19.5
00:02:24.9	Outboard Engines Cutoff Backup Enable	S-IC	T_2 + 19.7
00:02:30.7	Outboard Engines Cutoff – Start of Time Base No. 3 (T_3)		T_3 + 0.0
00:02:30.8	LH_2 Tank High Pressure Vent Mode	S-II	T_3 + 0.1
00:02:30.9	S-II LH_2 Recirculation Pumps Off	S-II	T_3 + 0.2
00:02:31.2	S-II Ullage Trigger	S-II	T_3 + 0.5
00:02:31.4	S-IC/S-II Separation (No. 1)	S-IC	T_3 + 0.7
00:02:31.5	S-IC/S-II Separation (No. 2)	S-IC	T_3 + 0.8
00:02:31.6	S-II Engines Cutoff Reset	S-II	T_3 + 0.9
00:02:31.7	Engines Ready Bypass	S-II	T_3 + 1.0
00:02:31.8	Prevalves Lockout Reset	S-II	T_3 + 1.1
00:02:31.9	Switch Engine Control to S-II and S-IC Outboard Engine Cant Off 'A'	IU	T_3 + 1.2
00:02:32.0	S-IC Outboard Engines Cant Off 'B'	IU	T_3 + 1.3
00:02:32.1	S-II Engine Start	S-II	T_3 + 1.4
00:02:32.2	S-II Engine Out Indication A Enable; S-II Aft Interstage Separation Indication A Enable	IU	T_3 + 1.5

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
00:02:32.4	S-II Engine Out Indication 'B' Enable; S-II Aft Interstage Separation Indication 'B' Enable	IU	T_3 + 1.7
00:02:32.6	Engines Ready Bypass Reset	S-II	T_3 + 1.9
00:02:32.7	Measurement Transfer Mode Position 'B'	S-IVB	T_3 + 2.0
00:02:33.7	S-II Hydraulic Accumulators Unlock	S-II	T_3 + 3.0
00:02:36.9	PU System Open Loop Arm	S-II	T_3 + 6.2
00:02:37.1	Chilldown Valves Close	S-II	T_3 + 6.4
00:02:37.4	S-II Start Phase Limiter Cutoff Arm	S-II	T_3 + 6.7
00:02:37.6	High (5.5) Engine Mixture Ratio On	S-II	T_3 + 6.9
00:02:38.4	S-II Start Phase Limiter Cutoff Arm Reset	S-II	T_3 + 7.7
00:02:38.5	Prevalves Close Arm	S-II	T_3 + 7.8
00:02:42.4	Tape Recorder Record Off	IU	T_3 + 11.7
00:02:42.6	Stop Data Recorders	S-II	T_3 + 11.9
00:03:01.4	S-II Aft Interstage Separation	S-II	T_3 + 30.7
00:03:01.7	Water Coolant Valve Open	IU	T_3 + 31.0
00:03:32.1	Flight Control Computer Switch Point No. 3	IU	T_3 + 61.4
00:04:35.7	Start Second PAM-FM/FM Calibration	S-II	T_3 + 125.0
00:04:40.7	Stop Second PAM-FM/FM Calibration	S-II	T_3 + 130.0
00:05:42.1	Flight Control Computer Switch Point No. 4	IU	T_3 + 191.4
00:05:53.4	TM Calibrator In-flight Calibrate On	IU	T_3 + 202.7
00:05:58.4	TM Calibrator In-flight Calibrate Off	IU	T_3 + 207.7
00:06:03.4	Measurement Control Switch No. 2 Activate	S-II	T_3 + 212.7
00:06:15.7	Start Third PAM-FM/FM Calibration	S-II	T_3 + 225.0
00:06:20.7	Stop Third PAM-FM/FM Calibration	S-II	T_3 + 230.0
00:07:21.6	TM Calibrator In-flight Calibrate On	IU	T_3 + 290.9
00:07:26.6	TM Calibrator In-flight Calibrate Off	IU	T_3 + 295.9
00:07:30.7	S-II LH_2 Step Pressurization	S-II	T_3 + 300.0
00:08:01.9	Charge Ullage Ignition On	S-IVB	T_3 + 331.2
00:08:02.1	S-II/S-IVB Ordnance Arm	S-II	T_3 + 331.4
00:08:03.0	Tape Recorder Record On	IU	T_3 + 332.3
00:08:03.2	Start Data Recorders	S-II	T_3 + 332.5
00:08:05.8	S-II LOX Depletion Sensors Cutoff Arm	S-II	T_3 + 335.1

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
00:08:06.0	S-II LH_2 Depletion Sensors Cutoff Arm	S-II	T_3 + 335.3
00:08:39.8	Cutoff S-II J-2 Engines – Start of Time Base No. 4 (T_4)	S-II	T_4 + 0.0
00:08:39.9	Start Recorder Timers	S-II	T_4 + 0.1
00:08:40.0	Prevalves Close Off	S-IVB	T_4 + 0.2
00:08:40.1	S-IVB Engine Cutoff Off	S-IVB	T_4 + 0.3
00:08:40.2	LOX Tank Flight Pressure System On	S-IVB	T_4 + 0.4
00:08:40.3	Engine Ready Bypass	S-IVB	T_4 + 0.5
00:08:40.4	LOX Chilldown Pump Off	S-IVB	T_4 + 0.6
00:08:40.5	Fire Ullage Ignition On	S-IVB	T_4 + 0.7
00:08:40.6	S-II/S-IVB Separation	S-II	T_4 + 0.8
00:08:40.8	S-IVB Engine Start On	S-IVB	T_4 + 1.0
00:08:41.0	Flight Control Computer S-IVB Burn Mode On A	IU	T_4 + 1.2
00:08:41.1	Flight Control Computer S-IVB Burn Mode On B	IU	T_4 + 1.3
00:08:42.0	Fuel Chilldown Pump Off	S-IVB	T_4 + 2.2
00:08:42.3	S-IVB Engine Out Indication 'A' Enable	IU	T_4 + 2.5
00:08:42.5	S-IVB Engine Out Indication 'B' Enable	IU	T_4 + 2.7
00:08:43.8	Fuel Injection Temperature OK Bypass	S-IVB	T_4 + 4.0
00:08:44.0	S-IVB Engine Start Off	S-IVB	T_4 + 4.2
00:08:45.6	First Burn Relay On	S-IVB	T_4 + 5.8
00:08:49.6	Charge Ullage Jettison On	S-IVB	T_4 + 9.8
00:08:52.3	Fire Ullage Jettison On	S-IVB	T_4 + 12.8
00:08:53.6	Ullage Charging Reset	S-IVB	T_4 + 13.8
00:08:53.8	Ullage Firing Reset	S-IVB	T_4 + 14.0
00:08:54.0	Fuel Injection Temperature OK Bypass Reset	S-IVB	T_4 + 14.2
00:08:54.2	Tape Recorder Record Off	IU	T_4 + 14.4
00:08:56.6	TM Calibrator In-flight Calibrate On	IU	T_4 + 16.8
00:09:01.6	TM Calibrator In-flight Calibrate Off	IU	T_4 + 21.8
00:09:03.8	Heat-Exchanger Bypass Valve Control Enable	S-IVB	T_4 + 24.0
00:09:05.5	In-flight Calibration Mode On	S-IVB	T_4 + 25.7
00:09:06.0	TM Calibrate On	S-IVB	T_4 + 26.2

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
00:09:11.0	TM Calibrate Off	S-IVB	T_4 + 31.2
00:09:11.5	In-flight Calibration Mode Off	S-IVB	T_4 + 31.7
00:11:10.2	Engine Pump Purge Control Valve Enable On	S-IVB	C.O. -7.0
00:11:21.1	Velocity Cutoff of S-IVB Engine – Start of Time Base No. 5 (T_5)	S-IVB	T_5 + 0.0
00:11:21.2	S-IVB Engine Cutoff	S-IVB	T_5 + 0.1
00:11:21.3	Point Level Sensor Disarming	S-IVB	T_5 + 0.2
00:11:21.4	S-IVB Ullage Engine No. 1 On	S-IVB	T_5 + 0.3
00:11:21.5	S-IVB Ullage Engine No. 2 On	S-IVB	T_5 + 0.4
00:11:21.7	S-IVB Ullage Thrust Present Indication On	IU	T_5 + 0.6
00:11:21.9	First Burn Relay Off	S-IVB	T_5 + 0.8
00:11:22.3	LOX Tank Flight Pressure System Off	S-IVB	T_5 + 1.2
00:11:22.5	LOX Tank Pressurization Shutoff Valves Close	S-IVB	T_5 + 1.4
00:11:22.7	Engine Pump Purge Control Valve Enable On	S-IVB	T_5 + 1.6
00:11:24.6	Flight Control Computer S-IVB Burn Mode Off 'A'	IU	T_5 + 3.5
00:11:24.8	Flight Control Computer S-IVB Burn Mode Off 'B'	IU	T_5 + 3.7
00:11:25.2	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_5 + 4.1
00:11:25.3	TM Calibrator In-flight Calibrate On	IU	T_5 + 4.2
00:11:26.1	SC Control of Saturn Enable	IU	T_5 + 5.0
00:11:27.6	In-flight Calibration Mode On	S-IVB	T_5 + 6.5
00:11:28.1	TM Calibrate On	S-IVB	T_5 + 7.0
00:11:30.3	TM Calibrator In-flight Calibrate Off	IU	T_5 + 9.2
00:11:31.1	S-IVB Engine Out Indication 'A' Enable Reset	IU	T_5 + 10.0
00:11:31.3	S-IVB Engine Out Indication 'B' Enable Reset	IU	T_5 + 10.2
00:11:31.5	S-1 RF Assembly Power Off	IU	T_5 + 10.4
00:11:32.4	Tape Recorder Playback Reverse On	IU	T_5 + 11.3
00:11:33.1	TM Calibrate Off	S-IVB	T_5 + 12.0
00:11:33.6	In-flight Calibration Mode Off	S-IVB	T_5 + 12.5
00:11:43.1	Single Sideband FM Transmitter Off	S-IVB	T_5 + 22.0
00:12:20.1	LH_2 Tank Continuous Vent Orifice Shutoff Valve Open On	S-IVB	T_5 + 59.0
00:12:20.2	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open On	S-IVB	T_5 + 59.1
00:12:22.1	LH_2 Tank Continuous Vent Relief Orifice Shutoff Valve Open Off	S-IVB	T_5 + 61.0

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
00:12:22.2	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open Off	S-IVB	T_5 + 61.1
00:12:43.2	Tape Recorder Playback Reverse Off	IU	T_5 + 82.1
00:12:48.1	S-IVB Ullage Engine No. 1 Off	S-IVB	T_5 + 87.0
00:12:48.2	S-IVB Ullage Engine No. 2 Off	S-IVB	T_5 + 87.1
00:12:48.3	S-IVB Ullage Thrust Present Indication Off	IU	T_5 + 87.2
00:19:41.1	PU Inverter and DC Power Off	S-IVB	T_5 + 500.0
00:21:23.7	Engine Pump Purge Control Valve Enable Off	S-IVB	T_5 + 602.6
00:54:41.1	Aux Hydraulic Pump Flight Mode On	S-IVB	T_5 + 2600.0
00:55:29.1	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_5 + 2648.0
01:34:41.1	PU Inverter and DC Power On	S-IVB	T_5 + 5000.0
01:41:21.1	Aux Hydraulic Pump Flight Mode On	S-IVB	T_5 + 5400.0
01:42:09.1	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_5 + 5448.0
03:06:21.1	Aux Hydraulic Pump Flight Mode On	S-IVB	T_5 + 10500.0
03:14:21.1	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_5 + 10980.0
02:41:02.7	Begin Restart Preparations – Start of Time Base No. 6 (T_6)		T_6 + 0.0
02:41:02.8	S-IVB Restart Alert On	IU	T_6 + 0.1
02:41:03.0	SC Control of Saturn Disable	IU	T_6 + 0.3
02:41:03.7	In-flight Calibration Mode On	S-IVB	T_6 + 1.0
02:41:03.9	TM Calibrator In-flight Calibrate On	IU	T_6 + 1.2
02:41:04.1	TM Calibrate On	S-IVB	T_6 + 1.4
02:41:08.9	TM Calibrator In-flight Calibrate Off	IU	T_6 + 6.2
02:41:09.1	TM Calibrate Off	S-IVB	T_6 + 6.4
02:41:09.7	In-flight Calibration Mode Off	S-IVB	T_6 + 7.0
02:41:12.7	S-IVB Engine Cutoff Off	S-IVB	T_6 + 10.0
02:41:13.2	Single Sideband FM Transmitter On	S-IVB	T_6 + 10.5
02:41:39.0	LH_2 Tank Vent and Latching Relief Valve Boost Close On	S-IVB	T_6 + 36.3
02:41:39.2	LOX Tank Vent and NPV Valves Boost Close On	S-IVB	T_6 + 36.5
02:41:40.0	S-IVB Restart Alert Off	IU	T_6 + 37.3
02:41:41.0	LH_2 Tank Vent and Latching Relief Valve Boost Close Off	S-IVB	T_6 + 38.3
02:41:41.2	LOX Tank Vent and NPV Valves Boost Close Off	S-IVB	T_6 + 38.5

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
02:41:44.0	Burner LH_2 Propellant Valve Open On	S-IVB	T_6 + 41.3
02:41:44.3	Burner Exciters On	S-IVB	T_6 + 41.6
02:41:44.7	Burner LOX Shutdown Valve Open On	S-IVB	T_6 + 42.0
02:41:44.9	LH_2 Tank Continuous Vent Valve Close On	S-IVB	T_6 + 42.2
02:41:45.5	Burner LH_2 Propellant Valve Open Off	S-IVB	T_6 + 42.8
02:41:46.2	Burner LOX Shutdown Valve Open Off	S-IVB	T_6 + 43.5
02:41:46.9	LH_2 Tank Continuous Vent Valve Close Off	S-IVB	T_6 + 44.2
02:41:48.1	Burner Exciters Off	S-IVB	T_6 + 45.4
02:41:50.7	Burner Automatic Cutoff System Arm	S-IVB	T_6 + 48.0
02:41:50.8	LH_2 Tank Repressurization Control Valve Open On	S-IVB	T_6 + 48.1
02:41:51.0	LOX Tank Repressurization Control Valve Open On	S-IVB	T_6 + 48.3
02:44:41.7	Aux Hydraulic Pump Flight Mode On	S-IVB	T_6 + 219.0
02:45:11.7	LOX Chilldown Pump On	S-IVB	T_6 + 249.0
02:45:16.7	Fuel Chilldown Pump On	S-IVB	T_6 + 254.0
02:45:21.7	Prevalves Close On	S-IVB	T_6 + 259.0
02:47:42.7	In-flight Calibration Mode On	S-IVB	T_6 + 400.0
02:47:42.9	TM Calibrator In-flight Calibrate On	IU	T_6 + 400.2
02:47:43.1	TM Calibrate On	S-IVB	T_6 + 400.4
02:47:47.9	TM Calibrator In-flight Calibrate Off	IU	T_6 + 405.2
02:47:48.1	TM Calibrate Off	S-IVB	T_6 + 405.4
02:47:48.7	In-flight Calibration Mode Off	S-IVB	T_6 + 406.0
02:48:32.7	Second Burn Relay On	S-IV	T_6 + 450.0
02:48:32.8	PU Valve Hardover Position On	S-IVB	T_6 + 450.1
02:49:16.3	S-IVB Restart Alert On	IU	T_6 + 493.6
02:49:19.0	S-IVB Ullage Engine No. 1 On	S-IVB	T_6 + 496.3
02:49:19.1	S-IVB Ullage Engine No. 2 On	S-IVB	T_6 + 496.4
02:49:19.2	S-IVB Ullage Thrust Present Indication On	IU	T_6 + 496.5
02:49:19.3	LOX Tank Repressurization Control Valve Open Off	S-IVB	T_6 + 496.6
02:49:19.4	LH_2 Tank Repressurization Control Valve Open Off	S-IVB	T_6 + 496.7
02:49:19.5	Burner LH_2 Propellant Valve Close On	S-IVB	T_6 + 496.8
02:49:19.7	Burner Automatic Cutoff System Disarm	S-IVB	T_6 + 497.0
02:49:19.9	LH_2 Tank Continuous Vent Valve Close On	S-IVB	T_6 + 497.2

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
02:49:20.3	Repressurization System Mode Select On (AMB)	S-IVB	T_6 + 497.6
02:49:21.9	LH_2 Tank Continuous Vent Valve Close Off	S-IVB	T_6 + 499.2
02:49:22.5	Burner LH_2 Propellant Valve Close Off	S-IVB	T_6 + 499.8
02:49:22.7	LOX Tank Repressurization Control Valve Open On	S-IVB	T_6 + 500.0
02:49:24.0	Burner LOX Shutdown Valve Close On	S-IVB	T_6 + 501.3
02:49:27.0	Burner LOX Shutdown Valve Close Off	S-IVB	T_6 + 504.3
02:49:42.7	LH_2 Tank Repressurization Control Valve Open On	S-IVB	T_6 + 520.0
02:50:22.1	Prevalves Close Off	S-IVB	T_6 + 559.4
02:50:22.7	S-IVB Restart Alert Off	IU	T_6 + 560.0
02:50:31.3	Engine Ready Bypass	S-IVB	T_6 + 568.6
02:50:32.1	Fuel Chilldown Pump Off	S-IVB	T_6 + 569.4
02:50:32.3	LOX Chilldown Pump Off	S-IVB	T_6 + 569.6
02:50:32.7	S-IVB Engine Start On	S-IVB	T_6 + 570.0
02:50:35.7	S-IVB Ullage Engine No. 1 Off	S-IVB	T_6 + 573.0
02:50:35.8	S-IVB Ullage Engine No. 2 Off	S-IVB	T_6 + 573.1
02:50:35.9	S-IVB Ullage Thrust Present Indication Off	IU	T_6 + 573.2
02:50:39.9	S-IVB Engine Out Indication 'A' Enable	IU	T_6 + 577.2
02:50:40.0	LOX Tank Repressurization Control Valve Open Off	S-IVB	T_6 + 577.3
02:50:40.1	S-IVB Engine Out Indication 'B' Enable	IU	T_6 + 577.4
02:50:40.2	LH_2 Tank Repressurization Control Valve Open Off	S-IVB	T_6 + 577.5
02:50:40.3	Flight Control Computer S-IVB Burn Mode On 'A'	IU	T_6 + 577.6
02:50:40.5	Flight Control Computer S-IVB Burn Mode On 'B'	IU	T_6 + 577.8
02:50:40.7	Fuel Injection Temperature OK Bypass	S-IVB	T_6 + 578.0
02:50:40.9	LOX Tank Flight Pressure System On	S-IVB	T_6 + 578.2
02:50:41.1	LOX Tank Pressurization Shutoff Valves Open	S-IVB	T_6 + 578.4
02:50:41.3	S-IVB Engine Start Off	S-IVB	T_6 + 578.6
02:50:45.7	PU Valve Hardover Position Off	S-IVB	T_6 + 583.0
02:50:50.7	Fuel Injection Temperature OK Bypass Reset	S-IVB	T_6 + 588.0
02:55:00.7	Flight Control Computer Switch Point No. 6	IU	T_6 + 838.0
02:55:12.7	Second Burn Relay Off	S-IVB	T_6 + 850.0
02:55:54.8	Point Level Sensor Arming	S-IVB	T_6 + 892.1

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
02:55:54.8	S-IVB Engine Cutoff - Start of Time Base No. 7 (T_7)	S-IVB	T_7 + 0.0
02:55:54.9	S-IVB Engine Cutoff	S-IVB	T_7 + 0.1
02:55:55.3	LH_2 Tank Continuous Vent Orifice Shutoff Valve Open On	S-IVB	T_7 + 0.5
02:55:55.4	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open On	S-IVB	T_7 + 0.6
02:55:55.5	LOX Tank NPV Valve Open On	S-IVB	T_7 + 0.7
02:55:55.6	LH_2 Tank Latching Relief Valve Open On	S-IVB	T_7 + 0.8
02:55:55.7	Point Level Sensor Disarming	S-IVB	T_7 + 0.9
02:55:55.8	LOX Tank Pressurization Shutoff Valves Close	S-IVB	T_7 + 1.0
02:55:55.9	LOX Tank Flight Pressure System Off	S-IVB	T_7 + 1.1
02:55:56.0	Second Burn Relay Off	S-IVB	T_7 + 1.2
02:55:57.3	LH_2 Tank Continuous Vent Orifice Shutoff Valve Open Off	S-IVB	T_7 + 2.5
02:55:57.4	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open Off	S-IVB	T_7 + 2.6
02:55:57.5	LOX Tank NPV Valve Latch Open On	S-IVB	T_7 + 2.7
02:55:57.6	LH_2 Tank Latching Relief Valve Latch On	S-IVB	T_7 + 2.8
02:55:58.4	Flight Control Computer S-IVB Burn Mode Off 'A'	IU	T_7 + 3.6
02:55:58.5	LOX Tank NPV Valve Open Off	S-IVB	T_7 + 3.7
02:55:58.6	LH_2 Tank Latching Relief Valve Open Off	S-IVB	T_7 + 3.8
02:55:58.7	Flight Control Computer S-IVB Burn Mode Off 'B'	IU	T_7 + 3.9
02:55:58.9	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_7 + 4.1
02:55:59.5	LOX Tank NPV Valve Latch Open Off	S-IVB	T_7 + 4.7
02:55:59.6	LH_2 Tank Latching Relief Valve Latch Off	S-IVB	T_7 + 4.8
02:55:59.8	SC Control of Saturn Enable	IU	T_7 + 5.0
02:56:04.8	S-IVB Engine Out Indication 'A' Enable Reset	IU	T_7 + 10.0
02:56:05.0	S-IVB Engine Out Indication 'B' Enable Reset	IU	T_7 + 10.2
02:56:19.8	Single Sideband FM Transmitter Off	S-IVB	T_7 + 25.0
02:58:24.5	LOX Tank NPV Valve Open On	S-IVB	T_7 + 149.7
02:58:25.5	LOX Tank NPV Valve Open Off	S-IVB	T_7 + 150.7
02:58:28.5	LOX Tank Vent and NPV Valves Boost Close On	S-IVB	T_7 + 153.7
02:58:30.5	LOX Tank Vent and NPV Valves Boost Close Off	S-IVB	T_7 + 155.7
03:10:53.8	LH_2 Tank Latching Relief Valve Open On	S-IVB	T_7 + 899.0
03:10:54.6	LH_2 Tank Continuous Vent Valve Close On	S-IVB	T_7 + 899.8
03:10:54.8	LH_2 Tank Latching Relief Valve Open Off	S-IVB	T_7 + 900.0

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
03:10:56.6	LH_2 Tank Continuous Vent Valve Close Off	S-IVB	T_7 + 901.8
03:10:57.8	LH_2 Tank Vent and Latching Relief Valve Boost Close On	S-IVB	T_7 + 903.0
03:10:59.8	LH_2 Tank Vent and Latching Relief Valve Boost Close Off	S-IVB	T_7 + 905.0
03:15:54.8	CCS Coax Switch Low Gain Antenna	IU	T_7 + 1200.0
03:15:55.0	PCM Coax Switch Low Gain Antenna	IU	T_7 + 1200.2
03:15:55.2	IU Command System Enable	IU	T_7 + 1200.4
03:49:14.8	Aux Hydraulic Pump Flight Mode On	S-IVB	T_7 + 3200.0
03:50:02.8	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_7 + 3248.0
03:55:55.2	LH_2 Tank Latching Relief Valve Open On	S-IVB	T_7 + 3600.4
03:55:57.2	LH_2 Tank Latching Relief Valve Latch On	S-IVB	T_7 + 3602.4
03:55:58.2	LH_2 Tank Latching Relief Valve Open Off	S-IVB	T_7 + 3603.4
03:55:59.2	LH_2 Tank Latching Relief Valve Latch Off	S-IVB	T_7 + 3604.4
04:10:53.8	LH_2 Tank Latching Relief Valve Open On	S-IVB	T_7 + 4499.0
04:10:54.8	LH_2 Tank Latching Relief Valve Open Off	S-IVB	T_7 + 4500.0
04:10:57.8	LH_2 Tank Vent and Latching Relief Valve Boost Close On	S-IVB	T_7 + 4503.0
04:10:59.8	LH_2 Tank Vent and Latching Relief Valve Boost Close Off	S-IVB	T_7 + 4505.0
04:51:07.4	DCS Command TD and E Enable - Start Time Base 8 (T_8)	S-IVB	T_8 + 0.0
04:51:07.6	S-IVB Engine EDS Cutoff No. 2 Disable	S-IVB	T_8 + 0.2
04:51:07.8	LH_2 Tank Continuous Vent Orifice Shutoff Valve Open On	S-IVB	T_8 + 0.4
04:51:08.0	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open On	S-IVB	T_8 + 0.6
04:51:08.2	Engine Pump Purge Control Valve Enable On	S-IVB	T_8 + 0.8
04:51:08.4	LH_2 Tank Repressurization Control Valve Open On	S-IVB	T_8 + 1.0
04:51:09.8	LH_2 Tank Continuous Vent Orifice Shutoff Valve Open Off	S-IVB	T_8 + 2.4
04:51:10.0	LH_2 Tank Continuous Vent Relief Override Shutoff Valve Open Off	S-IVB	T_8 + 2.6
05:02:37.4	Aux Hydraulic Pump Flight Mode On	S-IVB	T_8 + 690.0
05:02:57.4	Passivation Enable	S-IVB	T_8 + 710.0
05:03:07.4	Engine Mainstage Control Valve Open On	S-IVB	T_8 + 720.0
05:03:07.6	Engine HE. Control Valve Open On	S-IVB	T_8 + 720.2
05:04:36.4	Engine Mainstage Control Valve Open Off	S-IVB	T_8 + 809.0
05:04:36.6	Engine HE. Control Valve Open Off	S-IVB	T_8 + 809.2
05:08:10.6	LOX Tank NPV Valve Open On	S-IVB	T_8 + 1023.2

Table 4.3-1 Typical Saturn V Flight Sequence, Time Base 0 through 8 (Cont)

Nominal Flight Time Hr:Min:Sec	Command	Stage	Time from Base (Seconds)
05:08:12.6	LOX Tank NPV Valve Latch Open On	S-IVB	T_8 + 1025.2
05:08:13.6	LOX Tank NPV Valve Open Off	S-IVB	T_8 + 1026.2
05:08:14.6	LOX Tank NPV Valve Latch Open Off	S-IVB	T_8 + 1027.2
05:08:16.8	Engine HE. Control Valve Open On	S-IVB	T_8 + 1029.4
05:20:51.1	LH_2 Tank Repressurization Control Valve Open Off	S-IVB	T_8 + 1800.5
05:23:50.5	LH_2 Tank Latching Relief Valve Open On	S-IVB	T_8 + 2031.0
05:23:51.7	Aux Hydraulic Pump Flight Mode Off	S-IVB	T_8 + 2032.2
05:23:52.5	LH_2 Tank Latching Relief Valve Latch On	S-IVB	T_8 + 2033.0
05:23:53.5	LH_2 Tank Latching Relief Valve Open Off	S-IVB	T_8 + 2034.0
05:23:54.5	LH_2 Tank Latching Relief Valve Latch Off	S-IVB	T_8 + 2035.0
05:23:55.0	Engine HE. Control Valve Open Off	S-IVB	T_8 + 2330.0
05:23:55.2	Passivation Disable	S-IVB	T_8 + 2330.2
05:37:47.4	S-IVB Ullage Engine No. 1 On	S-IVB	T_8 + 2800.0
05:37:47.6	S-IVB Ullage Engine No. 2 On	S-IVB	T_8 + 2800.2
05:42:27.4	S-IVB Ullage Engine No. 1 Off	S-IVB	T_8 + 3080.0
05:42:27.6	S-IVB Ullage Engine No. 2 Off	S-IVB	T_8 + 3080.2
05:50:40.2	Engine Pump Purge Control Valve Enable Off	S-IVB	T_8 + 3600.4

CHAPTER 5
MEASURING AND TELEMETRY

SECTION 5.1
INTRODUCTION

The combined measuring and telemetry system is essentially an independent operating subsystem within the overall Astrionics System.

The combined measuring and telemetry systems of the Saturn Launch Vehicles measure physical quantities and signals onboard the vehicle and transmit the data to ground stations. The complexity of the launch vehicle and its missions dictate a large number of measurements. The data transmitted by the measuring and telemetry systems supply information for the following operations:

- Automatic preflight checkout of the vehicle.
- Monitoring of vehicle performance during powered flight.
- Postflight evaluation of vehicle performance.
- Monitoring and checkout of the vehicle during orbital flight.
- Verification of commands received in the vehicle from ground stations.

Figure 5.1-1 illustrates the signal flow through the system. The transducers convert the physical quantities to be measured (e.g., pressure, temperature, etc.) into electrical signals. These signals are modified, when necessary, by signal conditioning devices into voltages suitable as inputs to the telemetry system. Some quantities are already in electrical form and need no transducers or conditioning. The measuring distributor feeds the conditioned signals

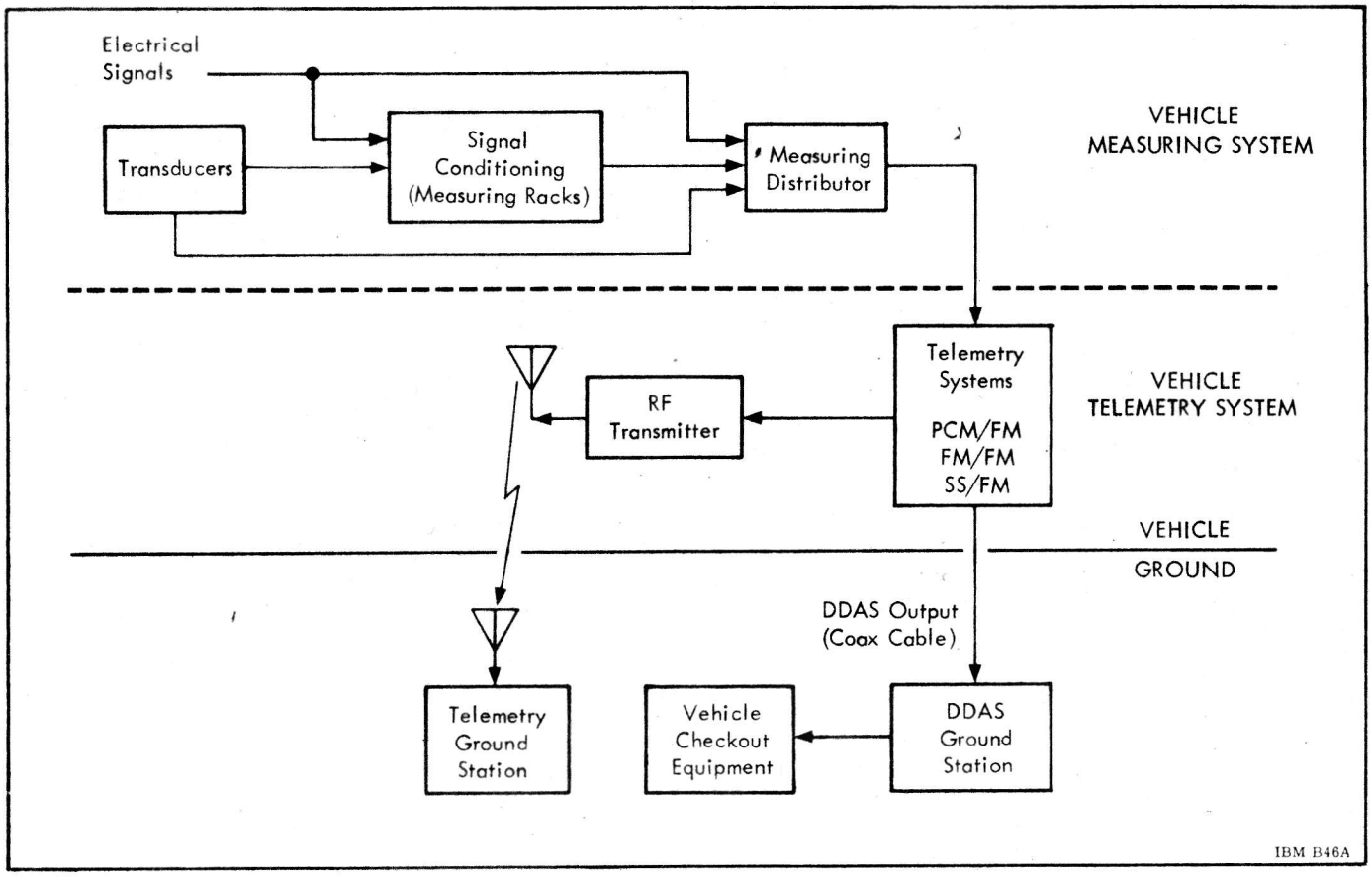


Figure 5.1-1 Measuring and Telemetry System

to the telemetry system. In the telemetry system, the signals are inserted on rf carriers and transmitted during flight to the telemetry ground stations. Before launch, the measuring and telemetry systems send digital data by coaxial cable from each stage of the vehicle to the checkout facility. The digital information is used for automatic checkout of the vehicle on the launch pad. In this mode, the telemetry system operates with the launch site Digital Data Acquisition System (DDAS).

Each stage of the launch vehicle has an independent measuring and telemetry system, DDAS output, and rf transmission equipment. In addition, the PCM telemetry system of the S-IVB Stage is interconnected with the PCM telemetry system in the IU for redundant transmission of some important measurements.

For monitoring of digital data, the IU telemetry system has an interface with the LVDC through the LVDA. As the measuring and telemetry system in each stage is essentially the same, the IU measuring and telemetry system will be used as an example throughout this chapter.

To simplify vehicle checkout, data handling, etc., standardization is practiced wherever feasible. A remote automatic checkout system is standardized on each stage to provide automatic checkout of measurements from ground equipment.

An airborne television system is also used to transfer data from the vehicle to the ground. This system is used on Saturn V Vehicles to observe the propulsion engines during flight.

SECTION 5.2
MEASURING SYSTEM

5.2.1 GENERAL

The measuring system includes transducers, measuring racks (which contain the signal conditioning modules), measuring distributors, measuring rack selectors, and measuring voltage supplies. The measuring system converts the signal or quantity to be measured into an electrical signal that is acceptable to the telemetry system. According to this definition, the measuring system ends at the input to the telemetry system (at the subcarrier oscillator, multiplexer, etc.). Figure 5.2-1 illustrates typical components of the measuring system. The measurements in the launch vehicle cover the areas of:

Propulsion	Guidance and
Structure	control .
Flight mechanics	Environment

Physical quantities to be measured, such as, pressure, temperature, and vibrations must be transformed by transducers into electrical signals for transmission by telemetry. Measurements of electrical signals (voltages, currents, and frequencies) originating in onboard equipment are used for monitoring the performance of this equipment and the sequence of flight events (e.g., stage separation, engine cutoff, and others). The signals to be measured exist in analog and digital form. Measurements of all electrical signals do not require transducers.

The measurements made in the various stages of Saturn IB and V Launch Vehicles are listed in Table 5.2-1. The number and type of measurements given in the table are best estimates and are subject to changes as the development of vehicles proceeds. This applies particularly to the figures for operational vehicles since a larger number of measurements is necessary for performance evaluation and testing of research and development vehicles. Because of the large number of different measurements, no detailed list of measurements is given. Table 5.2-2 indicates some of the quantities measured in a typical Saturn V Vehicle.

Certain measurements will be used as inputs to the emergency detection system (see Chapter 4). Operational measurements are those measurements used for flight (mission) control. Operational measurements indicate the state of the vehicle and its systems and also provide trend information (beginning with the orbital flight phase). All operational measurements are transmitted over the PCM telemetry links of the S-IVB Stage and the IU. Typical operational measurements for the Saturn V Vehicles are given in Table 5.2-3.

5.2.2 TRANSDUCERS

Generally, transducers change energy from one form to another. In measuring techniques, they are used as electromechanical measuring instruments which contain sensing devices for converting mechanical and environmental quantities into electrical signals. Evaluation of vehicle performance and in-flight monitoring requires the measurement of a large variety of physical quantities onboard the vehicle. Therefore, many different types of transducers are used. Some typical transducers and the corresponding measurements are listed in Table 5.2-2. Because of the many types of transducers and measurements used in launch vehicles, no attempt is made to give a complete description of all transducers on each stage. The following measurement descriptions generally apply to the S-IB and S-IC Stages. The number of transducers used in each stage may be found in Table 5.2-1. Figure 5.2-2 illustrates several typical transducers.

BENDING MODE VIBRATION MEASUREMENTS (ALL STAGES)

Bending measurements are made using force-balance accelerometers. The principle of operation of the force-balance accelerometer is shown in Figure 5.2-3. These instruments operate as a subminiature servosystem, which is responsive to linear acceleration along its sensitive axis. Due to inertia, the acceleration sensitive mass, commonly called the paddle wheel, moves relative to the position de-

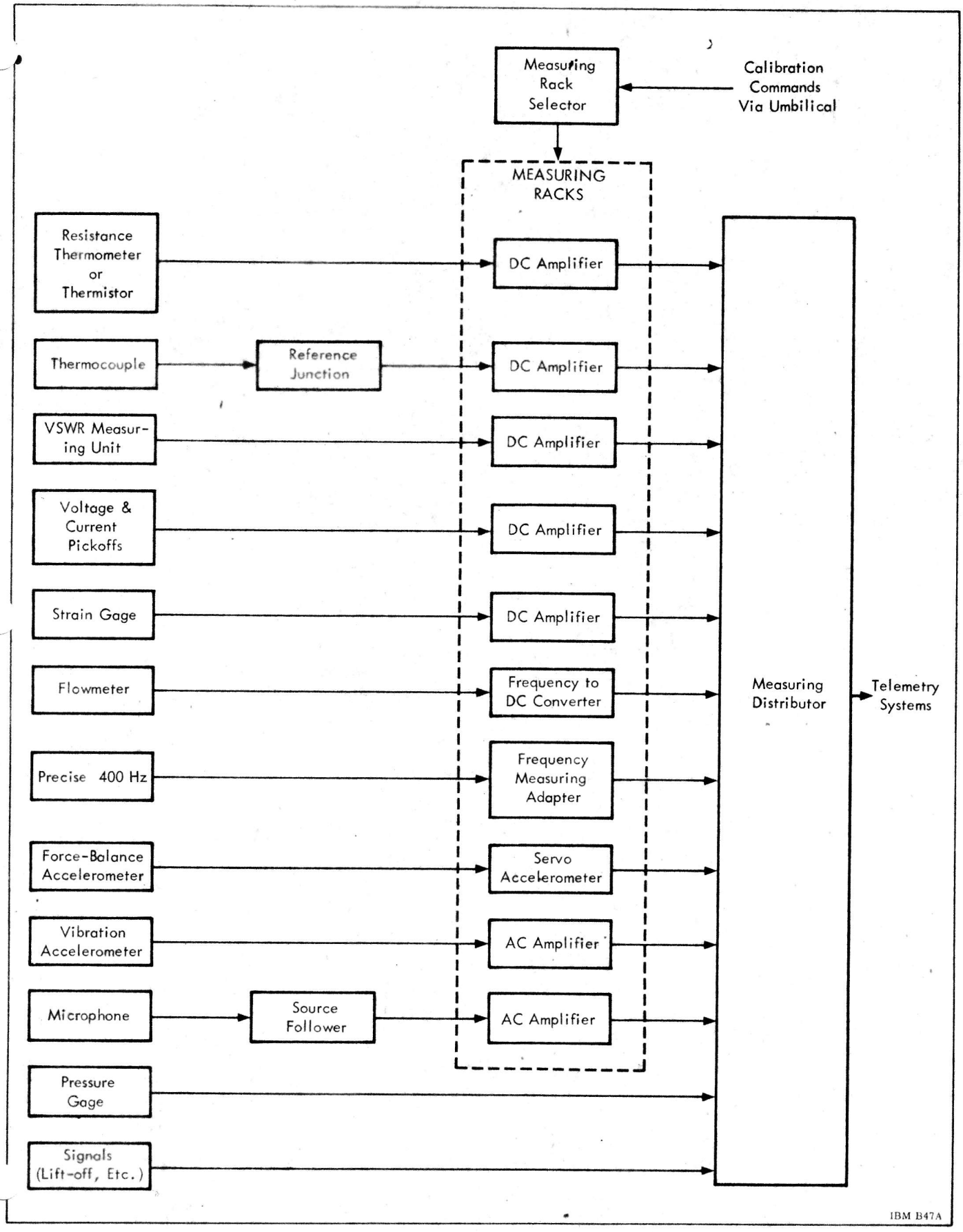


Figure 5.2-1 Typical Saturn Measuring System

Table 5.2-1 Number of Measurements, Transducers, and Measuring Racks (Typical)

SATURN IB						
Stage	Measurements R & D	Measurements Oper	Transducers R & D	Transducers Oper	Measuring Racks R & D	Measuring Racks Oper
S-IB	403	263	305	106	19	5
S-IV B	513	218	298	115	17*	7*
IU	315	200	92	45	9	4
Total Vehicle	1231	681	695	366	45	16
SATURN V						
Stage	Measurements R & D	Measurements Oper	Transducers R & D	Transducers Oper	Measuring Racks R & D	Measuring Racks Oper
S-IC	872	297	723	157	27	5
S-II	976	446	589	180	35	8
S-IV B	589	218	298	115	17*	7*
IU	337	215	92	45	10	4
Total Vehicle	2774	1176	1702	497	89	24

* Signal conditioning panels

tector when acceleration is applied. The position-error detector and servoamplifier generate a feedback signal to the restoring mechanism. The electromechanical servoaction results in a balance between the input force proportional to the acceleration and the feedback force proportional to the current in the restoring coil. The restoring current, or the voltage it develops across a series resistor, provides the output of the accelerometer, and is a precise measurement of acceleration.

The advantage of the force-balance accelerometer over earlier potentiometer type accelerometers is that friction is almost negligible. The force-balance accelerometer will sense both extremely slow vibrations and continuous acceleration in a single direction. The same instruments are employed to sense lateral acceleration along the pitch and yaw axes in the IU. Similar measurements are also made to determine the bending or flapping actions of the vehicle fins.

FLIGHT MECHANICS MEASUREMENTS

Longitudinal acceleration measurements are made to measure the thrust decay of engines. These measurements are made with the same type of accelerometers that are used for strain and vibration measurements. Longitudinal acceleration measurements to determine thrust and thrust decay of the S-IVB Stage are made in the IU.

Angular velocity measurements are made using Rate Gyros (see Chapter 3). The instrument is accurate within a range of ±10 degrees per second. In case of a catastrophic situation, the vehicle also carries Rate Gyros to measure angular movement in excess of 100 degrees per second along the pitch and yaw axes.

Propulsion system measurements are made by pressure transducers, flowmeters, tachometers, and liquid level sensors. A brief functional description for each is given in the following paragraphs.

PRESSURE MEASUREMENTS

Pressure measurements are made by two different methods: potentiometric and strain gage.

The potentiometric transducer is basically a wirewound potentiometer with the wiper mechanically connected to a pressure controlled diaphragm as illustrated in Figure 5.2-4. The output voltage is obtained by applying 5 Vdc to the potentiometer. The magnitude of the output will vary from 0 to 5 volts, depending upon the position of the wiper. Since the output voltage is within the limit required by the telemetry subsystem, no signal conditioning is required.

Table 5.2-2 Typical Saturn V Measurements

Quantity Measured	Typical Transducer
Acoustic energy	Microphone
Temperature	Resistance thermometer, thermocouple, or thermistor
Pressure	Bourdon tube or bellows pressure transducers
Vibration	Piezoelectric accelerometer
Liquid flow rate	Turbine-type flowmeter
Liquid level	Level probe
Strain	Strain gauge
RPM (turbopump)	Tachometer
Acceleration	Force balance accelerometer
Position	Potentiometer
Angular velocity	Rate gyro
Voltage, current, and frequency	—
Signals	—
Guidance and Control signals	—
RF & telemetry signals	—

Table 5.2-3
Typical Saturn V Operational Measurements

S-IVB Auxiliary Propulsion System

- Propellant level
- Helium supply pressure
- Propellant temperature

S-IVB Main Propulsion System

- Gas supply pressure
- Propellant valve positions
- Propellant mass
- Engine sequencing signals
- Tank pressure
- Propellant flow
- Thrust chamber pressure
- Hydraulic system pressure and fluid temperature

S-IVB/IU Electrical System

- Battery voltages and currents
- Bus voltages and currents
- Inverter voltages

S-IVB Attitude Control and Stabilization System

- Attitude control signals (pitch, yaw, roll)
- Angular velocity (pitch, yaw, roll)
- Engine actuators position
- Control computer temperature
- Servo amplifier signals
- Spatial amplifier signals
- Valve positions

Navigation, Guidance, and Digital Signal

- Steering commands (pitch, yaw, roll)
- Space fixed velocity (3 components)
- Space fixed displacement (3 components)
- Computer time
- Time to S-IVB second ignition and cutoff
- Accelerometer output (X, Y, Z)
- Gyro servo output (X, Y, Z)
- Gimbal angles (pitch, yaw, roll)
- Launch Vehicle Digital Computer signals
- Temperatures of computer and platform components
- Air bearing supply pressure
- Switch Selector output

Environmental Control System

- Pressure and temperature of coolant at several places
- Cold plate temperature
- Gas supply pressure

Instrumentation and Communication System

- Power output of the PCM transmitter (S-IVB & IU)

Approximately 70 per cent of the total pressure measurements are made with the potentiometric type transducer.

On the S-IB Stage most of the potentiometric type pressure transducers may be calibrated while on board the vehicle by using the calibration valve that is associated with each transducer. The calibration valve, connected between the transducer and the source of pressure being measured, may be coupled to a calibration line that is connected through a quick disconnect coupling to a controlled pressure source. When the calibration line is connected to the valve, the transducer sensor is mechanically positioned to sense the controlled pressure. The transducer automatically returns to sense the system pressure when the calibration line is removed. All other type pressure transducers are calibrated electrically.

In addition to the potentiometric pressure transducer, pressure measurements are made with unbonded strain gages (Figure 5.2-5). Each strain gage transducer consists of four individual strain gages mechanically connected to a pressure sensitive diaphragm and arranged in such a manner that compression on two of the gages results in tension on the other two. This action, in effect, results in an output when the strain gage transducer is excited by an external voltage. The output voltage of the strain gage transducer is approximately 40 millivolts at full pressure; therefore, the signal must be fed into a signal conditioner (dc amplifier) before it can be applied to the subcarrier oscillator. In some cases, the signal conditioning is incorporated in the transducer package.

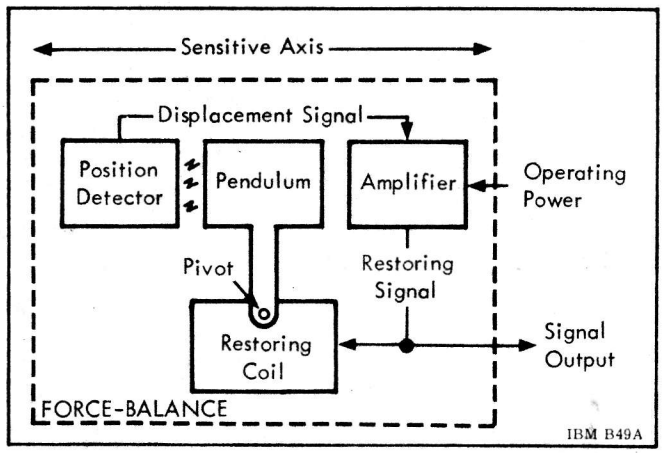


Figure 5.2-3 Force-balance Accelerometer Block Diagram

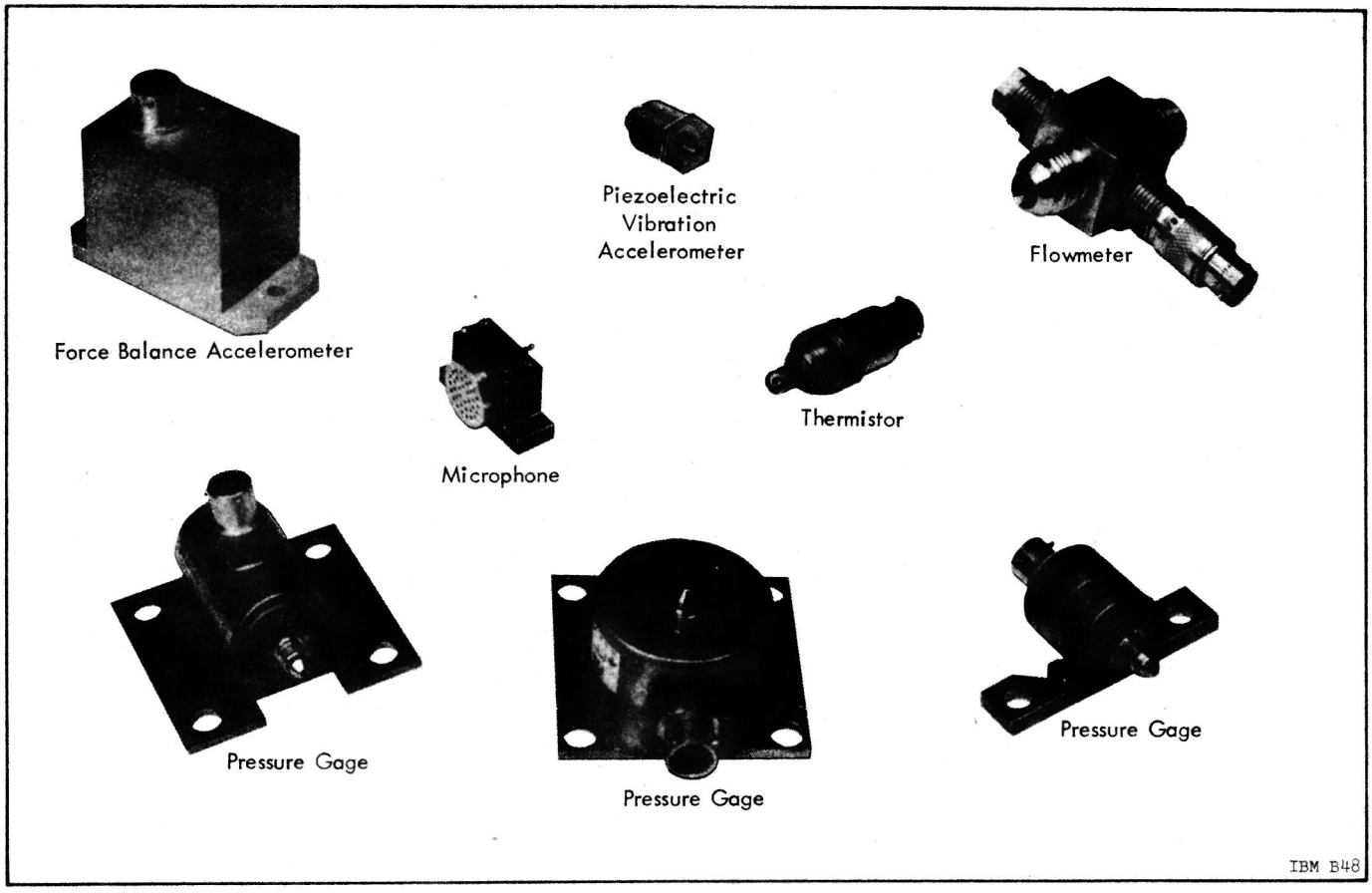


Figure 5.2-2 Typical Transducers

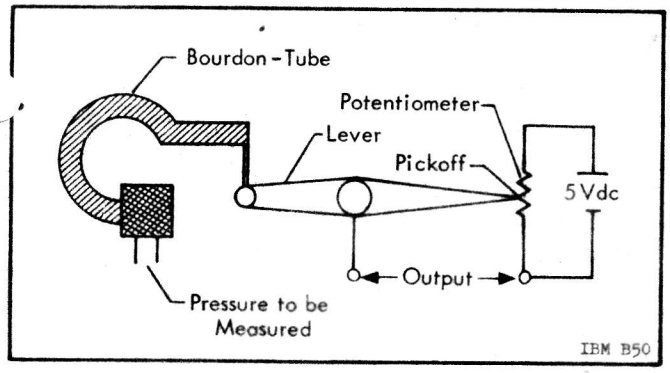


Figure 5.2-4 Bourdon-tube Potentiometer Type Pressure Transducer

RPM MEASUREMENTS (S-IB STAGE ONLY)

This measurement utilizes a variable reluctance type of tachometer mounted on the turbine. As the turbine turns, the varying reluctance of a magnetic path generates an ac voltage. The frequency of the output voltage is proportional to the rpm of the turbine. This frequency is too high for the bandwidth of the available telemetry channels; therefore, signal conditioning is required to divide the frequency by 32 to make the output signal compatible with available telemetry channels.

The signal conditioner is a magnetic frequency divider which uses the rectangular hysteresis characteristics of a saturable core.

LIQUID LEVEL MEASUREMENTS (S-IB STAGE ONLY)

The liquid level of the propellant is measured by two different methods: the discrete and the continuous method. The discrete method (Figure 5.2-6) utilizes a photo-electric cell to obtain signal output. The sensor consists of a light source, photo-electric cell, and a prism. Because the liquid diffuses the light rays, no output is obtained until the level of the liquid drops below the prisms. As the level of the liquid drops below the prism, light rays from the light source are reflected back to the photo-electric cell by the prism faces, which are at 45-degree angles to the light rays. Fifteen sensors are located along the length of the tank. When the output from one sensor is detected, it is possible to determine the amount of propellant (fuel or lox) that was consumed in the time interval that lapsed between outputs from this sensor and one that was previously initiated.

The continuous method of measuring liquid level is used in the lower portion of the propellant tank to determine the amount of propellants remain-

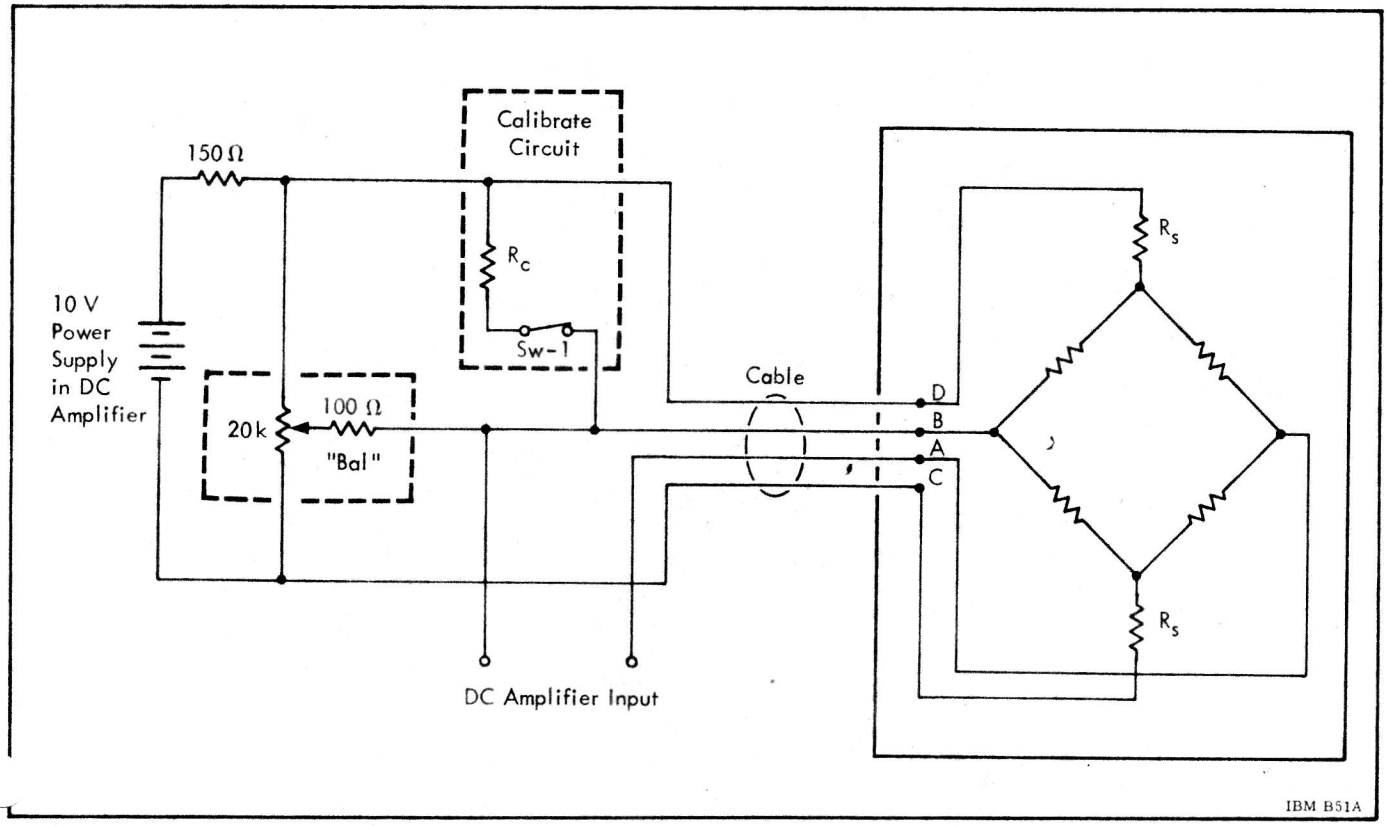


Figure 5.2-5 Strain-gage Type Pressure Transducer

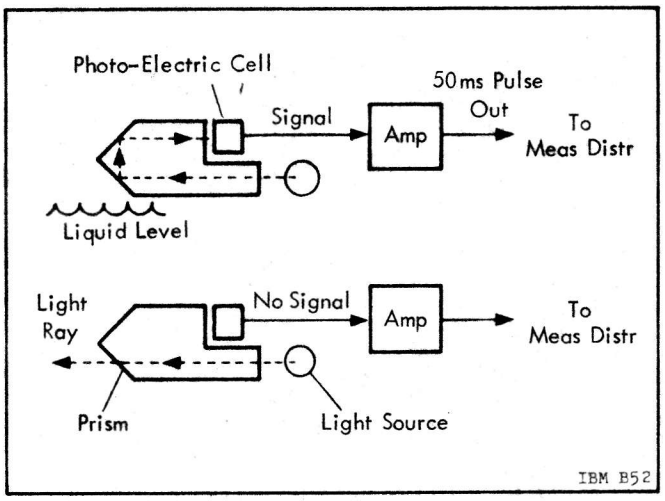


Figure 5.2-6 Liquid Level, Discrete, Functional Diagram

ing after engine cutoff. Principles of operation of the continuous method are illustrated in Figure 5.2-7. The sensor consists of two tandem capacitors with the dielectric being the propellant. The top capacitor (C_s) is approximately 40 inches in length and exhibits a capacitance proportional to the height of the liquid and the dielectric constant of the liquid. The bottom capacitor (C_r) is approximately 3 inches in length and is submerged in propellant when a measurement is made. The capacitance of C_r is proportional to the dielectric constant of the liquid.

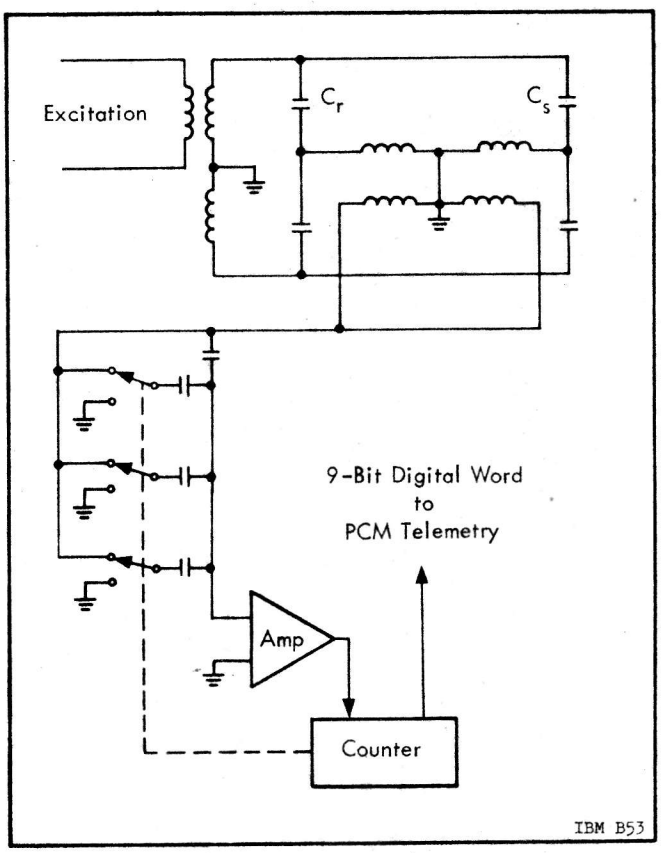


Figure 5.2-7 Liquid Level Sensor Electrical Schematic

Each capacitor is connected in a bridge circuit. The outputs of the two bridge circuits are connected as the excitation to a third bridge circuit which is always kept in balance by an electronic servo system. The feedback elements of the servosystem are nine binary weighted capacitors controlled by a counter. The counter provides a parallel binary output for telemetry.

FLOW RATE MEASUREMENTS

Flowmeters convert the rate of flow of a fluid (amount per unit time) within a pipe into an electrical signal. The rate of flow is represented by the frequency of the signal. The output signal must be signal conditioned to form a 0 Vdc to 5 Vdc signal. Most flowmeters are equipped with a mechanical locking device to prevent damage to the turbine during purge operations.

The flowmeter casing (see Figure 5.2-8) consists of a short piece of pipe the same size as the piping being measured. Within the casing is a free-turning turbine. External to this casing is a coil surrounded by a permanent magnetic field. Fluid pumped through the piping and flowmeter causes the turbine to turn at a rate directly proportional to the velocity of the fluid. The metal turbine blades disturb the magnetic field, thus inducing a current into the coil. This current is changed each time a turbine blade disturbs the magnetic field. The frequency of

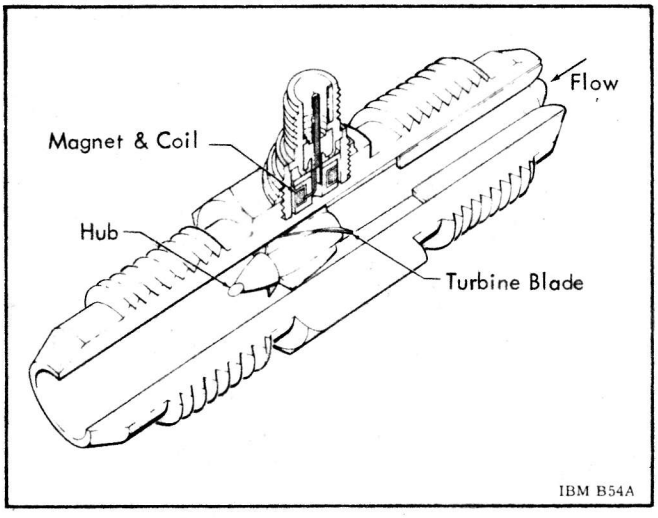


Figure 5.2-8 Basic Principles of a Flowmeter

the current change is proportional to the turbine speed which is proportional to the fluid velocity. The dc signal output is sent to a dc amplifier signal conditioning module or to a frequency to dc converter signal conditioning module.

TEMPERATURE AND RADIATION MEASUREMENTS

The principal temperature and radiation measurements are in the following areas:

- Cryogenic temperature measurements
- Heat flux (radiation and convective)
- Temperature measurements
- Fire detection temperature measurements
- General environmental temperature measurements

Cryogenic Measurements. An important factor in engine operating efficiency is the density of the oxidizer and the fuel. As density is inversely proportional to temperature, temperature measurements are performed at critical points in these systems during flight. The operating efficiency of the engines can be determined from these and other measurements.

Cryogenic measurements are performed by means of resistance thermometers located in the fuel and lox tanks and in the plumbing for both of these systems. These positive temperature-coefficient resistors are fabricated of high purity platinum and require precise calibration techniques.

The maximum temperature range of these devices is from -200°C to +300°C (-328°F to +572°F). Data reduction is accomplished through a straightforward temperature versus resistance method. As in the other temperature measurements, dc amplifiers are employed to increase the output signal level to the required 0 to 5-volt telemetry input level.

Heat Flux (Thermal Radiation) Measurements. Calorimeters are located at strategic points on the engine heat shield to measure thermal radiation and thus permit a precise calculation of the minimum insulation weight allowable at these points.

One type of calorimeter measures both thermal radiation and convective heat transfer. The heating rate is determined from the temperature versus time characteristics of the copper slug.

Another type of calorimeter utilized in some measurements on the Saturn Vehicle is the "thin film" or "membrane" calorimeter. This calorimeter employs a thin disc of constantan welded to a copper heat sink. An insulated copper lead is attached to the center of the disc and another insulated copper lead is attached to the copper heat sink. The temperature differential between the center of the disc and the circumference of the disc produces the emf output which is telemetered to the ground. The emf output of the membrane calorimeter is a linear function of the incident heating rate with the slope of the output curve being determined by the physical size of the constantan disc.

Fire Detection Measurements (S-IB and S-IC Stages Only). The prelaunch fire detection system is operative during the period prior to vehicle lift-off. When the air temperature, measured at critical points, rises at a rate beyond a specified value, an alarm signal is initiated in the blockhouse and an automatic engine cutoff occurs.

A series of thermocouples, arranged in loops with several thermocouples in each loop, are used. The thermocouples are located in back of the heat shield and in the engine compartment. The rate of rise of the temperature of the air is measured in the immediate vicinity of the thermocouple, rather than the radiated heat from some point remote from the measuring device. The system does not define the exact location because of the series loop configuration.

General Temperature Measurements. Surface temperature measurements are made with thermocouples, thermistors, and resistance thermometers. Thermocouples are normally used when the measuring range is 150°C (302°F) or greater, and resistance thermometers and thermistors are used for ranges of less than 150°C. The resistance thermometers are extremely accurate positive temperature coefficient resistors. Thermistors are semiconducting devices which exhibit a high-negative-temperature coefficient of resistance. Ambient air measurements down to -20°C (-4°F) are also performed with thermistors.

Thermocouples and Zone Boxes. Three types of thermocouples are used on the vehicles. In the circuit consisting of 2 metals, an emf will be produced at the measuring junction if a temperature difference exists between the measuring and the reference junctions. The 3 types in use are: chromel/alumel, iron/constantan, and platinum/platinum 10 percent rhodium.

Thermocouples provide measurements of surface heat, fuel temperature, ambient air temperatures, and are used as fire detection gages.

In a laboratory, the reference junction is usually maintained at 0°C (32°F). For vehicular purposes, such a temperature limitation is impractical; therefore, an alternate method has been selected. Changes in reference junction temperature during flight are compensated for electrically by means of a bridge circuit with a resistance thermometer in one leg. A typical bridge circuit with zone box is shown in Figure 5.2-9. The reference junction is contained within the zone box. The zone box is the junction between the vehicle network wiring and the thermocouple leads. A resistance thermometer is in thermal contact with the reference junction. The resistance thermometer has a known positive temperature coefficient. Since the resistance thermometer controls the resistance of one leg of the bridge, the output emf of the bridge circuit will follow the temperature induced emf output of the thermocouple (reference junction). The bridge circuit is so calibrated that it will cancel any emf produced by the reference junction as a result of an increase or decrease in temperature. The dc amplifier increases the output signal level to the required telemetry input level of 0 to 5 volts.

VIBRATION MEASUREMENTS

Vibration measurements are made to determine the structural strength and stability of the Saturn Vehicle. Vibration and stress sensors are mounted on the propellant tanks, turbopumps, engine mountings and engine combustion chamber, and at structural junction points of the vehicle. Two types of accelerometers are used as vibration sensors on board the vehicles; the piezoelectric and the strain gage types.

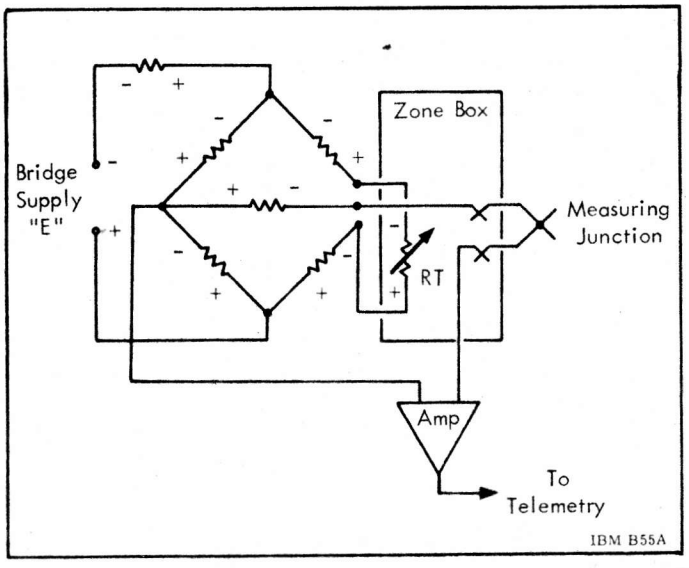


Figure 5.2-9 Typical Bridge Circuit

Piezoelectric Accelerometer. Because of its small size, light weight, and frequency response, the piezoelectric accelerometer is extensively used for flight vibration instrumentation. The frequency response of a typical piezoelectric accelerometer ranges from about 5 hertz to several kilohertz. For flight measurements, the useful frequency response is limited to the bandwidth of the telemetering channel. This type of accelerometer will not respond to near constant acceleration. The effects of vehicular acceleration are thus eliminated from the measurements, and only local vibration is detected by the sensor.

The piezoelectric accelerometer (Figure 5.2-10) consists of a seismic mass which applies a force to a piezoelectric crystal, causing it to generate an electrical signal. The electrical output is proportional to the force applied to the crystal and is an indication of acceleration or vibration. The high-impedance output of the device is coupled to a high-input-impedance emitter-follower stage to maintain adequate low-frequency response.

The emitter-follower can be integral to the accelerometer case, or it can be physically removed but joined electrically through a coaxial cable. Typical sensitivity is in the order of 32 mv/g. Temperature environment is the determining factor in the choice of crystal material to be used. A sufficiently broad range of sensor types is available to permit vibration measurements to be made in almost any temperature environment. The accelerometers are capable of operating up to an acceleration level of several hundred g's and to a lower limit determined by the associated electronic circuits. In flight applications, the range is normally from ±3g to ±70g. Tests have indicated that the acoustic environment encountered on the vehicle will have negligible effect on accelerometer output. This is the sensor most frequently used for vibration measurements.

Strain Gage Accelerometer. The accelerometer (Figure 5.2-11) consists of a mass suspended from strain-sensitive wires connected in a Wheatstone bridge. When a force is applied to the mass, the resistances of the supporting wires change, thus unbalancing the bridge and causing an output voltage. The heavy arrows show the lower resistance circuit of an unbalanced bridge. The extent of the unbalance is indicated by the increase in voltage at the meter. In practice, a bias voltage is used to produce a 2.5-volt potential at the output of the amplifier when the mass is at rest. The bias prevents the output from going negative as the movements of the mass

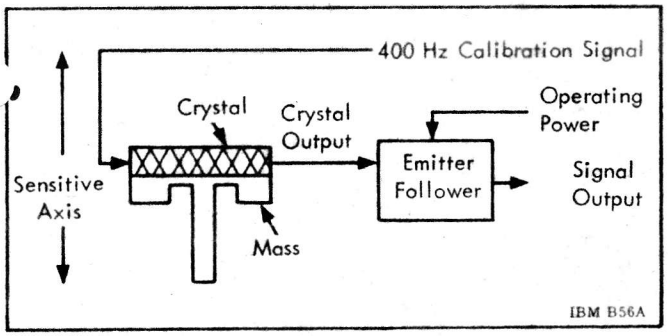


Figure 5.2-10 Piezoelectric Accelerometer and Emitter Follower

is in both directions. Furthermore, the bias confines the output voltage to the 0 to 5-volt range.

ACOUSTIC MEASUREMENTS

An acoustic transducer converts a sound into a proportional electrical signal. The transducer consists of two pieces — a microphone and a source follower (see Figure 5.2-12). The output signal must be signal conditioned to form a 0 Vdc to 5 Vdc signal. As sound is a movement of air molecules, an acoustic transducer can operate only in the atmosphere.

Microphone - The microphone uses the piezoelectric effect of a crystalline structure to produce an output. The unit is sensitive to sound pressure levels of 110 db to 190 db in the frequency ranges of 50 Hz to 3150 Hz. The microphone consists of a crystal solidly bonded to a mass with a sound-sensitive diaphragm attached to the crystal. The microphone is mounted directly to the structure with the diaphragm facing the area to be measured for sound. Sound pressure applied to the diaphragm causes it to vibrate and this vibration causes compression-tension forces to be felt by the crystal. The crystal generates a small electrical signal proportional to the applied sound pressure. The amplitude of the signal represents the db level and the frequency represents the frequency of the sound. The electrical output of another crystal/mass assembly (which is mounted opposite the first) is coupled directly to the output of the first. Unwanted crystal outputs induced by structural vibrations are thus cancelled out and are not felt on the microphone output. The output of the microphone is coupled via coaxial cable to the source follower.

Source Follower - The source follower electrically isolates and increases the current of the microphone output. The source follower is a transistorized unit less than 3 inches in its longest dimension. The source follower receives operating power from the Measuring Rack. The output of the source follower is routed to an ac amplifier signal conditioning module. Prior to launch, the source follower and subsequent

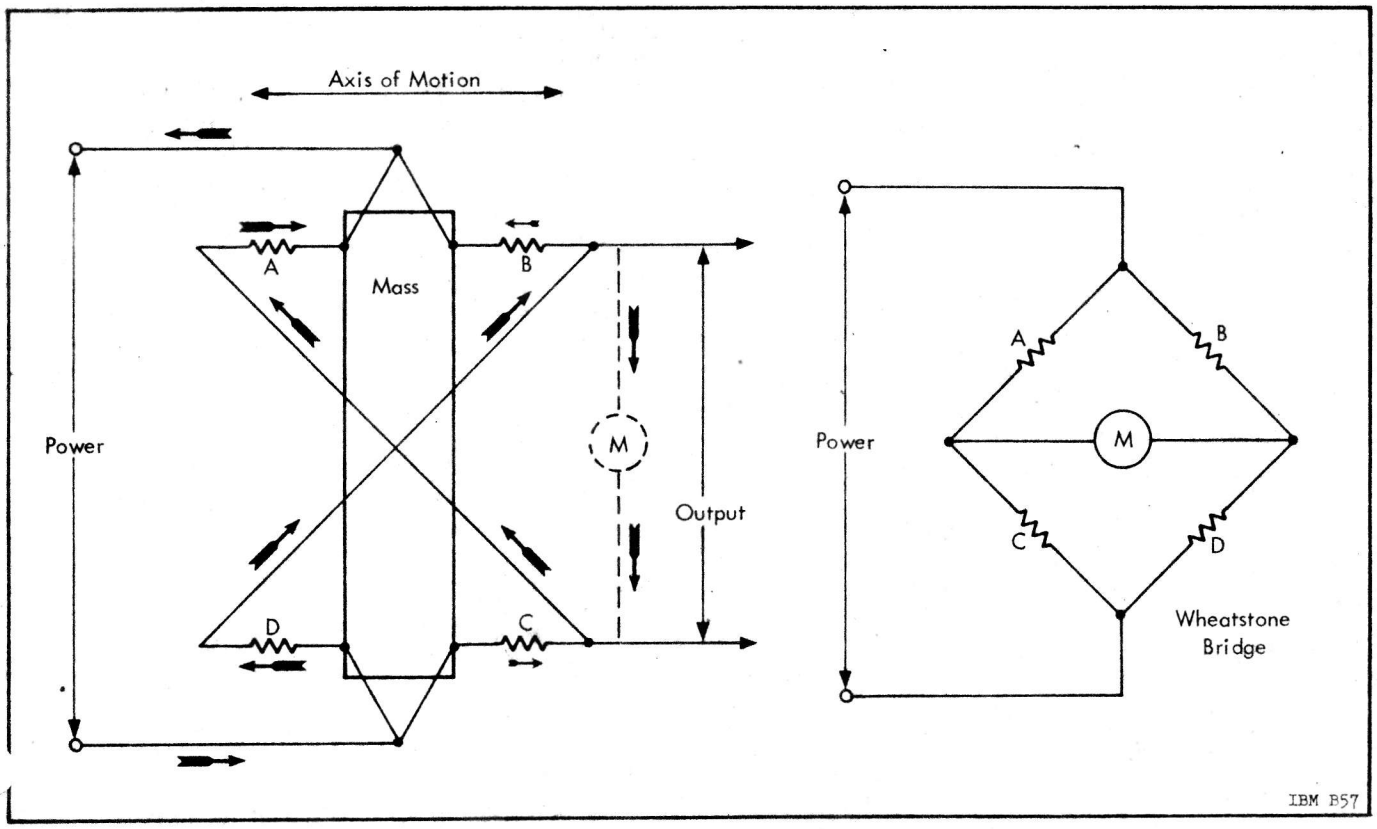


Figure 5.2-11 Strain-gage Accelerometer Block Diagram

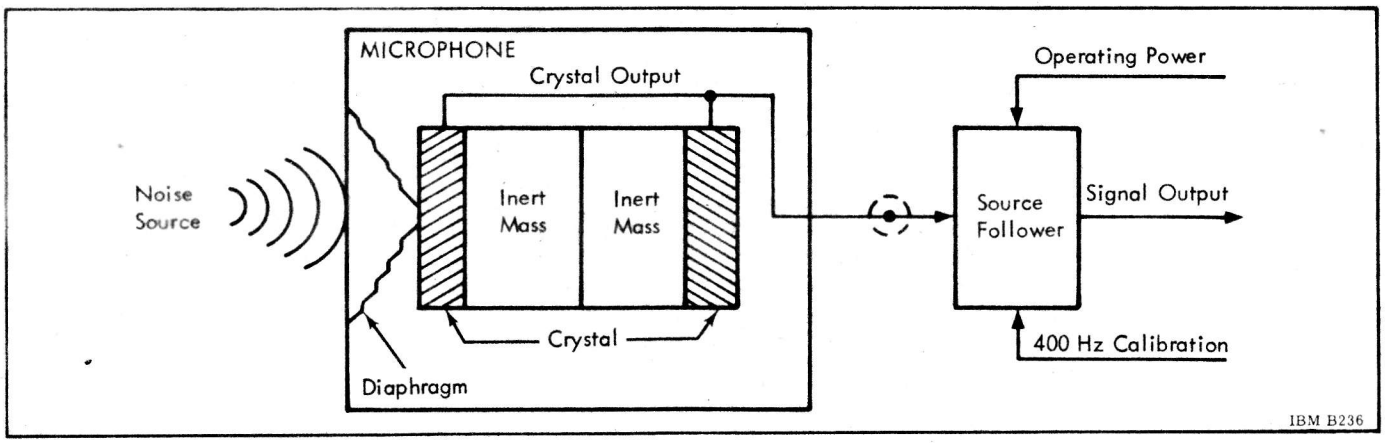


Figure 5.2-12 Acoustic Transducer Functional Diagram

components can be calibrated by application of a 400 Hz signal.

RF POWER MEASUREMENTS

The VSWR measuring unit is used as an rf power transducer. It contains eight coupler assemblies, each of which measures the transmitted or reflected power of a telemetry transmitter. Each of the eight measurement output signals from the unit is low-level dc and is fed to a dc amplifier signal conditioner module.

A typical rf input signal (see Figure 5.2-13) is in the frequency range of 230 MHz to 260 MHz, with 22 watts of power. Each measurement is inductively picked off by a coupling loop inserted into the electromagnetic field about the input signal conductor. The loop is inserted so as to be sensitive to energy travelling in one direction only; therefore, one loop is necessary for transmitted power monitoring and another loop for reflected power monitoring. A crystal detector rectifies the voltage in each pickoff line.

5.2.3 SIGNAL CONDITIONING

The following discussion on signal conditioning applies primarily to the Instrument Unit.

The signal conditioning system takes the signal to be measured and converts it to a signal that is acceptable to telemetry. The signal may be an electrical signal from the vehicle or it may be the output from a transducer. Certain transducers have output signals which do not require signal conditioning. These signals are fed directly to the Measuring Distributor.

A modular concept is used in the IU signal conditioning system. This consists of a number of measuring racks, each having a maximum of 20 measuring modules (channels) plus 2 channel selectors. These modules which plug into the Measuring Rack consist of dc amplifiers, ac amplifiers, channel selectors (for calibration) and other modules. The amplifiers have the provisions for plug-in signal conditioning cards to obtain a very flexible measuring system with a minimum number of components.

The measuring rack is a fabricated sheet metal structure with a tight fitting cover. It is not pressurized or hermetically sealed but has a gasket seal on the cover and a pressure relief valve to maintain a minimum internal pressure of approximately 20.7 N/M^2 (3 psi). The internal electrical connections are made through a multilayer printed circuit board with flexible integral cable to the external connectors. The multilayer board is also the mechanical support for the measuring module connectors. A typical Measuring Rack of the type used in the IU is shown in Figure 5.2-14.

Signal conditioning in other vehicle stages is accomplished in a similar way. Signal conditioning modules are mounted in measuring racks containing 20 modules each. In the S-IVB Stage, signal conditioning modules are mounted on panels distributed throughout the stage. The number of Measuring Racks in each stage is given in Table 5.2-1.

DC AMPLIFIERS

There is only one type of dc amplifier module used on the IU. By making use of individually tailored range cards, this one amplifier is used for measuring temperatures, pressures, currents, voltages, error signals, and other measurements.

The dc amplifier module changes dc measurement signals or low-frequency ac measurement signals to a 0 Vdc to 5 Vdc range. The dc amplifier module physically consists of two parts: a range card and a fixed gain amplifier. The range card plugs into the

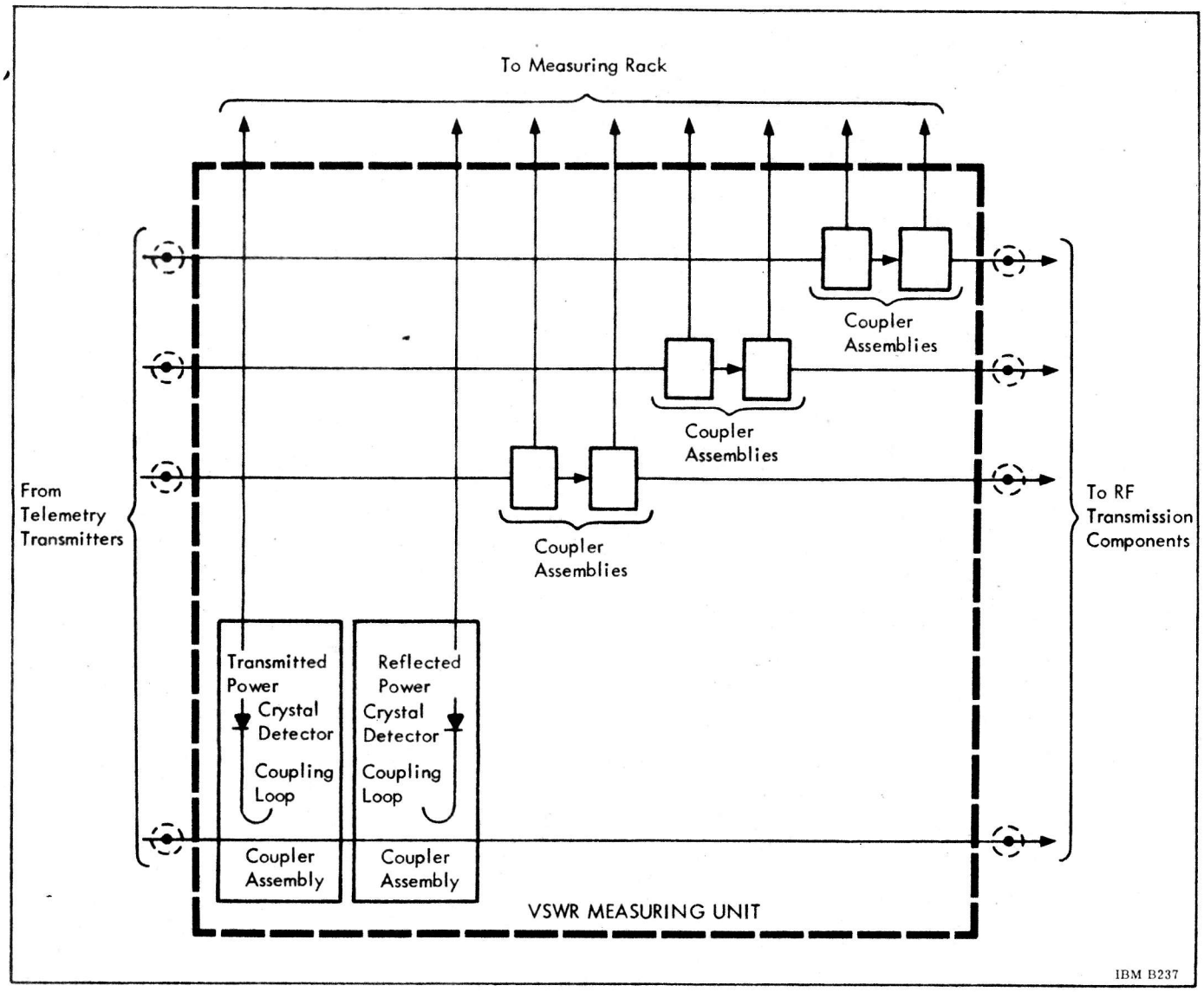


Figure 5.2-13 RF Power Transducer Functional Diagram

amplifier module. Different types of range cards are selected to adapt the measurement signal to the fixed amplifier. Regulated power used by the range card and the amplifier is generated in the amplifier module (see Figure 5.2-15). The output regulator provides a precise 10 Vdc to the range card for use by the bridge network and the calibration network.

The input signal to a dc amplifier module is first routed straight through the amplifier portion to the range card. The range card conditions the signal to a 50 mV range and sends it back to the amplifier portion for amplification to a 5 V range. The amplified signal is then routed back to the range card for addition of bias voltage if necessary. From the range card the signal is returned to the amplifier portion and on out to the measurement distribution equipment.

Two relays are provided for checkout and calibration of the amplifier and associated measuring system. These relays are operated remotely through the Remote Automatic Calibration System (RACS).

AC AMPLIFIERS

Only one type of ac amplifier is used in the IU. The ac amplifier has the same type range card as the dc amplifier. It is used primarily for vibration and acoustic measurements.

The amplifier has a gain of 240 and a frequency response of 50 to 3000 hertz. Since practically all vibration and acoustic measurements are on SS/FM telemetry, the lower frequency response limit was designed to be 50 hertz. The output is transformer isolated from the input and ground.

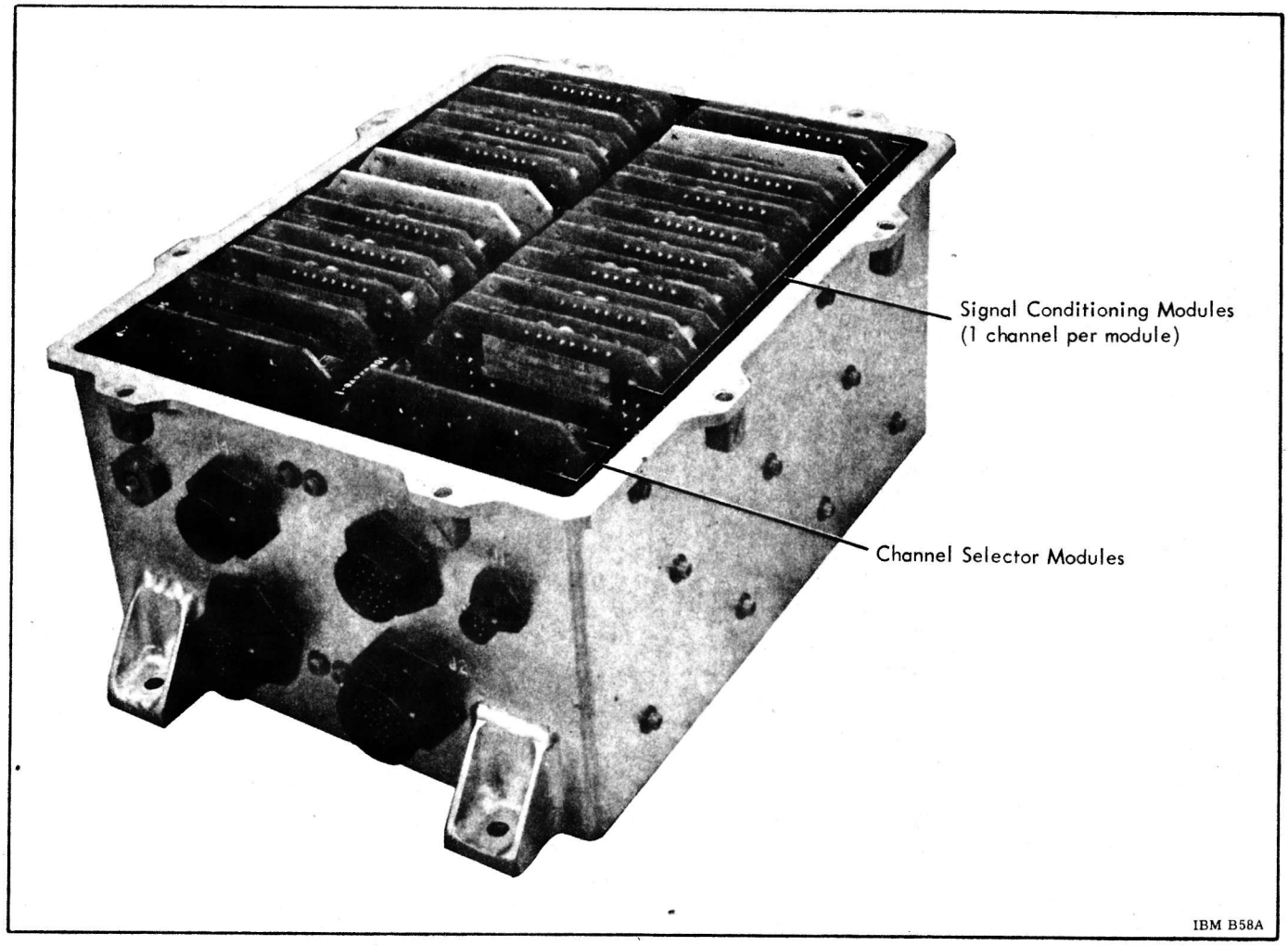


Figure 5.2-14 Typical Measuring Rack

The amplifier contains an internal dc-to-dc converter to supply an isolated power source for the amplifier and to provide an isolated power source for use with the vibration transducers and emitter followers. The ac amplifier has the same type limiting circuits and calibration relays as the dc amplifier.

RANGE CARD

The range card is a printed circuit card used with the dc and ac amplifiers. The card provides the necessary flexibility to obtain the measurements required on the Saturn Vehicle with a small number of different type amplifiers. Thus, only one type of dc amplifier and one type of ac amplifier are used on practically all the measurements requiring signal conditioning. The range card contains bridge completion resistors, calibration resistors, bias networks gain adjustment, or other conditioning circuits.

Range cards are individually tailored to particular measurements but all range cards fall into two general categories: a voltage divider range card which transforms an input voltage into a proportional 50 mV range and a bridge range card which monitors varying resistive networks and transforms the varying resistance into a proportional 0 to 50 mV range. Bridge range cards are used with resistive type temperature transducers (the transducer is the variable leg of the bridge).

A circuit diagram of a typical bridge card for temperature measurements is shown in Figure 5.2-16. In this case, the transducer is a thermistor. Small range changes can be made by the range adjustment potentiometer. By changing resistors, the range can be changed by a large amount and several ranges of temperature can be measured by using one basic range card. The system can be calibrated by using the Remote Automatic Calibration System (RACS) to shunt fixed resistors across the bridge.

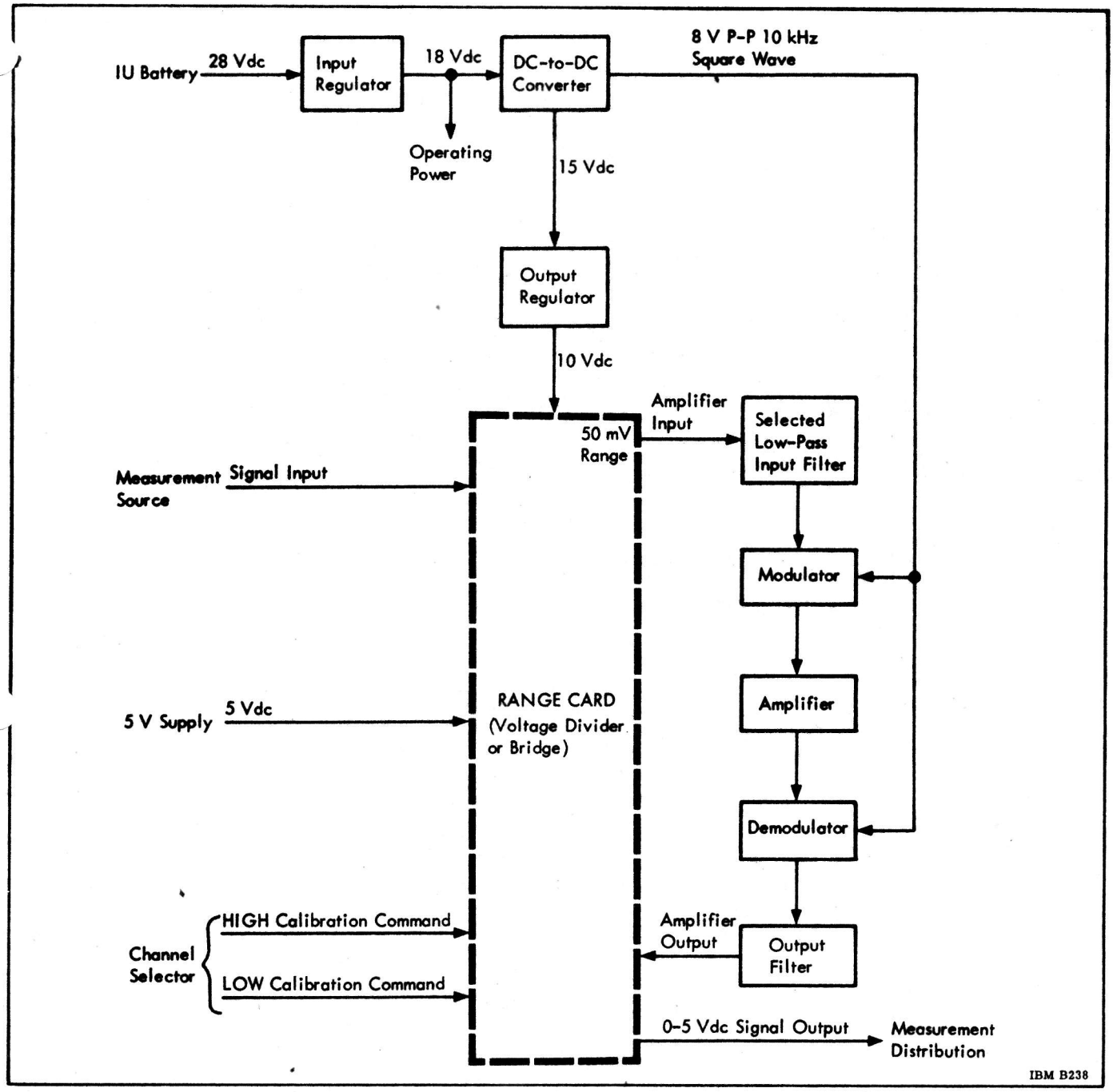


Figure 5.2-15 DC Amplifier Block Diagram

SPECIAL MODULES

There are several measurements that require signal conditioning that are not compatible with the ac or dc amplifier. Special signal conditioning modules are used for these measurements. Examples of these modules are: the frequency-to-dc converter used with flowmeters, the servo accelerometer unit used with force balance accelerometers, and the frequency measuring unit used to accurately monitor the 400-hertz vehicle supply. Most of the special modules have relays for calibration and checkout.

5.2.4 MEASURING DISTRIBUTION

The measuring distributors accept the 0 to 5-volt output of the signal conditioning modules and routes them to the proper telemetry channels. Most measurements in the measuring system are connected to the distributor to be directed to their preassigned channel. The distributors provide versatility in changing channel assignments; changes are made by physically rearranging jumper wires within the measuring distributors. The versatility of the distributors eliminates extensive cable changes and allows channel

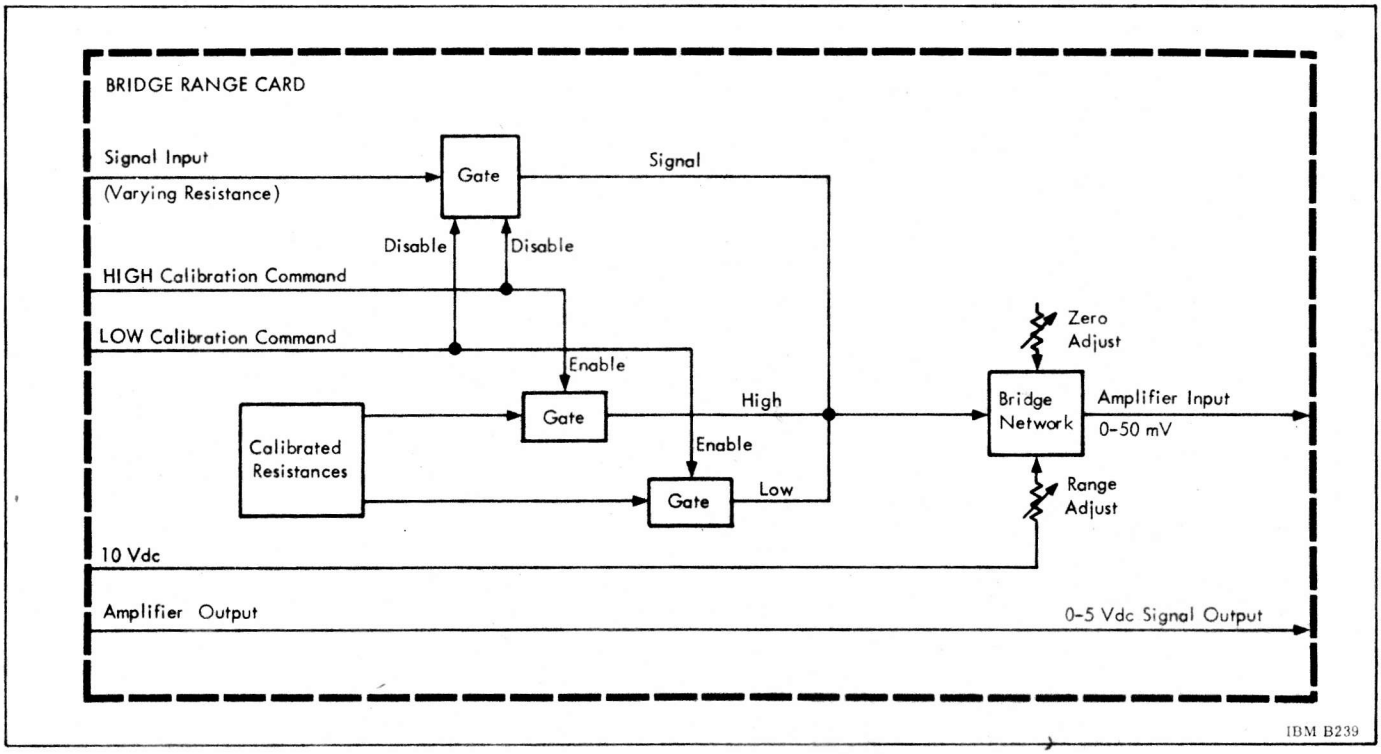


Figure 5.2-16 Typical Range Card for Temperature Measurements

changes to be made during checkout. More than one measuring distributor may be used depending on the number of measurements to be made and the physical location within the IU of the measurements to be made.

Switching functions connect different sets of measurements to the same telemetry channels during different flight periods. These switching functions, controlled by the Control Distributor, are performed in the Measuring Distributor. Switching functions, controlled from the ground via the umbilical cable, connect measurements not required during flight to digital data acquisition system channels for ground checkout and return the channels to flight measurements after checkout.

5.2.5 MEASUREMENT CALIBRATION

The Remote Automatic Calibration System (RACS) permits a remote calibration of the measuring system prior to launch. During vehicle checkout, calibration of measurements is accomplished through use of the RACS. Any corrections required can be made by adjusting potentiometers on the amplifier range cards. If the measuring system drifts or deviates from the final adjustments, the data obtained from RACS is used to correct the flight data for more accurate measurements.

Each signal conditioning module contains 2 relays and the necessary circuit to simulate the transducer as well as the upper (HI) end and the lower (LO) end of the signal range for that particular measurement. The transducer is connected to the module when the RACS is in the RUN mode.

A binary-coded signal is sent from the GSE through the umbilical cable to the Measuring Rack Selector in the vehicle to select a particular measurement for calibration. Figure 5.2-17 shows the RACS for the IU. Each stage has a separate RACS. The signals are generated in the GSE either by a manual keyboard or from a computer program. These signals are decoded on the vehicle and distributed to the various Measuring Racks to operate the checkout relays.

The calibration command signal consists of 13 bits in parallel. There are 6 bits for rack selection, 5 bits for channel selection, and 2 bits for mode selection. (One checkout relay in each module is for the HI mode checkpoint, and the other is for the LO mode checkpoint.) The same code is used on all stages to provide a 31-rack capacity. The IU RACS is designed for 14 racks.

On the vehicle, the code is received in the Measuring Rack Selector. The rack select code is decoded and the signal is addressed to the proper Measuring Rack. Buffer circuits for mode codes and channel codes are provided in the Measuring Rack Selector which acts as a distribution point to the various Measuring Racks. The signals go to the channel selector module in the selected Measuring

Rack. Operation of the channel selector requires the following conditions:

Rack select signal present
Channel select signal present
Mode signal present (HI or LO)

There are two channel selectors in each Measuring Rack. One decodes channels 1 through 10 and the other decodes channels 11 through 20. The channel selector contains the necessary diode matrices and latch circuits to complete the operation of the RACS.

The channel select modules contain 20 AND gates. When the 3 conditions mentioned above are fulfilled, the addressed AND gate "latches in" and energizes the corresponding calibration relay in the signal conditioning module. This relay will remain energized until another signal is sent to change the mode.

In addition to HI and LO modes, there is a third mode of operation, called RUN mode, which is selected when both calibration relays are in an unenergized state. The RUN mode is the normal mode of operation with the transducer or input signal connected to the signal conditioning module. During calibration (following HI or LO mode), the RUN mode is achieved by sending the proper code to the vehicle. Since the RACS is used only before launch, it is wired in such a way that the power is removed at launch. Removal of the power causes all relays to switch to RUN mode. This eliminates the possibility of leaving any module in the checkout state (HI or LO).

Any number of channels can be selected individually, simultaneously, or in any sequence or combination (with any combination of a HI, LO, or RUN selection at the GSE keyboard). The GSE display panels are used to monitor the signal (code) sent to the vehicle (there is no code feedback from the vehicle). The calibration results are observed through the telemetry system and connected ground checkout system.

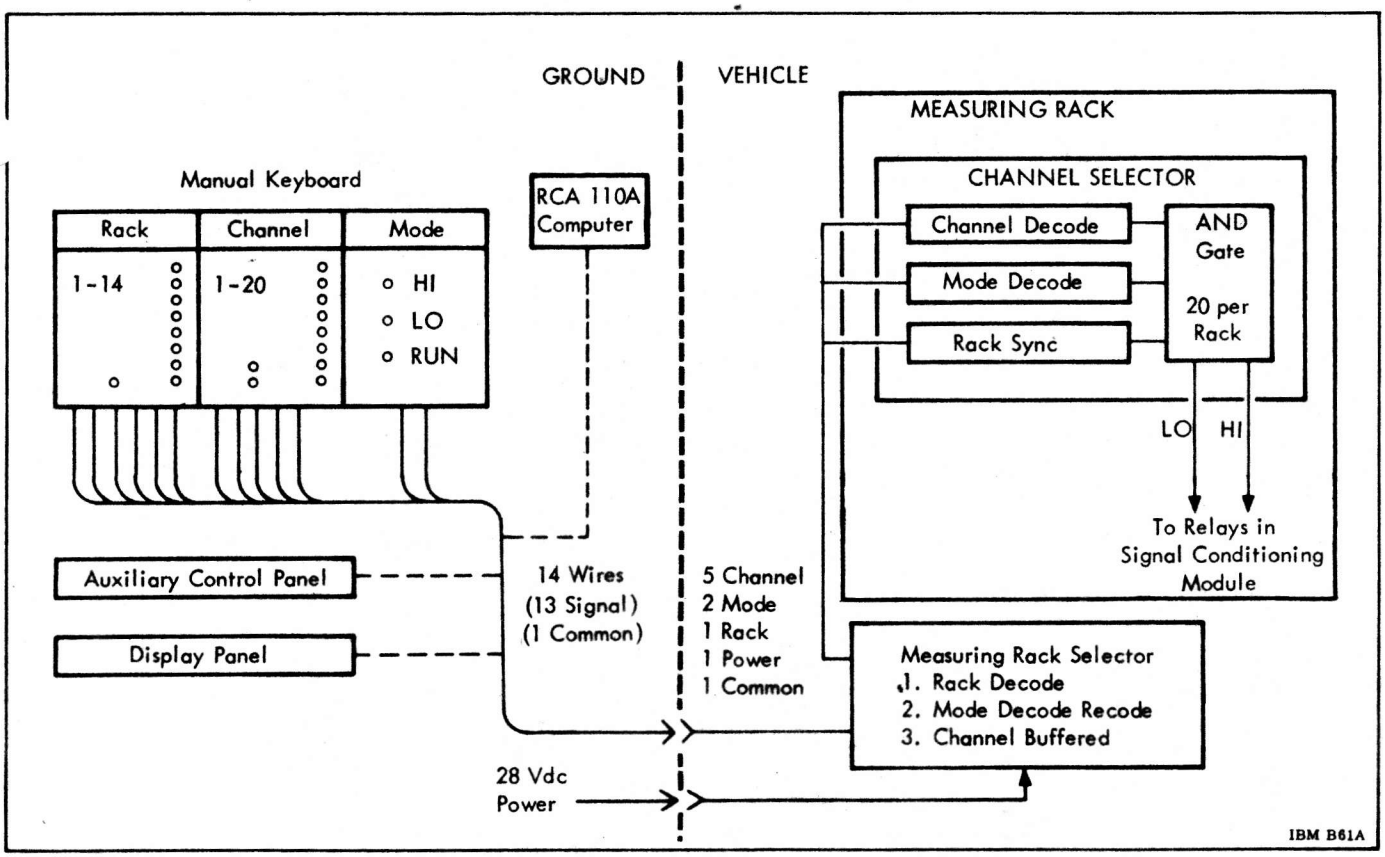


Figure 5.2-17 Block Diagram of RACS for the IU

SECTION 5.3
TELEMETRY

5.3.1 GENERAL

Each stage of the Saturn Vehicle carries an independent telemetry system. These systems modulate the signals from the measuring system onto RF carriers for transmission to ground stations. Three different modulation techniques are applied in the telemetry system of each stage:

- FM/FM telemetry uses frequency modulation/frequency modulation with Pulse Amplitude Modulation (PAM) and triple Frequency Modulation (FM^3) as auxiliary techniques
- SS/FM telemetry uses single sideband modulation/frequency modulation
- PCM/FM telemetry uses pulse code modulation/frequency modulation

These different modulation techniques provide efficient transmission of the large number and variety of measuring data which have different requirements of bandwidth and accuracy (Table 5.3-1).

DATA CATEGORIES

Low-response/low and medium-accuracy data may be sufficiently defined by sampling at a rate of 10 hertz, or less. In terms of frequency response this would be 2 or 3-hertz maximum variation. This category includes temperature, pressure, and other measurements where rapid variations are not very likely or are not of interest.

Low-response/high-accuracy data requires accuracies of 1 percent or better. Examples are longitudinal acceleration and combustion chamber pressure measurements.

Medium-response/medium-accuracy data requires a 5 to 40-hertz response. Data in this category can be handled by sampling at 100 to 125 hertz per channel or less, or by FM/FM channels below the 3-kilohertz subcarrier using the standard deviation ratio of 5.

High-response/medium-accuracy data requires a 50 to 1000-hertz channel response. This type of data is readily handled by FM/FM subcarriers.

Wideband low-accuracy data has a bandwidth of roughly 50 to 3000 hertz and normally no dc component of interest. Vibration data and sound intensity fall within this classification.

Event measurements constitute a special category. Interest in this data is limited to whether or not

Table 5.3-1 Data Categories

Type	Frequency Response (hertz)	Accuracy Required (percent)
1. Low-response/low and medium-accuracy	2-3	2-5
2. Low-response/high-accuracy	2-3	1
3. Medium-response/medium-accuracy	5-40	2
4. High-response/medium-accuracy	50-1000	2
5. Wideband low-accuracy	50-3000	5
6. Event measurements	---	---
7. Digital measurements	---	---

an event has occured and, if so, the time of occurrence with respect to a specified time resolution.

In addition, much data originates in digital form; e.g., signals from the LVDC

MODULATION METHODS

The wideband data-carrying capability of standard FM/FM telemetry is very poor. The FM/FM system has one channel with a frequency response of 0 to 1050 hertz at a subcarrier deviation ratio of 5; the other channels have decreasing frequency responses down to 6 hertz. The sum of all the channel bandwidths is only 4700 hertz. The bandwidth efficiency of a standard FM/FM system with subcarriers operating at a deviation ratio of 5 is about 1.6 percent. A corresponding figure for a PAM/FM system is about 3.5 percent; for a PCM/FM system, it is about 3.0 percent.

The necessity to transmit wideband data (acoustic and vibration measurements) led to the use of SS/FM telmetry. An rf carrier is frequency modulated with single-sideband, amplitude-modulated carriers. The bandwidth efficiency of such a system is roughly 10 times greater than that of FM/FM. It is capable of transmitting 45 kilohertz of data over the same bandwidth used by the FM/FM link to transmit 4700 hertz of data.

A theoretical comparison of the signal/noise performance of the SS/FM with a standard FM/FM system is useful. Since single-sideband subcarriers do not possess wideband gain, it would logically be expected that SS/FM would perform less favorably in this respect than FM/FM, probably by a factor equal to $\sqrt{3}$ times the deviation ratio, which is the wideband gain of the FM subcarrier. However, if the modulating signal of such a system is to be vibration data, other factors can more than compensate for the lack of wideband gain in the subcarrier.

These compensating factors result from a prior knowledge of the nature and characteristics of vibration data. A Gaussian or normal curve is a good approximation of amplitude distribution characteristics of such data. Since the summation of Gaussian functions is a Gaussian function itself, the composite signal modulating the transmitter (in an SS/FM system carrying vibration data) could be expected to resemble a Gaussian function. The peak-to-peak amplitude of the data applied to an FM subcarrier must be limited to the band edges of the subcarrier channels, the deviation being ± 7.5 percent of center frequency, to prevent adjacent channel interference. Thus, when data possesses a high peak-to-rms ratio, the signal capacity of the channel is reduced below its signal capacity for a sine wave modulating signal (1.41 peak-to-rms ratio). Correspondingly, Gaussian data with a peak-to-rms ratio of 4.0 reduces rms data capability to 2.83.

No such inherent peak data restriction exists in the SS/FM system. The data peaks of the individual channels add in a random manner, resulting in an amplitude distribution of the composite signal similar to that of the data at the channel inputs and having a peak factor of approximately the same magnitude. Thus, with Gaussian-type characteristics and an identical number of channels, the SS/FM system will accommodate two or more times as much peak carrier deviation per channel as an FM/FM system.

Data which originates in digital form and data requiring high accuracy are transmitted through the PCM/FM system. The digital data transmission link is relatively insensitive to imperfections in the transmission channel. Above a threshold noise level, the accuracy is not appreciably affected by noise in the channel. Nonlinearity in the transmission channel is of little consequence. By a relatively simple and reliable operation, the serial digital data which contains noise and deteriorated rise time can be regenerated into its original noise-free form.

Also, digital data transmission is compatible with real-time data processing by digital computers at ground stations. A separate digital data output of the PCM/FM system is used for automatic preflight checkout of the launch vehicle. This is called the Digital Data Acquisition System (DDAS). A Mod 301 PCM/DDAS Assembly in the PCM/FM system is connected with the LVDC for checkout of the S-IVB/IU Stage in orbit. During flight, all operational data is transmitted over the PCM/FM link.

MULTIPLEXING METHODS

To increase the data handling capacity of telemetry systems, several data channels are multiplexed. Two types of multiplexing are utilized: frequency-division multiplexing and time-division multiplexing.

Frequency-division multiplexing is the process of simultaneous frequency sharing of one rf carrier transmission link by dividing the available bandwidth into a number of channels, each with a separate center

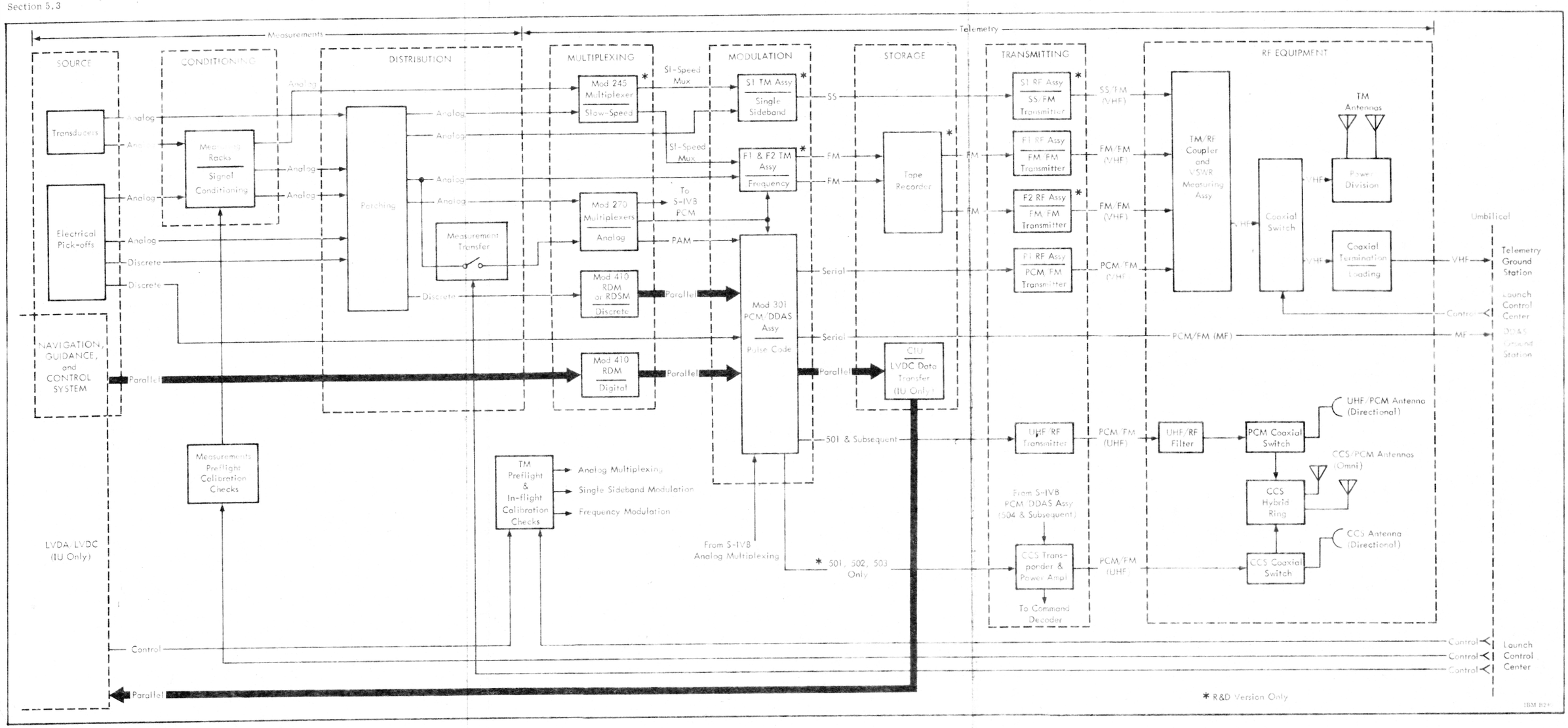


Figure 5.3-1 Saturn V Instrumentation System Functional Data Flow

frequency. Spacing is provided between these channels to allow each channel to be frequency modulated or deviated about the center frequency. After modulation occurs, the subcarrier signals are combined linearly, and the resultant composite signal is used to frequency modulate an RF carrier. FM/FM and SS/FM are examples of this frequency division multiplexing.

Time-division multiplexing is the process of sequential sampling of two or more data sources and applying the data samples to a common output in a fixed sequence. The samples may or may not be separated by a "dead time" space. Usually some marker is made a part of the output signal to designate the beginning or end of a sampling cycle. This is for identification and synchronization purposes at the data reduction point.

The Saturn telemetry systems make use of several types of time-division multiplexers. The Mod 270 Multiplexer Assembly is a time-division multiplexer for analog data. It is used in conjunction with the FM/FM telemetry system and the PCM/FM system. The Mod 245 Multiplexer Assembly provides time-division multiplexing for wide-band data and is used for SS/FM telemetry and FM/FM telemetry. The remote digital submultiplexers and digital multiplexers are used in connection with the Mod 301 PCM/DDAS Assembly. Remote analog submultiplexers are used for analog data connected to the Mod 270 Multiplexer Assembly.

TRANSMISSION CARRIERS

The number of RF carriers allotted to each modulation technique is chosen to provide an appropriate balance of data transmission capability to handle the quantities and varieties of data originating on the stage. The telemetry equipment associated with each stage consists of a "building-block" arrangement, which may be connected in numerous combinations to satisfy specific measuring requirements. The number of carriers allocated to FM/FM, SS/FM, or PCM/FM and also the specific combination of building blocks vary from stage to stage and from vehicle to vehicle.

TYPICAL S-IVB/IU TELEMETRY SYSTEM

Figure 5.3-1 is a functional flow diagram of a typical instrumentation system for Saturn V. Flight (mission) control data is sent in parallel to the IU PCM/FM and S-IVB PCM/FM systems as indicated in the figure. Therefore, in the event of a failure in one of the PCM systems (IU or S-IVB), the other PCM system can be used to transmit the flight control data. In operational vehicles, the number of multiplexers and FM/FM systems will be reduced, and the SS/FM telemetry will be omitted.

Table 5.3-2 lists the type and number of telemetry systems and multiplexers used in the stages of Saturn Vehicles. Because of the smaller quantity of measurements required in operational vehicles, the number of telemetry systems is also reduced. (Figures given for operational vehicles are "best guess" at the present time.)

From one to six time-division multiplexers are synchronized from a central timing source located in the PCM/DDAS Assembly. Each time-division multiplexer provides an output to the PCM/DDAS Assembly which combines the outputs into a single serial wavetrain. The individual analog samples are digitized and combined into a digital format which is transmitted via coaxial cable to the ground checkout equipment. This data is also transmitted via a PCM/FM carrier for in-flight monitoring.

Each of the time-division multiplexers has a second data output which is identical to the output provided to the PCM/DDAS Assembly except that it is conditioned for PAM transmission. These outputs may modulate a 70-kilohertz, voltage-controlled oscillator in FM/FM telemeter assemblies. This arrangement provides redundant transmission of some multiplexer outputs using both PAM and PCM techniques.

In the following paragraphs, the telemetry systems are described in the order of data flow. Starting from the telemetry equipment closest to the data source, the descriptions continue toward the transmitting equipment. Figure 5.3-1 should be used as a reference to these system descriptions.

5.3.2 SLOW SPEED MULTIPLEXING

MOD 245 MULTIPLEXER

The Mod 245 Multiplexer Assembly is a time-division multiplexer which is used in conjunction with an SS/FM Assembly multiplexer and FM/FM multiplexer link. This unit can sample a maximum of 80 data channels and provide 16 channels of output data. It is primarily used for multiplexing wideband vibration data.

The Mod 245 Multiplexer Assembly, Figure 5.3-2, consists of 20 plug-in subassemblies. Of these 20 subassemblies, 4 are common subassemblies

Table 5.3-2 Telemetry Systems in the Various Saturn Vehicle Stages

Stage	Telemetry System	Number of Systems		Number of Multiplexers		Transmitter	
		R&D	Oper	R & D	Oper	Frequency	Power
IU	FM/FM SS/FM PCM/FM	2 1 1	1 - 1	1 CIU 2 Mod 270 1 Mod 245 1 RDM Mod 410	1 CIU 2 Mod 270 2 RDM Mod 410	Saturn IB: 225-260 MHz Saturn V: 225-260 MHz and 2200-2300 MHz	20 W
S-IVB	FM/FM SS/FM PCM/FM	3 1 1	1 - 1	4 Mod 270 1 Mod 245	2 Mod 270	225-260 MHz	20 W
S-II	FM/FM SS/FM PCM/FM	3 2 1	2 - 1	5 Mod 270 1 Mod 245 7 RASM 2 RDSM	2 Mod 270 2 RDSM 2 RASM	225-260 MHz	20 W
S-IC	FM/FM SS/FM PCM/FM	3 2 1	1 - 1	4 Mod 270 2 Mod 245 1 RDSM	1 RDSM 2 Mod 270	225-260 MHz	20 W
S-IB	FM/FM SS/FM PCM/FM	2 1 1	1 - 1	3 Mod 270 1 Mod 245 2 RDSM	2 Mod 270 1 RDSM	225-260 MHz	20 W

Note: CIU = Computer Interface Unit
RDSM = Remote Digital Submultiplexer
RASM = Remote Analog Submultiplexer
RDM = Remote Digital Multiplexer (Mod 410)

(1 logic and timing unit, 1 regulator unit, 1 inverter unit, and 1 driver and voltage-controlled oscillator unit). The remaining 16 subassemblies are multiplexer units.

The data units are made up of 4 types. They are as follows:

- Two multiplexed channels with a sample period of 5.7 seconds each.
- Four multiplexed channels with a sample period of 2.9 seconds each.
- Five multiplexed channels with a sample period of 2.3 seconds each.
- One continuous channel.

The 3 types of multiplexer units all use 12-second sampling cycles. The different sample times are separated by "dead time". The sampling cycles are separated by longer periods of "dead time". Frequency response of the input is 0 to 5000 hertz. Input impedance is a constant 100 kilohms. Input signal level can be 0 to +5 volts peak to peak, or 0 to +5 volts dc. Output impedance is 1 kilohm at 0 to 5000 hertz. A dummy unit is used for continuous data.

Additional timing information is also transmitted using a 960 ± 70-hertz voltage controlled reference oscillator for data reduction purposes. This is fed into the special service channel in the SS/FM Assembly.

5.3.3 SS/FM TELEMETRY

The Saturn SS/FM telemetry system is designed specifically for transmission of the large volume of vibration data from the Saturn Vehicle. This system can transmit 15 channels, each having a response

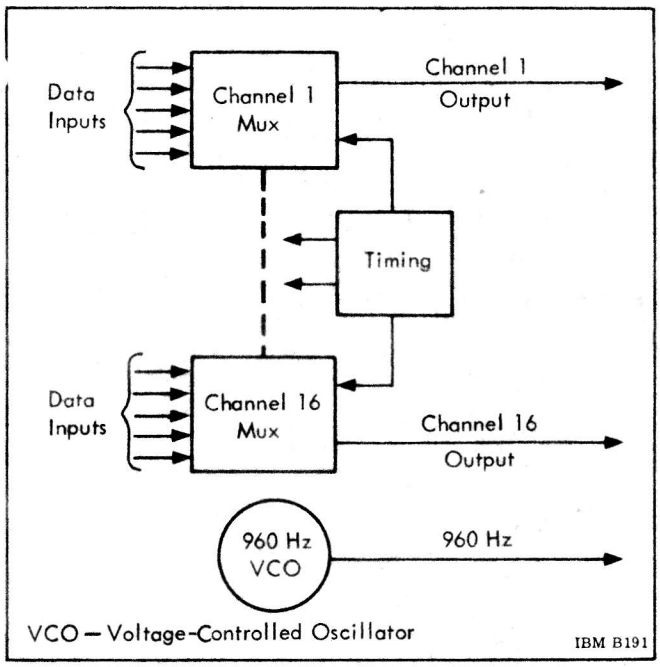


Figure 5.3-2 Mod 245 Multiplexer Block Diagram

of 30 to 3000 hertz, for a total data bandwidth of approximately 45 kilohertz within the standard telemetry carrier bandwidth.

A basic SS/FM telemetry system is comprised of a slow speed multiplexer, an SS Telemetry Assembly, and rf assembly similar to the FM/FM RF Assembly. The SS/FM Assembly is used in conjunction with a slow speed multiplexer (Mod 245) to expand its data-handling capability by time-sharing specific data channels. SS/FM telemetry is not used in operational vehicles.

SS TELEMETRY ASSEMBLY

Each of the 15 data inputs is fed to a balanced modulator and heterodyned with a 455-kilohertz carrier (Figure 5.3-3). The output of the modulator is fed to a mechanical bandpass filter (455 to 458 kilohertz) which passes only the upper sideband. The output of the filter is fed to a second balanced modulator where it is translated to the proper baseband frequency. The baseband position is determined by the carrier supplied from the frequency synthesizer. The two balanced modulators and the mechanical bandpass filter for each data channel make up the channel units. The channel units are identical for all channels.

The second modulator carriers are supplied to the channel unit from the frequency synthesizer and comb filters. These 15 subcarriers transpose the data to an assigned frequency between 4.74 and 72 kilohertz. These are the lower sideband outputs of the second modulators.

Both sidebands of the second modulators go to the summing amplifier No. 1 and the 200-kilohertz low-pass filter where all upper sidebands of the second modulator are filtered out. Here a 75.835-kilohertz pilot tone is summed into the channel unit outputs. The pilot tone provides a signal at the receiving station for demodulation of the 15 channels.

After leaving the 200-kilohertz low-pass filter, the composite signal is passed through a signal regulator. From the signal regulator, the composite signal is summed with the signal from the non-translated special service channel. The frequency response of this channel is 0 to 1200 hertz. Its normal use is to carry a 890 to 1030-hertz synchronizing signal provided by the Mod 245 Multiplexer Assembly for demultiplexing the signals at the receiver. The output of the summing amplifier No. 2 is used to frequency modulate an rf transmitter

All the carrier signals and the pilot tone are generated internally in the airborne SS/FM assembly by a single 910.025-kilohertz crystal oscillator. This signal is used to drive a flip flop which provides the 455.012-kilohertz carrier signal and a frequency synthesizer provides all sub-carriers and the pilot tone from the comb filters.

To provide a 3-kilohertz information bandwidth and allow sufficient guardband, a channel spacing of 4.74 kilohertz is used. This spacing is convenient to generate in the synthesizer and allows an adequate guardband of 1.74 kilohertz. The 75.83-kilohertz pilot tone falls just above the highest baseband frequency. It is used as a reference in the ground demodulation equipment to regenerate the basic 455 and 4.74-kilohertz frequencies. Since the amplitude of the transmitted 75.83-kilohertz pilot tone is regulated, it is also used as an automatic gain control.

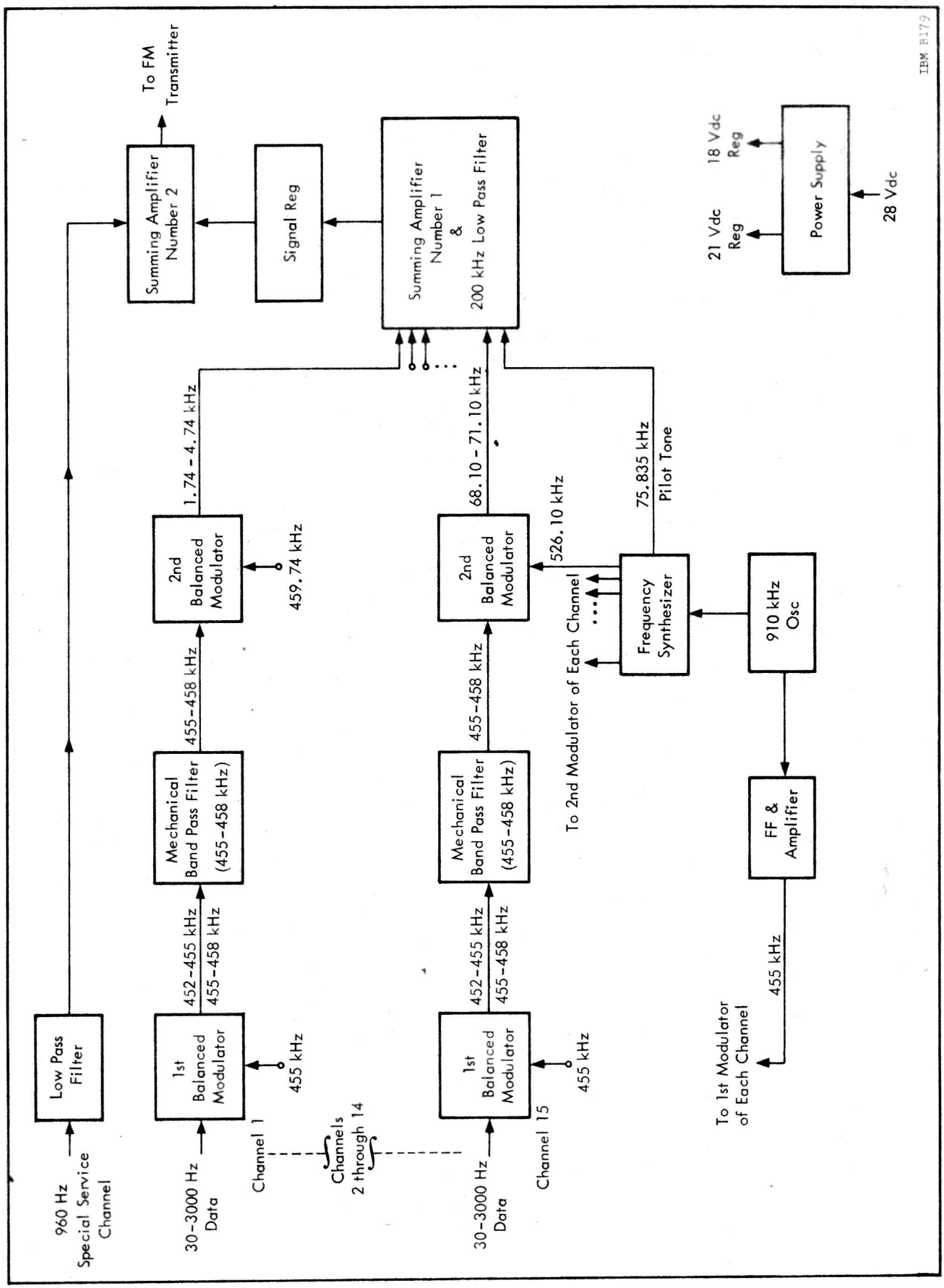


Figure 5.3-3 Airborne SS Telemetry Assembly Block Diagram

5.3.4 FM/FM TELEMETRY

The FM/FM telemetry system frequency multiplexes the input data. The conditioned signals derived from pressure, temperature, etc., modulate the frequency of the subcarrier oscillators. The combined output of several subcarrier oscillators is again frequency modulated on the RF carrier. Standard IRIG frequency channels are assigned. The data bandwidth capabilities of these channels are shown in Table 5.3-3. Slow-varying data is applied to the low-frequency channels; data with higher frequency variations must be applied to the higher frequency channels. FM/FM systems are susceptible to various sources of noise and distortion (fluctuation noise, crosstalk, harmonic distortion of the individual subcarrier signals, subcarrier data feed-through, and distortion of individual subcarrier signals due to band-limiting filters), which affect the accuracy of the telemetered data. The basic components of an FM/FM telemetry system are: a Mod 270 Multiplexer Assembly, an FM/FM Assembly and an RF Assembly.

Each of the subcarrier oscillators of an FM/FM system may be preceded by another subcarrier group. Each of these "sub-subcarriers" would, in this case, be modulated by the actual measurement values. This technique is called FM/FM/FM, or FM^3. The technique trades bandwidth for additional channels; therefore, the frequency response of the channels is much lower. Since another modulation stage is used, the technique is less accurate than FM/FM.

A time-multiplexed signal may be fed into a subcarrier oscillator of an FM/FM system to increase the channel capacity. Time multiplexing consists of sequentially sampling a number of data signals with an electronic or mechanical commutator. The commutator output appears as a train of pulses of varying amplitude. This technique is known as Pulse-Amplitude Modulation (PAM/FM/FM).

The basic modulation scheme and principal components used (subcarrier oscillators, mixer, power amplifier, and transmitter) are essentially the same for the FM/FM system in each stage. Figure 5.3-4 shows a typical Saturn Stage FM/FM system. Each channel receives a signal from the Measuring Distributor. This input signal modulates a voltage-controlled subcarrier oscillator. The frequency-modulated signals from the various subcarrier oscillators are combined in the mixer amplifier. The composite signal is frequency modulated on a radio-frequency carrier in the VHF band (225 to 260 megahertz) for transmission to the ground stations. The transmitter provides a signal power level of approximately 20 watts.

The available standard IRIG channels may be utilized in different ways. The system shown in the figure uses 13 continuous data channels (channels 2 through 14). The input signals from the Measuring Distributor are in the range of 0 to +5 volts dc (2 to 7 volts peak-to-peak ac when a bandpass filter is used in place of a channel or subchannel oscillator).

When used, FM^3 is applied to the channels above channel 13. A subcarrier channel of 70 kilohertz (±30 percent) is used for time-multiplexed signals from the Mod 270 Multiplexer Assembly. When this PAM technique is applied, all IRIG channels above 30 kilohertz will not be used. The Mod 270 solid-state, time-division multiplexer operates at a rate of 3600 samples per second. It consists of 30 primary channels which are sampled 120 times per second. In addition, 10 submultiplexers may be used on selected main channels; each sampled at a rate of 12 per second. The multiplexer accepts input signals in the range of 0 to 5 volts dc and provides two PAM wave train outputs. One wave train modulates the 70-kilohertz, voltage-controlled subcarrier oscillator with a frequency deviation of ±30 percent (i.e., 49 to 91 kilohertz for an input signal from 0 to 5 volts dc). The second wave train is used for the PCM system.

RF ASSEMBLY

The RF Assembly accepts single sideband FM and FM analog signals from the telemetry assemblies and provides the highly-stable, close-tolerance carrier frequency (±0.01 percent). It further provides the capability of varying the carrier frequency in a manner (±1 percent of the best straight line approximation for 125-kilohertz deviation at modulation frequencies from 300 hertz to 100 kilohertz) proportional to the input signal amplitude, thereby providing an RF link from the measurement systems in the flight vehicle to the ground receiving station.

5.3.5 PAM MULTIPLEXING

MOD 270 MULTIPLEXER

The Mod 270 Multiplexer Assembly (time division) is basically a 30 by 120 multiplexer (30 channels, each sampled 120 times per second). It accepts voltage inputs in the range of 0 to 5 volts (high level data) and provides two PAM wavetrain outputs, one (with pedestal) for input to a 70-kilohertz ±30 percent

Table 5.3-3. IRIG Subcarrier Frequencies and Deviations

Channel (Band)	Center Frequency (Hz)	Lower Limit (Hz)	Upper Limit (Hz)	Deviation (percent)	Frequency Response† (Hz)
1	400	370	430	±7.5	6.0
2	560	518	602	±7.5	8.4
3	730	675	785	±7.5	11.0
4	960	888	1,032	±7.5	14.0
5	1,300	1,202	1,398	±7.5	20.0
6	1,700	1,572	1,828	±7.5	25.0
7	2,300	2,127	2,473	±7.5	35.0
8	3,000	2,775	3,225	±7.5	45.0
9	3,900	3,607	4,193	±7.5	59.0
10	5,400	4,995	5,805	±7.5	81.0
11	7,350	6,799	7,901	±7.5	110.0
12	10,500	9,712	11,288	±7.5	160.0
13	14,500	13,412	15,588	±7.5	220.0
14	22,000	20,350	23,650	±7.5	330.0
15	30,000	27,750	32,250	±7.5	450.0
16	40,000	37,000	43,000	±7.5	600.0
17	52,500	48,560	56,440	±7.5	790.0
18	70,000	64,750	75,250	±7.5	1050.0
19	93,000	86,025	99,975	±7.5	1395.0
A††	22,000	18,700	25,300	±15	660.0
B	30,000	25,500	34,500	±15	900.0
C	40,000	34,000	46,000	±15	1200.0
D	52,500	44,620	60,380	±15	1600.0
E	70,000	59,500	80,500	±15	2100.0
F	93,000	79,050	106,950	±15	2790.0
X†††	70,000	49,000	91,000	±30	4200.0

† Frequency response is based on a deviation ratio of five.

†† Increased deviation bands A through X may be employed by omitting other bands of that center frequency and the following bands:

Band Used	Omit Bands
A	13, 15, and B
B	14, 16, A, and C
C	15, 17, B, and D
D	16, 18, C, and E
E	17, 19, D and F
F	18 and E
X	16, 17, C, and D

††† Utilized for PAM/FM/FM and is not a standard IRIG channel.

FM/FM subcarrier and a second (without pedestal) for the PCM/DDAS Assembly. A block diagram of the Mod 270 Multiplexer Assembly is shown in Figure 5.3-5.

A time-division multiplexer consists of three major parts: a set of switches or gates for each output channel, a timing device (logic generator), and a power supply.

The gates, acting as electronic switches, sequentially connect the data inputs to the multiplexer output on commands from the timing circuits.

The timing, or logic, circuits provide the signals which open and close the data gates at the desired times and in the desired sequence.

Multiplexers are normally located in proximity to data sources in order to minimize cabling weight. Each multiplexer houses sampling gates for up to 234 data channels. By means of flexible plug-in modules, variations in numbers of channels and sample rates may be accomplished within the multiplexers. These multiplexers also accept pre-sampling filters where required for specific measurements. Remotely located submultiplexer assemblies may also be used to increase the capacity of each individual multiplexer to 270 channels.

Twenty-seven of the thirty primary channels are data channels while the remaining three are utilized for amplitude references and PAM frame identification. Ten-channel gate modules, which plug into the assembly, may be used to submultiplex primary channels 1 through 23. Each of these 10 sub-channels then provides a sampling rate of 12 times per second. Any number of the 23 channels may be submultiplexed or utilized as 120-sample-per-second channels. When used at the primary sample rate, a submultiplexer "dummy" card (or a pre-sampling filter if required) is inserted in place of the submultiplexer module. The four remaining primary data channels (24, 25, 26, 27) are always utilized as 120-sample-per-second channels. Each of the 27 primary data channels may be submultiplexed external to the basic assembly.

A zero amplitude reference is inserted on channel 28 of the output wavetrains except in the frame corresponding to sub-channel 10, where a 5-volt amplitude reference is inserted to provide master frame identification. Channels 29 and 30 carry a 5-volt reference level and are bridged together to form PAM frame identification. Except for the channel 29-30 bridge, all channels are inserted as 50 percent duty cycle pulses on both output wavetrains.

A zero pedestal of 1.2 volts is added to the wavetrain output applied to the 70-kilohertz VCO of the PAM/FM/FM telemetry system. The output wavetrains have a pulse rate of 3600 pps.

A calibration generator, located in the assembly, provides in-flight calibration capability. Calibration is initiated by an external command which in the Saturn telemetry system is provided by the TM Calibrator (Mod II). When a calibrate command is received, the calibration generator delays its sequence until the beginning of the following master frame. It then applies a sequence of five calibration voltages to all data channels (channels 28, 29, and 30 are unaffected by the calibration). The calibration voltage levels are in order: 0, 25, 50, 75, and 100 percent of full-scale data voltage. Each voltage level is sustained for one master frame (83.4 milliseconds), requiring approximately 400 milliseconds for the complete sequence. Paragraph 5.3.7 describes the calibration function in greater detail.

Internal logic functions of the Mod 270 Multiplexer Assembly operate from its internal 3600-hertz multivibrator clock. However, the sample and frame rates can be synchronized to external pulses of the correct frequency and waveform. In the Saturn telemetry system, these synchronizing signals are provided by the Mod 301 PCM/DDAS Assembly. The synchronizing waveforms consist of a 3600-hertz square wave and a 4 pps pulse approximately 278 microseconds in duration occurring during channel one of each 30th frame.

The Mod 270 Multiplexer Assembly also provides synchronizing signals as outputs. These are identical to the waveforms previously described, except the frame sync pulse has a repetition rate of 12 pps instead of 4 pps. See Figure 5.3-6. These synchronization outputs are normally utilized to control remote submultiplexer packages.

The submultiplexers are composed of selection gates that subdivide the main multiplexer channels. Ten submultiplexer channels are connected to each main multiplexer channel, thus reducing the sampling rate from 120 per second to 12 per second.

Each gate functions in the following manner: The input side of a gate is tied to the data to be sampled, and the output side is tied to the main multiplexer channel. The normally open gate closes upon application of a current pulse to the transformer to allow information to pass through to the main multiplexer. This current pulse is obtained by grounding

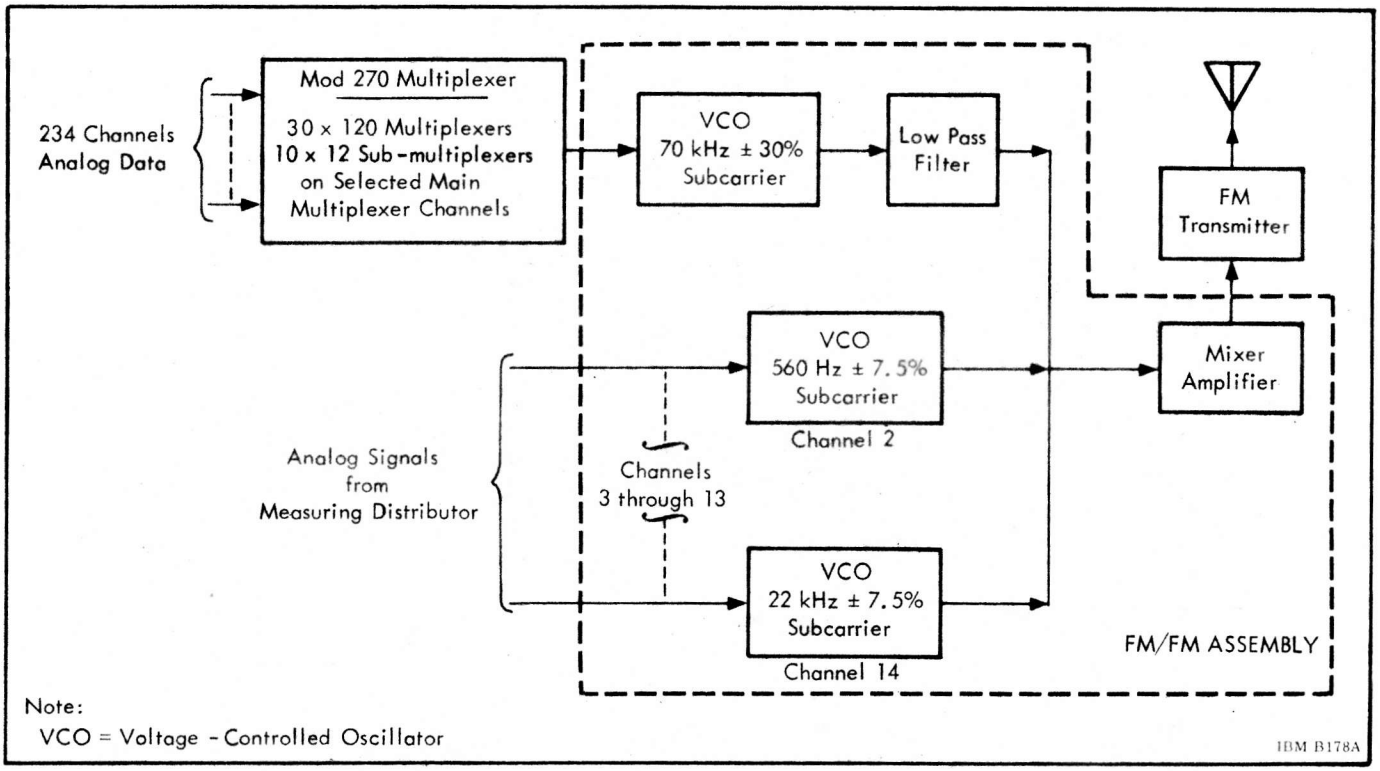


Figure 5.3-4 Typical R&D FM/FM Telemetry System Block Diagram

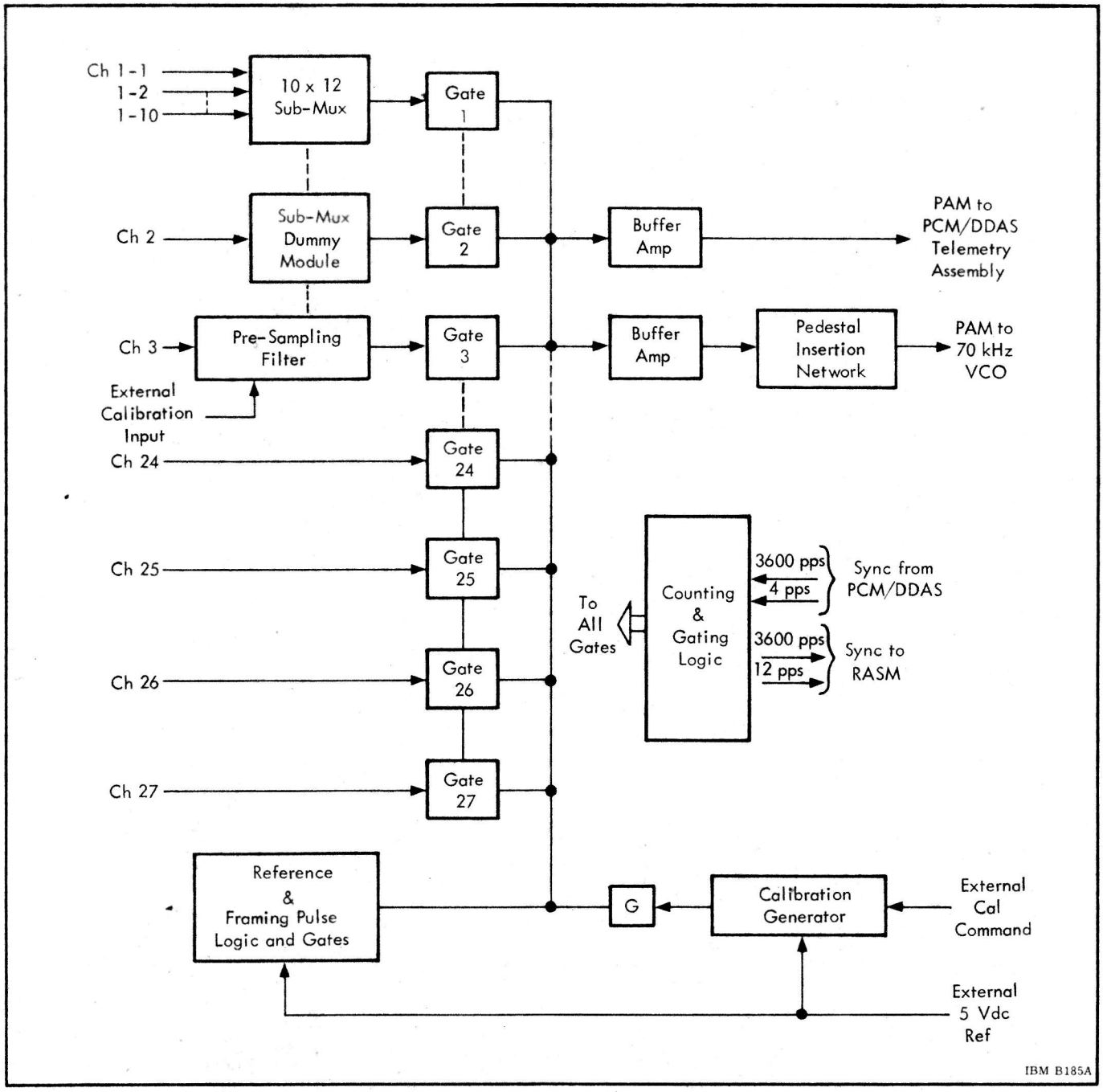


Figure 5.3-5 Mod 270 Multiplexer Block Diagram

one side of the transformer and connecting the other side to the decoded output of the "T" counter.

The gates are connected in columns of ten, and all outputs of a particular column are connected to one main multiplexer channel input.

The submultiplexer "dummy" card is used when a sampling rate of 120 times per second is required. This card, used in place of the submultiplexer card, provides a direct path from the data being sampled to the main multiplexer board. An RC load mounted on this board (the same as on all submultiplexer cards) prevents data spikes from being passed through.

The characteristics of the Mod 270 Multiplexer Assembly are given in Table 5.3-4.

5.3.6 PCM/DDAS TELEMETRY SYSTEM

The PCM/DDAS telemetry system serves a dual purpose in the Saturn Launch Vehicle. This

Table 5.3-4 Mod 270 Multiplexer Assembly Performance Characteristics

Characteristic	Specification
Time Stability	
Clock rate	3600 Hz + 2%
Duty cycle	139 μs ± 5%
Linearity (best straight line)	± 0.1%
Accuracy	
Output of amplifier (without pedestal)	± 0.1%
Output of amplifier (with pedestal)	± 0.5%
Pedestal Stability	1.2 V ± 50 mV
Reverse Current (all channels at 5 V except channel under test which is short circuited)	2 μA (max)
Input Impedance of Channel (excluding 100k input terminating resistor)	5 megohm(min)
Output No. 1 (without pedestal)	100 Ω (max)
Output No. 2 (with pedestal)	2k (max)

system functions as a telemetry link for digital data (PCM/FM) and as a part of the DDAS. PCM/FM is required on the launch vehicle in order to obtain sufficient accuracy, with acceptable bandwidth efficiency, for digital data transmission from data sources such as the LVDC. This accuracy is possible because of two main reasons: first, the scheme requires no digital to analog conversion for digital and discrete inputs, and second, transmission of a serial bit configuration allows a good signal to noise ratio for a weak and deteriorated signal received at a distant ground station.

Before launch, PCM/DDAS also provides measurements to the launch computer in the ground checkout stations via coaxial cable.

SYSTEM COMPONENTS

To provide flexibility, the system is built up from several assemblies which may be combined as required in a particular stage application. The following assemblies may be used to build up a PCM/DDAS telemetry system:

- Mod 301 PCM/DDAS Assembly
- Mod RDSM-1D Remote Digital Submultiplexer

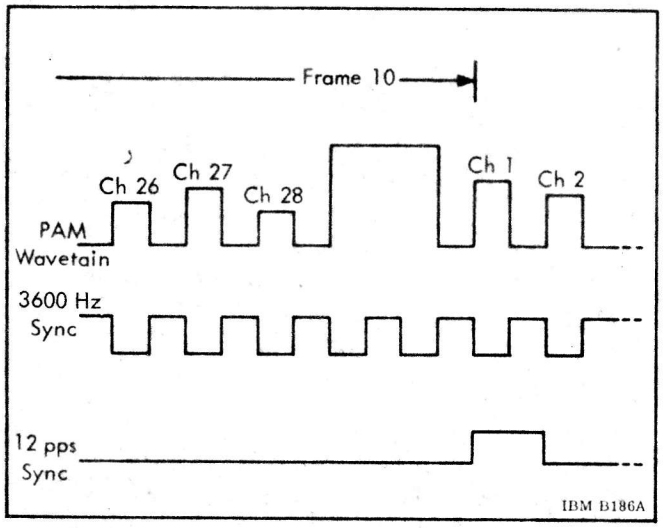


Figure 5.3-6 Mod 270 Multiplexer Assembly Waveforms

- Mod 410 Remote Digital Multiplexer (RDM)
- Mod 270 Multiplexer Assembly
- A Remote Analog Submultiplexer (RASM) which may be used with a Mod 270 Multiplexer Assembly (S-II Stage only)
- Computer Interface Unit (CIU)
- PCM/RF Assembly

The Mod 301 PCM/DDAS Assembly is the central piece of equipment in both the telemetry link and the DDAS link. It provides the output signals for telemetry and automatic checkout.

The Mod RDSM-1D Remote Digital Submultiplexer is used to connect digital data sources to the Mod 301 PCM/DDAS Assembly.

The Mod 410 Remote Digital Multiplexer is used in the IU to connect the LVDC digital data, and discrete sources to the Mod 301 PCM/DDAS Assembly.

The Mod 270 Multiplexer Assembly is used to connect analog data into the Mod 301 PCM/DDAS Assembly.

The RASM may be used to submultiplex data being fed through the Mod 270 Multiplexer Assembly (on the S-II Stage of the Saturn V Vehicle only).

The CIU allows the LVDC, operating through the LVDA, to read selected measurement data which is being transmitted through the Mod 301 PCM/DDAS Assembly.

The PCM/RF Assembly contains the signal conditioner, power amplifier, and RF transmitter for the telemetry link.

SYSTEM USES

During preflight checkout, the telemetry system presents digital data over coaxial cables to one or more locations remote from the vehicle. These measurements are available to digital computers in real time through a special data-receiving facility interfaced with the computers. The data-receiving facility also provides outputs for display of selected channels in either digital or analog form for visually determining the status and readiness of vehicle subsystems and tape records the DDAS inputs for analysis at a later time.

During the launch, earth orbiting, and lunar-injection phases, there are times when information processed by the LVDC is desired at the ground station. Since the information to be telemetered is dependent on particular missions and has a random characteristic, provision will be made in the telemetry to accomodate these outputs. Specific PCM telemetry system channels are assigned to accommodate the LVDA 40-bit outputs. The assigned channels are sampled at a rate of 240 times per second.

The LVDA identifies valid data by the presence of a validity bit which has no significance to the telemetry but is transmitted as part of the data telemetered to the ground. The ground computer automatically determines the existence of valid data by recognizing the validity bit in a data word. The validity bit is present with the valid data for at least 4.5 milliseconds to ensure at least one transmission of the valid data.

During flight, the DDAS function is performed between the telemetry system, LVDA, and LVDC. Upon request, data in digital form is made available to the LVDC during flight and is used by the LVDC to perform vehicle checkout.

The telemetry system in the S-IVB/IU functions during launch, earth orbit, and lunar-injection phase of the mission. During these phases, periodic checks are required of the vehicle's performance or operating status. This is accomplished by inserting specific segments of the telemetered information into the computer.

During orbital checkout, which is initiated by a command signal to the LVDC via the IU command, the LVDC requires a real-time value of measurements, which are part of the total measurements being telemetered by the S-IVB/IU Stage telemetry system.

Selective transfer of measurement values from the S-IVB/IU Stage telemetry systems to the LVDA is accomplished through the DDAS/Computer Interface Assembly. This assembly contains the timing and comparison logic necessary to separate the selected channel from the IU PCM/DDAS format. A time division multiplexer, located in the S-IVB Stage, transfers S-IVB measurements needed for checkout and mission control to the IU PCM/DDAS Assembly.

The LVDA signifies the specific data channel to be transferred by means of a 12-bit channel address. Upon receipt of a "data-request" signal from the LVDA, the DDAS/Computer Interface Assembly initiates a transfer sequence which consists of:

- Awaiting the next appearance of the signified channel in the PCM/DDAS format.
- Writing the data sample into a 10-bit holding register within the assembly.
- Providing a "data-ready" signal to the LVDA indicating that the selected data is available.

So long as the "data-request" signal remains at the request level, subsequent samples of the selected channels are transferred into the holding register as they appear in the format of the PCM/DDAS Assembly. When the LVDA returns the "data-request" signal to the standby level, the last value transferred remains in the holding register until another transfer sequence is initiated.

When the LVDA receives the "data-ready" signal, it branches to a sub-routine which operates to transfer the data from the telemetry output register to the LVDA. Synchronization between the telemetry system and the LVDA is accomplished in the following manner: Each time the telemetry receives an address from the LVDA, followed by a valid "data-request" signal, it recognizes this input as the initiation of a new data-seeking cycle as well as a signal to read in the data. Upon this recognition by telemetry, it first resets its output data register and then begins seeking the data requested by the LVDA. The LVDA and LVDC ensures that a new address with a valid read bit is not generated until data from the telemetry output register has been received in response to the previous address.

MOD 301 PCM/DDAS ASSEMBLY

The Mod 301 PCM/DDAS Assembly performs six major functions as follows:

- Scans the PAM wavetrains of several (1 to 6) Mod 270 PAM Multiplexer Assembles in a programmed sequence and combines these wavetrains into a single PAM wavetrain.
- Encodes the PAM samples in this wavetrain into 10-bit digital form.
- Accepts data in digital form and programs it into selected time slots in the output serial format.
- Generates the required frame and master frame identification codes, combines these codes with the digital and encoded analog data, and arranges the desired serial format for output.
- Provides a 600-kilohertz FM modulated carrier as the DDAS output, and an NRZ modulating output for the PCM/RF Assembly.
- Provides the synchronization outputs necessary to synchronize the Mod 270 Multiplexer Assemblies and remote digital multiplexers.
- Provides a parallel digital output to the CIU.

Figure 5.3-7 is a functional block diagram of the Mod 301 PCM/DDAS Assembly. It is composed of the six functional subsystems listed below:

- PAM scanner (and associated program patch).
- Analog-to-digital converter.
- Digital multiplexing and formating logic.
- Clock programming and timing logic.
- DDAS voltage controlled oscillator.
- Power supplies.

PAM Scanner. The PAM scanner connects one or more Mod 270 Multiplexer Assembly outputs in a programmed sequence to the ADC input for digitizing. By means of the scanner program patch, any multiplexer arrangement compatible with the system application can be accomodated. Up to three multiplexer arrangements (modes) may be programmed at the scanner patch, and the automatic switching between modes is accomplished by applying external 28-volt dc commands.

The scanner gates are 4-transistor, back-to-back, balanced configurations which switch both legs of the PAM circuit of each PAM multiplexer. The transformer coupling of the switching logic input of the gates provides a favorable impedance condition for the PAM signals.

The PAM scanner and program patch are packaged on printed circuit cards which plug into the Mod 301 PCM/DDAS Assembly.

Analog-to-Digital Converter. The analog-to-digital converter encodes the PAM signals received through the PAM scanner by the successive approximation method. The digital output is fed in parallel form to a parallel storage register according to commands received from the programming and timing logic. Figure 5.3-8 shows a functional block diagram of the ADC. Its operation is non-synchronous (not synchronized with other parts of the system) and at a clock rate of approximately 250 kilohertz which is provided by a blocking oscillator.

Encoder command pulses at the system word rate are provided by the programming logic. When an encode command is received by the ADC, it begins an encode cycle at its own clock rate; this requires approximately 56 microseconds. At the end of the cycle, the ADC register switches have been set to the digital equivalent of the analog quantity present at the buffer input during the encode cycle. The logic levels from the register switches provide a parallel digital output until the next encode command arrives. The register switches are then reset and a new encode cycle follows.

Digital Multiplexing and Formatting Logic (See Figure 5.3-9). The function of the digital multiplexing and formatting logic is to combine the encoded data from the ADC, externally generated digital data, and frame (and master frame) identification words into the required output sequence. The specific time slot into which data is inserted is controlled by command pulses from the programming and timing logic. The 10-bit output of the ADC is transferred into the parallel storage register by each word rate clock pulse (so long as the encoder inhibit bus is unenergized). When the encoder inhibit bus is energized, the ten AND gates at the ADC output are disabled, and the ADC output is not transferred into the parallel storage register.

Up to ten 10-bit groups of digital data from external sources can be programmed into selected time slots at any of the four system sampling rates. The data is accepted in parallel. A zero-volt level

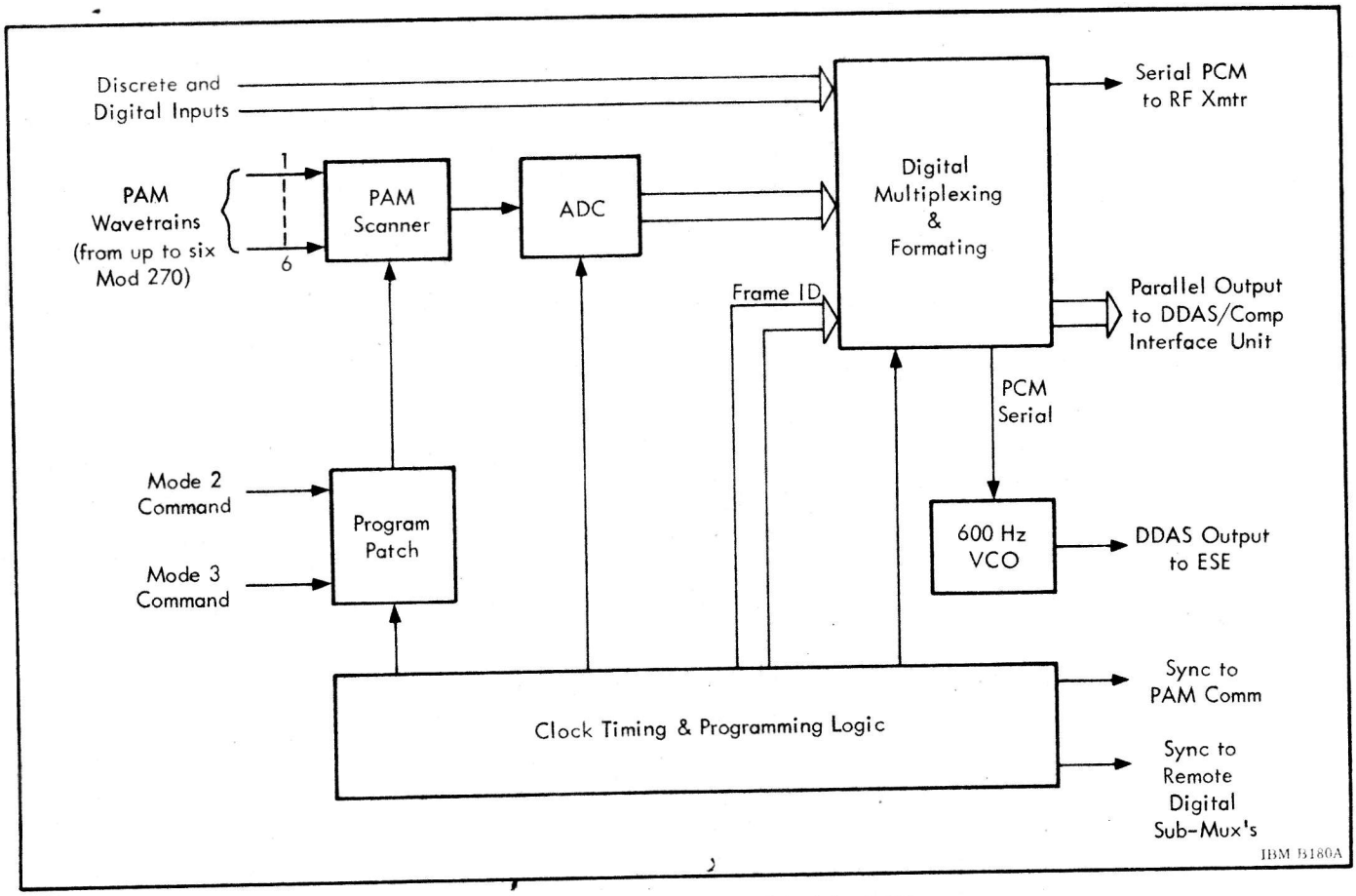


Figure 5.3-7 PCM/DDAS Assembly Block Diagram

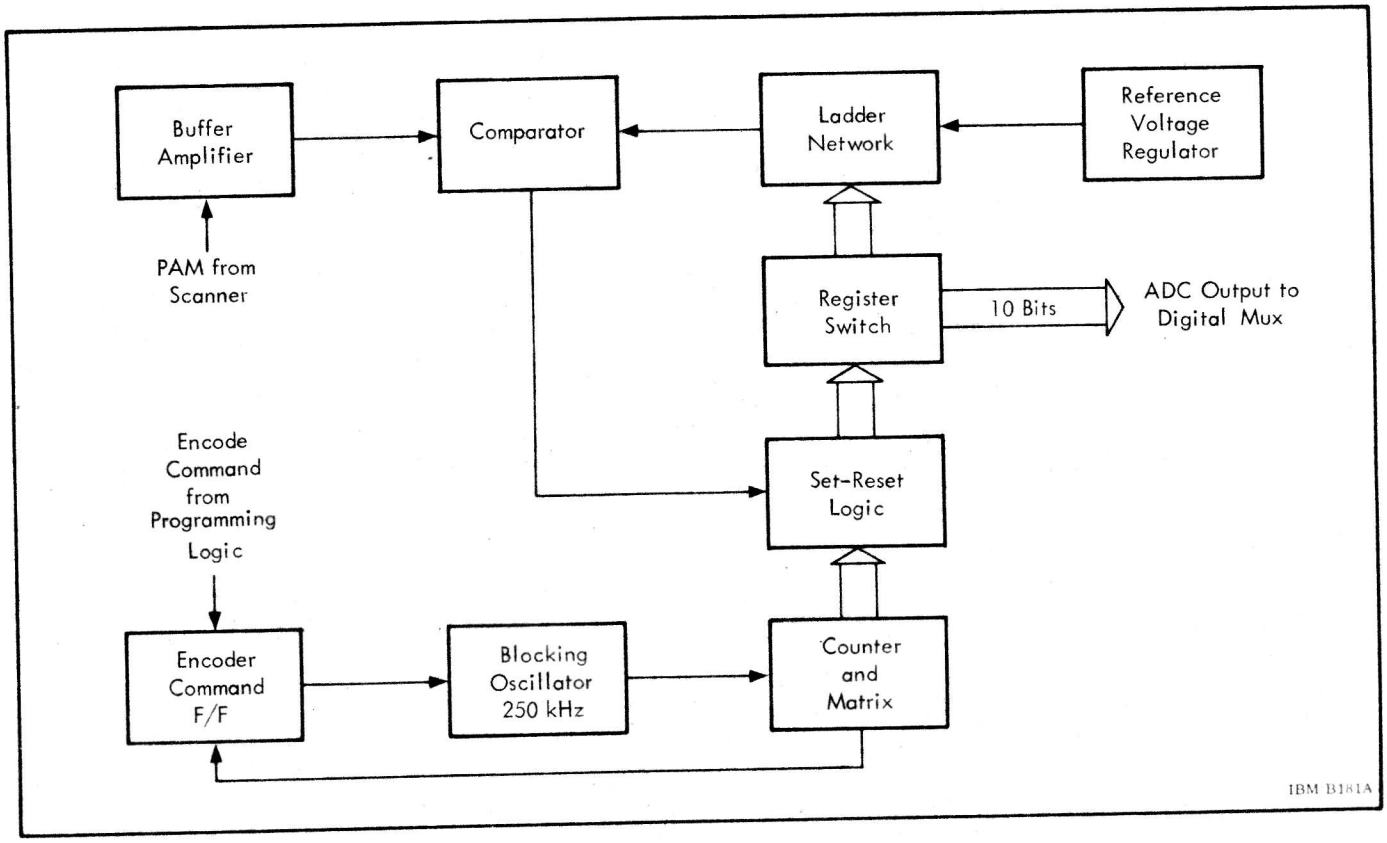


Figure 5.3-8 Analog-to-Digital Converter Block Diagram

represents a logical "0" and a positive level represents a logical "1". Inputs are buffered and then shifted into a magnetic core register before being transferred into the parallel storage register. The MCR provides temporary storage and dc isolation of the data source. Each MCR, along with its ten associated buffers and other circuits, is powered by an individual supply which is dc isolated. This permits monitoring of several digital data sources without interconnecting their dc commons.

The digital input section has 10 channels. Each channel will accept a 10-bit input in parallel form. To increase the data handling capacity, the input section may be fed from 10-channel remote digital multiplexers.

A WRITE command to an MCR causes the 10 bits of data to be stored in the magnetic cores. The WRITE command is programmed (at the command program patch) to occur before the time for transfer of the data into the PSR. Typically, the command occurs during the previous word time, but it can be programmed to occur at any word time after the previous sample of the specific channel is read into the PSR. For example, several 10-bit data sets can

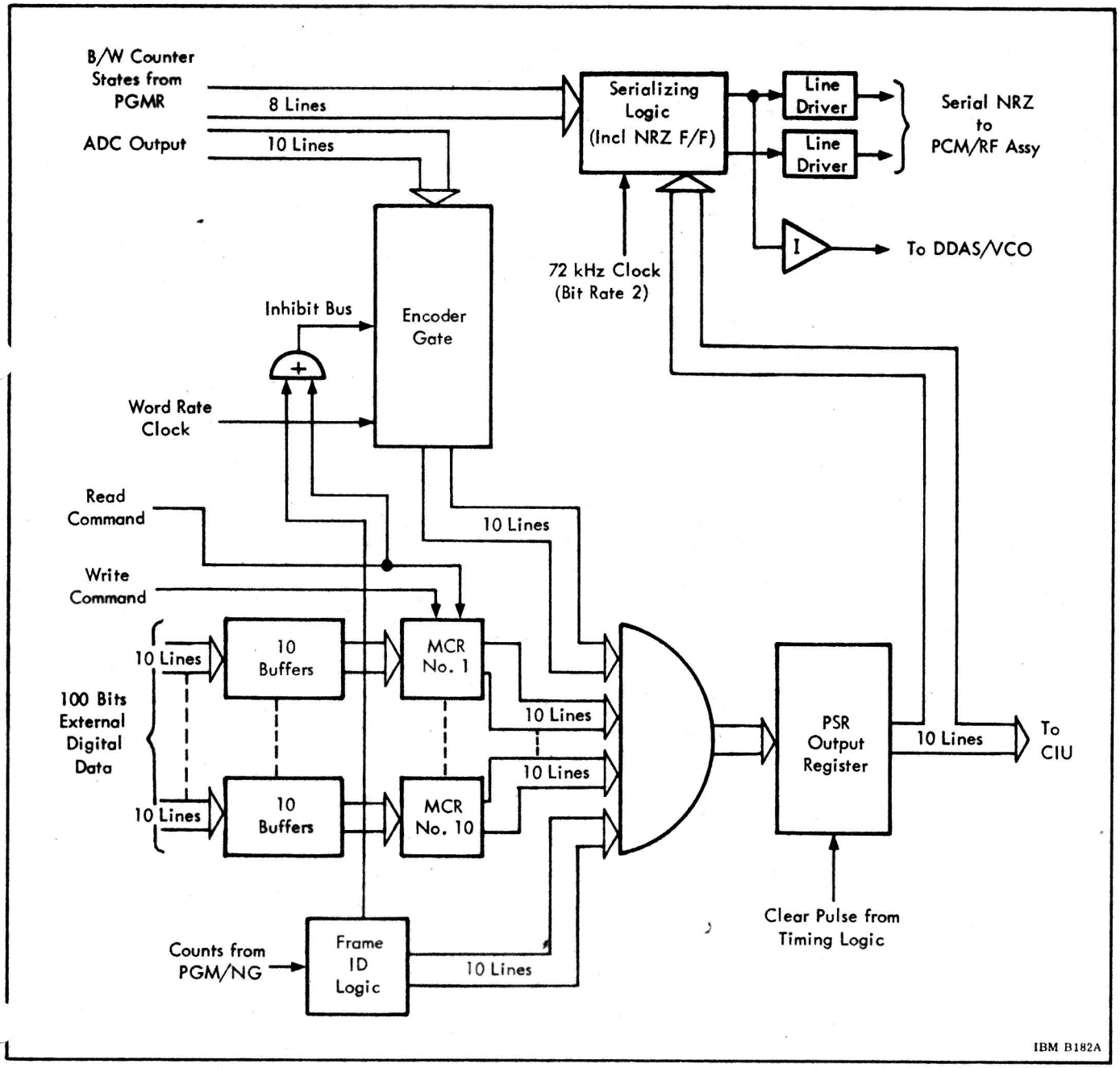


Figure 5.3-9 Digital Multiplexing and Format Logic

be written into their MCR's simultaneously and then placed into specific time slots in the output format. This mode of operation is utilized in monitoring a 40-bit set of data from the LVDC.

The READ command to the MCR is timed to transfer the data into the output register during the least significant bit time of the previous word time. READ commands are also OR'd together to provide a function for inhibiting the transfer to ADC data through the encoder gate.

The frame identification logic generates three unique code groups and inserts them consecutively during the last three word times of the PCM/DDAS frame. Once each 30th frame, the frame ID logic receives a signal from the frame ID reversal flip flop. This signal causes the frame ID logic to complement (reverse) all bits in the frame ID code of the 30th frame. This forms the master frame identification code. The code group is as follows:

Word 29B	1 0 1 1 0 1 1 1 1 0
Word 30A	1 0 1 0 0 0 1 0 0 1
Word 30B	1 1 0 0 0 0 0 1 1 0

The serializing logic shifts the contents of the PSR bit-by-bit into an NRZ flip flop, thus forming the serial NRZ output. The states of the bits per word counter are decoded, combined with the PSR outputs, and clocked to provide set-reset pulses to the NRZ flip flop. The two complementary outputs of the NRZ flip flop are buffered and provided at an output connector for use as a modulating input to the PCM/RF Assembly. One side of the NRZ flip flop provides a modulating input to the DDAS/VCO.

Clock, Programming, and Timing Logic. (See Figure 5.3-10) The clock, programming, and timing logic provides the timing signals necessary for the Mod 301 PCM/DDAS Assembly as well as signals required to synchronize logic in other telemetry assemblies.

One phase of the 72-kilohertz clock provides bit rate pulses to the serializing logic while the other phase steps the B/W counter. The outputs from each trigger of the B/W counter are decoded in the serializing logic and used to select stages of the PSR to form the serial bit train which controls the NRZ flip flop.

Count "2" of the B/W counter is decoded and initiates a series of three successive timing pulses which are 1.75 microseconds apart. The first (clear) pulse occurs approximately 2 microseconds after the least significant bit is transferred to the NRZ flip flop and resets all 10 stages of the PSR. The second pulse (READ clock) provides the correct timing phase for the transfer of data into the PSR from the ADC, the frame ID logic, or an MCR. The third pulse (WRITE clock) provides the proper phasing for writing external digital words into the MCR's. This pulse also signals the ADC to proceed with digitizing the succeeding analog signal.

The reset pulse of the B/W counter steps the group counter. This pulse occurs during the 2^2 bit time because of offset in the serializing logic. This allows settling time for the analog data inputs, (which are gated by the scanner in synchronism with the group counter) before the ADC begins digitizing. The group counter is a divide-by-two counter (one flip flop).

The reset pulse of the group counter steps the channel counter at a rate of 3600 pps. This consists of a divide-by-five counter and a divide-by-six counter which together form a divide-by-thirty counter.

The reset of the channel counter steps the divide-by-ten frame counter and the divide-by-three multiplexer counter. Both of these counters are stepped at the PCM/DDAS frame repetition rate of 120 times per second.

The 4 counters define each time slot in the PCM/DDAS format. The divide-by-two group counter provides the timing for the interlacing of two multiplexer groups. Each group is comprised of up to three Mod 270 Multiplexers which are controlled by the divide-by-three multiplexer counter. The divide-by-three multiplexer counter provides timing for the sharing of specific mainframe time slots. The divide-by-thirty channel counter steps in sychronism with the sampling action of the 30 by 120-channel analog gates (each sampled 120 times per second) in the Mod 270 Multiplexer Assemblies. The divide-by-ten frame counter steps in synchronism with the 10 by 12 submultiplexers (10 gates sampled 12 times per second).

The counts of each of the 4 counters are decoded and routed to the command program patch. A programming arrangement provides selection of READ and WRITE commands corresponding to specific time slots. These commands provide the timing signals to the MCR's necessary to place external digital data inputs into a specific format. Decoded outputs of the group counter and multiplexer counter are also routed to the scanner program patch, which provides selection of the multiplexer scanning sequence. Up to three multiplexer-scanning sequences may be programmed

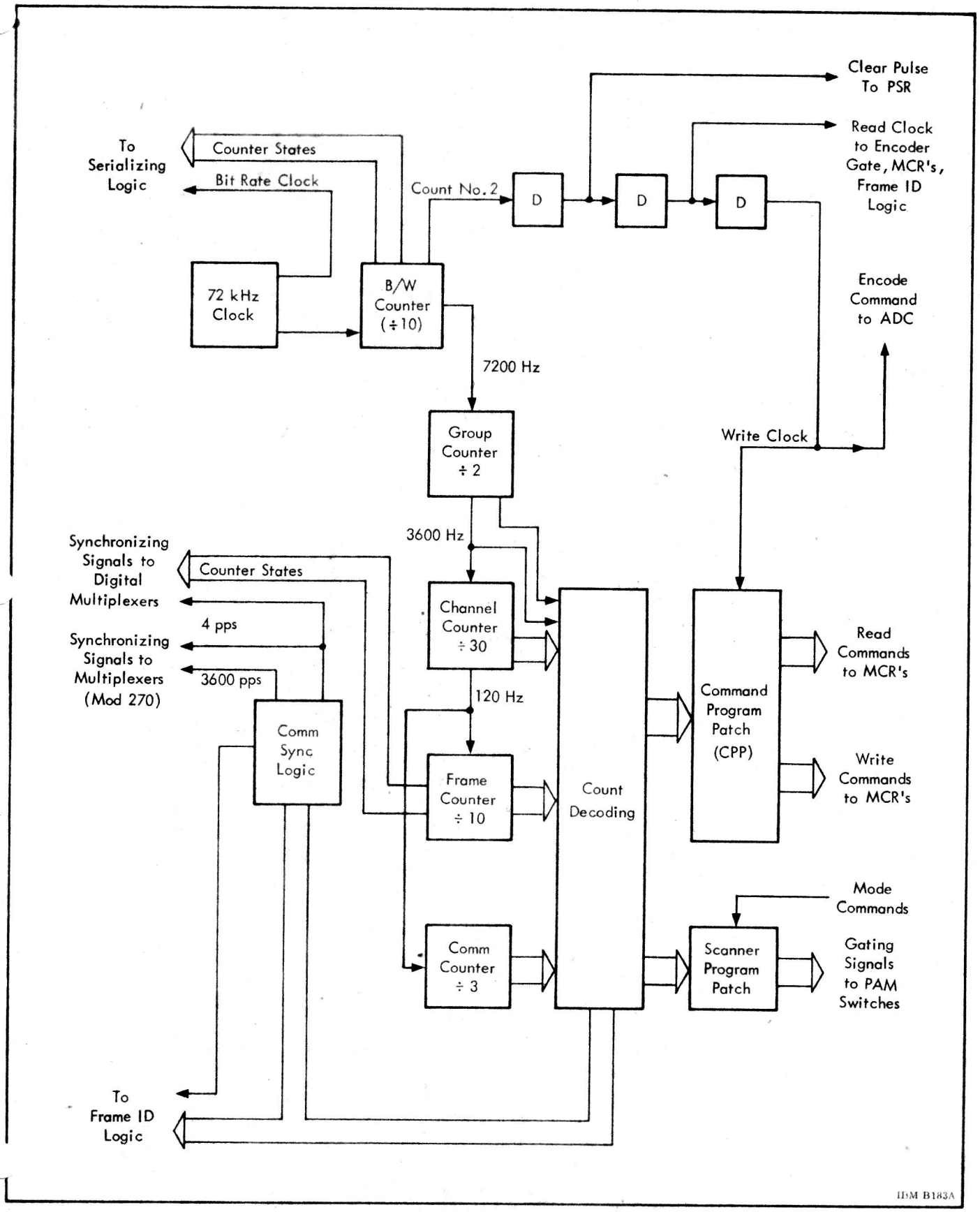


Figure 5.3-10 Clock Programming and Timing Logic Block Diagram

on the scanner program patch. A specific sequence is selectable by an externally generated mode command. The mode commands are 28-volt dc signals from GSE, the vehicle command, or other sources appropriate to the application. (Note: Mode 1 does not require application of an external mode command voltage.)

The control logic also generates 3 sets of waveforms used for synchronizing logic in other assemblies to the clock and frame rates of the Mod 301 PCM/DDAS Assembly. Two sets of waveforms provide the correct waveform shape, frequency, and phase for synchronizing Mod 270 Time Division Multiplexers. The two waveform sets are identical except for the offset in phase necessary for interlacing group A and group B multiplexers. Each set consists of a 3600-hertz square wave and a 278-microsecond pulse with a repetition rate of 4 pulses per second.

The third waveform set consists of an output from each stage of the divide-by-ten frame counter and a 3600-hertz square wave. This set of waveforms is utilized to synchronize remote digital multiplexer assemblies (Model 410).

DDAS Voltage Controlled Oscillator. The DDAS/VCO provides an FM modulated carrier (600 kilohertz) for transmission of the PCM/DDAS signal (via coaxial cable) to DDAS receiving equipment.

A 600-kilohertz transistor multivibrator is bias modulated by the serial NRZ data. An amplifier preceding the multivibrator presents an impedance of approximately 50 kilohms to the NRZ data input and also provides a non-linear modulating characteristic which makes the frequency deviation relatively insensitive to variations in the input data logic levels. A frequency deviation of approximately ± 35 kilohertz is used.

A common-collector buffer stage drives a filter which is designed to remove harmonics from the multivibrator output.

Power Supplies. There are six separate power supplies used in the Mod 301 PCM/DDAS Assembly.

A 28 Vdc-to-28 Vdc converter regulates the primary 28 Vdc power to the assembly and isolates the digital return in the Mod 301 PCM/DDAS Assembly from the vehicle 28 Vdc return line. It supplies 28 Vdc ± 1 percent at a nominal 25 watts output to the remaining power supplies in the system.

The 6 Vdc card accepts + 28 volts from the converter and provides + 6 Vdc at 250 mA, and - 6 Vdc at 50 mA. The + 6 Vdc output provides collector voltage to the programming, timing, and scanning portions of the Mod 301 PCM/DDAS Assembly. The - 6 Vdc output provides base bias voltage to the same circuits.

The +18 Vdc and +5 Vdc card accepts, regulates, and converts 28 Vdc to +18 Vdc and +5 Vdc. All circuit returns on this card are common. These voltages are used in the non-critical and digital circuits in the ADC (encoder) section of the assembly.

The -9 Vdc supply card provides bias voltage for the encoder section of the Mod 301 PCM/DDAS Assembly.

The +15 Vdc regulated supply obtains its input voltage from the +18 Vdc supply. The +15 Vdc is used as the reference voltage from which the comparison voltage is derived for the ladder network in the encoder.

The + 12 Vdc supply is a simple Zener-resistor divider. It is used to provide bias voltage for the circuits on command program patch B.

REMOTE DIGITAL SUBMULTIPLEXER (MOD RDSM-1D)

The Remote Digital Submultiplexer provides additional digital data handling capability to the PCM telemetry system. A maximum of 100 inputs are provided (see Figure 5.3-11). These inputs are sampled sequentially in groups of 10 and then applied to an output register with 10 outputs. The inputs may be utilized individually or in groups to form digital words. The RDSM handles digital or discrete information only; i.e., its inputs and outputs are set voltage levels which represent either ON-OFF conditions or binary numbers.

The PCM programmer located in the Mod 301 PCM/DDAS Assembly controls the sequential sampling action of the RDSM. The control signal consists of a 4-bit binary word which arrives in parallel format and represents timing information.

The RDSM provides a high degree of flexibility of application by use of isolated input gates and isolated power supplies. The unit has two isolated power supplies; regulated 20 Vdc and + 5 Vdc gate-collector supply. The regulated 20 Vdc is derived from the 28 Vdc vehicle supply by a dc-to-dc converter. The +5 Vdc gate supply is developed on each gate card by rectifying and filtering the 3600 pps clock signal from the PCM programmer.

The binary inputs to word gates are 0 ± 0.5 volt for a logical "0" input and 7 ± 3 volts for a logical "1" input (in a Type IV RDSM, a logical "1" input is approximately 28 Vdc). The binary outputs from the RDSM and the PCM programmer are the same, 0 ± 0.5 volt and 5 ± 1 volts.

An auxiliary card is available with the RDSM. It may be added to the unit to adapt it to a specific input. This auxiliary card is a divide-by six card which has an output signal that is used to cycle the liquid level measuring system.

REMOTE DIGITAL MULTIPLEXER (MOD 410)

One of these assemblies will be utilized in the Instrument Unit to take the 40-bit (parallel) words from the LVDC/LVDA and provide 10-bit words at the output to feed the LVDC words into the Mod 301 PCM/DDAS Assembly for transmission to the ground. Another Mod 410 Assembly will be utilized for other digital and discrete inputs.

A detailed diagram is given in Figure 5.3-12. There are 40 data input bits from the LVDA which are fed into the MCR cards for storage and subsequent insertion into the proper time slots of the system format. These time slots will be determined by the command program patch. From the Mod 301 PCM/DDAS Assembly multiplexer, there are two sync pulse inputs to the 410 timing logic; a 3.6-kilohertz group sync pulse, and a 4-hertz master frame sync pulse. Delay circuits in the timing logic provide the correct sequencing of the write, clear, and read commands. The timing logic also steps the 3, 5, 6, and 10 counters. The outputs of the counters are decoded by the command program patches A and B to provide assembly timing which is sufficient to accurately define the occurence of time slots in the system format.

DDAS/COMPUTER INTERFACE UNIT

A system interconnection diagram for the DDAS/Computer Interface Unit is illustrated in Figure 5.3-13. Figure 5.3-14 is a block diagram showing logic and circuit arrangements for the DDAS/Computer Interface Unit. Positive true logic levels and positive circuit triggering is assumed.

The buffer and dc isolation circuits provide the required input impedance to data and synchronizing signals from the PCM/DDAS. The circuits also contain magnetic coupling elements which provide isolation between the circuits of the PCM/DDAS and other circuits within the assembly. It should be noted that dc isolation is not required between the LVDA and the assembly logic circuits.

The timing and resetting logic circuits derive the common reset for the counter array and a clock of the correct phase for transfer of data into the holding register from the synchronization signals.

The counter array consists of three binary counters (A, B, and C) each having an internal reset which provides a recycle each 30, 10, and 3 counts, respectively. Each counter is also reset to a count of 1 by the common reset from the timing and resetting logic.

Counter A consists of 5 flip flops, arranged to provide a divide-by-thirty binary counter. Its input consists of the restored 3600 pps synchronization input to the assembly. At the end of count period 30, counter B is internally reset to a count of 1. The internal reset of counter A is also provided as an input to counters B and C.

Counter B consists of 4 flip flops configured as a divide-by-ten binary counter. Its input is triggered 120 times per second by the internal reset of counter A. At the end of count period 10, counter B is internally reset to a count of 1.

Counter C consists of 2 flip flops configured as a divide-by-three binary counter. Its input is triggered at 120 times per second by the internal reset of counter A. At the end of count period three, counter C is internally reset to a count of 1.

The twelve address lines from the LVDA are first buffered, and logic levels are transposed to the internal logic levels of the assembly. They are then compared to the states of the counter array by three comparators and two zero detectors.

Comparator A compares address bit 1 with waveform b, and address bits 2 through 6 with the states of flip flops one through five, respectively, of counter A.

If address bits 7 through 10 are all in the zero state, zero detector No. 1 provides an output which is combined in the OR gate OR_1 with the output of comparator B. Hence OR_1 provides a true output for either an in-register, or all zeros condition of the four address bits.

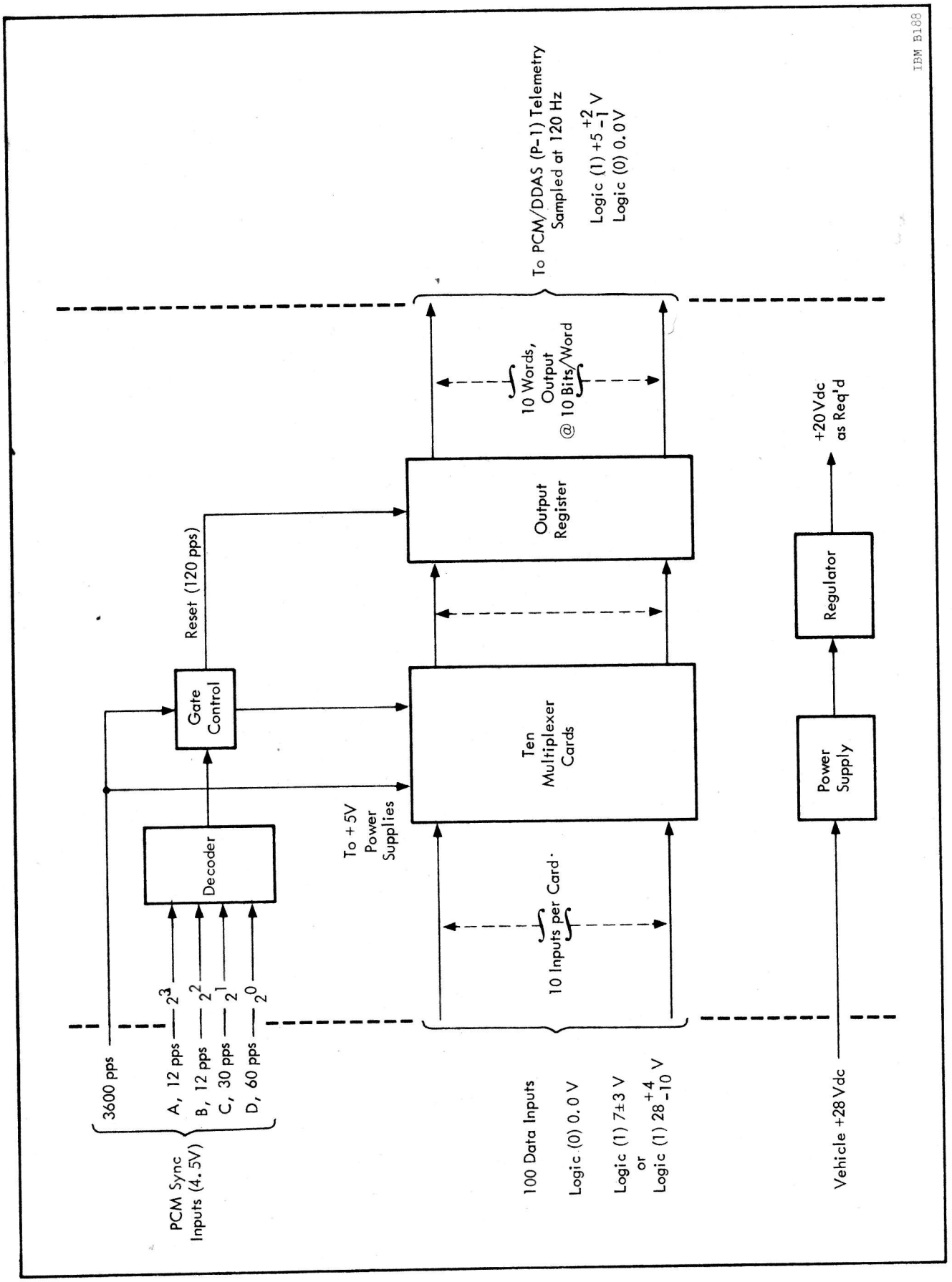


Figure 5.3-11 Remote Digital Submultiplexer

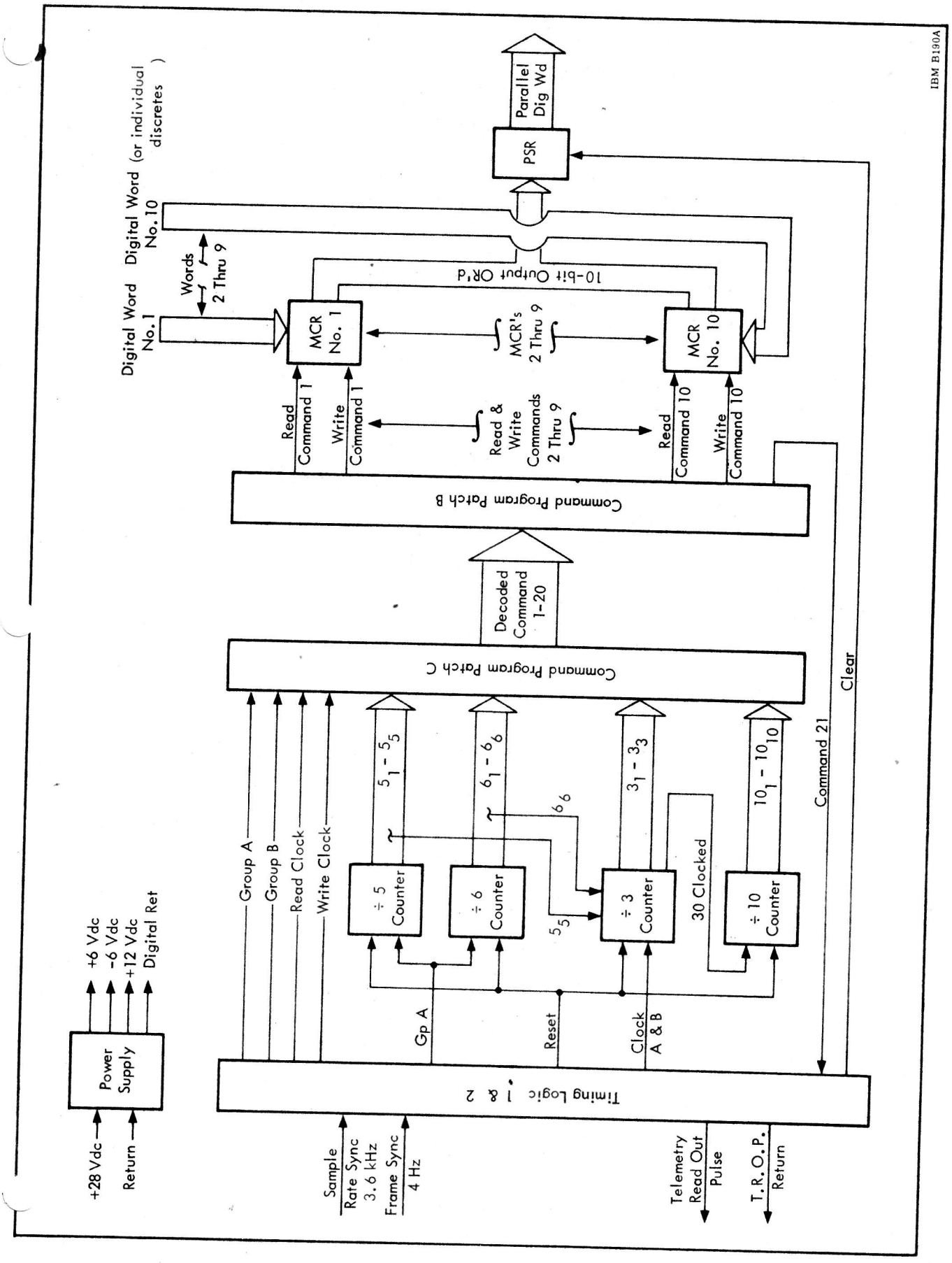


Figure 5.3-12 Mod 410 Multiplexer Block Diagram

Comparator C compares address bits 11 and 12 with flip flops one and two, respectively, of counter C.

If address bits 11 and 12 are both in the zero state, zero detector No. 2 provides an output which is combined in OR gate OR_2 with the output of comparator C. Hence OR_2 provides a true output for either an in-register, or all-zeros condition of address bits 11 and 12.

The zero detector provides a means by which the address bits may instruct that the status of either (or both) counter B and C be disregarded. This will provide access to the various sampling rates of the PCM/DDAS. The outputs of comparator A, OR_1, and OR_2 are applied to the data entry AND gate (AND_1). The in-sync detector provides a check of the correct synchronization state of the counters and prevents a transfer of data from occurring when the assembly timing is not synchronized with the PCM/DDAS. The output of the in-sync detector is then applied to AND_1 as a synchronization pulse.

The data request signal (after buffering and logic level transposition) is also applied as a true logic level to AND_1. If the in-sync detector output to AND_1 is true, the next "comparison true" signal then activates AND_1 and a clock pulse passes through to clear the holding register. After a delay of a few microseconds, the data inputs are gated into the holding register. The gating pulse also triggers the monostable multivibrator, which provides a "data ready" signal to the LVDA.

PCM/RF ASSEMBLY

The Model II PCM/RF Assembly uses the PCM pulse train from the PCM/DDAS Telemeter as modulation for a vhf carrier. The unit is all solid-state circuitry except for the regulated tube-type power amplifier.

The double-ended pulse train from the PCM/DDAS Telemeter is first fed to the PCM signal conditioner (see Figure 5.3-15). This module translates the positive-going and negative-going input excursions into corresponding positive and negative output voltages. This flip-flop circuit maintains the positive or negative voltage output until it is changed by the next input excursion of the opposite polarity. These positive or negative voltages are fed through a jumper plug before being used as the modulation to the transmitter module. The jumper plug is located on an external connector that could furnish the signal to a tape recorder.

The positive level of the two-level input causes the crystal-controlled transmitter module to transmit at its high-band edge, and the negative level at its low-band edge. The power of this carrier is then amplified and filtered to remove the upper harmonics and spurious frequencies. This results in a carrier with a power of 20 watts.

UHF/RF TRANSMITTER ASSEMBLY

The UHF/RF Transmitter Assembly uses the PCM pulse train from the PCM/DDAS Telemeter

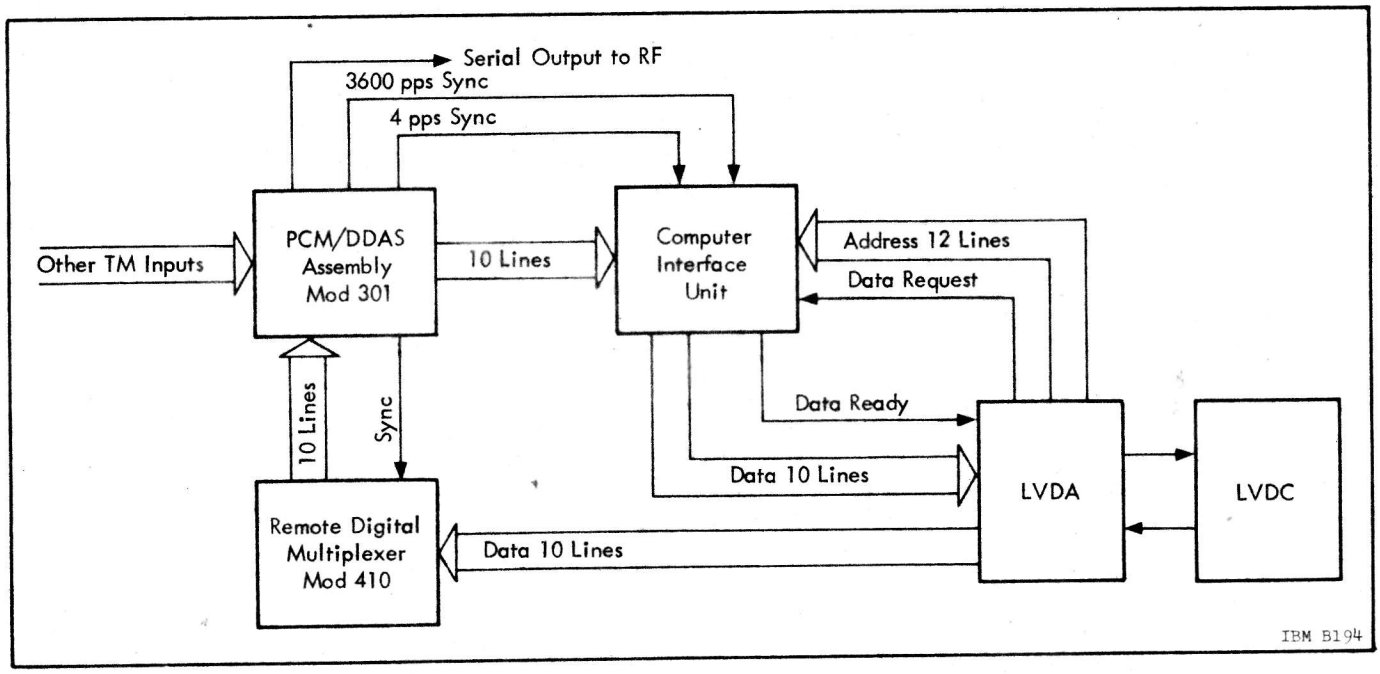


Figure 5.3-13 Computer Interface Unit System Interconnection Diagram

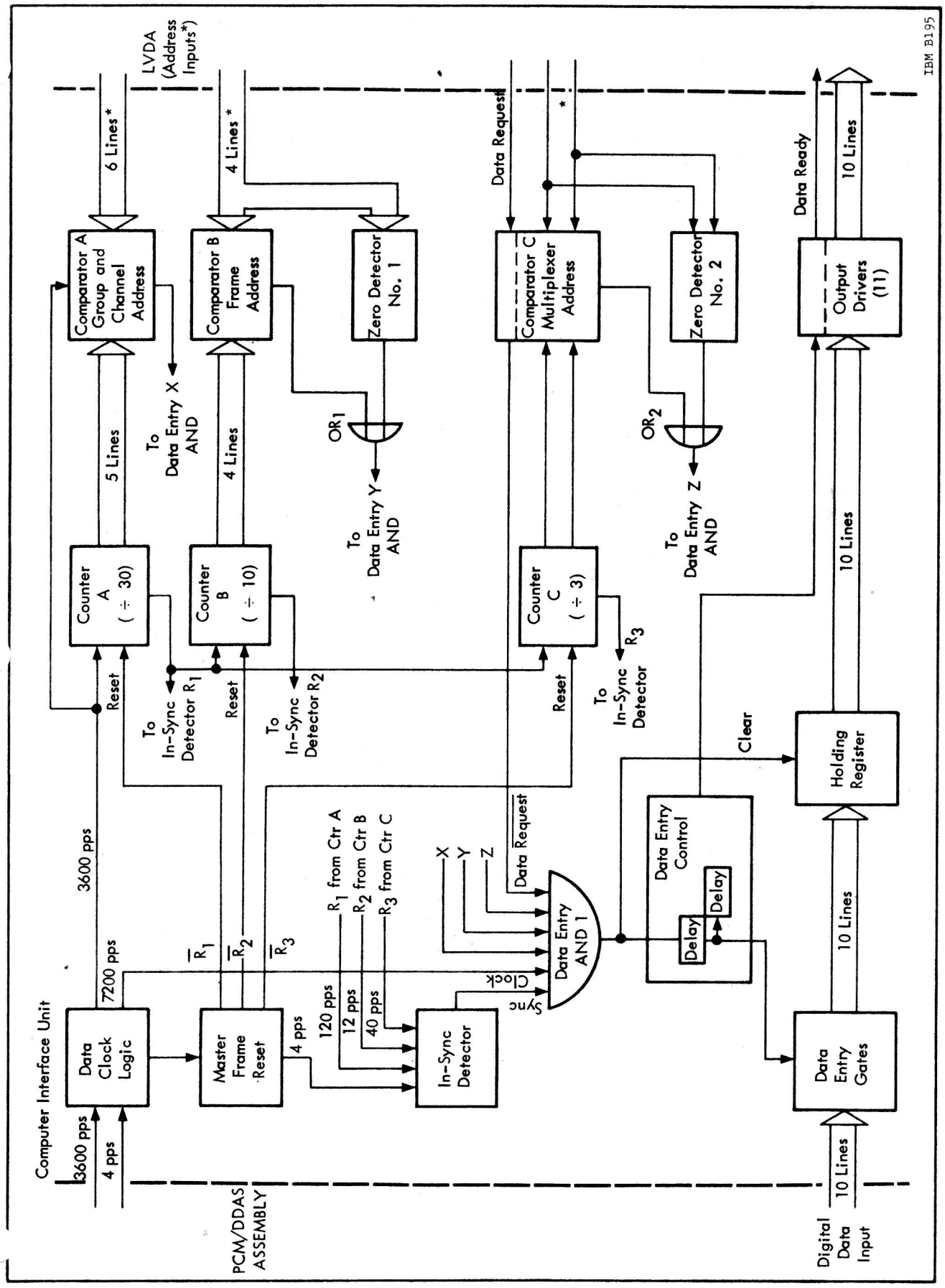


Figure 5.3-14 Computer Interface Unit Block Diagram

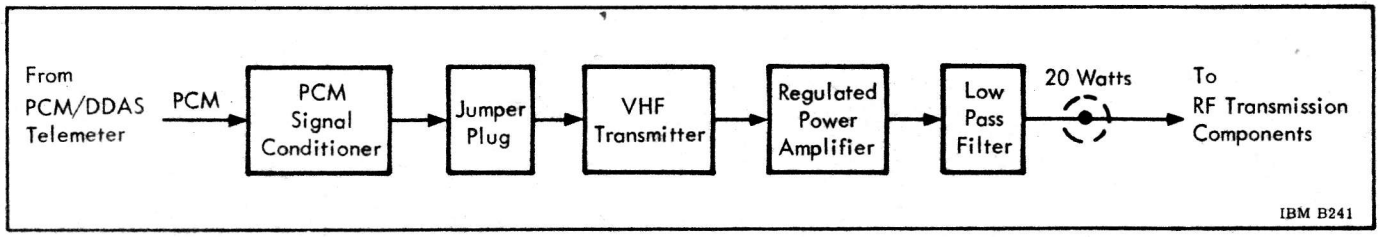


Figure 5.3-15 PCM/RF Assembly Block Diagram

Assembly as modulation for a UHF carrier. The unit operates in parallel with the PCM/RF Transmitter Assembly. See Figure 5.3-1 for the location and function of the UHF/RF Transmitter Assembly within the telemetry system. The unit uses a combination of solid-state devices and vacuum tubes to transmit through the RF transmission components.

A UHF/RF Filter serves as a bandpass filter for the output of the UHF/RF Transmitter. The filter ensures that noise generated by the transmitter is not radiated by the UHF antenna (which, if unfiltered, could overlap the signal received by the CCS receiving antennas).

CCS TELEMETRY

Information on the Command and Communication System (CCS) – as related to the Saturn Telemetry System – may be found in Section 6.4.

5.3.7 TELEMETRY-CALIBRATION

The purpose of TM calibration (see Figure 5.3-16) is to assist in determination of telemetry equipment accuracy. This is done by furnishing selected telemetry equipment with known, precise inputs in place of the normally broadcast measurements signals. The normally broadcast signals are compared to the calibrated broadcast signals to obtain the exact degree of telemetry equipment accuracy.

TM calibration is used during flight and prelaunch checkout. During flight, TM calibration is controlled by the program of the LVDC. For prelaunch checkout, TM calibration is controlled by ESE in the control center.

Two components and special circuitry in other components provide TM calibration. The two components are the TM Calibrator and the TM Calibrator Controller. Special circuits to accept calibration inputs are located in F2 and P1 Multiplexers, F1 and F2 Telemeters, and S1 Telemeter.

The TM Calibrator and TM Calibrator Controller function together to furnish and control the calibration inputs to the telemetry components. These two units together are referred to as the Calibrator-Controller Assembly. The Calibrator selects the calibration signal level and selects the component to be calibrated. The Controller furnishes regulated power to the Calibrator and also serves as an interface unit, routing and isolating all signals to and from the Calibrator.

The Calibrator-Controller Assembly furnishes six outputs for calibration of model 270 multiplexers or FM telemeters, and three outputs to calibrate single sideband telemeters. Each of these units that are to be calibrated contain circuitry to accept the calibration command and apply the calibrated signals to their individual data channels. While up to nine components can be calibrated by the Calibrator-Controller Assembly, the full capability is not used. For clarity of explanation, this description of operation assumes that full capability is used.

To increase system flexibility, all inputs and outputs of the Calibrator-Controller Assembly are routed through a Measuring Distributor. This allows the inputs and outputs to be patched to selected telemetry equipment without modification to launch vehicle wiring.

During prelaunch checkout, the calibration capabilities are greatly expanded. Any of several preflight calibrations may be selected in addition to the normal inflight calibration.

The equipment is operated in either the inflight mode or the prelaunch mode. During inflight mode, the telemetry equipment is calibrated by preset signals in a preset sequence when commanded to do so by the LVDC program. During prelaunch mode, the LVDC command may be simulated or variable calibration signals may be furnished to the telemetry equipment.

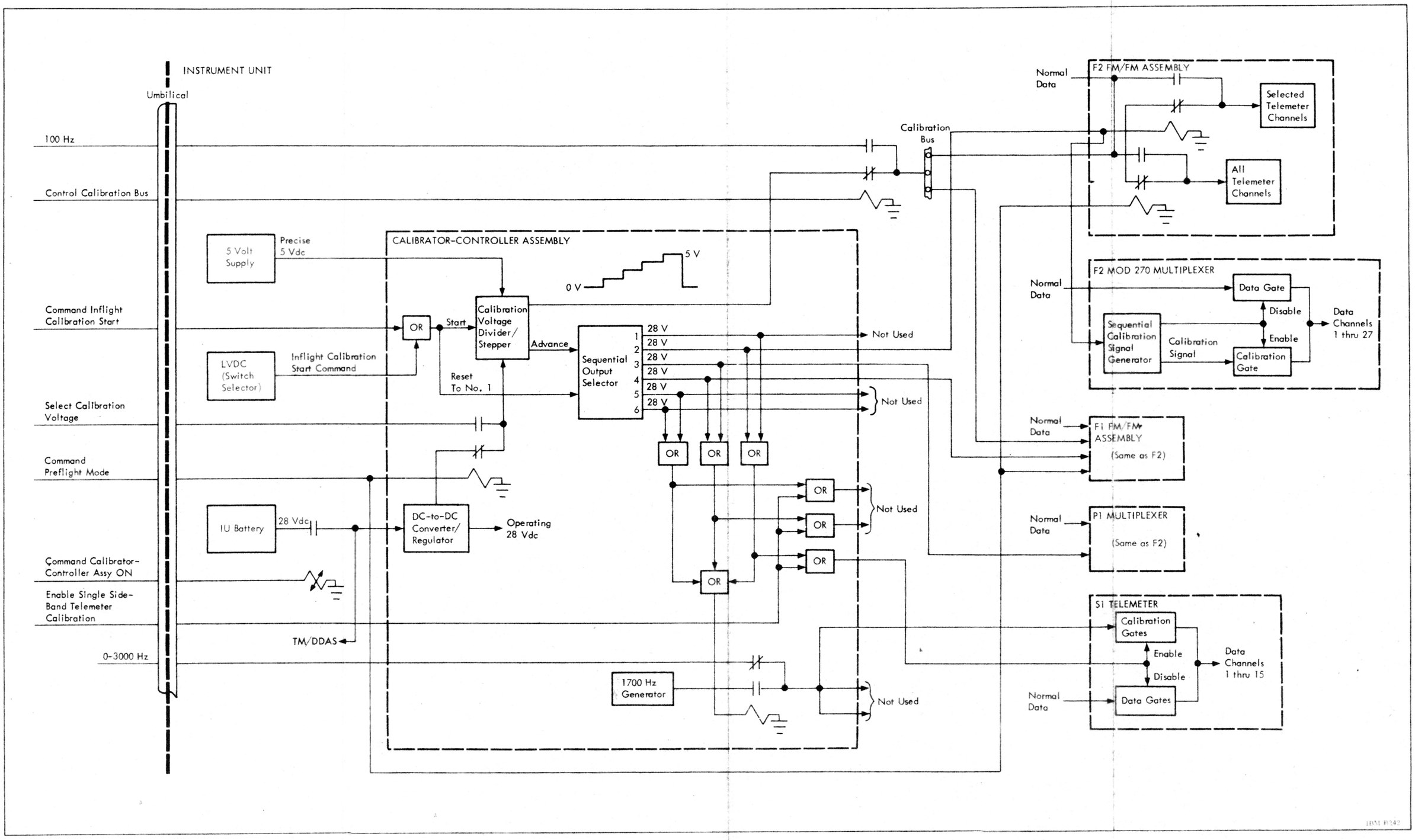


Figure 5.3-16 Telemetry Calibration Functional Diagram

SECTION 5.4
TELEVISION SYSTEM (SATURN V)

The Saturn V Launch Vehicle television system will be used to provide both real-time and permanent visual data on the performance of certain vehicle functions. No television is planned for use on Saturn IB operational vehicles.

A block diagram of the vehicle and ground equipment is illustrated in Figures 5.4-1 and 5.4-2. Table 5.4-1 lists the television system characteristics.

Figure 5.4-1 illustrates the path of the video signal from the camera, through the video register, to the transmitter. A description of the circuitry follows:

The television cameras are small, having an outside diameter of 7 centimeters (2.8 inches) and a length of 35 centimeters (13.8 inches) The Saturn V television system will include two such cameras.

The video register unit is a sync generator and video multiplexing unit. This unit is capable of driving up to 4 cameras, accepting the video outputs of each, and multiplexing the output at either a field, frame, or 2-frame rate. The Saturn V system will be multiplexed at a 2-frame rate.

Since there are actually 4 areas to be viewed in the engine compartment and only 2 cameras, a split fiber optic bundle is used on each camera. Each bundle is split at the lens' end and uses two objective lenses. The view covered is shown in Figure 5.4-3.

The output of the video register unit is fed to the transmitter, which is an FM system.

The ground system shown in Figure 5.4-2 provides 2 units for recording the demodulated signal as it is received and a system for real-time viewing.

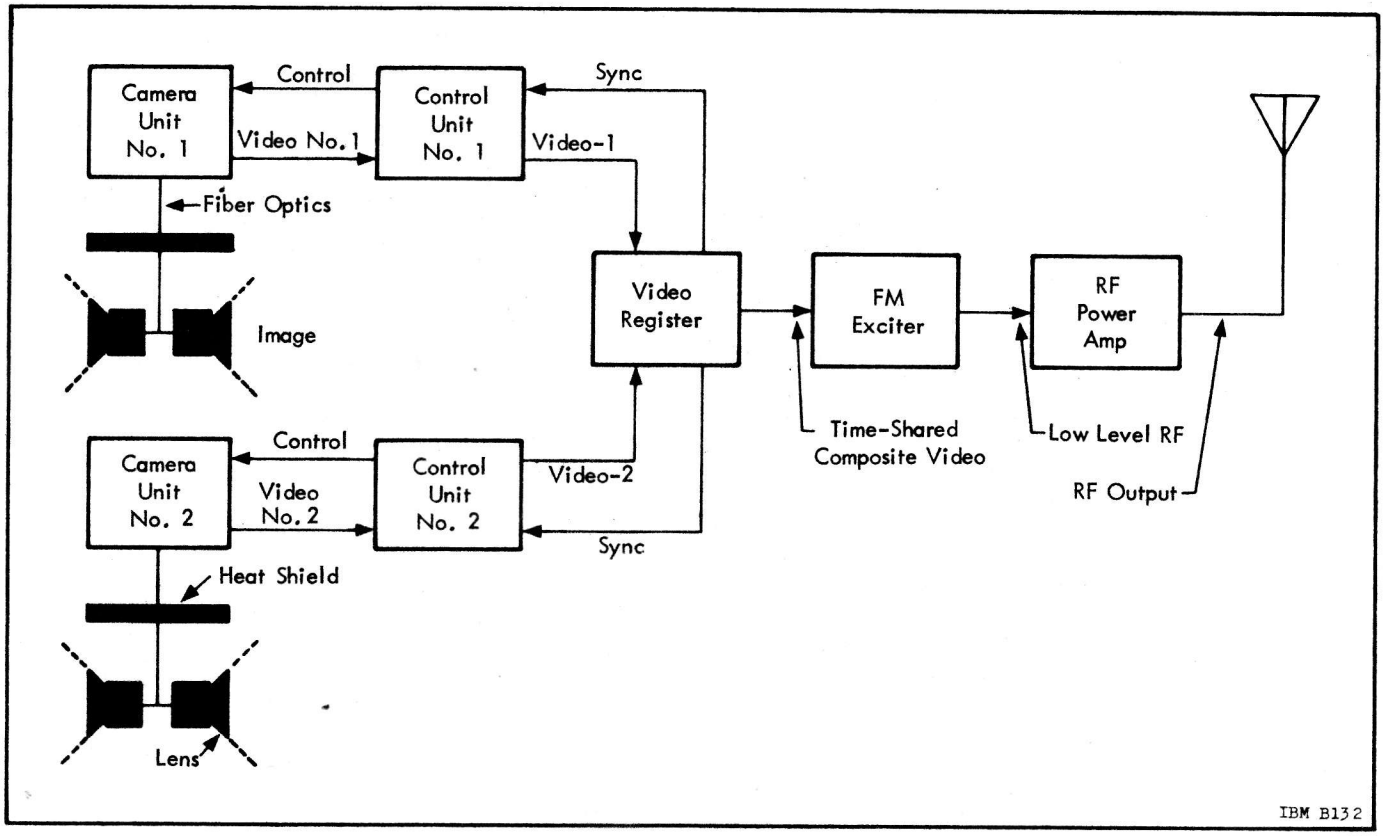


Figure 5.4-1 S-IC Television Function Block Diagram

Table 5.4-1 Saturn V Launch Vehicle Television Characteristics

Transmitter	
Video bandwidth	8 MHz
Modulation	FM
Deviation	10 MHz (for complete video
Output power	2.5 watts (minimum)
Unmodulated frequency	1705 MHz ± 0.20%
Video resolution (horizonal) of received picture	500 lines
Closed Circuit Camera System	
Camera light sensitivity	10.76 lumens/meter^2 (1.0 foot candle)
Video bandwidth	8 MHz
Frame rate	39/second
Scanning	2:1 Interlace
Specifications of Television Ground Station for Support of Saturn Television Systems	
Parametric amplifier	
Gain	20 db (minimum)
Noise figure	1.35 db
Frequency range	1700 to 1720 MHz
Receiver	
Frequency range	1700 to 1720 MHz
Gain	90 db (minimum)
Noise figures	12 db (maximum)
Signal Processing and Distributing Amplifier	
Video bandwidth	8 MHz
Number of outputs	4
Sequence Decoder	
Video bandwidth each output	8 MHz
Number of outputs selectable	1 to 16
Switching time	0.1 us
Video Tape Recorder	
Video bandwidth	5.5 MHz
Tape speed	38 cm/s (15 in./s)
Recorder time	96 minutes
Kinescope Recorder	
Camera frame rate	30/second
Film capacity	365.8 meters/minute (1200 feet/minute)
Viewing Monitor	
Video bandwidth	8 MHz
Video resolution (horizontal)	600 lines

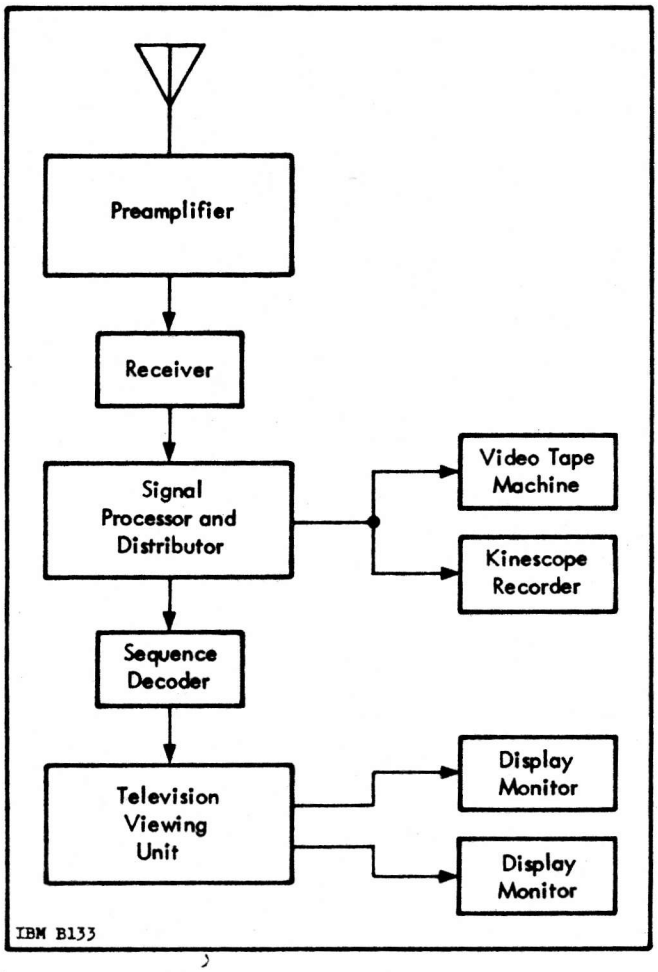


Figure 5.4-2 Television Ground Receiving Station

The systems used for recording the video are one broadcast-type video recorder and one kinescope recorder. Video recorded on both of these systems is still in a multiplexed sequence. For real-time viewing, special equipment is required (i.e., sequence decoder and television viewing unit).

The function of the sequence decoder is to demultiplex the video signal and feed the output of each camera to the same monitor. If the sequence decoder were used alone, the video being fed to each monitor would be composed of 2 frames of video followed by 2 blank frames.

To eliminate the "blinking" picture caused by the above signal, the television viewing unit is provided. This unit uses a storage system and command signals from the sequence decoder to fill the blank 2-frame time with video information from the previous frame. This gives a steady picture. The picture information rate, however, would be at 7-1/2 frames per second. Although the picture appears steady, motion would be jerky.

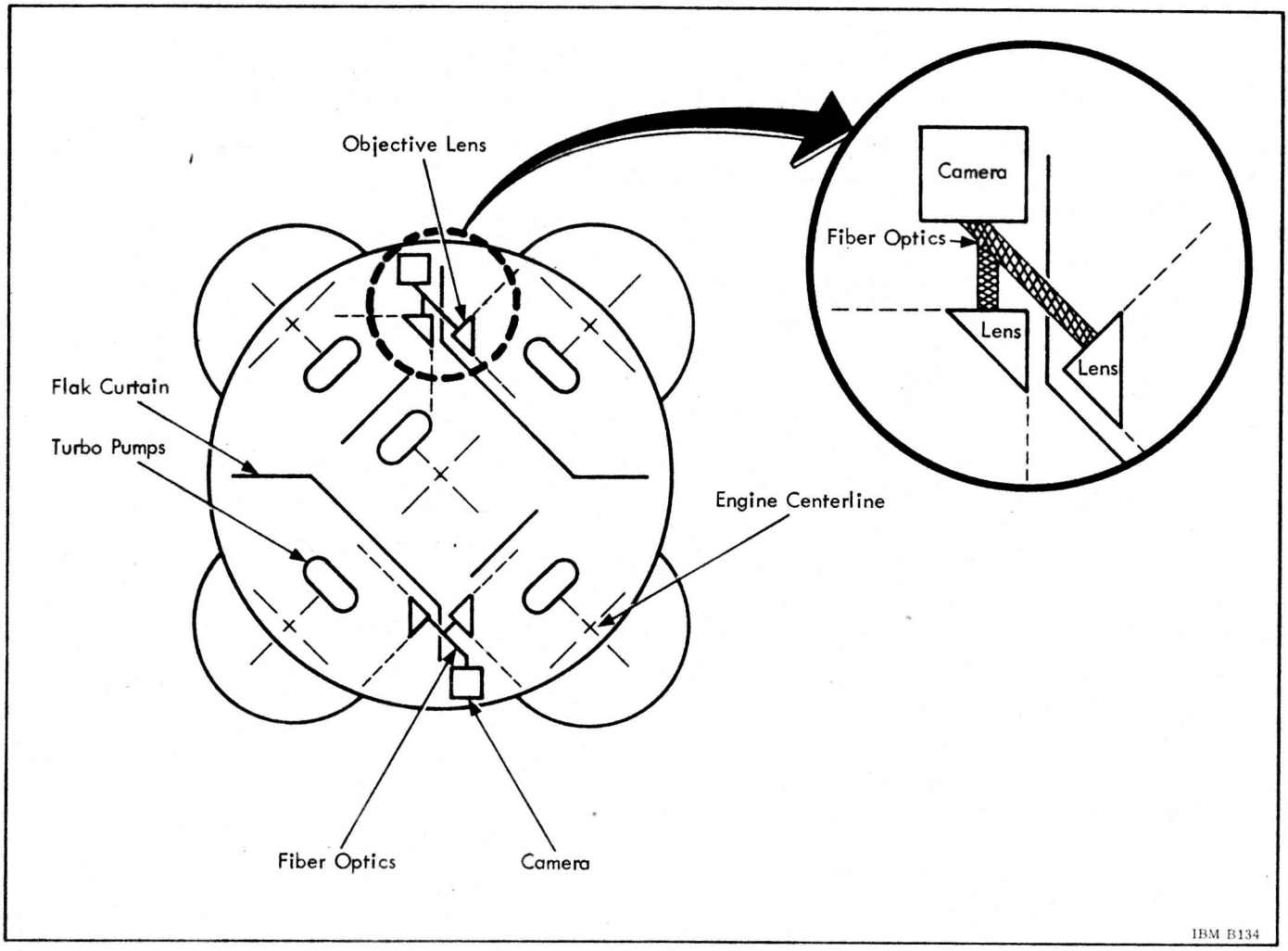


Figure 5.4-3 S-IC Tentative Television Optic Layout

SECTION 5.5
OPTICAL INSTRUMENTATION

Recoverable, inflight 16mm motion picture cameras are used by Saturn IB/V Launch Vehicles to record specific events (e.g., stage separation). The cameras are mounted in camera capsules within ejection tubes. The complete units are located in close proximity to the subjects the cameras are to record.

When the cameras have completed their missions, the capsules (with cameras intact) are pneumatically ejected from their mounting tubes. Following this ejection, camera capsule stabilization flaps are deployed. At an altitude of 4300 meters (14,100 feet), a paraballoon is inflated and causes the stabilization flaps to fall away. A recovery radio transmitter and flashing light beacon, located on the paraballoon, are then turned ON. (Saturn IB capsules do not use the beacon recovery aid.)

After touchdown, the capsule effuses a dye marker to aid visual sighting of the capsule and a shark repellent to protect the camera capsule, paraballoon, and recovery team.

CAMERA CAPSULES

The camera capsule, shown in Figure 5.5-1 contains 3 compartments—the camera compartment, recovery systems compartment, and lens compartment. The camera compartment provides:

- Rigid camera mounting
- Controlled atmosphere
- Camera protection
- Control system (recovery aids deployment)

The recovery systems compartment provides the following aids:

- Stabilization flaps
- Paraballoon
- Radio transmitter
- Light beacon (Saturn V only)
- Dye marker
- Shark repellent

The lens compartment provides:

- Secure lens mounting
- Controlled atmosphere
- Lens protection
- Double bulkhead protection (against water leaks)

The Saturn IB radio transmitter is pulse modulated and operates on a frequency 242 megahertz at 15 watts for a lifetime of 36 hours (20 hours on Saturn V). The light beacon, used on Saturn V, operates at a rate of 40 flashes per minute.

CAMERA MISSIONS

On AS-501 and 502, the S-II Stage carries two camera capsules mounted on the structure at Positions I and III. From this position, the capsules view first plane separation, J-2 engine start, engine gimballing, and second plane separation. In addition, the S-II Stage on AS-502 carries 2 rings of separation tracking aid lights on the aft interstage. The rings each contain fourteen 62-watt lamps. The upper lamps provide S-IC camera reference, and the lower lamps are for the S-II cameras.

On AS-502 and 503, the S-IC stage is equipped with 4 recoverable film camera capsules. Two of these cameras, located on the S-IC forward interstage, view forward during the first plane separation and J-2 engine start. The other 2 capsules, mounted on top of the LOX tank at Positions II & IV, contain pulse cameras which view aft into the LOX tank through fiber optics bundles. The LOX tank is lit by strobe lights which operate at a rate of 5 flashes per second. One strobe light provides spotlight illumination of the tank bottom; and the other provides a wide beam for general tank illumination. The strobe lights and pulse cameras are operated and synchronized by a pulse from the camera film marking timer at a rate of 5 per second. The timer also provides for film marking in binary code. A similar timer is used on the S-II stage.

Table 5.5-1 summarizes the coverage provided by the optical instrumentation system.

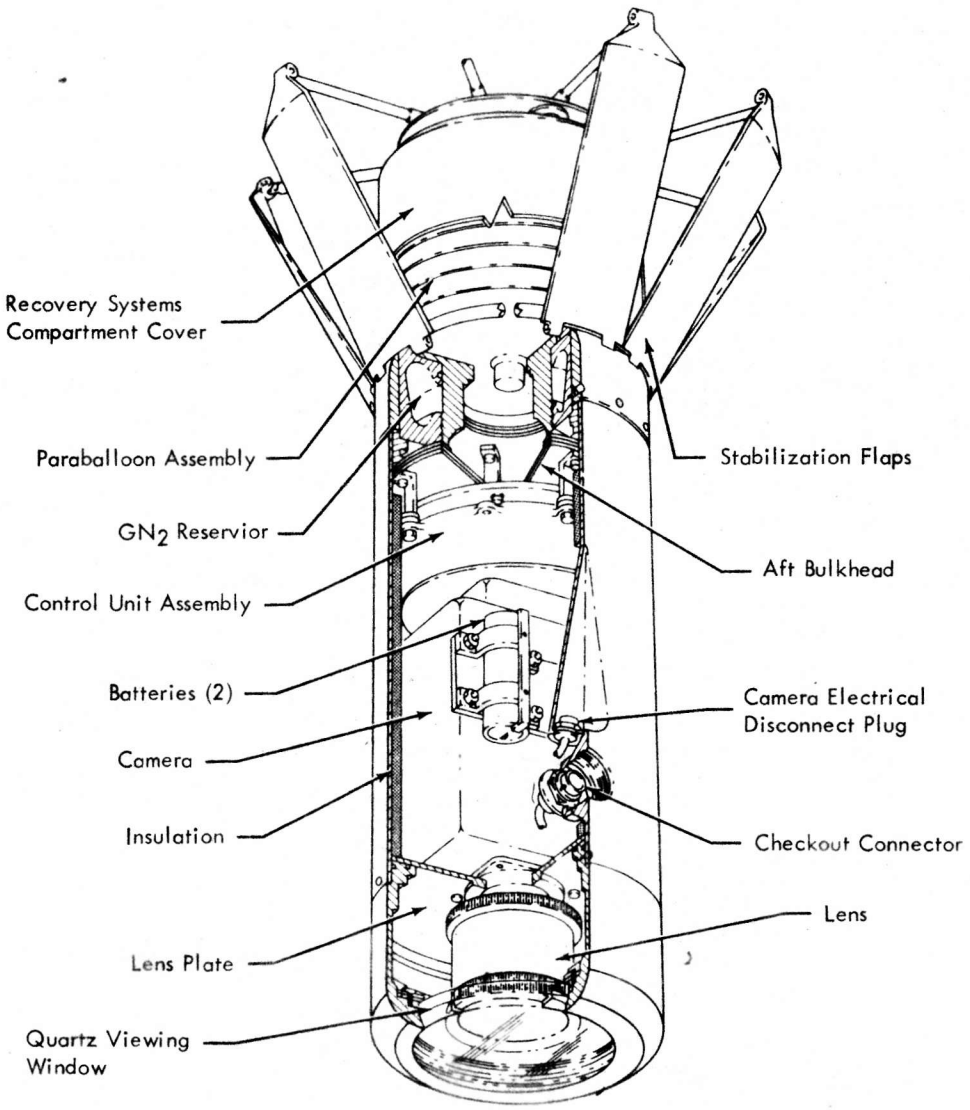


Figure 5.5-1 Typical Direct-View Camera Capsule

Table 5.5-1 Saturn Onboard Motion Picture Coverage

Location of Film Cameras	Coverage Provided	No. of Cameras	Frame Rate	Running Time (seconds)	Vehicle Effectivity	Illumination
Top of S-IB Stage between Positions I & II and III & IV	S-IB/S-IVB separation and J-2 engine start	2	128	29	201, 202, 203	Natural
Top of S-IC LOX tank at Positions II & IV	Interior of LOX tank	2	5	226	502, 503	Strobe lights
S-IC forward inter-stage at Positions I & III	S-IC/S-II separation and J-2 engine start	2	100	27	502, 503	Natural with separation tracking aid lights
S-II thrust cone at Positions I & III	S-IC/S-II separation, S-II second plane separation and J-2 engine start	2	100	38	501, 502	Natural with separation tracking aid lights

CHAPTER 6
RADIO COMMAND SYSTEMS

SECTION 6.1
INTRODUCTION

The Saturn Vehicles carry two radio command systems, one for range safety and the other for data transmission to the Instrument Unit (IU).

The range safety command system provides a means to terminate the flight of the vehicle by radio command from the ground in case of emergency situations in accordance with range safety requirements. Each powered stage of the vehicle is equipped with two Command Receivers/Decoders and the necessary antennas to provide omnidirectional receiving characteristics (range safety requirements). The command destruct system in each stage must be completely separate and independent of those in other stages. In case of vehicle malfunctions which cause trajectory deviations larger than specified limits, the vehicle will be destroyed by the Range Safety Officer by means of the range safety command system. The range safety command system is active until the vehicle has achieved earth orbit. After successful insertion into earth orbit, the destruct system is deactivated (safed) by command from the ground. The early Saturn IB and Saturn V Vehicles will be equipped with a tone command system (AN/DRW-13) which will be replaced in later vehicles by a system called the secure range safety command system.

The IU command system provides digital data transmission from ground stations to the Astrionics System in the IU. This command system will be used to update guidance information or to command certain functions in the S-IVB/IU Stage. The IU command system will not be used during powered flight phases.

Section 6.3 presents a description of the secure range safety command system, which is applicable to each powered stage of both the Saturn IB and the Saturn V Vehicles.

Section 6.2 presents a description of the IU command system used on the Saturn Vehicles. In general, the Saturn IB and Saturn V IU command systems are similar in operation, and the material presented in this chapter is applicable to the IU command system on both vehicles. The exception is subsection 6.2.4 (Command Receiver), which is applicable only to the Saturn IB Vehicle. The Command Receiver in the Saturn IB IU is replaced on Saturn V by the Command and Communication System (CCS) Transponder (subsection 6.4.2).

The Saturn V CCS consists of the transponder, a power amplifier, and an antenna system. The CCS transponder is a phase coherent receiver-transmitter which receives and demodulates a composite 2101.8 MHz carrier containing the command signal and a Pseudo-Random Noise ranging code. It transmits the response to the ranging code, and also PCM telemetry data, on a 2282.5 MHz carrier. The CCS Power Amplifier boosts the output of the CCS Transponder to a nominal 15 watts. The rf carrier is then transmitted through the CCS antenna system. The CCS antenna system is switched by a Switch Selector command from omnidirectional to directional low-gain or high-gain antennas as required by the mission profile.

SECTION 6.2

INSTRUMENT UNIT COMMAND SYSTEM

6.2.1 GENERAL SCHEME

The IU command system is used to transmit digital information from ground stations to the Launch Vehicle Digital Computer (LVDC) in the IU. Figure 6.2-1 is a block diagram of the command system for Saturn V.

The commands and data to be transmitted to the vehicle originate in the Mission Control Center (MCC) in Houston, Texas, and are sent to the remote ground stations of the Manned Space Flight Network where they are transmitted to the vehicle. At the ground stations, the command messages (in digital form) are processed, temporarily stored, and then modulated onto an rf carrier by a Digital Command System (DCS). The command message is transmitted in the S-band on a carrier frequency of 2101.8 MHz.

The signal (often referred to as up-data) is received and demodulated by the CCS Transponder. The resultant signal is fed to a Command Decoder where address verification and final message decoding is accomplished. From the Command Decoder, the command message (in digital form) is sent through the Launch Vehicle Data Adapter (LVDA) to the LVDC. Verification of the acceptance or rejection of the command message is telemetered to the ground station via the IU telemetry system. If a message is rejected, pertinent data concerning the rejection will also be telemetered. In the case of the Saturn V command system, the telemetry messages are actually transmitted through the transmitter portion of the CCS Transponder. The CCS Power Amplifier boosts the rf signal to approximately 15 watts.

At the ground station, the verification and acceptance data is recovered from the telemetry

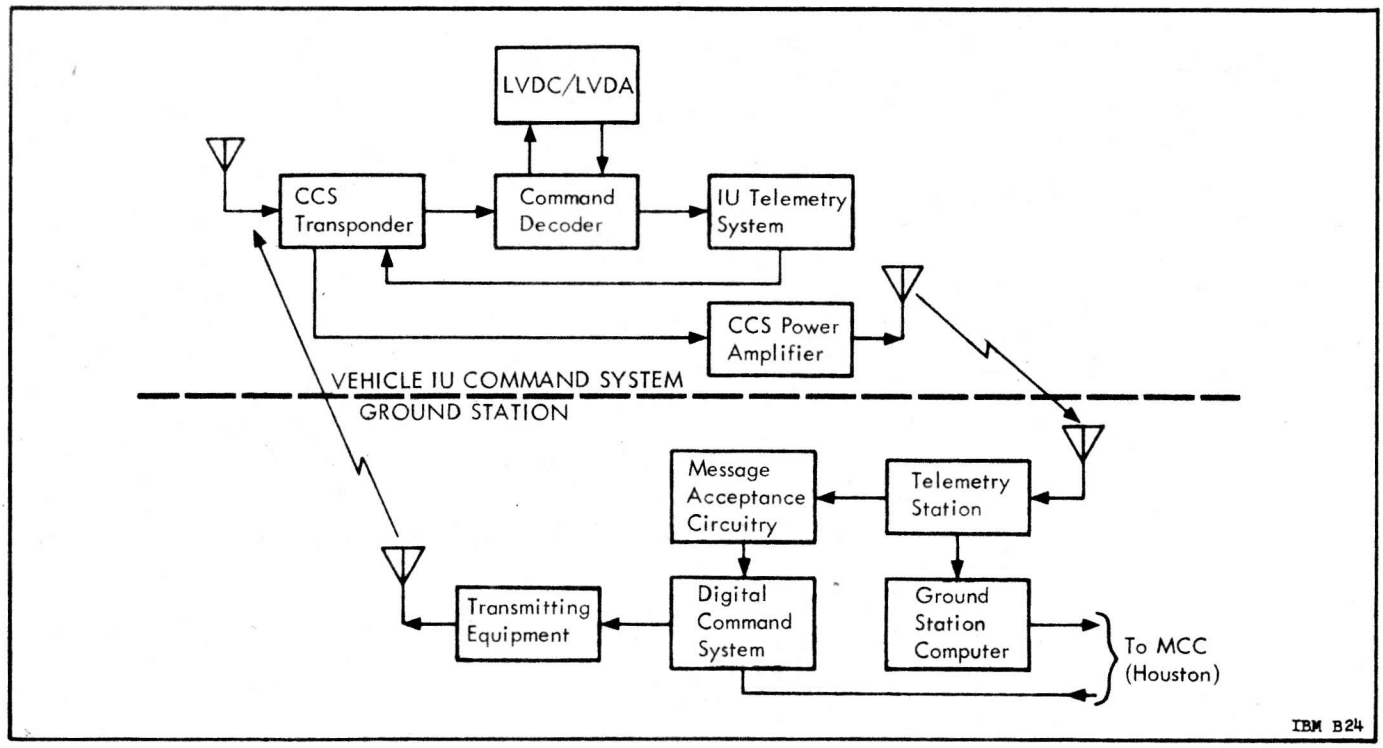


Figure 6.2-1 Saturn V IU Command System

message and fed to the DCS through special circuitry. The remainder of the telemetry data is forwarded to the MCC. If and acceptance message is not received by the ground station within a preset length of time, the same message will be retransmitted. Presently, a total of seven such attempts will be made before the message is abandoned.

The Saturn IB Vehicles use a slightly different command system configuration, which is shown in Figure 6.2-2. The primary difference is that the Command Receiver, instead of the CCS Transponder is used to receive and demodulate the up-data messages. The functional schemes of the Saturn IB and Saturn V command systems are identical with the exception of carrier frequencies used: Saturn IB uses 450 MHz and Saturn V uses 2101.8 MHz.

The IU command system is closely related to the Apollo Spacecraft up-data link. Both systems use essentially the same ground station equipment of the Manned Space Flight Network.

6.2.2 MODULATION TECHNIQUES

The ground modulator used with the IU command system is the same as the one used on the Gemini Program and for the Apollo Spacecraft up-data link. This modulator is part of the DCS console, which serves as the encoder for several different space programs.

The DCS utilizes Phase Shift Keyed (PSK) modulation. This PSK modulation is accomplished by algebraic addition of a 1 kHz reference sine wave to a phase coherent 2 kHz sine wave. (Refer to Figure 6.2-3). A "1" or a "0" sub-bit is generated each cycle of the 1 kHz sine wave, beginning at the zero crossing when the sine wave is going positive. A "1" sub-bit is generated by addition of a positive going 2 kHz sine wave to the 1 kHz sine wave. For a "0" sub-bit, the 2 kHz sine wave is phase shifted 180 degrees and added to the 1 kHz sine wave. This composite waveform then modulates an rf carrier for transmission to the vehicle. In the Saturn IB IU command system, the 450 MHz rf carrier is frequency modulated. In the Saturn V IU command system, the composite baseband waveform frequency modulates an intermediate carrier (subcarrier) of 70 kHz, which in turn phase modulates a 2101.8 MHz rf (S-band) carrier. The Saturn IB modulation scheme (at 450 MHz) is referred to as PSK/FM, and the Saturn V modulation scheme (at 2101.8 MHz) is called PSK/FM/PM.

6.2.3 COMMAND WORD FORMAT

The command word consists of 35 digital bits which are used for data transmittal, addressing, and control. A standard command-word format is shown in Figure 6.2-4 and is applicable for Saturn IB and V Vehicles.

The first 3 bits of each command word represent a vehicle address and are referred to as "X" bits.

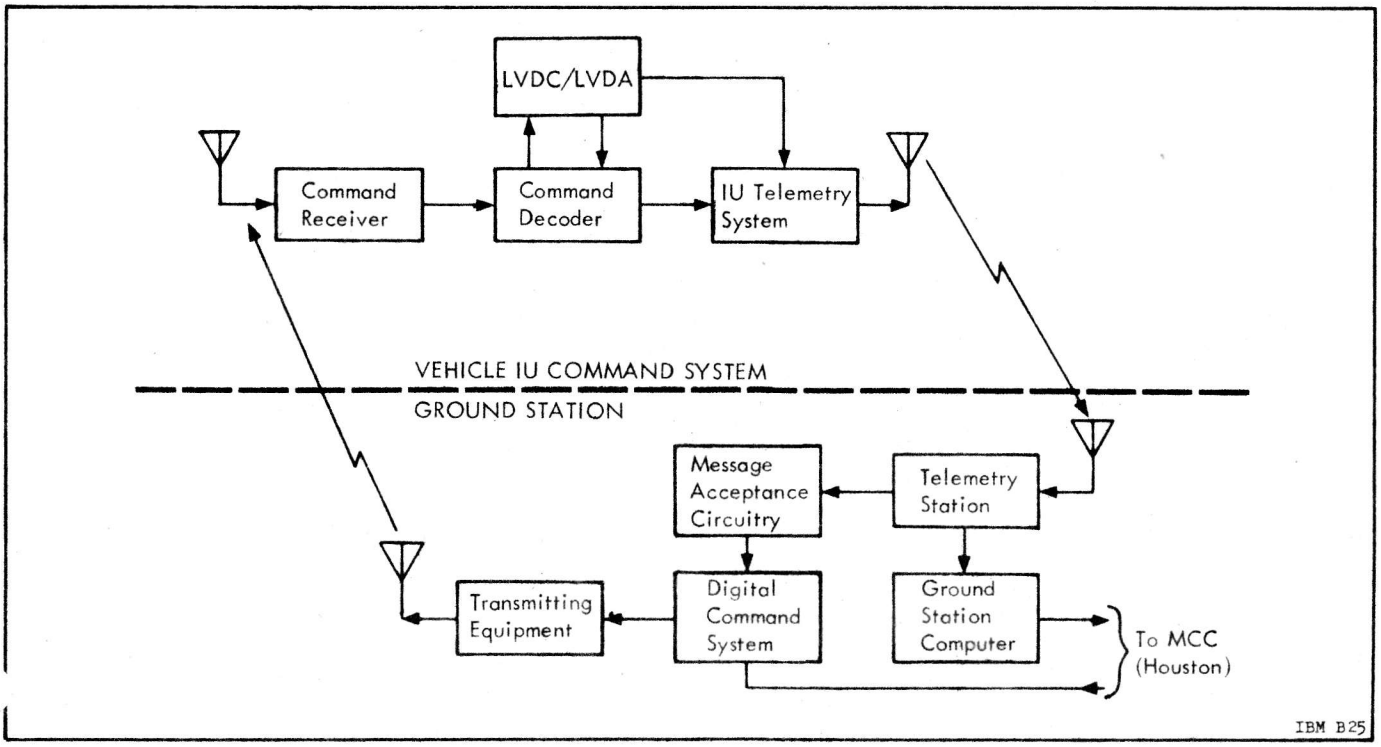


Figure 6.2-2 Saturn IB IU Command System

The remaining 32 bits are made up of "1's" and "0's" as determined by the message content. Fourteen of these 32 bits are used as decoder address bits and are distributed throughout the word. The 14 bits are compared with a prewired address in the Command Decoder and perform a dual function of address verification and error checking. Since more than one Command Decoder may be used on the same vehicle, this addressing scheme will ensure correct message reception.

The remaining 18 bits of the command word are used as control bits and actual digital data for the LVDC/LVDA. (All data bound for the LVDC is processed by the LVDA, which is the input-output device for the LVDC.)

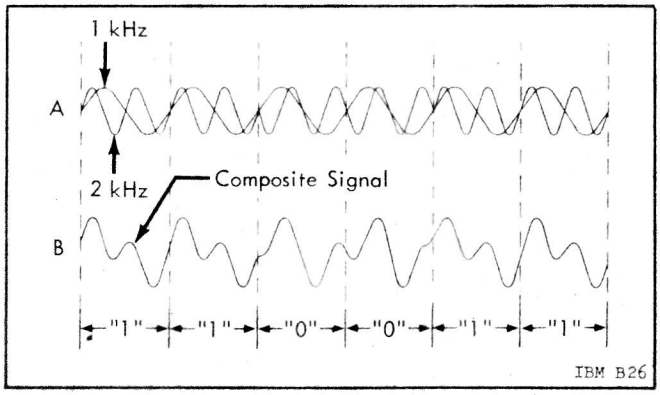


Figure 6.2-3 Phase Shift Keyed Signals

The LVDC is programmed to receive two types of command words from the Command Decoder: mode command words and data command words. The LVDC is able to distinguish between these command words by checking the status of bits 10 and 12, which are labeled as Orbital Mode/Data (OM/D) bits. These bits are logically combined into one bit as they enter the LVDA. Similarly, bits 8 and 9 are combined in the LVDA to form a single interrupt bit. This interrupt bit informs the LVDC that a command message has been received and is awaiting processing. The remaining 14 bits contain the command message intended for the LVDC. Of these 14 bits, 7 bits are actual (true) message bits, and 7 are the complement (exact opposite) of the true bits. This scheme serves as another reliability check on the command message.

Each of the 35 bits is encoded into 5 sub-bits (total of 175 sub-bits). The vehicle address is encoded into a different sub-bit pattern than the following 32 information bits. The sub-bit patterns are chosen for optimum differentiation between bits to provide maximum error detection capability. For any given flight, only three of the possible 32 ($2^5 = 32$) 5-bit patterns are used.

To simplify the following discussion, the sub-bits will be disregarded unless particular reference is made to them.

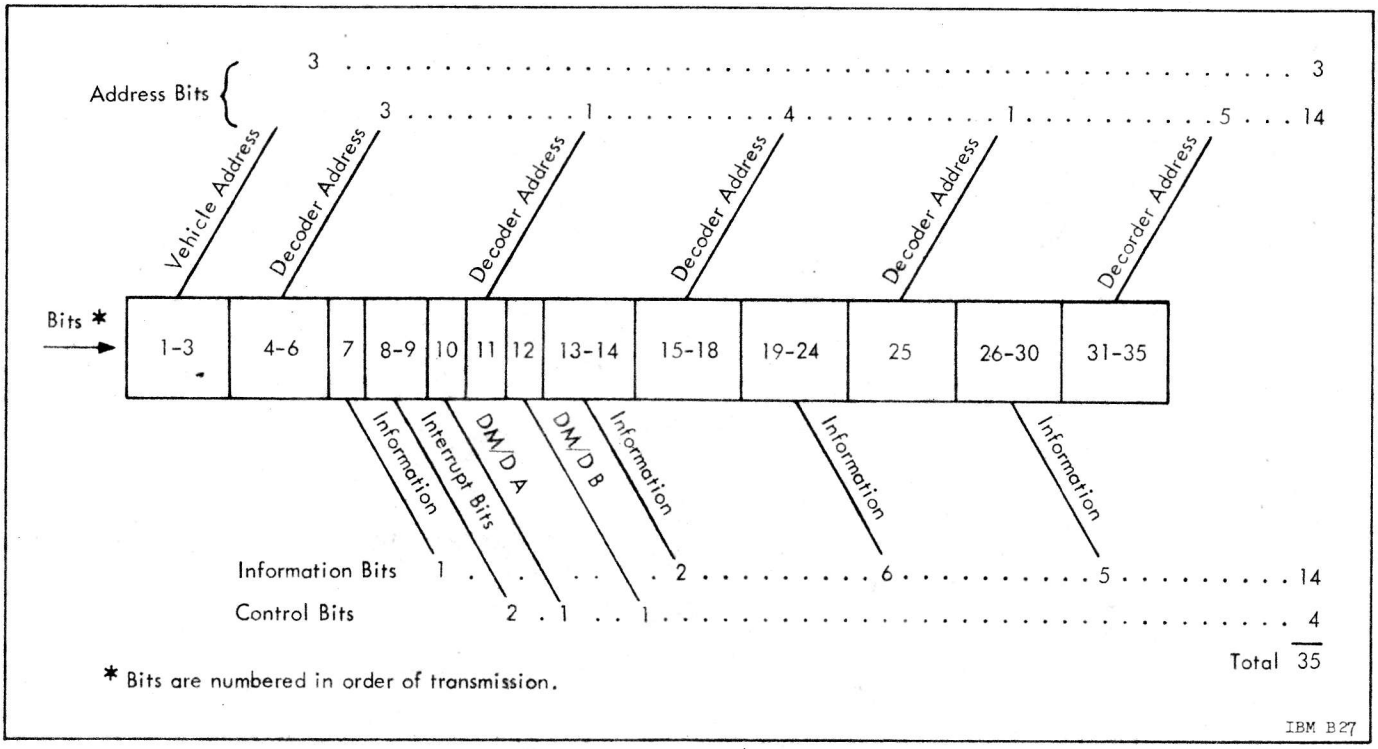


Figure 6.2-4 Command Word Format Showing Address and Information Distribution

MODE AND DATA COMMANDS

The command interrupt routine of the LVDC program is programmed to receive up to a maximum of 26 different mode commands. Normally, about one-third of these commands are common to all flights and the remainder are either unused or are programmed for a particular vehicle or flight. Common mode commands include such commands as:

- Update of a time base
- Navigational update
- Execution of Switch Selector routines
- Telemetering of memory contents
- Termination of other command routines
- Alteration of target azimuths.

All mode commands are completed in one message word. A mode command format is shown in Figure 6.2-5.

Data commands, as the name implies, contain digital data to supplement a given mode command. The format for each data command is unique to the mode command with which it is used. Since some mode commands require more data than others, the number of data words will vary with the command. For example, a navigational update requires 35 data words, while a time base update requires only 1 data word. A 1-word data command format is shown in Figure 6.2-5.

Bit position 8 of the data command word is the sequence bit for multi-worded data commands. The first data command word will always have a logical "1" in the bit 8 position. Following data command words will have alternate "0's" or "1's" in that position. These bits are checked by the program to ensure that the data command words are being received in the correct order and that a word has not been accidently lost. It should be noted that bit 8 of a mode command word will always be a logical "0", since it is a single word message, it will not alternate.

COMMAND PROCESSING

The LVDC will interrogate the OM/D bit and 14-bit command word each time the IU Command Decoder sets an interrupt bit into a special LVDA storage register. The LVDC command program is a special routine designed to process the incoming command message. Normally, the LVDC will be executing its main flight and orbital programs, but it is prepared to receive a mode command. When interrupted by a command message, the LVDC will:

- Verify that the OM/D bit is a "1", indicating mode information.
- Test the command word (check the 7 true bits against the 7 complement bits).
- Decode and verify the command.
- Telemeter a status code indicating to the ground that the LVDC has entered a command routine.
- Prepare to accept data to supplement the mode command.

If the commanded routine requires data, a Command Decoder interrupt will initiate the following sequence:

- Verify that the OM/D bit is a logical "0", indicating data information.
- Test the command word (check the 7 true bits against the 7 complement bits).
- Verify that the data is received in sequential order. (Bit 8 will alternate between a logical "1" and "0" for multi-worded data messages.)
- Temporarily store the data
- Prepare, if necessary, to receive the next data word.

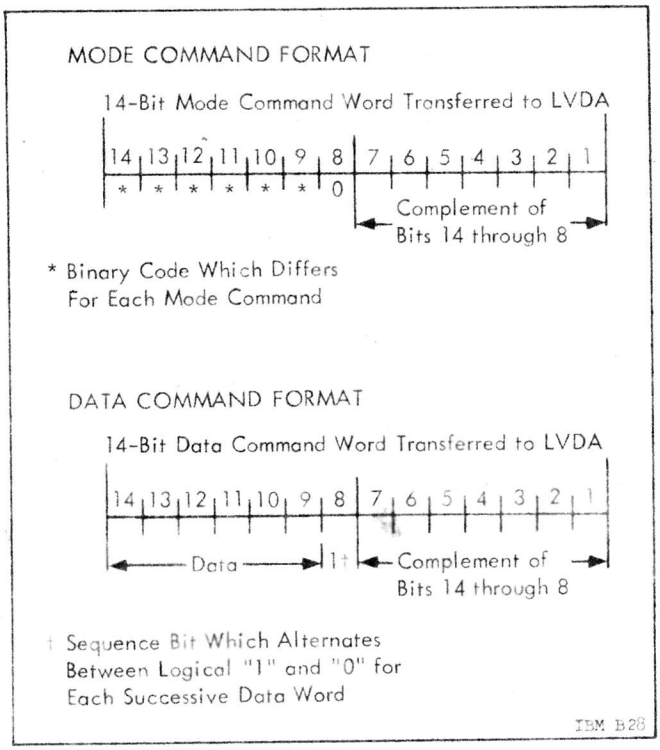


Figure 6.2.-5 Command Word Format

Once the LVDC has entered a commanded routine, it will not accept another mode command (except a terminate) until all data has been received and the routine has been executed. The terminate command will discontinue any routine in progress.

6.2.4 COMMAND RECEIVER

The Saturn IB IU command system uses the MCR-503B Command Receiver with a frequency range of 406 to 450 MHz. In the Saturn V Vehicle, the IU command is received by the CCS Transponder of the Saturn command and communication system. The CCS Transponder is described in Subsection 6.4.2.

A block diagram of the Command Receiver is shown in Figure 6.2-6. The received rf signal is coupled from the rf input, J1, to a fixed-tuned, low-pass filter. The output of the low-pass filter is connected to a critically coupled, double-tuned bandpass filter, which is tunable over the required frequency range of 406 to 450 MHz. The bandpass filter output is amplified by an rf amplifier stage. This amplifier provides additional rejection to signals outside the receiver passband and is tunable over the required frequency range. The low-pass filter, bandpass filter, and rf amplifier are contained in the preselector assembly.

The preselector assembly output is coupled to the first mixer. Here the x3 multiplied output of the crystal oscillator is heterodyned with the rf signal to produce the first IF signal. The first IF signal is amplified by the first IF amplifier and applied to the second mixer, where it is heterodyned with a signal at the crystal oscillator frequency to produce the 10.7 MHz second IF signal. The first and second mixer, first IF amplifier, crystal oscillator, and x3 frequency multiplier are contained in the first IF amplifier assembly. The -3 db bandwidth of this assembly is approximately 1.5 MHz and the gain is approximately 43 db.

The output of the first IF amplifier assembly is coupled directly to an IF bandpass filter. This passive LC filter determines the overall receiver bandpass characteristics.

The bandpass filter output is fed to the second IF amplifier assembly, which contains two feedback IF amplifier pairs. The output of the second IF amplifier pair feeds both the limiter-discriminator assembly and the low-level TM amplifiers. The low-level telemetry output is a dc voltage that is proportional to the receiver rf input signal.

Limiting is accomplished in the first limiter by back-to-back diodes in a transistor's collector circuit. The second limiter limits by saturation and cutoff of a transistor and drives a Foster-Seeley discriminator. The discriminator's sensitivity is approximately 4 millivolts rms per kHz of peak deviation. The emitter follower output stage is used for impedance isolation between the discriminator and the audio amplifier.

The audio frequency amplifier consists of an audio amplifier, a phase inverter, and a low impedance output amplifier. The audio frequency amplifier output feeds two 47-ohm isolation resistors, each one of which feeds an output connector. These resistors allow one output to be shorted to ground without reducing the other output voltage more than 3 db. One of the outputs is used as the input for the IU Command Decoder. The audio frequency amplifier output also feeds a bandpass filter in the high-level TM circuits. This filter's output is fed to an AGC-controlled amplifier and then through an amplifier to the high-level telemetry detector circuit. The telemetry voltage thus obtained will provide a useful measure of rf input signal strength.

Characteristics of the MCR-503B Command Receiver are given in Table 6.2-1.

6.2.5 COMMAND DECODER

The Command Decoder is the interface unit between the Command Receiver and the LVDA. The Command Receiver demodulates the rf carrier and presents the PSK signals (Figure 6.2-3) to the Command Decoder. The Command Decoder is common to both the Saturn IB and the Saturn V Vehicles. The physical and electrical characteristics of the Command Decoder are given in Table 6.2-2.

Data transmission is made through a 32-bit word which is preceded by three vehicle address bits ("X"-bits). Each data and address bit is composed of 5 sub-bits. The 175 sub-bit message must be decoded into the original message configuration of 35 bits before the data can be transferred into the LVDA for LVDC acceptance.

The functions of the Command Decoder are as follows:

- Demodulate the PSK baseband subcarriers.
- Recover the original 175 sub-bits.

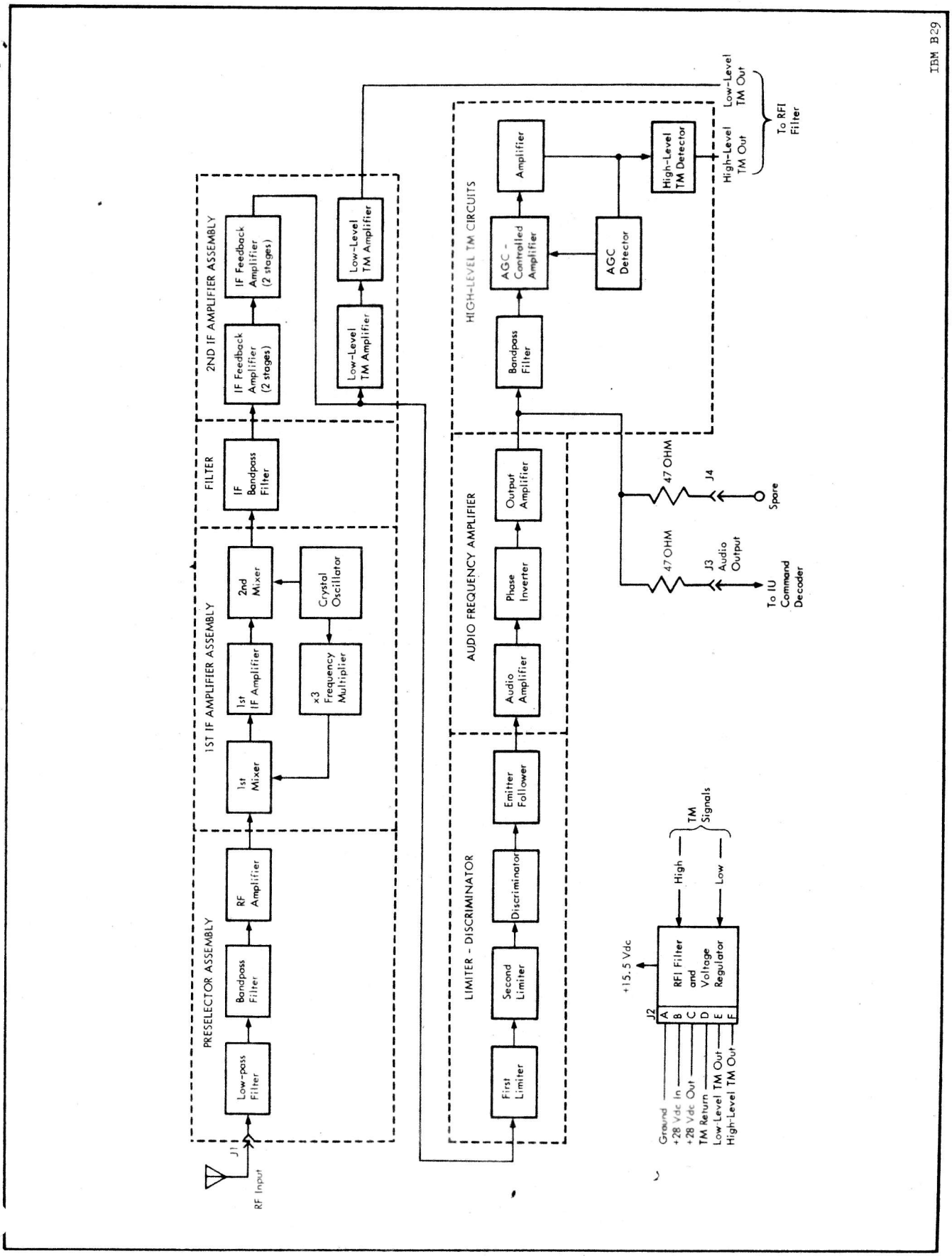


Figure 6.2-6. Command Receiver Block Diagram

- Compare each 5 sub-bit group against three prewired bit codes to recover the 35-bit command word.
- Check that all 35 bits are received.
- Check that each bit is received within the 5-millisecond bit period.
- Check that the 3-bit vehicle address and the 14-bit decoder address are correct.
- Inhibit any further decoding if any of the checks are invalid.
- Present the 18 information bits to the LVDA in parallel form.
- Present an address verification signal to PCM telemetry.
- Receive an LVDC reset signal from the LVDA and present this signal to PCM telemetry.

A detailed description of the Command Decoder logic and operation is given in the following paragraphs. Figure 6.2-7 and 6.2-8 supplement the text. Figure 6.2-7 is a logic diagram of the circuitry discussed. An explanation of the logic symbols used is found with the figure. Figure 6.2-8 shows a typical wiring scheme of code plug J4.

LOGIC DESCRIPTION

PSK Detector. The PSK signals from the Command Receiver are first routed through 2 filters – a lowpass filter and a bandpass filter (not shown on Figure 6.2-7) – before being applied to the PSK sub-bit detector (PSK Detector). The PSK detector is shown in the upper left-hand portion of the figure. The purpose of the PSK detector is to separate the 1 kHz and 2 kHz signals, compare the phase of the 2 kHz signal with the 1 kHz reference signal once each millisecond, and generate a pulse on the "1" output circuit or the "0" output circuit, as the case may be.

The PSK detector amplifies and shapes the 1 kHz and 2 kHz signals from the filter to determine the phase of the 2 kHz signal with respect to the 1 kHz signal. The relative phase of the signals determines the sub-bit "1's" and "0's" as required. The PSK detector output is then applied to the appropriate (set or reset side) of a 5-bit shift register and is also used to step a 5-bit counter.

5-Bit Counter and Shift Register. The sub-bit "1's" and "0's" from the PSK detector are differentiated and written into the 5-bit shift register as required, and routed to code plug J4 (Figure 6.2.8). From the code plug, the appropriate sub-bit "1's" and "0's" are connected to their respective AND circuit comparators.

As each group of 5 sub-bits is written into the 5-bit shift register, they are counted by the 5-bit counter. When the 5-bit counter reaches a count of five, a positive pulse is produced and used to open gates AND8, AND9, and AND10 (through OR6) to provide a "1" code enable, "0" code enable, or an "X" bit count pulse when the correct sub-bit pattern is written into the 5-bit shift register.

Table 6.2-1. Command Receiver Characteristics

Frequency range	406 to 450 MHz
Frequency deviation	± 30 kHz (for 1 Vrms output)
Quieting	15 db at 10 microvolts
Maximum RF input	2.0 Vrms
Input VSWR	1.5:1 maximum
Tuning stability	± 30 kHz
Oscillator	Crystal controlled, single crystal
RF bandwidth (-3 db)	340 ± 30 kHz
RF bandwidth (-60 db)	1200 kHz
Type of output	Audio, two isolated outputs
Audio bandwidth (-3 db)	100 Hz to 80 kHz
Audio distortion	Less than 5 percent
Audio output level	1 Vrms into 75-ohm load (with two tones, ± 30 kHz deviation per tone)
Input voltage	+24 Vdc to +36 Vdc
Power	3.5 watts at 28 Vdc
Weight	1.4 kg (3.1 lbs)
Dimensions	
Height	11.1 cm (4.3 in.)
Width	13.4 cm (5.3 in.)
Depth	11.9 cm (4.7 in.)

Table 6.2-2. Command Decoder Characteristics

Primary Voltage	+28 (+10, -6) Vdc
Operating Current	80 ± 10 mA
Audio Input	1.9 (+0.35, -1.25) Vrms
Binary Output Functions	
"One"	28 (+0, -3) Vdc
"Zero"	0 ±0.5 Vdc
Data Output Impedance	Less than 1000 ohms
Weight	3.85 kg (8.5 pounds)
Outline dimensions	
Height	10.79 cm (4.24 in.)
Length	22.60 cm (8.91 in.)
Width	18.39 cm (7.41 in.)

The 5-bit register has 10 outputs (2 for each position) resulting in 32 (2^5) possible sub-bit patterns. Each of the 3 sub-bit comparators, "X", "0", and "1", (AND10, AND7, AND6) have 5 wires connected to the 5-bit shift register, via code plug J4, with 1 wire to each position. Hence, gate AND10 will have an output when the correct 5-bit code is written into the 5-bit shift register, thereby generating an "X" bit count pulse. The same is true for AND7 and AND6, thereby generating a "0" code or a "1" code, respectively. For example, the sub-bit code for a data "1" may be chosen as "11010", the sub-bit code for a data "0" may be chosen as the data "1's" complement, (00101), and the "X sub-bit code may be chosen as "11000".

During intevals when no messages are being transmitted, all sub-bit "1's" are transmitted. However, the comparators have no output since there is no code pattern; that is, all "1's". The first three data bits of a transmitted message are designated as "vehicle address" and are sub-bit coded as "X's". Since the message is bracketed by continuous sub-bit "1's", the "X" comparator (AND10) is initially enabled by the output from OR6, permitting an "X" comparison at any time the 5-bit shift register pattern is correct. The "X" bits are counted in a 3-bit counter referred to as the "X" counter. The "count of three" output of the 3-bit counter enables AND4 and AND5 after three "X" bits have been counted.

The input to the missing-bit clock (center of the figure) is the output from OR3. The composite signal is therefore the "X" bit count pulse, "1" code enable, or "0" code enable. During normal message decoding, the pulse spacing is 5 milliseconds (200 bits per second, bps). The missing-bit clock is essentially two monostable multivibrators which, if a proper message is being received, will provide a continuous output from OR5. This is accomplished by alternately triggering the 2 multivibrators (MVB's). The ON cycle of the MVB's (5.4 milliseconds) is adjusted to be slightly greater than the duration of each data bit (5.0 milliseconds). Thus, the OFF MVB is triggered ON, 400 microseconds before the ON MVB completes its cycle. Under normal operating conditions and with no bit missing, OR5 will always have at least 1 input.

The output from AND11 at the first "X" bit count pulse will reset the 5-bit counter and will pass through OR7 to reset the 3-bit counter. The 3-bit counter is also reset through OR7 by the pulse from OR5, when the absence of a bit is detected by the missing-bit clock, or when the computer reset pulse occurs at the completion of a data transfer to the LVDA.

32-Bit Shift Register. The 32 bits following the three "X" bits are coded "0's" or "1's" as required. Each time a count-of-five state is reached by the 5-bit counter, a comparison is made to determine if the bit is a "0" or a "1". These 32 bits are then written into a 32-bit shift register.

The decoder address is prewired and composed of 14 of the 32 bits of the shift register. These 14 bits must be true to have an output on the address verify bus. The diodes of the bus may be connected to the set or reset side of each shift register stage as prescribed by the decoder address desired.

The 18 data bits are buffered and sent to the LVDA for processing. For simplicity, the complete buffering and gating logic is not shown in the figure.

Shift Out and 32-Bit Counter. The input shift pulses to the 32-bit shift register are counted by a 32-bit counter. At a count of 32, an MVB is triggered, strobing gate AND12. At this time, the 32 data bits have been completely written into the 32-bit shift register. If the decoder address in the register is correct, gate AND12 is opened and the output pulse is used to:

- Set the output flip-flop to enable the output AND gates and reset the 3-bit counter
- Trigger two address verify MVB's.

LOGIC SYMBOLOGY

AND gate

AND gate with inhibiting input

OR circuit (buffer)

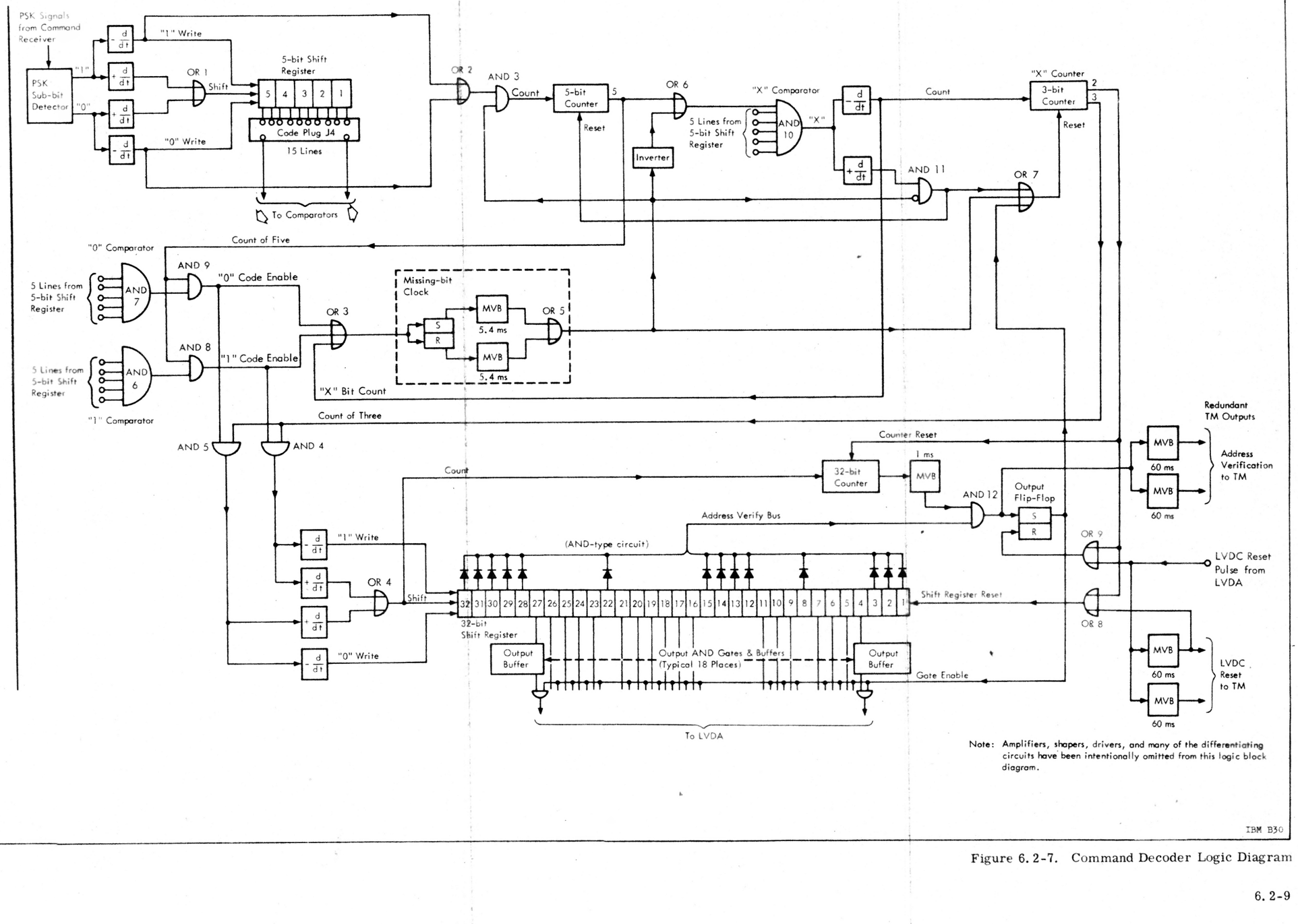
MVB (ms) — Monostable multivibrator. Time period of MVB is shown adjacent to symbol.

S / R — Bistable multivibrator (flip-flop). Reset (R) output is significant immediately after Reset input has occurred. The same is true for the Set (S) side.

$\frac{d}{dt}$ — Differentiating circuit which produces pulse at the leading and trailing edges of gate waveforms. A minus sign placed inside symbol indicates that only the trailing-edge pulse is significant. A plus sign indicates that the leading edge is significant.

Inverter — Logical inversion. Inverts from significant to inhibiting and vice-versa. The term "significant", as used herein, implies nothing about the polarity of a given waveform.

ms - Millisecond
MVB - Multivibrator
R - Reset
S - Set



Note: Amplifiers, shapers, drivers, and many of the differentiating circuits have been intentionally omitted from this logic block diagram.

IBM B30

Figure 6.2-7. Command Decoder Logic Diagram

The LVDC reset pulse, which occurs after LVDC acceptance of the command message, resets the output flip flop through OR9, thus disabling the output AND gates. The LVDC reset pulse also triggers two LVDC reset MVB's. An output from one of the MVB's is returned to OR8 to reset the 32-bit shift register.

Output Monostable Multivibrators. The address verify pulse from the address verify bus (via AND12) is routed to two redundant MVB's. The output pulse width of each MVB is set to 60 milliseconds. These output pulses are sent to the telemetry system to denote decoder address verification. As mentioned in the preceeding paragraph, the LVDC reset pulse from the LVDA is used to trigger another pair of redundant MVB's (60 milliseconds). These MVB's acknowledge receipt of the LVDC reset pulse. Although not shown, the outputs of these MVB's are buffered to meet the required input voltage levels of the IU telemetry system.

DETAILED OPERATION

The first "X" bit comparison in the command message generates a 1-millisecond pulse which is differentiated and passes through AND11 to reset the 5-bit counter and, through OR7, to reset the 3-bit counter. The trailing edge of the pulse also advances the 3-bit counter by one count and starts the missing-bit clock. When the missing-bit clock starts, the output of OR5 will: (1) open AND3, enabling the 5-bit counter, and (2) inhibit AND11, preventing the next "X" comparison from generating a reset pulse.

As the next 5 sub-bits are written into the 5-bit shift register, they are counted by the 5-bit counter. When the counter reaches a count of five, the output passes through OR6, thus enabling a second "X" comparison. A valid "X" comparison will generate a 200-microsecond pulse. This pulse will advance the 3-bit counter to the count-of-two state and will also keep the missing-bit clock running. The count-of-two output from the 3-bit counter will: (1) clear the 32-bit shift register through OR8 (the cleared state of this register is when there is a "0" stored in the "0" side of all stages), (2) send a reset pulse to the 32-bit counter, and (3) send a reset pulse to the output flip flop through OR9. After the third "X" bit has been recognized, the count-of-three output from the 3-bit counter will provide a direct-coupled signal to AND4 and AND5. As long as this signal is present, AND4 and AND5 are "open"; i.e., they will allow valid "0" and "1" bits to pass through.

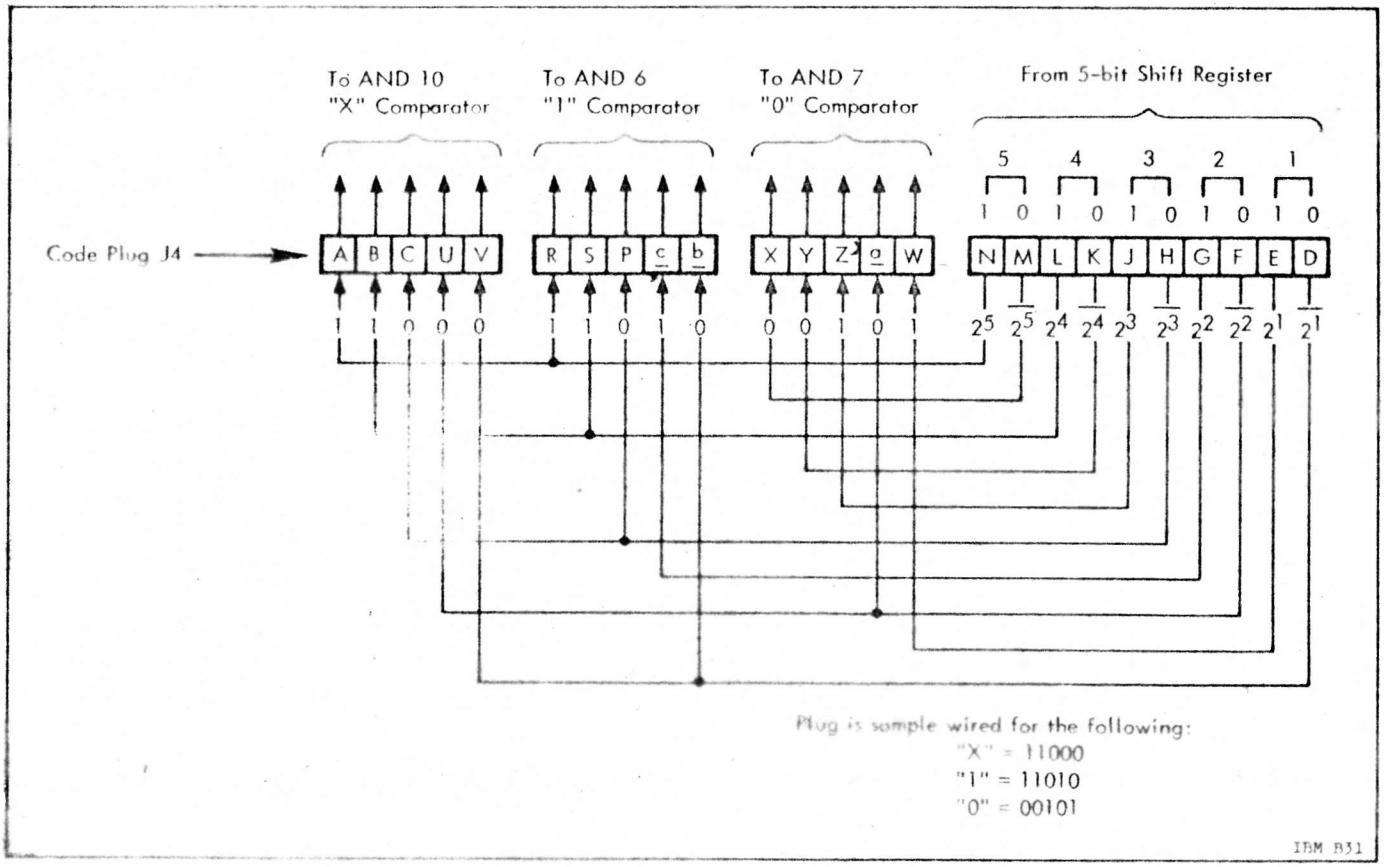


Figure 6.2-8. Sample Wiring of Code Plug J4

The next 32 bits will be sub-bit coded with "0's" and "1's" as received. Each time a count-of-five state is reached by the 5-bit counter, a comparison is made to determine if the bit is a "0" or a "1". A pulse will be produced at the output of OR3, thus keeping the missing-bit clock running. These 32 bits will also be shifted and written into the 32-bit shift register and counted by the 32-bit counter. Upon the count of 32, a 1-millisecond monostable MVB is triggered ON. This signal opens AND12 and allows an address comparison to be made. If the address is correct, a signal will pass through AND12 and trigger the output flip flop to its set state. In addition, two 60-millisecond monostable MVB's will be triggered ON by AND12 to provide an indication to the telemetry system that the address was valid. Redundant MVB's are used for reliability.

The set output of the output flip flop also resets the 3-bit counter (through OR7) and provides an enabling voltage to the 18 data-output AND gates. The binary information stored in the 18 data stages of the 32-bit shift register is thus transferred in parallel form to the LVDA. When the LVDC data processing routines accept these data bits, a reset pulse (acknowledging receipt) is sent through the LVDA to the Command Decoder. This pulse will pass through OR9 to reset the output flip flop (disabling the 18 output AND gates). The same pulse will also trigger two 60-millisecond monostable MVB's and thus clear the 32-bit shift register through OR8. The outputs of these 2 MVB's are sent to the telemetry system to indicate receipt of the LVDC reset pulse. If, for some reason, the LVDC reset pulse does not arrive prior to the beginning of the next message, the second "X" bit of vehicle address will provide an output from the 3-bit counter to reset the Command Decoder circuits.

6.2.6 DATA VERIFICATION

The application of the IU command system and the information transmitted through the system require a high probability that a correct command message will be received in the vehicle. This high probability is obtained by the use of several different techniques throughout the command system.

First, the Manned Space Flight Network is designed to provide a high degree of data transmission accuracy from the originating station in Houston, Texas to the down-range DCS, which actually transmits the message to the vehicle. Secondly, to transpose a "1" bit to a "0" bit or vice-versa, every one of the 5 sub-bits must be transposed to its complement, and this must be done in multiples of five in synchronism with the bit rate (200 bps), otherwise, the message will be rejected. Thirdly, 17 bits of each 35-bit transmission must be correct (there is no possibility of an undetected error here) before the 18 information bits are presented to the LVDA. Last of all, a verification loop utilizing telemetry as a down-link is employed.

The verification loop works as follows. If the 14-bit address is correct, an address verification pulse is sent to telemetry. This pulse is decommutated in real time at the ground station and presented to the message acceptance pulse circuitry (Figure 6.2-9). A second pulse is also derived in the vehicle and sent to telemetry. This is the LVDC reset pulse which signifies that the LVDC has received, verified, and processed the 18 information bits. This pulse is also decommutated in real time and routed to the message acceptance pulse circuitry. The address verification pulse triggers a 200-millisecond monostable MVB to the ON state. The LVDC reset pulse will occur a short time thereafter and trigger a 10-millisecond monostable MVB to the ON state. If the LVDC reset pulse does not appear during the ON time of the address verification pulse MVB, the pulse will not appear at all for a given transmission. The two MVB outputs are fed to an AND gate, which will have an output only when both MVB's are ON.

The 10-millisecond pulse thus produced is called the message acceptance pulse and is fed to the DCS. The DCS uses this message acceptance pulse as a "next-message-transmit" pulse. Upon receipt of this pulse, the DCS will transmit the next message (if any). If the message acceptance pulse does not appear within a certain length of time (approximately 400 milliseconds from start of message), the DCS will then retransmit the message.

An LVDC verification of a received command word is accomplished by programming techniques and the message format itself. In the command word format transmitted from the ground, one-half of all data bits are transmitted as required in "true" form and the other half in complementary form. This is called duplex coding. The LVDC will reject a command unless the complement bits check out to be the

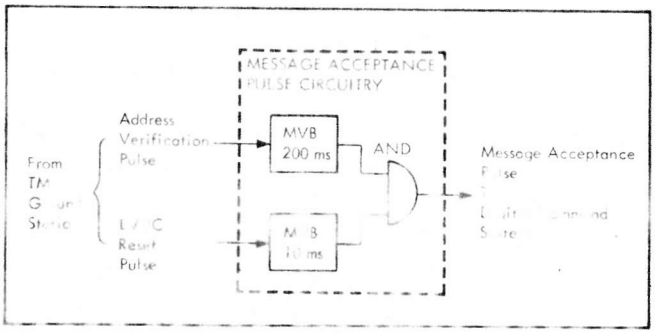


Figure 6.2-9. Message Acceptance Pulse Circuitry Block Diagram

inverse of the true bits. Such a procedure provides a greater probability of receiving the same message as was transmitted.

SECTION 6.3

SECURE RANGE SAFETY COMMAND SYSTEM

6.3.1 OVERALL SYSTEM

The secure range safety command system provides a high degree of protection against intentional interrogation by unfriendly intruders and against unintentional interrogation (false alarms) by noise. The security against intentional interrogation is measured by the fraction of the total code combinations that an intelligent unfriendly interrogator, having unlimited technical resources, would be able to transmit during equipment access time. It is assumed that all system parameters are known to him except the code-of-the mission. The security against unintentional or randomly generated false alarms is, as it should be, much greater than against intentional, intelligent interrogation. All hardware is unclassified except the actual flight code plugs.

A simplified block diagram of the secure range safety command system is illustrated in Figure 6.3-1. Each address character is chosen by the code plug. Two identical code plugs, one in the ground encoder and the other in the flight decoder, are used. This removable, inexpensive, easily stored code plug minimizes the actual operational difficulties of handling the security aspects of the system, thus eliminating the necessity of classifying the system hardware (decoder and encoder).

6.3.2 MESSAGE FORMAT

The message transmitted to the vehicle consists of 2 words; an address word and a function or command word. The address word consists of 9 characters of a high-alphabet system, and the function word consists of 2 characters; thus the total message comprises 11 characters.

Each character consists of two simultaneous symbols, which are audio-frequency tones between 7.35 kHz and 13.65 kHz. Each character can be tone coded by choosing from a symbol alphabet of 7 tones.

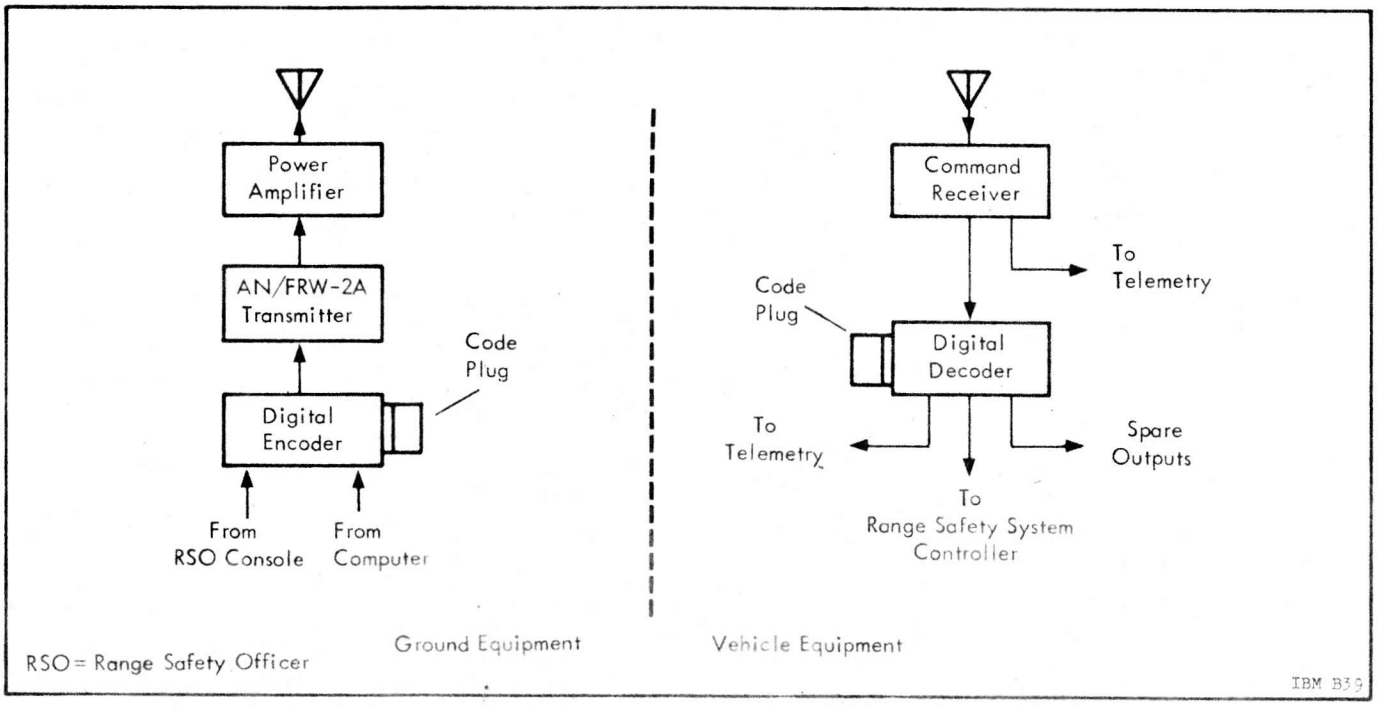


Figure 6.3-1 Secure Range Safety Command System

Since 2 tones are used simultaneously, the character alphabet is established at 21 possibilities or choices (no choice is repeated within a given word). Thus the encoding scheme is logically called high-alphabet.

The security of the message is realized mainly from the fact that only 9 out of 21 possibilities are used per address, and that these 9 address characters are position coded. The limited time of access to the equipment is the final factor in the security, for any code can be broken if access time is unlimited.

The function word consists of 2 characters. Since there are 21 character-coding arrangements available for the first function character and 20 for the second, 420 character/position codes are available for the function word. Only 5 functions are required of the system. To provide the maximum langauge difference between any two of these functions, 5 codes were chosen as commands in a spacing scheme which provides maximum security against command translations. These commands and their codes are listed in Table 6.3-1.

Each character period, including "dead time", is approximately 8.6 milliseconds in duration, except the eleventh, which is three times as long.

Each character of the 9 character address word is unique within a given address, and therefore the new system can operate without the necessity of a transmitted clock or reference synchronizing information. The symbols are, however, synchronous with the character interval period (and with each other) and are spaced and phased to minimize intersymbol interference, which could create unwanted characters.

Table 6.3-1 Coding Scheme for Function Characters

Command	10th Character Tones	11th Character Tones
1. Destruct (propellant dispersion)	1 and 2	1 and 3
2. Arm/fuel cutoff (charging of the EBW firing unit and thrust termination.)	2 and 3	2 and 4
3. MSCO/ASCO (Saturn spare No. 1)	4 and 5	4 and 6
4. Spare (No. 2)	3 and 4	3 and 5
5. Safe (command system switched OFF)	5 and 6	5 and 7

Note: Commands are listed in priority order.

The main RF carrier (450 MHz) is frequency modulated by a subcarrier system which in turn employs a multiple frequency shift technique. The term frequency shift keying is also used to describe the technique. The portion of the baseband occupied by the subcarrier system is approximately the same as that now reserved and used for range safety purposes (see Figure 6.5-2). The nominal tone frequencies, however, are not the same as the inter-range instrumentation group tone channel frequencies. The tone-frequency spacing is by design an integral multiple of the character repetition rate. This makes possible a simple phase-coherent tone keying scheme.

6.3.3 GROUND EQUIPMENT

A block diagram of the ground system is illustrated in Figure 6.3-2.

When the range safety officer decides to initiate a command from his console, he actuates a hooded toggle switch. The output of the encoder is then routed in parallel form to a tone remoting transmitter which processes the message for transmission over the 8 km distance to the transmitter site. A tone remoting receiver at the transmitter site demodulates the message and feeds it to a modulator that converts the parallel information to the high-alphabet 11-character format. The 11 dual-tone bursts are then fed to the AN/FRW-2A Transmitter System and to the vehicle. For reliability, a completely redundant backup system is provided, with a continuously monitoring error detector that provides automatic transfer to the backup system in case of a failure in the primary chain (this error detection and switching circuitry is not shown in the diagram).

The range safety equipment incorporates a priority-interrupt scheme that will interrupt any command being transmitted and transmit any higher-priority command selected by the range safety officer or originated by the computer. After completion of the transmission of the higher-priority command, the transmission of the interrupted command will resume.

The equipment at the downrange sites is illustrated in the block diagram of Figure 6.3-3. All downrange sites are connected by cable, and when the range safety officer presses a command switch on his console, the command pulse will be transmitted over the cable via the supervisory control system

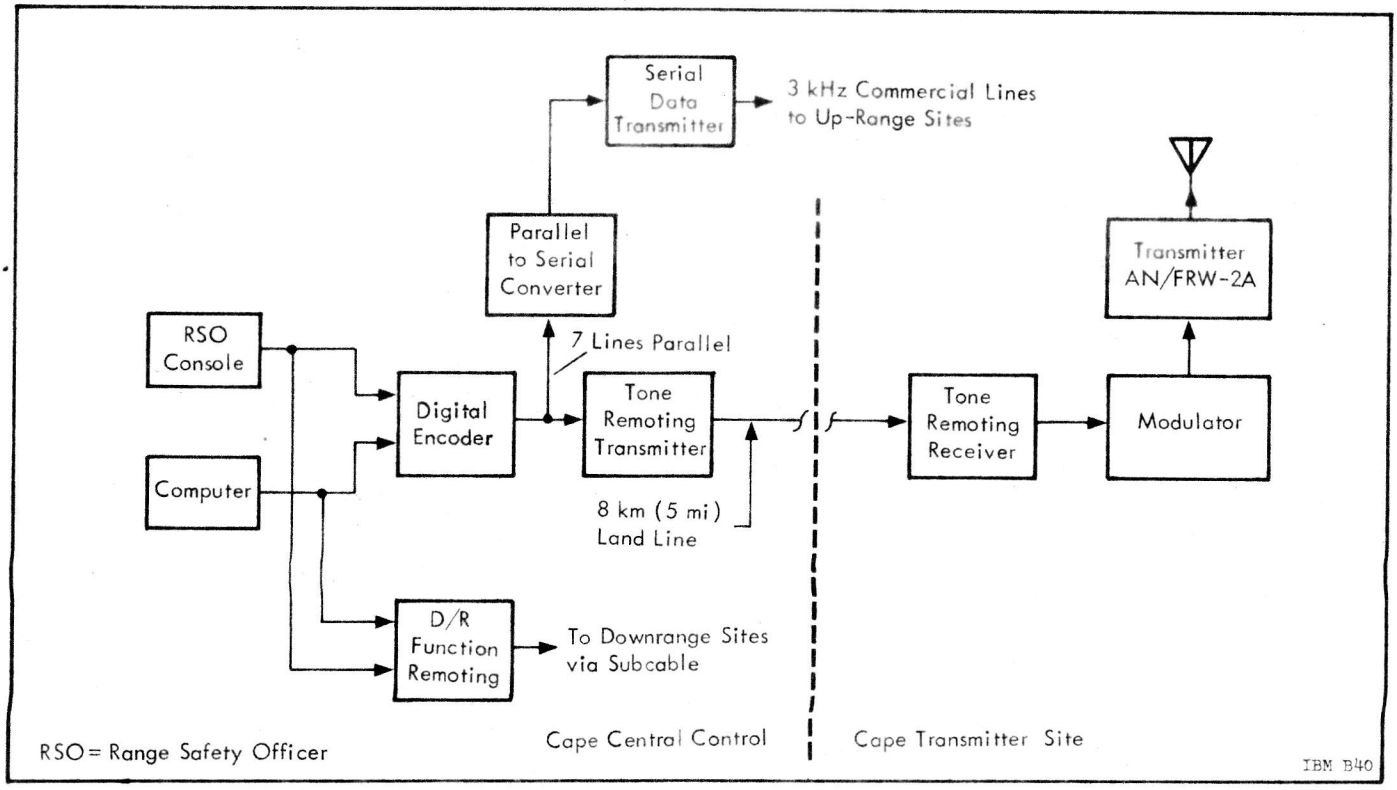


Figure 6.3-2 Range Safety Ground System

(this system will be replaced by a digital remoting system in the near future). All sites will receive the command, and the transmitter on the air at the moment the command is received transmits the message to the vehicle (to keep the onboard receiver captured, one transmitter is always radiating).

When the vehicle must be interrogated from an uprange site, the signal processing and routing is slightly different. As the parallel data leave the encoder at the cape central control, they are changed to serial form by a parallel-to-serial converter and then applied to a serial data remoting transmitter. After being checked for errors, the serial message will be received at the proper uprange site, converted to parallel form, and fed to the modulator. The modulator will convert the binary-coded message to the high-alphabet 11-character format. This message is then transmitted to the vehicle.

6.3.4 VEHICLE-BORNE EQUIPMENT

ANTENNAS

The type and number of antennas used will be such that their radiation pattern meets the requirements of range safety at the Eastern Test Range.

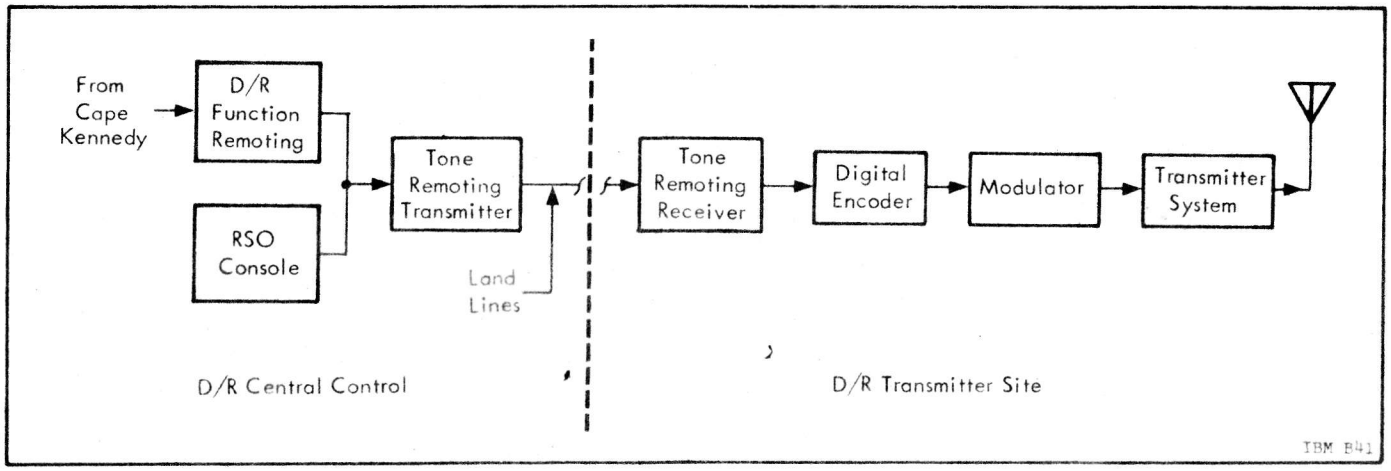


Figure 6.3-3 Downrange Station

RECEIVER

The command signal from the ground station is received in the vehicle with the MCR-503 Receiver. The same type of receiver is used also in the Instrument Unit command system and is described in Section 6. 2.

DECODER

A logic diagram of the vehicle-borne decoder is illustrated in Figure 6. 3-5. The front end consists of the filter driver, optimum decision circuitry, seven tone filters, and seven threshold detectors. The optimum decision circuitry will be discussed in more detail later, but operationally, the circuit can be considered as a hybrid, fast-acting AGC circuit. The purpose of each filter is to detect a particular tone, and the purpose of the threshold detectors is to establish the decision level and to amplitude standardize the output of each filter into a well-shaped pulse suitable for use in the circuitry which follows.

- The AND matrix consists of 21 AND gates and interconnections to the input of the code plug. The purpose of the matrix is to form the main alphabet of characters from the sub-alphabet of symbols (tones).

- The code plug consists of a multi-pin plug wired in the chosen code-of-the-mission configuration. The code plug can be wired in a number of unique ways. The purpose of the code plug is to unscramble the code and apply the 9 address character outputs to the sequence register. A second purpose of the plug is to present the 12 unused characters to OR 1.

- The sequence register or address memory consists of: (1) eight electronic switches (SW1 through SW 8), (2) one delay element consisting of a monostable multivibrator (DELAY MVB 1) and a trailing-edge differentiator, and (3) eight AND gates with inhibiting inputs (AND 1 through AND 8). In general, the purpose of the sequence register is to provide a pulsed signal to the input of AND 9 if each of the 9 characters of the address word is received in the proper sequence. A second function of the register is to provide a pulsed signal (up to eight) to the input of OR 1 if one or more characters are received out of sequence. The register will not provide a signal to the input of OR 1 if a character is repeated, which is desirable since radar blanking could cause a friendly character to be interrupted. The purpose of the eight passive time-delay elements (τ) in the register is to prevent an unfriendly intruder from gaining any advantage by transmitting more than 2 tones simultaneously. If 3 tones are transmitted, 3 characters will be formed. Because of the short time delay introduced by (τ), 2 of the 3 characters will be recognized as being out of sequence, even if they have the correct tone coding.

- The false-character action circuit consists of OR 1, OR 3, CLEAR MVB, FF 9, and AND 9. The purpose of this circuit is to provide a pulse whenever, (1) one of the unused characters is received, or (2) a character is received out of sequence. The pulse appears at the output of OR 1 and is routed to 3 places. First, it triggers FF 9 to its set state, which inhibits AND 9 so that the ENABLE MVB cannot be turned ON for the duration of the message interval, regardless of what occurs elsewhere in the decoder. Second, it passes through OR3 and clears (resets) the sequence register. A third action also to be initiated, provided that the character corresponding to point A has not yet occurred, is the triggering of the interval timer (a monostable multivibrator).

- The interval timing circuit consists of OR 2, the interval timer multivibrator, and a differentiating circuit which produces a pulse at the end of the timed interval. This pulse resets all decoder circuitry to the proper condition for receiving another message. Note that the presence of any of the 21 possible characters will initiate the timer. The purpose of OR 2 is to allow either the first character (point A) or any of the other 20 characters (the output of OR 1) to initiate the timer. The function of OR 6 and AND 16 is to establish a fixed recovery time for the interval timer MVB.

- The enabling circuit consists of DELAY MVB 2, the ENABLE MVB, and the power switch. The purpose of this circuit is to

prevent the function relays from being activated until after the address has been verified and the 11th character has arrived. Only when the 9 address characters have been sent in accordance with the chosen code, will a pulse appear at the input of AND 9, find it uninhibited, and trigger DELAY MVB 2. When this multivibrator completes its cycle, the -d/dt circuit triggers the ENABLE MVB ON for the function interval. The "ON" state of the ENABLE MVB closes the power switch, thus providing power to the function relays and associated logic circuitry.

- The decoding inhibit circuit consists of OR 4, OR 5, and AND 15. In general, the purpose of this circuit is to prevent decoding during the "clear" interval of the sequence register. The circuit does not function during the reception of a friendly message and therefore will not be discussed further.

- The function relays and logic circuitry represent the remainder of the decoder. The purpose of this circuitry is to allow the proper command transmission to close the appropriate relay(s), which supplies 28-volt power to the desired output functions.

- Signal tracing a friendly message. The code jack (Figure 6.3-5) has 21 inputs and 9 address outputs. For purposes of analysis, assume that the code plug is wired as shown in Figure 6.3-4 (top).

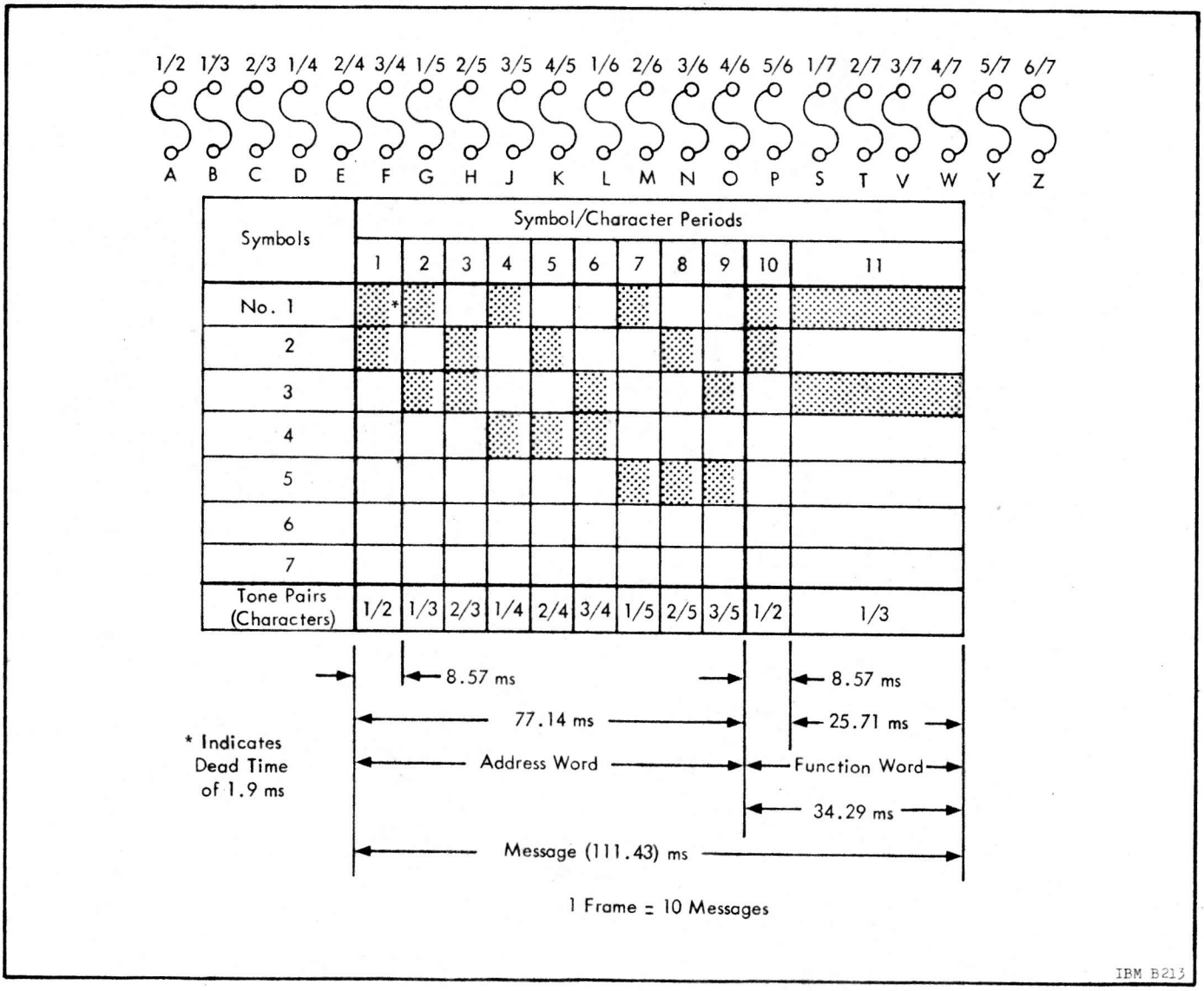


Figure 6.3-4 Code Plug Wiring

Based on such a code-plug wiring and on the message format previously mentioned, the total transmitted message will appear as shown in Figure 6.3-4 (bottom) if a command is to be effected. (The command is assumed to be destruct.)

The demodulated composite audio signal corresponding to the chosen tone pairs is fed from the receiver to the seven tone filters in the decoder. The filter outputs are matrixed to the 21 AND gates, thus providing the 21 required combinations. The outputs of the 21 AND gates are wired to a connector that feeds the input of the removable code plug. Assuming the code-plug wiring shown in Figure 6.3-4, the first tone pair (1 and 2) will cause a pulsed signal to appear on the output side of the code plug at point A. The signal at point A is distributed to 2 points: (1) it turns ON[1] the first electronic switch (SW 1) in the sequence register, which in turn supplies a voltage to the inhibiting input of AND 1; and (2) it passes through OR 2 and AND 16 and turns ON the interval timer. Approximately 8.5 milliseconds after the start of the first character, the second character arrives. Tone pair 1 and 3 corresponds to point B, and a pulsed signal at this point is distributed to 2 places: (1) it is applied as a signal input to AND 1, but cannot pass through because of the presence of the inhibiting voltage from SW 1; and (2) it turns ON SW 2. In addition, the output of SW 2 supplies a voltage to the inhibiting input of AND 2.

The third through the eighth characters (C through H) create results analogous to those of A and B. When the ninth-character pulse arrives (point J), it triggers DELAY MVB 1 to its "ON" state. When the multivibrator completes its cycle, the -d/dt circuit applies a pulse to AND 9. Since the interval timer is in its "ON" state and FF 9 is in the "reset" state, AND 9 will not be inhibited. Thus this pulsed signal will be allowed to pass through and trigger DELAY MVB 2 to its "ON" state. Eight and five tenths milliseconds later, the ENABLE MVB will be triggered to its "ON" state. Note that at no time during the address word is there an output from OR 1. This is because the address is the correct address and an output from OR1 will occur only if the address is not correct. After the ninth-character pulse turns ON the ENABLE MVB, the voltage thus obtained is (1) used to turn ON the power switch, which in turn supplies 28-volt power to the relay armatures, and (2) used as the supply voltage input to SW 10 and SW 11. Since we have assumed a destruct command, the tenth-character pulse will be formed by tone pair 1 and 2. This pulse will turn ON SW 10. The output of SW 10 is applied as a control voltage input to AND 10. Note that even though the time period of the tenth character is over, neither of the 2 relays is as yet energized. When the eleventh-character pulse arrives, it passes through AND 10 and is used to turn ON SW 11, thus energizing both relays in the destruct channel. Since both relays are now closed, 28 volts will be applied to the appropriate pin of the output plug and routed out of the decoder to the range safety system controller, which then takes over and initiates the destruct action and any preliminary critical functions (such as payload jettison, if applicable). As soon as the ENABLE MVB completes its cycle, the power switch will turn OFF, thus turning OFF SW 10 and SW 11. A short time later, the interval timer will complete its cycle, and the -d/dt circuits will reset all decoder circuitry to the proper state.

Much attention has been given to preventing execution of a catastrophic command should one component (transistor, relay, etc.) fail during flight. In many cases of component failure, the decoder design will still allow reliable interrogation.

The purpose of the DELAY MVB 2 is to delay the triggering of the ENABLE MVB for 8.5 milliseconds. This is necessary if complete freedom of choice for the ninth-character coding is to be maintained, for observe what would happen if the ninth, tenth, and eleventh characters were coded as follows (assuming that DELAY MVB 2 was not present):

9th	10th	11th
5 and 6	1 and 2	1 and 3

Destruct command

Since the ninth character corresponds to the first function-character of the safe command, and since the ENABLE MVB would be turned ON upon recognition of the ninth character, SW 14 would turn ON. This would degrade reliability and increase the probability of a command translation, since the intended command is destruct. Delaying the turn-ON of the ENABLE MVB until the time period of the ninth character is over, solves the problem without restricting the choice of the ninth character coding to one of the codes not used for a tenth character.

[1] Each electronic switch in the sequence register assumes the OFF state when B+ is removed. Therefore, when the decoder is first turned ON, all switches are OFF.

CLOSED-LOOP CHECKOUT

Until such time that a full security requirement is placed on flights of the Saturn Vehicle, the code-of-the-mission will be openly transmitted during the prelaunch countdown. This will be done to facilitate the pad checkout procedures.

If it is ever necessary to utilize the full security capabilities of the system, then a closed-loop prelaunch checkout procedure will be used in lieu of the open-loop transmission. In anticipation of such a requirement, a closed-loop procedure is being developed which will be compatible with the range procedure.

The characteristics of the Command Decoder are given in Table 6.3-2.

Table 6.3-2 Characteristics of the Command Decoder

Number of inputs	Two (isolated): receiver and hardwire
Type of input	Audio (75 ohms)
Audio input level	1 V rms per tone (1.4 V rms per tone pair)
Input dynamic range	At least 12 db (0.56 V rms to 2.2 V rms)
Sensitivity	Approximately 0.2 V rms at room temperature
Number of command outputs	Five
Type of output	Switched +28 Vdc rated 2 amperes (resistive) each output
Duration of output	Approximately 25 milliseconds
Type of code plug	Quick disconnect (Deutch)
Weight	3.85 kg (8.5 lbs)
Power	
Quiescent	2.5 watts (no audio input)
Operating	3 watts
Input voltage	+24 to +38 Vdc
Outline Dimensions	
Height	10.79 cm (4.24 in.)
Width	22.6 cm (8.9 in.)
Depth	18.39 cm (7.24 in.)

SECTION 6.4
SATURN COMMAND AND COMMUNICATION SYSTEM

6.4.1 GENERAL INTRODUCTION

The Command and Communication System (CCS) uses a phase-coherent, receiver-transmitter scheme and is capable of establishing a communication link between Unified S-Band (USB) ground stations and the IU of the Saturn V Vehicle. Specifically, the CCS can:

- Receive and demodulate command up-data for the LVDC/LVDA in the IU
- Transmit Pulse Code Modulated (PCM) mission control measurements to the ground stations for processing
- Retransmit a Pseudo-Random Noise (PRN) range code that is received from the USB ground stations.

The CCS is located in the IU and consists of a transponder, a power amplifier, and an antenna system.

The operational requirements of the CCS include command up-data and telemetry down-link. Ranging is desirable but not mandatory, and command up-data is not required on a continuous basis throughout the entire lunar mission. The requirement for command up-data varies according to the particular phase of the flight profile. During the launch phase, there is no requirement for up-data since the launch is of such short duration that there is not sufficient time to analyze and make an action decision on unpredictable situations. The LVDC is triple-redundant and is programmed for all predictable situations.

After insertion into an earth parking orbit, command up-data will be required on a non-continuous basis. If all systems are functioning properly, the LVDC will be corrected (if necessary) and updated with the data required to accomplish translunar injection. At a distance of approximately 20,000 kilometers (10,800 nautical miles), the S-IVB/IU separates from the Spacecraft and is no longer needed for mission success.

During the launch and earth parking orbit phases, VHF transmitters are the prime telemetry source. However, at distances of approximately 10,000 kilometers (5400 nautical miles) and greater, VHF transmission is inadequate, primarily due to vehicle and ground antenna gains. After injection, the CCS Transponder becomes the prime telemetry link.

Under normal circumstances, there is no mandatory tracking requirement for the CCS. During launch, tracking is provided by C-band beacons and surface radar, with the Spacecraft transponders providing tracking aid during other phases. However, the CCS Transponder will have tracking PRN receive-transmit capability and may be used as a backup to the Command and Service Module (CSM) Transponder in case of failure or desire for a cross-check.

Since the CCS and LM Transponders have identical frequencies, a possibility of interference exists if the two are operated simultaneously at close range. The CCS Transponder has the capacity to shut down its transmitter section by an external command. This shutdown command will be initiated before the LM Transponder is used. The CCS Transponder receiver section will remain operative so that commands may be received at all times. It is desirable that the CCS Transponder transmitter section be turned back ON after sufficient separation from the LM Transponder. This will allow receive-transmit ranging to better define the trajectory of the S-IVB/IU after separation from the spacecraft.

6.4.2 CCS COMPONENTS

CCS TRANSPONDER

The CCS Transponder is an S-band, continuous-wave, phase-coherent transponder that is used as the communications link between the ground stations and the Saturn V IU.

In addition to the receive-transmit conventional transponder function, the CCS Transponder incorporates a demodulating function for the up-data (received) signal and a modulating function for the down-link (transmitted) signal. Also, both input and output telemetry functions are available in the CCS Transponder. The overall purpose of the CCS Transponder can be described briefly as follows:

- Receive and demodulate command data for updating the LVDC.
- Transmit mission control telemetry measurements from the Saturn V Vehicle.
- Coherently retransmit a PRN ranging code that is received from the ground.

The CCS Transponder consists of a double-conversion, phase-coherent receiver and a continuous wave transmitter in which the received and transmitted signals are integrally related in both frequency and phase. Figure 6.4-1 is a block diagram of the CCS Transponder.

The S-band signals received by the IU CCS antenna system are coupled to a preselector in the CCS Transponder. The preselector eliminates unwanted frequencies and passes the desired frequencies to the first mixer.

The first mixer also receives a signal frequency from a x108 frequency multiplication circuit. The two signals are combined in the first mixer to produce the usual superheterodyne frequencies at its output.

Following the first mixer is a preamplifier stage that includes a bandpass filter, which passes only the difference-frequency component of the mixer output. The gain of this circuit is controlled by an AGC voltage from an AGC loop circuit.

The output of the preamplifier is applied to the first IF amplifier. This amplifier provides gain to the first IF signal (with gain control again being a function of AGC voltage) before application to a second mixer.

The second mixer receives a signal frequency from a x3 frequency multiplication circuit. The second IF output of the second mixer is applied to a bandpass filter and to a demodulation and detector circuit.

The second IF output signal from the bandpass filter is applied simultaneously to a linear second IF amplifier and to a limited second IF amplifier. The second IF signal that is amplified by the linear amplifier is applied to the AGC loop circuit. The second IF signal that is amplified by the limited amplifier is applied to a phase-lock loop circuit and Voltage Controlled Oscillator (VCO).

The second IF signal from the second mixer is applied to the demodulation and detector circuit and is phase demodulated, leaving a PRN rangin code and a

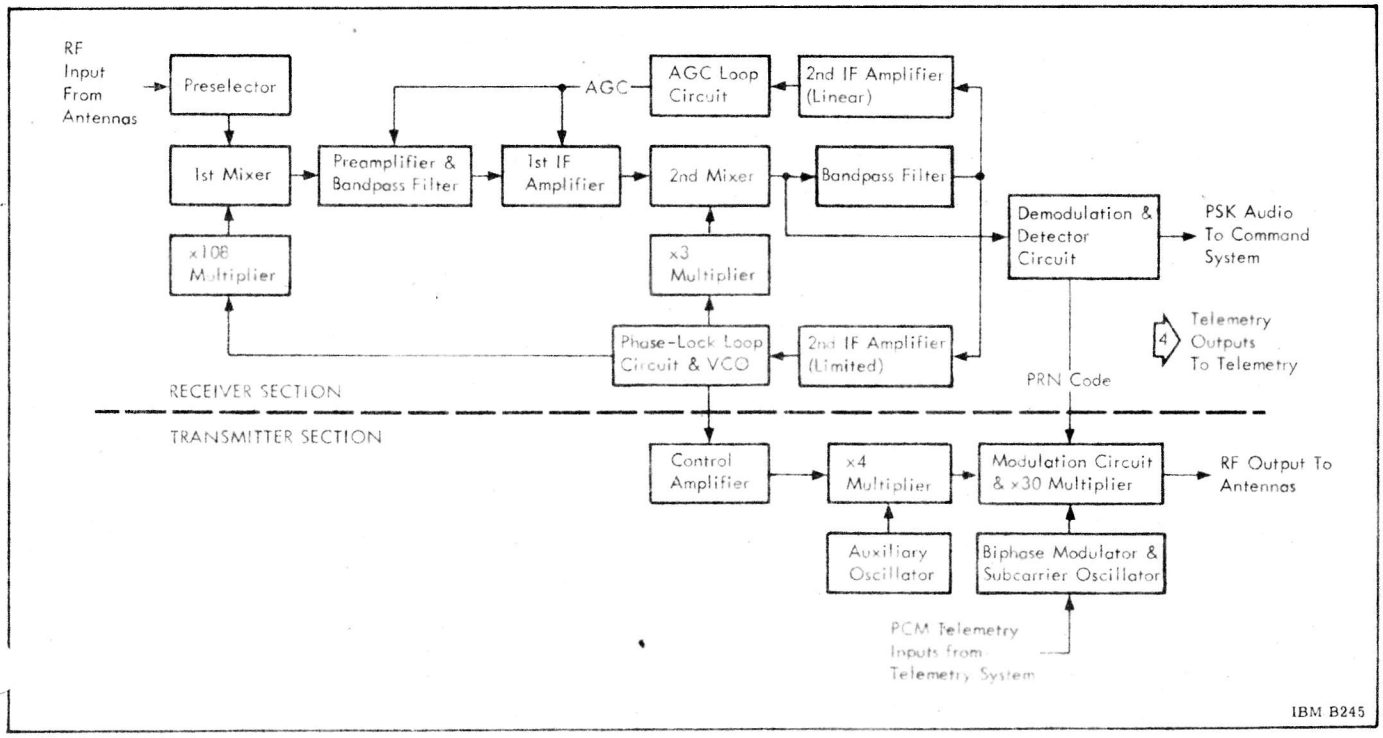


Figure 6.4-1. CCS Transponder Block Diagram

frequency-modulated 70 kHz subcarrier. The PRN ranging code is sent to the transmitter section for modulating the down-link signal. The subcarrier is demodulated by the detector circuit into a composite audio signal that contains PSK digital information. This signal is then applied to the IU command system Command Decoder for decoding and ultimate use by the LVDC. The demodulator circuit is disabled if the receiver is not in phase-lock.

When the receiver is in phase-lock with the received signal, the VCO in the phase-lock loop provides a signal to a control amplifier in the transmitter section. If the receiver is not in phase-lock, this signal is disabled by the control amplifier before reaching a x4 frequency multiplier. In this case, an auxiliary oscillator is enabled to provide a signal to the x4 frequency multiplier at the same frequency. In this manner, a carrier signal is applied to the x4 frequency multiplier if the receiver is either in or out of phase-lock.

The x4 frequency multiplier provides an output for a modulation circuit and x30 multiplier that is the fourth harmonic of the VCO or auxiliary oscillator signal frequency. This carrier signal is applied to the modulation circuit, where it is phase modulated by a 1.024 MHz biphase-modulated subcarrier that is generated in a biphase modulator and subcarrier oscillator circuit. Also, if the receiver is in phase-lock, the PRN ranging code is similarly modulated on the carrier. The phase-modulated carrier is then given x30 frequency multiplication, amplified, and filtered before leaving the CCS Transponder as the down-link signal. The output signal from the transmitter, however, may be disabled by a command input signal, and the CCS Transponder will then function only as a receiver.

The CCS Transponder also provides four isolated telemetry outputs for the IU telemetry system. These outputs are used to monitor the CCS Transponderoperation from the ground.

Table 6.4-1 lists the main characteristics of the CCS Transponder.

CCS POWER AMPLIFIER

The CCS Power Amplifier amplifies a modulated S-band signal for transmission from the Saturn Vehicle to ground stations. This rf signal is generated within the CCS Transponder.

Operation of the CCS Power Amplifier is controlled by commands received from ground stations via the IU command system. Standby (warmup) and operational modes are provided for in the amplifier design. The CCS Power Amplifier is divided into two functional sections: an rf channel and a power supply. Figure 6.4-2 is a block diagram of the CCS Power Amplifier.

The rf channel is shown on the top half of Figure 6.4-2. The rf input is applied to an attenuator, which limits the input power to a Traveling-Wave Tube (TWT). The TWT, used for its broad-band power amplification characteristics, amplifies the rf signal and applies the amplified signal to a harmonic suppression filter. The output of the filter is then applied to an rf isolator. This circuit prevents damage to the TWT that may be caused by possible mismatches present at the output of the CCS Power Amplifier. The output signal is then filtered in a bandpass filter and applied to the rf output for connection to the CCS antenna system.

The power supply is shown in the lower half of Figure 6.4-2. An RFI assembly filters the incoming 28 Vdc power and applies it to a voltage regulator. In addition, the RFI assembly filters telemetry status signals provided by the CCS Power Amplifier and a high voltage control signal that is received as a command signal from a ground station. Status signals from the CCS Power Amplifier are transmitted to the ground via the IU telemetry system to allow monitoring of principal performance parameters.

Table 6.4-1. CCS Transponder Characteristics

Received Frequency	2101.8 MHz
Transmitted Frequency	2282.5 MHz
Offset Ratio	221/240
Receiver RF Bandwidth	12 MHz
Transmitter RF Bandwidth	25 MHz
Dynamic Range	100 db
Tracking Range	± 180 kHz
Transmitter Power	250 mW
Input Power	35 Watts
Input Voltage	28 ± 4 Vdc
Weight	9.75 kg (21.5 lb)
Dimensions	13.7 x 24.9 x 37.8 cm (5.4 x 9.8 x 14.9 in.)

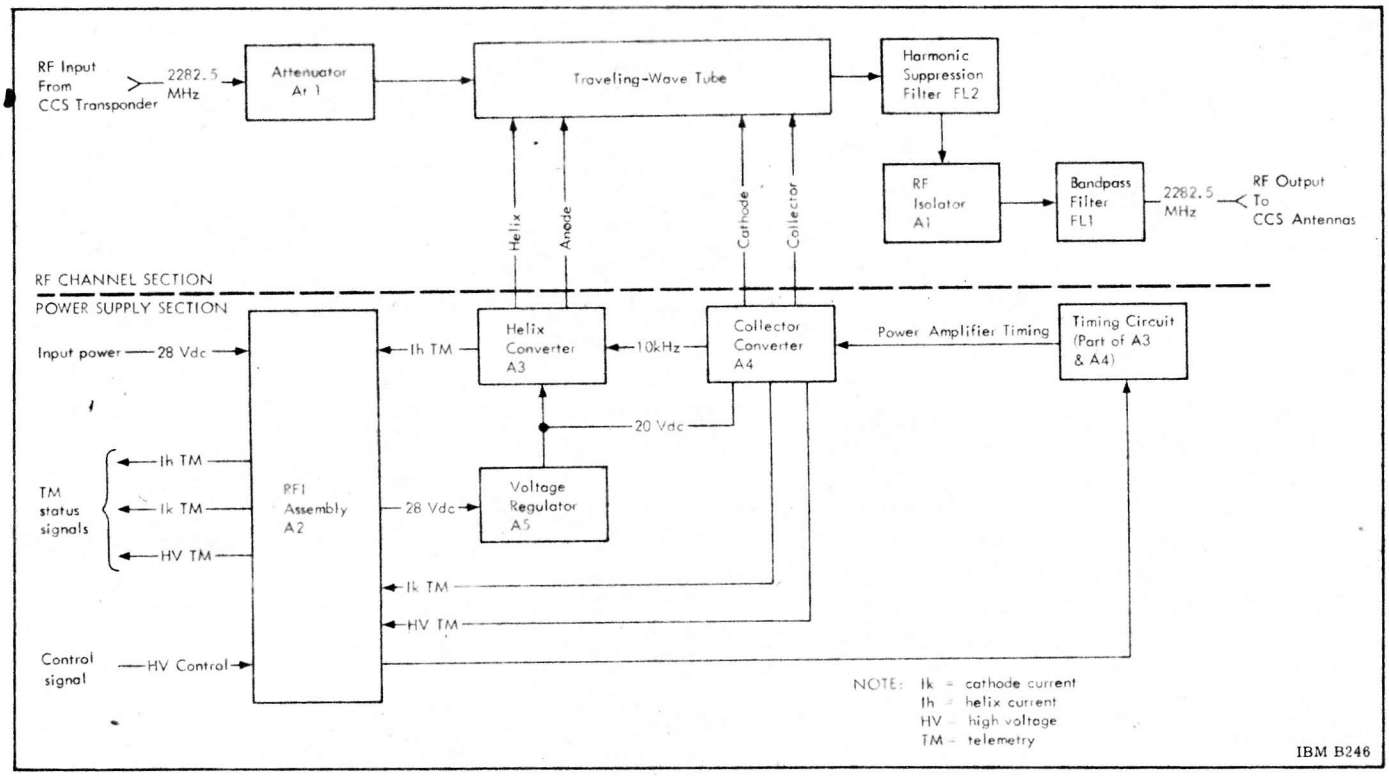


Figure 6.4-2. CCS Power Amplifier Block Diagram

Table 6.4-2 CCS Power Amplifier Characteristics

Input Voltage	28 ± 4 Vdc
Power Consumption	
Operate Mode	95 watts
Disable Mode	20 watts
Center Frequency	2282.5 MHz
Bandpass	20 MHz Flat ± 1 db
Drive Power	250 to 500 mW at 2282.5 MHz
Output Power	15 watts (min)
Input Terminal Impedance	50 ohms nominal at a VSWR ≤ 1.3:1
Output Terminal Impedance	50 ohms nominal at a VSWR ≤ 1.5:1
Output Isolation	20 db (min)
Output Spurious Response	No greater than negative 95 dbm at 2104 ± 5 MHz
Weight	9.072 kg (20 lb)
Dimensions	41.1 x 16.8 x 13.7 cm (14.2 x 6.6 x 5.4 in.)

Input power (28 Vdc) is applied to a voltage regulator which provides regulated 20 Vdc power for operation of the collector and helix converters. The collector converter provides a cathode reference of 0 Vdc and a collector operating voltage of 1200 Vdc for the TWT. The helix converter provides an anode voltage of 1800 Vdc and a helix voltage of 1650 Vdc, for operation of the TWT. All TWT voltages are measured with respect to the cathode.

Table 6.4-2 lists the main characteristics of the CCS Power Amplifier.

CCS ANTENNA SYSTEM

The CCS antenna system is designed to meet 3 requirements:

- To provide adequate coverage for prelaunch conditions.
- To provide the wide angular coverage required at low altitude during earth parking orbit.
- To provide narrow angular coverage of all stations which are optically visible during the period from injection to Spacecraft separation.

To meet these requirements, the system consists of an omnidirectional antenna pair for the receiver section of the CCS Transponder and an omnidirectional pair and a directional antenna for the transmitter section of the CCS Transponder. Figure 6.4-3 is a block diagram of the CCS antenna system. The omnidirectional pair for the receiver section is permanently connected and essentially maintains omnidirectional angular coverage for the receiver from launch throughout the mission. The transmitter section of the CCS Transponder operates into an omnidirectional pair from launch through injection to a point approximately 10,000 kilometers (5400 nautical miles) from the earth. At this distance, the path loss becomes great enough to require additional gain from the vehicle antenna system, and the transmitter is then switched to a single, multi-gain directional antenna.

A dc switching signal from the IU Switch Selector positions the CCS Coaxial Switch to one of its three output positions. For CCS transmissions of relatively short range, the transfer path of the CCS Coaxial Switch routes the rf signals to the two CCS/PCM omnidirectional antennas, via the CCS Hybrid Ring. These antennas use an omni, or dispersed, radiation pattern to propagate the rf energy earthward. The omnidirectional antenna elements are located diametrically opposite on the vehicle body and are driven with equal power.

For medium range transmissions, the CCS Coaxial Switch is switched to its second position. The rf signal is then routed to the low-gain element of the CCS directional antenna, which has two sets of radiating elements: one for low-gain and one for high-gain radiation. Long-range transmissions utilize the high-gain, narrow-beam element of the antenna and are routed through a third position of the CCS Coaxial Switch. The beamwidth of the directional antenna is adjustable, in two steps, so that the beamwidth may be reduced. (As the range becomes greater, the angle subtended by the earth becomes smaller, and the required gain increases.) The orientation of the directive antenna pattern remains fixed with respect to the vehicle, and directing of the pattern toward the ground stations is accomplished by attitude control of the vehicle.

The CCS Transponder and PCM/UHF telemetry system transmitter may be switched to share omnidirectional antennas or to their separate directional antennas as just described. The PCM/UHF telemetry system is included on the figure because of the CCS Hybrid Ring function in connecting the two systems to a common antenna network.

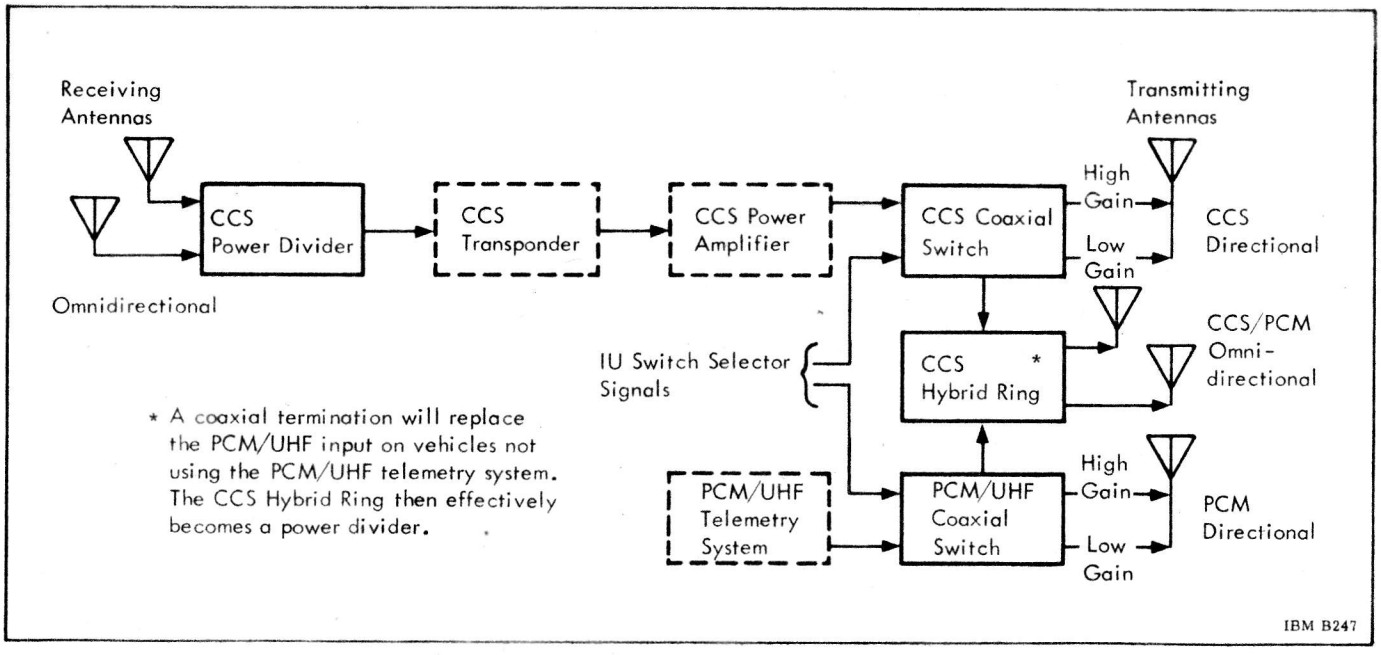


Figure 6.4-3. CCS Antenna System Block Diagram

CHAPTER 7
TRACKING SYSTEMS

SECTION 7.1
TRACKING INSTRUMENTATION

The purpose of radio tracking is the determination of the vehicle's trajectory. Tracking data is used for mission control, range safety, and post-flight evaluation of vehicle performance.

The Saturn vehicles carry several tracking transponders as listed in Table 7.1-1. A combination of tracking data from different tracking systems provides the best possible trajectory information and increased reliability through redundant data. The tracking of the Saturn Vehicle may be divided into 4 phases: (1) powered flight into earth orbit, (2) orbital flight, (3) injection into translunar trajectory, and (4) coast flight after injection.

Continous tracking is required during powered flight into earth orbit. A tracking ship will be located in the Atlantic to obtain very important tracking data, required for orbit determination, during the insertion into earth orbit. Figure 7.1-1 shows tracking stations used during the powered flight into earth orbit. The number of stations which can "see" the vehicle depends on the launch azimuth. Station visibilities are indicated in Figure 7.1-2 for launch azimuths of 72.5 degrees and 105 degrees. The figure is based on a typical Saturn V powered flight trajectory.

In addition, the Saturn Vehicle will be tracked from S-band stations at Cape Kennedy and on the Atlantic tracking ship. These stations have dual tracking capability; i.e., they can simultaneously track the two S-band transponders on the vehicle (one in the IU and the other in the Apollo Spacecraft). The S-band station on Bermuda has only a single capability and will track the Apollo Spacecraft transponder.

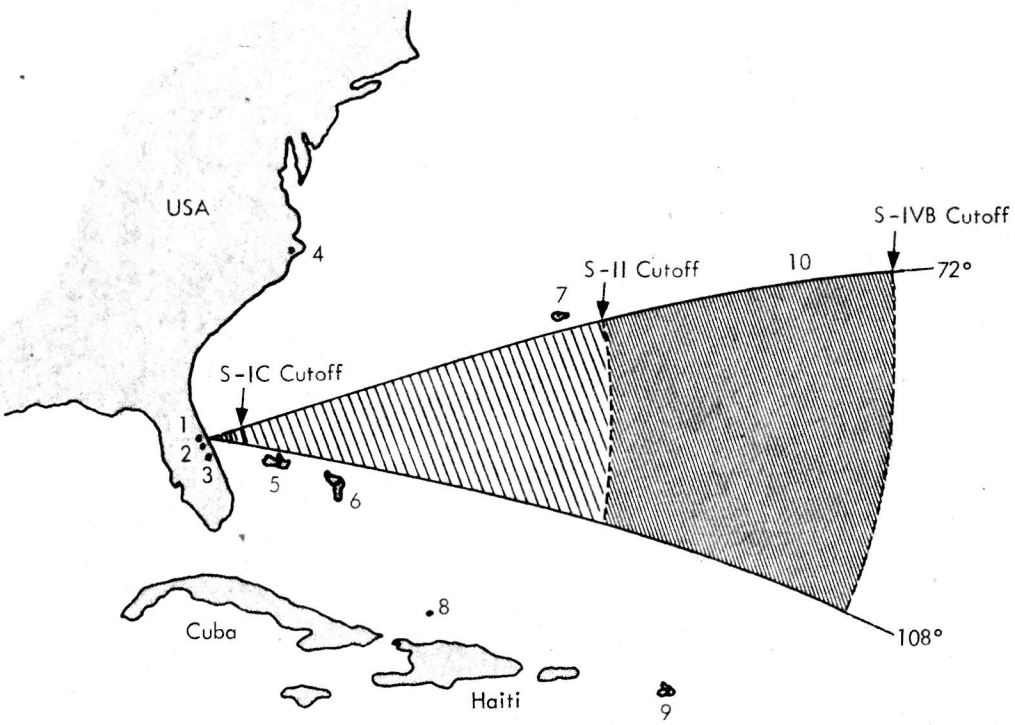
During orbital flight, tracking is accomplished by S-band stations of the Manned Space Flight Network and by C-band radar stations listed in Table 7.1-2. The Deep Space Instrumentation Facility S-band stations can track the Apollo Spacecraft to the moon and will also be involved in tracking after injection. Tracking information collected during orbital flight may be used to update the Saturn guidance system before injection.

In addition to land-based stations, five tracking ships, equipped with C-band radar and S-band stations, will be available. One of these ships will be used for insertion tracking in the Atlantic.

Tracking requirements for the launch vehicle during second burn of the S-IVB Stage and during the flight period following injection have not been completely defined. Stations listed in Table 7.1-2 will participate in this operation. The DSIF and MSFN stations have essentially the same capabilities. All S-band tracking stations will be equipped for reception of PCM telemetry at UHF frequencies.

Table 7.1-1 Saturn Tracking Equipment

Tracking System	Frequency Range	Utilization	Location	Effectivity
C-Band Radar	5400 - 5900 MHz	All flight phases	IU	all Saturn IB and all Saturn V
AZUSA/GLOTRAC	5000 MHz	Launch	IU	201 - 501 -
ODOP	890 - 960 MHz	Launch	S-IB S-IC	all Saturn IB all Saturn V
S-Band	2000 MHz	All flight phases	IU	all Saturn V



Number	Location	Tracking System
1.	Cape Kennedy, Florida	C-Band Radar ODOP AZUSA/GLOTRAC
2.	Patrick AFB, Florida	C-Band Radar
3.	Jupiter Inlet, Florida	GLOTRAC
4.	Atlantic, North Carolina	GLOTRAC Receiver
5.	Grand Bahama Island	C-Band Radar
6.	Little Carter Cay	GLOTRAC Receiver
7.	Bermuda Island	C-Band Radar GLOTRAC Transmitter & Receiver
8.	Grand Turk Island	C-Band Radar
9.	Antigua	C-Band Radar GLOTRAC Receiver
10.	Atlantic Ship (Position depends on launch azimuth)	C-Band Radar

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Figure 7.1-1 Launch Phase Tracking Stations

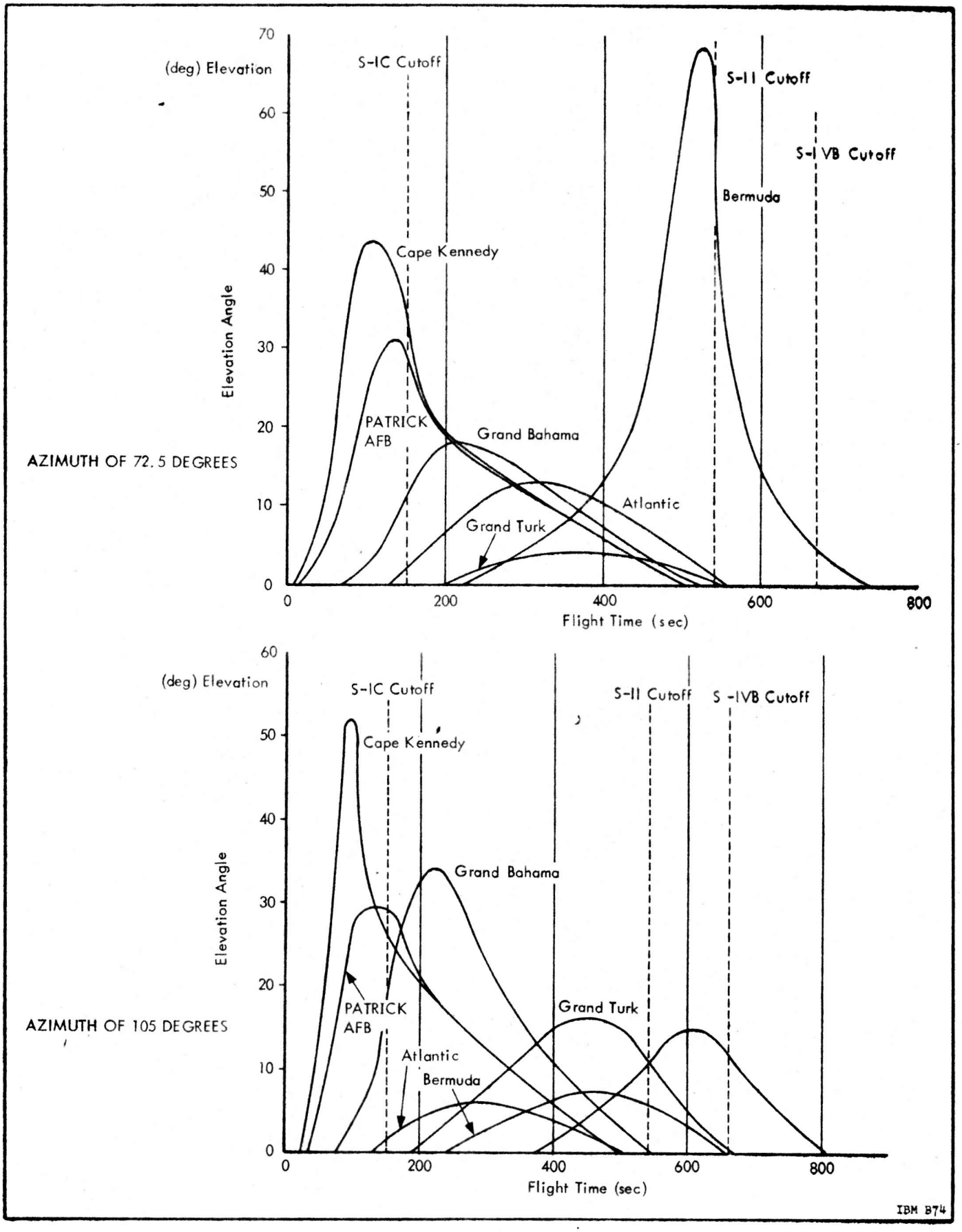


Figure 7.1-2 Station Visibility for Saturn V Powered Flight

Table 7. 1-2 Orbital Tracking Stations

Name and Location	S-Band Tracking Single Dual	Ant. Dia		C-Band Radar
Cape Kennedy, Florida	D	9.2 m	MSFN	X
Bermuda	S	"	"	X
Antigua Island	S	"	"	X
Canary Island	S	"	"	X
Ascension Island	D	"	"	X
Canarvon, Australia	D	"	"	X
Hawaii, USA	D	"	"	X
Guaymas, Mexico	S	"	"	
Wallops Island, USA	D	"	"	
Guam	D	"	"	
Texas Station, USA	S	"	"	
Canberra, Australia	D	26 m	DSIF/ JPL	
Goldstone, USA	D	"	"	
Madrid, Spain	D	"	"	
Goldstone, USA	D	"	MSFN	
Madrid, Spain	D	"	"	
Canberra, Australia	D	"	"	
Point Aguello, USA				X
White Sands, USA				X
1 Ship (Atlantic)	D			X
4 Ships	S			X

9. 2 m = 30 ft 26 m = 85 ft

MSFN - Manned Space Flight Network
DSIF - Deep Space Instrumentation Facility
JPL - Jet Propulsion Laboratory

SECTION 7.2

C-BAND RADAR

The function of the C-Band Radar Transponder (Model SST-135C) is to increase the range and accuracy of the radar ground stations equipped with AN/FPS-16, and AN/FPQ-6 Radar Systems. C-band radar stations at the Kennedy Space Center, along the Atlantic Missile Range, and at many other locations around the world, provide global tracking capabilities. Beginning with Vehicles 204 and 501 two C-band radar transponders will be carried in the IU to provide radar tracking capabilities independent of the vehicle attitude. This arrangement is more reliable than the antenna switching circuits necessary if only one transponder would be used.

The transponder receives coded or single pulse interrogation from ground stations and transmits a single-pulse reply in the same frequency band. A block diagram of the transponder is shown in Figure 7.2-1. A common antenna is used for receiving and transmitting. The transponder consists of five functional systems: superheterodyne receiver, decoder, modulator, transmitter, and power supply. The duplexer (a 4-port ferromagnetic circulator) provides isolation between receiver and transmitter. Interrogating pulses are directed from the antenna to the receiver, and reply pulses are directed from the transmitter to the antenna. The preselector, consisting of three coaxial cavaties, attenuates all RF signals outside the receiving band. The received signal is heterodyned to a 50 MHz intermediate frequency in the mixer and amplified in the IF amplifier which also contains the detector. In case of coded transmission, the decoder module provides a pulse output only if the correct spacing exists between pulse pairs received. The shaped-pulse output of the decoder is directed to the modulator which converts it into a high-power, precisely-shaped and precisely delayed pulse which is applied to the magnetron to produce the reply pulse. Six telemetry outputs are provided: input signal level, input PRF, temperature, incident power, reflected power, and reply PRF.

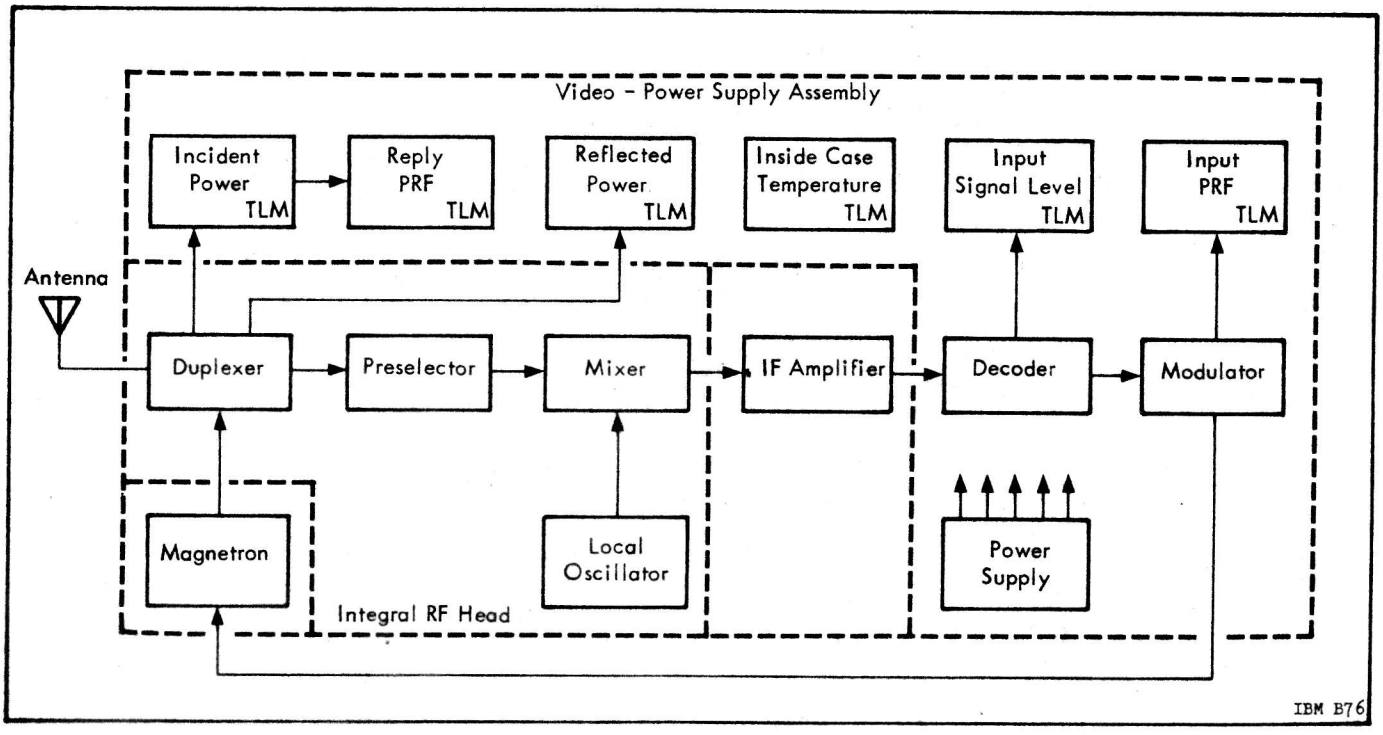


Figure 7.2-1 SST-135C Transponder System Block Diagram

Semiconductors are used in all circuitry, with the exception of the local oscillator and magnetron. The characteristics of the transponder are given in Table 7.2-1.

The radar ground stations determine the position of the vehicle C-band transponder by measuring range, azimuth angle, and elevation angle. Range is derived from pulse travel time, and angle tracking is accomplished by amplitude-comparison monopulse techniques. As many as four radar stations may track the beacon simultaneously. Some data about the AN/FPS-16 and AN/FPQ-6 radar is listed in Table 7.2-2.

Table 7.2-2 Radar Ground Station Characteristics

	AN/FPS-16	AN/FPQ-6
Frequency band (MHz) . .	5400-5900	5400-5900
Peak power (mw)	1.3	3.0
Antenna size (meters). . . .	3.9	9.2
Antenna gain (db)	47	52
Receiver noise figure (db) .	6.5	8
Angle precision (units) . . .	0.15	0.1
Range precision (meters). .	4.5	3.0

Table 7.2-1 C-Band Radar Transponder, Model SST-135C

Receiver Characteristics	
Frequency (tunable externally)	5400 to 5900 MHz (set to 5690 ±2 MHz)
Frequency stability	± 2.0 MHz
Bandwidth (3 db)	10 MHz
Off-frequency rejection	50 db image; 80 db minimum, 0.15 to 10,000 MHz
Sensitivity (99% reply)	-65 dbm over entire frequency range and all environments
Maximum input signal	+20 dbm
Interrogation code	Single or double pulse
Pulse width	0.2 to 5.0 us (single pulse), 0.2 to 1.0 us (double pulse)
Pulse spacing	Continuously settable between 5 and 12 us (set to 8 ±0.05 us)
Decoder limits	±0.25 us accept, ±0.85 us reject (5 to 12 us)
Transmitter Characteristics	
Frequency (tunable externally)	5400 to 5900 MHz (set to 5765 ± 2 MHz)
Peak power output	400 watts minimum, 700 watts nominal
Pulse width	1.0 ± 0.1 us
Pulse jitter	0.020 us maximum for signals above -55 dbm
Pulse rise time (10% to 90%)	0.1 us maximum
Duty cycle	0.002 maximum
VSWR of load	1.5:1 maximum
Pulse repetition rate	10 to 2000 pps; overinterrogation protection allows interrogation at much higher rates with count-down; replies during overinterrogation meet all requirements
Transponder Characteristics	
Recovery time	50 us single pulse, 62 us double pulse maximum for input signal levels differing by up to 65 db (recovers to full sensitivity with no change in transmitter reply power or frequency with multiple radars interrogating simultaneously)
Fixed delay	Settable 2 ± 0.1 and 3.0 to 0.01 us (set to 3.0 ± 0.01 us)
Delay variation with signal level	50 nanoseconds maximum from -65 dbm to 0 dbm
Power requirements	24 to 30 volts
Primary current drain	0.7 ampere standby; 0.9 ampere at 1000 pps
Weight	2.5 kg (5.5 lbs)

SECTION 7.3

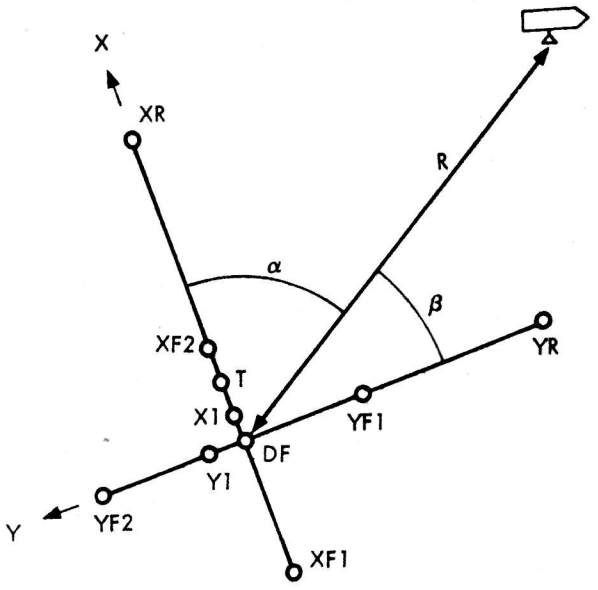
AZUSA/GLOTRAC

7.3.1 AZUSA

AZUSA is an interferometer tracking system which determines the position of a vehicle-borne transponder. Two AZUSA stations are in operation, one station (MK II) at Cape Kennedy and the other station (MK I) at Grand Bahama Island. The AZUSA system provides real-time tracking data used for range safety impact prediction and post flight trajectory analysis. AZUSA stations cover only a portion of the Saturn V powered flight trajectory.

The position of the vehicle (transponder) is determined at the AZUSA ground stations by measuring range (R) and two direction cosines (l, m) with respect to the antenna baselines. The antenna layout of the AZUSA MK II station, shown in Figure 7. 3-1, consists of two crossed baselines (at right angle) with three antenna pairs each. The transmitter antenna (T) radiates a CW signal at 5 GHz to the vehicle. This signal is offset by 60 MHz in the transponder and retransmitted to the ground station receiving antennas. The direction cosine, with respect to a baseline, is obtained from the measurement of the phase difference between signals received at spaced antenna pairs along this baseline. The range to the transponder is found by measuring the phase difference between transmitted and received signal. For range ambiguity resolution, the transmitted carrier is modulated with several low frequencies.

Direction cosine measurement is accomplished by using the antennas in pairs to provide baselines of 5 meters, 50 meters, and 500 meters as indicated in the table of Figure 7. 3-1. A conical scan antenna (DF) yields unambiguous direction measurement and furnishes ambiguity resolution for the 5-meter baselines. The 5-meter baselines resolve ambiguity for the more accurate 50-meter baselines, and the 500-meter baselines supply information for computing cosine rate data. The direction finder antenna DF (conical scan antenna) provides pointing information for all other antennas.



$l = \cos\alpha = \frac{L_x}{R}$

$m = \cos\beta = \frac{L_y}{R}$

T: Transmitter Antenna
DF: Direction Finder Antenna (Receiving)
XF, XR, YF, YR: Receiving Antennas
L: Distance between antennas

Antennas	Baseline Length L_x , L_y	Measurements
DF - X1	5 m	Intermediate cosα
XF1 - XF2	50 m	Fine cosα
XF1 - XR	500 m	Rate cosα
DF - Y1	5 m	Intermediate cosβ
YF2 - YF1	50 m	Fine cosβ
YF2 - YR	500 m	Rate cosβ

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Figure 7. 3-1 AZUSA (MK II) Ground Station Layout

The signals received at the two spaced antennas of an antenna pair have a phase difference caused the difference in range between the transponder and each of the antennas. This phase difference is measured and used to compute the direction cosine. The accuracy of the measurement increases with increasing baseline length, but data becomes ambiguous and coarse measurements are necessary for ambiguity resolution.

Range is determined at the ground station by comparing the instantaneous phase of the transmitted modulation signal to that of the received modulation signal. The resulting phase difference is directly proportional to the propagation time from the ground station to the transponder and back to the ground station. In other words, phase difference is proportional to range. Using a high range modulation frequency to obtain fine resolution, results in output data that are ambiguous, the number of ambiguities is proportional to the modulation frequency.

The ambiguities in range measurement are resolved by using three modulation frequencies that are obtained by the frequency division of a single, precise, frequency source at the ground station. The phase shift is measured for each one of these harmonically related frequencies. The lower frequency phase data is used to resolve the ambiguities in the next higher frequency phase data. This arrangement has, as advantages, the resolving power of the highest frequency signal and the extended unambiguous range data provided by the lower data frequency. The modulation signals used for range measurement are 157.4 Hz, 3.934 kHz, and 98.356 kHz. The fine range modulation signal, 98.356 kHz, remains ON at all times so the transponder can "lock-on" with the ground station. Higher resolution range data is obtained by coherent carrier phase comparison.

The coherent transponder includes a phase-control loop in which the 98.356 kHz fine range modulation frequency is multiplied by a factor of 612 to establish the transponder offset frequency (60.194 MHz) and a frequency and phase-coherent response signal (5000 MHz).

At the ground station, the 98.356 kHz frequency is also multiplied by 612 to equal the transponder offset frequency (60.194 MHz). Both, the 5000 MHz signal received from the transponder and the data signal, are heterodyned with a local oscillator signal to obtain approximately 5 MHz. Data and reference signals are then fed into a discriminator which provides one pulse (count) output for each 360-degree phase difference (1 cycle) in the input circuit. Plus and minus pulses are fed on separate lines to a bidirectional counter. The coherent carrier range data is then fed to an IBM 7090 Computer with the direction cosine data (l, m) and modulation-derived slant range data. The computer, using 20 input samples per second, solves the equations for the position of the vehicle.

AUTOMATIC FREQUENCY CONTROL LOOP

The AZUSA Type-C Transponder used in the Saturn Vehicles is a part of the overall AFC loop in the AZUSA system (Figure 7.3-2). Upon transponder activation, the klystron transmits a 5060.194 MHz signal which is swept ±2 MHz by a 15 Hz internal sweep generator. This enables the ground station and the transponder to find a common frequency so that lock-on can occur. When frequency lock-on occurs, the 5060.194 MHz signal transmitted by the ground station will be shifted slightly by AFC action so that, after the transponder receives the signal and retransmits it, the frequency received by the ground station receivers will be 5000 MHz. The 5060.194 MHz (plus Doppler) signal entering the transponder receiver is mixed with a fraction of the retransmitted signal to produce a 60.194 MHz offset frequency. A frequency discriminator is used to maintain the offset frequency within 30 Hz.

Phase lock between the transponder and ground station is established by multiplying the fine range modulation frequency (98.356 kHz) received from the ground station and using it as a reference for a phase discriminator. This phase discriminator has higher output gain than the frequency loop discriminator and holds the transponder offset frequency (60.194 MHz) correct to within a fraction of a cycle. The Type-C Transponder uses this combination frequency-phase discriminator to obtain maximum stability in both AFC and APC loops. This coherent condition in the transponder enables phase measurements to be made at the ground station between the received 5000 MHz signal and the 5060.194 MHz transmitted signal (heterodyned to 5000 MHz) to obtain high-resolution incremental range data. Similarly, phase comparison of the transmitted and received 98.356 kHz modulation signals produces non-ambiguous range data.

Before lock-on, the transmitter local AFC loop and the local over-all AFC loop are used to keep the ground station transmitter frequency at 5060.194 MHz. When the ground station and the transponder are frequency locked, a 5 MHz signal from the ground station range receiver IF amplifier controls the over-all AFC loop. This high-gain loop overrides both the local over-all AFC loop and the transmitter AFC loop

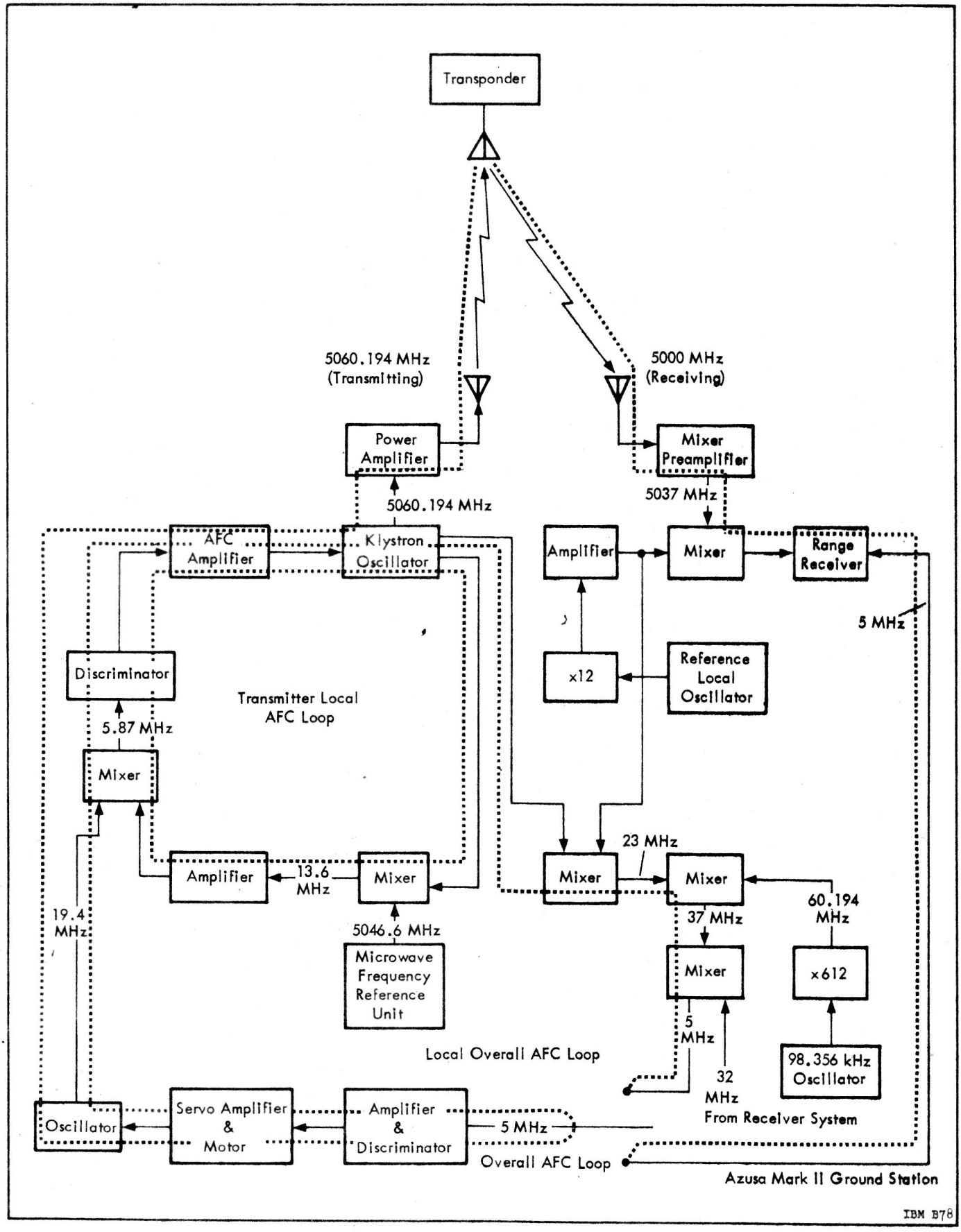

Figure 7. 3-2 AFC Loops, Ground Station and Transponder

(Figure 7. 3-2). Should the return signal received from the transponder deviate from 5000 MHz at the ground station receiver, the ground station receiver will detect the error and cause the ground station transmitter frequency to shift slightly in a direction to correct the error (through AFC action). The transponder receiver detects the frequency or phase change and corrects the return frequency so that the offset frequency remains exactly 60. 194 MHz (through the transponder AFC and APC loops). Thus, the vehicle-to-ground link maintains a constant frequency (5000 MHz) at the ground station receivers despite systematic frequency drift and Doppler shift.

TRANSPONDER

In the transponder (Figure 7. 3-3), the 5060. 194 MHz interrogation signal and the 5000 MHz klystron local oscillator signal produce a 60. 194 MHz IF, or offset frequency, in the crystal mixer. This signal is mixed with a 55. 2 MHz second local oscillator signal. The second IF (4. 994 MHz) is amplified and fed to the receiver frequency discriminator where the range signals which modulate the ground station carrier are detected. This range modulation (98. 356 kHz) is fed to the compensation network. The 4. 994 MHz IF signal is also fed to the phase network and to one side of the frequency-phase discriminator.

A 4. 994 MHz reference signal for phase lock is provided as follows: The 98. 356 kHz range signal is directed through the compensation network, an amplifier, and two crystal filters, to a frequency multiplier circuit. Here the signal is multiplied to 60. 194 MHz. (One crystal filter is in the compensation network subassembly and one is in the sweep oscillator subassembly.) The 60. 194 MHz signal enters the phase network and is mixed with 55. 2 MHz from the receiver second local oscillator to obtain the 4. 994 MHz reference for the phase discriminator.

In the compensation network, the phase and frequency discriminator error voltage from the phase network overrides the output from the sweep oscillator. It is then combined with the 98. 356 kHz range modulation and fed to the modulator. In the modulator these signals are superimposed on the klystron anode voltage. The dc error signal maintains phase lock between the 5060. 194 MHz received signal and the 5000 MHz response signal. The 98. 356 kHz is used to modulate the response signal. The 98. 356 kHz phase shift in the transponder is held to an absolute minimum so that phase comparison of the received signal and transmitted signal at the ground station will indicate actual range to the transponder.

The waveguide subassembly is designed with two bandpass filters internally connected to a symmet-

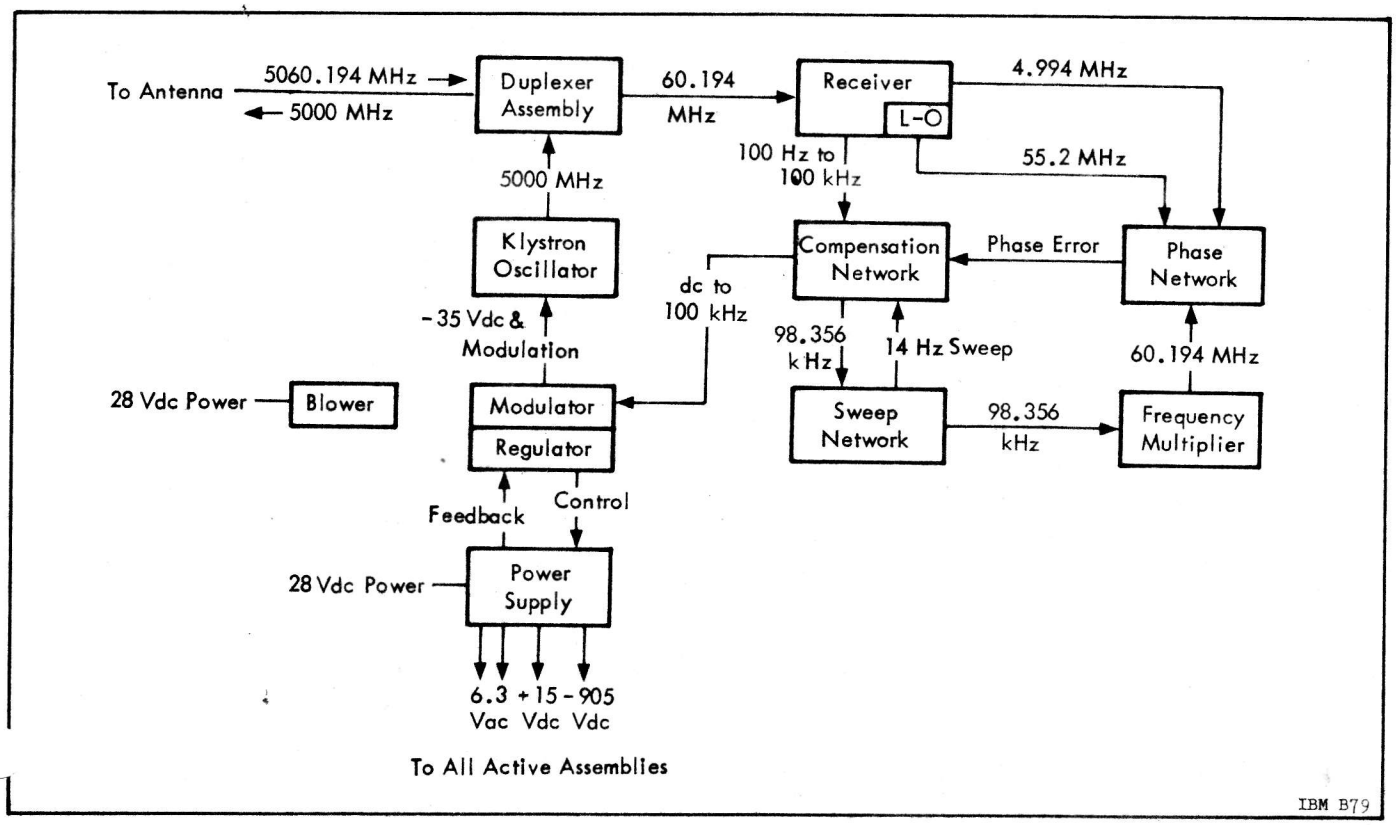

Figure 7. 3-3 AZUSA Transponder Block Diagram

rical Y section. This arrangement permits the use of a single receiving-transmitting antenna. The klystron output is carried to the 5000 MHz filter by coaxial cable. The signal passes through a 3-section filter, the symmetrical Y, and a waveguide-to-coaxial transition and is carried to the antenna by coaxial cable. A 5060.194 MHz signal entering the antenna passes through the same coaxial cable into the waveguide. A 2-section filter passes the incoming 5060.194 MHz signal and a small amount of the 5000 MHz signal present in the symmetrical Y to a crystal mixer which produces a 60.194 MHz offset frequency.

The Type-C Transponder uses transistors in all circuitry except for the klystron. The Type-C Transponder operates also with GLOTRAC stations described briefly in the following paragraphs. Table 7.3-1 lists the characteristics of the AZUSA system.

7.3.2 GLOTRAC

GLOTRAC (GLObal TRACking) was originally planned as a global tracking system, but changes in programs restricted the number of ground stations. GLOTRAC uses the AZUSA Type-C Transponder in the vehicle. GLOTRAC ground stations are equipped with either a transmitter or a receiver or both as indicated in Figure 7.1-1. Both existing AZUSA stations may be considered as part of GLOTRAC. The transponder in the vehicle is interrogated by an AZUSA ground station or by a GLOTRAC transmitter site. The transponder offsets the received frequency and retransmits the signal to GLOTRAC receiving sites where the Doppler shift is measured by comparing the received signal with the transmitter signal (if receiver is located near the transmitter) or with a local frequency source. The measured Doppler shift provides the range sum similar to ODOP (refer to Section 7.4). At GLOTRAC stations equipped with both a transmitter and receiver, the range to the transponder is measured by phase comparison between the transmitted and received signals. The AZUSA Type-C Transponder can also be interrogated by C-band radars for range and angle determination.

The range rates measured at three receiving stations yield the vehicle velocity, and by integrating this velocity, the position is obtained. Initial conditions for integration are obtained from radar range measurements. Data measured at all stations is transmitted to the computer at Cape Kennedy. Accuracy of GLOTRAC measurements is 30 meters (98.4 feet) in position and 0.15 meters/second (0.49 feet/second) velocity.

Table 7.3-1 AZUSA Characteristics

Transponder Type-C	
Receiver frequency	5060.194 MHz
Transmitter frequency	5000.000 MHz
RF power output	2.5 watts
Input voltage	28 Vdc
Input current	-5 amperes
Receiver input signal	-12 to -90 dbm
Weight	8.74 kg (19.3 lbs)
Size	0.006 meters^3 (372 inches^3)
AZUSA Ground Station Mark II	
Transmitted power	2 kw
Transmitter frequency	5060.2 MHz ±0.75 MHz
Ranging modulation	157.4 Hz, 3.934 kHz, 98.351 kHz
Receiver frequency	5000 MHz
Receiver sensitivity	-145 to -147 dbm
Receiver antenna gain	33 db (MK II)
Accuracies:	
Range	3.05 meters
Angle	1 x 10^{-5} in cosine data

SECTION 7.4

ODOP TRACKING SYSTEM

The ODOP (Offset DOPpler) tracking system is essentially the same as the UDOP system used for many years at the Atlantic Missile Range, but ODOP operates at different frequencies. It is a phase-coherent, multistation Doppler tracking system which measures position of a vehicle equipped with the ODOP transponder. ODOP stations are located at and around Cape Kennedy. The ODOP transponder is carried in the first stage (S-IB or S-IC) of the Saturn Vehicles and, therefore, ODOP tracking data is limited to the flight of the first stage only. The ODOP tracking system provides data immediately following lift-off while other tracking systems cannot "see" the vehicle or their accuracy is reduced by multipath propagation during the early phase of the flight.

The basic operation of the ODOP system is illustrated in Figure 7.4-1. The ground transmitter radiates a CW signal of 890 MHz to the transponder in the vehicle. The transponder shifts the received signal in frequency by 70 MHz and retransmits it to the receiving stations (R1, R2, R3). The signal from the transponder received at the ground stations contains a 2-way Doppler shift f_D which is extracted by mixing the received signal (f_i = 960 MHz + f_D) with the reference frequency (f_R = 960 MHz) derived from the transmitter frequency. Actually, a reference frequency of 53.33 MHz is transmitted over a VHF link to each transmitter station and then multiplied by a factor of 18, yielding 959.94 MHz. When this frequency is combined with the signal received from the

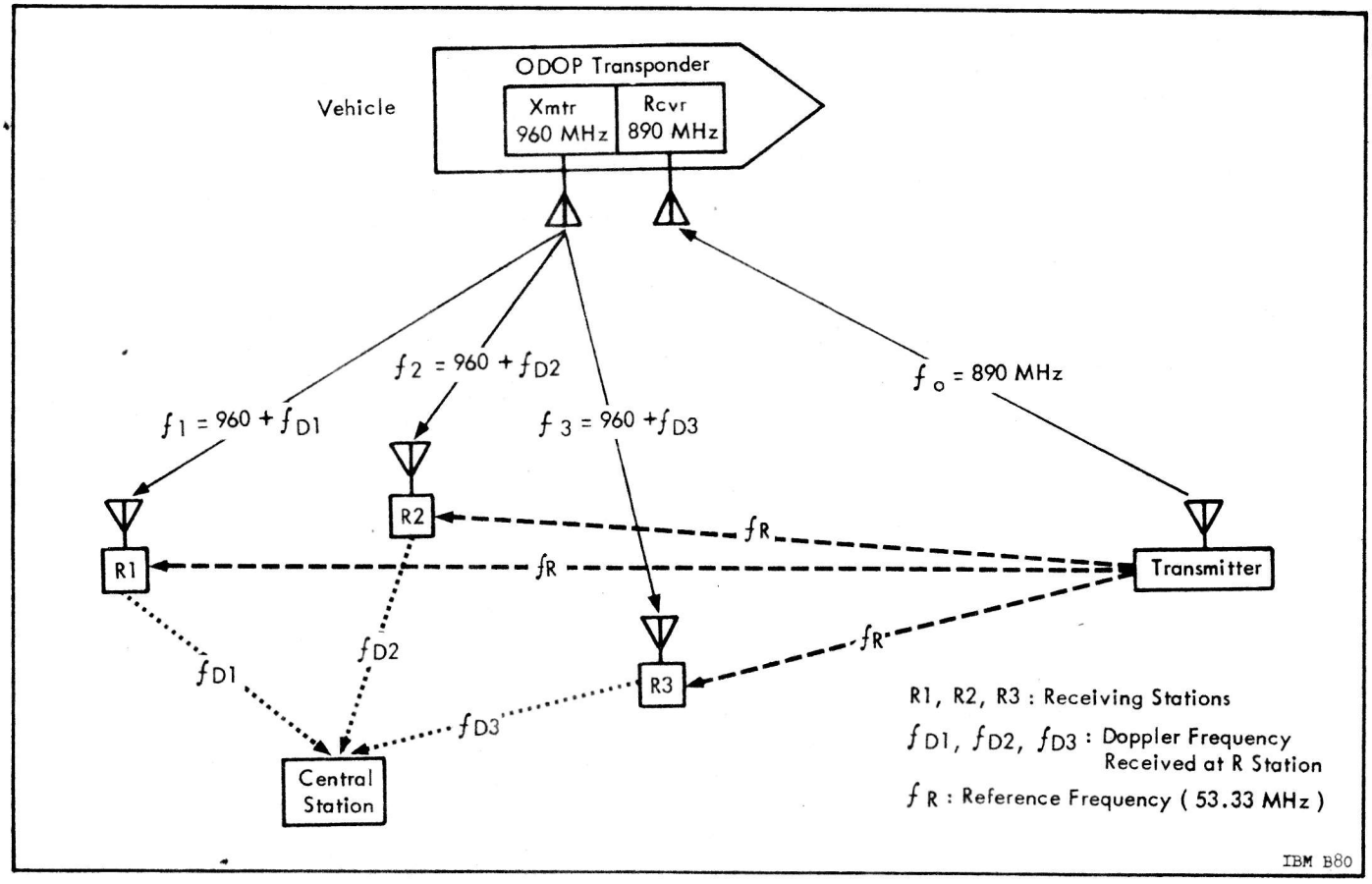

Figure 7.4-1 ODOP System Configuration

transponder, the Doppler shift is obtained with a 60 kHz bias frequency (60 kHz $+f_D$). The UDOP system used a transmitter frequency of 450 MHz which was doubled in the transponder (900 MHz). The higher frequency in the ODOP system (890 MHz versus 450 MHz) is less affected by the ionosphere and the result is increased tracking accuracy.

The Doppler frequencies, f_D, (including the bias frequency) from all receiving stations are transmitted to the central station and recorded on magnetic tape. Integration of the Doppler frequency received at a particular station provides the range sum, i.e., the distance transmitter-transponder-receiver. At least three range sums (for three different stations) are necessary to compute the position of the vehicle (transponder). The ODOP system uses 20 receiver stations around Cape Kennedy for redundancy and optimum tracking geometry. ODOP tracking data is not available in real time but is obtained from post-flight evaluation.

A block diagram of the ODOP transponder is shown in Figure 7.4-2. It is a modified version of the transponder used by the Jet Propulsion Laboratory in the Ranger Vehicles. Separate antennas are used for the receiver and the transmitter. The transponder consists of a double superheterodyne receiver (890 MHz) and a transmitter (960 MHz). The signal transmitted from the transponder is phase-coherent with the signal received by the transponder. Phase coherence is accomplished by an automatic phase tracking loop. The transponder is completely transistorized.

The characteristics of the ODOP tracking system are listed in Table 7.4-1.

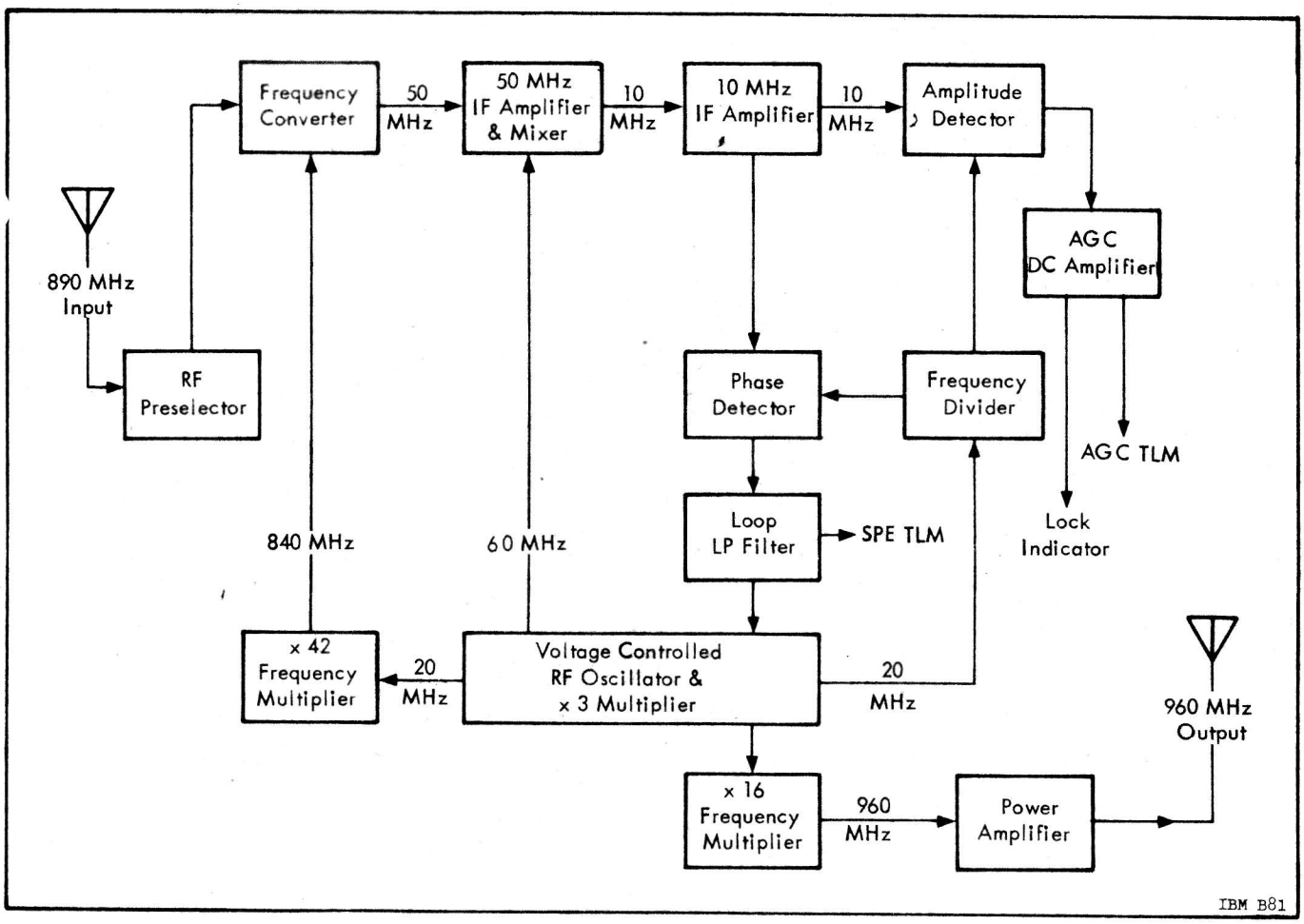

Figure 7.4-2 ODOP Transponder Block Diagram

Table 7.4-1 ODOP System Characteristics

Ground Transmitter:	
Frequency	890 MHz
Transponder:	
Receiver frequency	890 MHz
Receiver noise figure	14 db
Receiver threshold sensitivity	-132 dbm
Predetection bandwidth	100 kHz
Threshold noise bandwidth.	600 Hz
Strong signal noise bandwidth	1400 Hz
Transmitted frequency.	960 MHz
Transmitter power	1 watt
Required dc power	36 watts (28 volts)
Weight	10.25 kg (23.0 lbs)
Size	7370 cm^3 (448 in^3)
Ground Receiving Station:	
Receiver frequency	960 MHz
Receiver sensitivity	Not Available
Receiver bandwidth	Not Available
Receiver noise figure	Not Available

SECTION 7.5
S-BAND TRACKING

S-Band tracking of the Saturn V Vehicle is provided by the Command and Communication System (CCS). The CCS is a phase-coherent, receiver-transmitter system capable of establishing a communication link between the Unified S-Band (USB) ground stations and the IU of the Saturn V Vehicle. The CCS consists of a transponder, a power amplifier, and an antenna system and provides for launch vehicle up-data command, down-link PCM telemetry, and turn-around ranging. Section 6.2 of this document discusses the up-data command capability. Section 6.4 discusses the functional characteristics of the CCS components and the down-link PCM telemetry function and interface with the CCS. This section deals with the technique and characteristics of the turn-around ranging capability.

The USB ranging system is a variation of the classical radar ranging method of measuring the round trip propagation time of a signal from a ground transmitter to a vehicle transponder and back to a ground station. The ground based ranging system transmits an S-band carrier (2101.8 MHz) phase modulated by a particular type of pseudo-random binary ranging code (pseudo-random noise – PRN) to the CCS Transponder in the launch vehicle (Figure 7.5-1). The code modulation is detected in the CCS Transponder and used to modulate a down-link S-band carrier (shifted in frequency from the up-data carrier to 2282.5 MHz), which is then received by the ground receiver using the same antenna as is used for transmitting. Ground antenna steering is accomplished by monopulse signal null processing. The ground receiver is a type of phase-locked receiver which tracks both the S-band carrier and the PRN code. A range "fix" is derived by cross-correlating the transmitted code with the received code and noting the value of the shifting parameter which gives the maximum cross-correlation reading. From this shifting parameter value, the signal round trip propagation time is known. After a course range fix has been established, the PRN code can be disabled and a range update derived from noting the doppler shift in a 2-bit clock modulation of the carrier. Hence, the ranging system changes from a sampled system to an incremental system. Any loss of data or carrier will result in re-transmission and correlation of the PRN code for an exact ranging "fix" before reverting to the incremental updating again. Azimuth and elevation angles are determined from the ground antenna gimbal readouts.

7.5.1 RANGING CODE

The USB ranging system utilizes a continuous coded pulse transmission, rather than a system of one or several pulses, to avoid ranging ambiguity and to enhance the probability of detection of the return pulse.

If, in a conventional pulsed ranging system, the repetition period of the pulse is less than the time required for the signal to travel to the target and return, there will be ambiguity in the range measurement. Since the USB ranging system is designed to be compatible with the goals of the complete Apollo program, it must provide unambiguous ranging to lunar distances. At lunar distances, the ambiguity can be avoided only if the pulse repetition period is greater than 2.6 seconds.

If a single pulse of 1-microsecond duration is sent to the vehicle and returned after 2.6 seconds, it will be greatly attenuated. The power in this pulse must be averaged over the 2.6-second interval, greatly reducing the chance of detection at such a range. A train of pulses can be transmitted to increase the average power received, but the transmitter must wait at least 2.6 seconds between transmissions for the train of pulses to be received in order to distinguish between two pulse trains. This increases the average power received greatly, but even a greater improvement can be made by sending a train of coded pulses such that the series of pulses in the code is not repeated during the 2.6 second interval. If, at the same time, the numbers of zeros and ones are equally divided, there is the same power as contained in the same period of a train of equally spaced pulses, but the transmitter no longer has to wait for the first pulse group to be received before sending the next. The PRN code is such a train of coded pulses and does not repeat itself for a total period of approximately 5.4 seconds. The PRN code is generated in the ground

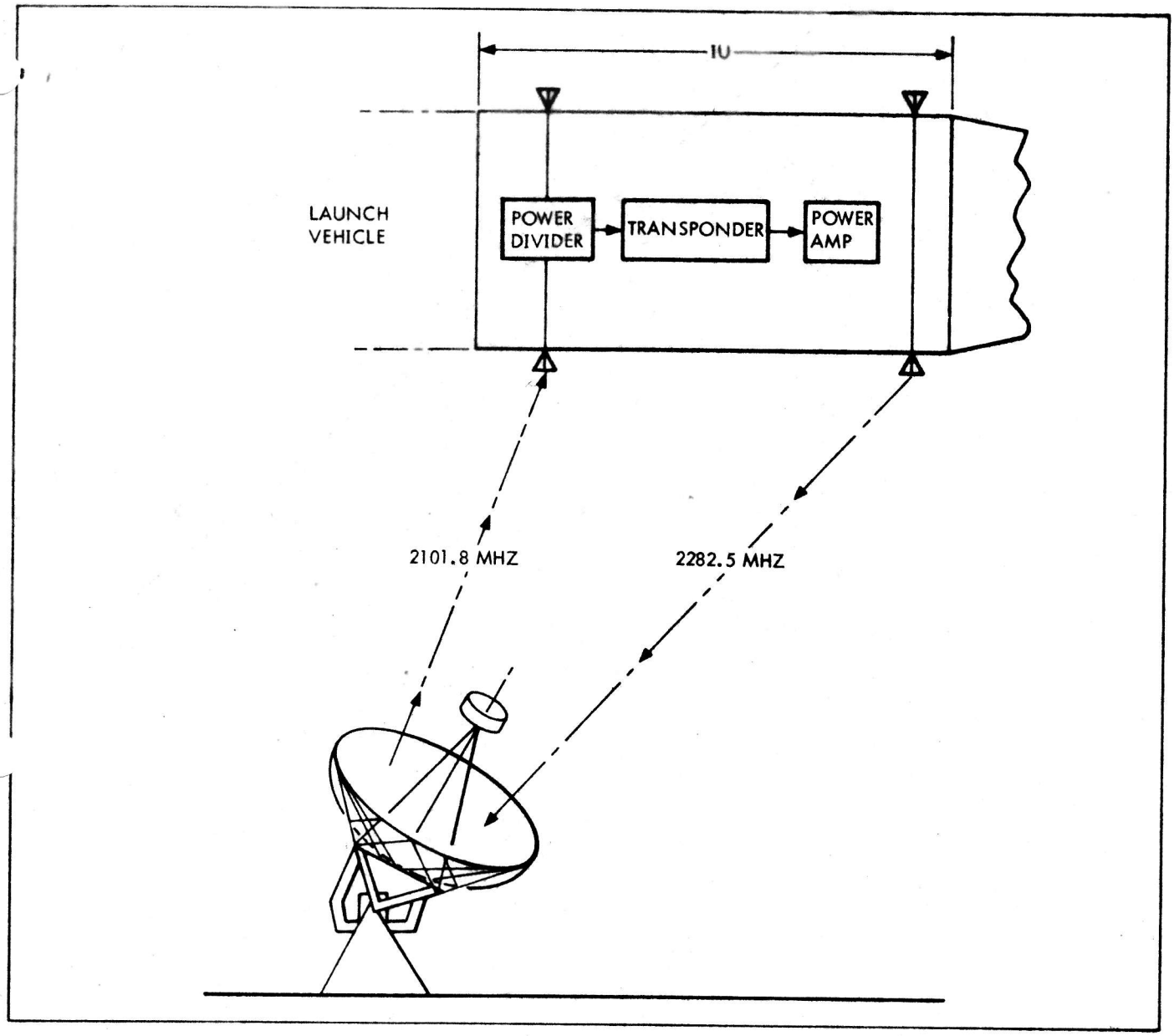

Figure 7.5-1 S-Band Tracking Configuration

equipment by digital shift registers with suitable feedback functions. This PRN code has the property that when the transmitted and received codes are compared on a bit-by-bit basis, correlation or matching can only be achieved at one unique value of delay or correlation parameter. To make an unambiguous range measurement at lunar distance would require a code period of several million bits in length and, at most, the same number of trial matchings for acquisition. The actual code is achieved by combining, bit by bit, several repetitive subcodes or code components in accordance with Boolean expression. The subcode components, designation, and length in bits are:

CL code component – 2 bits

X code component – 11 bits

A code component – 31 bits

B code component – 63 bits

C code component – 127 bits

The length in bits of the total code is the product of the lengths in bits of the individual components, or 5,456,682 bits.

Further, it is possible to acquire the total code by acquiring the components individually in turn. This reduces the number of correlation readings (or matchings) required from approximately 3-1/3 million to 232. The 2-bit CL component is not acquired by digital means, but rather is used in the process of establishing a clock-loop in the ranging receiver.

7.5.2 RANGE DETERMINATION AND FUNCTIONAL OPERATION

The process of determining the range (R_T) of a space vehicle from a ground station, or the equivalent round trip propagation time of an rf signal, can be generally stated as the relation:

$$R_T = R_0 + \int_0^{T_0} R\,dt$$

where R_0 is the range at some reference time T_0, and the integral is the sum of range increments since that time.

The constant of integration (R_0) is determined by determining the fixed range at the start of ranging acquisition. The term R_0 can be expressed as NT + d, where N is some unknown integral number of clock code periods (T) plus a delay (d) equal to some unknown fraction of T (see Figure 7.5-2).

The clock code period (T) is known. Determining the value of N is accomplished by digitally shifting the components of the received code and measuring the correlation indication at each shift position until a maximum is obtained. The fractional

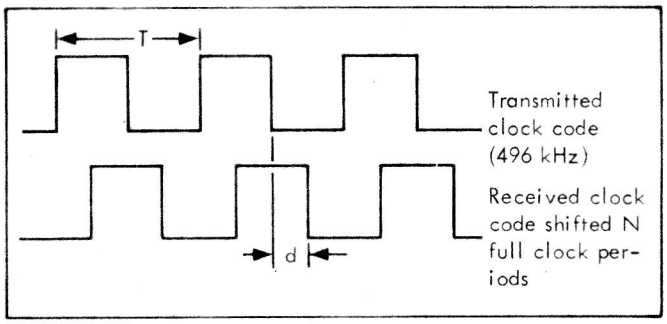

Figure 7.5-2. Constant R_0 Expressed as a Function of N and d

clock-cycle delay (d) is determined by the time offset, or delay, between transmission and reception of a given point in the clock code. The operations required to determine R_0 are referred to as range acquisitions and are the only operations requiring the use of the PRN codes. Once acquisition has been accomplished, it is possible to disable the full code modulation and modulate the carrier instead with the 2-bit clock component only. The advantage of changing from full code to 2-bit clock modulation lies in the fact that this not only cuts down on the required sideband power but also limits the spectral distribution of ranging frequencies to two single spectral lines--496 kHz above the S-band carrier.

The integral in the expression for R_T is determined by continually tallying the full doppler cycles derived from comparison of received carrier submultiples (every 16th S-band carrier doppler cycle). Once acquisition has been accomplished, the resolution of the tracking system is approximately ± 1 meter.

CHAPTER 8
POWER SUPPLY AND DISTRIBUTION SYSTEM

SECTION 8.1

GENERAL DISCUSSION

The power supplies for the Saturn Vehicles provide the electrical power necessary to operate the various onboard electronic and electromechanical components. Each vehicle stage contains batteries, power supplies, cables, connectors, and distributors. The distribution system interconnects these units. Figure 8. 1-1 illustrates the arrangement of the power and distribution system components within each Saturn V Stage.

While the component interconnection is similar in each stage, the grounding scheme differs between stages. The IU grounding system is discussed later in this chapter.

The Power Distributor is the only distribution system component whose basic function may not be obvious. Essentially, it is a junction box which provides quick access to stage circuitry and overall stage and vehicle logic. Such a device becomes necessary because of the impact on airborne and ESE hardware which is created by the variety of mission requirements assigned to the Saturn Vehicles. The Power Distributors are equipped with terminals, relays, resistors, and diodes. These component parts are either hard mounted or mounted on printed circuit boards to permit rapid access to the distribution, switching, and isolation networks.

An illustration of the power and distribution system is shown in Figure 8. 1-2. The figure represents a small portion of the actual logic involved, and only the IU system is detailed.

Functions provided by the power supply and distribution system include the following:

- Primary power is fed to high current capacity buses in the Power Distributor. Components which require high current levels are supplied directly from these buses.
- Each stage is equipped with a power transfer switch to select a power source either internal or external to the vehicle. During normal checkout operations, a ground power source will be used in place of the airborne batteries. A detailed explanation of power transfer is provided in Section 8. 2.
- Each power source generally supplies at least one bus in each distributor.
- Buses are provided to other stages for event logic and EDS signal transmission.
- Power requirements, other than that supplied by the airborne batteries, are usually provided by a special power supply (e. g., power source for component D in Figure 8. 1-2).
- Distributor switching facilitates checkout operations and is essential for control of certain flight events. Figure 8. 1-2 illustrates how both intra-stage and inter-stage switching is accomplished.
- During prelaunch operations, many switching operations are possible from the ESE. Figure 8. 1-2 illustrates how Power Distributor relays K1 and K2 are utilized to control the power to components C and D when the power transfer switch is in the external position. Typical Switch Selector control of power application and discrete event transmission is illustrated by the configuration of relays K3 and K4.

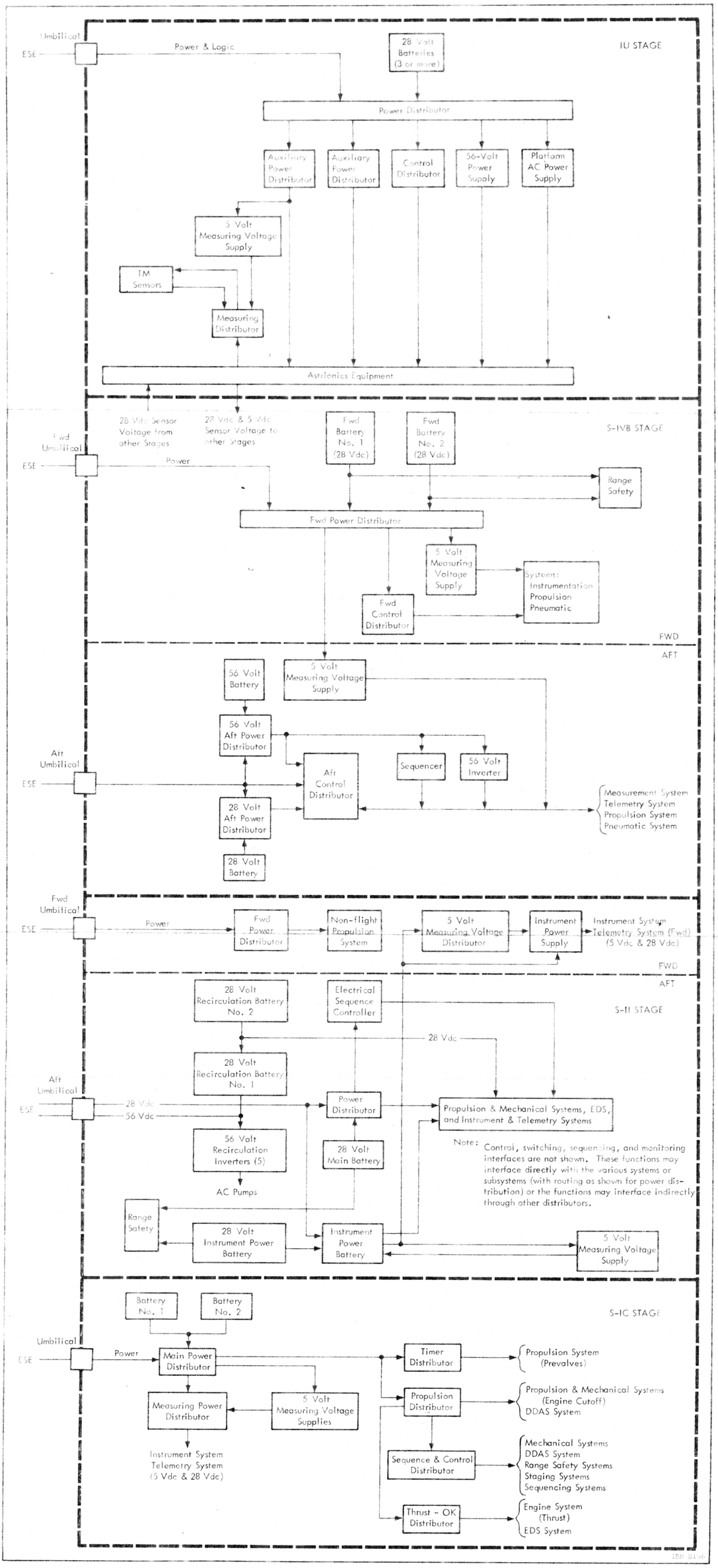

Figure 8.1-1 Block Diagram of the Saturn V Power Supply and Distribution Systems

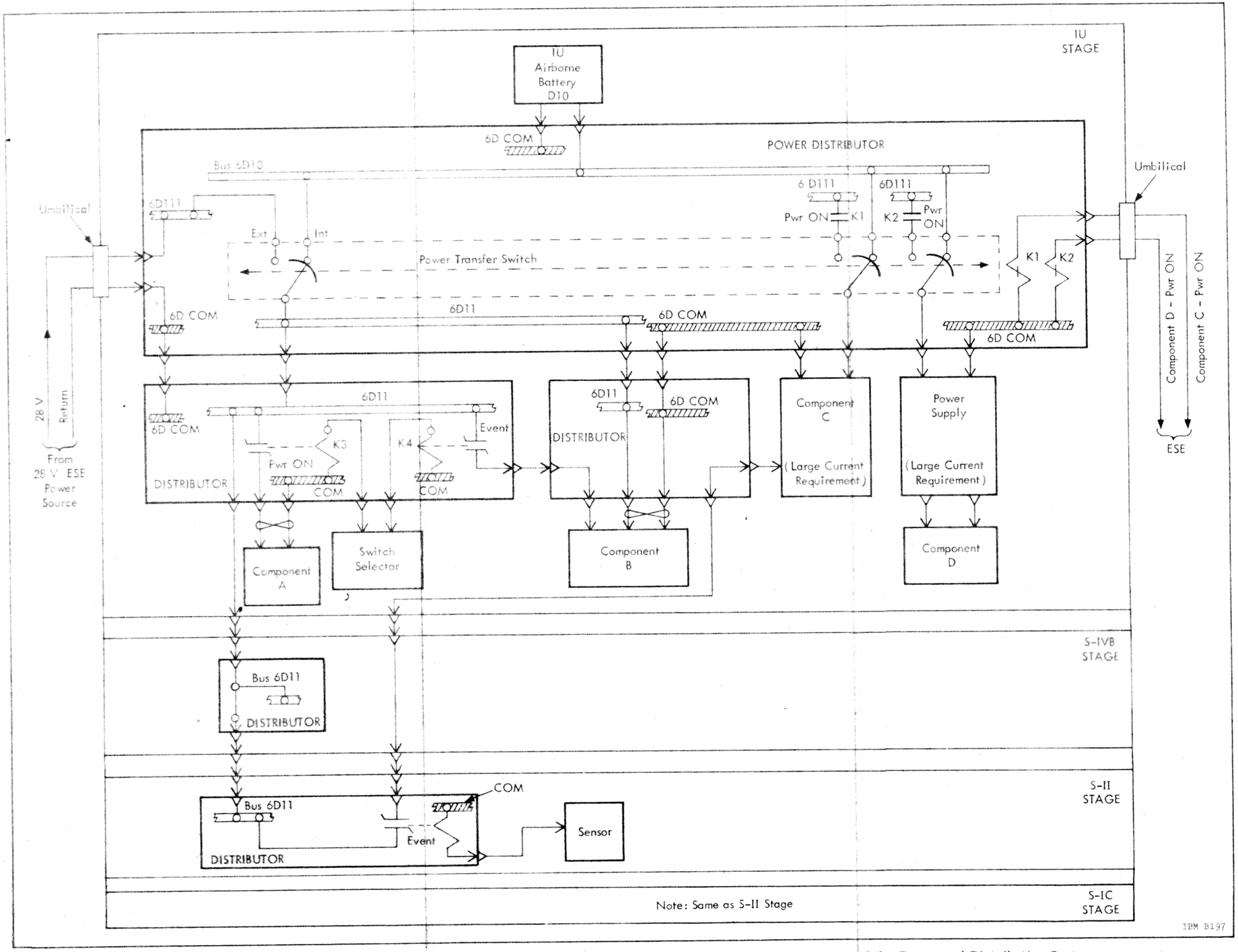

Figure 8.1-2 Partial Schematic of the Power and Distribution Systems

SECTION 8.2

IU POWER AND DISTRIBUTION SYSTEMS

The following paragraphs discuss the power supplies and distribution system within the IU of the vehicle. The operation of the other stages is somewhat similar to that of the IU, and detailed discussions of these stages will not be presented.

8.2.1 POWER SYSTEM

The IU power components may be divided into 3 groups:

- Primary 28 Vdc power sources (internal and external)
- Stabilized Platform system power
- Measuring and telemetry system power

PRIMARY POWER SOURCES

The total IU power requirements vary according to mission assignment. The initial Saturn V Vehicles will use four IU batteries. As the vehicle load requirements decrease, 3 batteries will normally be used.

As stated in Section 8.1, each stage is equipped with a power transfer switch which is used to select either an internal or an external power source. During normal checkout operations, power from the ESE will be used in place of the vehicle batteries. A discription of the batteries will be found in Section 8.3.

Approximately 30 seconds prior to lift-off, a power transfer sequence (to internal power) is initiated. This action is accomplished by the power transfer switch which is similar to the switch illustrated in Figure 8.2-1.

To switch to internal or external power, an ESE command (28 Vdc) is sent to one of the drive-motor field coils. The motor switches the make-before-break contacts to the desired position. The switch will remain in that position until another ESE command is generated.

During prelaunch testing, the power transfer switch will be actuated several times. Figure 8.2-2 illustrates how the ESE generated power is used to simulate the airborne battery. As shown in the figure, the primary 28 Vdc (external) power is normally routed through an umbilical to the IU Power Distributor. The battery simulator shunts the internal and external buses in the Power Distributor to provide power to both input contacts of the transfer switch. During an umbilical plug drop test, a test cable is used to maintain continuity when the umbilical circuit is opened.

STABILIZED PLATFORM SYSTEM POWER

The Stabilized Platform system requires several unique voltages. These are provided by the ST-124-M Platform AC Power Supply and the 56 Volt Power Supply. See Figure 8.2-3. The AC Power Supply is defined as a part of the Stabilized Platform system and is presented in Chapter 14. Details of the 56 Volt Power Supply are contained in Section 8.4.

MEASURING AND TELEMETRY SYSTEM POWER

The measuring and telemetry system requires special excitation and reference voltages for transducers and signal conditioning equipment. The power flow for this system is shown on Figure 8.2-4.

The 5 Volt Measuring Voltage Supply generates a highly regulated 5 Vdc output for use as a signal conditioning reference voltage and as excitation for some transducers. Transducer excitation voltages, other than the 5 Vdc supplied by the Measuring Voltage Supply, are generated in the Measuring Racks.

8.2.2 IU DISTRIBUTION SYSTEM

The IU distribution system provides the following:

- Power switching to large loads
- Power switching to medium loads
- Switching of low-power logic signals
- Proper interconnection of all electrical equipment

The Power Distributor performs the required switching of high-current loads. Medium-current load switching is accomplished by the Control Distributor and two Auxiliary Distributors. The large number of unique requirements presented by the emergency detection and instrumentation systems necessitates separate distributors for each of these systems. The remainder of the logic switching is performed by the Control Distributor and, to a limited extent, by the two Auxiliary Distributors.

The placement of the Control, EDS, and Auxiliary Power Distributors is illustrated in Figure 8.2-5. In general, components which require high-current switching are mounted near the Power Distributor, nd components requiring numerous logic switching are located near the Control Distributor. The distributor mounting, relative to other components, provides for a minimum amount of cabling.

Certain hardware configuration problems arise where it is impractical to alter or redesign existing components just to provide correct signal routing. In cases such as this, a device called a Plug-type J-box is used. The J-box is a standard plug used as an adapter.

Redundancies in circuit design provide an increase in vehicle reliability. Certain components receive primary power from three separate batteries as a precaution against a primary power failure.

Measuring Distributors route the numerous airborne measurements to their respective destinations. A measurement originates in a transducer or within another component and is routed either directly to the telemetry system or indirectly through a Measuring Rack signal conditioning module and a Measuring Distributor.

The large number of telemetry signals and numerous configuration changes require several Measuring Racks. The signal conditioning modules within the Measuring Racks, condition measurement signals to adapt them to the electrical input requirements of the telemetry systems. Measuring Racks output signals are routed to the Measuring Distributors. The Measuring Distributors provide the routing, voltage division, and current-limiting networks to ensure compatability between the measuring and telemetry systems. Through their switching capabilities, the Measuring Distributors can change the selection of measurements monitored by the telemetry system. The switching function transfers certain measurements to channels which had been allotted to expended functions. If it were not for this switching, these channels would normally be "wasted" for the remainder of the flight. The Measuring Distributor also provides the option of using rf link or PCM (DDAS) coaxial cable transmission during checkout operations for a more thorough and comprehensive system test evaluation.

The EDS Distributor contains the relay logic needed to monitor and interpret emergency indications and to issue the appropriate commands. Since the EDS Distributor is an integral part of the EDS, a more thorough description will follow in Chapter 9, Emergency Detection System.

8.2.3 IU GROUNDING SYSTEM

IN-FLIGHT ELECTRICAL GROUNDING

All Instrument Unit grounding is referenced to the outer skin of the stage. The methods used to accomplish IU grounding are illustrated in Figure 8.2-6. Each area will be described separately.

Power System Grounding. The power system is grounded by means of hardwires routed from the 6D COM bus in the Power Distributor to the 601E1 ground stud attached to the stage skin. This connection provides the single-point ground for the power system. All 6D COM buses in the various distributors are wired back to the 6D COM bus in the Power Distributor. The common buses, for the most part, are isolated from the chassis of the components in which they are enclosed. Isolating power supplies are utilized in some instances to accomplish this. The close proximity of the Power Distributor, batteries, and outer skin power ground termination point (601E1) assures that a relatively low potential difference will be developed by their respective ground levels.

Electrical or Black Box Grounding. Grounding of individual boxes and components is accomplished by direct metal-to-metal contact of the black box and cold plate or stage skin. All common return lines are isolated from the component chassis except in a

very few instances (e.g., some parts of the telemetry system).

Shield Grounds Internal to Black Boxes. Internal shields are connected directly to black box chassis where they are referenced to stage skin by means of metal-to-metal contact.

Shield Grounds for Cabling System. Cable Shields are grounded by 2 methods. They are as follows:

- Most shields are connected to the 6D COM bus in one of the distributors. This is accomplished by extending the shield through the last small contact of the distributor connector where it is routed to the 6D COM bus. Where several cables are connected in series, the cable shields are routed through the last small contact of the interconnecting connector. This method is used in order to keep the cable shielding continuous from the black boxes through each interconnecting cable to the distributor.

- When the shielded cables are routed between two black boxes and do not terminate at a distributor, a second method of terminating cable shielding must be utilized. In this case, only one end of the shield is grounded. The shield is routed through the last small connector contact on one of the components and terminated at the chassis. The black box chassis is grounded normally (as outlined earlier). Where several shielded cables are connected in series from black box to black box, the cable shield is made continuous by routing the shield through the last small contact of the interconnecting connectors.

RF Grounding. RF grounding of components is effected by means of metal to metal grounding. Refer to the paragraph on electrical or black box grounding. RF connectors and cables are grounded through the shell of the connector to the black box.

PRELAUNCH GROUNDING

The IU and ESE common systems are referenced to earth ground prior to launch. Shortly after engine ignition, the umbilicals are ejected. To assure the IU remains at earth potential until all umbilicals are ejected, two single-wire grounding cables are connected to the IU. They are the final conductors to be disconnected from the IU Stage. One of these cables is connected to the ESE 6D COM bus. This cable is routed through a single-conductor connector located below the umbilical plate and is terminated at

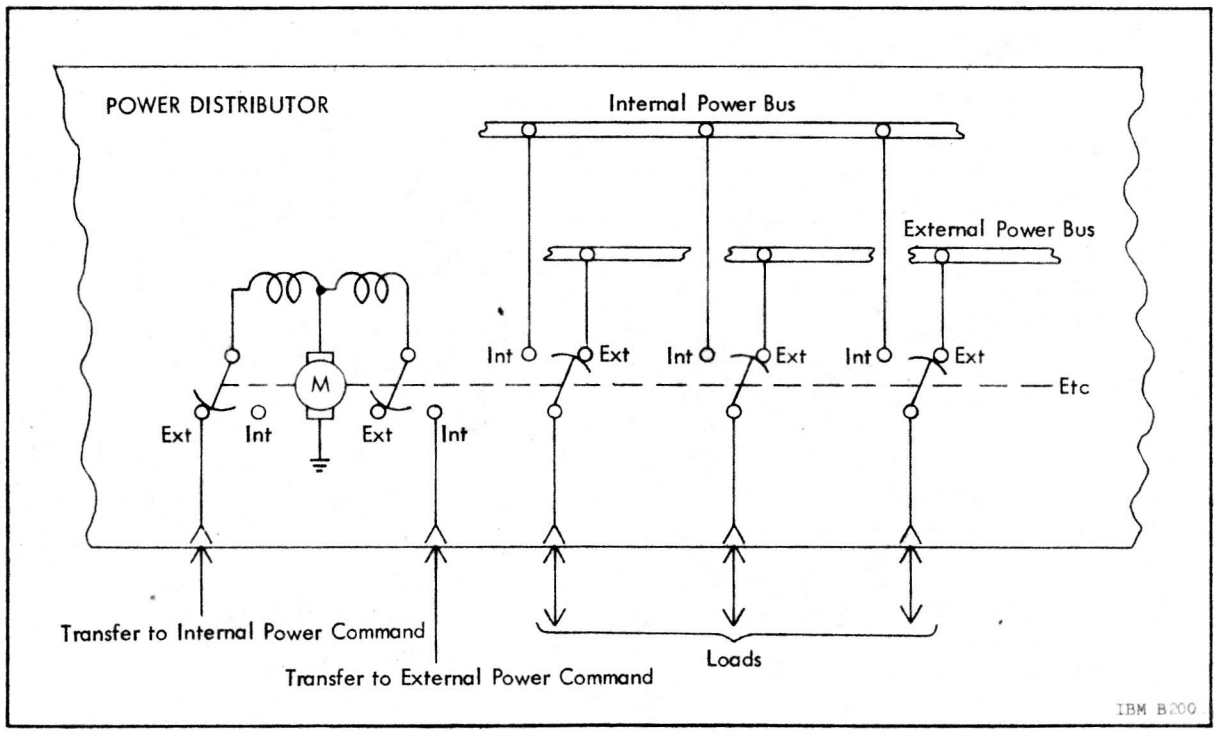

Figure 8.2-1 Partial Schematic of the IU Power Transfer Switch

stage single-point ground terminal, 601E1. Cables routed from the ESE across the swing arms to the stage umbilical have an overall RF shield to avoid induced signals from local tracking antennas. These shields are terminated by a second single-conductor cable which is routed from the ESE side of the umbilical through a one-pin connector to stage skin terminal 601E2. This connector is also located below the umbilical plate.

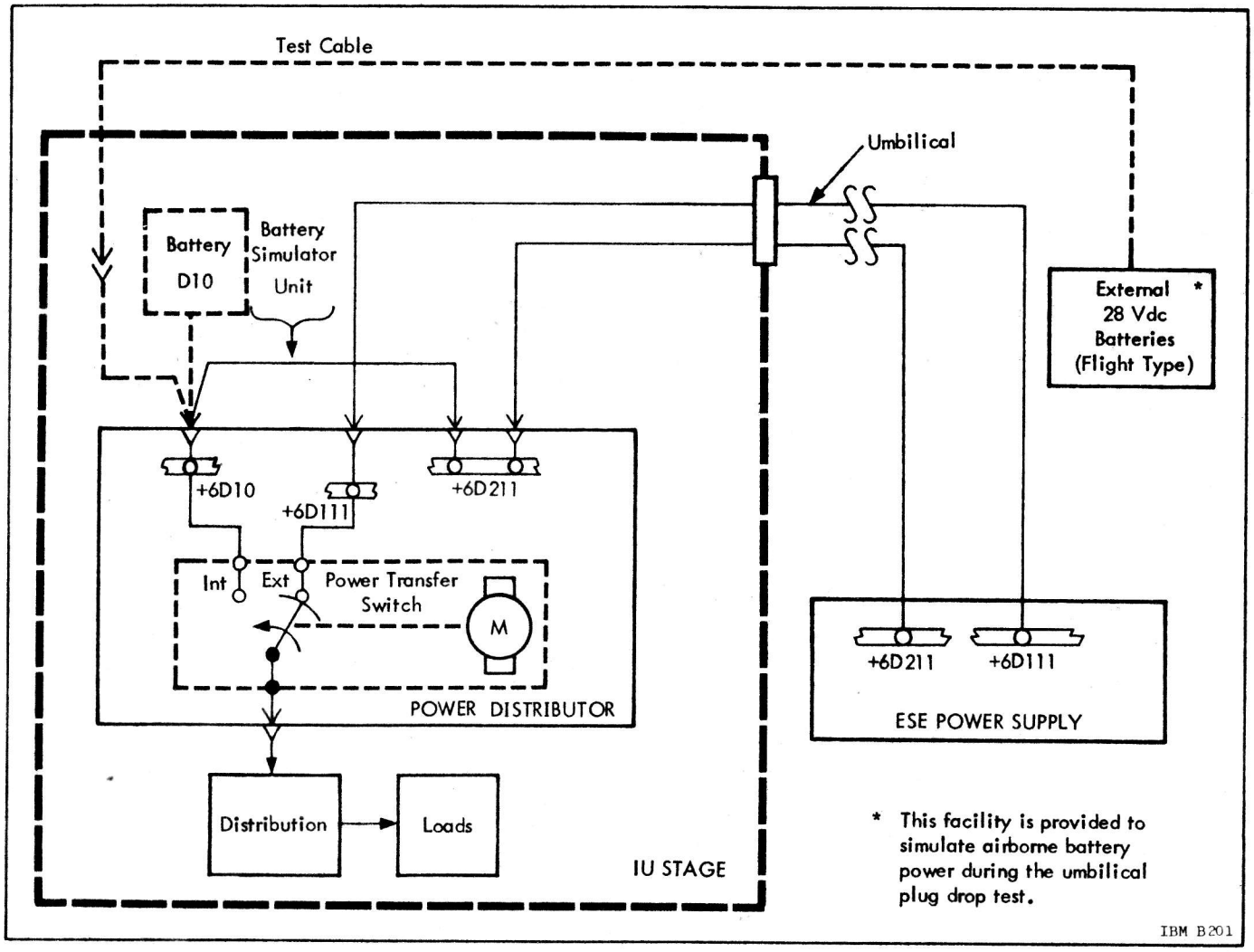

Figure 8.2-2 Ground Checkout Configuration of IU Power Derivation

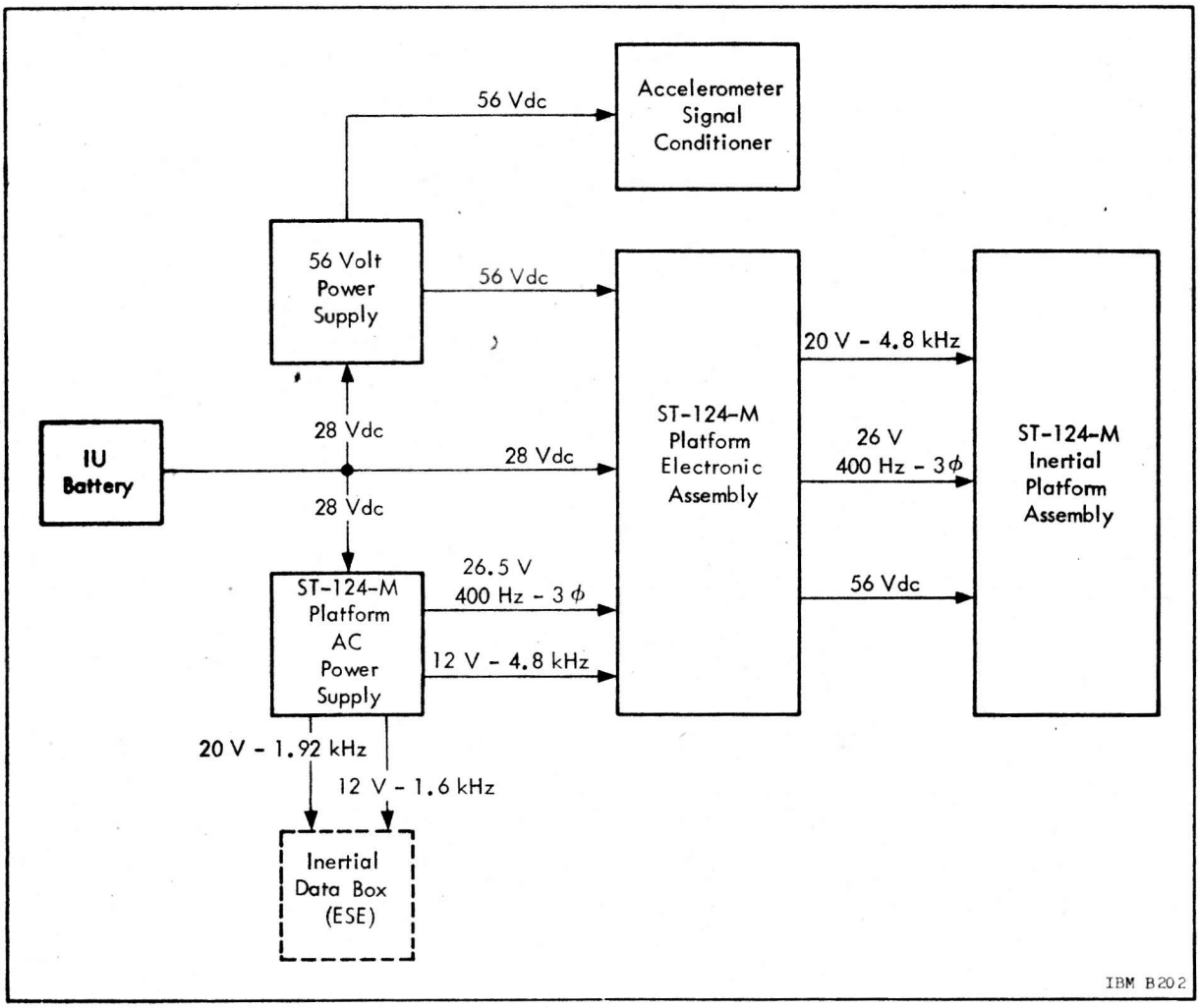

Figure 8.2-3 Stabilized Platform System Power Distribution

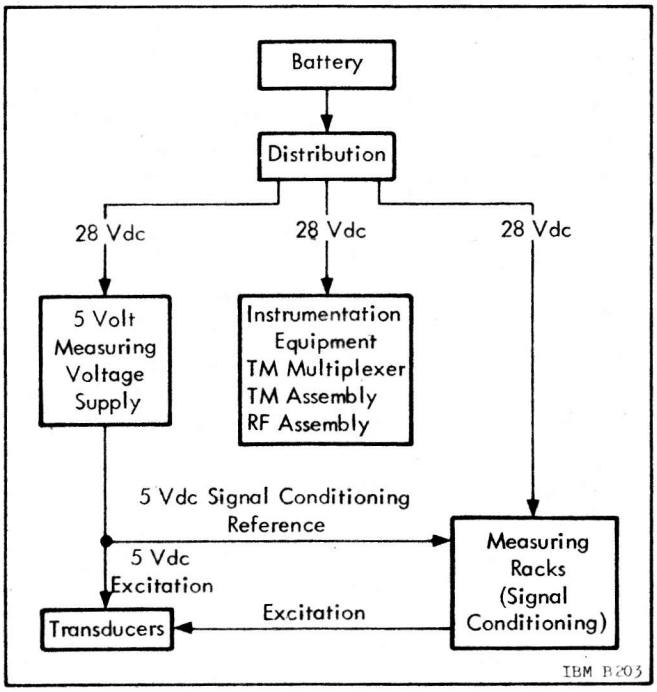

Figure 8.2-4 Measuring and Telemetry System Power Distribution

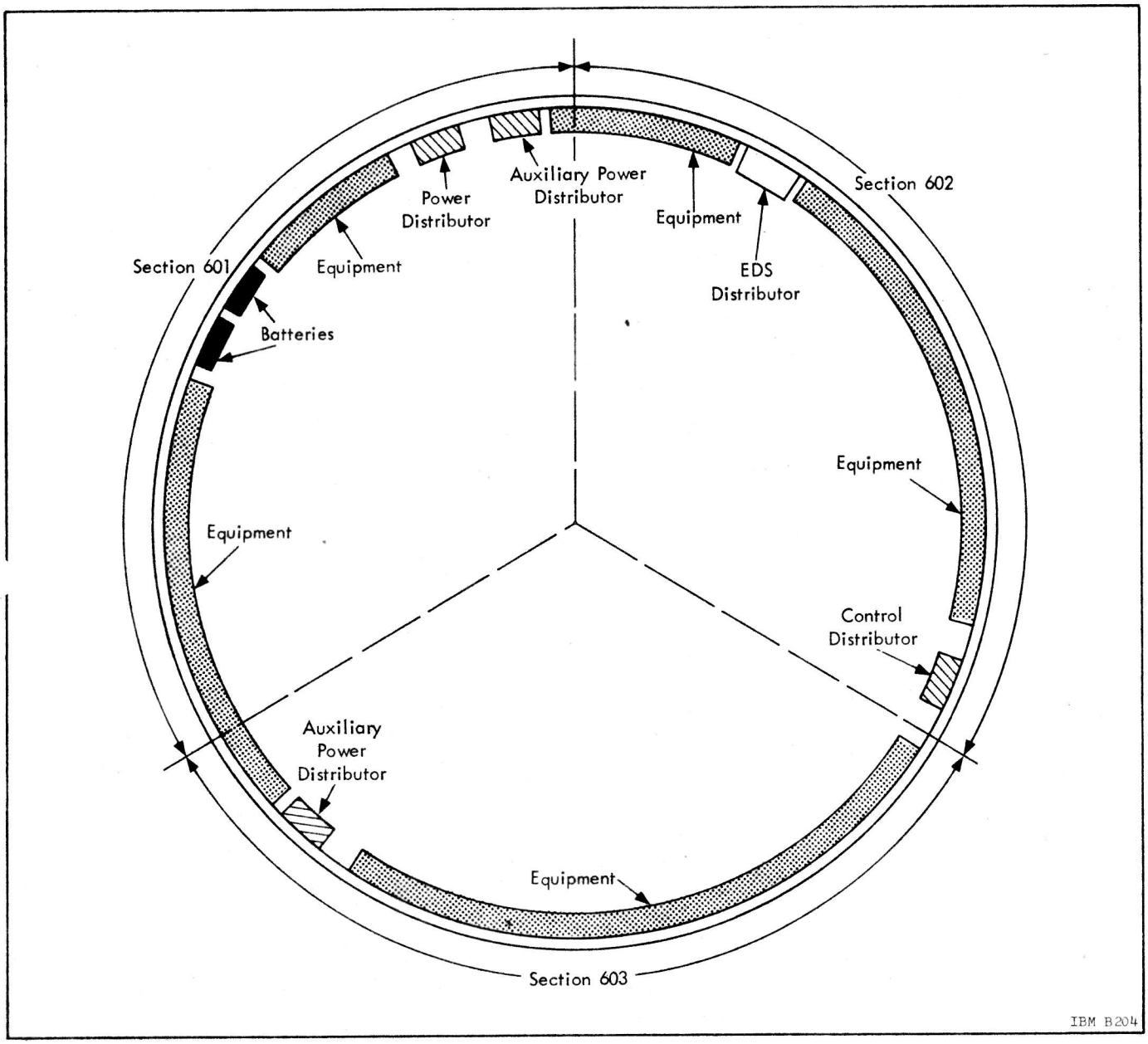

Figure 8.2-5 IU Distribution Equipment Layout

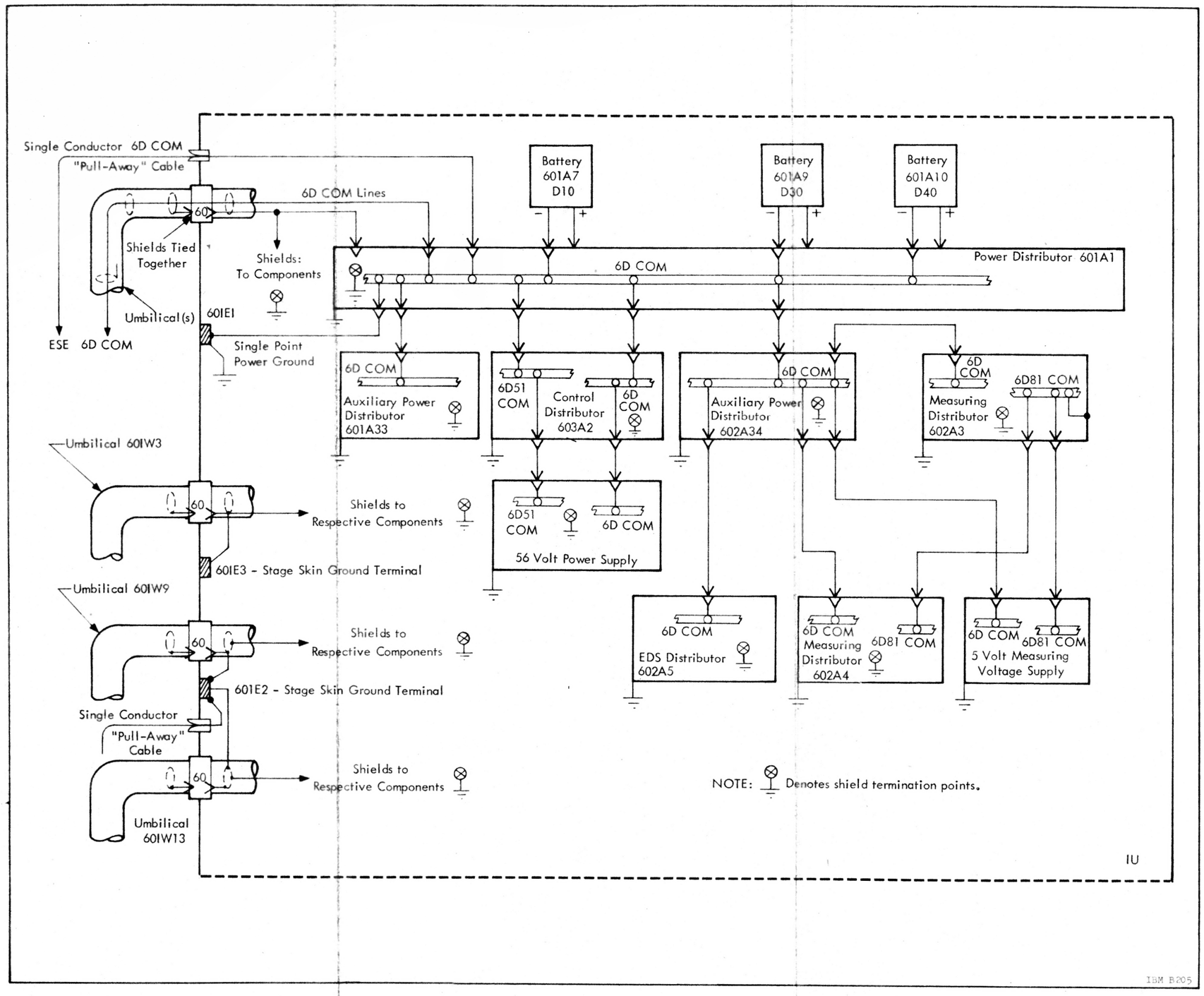

Figure 8.2-6.
IU Grounding System for Saturn IB and V Vehicles

SECTION 8.3

BATTERIES

Three or more 28 Vdc batteries are used in the IU as the primary power source for all electrical components. Each power source is a dry-charged, alkaline silver-zinc, primary battery. Figure 8.3-1 is a photgraph of a typical IU battery. During launch countdown, droxide (KOH) electrolyte.

A primary battery contains 20 series-connected cells, each producing a nominal 1.5 volts. Occasionally, the full 20-cell output voltage may not be required by the IU circuitry. In such cases, 18 or 19 cells may be selected by varying the wiring configuration of the cell selector receptacle.

To prevent an excessive internal pressure buildup, a relief valve is provided. The valve vents internal pressures in excess of 69,000 N/meter^2 g (10 psig).

Table 8.3-1 summarizes the major IU battery characteristics.

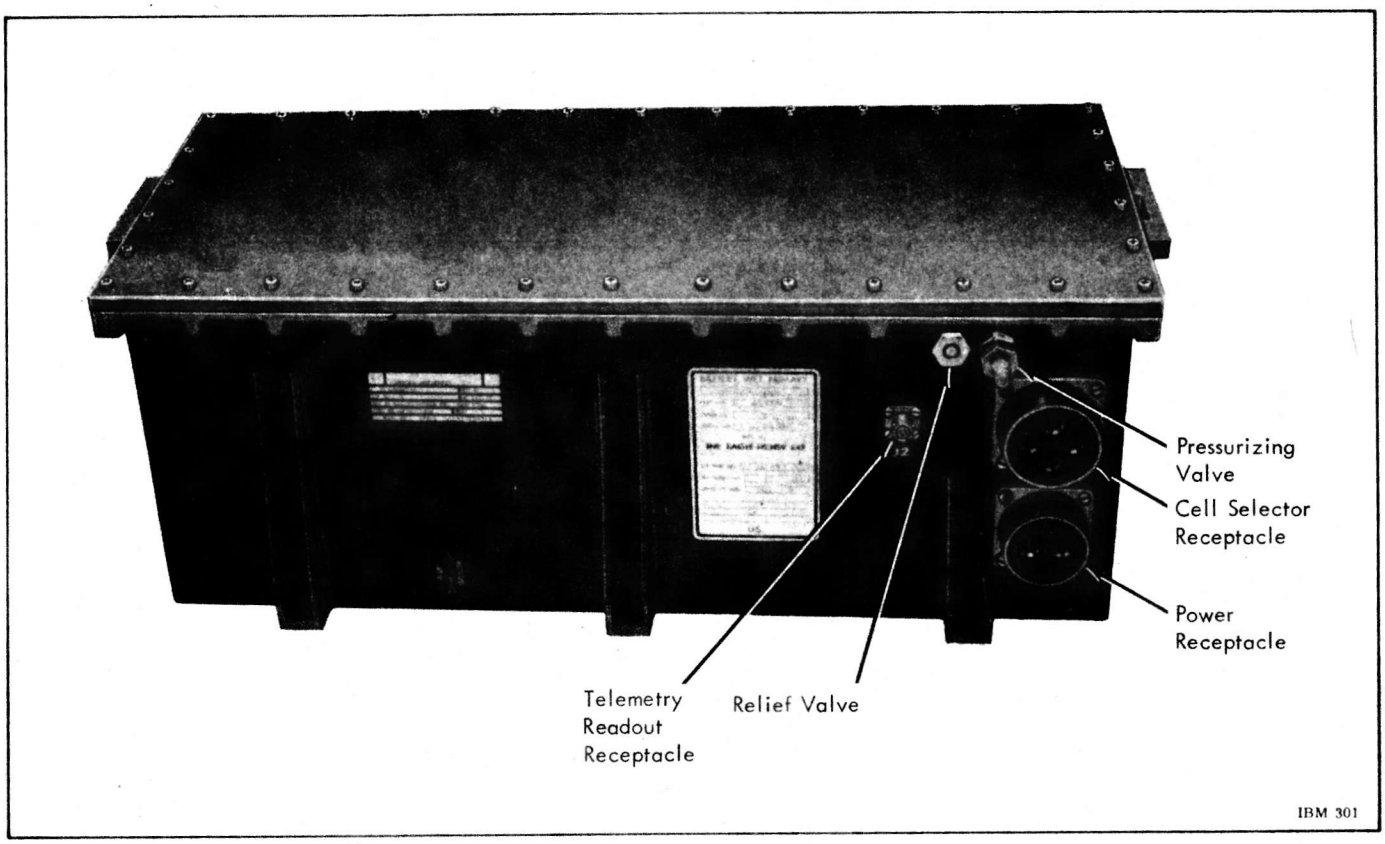

Figure 8.3-1 Instrument Unit Battery

Table 8.3-1 IU Battery Characteristics

Battery Type	MAP 4240 - Dry charged
Cells	
Number	20 (with provisions for selecting 18 or 19 cells if required)
Nominal voltage per cell	1.5 Vdc
Material	Alkaline silver-zinc
Electrolyte	Potassium hydroxide (KOH)
Output	
Voltage	+28 ± 2 Vdc
Current	35 amperes for a 10-hour load period (if used within 120 hours after activation)
Measurements available	Current output Internal temperature
Cooling System	Cold plate
Ambient Temperature Range	+10°C to +48.9°C (+50°F to +120°F) for proper operation
Heat Transfer Characteristics	
Dissipation	0.07 W/cm^2 (0.47 W/in.^{2})
Surface area	2074 cm^2 (321.4 in.^{2})
Total dissipation	150 watts
Physical Characteristics	
Activated weight	75 kg (165 pounds)
Dimensions	
Length	64 cm (25.4 in.)
Width	29 cm (11.44 in.)
Depth	23 cm (9.16 in.)

SECTION 8.4

56 VOLT POWER SUPPLY

The 56 Volt Power Supply furnishes power required by the ST-124-M Platform Electronic Assembly, and the Accelerometer Signal Conditioner on board Saturn space vehicles.

The 56 Volt Power Supply consists of an input filter, a saturating core square wave oscillator, pulse width modulator, saturated mode switching driver, saturated mode switching power amplifier, a full wave rectifier and adder, an output filter, and a reference bridge, see Figure 8.4-1. Unregulated 28 Vdc power from the primary power supply batteries is applied to the input. The unregulated 28 Vdc power is filtered and fed to the collectors of the transistors contained in the saturating core square wave oscillator, saturated mode switching driver, and saturated mode switching power amplifier.

A 2-kilohertz square wave is developed by the saturating core oscillator and is transformer coupled to the pulse width modulator stage. It is then applied to the driver and the power amplifier stage, after which it is rectified and filtered. The final output of the 56 Volt Power Supply is applied to a reference bridge. The reference bridge is capable of sensing an increase or decrease at the output of the power supply. Sensing a change of output, the reference bridge passes this change to the pulse width modulator which will increase or decrease the input to the switching driver.

A summary of performance characteristics of the power supply is presented in Table 8.4-1.

Table 8.4-1 56 Volt Power Supply Characteristics

ELECTRICAL CHARACTERISTICS	
Input Voltage	24 to 32 Vdc
Output Voltage	
0 to 1 A load	56 ± 0.5 Vdc
1 to 8 A load	56 ± 2.5 Vdc
8 to 10 A load	56 ± 3.5 Vdc
Output Load	
Normal	1.0 A
Peak	6.0 A
Output Ripple	
0 to 5 A load	0.25 Vp-p (max)
Adjustability with 1 A load	56 ± 0.5 Vdc
Efficiency	65 percent
Operating Temperature Range	0 °C to 50 °C (32 °F to 122 °F)
PHYSICAL CHARACTERISTICS	
Weight (max)	4.3 kg (9.5 pounds)
Dimensions	
Length (max)	24.6 cm (9.7 in.)
Width (max)	16.8 cm (6.6 in.)
Depth (max)	10.8 cm (4.2 in.)

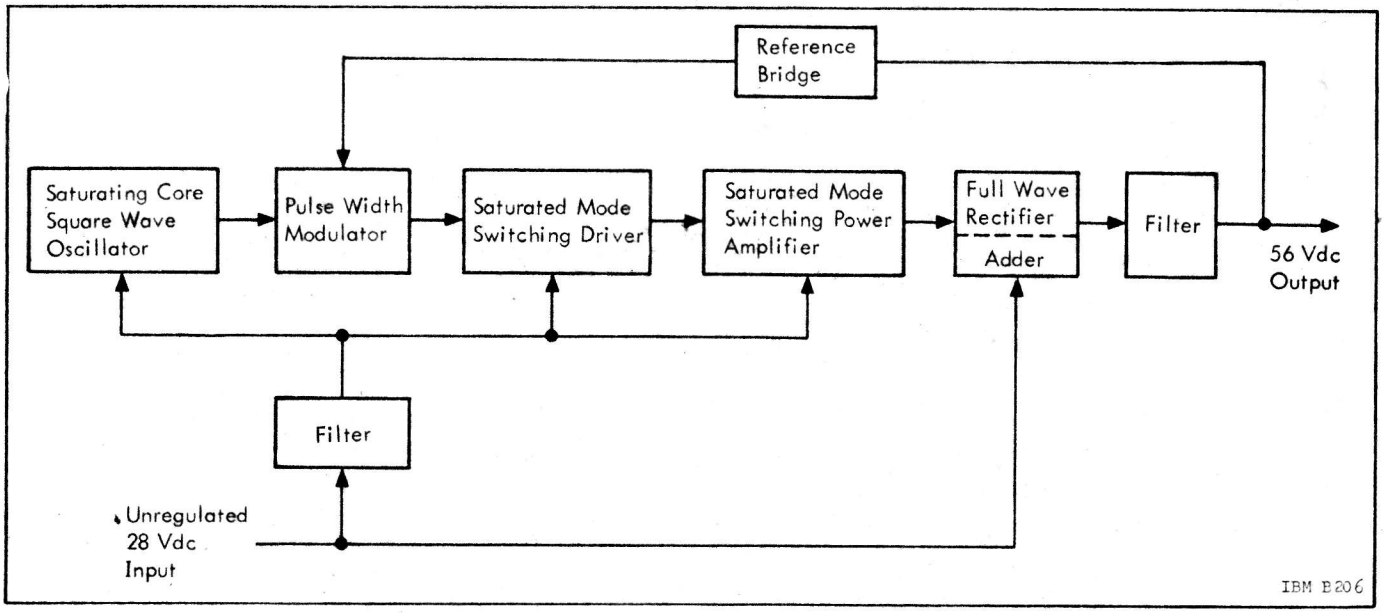

Figure 8.4-1 56 Volt Power Supply Block Diagram

SECTION 8.5

5 VOLT MEASURING VOLTAGE SUPPLY

The 5 Volt Measuring Voltage Supply provides excitation voltage for the various temperature, pressure, and engine position transducers within the IU instrumentation system. The measuring supply is also used to provide a reference voltage for inflight calibration of certain telemetry channels.

The power supply consists of the following major elements:

- Input filter-regulator circuit
- DC-to-DC converter circuit
- Output regulator-filter circuit

Figure 8.5-1 is a block diagram of the 5 Volt Measuring Voltage Supply. Unregulated 28 Vdc is applied to the input filter-regulator circuit. In this circuit, the 28 Vdc source voltage is filtered and line variations are removed. The output of the regulator is compared to a constant reference voltage and the resulting error voltage is applied to an amplifier which varies the duty cycle of a transistor switch. The output of the transistor switch is a square wave whose period is a function of the error voltage detected in the comparator. A filter circuit follows the switch to provide an average value of the output. The output of the input filter-regulator circuit is applied to the square wave oscillator portion of the dc-to-dc converter. The square wave oscillator output voltage is reduced in the stepdown transformer and is rectified and filtered prior to being applied to the output regulator-filter circuit. Output regulation is accomplished by varying conduction through the series regulator (control element). The conduction of this transistor is controlled by the magnitude of the error voltage sensed by the comparator.

An overload protection circuit is provided to limit the series regulator current to a safe level in the event of an overload at the output.

The characteristics of the 5 Volt Measuring Voltage Supply are presented in Table 8.5-1.

Table 8.5-1 5 Volt Measuring Voltage Supply Characteristics

ELECTRICAL CHARACTERISTICS	
Input	
Voltage	24 to 32 Vdc
Current (max)	0.6 A
Power (max)	14.4 W
Output	
Voltage (with 0-1A output)	5.000 ±0.005 Vdc
Range of output adjustment (with 0-1A output)	±0.050 Vdc
Current	0 to 1A
Power (with 0-1A output	5W
PHYSICAL CHARACTERISTICS	
Weight	1.1 kg (2.5 pounds)
Dimensions	
Length	12.2 cm (4.8 in.)
Width	12.6 cm (4.9 in.)
Depth	5.1 cm (2.0 in.)
Cooling	Cold plate
Heat transfer surface area	14.6 cm^2 (22.1 $in.^2$)
Heat transfer of mounting area	0.05 W/cm^2 (0.32 $W/in.^2$)

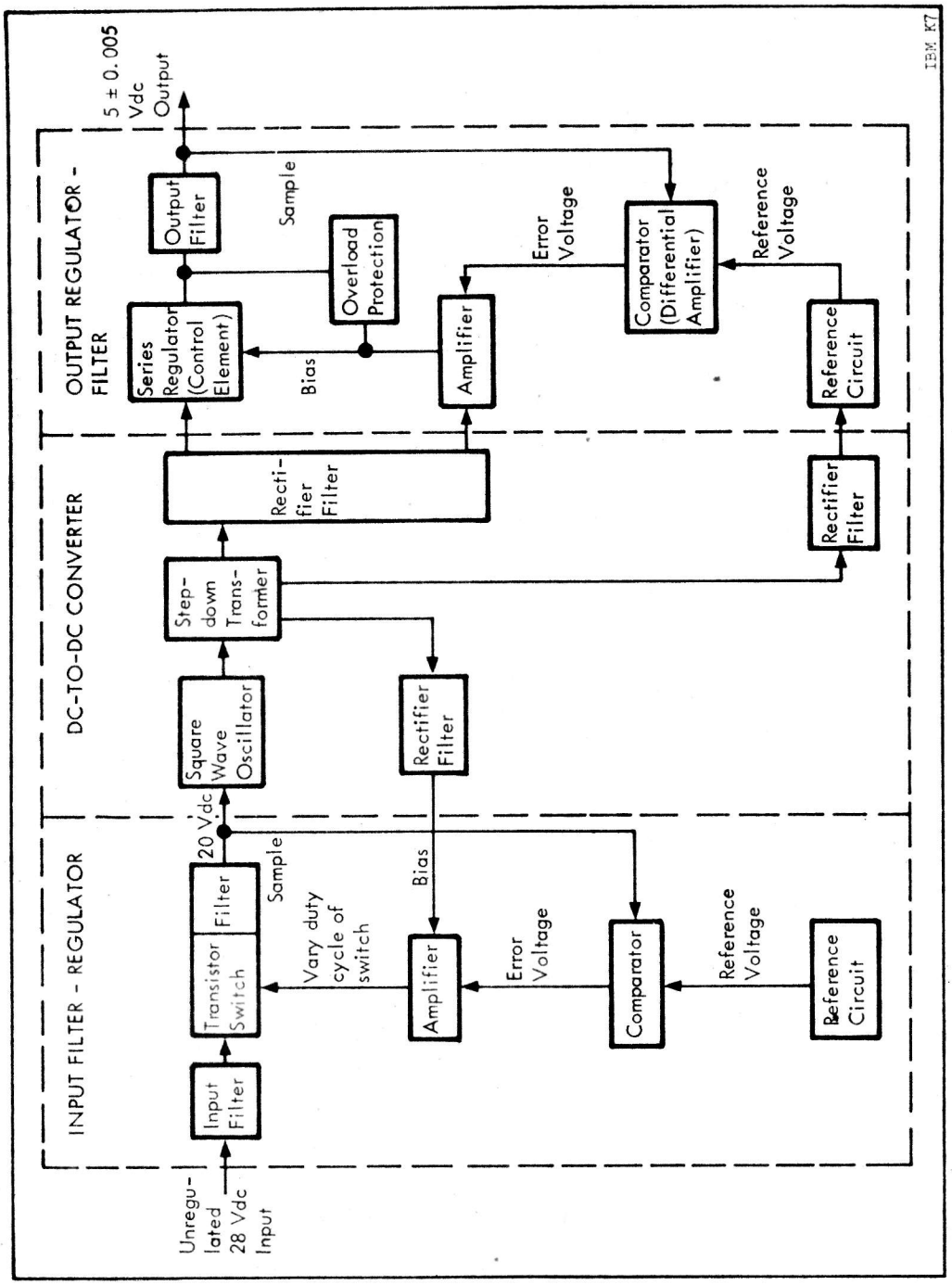

Figure 8.5-1 5 Volt Measuring Voltage Supply Block Diagram

CHAPTER 9
EMERGENCY DETECTION SYSTEM

SECTION 9.1
CREW SAFETY SYSTEM

An Emergency Detection System (EDS) detects malfunctions in the launch vehicle which lead to emergency situations. The EDS is one part of the crew safety system. The other part of the crew safety system is the launch escape system which removes the flight crew from the vicinity of the malfunctioning vehicle. Essentially, there are two kinds of emergency situations: explosion of the vehicle propellants and breakup of the vehicle by aerodynamic forces.

The crew safety system for Apollo/Saturn Vehicles is semiautomatic. The system can sense failure modes that slowly lead to catastrophic conditions and can indicate these failures on a display panel for the flight crew to allow them to make the abort decision.

The system can also automatically initiate an abort when it senses a failure mode that will lead to a rapid vehicle breakup. Studies of many failure modes have shown that despite the tremendous mass and inertia of the Saturn Vehicles, the time from occurrence of a malfunction until the vehicle reaches a "breakup" angle of attack can be very short. Therefore, a fast responding automatic capability must be included in the crew safety system.

The Saturn V crew safety system is very similar to the Saturn IB system but has 3 stages to monitor. Because of increased loading, the system must also monitor propellant tank pressures in the S-II and S-IVB Stages.

9.1.1 GUIDELINES FOR CREW SAFETY

The EDS must be as simple as possible because of space and weight limitations of flight hardware and because any detection equipment has a possibility of malfunctioning and causing the abort of an otherwise successful mission. For this reason, the number of sensors in the EDS must be kept to a minimum. This decrees that the effect of a malfunction is sensed rather than the malfunction itself. As an example, the EDS can be simplified by monitoring the angle of attack and attitude rates of the vehicle rather than the position of each engine actuator. (Engine actuator failures lead to loss of control and eventual vehicle breakup because of an excessive angle of attack.) Since other vehicle failures lead to this same effect (excessive angle of attack and/or attitude rates), the monitoring of failure effects yields a considerable simplification of the crew safety system. This method of simplification is possible only when the time between failure sensing and catastrophic vehicle loss is enough to allow a safe escape distance from the vehicle.

An important guideline used in the development of the Apollo/Saturn crew safety system is that, whenever enough time is available, the decision to abort will be left to the flight crew rather than be automatically initiated. It is felt that no matter how reliable the automatic abort system is made, it can never replace the logic, judgement, and observation powers of the flight crew. However, many of the failure modes of the vehicle do not allow sufficient time for the flight crew to make a decision and react to the emergency; in these cases, the crew must rely on the automatic abort system.

Since a falsely initiated abort could ruin an otherwise successful mission, the EDS has been designed to reduce the probability of a false automatic abort to an insignificant level. It is extremely important that the crew safety system does not degrade the mission success probability.

Table 9.1-1 shows some of the more important design guidelines.

9.1.2 FAILURE ANALYSIS

The design of the EDS is based on failure mode and effect analysis. This is a complete analysis of each stage, system, subsystem,

Table 9.1-1 Important Guidelines for the Crew Safety System for Saturn Apollo Vehicles

Simplicity	- Use minimum number of sensors and sense effect of failure rather than cause — when time permits.
Abort Decision	- Made by flight crew whenever time permits — manual rather than automatic.
Mission Degradation	- Probability of false automatic abort reduced to insignificant level.

- Initiation of manual abort will be based on at least two separate and distinct indications.
- In the event of conflicting information from the onboard crew safety system and telemetered data relayed to the Spacecraft from the ground, the onboard information shall always take precedence.
- Triple redundant electrical circuits utilizing majority voting logic will be used for all automatic abort signals.
- As a design objective, redundant circuitry will be used for manual abort indications from the Saturn Launch Vehicle to the Spacecraft.
- It shall be a design objective that no single point electrical failure in the onboard crew safety system will result in an abort.

nd component within the vehicle to determine which component failure modes can cause a failure of the subsystem, which subsystem failures can cause failure of the system, and which system losses can cause loss of the stage and/or vehicle. A failure mode and effect analysis begins at the component level and investigates each possible way in which the component can fail (i.e., open, short, rupture, leak). The effect of the particular failure is analyzed on higher levels of assembly until the effect of that particular component failure on the space vehicle is determined.

Once the failure analysis of a component is completed, a criticality number is assigned to the component. For example, a number 10 indicates that this component can be expected to cause a vehicle loss about 10 times out of 1 million flights.

After the criticality number has been derived for each component, the numbers are summarized for each subsystem, system, and stage of the vehicle— vehicle dynamics must be analyzed and structural limits determined. For example, a failure mode and effect analysis shows that a particular group of control component failures can cause the engines to gimbal "hardover"; this would mean vehicle loss and a ticality number could be derived to show the expected frequency of this failure.

The criticality numbers are summarized on a summary chart which is referred to as a "failure tree". Figure 9.1-1 represents the latest failure tree summary of the IU Astrionics system of the Saturn IB Vehicle. In this figure, the failure is traced back only 3 or 4 levels and does not reach the component mode in most cases.

Beyond this analysis of failures, the length of time between the occurrence of the failure and the time of reaching the critical angle of attack must be known. This is a function of the time of flight. If the failure occurs about maximum Q, we may have the worst case condition and less time is available between the occurrence of the failure and structural breakup of the vehicle. To determine these limits, the structural limit curves must be drawn for each type of failure (control engines hardover, engines null, engines out, etc.). These curves show the various combinations of vehicle angle of attack and engine gimbal angle at which the structural limits of the vehicle are exceeded, as a function of time of flight. As an example of these curves, refer to Figure 9.3-1. Curves must also be drawn of the actual expected excursions of vehicle angle of attack and engine gimbal angle during each of these vehicle failure modes. The two sets of curves must then be analyzed to determine whether (and at what time)

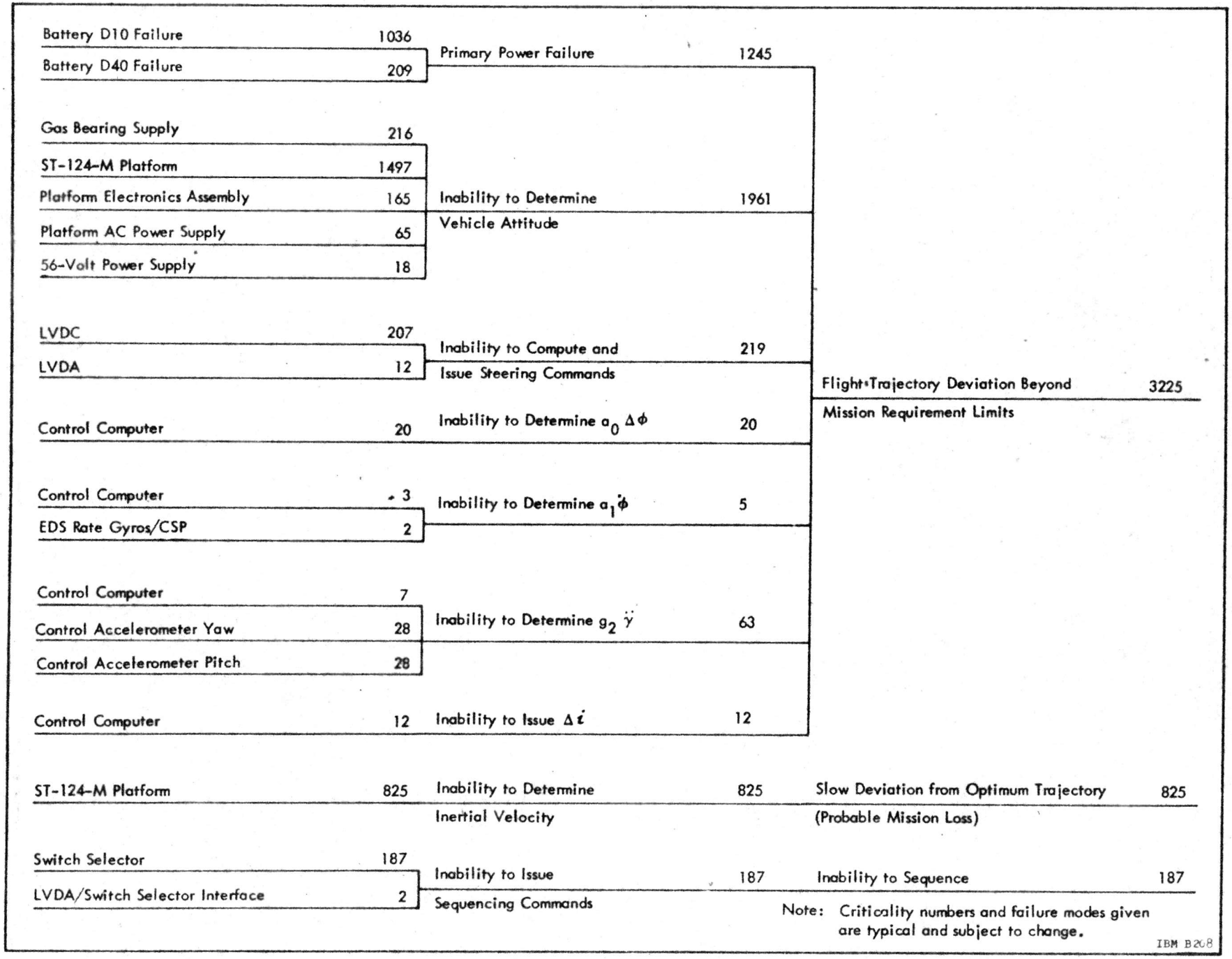

Figure 9.1-1 Saturn IB IU Astrionics System Failure Modes

the structural limits of the vehicle will be exceeded for each particular failure condition.

From the information on the effect of these failures and the information on the vehicle dynamics or structural limits, the time available between occurrence of the failure and catastrophic loss of the vehicle can be derived. This time will indicate the response time required of the detection mechanism. The time will determine whether the crew has sufficient time to recognize the emergency warning and make a decision as to when to abort. If human response would be too slow, the abort or escape must be automatically initiated. A range of safe limits is assigned to each parameter selected for monitoring. Performance within these limits assumes the parameter to be functioning normally. Generally, the selected parameter could have a range of acceptable tolerance bounded by both an upper and lower level of safety (e.g., over pressure and under pressure in a pressurized tank). However, in some conditions only one safety limit is needed (e.g., high angles of attack). As long as conditions of the measured parameter stay within the safety zone, it is assumed that all components are operating satisfactorily. If the measured value approaches the danger level, a catastrophic failure is imminent.

The problem is to decide at what level to place the abort level. If the abort level is placed too close to the tolerance limit, an abort might be needlessly triggered. If, on the other hand, it is moved too close to the danger level (to hedge against a needless abort), there may not be time enough for a safe escape because of various systems delays. The task is often complicated because the danger levels, as well as the tolerance zone, of certain parameters may change as a function of time. Other factors that further complicate the problem are transients which momentarily exceed the danger level but offer no catastrophic threat. These must be taken into account during crew safety systems design.

SECTION 9.2

EMERGENCY DETECTION SYSTEM

The Saturn/Apollo emergency detection system has triple redundant sensors and majority voting logic for all the automatic abort parameters. Dual redundancy is used for most of the manual abort sensors. The redundancy is so arranged that the predominant failure mode of the sensing system has been protected against. The guideline rule of having at least two separate and distinct indications of failure before initiating a manual abort is a protection against any inadvertent aborts from malfunctioning sensor systems. The displays used in the Spacecraft are "fail safe" wherever practical. Where possible, the meters used for display of analog signals are "zero offset". This means that the predominant failure modes of the sensing system (loss of power, etc.) will indicate off scale conditions (either high or low) rather than readings within the scale of interest. The indicator lights used for discrete indications to the flight crew are dual-bulb lights and so arranged that the crew cannot distinguish whether one or both lights are on. A failure of one light will not be noticed by the flight crew. The other failure mode (inadvertent light) is protected against by requiring two separate and distinct indications of failure.

The Saturn IB/V crew safety system is shown in the functional diagrams, Figures 9.2-1 and 9.2-2. Monitored parameters are: stage thrust for both stages, guidance computer status, angular attitude rates, attitude error, and angle of attack for Spacecraft display. Automatic abort is initiated for S-IB and S-IC two-engine-out or for excessive angular rates in pitch, roll, or yaw; these automatic abort limits are switched out either automatically by the flight programmer or manually by the crew according to mission rules. Provision is also made for an abort request light to be energized from the ground control center. At the ground control center, all of the various crew safety system parameters are monitored by using telemetry information from the vehicle. Other telemetered data is available at the MCC so that the flight director can scan all flight critical data and warn the flight crew by voice communication of any impending danger. This facility provides an early warning to the flight crew by giving information on trends of various vehicle parameters, thereby alerting them to certain types of failure indications which may appear on their display panel. The flight crew will not abort on the telemetry information alone but they may use it as backup data for an abort decision.

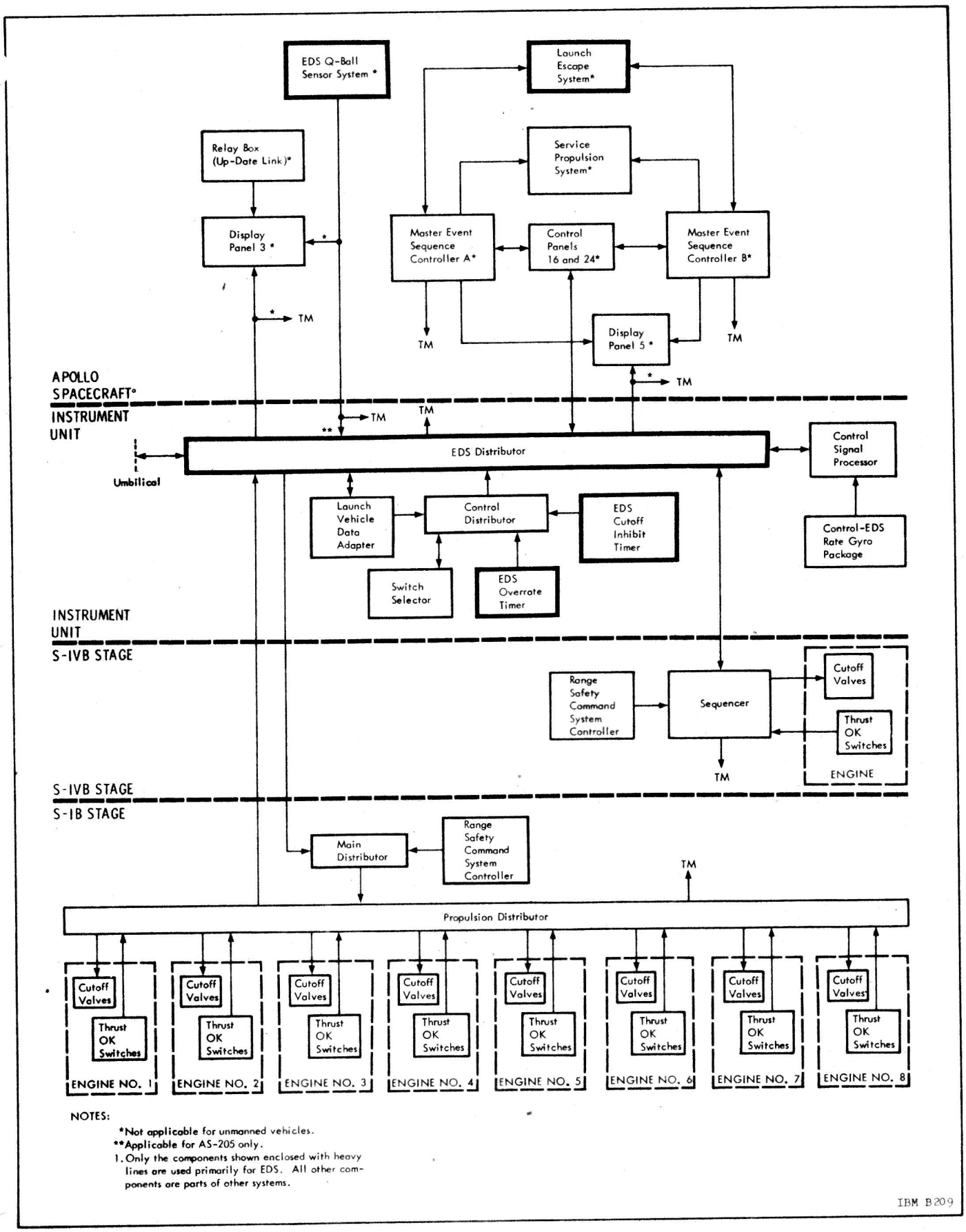

Figure 9.2-1. Crew Safety System (Saturn IB)

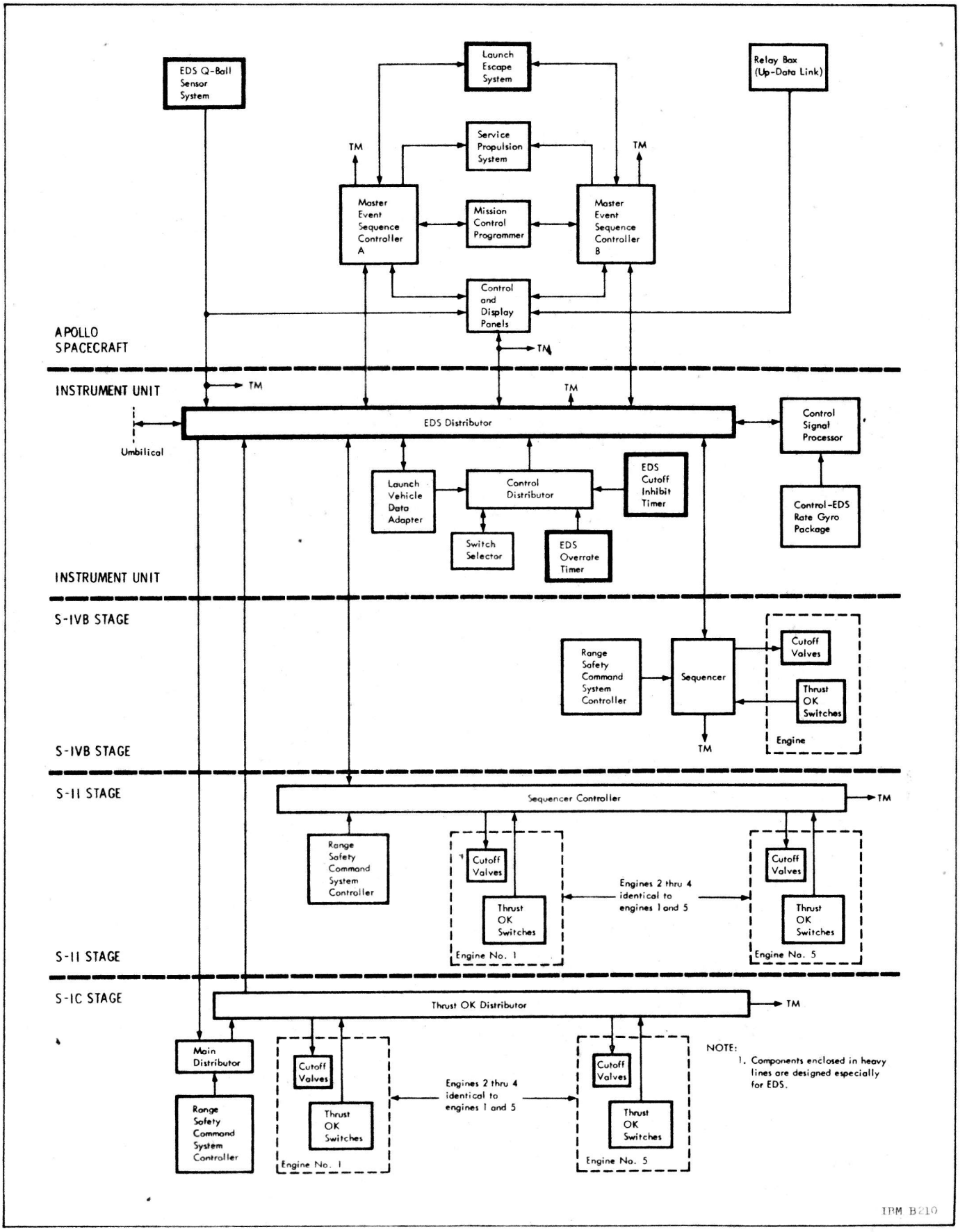

Figure 9.2-2 Crew Safety System (Saturn V)

SECTION 9.3

EDS OPERATION FOR SATURN VEHICLES

9.3.1 GENERAL CONSIDERATIONS

A signal from the Spacecraft to the ground will indicate that no automatic abort signal is active prior to launch release. A signal at lift-off will automatically activate the EDS automatic abort mode. Provisions will also be made to manually interrupt the entire automatic abort signal in the Spacecraft.

An automatic abort signal occurring a preset time after liftoff will initiate: (1) engine shutdown on the active stage and (2) the Spacecraft abort sequence. The preset time is determined by the vehicle mission. If the automatic abort occurs prior to the preset time after liftoff, only the Spacecraft abort sequence will be initiated. Cutoff of the active stage will then be controlled by the Range Safety Officer.

Initiation of a manual abort will be based on at least two separate and distinct indications. These may be a combination of EDS sensor displays, physiological indications, and ground information to the Astronaut. In some cases, the two indications may come from the same parameter, but the indication and sensor systems will be independent.

In the event of conflicting information from the onboard EDS and telemetered data relayed to the Spacecraft from the ground, the onboard information will always take precedence.

Prior to a certain flight time (to be determined by range safety constraints), abort commanded engine shutdown capability will be locked out by provisions in the launch vehicle circuitry.

A signal will be provided to the Spacecraft to energize the abort request indicator light when the range safety officer commands destruct system arming. This command also terminates engine thrust.

Triple redundant electrical circuits utilizing majority voting logic will be used for all automatic abort signals. Redundant circuitry will be used for manual abort indication from the launch vehicle to the Spacecraft. Batteries used for EDS will be electrically isolated from each other. No single-point electrical failure in the onboard EDS will result in an abort.

Provision is made to manually shut down the engines on any stage from the Spacecraft without initiating an abort. A redundant means for accomplishing EDS-commanded engine shutdown is provided.

Provision is also made in the Spacecraft and launch vehicle for a manual initiation of staging (S-II and S-IVB). These provisions will enable abort into orbit.

9.3.2 EMERGENCY DETECTION PARAMETERS FOR AUTOMATIC ABORT (SATURN V)

Angular Overrates. This automatic abort parameter covers all control failures which rapidly lead to an excessive angle of attack and subsequent vehicle breakup. Information will be supplied by the control EDS Rate Gyro Package which consists of three rate gyros for each control plane. These gyros are located in the Instrument Unit. An automatic abort will be initiated when 2 out of 3 gyros in any plane indicate that permissible angular rates are exceeded.

Provisions are made to manually deactivate the automatic abort signal for all 3 planes simultaneously with 1 switch located in the Spacecraft. Manual deactivation time is to be established by mission rules. Capability for deactivating either the roll or pitch/yaw/roll signals by sequencing, prior to first stage inboard engine cutoff, will be available within launch vehicle circuitry.

Adjustable sensor limit settings are provided in pitch and yaw within 2 to 10 degrees/second and in roll within 5 to 20 degrees/second. Sensing hardware must be removed from the launch vehicle to accomplish these adjustments.

S-IC Two-Engines-Out. The loss of thrust on two or more engines will initiate an automatic abort. This automatic abort mode covers failures occurring near the pad and possible range safety action. Deactivation of the automatic abort capability prior to inboard

engine cutoff arming is provided by the launch vehicle sequencer.

This automatic abort capability may be manually deactivated from the Spacecraft. Manual deactivation times will be established by mission rules.

A minimum of two thrust sensors are used on each S-IC engine to provide inputs into the EDS circuitry. Action of at least 2 sensors are required to indicate loss of engine thrust.

9.3.3 EMERGENCY DETECTION PARAMETERS FOR MANUAL ABORT (SATURN V)

S-IC Stage Thrust. The status of each engine of the S-IC Stage is displayed in the Spacecraft (five indicator lights). Upon loss of engine thrust, these engine status lights are energized by a discrete signal.

- An abort for one-engine-out will be governed by mission rules.
- A minimum of two thrust sensors are used on each S-IC engine to activate the engine-out status lights.

S-II Stage Thrust. The status of each engine of the S-II Stage is to be displayed in the Spacecraft (five indicator lights). Upon loss of engine thrust, these engine status lights are energized by a discrete signal.

- Abort on one-engine-out will be governed by mission rules.
- A minimum of two thrust sensors are used on each S-II engine to activate the engine-out status lights.
- Transition from S-IC monitoring to S-II monitoring at staging is accomplished within the launch vehicle circuitry.

S-IVB Stage Thrust. The status of the S-IVB engine thrust is displayed in the Spacecraft (one indicator light). Upon loss of engine thrust, the engine-out status light is energized by a discrete signal.

- Engine thrust is monitored throughout S-IVB burn.
- Abort because of thrust loss is governed by mission rules.
- A minimum of two thrust sensors are used on the S-IVB engine to activate the engine-out status light.
- Transition from S-II monitoring to S-IVB monitoring at staging is accomplished with the launch vehicle circuitry.

Staging Sequence. Physical separation of stages including the S-II second plane separation, are indicated in the Spacecraft by lights, or other suitable discrete indications. In case of no separation, abort will be governed by mission rules.

Launch Vehicle Attitude Reference Failure. Improper operation of the launch vehicle attitude reference (sensed by the IU guidance and control system) will energize an indicator light in the Spacecraft.

Abort or switchover to Spacecraft guidance will be governed by mission rules.

Angle of Attack. An angle-of-attack function is displayed by an analog indicator in the Spacecraft. This parameter is an indication of slow control failures which lead to excessive angles of attack.

The measured pitch and yaw components are combined in vector form into a total angle-of-attack indication.

The type of measurement to be displayed and the limit settings (if necessary, as a function of flight time) will be determined later. Limit settings will govern abort action.

S-II Fuel Tank Pressures. Fuel tank pressures in the S-II Stage are displayed in the Spacecraft by means of an analog display. This parameter requires a redundant sensor and display system.

S-IVB Fuel and LOX Tank Pressures. Fuel tank pressures in the S-IVB Stage are displayed in the Spacecraft by means of an analog display. This parameter requires a redundant sensor and display system. In addition, after S-II/S-IVB separation, S-IVB LOX tank pressures are displayed in the Spacecraft. After separation, the S-II fuel tank pressure display is used to indicate the S-IVB LOX tank pressures..

Attitude Error (Spacecraft). Attitude errors from the Spacecraft guidance and navigation system are displayed in analog form on the flight director attitude indicator. This parameter is an indication of slow control failures leading to excessive angles of attack or excessive attitudes.

The Spacecraft guidance and navigation system will be preprogrammed with the launch vehicle tilt program for the S-IC flight period. Limit settings as a function of flight time (to be determined later) will govern abort actions.

Angular Rates. A single launch vehicle overrate indicator light in the Spacecraft is energized by the IU Control-EDS Rate Gyro Package when permissible angular rates are exceeded in any plane. This indication primarily covers the flight period in which the overrate automatic abort capability is deactivated.

Spacecraft angular rates are presented by analog display on the flight director attitude indicator. The sensing device for this information is the Apollo rate gyro package. Limit settings, as a function of flight time, determine abort actions.

9.3.4 SATURN IB EDS OPERATION

The EDS operation for Saturn IB is different only in the following areas:

- In the S-IB Stage, eight engines are monitored (five in Saturn V).
- Since the Saturn IB has no S-II Stage, any function connected with this stage does not exist in Saturn IB EDS.
- The S-IVB fuel tank pressure is not monitored in Saturn IB Vehicles.

Limits for the critical angle of attack (during the time of maximum dynamic pressure) are shown in Figure 9.3-1. Abort criteria is summarized in Table 9.3-1, and EDS design ground rules are listed in Table 9.3-2.

Table 9.3-1 Saturn IB Abort Criteria and Ground Rules

Auto-Abort Parameters:

- Angular overrates
- Loss of thrust on two or more S-IB Engines

Indications for Manual Abort:

- S-IB thrust (eight indicator lights)
- S-IVB thrust (one of the eight S-IB indicator lights)
- Staging sequence (use of S-IB thrust indicator lights)
- Launch vehicle attitude reference fail (one indicator light)
- Angle-of-attack (Q-ball on meter)
- Attitude error (Spacecraft G&N system on flight director attitude indicator)
- Angular overrates (one indicator light)
- Abort request (one indicator light; signal path is either through Spacecraft up-data rf link, launch vehicle range safety command rf link, or through launch vehicle hardwire prior to liftoff)

Manual Abort Ground Rules

Manual abort will be governed by mission rules within the following ground rules:

- Manual abort will be initiated based on at least two separate and distinct indications.
- No abort will be initiated over rf; an abort request will be given based on telemetered data but the onboard information shall always take precedence.

Table 9. 3-2 Saturn IB EDS Design Ground Rules

EDS Design Ground Rules:

- **Reliability goals:**

  Probability of detecting failure - 0. 9973
  Probability of not detecting false failure - 0. 9997

- No single failure in EDS circuits will prevent detection of a true failure or cause detection of a false failure.
- All failures that jeopardize crew safety will be eliminated if possible.

How Design Ground Rules Are Achieved:

- Use of 2 out of 3 voting circuits in the automatic abort capability
- Use of redundancy in the indications for manual abort capability
- Complete EDS checkout during countdown
- Interlocking EDS-ready in liftoff circuits
- Interlocking J-2 engine-ready with ignition
- Interlocking separation with S-IVB ignition

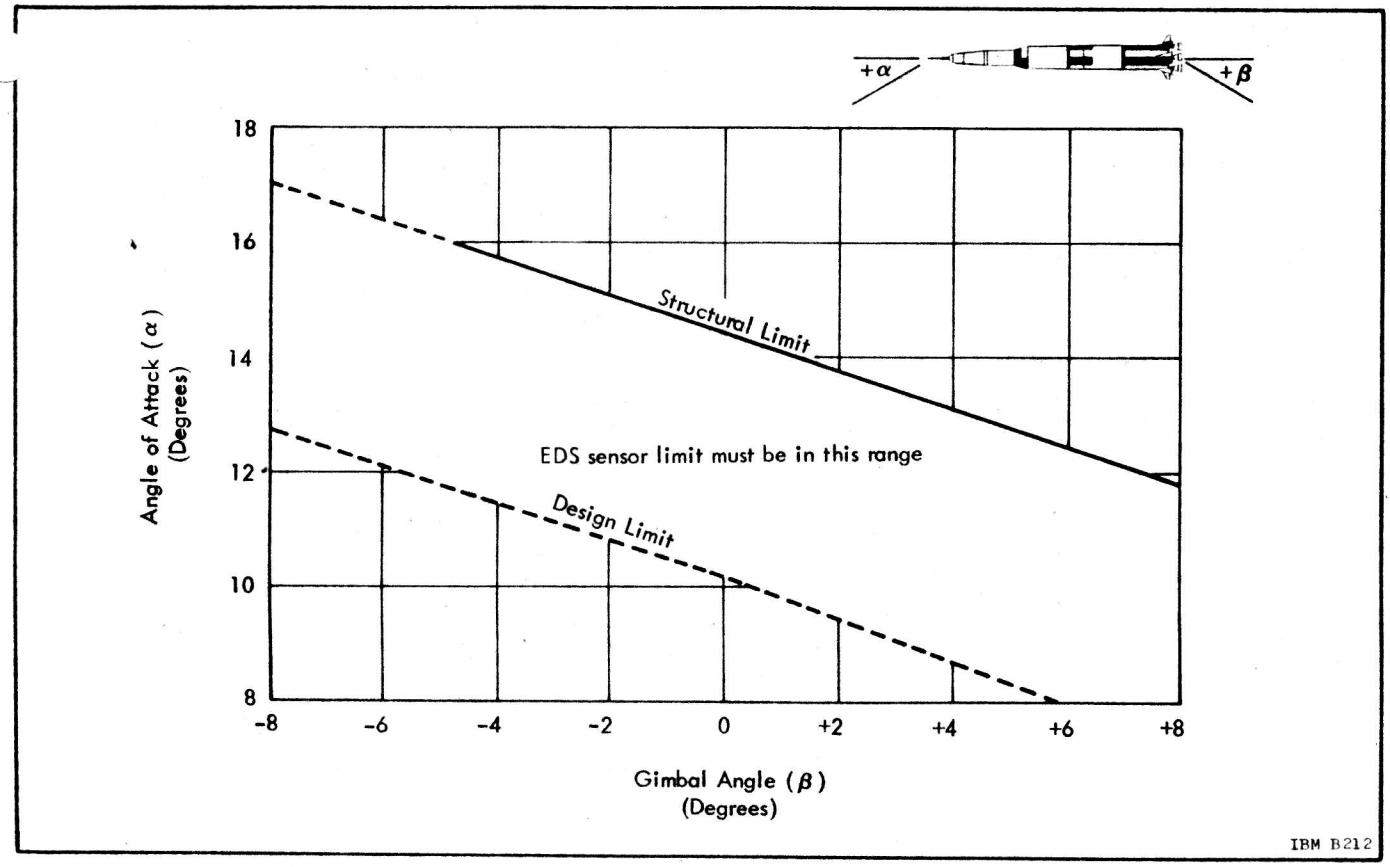

Figure 9. 3-1 Saturn IB Critical Angle of Attack Versus Gimbal Angle (76 Seconds)

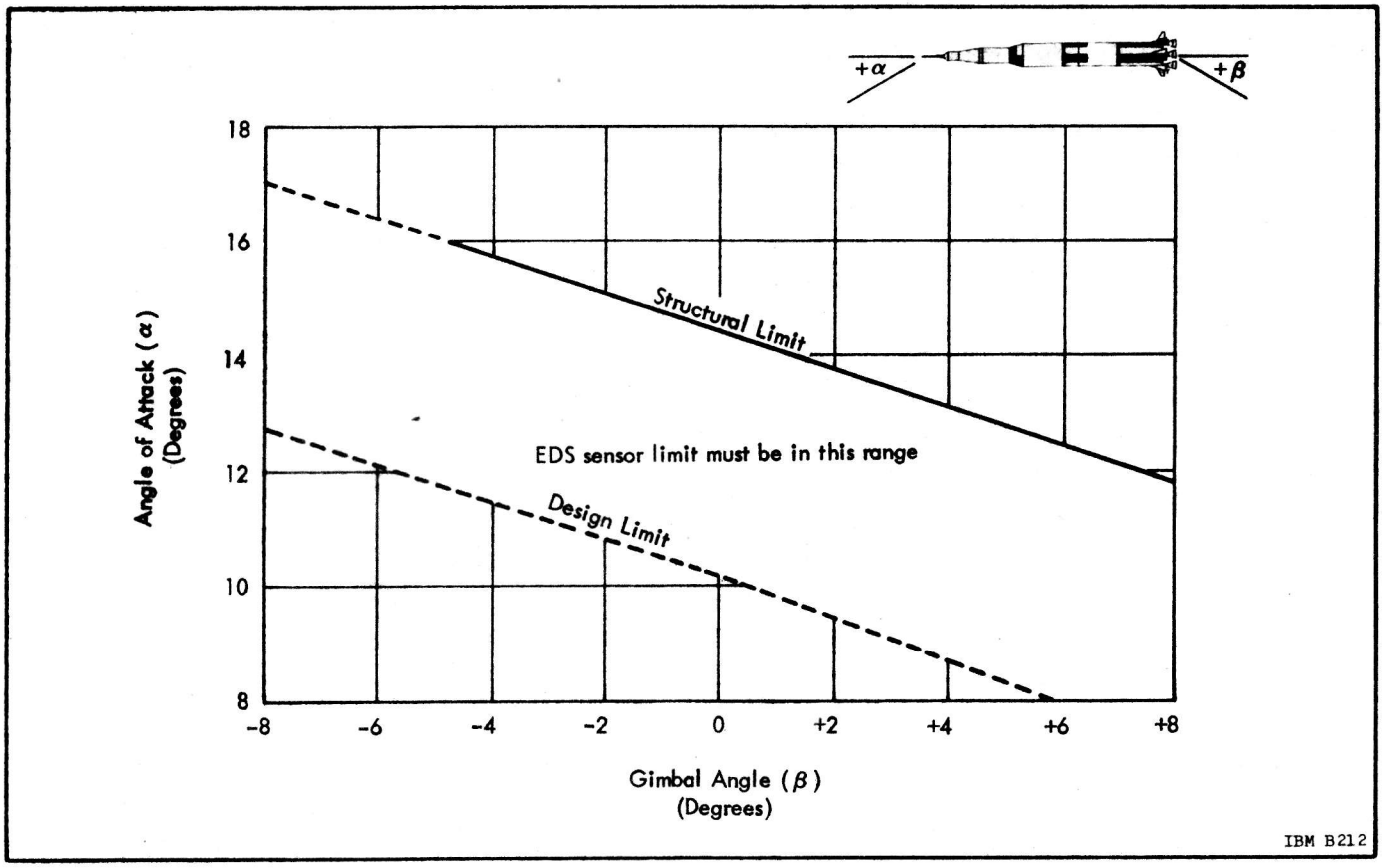

Figure 9.3-2 Saturn IB Critical Angle of Attack Versus Gimbal Angle (76 Seconds)

CHAPTER 10
LAUNCH SITE SUPPORT SYSTEMS

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CHAPTER 11
FLIGHT PROGRAM

SECTION 11.1
INTRODUCTION

The generalized Flight Program System is composed of two basic parts or subsystems; the application subsystem and the control subsystem. The application subsystem is a collection of programs whose sole purpose is to perform the individual actions or functions which comprise the task of an LVDC flight program for a given mission or missions. The control subsystem, however, is mission independent and is itself divided into three parts; an executive control program, a common utility package, and a common communications and data area. The primary purpose of the control subsystem is to control the sequence and order of operation of all programmed functions specified for a particular mission task.

The application subsystem provides a master pool of all defined LVDC functions which can be used to generate a total Flight Program configuration for any given mission task or application. It is actually composed of a collection of independent, closed program units called application modules. Each application module is defined to be an operationally independent program exclusively designed to perform one or a number of related functions; e.g., navigation, guidance, accelerometer processing, or minor loop. The operational linkage, sequence, and execution of the application modules for a given task are governed by the requirements and operation of the control subsystem executive program.

The total operational requirements of all application modules for a given mission task and its phases are determined prior to program generation. At program assembly time, these requirements are defined to the system via system executive macros which generate a set of master queue/control tables. These requirements include such things as module identification, mode of operation, and sequence and time frame of execution for each function of each phase of the mission.

All application modules so specified at assembly time are automatically selected from the application subsystem and linked to the Executive Control Program by the LVDC Assembler as a flight program configuration. The Executive Control Program will accomplish real-time control of these modules by means of the resultant master queue/control tables generated at assembly time.

The queue/control tables initially specify a fixed order and time frame of execution of all application modules for a given mission. Real-time conditions, such as the results of calculations or external events, may require changes to this sequence of module execution. Provision is made to allow real-time modification of the queue/control tables. This provision is called "queuing." Queuing allows an application module to specify to the Executive Control Program that another module or itself is to be rendered inactive (queued-out) or active (queued-in). All active modules will be executed according to the queue/control table in which they are specified, while inactive modules will be ignored or bypassed.

Although application modules are operationally independent of one another, there nevertheless exists a need for intermodule communications for the purpose of passing data in the form of inputs and outputs. In order to standardize and isolate communications between application modules or between the executive program and application modules, a common or universal communications and data area is provided by the control subsystem. All interprogram communications must be accomplished through this medium.

The control subsystem also provides a common utility package available for use by application program modules. This package consists of a number of routines which perform mission independent utility functions such as sine-cosine calculations or matrix multiply operations.

SECTION 11.2
PROGRAM DESCRIPTION

11.2.1 EXECUTIVE CONTROL PROGRAM

The Executive Control Program is a group of interacting subprograms whose primary purpose is to control the sequencing and scheduling of the execution of individual application program modules to meet the operational requirements of a given LVDC mission. It examines interrupts and priority control tables to determine order of execution of functions and provides a means of transferring and returning operational control to and from the functional program modules.

In order to perform its task properly, the Executive Control Program must be cognizant of the configuration and requirements of the particular Flight Program to be executed. The design and organization of the Executive Control Program therefore, is based on the use of sets of master queue/control tables by which the total application requirements of any given mission can be specified. Through these tables a mission and its operational phases can be completely defined to the Executive Control Program. They provide the identification of functions to be performed, the normal sequence and order of these functions, their associated time requirements, and initial queue (active or inactive) status. Furthermore, these tables can be dynamically altered (queuing) during the program execution to reflect changing requirements due to phase-to-phase transition or as the result of external events or program calculations. The Executive Control Program, then, directs and controls the operation of the total Flight Program basically through the use of master queue/control tables.

The structure (Figure 11.2-1)* of the Executive Control Program consists of the following subprograms or components.

MISSION EXECUTIVE SUBPROGRAM

The Mission Executive Subprogram performs general system initialization, determines which phases of the specified mission are to be executed, generates required control words for phase initialization, gives control to the Phase Initializer to initiate phase execution, and performs all required system terminal housekeeping at mission end. Figure 11.2-2 illustrates the mission Executive Subprogram.

Upon initial entry, the Mission Executive inhibits all interrupts, initiates a real-time clock reading, and initializes accumulated time in mission and user reference. The program then performs all initialization required for the proper operation of the Interrupt Processor and the Timer 1 Scheduler. Pointers for internal use are initialized and the Timer 1 Scheduler is called to initiate operation of the timer 1 interrupt counter. The Timer 1 Scheduler in turn, schedules the first timer 1 interrupt for the user module (minor loop) initially specified by the system macro defining all user interrupt routines. Control is then returned to the Mission Executive for phase selection. The first timer 1 interrupt, however, will not be processed until the first phase beings execution, i.e., not until the timer 1 interrupt inhibit is removed at the completion of timer 2 scheduling performed at the end of first phase initialization.

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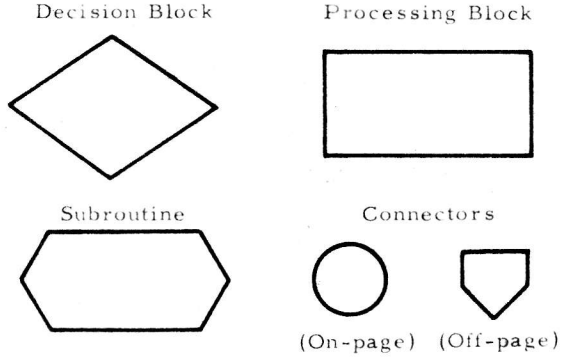
* The figures in this section contain word flow diagrams of a typical Saturn flight program. A number of loops are illustrated and are followed by several figures which give a functional breakdown of the various routines. A further breakdown of of the routines, (i.e., subroutine) is beyond the scope of this book. The following symbols are used to represent program functions:



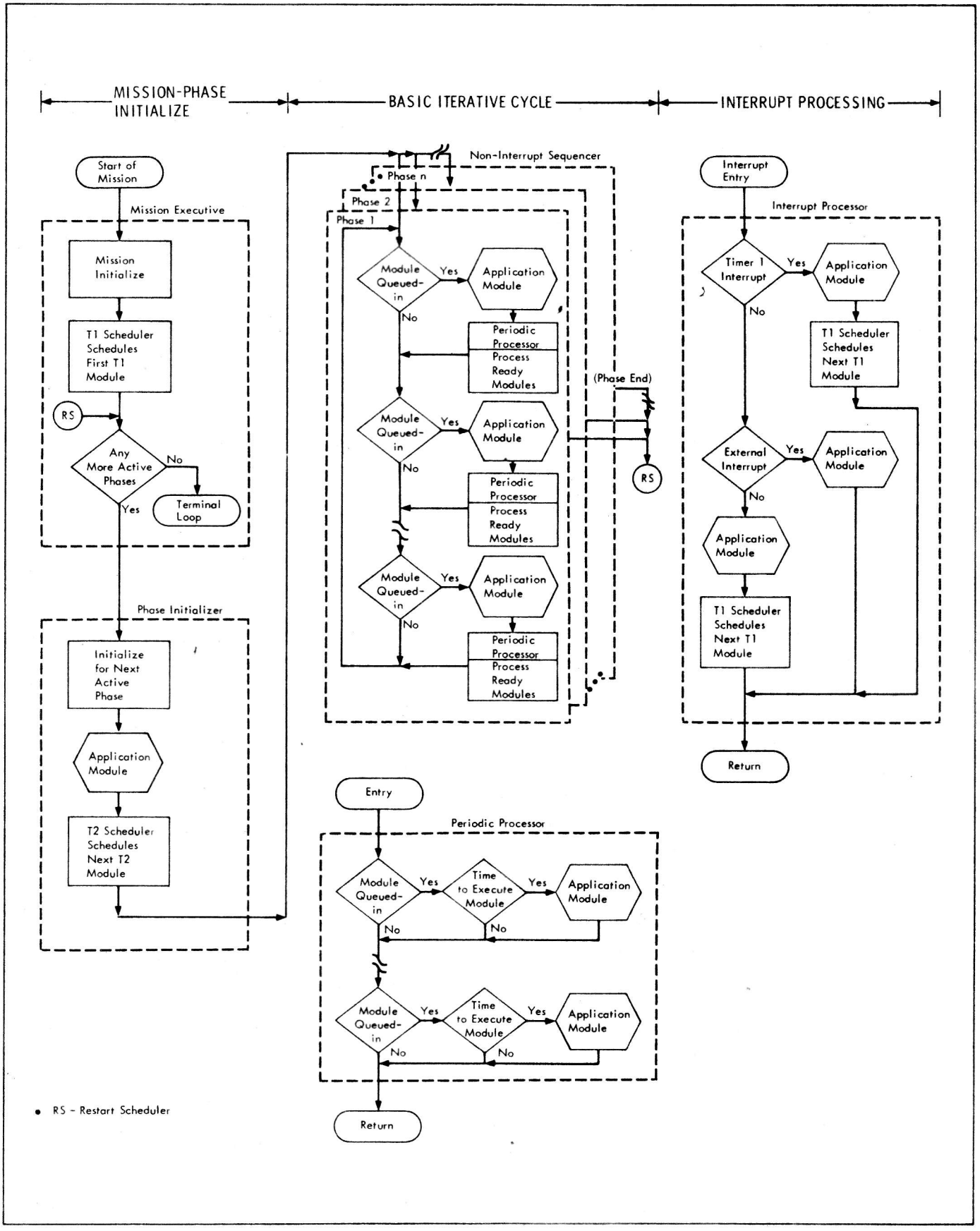


Figure 11.2-1 Control Program Structure

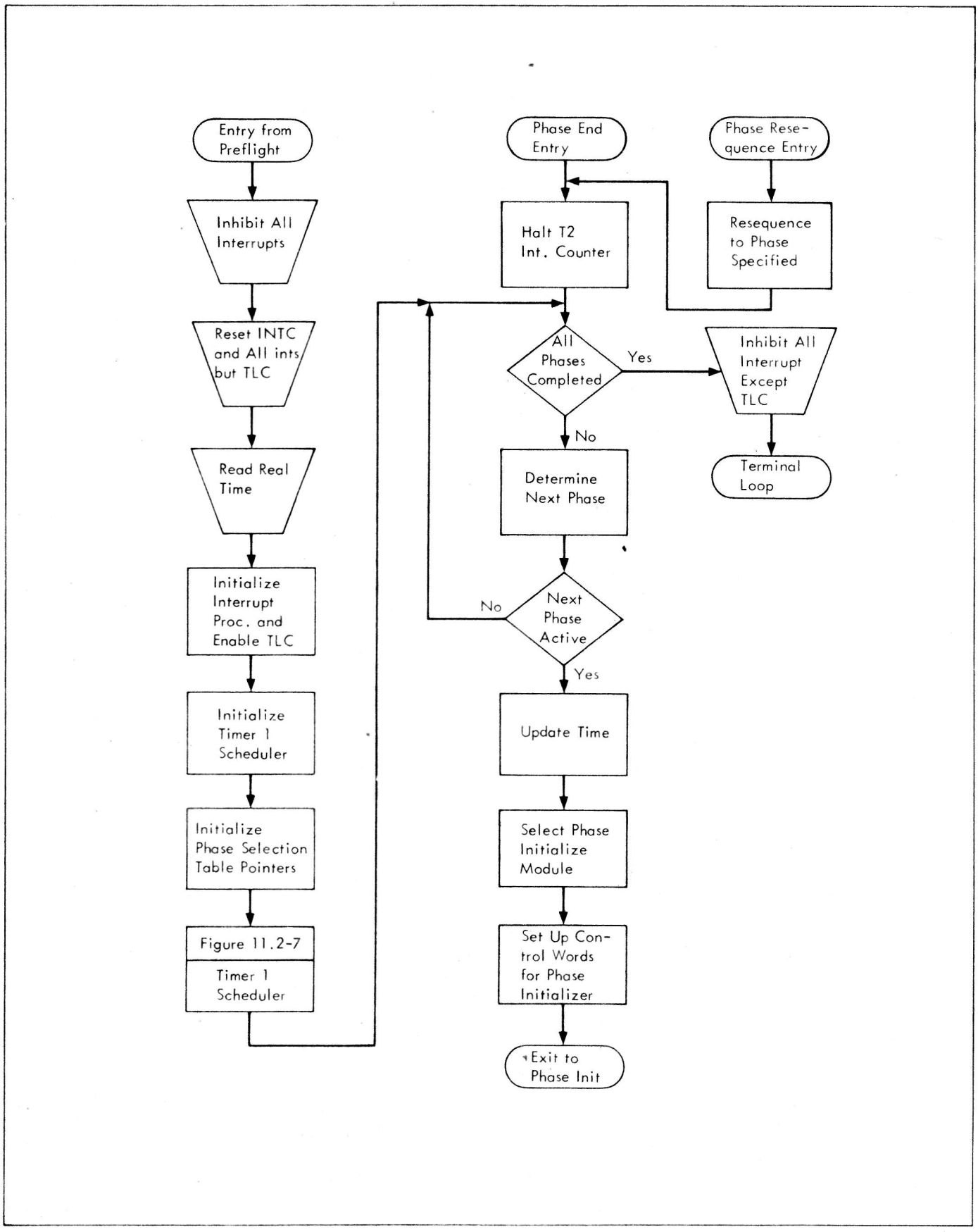


Figure 11.2-2 Mission Executive

The Mission Executive determines the next phase to be executed by means of a special Active Phase Indicator Word generated by the mission initialization system macro. This indicator consists of individual bits arranged in chronological order for each phase defined. Each bit indicates whether or not the corresponding phase is to be executed. At program generation time, all phases defined are set active. If there are no more active phases to be executed, the Mission Executive will perform all required terminal housekeeping functions and enter a terminal loop. If any active phases remain to be executed, the next in order is selected. Control words associated with the phase that is to be executed are obtained from the Phase Control Word Table and supplied to the Phase Initializer. The Mission Executive then gives control to the Phase Initializer and is not reentered again until phase execution is completed. Since phase termination will normally be dependent upon a particular function or calculation performed by some application module, or an external event processed by an application module, it will be the responsibility of that application module to accomplish Mission Executive reentry at phase end.

PHASE INITIALIZER SUBPROGRAM

The Phase Initializer (Figure 11.2-3) is entered only from the Mission Executive. Entry is made each time the Mission Executive selects a new phase of a given mission for execution. Upon entry, the Phase Initializer Subprogram uses control information supplied to it to set the master queue tables to the initial queue status specified for the selected phase. This information also provides the linkages to the appropriate user specified application initialize module and to the Sequential Control Table for that phase.

After all queue tables are initialized, the Phase Initializer executes the user application initialize module which returns control at completion. The Timer 2 Scheduler is then called to initiate operation of the timer 2 interrupt counter. At completion of timer 2 scheduling, control is passed to the Non-Interrupt Sequencer to control the execution of the application modules which comprise the basic iterative cycle of the given phase.

NON-INTERRUPT SEQUENCER

Essentially, the Non-Interrupt Sequencer consists of a number of tables: a Sequential Control Table for each phase of the mission and a single

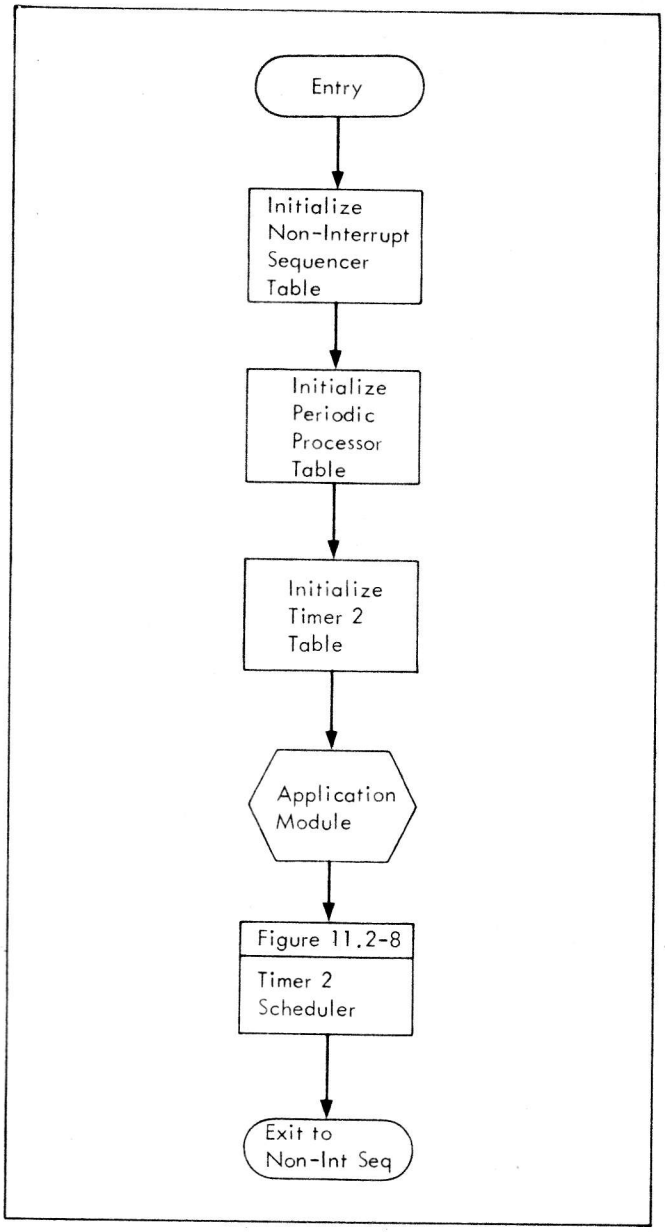


Figure 11.2-3 Phase Initializer

Sequential Queue Table for the total mission. Each control table is an executable table, i.e., it is made up of executable instructions. It is actually one of these tables that is given control at completion of phase initialization. The selected table will remain in control executing associated application program modules in an iterative loop until some user application module detects phase-end conditions and effects reentry to the Mission Executive.

Each entry in the Sequential Control Table picks up a specific entry from the Sequential Queue Table and checks to see if it is queued-in. (Figure 11.2-4). If the entry is queued-in, the correspond-

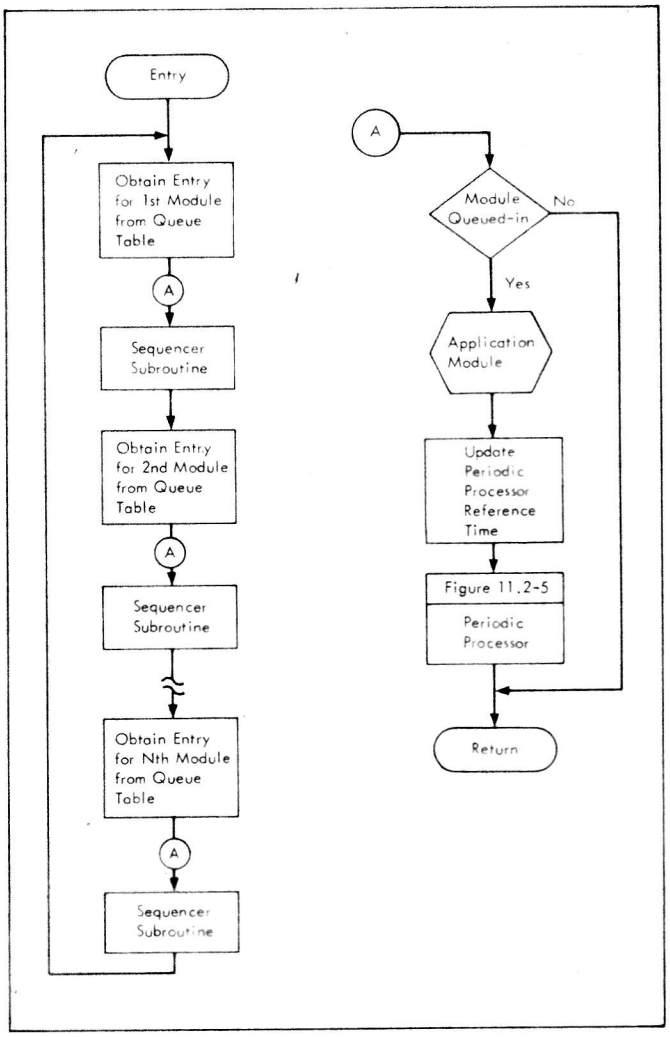


Figure 11.2-4 Non-Interrupt Sequencer

ing application module is executed. If the entry is not queued-in, the application module is ignored. Before processing the next control table entry, a check is made to determine whether or not it is time to call the Periodic Processor. If the test is passed, accumulated time in mission, phase, and user reference is automatically updated and control passed to the Periodic Processor. When control is returned at the completion of periodic processing or if the time test was originally not passed, the next control table entry in sequence is processed. After the last entry in the phase Sequential Control Table has been processed, a transfer is made back to the beginning of the table and the processing procedure repeated. This iterative loop will continue until some application module returns control to the Mission Executive at phase end.

PERIODIC PROCESSOR

The Periodic Processor (Figure 11.2-5) is entered at a system determined frequency from the Non-Interrupt Sequencer. The Periodic Processor is basically an executable queue/control table, the Periodic Table. This table consists of entries to time tests which provide for servicing time-dependent, periodic application modules.

Upon entry, the first item in the queue/control table is processed. If the entry is queued-in, an associated time test is made to determine whether or not a corresponding application module is to be called. If the time-test is passed, the application module is executed and time for its next execution updated. The next entry in sequence in the queue/control table is then processed in the same manner. If a table entry is queued-out, no time test or application module will be executed before proceeding to the next entry. Likewise, if any time test is not passed, the corresponding application module will not be executed before proceeding to the next table entry. Control is returned to the Non-Interrupt Sequencer after all Periodic Table entries have been processed.

INTERRUPT PROCESSOR

The Interrupt Processor services all LVDC/LVDA interrupts on a priority basis and routes control to appropriate application modules (Figure 11.2-6). Program controlled interrupts and externally controlled interrupts are the two basic classes of interrupts serviced under a system defined level of priorities within the Interrupt Processor. The four basic levels of priority are as follows:

- Level 4 TLC (LVDC Simultaneous Memory Failure) interrupt.
- Level 3 Timer 1 interrupt.
- Level 2 External interrupts (other than TLC) by order of assignment to the LVDA Interrupt Storage Register.
- Level 1 Timer 2 interrupt.

These levels determine the order in which processing will occur whenever more than one interrupt requires servicing at the same time. They also indicate the degree of priority provided for

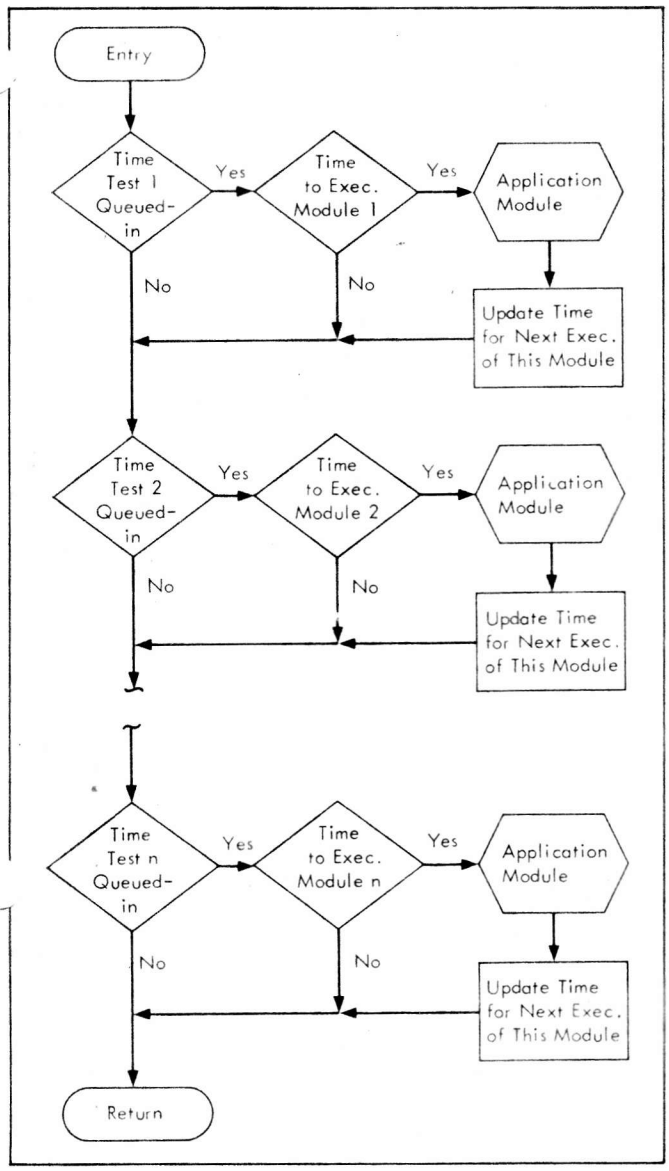


Figure 11.2-5 Periodic Processor

associated application module processing. Processing at any level may be interrupted and delayed until all required processing at the higher level is completed. All processing performed on a non-interrupt basis is effectively at a level "0" priority.

The timer schedulers also make use of a priority scheme in selecting the next application modules to be serviced by the timer interrupts. This priority scheme, however, is only in effect when at least two application modules specify identical times for use of the same timer interrupt.

The two program controlled interrupts which operate under control of programmable counters are: Timer 1 (formerly the Minor Loop Counter) and Timer 2 (formerly the Switch Selector Counter). Both of these counters operate at a 492.2 microsecond rate. The Timer 1 Counter is a continuously operating wrap-around counter, which will automatically generate an interrupt every 4.032 seconds (maximum counter value) if not under program control. The Timer 2 Counter is not a wrap-around counter. It will generate an interrupt only if initiated under program control.

Timers 1 and 2 are used to service application modules requiring high timing accuracy on a requested or cyclic basis. The timer counters are controlled only by the system scheduler routines (one is provided for each timer) which determine when the next timer interrupts are to occur and the application modules to be serviced. The Interrupt Processor allows timer 2 scheduling and the application modules serviced by Timer 2 to be interrupted by the timer 1 interrupt. Timer 1, therefore, is intended for use by high priority functions while Timer 2 is for functions of a lower priority.

All application modules serviced by the timers are required to return control to the Interrupt Processor upon their completion. The Interrupt Processor will then call the appropriate scheduler routine to determine the next use of the counter. Upon completion of scheduling, control will again be returned to the Interrupt Processor which returns control to the last interrupted program location.

TIMER 1 SCHEDULE

The Timer 1 interrupt is reserved for modules whose operational accuracy requirements demand stringent timing. The Timer 1 Scheduler (Figure 11.2-7) is designed to determine which of two modules is to execute next and to schedule the Timer 1 interrupt.

The Timer 1 Scheduler gives a higher priority to one module when both modules are scheduled for the same time or are late. The higher priority module is predominantly used for minor loop operations. The lower priority module is predominantly used for Switch Selector operations. The two application modules and/or their entry points may be changed by queuing operations from other modules.

The Timer 1 Scheduler is entered from the Interrupt Processor following the execution of a Timer 1 module or from an application module whenever a Timer 1 queuing operation is performed. Upon entry, the scheduler will decide which module

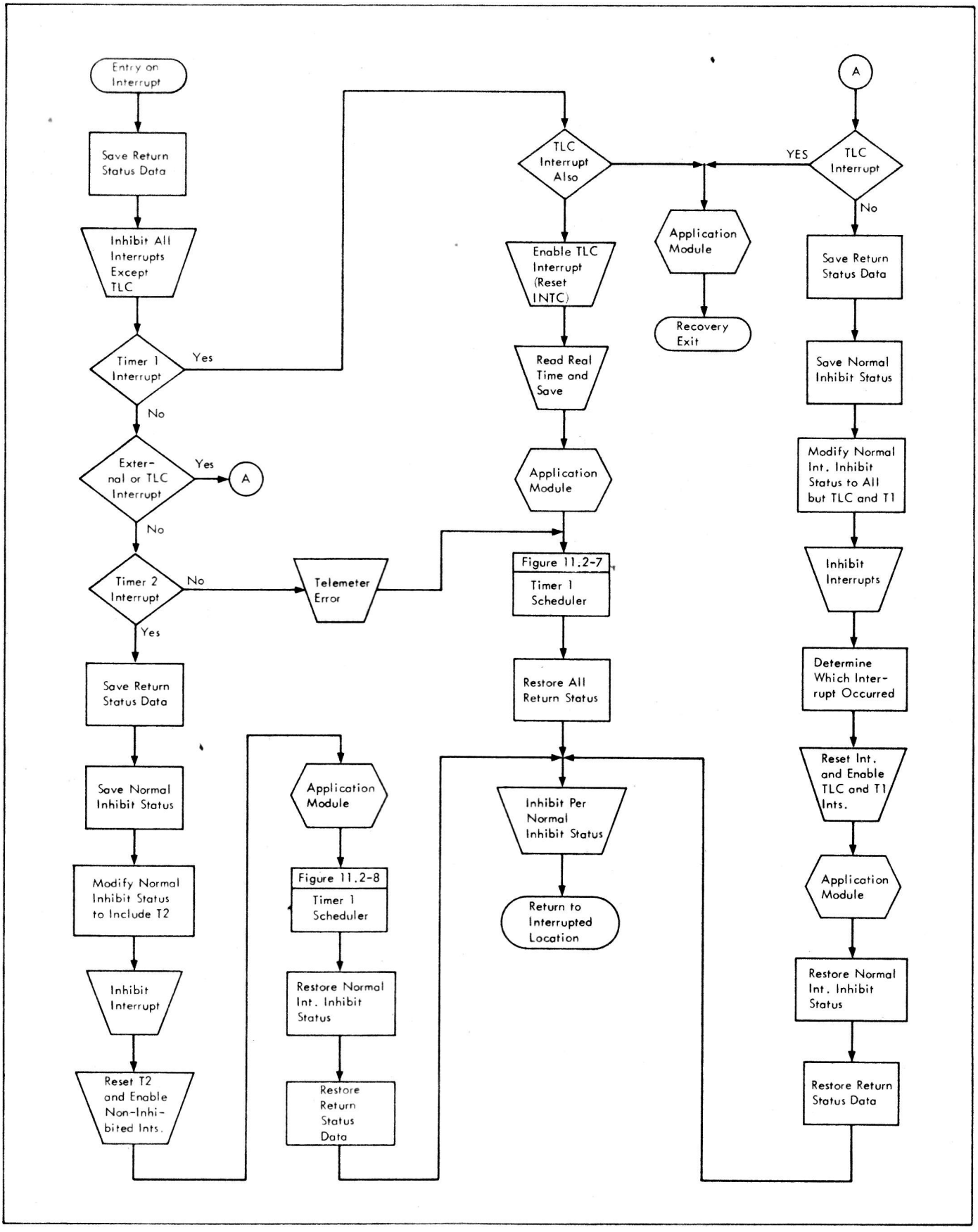


Figure 11.2-6 Interrupt Processor

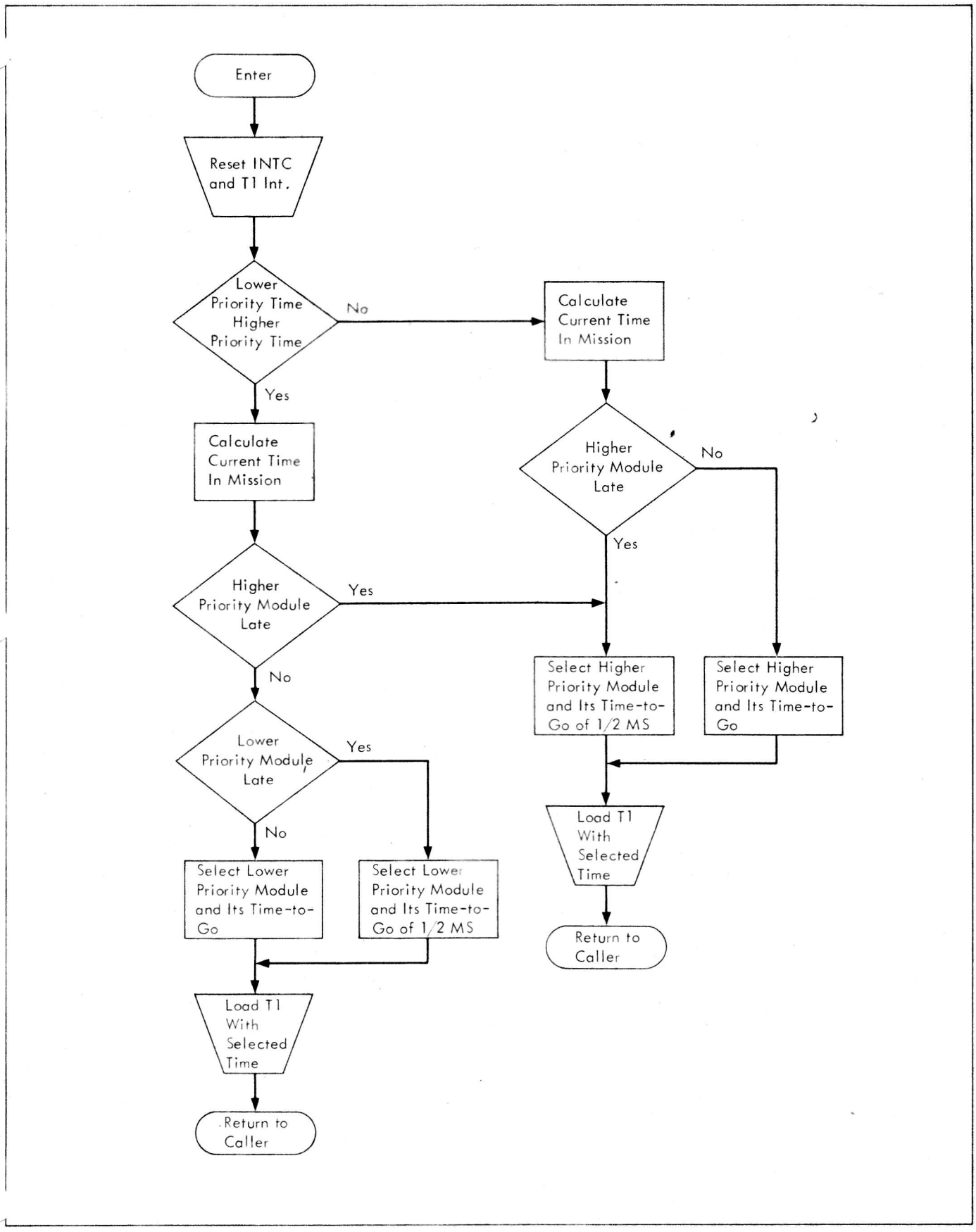


Figure 11.2-7 Timer 1 Scheduler

requires the use of the next Timer 1 interrupt. Proper linkages for the execution of the selected module by the next Timer 1 interrupt are then set up, the Timer 1 counter is loaded with the associated time-to-go, and control is returned to the Interrupt Processor.

TIMER 2 SCHEDULER

The Timer 2 Scheduler (Figure 11.2-8) is automatically entered from the Interrupt Processor whenever any module services by the timer 2 interrupt completes processing. It is also automatically entered via the system queue macro whenever any timer 2 queuing operation is performed. The Timer 2 Scheduler is basically an executable table, the Timer 2 Table. This table consists of entries to time tests which provide for servicing time-dependent priority application modules on a requested basis.

Upon entry, the scheduler first selects itself as a module to be executed 4 seconds later. This is done to maintain control of scheduling in case no application module requires the use of the timer 2 interrupt within the maximum time delta (4.032 seconds) which the timer can accommodate.

The scheduler then steps through the entries in the Timer 2 Table. Each queued-in time test determines whether or not the associated application module requires use of the interrupt before the currently selected module. If so, that module and its associated request time becomes the current selection. This process is repeated until all table entries have been checked. Linkage to the last selected module is set up for execution on the next timer 2 interrupt, timer 2 is loaded with the associated request time and control is returned to the calling routine.

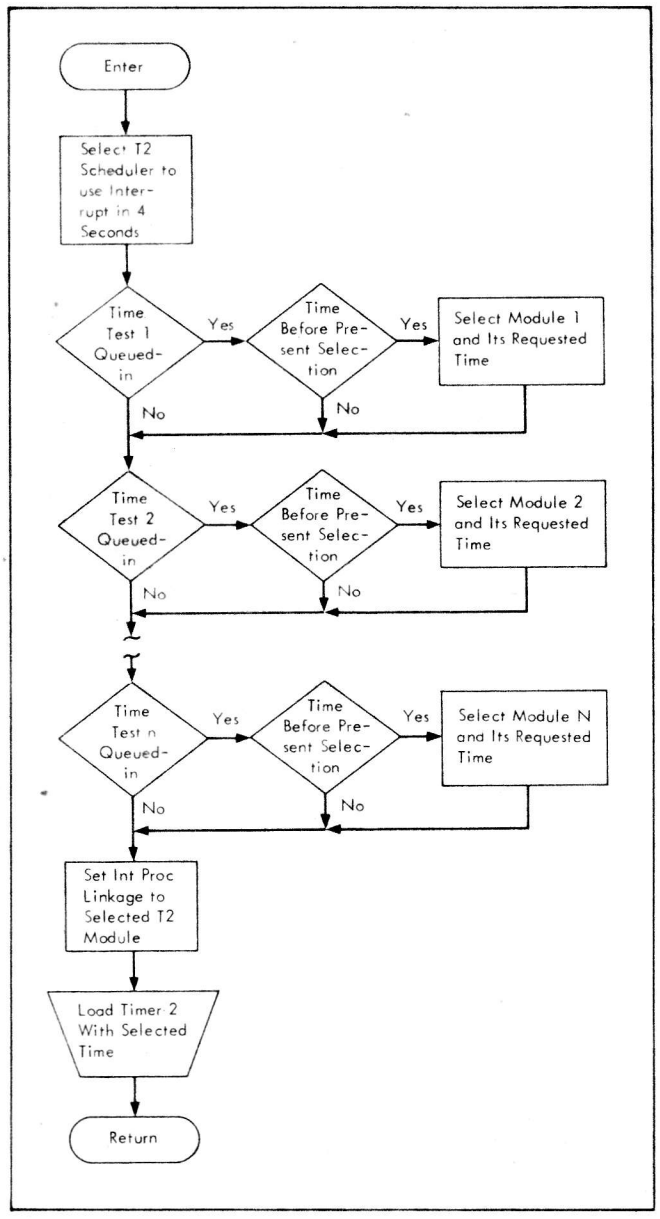
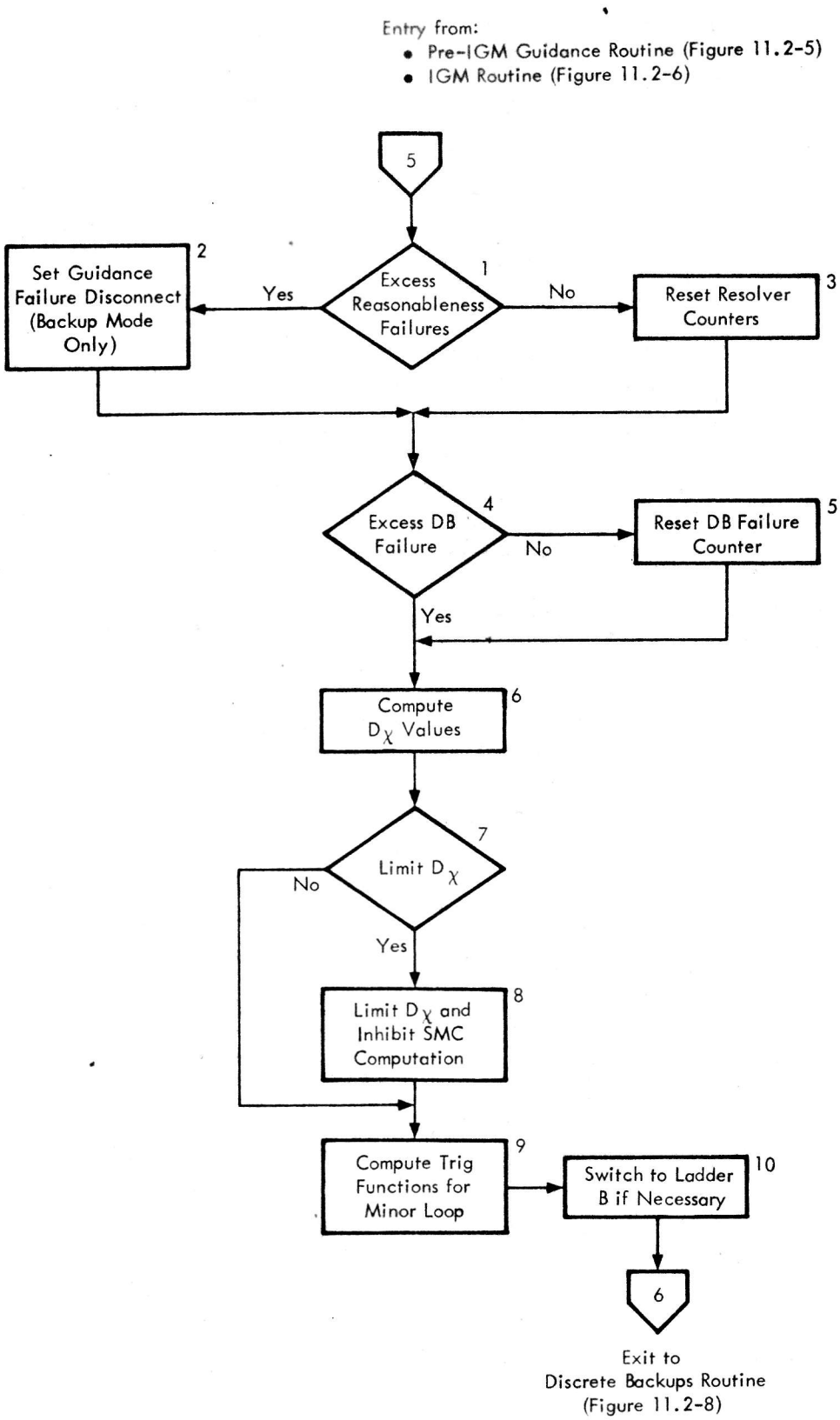


Figure 11.2-8 Timer 2 Scheduler



NOTE - This is block 8 of Figure 11.2-1

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Figure 11.2-7 Minor Loop Support

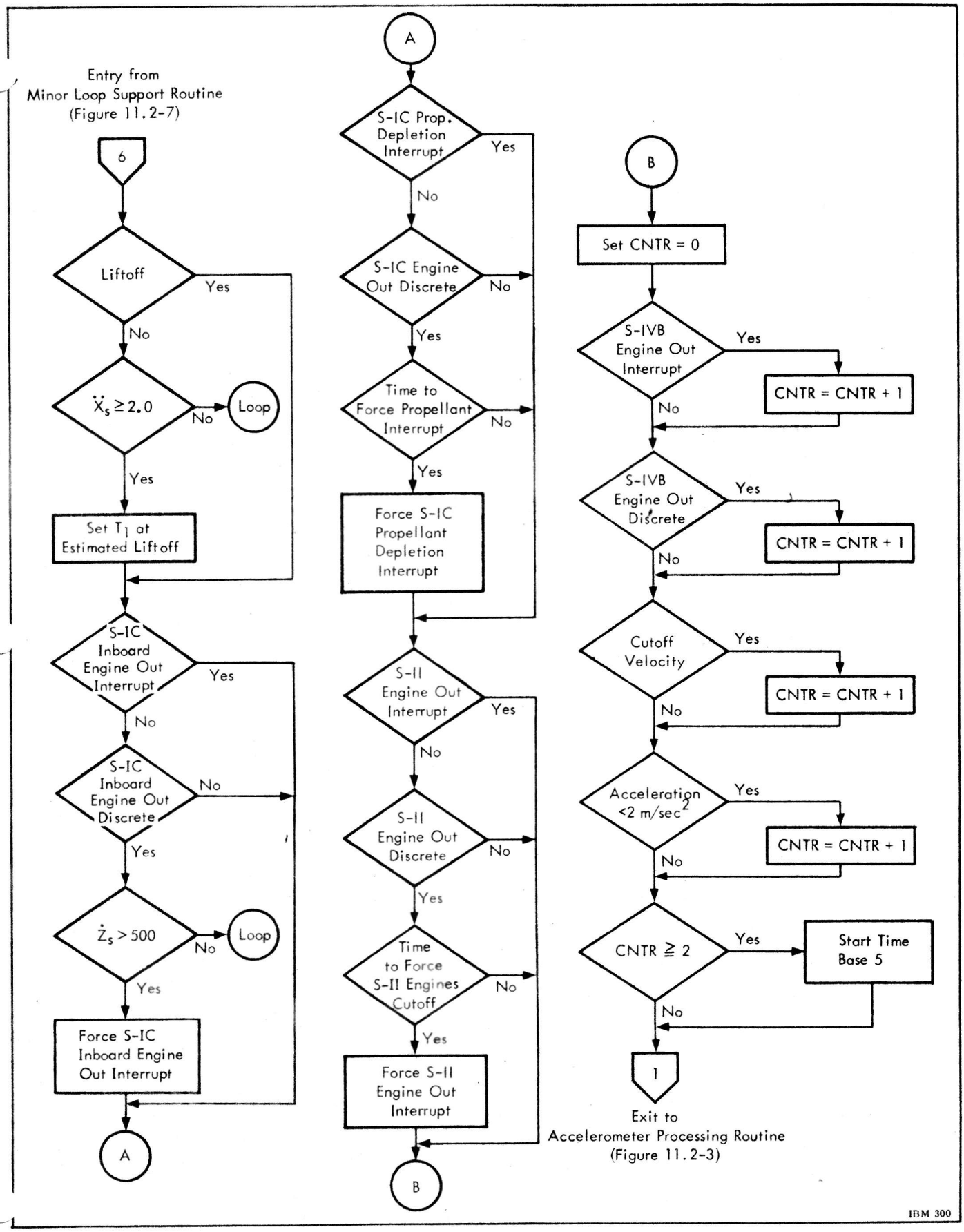


Figure 11.2-8 Discrete Backups

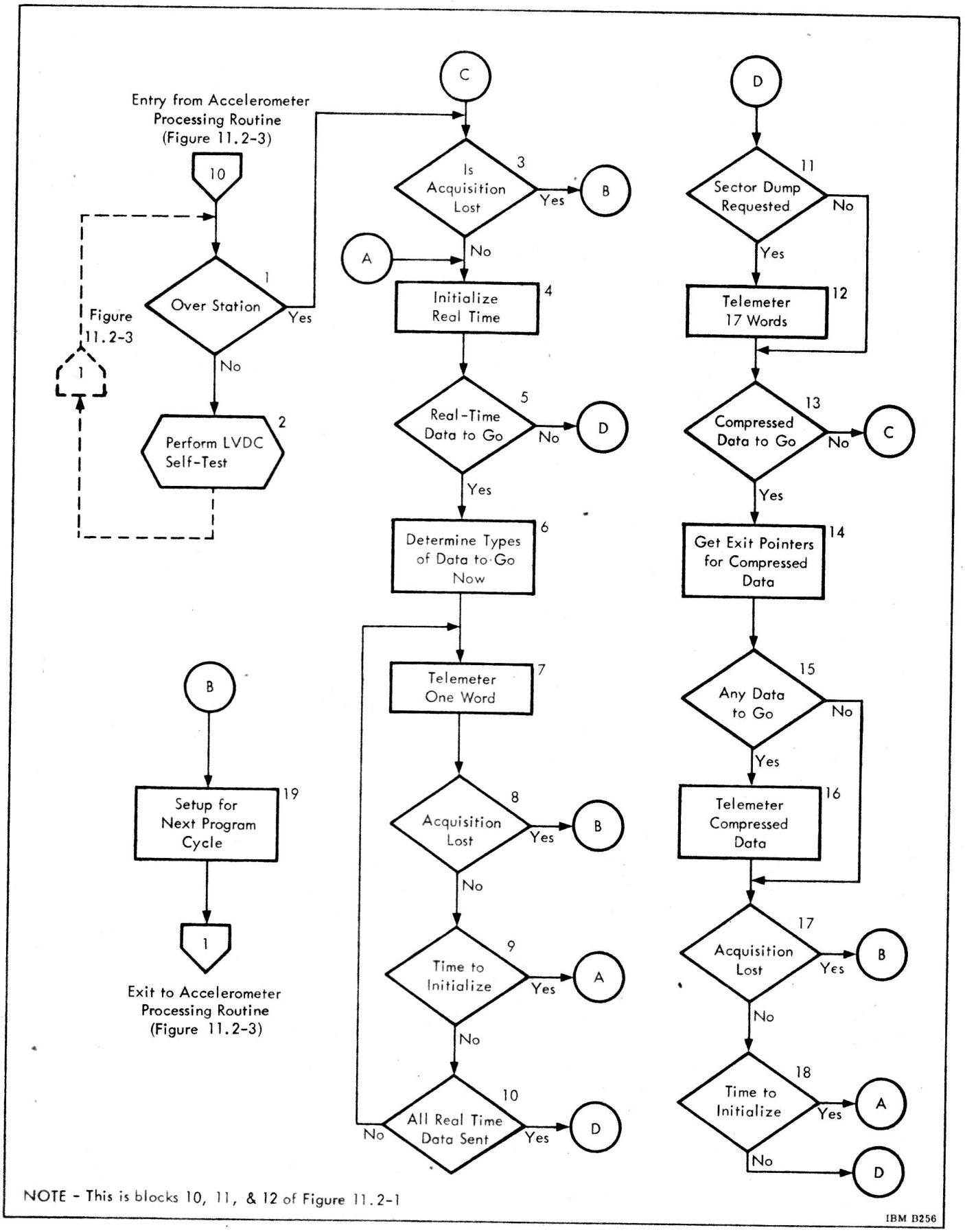
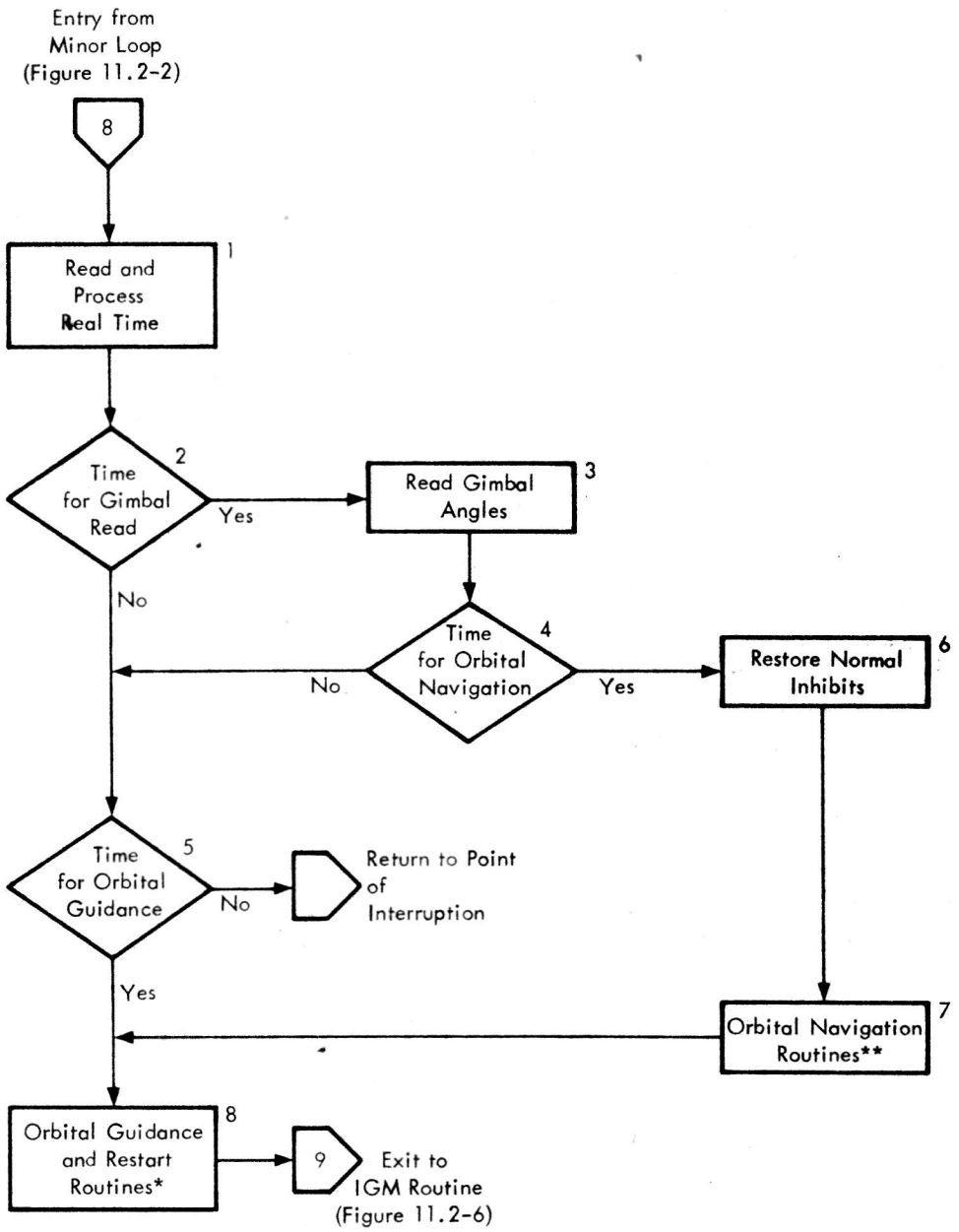


Figure 11.2-9 Orbital Flight Program



* Routines include:
- Predict positions and velocities
- Compute gravitation
- Compute drag
- Compute vent thrusts
- Accumulate position, velocity, & acceleration

** Routines include:
- Interpolate $X_S Y_S Z_S$
- Calculate $X_4 Z_4$
- Compute target & perigee vectors
- Issue χ commands
- Prepare for restart of S-IVB
- Calculate restart conditions

IBM B257

Figure 11.2-10 Orbital Processing

SECTION 11:3

FLIGHT PROGRAM DESCRIPTION

11.3.1 FLIGHT PROGRAM CONFIGURATION

The Flight Program is composed of the control program, common communications area, and all application modules. The configuration of the Flight Program is defined by the flight programmer via system macros. Program definition macros are separated into three categories; mission, phase, and interrupt macros. Mission macros define all modules which will execute under direct control of the control program during the mission, and the controlling subsystem under which each will execute.

- Phase 1 Boost (First) From GRR to T_5 +100 SEC
- Phase 2 Parking Orbit T_5 +100 to T_6 -9 SEC
- Phase 3 Boost (Restart/TLI)* T_6 -9 SEC to T_7 +20 SEC
- Phase 4 Post TLI T_7 +20 SEC to End of Mission

Interrupt macros consist of two types, which are concerned with interrupt processing:

- Specifies external system interrupts which are to be active, and module that is to gain control on occurrence of a given interrupt.
- Specifies Timer 1 controlled minor loop module and modules execution rate.

11.3.2 APPLICATION MODULES(DIRECTLY CONTROLLED)

Application modules are operationally independent of one another in regard to their sequence and time frame of execution. Module execution is controlled by the system Executive Control Program in one of two ways: directly, where the module is called by the executive or indirectly, where the module is called as a subroutine by another module that is under direct control of the executive. Each module performs its function and then returns control to the calling source.

* (Translunar Injection)

The following is a list of application modules that will be utilized by the Generalized Flight Program and a description of each is included. The order of module presentation is referenced to the subprograms of the Executive Control Program. Application modules are controlled directly by these subprograms. General flow of the Saturn V Flight Program is illustrated in Section 11.3.4. The times that the modules are queued-in are also indicated.

NON-INTERRUPT SEQUENCER — PHASE 1 AND 3

The non-interrupt sequencer consists of 18 directly controlled modules:

- Accelerometer Read (AR) - The accelerometer read module reads Platform signals and formats the raw data for use in the Accelerometer Processing Module. The AR Module will perform the function every computation cycle during Phases 1 and 3.
- Simulated Accelerometers (SA) - The function of the SA module is to compute simulated velocity increments for a predetermined thrust model during the Flight Simulation Mode of program operations. The SA module will perform once per computation cycle during Flight Simulation Mode only.
- Accelerometer Processor (AP) - The AP module detects velocity measurement errors through reasonableness test and accumulates velocity measured by the Platform accelerometers. The AP module performs the function every computation cycle during Phases 1 and 3.
- F/M Calculations (DV) - The function of the DV module is to compute the actual acceleration from the accelerometer readings once per computation cycle.
- Boost Navigation (NE) - The function of the NE module is to determine the vehicle position and velocity in an earth centered inertial coordinate frame once per computation cycle during Phases 1 and 3.

- Restart Calculations (TC) - The function of the TC module is to calculate the target orbit parameters. This function is performed only in Phase 3 at a preset time in T_6.
- Phase Actuator (PA) - The function of the PA module is to terminate the present phase and start the specified phase.
- Time Tilt Guidance (TT) - The function of the TT module is to generate steering commands (guidance Chi's) as a function of time from liftoff through the S-IC Stage burn.
- Chi Computations (CC) - The function of the CC module computes the pitch and yaw commands in the S-System and telemeters the roll, pitch and yaw commands in both the boost and orbital modes. CC is entered once per computation cycle from IGM while IGM is active during Phases 1 and 3, and entered once per second from Orbital Guidance module during Phases 2 and 4.
- Iterative Guidance Mode (IG) - The function of the IG module is to compute the required vehicle steering commands to place the vehicle in the desired orbit using navigation variables (position, velocity, acceleration), time, desired terminal conditions and vehicle performance data.
- S-IVB Cutoff Prediction (HS) - The function of the HS module is to ensure the required velocity is achieved by precisely determining when to issue the S-IVB Cutoff command to the Switch Selector.
- Orbit Guidance (OG) - The function of the OG module is to compute the desired vehicle attitude during periods when no propulsive thrust is available and attitude control is provided by the Auxiliary Propulsion System. Orbital guidance is computed once per second.
- Time-to-Go to Restart and Beta Test (RS) - The function of the RS module is to predict the exact time to start the chilldown sequence (restart) and to initiate T_6 when the beta test is passed (the vehicle position satisfies a geometrical relationship with the target vector for the selected restart opportunity).
- Time Base 1 (TB1) - The function of the TB1 module is dual purpose: (1) indicates TB1 when accessed by the Liftoff module, when the inertial vertical acceleration back up condition is met or when entered on a Timer 2 interrupt scheduled by Events Processor in the repeatable Flight Simulation Mode, (2) terminates flight program processing if the acceleration condition is not met by a predetermined time.
- Time Base 5/7 (TB57) - The function of TB57 module is to check S-IVB cutoff conditions necessary to initiate TB 5 or 7. When all required conditions have occurred, the appropriate time base will be initiated.
- Minor Loop Support (MS) - The function of the MS module is to calculate the altitude increments (delta Chi's) and the terms of the Platform to body coordinate transformation used by the minor loop module.
- Simulated Platform Gimbal Angles (PG) - The function of the PG module is to compute the expected gimbal angles due to earth's rotational rate in order to compensate for the actual Platform gimbals read during Flight Simulation Mode of program operation with the system powered up and connected.
- ETC/BTC (EB) - At the end of each computation cycle, the EB module will mark the end of the current telemetry cycle and the beginning of the next telemetry cycle. The module will also serve as a telemetry catch up module and will reset system status words if required.

PERIODIC PROCESSOR

The Periodic Processor consists of four directly controlled modules:

- Discrete Processor (DP) - The DP module accesses individual discrete and time base modules to perform all functions required when it detects a change in the logic stage of any of the discretes specified for processing.

- 30 Second Data Compression (PC30) - The module compresses and stores the 30 composite Error Monitor Register word if a change occurred during the 30 second interval.
- 50 Second Data Compression (PC50) - The module compresses and stores accelerometer data every 50 seconds. It also stores and compresses any change in the discrete inputs and discrete input spares occurring during the 50 second interval.
- 100 Second Data Compression (PC99) - The function of the PC99 module is to compress and store the 5 gimbal angles and back up gimbal angles every 100 seconds.

NON-INTERRUPT SEQUENCER PHASE 2 AND 4

The non-interrupt sequencer phase 2 and 4 contains 3 directly controlled modules:

- Data Compression Telemetry (CT) - This module serves as the active major loop during orbit after there has been an acquisition gain. The module telemeters different types of data which have been stored from the previous dark period and/or which are sampled at known intervals.
- Sector Dump Telemetry (DT) - The DT module telemeters the entire contents of one, a series, or all LVDC memory sectors when a DCS sector dump is requested.
- Service Periodic Processor (P212) - A control program routine which is queued-in during Phases 2 and 4 to ensure that the Periodic Processor is executed.

INTERRUPT PROCESSOR

The interrupt processor contains 16 directly controlled modules:

- Minor Loop (ML) - The minor loop module has four functions; (1) to read Platform gimbal angles, to compute yaw, roll, and pitch attitude corrections required to drive the engine gimbals to the desired position, (2) to perform various tests on the Platform gimbal angle outputs to verify the hardware in the LVDA and ST-124 Platform, (3) to ensure that the gimbal angle data and attitude error commands are telemetered by the Data Output Multiplexer, and (4) to access the cutoff logic module when requested.
- Liftoff Search (LO) - The function of the LO module is to monitor the discrete input register for indication of vehicle liftoff (DI24) and on detecting the Discrete Input (DI) access the Time Base 1 module to initiate TB1.
- Switch Selector Processing (SS) - The function of the SS module is to process the switch selector commands issued by the LVDC/LVDA. The module must determine which stage and Switch Selector address is to be actuated, issue the command at the scheduled time, and compensate for any Switch Selector malfunction which may occur in the process of issuing the command.
- Simultaneous Memory Error Recovery (TS) - This module will attempt recovery from a TLC interrupt and provide pertinent data for analysis.
- Digital Command System (DS) - The function of the DS module is to accept and process DCS commands. The DCS provides a limited real-time means of controlling specific flight program timing, navigation, guidance, targeting and sequencing functions and obtaining specific program information.
- Time Base 2 (TB2) - The function of the TB2 module is to initiate TB2 on the occurrence of a scheduled Timer 2 interrupt.
- Time Base 3 (TB3) - This module will initiate TB3 when the S-IC Propellant Depletion interrupt occurs or when the S-IC Outboard Engine Cutoff "B" discrete is detected.
- Time Base 4 (TB4) - This module will initiate TB4 when S-II Propellant Depletion interrupt occurs or when the S-II Engines Out discrete is detected.
- Time Base 5/7 (TB57) - The function of the TB57 module is to check S-IVB cutoff conditions required to initiate TB5 or 7. When all necessary conditions have occurred, the appropriate time base will be initiated.
- Phase I and III Time Update (UM) - This module will update system time and access the minor loop error monitor module.

- Ladder Ramp Processor (LR) - This module will provide the ML module with all data needed to output a predefined ladder ramp profile when operating in Flight Simulation Mode.
- Events Processor (EP) - This module schedules the time of execution of various time based referenced functions. The EP module gives control to the appropriate event submodule which performs the actual function.
- Time Tilt Guidance (TT) - The function of the TT module is to generate steering commands through S-IC burn. TT is entered from Timer 2 when scheduled for time tilt segment change.
- Navigation Update Implementation (NU) - The function of this module is to insert navigation update, state vectors and reschedule the orbital timeline.
- Phase II and IV Control (CM) - The CM module maintains the navigation and guidance timeline for the orbital phases of operation. It is entered from Timer 2 every eight seconds and once each second for navigation and guidance processing, respectively.
- Water Methanol Activate (M. EPWM) - This module is queued-in once to enable water methanol discretes.

11.3.3 APPLICATION MODULES(INDIRECTLY CONTROLLED)

Indirectly controlled modules are described in tables 11.3-1, 11.3-2, and 11.3-3. The tables are referenced to the subprograms of the Executive Control Program. A small number of indirectly controlled modules are multiple listed. This occurs when a module is under direct control of the Control Program and when a module is accessed from modules operating under different control program components. This results from the different timing requirements between boost and non-powered phases of flight.

11.3.4 GENERAL FLOWCHARTS

A general flow of the Saturn V Flight Program is shown in Figures 11.3-1 through 11.3-5. The modules shown are only those which are directly controlled by the control program. Explanations for each modules' queue status is provided beside each module.

Table 11.3-1. Modules Controlled by Non-Interrupt Sequencer Modules during Phase 1 and 3

Module Name	Control Comments
Chi Computations (CC)	Accessed by IGM and by orbit guidance.
Disagreement Bit Processor (DG)	Accessed by minor loop if a gimbal disagreement bit is detected.
Gravitation Acceleration (GR)	Accessed by boost navigation and by orbit navigation each execution.
Variable Launch Azimuth (LA)	Accessed once by phase initialization for Phase 1 initialization.
Digital Output Multiplexer (OD)	Accessed by ETC/BTC each execution.
Steering Misalignment Correction (SM)	Accessed by IGM at a preset time in T_3 and T_6 (Phases 1 and 3).
M/F Smoothing (ST)	Accessed by F M calculations at preset times.

Table 11.3-2. Modules Controlled by Periodic Processor Modules

Module Name	Control Comments
Discrete Inputs 11, 14, and 19 (DP1)	Accessed only during Phase 1 by Discrete Processor if DINs are detected.
Discrete Inputs 13 and 21 (DP2)	Accessed only during Phase 1 by Discrete Processor if DINs are detected.
Discrete Inputs 17 and 22 (DP3)	Accessed by Discrete Processor only during S-II or S-IVB burns when DINs are detected (Phases 1 and 3).
Discrete Inputs 10 and 15 (DP4)	Accessed only during Phase 1 by Discrete Processor upon detecting change in DINs state.
Water Methanol Discrete (DP6)	Accessed by Discrete Processor during all phases (during Phases 2 and 4 accessed on Timer 2 level) upon detecting change in DIS state unless inhibited by DCS.
Second Opportunity Initialize (SO)	Accessed by Discrete Processor during time interval in Phase 3.
Time Base 3 (TB3)	Accessed during Phase 1 by Discrete Processor if time base is initiated by S-IC Outboard Engine Cutoff "B" discrete instead of by interrupt.
Time Base 4 (TB4)	Accessed during Phase 1 by Discrete Processor if time base is initiated by S-II Engine Out discrete instead of by interrupt.
Note: DCS - Digital Command System DIN - Discrete Input DIS - Discrete Input Spare	

Table 11.3-3. Modules Controlled by Interrupt Processor Modules

Module Name	Control Comments
Cutoff Logic (CO)	Accessed by Minor Loop in Phases 1 and 3 when time-to-go to issuance of S-IVB Cutoff Command is less than preset value.
Discrete Processor (DP)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
ETC/BTC (End of Telemetry Cycle/Begin Telemetry Cycle) (EB)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
Minor Loop Error Monitor (EC)	Accessed every 1.6 seconds by Phase I and III Time Update during Phases 1 and 3. Accessed every second by Phase II and IV Control during Phases 2 and 4.
Acquisition Gain/Loss (GL)	Accessed every 8 seconds by Phase II and IV Control during Phases 2 and 4.
Minor Loop Support (MS)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
Navigation Extrapolation (NI)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
Orbit Navigation (NZ)	Accessed every 8 seconds by Phase II and IV Control during Phases 2 and 4.
Orbit Accelerations (OA)	Accessed by Orbit Navigation every 8 seconds during Phases 2 and 4.
Orbit Guidance (OG)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
Phase Activator (PA)	Accessed once in Phase 2 for transition to Phase 3 by the Phase II and IV Control.
One Second Data Compression (PCOI)	Accessed every second by Phase II and IV Control during Phases 2 and 4.
Time-to-go to Restart and Beta Test (RS)	Accessed during Phase 2 every second by Phase II and IV Control.
Time Base 6 (TB6)	Accessed by Time-to-go to Restart and Beta Test.
Phase II and IV Time Update (TU)	Accessed every second by Phase II and IV Control during Phases 2 and 4.

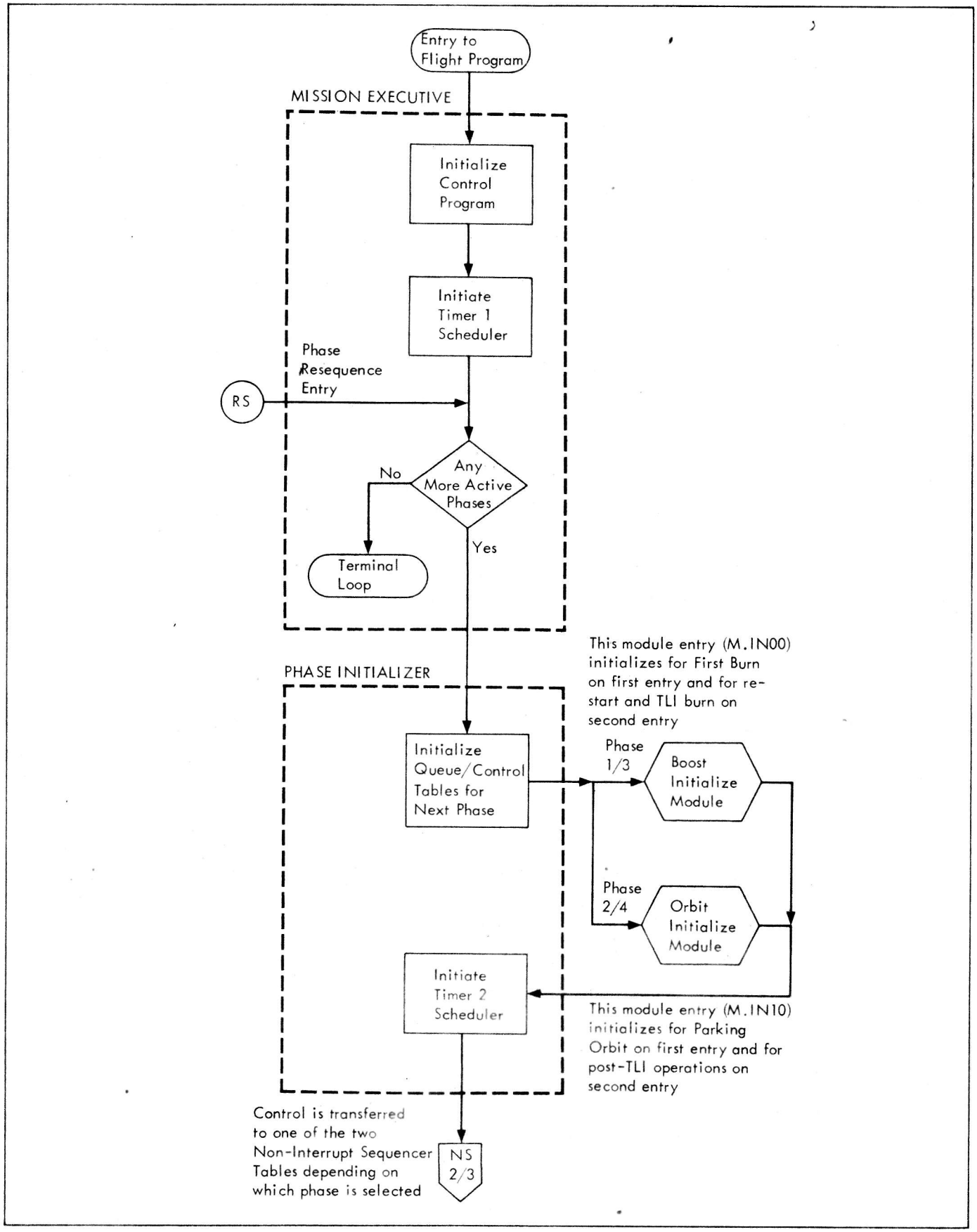


Figure 11.3-1 General Flow of Saturn V Flight Program

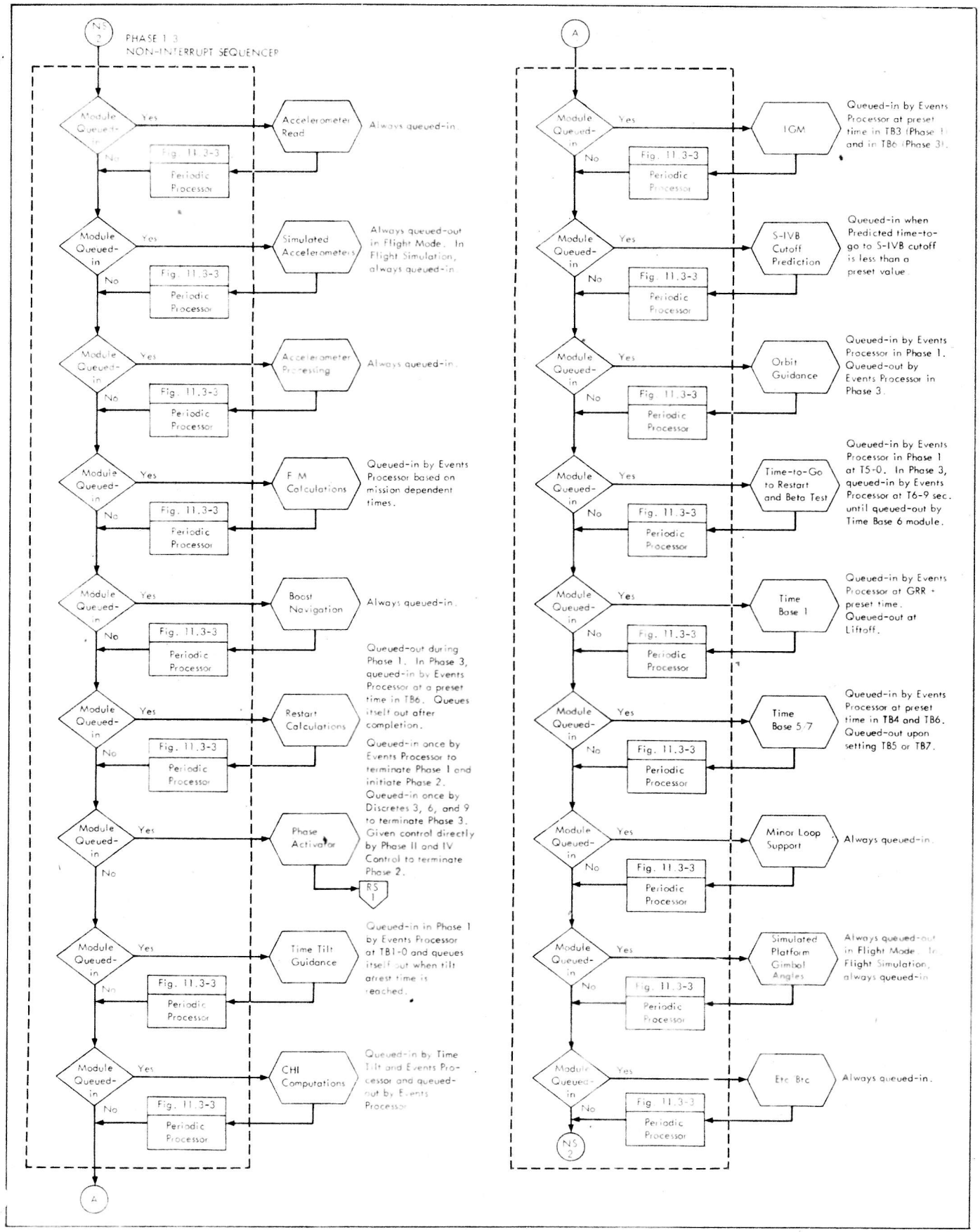


Figure 11.3-2 General Flow of Saturn V Flight Program (Cont)

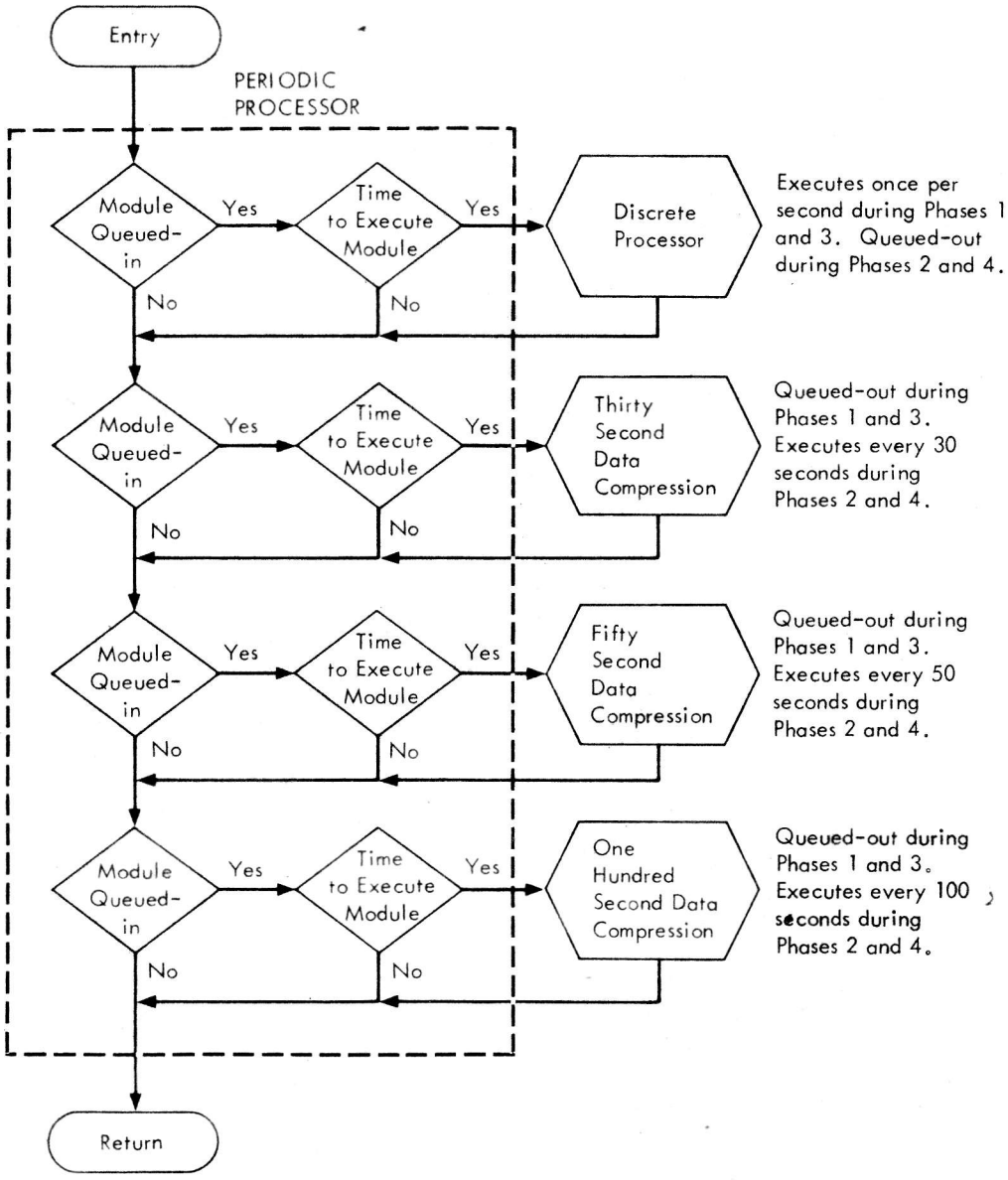


Figure 11.3-3 General Flow of Saturn V Flight Program (Cont)

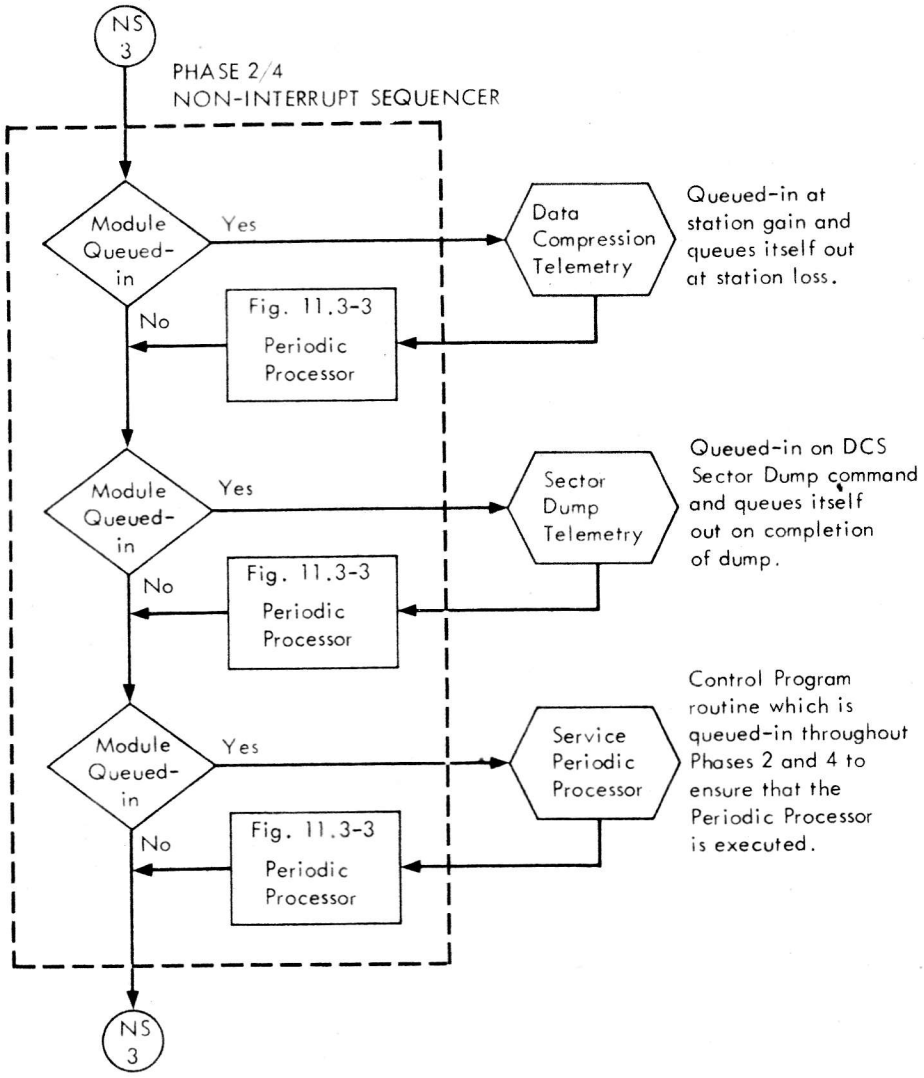


Figure 11.3-4 General Flow of Saturn V Flight Program (Cont)

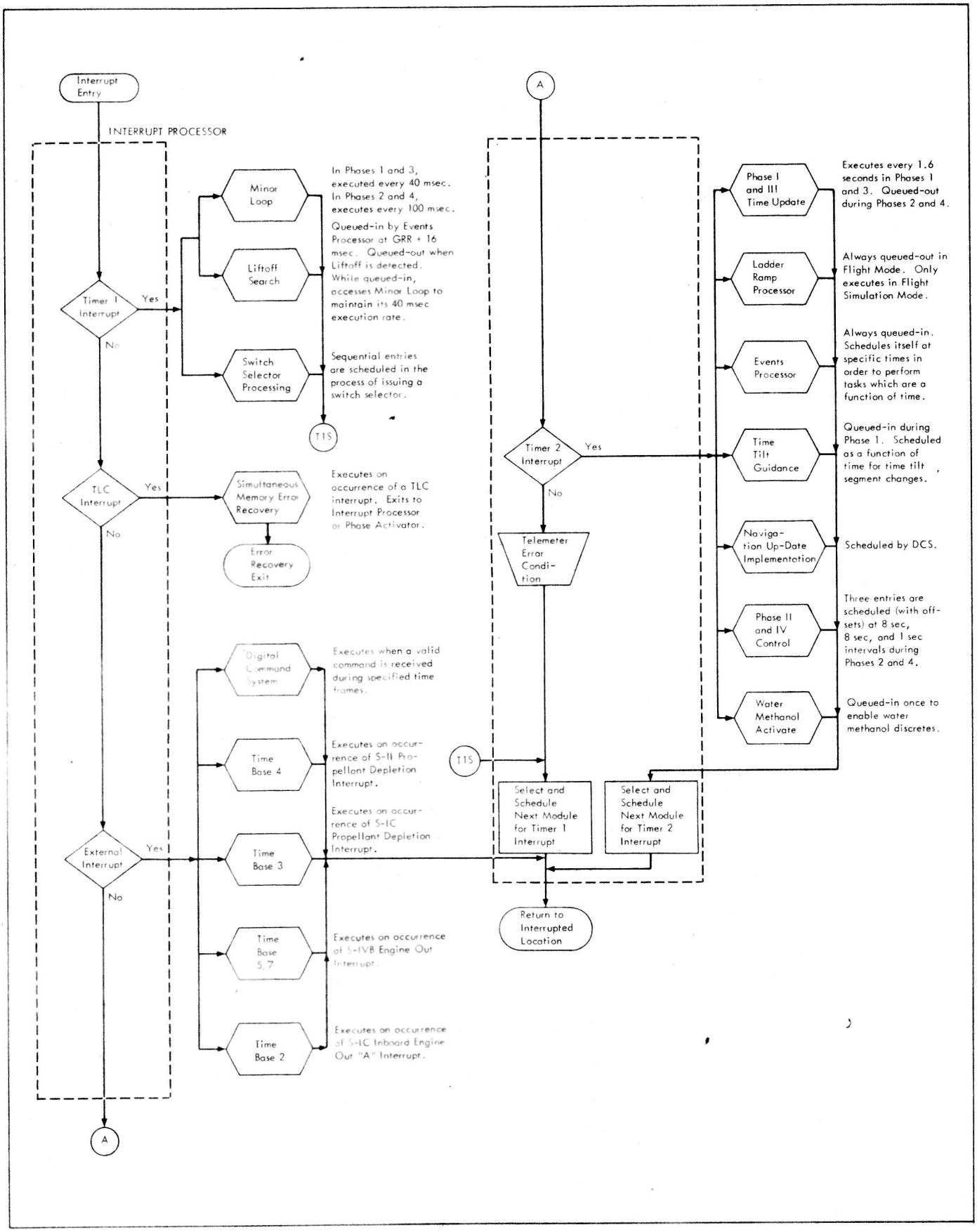


Figure 11.3-5 General Flow of Saturn V Flight Program (Cont)

11.3.5 PROGRAM FUNCTIONAL REQUIREMENTS

The Flight Program is an integral part of: (1) the Guidance and Control System comprising the LVDC/LVDA, ST-124M Inertial Platform, and the FCC (2) the launch vehicle sequencing system comprising the discrete input, discrete output, and interrupt registers of the LVDA and the stage Switch Selectors.

The integration of these systems is accomplished through the Flight Program. It provides a flexible mechanism by which the system functional and detailed specifications may be altered, within wide limits, to accomplish a wide variety of missions without changes to the launch vehicle hardware.

All LVDC inputs and outputs pass through the LVDA. All mention of Flight Program input/output will be interpreted as communication with equipment external to the LVDC/LVDA with the understanding that the external equipment is physically connected to the LVDA rather than the LVDC, and that inputs and outputs are, in actual fact, relative to the LVDC/LVDA hardware and only controlled by the program.

The Flight Program is required to provide for the following primary functions throughout the mission although specific requirements will vary with mission phase:

- Navigation
- Guidance
- Attitude control
- Launch vehicle sequencing
- Telemetry
- Programmed backups to specific hardware functions
- Command processing
- Data compression

In addition to the specifically identified requirements, the routine requirements of "housekeeping" and program sequencing and control exist. However, these are induced requirements of program implementation rather than program requirements and will not be discussed further in the requirements section.

PRELAUNCH AND INITIALIZATION

The prelaunch sequence of events is referenced to the estimated liftoff time. The sequence begins approximately 12 minutes prior to estimated liftoff (T-12 minutes). Until this time, the LVDC has been under control of the Ground Control Computer (GCC) to perform prelaunch functions. At T-12 minutes the RCA-110A issues a "Prepare to Launch" (PTL) command to the LVDC. During the PTL period the LVDC:

- Accepts an initial value for and maintains Greenwich Mean Time.
- Issues a special PIO which keeps all ladder outputs at zero.
- Interrogates the error monitor register.
- Performs the LVDC/LVDA self-test program.
- Monitors the accelerometers and calculates the Platform off-level. The amount of off-level is telemetered once per second.
- Performs reasonableness checks and monitors certain discrete input and interrupts.
- Samples Platform gimbal angles, accelerometers, and time. Telemeters these quantities 6 times per second.
- Perform azimuth calculations for azimuth laying.
- Processes the GRR interrupt and transfers LVDC control to the Flight Program.

At T-187 seconds, the automatic launch is started. At T-22 seconds, the Ground Reference Alert (GRRA) is issued by the Launch Sequencer and sent to the LVDC. This signal terminates the PTL computation cycle by eliminating LVDC Self-Test and Platform off-level computation. At T-17 seconds, the GRR interrupt is sent to the LVDC and program control is transferred to the Flight Program. When the GRR interrupt is received by the LVDC and recognized by the Flight Program, the following events take place:

- Time base zero (T_0) is started.
- Initial acceleration and gimbal angle readings are read and stored.
- The flight azimuth is calculated.
- Calculates parking orbit and translunar injection targeting parameters.
- All flight variables are initialized.
- A discrete output is set to indicate that the Flight Program is in the flight mode and ready for liftoff.

When the initialization is complete, the LVDC begins the navigational calculations and minor loop processing. At T-8.8 seconds, engine ignition is started. At T+0, liftoff occurs and a new time base (T_1) is initiated. Indication of liftoff is provided to the LVDC by a discrete input.

MAJOR LOOP (BOOST)

The Non-Interrupt Sequencer phases 1 and 3 shown in Figure 11.3.2 illustrates the sequence of the modules processed during the boost mode of flight. The various routines are divided into functions and are implemented by the application modules. Depending upon the mode of operation and time of flight, the program will follow the appropriate "path."

The major loop begins with the GRR interrupt (T-17 SEC) when program control is transferred from the RCA-110A to the LVDC stored Flight Program. This step starts the boost initialization mode at T_0. During the first 17 seconds, until T_1 time, the major loop will follow a path through accelerometer processing, boost navigation, minor loop support, discrete processing, and other associated modules. At liftoff (T_1), the flow remains the same as previously described but TT is now included in the loop. The TT computations will continue in a repetitive cycle until the end of the first stage burn. During the second stage burn, the loop will include the same processing as before except the IGM module will replace the TT. The IGM path is implemented during the boost period and any additional launch vehicle burn periods, and is completed when the vehicle enters the earth's parking orbit or is inserted into the target orbit. Upon entering the orbit, the application modules, S-IVB cutoff Prediction, Time Base 5/7, and Orbital Guidance becomes part of the flow path. After S-IVB cutoff, the vehicle is in orbit and the Flight Program now switches to the orbital major loop and the orbital routines.

Accelerometer Processing

The accelerometer processing module, shown in Figure 11.3.2, has two main objectives: to accumulate vehicle velocity as measured by the Platform or through backup profile, and to detect velocity measurement errors through the reasonableness tests.

The velocities measured by the Platform accelerometers are accumulated in counters in the LVDA in increments of 0.05 meter per second. Disagreement, zero, and reasonableness tests are applied to the velocity change in each accelerometer input in order to detect erroneous accelerometer counter readings. If the change passes the previous mentioned tests, the total velocity for each accelerometer is incremented by the change.

The disagreement test compares both the A and B readings of each accelerometer. If the readings of each accelerometer agree within two pulses, the A change reading is used for the zero and reasonableness tests. If they disagree, the reading change closest to the expected change is selected for the zero and reasonableness tests. The expected change (EC) is obtained by an approximate resolution of acceleration through the measured gimbal angles. This value of acceleration used is that which was computed during the last computation cycle.

The selected counter is now tested for zero change. All changes greater than one pulse are considered non-zero and will be tested immediately for reasonableness. Changes of one pulse or less are considered valid if the zero test is disabled or if the EC is less than or equal to Aco where $Aco = 20 (F/M) \Delta T \sin 2^\circ$. A zero change is unacceptable if the zero test is enabled and the EC is greater than Aco where $Aco = 20 (F/M) \Delta T \sin 6^\circ$. The times to enable and disable the zero test are defined in the Events Sequence Timeline table.* All acceptable zero changes will be tested for reasonableness. Unacceptable zero changes are replaced by a backup value derived from $(F/M)c$ acceleration profile.

If the selected change passes the zero test, it is next subjected to the reasonableness test. The change is reasonable if it falls within the ± 50 percent of the expected change enlarged by a reasonableness test constant (RTC) multiplied by the computation cycle length (Δt). Should the selected reading fail the reasonableness test, an appropriate velocity change $(F/M)c$ is computed from the current gimbal angle, Δt, and prestored values of thrust, mass, and mass flow rates. The reasonableness test will not correct the cause of the velocity error but will attempt to prevent such errors from causing corresponding errors in guidance and navigation quantities.

The reciprocal of F/M is computed in the ST application module and is used during the IGM calculations. Due to the nature of digital computations and the low frequency oscillations of fuel slosh, the values of M/F require smoothing to prevent instability in IGM. Filters are utilized to attenuate or reduce

* Located in LVDC Equation Defining Document for Saturn V Flight Programs Part I and II Program Requirements Revision B, MSFC NO. III-4-423-15 and IBM NO. 69-207-0001.

the effects of fuel slosh and to inhibit noisy or oscillatory desired attitude commands computed during IGM. The filter is magnitude and rate limited.

Boost Navigation

The boost navigation module performs the computational process required to determine position, velocity and acceleration needed as inputs to the boost guidance equations. Position is obtained utilizing the following equations. The equations are shown only for the X-axis for reasons of simplicity. Computations for the other axes are identical. All computations are performed in the inertial coordinate system:

$$\Delta Xsg = (Xsg + 1/2\ \ddot{X}sg\ \Delta t)\ \Delta t$$

$$\Delta Xmf = 1/2\left[\dot{X}m + \dot{X}m(past)\right]/\Delta t$$

$$Xs(new) = Xs(past) + \Delta Xsg + \Delta Xmf + \dot{X}o\ \Delta t$$

Where the new value of position (Xs) is the summation of the past position plus the changes in position due to gravitational velocity and acceleration, thrust acceleration, and earth's rotational velocity.

The gravitation subroutine utilizing a Fischer Ellipsoid Math Model evaluates only the round earth and first oblateness terms during boost. The evaluation of gravitation is a three step process. In the first step, the Y component of the vehicle position in the gravitational coordinate system is computed. Next the gravitational acceleration is computed from a zonal harmonic expansion of the earth potential. The third step transforms the gravitational components back into the navigation coordinate system. The accuracy of the navigation routine is not seriously degraded by neglecting the third and fourth terms in the potential expansion. To improve the accuracy, the third and fourth harmonic terms are used during orbital navigation since the total time in orbit is several hours and S-IVB restart depends on the computed vehicle position.

The Boost Navigation Module also performs the computational process to obtain the new values of velocity. The respective equations required to perform the computation in this module are:

$$\dot{X}sg = \dot{X}sg(past) + \left[\ddot{X}sg + \ddot{X}sg(past)\right]\Delta t/2$$

$$\dot{X}s = \dot{X}m + \dot{X}sg + \dot{X}o$$

where space fixed velocity is the summation of the velocities due to thrust, gravity and earth's rotation.

The boost navigation routine is used from GRR until 100 seconds after the first S-IVB cutoff, and again from the beginning of restart preparations until 20 seconds after the second S-IVB cutoff.

Time Tilt Guidance

Time Tilt or first stage guidance deals with the method of generating steering commands (Chi) from GRR to the initiation of IGM.

After liftoff, the trajectory of the vehicle is maintained in a vertical position by maintaining the initial guidance commands at their prelaunch values for approximately 11 seconds. The initial roll angle is established by storing the last roll gimbal angle reading during the Prepare to Launch Routine. At T_1 + 1 second, the vehicle is given a 1.25 degree yaw command to ensure tower clearance. At T_1 + 8.75 seconds, yaw is commanded to zero to return the vehicle to a vertical position and the roll attitude is held constant until the launch umbilical tower is cleared. When a change of position in the Xs direction of 138 meters has been detected, the roll angle is commanded to zero. The roll angle is the angular difference between alignment of the vehicle's position I on the launch pad and the desired flight azimuth. Fin I and position I on Saturn IB vehicles coincide whereas on Saturn V vehicles fin I and position I differ by 45 degrees. In the case of an accelerometer failure and the altitude cannot be accurately determined, a time backup, at approximately 13 seconds, is provided to initiate the roll maneuver. After the roll maneuver is completed, Chi X and Chi Z remain zero while Chi Y is computed by the fourth-degree time polynomial, obtained from a least-square curve fit of the nominal baseline Chi versus time. Rate limiting to keep the rate changes within safe bounds prevents the commanded gimbal changes from exceeding one degree per second.

If an S-IC engine failure occurs during TT, the pitch angle is frozen for a specific time which varies as a function of the time of engine out failure. When the freeze period is completed, the original Chi Y versus time profile is resumed. Tilt arrest occurs at approximately 160 seconds after liftoff. If an engine failure occurs, the tilt arrest time is increased by the duration of the freeze time. After tilt arrest the Chi X and Chi Z commands remain frozen at zero and the Chi Y command is frozen until the initiation of IGM. This freeze continues for approximately 40 seconds of the S-II stage flight to eliminate excessive flight perturbations caused by S-IC burnout and S-II ignition.

IGM Routine

The IGM is so called because of the iterative method of computation used. IGM is normally implemented during two periods of flight. The first period (boost) begins during S-II burn and terminates at first S-IVB cutoff when the launch vehicle enters an earth parking orbit. The second period begins after S-IVB reignition and is completed upon insertion of the vehicle into the target orbit at second S-IVB cutoff.

The function of IGM is to compute the angles necessary to point the vehicle thrust vector along the optimum path to achieve the desired S-IVB cutoff conditions under expected types and magnitudes of vehicle perturbations. The terminal conditions for IGM are constrained by five quantities; (1) radial distance from the center of the earth, (2) velocity magnitude, (3) path angle, (4) inclination of orbit plane, (5) longitude of descending mode of the orbit plane relative to the launch meridian. The velocity, radius, and path angle are in the orbit defined by the inclination and descending mode. Once during each computation cycle, the state of the vehicle (velocity, position, longitudinal acceleration, and gravitational acceleration) is compared with the terminal conditions to determine the deficiency in velocity and altitude. Assuming constant thrust and mass flow rate of the propellant, the IGM scheme computes the direction in which the thrust vector must be pointed to remove these deficiencies in the most optimum fashion before S-IVB cutoff.

The thrust vector steering law ($\chi = a + bt$ is a general form of the equation) on which IGM is based is approximately the optimum steering function for planar motion of a point mass vehicle over a flat earth. The guidance equation for Chi (χ - shown below) is applied in both pitch and yaw planes in IGM to provide three dimensional guidance:

$$\chi z = \tilde{\chi} z - 1/\pi (K_3 - K_4 \Delta T_N)$$

$$\chi y = \tilde{\chi} y - 1/\pi (K_1 - K_2 \Delta T_N) - \phi T - 1/2$$

where

$\tilde{\chi} z$ and χy are the velocity constraints

K_2 and K_4 are the ideal altitude and velocity rate terms.

K_1 and K_3 are the altitude constraints.

ΔT_N is the length of previous computation cycle.

ϕt is the terminal range angle.

In IGM, the terms of the linear thrust attitude law are computed based on averaging the effects of gravity over the range left to travel before cutoff. Since there are no restraints placed on the terminal range, all IGM computations are made in the injection coordinate system so that the flat earth assumptions employed are not violated. The X_v axis of the injection coordinate system is defined by ψt, the total range angle with respect to X_4 axis of the target plane coordinate system. The angle ψt is computed from the range left to travel and the instantaneous range.

The major IGM quantities as previously described must be computed every computation cycle. There are two other quantities which give an indication of the vehicle performance and which are important components in the computation of the above quantities. One is tau (τ) which represents the velocity that can be gained by burning up all of the remaining vehicle mass at a constant mass flow rate. The other is time (T) which is the remaining period until cutoff.

There are several more functions which are associated with IGM. These are the steering misalignment corrections (SMC), terminal steering, S-IVB cutoff command and coordinate transformation. SMC terms are used to account for the fact that the thrust vector and the longitudinal axis of the vehicle may not be collinear. The IGM scheme has inherent instability as the time left to burn approaches zero which requires modification of the method to compute the steering commands as cutoff is approached. A special method is used to determine when the velocity constraints will be satisfied for issuing the S-IVB cutoff command. IGM computations are performed in the injection coordinate system whereas the state of the vehicle is determined in the inertial coordinate system. Thus it is required to transform between the two systems.

Minor Loop Support

Minor loop support functions consist of computing attitude change increments and the coefficients for the gimbal-to-body transformation to be used in the minor loop. Desired attitude commands (χ'_x, χ'_y, χ'_z will be computed each minor loop by adding the fixed increments ($\Delta\chi'_x$, $\Delta\chi'_y$, $\Delta\chi'_z$) to the previous attitude command values. These attitude increments

will be computed by dividing the difference between the guidance commands (χ_x, χ_y, χ_z) and the present minor loop attitude commands by the number of times the attitude commands are to be incremented between minor loop support computations.

The attitude increments must be magnitude limited to provide rate limiting on the minor loop attitude commands and prevent divergence between the desired and actual vehicle attitudes.

The number of times the attitude commands are to be incremented and the values of the pitch, yaw, and roll attitude increment limits for all periods of flight are listed in the Event Sequence Timeline.

The attitude errors are computed in the Inertial Platform gimbal system and must be transformed in the minor loop to provide attitude error signals in the body-reference frame. To compensate for the changing relationship between the two reference frames, the average roll and yaw attitude angles predicted for the next computation cycle must be used to calculate the coefficients.

Discrete Backups

The Discrete Backup processing routine is primarily an operational routine during boost mode to ensure that discrete events, commanded by the LVDC and scheduled with time, occur. The sequencing is performed by comparing elapsed time with the scheduled time for the events. Events are referenced to some critical flight event, hence time must be accumulated from these events. Each critical event causes a time base to be started. The indication that the critical event has occurred is given to the LVDC by either an interrupt, a discrete input or computed conditions. Because of the criticality of the establishment of these time bases, Flight Program backups are provided to initiate the time bases. For Saturn V vehicles, there are eight major time bases. Alternate time bases are provided to be used as contingency backups and may vary from mission to mission. The major critical events or time bases are:

T_0 GRR initiation

T_1 Liftoff (LO)

T_2 S-IC Inboard Engine Cutoff (IECO)

T_3 S-IC Propellant Depletion/Engine Cutoff

T_4 S-II Propellant Depletion/Engine Cutoff

T_5 S-IVB Cutoff (Boost)

T_6 S-IVB Restart Preparation

T_7 S-IVB Cutoff (Orbital Phase)

T_8 Slingshot and Passivation

Time Base 1 is initiated by a liftoff discrete provided by the liftoff relay in the IU at umbilical disconnect. The program will not start T_1 or recognize the discrete until 16 seconds after T_0. As a backup, if the vertical acceleration exceeds 2 meters per second per second for four computation cycles, liftoff is assumed and T_1 is begun. If a vertical acceleration greater than $2M/Sec^2$ is not sensed for four computation cycles prior to 150 seconds after T_0, a one instruction loop is executed and T_1 cannot start.

Time Base 2 is initiated by the S-IC Inboard Engine Out "A" interrupt. Backup for T_2 is S-IC Inboard Engine Out "B" discrete. The downrange velocity is checked after the backup discrete is reorganized. If sufficient downrange velocity exists, the LVDC will issue T_2. The checking of the downrange velocity is a safeguard against starting T_2 should T_1 be started without liftoff. If T_2 is not started, the other time bases cannot be started.

Time Base 3 is initiated in response to the S-IC Propellant Depletion/Engine Cutoff interrupt which indicates that the outboard engines have been cut off. S-IC outboard engine cutoff discrete provides a backup to initiate this time base.

Time Base 4 is started at S-II engine cutoff in response to the S-II Propellant Depletion/Engine Cutoff interrupt which indicates that the propellant level has reached a certain level and the S-II cutoff sequence has been initiated. The cutoff sequence itself is initiated and executed within the stage upon receipt of the depletion signal from the propellant level sensors. This interrupt will be honored only after the propellant depletion arm signal is given. Backup for this interrupt is provided by the S-II Engine Out discrete.

Time Base 5 is initiated by S-IVB cutoff. There are four conditions which serve as inputs to the cutoff logic. These conditions are S-IVB Engine Out interrupt, S-IVB Engine Out discrete, S-IVB velocity cutoff, and low accelerometer pulse count. Any two or more of these conditions are recognized by the logic as an indication to start Time Base 5.

Time Base 6 is not processed in the time base routine but will be initiated by the LVDC when it solves the restart equation or upon LVDC receipt of the S-IVB Ignition Sequence Start signal from the spacecraft during spacecraft control.

Time Base 7 is started at the second cutoff to the S-IVB. The processing for initiating Time Base 7 is identical to conditions previously described for Time Base 5. Time Base 8 is started via receiving the DCS command.

Since Switch Selector outputs are a function of time (relative to one of the time bases), no Switch Selector output is generated if one of the discrete signals is missing. The backup routine is provided to avoid this condition and to ensure proper sequencing of events. The backup routine will force the program into the correct time base if the critical signals do not occur when they are expected.

MAJOR LOOP (ORBITAL)

The Non-Interrupt Sequencer phase 2 and 4 and Periodic Processor shown in Figures 11.3-3 and 11.3-4 illustrate the application modules processed during orbital mode. During orbital flight when the vehicle is not over a ground station, the data that has been stored by the LVDC since loss of previous station as well as real-time data presently being calculated must be telemetered.

Navigation, guidance, and attitude control functions are carried out on a regular basis under control of the Interrupt Processor. Orbital navigation is performed every 8 seconds and orbital guidance is performed every second. This sequence of operations is performed under the function of the Phase 2 and 4 Control Module. Event sequencing is carried out by the Switch Selector Processing Module in response to the Switch Selector interrupt. Ground commands are processed in response to the Digital Command Module which has an interrupt priority below that of the minor loop and the Switch Selector.

INTERRUPT PROCESSING

The LVDC has a feature which permits interruption of the normal functions performed in the major loop to free the computer for priority work. When such a priority task arises, an interrupt is generated. Refer to Figure 11.3-1. This transfers control to a special routine upon completion of the instruction then being executed. This special routine establishes the mechanism for eventual return to the main program, identifies the source of the interrupt, and then transfers control to the routine which performs the functions required by the interrupt. During this period, all other interrupts are inhibited with the exception of the temporary loss of control (TLC) interrupt. The intervention of a TLC is permitted during the processing of any interrupt except a previous TLC.

When the program recognizes an interrupt, it first checks to see if it resulted from a TLC. If not, the program then checks for a minor loop (Timer 1) interrupt. This is done under program control independent of the logical priorities of the respective bits in the interrupt storage register; the minor loop interrupt bit in the storage register is a higher order bit than the TLC bit. If the source of the interrupt is not a minor loop, the computer systematically determines the source of the interrupt by examining the remaining bits in the register. Regardless of the type of interrupt recognized by the program, the interruption can occur at any point in the major loop. If for example, the interrupt occurs during the 50th instruction of the boost navigation routine, the specific instruction would be completed, the program would branch to the interrupt routine, perform the required operation and return to the 51st or next instruction of the boost navigation routine. The performance of the boost navigation routine would not be affected in any way except for the small delay required to perform the interrupt routine. When processing of the interrupt is complete and control is returned to the main program, the interrupt inhibits are removed. If time is within 60 milliseconds of S-IVB cutoff, only the Switch Selector interrupt inhibit is removed so the S-IVB cutoff can occur at exactly the correct time. If S-IVB cutoff is not eminent, all interrupt inhibits are removed.

The LVDC/LVDA has provision for 12 interrupts. Interrupt Processor Section 11.2 lists the four basic levels of interrupt priorities.

With the exception of the minor loop interrupt, which is discussed in a separate section, a brief description of the remaining interrupts is given below:

- Switch Selector Interrupt (Timer 2) - This interrupt is used to initiate the Switch Selector processing routine. The processing routine provides a convenient and accurate means for sequencing internal program events and issues the output commands necessary to actuate the Switch Selector hardware.
- Temporary Loss of Control (TLC) Interrupt - A TLC interrupt indicates that simultaneous memory failures have occurred in both memory core A and B. After processing of this interrupt the Flight Program will return to accelerometer processing routine if in boost, or to the beginning of orbit initialize if in that routine.

- Command Decoder Interrupt - This interrupt conditions the LVDC to accept commands from ground stations to modify or execute Flight Program functions.
- Guidance Reference Release (GRR) Interrupt - This interrupt indicates that the Platform has been released. It occurs 17 seconds prior to liftoff and is the point at which program control is transferred to the Flight Program.
- S-II Propellant Depletion Interrupt - This interrupt indicates that propellant has reached a certain level in the tanks and the S-II cutoff sequence has been initiated. Time Base 4 is initiated in response to this interrupt.
- S-IC Propellant Depletion Interrupt - This interrupt indicates that the S-IC outboard engines have been cut off. Time Base 3 is initiated by this cutoff.
- S-IVB Engine Out Interrupt - This interrupt indicates to the LVDC that S-IVB cutoff has occurred. Four inputs to the cutoff logic must be implemented prior to issue of interrupt.
- Program Recycle (RCA-110A) Interrupt - This interrupt applies only to ground routines and is inhibited throughout flight. The interrupt, when issued, terminates ground routines involved in a loop.
- S-IC Inboard Engine Out "A" Interrupt - This interrupt indicates LOX or fuel low level. Time Base 2 is initiated by this interrupt.
- Command LVDA/RCA-110A Interrupt - This interrupt formerly applied only to the ground routines. The interrupt is no longer used and is classified as a spare.

MINOR LOOP OPERATION

The minor loop, which is initiated as a Timer 1 interrupt, is shown in Figure 11.3.5 as part of the Interrupt Processor flow. The prime function of the minor loop is to perform the computations necessary to control vehicle attitude. The launch vehicle attitude, in the form of angular displacements measured by Inertial Platform gimbal resolvers, will be read into the LVDC through LVDA hardware. The attitude error must be computed by differencing the attitude angles with the desired attitude angles computed by the guidance equations. The resulting attitude error must be transformed to the body reference frame, limited in magnitude and rate of change, and issued to the flight control system.

The control functions of determining vehicle attitude and computing and issuing attitude error commands are called the minor loop. These functions must be performed 25 times per second during boost and 10 times per second during orbit. The supporting control functions of computing attitude change increments and coefficients for the gimbal-to-body transformation required for attitude error command computations are called minor loop support functions. These functions must be performed once per computation cycle during boost and once per second during orbit.

The minor loop samples the yaw gimbal resolver, evaluates the yaw gimbal resolver data, computes the yaw attitude angle, and computes and issues the yaw attitude error command. This process must then be repeated for the pitch and roll gimbals.

Minor loop functions are performed every 40 ms during boost and every 100 ms during orbit. The tolerance on the time between minor loops is less than plus 2 ms or minus 1 ms. However, the start of a minor loop may be delayed if interrupt-protected processing is underway. During boost, occasional delays of up to 8 ms may result from interference by switch selector processing and a delay of up to 60 ms may occur just prior to each S-IVB cutoff. In orbit, minor loops may be delayed up to 12 ms by command decoder-interrupt processing.

REAL-TIME TELEMETRY AND DATA COMPRESSION

The Flight Program provides telemetry for both real-time analysis and post flight evaluation. Continuous real-time telemetry must be generated throughout the mission. During periods of orbital navigation, certain quantities must be sampled, tested, and stored according to specified norms. This compressed data must be stored in LVDC memory and transmitted during acquisition of designated telemetry dump stations, after the real-time telemetry has been processed.

During periods of station acquisition, certain priorities are assigned to the data being telemetered. Real-time data has the highest priority. This data originates in the LVDC and LVDA and is telemetered at a maximum rate of 240 words per minute. Three

types of telemetry words are transmitted as real-time data with the following priority:

- LVDC telemetry - consist of quantities calculated in the LVDC such as positions, velocities, guidance commands, mode code words, etc.
- Error data words - error words are generated automatically by the LVDA each time a bit is set in the Error Monitor Register.
- LVDA (DOM telemetry) - these telemetry words include gimbal angles, attitude commands, accelerometer inputs, digital inputs and digital outputs.

Real-time data is telemetered one word at a time until the station is lost or until all the real-time data is sent. The Digital Command System can command the sector dump routine once all the real-time data has been sent. This routine provides the capability for commanding the program to telemeter the entire contents of one LVDC memory sector (17 words) or a series of memory sectors within the same memory module.

Navigation computations are made once per major loop during the boost mode and once per 8 seconds during orbital mode. All specified navigation quantities must be telemetered each time they are computed and within the same computation cycle. These quantities include the position, velocity, and acceleration vectors due to thrust, gravitation, and initial conditions.

The guidance commands, the changes in the guidance commands and the time that these updates are valid, and the attitude of the vehicle must be telemetered once per major loop during boost mode and once per second during orbital mode.

The accelerometers must be read in both boost and orbital modes. In boost, the accelerometer readings are used in navigation computations; in orbit, they are read for telemetry purposes only.

During orbital mode, significant time intervals will occur during which the vehicle will be out of electromagnetic view of a telemetry dump station. During these intervals, data must be processed and stored in the LVDC for later transmission when the vehicle comes within electromagnetic view of the next telemetry dump station. The processing and storing of these data is referred to as data compression.

Data to be compressed are divided into three groups:

- Group A - time compressed data, in which quantities are sampled and stored at regular intervals. Data in this group includes fine and backup gimbal angles, and accelerometer outputs.
- Group B - occurrence compressed data, in which data describing certain events is stored when the events occur. Data is this group include discrete inputs, outputs and interrupt descriptions, TLC HOP (computer instruction) constants, Switch Selector stages and addresses.
- Group C - amplitude compressed data, in which regularly sampled quantities are stored only when they change by more than a prescribed amount. Data in this group includes error monitor register contents, mode code 28 discrete inputs and discrete input spares.

CHAPTER 12
INSTRUMENT UNIT

SECTION 12.1
INTRODUCTION

The Instrument Unit is a cylindrical structure 6.6 meters (260 inches) in diameter and 0.9 meters (36 inches) in height, mounted on top of the S-IVB Stage as illustrated in Figure 12.1-1. The IU is attached to the S-IVB Stage and to the Spacecraft/Lunar Module Adapter (SLA) and remains attached to both after Command and Service Module (CSM) and Lunar Module (LM) separation.

The IU contains the equipment necessary to:

- Perform guidance and control of the vehicle from liftoff through CSM and LM separation
- Aid in radar tracking of the vehicle
- Provide a command link for ground control of the vehicle
- Provide temperature control for the electronic equipment in the IU and the S-IVB Stage forward skirt. Instrumentation is provided to monitor performance of this equipment.

Before liftoff, connections from the IU to ground support equipment are made through quick disconnect couplings at the IU umbilical plate. Access to equipment in the IU, LM, and S-IVB Stage forward skirt is provided through a door in the IU structure. The access door has been designed to act as a load carrying part of the IU. The umbilical plate is located next to the access door. An externally mounted, spring-loaded door automatically shuts over the umbilical plate to prevent contamination and possible fouling of connectors when the umbilical pulls loose at launch.

The principal components in the IU structure are bolted together to form a cylindrical ring. The basic structure is comprised of three 120-degree segments. Each segment is made by bonding an outer surface sheet and an inner surface sheet to an aluminum honeycomb core. Each segment contains the inserts, pads, and brackets required to mount the IU equipment. The top and bottom edges of the structure are aluminum alloy channels bonded to the honeycomb core and surface sheets. The combined thickness of the structure is 2.42 centimeters (0.95 inch).

Electrical cables used to interconnect equipment mounted on the IU structure are supported by a cable tray. The cable tray, made of aluminum alloy tubing, is mounted above and around the inside of the IU structure. The cable tray also supports the ducts used in the IU purge system.

The IU equipment is secured to the structure by bolting directly to the structure or by bolting to thermal conditioning panels attached to the structure.

The combined weight of the IU structure, Astrionics equipment, and environmental control equipment is 4200 pounds.

Typical arrangement of the equipment in the IU for operational and R & D Saturn Vehicles is illustrated on Figure 12.1-2 through 12.1-7.

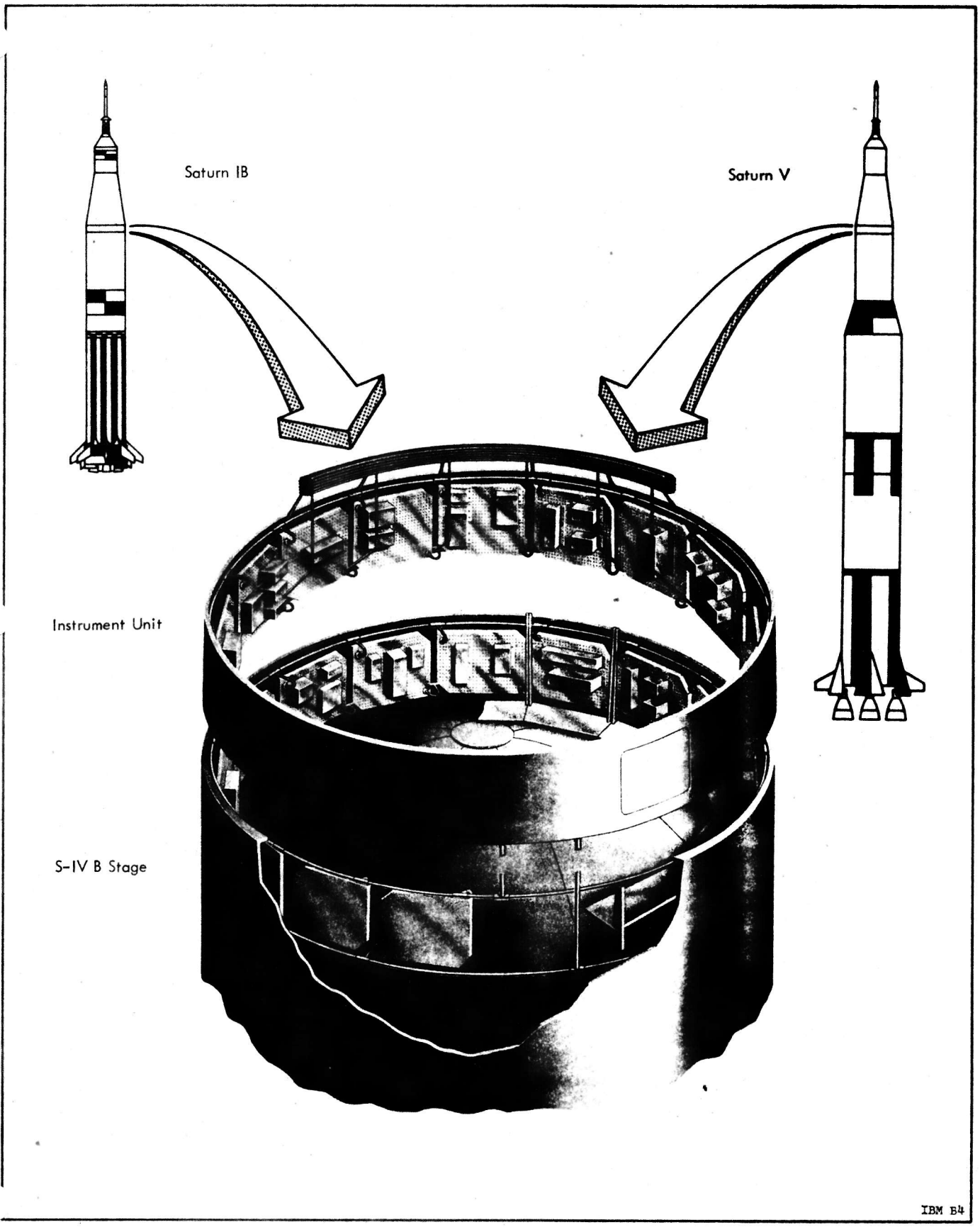


Figure 12. 1-1 Saturn IB and V Instrument Unit Physical Location

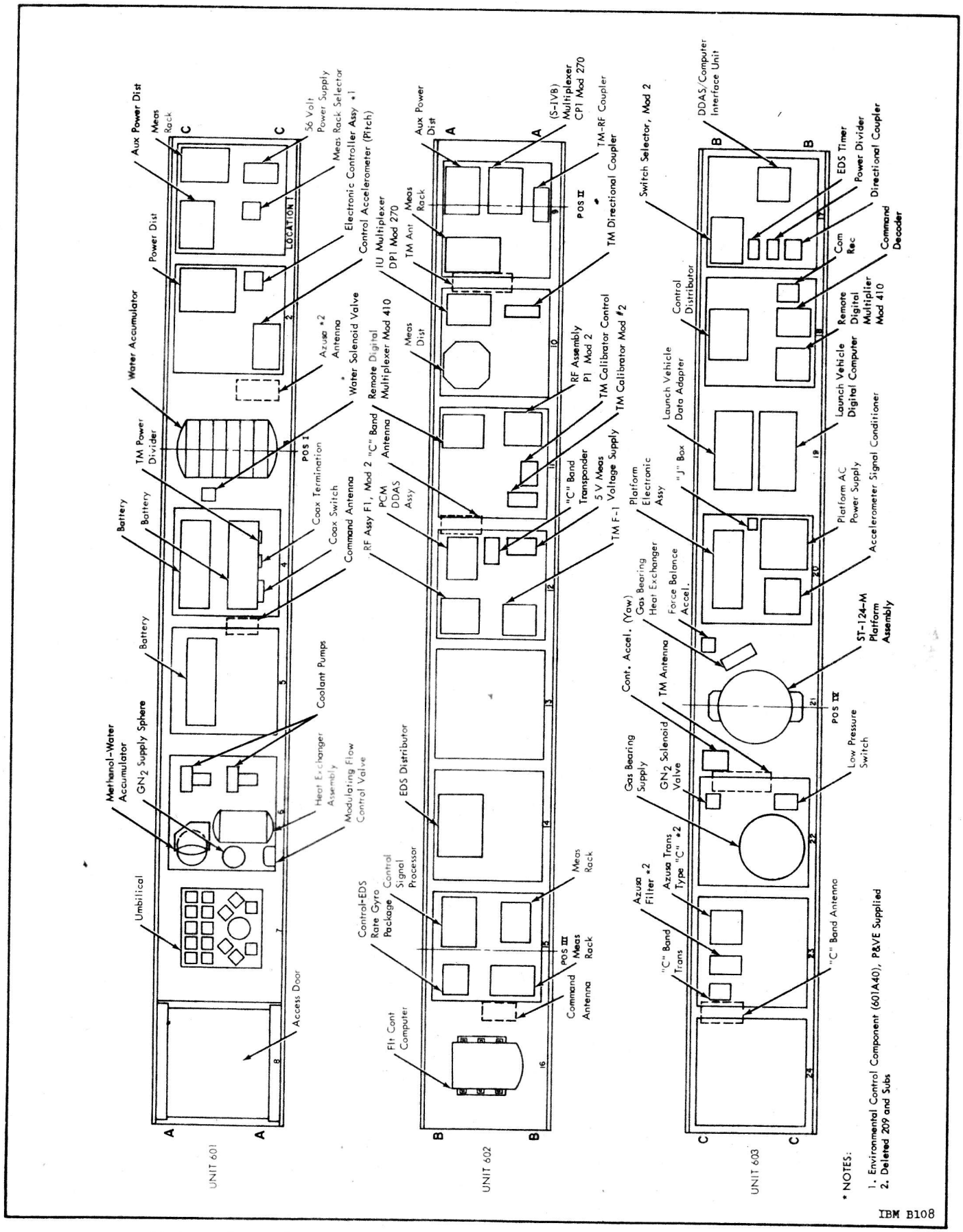


Figure 12.1-2. Saturn IB Instrument Unit Equipment Layout, Typical Operational Vehicles

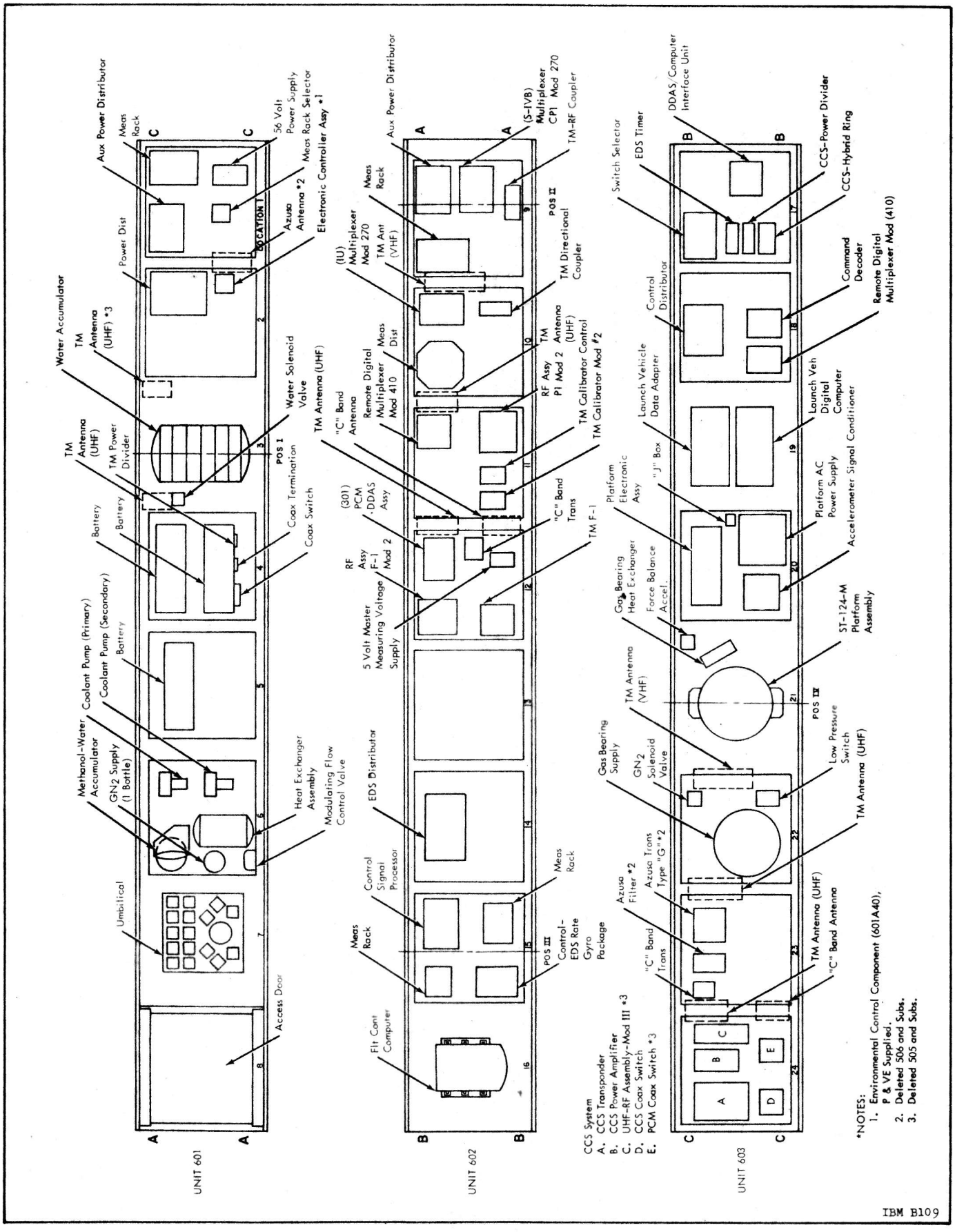


Figure 12.1-3. Saturn V Instrument Unit Equipment Layout, Typical Operational Vehicles

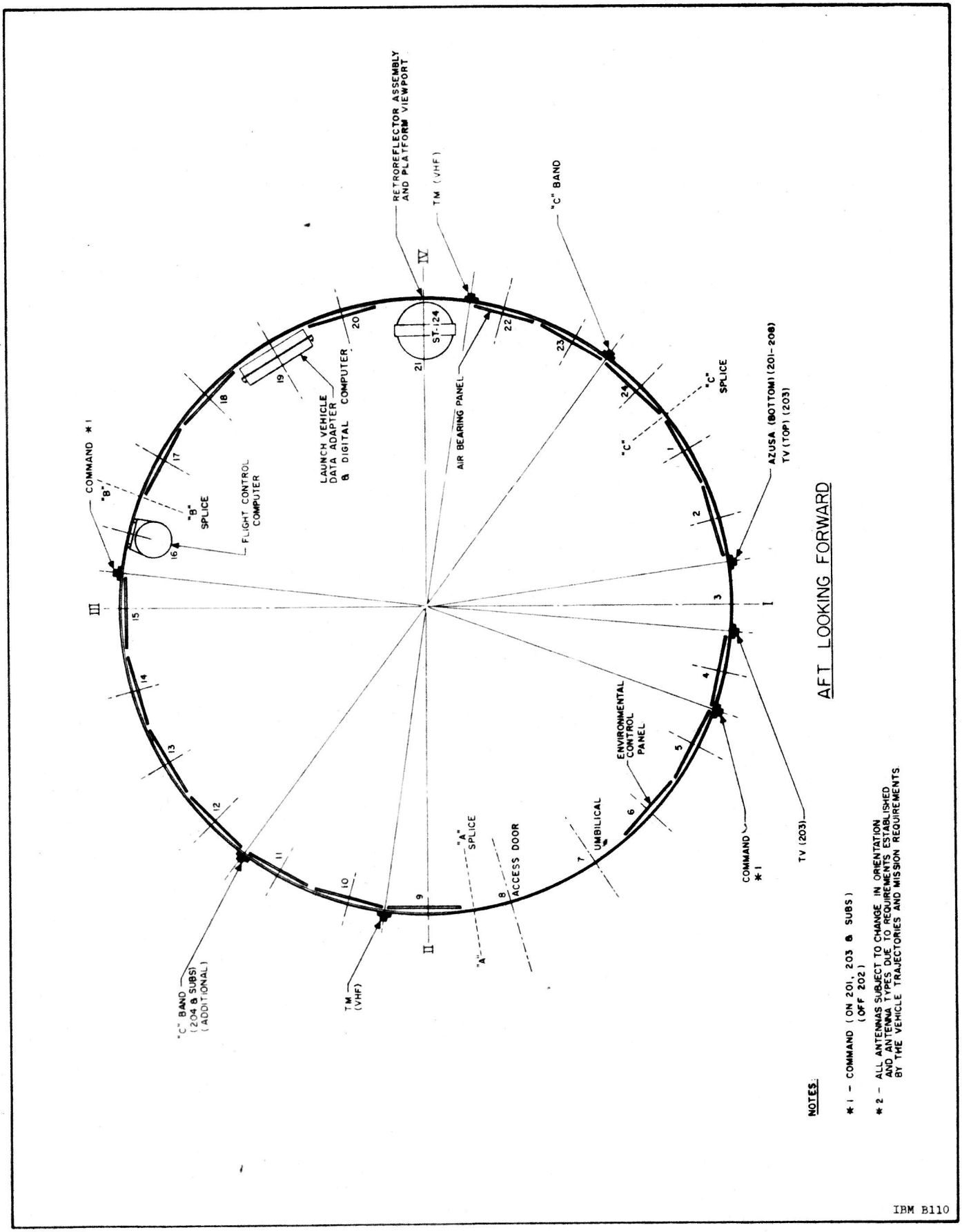


Figure 12.1-4. Saturn IB Instrument Unit Equipment Layout, Typical Antenna Orientation

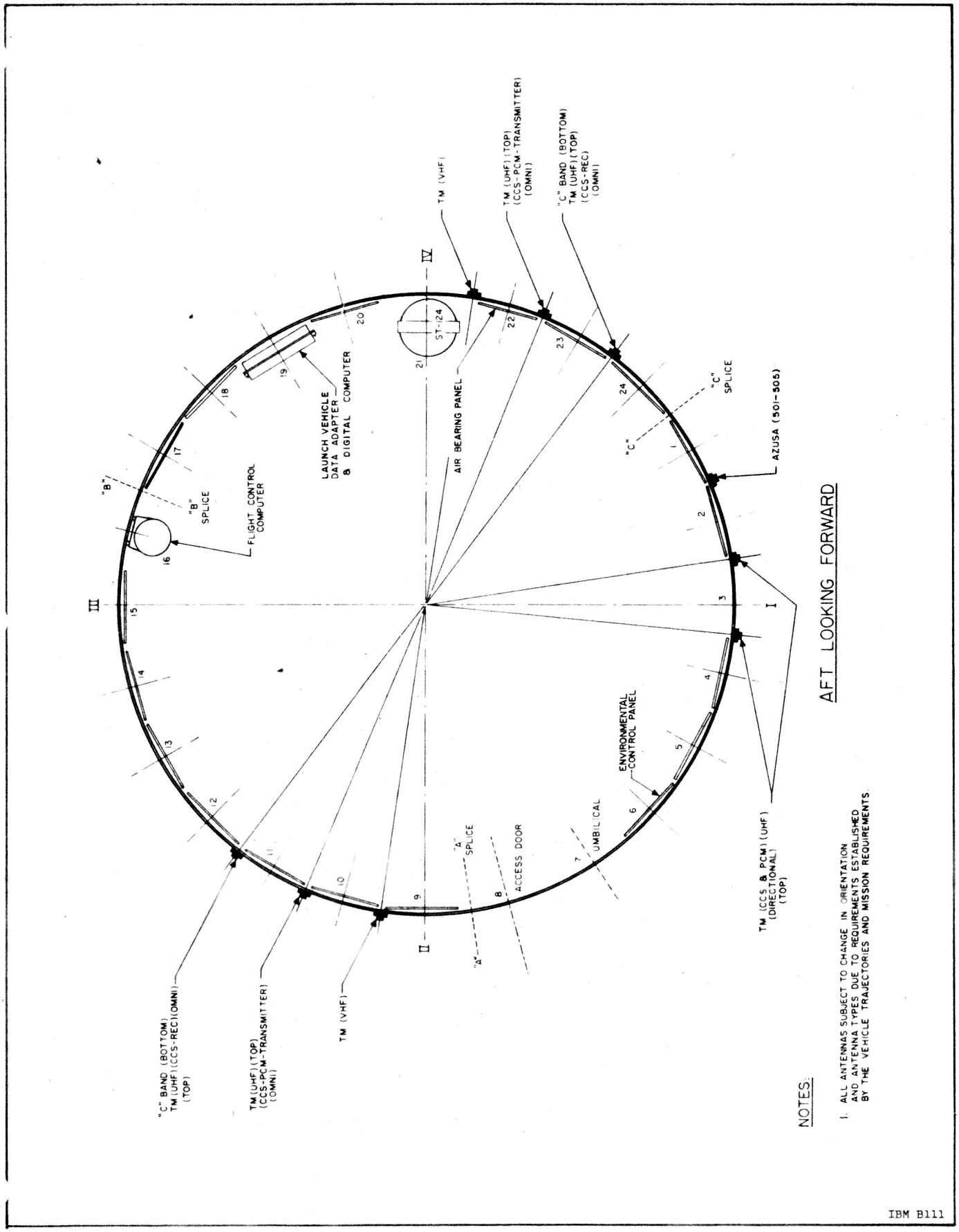


Figure 12.1-5. Saturn V Instrument Unit Equipment Layout, Typical Antenna Orientation

CHAPTER 13
ENVIRONMENTAL CONTROL SYSTEM

SECTION 13.1
THERMAL CONDITIONING SYSTEM

A thermal conditioning system is provided in the S-IVB Stage forward compartment and the Instrument Unit of the Saturn Launch Vehicles. The thermal conditioning system heats or cools the Astrionics equipment as required during prelaunch and flight.

The thermal conditioning system contains 16 thermal conditioning panels (cold plates) in the S-IVB Stage and 16 in the Instrument Unit. Most of the equipment which requires thermal conditioning is mounted on cold plates; however, some equipment such as the Launch Vehicle Digital Computer and Data Adapter have integral coolant passages and are not mounted on cold plates. Each cold plate measures 76.2 centimeters by 76.2 centimeters (30 inches by 30 inches) and contains tapped bolt holes positioned on a 5.1-centimeter (2-inch) square grid. (A cold plate is illustrated in Figure 13.1-1.) This hole pattern permits maximum flexibility of component mounting on the cold plates.

A coolant fluid of 60 percent methanol, 0.1 percent sodium benzoate, and 39.9 percent water by weight is circulated through the cold plates and equipment having integral cooling passages. Each cold plate is capable of dissipating approximately 420 watts.

A diagram of the environmental control system is shown in Figure 13.1-2. The manifold and methanol-water accumulator are filled with coolant through either of the quick disconnects at the S-IVB/IU interface. The methanol-water accumulator provides damping of pressure fluctuations, a constant coolant pump inlet pressure, and compensation for thermal expansion of the coolant, and supplies additional coolant should any be lost.

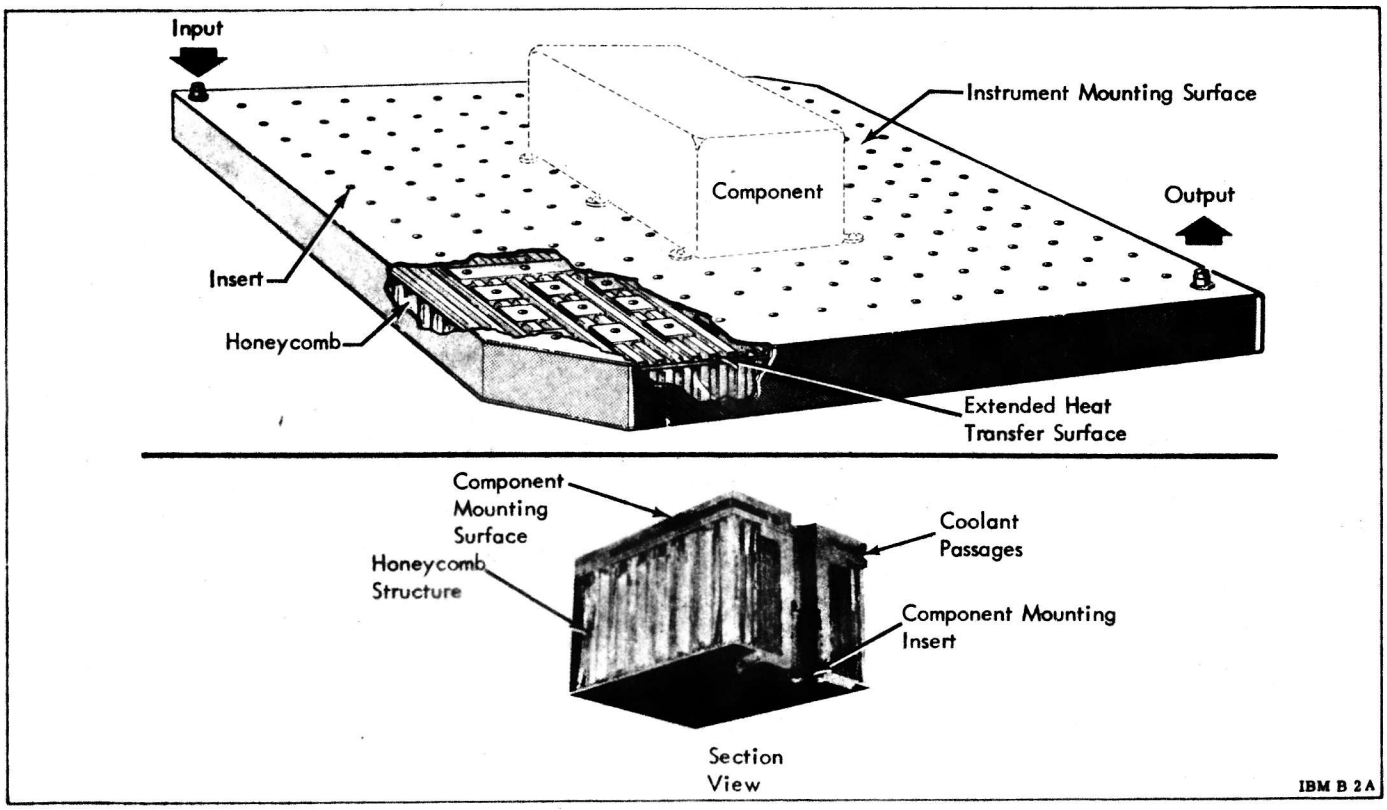


Figure 13.1-1 Thermal Conditioning Panel Details

The menthanol-water accumulator and water accumulator are pressurized with gaseous nitrogen (GN_2) that is stored at 20.7 x 10^6 N/m^2g (3000 psig) in the 2690-cubic-centimeter (165-cubic-inch) storage sphere. The GN_2 is filtered by filter A, the pressure reduced to approximately 114 x 10^3 N/m^2a (16.5 psia) by the pressure regulator, and then applied to the methanol-water accumulator. The orifice regulator reduces the 114 x 10^3 N/m^2a (16.5 psia) GN_2 pressure to 34.5 x 10^3 N/m^2a (5 psia), and this pressure is used to pressurize the water accumulator. The orifice regulator vents GN_2 into the Instrument Unit compartment to maintain constant pressure on the water accumulator. A flexible membrane is contained within both accumulators and provides a barrier that prevents mixing of the GN_2 and the liquid.

The bleeder assembly is opened during filling of the methanol-water and water accumulators. This provides an escape port for air which could otherwise be trapped and allows the flexible membranes in the accumulators to retract.

Filling of the water accumulator is accomplished manually by pouring water into the accumulator through the water fill port. The flow of water from the water accumulator to the flight heat exchanger (sublimator) is controlled by water solenoid valve C. This valve is energized (closed) during prelaunch operations since cooling of the methanol-water coolant is accomplished by the preflight heat exchanger.

Filling of the 165-cubic-inch storage sphere with GN_2 is controlled by GN_2 solenoid valve A. A high pressure source of GN_2 is applied to the GN_2 supply and emergency coupling vent quick disconnect. A pressure transducer indicates when the sphere is pressurized to the proper value. At this time, GN_2 solenoid valve A is deenergized (closed). The solenoid valve also provides for the venting of the system during prelaunch operations, if required.

During prelaunch operations, the methanol-water coolant is circulated through a closed-loop system by electrically driven, redundant coolant pumps. Coolant pump No. 2 is a backup pump used only if the fluid pressure drops below 248 x 10^3 N/m^2a (36 psia). At this pressure level, a pressure switch closes and the pumping operation is transferred from coolant pump No. 1 to coolant pump No. 2. Check valves prevent fluid flow through the inoperative pump. The coolant flows past the coolant temperature sensor, through the orifice assembly, and then through the cold plates, gas bearing heat exchanger, and internally cooled equipment within the Instrument Unit. The orifice assembly diverts a portion of the coolant to the cold plates in the S-IVB Stage. The coolant in the return line either passes through the sublimator and preflight heat exchanger to the pumps or flows through the bypass line to the pumps, thus completing the closed loop. The orifices shown in the LVDA, LVDC, and Flight Control Computer lines maintain the proper coolant flowrate through their respective component.

The coolant temperature sensor, located near the pump outlet, senses the coolant temperature and supplies an electrical signal to the Electronic Controller Assembly which controls the modulating flow control valve. The modulating flow control valve diverts varying amounts of coolant through the sublimator and preflight heat exchanger if the coolant requires cooling. If the coolant requires no cooling, an appropriate quantity of coolant is bypassed around the sublimator and heat exchanger.

As previously mentioned, during prelaunch operations the sublimator is inactive and the preflight heat exchanger cools the closed-loop coolant. A temperature controlled methanol-water mixture, supplied by the ground support equipment, is circulated through one section of the preflight heat exchanger, thus cooling the closed-loop coolant that flows through the other section.

During flight, the operation is the same except that the sublimator is active and the preflight heat exchanger is inactive. However, the sublimator does not operate until approximately 180 seconds after liftoff, at which time the ambient pressure is low enough to sustain sublimation. Calculations indicate that during the transient phase, the thermal capacity of the electronic equipment and thermal conditioning system is sufficient to prevent over-heating of the equipment.

The temperature of the closed-loop coolant is controlled during flight by controlling the water flow from the Water Accumulator to the Sublimator. When the IU ambient pressure is low enough to sustain sublimation and the closed-loop coolant temperature is above approximately 16.1 °C (61 °F), water solenoid valve C is de-energized (opens) allowing water to flow from the water accumulator to the sublimator. Water under pressure enters the sublimator and flows into the pores of the porous plate. As the water in the pores encounters the space vacuum at a temperature and pressure below the triple point of water, an ice layer forms at the outer water surface and continues to build-up back towards the water passage. As heat is transferred through the water passage and ice layer, the outer suface sublimes. As the heat level is increased, the ice sublimes at a faster rate, increasing the water flow rate. The converse is also true.

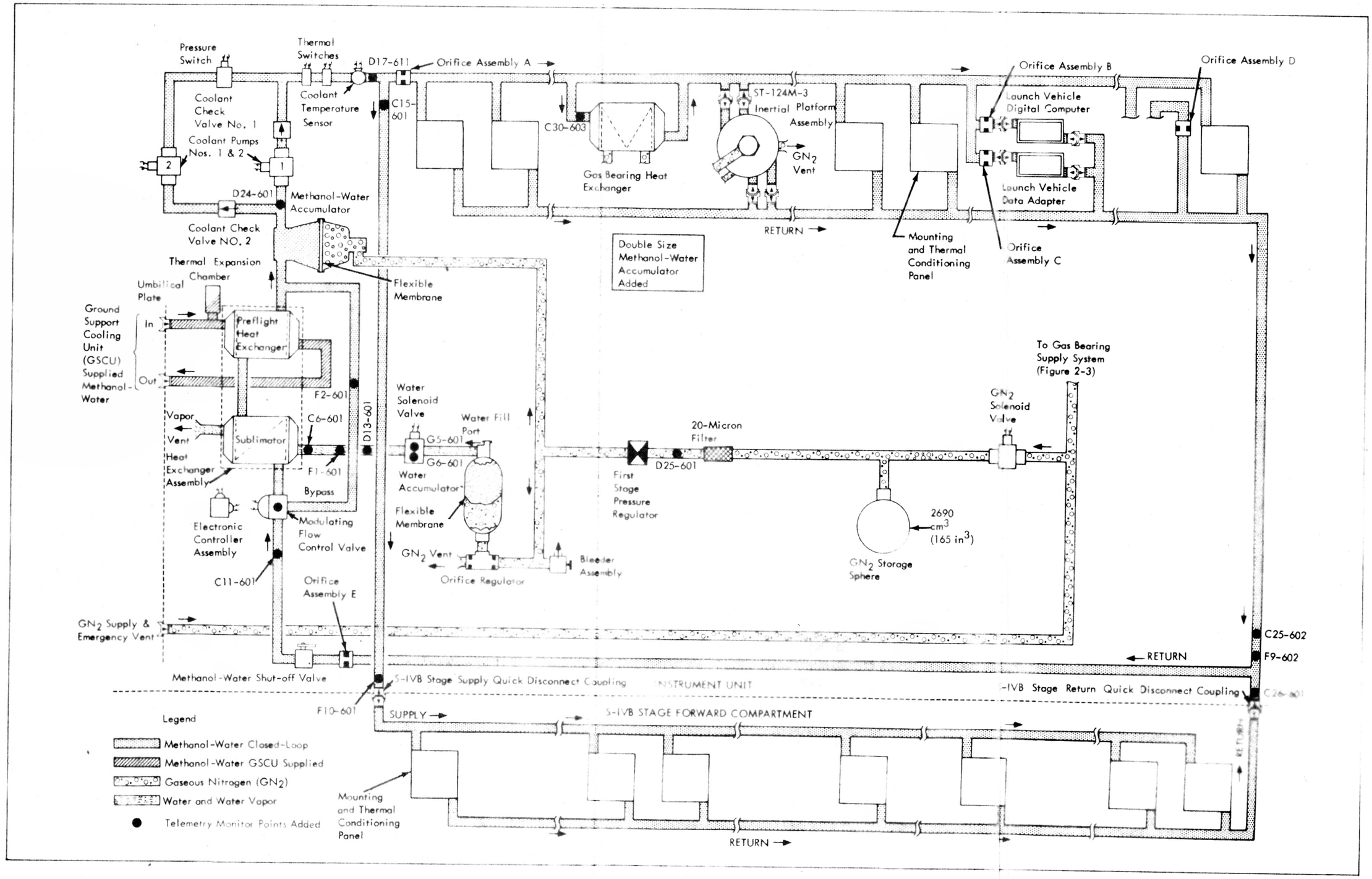


Figure 13.1-2
Environmental Control System Mechanical Diagram

When the closed-loop coolant temperature drops below approximately 15 °C (59 °F), water solenoid valve C is energized (closed), stopping water flow to the sublimator and causing sublimation to cease.

In addition to the previous description of sublimator operation, a theory exists that two modes of heat transfer occur in the sublimator. This theory – sublimation and evaporation – is as follows: Water under pressure enters the sublimator (refer to Figure 13.1-3) and flows into the pores of the porous plates. As the water in the large pores encounters the space vacuum, freezing occurs and an ice plug is formed. In the small pores which are non-wetted and can retain water by surface tension, the water fills the pores to a distance where the restriction is small enough to retain water at the inlet pressure. As the heat flux increases, the ice in the large pores sublimes at the solid-vapor interface and is formed at the liquid-solid interface. The vapor or steam is vented overboard. When the heat flux becomes great enough to prevent all ice from existing, any further increase in the heat load will raise the evaporation temperature. The heat load reaches a maximum when no ice exists and the heat sink temperature is zero degrees Centigrade (32 degrees Fahrenheit).

As can be seen, the sublimator has an advantage over a heat exchanger in that the flow of water is self-regulating – as the heat flux decreases, ice plugs are formed in the pores and the flow of water also decreases.

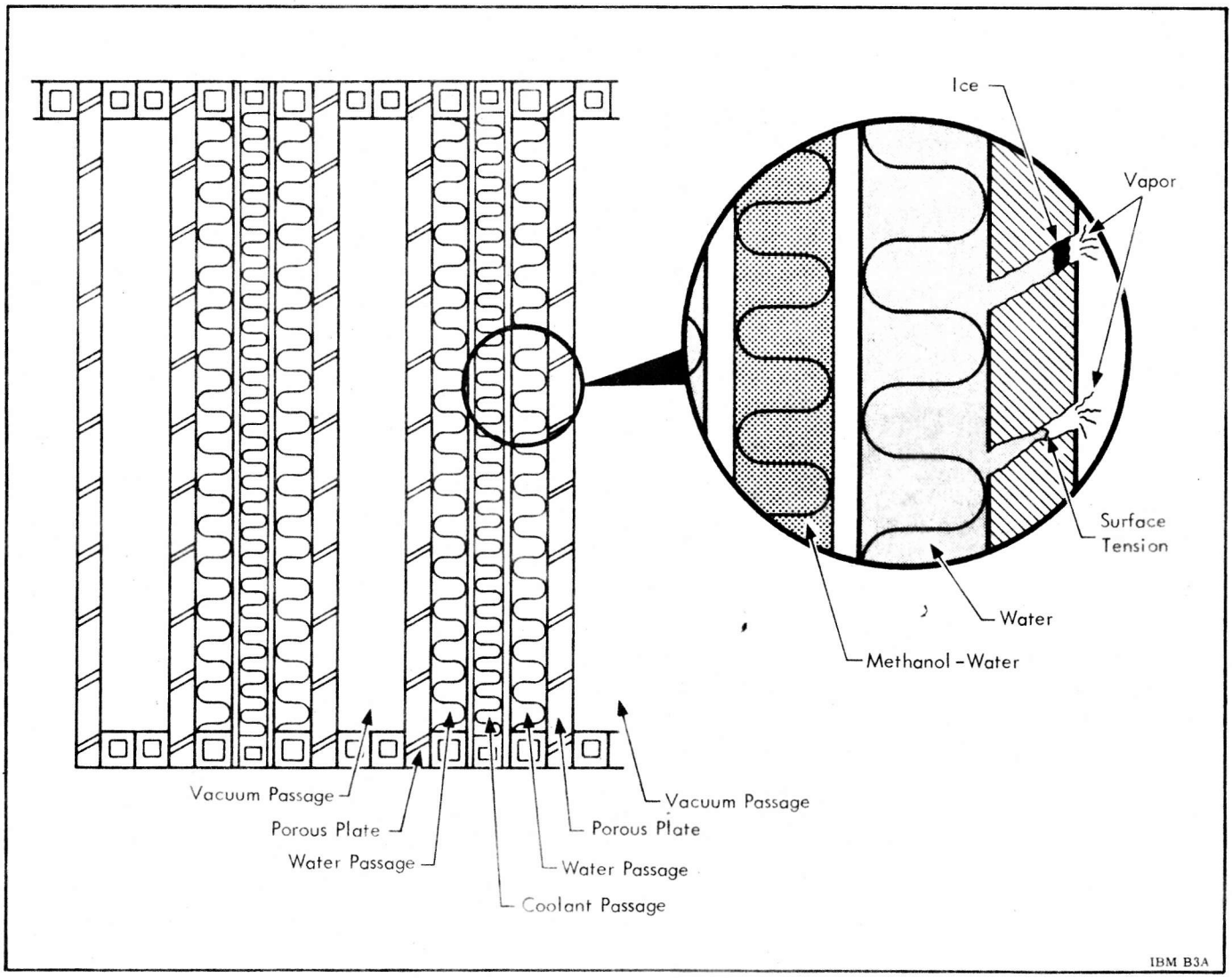


Figure 13.1-3 Sublimator Details

SECTION 13.2
GAS BEARING SUPPLY SYSTEM

The gas bearing supply system furnishes GN_2 at a regulated temperature and pressure for lubrication of the gas bearings in the ST-124-M Inertial Platform Assembly.

The system is filled through the GN_2 supply and emergency vent quick disconnect (refer to Figure 13.1-2) from a ground supplied source. A pressure transducer indicates when the pressure in the 0.056-cubic-meter (2-cubic-foot) storage sphere is approximately 20.7×10^6 N/m^2g (3000 psig). At this time, normally closed solenoid valve B is deenergized (closed) and the GN_2 source can be removed.

The GN_2 flows from the storage sphere, is filtered by filter B, and reduced to a pressure suitable for lubrication of the gas bearings by the pressure regulator and filter. The GN_2 is cooled or heated as required as it passes through the gas bearing heat exchanger, is filtered by filter C, and then applied to the gas bearings in the Platform. After lubricating the gas bearings, the GN_2 is vented into the Instrument Unit compartment.

A reference pressure is fed-back from the Platform to the pressure regulator and filter. This feed-back reference pressure maintains the pressure across the gas bearings constant by controlling the pressure regulator and filter output pressure; i.e., a decrease in pressure across the gas bearings causes the pressure regulator and filter output to increase.

The low pressure switch, which is calibrated through the calibrate quick disconnect, indicates when the pressure in the 0.056-cubic-meter (2-cubic-foot) sphere decreases below approximately 6.9×10^6 N/m^2g (1000 psig). Should an indication of a pressure decrease occur during prelaunch operations, the Platform would be shut down until the 0.056-cubic-meter sphere could be repressurized. Under normal in-flight conditions, this should not happen unless a leak or malfunction is present in the system.

SECTION 13.3
PREFLIGHT AIR/GN_2 PURGE SYSTEM

The Preflight Air/GN_2 Purge System, hereafter referred to as Purge System, is connected to the ground support environmental control system through a connection on the Instrument Unit umbilical plate.

Temperature and humidity controlled, filtered air, or GN_2, is supplied through the Purge System to maintain a controlled environment in the Instrument Unit and S-IVB Stage forward compartment. A simplified diagram of the Purge System is contained in Figure 13.3-1.

The Purge System is divided into 2 branches by the purge system "Y". The branches end and are capped at panel 19 of the Instrument Unit. The air, or GN_2, is forced through the Purge System tubing and vents into the Instrument Unit and S-IVB Stage forward compartment through regularly spaced holes in the flexible tubing assemblies.

A cool, dry environment must be maintained or moisture will collect on the mounting and thermal conditioning panels and the panels will rust. The conditioned air is supplied through the Purge System from completion of the erection of the Instrument Unit to approximately 30 minutes prior to the start of vehicle fueling. A secondary function of the conditioned air is to provide a cool, dry environment for the on-board equipment and for the assembly personnel.

Conditioned GN_2 is supplied through the Purge System from approximately 30 minutes prior to the start of vehicle fueling to liftoff. The conditioned GN_2 is supplied to maintain an inert, cool, dry environment. Venting GN_2 into the Instrument Unit and S-IVB Stage forward compartment reduces the oxygen content of the environment and reduces the possibility of the environment being combustible.

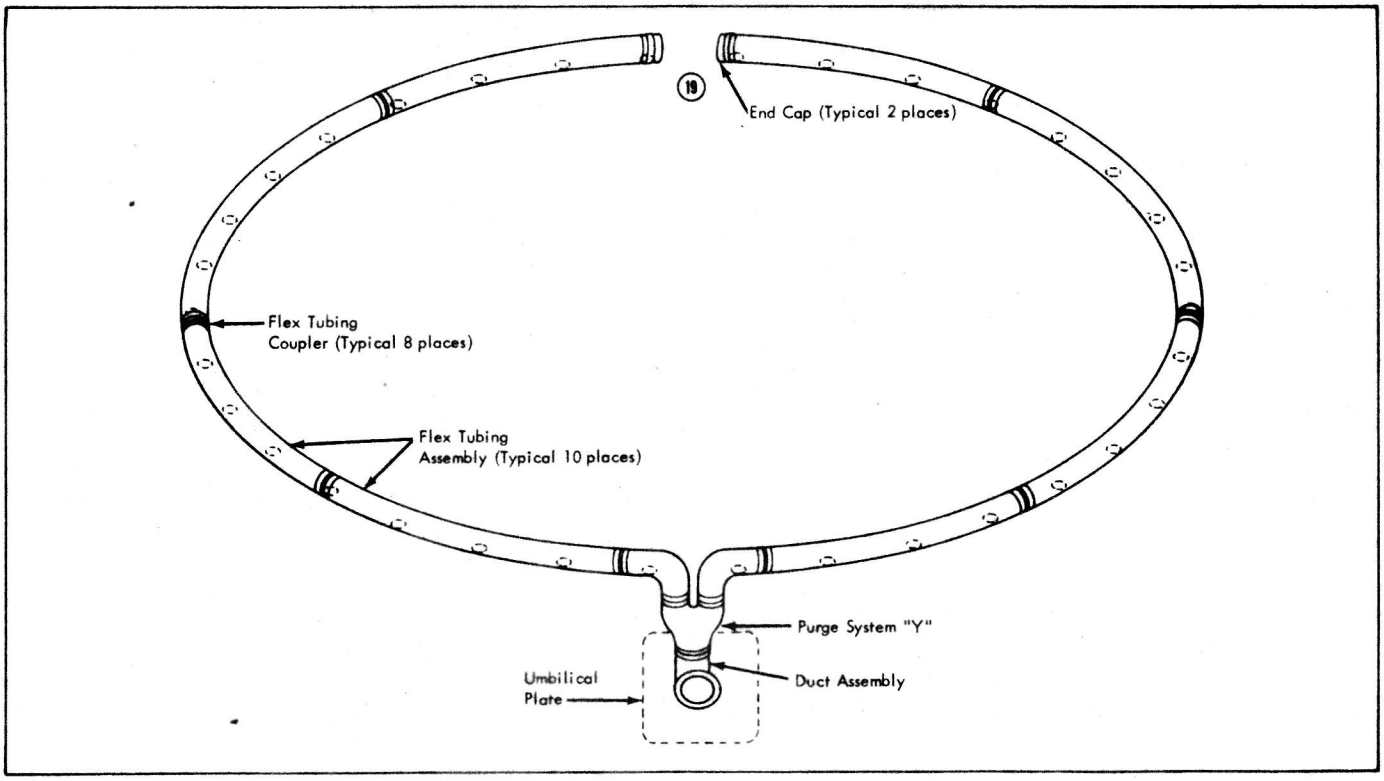


Figure 13.3-1 Preflight Air/GN_2 Purge System

SECTION 13.4
HAZARDOUS GAS DETECTION SYSTEM

The Hazardous Gas Detection System, hereafter referred to as Detection System, is used to monitor for the presence of hazardous gases in the Instrument Unit and S-IVB Stage forward compartment during vehicle fueling. The monitoring operation is continuous from the start of vehicle fueling to umbilical disconnect at liftoff.

Figure 13.4-1 is a diagram of the Detection System.

The Detection System consists of 4 tubes which are open ended between Instrument Unit panels 1 and 2, 7 and 8, 13 and 14, and 19 and 20. The tubes are connected to a quick disconnect coupling on the umbilical plate through a series of "T" fittings and a single tube.

The ground-based hazardous gas detection equipment extracts samples through the 4 tubes and monitors the samples for the presence of hazardous gases.

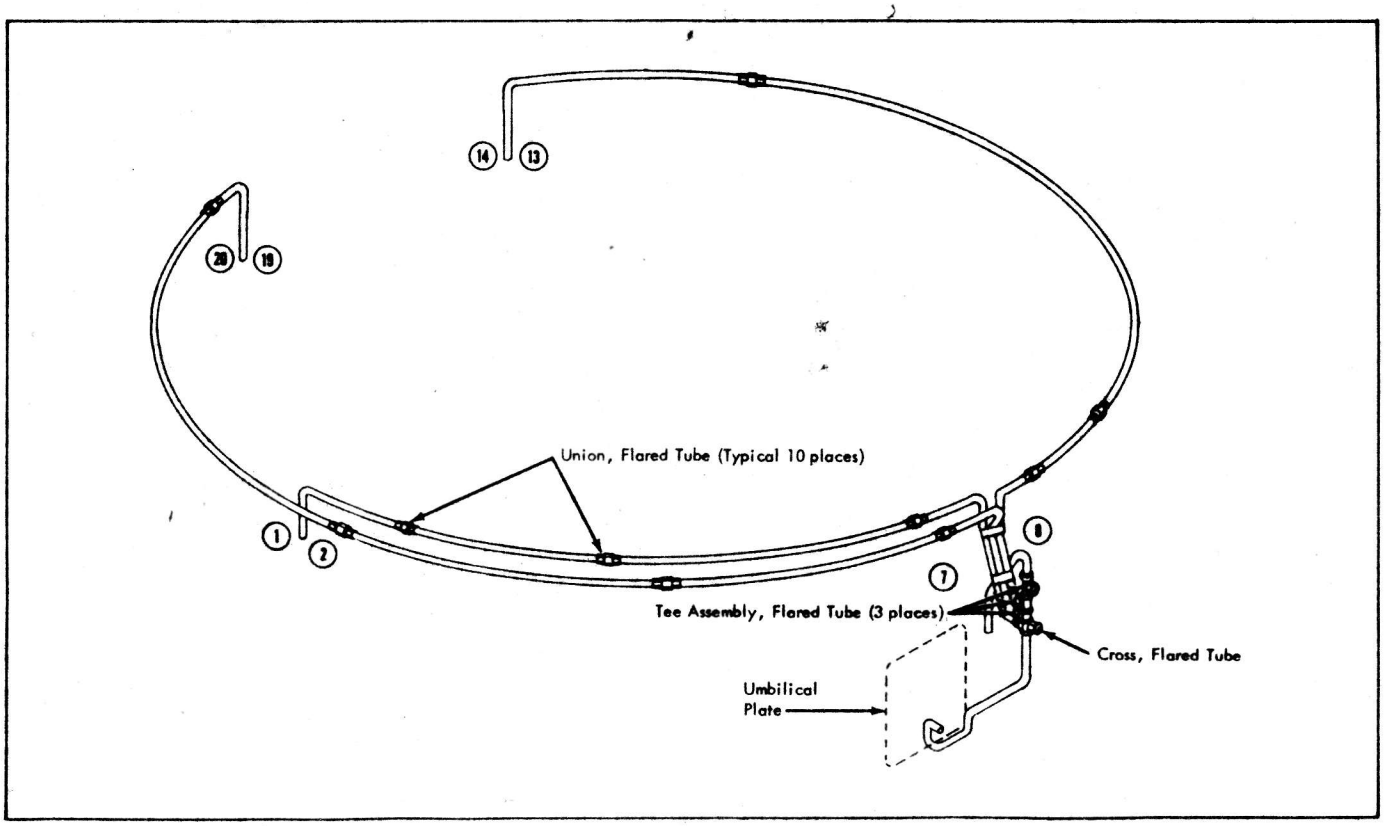


Figure 13.4-1 Hazardous Gas Detection System

CHAPTER 14
STABILIZED PLATFORM

SECTION 14.1
INTRODUCTION

The ST-124-M Stabilized Platform system* (see Figures 14.1-1 and 14.1-2) provides the inertial reference coordinates, integrated acceleration data, and vehicle attitude measurements with respect to these coordinates for navigation, guidance, and control of the Saturn Launch Vehicles.

The Platform system consists of 6 assemblies:

- ST-124-M Inertial Platform Assembly**
- ST-124-M Platform Electronic Assembly (PEA)
- ST-124-M Accelerometer Signal Conditioner (ASC)
- ST-124-M Platform AC Power Supply (PACPS)
- Gas Bearing Supply

The Platform system is self-contained and requires only inputs from the environmental conditioning system and the 28-volt dc power source.

The interface between the Platform system and other components of the Saturn navigation, guidance, and control system is shown in Figure 14.1-3. The accelerometer output signals are shaped by the

* For the purpose of brevity, the ST-124-M Stabilized Platform system will hereafter (within Chapter 14) be referred to as the Platform system.

** For the purpose of brevity, the ST-124-M Inertial Platform Assembly will hereafter (within Chapter 14) be referred to as the Platform.

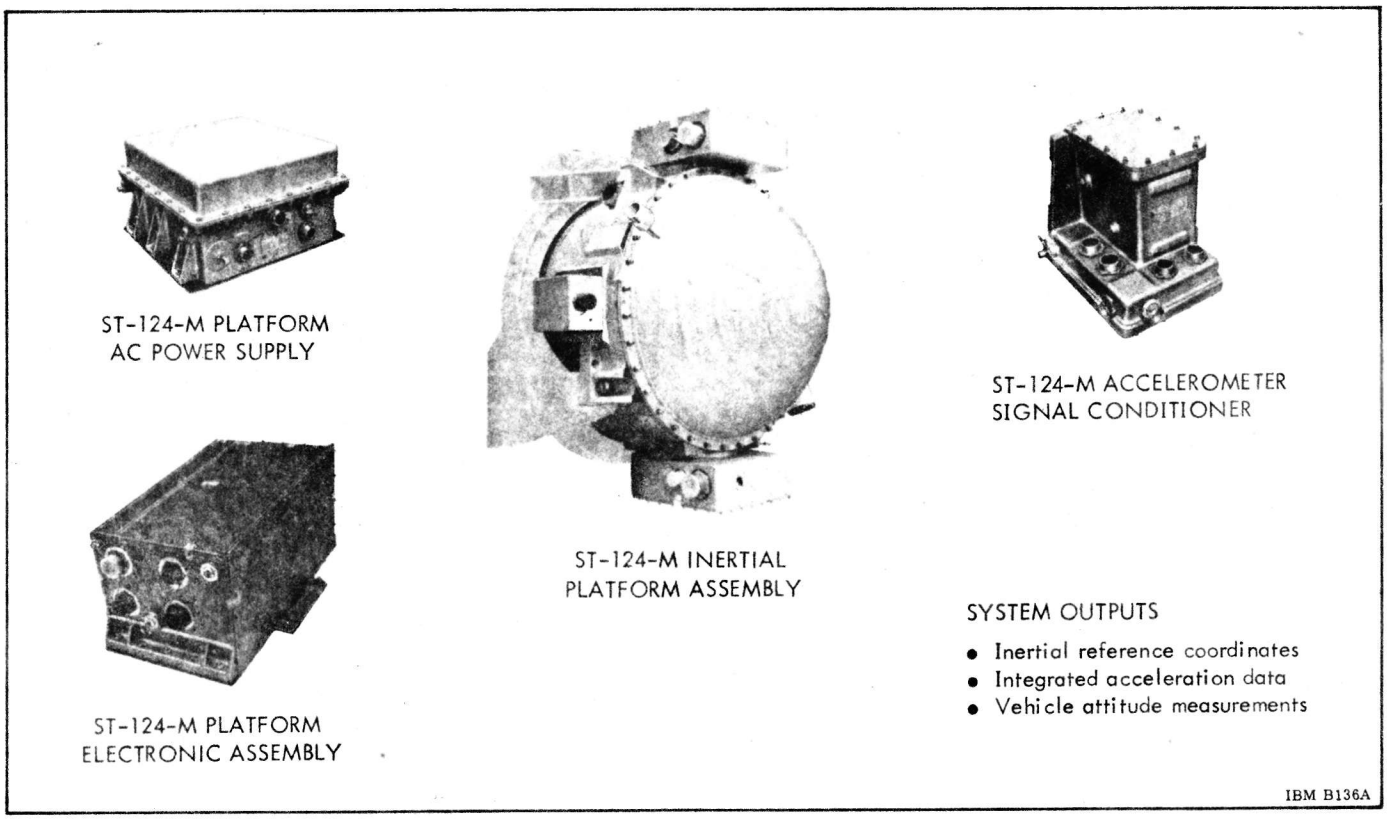


Figure 14.1-1. ST-124-M Stabilized Platform System (Saturn IB/V)

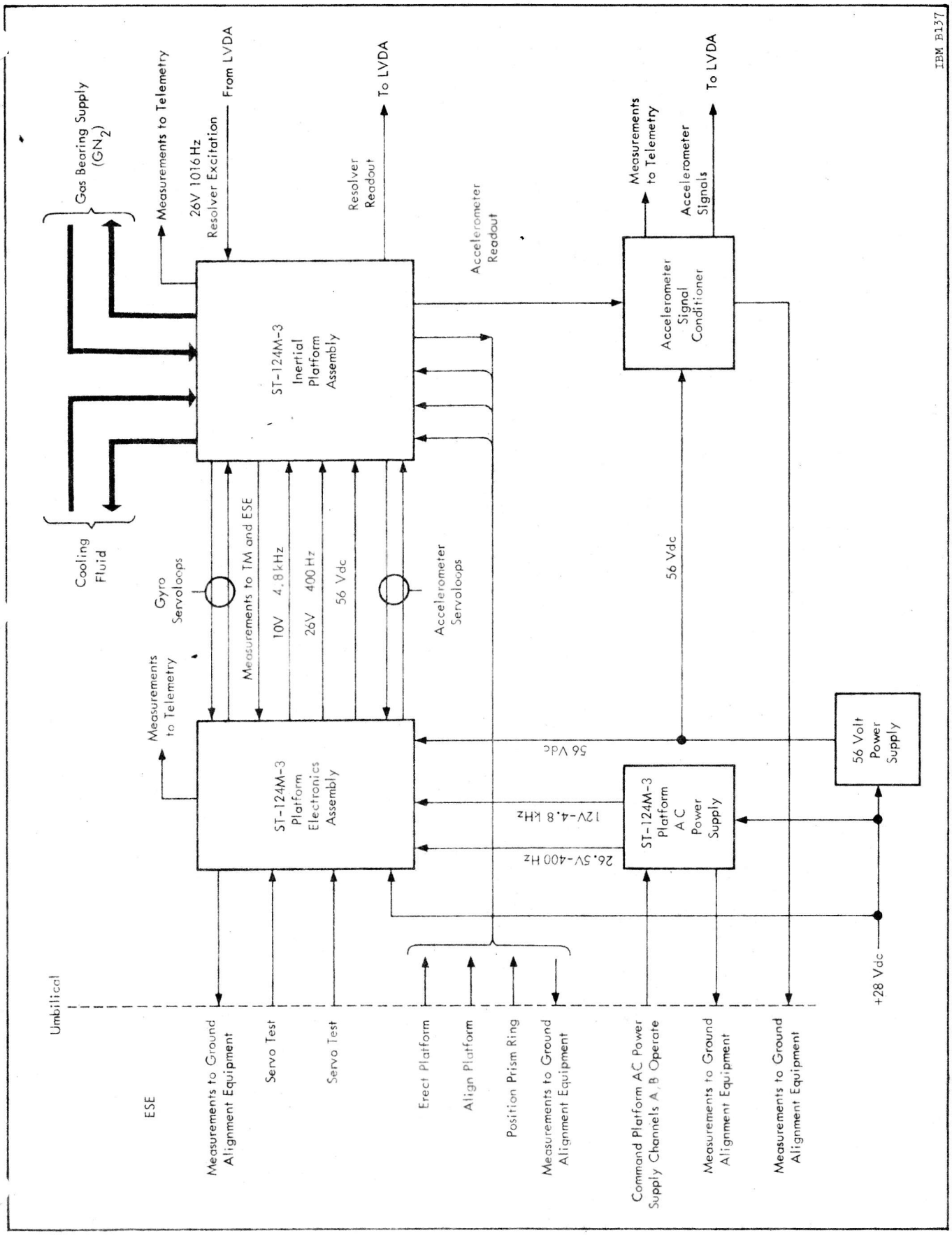


Figure 14.1-2. Stabilized Platform System Block Diagram

Accelerometer Signal Conditioner and then converted into a digital code by the Accelerometer Signal Processor (ASP) in the LVDA. The signals from the gimbal resolvers are converted to binary numbers in the Crossover Detector (COD) in the LVDA. The resolver chain output is used for prelaunch checkout only.

The Platform servo amplifier contains solid state electronics to close the platform gimbal servoloops and the accelerometer servoloops, and an impulse function generator for automatic checkout of each servoloop.

Electrical Support Equipment (ESE) associated with the Platform system is located at the launch site and the launch control center. At the Launch site, an azimuth-laying theodolite is located approximately 700 feet from the base of the vehicle. The theodolite installation trasmits signals via underground cables to the Platform System ESE located in the launch umbilical tower. Platform system ESE in the launch umbilical tower consists of an inertial data box, an alignment amplifier panel, an azimuth control panel, a theodolite amplifier panel, and accelerometer monitor panels. The equipment contained in the launch umbilical tower interfaces with the onboard Platform system, the RCA-110A launch umbilical tower computer, and the data link. In the launch control center, additional Platform system ESE interfaces with the launch control center RCA-110A Computer and data link. This equipment consists of a platform checkout and monitor panel, a platform control panel, an azimuth laying panel, and an azimuth-laying, video-monitor panel. Total remote control and automation of the Platform system is accomplished from the launch control center by use of the Platform system ESE, the launch control center RCA-110A Computer, and the data link.

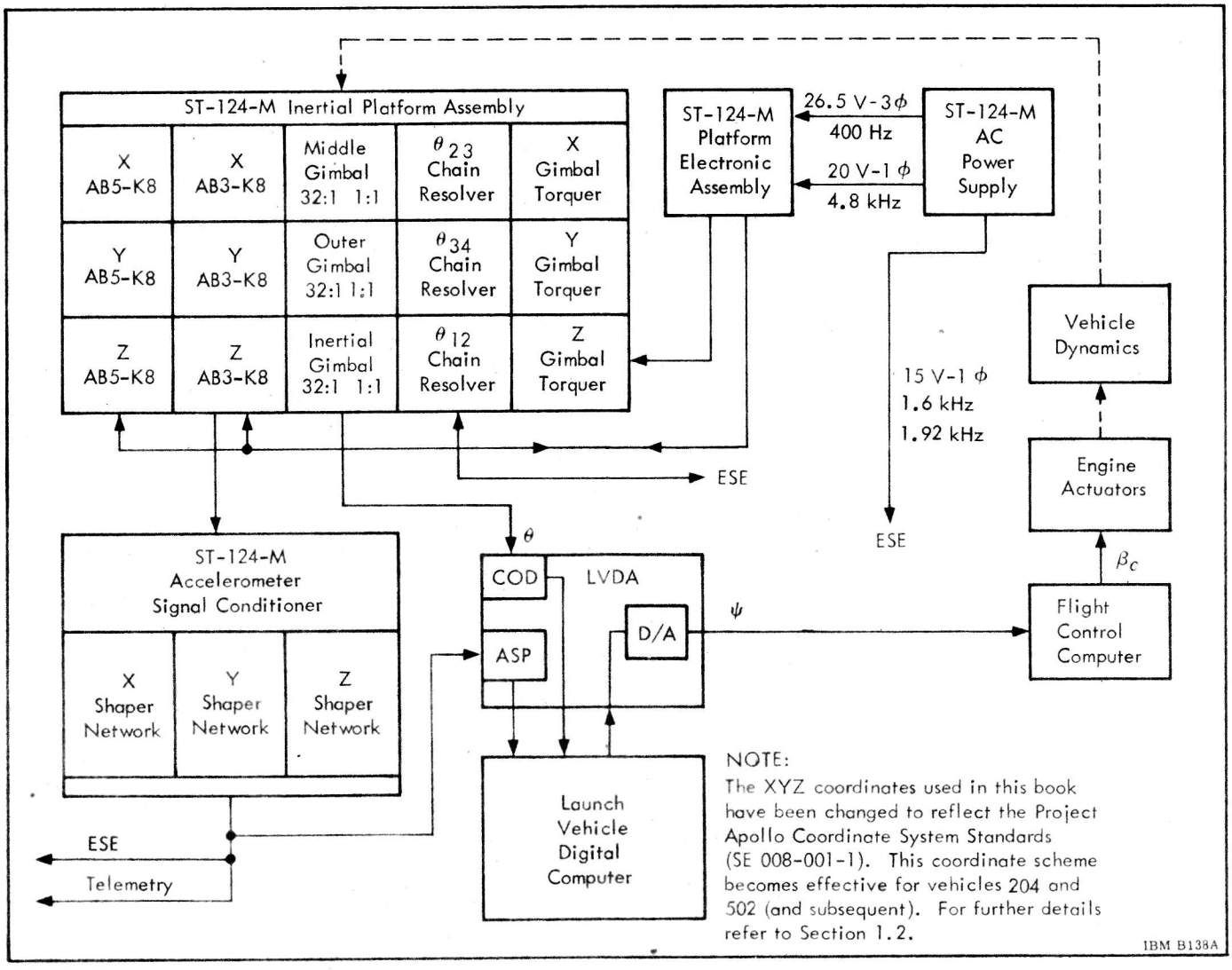


Figure 14.1-3. Stabilized Platform System Signal Interface

SECTION 14.2

ST-124-M INERTIAL PLATFORM ASSEMBLY

The Platform in the Saturn IB/V Vehicles is a 3-gimbal system (Figure 14.2-1). The gimbals are designated as the outer, middle, and inertial gimbals. The gimbals which allow rotation about the X and Y axes have unlimited freedom, while the gimbal for the Z axis* (yaw) is limited to ±45 degrees of rotation.

The inertial, or inner, gimbal provides a rotationally-stabilized table upon which three integrating accelerometers are mounted. The gimbal system allows the inertial gimbal rotational freedom. Three single-degree-of-freedom gyroscopes provide the reference for the stabilized table. The gyros have their input axes aligned along an orthogonal inertial coordinate system X_I, Y_I, and Z_I of the inertial gimbal, as shown in Figure 14.2-2. The signal generator, which is fixed to the output axis of the gyro, generates electrical signals proportional to torque disturbances. These signals are transmitted to the servoelectronics, which terminate in the gimbal pivot servotorque motors. The servoloops maintain the inner gimbal rotationally-fixed in inertial space.

The inertial gimbal has three pendulous integrating gyro accelerometers oriented along the inertial coordinates X_I, Y_I, and Z_I (Figure 14.2-3). Each accelerometer measuring head contains a pendulous single-degree-of-freedom gyro; the rotation of the measuring head is a measure of integrated acceleration along the input axis of the accelerometer. The Y accelerometer measures acceleration perpendicular to the thrust vector (crossrange acceleration). The outputs of the X and Z accelerometers are used to compute the pitch angle of the vehicle acceleration vector and the required cutoff velocity.

The coordinate erection and orientation system of the Platform aligns the X_I coordinate along the launch local vertical parallel to the gravity vector and aligns the Y_I coordinate perpendicular to the desired flight plane. The coordinate orientation is accomplished by use of an automatic alignment system which is a part of the ESE on the ground. The leveling alignment servoloops (Y and Z) generate torquing voltages which are a function of the earth's angular velocity, the latitude of the launch site, and the azimuth of the Z_I coordinate (launch azimuth). These voltages are applied to the Y and Z gyro torquers and cause each gyro to torque its respective gimbal until the servos are nulled. Platform coordinates are established in azimuth with the roll alignment servoloop. The output of the roll alignment servoloop is a function of the earth's angular velocity and the latitude of the launch site. Azimuth alignment, being a commanded function, is accomplished by injecting azimuth alignment signals directly into the roll alignment loop and torquing the roll gimbal with the X gyro. The azimuth alignment position can be updated at any time by the launch control computer.

The reference coordinate frame of the Platform maintains a fixed relationship to the inertial gimbal. This coordinate frame is accurately positioned prior to vehicle liftoff and remains space-direction fixed after vehicle liftoff. The gimbals of the Platform allow the inertial gimbal rotational freedom with respect to the vehicle. The gimbal pivots are the axes about which the gimbals turn with respect to each other. The ±Y pivots couple the inertial (stabilized) d) gimbal to the middle gimbal; the Y pivot axis is normally along the vehicle pitch axis at launch. The ±Z pivots couple the middle gimbal to the outer gimbal; the Z pivot axis is normally along the vehicle yaw axis. The ±X pivots couple the outer gimbal to the

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

Platform mounting base; the X pivot axis is normally along the vehicle roll axis at launch. The Platform ivot scheme is shown in Figure 14.2-4. The X, Y, nd Z pivots are controlled by dc torque motors; the X pivot torquer has approximately twice the torque capacity of the other pivot torquers. This accommodates the reflected torque when the middle gimbal is not orthogonal with the outer gimbal. For transfer of electrical signals across the ± X and ± Y pivots, slip-ring capsules are used. A flex cable is used on the ± Z pivot because of its limited freedom.

Dual-speed resolvers (32:1 and 1:1) are used as shaft angle encoders on the +X, +Y, and +Z pivots. The outputs of these resolvers are converted into a digital code in the LVDA. The system also has an analog resolver chain which utilizes single-speed resolvers on each pivot and three program resolvers

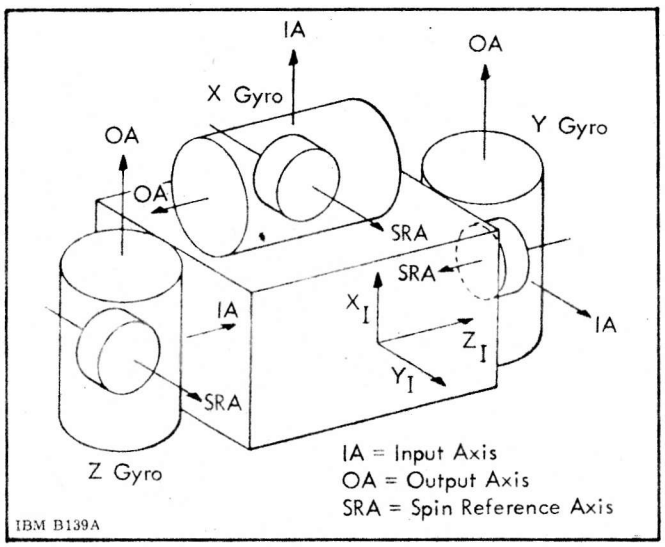


Figure 14.2-2 Orientation of Gyro Axes

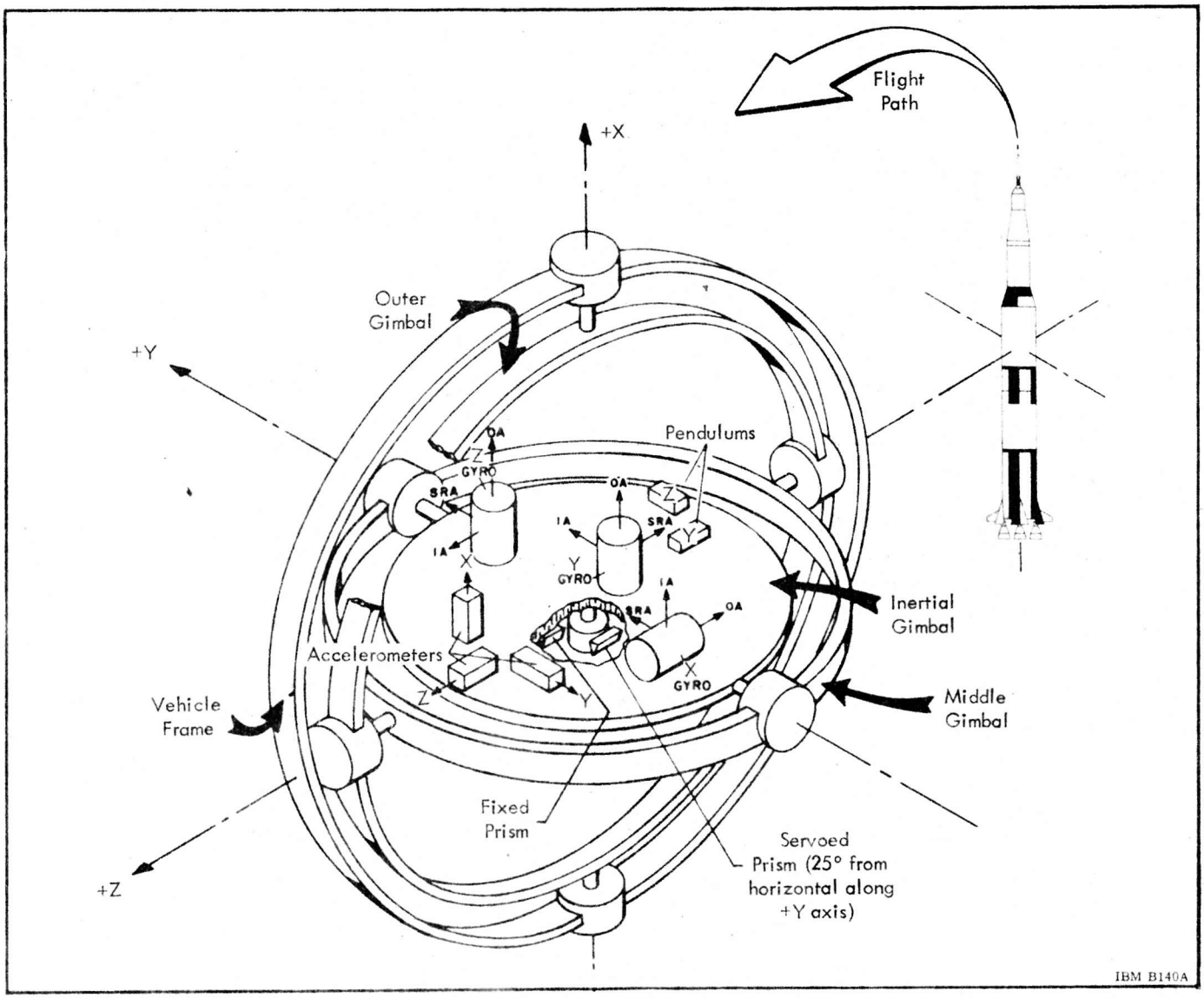


Figure 14.2-1 ST-124-M Gimbal Configuration

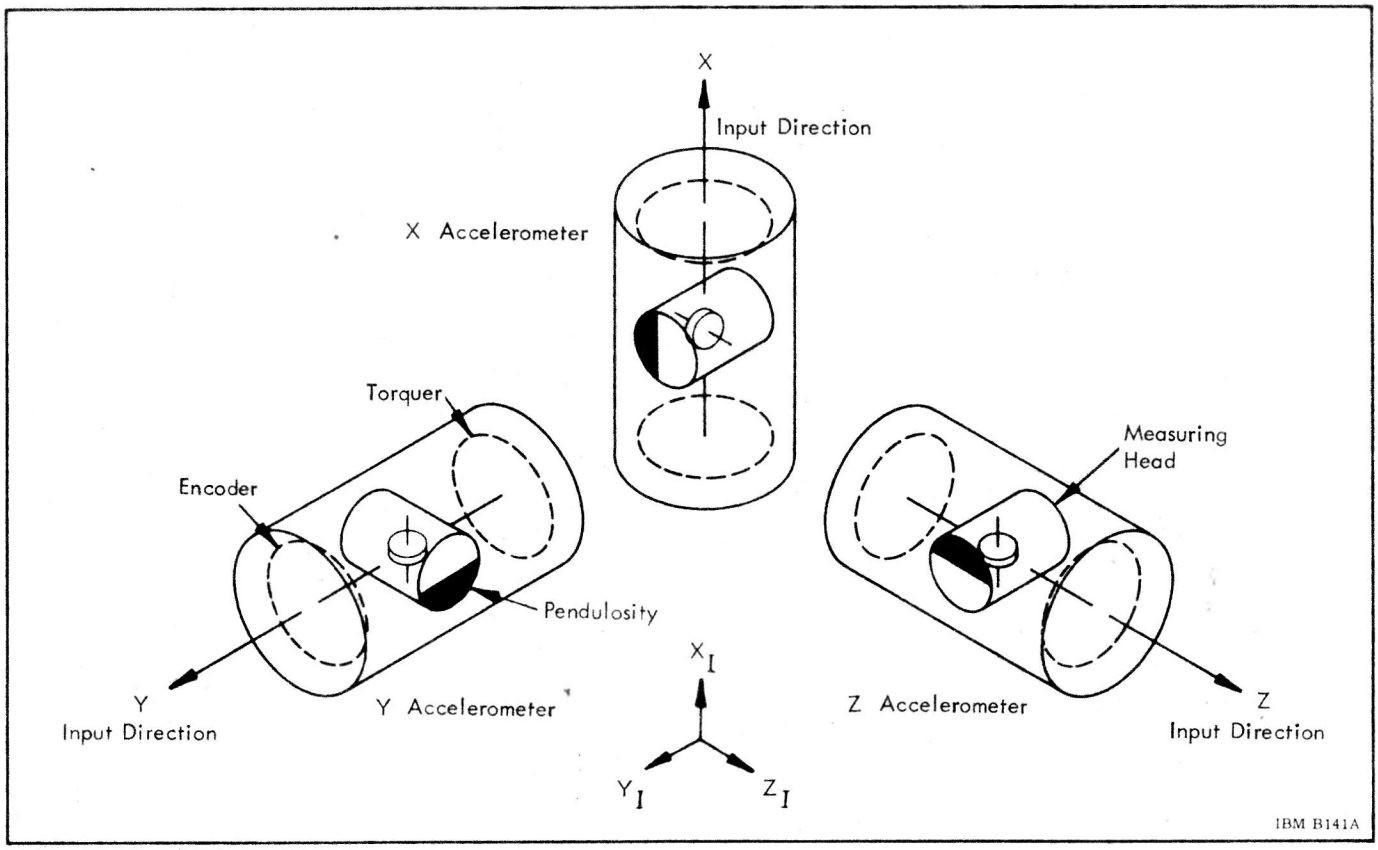


Figure 14.2-3 Orientation of Accelerometer Axes

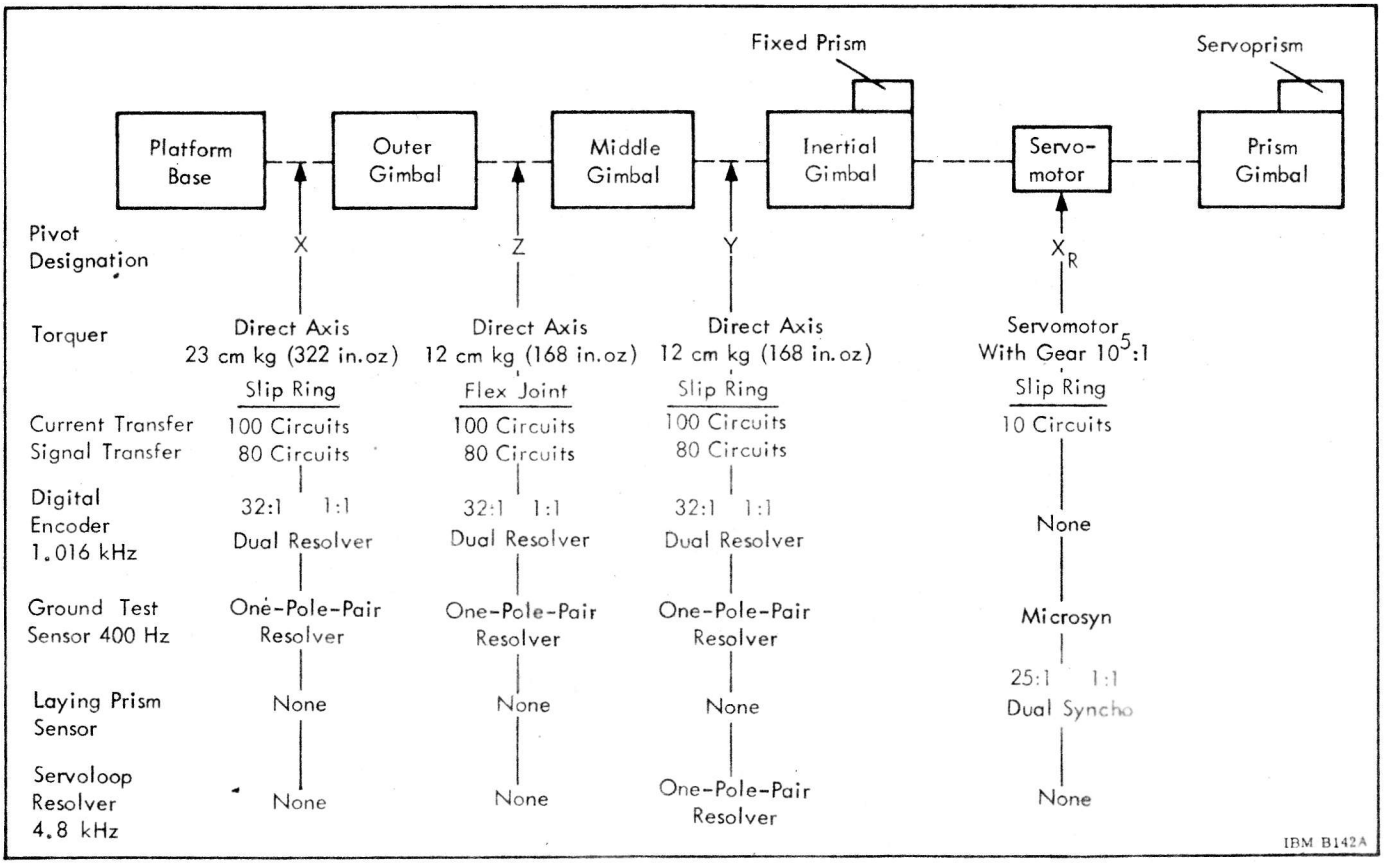


Figure 14.2-4 Platform Gimbal Pivot Scheme

in the inertial data box. This is used with the ground ESE only to facilitate checkout and test. If required, the resolver chain system can be used as flight equipment to measure the gimbal angles and to provide the vehicle attitude signals.

The +X and +Y pivots each contain a 100-circuit slip-ring cartridge for passing electrical signals across the pivots. The -X and -Y pivots each contain an 80-circuit slip-ring cartridge. All critical signals are routed through the plus pivots while all power transmission is over the minus pivots. The slip rings are built up by electrodeposition of 0.015 inch of copper base with a flashing of nickel to prevent gold migration and electrodeposition of 0.015 inch of gold on the outside. The rings are dielectrically isolated and supported with a filled epoxy. A one-piece stainless steel cross-spline along the center serves as the main structural member of the ring subassembly (Figure 14.2-5). The leadwire is fastened to the ring by electrodeposition and is routed along the spline to the mounting flange.

A 90-degree V-groove is machined into the rings to serve as a guide for the brushes. Dimensional tolerance on the ring assembly is controlled by a grinding process where the V-grooves in all rings are ground in a single operation. A set of miniature precision bearings and the brush blocks' mounting frame complete the ring assembly.

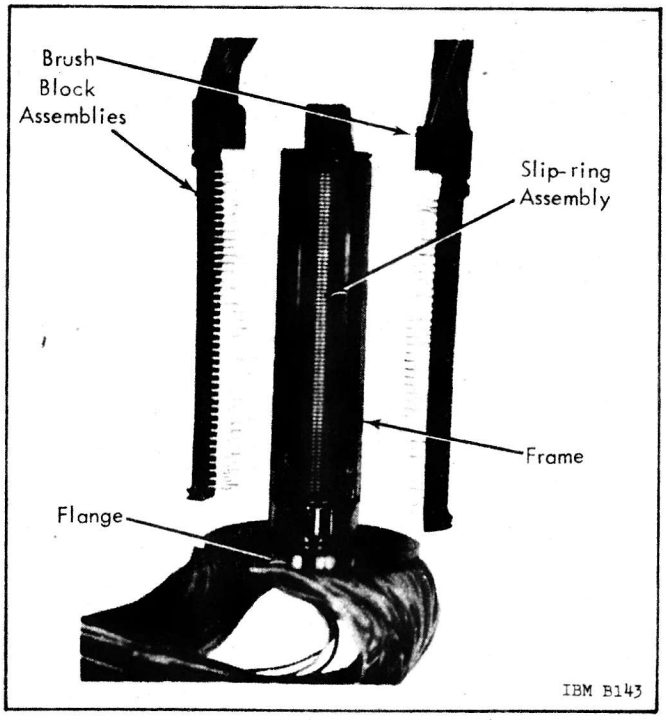


Figure 14.2-5 Slip-ring Capsule

The two brush block subassemblies allow complete redundancy for each brush. The brushes are preformed and prestressed Ney-ORO-28A (75% gold, 22% silver, and 3% nickel) material. The brush blocks are a filled epoxy structure aligned with dowel pins and secured with screws to the frame. The leadwire is an unpigmented teflon-insulated nickel-plated copper, 19/42, size 30 AWG, stranded wire.

Acceptance testing of each unit includes 100-hour run-in time, temperature cycling, noise tests, and an X-ray of the completed assembly.

Table 14.2-1 lists the slip-ring cartridge characteristics.

The X_R prism gimbal pivot is controlled through a gear reduction of 10^5:1 by a servomotor mounted to the inertial gimbal. The angle between the prism gimbal and the inertial gimbal is accurately sensed by dual synchros (25:1 and 1:1) and controlled with a followup servo.

Table 14.2-1 Slip-Ring Cartridge Characteristics

Current Rating		1 A at 125 V, 400 Hz continuous per circuit
Noise Limit		10 μV/mA
Contact Resistance		0.125 ohm per circuit
Breakaway Friction		2 g cm/circuit
Environmental		
	Temperature	-55°C to +100°C (-67°F to +212°F) storage 0°C to +60°C (32°F to +140°F) operation
	Vibration	15 g, 20-2000 Hz 3-hour test time per axis
	Shock	30 g, 3 milliseconds 20 g, 11 milliseconds
	Acceleration	20 g
Life		
	Useful Life	8760 hours (storage and operating)
	Operating Life	1000 hours will meet noise specification 5000 hours with maximum of 100% increase in noise specification

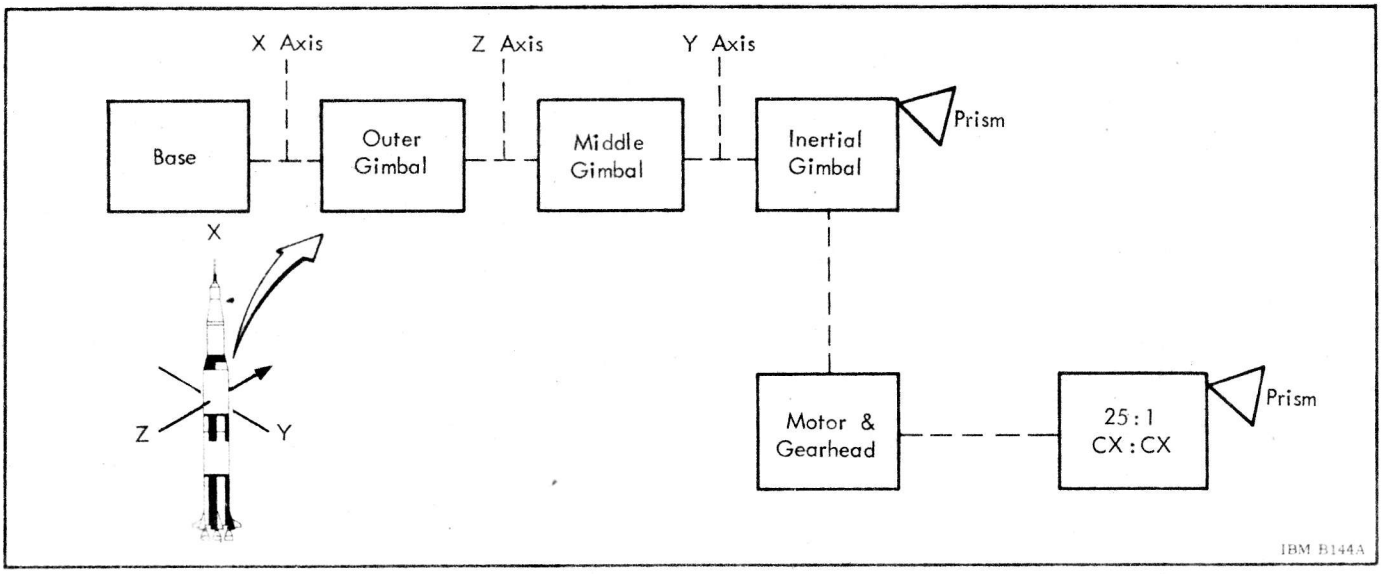


Figure 14.2-6 Platform Gimbal Arrangement

The three-gimbal Platform, as described, is the normal launch pad configuration and is illustrated in Figure 14.2-6.

The weight of the Platform is 51 kilograms (112 pounds). The Platform is mounted in the Saturn IB/V IU at control position IV on accurately machined surfaces which are initially qualified to the IU coordinates to ±3 arc minutes. A window in the IU at control position IV provides a line-of-sight to the Platform azimuth laying prisms for penetration of the azimuth laying theodolite light source (Figure 14.2-7).

The electrical connectors and hemispherical covers of the Platform are sealed so that exhaust gas

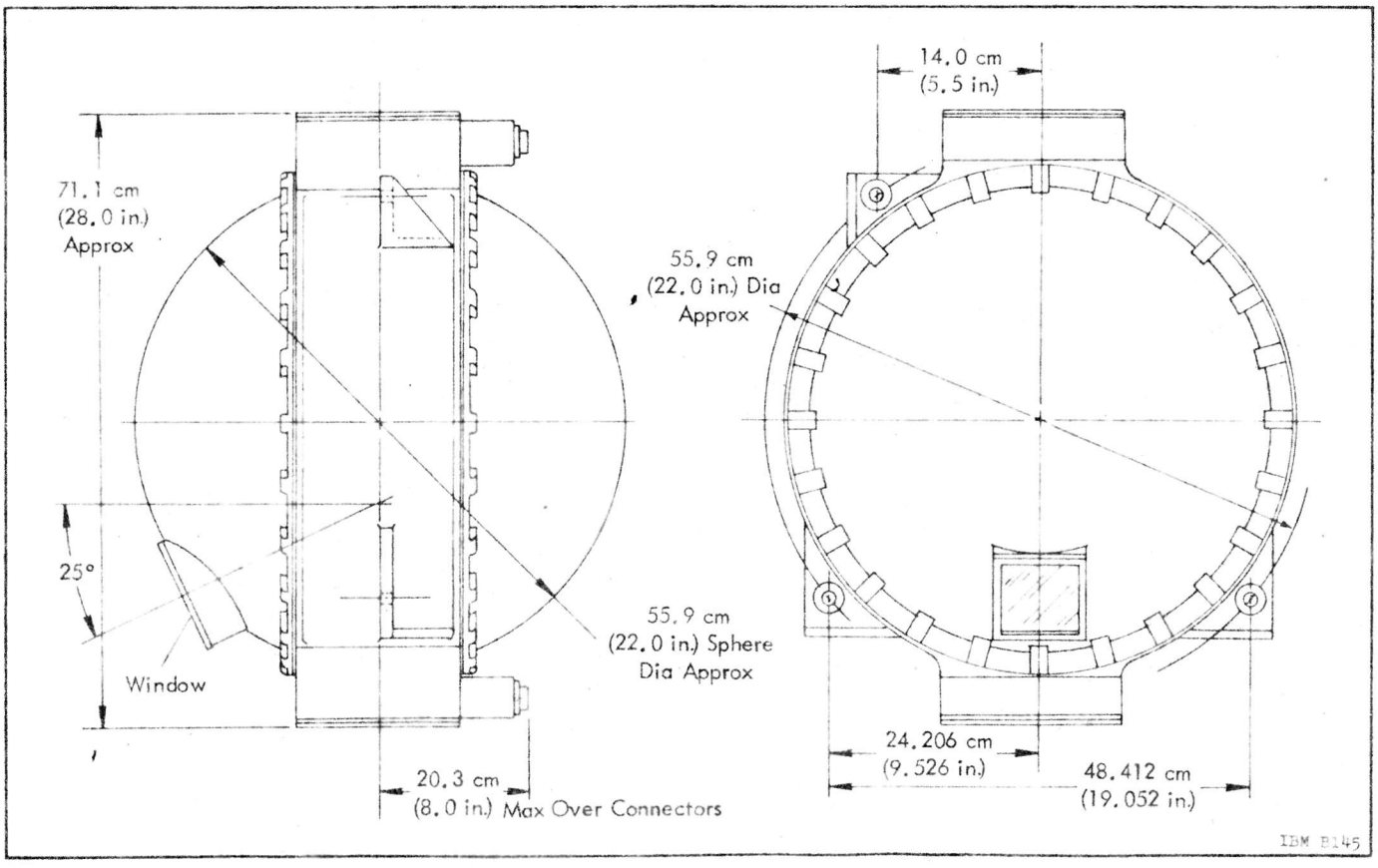


Figure 14.2-7 ST-124-M Inertial Platform Assembly

from the gas bearing components must pass through a special orifice in its base. This orifice is a pressure-regulating device which stabilizes the internal ambient pressure at 8.3 N/cm^2a (12 psia). Because of the characteristics of this orifice, the internal pressure will rise to approximately 11.75 N/cm^2a (17 psia) in a one-atmosphere ambient and will drop to the controlled pressure of 8.3 N/cm^2a (12 psia) approximately one minute after liftoff.

The covers also serve as heat exchangers for removing excess heat from the Platform. The methanol-water coolant from the environmental control system flows through passages in the covers to remove the excess heat. The methanol-water solution is maintained at 15.0 ± 2.2 °C (59 ± 4 °F) by the IU environmental control system. The mass temperature of the Platform stabilizes at approximately 43 °C (110 °F). The hemispherical covers are fabricated of aluminum and are secured to the Platform base with cap screws and sealed with full-volume 0-rings.

The Platform gimbals, pivot housings, and the base are machined from beryllium, which provides the greatest stiffness-to-weight ratio, stability after machining, and excellent heat transfer characteristics.

The inertial gimbal is geometrically the most complicated gimbal and the most difficult to fabricate (Figure 14.2-8). This gimbal supports the three stabilizing gyros, three accelerometers, two pendulums, the inertial prism, the synchro prism assembly, and electronic modules. The mounting surfaces for the gyros, accelerometers, pendulums, and prisms are precision-machined surfaces. Orthogonality of the accelerometer mounting surfaces is ± 3 arc seconds; that of the gyros mounting surfaces is ± 2 arc minutes. The pendulums are matched to the accelerometers to ± 3 arc seconds, and the prisms are matched to the inertial coordinates to ± 3 arc seconds. Gas supply passages are machined inside the inertial gimbal, and special fittings on the gas bearing components allow them to be plugged directly into the gas supply passages.

The gimbal rings are designed as spherical sections. This geometry was chosen to give maximum mechanical rigidity and stability and to provide symmetrical moments of inertia for servoloop design.

Gimbal load bearings are designed so that minimum shear is placed on the gimbal. This is accomplished by using a pair of bearings on one pivot of each gimbal which is preloaded against each other with a 36.3-kilogram (80-pound) load. The other pivot of each gimbal has a single gothic arch type bearing loaded with a 2.27-kilogram (5-pounds) preload.

Gimbal pivot resolvers are assembled in separate beryllium housings and attached to the pivots with stiff diaphragms. This allows a minimum eccentricity between resolver rotor and stator, bench testing of the assembled resolver, and easy replacement without disassembly of the gimbal structure at the load bearings.

Nitrogen gas is transported across the pivots through an annulus with 0-ring seals. The total leak rate of the pivot annulus will be less than 1400 cm^3/min (0.05 cfm) at Standard Temperature and Pressure (STP).

Structural resonance frequency of the outer and middle gimbals is 265 hertz and 330 hertz, respectively. A structural resonant frequency of 120 hertz is obtained on the inertial gimbal because of the stiffness of the beryllium gimbal rings. There is a secondary resonant frequency of the inertial gimbal at 280 hertz, which is obtained from the bearings and pivot trunnions. Above 280 hertz, the gimbals attenuate base vibration inputs to provide a smooth support for the components.

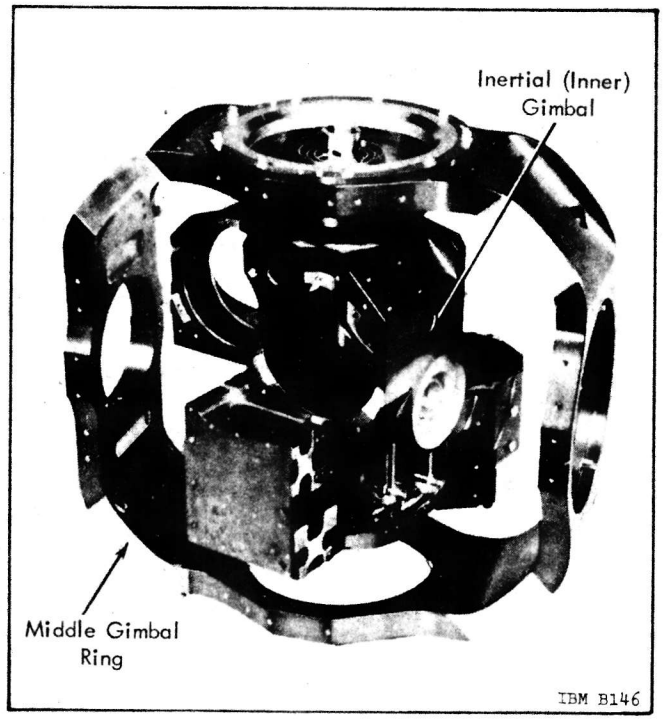


Figure 14.2-8 Gimbal Design

SECTION 14.3
GYRO AND ACCELEROMETER SERVOSYSTEM

The Block diagrams of the gyro and accelerometer servoloops are shown in Figures 14.3-1 and 14.3-2, respectively. The servoloops use a 4.8-kilohertz suppressed carrier modulation system with the signal generator outputs being amplified and demodulated on the gimbals of the Platform. The dc signal from the detector output is transferred from the Platform to the Platform Electronic Assembly. The dc signal is shaped by a lag-lead stabilization network, remodulated at 4.8 kilohertz, amplified, and then demodulated prior to entering the dc power bridge. This dc power bridge provides a current source drive for the direct axis dc gimbal torquer. The 4.8-kilohertz carrier provides sufficient bandwidth for the servoloop while the current driver for the torquer maintains the gain in the servoloop independent of torquer heating and commutator brush resistance.

The Y servoloop has the Y gyro output signal phase-shaped and amplified and sent to the Y pivot torquer.* The X and Z gyro output signals are resolved along the X and Z coordinates of the middle gimbal by a resolver mounted along the -Y pivot. The outputs of the resolver are amplified and demodulated. The resolved signals are then shaped and amplified and fed to their corresponding gimbal pivot dc torquer. No gain compensation such as secant θ_Z is used in the outer gimbal servoloop for middle gimbal angle deviation. Figure 14.3-3 shows the hardware which comprises a gimbal servoloop.

Block diagrams of the gyro servoloop and accelerometer servoloop are shown in Figures 14.3-4 and 14.3-5, respectively.

The principle function of the servosystem is to maintain α near 0 in the presence of various disturbances (see Figure 14.3-6). A logical measure of system performance is the ratio $\frac{T_\alpha}{\alpha}$ which describes the maximum angular deviation for specified inputs (T_α = torque about IA). For instrumentation reasons, $\frac{T_\alpha}{\beta}$ is used because α is very small for frequencies below ten times the resonant frequency. The angular motion β resulting from α is normally a much larger signal by the multiplication factor $\frac{H}{J_\beta s}$ (the gyro transfer function) and is easily measured at the input to the servoamplifier, F(s). In system design, the ratio $\frac{T_\alpha}{\beta}$ is made as large as possible, consistent with good transient response.

The single-axis approach to the design of the servosystem is expedient, but it ignores the effect of mechanical and electromechanical interaxis coupling. Mechanical interaxis coupling will occur if the principal axes of the inertial gimbal do not coincide with the input axes of the gyroscopes. Also, products of angular motion will occur if the moments of inertial are unequal. Fortunately, in the design and fabrication of the inertial gimbal, close tolerance controls make these effects negligible relative to other interaxis coupling.

The output signal (β) of the single-axis gyro is a measure of the angle between the gyro float and the gyro case. This is the signal used in the Platform servoloop. Because the gyro case is mounted to the inertial gimbal, disturbances about its output axis are reflected into other servoloops. Therefore, motions of the gyro case about its output axis are coupled into the servoloop for that gyro.

The effect on servostability of this pickoff coupling depends on the orientation of the gyros on the Platform. A multiplicity of possible gyro orientations exists for a Platform, but it is not possible to orient three single-axis gyros with mutually orthogonal input axes in such a way that there is not at least one closed loop of gyro pickoff interaxis coupling. Addi-

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

tional considerations for orientation of the gyros on the inertial gimbal must be made. These include the coning or rectification drift and the unequal elasticity (anisoelasticity) in the gyro spin axis and in put axis which give rise to a steady state drift rate. The effect of gyro orientation is a function of the direction of applied linear acceleration or vibration and varies sinusoidally as the acceleration vector is rotated about the gyro's output axis.

Figure 14.3-6 is a sketch of the Platform gyro orientation. The inertial gimbal is gimballed for 3 degrees of freedom relative to the vehicle about the three mutually-perpendicular axes identified as α_X,

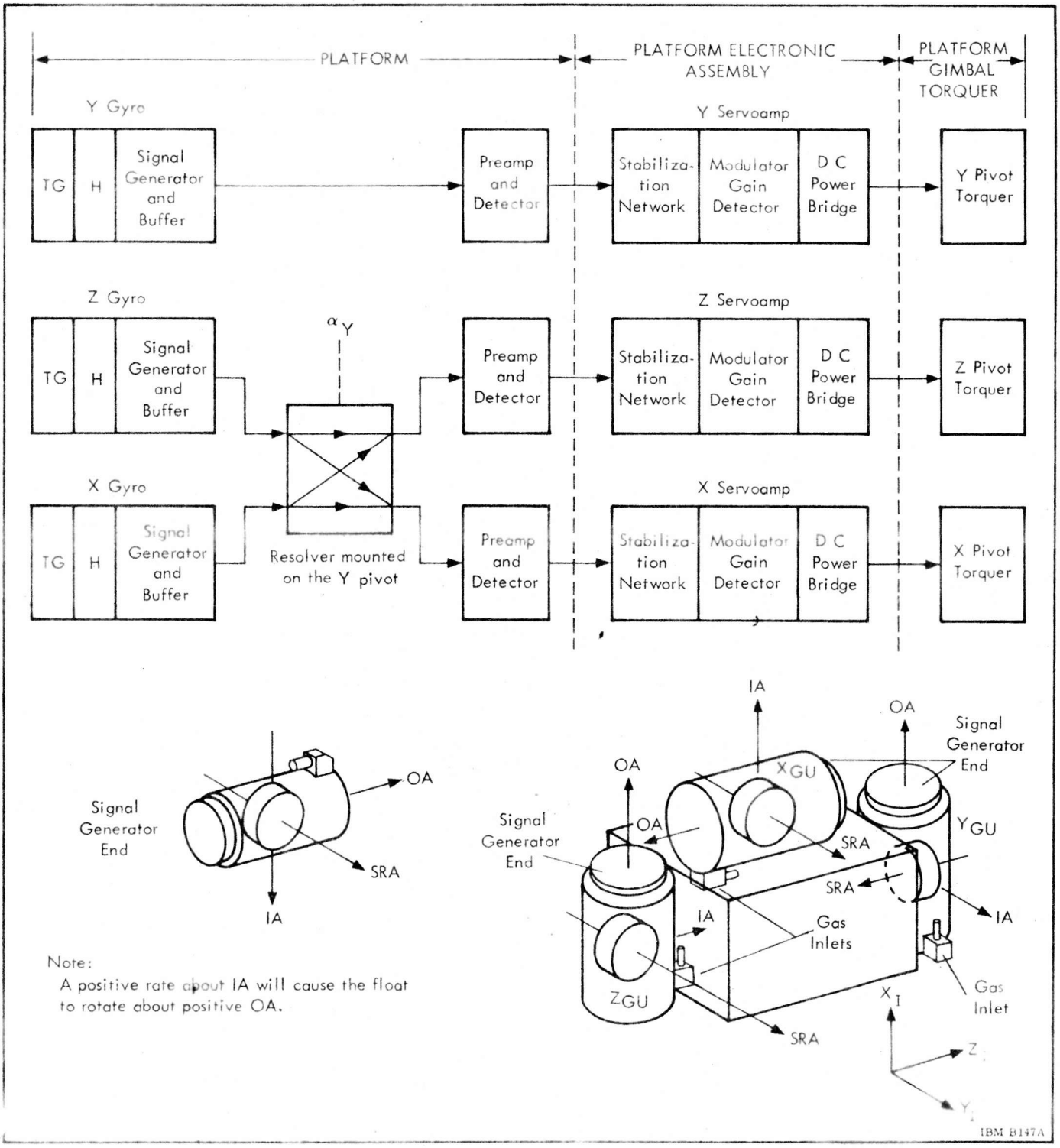


Figure 14.3-1 Gyro Servoloops Block Diagram

α_Y, and α_Z. Each gyro is represented by mutually-perpendicular vectors which define the angular momentum (H), the input angular motion (α), and the output motion (β). The gyros are identified with their particular platform axes. The Platform angular motion about the input axis of the X gyro is coupled into the pickoff of the Y and Z gyros, and angular motion about the input axis of the Z gyro is coupled into the pickoff of the X gyro.

The actual pickoff signals which are fed to the amplifier can be expressed as (Figure 14.3-6):

$$\sigma_X = \beta_X + \alpha_Z$$

$$\sigma_Y = \beta_Y - \alpha_X$$

$$\sigma_Z = \beta_Z + \alpha_X$$

The 3-axis servosystem block diagram shown in Figure 14.3-7 illustrates this coupling through the gyro output axes. The motion about the Y axis is coupled into the Y axis servo but does not feed back into either of the other two gyro servoloops. Therefore, the Y axis servo will be disturbed by motion of the X axis but no stability problem results. There is coupling of the input angles α_X and α_Z to the output motions β_X and β_Z, respectively. Therefore, a closed loop is formed which, in addition to causing cross axis disturbances, must also be considered as to its effect on servo performance. A resolver (α_Y) provides continuous coupling between the inertial components and the gimbal about which compensating servotorques are applied. This effect is shown by the sinusoidal coupling between the X and Z axes.

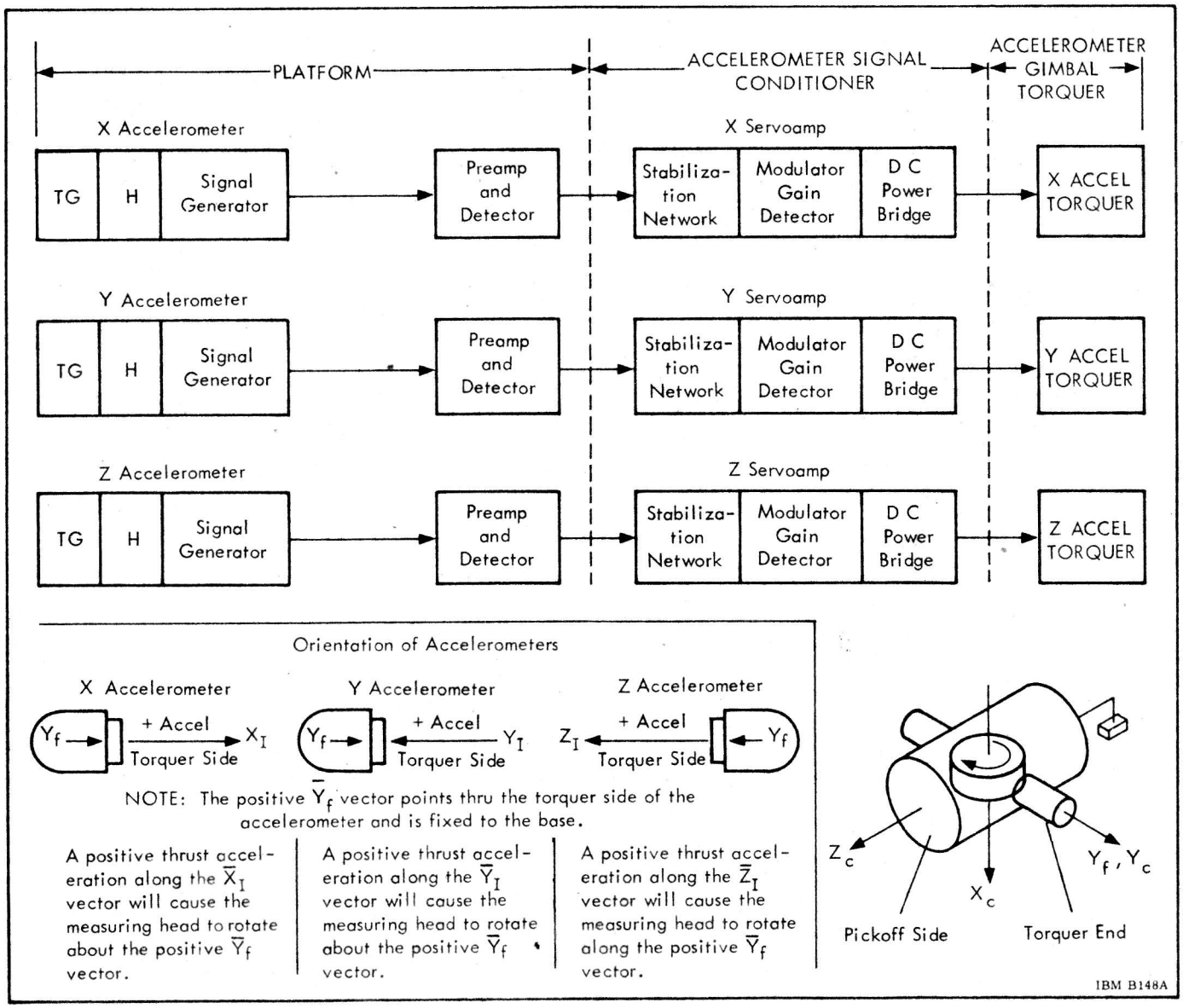


Figure 14.3-2 Accelerometer Servoloops

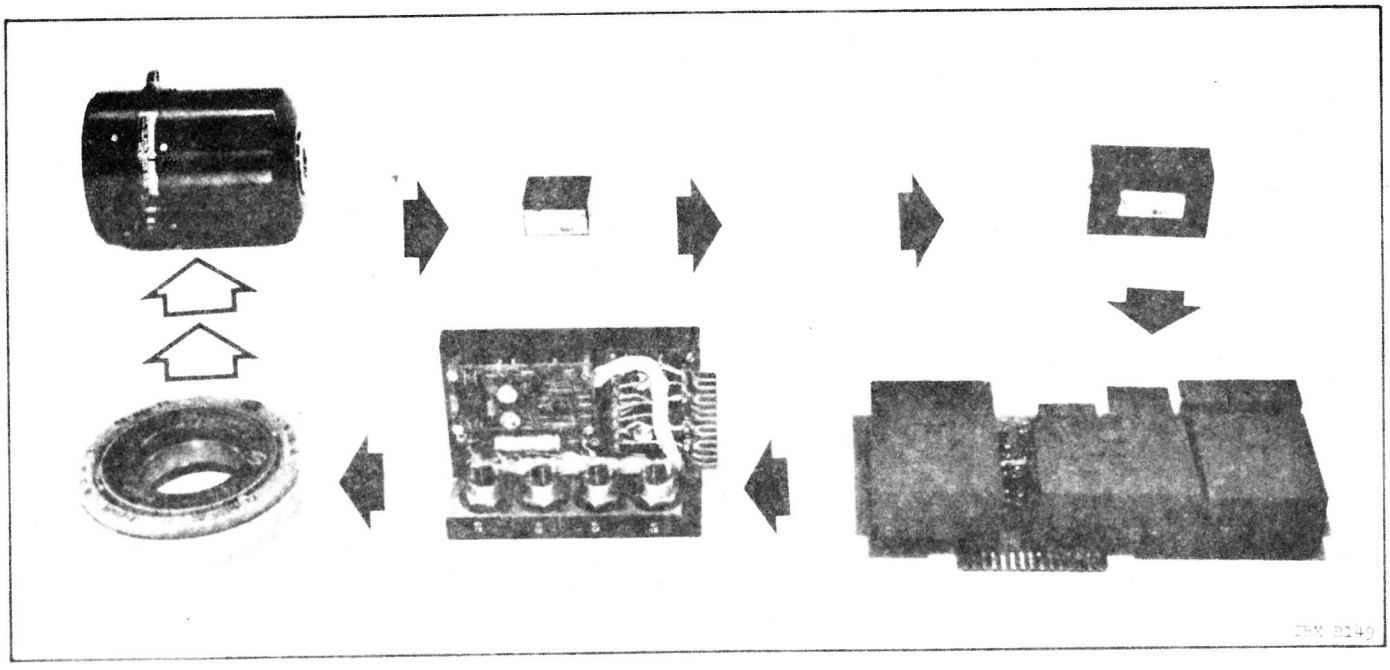


Figure 14.3-3 Gimbal Servoloop Hardware

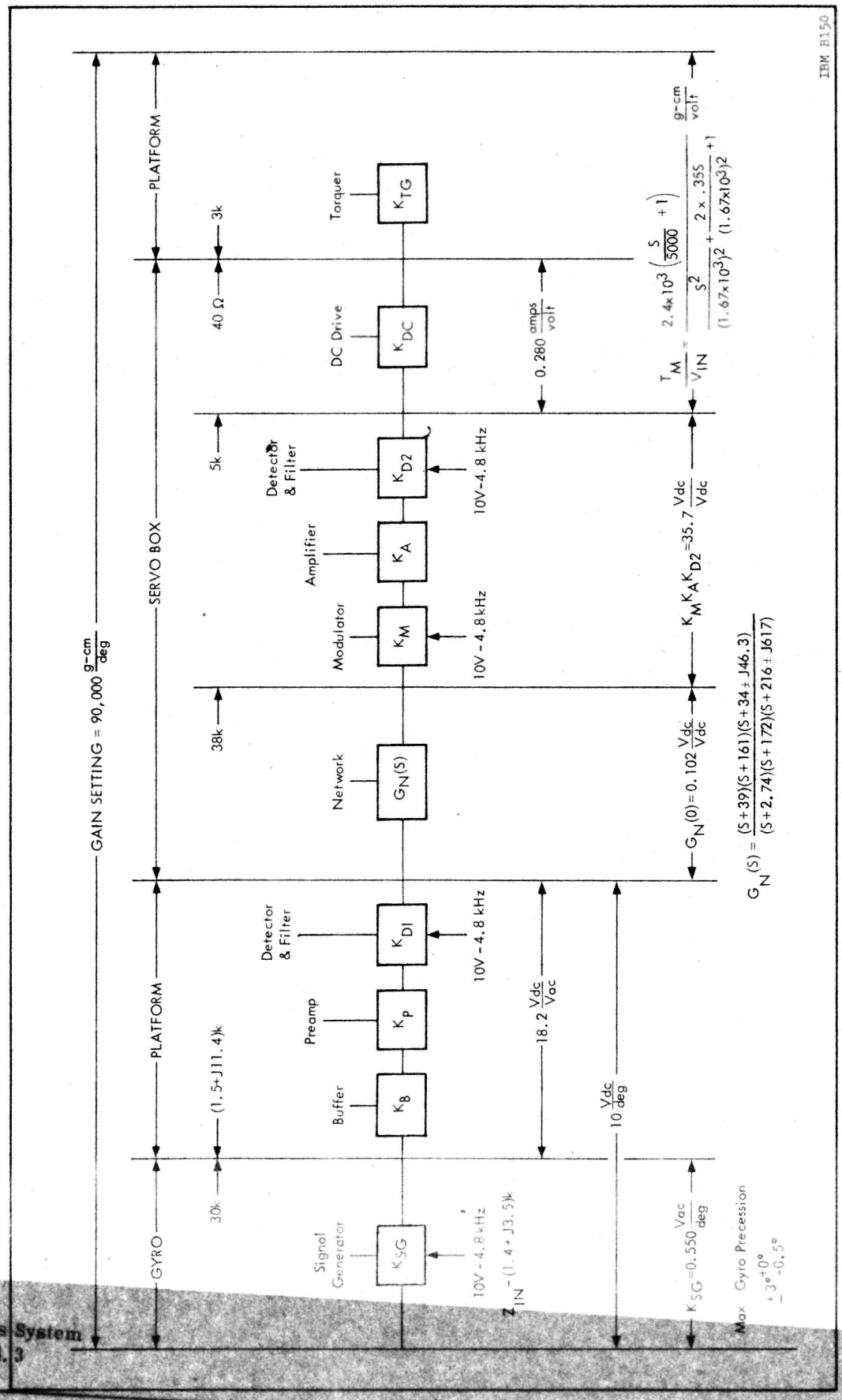


Figure 14.3-4. Typical Gimbal Electronics Block Diagram

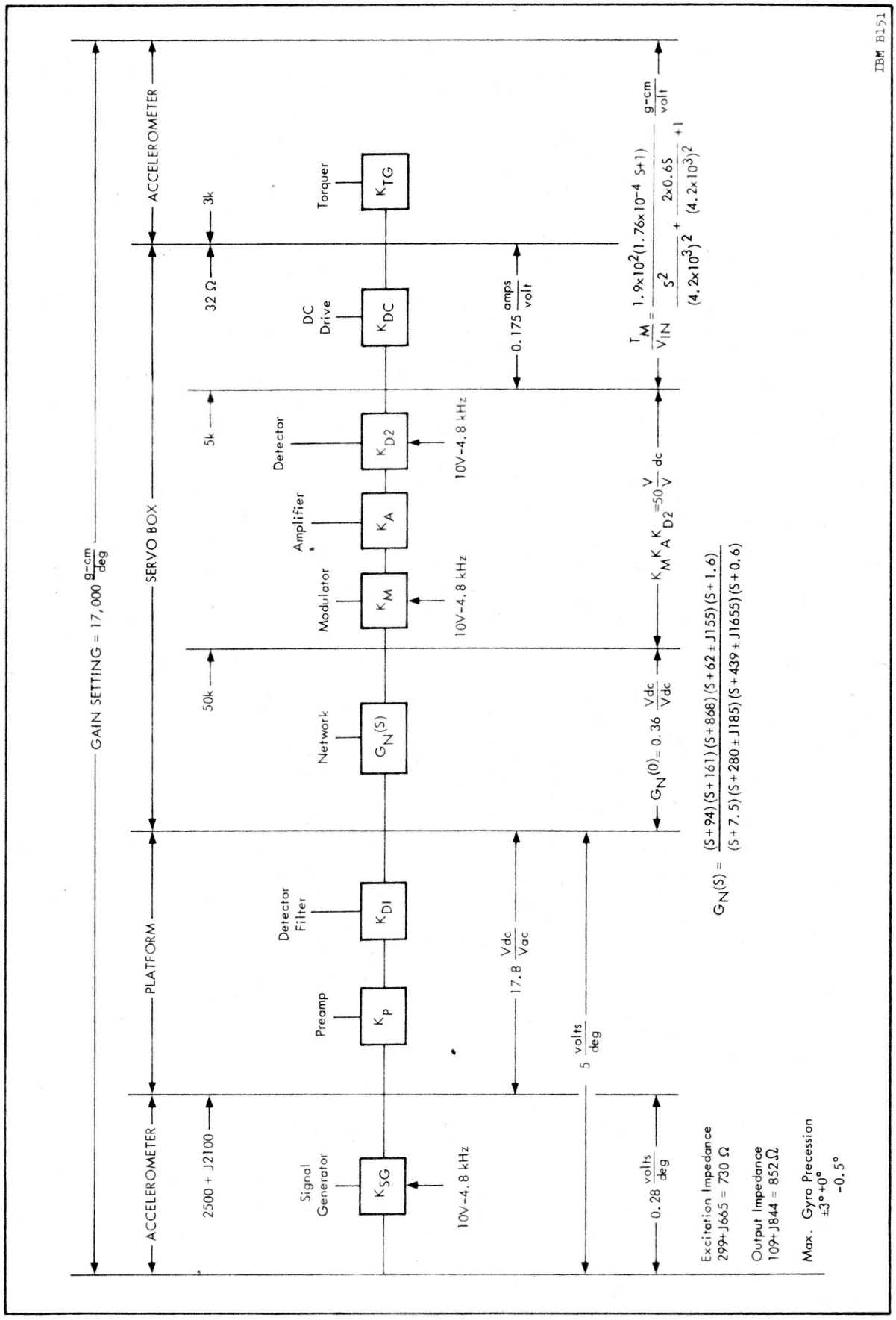


Figure 14.3-5. Accelerometer Electronics Block Diagram

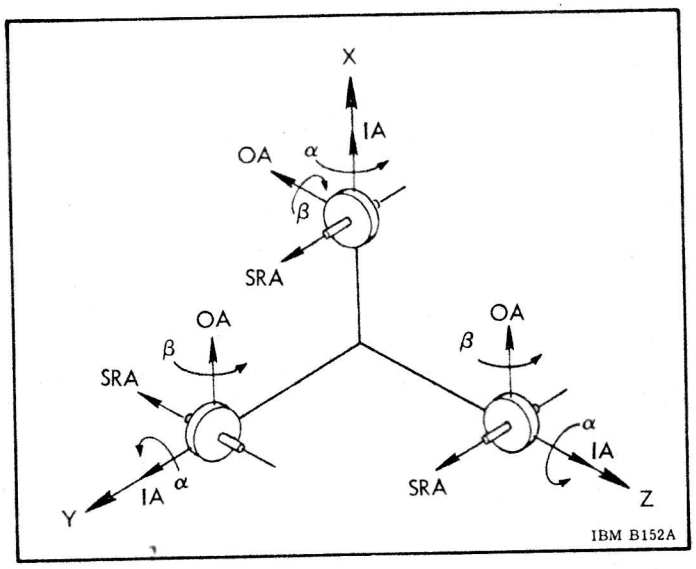


Figure 14.3-6 ST-124-M Gyro Orientation

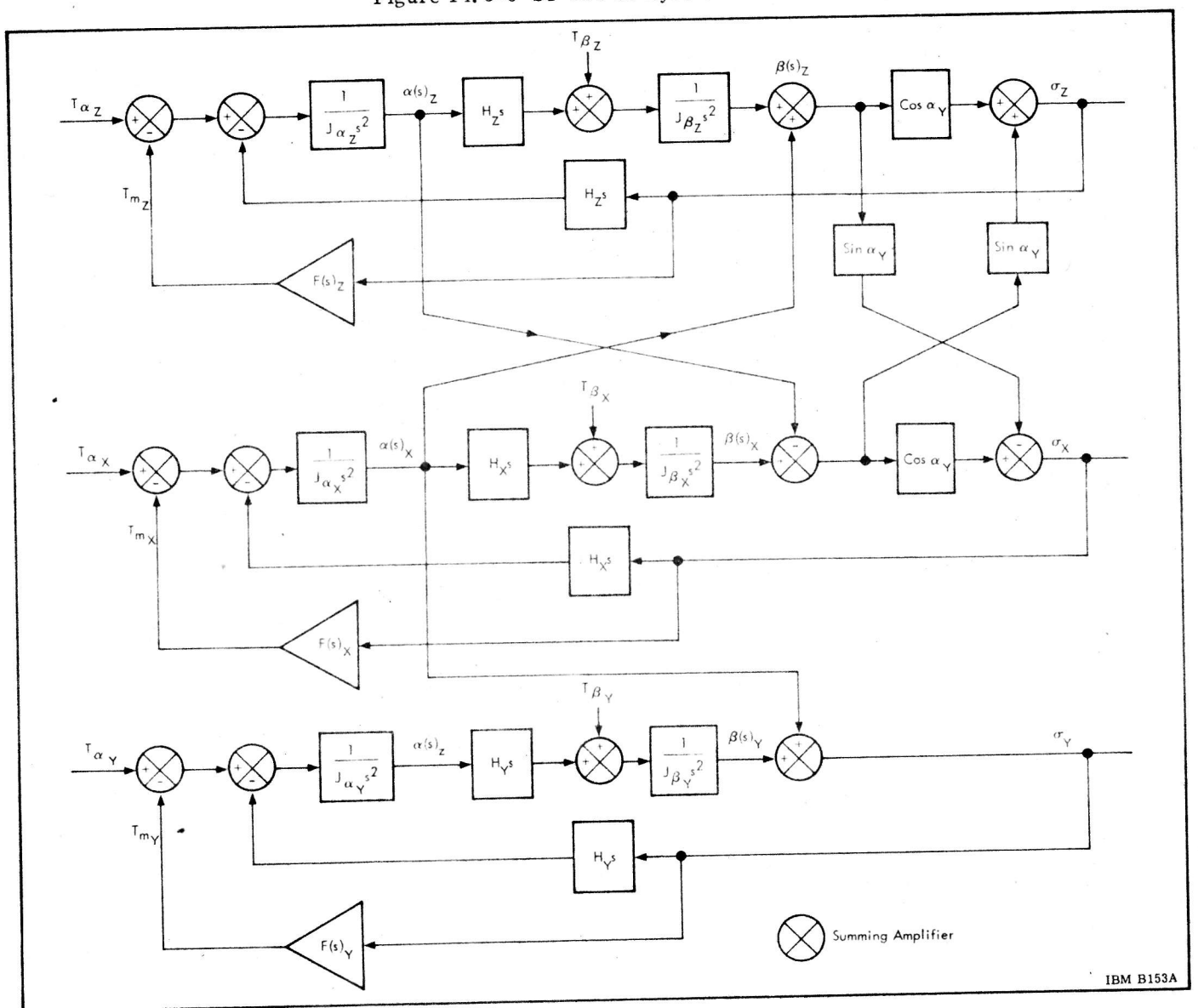


Figure 14.3-7 Three-axis Inertial Platform Assembly Block Diagram

SECTION 14.4
GIMBAL ANGLE DUAL-SPEED RESOLVERS

As shown in Figure 14.4-1, the +X, +Y, and +Z gimbal pivots have dual-speed analog resolvers for angular readouts.* The resolver output voltages are sent to the LVDA for analog-to-digital conversion. A schematic diagram is shown in Figure 14.4-2.

The dual resolver provides the required high readout accuracy. The LVDC/LVDA processes the measured gimbal attitude signals and computes the roll, pitch, and yaw vehicle body rates for the attitude control system.

The dual resolver has both a 32-speed and a single-speed winding on the same magnetic structure. The 32-speed winding provides 32 electrical rotations for one mechanical shaft rotation. The reference voltage, or resolver excitation (V_1), is 26 volts, 1016 hertz. The output winding drives an RC bridge network as shown in Figure 14.4-2.

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

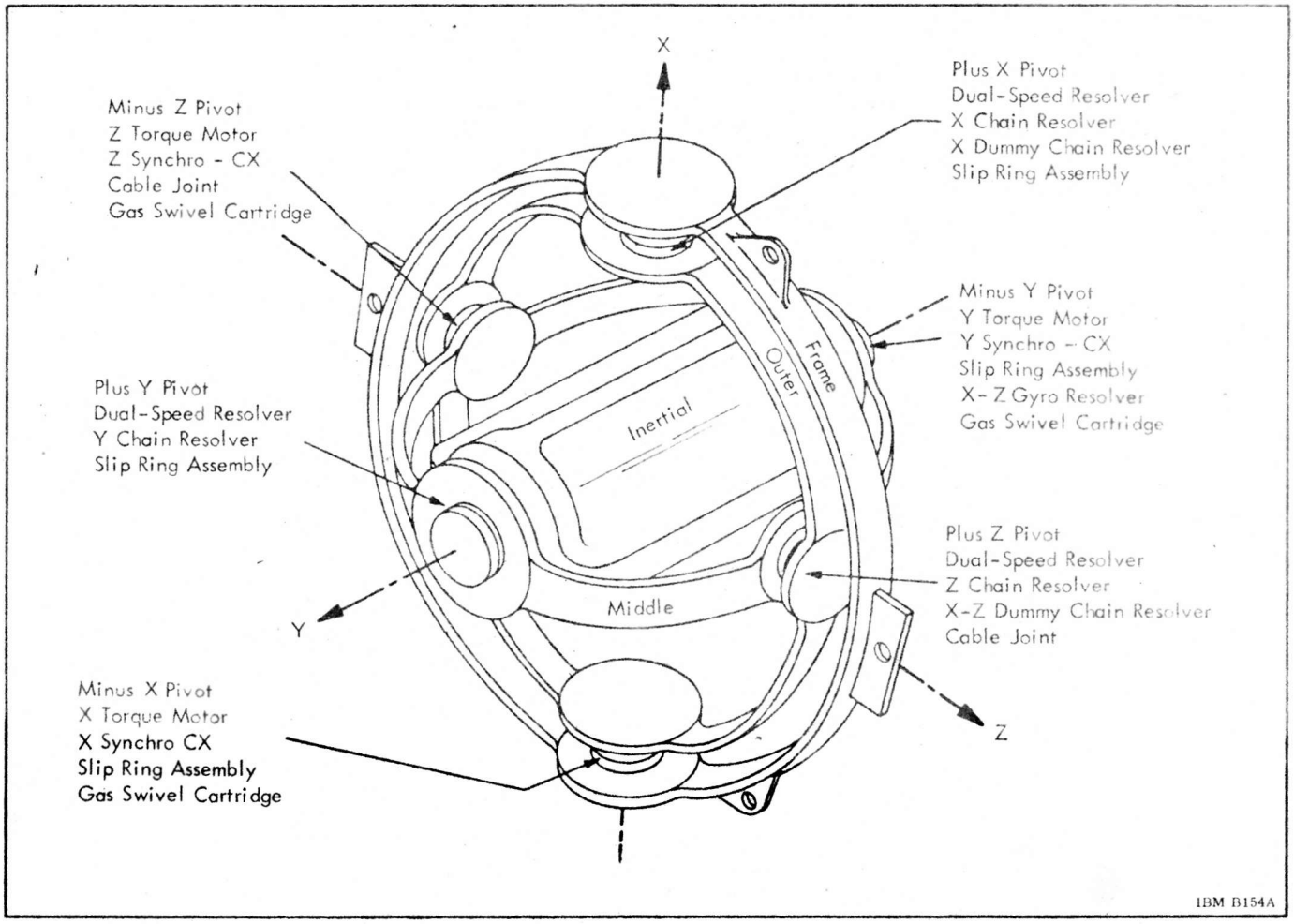


Figure 14.4-1. Three-Gimbal Configuration

The voltage V_2 at the input to the start pulse generator can be expressed as

$$V_2 = \frac{E}{\sqrt{2}} e^{j(32\theta - \pi/4)}$$

and the voltage V_3 at the input to the stop pulse generator can be expressed as

$$V_3 = \frac{E}{\sqrt{2}} e^{-j(32\theta - \pi/4)}$$

where E is the open circuit resolver voltage and θ is the rotation or mechanical angle in radians.

From the ratio of $\frac{V_2}{V_3} = e^{j(64\theta - \pi/2)}$, it is seen that the phase shift of V_2, with respect to V_3, is 64 times the angle θ or a multiplication by a factor of 2 occurs in the bridge network.

As the instantaneous voltage V_2 passes through zero with a positive slope, a start pulse is generated which opens a gate and a counter counts a 2.048 megahertz clock frequency. As V_3 passes through zero with a positive slope, a stop pulse is generated which closes the gate and stops the counter. The number of cycles counted is a measure of the gimbal angle (Refer to the vector diagram in Figure 14.4-3).

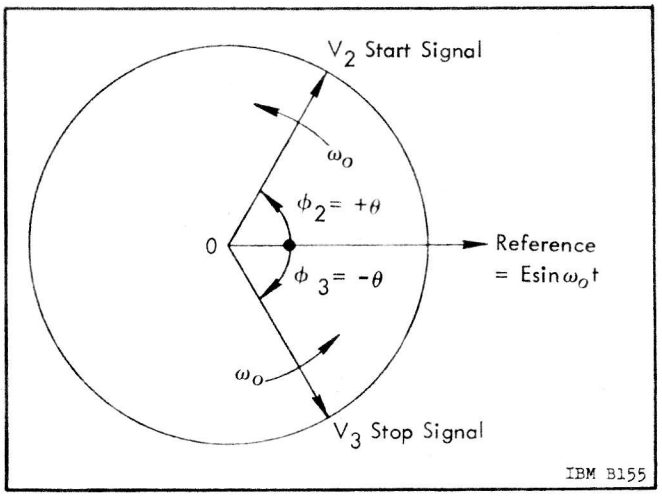
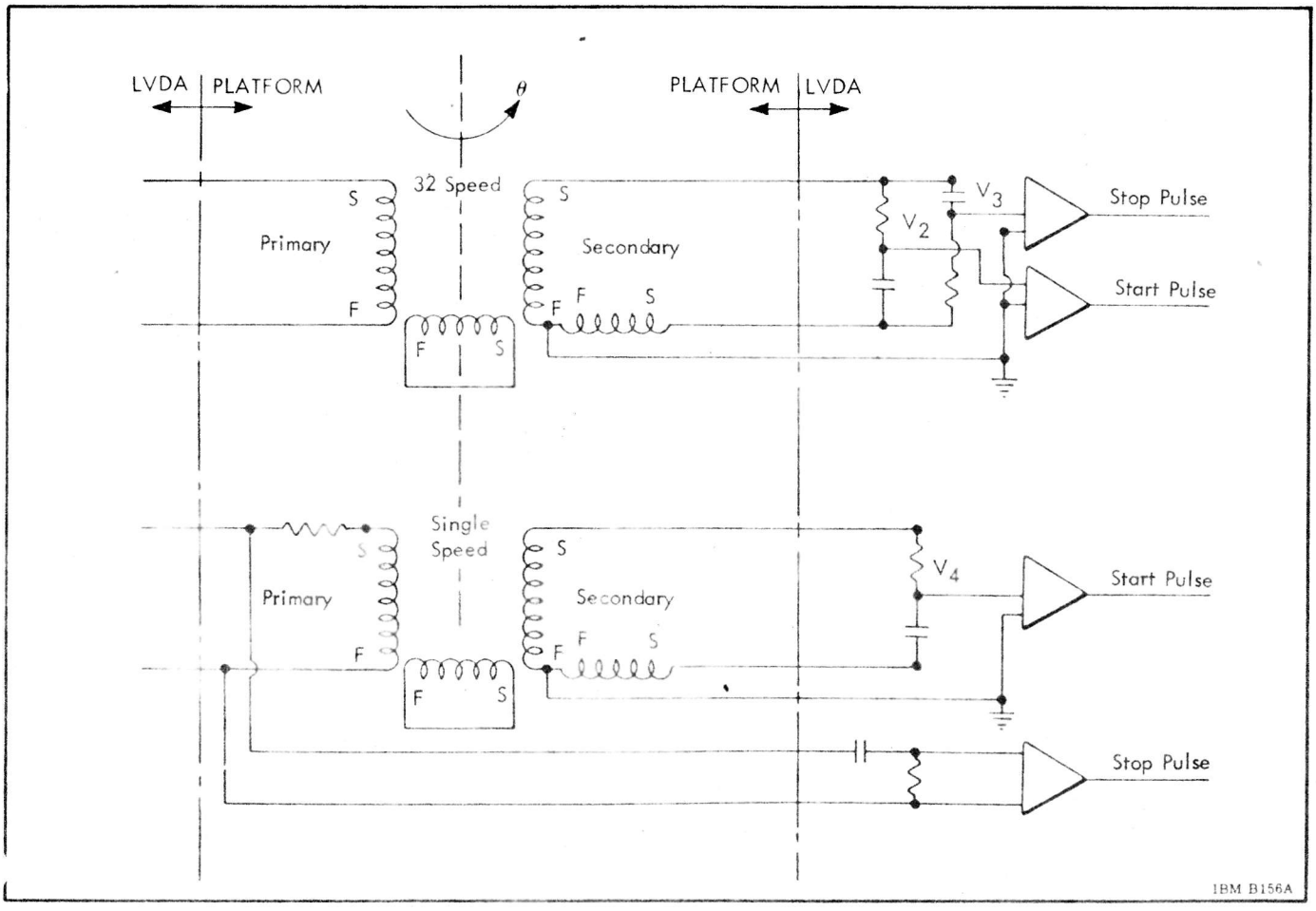


Figure 14.4-3 Gimbal Angle Vector Diagrams



. Figure 14.4-2. Dual-Speed Resolver Schematic

The single-speed winding uses a single RC passive network which generates a start pulse; the stop pulse is obtained from the reference voltage to the resolver primary as shown in Figure 14.4-2. The method of counting is the same as for the 32-speed windings. This information is utilized only if the 32-speed winding is lost. Thus, degraded accuracy occurs rather than complete failure.

The LVDA provides two frequency reference sources, one for the 32-speed winding and one for the single-speed winding. These references are controlled by the same frequency standard to insure that the gimbal angle measurement will not be lost if one reference source fails.

The 32-speed system accuracy is basically insensitive to temperature variation of the resolver, as well as impedance unbalance in the output windings. The open circuit voltage of the resolver is the basic reference voltage as shown in the equations.

The resolver and performance characteristics of the angular readouts are listed in Table 14.4-1.

The Platform system also contains an analog resolver chain system which can provide vehicle roll, pitch, and yaw attitude steering signals directly to the control system. This is a backup system and is not planned as flight equipment. The capabilities will be utilized in the ground checkout system to program the platform gimbals for vehicle control system calibration.

The resolver chain system includes three servo-driven resolvers whose shafts are time programmed from the ground computer with a maximum rate of 2 degrees per second; operational rate is 1 degree per second. These units are located in the inertial data box.

The resolver chain schematic is shown in Figure 14.4-4. The resolvers X_X, X_Y, and X_Z are the time-programmed units. The characteristics of the resolver chain system are listed in Table 14.4-2.

The resolver chain performs coordinate transformation computations. From Figure 14.4-4, it can be seen that the resolver chain provides six transformation matrices. With proper detection, two chain references (f_1 and f_2) allow vehicle roll, yaw, and pitch signals to be detected from the transformation matrices. The 1.6-kilohertz signal on the $\overline{Y}_B$ winding and the 1.6-kilohertz signal on the $\overline{X}_B$ at the output of the resolver chain provide the roll and pitch rates, respectively. The 1.92-kilohertz signal on the $\overline{X}_B$ winding provides the yaw rate. If redundant steer-

Table 14.4-1 Angular Readout Characteristics

Resolver Characteristics	32-Speed	Single-Speed
Excitation voltage	26 V ± 5%	26 V ± 5%
Harmonic content of excitation	0.1%	0.1%
Excitation frequency	1016 Hz ± 0.01%	1016 Hz ± 0.01%
Excitation power	1.8 W	0.08 W
Mechanical accuracy	± 10 arc sec	± 30 arc min
Secondary voltage maximum (open circuit)	5.0 V	5.0 V

System Characteristics	
System high speed	64:1
System low speed	1:1
Static accuracy	± 30 arc seconds
Dynamic accuracy (error is proportional to input rate)	20 arc seconds at 0.2 rad/second
Computer clock frequency	2.048 MHz ± 0.01%
Temperature range for optimum accuracy	± 30° C (54°F)

Table 14.4-2 Resolver Chain System Characteristics

Excitation		Demodulator Output	
f_1	26 V, 1.6 kHz	To control computer	3 Vdc/degree of arc
f_2	26 V, 1.92 kHz	To telemetry (fine)	± 2.5 Vdc/ ± 3 degrees
		(coarse)	± 2.5 Vdc/ ± 15 degrees
		Linear range	± 15 degrees

ing signals were required, a third reference (f_3) could be inserted at $\bar{X}_0$ and the detection system would provide an additional roll, yaw, and pitch signal at Z_B and $\bar{Y}_B$.

The detection scheme for the resolver chain is shown in Figure 14.4-5. When the vehicle coordinate system is aligned to the navigational coordinate system, the $\bar{Y}_B$ winding will have a standing voltage of 15 volts, 1.92 kilohertz which is in phase with vector $\bar{Y}_0$. This bias voltage is removed by a bucking voltage obtained from $\bar{Y}_0$ (f_2). The signals are filtered and, by means of signal bucking, detection filtering, modulation amplification, and redetection, are separated as shown in Figure 14.4-5. The output signals are dc with a scale factor of 3 volts per degree. The "3-sigma" accuracy of the resolver chain is 9 arc minutes over a complete cycle.

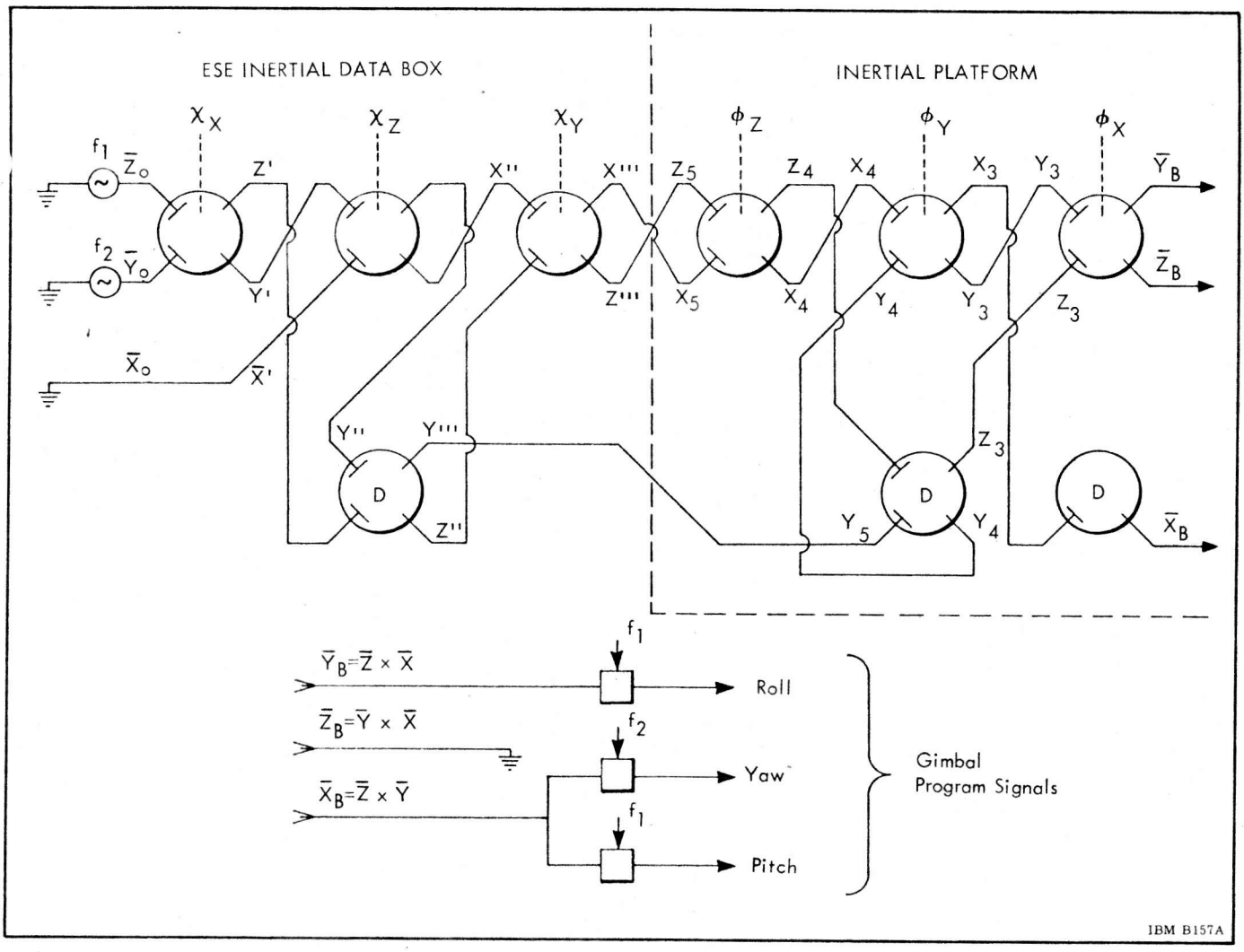


Figure 14.4-4 Resolver Chain Schematic

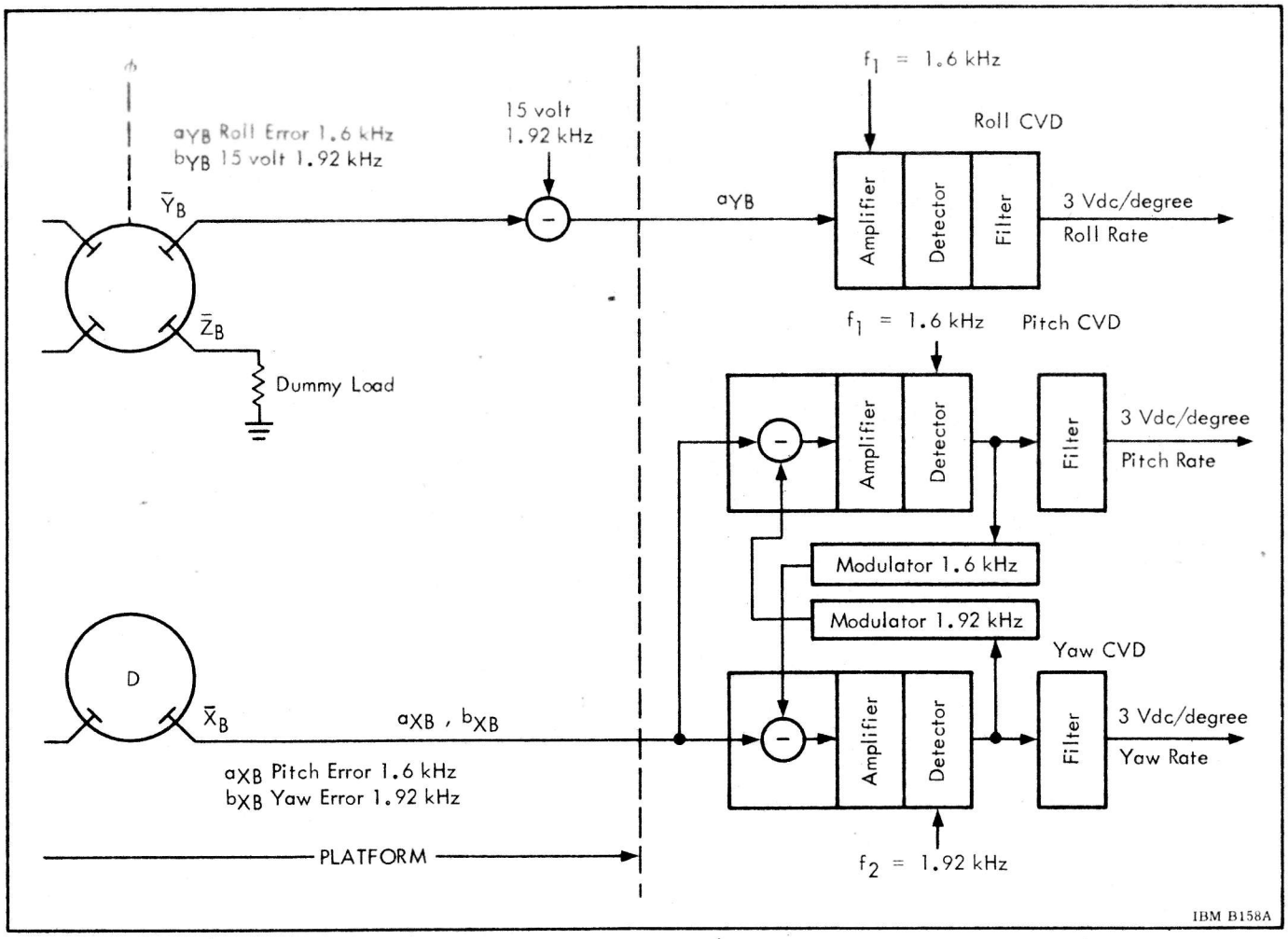


Figure 14.4-5. Resolver Chain Signal-Detection Scheme

SECTION 14.5
OTHER PLATFORM SYSTEM UNITS

14.5.1 PLATFORM ELECTRONIC ASSEMBLY

The ST-124-M Platform Electronic Assembly contains the electronics, other than those located in the Platform, required for the Platform axis and accelerometer stabilization. Switching electronics for controlling Platform system power and checkout functions are also located in the Platform Electronic Assembly. The electronics are printed circuit, modular constructed, and are fitted into the box with an electrical connector (for ease of assembly and maintenance).

Components or modules requiring pressurization are protected by epoxy encapsulation. Internal heat sources are heat-sinked to the main casting, with heat being removed by conduction into the temperature controlled mounting panels (cold plates) of the Instrument Unit. For system evaluation, critical control signals are conditioned in the Platform Electronic Assembly and supplied to telemetry.

The Platform Electronic Assembly is a cast magnesium structure and is mounted to the cold plates with pads which extend out from the box structure. The box has a light-gauge sheetmetal cover, which is gasket-sealed and maintains a pressure of 1.4 N/cm^2g (2 psig). Internally, the box contains a cast magnesium deck for mounting electronic components and a grooved rack for mounting printed circuit modules. The assembly weighs 19 kilograms (42 pounds).

14.5.2 PLATFORM AC POWER SUPPLY

The ST-124-M Platform AC Power Supply (Figure 14.5-1) furnishes the power required to run the gyro wheels, excitation for the platform gimbal synchro, and frequency sources for the resolver chain references and for gyro and accelerometer servo-systems carrier. The power supply is a regulated, solid-state, three-phase, ac power supply capable of supplying up to 250 VA continuously. With an input voltage from 24 to 30 Vdc, it produces a three-phase sine wave output, which is fixed at 26.5 volts (rms) line-to-line at a fixed frequency of 400 ± 0.01 hertz. Three single-phase, 20-volt (no load) reference-square-wave outputs of 4.8 kilohertz, 1.92 kilohertz, and 1.6 kilohertz are also provided.

The oscillator in the power supply generates a temperature-stable square wave of 19.2 kilohertz derived by frequency division from a 2.45-megahertz quartz crystal oscillator. This 19.2-kilohertz square wave is the frequency source from which all the frequency outputs are derived.

The frequency divider network, referenced with the 19.2-kilohertz square wave, produces two buffered 4.8-kilohertz square waves. One 4.8-kilohertz wave becomes the "clock pulse" for the cycle register; the other feeds the regulator-driven amplifier. In addition, the network provides dividers and buffers for the auxiliary outputs. All frequency-divider circuits use Johnson-type counter logic to provide symmetrical square wave outputs to eliminate complicated decoding gates. The network section utilizes integrated circuits construction.

The cycle register produces six push-pull, square-wave, 400-hertz outputs phased in 30-degree time increments. The 4.8-kilohertz signal from the divider network is used as the clock pulse to trigger the six register flip flops. The flip flops are bistable circuits of the same type (integrated-circuit) used in the frequency divider network.

Each cycle register flip flop drives one channel of the power amplifier. One channel consists of two cascaded push-pull stages which are transformer coupled; all transistors operate in the switching mode, which contributes to the high efficiency of the inverter. Each channel excites a push-pull primary winding of a toroidal output transformer. The secondary windings consist of three per transformer with a 4:3:1 winding ratio (A of Figure 14.5-2). Each of the outputs has 1 winding from each of the 6 transformers (B of Figure 14.5-2) in a combination of 3 pairs with a 4:3:1 wattage ratio. The manner in which these ratios are used in the generation of the sine wave output is illustrated in C of Figure 14.5-2.

The output voltages contain 15-percent harmonic distortion. A low-pass output filter reduces this distortion by approximately 10:1. The voltage regulator compares a sample of the three-phase output voltage with a stable Zener reference voltage, then amplifies the error and biases the power amplifier to close the loop.

The 19.2-kilohertz oscillator, the frequency dividers, the network dc supply, and the cycle register operate in dual redundancy. If the 400-hertz voltage is not detected in channel A, a bistable switching circuit will instantly switch power demand to channel B.

The Platform AC Power Supply box is cast magnesium and has a light-gauge sheetmetal cover, which is gasket-sealed and maintains a pressure of 1.4 N/cm^2g (2 psig). Modular-potted construction is used throughout. Motherboard printed circuit boards with integrated circuitry minimize internal wiring. The weight of the assembly is 14.5 kilograms (32 pounds).

14.5.3 ST-124-M ACCELEROMETER SIGNAL CONDITIONER

The ST-124-M Accelerometer Signal Conditioner accepts the velocity signals from the Platform accelerometer optical encoders and shapes them before they are passed on to the LVDC/LVDA. Each accelerometer requires 4 shapers — a sine shaper and a cosine shaper for the active channel and a sine shaper and a cosine shaper for the active channel and a sine shaper and cosine shaper for the redundant channel.

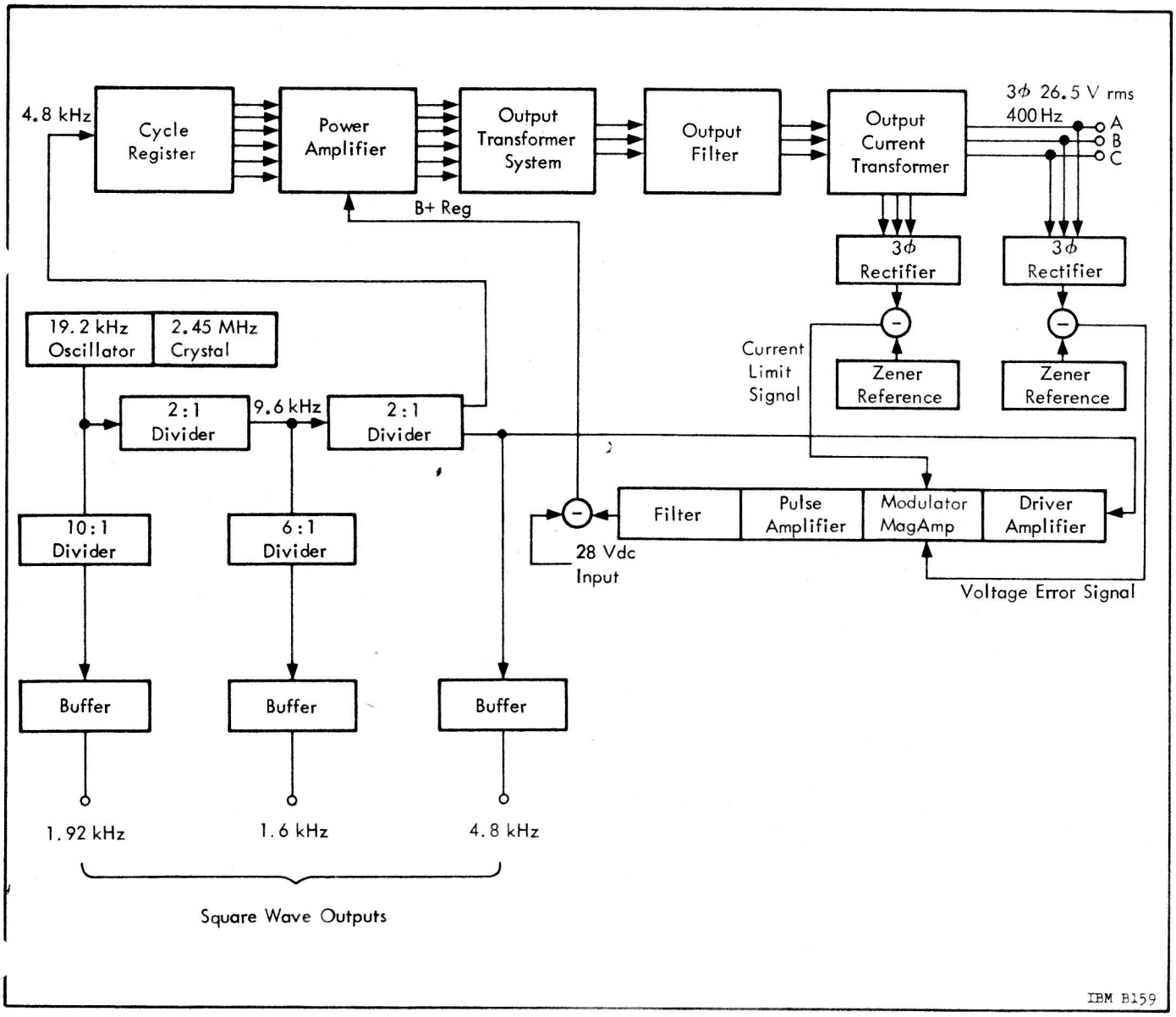


Figure 14.5-1. Platform AC Power Supply Block Diagram

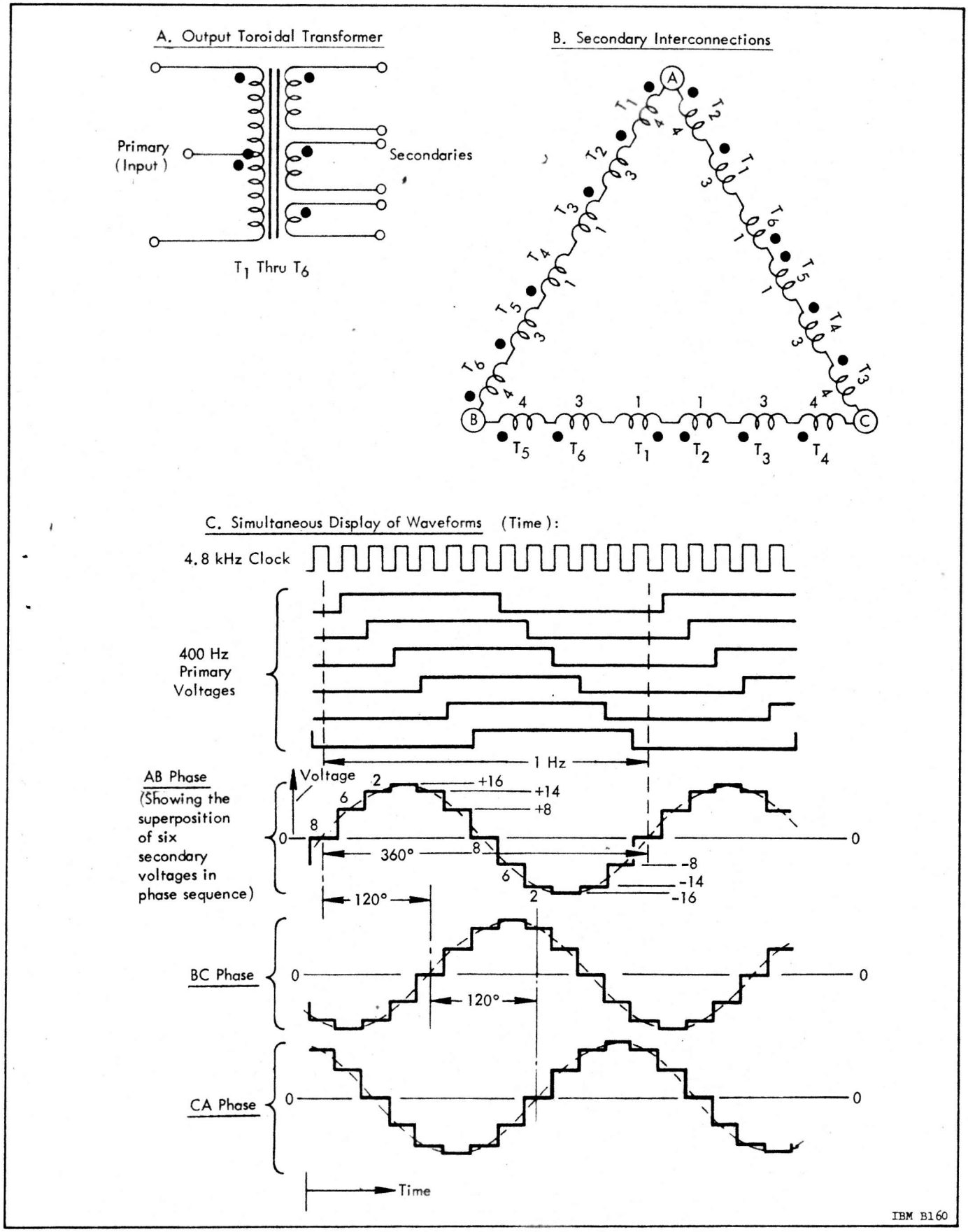


Figure 14.5-2 Generation of 3-Phase, 400-Hertz Voltage

Also included are four buffer amplifiers for each accelerometer — one for each sine and cosine output. The output of these buffers is furnished to the blockhouse for a prelaunch accelerometer calibration check. The accelerometer telemetry velocity signals are also conditioned in this assembly. Characteristics of the velocity signals are listed in Table 14.5-1.

The total assembly weighs approximately 4.5 kilograms (10 pounds) and is fabricated from a magnesium casting. Light-gauge sheetmetal covers with gasket seals maintain an internal pressure of 1.4 N/cm^2g (2 psig).

Table 14.5-1 Characteristics of the Accelerometer TM Velocity Signals

Output voltage levels	0-6 volts minimum (3 volt bias) 0-8 volts maximum (4 volt bias)
Signal rise time	10 μs on square wave
Output frequency of acceleration signal	$\pm$ 20 g (50 Hz/g)

SECTION 14.6
PLATFORM ERECTION SYSTEM

The erection of the Platform to the local vertical is accomplished by two gas bearing pendulums which are fitted to the inertial gimbal. The input axes of the pendulums are parallel to the Y and Z accelerometer measuring axes*.

The gas bearing pendulum is a single-axis gravity-sensing device. Its sensing element is a gas-floated slug which supports a soft iron core as shown in the cutaway view of Figure 14.6-1. The iron slug moves inside the coils of a linear differential transformer which provides the electrical output signal. Damping of the slug motion is provided by a chamber and an exhaust orifice while the spring restraint is obtained magnetically.

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

The characteristics of the pendulums are listed in Table 14.6-1.

A block diagram of the erection system is shown in Figure 14.6-2. The input axes of the Y and Z pendulums are along the inertial gimbal Y and Z axes, respectively. The pendulum output is amplified by a preamplifier on the Platform and then transmitted to the ground equipment alignment amplifier.

The alignment amplifier provides a proportional plus integral path to the torquer drive amplifier, which returns the signal from the ground to the variable coil of the gyro torque generator. The erection system is a second order system with a natural frequency of 0.05 radian per second and a damping ratio of 0.5. The leveling accuracy of the erection system is ± 2.5 arc seconds.

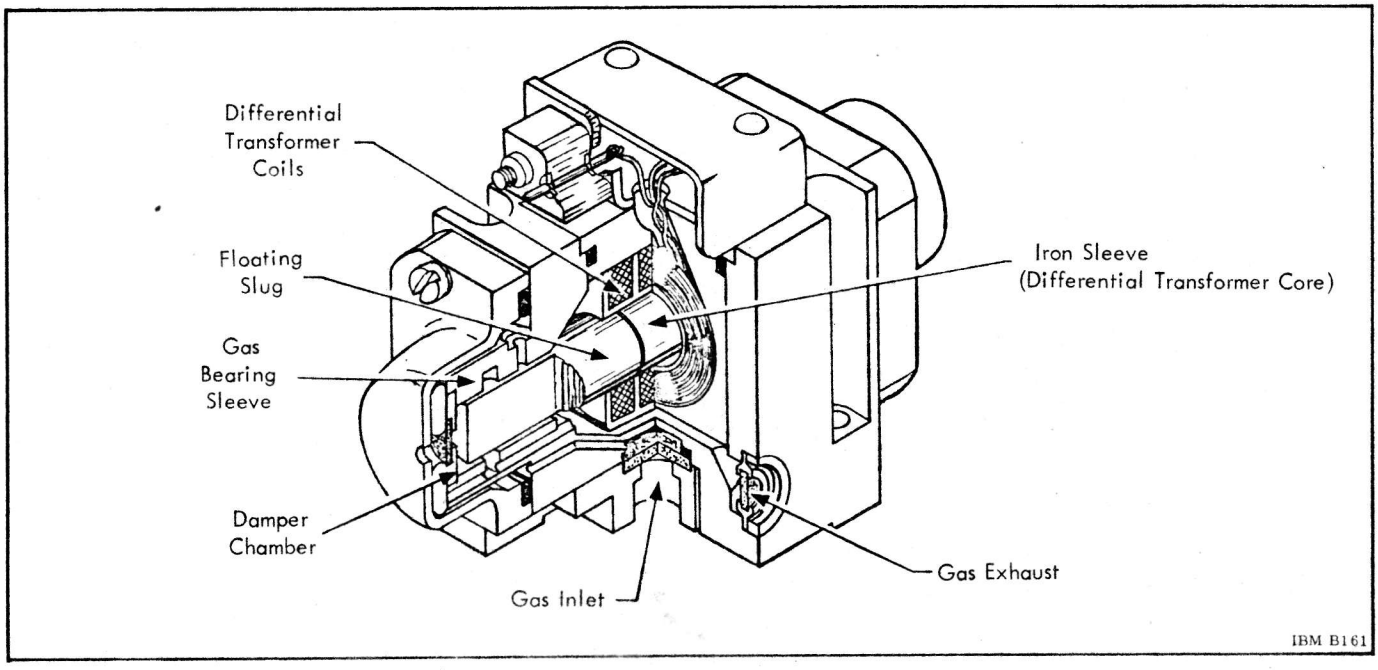


Figure 14.6-1 Gas Bearing Pendulum

Table 14.6-1 Gas Bearing Pendulum Characteristics

Physical Characteristics	
Volume	57.5 cm^3 (3.5 in^3)
Weight	75 grams (0.6165 pound)
Gas Bearing	
Gas pressure	10.3 N/cm^2d (15 psid)
Gas flow	0.028 m^3/h ($\approx$ 1 SCFH)
Gas gap	0.015 to 0.02 cm (0.006 to 0.008 in.)
Signal Generator	
Type	Inductive
Excitation	4 V, 400 hertz
Sensitivity	400 mV/degree
Performance	
Leveling accuracy	± 2.5 arc seconds
Input range	± 0.5 degree (signal saturation)
Time constant	10 seconds

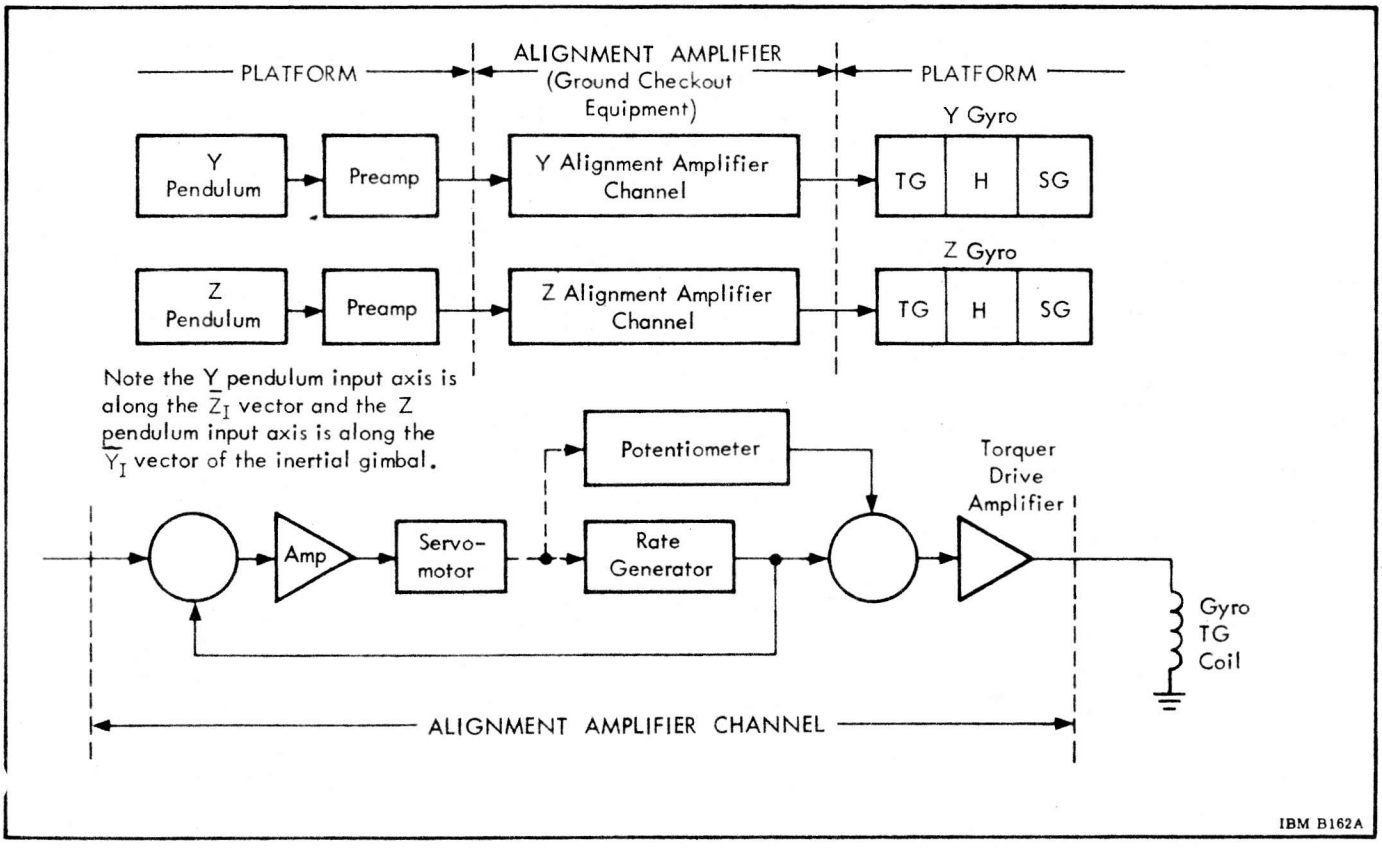


Figure 14.6-2. Platform Erection System Block Diagram

SECTION 14.7
AZIMUTH ALIGNMENT SYSTEM

The azimuth alignment system orients the Platform +Z coordinate axis* to the desired flight azimuth. To obtain the high accuracy requirement, the azimuth alignment system utilizes electro-optical techniques. The basic elements of the azimuth alignment system are an autocollimating theodolite with detection system, synchro encoder servosubsystem, launch control computer for azimuth programming and reference, and an alignment torquing servosubsystem. Fitted to the inertial gimbal is a porro prism (intermediate infrared) with its dihedral edge parallel to the Z axis of the inertial gimbal. A second prism (near infrared) is fitted to the stator of the two-speed synchro which has its dihedral edge free to rotate in the Y-Z plane (Figure 14.7-1).

The basic element of the optical system is the SV-M2 Theodolite (Figure 14.7-2). The system consists of an autocollimating theodolite with necessary optics and detectors, a penta mirror set, an automatic sway control system, reference prism with stand, closed circuit TV monitoring system, and support electronics and control.

The theodolite has three control channels — the synchro prism, the inertial prism, and a trihedral prism (Figure 14.7-3). An infrared energy spectrum is generated by a tungsten filament lamp. This spectrum has a bandwidth of two microns which lie between 0.7 and 2.7 microns. Atmospheric absorption of infrared in this bandwidth occurs at 1.35 and 1.8 microns. Therefore, the control channels are divided at 1.35 and 1.8 microns with the 0.7 to 1.35 microns near infrared-band assigned to the synchro prism, the 1.25 to 1.8 microns intermediate infrared-band assigned to the inertial prism, and 1.8 to 2.6 micron far infrared-band assigned to the trihedral prism (Figure 14.7-4). The prisms have a dichroic multilayer coating that allows only the desired bandwidth of energy to pass.

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

The angular position of the synchro prism is controlled directly from the theodolite. A theodolite error signal drives a servoamplifier which is located in the launch umbilical tower. The amplifier output is transmitted to the Platform where it excites a servomotor located on the inertial gimbal. The servomotor positions the synchro prism through a gear train of 10^5:1, reducing any angular error to zero. This loop is active throughout countdown until vehicle liftoff. The angle between the inertial gimbal (navigation coordinates) and movable prism is measured by a precision 25:1 dual-speed control transmitter synchro (Figure 14.7-5). The inertial prism is controlled by the theodolite output signal through the roll alignment servoelectronics by torquing the roll gimbal until the prism is acquired.

The trihedral prism, which is fixed to the vehicle, is used as reference for a servosystem to position the penta mirror which provides the theodolite with the capability of translatory tracking. At the vehicle elevation of the Platform system, the SV-M2 Theodolite (Saturn V, Mod 2) will compensate for a ± 35.5 centimeters (± 14 inches) translation movement of the vehicle. The trihedral prism servoloop increases the aperture of the autocollimator from 20 centimeters (8 inches) to 81 centimeters (32 inches) at a rate of 81 centimeters/second (32 inches/second).

Prism acquisition signals from the three channels are generated with the same infrared-coded bandwidths that produce the error signals. These are used to automatically block and/or initiate other events in the vehicle launch procedure and azimuth alignment system. Indicator lights on the theodolite control panel in the launch control center confirm that the 3 prisms are in the acquisition range of the theodolite. Two closed-circuit TV monitor systems provide the launch control center with a view of the 3 prisms and a monitor of the theodolite control and display panel in the theodolite hut.

The elevation angle (nominally 25 degrees from horizontal) of the theodolite is set by a dc motor-driven actuator which is manually controlled

from the launch control center. At the Saturn V launch complex, the theodolite can operate with a 35.5 centimeter (± 14 inches) variation in elevation without requiring any adjustment.

The encoder-synchro package consists of a 25:1 dual-synchro, an 18-bit optical shaft angle encoder, and a motor-tachometer-gear assembly. The encoder is provided with an enclosure containing strip heaters to maintain the temperature within ± 5°C (9°F), maintaining the designed accuracy of ± 10 arc seconds. The encoder system has a self-generated encoder sampling time of 20 milliseconds. The output is a cyclic gray code with logic levels of 0 or 28 volts. The 25:1 dual synchro with the platform dual synchro has a back-to-back control transmitter: control transformer error of ± 10 arc seconds.

The reflected infrared energy from the prisms is acquired by the theodolite's optics. From this coded energy, the theodolite detects deviations from the desired position of the prisms. These coded signals are separated into their respective channels by slit prism angle filters and dichroic beam splitters.

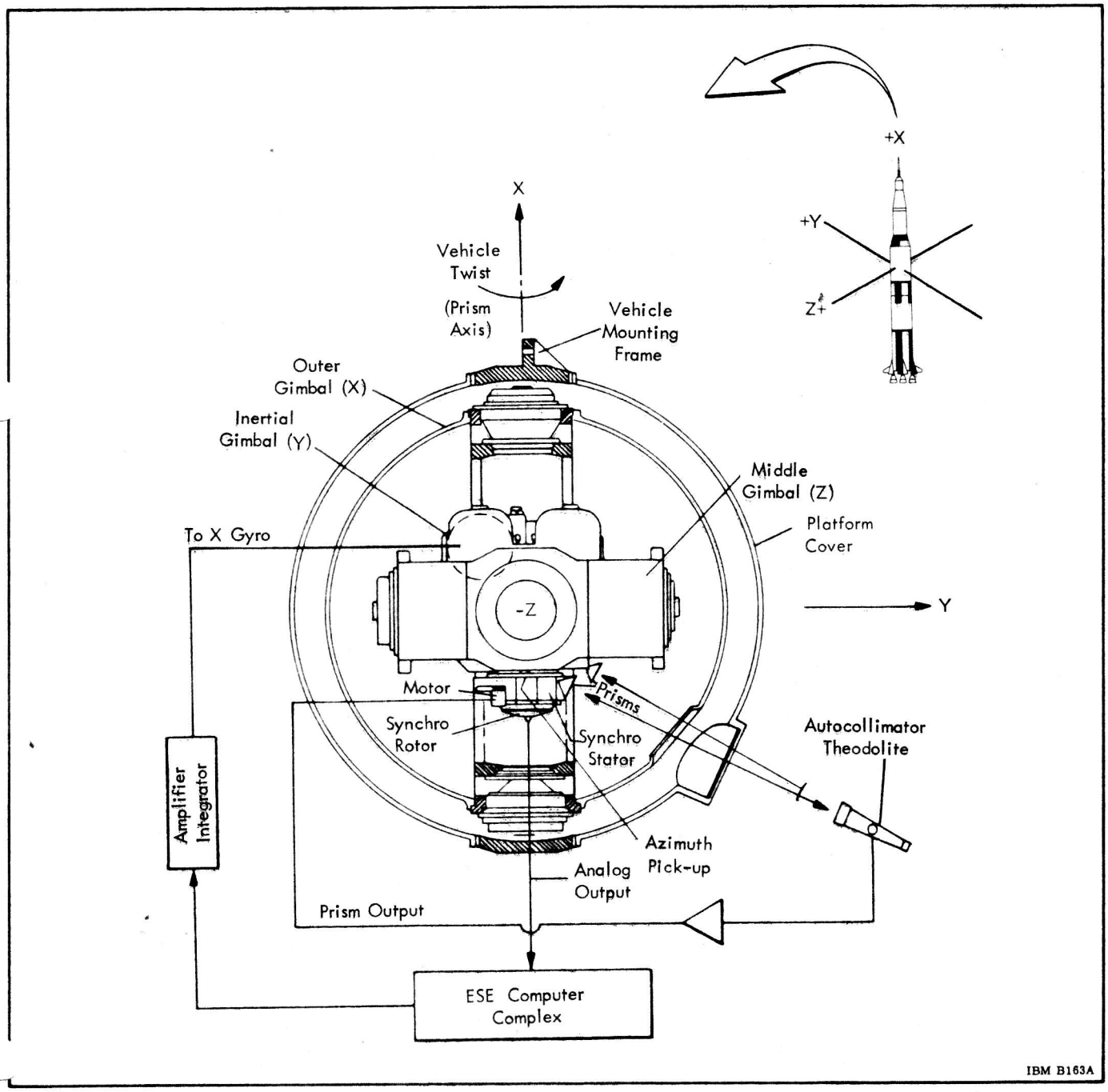


Figure 14.7-1 Automatic Azimuth Alignment

The dichroic beam splitters have a dichroic multilayer coating similar to the prisms. Each of the three channels has acquisition detectors which generate dc signals when the prisms are within the acquisition range of the theodolite. These signals are used to indicate acquisition and to control relay switching in various other vehicle-associated control functions. When an error exists in any channel, a representative portion of the infrared energy passes through the slit prism filter to the dichroic beam splitter and on to a lead sulfide detector. A phase-oriented ac voltage is generated which is directionally proportional to the angular error. This voltage is amplified and demodulated to achieve the desired signal gradient of 100 millivolts per arc second.

The simplified azimuth block diagram in Figure 14.7-6 shows the operation of the azimuth alignment system. After all systems have been energized, the erection system positions the inertial gimbal to the local vertical. The azimuth alignment equipment is switched into the acquisition mode. This closes contacts A, B, C, and D and opens contacts E, F, G, and H. A bias signal is injected into the synchro prism servoloop to drive this prism into acquisition; the acquisition signal removes the bias and closes the synchro prism servoloop on the theodolite and drives the synchro prism to null.

The output of the dual-speed control transformer drives the encoder-synchro servoloop until the synchro output is zero through contact E. The RCA-110A Launch Computer reads and stores the position of the 18-bit encoder. Thus, the baseline azimuth is stored in the computer. This is the azimuth of the navigation coordinate system and is the reference from which launch azimuth is established. Any deviation from this position will generate an error signal in the CX:CT measurement causing the X gyros to torque the gimbal and reduce the error to zero.

The mission azimuth is established with contacts A, B, C, and D open and contacts E, F, G, and H closed. The launch control computer computes the

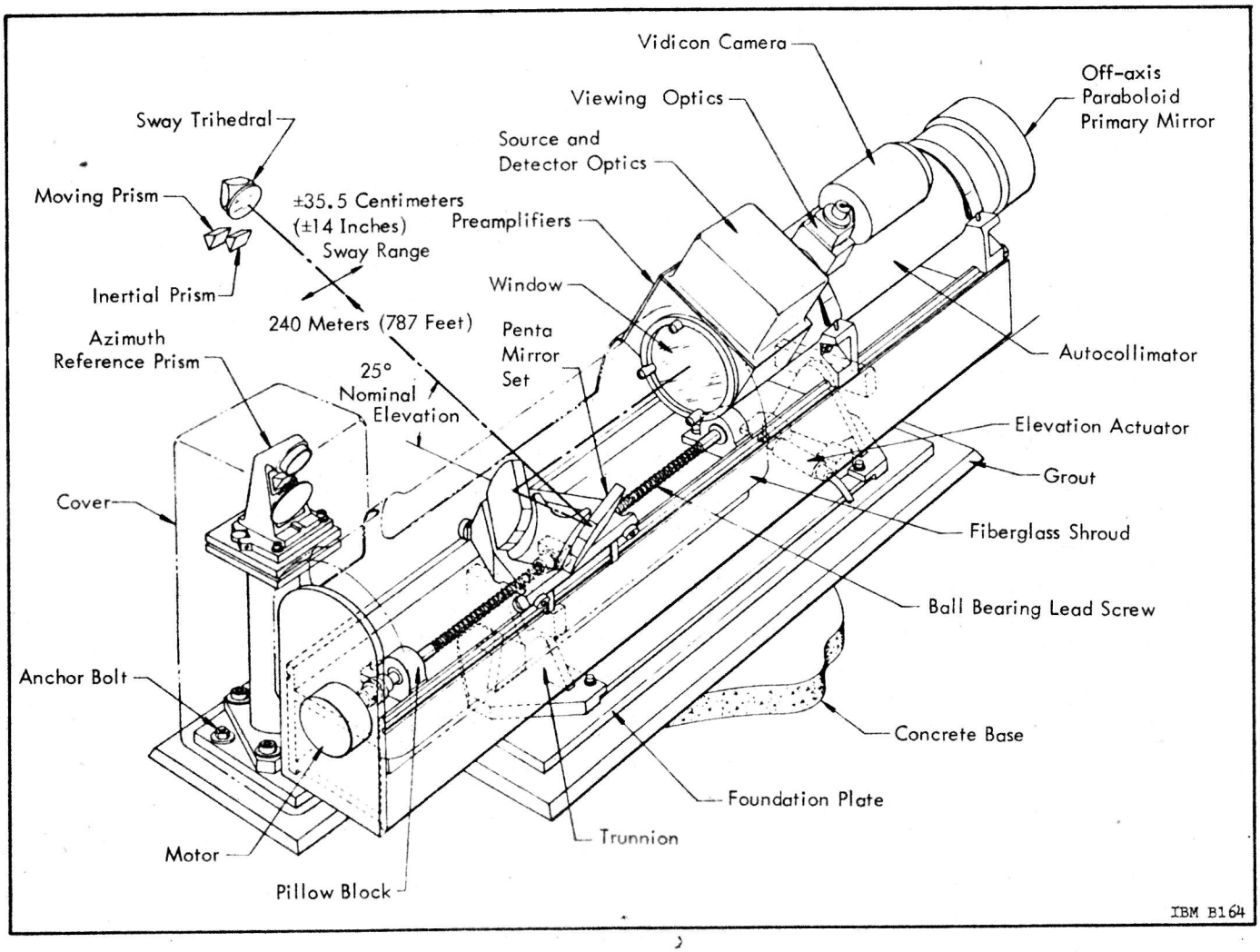


Figure 14.7-2 Theodolite

azimuth program angle by comparing the baseline azimuth to the stored mission azimuth and torquing the synchro-encoder repeater until the encoder output agrees with the computer. The error signal from the dual-speed synchro system is fed to the X gyro alignment loop and drives the inertial gimbal to the mission azimuth which also nulls the CX:CT unbalance. The synchro prism is held fixed with respect to the optical beam from the theodolite on the baseline azimuth. The inertial gimbal (navigation coordinates) is held on the mission azimuth with the CT acting as an azimuth pickoff. The azimuth angle computation is a function of the predicted launch time. The computer program translates any deviations from the predicted launch time into a respective azimuth angle change and repositions the inertial gimbal to the changing azimuth through the encoder synchro. The mission azimuth is displayed in the launch control center by a digital monitor.

The analysis of the azimuth alignment error shows the root sum squared system error to be less than ± 20 arc seconds.

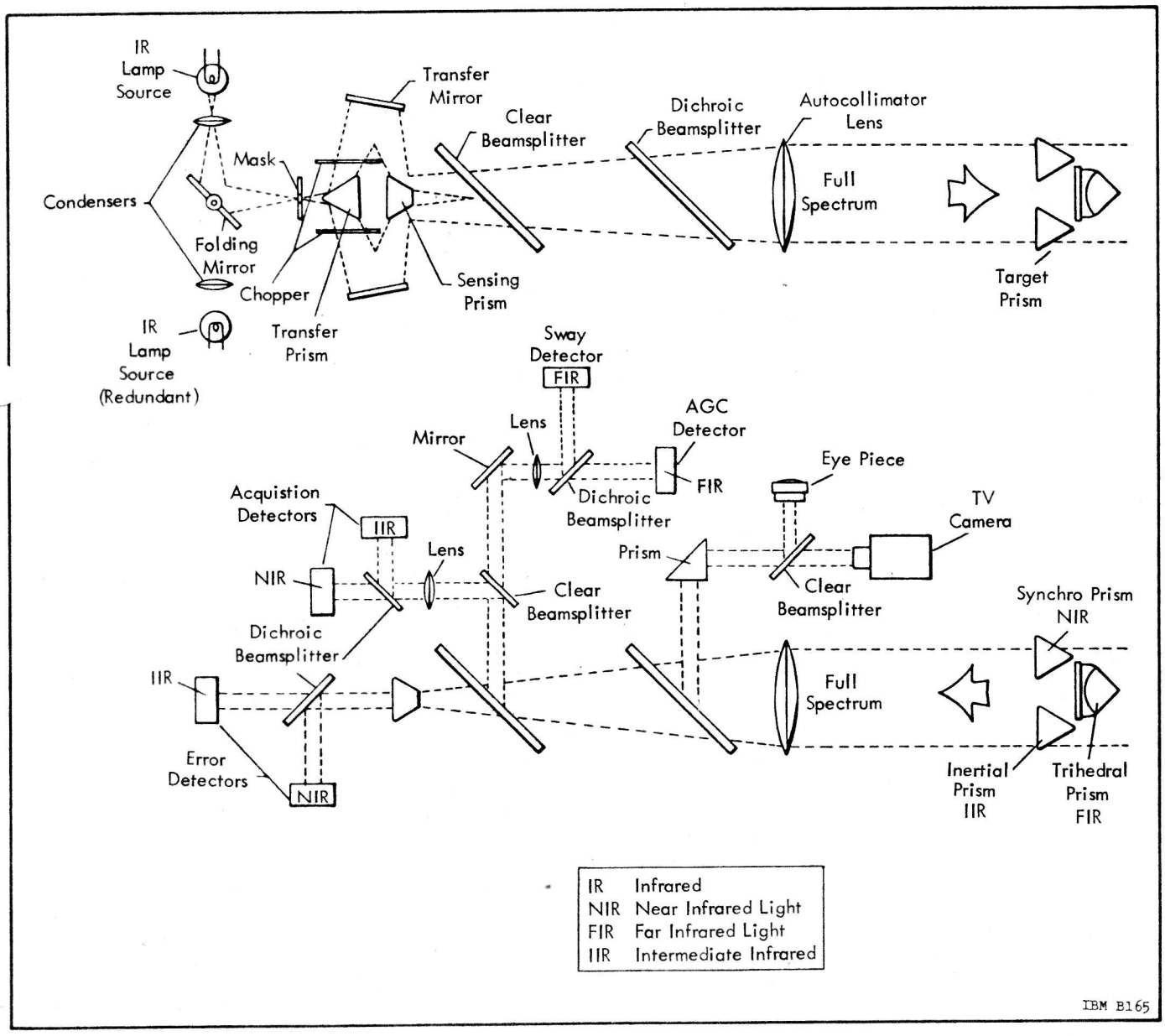


Figure 14.7-3 Optical Schematic Diagram of SV-M2 Theodolite

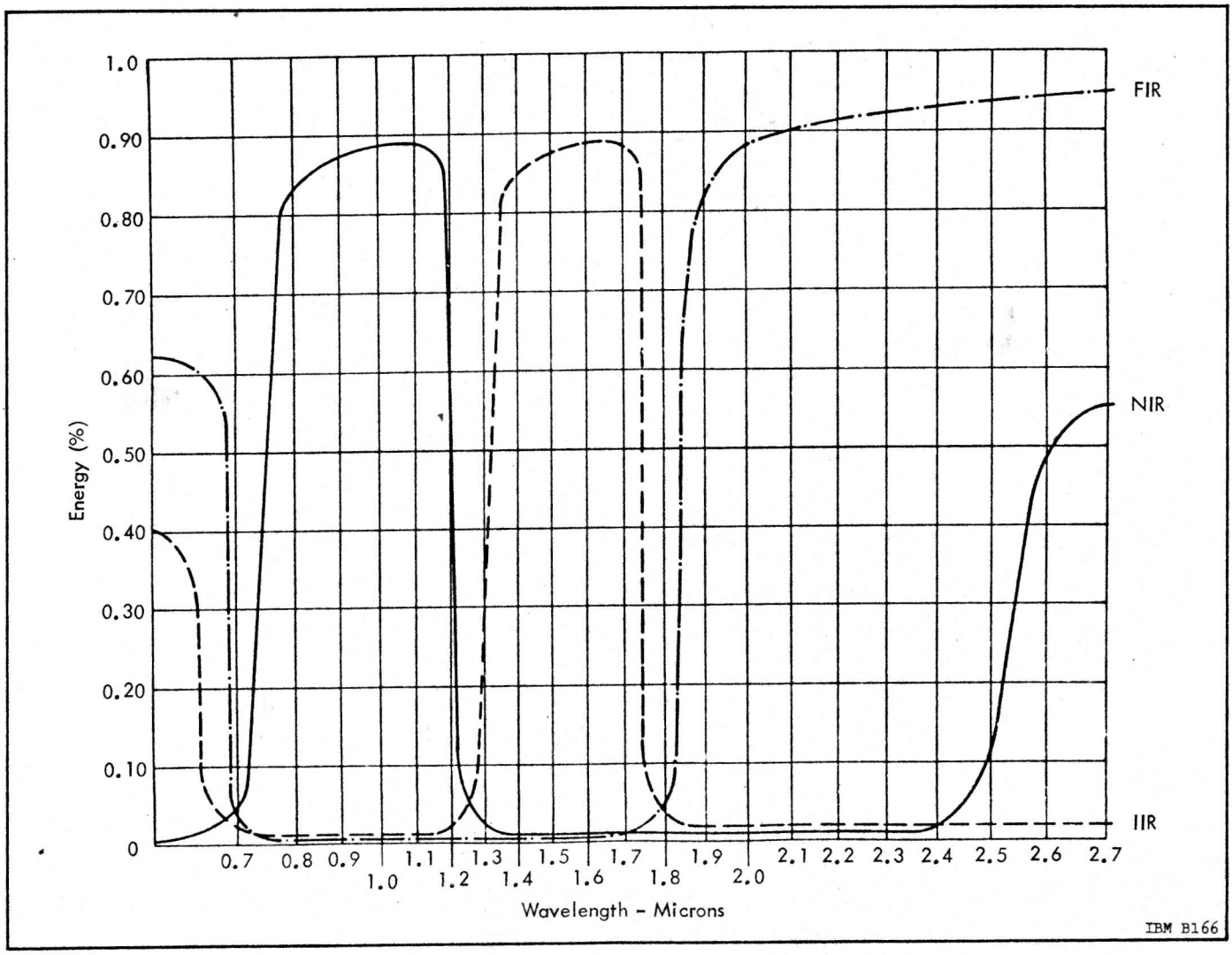


Figure 14.7-4 Optical Spectrum

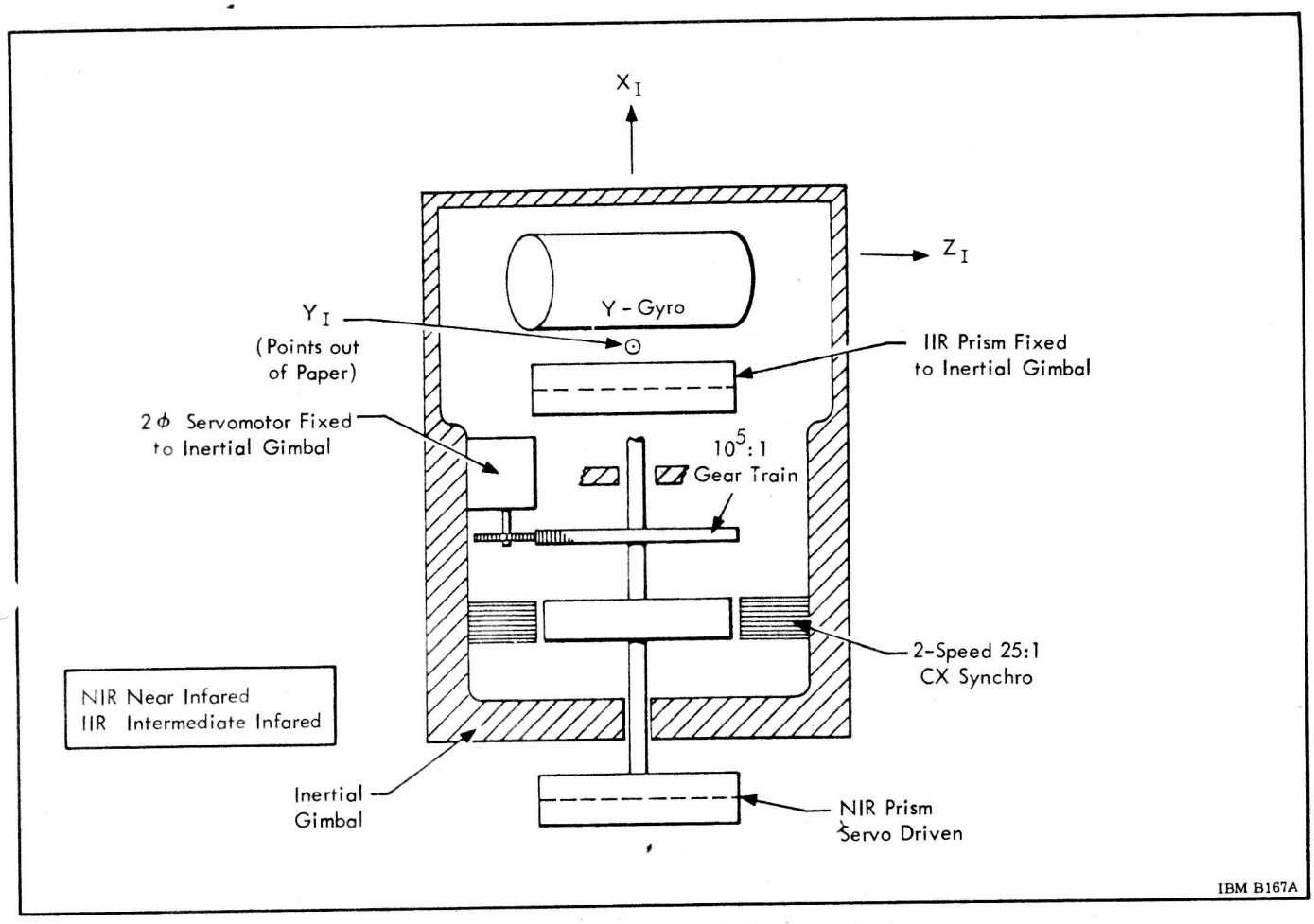


Figure 14.7-5 Optical Gimbal Laying System

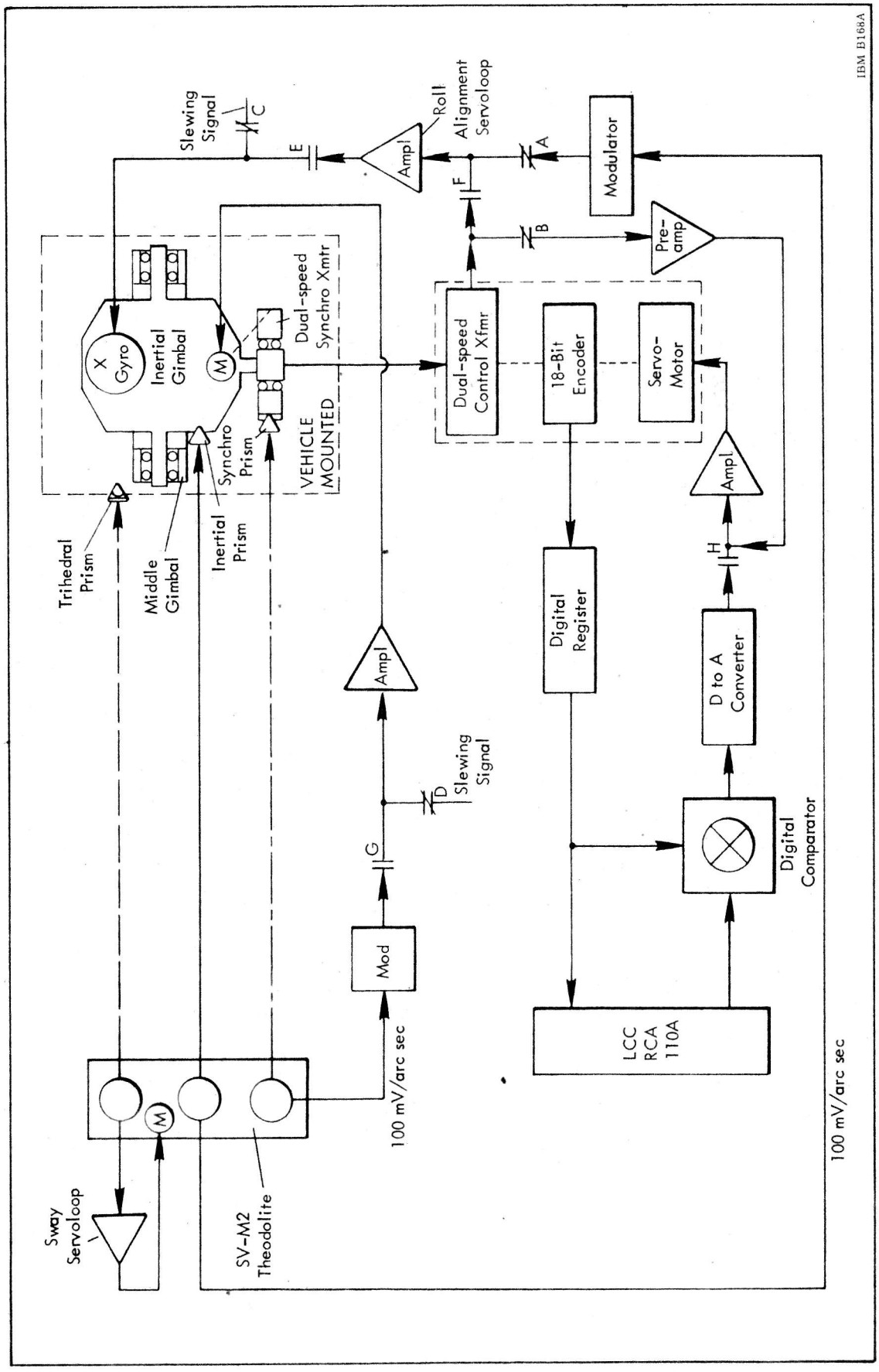


Figure 14.7-6. Azimuth Alightment Scheme

SECTION 14.8
GAS BEARING GYRO

The Platform contains three AB5-K8 gas bearing single-degree-of-freedom gyros. These components measure the vehicle motion; their performance capabilities define the hardware accuracies of the guidance system. No active compensation is used in the LVDC for instrument error terms and absolute tolerances are established for the life of the instruments.

The gas bearing gyro is shown in a cutaway view of Figure 14.8-1. The cylindrical, externally-pressurized gas bearing suspends the cylinder between the sleeve and endplates, as shown in Figure 14.8-2, and provides both axial and radial centering. The endplates are bolted to the sleeve and their assembly forms the case of the gyro.

Dry GN_2 is passed through two rows of 24 holes with millipore discs in the sleeve to act as flow diffusers and provide the bearing stiffness. The gas in the cylinder chamber generates the hydrostatic bearing and flows symmetrically to both endplates, escaping around the hub at each end of the cylinder. The sleeve, endplates, and cylinder are constructed of beryllium with machined tolerances of 5×10^{-4} millimeters (20 microinches) in roundness and in squareness.

The gyro wheel shown in Figure 14.8-2 mounts in a yoke of the cylinder endcap. The neck section of the yoke is controlled to minimize the anisoelastic drift of the wheel assembly. The endcap is mounted in the cylinder forming the gyro cylinder assembly. The cylinder is helium filled to reduce windage losses. The wheel is a two-pole, synchronous hysteresis motor. Precision bearings are fabricated to the beryllium shaft with the motor laminations and windings to form the stator of the wheel. The rotor is made up of an elkonite ring with P-6 hysteresis laminations shrink-fitted into the elkonite ring and beryllium endbells which are bolted to each side.

The signal generator and torque generator, shown in Figure 14.8-2, are coupled to the cylinder by means of a copper-shorted loop which is mounted on the cylinder. The signal generator is an ac-type, shorted-loop, single-winding sensor for the angular displacement of the gyro about its output axis. The torque generator operates like an eddy current motor. It provides only alignment torques for initial erection. The 3-phase, 400-hertz wheel power is transmitted by ribbon flex leads to standoffs on the gyro cylinder. A magnetic shield is placed between the gyro case and the signal generator. Dust covers, which are also magnetic shields, complete the assembly.

The electrical schematic for the AB5-K8 stabilizing gyro is shown in Figure 14.8-3. The coordinate definition for a single gyro is also shown. The wheel phase rotation A-B-C, American Standard, with the gyro connected to the 26-volt, 400-hertz supply, causes the gyro wheel to rotate in a negative direction about the gyro spin reference (X_{GU}) vector. *

Table 14.8-1 lists the gyro characteristics.

* The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 204 and 502 (and subsequent). For further details refer to Section 1.2.

Table 14.8-1 Gyro Characteristics

Gyro Wheel	
Type	Synchronous hysteresis
Angular momentum	2.0×10^6 g/cm^2/s
Wheel speed	24,000 rpm
Wheel excitation	26 V, 3-phase, 400 Hz
Wheel bearing preload	3.4 kg (7.5 pounds) operating
Wheel power at sync	10 W
Wheel life	3000 hours, minimum
Wheel mount	Symmetrical
Wheel sync time	90 seconds
Gas Bearing	
Gas pressure	10.3 N/cm^{2}d (15 psid)
Gas flow rate	2000 cc/min STP (122 in.^{3}/min)
Gas gap (one side)	0.015 to 0.02 cm (0.006 to 0.008 in.)
Orifice restrictors	Millipore discs
Sleeve material	Anodized beryllium
Endplate material	Anodized beryllium
Cylinder material	Anodized beryllium
Signal Generator	
Type	Short turn reluctance
Excitation	10 V, 4.8 kHz
Sensitivity	470 mV/° with 10 k load
Float freedom	$\pm 3^{\circ}{}^{+0^{\circ}}_{-0.5^{\circ}}$
Torquer (for platform erection and earth rate bias only)	
Type	Shorted turn reluctance
Normal erection rate	6°/min
Fixed coil excitation	26 V, 400 Hz, 45 mA
Maximum variable coil excitation	30 V, 400 Hz, 50 mA
Impedance	
Fixed coil resistance	184 Ω
Fixed coil impedance	555 Ω ∠+31° (400 Hz)
Variable coil resistance	190 Ω
Variable coil impedance	330 Ω ∠+53° (400 Hz)

Table 14.8-1 Gyro Characteristics (Cont'd)

Physical Characteristics	
Size	
Diameter	7.6 cm (3 inches)
Length	10.2 cm (4 inches)
Weight	900 grams (2 pounds)
Mounting	3-point flange mounting
Temperature Characteristics	
Calibration temperature	42.5 °C (108.5 °F) (gyro housing)
Drift versus temperature gradient	0.009°/hr/°C

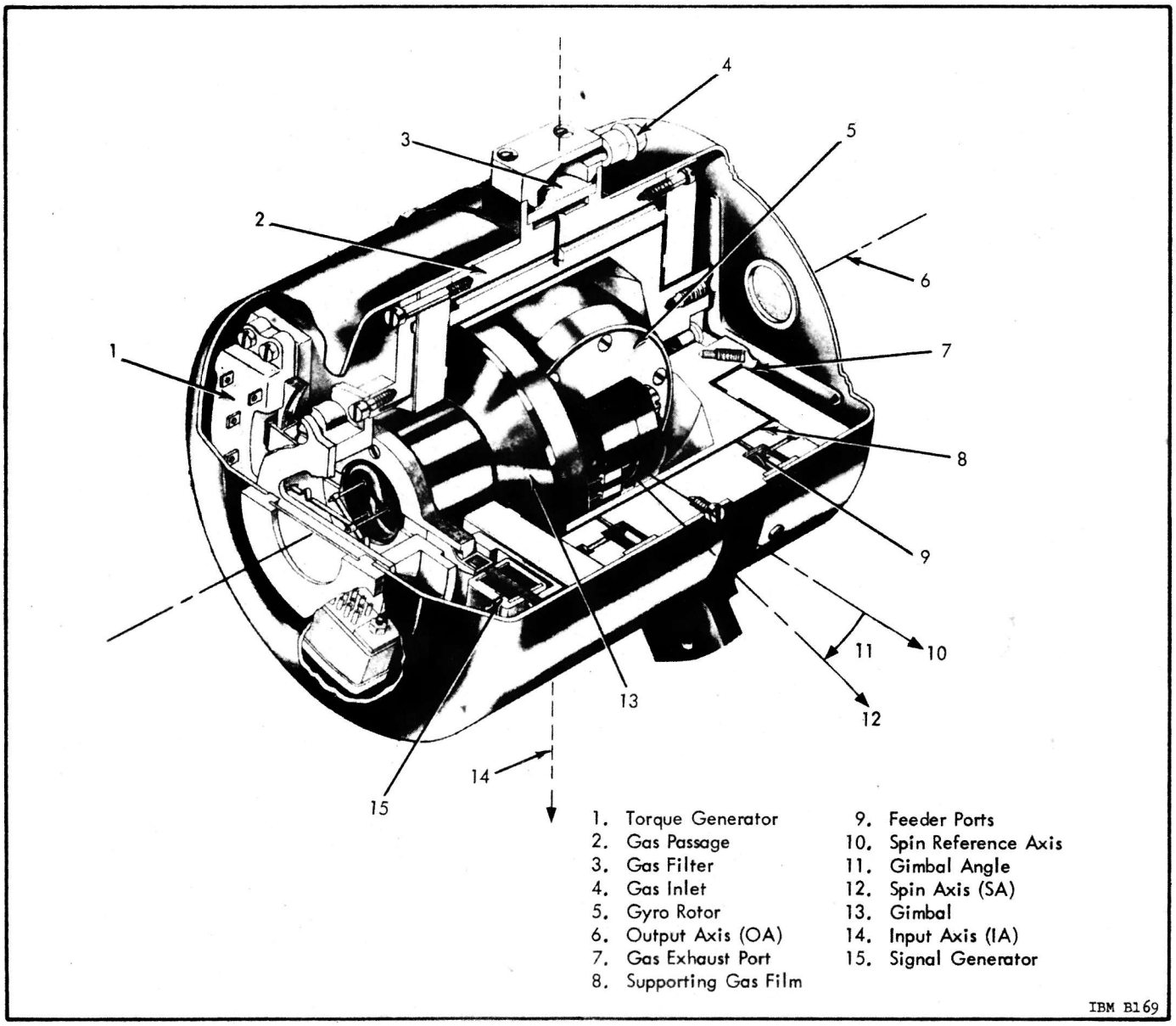


Figure 14.8-1. Cutaway View of a Single Axis-Integrating Gyro

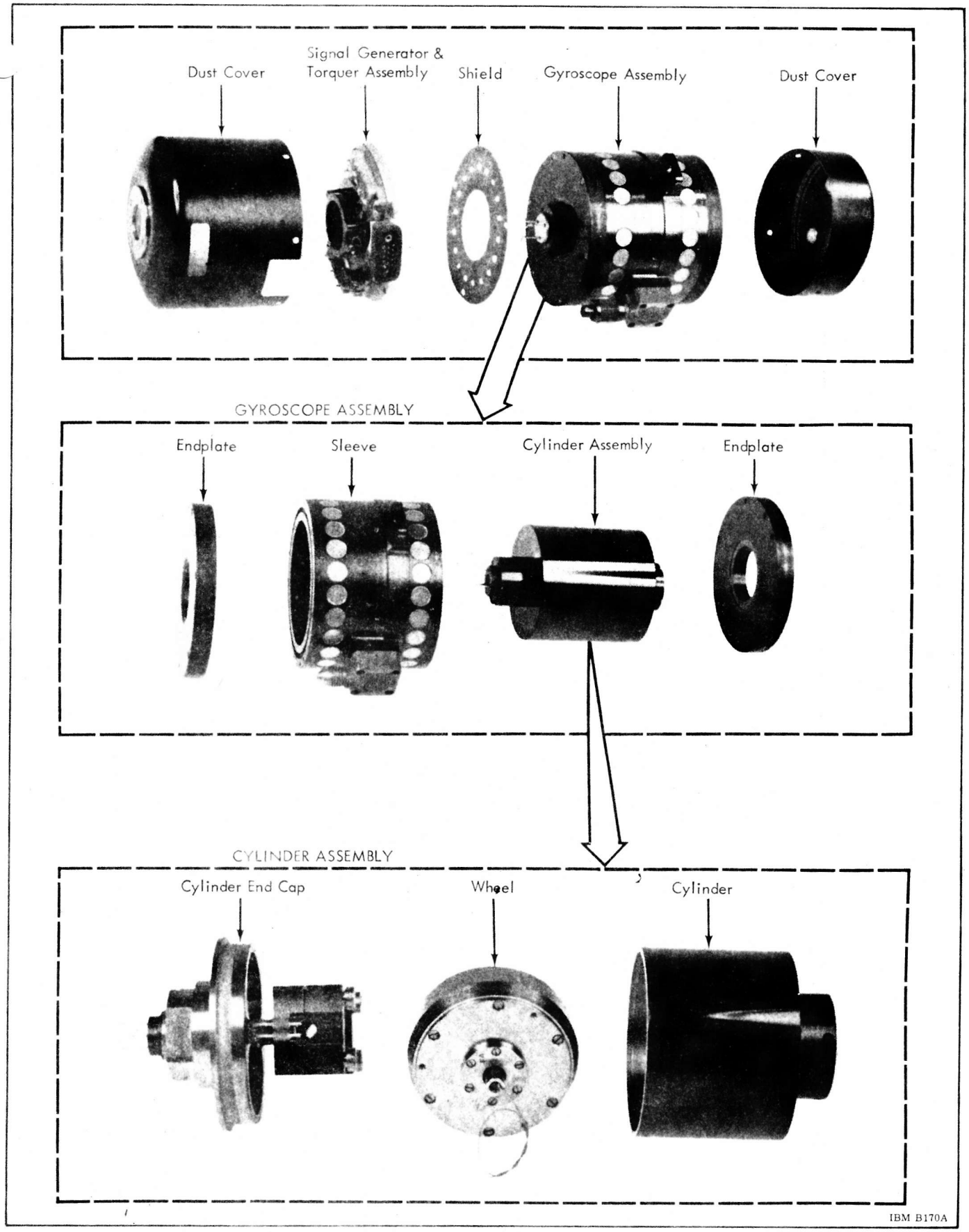


Figure 14.8-2 Exploded View of a Gas Bearing Gyro

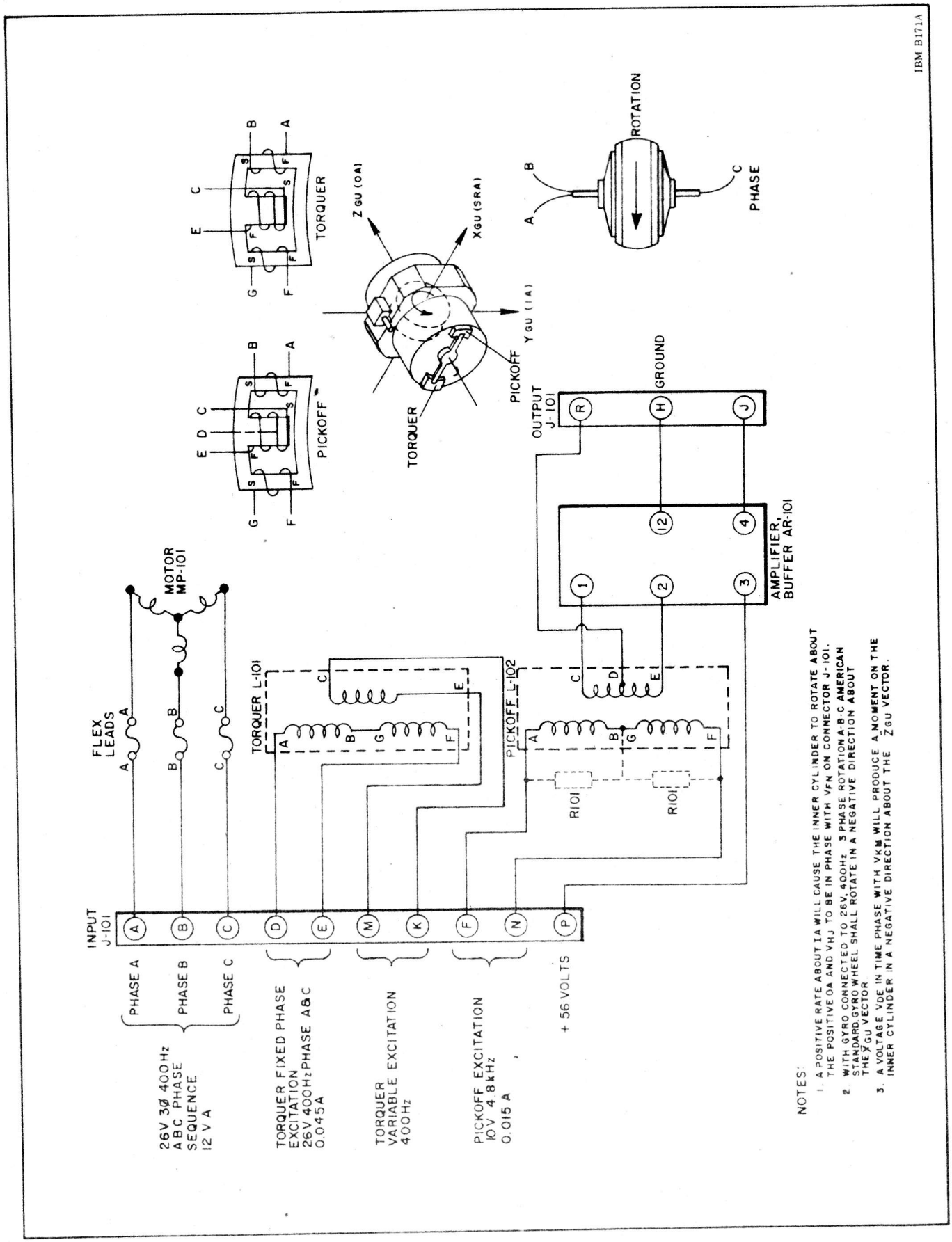


Figure 14.8-3. Stabilizing Gyroscope Electrical Schematic AB5-K8

SECTION 14.9

PENDULOUS GYRO ACCELEROMETER

The AB3-K8 instrument is a pendulous gyro accelerometer; a cutaway view and a schematic are shown in Figure 14.9-1 and Figure 14.9-2, respectively.

The accelerometer is a single degree-of-freedom gyro unbalanced about its output axis. The gyro motor and flywheel of the gyro accelerometer are shifted along the spin reference axis to obtain desired pendulosity about the gyro output axis. The pendulous cylinder is machined with a pair of pivots mounted into a frame with a set of Class-7 bearings. Thus, the cylinder is free to rotate about the gyro input axis, which is aligned in the acceleration-measuring direction. A torque is produced by the unbalance or pendulosity which is proportional to the acceleration to which the pendulous mass is subjected. A signal generator measures the precession angle of the gyro and a servo closes the loop to a direct-axis torquer which is mounted on the gyro input axis. Thus, the gyro measuring head is stabilized and the pendulous weight is held perpendicular to the input axis. The speed of the measuring head or gyro, with respect to inertial space, is proportional to thrust acceleration along the input axis, and the position of the measuring head is a measure of thrust velocity. An optical incremental encoder is mounted on the input axis and provides a measure of the thrust velocity. The power source for the synchronous spin motor is referenced from a crystal-controlled frequency, guaranteeing a constant accelerometer scale factor, or velocity increment/revolution, about the input axis.

The symmetrical gyro wheel is mounted in a cylinder that is suspended on a hydrostatic gas bearing. The gyro is constructed the same as the AB5-K8 gyro except there are two rows of 18 holes for feeding gas into the bearing. All nonmagnetic parts are machined from beryllium material except the endplates. which are fabricated of Monel to reduce the servoloop nutation frequency.

The electrical schematic for the AB3-K8 accelerometer is shown in Figure 14.9-3. The wheel phase rotation A-B-C, American Standard, with the gyro connected to a 26-volt, 400-hertz, 3-phase power supply, causes the wheel to rotate in a positive direction about the spin reference axis vector.

Table 14.9-1 lists the accelerometer characteristics.

Table 14.9-1 Accelerometer Characteristics

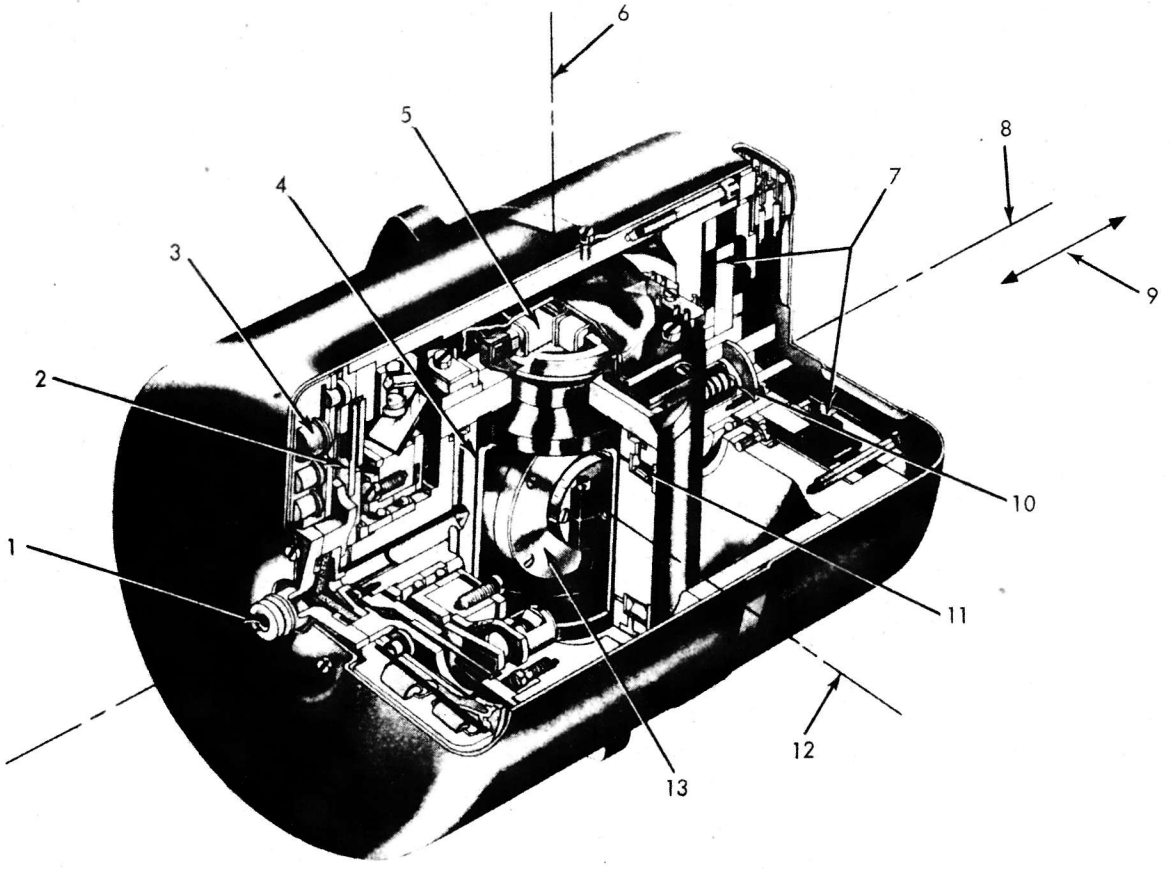
Gyro Wheel	
Type	Synchronous hysteresis
Angular momentum	94,000 g/cm^2/s nd (1290 lbf/in.^{2}/s)
Wheel speed	12,000 rpm
Wheel excitation	26 V, 3-phase, 400 Hz
Wheel sync time	90 s
Wheel power at sync	4.0 W
Wheel life	3000 hours, minimum
Wheel mount	Symmetrical
Wheel bearing preload	903 grams (1.99 pounds) operating

Table 14.9-1 Accelerometer Characteristics (Cont'd)

Gas Bearing	
Gas pressure	10.3 N/cm^2d (15 psid)
Gas flow rate	~1700 cc/min STP (~100 $in.^3$/min)
Gas gap	0.015 to 0.02 cm (0.006 to 0.008 in.)
Orifice restrictors	Millipore discs
Sleeve material	Anodized beryllium
Endplate material	Monel
Cylinder material	Anodized beryllium
Signal Generator	
Type	4-pole shorted turn reluctance
Excitation	10 V, 4.8 kHz
Sensitivity	280 mV/° with 700 Ω load
Float freedom	$\pm 6^{\circ}\ ^{+0^{\circ}}_{-0.5^{\circ}}$
Torque Motor	
Type	Direct-axis dc torquer
Maximum torque	1.44 kg cm at 1.1A and 44V
DC resistance	32.6 ohms
Inductance	12.5 millihenries
Velocity Pickoff	
Type	Digital encoder (optical grid)
Count	6000 count/revolution
Resolution	5 cm/s/bit (1.96 in./s/bit)
Output	Incremental with redundant channels
Physical Characteristics	
Size	
Diameter	8.3 cm (3.25 inches)
Length	12.8 cm (5 inches)
Weight	1200 g (2.64 pounds)
Mounting	3-point flange mounting

Table 14.9-1 Accelerometer Characteristics (Cont'd)

Performance	
Accelerometer scale factor	300 m/s/revolution of output axis (985 feet/s/revolution)
Pendulosity	20 g/cm
Temperature Characteristics	
Calibration temperature	42.5 °C ambient (108.5 °F) (on housing gyro)
Ambient temperature range for required accuracies	43 °C ± 3 °C (109 °F ± 5.4 °F)



1. Gas Inlet
2. Encoder Discs
3. Encoder Electronics
4. Supporting Gas Film
5. Servo Pickoff
6. Gyro Output Axis
7. Torquer
8. Gyro Input Axis
9. Accelerometer Measuring Direction
10. Slip Ring Capsule
11. Feeder Ports
12. Spin Reference Axis
13. Gyro Rotor

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Figure 14.9-1. Cutaway View of a Pendulous Integrating Gyro Accelerometer

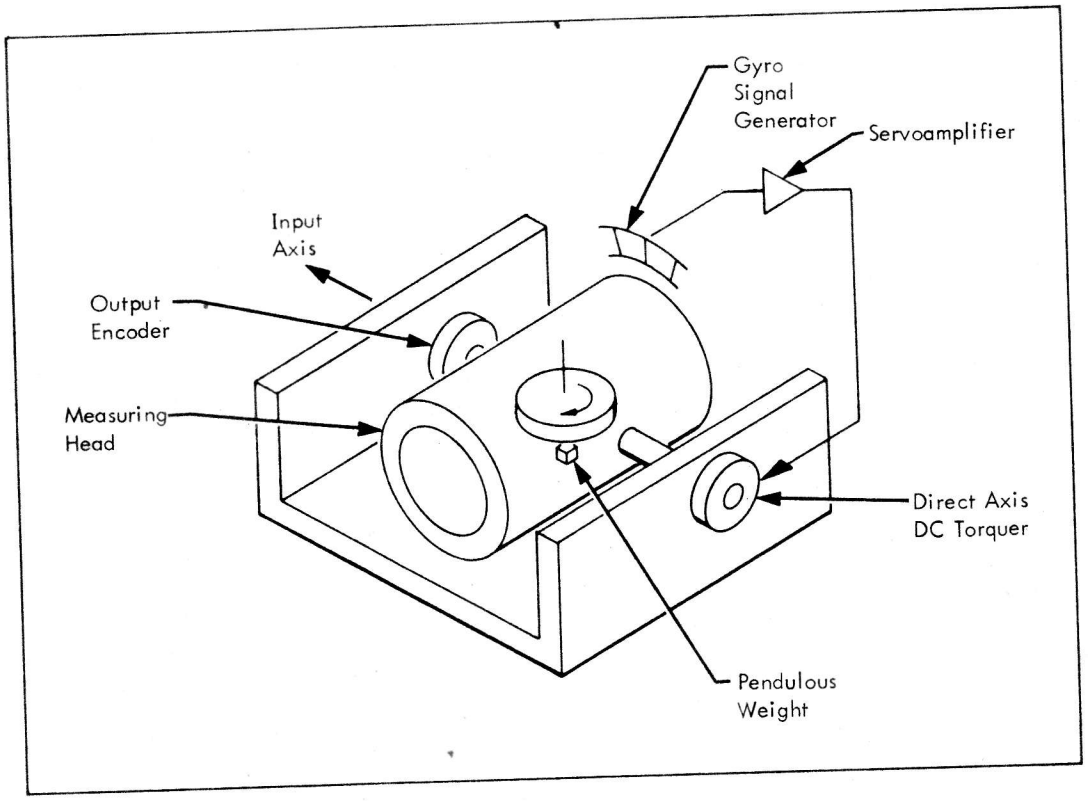
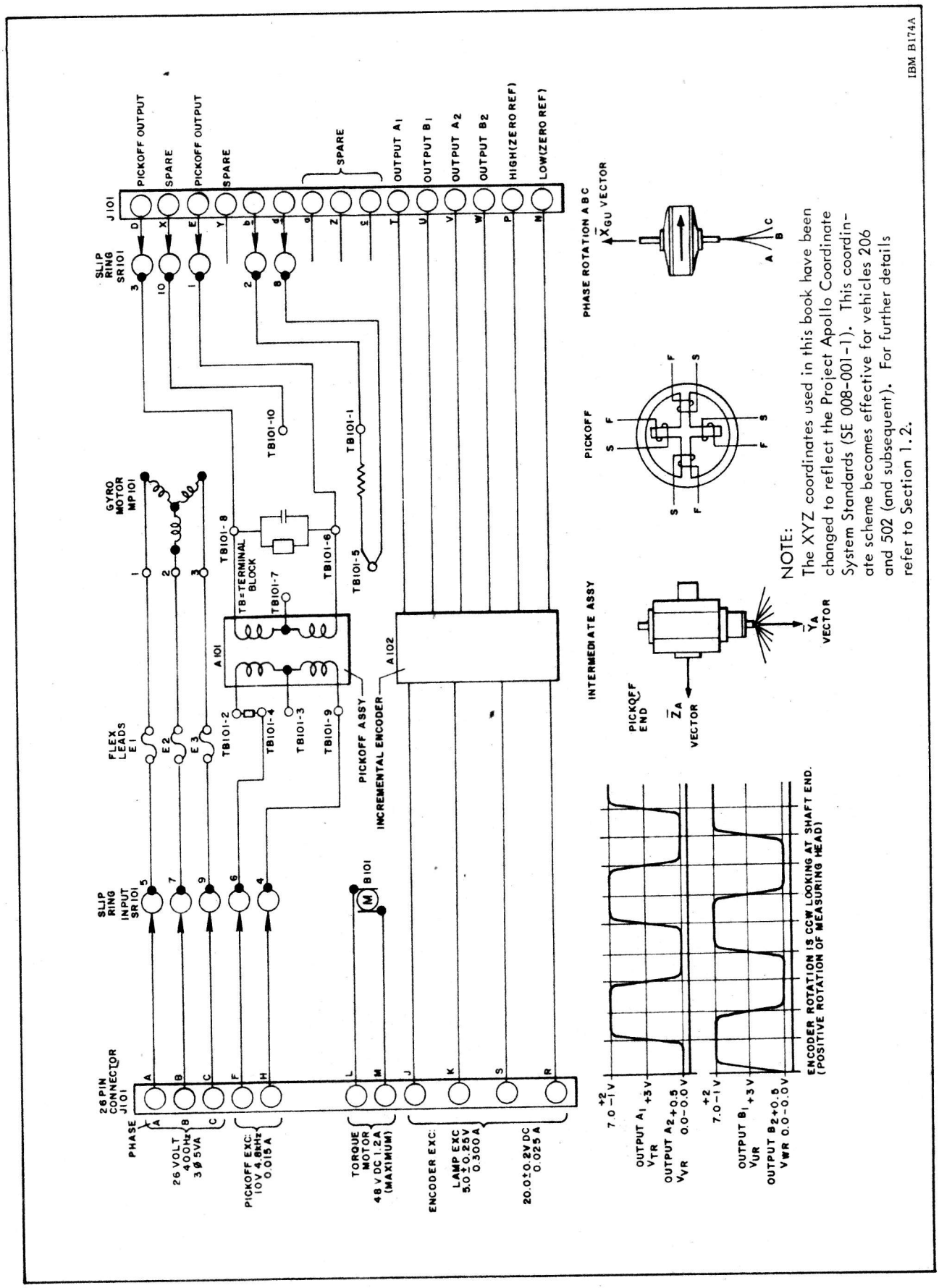


Figure 14.9-2. Pendulous Integrating Gyro Accelerometer Diagram



NOTE:
The XYZ coordinates used in this book have been changed to reflect the Project Apollo Coordinate System Standards (SE 008-001-1). This coordinate scheme becomes effective for vehicles 206 and 502 (and subsequent). For further details refer to Section 1.2.

Figure 14.9-3 Electrical Schematic of an AB3-K8 Acceleometer

SECTION 14.10
POWER AND GAS REQUIREMENTS

The input power requirements and the expected heat dissipation of the Platform system assemblies are shown in Figure 14.10-1. The input power figure shows the normal (quiescent) requirements and the peak (maximum disturbing forces and g loading) requirements.

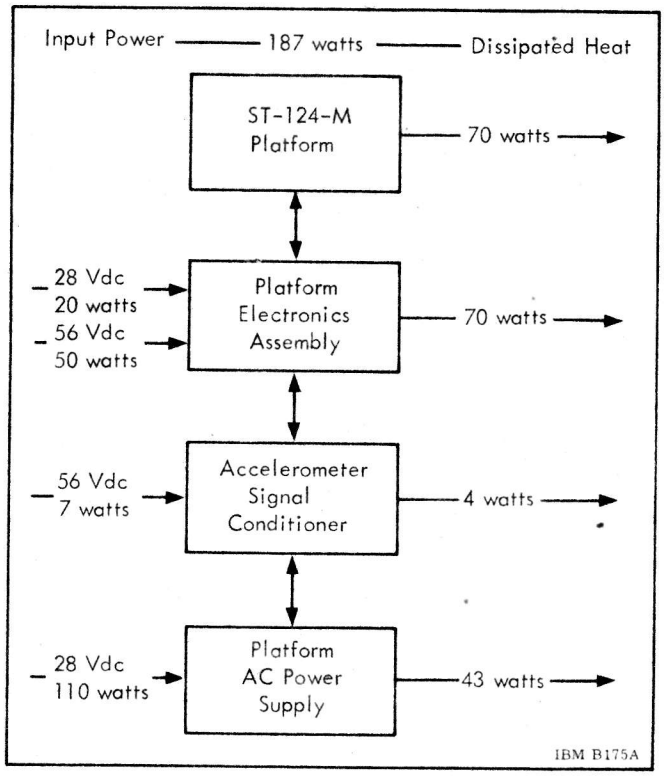


Figure 14.10-1 System Power Requirements and Heat Dissipation

The Platform has 250 watts of resistive heating with the application of 115 volts, 60 hertz, or 400 hertz. The resistive heaters are used to assist the Platform to reach its optimum operating temperature. Thermostats, located inside the Platform, control the heaters and turn them off at a prescribed temperature. The Platform component heat dissipation then raises the Platform to operating temperature. The heaters will also be available if inflight environment dictates the necessity for heating.

Inflight Platform temperature is controlled by circulating a constant-temperature fluid through ducts in the platform covers. The exterior of the Platform is painted with aluminum to provide an emissivity of approximately 0.4, thus providing a near-constant temperature radiating surface. Blowers will be utilized to circulate the internal GN_2 and maintain normal temperature gradients across the gimbals.

The GN_2 is supplied from a 0.056-cubic-meter (2-cubic-foot) storage reservoir, pressurized to 20.7×10^6 N/m^2 (3000 psi), and regulated to 10.3×10^4 N/m^{2}d (15 psid). Temperature conditioning of the GN_2 is performed by the IU methanol-water environmental control system. The Platform requires 1.4×10^{-3} cubic meters per minute (0.5 cubic foot per minute) of GN_2.

Table 14.10-1 lists the power supply specifications.

Table 14.10-1 Power Specifications

28 Vdc	
Voltage regulation	± 2.0 Vdc
Ripple content	0.5 V
Normal current	9 A
Peak current	11 A
56 Vdc	
Voltage regulation	± 2.5 V
Ripple content	0.25 V
Normal current	1.0 A
Peak current	6.0 A

CHAPTER 15
LVDA AND LVDC

SECTION 15.1

INTRODUCTION

The combination of the LVDA and the LVDC forms an electronic computer system. The LVDA is the input/output device of the LVDC. Any signal to or from the LVDC is routed through the LVDA. In addition, the LVDA serves as central equipment for interconnection and signal flow between the various systems in the Instrument Unit. The LVDA converts signals from digital to analog form and vice versa. The separation into LVDA and LVDC offers several advantages; the 2 assemblies, each having approximately half the size and weight of a combined unit, can be mounted more conveniently in the vehicle. Also, flexibility is gained since functional or operational changes in the Saturn Astrionics System will essentially affect the LVDA only and can be implemented without changing the LVDC.

The LVDA and the LVDC are involved in the following main operations:

Prelaunch checkout
Navigation and guidance computations
Vehicle sequencing
Orbital checkout

The interconnections between LVDA, LVDC, and other Astrionics equipment are indicated in Figure 15. 1-1.

The LVDC contains the logic circuits, the memory and the timing system required to perform arithmetic operations. The LVDA houses circuitry for temporary storage and conversion of data for communication with the LVDC and the power supplies for the LVDA and the LVDC.

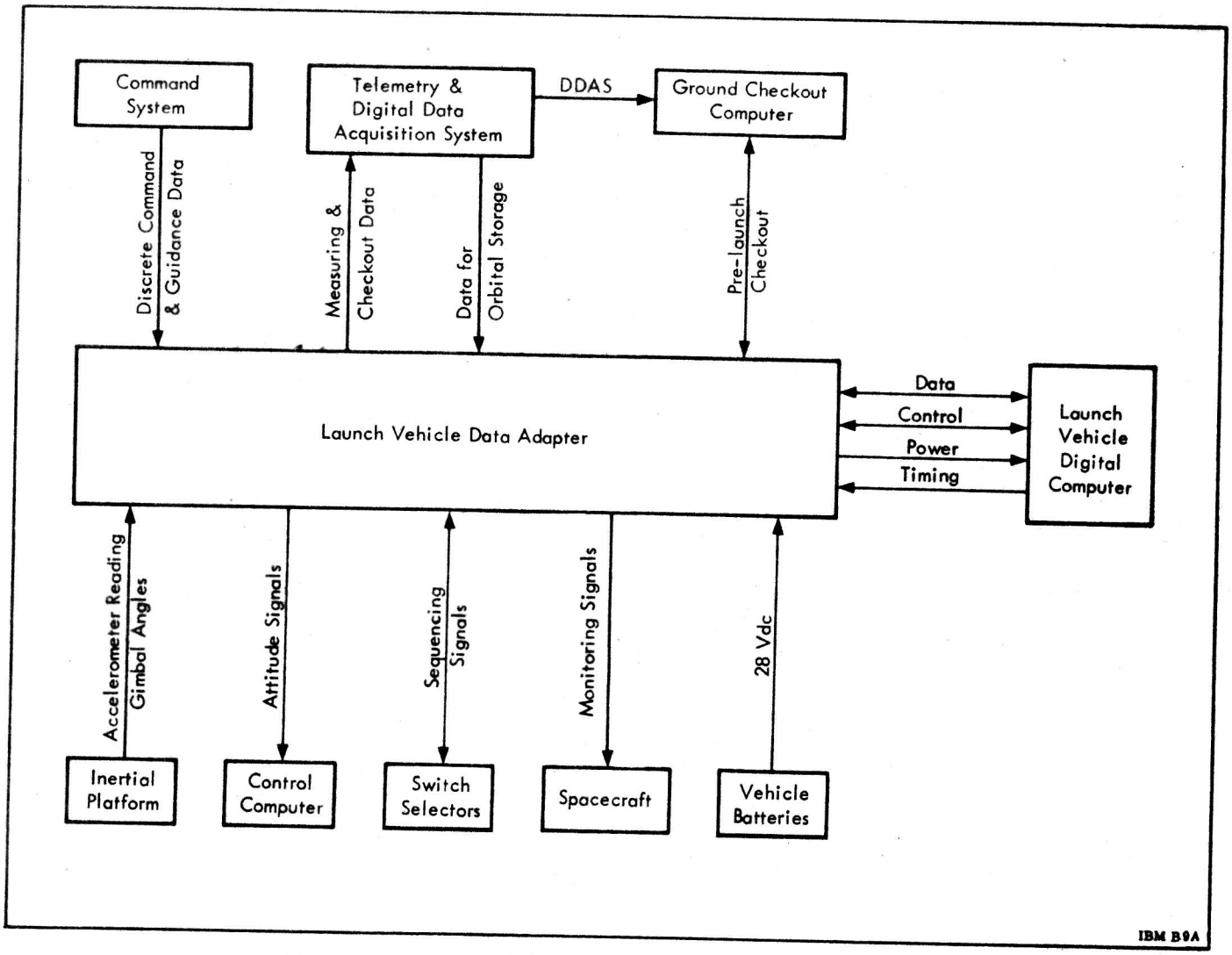


Figure 15.1-1 Connections Between LVDC, LVDA, and the Astrionics System

SECTION 15.2

PHYSICAL DESIGN

Microminiature packaging techniques are used as much as feasible in the LVDA and LVDC. Semiconductor chips are mounted on square ceramic wafers (side length 7.5 mm, ≈ 0.3 in.) on which interconnecting wiring and film resistors have been deposited by silk-screen printing and firing (Figure 15.2-1 . The devices, called unit logic devices, are attached to multilayer interconnection boards using solder reflow techniques by infrared heating. Each multilayer interconnection board has a capacity of 35 unit logic devices. Two multilayer interconnection boards are bonded back-to-back to a supporting metal frame to form a logic page assembly (Figure 15.2-2). Multilayer interconnection boards and pages are joined by connectors to a central multilayer printed circuit board.

For applications requiring extreme accuracy or large drive current capability, circuit modules composed of conventional discrete components are utilized. These find greatest application in the LVDA, but are also used in the LVDC as memory drivers. The circuit modules are mounted on the interconnection boards previously mentioned. In volume, one circuit module page is equivalent to three unit logic device pages.

The magnesium-lithium frames of the LVDC and the LVDA are cooled by circulating a liquid coolant through channels in the frame to remove heat generated by the electronic components. This cooling provides a low operating temperature for the electronic components and results in a high reliability for the devices. The coolant is provided by the IU environmental control system.

An exploded view of the LVDA is shown in Figure 15.2-3. Figure 15.2-4 shows an exploded view of the LVDC.

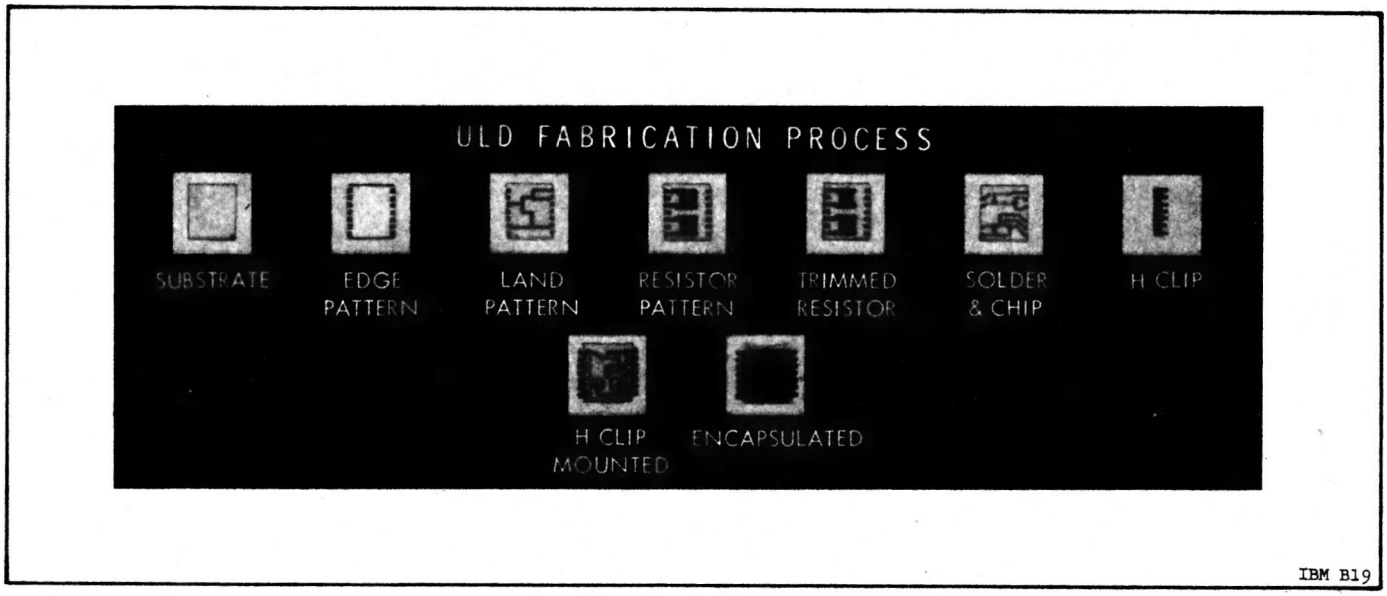


Figure 15.2-1 Unit Logic Device Buildup

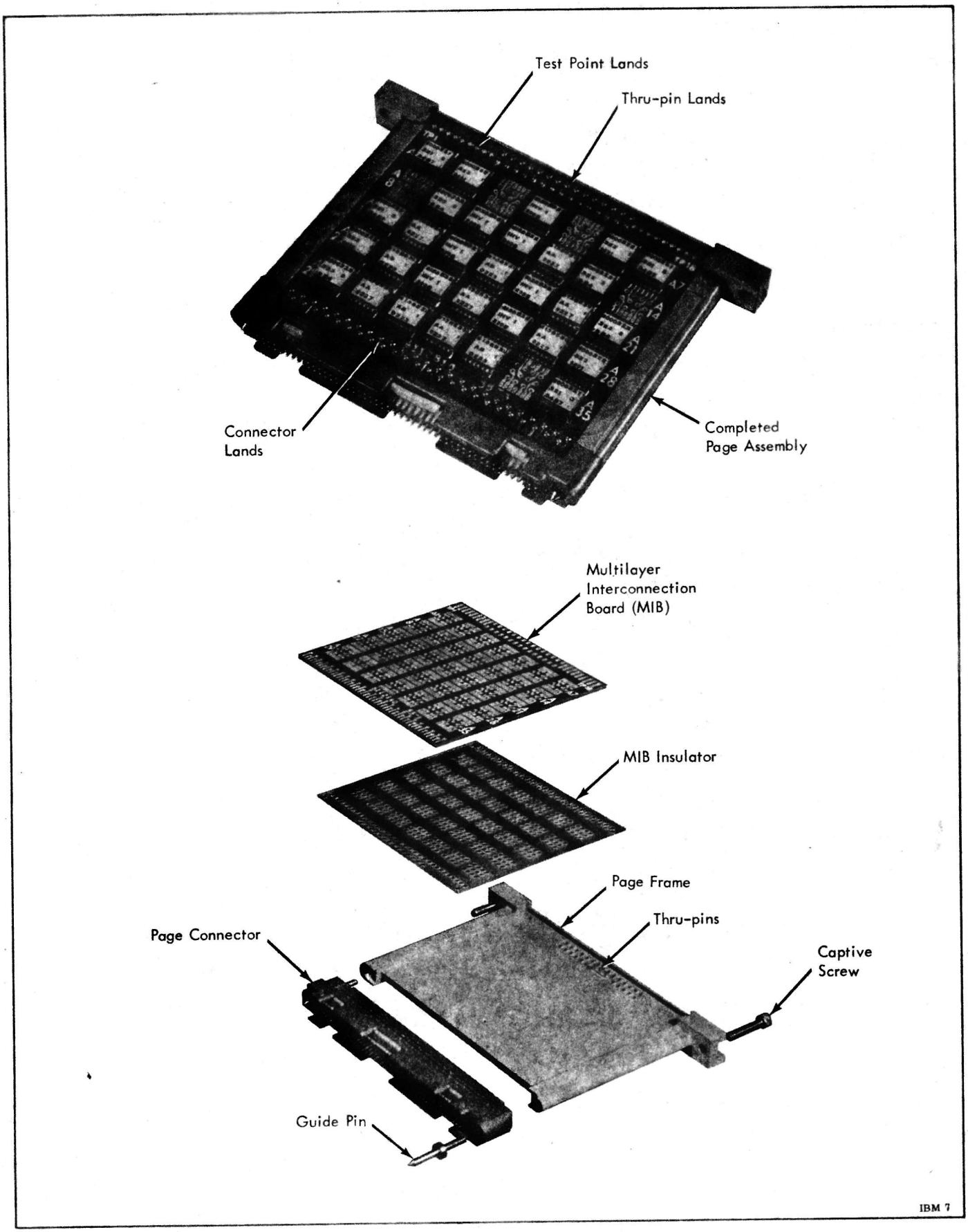


Figure 15.2-2. LVDC Logic Page Assembly

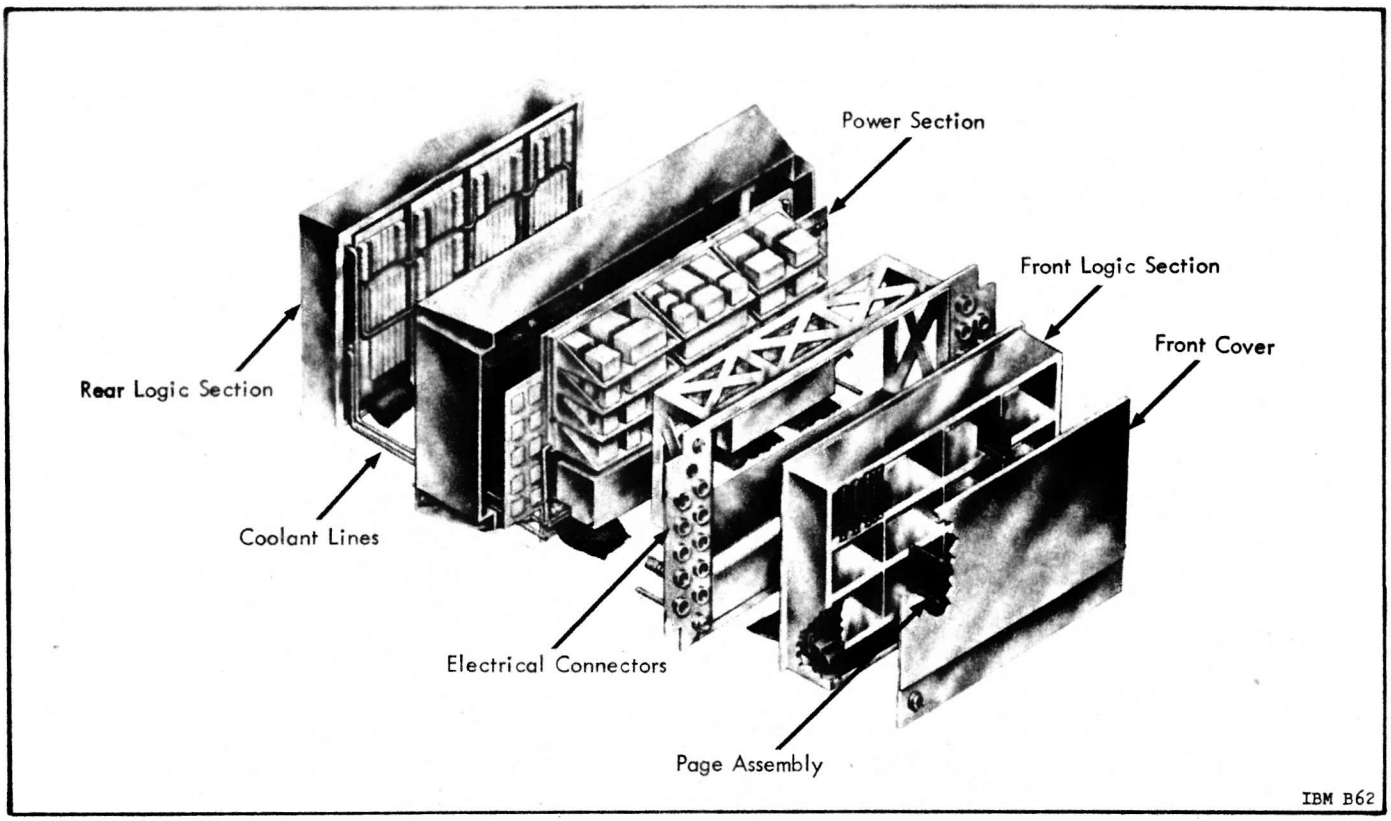


Figure 15.2-3 Exploded View of the Launch Vehicle Data Adapter

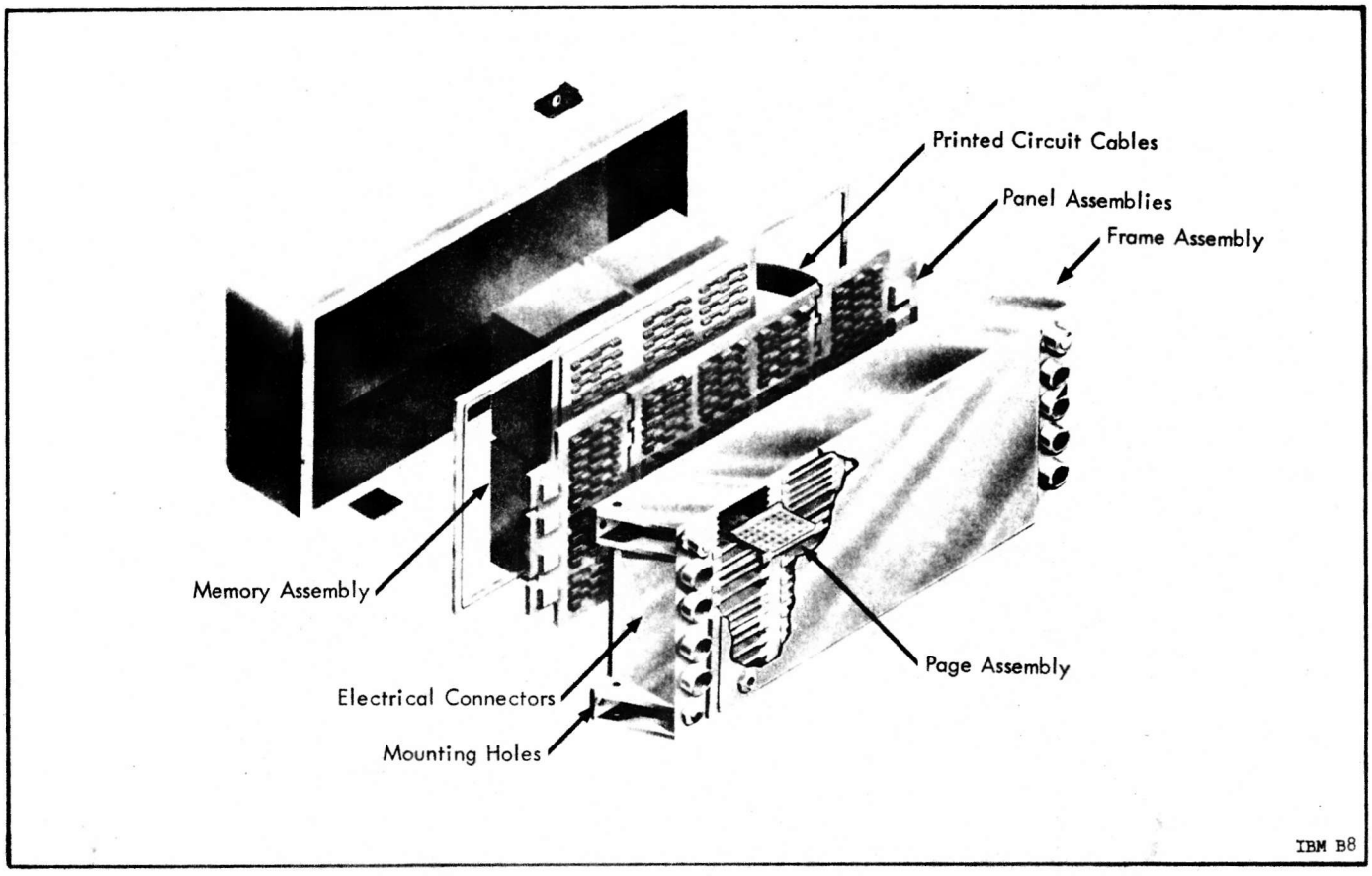


Figure 15.2-4 Exploded View of the Launch Vehicle Digital Computer

SECTION 15.3

RELIABILITY

Reliability of the LVDC is predicated on the use of triple modular redundancy in the central computer. The LVDC is divided into 7 modules (Refer to Table 15.3-1) which are triplicated. Calculations and simulation based on Monte Carlo techniques indicate a reliability of 0.996 for 250 hours (0.999966 for a 6-hour mission) for the computer logic and memory using triple modular redundant and duplex techniques, respectively. This is compatible with the minimum design objective of a reliability of 0.98 for a 250-hour mission for the combination of the LVDC and LVDA. For comparison, the equivalent simplex logic has a reliability figure of 0.955 for 250 hours. Theoretically, the reliability of a duplex module exceeds that of triple redundant modules by a factor $\frac{2R - R^2}{3R^2 - 2R^3}$, but the difference is of a second order effect for values of R close to "one" and therefore negligible. Duplex redundancy, however, has limited application because of the problem of determining which one of the two units failed.

The triple modular redundant logic system of the LVDC uses three identical simplex logic channels (Figure 15.3-1) and subdivides each channel into seven functional modules. The outputs from corresponding modules are voted upon in voter circuits before the signal is sent to the next modules. Figure 15.3-2 shows typical modules and voters. The output of the voter circuit is equal to the majority of the inputs to the circuit. Thus, even if one of the three inputs is incorrect, the output to the next module will be correct.

Table 15.3-1 TMR Computer Module Breakdown

Module Number	Module Name or Description
1	Computer Timing
2	Transfer Register
3	Arithmetic Unit
4	Multiply and Divide
5	Operation Code
6	Memory Address Register and Decoder
7	Memory Timing and Parity Check

An average of 13 output signals from each module are voted on. The voter circuit outputs may go to any of the other subdivided modules of the LVDC. This allows correct computations to be obtained, even with several malfunctions in the LVDC, provided two identical modules of a triple redundant set are not in error.

This method provides greater reliability than using three independent computers. If the outputs from three independent computers were compared, any malfunction in two of the computers would cause the computation to be in error.

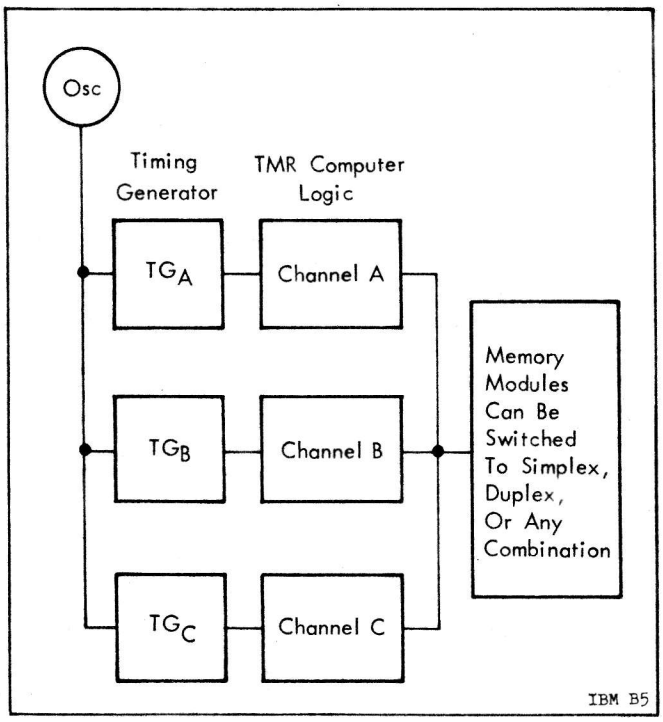


Figure 15.3-1 Computer Redundancy Configuration

Disagreement detectors are used on module outputs as shown in Figure 15. 3-2 to indicate a failure in the system. Approximately 13 disagreement detectors are logically combined and fed to a register in the LVDA. These signals are then fed to the telemetry buffer register for monitoring either before launch or in flight.

The memory system has two individual memories which can be used in parallel (duplex) for increased reliability or completely independent (simplex) for increased capacity. In the duplex mode, information is read out of both memories from corresponding cores and by means of a selection network, just one memory output will be used. If the selected memory should contain an error (parity or timing), the information from the other memory would be used with the correct information being readback into both memories. Thus, the computer can correct memory errors.

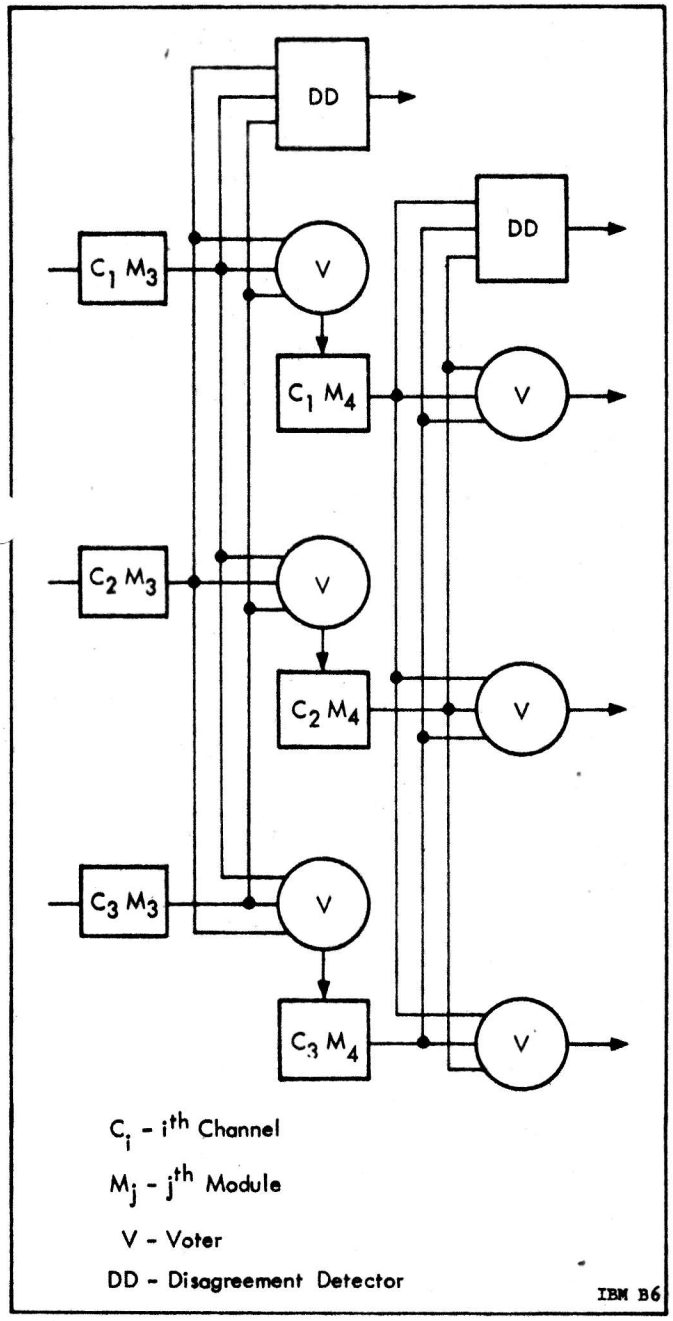


Figure 15. 3-2 Triple Modular Redundancy (TMR)

SECTION 15.4

DESCRIPTION OF THE LAUNCH VEHICLE DIGITAL COMPUTER

15.4.1 GENERAL CHARACTERISTICS

The Launch Vehicle Digital Computer is a general purpose computer which, under control of a stored program, processes data using fixed-point, two's complement arithmetic. Data is processed serially in two arithmetic sections which can, if desired, operate concurrently. Addition, subtraction, and logical extractions are performed in one arithmetic section while multiplication and division are performed in the other.

The principal storage device is a random access, ferrite-core memory with separate controls for data and instruction addressing. The memory can be operated in either a simplex or duplex mode. In duplex operation, memory modules are operated in pairs with the same data being stored in each module. Readout errors in one module are corrected by using data from its mate to restore the defective location. In simplex operation, each module contains different data which doubles the capacity of the memory. However, simplex operation decreases the reliability of the LVDC since the ability to correct readout errors is sacrificed. The memory operating mode is program controlled. Temporary storage is provided by static registers composed of latches and by shift registers composed of delay lines and latches.

LVDC ELEMENTS

The LVDC is composed of the following eight functional elements:

Timing	Program Control
Memory	Arithmetic
Memory Control	Multiply-Divide
Data Control	Voting

Figure 15.4-1 is a block diagram of the LVDC showing the major parts of each functional element (except the voting element) and how they are interconnected. The heavy lines on the diagram show major paths of information flow.

Timing Element. The timing element develops 3 levels of standard timing signals which synchronize and control logic operations in the remaining 7 elements. Direct outputs of the timing element are used in every functional element, except the memory element which generates its own timing signals.

Memory Element. The memory element and the memory control element operate together to store the programmed instructions and the constants and data required by the program. The memory element is composed of up to eight memory module assemblies, each of which contains a ferrite-core array and all the circuits necessary to transfer data to and from the module. The memory control element determines when a transfer will occur and selects both the direction of transfer and the memory location to be exercised. Buffer storage for data enroute between the memory and the central computer is also located in the memory control element.

In addition to controlling data transfers, the memory control element determines the mode (simplex or duplex) in which the memory will operate. In duplex operation, the memory modules are divided into 2 groups, effectively forming two separate memories with identical contents. The even numbered modules make up the "A" memory and the odd numbered modules make up the "B" memory. Each module in the "A" memory is paired with a module in the "B" memory which contains the same information. The memory control element selects both modules of a pair and provides separate buffer storage for each

memory. The 2 memories are operated simultaneously, but the LVDC uses information from only 1 memory. The memory select and error monitor circuit determines which memory will be used and changes the selection when an error is detected in the active memory. The memory select and error monitor circuit continuously samples the drive currents in each memory and checks the parity of each word transferred out of both memories. In simplex operation, each module contains different information, and only one module is selected at a time. The memory select and error monitor circuit then makes the memory selection follow the selected module so that the "B" memory is active when an odd numbered module is selected and the "A" memory is active when an even numbered module is selected. The ability to correct errors is sacrificed in simplex operations.

Data and constants are stored in the memory in 2 segments called syllables. Thus, the memory is described as being divided into syllables. One syllable of data is transferred to or from the memory at a time; consequently, two memory cycles are necessary to transfer a complete data word. Instructions are only half the length of data words and are stored one per syllable. The syllable selection for instructions is stored in the syllable select circuit of the memory control element. Timing signals determine whether the stored selection will be used or the selection will be sequenced to read both syllables of a data word.

When a memory operation is required, the memory control element provides a sync impulse to the memory element. Memory mode and module select circuits direct the impulse to two memory modules for duplex operation or one module for simplex. Once impulsed, each memory module generates all the timing signals and drive currents required to complete its cycle.

The memory clock drivers produce either read or store timing pulses, depending on a control signal from the memory timing and sync select circuits. The memory address decoders reduce the address of the desired memory location to selection signals for the X and Y memory address drivers of that location in each syllable of the memory.

The syllable select circuit determines which syllable will be used. Syllable and address selection signals are applied to all the modules in the memory. However, only the module (or modules for duplex) which receives a sync impulse will generate the memory clocks which cause the module to cycle. When the memory clocks occur, data is transferred in parallel between the memory buffer registers A and B and the selected memory location. All data entering or leaving the memory passes through the memory buffer registers enroute to or from the data control element.

Data Control Element. Data words and constants enter the transfer register from the memory in 2 syllables. Each syllable enters the transfer register in parallel and is then serialized and distributed to the arithmetic element, the multiply-divide element, or the LVDA. Some special constants are also distributed to the program control and memory control elements in serial form.

Data words which are bound for the memory enter the transfer register in serial form. The transfer register then divides them into syllables and forwards each syllable to the memory buffer registers in parallel. At the memory buffer registers, a parity bit is added to each syllable before it is stored in the memory. The parity counter monitors the number of "1's" entering the transfer register and assigns odd parity to the memory buffer registers by controlling the parity bit. Odd parity means that the total number of "1's" in a syllable is odd.

Another item which enters the transfer register serially is the contents of the instruction counter. The instruction counter controls the normal sequencing of the program through the memory. Just before a new instruction is required, the contents of the instruction counter are shifted into the transfer register and transferred in parallel to the address register in the program control element. The address register then selects the memory location of the new instruction.

When the new instruction is read, it is transferred from the memory buffer registers into the transfer register. The instruction is then separated into an operation code and an operand address; the 2 parts are transferred in parallel to the program control element. The operation code is loaded into the operation code register and the operand address into the address register. The operand address of some instructions constitutes a special constant which, in addition to the parallel transfer, is shifted out of the transfer register in serial form.

Program Control Element. The program control element stores and decodes the programmed instructions and in addition, controls sequencing the

program through the memory. The operation code register and the address register store their respective parts of the instructions. Outputs of the operation code register, and those of the operation decoders, control the arithmetic and multiply-divide elements, the data and memory control elements, and parts of the program control element to perform the commanded operations.

The address register selects the memory location of the data to be used in the commanded operation. When the operation is complete, the address register is reloaded with the contents of the instruction counter to address the next instruction. The address register is augmented by the data module register and the instruction module register (located in the memory control element) and by the data sector register and the instruction sector register in the program control element.

The module and sector registers preselect an area of the memory within which the program must operate. As implied by the names of the registers, 2 selections are made, one for data and one for instructions (the same area may be selected for both).

The address register then selects individual locations within the preselected areas from which data and instructions will be read. Timing signals discriminate between instruction and data addressing. The contents of the module and sector registers are changed upon command of the program.

It was noted previously that the program control element controls sequencing the program through the memory. Actually, the program controls its own sequencing through the use of instructions which command the program control element to change the contents of the module and sector registers (discussed in the preceding paragraph) and the instruction counter.

The instruction counter stores the address of the next instruction to be operated. Each time the LVDC performs an instruction, the instruction address is incremented by one to develop the address of the following instruction. In this manner, the program steps sequentially through the area of memory selected by the instruction module register and the instruction sector register.

The sequential stepping continues until the program issues an instruction to alter the sequence or select a different area of the memory to read instructions from. Area selection is changed by shifting a "HOP constant" out of the transfer register which reloads the instruction counter to select the starting location of the next instruction sequence. The instruction counter then begins stepping sequentially through the newly selected memory area beginning at the specified starting point.

The instruction counter can also be reloaded without affecting the module and sector registers. This feature permits repeating short program loops and enables the LVDC to make logical choices. When commanded, the LVDC can examine the contents of the accumulator register for certain conditions and alter the program sequence if the condition exists. If the condition is not met, sequential stepping continues.

The program control element also contains two other circuits which can alter the normal program sequencing, the start-stop control and the interrupt control circuits. The start-stop control circuit provides the means to externally control starting and stopping the LVDC and to single-step through its program one instruction at a time. Application of a HALTV signal results in clearing certain registers to an initial condition and directs the LVDC to the first instruction of its program. During power application, the HALTV signal remains ON until power is fully applied to prevent spurious instructions from being operated. A CSTN signal is manipulated by the test equipment to step through the program one instruction at a time, on command.

The interrupt control circuit enables external equipment to break off normal sequencing of the program and direct it to process data of a higher priority. The interrupt control circuit allows the instruction in progress at the moment of the interruption to finish, then forces execution of a command to reload the instruction counter and the module and sector registers.

The first few instructions of the new program sequence store the contents of the important registers in order to preserve the conditions existing in the LVDC at the moment of interruption. Once the priority data has been processed, the LVDC can restore these conditions and resume operation where it left off. The very first item to be stored must be a HOP constant defining the location at which the interrupt occurred. This constant is produced by the HOP constant serializer and is used to redirect the program to the point of interruption.

Arithmetic and Multiply-Divide Elements. The arithmetic and multiply-divide elements encompass the machine's total computing ability. The arithmetic element performs addition, subtraction, shifts, and logical extractions. The multiply-divide element

failure occurred during the read operation, the memory select and error monitor circuit provides an error indication to the LVDA. Upon sensing an error, the memory select and error monitor circuit also places both sets of inhibit drivers under control of the memory buffer register containing correct information, and if the error is in the selected memory, changes the memory selection. The instruction is then transferred from the selected memory buffer register to the transfer register.

Reading a ferrite-core memory destroys the information in the memory. Consequently, a read operation must always be followed by a store (or restore) operation to preserve the contents of the memory. The restore operation is accomplished after the instruction has been transferred to the transfer register. The memory timing and sync select circuit changes the conditioning level to the memory clock drivers so that they produce store timing pulses, then delivers a second sync impulse to the memory mode and module select circuit. There have been no changes in address or memory module selection, therefore the same memory location is exercised again. However, on this memory cycle, data is transferred from the memory buffer registers to the memory through the inhibit drivers.

Almost immediately upon entering the transfer register, the instruction is separated into an operation code and an operand address. The operation code defines what operation will be performed, and the operand address gives the location in memory of the data to be used in the operation. The operation code is transferred in parallel to the operation code register and the operand address to the address register. The remainder of the operation is dependent upon the code transferred to the operation code register. The code can specify any of three general types of operations: (1) those which require data from memory, (2) those which place data into the memory, and (3) those which do not use the memory.

Assume first that the operation code requires data to be read from the memory. The syllable select circuit selects syllable zero, the first syllable of the data word. The memory timing and sync select circuit conditions the memory address decoders to combine and decode the contents of the address register and the data sector register; it then initiates a read cycle in the memory which transfers the first half of the data word to the memory buffer registers. While in the memory buffer registers, the half-data word is parity checked, then transferred to the transfer register and restored in the memory. The transfer register serializes the data by shifting it to the TRS output latch. The TRS output makes the data available to the arithmetic and multiply-divide elements, the program and memory control elements, and the LVDA. Outputs from the operation code register and the operation decoders determine which element will accept it and how it will be used.

As the first half of the data word nears the end of the transfer register, the syllable select circuit selects syllable 1 and the memory timing and sync select circuit initiates another read cycle in the memory. This read cycle transfers the second half of the data word into the memory buffer registers where it is parity checked. Then, just in time to fall in behind the last bit of the first half of the data word, the second half of the data word is transferred into the transfer register. The transfer register continues shifting and the two halves of the data word appear as a continuous serial output on the TRS line.

To obtain the result of a multiply or divide operation, the operand address specifies the product-quotient register. When the product-quotient register is addressed, the memory is inhibited and the product or quotient is shifted directly into the accumulator register without passing through the transfer register.

When providing a data output, the transfer register is synchronized with the accumulator register. Thus, the output of the transfer register and the contents of the accumulator register can be combined bit-for-bit in the add-subtract logic. The results of these operations are placed in the accumulator register for recirculation. As the last bit of the accumulator contents emerges from the accumulator register, timing signals end the arithmetic processes in the add-subtract logic and the contents of the instruction counter begin to emerge from the accumulator register. The add-subtract logic increments the instruction count by one and reinserts it in the accumulator register immediately behind the result of the arithmetic operation. Simultaneously, the instruction count is shifted into the transfer register to address the next instruction.

When the operation code specifies that data is to be transferred into the memory, the basic operations are reversed. Instead of transferring 2 syllables of data to the transfer register which serializes them into a continuous unit, a continuous unit of serial data is shifted into the transfer register which divides it into syllables. The syllables are then transferred to the memory in parallel. Shortly after the instruction is loaded into the operation code and ad-

performs the iterative processes of multiplication and division. The 2 elements are independent and can, if desired, be operated concurrently.

Once a multiply or divide operation has been started, it runs automatically to completion and the next few instructions of the program are operated during its progress. During this time the arithmetic element is available for concurrent use. There is, however, a program option for multiplication which stops the program until the product of the multiplication is available. When using this option the product is placed in both the product-quotient register and in the accumulator register.

The accumulator register in the arithmetic element provides one of the operands for all the arithmetic instructions and the memory provides the other. For multiplication and division, the accumulator contents and the operand from memory are simply transferred into shift registers in the multiply-divide element for temporary storage during the iterative process. The remaining arithmetic operations combine the 2 operands in the add-subtract logic and place the result in the accumulator register. The result can then be sensed to control logical decisions or it can be transferred to the memory, the multiply-divide element, or the LVDA. The result remains unchanged in the accumulator register after sensing or transfer.

The multiply-divide logic senses the operands each iteration and forms a partial product or quotient. The final result is circulated in the product-quotient register until another multiply or divide operation is initiated, or until the LVDC is commanded to store data in the product-quotient register. Unlike the accumulator register which provides data to several destinations, the product-quotient register has only one outlet for its contents. All data leaving the product-quotient register must pass through the accumulator register. The product-quotient register contents are accessible to all arithmetic instructions except multiply and divide.

Voting Element. The voting element comprises the voters and disagreement detectors located between modules of the LVDC and between the central computer and the memory. The voters resolve differences between the outputs of triple redundant circuits before the outputs are passed on to succeeding circuits. Thus the LVDC can sustain multiple failures (but not identical failures occurring simultaneously) and still function reliably. The disagreement detectors monitor inputs to the voters and provide outputs which indicate when a failure has occurred. Since failures are self-correcting, there are no failure indications for non-catastrophic malfunctions in the computer logic except those from the disagreement detectors. The voting element is not shown in Figure 15.4-1 because it is widely disseminated through and between the functional elements.

TYPICAL OPERATION

Assume that the LVDC program has been initiated and is running smoothly. The area of the memory in which the program will operate has been selected and instructions are coming from syllable zero. The memory is operating in the duplex mode with memory "A" selected. For descriptive purposes, typical operation begins with reading an instruction from the memory. The address of the instruction is shifted out of the instruction counter and applied to the transfer register and the add-subtract logic in the arithmetic element. The add-subtract logic increments the count by one and reinserts it into the accumulator register where it is circulated. The instruction address is shifted into the transfer register and then transferred in parallel to the address register. The next events occur in the memory control element.

Timing inputs indicate to the syllable select circuit and the memory timing and sync select circuit that an instruction is due to be read. The syllable select circuit selects syllable zero (the stored syllable selection for instructions) in all memory modules. The memory timing and sync select circuit performs 3 functions at this time. It conditions the memory address decoders to decode the contents of the instruction sector register rather than the data sector register; it conditions the memory clock drivers of all memory modules to produce read pulses; and it delivers a sync impulse to the memory mode and module select circuit. The memory mode and module select circuit routes the sync impulse to the memory clock drivers of the two (duplex operation) memory modules selected by the instruction module register.

Upon being impulsed, the memory clock drivers produce read timing pulses which enable the selected X and Y drivers to transfer the instruction out of the addressed memory location. The memory sense amplifiers transmit the instruction to the memory buffer registers. The memory buffer registers store the instruction for parity checking and to enable the inhibit drivers during the restore memory cycle (explained later). If the parity of either memory buffer register is incorrect or if a drive current

.ress registers the data word to be stored begins to emerge from the accumulator register. Outputs from the operation code register and the operation decoders condition the transfer register to shift in step with the accumulator register and accept its output. As the data word enters the first position of the transfer register, the parity counter monitors the number of "1's" it contains. At this point, the focus moves to the memory control element.

Timing signals indicate to the memory control element that a data word is due to be transferred to or from the memory. The operation code specifies that data is going to the memory by causing the memory timing and sync select circuit to switch the read/store signal to store. The syllable select circuit selects syllable zero as the first syllable to be transferred. The memory timing and sync select circuit conditions the memory address decoders to enable the X and Y drivers of the memory location addressed by the address register and the data sector register. Just before the last bits of the syllable enter the transfer register, the memory timing and sync select circuit delivers a sync impulse to the memory mode and module select circuit. The memory mode and module elect circuit routes the impulse to the memory clock drivers of the selected data modules. The memory clock drivers produce read timing pulses, but the data transferred out of the memory is not sensed because a store, not read, operation has been specified. Since reading the memory is a destructive process, the addressed memory location is left cleared.

Simultaneous with clearing the memory location, the last bit of the syllable enters the transfer register and the syllable is transferred to the memory buffer registers. The transfer register continues shifting and the second syllable of data starts to file into the transfer register. At the memory buffer registers, a "parity bit" is added to the syllable entering the memory. The parity bit is controlled by the parity count circuit so that each memory buffer register contains an odd number of "1's". (Bear in mind that the parity count circuit monitors the number of "1's" in the syllable as it enters the transfer register.) The memory timing and sync select circuit then impulses the memory again, and the first syllable of data enters the memory through the inhibit drivers. The second syllable of data enters the memory in the same manner as the first and like the first includes its own parity bit.

It was noted previously that data could be stored in the product-quotient register. When this operation is specified, the memory is inhibited and the accumulator contents are shifted directly into the product-quotient register as one intact unit.

Operations which do not use the memory either shift the contents of the accumulator register or use the operand address as a constant for controlling the program. Shifting the contents of the accumulator register is accomplished by shortening or lengthening its circulation loop. Before the first bits of the accumulator contents begin to emerge, outputs from the operation code register and the operation decoders, along with control bits from the address register, alter the recirculation path of the accumulator register to effect the shift. When the last bit has been shifted, timing signals restore the loop to normal to prevent shifting the contents of the instruction counter. The instruction counter is then incremented and shifted into the transfer register to address the next instruction.

Among the operations which do not use the memory are those which make logical decisions based on the contents of the accumulator register. As noted previously, logical decisions are made by altering the contents of the instruction counter if a specified condition exists in the accumulator register. If the condition exists, the operand address of the instruction replaces the existing contents of the instruction counter and the next instruction begins the new sequence. Logical decisions are implemented by continuously sampling the accumulator contents part way through the register for the conditions upon which decisions are based. Thus, when a logical decision is initiated, most of the accumulator contents have already been sampled and the computer need not wait until the complete contents emerge from the register to make the decision. The contents of the instruction counter immediately follow the accumulator contents in the accumulator register. Consequently, when the last data bit has been sensed and the decision made, the contents of the instruction counter are still only part way through the accumulator register. If the condition is met, the accumulator register is broken just behind the last bit of the accumulator contents and the operand address is shifted into the accumulator register from the transfer register, replacing the existing instruction count.

Since the memory is not being used, the transfer register is not needed to distribute data from it, and therefore is not cleared after the instruction is distributed to the program control element.

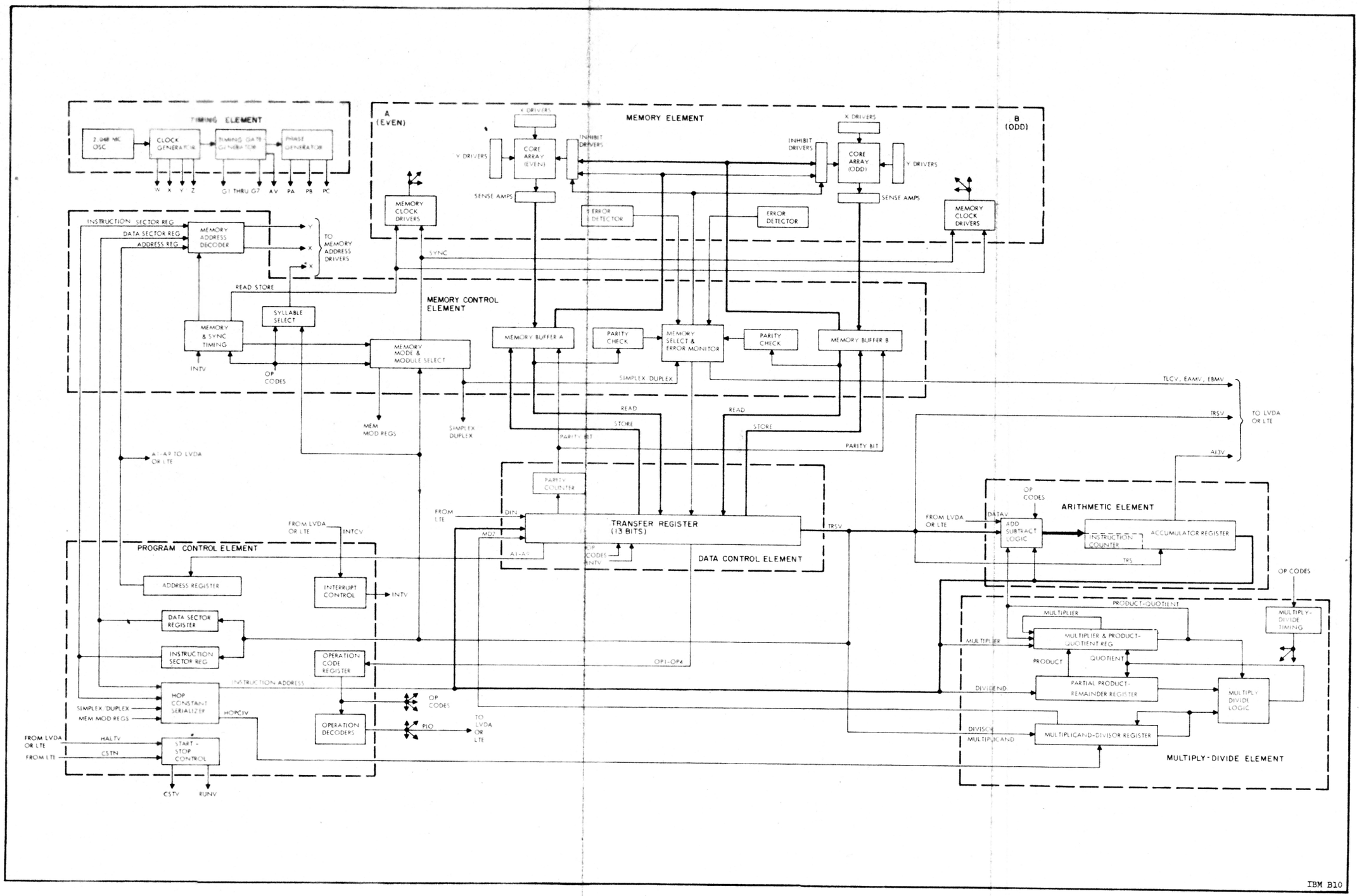


Figure 15.4-1 Computer Functional Block Diagram

If the condition is not met, the accumulator register is not broken and the existing contents of the instruction counter are retained to address the next instruction.

Data are processed by using two's complement arithmetic. Two's complement arithmetic eliminates the necessity for a recomplementation cycle when using sign plus magnitude arithmetic. Special algorithms have been developed and implemented for multiplication and division of two's complement numbers. Multiplication is done 4 bits at a time and division 2 bits at a time.

The LVDC is interconnected with the LVDA which contains input/output conversion electronics and power supplies for the LVDC. Salient characteristics of the triple modular redundant LVDC are summarized in Table 15.4-1.

Table 15.4-1 Launch Vehicle TMR Computer Characteristics

Characteristic	Description
Type	Stored program, general purpose, serial, fixed-point, binary
Clock	2.048 MHz clock, 4 clocks per bit, 512 kilobits per second
Speed	Add-subtract and multiply-divide simultaneously
Add time, accuracy	82 μs, 26 bits
Multiply time, accuracy	328 μs, 24 bits
Mult-hold time, accuracy	410 μs, 24 bits
Divide time, accuracy	656 μs, 24 bits
Memory	Random access toroidal core
Storage Capacity	Up to a maximum of 32,768 twenty-eight-bit words in 4096-word modules
Word Length	Memory word 28 bits: 2 instructions may be stored in one memory word
Data	26 bits plus 2 parity bits
Instruction	13 bits plus 1 parity bit
Input/Output	External: computer-programmed I/O control: external interrupt provided
Component Count*	40,800 silicon semiconductors and film resistors (cermet). Up to 917,504 toroid cores
Reliability*	0.996 probability of success for 250 hours using TMR logic and duplex memory modules
Packaging	Structure constructed of magnesium-lithium material, designed to house 73 electronic pages and 8 memory modules
Weight*	34 kg (75.0 lbs) (4 memory modules)
Volume*	0.07 meters^3 (2.4 feet^3)
Power*	150.0 watts (4 memory modules)

*Figures given here are estimated values

In the following paragraphs some details about the computer circuits and their operation will be described.

15.4.2 WORD ORGANIZATION

The LVDC uses a 28-bit word consisting of two 14-bit syllables. Each syllable includes 13 data bits and 1 parity bit. Each syllable is stored separately in the memory. The parity bits are used only to check the accuracy of transfers to and from the memory which leaves a data word 26 bits in length (Figure 15.4-2).

The use of the data word is at the discretion of the programmer. Each of the 26 bits may be used as an indicator to show the presence or absence of some condition, or the word may be used as a binary number for arithmetic computations. Binary numbers are represented by a sign bit and 25 magnitude bits; negative numbers are shown in two's complement form.

This text uses 2 methods for designating bit positions in the data word. Where the word represents a binary number, the bits are designated sign and 1 through 25, proceeding toward the least significant digit. When used in this context, bits 1 through 25 are called "magnitude bits". The bits are designated 1 through 26 when not referencing the data word as a binary number; bit 1 corresponds to sign and bit 26 corresponds to bit 25 of the numeric designations.

The computer word is also used to store the instructions of the computer program. Instructions are 13 bits in length with one instruction stored in each syllable of the computer word. An instruction consists of a 4-bit operation code (OP1-OP4) and a 9-bit address (A9, A1-A8). Figure 15.4-2 shows how the instructions are placed in the computer words.

15.4.3 TIMING

The basic unit of computer timing is called the "computer cycle". The duration of an LVDC cycle is approximately 82 microseconds; this is the time required for the LVDC to read, decode and operate its basic instructions. The signals which define a computer cycle originate in the phase generator. A computer cycle corresponds to a full cycle of the phase generator which produces three equal-length timing signals called phase A, phase B, and phase C. Thus, a computer cycle is defined by three "phase times".

The phase generator separates the computer cycle into "instruction time" and "operation time". As the names imply, instruction time is the period in which an instruction is read and decoded, and operation time is the period in which the operation commanded by the instruction is performed. Generally, instruction time occurs during phase A and operation time during phase times B and C.

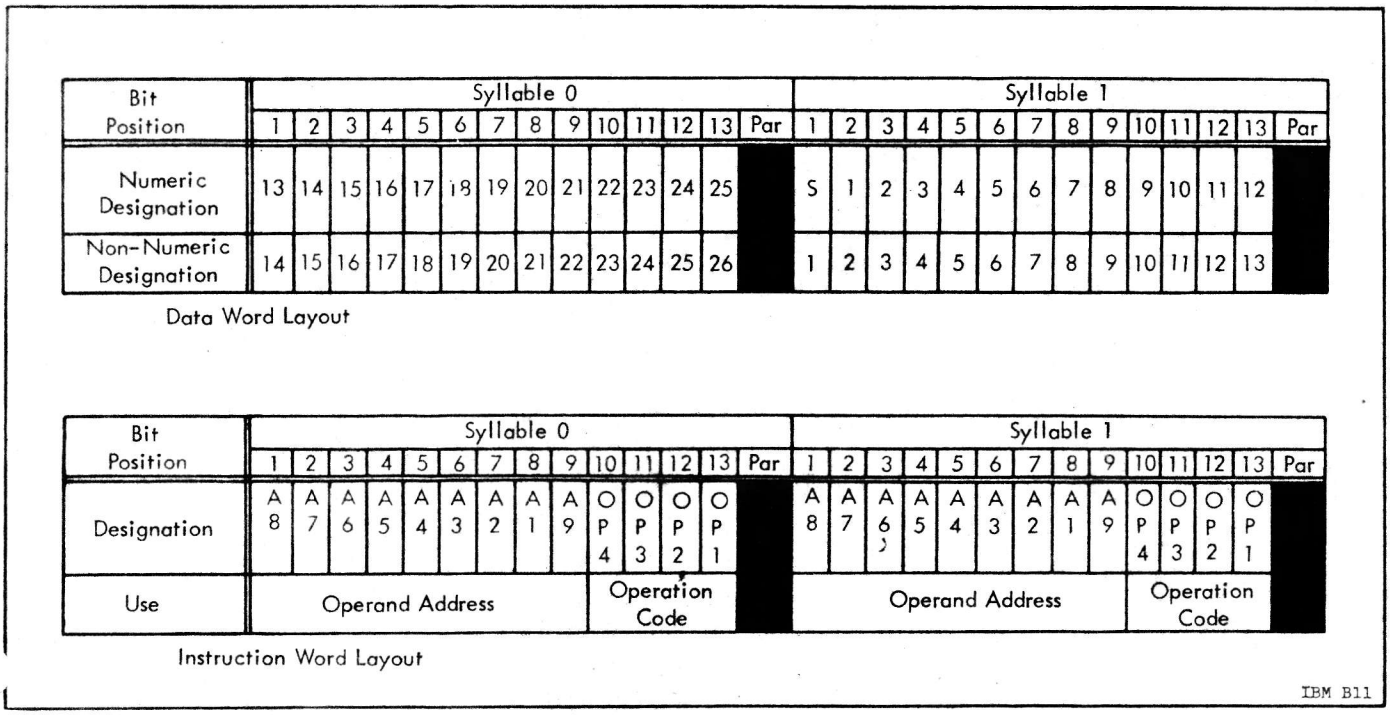


Figure 15.4-2 Word Organization

Notice the correlation between the organization of timing and word layout. The LVDC cycle is defined by 3 phase times and involves 3 syllables of information: 1 syllable for an instruction and 2 syllables of data for an operand. The correlation also extends downward one stop. A syllable consists of 14 bits (13 data and 1 parity) and each phase time is divided into 14 equal segments called "bit times". A bit time is the time each bit of data is stored in one position of a serial storage device before moving on to the next.

To facilitate several logic operations during each bit time, the bit times are subdivided into four equal parts called clocks. The clocks are identified by the letters W, X, Y, and Z and occur in alphabetical sequence. Figure 15.4-3 shows the relationships of the various levels of timing and gives the time duration of each level. Timing is given by a letter-number-letter abbreviation of the phase time, bit time and clock time in descending order of time duration. For example, an event resulting from the W clock of bit-time 11 during phase A is described as happening at A-11-W time. If one level of timing does not apply or has been previously established, that level may be dropped from the abbreviation; i.e., a circuit which operates independent of phase timing may produce an output at every 6-Z time.

The timing element contains all the circuits which generate timing signals for the operation of computer logic. Basically, the timing element consists of an oscillator and 3 cascaded frequency dividers: the clock generator (which includes the oscillator), the timing-gate generator, and the phase generator. The oscillator produces the basic timing signal, from which all other timing signals are derived. The clock generator divides its oscillator output frequency by four to produce a sequence of 4 clock signals which recur each bit time. The clock signals divide each bit time into 4 parts, enabling several logic operations to be performed on each serial data bit. The signals used to identify bit times are developed by the timing-gate generator.

The timing-gate generator divides the clock frequency by seven, producing seven timing gates which, with their complements, can be combined to identify 14 bit times. The phase generator then divides the output frequency of the timing-gate generator by three to define the 3 phases of the LVDC operation cycle. Several additional signals, embodying various combinations of phase, timing gate, and clock signals are generated by special timing circuits.

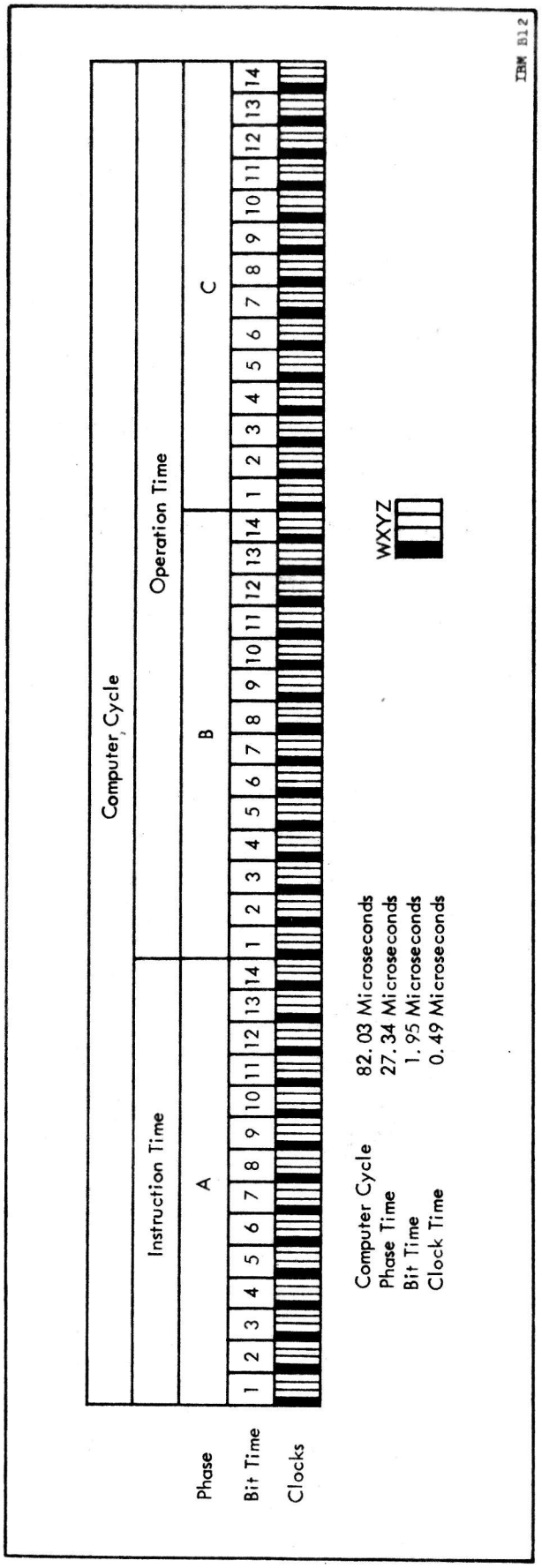


Figure 15.4-3 Computer Timing Organization

The clock generator consists of 4 parts: an oscillator, a buffer amplifier, timing logic, and clock drivers (Figure 15.4-4). (All parts except the oscillator are triple redundant; therefore, the following description applies to all channels.) The clock generator produces a repetitive sequence of four clock pulses (W, X, Y, and Z) which are used to time logic operations in the LVDC. A special clock called BON is generated for driving the delay lines. The logic clocks occur at a repetition rate of 512 kHz, while the delay-line clock occurs at a 2.048 MHz rate.

The oscillator produces a 2.048 MHz sine wave which is used, ultimately, to generate all other computer timing signals. The sine wave is amplified and shaped in the buffer amplifier which produces a complementary pair of square wave outputs, BO and BON. The BON signal is fed to the delay lines and the BO signal to the timing logic where it is frequency divided to generate signals which separate the 4 clocks.

A modified Pierce oscillator is used to generate the 2.048 MHz sine wave which is the basic timing signal for the clock generator. The oscillator contains only 6 components and draws all its operating current from the buffer amplifier. The low component count and absence of a supply-voltage input greatly enhances the oscillator's reliability.

15.4.4 MEMORY

A core memory provides the necessary storage medium in the LVDC. The memory is divided into memory modules. The number of memory modules may vary from one to eight. Each module consists of 14 planes with 128 by 64 cores in each plane (a total of 114,688). The basic module contains 4,096 non-redundant 28-bit words (one bit per core). The memory modules operate independently and may be used in either a simplex or duplex mode. In the simplex mode, each memory module is usable for programming. Duplex operation requires pairs of memory modules to function in parallel. Each pair of modules containing the same information, effectively halves the amount of storage that would be available if the same number of modules were operated simplex. With 8 memory modules operating in simplex, the computer has a memory capacity of 32,768 words (of 28 bits each) which is equivalent to the basic memory capability of the IBM 7090 commercial machine. Storage external to the memory is located predominantly in glass delay lines and latches to provide temporary storage for the accumulator, PQ registers, etc.

The organization of the memory modules is indicated in Figure 15.4-5. For addressing, the 128-core dimension is divided into two equal 64-core

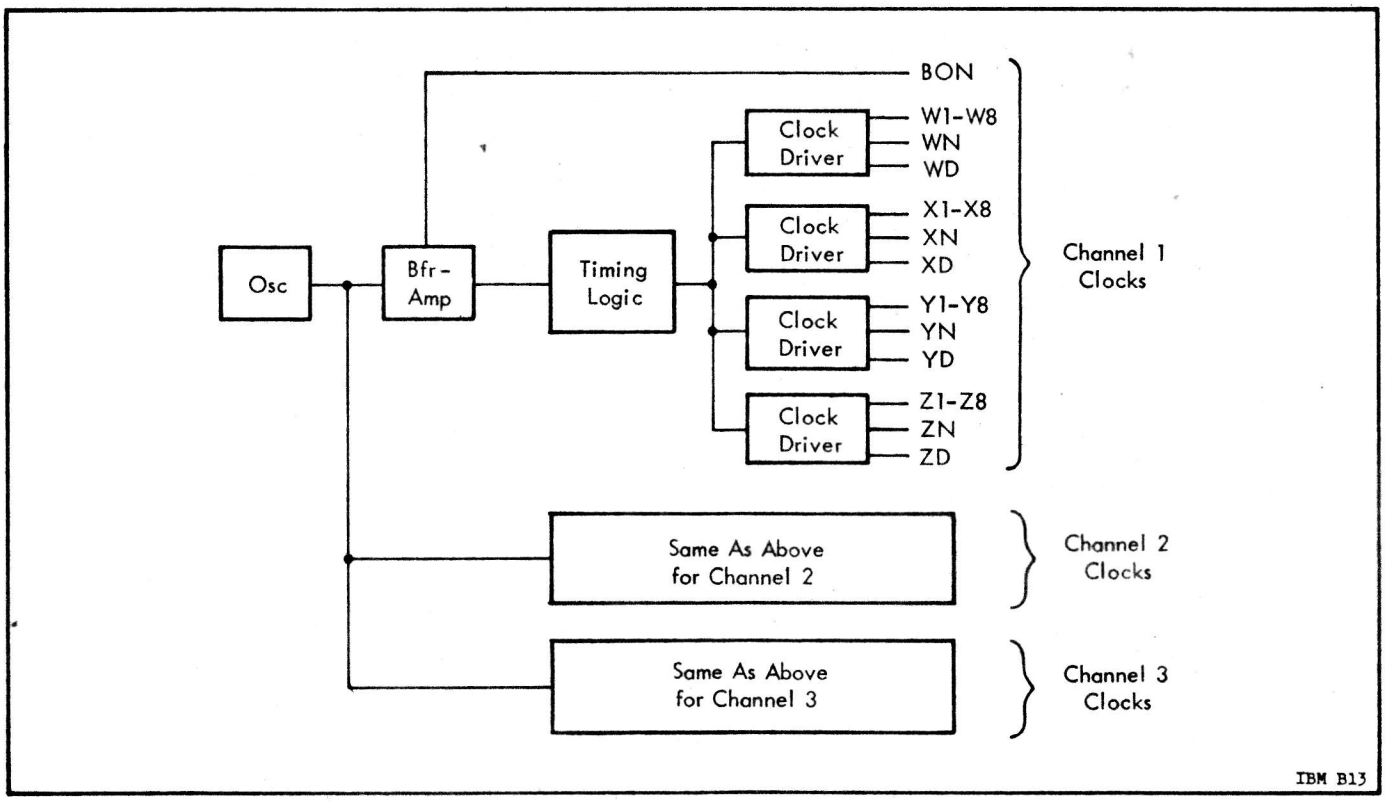


Figure 15.4-4 Clock Generator Block Diagram

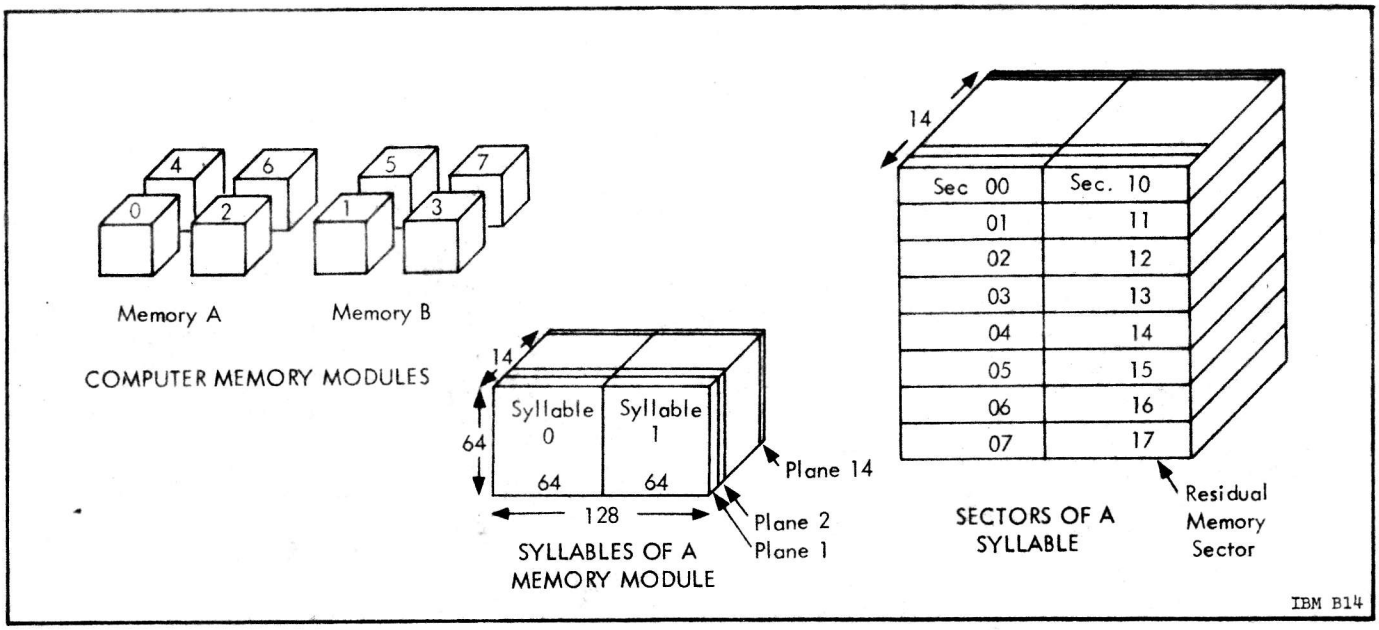


Figure 15.4-5 Memory Module Arrangement

sections to produce the syllable 0 and syllable 1 portions. Each syllable is then divided into 16 sectors (with 8 by 32 cores each). The last sector in each syllable is called residual memory. It provides a common storage area within the module (for constants, frequently used formulas, etc.) and allows efficient programming. Thirteen of the fourteen memory planes in the memory are for data and instructions and one plane for parity bits.

Each sector will have 256 addresses ranging from 0 through 377 (octal). Addresses of sector 17 (residual storage) will be 400 to 777 (octal). The selection of memory modules is program-controlled. The LVDC has the capability of using instructions from one module and data from another, or both from the same module.

To enable the memory to function with a serial arithmetic unit, a serial-by-bit operating mode is used. This is accomplished by taking two 13-bit memory words (syllable 0 and syllable 1) and producing a 26-bit computer word. The central computer logic then utilizes the serialized computer word. Odd parity is assigned to each half, or 13 bits, of a computer word when it is written into memory. A parity check is made on all information read from memory.

CORE MEMORY FUNDAMENTALS

Figure 15.4-6 illustrates the properties of a ferrite core. As shown in the figure, the core can be magnetized in either of 2 directions. By establishing that a core "contains" a "1" when magnetized in one direction and a "0" when magnetized in the opposite direction, the core can be used to store one "bit" of a binary number. The core is magnetized by passing a dc current of $\frac{I}{2}$ through the X and Y drive lines in coincidence.

The direction of magnetic flux about the core can be reversed by passing the same currents through the drive lines in the opposite direction. Reversing a core in this manner is called "switching" the core. A sense winding, represented by S in the figure, also passes through the core and lies within its magnetic field. When a core is switched, the resulting collapse and expansion of its magnetic field causes a pulse of voltage to be induced in the sense winding. Thus, if

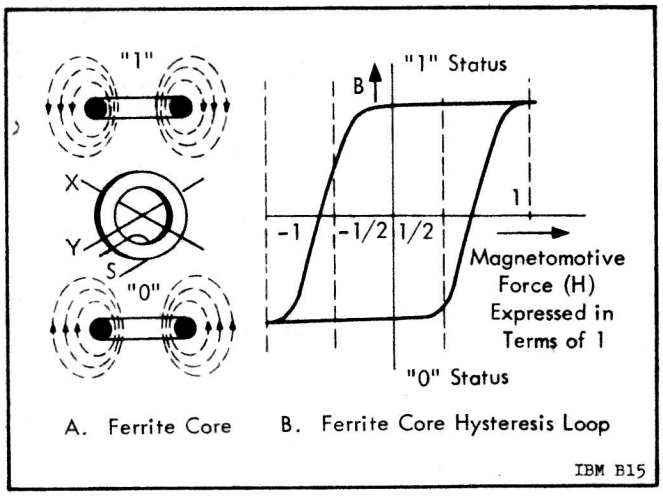


Figure 15.4-6 Ferrite Core Characteristics

a core containing a "1" is switched to a "0", the resulting voltage pulse in the sense winding can be amplified and used to set a latch, indicating the core contained a "1". If the core already contained a "0" it would not switch, and no voltage pulse would appear in the sense winding to set the latch.

This is the method used for reading information from a core memory. It is called "destructive readout" because after the core is read it no longer contains the "1" which was sensed from it. The latch into which the "1" was read is a buffer between the core and the circuits which use the stored information. The "buffer latch" stores the "1" until it can be transferred into the computer and until the core can be switched back to its original state. The process of driving a core to a "0" and sensing whether or not it produced an output is called a "read cycle". Switching the core back to its original state is called a "store cycle".

Cores are arranged in rows and columns as shown in Figure 15.4-7. An X drive line passes through all the cores in a column and a Y drive line through all the cores in a row. The unit is called a plane. The cores are positioned on the drive lines in a pattern which puts the magnetic fields of adjacent cores 90 degrees apart; this eliminates interference between cores. The sense winding runs parallel to the Y drive lines and passes through all the cores in the plane.

If the plane is viewed as the first quadrant of a Cartesian Coordinate System, the X and Y drive lines represent units along the X and Y axes. The location of each core can then be defined by the X and Y drive lines which pass through it. The circuits which operate the plane are controlled so that only one X and one Y drive line carry current at any given time. Only the core at the intersection of the selected drive lines receives the coincident current necessary to switch it. Hence, this method of selecting memory locations is called "coincident-current addressing". When a memory location is selected by coincident-current addressing, one core along each selected drive line receives the full current necessary to select it.

Computers operate using "words" which comprise a number of bits, thus the memory must be expanded to store a complete word in each location. The expansion is accomplished by providing a separate plane for each bit in the word. The planes are stacked one above the other to form an "array". Each X drive line is linked to the corresponding lines of the other planes in the array to form one continuous drive line. This drive line passes through the same locations in every plane of the array. The Y drive lines are similarly interconnected. Thus, when a pair of drive lines are energized, a core is selected in each and every plane at the corresponding intersection of the X and Y drive lines.

Each plane has a separate sense winding and buffer latch to allow the bits to be sensed individually. However, a problem is encountered in attempting to restore the information into the memory.

As presented up to this point, energizing a pair of drive lines switches all the cores in the addressed location to the same state. There is (thus far) no provision for storing numbers which contain both "1's" and "0's". Therefore, a fourth winding called an "inhibit" winding is wound through each plane to allow bits to be stored individually. The inhibit winding runs parallel to the X drive line and carries the same current (but in the opposing direction) as the drive line. These windings are utilized only during store cycles. During a store cycle, the drive lines attempt to switch every core in the addressed location to "1's". However, any buffer storage latches containing "0's" energize the inhibit windings in the corresponding planes. Inhibit current opposes the current in the X drive line and cancels its effect. Thus, the addressed cores in the inhibit planes feel only the half-select current of the Y drive line and do not switch. Since the cores in the addressed location were all switched to "0's" when they were read, any inhibited cores will simply remain in the "0" state.

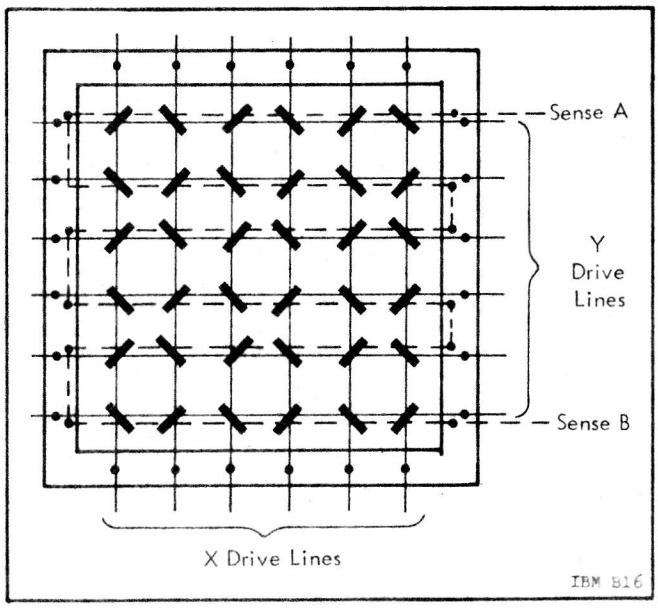


Figure 15.4-7 Core Plane

Associated with the array are a number of special circuits which are required to operate the array. Included in these circuits are the sense amplifiers, some special timing circuits, and the circuits which provide power to the drive lines and inhibit windings.

MEMORY MODULES

The memory element is composed of up to eight integral and asynchronous memory modules, which operate under control of the memory control element. The modules are termed "integral" because each module is a complete memory in itself. Included in each module are a core array and all the circuits required to transfer information to and from it. Asynchronous refers to the fact that the timing signals which carry a module through a memory cycle are developed within the module and are not in synchronism with any others in the computer. When information is to be transferred to or from the memory element, the computer delivers a sync impulse to the selected module (or modules), waits a reasonable time for the module to perform the transfer, and then continues (assuming that the transfer is complete). During the memory cycle, the memory control element provides signals to the memory element which control addressing and determine the direction of transfer.

Figure 15.4-8 is a block diagram of a memory module showing all the circuits it comprises. The memory clock drivers (upper left) receive the sync impulse from the computer and convert it to a series of read or store timing pulses. The timing pulses turn the memory address drivers and inhibit drivers ON and OFF and strobe the sense amplifiers at the

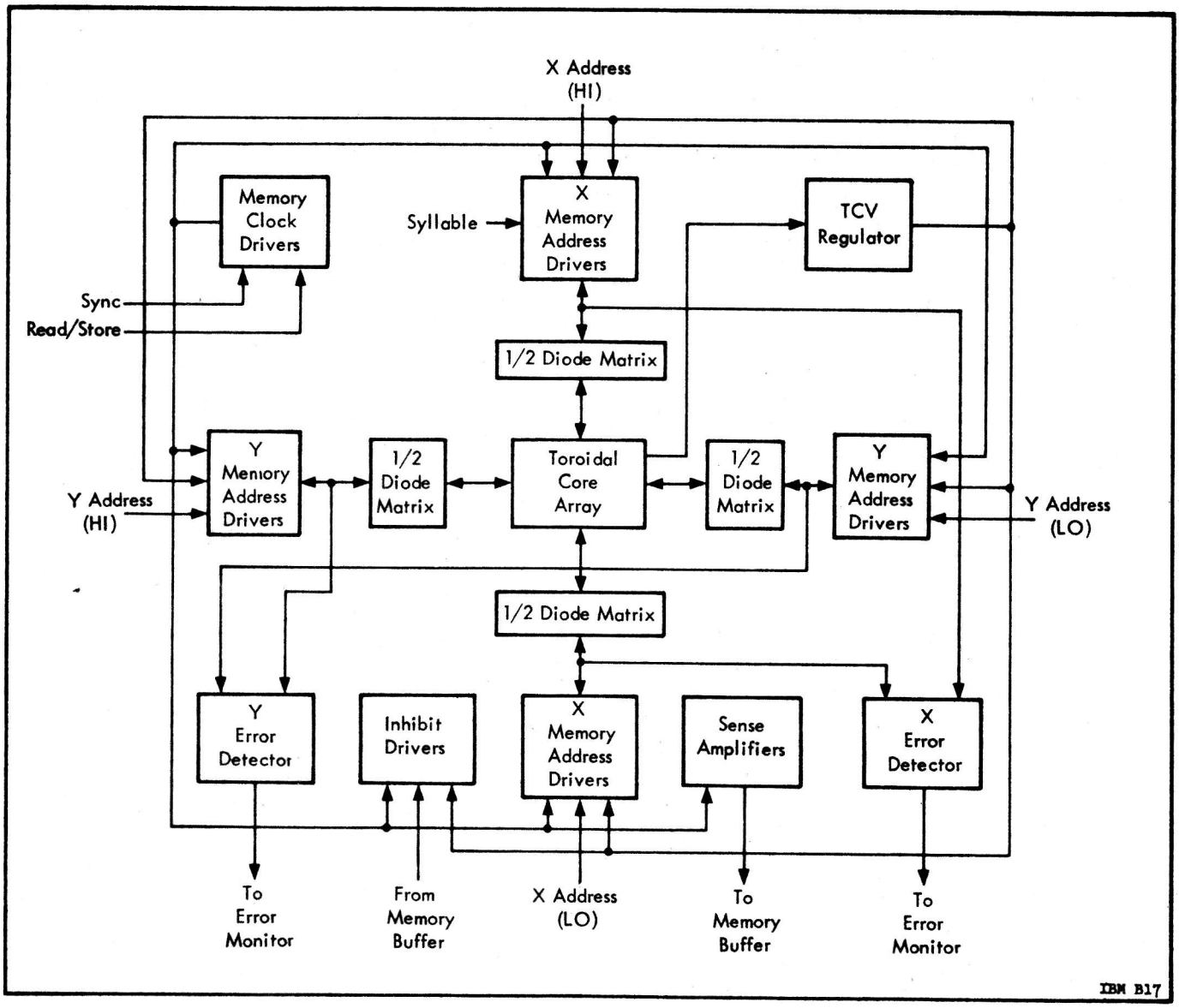


Figure 15.4-8 Memory Module Block Diagram

proper time. There are two memory address drivers for each drive line in the array. Addressing signals from the memory control element select one X and one Y drive line by conditioning two X and two Y memory address drivers. When the timing pulses occur, the conditioned memory address drivers pass coincident current pulses through the selected drive lines to switch the cores in the addressed location. Diode matrices provide isolation between drive lines. A pair of error detectors continuously sense X and Y half-select current to indicate addressing errors to error monitor circuits in the memory control element. A temperature controlled voltage regulator adjusts the memory address drivers and inhibit drivers to produce the optimum current output for the prevailing temperature in the array. A temperature sensing element, attached to the array, develops the inputs for the temperature controlled voltage regulator.

Static control signals from the memory control element determine whether information will be read or stored by conditioning the memory clock drivers to produce the appropriate series of timing pulses. If information is to be read, a series of read pulses is generated causing the memory address drivers to switch all the addressed cores to "0's". Read timing includes a strobe pulse for the sense amplifiers which is delayed from the drive current to allow for the inductive reactance of the windings through the array. If the purpose of the read cycle is to clear the addressed location so that new information may be stored in it, the strobe pulse is inhibited and the sense amplifiers produce no outputs.

If a store cycle is required, the timing pulses produced by the memory clock drivers reverse the polarity of the memory address driver outputs. The memory address drivers then attempt to drive all the addressed cores to "1's"; however, the store pulses are also routed to the inhibit drivers. Any inhibit drivers conditioned by "0's" in the memory buffer register will produce an output opposing the X drive current. Inhibited cores feel only the Y half-select current and therefore remain in the "0" state.

The memory control element provides the timing, decoding, memory selection and temporary storage operations which are required to properly operate the memory element. The memory control element consists of two buffer registers, a timing and sync selection circuit, address decoding circuits, syllable selection circuits, a memory mode and module selection circuit, and an error monitor and memory select circuit.

The computer memory readout is destructive, i.e., as data is read from the memory, the applicable memory bits are all driven to "0". The buffer registers hold the data read from memory long enough so that it can be read back in, thereby making the memory readout effectively non-destructive.

In addition to saving the memory from progressive obliteration, the memory buffer registers feed memory data to the transfer register, and receive data to be stored in memory from the transfer register. The transfer register assumes the role of a shift register when it is receiving data to be loaded into memory. To function as a shift register, the transfer register makes use of multiple clocks. Therefore, special timing is required to lift data from the transfer register as soon as it has been loaded and before it starts another shift cycle. This timing is provided by the buffer register timing circuits which will be discussed later.

The memory select and error monitor circuit continuously checks the performance of the memory. During duplex operation, the memory buffer selection is controlled to correct transient errors and provide an uninterrupted flow of reliable information to the computer. Memory errors are detected by parity checking the buffer registers after every read cycle and by monitoring the outputs of the error detector circuits in the memory modules.

In duplex operation the A and B memories are cycled simultaneously but only one buffer register is selected to provide information to the computer. If an error is detected during a read cycle, the memory buffer containing good information is selected to control restoring both memories; thus the error, if transient, is corrected. If an error occurs in the memory selected to feed the computer, the selection is changed to the correct buffer before the information is used. Thus, the computer receives only reliable information unless both memories fail at the same storage location simultaneously. Operation is not restored to the previously selected memory unless the good memory should develop an error. Monitor signals are provided at the computer interface which indicate the status of each memory and simultaneous failure of both memories.

The memory select and error monitor circuit includes separate parity check and error-detector sensing circuits for each memory; these circuits are called the "error monitors". The error detectors in the memory modules indicate 3 types of addressing failures: (1) multiple address selection; (2) loss of half-select current and (3) spurious selection during

non-cycle times. These failures are combined into 2 types, "on current failures" and "no current failures" by the error-detector sensing circuits. Timing signals which enable the error monitors to sense the different types of errors at the appropriate times are common to both error monitors.

Information flows from the memory buffer registers in 2 directions, through the inhibit drivers into the memory and into the computer to be used. The memory select latches provide separate control over data flowing in each direction. Separate control is maintained so that errors occurring in the non-selected memory can be corrected from the selected memory without changing the selection of the memory buffer which is providing information to the computer.

15.4.5 COMPUTER INSTRUCTIONS

The computer uses a complement of 18 single-address instructions which are composed of a 4-bit operation code and a 9-bit operand address. The 4-bit operation code can select 1 of 16 different instructions to be executed; this range is extended to 18 by grouping 3 instructions under one operation code, then using bits A8 and A9 of the address to discriminate between them. Bits A8 and A9 serve no other function for the instructions which are grouped. A list of the 18 instructions available is given in Table 15.4-2 with the operation code and a brief description of each.

The 9-bit operand address permits selection of 512 memory addresses for use as operands or data storage locations. The memory is divided into a number of sectors, each containing 256 addresses. Address bits A1 through A8 select one of the addresses within the sector. Bit A9 determines whether the address will be in a sector previously selected by the program or in a special sector called "residual memory". Consequently, bit A9 is called the residual bit; residual memory is selected when A9 is a "1".

Instructions which do not require that data be read from the memory frequently use the operand address for special purposes. These special purposes are pointed out in the List of Instructions, Table 15.4-2, where they occur. For example, the shift instructions (SHF) always manipulate the contents of the accumulator and thus requires no operand address; this frees the operand address for use as shift control. One instruction which makes extensive use of its operand address is PIO. A complete breakdown of the PIO addresses is given in Table 15.4-3.

INTERRUPT

A limited program interrupt feature is provided to aid the input-output processing. An external signal can interrupt the computer program and cause a transfer to a subprogram. A computer interrupt occurs when the instruction in progress is completed. All interrupts automatically generate a HOP 400 (octal) instruction. The HOP constant designates the start of the subprogram. Storage of the contents of the instruction counter, sector and module registers, syllable latch, accumulator, and product-quotient registers must be accomplished by the subroutine itself. These values are stored for an eventual return to the interrupted program. Protection against multiple interrupts and interrupts during MPY and DIV operations is also provided.

The interrupt signal may be generated by a timed source. The rate at which it is generated is controlled by changing the magnitude of a number which is being continually summed. When the summed number reaches a predetermined value, the interrupt signal is generated. This is accomplished in the LVDA.

The main program can be resumed by adressing the contents of residual memory word 776 or 777 with a HOP instruction.

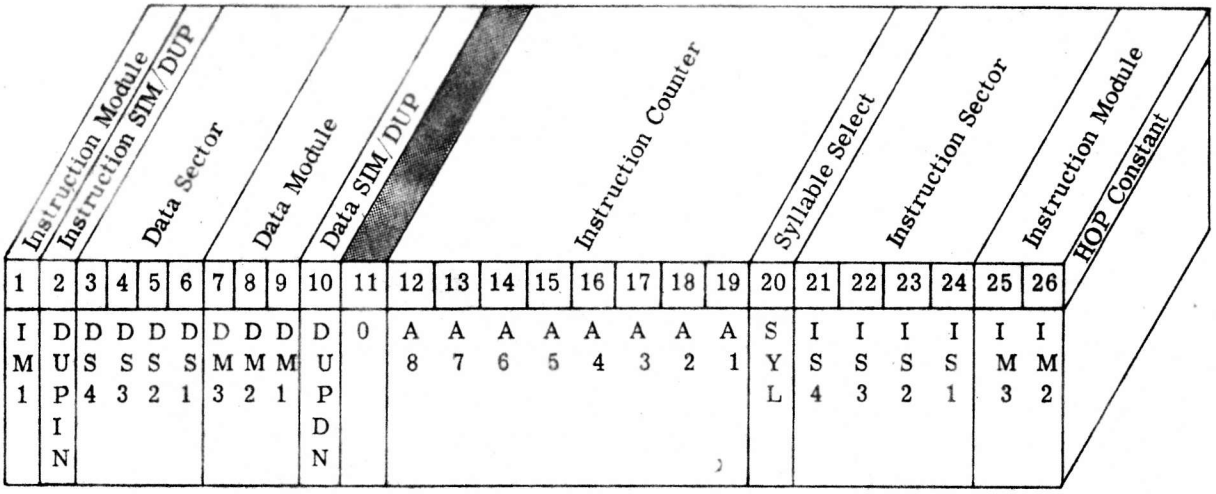
Certain discrete input signals are allowed to cause an interrupt. These are useful in causing the input-output subprogram to give immediate attention to an input or output operation.

The interrupt feature facilitates the timing of input-output operations by causing a transfer to an input-output subprogram. The interrupt signal is generated in the LVDA and may be set to interrupt at the highest rate at which any input-output quantity must be handled. This method avoids the necessity of keeping track of time expired since last entering the input-output subprogram.

The automatic interrupt also makes it possible to permit certain discrete inputs to cause an interrupt. Allowing discrete inputs to interrupt makes it possible to demand that the program give attention to an important discrete input. Communications between the LVDC and the vehicle telemetry monitoring system are thus facilitated.

Table 15.4-2 List of Instructions

Instruction	Operation Code 4 3 2 1	Description
HOP	0 0 0 0	Transfers program to memory location specified by HOP constant and controls simplex/duplex operation of memory. Operand address specifies memory location of HOP constant used to load the registers shown in HOP constant format (below). Full HOP constant MUST be specified each time. First instruction following HOP comes from new location.



MPY	0 0 0 1	Multiplies contents of memory location specified in operand address by contents of accumulator. Uses 24 high-order bits of each operand to form 26-bit product. Product of multiplicand and 12 low-order bits of accumulator is available by addressing 775 with second instruction following MPY; final product is available to fourth instruction following MPY. Program continues while MPY is in progress; concurrent use of accumulator is permitted.
SUB	0 0 1 0	Subtracts contents of memory location specified in operand address from contents of accumulator. Places remainder in accumulator.
DIV	0 0 1 1	Divides contents of memory location specified by operand address into contents of accumulator. The 24-bit quotient is available to the eighth instruction following divide by addressing the P-Q register (775). Program continues while DIV is in progress; concurrent use of accumulator is permitted.
TNZ	0 1 0 0	Conditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select if accumulator contents are not zero. Next instruction comes from new syllable and address. If accumulator is zero, perform next instruction in sequence.
MPH	0 1 0 1	Multiplies contents of memory location specified in operand address by contents of accumulator. Uses 24 high-order bits of each operand to form 26-bit product. Holds up program until multiplication is complete. Product is available from accumulator or P-Q register with instruction following MPH.
AND	0 1 1 0	AND's contents of memory location specified in operand address with contents of accumulator. Result is placed in accumulator.
ADD	0 1 1 1	Adds contents of memory location specified in operand address to contents of accumulator. Sum is placed in accumulator.

Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code 4 3 2 1	Description
TRA	1 0 0 0	Unconditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select. Next instruction comes from new syllable and address.
XOR	1 0 0 1	Exclusive - OR contents of memory location specified in operand address with contents of accumulator, bit-for-bit. When accumulator bit and bit from memory are different, a "1" is placed in the corresponding bit of the accumulator; if accumulator bit and memory bit are alike, a "0" is placed in the accumulator.
PIO	1 0 1 0	Process input or output. Operand address specifies input or output and gives address of data source and destination. See Figure 15.4-3 for listing of addresses.
STO	1 0 1 1	Contents of accumulator is stored in memory location specified by operand address. Contents of accumulator is unchanged. Data can be stored in P-Q register by using address 775. A STO instruction with operand address 776 or 777 causes contents of multiplicand register to be stored in memory location 776 or 777 as specified. These addresses are used for HOP-save feature.
TMI	1 1 0 0	Conditional transfer. Transfer operand address (A1-A8) to instruction counter and A9 to syllable select if accumulator sign is minus. Next instruction comes from new syllable and address. If accumulator sign is plus, perform next instruction in sequence.
RSU	1 1 0 1	Reverse subtract. Contents of accumulator are subtracted from contents of memory location specified by operand address. Remainder is placed in accumulator.
SHF	1 1 1 0 A8 = 0 A9 = 1	Contents of accumulator are shifted MSD or LSD a maximum of 2 bit positions as specified by operand address. Shift control codes are: Address Bit — Shift A1 = 1 — LSD 1 A2 = 1 — LSD 2 A5 = 1 — MSD 1 A6 = 1 — MSD 2 Clears accumulator if all shift control bits are "0's".
CDS	1 1 1 0 A9 = 0	Change data sector. Operand address is used as a constant to load registers indicated below.

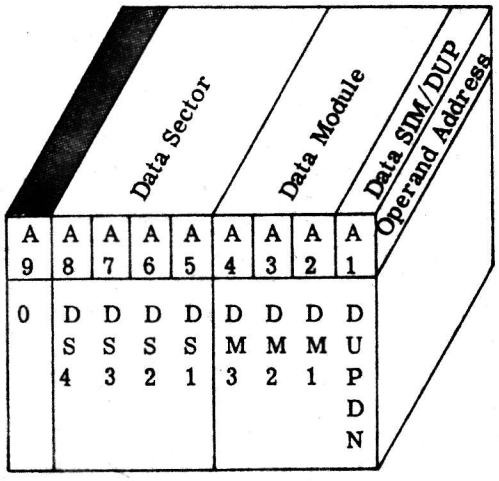
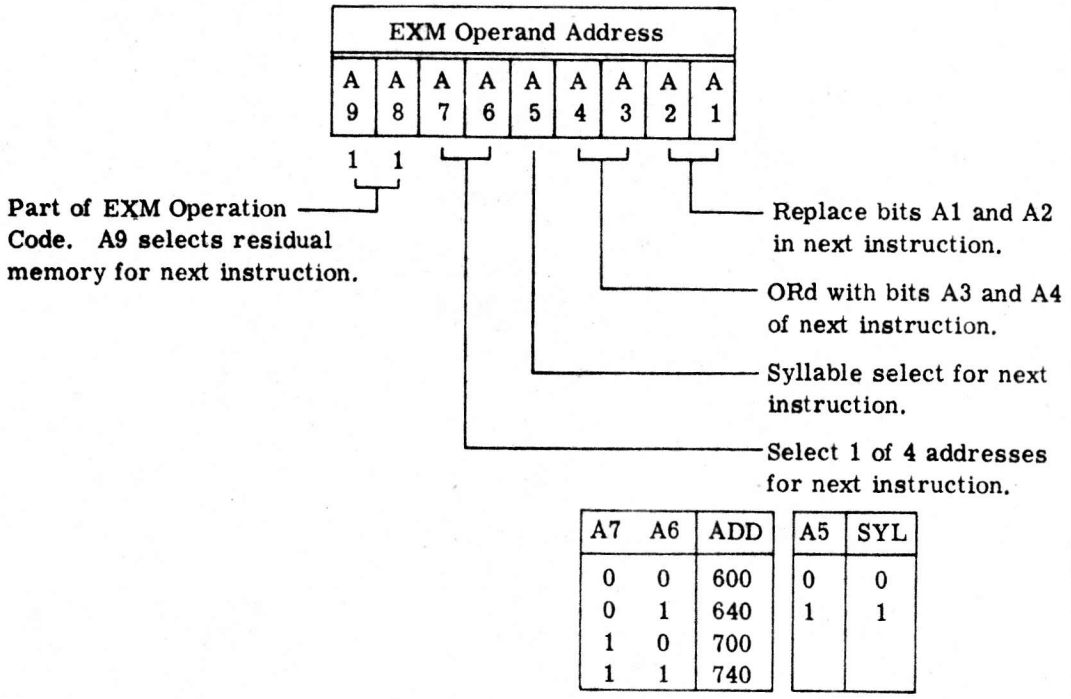


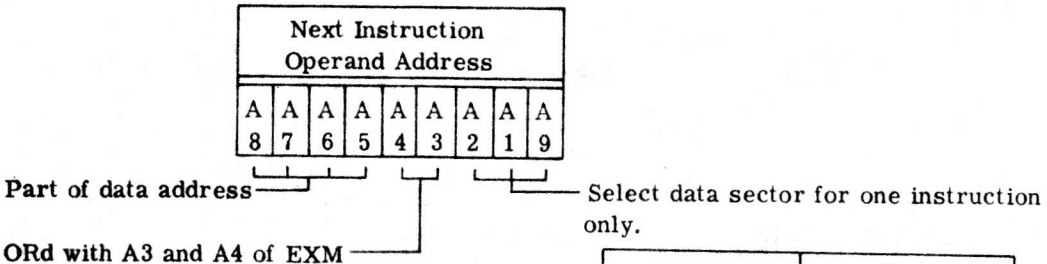
Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code (4 3 2 1)	Description
EXM	1 1 1 0 A8 = 1 A9 = 1	**Execute modified. Operand address selects 1 of 8 instructions in residual memory to be the next instruction executed and modifies its operand address as shown below prior to execution.**



A7	A6	ADD
0	0	600
0	1	640
1	0	700
1	1	740

A5	SYL
0	0
1	1



A2	A1	A9	Data Sector
0	0	0	04
0	0	1	14
0	1	0	05
0	1	1	15
1	0	0	06
1	0	1	16
1	1	0	07
1	1	1	17 (Res. Mem)

Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code 4 3 2 1	Description
EXM (cont)	1 1 1 0 A8 = 1 A9 = 1	EXM operation is diagrammed below.
CLA	1 1 1 1	Contents of memory location specified by the operand address are transferred to cleared accumulator.

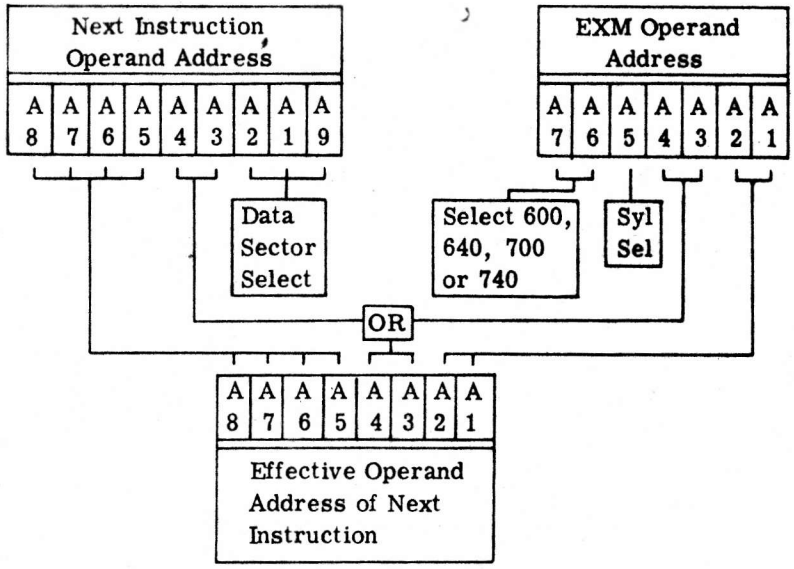


Table 15.4-3 PIO Addresses

Group Selection and Functions										
Group	Data Source	Data Destination	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 & 3	LVDC Accumulator	LVDA Telemetry Registers	X	0	└	Address			┘	0	X
1 & 3A	LVDC Main Memory	LVDA Telemetry Registers	0	1						0	X
1 & 3B	LVDC Residual Memory	LVDA Telemetry Registers	1	1						0	X
2	LVDC Accumulator	LVDA Output Registers	X	0						1	0
2A	LVDC Main Memory	LVDA Output Registers	0	1						1	0
2B	LVDC Residual Memory	LVDA Output Registers	1	1						1	0
4	LVDA Peripheral Inputs and Errors	LVDC Accumulator	X	0						1	1
5	LVDA Resolver Processor Inputs	LVDC Accumulator	X	1						1	1

Group Addresses							
Group 2	Group 4	Group 5	A7	A6	A5	A4	A3
			0	0	0	0	0
Mode Register		Spare No. 6	0	0	0	0	1
Discrete Output Register (Reset)			0	0	0	1	0
Discrete Output Register (Set)		Computer COD Counter Start	0	0	0	1	1
Internal Control Register (Set)	Error Monitor Register	Fine Gimbal No. 1	0	0	1	0	0
Internal Control Register (Reset)			0	0	1	0	1

Table 15.4-3 PIO Addresses (Cont)

Group Address								
Group 2	Group 4	Group 5	A7	A6	A5	A4	A3
Interrupt Register Reset Switch Selector Register (Load)		Coarse Gimbal No. 3 Computer COD Counter Start	0 0	0 0	1 1	1 1	0 1
Orbital Checkout Switch Selector & Discrete Output Registers(Read)	Command Receiver or RCA-110 Discrete Input Spares	Coarse Gimbal No. 1 Horizon Seeker No. 1 Spare No. 3	0 0 0 0	1 1 1 1	0 0 0 0	0 0 1 1	0 1 0 1
Switch Selector Interrupt Counter COD Error (Read) Inhibit Interrupt Minor Loop Timed Interrupt Counter	Telemetry Scanner Switch Selector	 Spare No. 4	0 0 0 0	1 1 1 1	1 1 1 1	0 0 1 1	0 1 0 1
	Real Time Accelerometer Processor X Accelerometer Processor Z	 Fine Gimbal No. 4 Spare No. 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 1 1	0 1 0 1
	Accelerometer Processor Y Interrupt Storage	Horizon Seeker No. 3 Horizon Seeker No. 2 Coarse Gimbal No. 4 Spare No. 5	1 1 1 1	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1
Ladder No. 1 Ladder No. 2 Ladder No. 3		Coarse Gimbal No. 2 Fine Gimbal No. 3 Spare No. 2	1 1 1 1	1 1 1 1	0 0 0 0	0 0 1 1	0 1 0 1
Ladder No. 4 Ladder No. 5		Fine Gimbal No. 2 Horizon Seeker No. 4	1 1 1 1	1 1 1 1	1 1 1 1	0 0 1 1	0 1 0 1

A maximum of 12 interrupts are provided for the LVDA. Under normal operating conditions, when a bit is set in interrupt storage, a HOP 400 will be forced to the LVDC upon completion of the instruction currently being executed. When the LVDC program has completed processing the interrupt, a PIO instruction addressing "Interrupt Register Reset" with the bit corresponding to the bit causing the interrupt set, must be sent to the LVDA just prior to executing the return HOP. This is necessary to inform the LVDA that the condition causing the interrupt has been processed. The LVDA will then check to see if the interrupt is still present. If the interrupt is still present, the LVDA will inhibit sending an interrupt for that particular condition until the interrupt has been removed. Once the interrupt has been removed the LVDA inhibit will be removed, and normal processing will be resumed.

15.4.6 COMPUTER CONTROL

The data control element consists of the transfer register and the parity counter. The transfer register is the central storage location in the LVDC which provides a two-way path for transfer of data or instructions between itself and the memory, or itself and other storage locations in the central computer. The parity counter assigns a parity bit to all syllables of data that are stored in the memory. When these syllables of data are subsequently read out of memory, their parity condition is checked against the parity bit.

The transfer register is a 13-bit shift register which receives from and sends inputs to the memory buffer registers, the arithmetic element, the multiply-divide element, and the external equipment.

The parity counter assigns parity bits by making all syllables have "odd" parity. The parity counter "counts" the number of "1's" in a syllable and adds a "1", as necessary, so that the total number of "1's" is an odd number. Thus, if the total number of "1's" is even, the parity counter adds a bit; if odd, no bit is added. The parity counter operates during a store operation when data is loaded into the memory.

The program control element steps the computer program through its instructions to execute the commanded operations. To accomplish this task, the program control element performs the following functions:

- Starts or stops the program under external control.
- Conditions the memory address decoders to select programmed instructions or data words.
- Selects data and instruction memory sectors under program control.
- Selects instruction addresses within a memory sector either automatically or under program control by an instruction counter.
- Stores, decodes, and initiates operation codes.
- Interrupts the program, under external control, to perform selected subroutines of the program.
- Generates a word (HOP constant) which reinstates the computer program at the instruction where it was interrupted, after completion of an externally commanded subroutine.

The program control element consists of:

- An address register.
- Data and instruction sector registers.
- Operation code register and decoders.
- Interrupt and start-stop control circuits.
- Any automatic HOP save circuit.
- An instruction counter.

The address register stores instruction or data word addresses while the selected word is read from memory. During an instruction word time, the address register stores the instruction address (from the instruction counter) to select the instruction word address. The operand address portion of the instruction word, stored during data word time, is used to select the data word address.

The address register consists of 9 latches, A1 through A9, with associated AND and inverter output circuits for added driving power. Latches A1 through A8 select 1 of the 256 memory locations in a sector; latch A9 determines whether the addressed data will come from a pre-selected sector, or from the residual memory. The addresses of selected memory locations are loaded into the address register from the transfer register. The address register outputs condition the address decoders in the memory control element and provide control to the LVDA for PIO operations. The transfer address latch provides timing and control for the register.

The instruction address (from the instruction counter) is stored in the address register from A-8-W through A-13-X time. During this period, the addressed instruction is read from memory and placed in the transfer register. The operand address portion of the instructions is then transferred to the address register at A-13-Z time for storage while the data word is read from or stored into memory.

The address register stores the data word address from A-14-W through the following A-7-X time. The address register is reset at A-7-Y and A-13-Y times prior to storing the instruction and data addresses.

An EXM instruction executes and modifies the operand address of one of the instructions stored in residual memory locations 600, 640, 700, and 740. The operand address portion of the EXM instruction is transferred into the address register at A-13-Z time. The data stored in latches A1 through A5 remains in the transfer register to select the syllable of the instruction to be executed and modify its address. This data must be cleared from latches A1 through A5 to select the desired residual memory locations.

The data and instruction sector registers store sector codes to select 1 of 16 memory sectors during operation and instruction times, respectively. Sector codes are loaded into both registers during a HOP instruction (HOP sets CDSV to load the data sector register); the data sector register is also loaded during a CDS instruction. The registers store the sector codes until the next HOP (or CDS) instruction commands them to change. The sector register outputs condition the memory address decoders.

The 4-bit operation code register stores the code of the commanded instruction while the instruction is executed. The operation code register outputs control the operation of the circuits which execute the instructions.

The operation code register, loaded by the transfer register, stores the operation code from A-12-Y to A-5-Y time (nearly a full computer cycle).

The operation decoders supplement the operation code register in controlling the operation of circuits which execute the commanded operations. The operation decoders decode programmed operation codes and computer signal combinations to generate control signals. The programmed operation codes which condition the decoders are supplied via the transfer register, address register, or operation code register.

The instruction address is incremented in the arithmetic element and stored in the unused portion of the accumulator register. The instruction address consists of 9 bits but only 8 bits are stored in the accumulator register. When the instruction address is transferred to the address register from the accumulator register to select an instruction, a "0" is forced into address register bit A9 position. The instruction address is increased by one each instruction time during normal operation. The instruction address is not increased during an EXM instruction, during the first four computer cycles of a MPH operation, or after the commanded instruction is completed during a CST operation. The instruction address can be changed during a transfer operation; the instruction address currently stored in the accumulator register is dropped and the transfer instruction operand address is loaded into the unused portion of the accumulator register. The instruction counter is actually part of the arithmetic element.

The LVDC is programmed by means of single-address instructions. Each instruction specifies an operation and an operand address. Instructions are addressed sequentially from memory under control of the instruction counter. Each time the instruction counter is used, it is incremented by one to develop the address of the next instruction. After the instruction is read from memory and parity checked, the operation code is sent from the transfer register to the operation code register, a static register which stores the operation code for the duration of the execution cycle.

The operand address portion of the instruction is transferred in parallel (9 bits) from the transfer register to the memory address register. The transfer register is then cleared.

If the operation code requires reading the memory, the contents of the operand address are read 14 bits at a time (including parity) from the memory into the buffer register where a parity check is made. Data bits are then sent in parallel to the transfer register. This information is then serially transferred to the arithmetic section of the computer. If the operation code is a STO, the contents of the accumulator are transferred serially into the transfer register and stored in two 14-bit bytes. A parity bit is generated for each byte.

Upon completion of the arithmetic operation, the contents of the instruction counter are transferred serially into the transfer register. This information is then transferred in parallel (just as the operand address has previously been transferred) into the memory address register. The transfer register is then cleared and the next instruction is read. This completes one computer cycle.

The data word is read from the memory address specified by the memory address register and from the sector specified by the sector register. Data from the memory goes directly to the arithmetic section of the computer where it is operated on as directed by the operation code.

15.4.7 ARITHMETIC SECTION

The arithmetic section contains an add-subtract element, a multiply-divide element, and storage registers for the operands. Registers are required for the accumulator, product, quotient, multiplicand, multiplier, positive remainder, and negative remainder. The add-subtract and the multiply-divide elements operate independently of each other. Therefore, they can be programmed to operate concurrently if desired; i.e., the add-subtract element can do several short operations while the multiply-divide element is in operation.

The arithmetic element performs the following general type of operations:

- Arithmetic (addition, subtraction, and shifting)
- Logical extraction
- Stores new operand and a new instruction counter (previously described)
- Modifies the stored instruction counter

The arithmetic element consists of the following (Figure 15.4-9):

- Accumulator Control circuits (Accum Control)
- Add/Subtract circuit (A/S)
- Accumulator Register (Acc Reg)

The A/S circuit and Acc Reg make up an accumulator which performs the arithmetic and logic operations and stores the results. The Acc Reg stores 2 pieces of data: the results of the arithmetic operation (called the stored operand) and the instruction counter.

The Accum Control circuits provide timing and conditioning gates for the A/S and Acc Reg circuits. (The conditioning gates are instruction oriented.)

The A/S circuit performs the following arithmetic and logical extraction operations:

Addition	(ADD)	Arithmetic
Subtraction	(SUB)	
Reverse-Subtraction	(RSU)	
Clear-and-Add	(CLA)	
And	(AND)	Logical Extraction
Exclusive OR	(XOR)	

In each of the preceding operations only the stored operand and the new operand are affected.

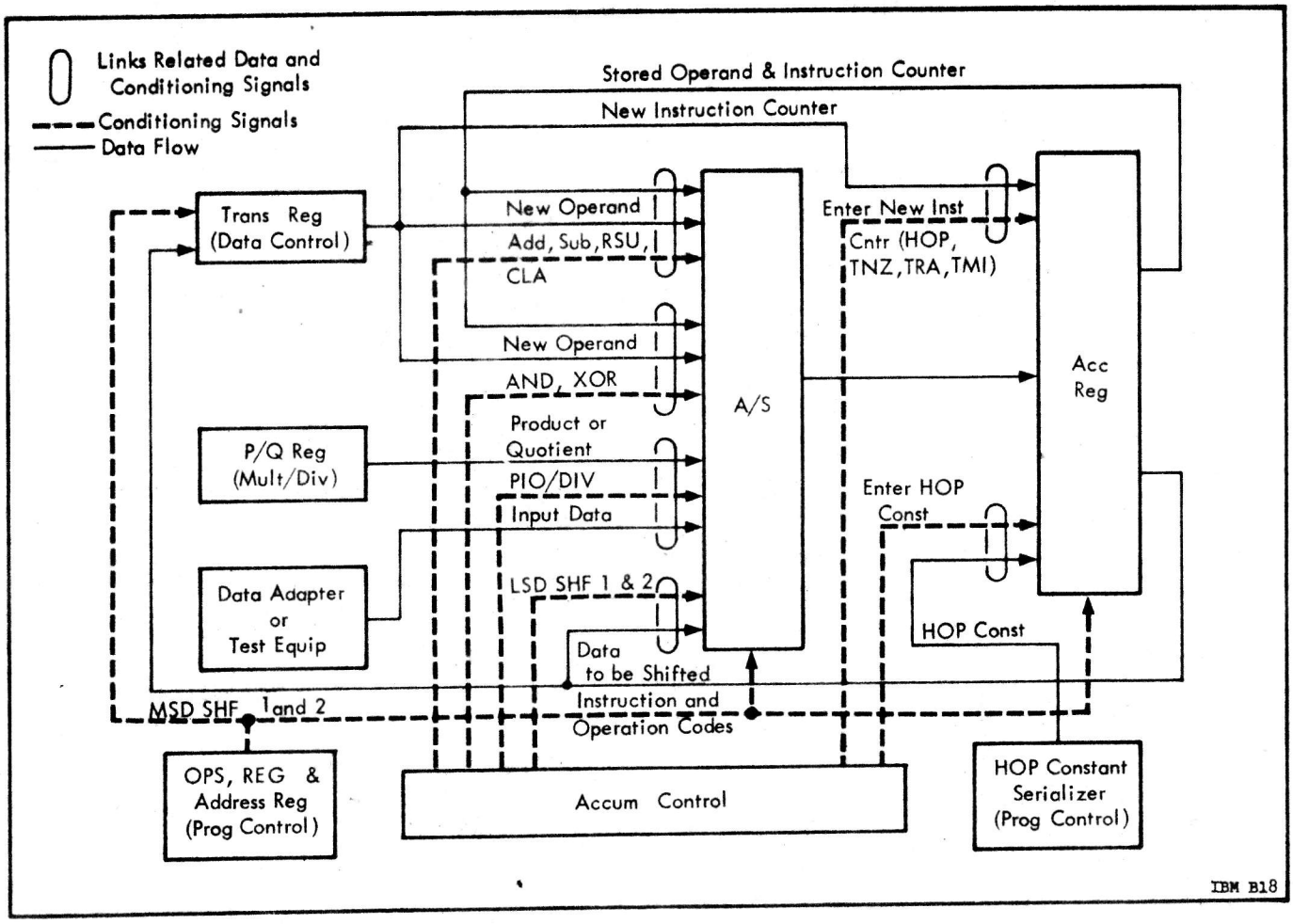


Figure 15.4-9 Arithmetic Element Block Diagram

(The instruction counter is recirculated and updated automatically, except during PIO operations.) During a CLA operation the stored operand is inhibited and the new operand enters the Acc Reg unaltered. Similarly, the product or quotient (from the multiply-divide element) and input data (from the LVDA or test equipment) enters through the A/S circuit and replaces the stored operand in the Acc Reg. During a SHF operation, the stored operand leaves the Acc Reg and returns early to the Acc Reg directly through the A/S circuit for an LSD shift 1 or 2; the stored operand leaves the Acc Reg and returns from the transfer register late for an MSD shift 1 or 2. MSD-shifted data from the transfer register enters the A/S as a new operand.

The Acc Reg is a circulating shift register which utilizes the A/S circuit to complete the loop. When no operations are called forth, the stored operand and instruction counter are continually circulated; the stored operand is unaltered and the instruction counter updated during each pass through the A/S circuit. A new instruction counter (required when performing one of the transfer operations) or a new instruction counter and HOP constant (which becomes the stored operand) may be entered directly into the Acc Reg when performing a HOP.

During each program cycle-time, the result of the simple arithmetic operations are circulated through the accumulator delay line and through the accumulator sync delay line channel to prevent processing of the results.

The multiply element operates in a 2-phase cycle, serial-by-four parallel, and requires 15 phase times, including instruction access time. The program initiates a multiply by placing the 24 high-order bits of the contents of the memory location specified by the operand address into the multiplicand delay line. The multiplier delay line contains the 24 high-order bits of the contents of the accumulator. The phase counter terminates a multiply instruction.

The instrumentation of the multiply algorithm requires 3 delay line channels. Two of the channels contain the partial product and the multiplier. These channels shift both the partial product and the multiplier 4 places to the right every 2-phase cycle. The third channel contains the multiplicand. The accumulator portion (fourth channel) of this delay line is not involved in the multiply operation and can be used concurrently with the multiply operation.

Upon initiation of a multiply and during every other phase time thereafter, the 5 low-order bits of the multiplier (MR_1, MR_2, MR_3, MR_4, and MR_5) are placed in latches or tratches and are used to condition addition or subtraction of multiples of the multiplicant to the partial product. The following algorithm is utilized for multiply:

$$P_i = 1/16 \left[P_{(i-1)} + \Delta 1 + \Delta 2 \right]$$

P_i is the new partial product, and $\Delta 1$ and $\Delta 2$ are formed according to the following rules:

MR_1	MR_2	MR_3	$\Delta 1$	--
MR_3	MR_4	MR_5	--	$\Delta 2$
0	0	0	0	0
1	0	0	+2M	+8M
0	1	0	+2M	+8M
1	1	0	+4M	+16M
0	0	1	-4M	-16M
1	0	1	-2M	-8M
0	1	1	-2M	-8M
1	1	1	0	0

M represents the multiplicand. For the first multiplication cycle $P_{(i-1)}$ and MR_1 are made zeros.

The divide element operates in a 2-phase cycle, serial-by-two parallel, and requires 27 phase times per divide, including instruction access time. The program initiates a divide by transferring the 26 bits of the addressed memory location (divisor) and the 26 bits of the accumulator (dividend) to the divide element. The phase counter terminates a divide operation.

The following algorithm is instrumented to execute divide:

$$Q_1 = R_{is} \cdot DV_s + \overline{R_{is}} \cdot \overline{DV_s} \qquad (1)$$

and

$$R_{i+1} = 2R_i + (1 - 2Q_i)\, DV \qquad (2)$$

where

$1 = 1, 2, 3, \ldots 24$

Q_i = The ith quotient bit

R_{is} = The sign of the ith remainder

DV_s = The sign of the divisor

R_i = The ith remainder

R_1 = The dividend

DV = The divisor

Equation (1) states that the ith quotient bit is equal to a "1" if the sign of the ith remainder is identical to the sign of the divisor. The high-order quotient bit (sign bit) is the only exception to this rule. Q_i as determined by equation (1) is used to solve equation (2) but must be complemented before it is stored as the sign bit of the quotient.

The instrumentation of the divide algorithm requires 3 channels of a delay line. One channel contains the quotient, one the divisor, and one the dividend. These 3 channels are used during multiply to contain the multiplier, the multiplicand, and the partial product respectively. The quotient and the remainder channels of the delay line have been lengthened by latches to shift 2 places to the left each 2-phase cycle. The divisor circulates once each 2-phase cycle.

In the two's complement number system, the high-order bit determines the sign of the number. Since this is the last bit read from memory, it is impossible to solve equations (1) and (2) until the entire divisor has been read from memory. However, equations (1) and (2) can have only two possible solutions.

Either,

$$Q_i = 1$$

and,

$$R_{(i+1)} = 2R_i - DV$$

or,

$$Q_i = 0$$

and,

$$R_{(+1)} = 2R_i + DV$$

Both the borrow of $2R_i - DV$ and the carry of $2R_i + DV$ are generated as the dividend and divisor registers are loaded. When the sign bits of these quantities are finally entered into their respective registers, equation (1) is solved for the first quotient bit. If this quotient bit is a one, the borrow is examined to determine the second quotient bit. If the first quotient bit is a zero, the carry is examined to determine the second quotient bit. The following truth table is solved to determine the second quotient bit if the first quotient bit is a one.

R_i	DV_s	B	$R_{(i+1)s}$	Q
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Where

R_i = The first remainder bit to the right of the sign bit

DV_s = The divisor sign

B = The borrow into the R_i, DV_s position

$R_{(i+1)s}$ = The sign of the new remainder

Q = The quotient bit as determined by comparing DV_s with $R_{(i+1)s}$ according to equation (2)

$$Q = \overline{R_i}\,\overline{DV_s}\cdot\overline{B} + \overline{R_i}\,DV_s\,\overline{B} + R_i\cdot\overline{DV_s}\cdot B + R_i\cdot DV_s\cdot B$$

$$= \overline{R_i}\cdot\overline{B}\,(\overline{DV_s} + DV_s) + R_i\cdot B\,(\overline{DV_s} + DV_s)$$

$$= \overline{R_i}\cdot\overline{B} + R_i\cdot B$$

The equation used in generating the new remainder, R_{i+2}, is obtained by expanding equation (2) as follows:

$$R_{(i+2)} = 2R_{(i+1)} + \left[1 - 2Q_{(i+1)}\right] DV$$

$$R_{(i+2)} = 2\left[R_i + (1 - 2Q_i)\,DV\right] + \left[1 - 2Q_{(i+1)}\right] DV$$

$$R_{(i+2)} = 4R_i + 2\,(1 - 2Q_i)\,DV + \left[1 - 2Q_{(i+1)}\right] DV$$

As $R_{(i+2)}$ is being generated, the next iteration of divide is started by generating, as already described, the borrow and carry for $2R_{i+2} \pm DV$.

No dividend register is described because it is considered to be the first remainder. Both multiply and divide operations require more time for execution than the rest of the computer operations. A special counter is used to keep track of the multiply-divide progress and stop the operation when completed. The product-quotient register has been assigned an address and is addressable from the operand address of the instructions SUB, AND, ADD, XOR, STO, RSU, and CLA. (Refer to Table 15.4-2 for a description of instruction codes.) The answer will remain in the product-quotient register until another multiply-divide is initiated.

Ultrasonic delay lines are utilized for short term storage. The delay medium is zero temperature-coefficient glass. One bit of information is a 0.2-microsecond pulse which propagates through the delay medium at the speed of sound in the medium. Ceramic transducers are used for energy conversion. Glass delay lines provide very reliable and stable short-term storage along with simple instrumentation.

The maximum data rate of the delay line in this computer is 2 megahertz. Thus, only one delay line, delay line driver, and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier, is easily implemented by gating the driver input and sense amplifier output with the four computer clocks.

The delay line input is actually provided by the delay line clock output of the clock generator and the delay line driver acts only as a logic gate. This scheme helps to increase the read-out timing margin and greatly simplifies the delay line driver circuitry.

SECTION 15.5

DESCRIPTION OF

THE LAUNCH VEHICLE DATA ADAPTER

15.5.1 GENERAL CHARACTERISTICS

The Launch Vehicle Data Adapter is the input/ output device for the Launch Vehicle Digital Computer and the central station for the signal flow in the Saturn Astrionics System.

The LVDA includes the following circuits:

- Various registers for buffering input and output signals.
- Delay lines for real time, accumulating accelerometer pulses, storing interrupts, line interrupt counters, and switch selector interrupt counters.
- Power supplies for the LVDA and LVDC.
- Digital-to-analog and analog-to-digital converters.
- Redundancy checkout circuit including channel switching, discrete output switching, and power supply switching.

The LVDA transforms input and output signals to a form that is compatible with the characteristics of the receiving equipment, controls the data flow in the IU, performs certain simple computation and logical operations on data, and provides temporary storage of data.

Communication with the computer is carried out through 512-kilobit per second serial transmission. The PIO instruction permits the specification of either input or output operations and addresses the device to be affected. A single 26-bit word is transferred to the computer accumulator or from the accumulator or memory.

The characteristics of the LVDA are listed in Table 15. 5-1.

15.5.2 DATA ADAPTER INPUT/ OUTPUT SIGNALS

The interconnections between the LVDA and the LVDC are shown in Figure 15. 5-1. Connections between the LVDA and equipment in the IU may be seen in Figure 15. 5-2.

The LVDA accepts discrete input signals from the stage Switch Selectors, IU Command Receiver, ground launch computer, Telemetry Computer Interface Unit, Telemetry Data Multiplexer, Control Distributor, and other vehicle equipment. It has output registers to provide discrete output signals to the above mentioned equipment. It also accepts and processes LVDC interrupt signals from the ground launch computer and the IU equipment.

The LVDA accepts 2-phase resolver analog signals from the ST-124M Inertial Platform Assembly and converts these signals to a digital number proportional to the electrical rotation of the resolver. It accepts and accumulates incremental velocity inputs from gray code incremental encoders on the platform accelerometers and converts digital signals to analog signals for use in the Flight Control Computer.

The LVDA interface has been standardized as much as possible. Digital inputs and outputs will be 0 and 28 Vdc, except for inputs from the optisyns, telemetry transmitter, and Computer Interface Unit. The signal characteristics, along with the input and output circuits, are listed in Table 15. 5-2.

Table 15.5-1 Data Adapter Characteristics

Item	Description
Computer input-output rate	512 kHz serial
Power supplies	6 duplexed regulated dc supplies 2 ac resolver power supplies
Switch Selector	8-bit Switch Selector input 15-bit Switch Selector output
Discretes	7 interrupt inputs from the IU 13 discrete outputs 32 discrete inputs
Buffer register Tab register Mode register	26 bits 8 bits 6 bits } Provide communication with the RCA-110 Ground Control Computer, telemetry transmitter, and DDAS
Digital-to-analog converter	8 bits plus sign, 2.5 millisecond operation, three attitude commands, and two spare outputs
Analog-to-digital converter	Equivalent of 17 bits from a 2-speed resolver
Platform	4 two-speed gimbal angle resolver inputs
Spares	10 single-speed resolver inputs
Delay lines	3 four-channel delay lines for normal operations 1 four-channel delay line for telemetry operations (DOM)
Telemetry	
Command Receiver data transmitter	14 bits for input data 38 data and identification bits plus validity bit and parity bit
Computer Interface Unit	15 bits address plus a data request bit for output data 10 bits for input data plus data ready interrupt
Output to launch computer	41 data and identification bits for output data plus discrete outputs
Input from RCA-110 Ground Control Computer	14 bits for input data plus interrupt
Number of components (estimated)	38,000 silicon semiconductors, cermet resistors, and other special components
Reliability	0.99 probability of success for 250 hours of operation; uses TMR logic, duplex special circuits, duplex power supplies
Packaging	125 electronic page assemblies, plus special electronic assemblies
Weight	80 kilograms (214 pounds)
Volume	0.1 cubic meter (3.6 cubic feet)
Power (without computer)	320 watts

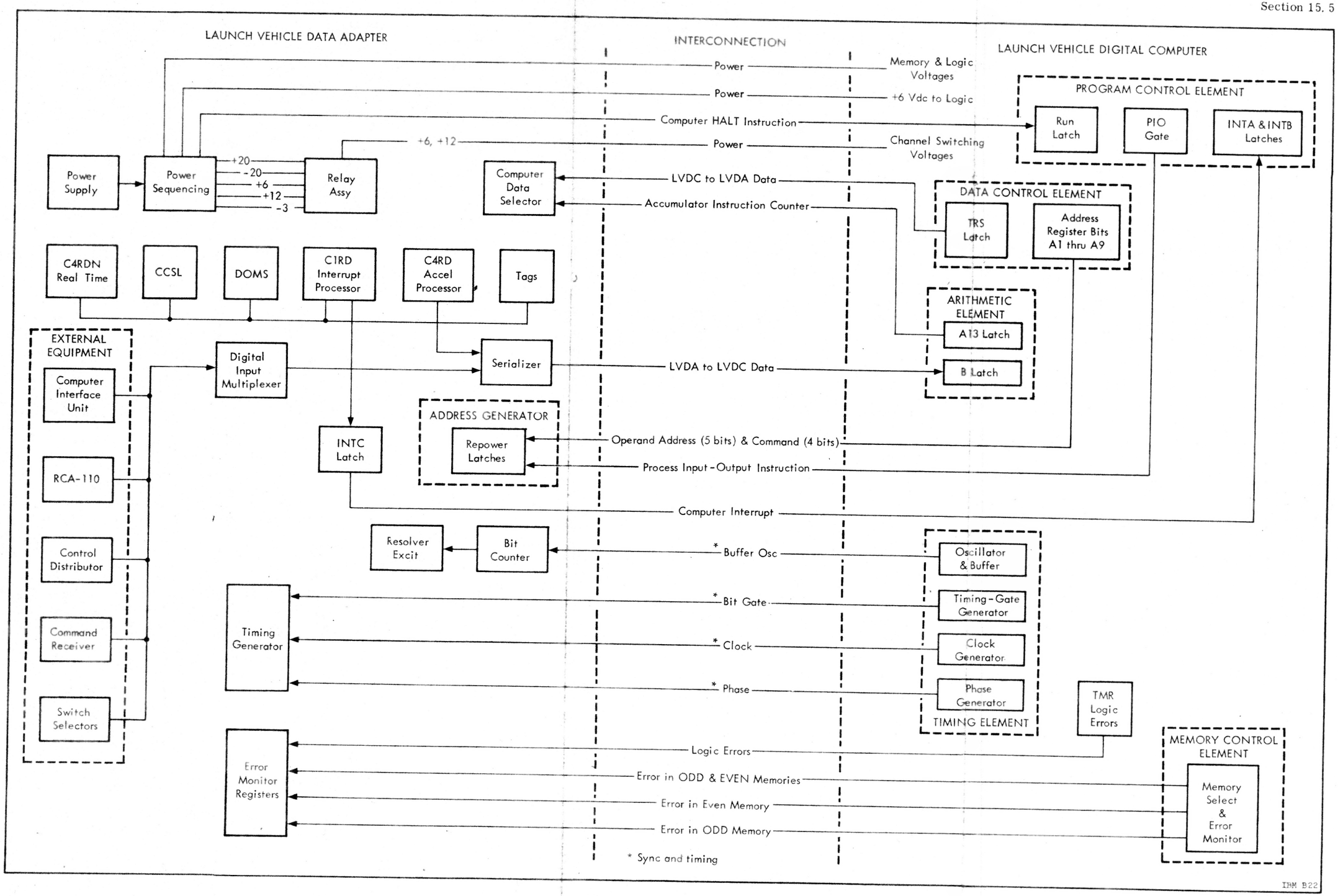


Figure 15.5-1 LVDA-LVDC Interconnection Block Diagram

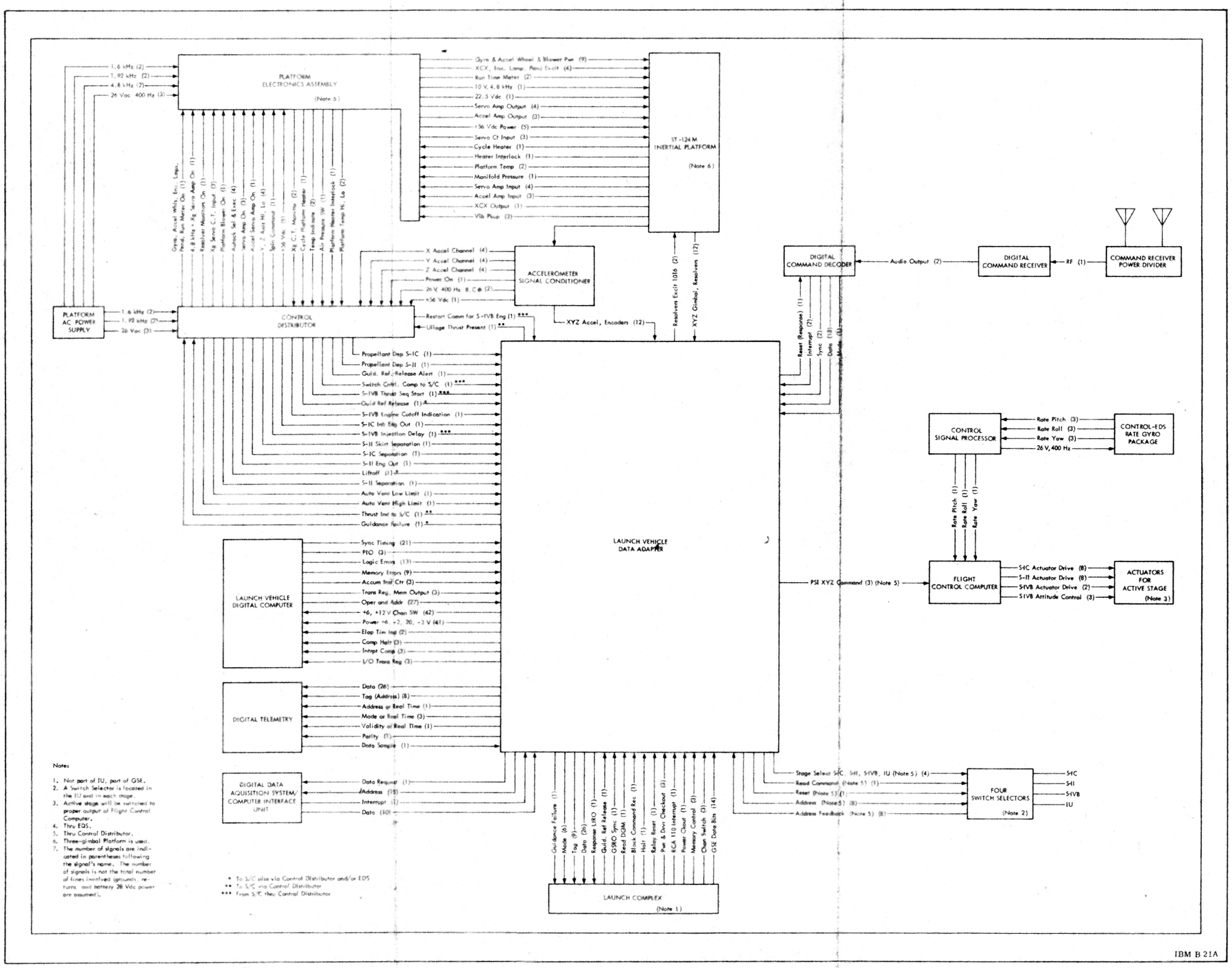


Figure 15.5-2 LVDA-IU Equipment Interconnection Block Diagram

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Timing Generator. The timing generator is TMR and generates timing gates for the LVDA circuits as follows:

- Each word time is approximately 82 microseconds in duration and is divided into three phase times of equal duration.
- Each phase time is approximately 27.3 microseconds in duration and is subdivided into 14-bit times of equal duration. The subdivision is accomplished by eight timing gates.
- Each bit time is approximately 1.95 microseconds duration and is subdivided into four equal clock times of 0.488 microsecond duration.

The timing generator receives four clock pulses, one bit gate, and one phase gate per TMR channel, as synchronizing signals from the LVDC.

Internal Control Discrete Register. Certain functions within the LVDA must be controlled by the LVDC. A 13-bit register, very similar to the discrete output register, is included to provide these controls.

Some of the functions of these discretes are:

- Control switching of duplex delay line channels.
- Selection of the duplex analog output channels to be used.
- Selection of coarse resolvers as backup of fine resolvers.

This register is so constructed that the state of any output can be changed without momentarily or permanently affecting the state of the other outputs.

Discrete Inputs. Discrete inputs are signals which do not require storage within the LVDA. The LVDA is designed to handle 32 of these inputs. The LVDC reads the discretes periodically and performs the necessary program steps.

Examples of discretes are:

- A signal from the Control Distributor indicating vehicle stage separation.
- A signal from the Spacecraft indicating a command to start the thrust sequence of the S-IVB Stage.

The discrete signals will be read in through the digital input multiplexer which is TMR. Groups of these discrete inputs are treated as words by the LVDC – one 24-bit word and one 8-bit word. Each word is read by the LVDC as requested by a PIO address.

Digital Input Multiplexer and Serializer. The digital input multiplexer accepts and serializes parallel digital input words. The word that is to be serialized will be selected by a PIO command from the LVDC. The selection of the word is determined by the configuration of the nine address bits accompanying the PIO instruction from the LVDC. The input selected is serialized at a 512-kilohertz rate and is fed to the LVDC accumulator.

The digital input multiplexer is connected with the following equipment:

Computer Interface Unit
Ground Computer
Control Distributor
EDS Distributor
Command Guidance Receiver
Switch Selectors

The digital input multiplexer also provides temporary storage of real time and gating signals from the TMR delay line and the crossover detector counters to the LVDC accumulator.

Channel Switching. To check the individual channels within the TMR logic sections of the LVDC and the LVDA, both in the laboratory and on the launching pad, a means of evaluating each channel separately will be provided. The channel-switching function will be under the control of external ground support equipment or the laboratory test equipment. Signal lines from this control equipment will operate the LVDA relays, which control bias voltages on the 3 channels of voters in the LVDC and LVDA, allowing TMR or simplex operation.

15.5.4 POWER SUPPLIES

The LVDA contains six duplexed dc power supplies and one pair of ac resolver supplies. It can tolerate supply voltage transients of ±50 volts, 1 millisecond half-period duration.

The pulse-width modulated duplex power supplies provide regulated dc power to the LVDA and LVDC by means of a dc-to-dc converter, from the vehicle +28 Vdc supplies.

Table 15.5-2 Signal Characteristics

Signal Name	Signal Characteristics	Internal Load Impedance (kilohms)	External Load Resistance to Ground	Design Goals	
				Rise	Fall
Resolver excitation	26 V ±5% rms at 1016 hertz 12 volt-amps at 0.9 power factor drive per excitation	17.3			
Inputs from resolver secondaries	5 V±8% rms at 1016 hertz	20.9			
Ladder outputs	+12.24 to -12.24 Vdc		6k (min); <0.1 μf		
Inputs from Command Receiver	Down level: 0±8 Vdc* Up level: + 24±8 Vdc	≥10			
Switch Selector feedback	Down level: 0±8 Vdc* Up level: + 24±8 Vdc	≥10			
Inputs from ground computer	Down level: 0±8 Vdc Up level: + 24± 8 Vdc	≥10			
Discrete inputs	Down level: 0±8 Vdc Up level: + 24±8 Vdc	≥10			
Interrupts from IU except DDAS	Down level: 0±8 Vdc* Up level: + 24±8 Vdc	≥10			
Inputs from Computer Interface Unit	Down level: 10 mA="0" Up level: 0±50 μA="1"	≥2			
DOM sync pulse from telemetry	Down level: 0 ± 1 Vdc Up level: 7.0 ±1.0 Vdc 100 us duration rep rate 240/s ± 5% evenly spaced	≥10			
Inputs from optisyns	Down level: 0±1 Vdc Up level: 7.0±1.0 Vdc	≥50			
Switch Selector outputs					
Reset and read command drivers	Down level: ** Up level: ≥21.5; ≤29.7 Vdc		≥ 75Ω ≤ 0.045 μf	≤0.1 ms	≤1 ms
Stage drivers	Down level: ** Up level: ≥ 21.5; ≤29.7 Vdc		≥ 122Ω ≤ 0.045 μf	≤0.1 ms	≤1 ms
Address drivers	Down level: ** Up level: ≥ 22.5; ≤29.7 Vdc		≥ 270Ω ≤ 0.0225 μf	≤0.1 ms	≤1 ms
TDL drivers to CIU & telemetry transmitter	Down level: 0±2 Vdc Up level: ≥22.5; ≤29.7 Vdc		≥ 2.5k≤100k ≤ 0.005 μf	≤ 5 μs	≤ 50 μs

Table 15. 5-2 Signal Characteristics (Cont)

Signal Name	Signal Characteristics	Internal Load Impedance (kilohms)	External Load Resistance to Ground	Design Goals Rise	Design Goals Fall
Command Decoder	Down level: 0±2 Vdc Up level: ≥22. 5;≤29. 7 Vdc		≥1. 7k ≤ 0. 005 μf		
SDL drivers to telemetry transmitter	Down level: 0±2 Vdc Up level: ≥22. 75;≤29. 7 Vdc		≥1. 5k ≤0. 00375 μf	≤5 μs	≤50 μs
SDI, SDL, SDH drivers to ground computer	Down level: ** Up level:≥23;≤29. 7 Vdc		SDI≥1. 125 k ≤0. 045 μf SDL≥1. 5k ≤0. 045 μf SDH 300Ω ≤ 0. 045 μf	≤0. 1 ms	≤1 ms
TDM discrete outputs	Down level: ** Up level: ≥ 21. 5;≤29. 7 Vdc		≥122Ω±10% ≤0. 0375 μf	***	***

* or open.
** Output current at down level is equal to 0 ±100 μA
*** Not determined.

15.5.3 CIRCUITS AND FUNCTIONS IN THE LVDA

Typical functions performed in the LVDA are the following:

Category I — Control data flow, including temporary storage.

Category II — Transform data into a form which is compatible with the characteristics of the receiving equipment.

Category III — Perform certain simple computational and logical operations on the data.

The following functions are typical of those included in Category I:

- The storage of telemetry data from the LVDC and LVDA in the buffer registers.
- The temporary storage of CIU addresses during orbital checkout.
- The transmission of guidance data from the LVDC to the analog Flight Control Computer.

Operations which require a change in the form of the data include (typical of those in Category II).

- Digital-to-analog, analog-to-digital, and signal level conversions.
- The formation of 40-bit launch computer and telemetry words from 26-bit LVDC words.
- Buffering of communications between the LVDC and the ground-based launch computer to reconcile the difference in clock rates.

The LVDA contributes to the efficient operation of the LVDC by performing many simple, though time-consuming, logical and computational tasks, such as (typical of those functions performed in Category III):

- Keeping track of real time.
- Decoding of operand address in PIO operations.

CIRCUIT DESCRIPTIONS

For the following description of various circuits in the LVDA, refer to Figure 15.5-3.

Delay Lines. The LVDA contains four glass delay lines which serve as temporary storage. The delay lines will be connected together as follows:

- Three delay lines are used in a redundant manner for normal LVDA operation.
- One delay line is used for telemetry operations.

The triple modular redundant delay line is organized around the LVDC timing such that the information it contains remains synchronized with the LVDC operation cycle. The total circulation time of the delay line and its associated electronics is equal to the basic LVDC operation cycle time of 81.9 microseconds (42-bit times). The delay line is divided into three 14-bit word times corresponding to the three LVDC phase times. Furthermore, the four clock times into which each LVDC bit time is divided are used to time-share the delay line among 4 "channels" of 512-kilohertz serial information. Hence, twelve 14-bit words can be stored in a single delay line by operating the line at a 2.048-megahertz rate. Table 15.5-3 illustrates how these word locations are used.

In performing a PIO operation, the LVDC sends out or looks for information only during phase B and C times. Real time is assigned to a phase A word time to facilitate the use of real-time information in the data output multiplexer. However, real time is made available to the LVDC during phase B via the digital input multiplexer register and the serial latch.

The velocity accumulations, which are the processed outputs of the accelerometer optisyns, are arranged to provide duplex redundancy, matching the duplexed optisyns. One line contains outputs Z_1 and X_2, another X_1 and Y_2, and a third Y_1 and Z_2. When the LVDC calls for a given velocity accumulation, it receives the processed output of one of the optisyns on the selected accelerometer during phase B and the outputs of the other optisyns on the same accelerometer during phase C. These 2 values are processed separately in the LVDC such that any one of the delay lines or any optisyn could fail without failing the system.

The real-time accumulation is voted upon in TMR voters during every circulation; thus the values in all 3 lines will always agree. The duplex operation of the accelerometer processors does not allow voting, so there is no guarantee that the absolute value of the 2 readings will agree. Real time is accumulated in 246.1-microsecond increments, while the least significant bit in the velocity measurement has a weight of 0.05 meter per second.

The delay line channels with data written at X (channel 3) and W (channel 2) clock times are used to time two of the functions in the computer program. Both of these functions occur during phase B. Time-to-go until the next LVDC interrupt for Switch Selector operations is counted down in channel 2. Time remaining before the start of the next minor loop is counted down in channel 3. These 2 countdowns occur at a rate of one count every 492.2 microseconds, and will generate an interrupt when they pass through zero. The length of the count will be determined by the LVDC,

Table 15.5-3 Use of Word Locations in the Delay Line

Channel Number	Write Time	Phase Time			Digital Computer Use
		Phase A	Phase B	Phase C	
1	Z clock	Spare	Spare	Interrupt storage	Read channel
2	W clock	Spare	Switch select or interrupt countdown	Interrupt limiting	Write channel
3	X clock	One-millisecond countdown	Minor loop interrupt countdown	Interrupt inhibit	Write channel
4	Y clock	Real-time accumulation	Velocity accumulation Z_1, X_1, or Y_1	Velocity accumulation X_2, Y_2, or Z_2	Read channel

which loads a value of time-to-go to initiate each count. Also, during phase A of channel 3, a 0.8-millisecond delay for use in the digital-to-analog converter is generated by counting 10 circulations of the delay line.

LVDC interrupts are stored during phase C of channel 1. Once the LVDC recognizes an interrupt, it will set the corresponding bit in phase C of channel 2, and will reset this bit in channel 1. The associated circuit will prevent a new interrupt from being recognized in this bit position until the previous interrupt has disappeared. The only constraint, therefore, on the length of the interrupt signal will be that it must last for at least 81.9 microseconds, the circulation time through the delay line and associated circuits. Interrupts may be stored without being recognized by setting the corresponding bits in phase C of channel 3.

Channel 1 may be conveniently read by the computer, while channel 2 may be conveniently written into from the computer. As many as 3 of the normal 14 bits may be sacrificed if it is desired to use either of these 2 channels in the opposite manner.

Interrupt Register. As a means of notifying the LVDC that immediate attention be given to an external operation, an interrupt line is wired from the LVDA to the LVDC. The interrupt register (delay line) is capable of accepting 12 different signals and storing them until the LVDC has acted upon them. The signals are OR'ed together so that only one interrupt line to the LVDC is required. After an interrupt, the LVDC branches to a subroutine to read the interrupt register by means of a PIO operation. A computer analysis is then made, testing the highest priority bit positions first in case more than one interrupt signal is stored in the register. During this testing, the LVDC stores the contents of the memory address register and the instruction counter and branches to an interrupt subroutine. While in this subroutine, the LVDC does not recognize further interrupts. The next to last instruction of the testing the highest priority bit positions first in case more than one interrupt signal is stored in the register. During this testing, the LVDC does not recognize further interrupts. The next to last instruction of the interrupt subroutine is a PIO instruction addressed to the interrupt register to reset the particular bit causing the interrupt. The hardware provides a time delay to prevent further immediate interrupts from the same source. The source must disappear and return before another interrupt is honored from that source. This prevents slow-acting devices such as relays from regenerating interrupts while they are being activated by discrete outputs which occur during the interrupt subroutine. Each interrupt signal must be at least 84 microseconds in duration to assure storage in the delay line.

The LVDC is also capable of inhibiting the interrupt, as commanded by the program, with PIO instructions whenever the function of the subroutine warrants this precaution. Examples of interrupts are:

- An interrupt which is timed to ensure regular processing of guidance data;
- An interrupt from the CIU indicating that requested data are available.

Nine of the interrupt signals will be generated external to the LVDA and LVDC and three will be generated internal to the LVDA and LVDC.

Interrupt Circuits. The operation of the interrupt circuits is as follows. Upon receipt of an interrupt signal, the LVDA will insert a bit in a time slot reserved for this particular interrupt in a TMR delay line register called the interrupt storage register. When the bit is placed in the register, the LVDA signals the LVDC that an interrupt has been received. Upon receipt of the LVDA interrupt signal, the LVDC will read the interrupt register and determine which interrupt has been received. The LVDC will then insert a bit in the corresponding time slot in another delay line register, called the interrupt limiting register, to indicate that the LVDC has acknowledged that particular interrupt. The logic of the interrupt storage and inhibit registers will be so arranged that once a particular interrupt appears, at the LVDA interface and interrupts the LVDC, it will not be capable of causing another interrupt unless it disappears and reappears again. Another delay line storage register, called the interrupt inhibit register, is provided. When the LVDC places a bit in a particular time slot, this bit will prevent the corresponding bit in the interrupt storage register from interrupting the LVDC. Any combination of bits may be placed in the interrupt inhibit register.

Switch Selector Register. This register is loaded by the LVDC whenever the computer wishes to give commands to specific vehicle devices such as fuel valve controls. The register has a 15-bit storage capacity and is loaded by a PIO instruction. The register thus controls the outputs of 5 Switch Selectors located within the stages of the vehicle. The 15 bits are used as follows:

- Eight bits make up a relay code which is distributed in parallel to each of the 5 Switch Selectors.
- Five bits determine which Switch Selector will be activated (no more than 2 selectors may be addressed at once).
- One bit commands the assigned Switch Selector to activate the device selected by the relay code.
- One bit resets all Switch Selector relays which were turned ON by the previously described bits.

The Switch Selector register contains both TMR and simplex circuits. The characteristics of the outputs are as follows:

- One reset output is TMR.
- One read output is TMR.
- Five stage-select outputs are TMR and capable of driving the stage-select input of one Switch Selector.
- Eight Switch Selector code outputs are simplex and capable of driving simultaneously 2 Switch Selector code inputs.

Switch Selector Feedback Inputs. When the Switch Selectors are operated as previously described, the relay tree feedback lines are tested to assure that the code was set properly by the LVDA. Eight lines from a separate set of contacts on the code relays contain the complement of the data word used to set the code relays. These lines are inputs to the LVDA which do not require storage and are addressed by the LVDA in the same manner as other discrete inputs. This feedback word is separated from the other discrete inputs so that the word may be processed more easily in the computer when comparing it with the word used to "set" the relay code.

Discrete Output Register. Certain functions within the vehicle, excluding those controlled by the Switch Selector register, are controlled by a 13-bit TMR discrete output register. An example of one function, which is controlled by the discrete output register, is a signal to the launch computer.

To ease programming requirements for changing specific discretes while not affecting others, the discrete output register is not loaded in the same way as the other registers. If certain discretes are to be activated, a PIO instruction is set up to address the "set" side of all latches in the register. Conversely, if certain discretes are to be deactivated, another PIO instruction selects the opposite or "reset" side of all latches in the register. The desired bits in the register are changed by placing "ones" in the corresponding bit locations of the data word transferred to the register from the LVDC, while the unchanged bit positions have "zeros" in the data word. Thus, the state of any output may be changed without momentarily or permanently affecting the state of the other outputs.

Buffer Register. The telemetry buffer register is a 26-bit storage register capable of providing 26 outputs in parallel. The register has 11 simplex bits and 15 TMR bits. It will be loaded by LVDC PIO operations or by the LVDA data output multiplexer. The register provides part of the interface required for transferring data to the telemetry data multiplexer and ground computer, and stores addresses for communication with the CIU. The CIU will be driven by the TMR portion of the register. Separate output drivers will be provided for driving the ground support equipment.

The output of the buffer register is provided in parallel to the telemetry multiplexer, the ground computer and the CIU. These systems read data from this register asynchronously with respect to LVDC timing.

Mode Register. The mode register is similar to the buffer register and other 1-word registers loaded by the LVDC. It provides storage for a 6-bit computer word which defines the computer mode of operation. While communicating with the launch computer, these 5 outputs are read in parallel by the launch computer. The telemetry data multiplexer reads three of these outputs when transmitting computer telemetry words, but real-time information data is substituted for these bits when LVDA data is transmitted. A PIO instruction loads the mode register from the LVDC. Three of the bits are loaded into the mode/real time register whenever the LVDC loads telemetry data into the buffer register. All six of the bits are transmitted to the ground computer or other ground support equipment through separate line drivers.

Tag Register. The 8-bit tag register is used to transmit identification bits for data being sent from the buffer register to the ground launch computer and to the telemetry data multiplexer.

Mode/Real-Time Register. The 5-bit mode/real-time register performs the following functions:

- When data is loaded into the buffer register from the LVDC, the mode/real-time register contains one validity bit, three mode bits and one address bit.

- When data is loaded into the buffer register from the LVDA data output multiplexer, the mode/real-time register contains 5 bits from the real time counter in the LVDA (except during time error identification operation at which time it will contain 5-bits from the real time counter). All outputs of this register are transmitted to the telemetry data multiplexer. The real-time/address bit is transmitted to the ground launch computer.

Validity Bit Generator. Since the telemetry data multiplexer addresses the LVDA asynchronously with respect to LVDC timing, it is possible for telemetry words to be read while they are being changed by PIO operations. However, data read at this time are invalid. Therefore, a signal must be included in the telemetry word which indicates the validity of the word. The validity bit generator performs this function. Data are invalid any time the computer mode register, tag register, and buffer register are being loaded.

The validity bit generator is a 1-bit simplex register which is turned ON whenever LVDC telemetry data is being loaded into the buffer register. This bit shares a bit position in the mode/real-time register with one of the real-time bits.

Data Request Generator. The LVDA has a 1-bit TMR data request generator as an output to the CIU. The presence of this bit informs the CIU that an address for it is in the buffer register. The bit is turned OFF by an interrupt from the CIU.

Parity Generator. To ensure that LVDC data sent out over the radio frequency telemetry link to ground equipment is received without error, a parity bit is included in each 40-bit data word sent out by the LVDA.

The telemetry data word is formed from 3 subwords plus a validity bit. The validity bit however, is not included in the parity check. Odd parity is used. This means that, excluding the validity bit, all the "ones" in the 3 subwords, plus the parity bit, add up to an odd number. The easiest way to generate total parity is to generate an individual parity bit for each subword. The three parity bits are then checked for total parity and a resultant parity bit is generated.

Ready-Bit Generator. During orbital checkout, the computer examines various parameters which are monitored by the telemetry system. The LVDC obtains one of these inputs by sending a CIU address to the buffer register. This 15-bit address is compared in the CIU address comparator. When comparison occurs, the telemetry word is stored in a 10-bit register which is read by the LVDA. Another line interrupts the LVDC to notify it that data are available.

Since the buffer register is continuously connected to the CIU address comparator, as well as the telemetry data multiplexer and the launch computer interface, it is necessary to indicate to the address comparator when the buffer register data are ready for comparison. This is the function of the ready-bit generator. The "ready-bit" is turned ON after the 15-bit address is loaded into the buffer register, under control of a special PIO instruction. The bit remains ON until after the address has been compared and the 10-bit data word has been stored; it is turned OFF by the line causing the computer interrupt.

Error Monitor Register. The error monitor register is a simplex register for storing disagreements between the inputs to the various voters in the LVDC and LVDA. It also stores some disagreements between the duplex circuits. The LVDA has the capability of addressing this register upon command from the LVDC through the data input multiplexer and telemetering it through the data output multiplexer. This register contains 26 bits.

Time-Error Identification. To ensure proper error identification, the computer program location, bit time, word time, and the source of error are telemetered.

Address Generator. During PIO operations, the LVDC must select a register in the LVDA which contains or receives the input-output data. The address of the selected register and the correct data are determined by the operand bits of the instruction word along with the PIO control lines from the computer. These functions are performed by the address generator. The address generator is TMR and decodes nine address lines from the LVDC upon receipt of a PIO instruction. The decoded address selects a register, or other circuit in the LVDA that the LVDC desires to send data to or receive data from.

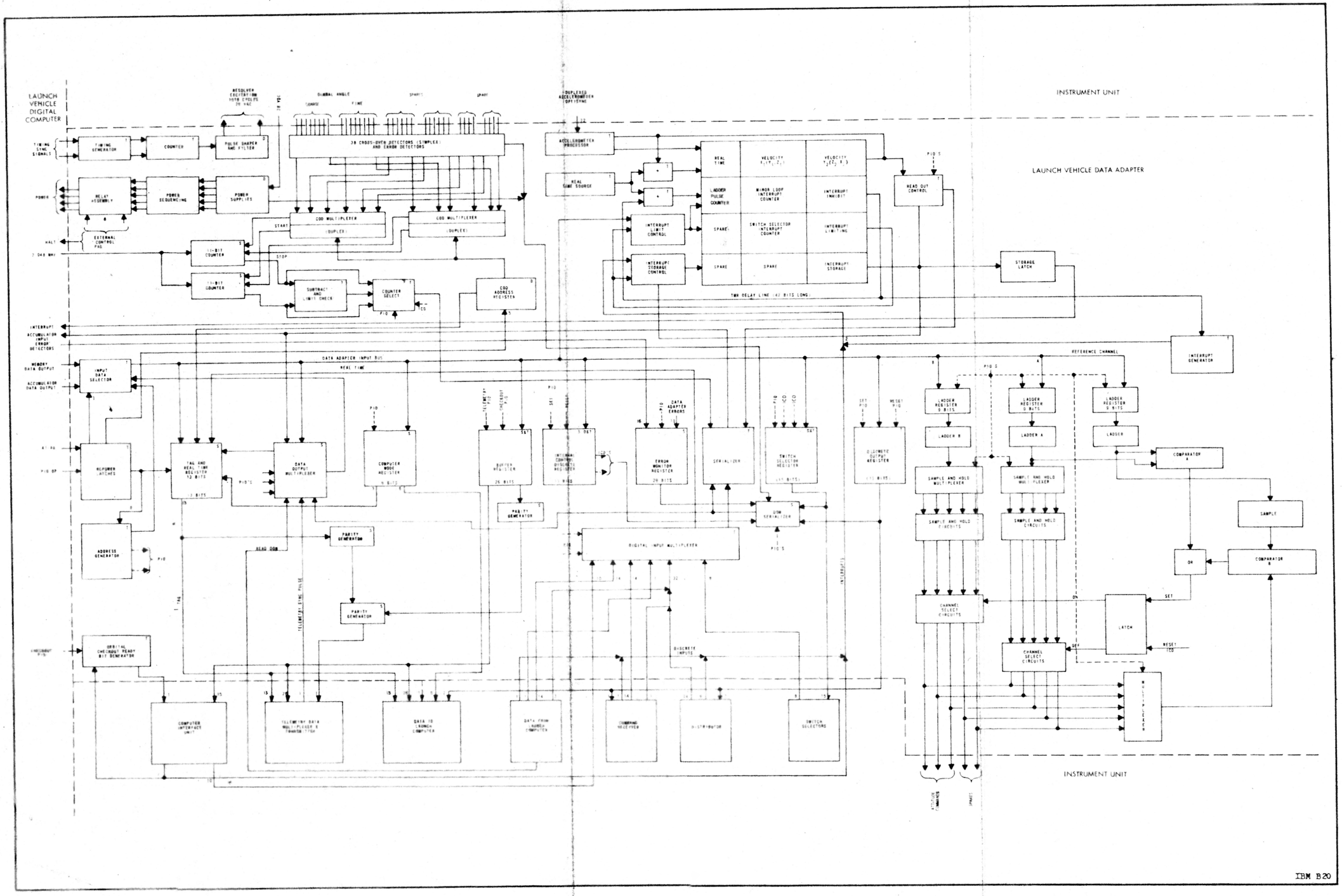

Figure 15. 5-3 Launch Vehicle Data Adapter Block Diagram

An example of a duplex redundant power supply is shown in Figure 15.5-4. Two regulated power supplies are connected in parallel. In each power supply, two feedback amplifiers are used in a duplex arrangement because they have the lowest reliability of the circuit. If one of the amplifiers fails, the isolation diodes allow the parallel amplifier to continue the regulation of the power converter. To further increase reliability, dc-to-dc power converters in the same duplex supply are connected to different +28 Vdc vehicle supplies. This allows one +28 Vdc vehicle supply to fail without a duplex supply failure. The regulated voltage supplies are: one +20 Vdc supply, one +12 Vdc supply, two +6 Vdc supplies, one -3 Vdc supply, and one -20 Vdc supply.

The ac power supply generates a well-filtered sine wave for excitation of various resolvers in the IU. The 1016-hertz frequency needed to drive the resolvers is obtained by counting down from computer timing pulses. This is accomplished with a 3-stage ring counter followed by a latch.

A variable clipper controls the amplitude of the 1016-hertz square wave obtained from the counter. The clipping level is set by level-sensing detector-amplifier circuitry. The fundamental component of the square wave is obtained by filtering, and is amplified to a 26-volt level which is adequate to drive the resolvers. The 26-volt level is maintained by an amplitude sensitive feedback circuit. The harmonic content is reduced by filtering. This filtering is accomplished by incorporating frequency selective feedback techniques in the amplifier circuitry.

The resolver frequency source is duplexed in a sense, i.e., each source supplies power for half of the resolver inputs in such a manner that fine and coarse resolver excitation for any input parameter is not supplied by the same source. Since fine and coarse inputs serve as a backup for each other (under the proper program control), duplex redundancy is used for the excitation source.

Associated with the power supplies are controls to:

- Provide channel switching (method of selecting one of the TMR channels for checkout) in the LVDA and LVDC.
- Provide power sequencing where required under ground equipment control.

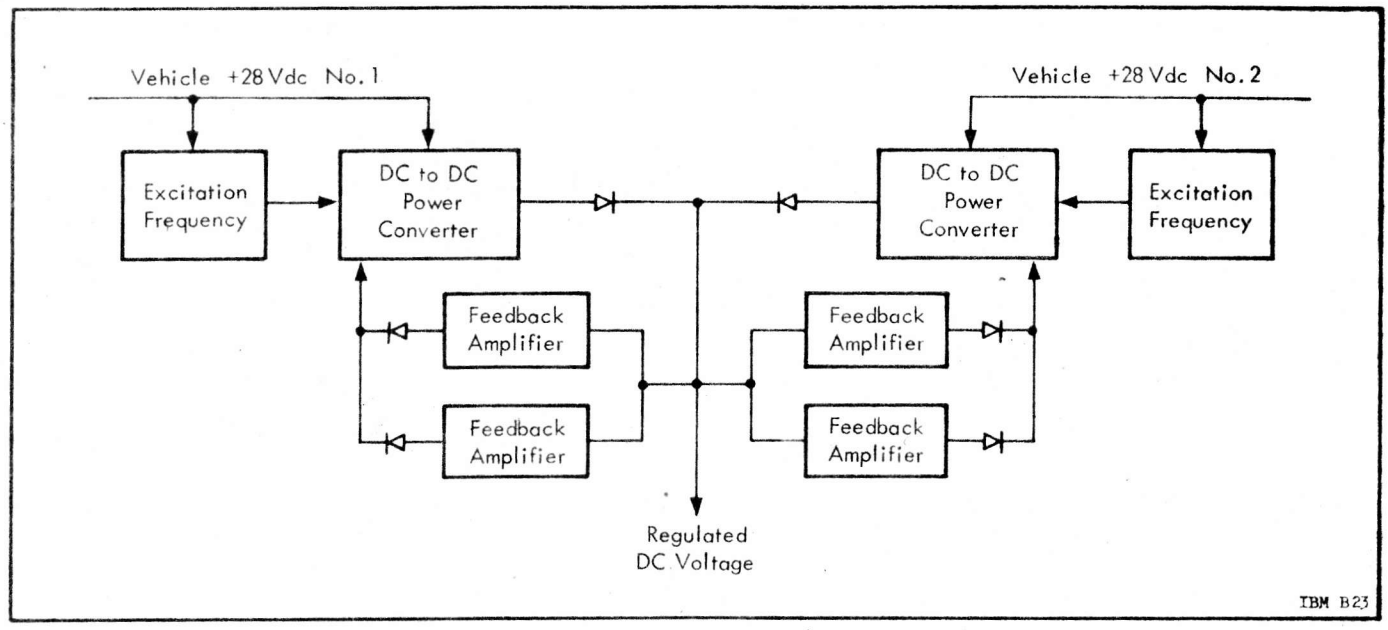

Figure 15.5-4 Redundant Power Supply Block Diagram

SECTION 15.6
INPUT-OUTPUT DATA PROCESSING

The solution to the navigation, guidance, and control problems of the Saturn Launch Vehicles requires processing of most input and output data by the LVDC/LVDA system. Generally, this processing is required for equipment compatibility, temporary data storage, and data transfer. There are six processing areas defined in the basic LVDC/LVDA scheme. These areas are:

- Gimbal angle processing
- Accelerometer processing
- Switch Selector processing
- Interrupt processing
- Telemetry processing
- Attitude command processing

Gimbal angle processing is an example of the complex processing required for data compatibility. The LVDA receives this data from the ST-124-M Inertial Platform Assembly (hereafter referred to as the Platform) in sinusoidal form and must then convert this intelligence to an acceptable digital form before the LVDC flight program can utilize it. The data is then stored within the LVDA until called for by the flight program. A PIO instruction then transfers the data to the LVDC.

The processing, which is detailed in the following paragraphs, is a combination of flight programming, timing, and LVDC/LVDA circuitry and logic The preceding sections in this chapter, as well as Chapter 11, will be helpful in understanding how this processing is accomplished and how the resultant input-output data is actually used by the flight program.

GIMBAL ANGLE PROCESSING

The pitch, yaw, and roll gimbal angles are measured by resolvers in the Platform. A dual resolver, coarse and fine, is used for measurement of each gimbal angle. The coarse ratio is 1:1, while the fine ratio is 32:1. Through electrical phase shifting, the two ratios are converted into three ratios - 1:1, 2:1, and 64:1. In the case of the 64:1 ratio, each mechanical rotation of the resolver shaft will cause 64 electrical rotations to occur. The three ratios are designated as coarse, backup, and fine, respectively. Since the fine gimbal reading is the most accurate, it is normally used in the processing scheme. The backup ratio, as its name implies, serves as a backup reading in case of malfunctions or errors. The coarse ratio is not used.

Figure 15.6-1 is a block diagram of a typical resolver system. The diagram incorporates the resolver located in the Platform and part of the LVDA circuitry. Two sinusoidal output voltages of the resolver secondaries are transmitted to an RC phase and shaping network in the LVDA. The waveforms are then sensed for their zero "crossover" points by 2 Crossover Detectors (COD's). The start COD output signal starts counters A and B at the zero crossover point of the positive going wave. The counters are stopped in the same manner by the output from the stop COD.

The overall flow diagram of the resolver signal processing is shown in Figure 15.6-2. Two identical 11-bit counters operate at the 2.048 MHz oscillator frequency. The two outputs are sent to the counter selector circuit, where one of the counters is selected, and its contents serialized and sent to the LVDC. The counter outputs are also sent to a subtract circuit where a difference is taken (A-B). If both counters are working properly, the difference (A-B) will be zero and either counter can be used. The limit checking circuitry is such that if the difference is within the limits of -4 and +3, either counter can be used. If the difference is greater than these limits, a disagreement bit will be set. The disagreement bit is part of the gimbal angle word placed in the accumulator when a gimbal angle PIO is issued. A decision must then be made as to which counter reading is correct. A comparison between individual counter readings and past readings is made by the flight program, and the best counter will be used. The checking process is repeated in hopes that both counters will work properly at the next reading. If a disagreement bit is set by three incorrect readings of the same angle during one computation cycle, the

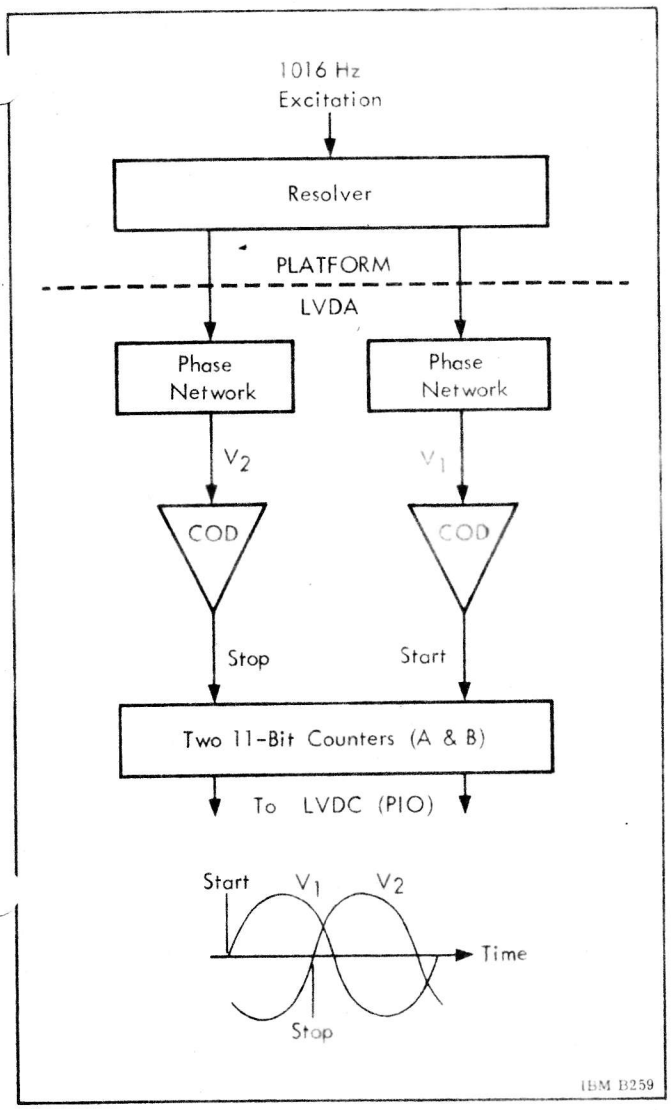

Figure 15.6-1 Resolver System Block Diagram

disagreement bit will be inhibited, and the good counter will be used throughout the remainder of the flight.

ACCELEROMETER PROCESSING

The Platform contains three accelerometers, which sense acceleration in each of the three (X, Y, and Z) orthogonal directions. Acceleration is indicated as a shaft rotation; the speed of rotation being proportional to acceleration. Since acceleration causes the accelerometer shaft to be displaced as a function of time, the shaft position (with respect to a zero reference) is proportional to velocity, and the accelerometer is referred to as an integrating accelerometer.

Each of the accelerometer shafts is linked to an optical encoding device called an optisyn. The optisyn converts the accelerometer shaft rotation to two pairs of sinusoidal signals, one pair is referred to as the direct channel and the other pair as the redundant channel. Each pair of signals consists of two sinusoidal waves approximately 90 degrees out of time phase. These signals are passed through the Accelerometer Signal Conditioner for wave shaping purposes before being received by the LVDA. Chapter 14 contains detailed information on the accelerometer assembly and the Accelerometer Signal Conditioner.

The LVDA, by means of accelerometer porcessor logic, receives the velocity information from the optisyns and converts it into a form that can be utilized by the LVDC. The LVDA accumulates velocity as measured by the Platform, and the LVDC attempts to detect velocity errors through reasonableness tests.

Each pair of signals generated by the optisyns appears at the LVDA as two voltages displaced in time as shown in Figure 15.6-3. The frequency of these square waves is directly proportional to the change in velocity sensed by the accelerometer. The LVDA tests the voltage level of each signal every 82.03 microseconds. As illustrated in the figure, there are four unique combinations of voltage levels definable at the times t_1, t_2, t_3, and t_4. The resulting code progresses in a positive direction as follows: 01, 00, 10, 11, 01, etc. It should be noted that this code does not progress in the same manner as a true binary code: 00, 01, 10, 11, 00, etc. Instead, it changes only one bit at a time, and is called a reflected binary code. (The term "gray code" is also used.)

The LVDA recognizes changes in the optisyn output signals as increments in velocity. The frequency of the square waves is 1500 cycles per accelerometer head revolution. Therefore, one revolution of the accelerometer head presents 6000 increments of velocity. Since the accelerometer integrates acceleration at the rate of 300 meters per second in one revolution, the resolution of the system is 0.05 meters per second for each increment.

An optisyn cycle is a progression through all the bit configurations that the optisyn can generate before it begins to repeat itself. Since the range of optisyn cycles (velocities) attained will be large, it is necessary to provide a means of counting and storing the number of optisyn cycles for processing by the LVDC. The count and store functions are provided in the LVDA by three duplexed accumulators called accelerometer processors. These processors consist of channel 4 of each of the three TMR delay lines, and the associated logic circuitry. The storage

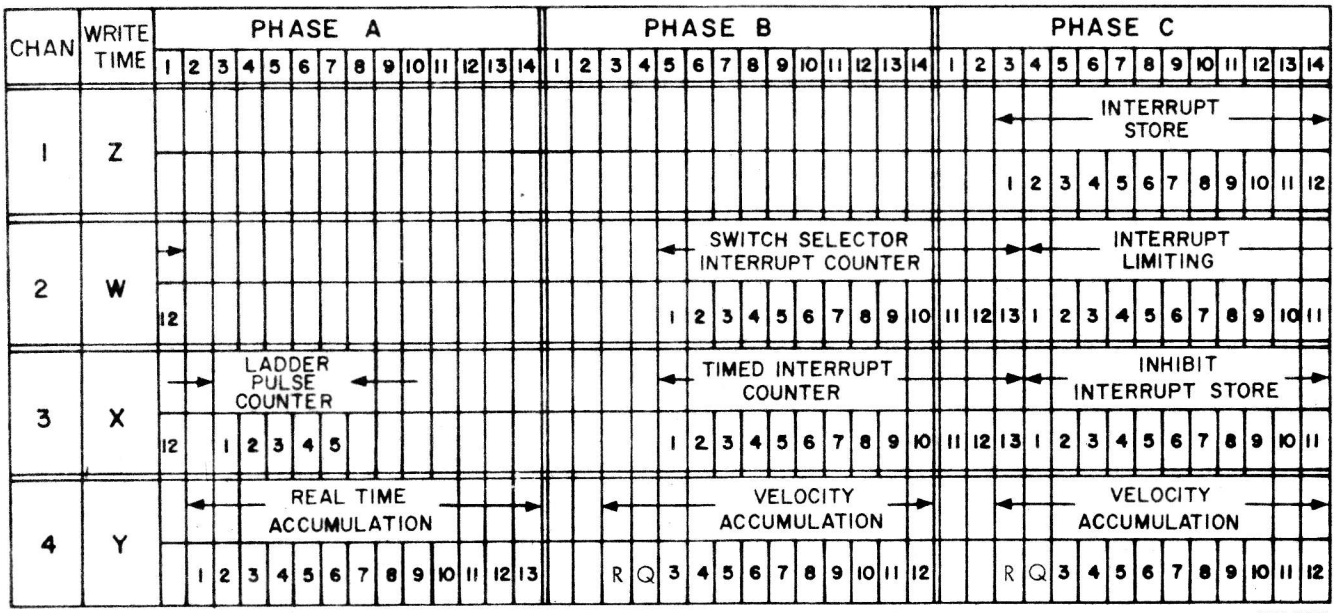

Figure 15.6-4 TMR Delay Line Configuration

sensed, a "1" is added to the 10 high order bits. Conversely, if completion of a negative cycle was sensed, a "1" is subtracted. The 10 high order bits are left unchanged if an optisyn cycle has not been completed.

SWITCH SELECTOR PROCESSING

The Saturn V system utilizes the computing system for control of mode and sequence of functions in all stages. The Switch Selector provides the communications link between the LVDC/LVDA (through the control distributor), the IU, and each stage. The Switch Selector is the device that has direct control of functional operation of the equipment on each stage. The sequencing scheme has the capability of selecting five Switch Selectors in the Saturn Vehicle – one per stage, one for the IU, and one spare (see Figure 4.2-1). Control of the individual units is commanded by the LVDC.

Each operation of the switch selectors and the processing components requires a PIO instruction word from memory in accordance with the stored program. At the proper point in the program, the computer will issue commands to initiate and operate the Switch Selector sequencing. These instructions will utilize increments of 15-bit Switch Selector computer words by transferring these bits to the LVDA from either the accumulator or a location in memory (through the transfer register). The 15-bit word is divided as follows: 5 bits for stage addressing, 8 bits for commanding an operation within that stage, 1 read bit, and 1 reset bit. The 15-bit Switch Selector register output is applied to each of the Switch Selectors. To increase the reliability of the operation, a two-way communication between the LVDC/LVDA and the Switch Selectors has been established. The LVDC/LVDA transmits command data to the Switch Selector and the Switch Selector transmits the complement of the command data back to the LVDC/LVDA for verification.

Switch Selector processing is accomplished in the following manner: (see Figure 15.6-6). The system is first tested for a hung stage by the Switch Selector routine. The program then issues a PIO instruction which loads the Switch Selector registers. The 15-bit computer word includes one of the five address bits being set to select the stage for Switch Selector operation along with a coded command word indicated by the eight command bits. The other two bits, the reset bit and the read bit, are zeros. At this time, a time delay occurs which is determined by the Switch Selector interrupt counter (18 milliseconds minimum). This delay is required to allow time for relays in the addressed Switch Selector to function. After the delay, the program issues another PIO instruction that loads the original eight command bits into the accumulator

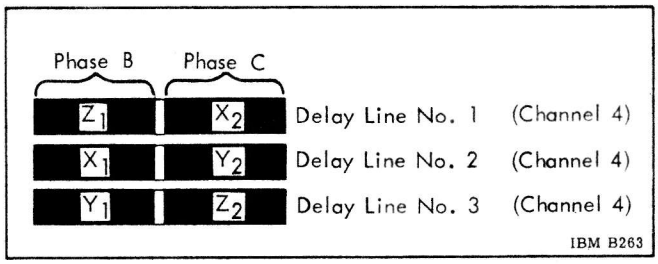

Figure 15.6-5 TMR Delay Line Storage of Velocity Information

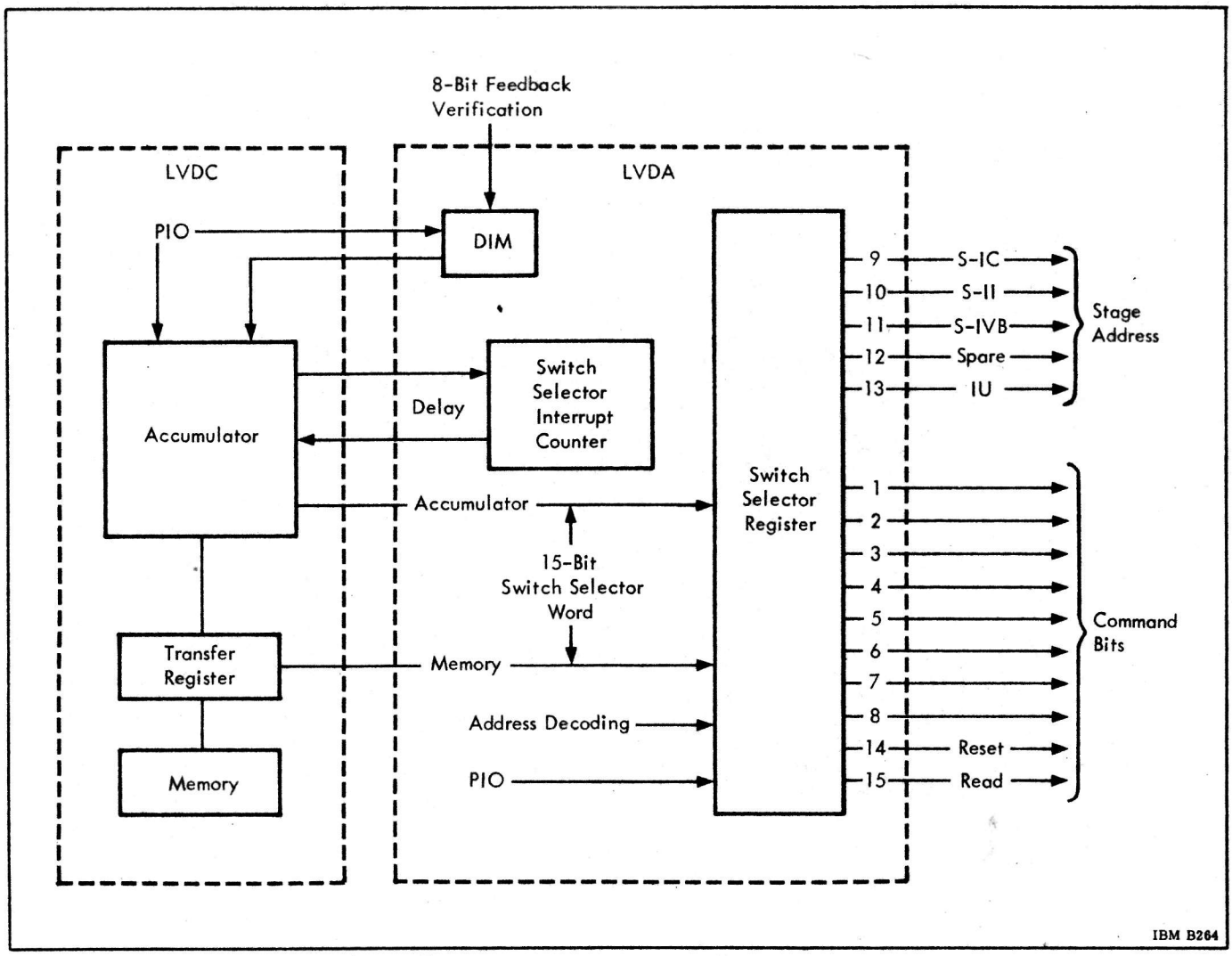

Figure 15.6-6 Switch Selector Processing

in complement form. The computer program then checks to verify that the feedback bits are the complement of the original command to the Switch Selector. There are two alternatives available at this point: If the feedback bits are correct, the program issues a word that sets the register bits to zero (except the address bit – for telemetry – and read bit). This turns ON the function that was selected by the original computer word. The read command must remain set for at least 25 milliseconds. If the feedback bits are incorrect, the program issues a PIO switch selector code with all 15 bits being zeros except bit 14, the reset bit. The operation then must assume a delay to allow all relays in the selected stage to reset. After the delay, the program issues a PIO instruction that sets the complement of the original command word along with the stage select bit or address. Due to the dual command decoding ability of the stage Switch Selector, this operation can select the same stage operation. The program must then go through another delay as determined by the Switch Selector interrupt counter. At the termination of the delay the program issues a PIO Switch Selector 15-bit word which is all zeros (except the address bit and read bit). This allows the commanded stage operation to be actuated.

Further information on the Switch Selector and its operation may be found in Chapter 4.

INTERRUPT PROCESSING

If some event should occur that requires immediate attention by the LVDC flight program, an interrupt signal is generated which sends the program to a special subroutine. Once the cause of the interrupt signal has been dealt with, the computer returns to the main program and continues on from the point of interruption. At present, three interrupt signals are developed internal to the LVDC/LVDA: minor loop interrupt, Switch Selector interrupt, and simul-

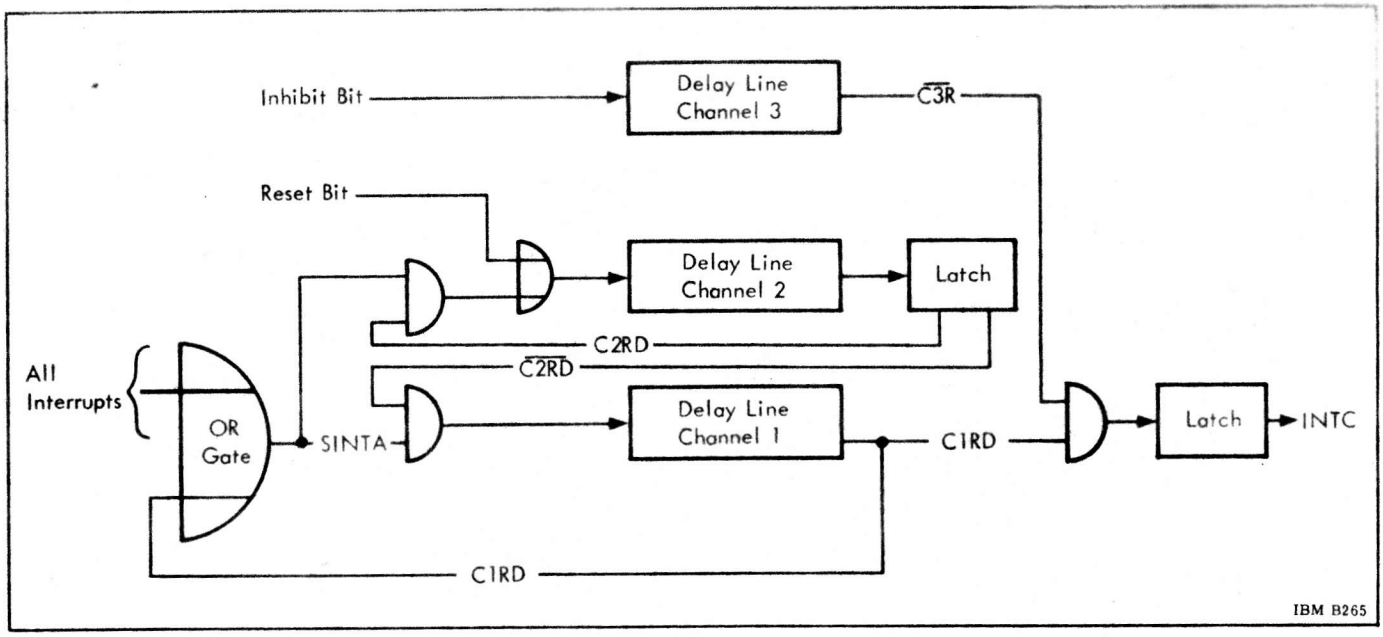

Figure 15.6-7 Interrupt Processing Logic

taneous duplex memory error interrupt (TLC). One interrupt comes from the Saturn Ground Control Computer, and the remaining eight interrupts are developed by various control elements in the spacecraft.

Interrupt processing requires the use of the Phase C time of three channels of the LVDA delay line. See Figure 15.6-4.

All of the interrupts to the LVDA are clocked individually and are OR'ed together so that when an interrupt does occur, it is sent over one line (SINTA) to Channel 1 of the Delay Line. See Figure 15.6-7. Each particular interrupt bit can be identified by the bit time that is sent to the delay line. Since only one interrupt is processed at a time, a certain priority is set up. This priority depends on the order that the various interrupt input lines are sampled. Upon leaving the delay line, the interrupt bit sets an interrupt computer latch (INTC). The output is sent to the LVDC to initiate an interrupt subroutine. If any other interrupts are encountered during the process, these bits are also put into the delay line, and upon completion of the present interrupt subroutine, the new interrupt is then dealt with. Once the LVDC interrupt subroutine is completed, an interrupt reset bit is sent to the second channel of the delay line in the LVDA. This reset bit corresponds in relative time to the interrupt bit in Channel 1 that it is meant to reset. The INTC signal being sent to the computer is reset. After passing through the delay line, the reset bit sets a latch ($\overline{C2RD}$ = 0) for one bit time, and effectively causes a delay of one machine cycle. This disables the AND gate to Channel 1 of the delay line. This is necessary in the event that the mechanism feeding the interrupt signal to the delay line (such as a slow-acting relay) had not yet reset its interrupt signal, another interrupt process would not be started. If the original interrupt had disappeared (SINTA = 0), the process stops and the next interrupt, if any, is then processed. If the original interrupt has not yet reset (SINTA = 1), the reset bit is recirculated in Channel 2 of the delay line until the interrupt does disappear.

If for some reason, the programmer does not desire a certain interrupt signal to be processed, a PIO command will be issued to inhibit any or all interrupts that might be sent to the LVDC over the INTC line. These inhibit bits are fed into Channel 3 of the delay line and correspond in relative time to the interrupt bits of Channel 1 that they are to inhibit. When an interrupt signal is produced (but an interrupt inhibit signal is also produced), the interrupt signal, C1RD, is activated as usual; but the interrupt computer signal, INTC, is held off since $\overline{C3R}$ equals 0 for that bit time.

TELEMETRY PROCESSING

In order to monitor conditions existing in the LVDC and LVDA during flight, the Mod 410 Digital Multiplexer (Chapter 5) samples information contained in telemetry registers within the LVDA at a rate of 240 times per second; i.e., every 4.17 milliseconds. These registers are recipients of two specific types of telemetry, LVDA telemetry and LVDC telemetry. The differences that distinguish the two types arise not only from where the telemetry information originates but also the method of processing this information.

LVDA Telemetry

Information handled by the LVDA is designated to be telemetered if:

- The information (other than LVDC telemetry information) is passed between the LVDA and LVDC.
- The LVDC issues a PIO instruction requesting information to be telemetered by the LVDA.
- Equipment error is indicated by an error monitor register.

The existence of any one of the above conditions causes the construction of an LVDA telemetry word.

All LVDA telemetry words have identical formats. The data is contained in 26 bits (which is formatted in several ways for its particular application). These bits are combined with 8 tag bits to define the type of data being telemetered and 5 bits of real time that identify the time at which the data was designated to be telemetered. Referring to Figure 15.6-8, the 39 bits of data, tag, and real time are channeled into the Data Output Multiplexer (DOM), which essentially consists of a 4-channel delay line and a distributor. Each channel is capable of storing a 39-bit word referred to as a "DOM word".

A word is stored in the DOM until the data portion of the DOM word is gated into a 26-bit buffer register. At the same time, the real time portion is transferred into a 5-bit real time/mode-validity register and the tag portion is transferred into an 8-bit tag register. The commutator action of the DOM selects a delay line channel which is currently storing a DOM word and directs this word into the registers. However, the word also remains in the DOM until it enters the Mod 410 Multiplexer. Every 4.17 milliseconds, the data stored in these registers is read into the Mod 410 Multiplexer along with the proper parity bit for a total of 40 telemetry bits. (Odd parity is used for telemetry transmission.) The multiplexer then issues a sync pulse and another word is gated from the DOM into the buffer, real time, and tag registers. If the DOM is empty, all zeros are continually read into the multiplexer.

Tag bits 1 through 7 identify the source of the 26 data bits contained in the DOM. Bit 8 is used to distinguish between LVDC and LVDA telemetry. This bit is "0" for all LVDA telemetry words.

An error indication in the error monitor register is the only condition under which an LVDA telemetry word is created without the issuance of a PIO instruction by the LVDC. The error monitor register stores disagreements between the inputs to certain voters and duplex circuits in the LVDA and LVDC. When an error occurs, an error time word is forced into the DOM. This word contains real time, phase time, clock time and the bit gate at which the error occurred, and the instruction counter setting at the time of the error. With this information the circuit causing the error can be determined.

LVDC Telemetry

Any information available to the LVDC can be made part of LVDC telemetry. By issuing a telemetry PIO instruction, the LVDC circumvents the DOM and loads the tag, real time/mode validity, and buffer registers with an LVDC telemetry word. This operation destroys the current contents of these registers thus giving the LVDC telemetry precedence over LVDA telemetry. However, a DOM word destroyed in these registers is still stored in the DOM and will be read again into the register at the occurrence of the next sync pulse.

It should be noted that an LVDC telemetry word may destroy another LVDC word if they both occur between adjacent sync pulses. But since telemetry PIO instructions are issued from the flight program, this hazard can be avoided by programming telemetry instructions at least 4.17 milliseconds apart.

An LVDC telemetry word is constructed from 26 bits of data, 9 tag bits, 3 computer mode bits and 1 validity bit. See Figure 15.6-8. The three mode bits are obtained from the LVDA mode registers. The validity bit is set to a "1" only while the LVDC is loading the telemetry registers. An indication of the validity of a telemetered LVDC word is necessary because the telemetry registers may be in the process of being

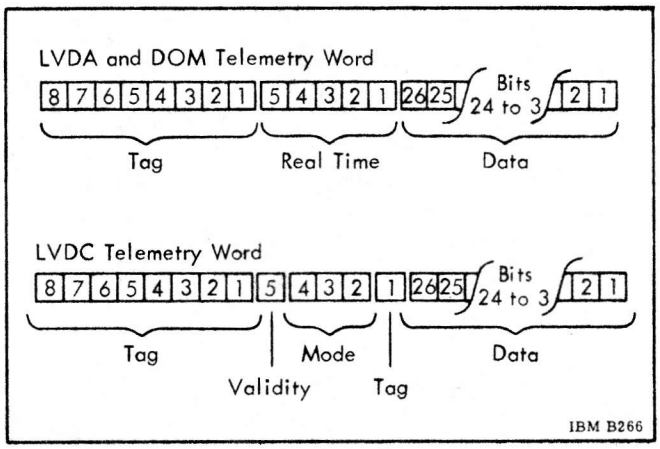

Figure 15.6-8 Telemetry Word Formats

loaded when the multiplexer is reading the telemetry registers. The validity bit being a "1" under such conditions indicates that the word in the telemetry registers is only partially loaded and, therefore, invalid.

Eight LVDC address bits are directed into the tag register. Bit 8 of this register is set to "1" to indicate LVDC telemetry and CIU operation. One address bit, three mode bits, and the validity bit are channeled into the real time/mode-validity register. The 26 bits of data are placed in the buffer register. After these registers are read into the Mod 410 Digital Multiplexer, the registers are again loaded from the DOM.

ATTITUDE COMMAND PROCESSING

The LVDC generates roll, pitch, and yaw attitude commands in a digital format. Under program control, these commands are transferred to the LVDA which processes and converts the digital data to analog voltages.

The LVDA processing operation includes digital to analog conversion, error detection, amplifying and scaling, telemetry buffering, and storage.

The LVDA continuously presents these analog commands to the Flight Control Computer where they are further processed before becoming the steering commands for the vehicle's attitude maneuvers.

Figure 15.6-9 is a block diagram of attitude command processing within the LVDA. Three identical 9-bit ladder registers temporarily store the digital commands (roll, pitch, or yaw) as they are alternately received from the LVDC. Two of the registers provide inputs for redundant channels within the D/A converter area. The third channel provides an input for a reference channel which is used in error detection. When a ladder group address PIO instruction is issued by the flight program, the ladder registers receive 9 bits of the computer data word (bits 17 through 25). The ladder decoders then convert the digital data stored in the ladder registers into an analog voltage. Each ladder decoder converts the 9 bits of incoming digital data. The first 8 bits (LR1 to LR8) determine the magnitude of the analog signal, and the ninth bit (LR9) determines the polarity. The decoder produces a negative output when LR9 is a "1" and a positive voltage when LR9 is a "0"

The outputs from ladder decoders A and B are applied to three output multiplexer-drivers. Each driver, when enabled by the proper control signal, will sample and store (hold) its respective pitch, roll, or yaw signal. The drivers contain "hold capacitors" which store these analog voltages for a limited time. See Figure 15.6-10. Since the stored voltage will tend to decay and cause erroneous output signals, the hold capacitors must be recharged at regular intervals. During boost flight, these capacitors are allowed to store the signal voltage for a maximum of 40 milliseconds before being recharged by an updated attitude command. During coast phase, the quality of the attitude commands are not as critical and only need to be updated at 100 milliseconds.* When enabled by control signals, bipolar electronic switches couple the decoder outputs to the appropriate hold capacitors and ladder amplifier. The control signals cause these switches to act as either open or closed circuits. The telemetry buffers convert the signal voltages to levels which are compatible with the telemetry equipment.

An error detector compares the reference ladder decoder output with both the ladder decoder A output and the output of the selected output multiplexer-driver. If the comparisons are within designated tolerances, the error detector allows the normally selected channel A to remain selected. If either or both comparisons are out of tolerance, the error detector will select channel B. Once the error detector has selected channel B, the channel will remain selected until the flight program commands a change.

Control circuits, under address decoder control, select the appropriate output multiplexer-driver and enable the error detector to sample the ladder decoder outputs. During the time when the ladder registers are being loaded, the control circuits also inhibit the drivers and error detector from sampling the decoder outputs.

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* The flight program routine for updating these commands is only cycled once per second, but the same routine reloads the ladder registers 10 times per second (100 milliseconds). This method of programming saves considerable computer time for other operations.

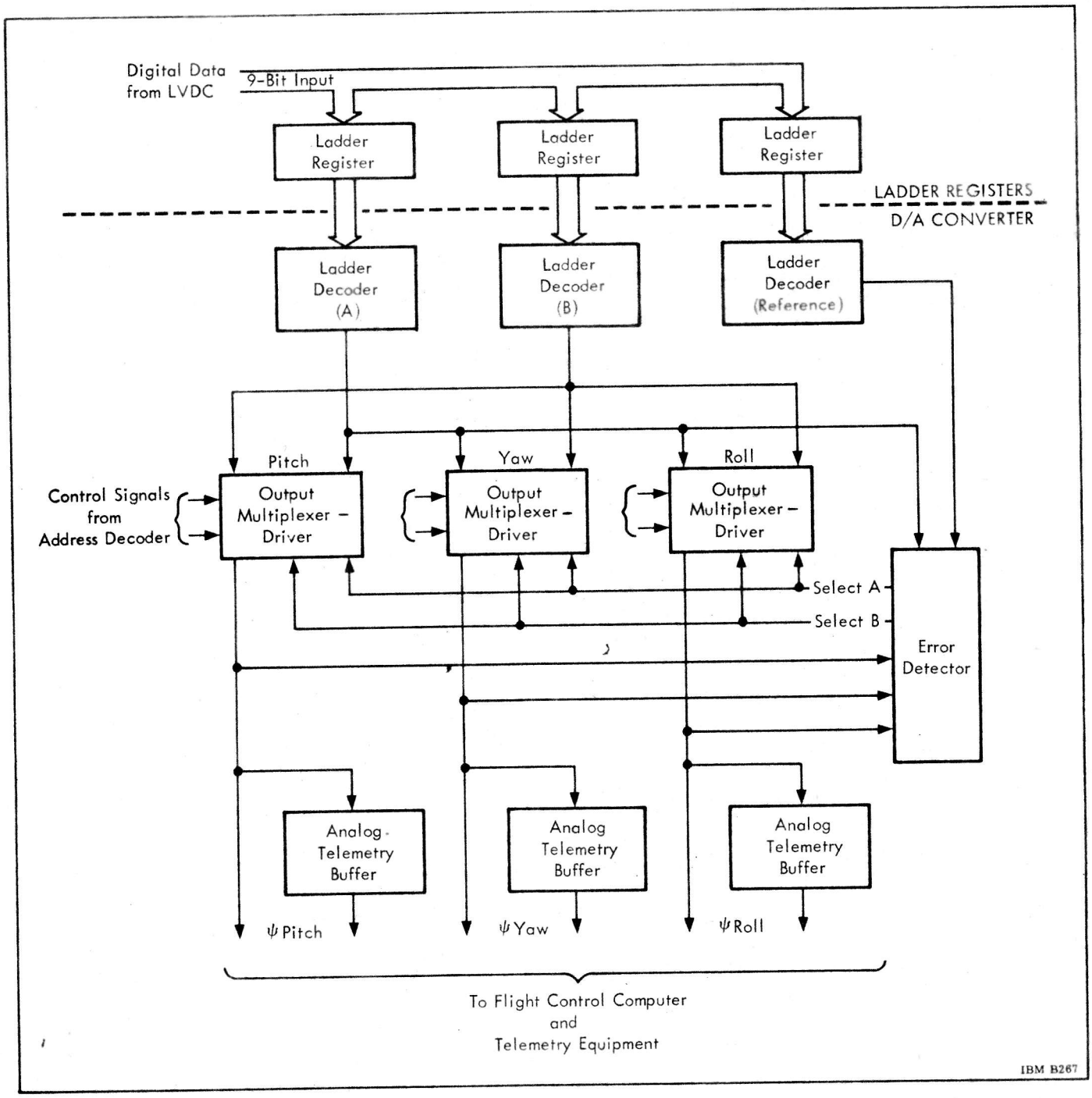

Figure 15.6-9 Attitude Command Processing Block Diagram

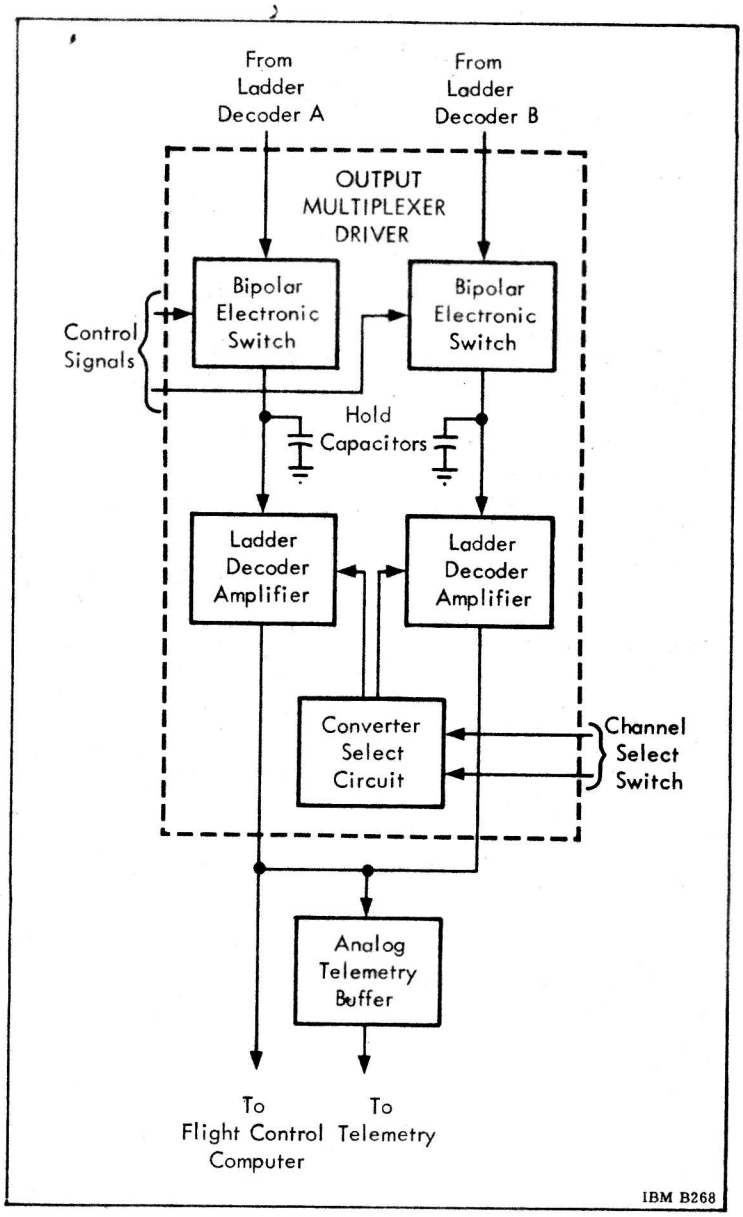

Figure 15.6-10 Output Multiplexer-Driver Block Diagram

ABBREVIATIONS

A

A	(A_Z) Flight Azimuth
A	Ampere
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AG	AND Gate
AGC	Automatic Gain Control
AM	Amplitude Modulation
AN	Ascending Node
AP	Accelerometer Processor (Module)
APS	Auxiliary Propulsion System
AR	Accelerometer Read (Module)
ASC	ST-124-M Accelerometer Signal Conditioner
ASP	Accelerometer Signal Processor
Aux	Auxiliary
AVP	Address Verification Pulse
A_Z	(A) Flight Azimuth
Acc/Reg	Accumulator Register
A/S	Add/Subtract

B

bps	Bits per Second
B/W	Bits/Word

C

CAT	Control Attenuation Timer
cc	Cubic Centimeter
CC	Chi Computations
CCS	Command and Communication System
CCSL	COD Counter Sequence Latch
CDSV	Change Data Sector-Voted
CG	Center of Gravity
CIU	Computer Interface Unit
CL	Center Line
COD	Crossover Detector
COM	Common
CM	Command Module
CM	Phase I and IV Control (Module)
cm	Centimeter
Const	Constant
CP	Center of Pressure
CPP	Command Program Patch
CRP	Command Received Pulse
CSM	Command and Service Module
CT	Control Transformer
CT	Data Compression Telemetry (Module)
CSTN	Single Step Operation - Not
CSTV	Single Step Operation - Voted
CVD	Command Voltage Demodulator
CX	Control Transmitter
CX:CT	Control Transmitter:Control Transformer

D

DATAV	Normal Data Input from External Equipment
DB	Disagreement Bit
db	Decibel
DCS	Digital Command System
DCW	Data Command Word
DDAS	Digital Data Acquisition System
deg	Degree
DIN	Special Data Input
DN	Descending Node
DOMS	Data Output Multiplexer Serializer Latch
DP	Discrete Processor (Module)
D/R	Downrange
DS	Digital Command System (Module)
DSIF	Deep Space Instrumentation Facility
DT	Selector Dump Telemetry (Module)
DV	F/M Calculations

E

EAMV	Error in Even Memories - Voted
EBMV	Error in Odd Memories - Voted
EBW	Exploding Bridge Wire
EDS	Emergency Detection System
EF	Emitter Follower
e.g.	Exempli Gratia (for example)
EP	Events Processor (Module)
ESE	Electrical Support Equipment
Etc.	Et Cetera (and so forth)
ETC/BTC	Module
EXT	External

F

FCM	Flight Combustion Monitor
FIR	Far Infrared
FM	Frequency Modulation
F/M	Thrust Acceleration (Force/Mass)

G

g	Gravity
GCC	Ground Control Computer
GM	Universal Gravitational Constant
GRR	Guidance Reference Release
GRRA	Guidance Reference Release Alert
GSE	Ground Support Equipment
GU	Spin Reference

H

H	Spinning Mass (Angular Momentum)
HALTV	Halt - Voted
HOPC1V	Generate HOP Constant - Voted
HS	S-IVB Cutoff Prediction
Hz	Hertz (cycle per second)

I

i	Inclination of Orbit (angle)
IA	Input Axis
ICD	Internal Control Discrete
ID	Identification
i. e.	Id Est (that is)
IECO	Inboard Engine Cutoff
IF	Intermediate Frequency
IGM	Iterative Guidance Mode
IIR	Intermediate Infrared
INTC	Interface Output Latch (Interrupts LVDC)
INTV	Interrupt - Voted
INV	Inverter
IR	Infrared
IRIG	Interrange Instrumentation Group
IU	Instrument Unit

J

	Jet Propulsion Laboratory

L

LES	Launch Escape System
LET	Launch Escape Tower
LM	Lunar Module
LO	Liftoff
LO	Liftoff Search
LOX	Liquid Oxygen
LR	Ladder Ramp Processor
LSD	Least Significant Digit
LTE	Laboratory Test Equipment
LVDA	Launch Vehicle Data Adapter
LVDC	Launch Vehicle Digital Computer

M

m	Meter
MAP	Message Acceptance Pulse
MCC	Mission Control Center
MCR	Magnetic Core Register
MEPWM	Water Methanol Activate (Module)
MHz	Megahertz (Megacycle)
ML	Minor Loop (Module)
MLCHI	Minor Loop Chi
Mod	Model
Mono	Monostable (Multivibrator)
MS	Minor Loop Support
ms	Millisecond
MSD	Most Significant Digit
MSFN	Manned Space Flight Network
mV	Millivolt
MVB	Multivibrator
MW	Megawatt

N

N	Newton
N	"Not" Condition, a Binary "0"
N/A	Not Applicable
NE	Boost Navigation (Module)
NIR	Near Infrared
NRZ	Non-Return-to-Zero
NU	Navigation Update Implementation (Module)

O

OA	Output Amplifier
ODOP	Offset Doppler
OECO	Outboard Engine Cutoff
OG	Orbit Guidance (Module)
O/D	Orbital Mode/Data
OP	Operational
OPR	Orbital Processing Routine

P

PA	Phase Actuator (Module)
PACPS	ST-124-M Platform AC Power Supply
PAM	Pulse Amplitude Modulation
PC 30	30 Second Data Compression (Module)
PC 50	50 Second Data Compression (Module)
PC 99	100 Second Data Compression (Module)
PCM	Pulse Code Modulation
PEA	ST-124-M Platform Electronic Assembly
PG	Simulated Platform Gimbal Angle (Module)
PIO	Process Input Output
PM	Phase Modulation
pps	Pulses per Second
PRF	Pulse Repetition Frequency
psi	Pounds per Square Inch
psia	Pounds per Square Inch Absolute
psid	Pounds per Square Inch Differential
psig	Pounds per Square Inch Gage
PRN	Pseudo-Random Noise
PSK	Phase Shift Keyed
PSR	Parallel Storage Register
PTL	Prepare to Launch
PU	Propellant Utilization (System)
P212	Service Periodic Processor (Module)

Q

Q	Aerodynamic Pressure

R

R	Reset
r (or) R	Vehicle Position
r_o	Initial Velocity
RACS	Remote Auto. Calib. System
RASM	Remote Analog Submultiplexer
R & D	Research and Development
RDSM	Remote Digital Submultiplexer
RET	Return
rf	Radio Frequency
rms	Root Mean Square
RPM	Revolutions per Minute
RSO	Range Safety Officer
RTC	Reasonable Test Constnat
RUNV	Start Signal - Voted

S

S	Set
s	Second
S&A's	Safe and Arm Devices
SA	Spin Axis
SA	Simulated Accelerometer (Module)
SC	(S/C) Spacecraft
SCCS	Saturn Command and Control System
SCFH	Standard Cubic Feet per Hour
SCO	Sucarrier Oscillator
Servo	Servomechanism
SDH	Simplex Driver - High
SDI	Simplex Driver - Intermediate
SDL	Simplex Driver - Low
SG	Signal Generator
SM	Service Module
SR	Shift Register
SRA	Spin Reference Axis
SS	Single Sideband
SS	Switch Selector Processing (Module)
ST	Application Module
STP	Standard Temperature and Pressure

T

TBD	To be Determined
TB1	Time Base 1 (Module)
TB2	Time Base 2 (Module)
TB3	Time Base 3 (Module)
TB4	Time Base 4 (Module)
TB57	Time Base 5/7 (Module)
TC	Restart Calculations (Module)
TD	Time Delay
TDH	TMR Driver - High Current
TDL	TMR Driver - Low Current
TDM	TMR Driver - Medium Current
TG	Torque Generator
TLC	Simultaneous Memory Errors
TLCV	Two Simultaneous Memory Errors - Voted
TM	Telemetry
TMR	Triple Modular Redundancy
TRS	Transfer Register Serial
TRSV	Transfer Register Serial - Voted

TS	Simultaneous Memory Error Recovery (Module)
TT	Time Tilt Guidance
TWT	Traveling - Wave Tube

U

UHF	Ultra-High Frequency
UM	Phase I and III Time Update (Module)
μs	Microsecond
USB	Unified S-Band

V

VAB	Vehicle Assembly Building
VCO	Voltage-Controlled Oscillator
VHF	Very-High Frequency
VSWR	Voltage Standing Wave Ratio

W

W	Watt

X

X	Roll Axis

Y

Y	Pitch Axis

Z

Z	Yaw Axis

SIGNS AND SYMBOLS

$\int$	Integral
∂	Partial Differential
$\surd$	Square Root
$\sim$	Difference
$\propto$	Varies as
$>$	Greater than
$<$	Less than
$\geq$	Greater than or equal to
$\leq$	Less than or equal to
∞	Infinity
$\cong$	Congruent to
$\approx$	Nearly Equal to
$\angle$	Angle
Δ	Change

Greek Alphabet

α	alpha	ν	nu
β	beta	ξ	xi
γ	gamma	o	omicron
δ	delta	π	pi
ϵ	epsilon	ρ	rho
ζ	zeta	σ	sigma
η	eta	τ	tau
θ	theta	υ	upsilon
ι	iota	ϕ	phi
κ	kappa	χ	chi
λ	lambda	ψ	psi
μ	mu	ω	omega

β	Feedback signal from S-IB actuators to Flight Control Computer.
β_c	Command to actuator from Flight Control Computer. (β_R β_P β_Y)
$\ddot{\gamma}_P$ $\ddot{\gamma}_R$	Lateral acceleration (S-IB only).
ΔX_g	Change to X_S caused by gravitation.
ΔX_T	Change to X_S caused by Platform-measured acceleration.
θ	Platform gimbal angle. Indicates the difference between vehicle attitude and Platform attitude.
$\theta_X \theta_Y \theta_Z$	Platform gimbal angles (vehicle attitude).
ϕ	(ϕ_L) Geodetic latitude of the launch site.
$\dot{\phi}$	Rate of angular attitude change.
$\dot{\phi}_R \dot{\phi}_P \dot{\phi}_Y$	Rate of attitude change in vehicle coordinates.

χ	Desired attitude change as determined by guidance computations.
$\chi_R\chi_P\chi_Y$	Guidance command angles (desired vehicle attitude).
$\chi_X\chi_Y\chi_Z$	Guidance command angles (Euler angles)
ψ	Attitude error signal
$\psi_R\psi_P\psi_Y$	Attitude error signals (steering commands)
ψ_T	Total range angle
a_0	Gain factor for attitude error (ψ) channels
a_1	Gain factor for attitude rate ($\dot{\phi}$) channels
a_e	Equatorial radius of the earth
g_2	Gain factor for lateral acceleration ($\ddot{\gamma}$) channels (Saturn IB only)
GN_2	Gaseous Nitrogen
I_{gX}	Computer gravitational velocity in the X_S direction
LH_2	Liquid Hydrogen
LO_2	Liquid Oxygen
N_2O_4	Nitrogen tetroxide
P	Constant used in computing gravitational acceleration and using: a_e = equatorial radius of the earth GM = universal gravitational constant J = constant ϕ = geodetic latitude of launch site A_Z = firing azimuth
r	(R) Vehicle position measured as a radius vector from the center of the earth to the vehicle
$\dot{r}$	Vehicle velocity after gravitational and initial velocity have been acounted for
S	Same as P
UVW	Gravitational coordinate system
V_s	Velocity
W	Same as P
$X_4Y_4Z_4$	Target plane (flight plane) coordinate system
$\dot{X}_g\dot{Y}_g\dot{Z}_g$	Components of gravitational velocity
$\ddot{X}_g\ddot{Y}_g\ddot{Z}_g$	Components of gravitational acceleration
$X_IY_IZ_I$	Inertial coordinate system (also expressed as $X_MY_MZ_M$)
$\dot{X}_I\dot{Y}_I\dot{Z}_I$	Components of thrust velocity (measured by the integrating accelerometers of the Platform)
$X_oY_oZ_o$	Initial position - launch site to earth's center
$\dot{X}_o\dot{Y}_o\dot{Z}_o$	Initial velocity
$X_SY_SZ_S$	Space-fixed navigational coordinate system (used for navigation and guidance computations)
$\dot{X}_S\dot{Y}_S\dot{Z}_S$	Inertial velocity
$X_VY_VZ_V$	Injection coordinate system

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