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NASA  
SUPPORT MANUAL

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APOLLO SUPPORT EQUIPMENT  
MAINTENANCE HANDBOOK

11237

CARRY-ON  
PCM SYSTEM  
MODEL C14-210(-0003)

(NAA PART NO. G16-851450-101)  
(VECTOR PART NO. PCM 7765)  
(ME 901-0141-0003)

CONTRACT NO. NAS 9-150  
EXHIBIT I, PARAGRAPH 10.9

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## INTRODUCTION

This technical manual provides maintenance instructions for the Carry-On Pulse Code Modulated (PCM) Telemetry System, Model C14-210 (-0003), NAA Part No. G16-851450-101, ME901-0141-0003 (Vector Part No. PCM 7765), manufactured by Vector of Southampton, Pennsylvania, a Division of United Aircraft Corporation for the Space & Information Systems Division of North American Aviation Inc. of Downey, California.

These instructions reflect the latest information available as of April 15, 1966. Appendix A contains a listing of specific time-dated source data utilized in the preparation of this manual.

This manual was prepared for the Space & Information Systems Division of NAA by Vector of Southampton, Pennsylvania, a Division of United Aircraft Corporation.



## SECTION I

## DESCRIPTION

1-1. PURPOSE OF EQUIPMENT.

1-2. The Carry-On PCM Telemetry System (hereinafter referred to as the C14-210-0003) is capable of time-division multiplexing 128 channels of analog and digital input data, and converting this data into a serial PCM format, consisting of 50 prime frames per second. Each prime frame contains 128 eight-bit words coded in NRZ-S fashion. The serial PCM output of the C14-210-0003 is channeled into the Apollo Checkout Equipment (ACE) ground station, processed by the computer system, then it is displayed at the consoles.

1-3. LEADING PARTICULARS.

1-4. Leading particulars of the C14-210-0003 are as follows:

## a. Dimensions

1. Length: 12 inches
2. Width: 12 inches
3. Height: 8.94 inches

## b. Weight: 35 pounds

c. Power Requirements: +28 ( $\pm 1.5$ ) vdc @ 1.5 amperes

## d. Performance Characteristics

## NOTE

A complete description of the input and output signal characteristics is contained in paragraph 2-3.

1. Total Number of Input Channels: 128
  - (a) Channels used for analog data: 58
  - (b) Channels used for digital data: 69
  - (c) Channels used for prime frame sync: 1



## 2. Analog Gates

- (a) Number: 48 total, including 6 spares.
- (b) Amplitude Level: 0 to +5 vdc; unipolar
- (c) Sampling Rate: 50 and 100 sps

## 3. Digital Input Data

- (a) Format: 9 parallel bits per sample, consisting of 8 data bits and 1 control bit.
- (b) Amplitude level
  - (1) Binary ONE: +3.5 to +10 vdc
  - (2) Binary ZERO: 0 ( $\pm 0.5$ ) vdc
- (c) Sampling rate: 50 sps/digital data channel

## 4. External Timing Signal Inputs

- (a) Data rate timing: 51.2 kc, negative-going square wave
- (b) Major frame synchronization: 1 pps, 10-microsecond, negative-going pulse

## 5. PCM Output

- (a) Type: NRZ-S
- (b) Format: 50 prime frames, consisting of 128 words each
- (c) Word length: Eight bits straight binary, MSB first
- (d) Bit rate: 51,200 bits/second
- (e) Output Level:
  - (1) Binary ONE: +7 ( $\pm 1$ ) vdc
  - (2) Binary ZERO: 0 ( $\pm 0.5$ ) vdc

- 6. Subframe Sync Output: 1 pps, 10-microsecond, negative-going pulse

- 7. Data Inhibit Output: Pulsetrain containing 58 negative-going, 156-microsecond pulses which occur each time an analog gate is sampled.

## 8. Primary Gate Control Channel Outputs:

70 negative-going, sequenced outputs  
156 microseconds in width which occur  
in coincidence with each digital data  
time and prime frame sync.



## e. Operating Environmental Conditions

1. Temperature: +15°F to +120°F (-9 to +49°C) without external cooling;  
-320°F to +250°F (-195°C to +121°C)  
at 450,000 feet simulated altitude using externally-supplied coolant.
2. Altitude: Sea level to 450,000 feet
3. Humidity: 0 to 100 percent relative humidity,  
including condensation of water.

## f. Coolant (High Altitude Operation)

1. Type: Water glycol
2. Composition
  - (a) Ethylene glycol: 62.500 parts by weight
  - (b) Distilled water: 37.422 parts by weight
  - (c) Triethanolamine phosphate: 1.563 parts by weight
  - (d) Sodium mercaptobenzothiazole (Nacap): 0.156 parts by weight
3. Parameters
  - (a) Weight per gallon: 9.04 pounds at +75°F (+24°C)
  - (b) Specific gravity by hydrometer: 1.090 at +40°F (+4.4°C)  
1.072 at +90°F (+32°C)
  - (c) Specific heat: 0.72 at +40°F (+4.4°C)  
0.75 at +90°F (+32°C)  
(Btu/pound/°F)
  - (d) Molecular weight: 62.07
  - (e) Viscosity: 10 at +40°F (+4.4°C)  
4 at +90°F (+32°C)  
(Centerpoises)
  - (f) Ph 7.2 to 7.8
4. Temperature, Inlet +40°F to +90°F (+4.4°C to +32°C)
5. Flow Rate: <9 pounds/hour
6. Pressure, Inlet: 150 psig maximum



## NOTE

The coolant temperature at the outlet of the C14-210-0003 should not exceed +120°F (+49°C). The pressure change between the inlet and outlet of the C14-210-0003 should not exceed 30 pounds per square inch at a flow rate of 9 pounds per hour.

1-5. EQUIPMENT DESCRIPTION.

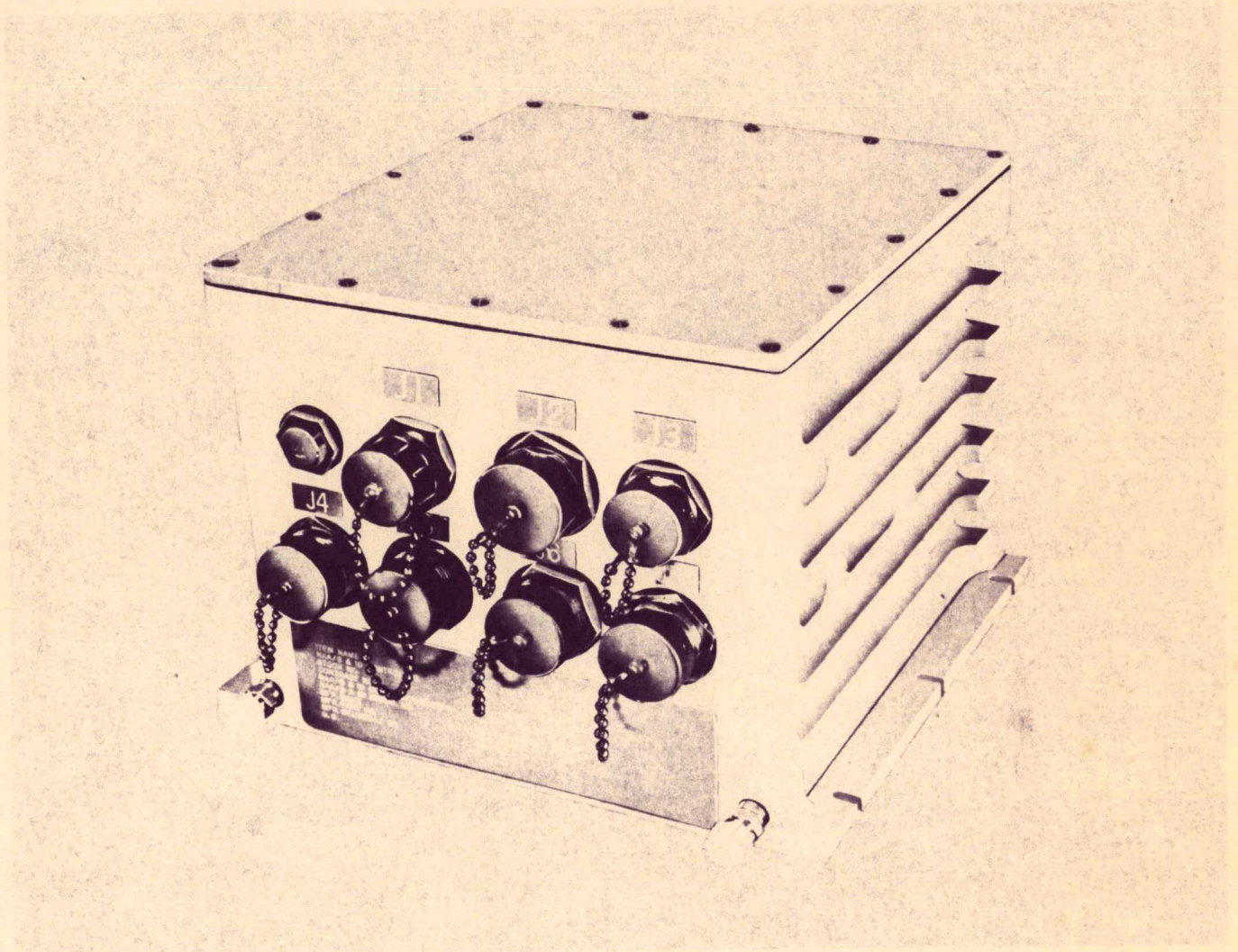
## 1-6. PHYSICAL.

1-7. The C14-210-0003 (figure 1-1) is packaged in an aluminum, rectangular-shaped housing which is hermetically sealed to minimize the effects of component outgassing. Two fittings located on the connector side of the housing and hollowed channels located within three sides of the housing permit the use of a coolant (water-glycol) for heat conduction during high altitude operation. Seven electrical connectors located on the exterior of the housing provide a means of applying input power and signals to the unit, obtaining the desired output signals, and monitoring system operation. An elapsed time indicator located on the connector plate provides a four-digit readout in hours of the accumulated operating time of the C14-210-0003.

1-8. The C14-210-0003 contains the following 16 plug-in circuit boards and a plug-in power supply:

- a. Board 1 (A1) Drivers & Inhibits
- b. Board 2 (A2) Drivers
- c. Board 3 (A3) Drivers
- d. Board 4 (A4) Inhibits
- e. Board 5 (A5) Analog Gates
- f. Board 6 (A6) Analog Gates
- g. Board 7 (A7) Analog Gates
- h. Board 8 (A8) A/D Converter, Card A
- i. Board 9 (A9) PGC Inhibit Trees
- j. Board 10 (A10) Programmer One Shots
- k. Board 11 (A11) Programmer One Shots
- l. Board 12 (A12) Programmer One Shots
- m. Board 13 (A13) Programmer One Shots
- n. Board 14 (A14) Programmer Gates & Timing
- o. Board 15 (A15) Parallel-to-Serial Converter
- p. Board 16 (A16) A/D Converter, Card B
- q. Board 17 (A17) Power Supply Assembly





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Figure 1-1. Carry-On Pulse Code Modulation System,  
Model C14-210 (-0003)



1-9. All of the preceding boards are readily accessible for removal/replacement. The circuit boards are located immediately beneath the top cover of the C14-210-0003. Each board contains modular assemblies which are interconnected to perform a particular circuit function or operation.

#### 1-10. FUNCTIONAL.

1-11. The functional description of the C14-210-0003 is presented on two levels. First, a general description of the complete system is used to familiarize maintenance personnel with the capabilities and interrelationships of the main functional sections. Then, each functional section is divided into individual circuit stages (modules), and a more complete explanation is developed on the basis of this last division.

1-12. Idealized waveforms, which show the relative timing of the various signals associated with a particular functional section, are presented wherever their inclusion is considered necessary to clarify the text.

1-13. The general system description is presented using block diagrams to represent each functional section. The functional section discussion is supported by simplified logic diagrams using symbols which are explained in Section VIII. The symbols used in the simplified logic diagrams and the reference designation numbers assigned to each symbol are the same as those used for the detailed logic drawings in Section VIII. In some isolated cases, individual circuit stages do not lend themselves to conversion to a standard logic symbol. These stages are shown in the diagrams as blocks, properly identified by functional name and input/output pin letters. The C14-210-0003 employs positive logic, whereby a logical ONE is defined as a voltage level more positive than that used for a logical ZERO. Throughout the system, the predominant voltage level used to represent a logical ONE is plus 10 volts; a logical ZERO is identified by a zero-volt level. In all cases, however, a logical ONE is more positive than a logical ZERO.

1-14. A block diagram of the C14-210-0003 is shown in figure 1-2. The A-numbers shown in the blocks refer to the reference designation number assigned to the plug-in circuit boards comprising each function.

1-15. Operation of the C14-210-0003 is synchronized by externally applied data rate timing and a major frame synchronization signal. The data rate timing is counted down in the timer section and used to provide intermediate internal control signals for the other sections of the C14-210-0003. The major frame sync signal synchronizes the operation of the timer and programmer sections with external processing equipment for purposes of data identification. Between the occurrence of major frame sync pulses, the C14-210-0003 generates 50 prime frames of PCM data. Each prime frame consists of 128 eight-bit words. The repetition frequency of the word bits is the same as that of the data rate timing.



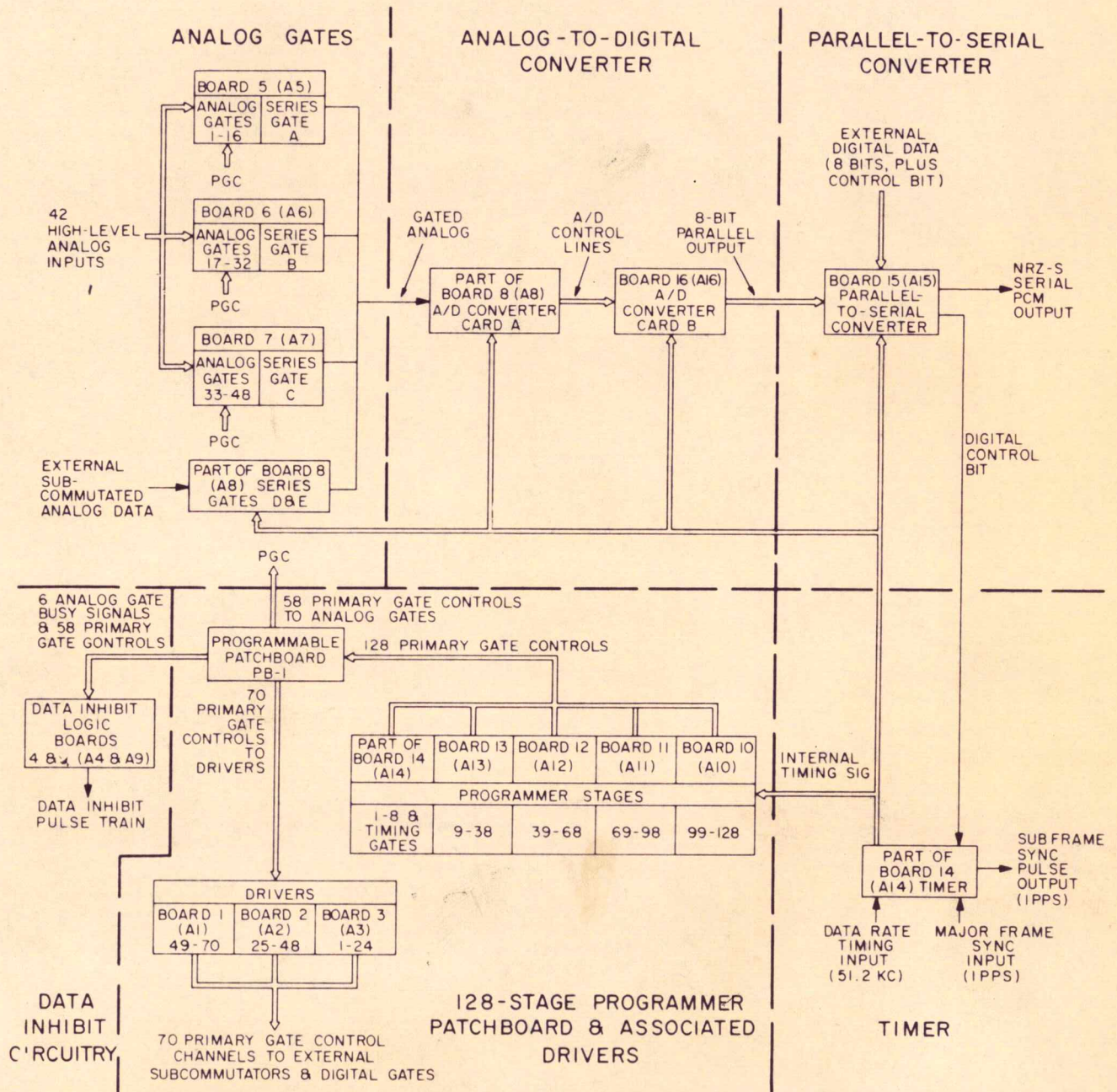


Figure 1-2. Block Diagram of C14-210-0003



1-16. The C14-210-0003 accepts the following three types of input data:

- a. High-level (0 to 5 volts) analog data.
- b. Subcommutated PAM data from 0 to 5 volts.
- c. Parallel digital data, consisting of eight digital data bits and one control bit.

1-17. The sampling sequence of the external inputs is determined by the wiring of the programmable patchboard. The 128 primary gate control signals from the programmer are connected to isolated terminals on the patchboard. Selected analog gate lines, driver inputs, and inhibit logic input points are also routed to isolated patchboard terminals. Hardwire jumpers from one patchboard terminal to another enable the proper analog gate, driver, and/or inhibit logic at a desired time during a prime frame.

1-18. Incoming analog data passes through the particular analog gate programmed to accept data, then it is routed to the analog-to-digital (A/D) converter. (Each time an analog gate is enabled, an analog gate busy signal is fed to the inhibit logic which, in turn, generates a data inhibit pulse.) The analog-to-digital converter compares the incoming analog data to a known reference voltage, then converts it into an eight-bit binary equivalent. The conversion is accomplished by an approximation-by-halves technique. After the data is converted, it is stored in the A/D register until it is transferred to the parallel-to-serial converter by a timer control signal. The parallel-to-serial converter changes the parallel A/D data into a serial NRZ-S format in synchronism with the data rate timing. The PCM output data is, however, delayed one primary gate control signal period from the particular primary gate control channel occurring at the time of data output. For example, the data sampled during primary gate control channel 1 time is shifted out of the C14-210-0003 during primary gate control channel 2 time.

1-19. Acceptance of digital data by the C14-210-0003 is dependent upon the presence of a digital control bit in the digital input word. If the nine-bit digital word contains a positive control bit greater than two volts in amplitude, the C14-210-0003 will accept and process this data; otherwise, it will be rejected. Parallel digital data inputs are applied directly to the parallel-to-serial converter for conversion to NRZ-S serial PCM format. This data is interleaved with the digitized equivalents of the analog inputs according to the program patchboard schedule.

1-20. Prevention of the simultaneous acceptance of digitized analog and external digital input data by the parallel-to-serial converter is accomplished by the state of the control bit. Each time an analog gate is energized, the C14-210-0003 generates a negative data inhibit pulse. The data inhibit pulse may be used by external equipment to generate a control bit input. A positive control bit causes the parallel-to-serial converter to accept digital information and a zero control bit causes it to accept digitized analog information.



1-21. The power supply assembly (not shown in figure 1-2) is a dc-to-dc converter unit which provides the necessary conversion and regulation of the voltages required to operate the analog and digital circuitry of the C14-210-0003.

1-22. A more complete discussion of the major functional stages comprising the C14-210-0003 is presented in the following paragraphs.

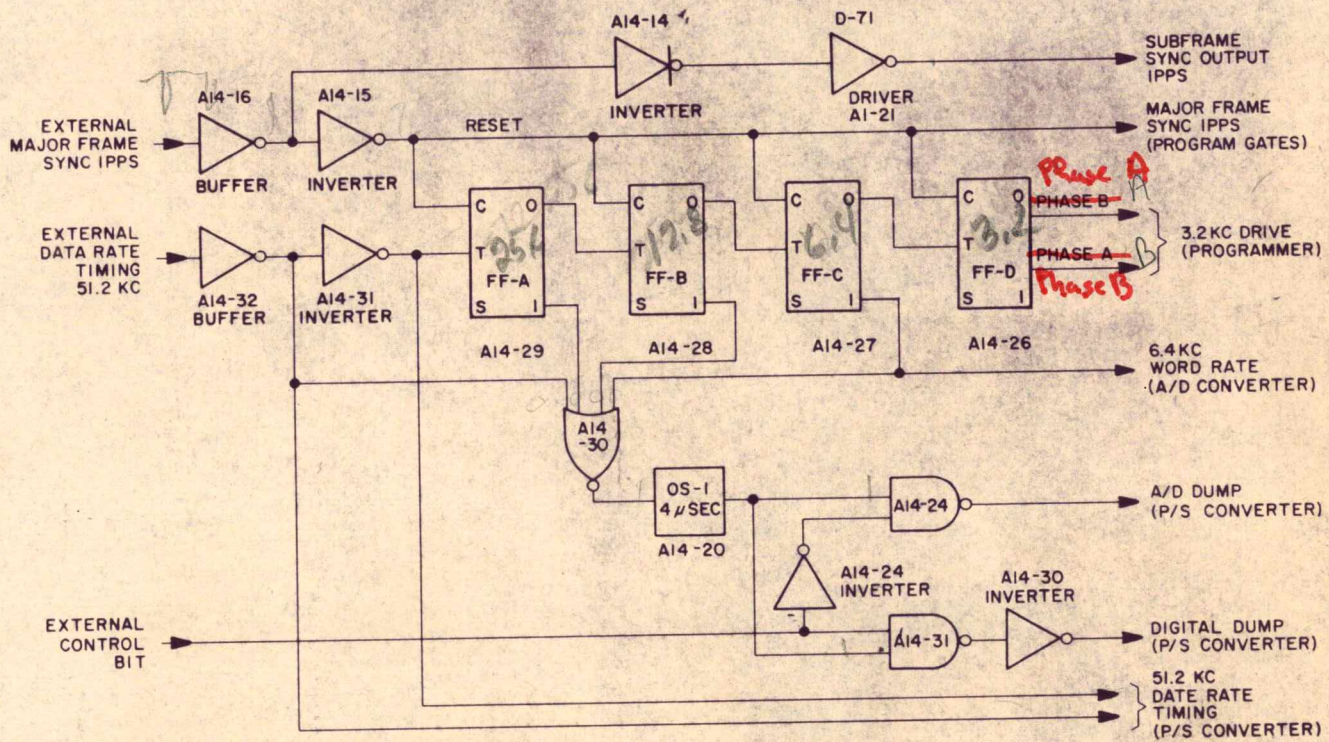
1-23. **TIMER SECTION.** A simplified logic diagram of the timer section is shown in figure 1-3. Basically, the timer section accepts the data rate timing and major frame synchronization inputs and uses these signals and their submultiples to control the operation and synchronize the data output of the C14-210-0003. Waveforms illustrating the timing relationship of the signals generated by this section are depicted in figure 1-4.

1-24. External major frame synchronization and data rate timing are negative-going signals with amplitude levels of zero volts and minus 2.7 to minus 6.5 volts dc. The major frame sync pulse occurs once per second, while the data rate timing is a 50 percent duty cycle square wave occurring at a frequency of 51,200 pulses per second. The leading edges of these negative-going signals occur within 0.4 microseconds of each other.

1-25. The external major frame sync pulse is initially applied to input buffer stage A14-16. This stage inverts the sync pulse and also rejects any input pulses less negative than minus 1.5 volts dc. The output of A14-16 is re-inverted by module A14-15 and the leading edge of this negative-going pulse clears the four-stage counter (FF-A through FF-D), thus readying the counter for receipt of data rate timing pulses. The positive pulse output of buffer stage A14-16 is also fed to inverter module A14-14. The negative pulse output of A14-14 is current amplified by driver 71 (A1-21) and routed to an output connector as the subframe synchronization signal. The subframe sync signal is a 10-microsecond, negative pulse capable of driving an external load impedance ranging from 90 to 10,000 ohms.

1-26. The data rate timing input voltage levels are re-established as positive pulses by buffer module A14-32. (This module also rejects any input pulses less negative than minus 1.5 volts dc.) The positive output of the buffer is fed to the parallel-to-serial (P/S) converter and also is re-inverted by module A14-31. The negative-going output of inverter A14-31 feeds directly into the trigger input of the first counter stage FF-A. Flip-flops FF-A through FF-D are connected in a divide-by-sixteen, down-counter configuration. Each data rate timing pulse decreases the content of the down-counter one count until a maximum of 15 pulses have been received. Upon receipt of the 16th data rate timing pulse, the counter recycles to 1111, then continues to count down towards 0000 as additional pulses are received. Since there are eight data timing bits per word and FF-C goes through two changes of state every eight data timing bits, its output is referred to as the word rate clock. This signal is routed to the A/D converter as a control signal for the analog conversion process.





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Figure 1-3. Timer Section, Simplified Logic Diagram



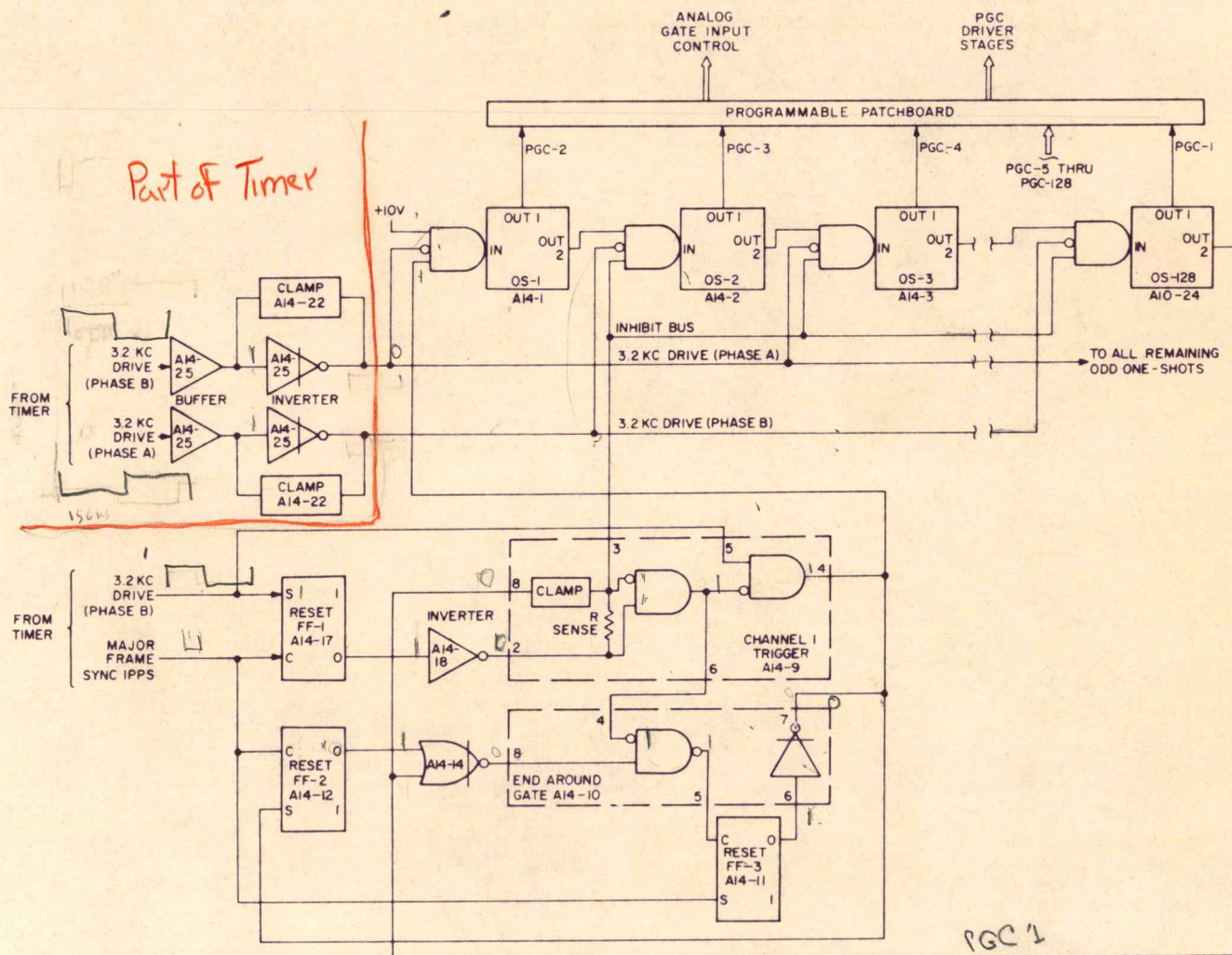
1-27. The one-side outputs of FF-A through FF-C are fed into NOR gate A14-30, together with the inverted data rate timing output of module A14-32. NOR gate A14-30 is used to detect the last data rate timing pulse occurring in each data word. To satisfy this gate and provide a positive-going trigger pulse to one-shot-1 (OS-1) A14-20, all four input signals must be at a low level (logical ZERO). As shown in the waveform diagram (figure 1-4), this condition occurs only during the first portion of each eighth data rate timing pulse. The leading edge of the positive output of NOR gate A14-30 triggers OS-1, thus generating a four-microsecond pulse each time a group of eight data rate timing pulses have been received. These pulses are fed to a set of steering NAND gates (A14-24 and A14-31), together with an external digital control bit. The coincidence of a positive control bit and the four-microsecond pulse output of OS-1 generates a negative-going, four-microsecond pulse at the output of NAND gate A14-31. This pulse is inverted positive by module A14-30 and routed to the parallel-to-serial (P/S) converter as the digital dump signal. Each time a control pulse is not received by the carry-on system, NAND gate A14-24 is enabled. Occurrence of a four-microsecond, OS-1 output pulse during this time period will generate a negative-going, four-microsecond pulse at the output of NAND gate A14-24. This pulse is routed to the P/S converter as the analog-to-digital (A/D) dump signal.

1-28. PROGRAMMER AND TIMING GATES. The programmer and timing gates section shown in figure 1-5 consists of a modified 128-stage ring counter (programmer) and associated gating circuitry (timing gates) necessary to synchronize and restart the operation of the programmer. In figure 1-5, each programmer stage is represented by a three-input AND circuit directly feeding a one-shot. For purposes of simplicity, programmer stages 4 through 127 have been omitted from this figure. Odd-numbered programmer stages (5, 7, 9, etc.) not shown in figure 1-5 operate essentially the same as OS-3, while, the even numbered stages (4, 6, 8, etc.) omitted, operate similar to OS-2.

1-29. The programmer provides primary gate control (PGC) pulses to control the commutating of 128 channels of input data. Synchronization of the programmer is controlled by the external major frame sync pulse at a one pulse-per second rate, and resetting is effected at a 50 pulse-per second rate by the output of the 128th stage being returned to the input of the first stage through a series of timing gates.

1-30. The channel 1 trigger module A14-9 and the end-around gate module A14-10 operate in conjunction with each other in the generation of the channel 1 trigger for programmer one-shot-1 (OS-1). The channel 1 trigger module generates an output when any one of the following three conditions occur: 1) receipt of major frame sync; 2) programmer one-shot-128 generates an output; and, 3) any one of the programmer one-shots fails to operate. The end-around gate recognizes the first two preceding conditions as normal and permits the channel 1 trigger generated by module A14-9 to be applied to OS-1. The third condition, however, is identified by the end-around gate module as abnormal system operation and the pin 7 output of this module inhibits the trigger pulse from being applied to OS-1.





M1509-5

Figure 1-5. Programmer & Timing Gates, Simplified Logic Diagram



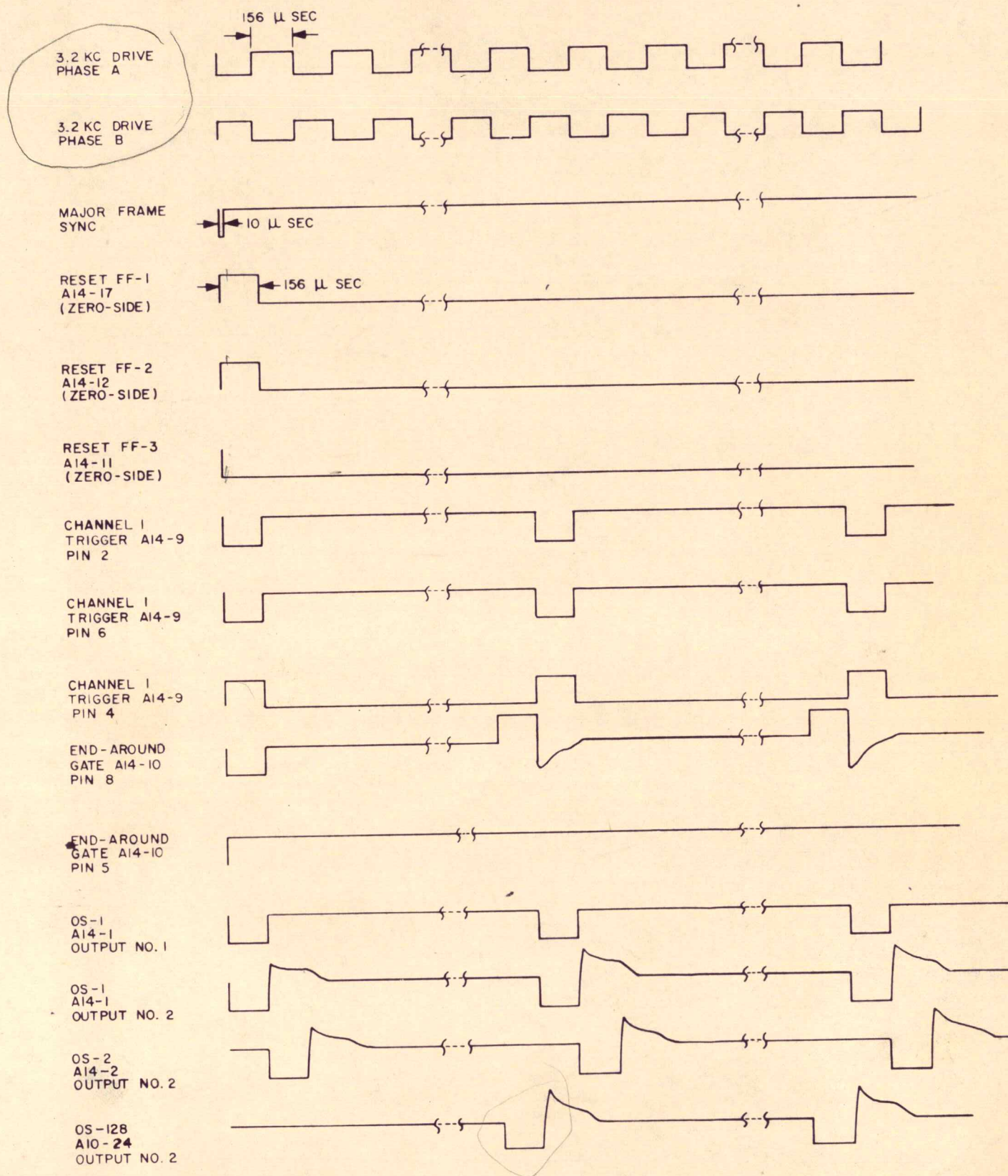


Figure 1-6. Programmer &amp; Timing Gates. Waveform Diagram

M1509-6



1-31. The positive-going pulse necessary to trigger OS-1 into operation is obtained from the pin 4 output of the channel 1 trigger module A14-9. The end-around gate module A14-10 permits only the correct or true channel 1 trigger pulses to be applied to OS-1, and inhibits the generation of spurious channel 1 trigger pulses in the event of a programmer one-shot malfunction. This is accomplished by connecting the pin 4 output of module A14-9 and the pin 7 output of module A14-10 in parallel.

1-32. Synchronization of the programmer is initiated upon receipt of the major frame sync pulse. The leading edge of this pulse clears reset flip-flops -1 and -2, and sets reset flip-flop -3 to the ONE state. The states of reset flip-flops -2 and -3 disable the end-around gate module. The zero-side output of reset flip-flop -1 enables the channel 1 trigger module by effectively applying a logical ZERO level to the input to its second AND gate. During this time, the other input (3.2 kc, phase B drive) to the second AND gate is at a logical ONE level. Since this satisfies the input conditions for the second AND gate, a positive trigger output is generated at pin 4 of the channel 1 trigger module.

1-33. As shown in the waveform diagram (figure 1-6), reset flip-flop -1 remains in the ZERO state for approximately 156 microseconds after receipt of the major frame sync signal. During this period, the pin 3 output (inhibit bus) of the channel 1 trigger module is at a low (logical ZERO) level. Since programmer stages 2 through 128 obtain one of their gate inputs via pin 3 of the channel 1 trigger module, all of these stages are inhibited from operating whenever the inhibit bus is at a logical ZERO level. Consequently, the only programmer one-shot capable of being activated at this time is OS-1. (Since OS-1 has this same gate input directly connected to plus 10 volts, its operation is independent of the level of the inhibit bus.)

1-34. The positive-going, 156-microsecond output of the channel 1 trigger module is applied to the input AND gate of OS-1. At this time, the other variable input (3.2 kc phase A) to OS-1 is at a logical ZERO level. Since this satisfies the input conditions for this gate, OS-1 receives a trigger pulse input and the ring counter operation is initiated. The two outputs of OS-1 are both negative-going, 156-microsecond pulses. Output number one of OS-1 is routed directly to the programmable patchboard and is identified as primary gate control channel 2 (PGC-2) in figures 1-5 and 1-6. Output number two which contains the positive recycle of magnetic one-shot No. 1, is fed to the AND gate input of the succeeding one-shot, OS-2.

1-35. The trailing edge of the phase B, 3.2 kc drive pulse immediately following the major frame sync pulse sets reset flip-flop -1 (A14-17) to the ONE state and returns the level of the inhibit bus to a logical ONE, thus readying OS-2 through OS-128 for operation. The 3.2 kc, two-phase drive applied to the programmer alternately enables the odd-and even-numbered programmer stages. The positive recycle present in the trailing edge of output number two of OS-1 triggers one-shot programmer -2 into operation. One-shot programmer -2 also generates two output



signals similar to OS-1. Its number one output is routed to the patchboard as PGC-3 and the positive recycle present in its number two output is used to turn on OS-3. Thus, it can be observed that by connecting the number two output of each programmer stage to the input of the succeeding stage, a ring counter operation is effected. This sequence continues until OS-128 generates an output. The positive-going trailing edge of output number 2 of OS-128 is inverted by module A14-14 and used to inhibit the operation of the end around gate at this particular time. Each time one of the programmer stages (OS-2 through OS-128) connected to pin 3 of the channel 1 trigger module is generating a negative-going output signal, the current drawn through the sensing resistor (connected between terminals 2 and 3 of module A14-9) inhibits the output of the channel 1 trigger module. The channel 1 trigger pulse is prevented from being generated since the inhibit input to the second AND gate in module A14-9 will be at a high (logical ONE) level whenever reset flip-flop -1 is in the ZERO state and any one programmer one-shot is in operation. At the time when it is desired to generate a channel 1 trigger pulse (for example, at the trailing edge of the output of OS-128), there are no programmer one-shots in operation. This condition causes no voltage drop to occur across the sense resistor and the output of the first AND gate in the channel 1 trigger module assumes a low (logical ZERO) level. The resultant logical ZERO level applied to the inhibit input of the second AND gate in coincidence with the phase B, 3.2 kc drive signal causes the output of this gate to rise to a high (logical ONE) level, thus generating a channel 1 trigger pulse. The trigger pulse output of A14-9 is applied to the input of OS-1 and the feedback path from OS-128 to OS-1 is completed. The clamp circuit between terminals 8 and 3 of the channel 1 trigger module provides a pulse-sharpening action for the trailing edge of the output of OS-128, in order to closely synchronize its occurrence with that of the leading edge of the output of OS-1.

1-36. If a programmer one-shot failure occurs during the operation of the ring counter, the channel 1 trigger module is enabled and it attempts to generate a false channel 1 trigger. The end-around gate module, however, is also enabled at this time by the negative-going, pin 6 output of the channel 1 trigger module, and its pin 5 output clears reset flip-flop -3. The high, zero-side output of FF-3 is inverted by the end-around gate and the negative level pin 7 output of A14-10 inhibits the output of the channel 1 trigger module. Since FF-3 will remain in the zero state until the arrival of the next major frame sync pulse, the ring counter operation will be inhibited at the particular stage of the ring counter where the malfunction occurred. Receipt of the next major frame sync pulse will reset FF-1, FF-2, and FF-3, thus synchronizing the start of the programmer and initiating the ring counter operation.

1-37. Clamp modules A14-22 associated with each phase of the 3.2 kc drive signal provide a pulse-sharpening action for the trailing edges of the drive signals. Since each drive line has considerable distributed capacitance to ground due to the parallel effect of 64 programmer one-shots, the trailing edges of the drive signals tend to become deteriorated. Each clamp module generates a positive voltage output pulse coincident with the trailing edge of the drive pulses. This provides a current source to rapidly charge the distributed capacitance, thus permitting the drive



voltage level to return quickly to a ground level.

1-38. PROGRAMMABLE PATCHBOARD. The programmable patchboard is the inter-connection point for the 128 primary gate control output signals from the programmer, the enable lines for the 48 analog gates, the input lines to the PGC drivers, and the input lines to the data inhibit circuitry. Hardwire jumpers between selected points on the patchboard permit connecting any four of the 128 primary gate control (PGC) signals to any analog gate enable line, driver input, or inhibit input. The patching schedule selected for the C14-210-0003 is listed in table 1-1. Primary gate control channel numbers preceded by an asterisk in this table are outputs of the C14-210-0003. The other PGC channels are used for internal programming.

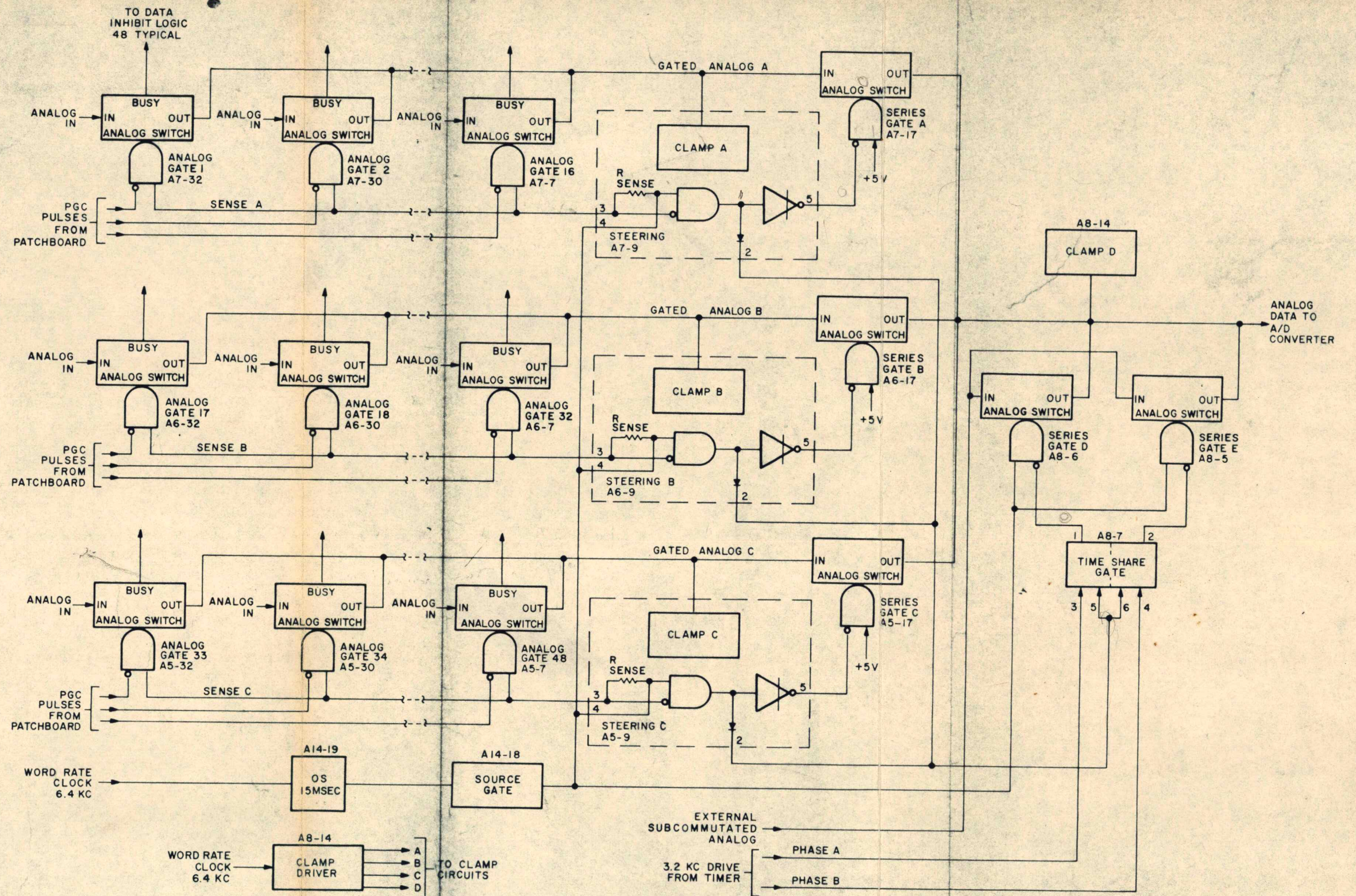
1-39. The programming schedule listed in table 1-1 provides for the acceptance of 42 high-level analog inputs, 69 digital data words, and subcommutated PAM data. Six analog gates (43 through 48) are reserved as spares and 16 analog gates are supercommutated at a sampling rate of 100 times per second. A total of 58 data inhibit pulses are generated for each prime frame of output data.

1-40. ANALOG GATES. A simplified diagram of the analog gates and associated circuitry is shown in figure 1-7. For purposes of simplicity, analog gates 3 through 15, 19 through 31, and 35 through 47 have been omitted from this diagram. Their operation, however, is essentially the same as that of the analog gates shown for each respective group.

1-41. In figure 1-7, the analog gates and series gates are represented by a two-input AND circuit driving an analog switch. Sixteen analog gates are grouped together and feed a common series gate. Each gate (analog or series) consists of a magnetic-core, blocking oscillator driver and a matched pair of switching transistors. The input conditions necessary to operate the blocking oscillator portion of this circuit are represented as a two-input AND gate. When the blocking oscillator is activated, it provides a transformer-coupled pulse to the two-transistor analog switch. The pulse output of the blocking oscillator drives the switching transistors into saturation and the analog data present at the input is transferred through the gate. This type of gating circuitry is characterized by its low value of offset voltage and the high degree of isolation between the analog input and the driver voltage. The analog switching transistors are oven-selected to minimize gate offset voltage throughout the entire operating temperature range of the C14-210-0003. Transformer coupling of the driver voltage completely isolates the analog input signal from the blocking oscillator drive signal.

1-42. To minimize the effects of stray capacitance and gate leakage resulting from paralleling the outputs of 48 analog gates, each group of 16 analog gates is connected to a series gate. This effectively reduces the capacitive loading of the analog source by a factor of approximately three. The series gate associated with each group of 16 analog gates is activated whenever one of the analog gates in that group is activated. This is accomplished by steering modules A5-9, A6-9, and A7-9.





MI 509-7

Figure 1-7. Analog Gates, Simplified Logic Diagram



Table 1-1. Patchboard Program Schedule

Programmer PGC Channel No.	Analog Gate No.	Data Inhibit No.	Digital Data Time (Control Bit)
*1			1
*2		(Prime Frame Sync)	
3	1	1	
*4			2
5	2	2	
*6			3
7	3	3	
*8			4
*9			5
10	4	4	
*11			6
12	5	5	
13	6	6	
*14			7
15	7	7	
*16			8
*17			9
*18			10
19	8	8	
*20			11
21	9	9	
*22			12
23	10	10	
*24			13
*25			14
26	11	11	



Table 1-1. Patchboard Program Schedule (cont )

Programmer PGC Channel No.	Analog Gate No.	Data Inhibit No.	Digital Data Time (Control Bit)
*27			15
28 ✓	12	12	
29 ✓	13	13	
*30			16
31 ✓	14	14	
*32			17
*33			18
*34			19
35 ✓	15	15	
*36			20
37 ✓	16	16	
*38			21
39 ✓	17	17	
*40			22
*41			23
42 ✓	18	18	
*43			24
44 ✓	19	19	
45 ✓	20	20	
*46			25
47 ✓	21	21	
*48			26
*49			27
*50			28
51 ✓	22	22	
*52			29



Table 1-1. Patchboard Program Schedule (cont )

Programmer PGC Channel No.	Analog Gate No.	Data Inhibit No.	Digital Data Time (Control Bit)
53✓	23	23	
*54			30
55✓	24	24	
*56			31
*57			32
58✓	25	25	
*59			33
60✓	26	26	
61✓	27	27	
*62			34
63✓	28	28	
*64			35
*65			36
*66			37
67✓	29	29	
*68			38
69✓	30	30	
*70			39
71✓	31	31	
*72			40
*73			41
74✓	4	32	
*75			42
76✓	5	33	
77✓	6	34	
*78			43
79✓	7	35	



Table 1-1. Patchboard Program Schedule (cont )

Programmer PGC Channel No.	Analog Gate No.	Data Inhibit No.	Digital Data Time (Control Bit)
*80			44
*81			45
*82			46
83✓	32	36	
*84			47
85✓	33	37	
*86			48
87✓	34	38	
*88			49
89✓	35	39	
90✓	11	40	
*91			50
92✓	12	41	
93✓	13	42	
*94			51
95✓	14	43	
*96			52
*97			53
*98			54
99✓	36	44	
*100			55
101✓	37	45	
*102			56
103✓	38	46	
*104			57
105✓	39	47	
106✓	18	48	



Table 1-1. Patchboard Program Schedule (cont )

Programmer PGC Channel No.	Analog Gate No.	Data Inhibit No.	Digital Data Time (Control Bit)
*107			58
108✓	19	49	
109✓	20	50	
*110			59
111✓	21	51	
*112			60
*113			61
*114			62
115✓	40	52	
*116			63
117✓	41	53	
*118			64
119✓	42	54	
*120			65
*121			66
122✓	25	55	
*123			67
124✓	26	56	
125✓	27	57	
*126			68
127✓	28	58	
*128			69



The clamp circuits (A, B, and C) shown in figure 1-7 are used to momentarily discharge the gated analog lines prior to the start of each analog sampling period. The first 15 microseconds of each sampling period is reserved for clamping. During the center five microseconds of this 15-microsecond period, the gated analog lines are discharged rapidly by the clamp circuit output to eliminate any residual voltage that may still be present on these lines from the previous sample.

1-43. Each time an analog gate is turned on, it generates a positive-going "busy" signal output which is routed to the data inhibit circuitry. The busy signal outputs are arranged in groups of eight analog gates, thus there is a total of six busy signal lines.

1-44. External subcommutated analog data is sampled alternately by series gates D and E whenever any one of the 48 analog gates is not sampling data. The outputs of these series gates are commoned together with the outputs of series gates A, B, and C, and routed to the analog-to-digital (A/D) converter. The combined outputs of the five series gates are also clamped during the first 15 microseconds of each sample period to minimize intermodulation.

1-45. Waveform diagrams depicting the timing relationship of the analog gate circuitry for four hypothetical sampling periods are shown in figure 1-8. Sampling periods one and two illustrate the acceptance of analog data by analog gate modules -1 and -2. The acceptance of external subcommutated analog data is illustrated during sampling periods three and four.

1-46. During sampling period one, the coincidence of a logical ZERO primary gate control pulse and a logical ONE source gate module output at the input of analog gate number 1 switches this gate on. (Note in figure 1-8 that the source gate module output does not reach a logical ONE level until after the line clamping has occurred.) *15 usec*  
The unipolar, zero to plus five-volt analog data applied to this gate is transferred to the input of series gate A module A7-17. The sense line A input to analog gate 1 draws its gate current through the sense resistor contained in steering module A (A7-9). Whenever this analog gate or any other analog gate contained in group A turns on, the current drawn through the sense resistor in module A7-9 lowers the voltage at pin 3 of this module, thus satisfying the conditions necessary to enable the steering module. The resultant negative-going output of steering module A turns on series gate A and allows the gated output of the analog gate to be transferred to the A/D converter. The positive-going pin 2 output of steering module A inhibits the time share gate during this time and prevents series gates D and E from accepting external subcommutated analog data. As shown by the waveform diagram, the operation of analog gate number 2 during sampling period two is quite similar to that just described for gate number 1. The analog output of gate number 2 is transferred through series gate A during the second sampling period. During this time, series gates D and E are again inhibited from accepting data.

1-47. During sampling periods three and four, all analog gates are off since it has been assumed that there are no primary gate control pulses being applied to the



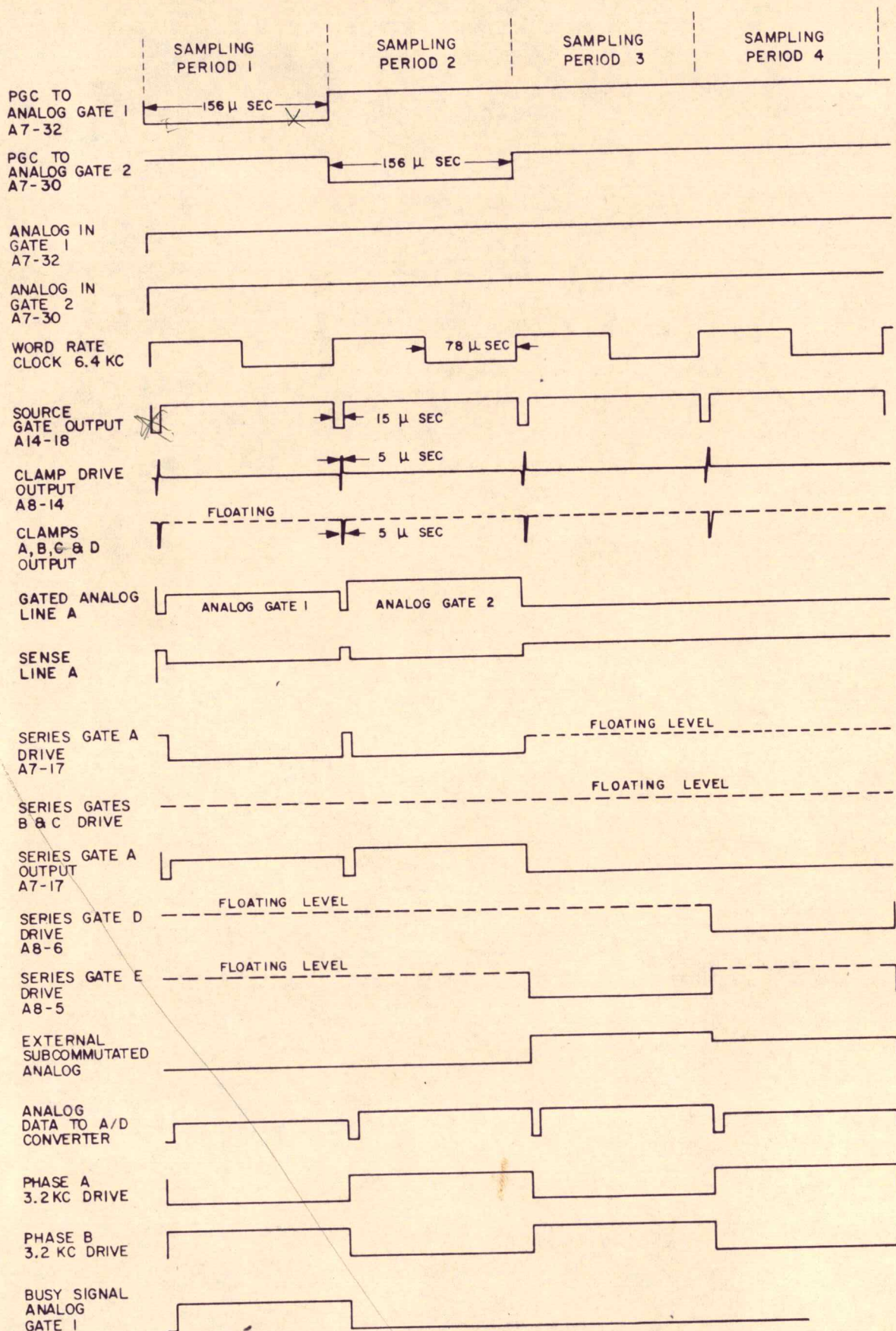


Figure 1-8. Analog Gates, Waveform Diagram

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analog gates. With all 48 analog gates not operating, the steering modules associated with series gates A, B, and C inhibit these series gates from operating. Series gates D and E, however, are enabled by the outputs of the time share gate module A8-7. The pin 2 output of the time share gate enables series gate E whenever all 48 analog gates are off and the phase B, 3.2 kc driver signal is at a logical ONE. This condition occurs during sample period three. The external subcommutated analog data is transferred through series gate E and routed to the A/D converter. During sample period four, the phase A, 3.2 kc drive signal is at a logical ONE and time share gate A8-7 is again enabled since all 48 analog gates are still in the off condition. The pin 1 output of the time share gate turns on series gate D and permits the external subcommutated data to be transferred to the A/D converter.

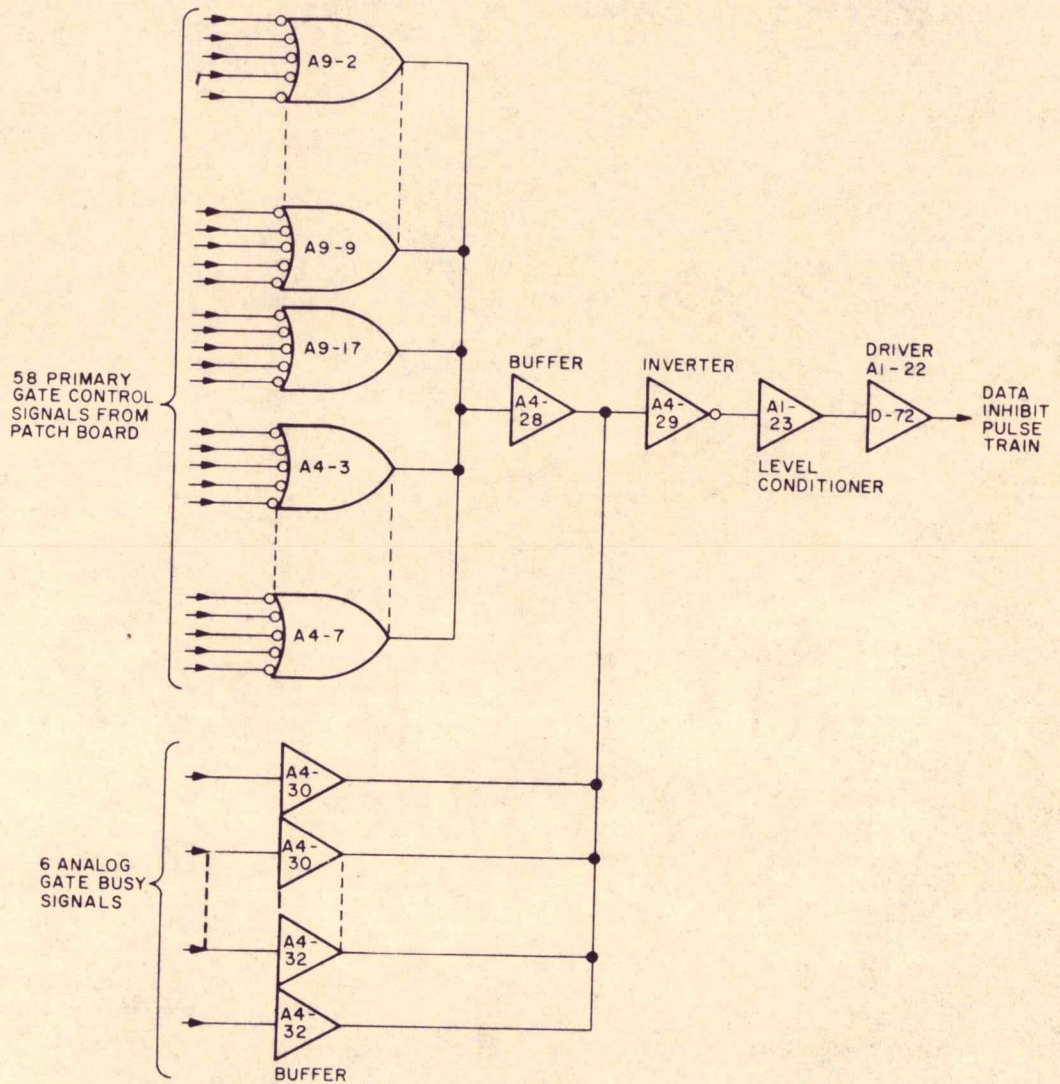
1-48. DATA INHIBIT. The data inhibit portion of the C14-210-0003, shown in figure 1-9, is used to generate a 156-microsecond, negative-going, data inhibit pulse whenever one of the 48 analog gates has been enabled. This is accomplished by ORING the 58 primary gate control pulses used to enable the analog gates with the busy-signal outputs of the analog gates. Fourteen OR gates, each activated by a negative PGC pulse, are used to detect when an analog gate has been enabled. The positive output of the OR gates is combined with the positive output of the six analog gate busy signals at the output of buffer module A4-28. Module A4-29 inverts this positive signal and its output is applied to level conditioner A1-23. The level conditioner clamps the data inhibit pulse levels at zero volts and minus six volts dc. The output of the level conditioner is applied to driver module -72 where the necessary current drive is obtained for the data inhibit output pulse train.

1-49. ANALOG-TO-DIGITAL CONVERTER. The analog-to-digital (A/D) converter accepts a word rate timing signal from the timer for synchronization, and analog data from the analog gates and external subcommutators for conversion to an eight-bit binary word. Encoding of the analog data takes place during the last half of the word rate timing signal, and the complete conversion process is accomplished in less than 50 microseconds.

1-50. Table 1-2 lists the analog-to-digital encoding values for the A/D converter. Note that an analog input of 0.00000 volts corresponds to a binary output of 00000001. The binary ONE bit contained in the output word for a zero-volt analog input is due to an intentional offset present in the comparison amplifier. Because of this offset, an analog input of 5.01000 volts or greater is required to produce a binary output of 11111111.

1-51. The simplified logic diagram and the associated waveform diagrams for the analog-to-digital converter are shown in figures 1-10 and 1-11, respectively. The common output of the series analog gates is fed as a zero-to five-volt PAM wave-train to the A/D converter for digitizing. The A/D converter operates on the principle of "successive approximations by halves". The incoming analog signal is first compared with a precise reference voltage of 2.50988 volts to establish the value of the most significant bit. After this is determined, the input signal is then





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Figure 1-9. Data Inhibit Circuitry, Simplified Logic Diagram



Table 1-2. Analog-To-Digital Encoding Values

Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB
0.00000	00000001	0.79051	00101001	1.58103	01010001
0.01976	00000010	0.81028	00101010	1.60079	01010010
0.03953	00000011	0.83004	00101011	1.62055	01010011
0.05929	00000100	0.84980	00101100	1.64032	01010100
0.07905	00000101	0.86957	00101101	1.66008	01010101
0.09881	00000110	0.88933	00101110	1.67984	01010110
0.11858	00000111	0.90909	00101111	1.69960	01010111
0.13834	00001000	0.92885	00110000	1.71937	01011000
0.15810	00001001	0.94862	00110001	1.73913	01011001
0.17787	00001010	0.96838	00110010	1.75889	01011010
0.19763	00001011	0.98814	00110011	1.77866	01011011
0.21739	00001100	1.00791	00110100	1.79842	01011100
0.23715	00001101	1.02767	00110101	1.81818	01011101
0.25692	00001110	1.04743	00110110	1.83794	01011110
0.27668	00001111	1.06719	00110111	1.85771	01011111
0.29644	00010000	1.08696	00111000	1.87747	01100000
0.31621	00010001	1.10672	00111001	1.89723	01100001
0.33597	00010010	1.12648	00111010	1.91700	01100010
0.35573	00010011	1.14625	00111011	1.93676	01100011
0.37549	00010100	1.16601	00111100	1.95652	01100100
0.39526	00010101	1.18577	00111101	1.97628	01100101
0.41502	00010110	1.20553	00111110	1.99605	01100110
0.43478	00010111	1.22530	00111111	2.01581	01100111
0.45455	00011000	1.24506	01000000	2.03557	01101000
0.47431	00011001	1.26482	01000001	2.05534	01101001
0.49407	00011010	1.28458	01000010	2.07510	01101010
0.51383	00011011	1.30435	01000011	2.09486	01101011
0.53360	00011100	1.32411	01000100	2.11462	01101100
0.55336	00011101	1.34387	01000101	2.13439	01101101
0.57312	00011110	1.36364	01000110	2.15415	01101110
0.59289	00011111	1.38340	01000111	2.17391	01101111
0.61265	00100000	1.40316	01001000	2.19368	01110000
0.63241	00100001	1.42292	01001001	2.21344	01110001
0.65217	00100010	1.44269	01001010	2.23320	01110010
0.67194	00100011	1.46245	01001011	2.25296	01110011
0.69170	00100100	1.48221	01001100	2.27273	01110100
0.71146	00100101	1.50198	01001101	2.29249	01110101
0.73123	00100110	1.52174	01001110	2.31225	01110110
0.75099	00100111	1.54150	01001111	2.33202	01110111
0.77075	00101000	1.56126	01010000	2.35178	01111000



Table 1-2. Analog-To-Digital Encoding Values (cont )

Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB
2.37154	01111001	3.16206	10100001	3.95257	11001001
2.39130	01111010	3.18182	10100010	3.97233	11001010
2.41107	01111011	3.20158	10100011	3.99209	11001011
2.43083	01111100	3.22134	10100100	4.01186	11001100
2.45059	01111101	3.24111	10100101	4.03162	11001101
2.47036	01111110	3.26087	10100110	4.05138	11001110
2.49012	01111111	3.28063	10100111	4.07115	11001111
2.50988	10000000	3.30040	10101000	4.09091	11010000
2.52964	10000001	3.32016	10101001	4.11067	11010001
2.54941	10000010	3.33992	10101010	4.13043	11010010
2.56917	10000011	3.35968	10101011	4.15020	11010011
2.58893	10000100	3.37945	10101100	4.16996	11010100
2.60870	10000101	3.39921	10101101	4.18972	11010101
2.62846	10000110	3.41897	10101110	4.20949	11010110
2.64822	10000111	3.43874	10101111	4.22925	11010111
2.66798	10001000	3.45850	10110000	4.24901	11011000
2.68775	10001001	3.47826	10110001	4.26877	11011001
2.70751	10001010	3.49802	10110010	4.28854	11011010
2.72727	10001011	3.51779	10110011	4.30830	11011011
2.74704	10001100	3.53755	10110100	4.32806	11011100
2.76680	10001101	3.55731	10110101	4.34783	11011101
2.78656	10001110	3.57708	10110110	4.36759	11011110
2.80632	10001111	3.59684	10110111	4.38735	11011111
2.82609	10010000	3.61660	10111000	4.40711	11100000
2.84585	10010001	3.63636	10111001	4.42688	11100001
2.86561	10010010	3.65613	10111010	4.44664	11100010
2.88538	10010011	3.67589	10111011	4.46640	11100011
2.90514	10010100	3.69565	10111100	4.48617	11100100
2.92490	10010101	3.71542	10111101	4.50593	11100101
2.94466	10010110	3.73518	10111110	4.52569	11100110
2.96443	10010111	3.75494	10111111	4.54545	11100111
2.98419	10011000	3.77470	11000000	4.56522	11101000
3.00395	10011001	3.79447	11000001	4.58498	11101001
3.02372	10011010	3.81423	11000010	4.60474	11101010
3.04348	10011011	3.83399	11000011	4.62451	11101011
3.06324	10011100	3.85375	11000100	4.64427	11101100
3.08300	10011101	3.87352	11000101	4.66403	11101101
3.10277	10011110	3.89328	11000110	4.68379	11101110
3.12253	10011111	3.91304	11000111	4.70356	11101111
3.14229	10100000	3.93281	11001000	4.72332	11110000



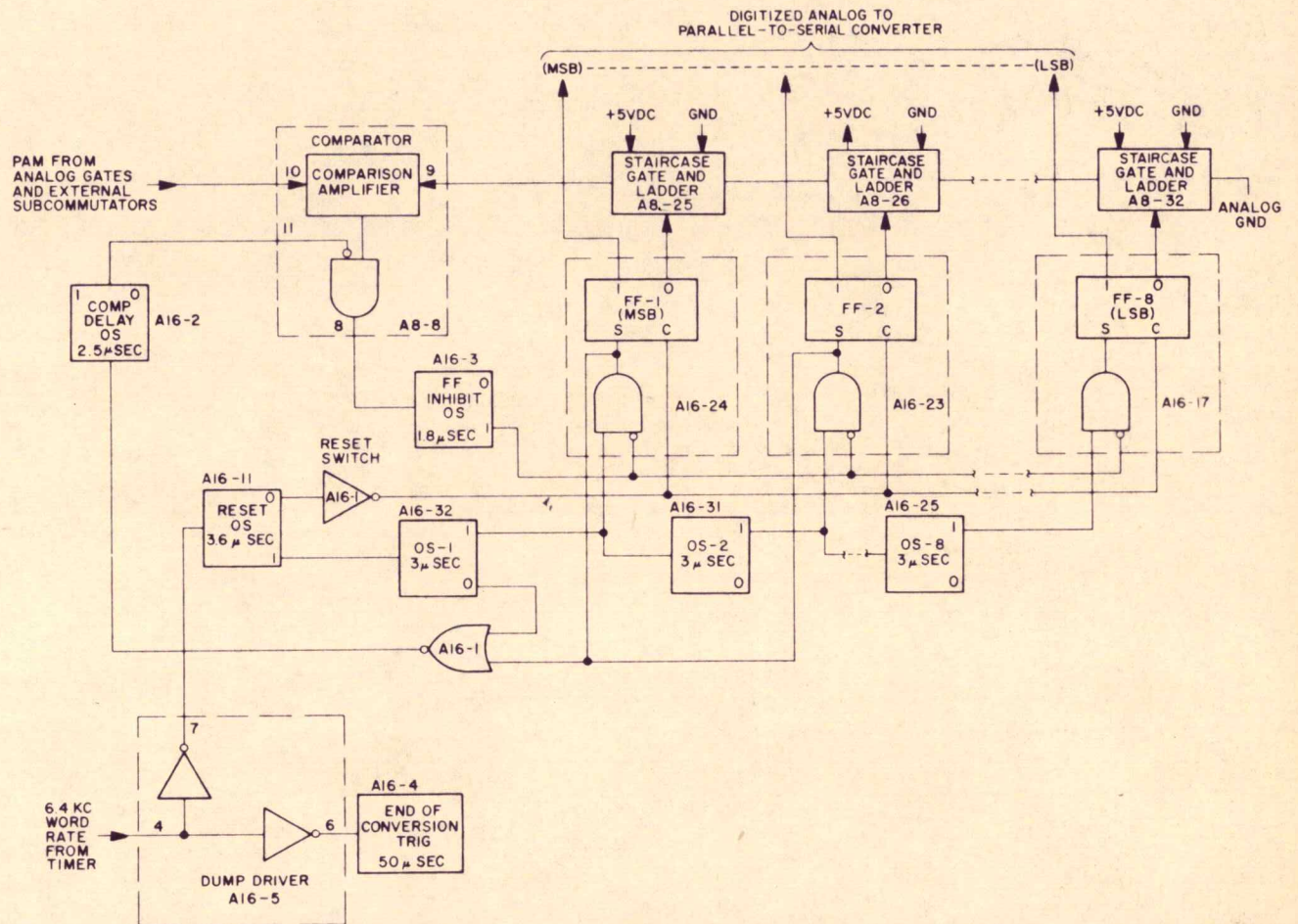
Table 1-2. Analog-To-Digital Encoding Values (cont)

Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB	Analog Voltage Input	Digital Output MSB LSB
4.74308	11110001	4.84190	11110110	4.94071	11111011
4.76285	11110010	4.86166	11110111	4.96047	11111100
4.78261	11110011	4.88142	11111000	4.98024	11111101
4.80237	11110100	4.90119	11111001	5.00000	11111110
4.82213	11110101	4.92095	11111010		

compared with 1.24506 volts (or 3.77470 volts) to generate the second bit. This comparison technique is repeated until the ONE or ZERO determination of each bit in the eight-bit conversion process is completed. At the end of the conversion, the eight-bit word is stored in the flip-flop register (FF-1 through FF-8) of the A/D converter. The one-side outputs of these flip-flops constitute the parallel output of the A/D converter. This information is transferred to the parallel-to-serial converter at A/D dumptime which occurs at the end of the word rate timing signal.

1-52. The conversion of each analog sample is initiated by the positive-going edge of the word rate signal input to dump driver module A16-5. The word rate signal is inverted by the dump driver and the negative pulse output of this module is used to trigger reset one-shot A16-11 into operation. The negative 3.6-microsecond output pulse of the reset one-shot is inverted by the reset switch module and the leading edge of the inverted pulse output of this module is used to clear the eight-stage, A/D converter storage register. The trailing edge of the one-side output of the reset one-shot triggers into operation the first of a series of eight A/D one-shots. The leading edge of the one-side output of the first A/D one-shot (OS-1) sets the most-significant-bit flip-flop (FF-1) to the ONE state. The zero-side output of this flip-flop switches the input to the staircase gate and ladder module A8-25 to a precise, plus five-volt reference supply. The negative pulse output of OS-1 is differentiated and inverted by NOR gate A16-1. The input circuit of this gate does not respond to positive-going pulses, thus, only the negative-going leading edge of the input pulse is inverted by A16-1. The positive pulse output of A16-1 triggers the comparator delay one-shot into operation. Two and one-half microseconds after the comparator delay one-shot receives a trigger pulse input, it provides a negative enable pulse to the comparator AND gate contained in module A8-8. During this time, the comparator's comparison amplifier has been comparing the incoming analog data with the output of the staircase ladder network. Since only FF-1 has been set to the ONE state, the ladder voltage input applied to pin 9 of the comparator is at 2.50988 volts. (See table 1-2.) If the analog input to the comparator is less than 2.50988 volts, the other input to the comparator AND gate (i.e., the comparison amplifier output) will remain at a logical ZERO and the flip-flop inhibit one-shot

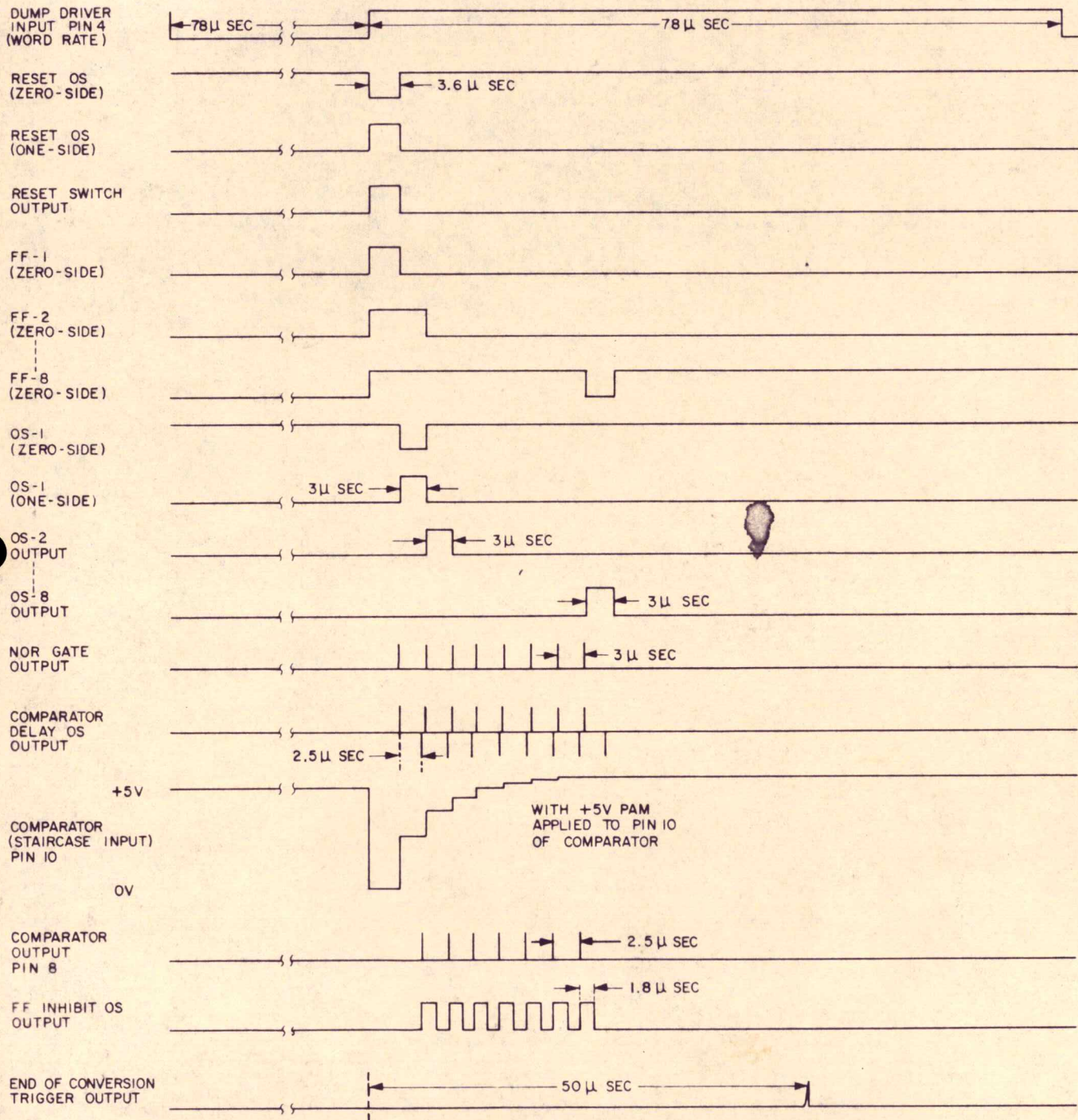




MI 509-10

Figure 1-10. Analog-to-Digital Converter, Simplified Logic Diagram





MI509-11

Figure 1-11. Analog-to-Digital Converter, Waveform Diagram



module A16-3 will not be triggered into operation. Therefore, the trailing edge of the one-side output of OS-1 will change the state of the most-significant-bit flip-flop (FF-1) back to a logical ZERO. If the analog input to the comparator is greater than 2.50988 volts, the comparison amplifier output will be at a logical ONE and the comparator AND gate will provide a positive trigger input to the flip-flop inhibit one-shot A16-3. The positive-going 1.8-microsecond pulse output of A16-3 inhibits the trailing edge of OS-1 from clearing FF-1, thus this flip-flop will remain in the ONE state and the conversion process will proceed to the next step. Note in the waveform diagrams that it has been assumed that a plus five-volt analog input has been applied to the A/D converter. For this assumption, the state of the most-significant-bit flip-flop would remain as a logical ONE for the first comparison. The trailing edge of the one-side output of OS-1 triggers both OS-2 and the comparator delay one-shot A16-2. The one-side output of OS-2 sets FF-2 to the ONE state which, in turn, raises the staircase output voltage to 3.77470 volts by also switching the input to staircase gate and ladder module A8-26 to the five-volt reference supply. During the three-microseconds that OS-2 is in operation, the comparison amplifier compares the new value of staircase voltage to that of the incoming analog voltage. Since it has been assumed that the analog input is plus five volts, FF-2 will be inhibited from reset during the occurrence of the trailing edge of the OS-2 output pulse and OS-3 (not shown) will be triggered into operation. This process continues until OS-8 has been triggered. At this time, the comparator will not generate an output pulse to the flip-flop inhibit one-shot since the incoming analog is at a lower value than the staircase voltage with all eight A/D flip-flops in the ONE state. The trailing edge of OS-8 will reset FF-8 to the ZERO state and, thus, complete the conversion process for the incoming analog data.

1-53. The one-side outputs of FF-1 through FF-8 are applied in parallel to eight AND gates in the parallel-to-serial converter. Upon the occurrence of an analog-to-digital (A/D) dump signal at the end of the word rate timing cycle, the eight-bit parallel output of the A/D converter is transferred to the parallel-to-serial converter.

1-54. PARALLEL-TO-SERIAL CONVERTER. The parallel-to-serial (P/S) converter accepts both an external, eight-bit, parallel digital word and the eight-bit, parallel output of the A/D converter, and changes these inputs to a non-return-to-zero, serial PCM format.

1-55. A simplified logic diagram of the P/S converter is shown in figure 1-12. The converter essentially consists of an eight-stage, serial shift/storage register with AND/OR gate inputs, a shaping flip-flop, and associated steering gates.

1-56. A timing diagram showing the waveforms generated within the P/S converter during the serialization of digitized analog data is shown in figure 1-13. This figure illustrates the signals generated during receipt of an A/D dump signal, however, operation of the P/S converter upon receipt of a digital dump signal is essentially the same as shown in figure 1-13.



1-57. The P/S conversion process is initiated by the receipt of either an A/D dump signal or a digital dump signal. (The generation of the dump signals was described previously in paragraph 1-27.) The A/D dump signal transfers in parallel the eight-bit digitized output of the A/D converter into the P/S converter's shift/storage register. The least-significant-bit is inserted into SR-1 and the most-significant-bit is inserted into SR-8. The data contained in the eight-stage shift/storage register is shifted from left to right in synchronism with the leading edge of the data rate timing signal. (The timing relationship of the data rate timing signal, shift pulses, and transfer pulse is shown in figure 1-13.) The first shift pulse occurring after parallel transfer of data into the register shifts the data stored in SR-1 to the input of SR-2, and so forth, until the data stored in SR-8 is shifted out of the register to the inputs of the steering NAND gates A and B. Upon the occurrence of the 10-microsecond, negative transfer pulse, the shifted data present at the inputs of SR-2 through SR-8 is transferred into the storage portion of these stages. The next shift pulse shifts the data contained in SR-2 through SR-8 one stage to the right, and the following transfer pulse transfers this data into SR-3 through SR-8. This process continues until all eight bits have been serially shifted out of SR-8.

1-58. As each data bit (logical ONE or ZERO) is shifted out of SR-8, it is NEEDED with the pulse output of one-shot A15-11, then applied to either the set or clear input of the shaping flip-flop A15-4. As shown in the waveform diagram, the 0.5 microsecond output of one-shot module A15-11 occurs in coincidence with the outputs of inverter module A15-2. Each time a logical ZERO is shifted out of SR-8, the output of NAND gate A sets the shaping flip-flop to the ONE state. A logical ONE output from SR-8 clears the shaping flip-flop. The zero-side output of the shaping flip-flop is a serial, non-return-to-zero signal containing the PCM equivalent of the input to the analog-to-digital converter. The output levels of the shaping flip-flop are conditioned by module A15-5, then current amplified by PCM driver module A15-16. The resultant output of A15-16 is a serial PCM signal capable of driving 600 feet of RG-180B/U coaxial cable terminated with a 95-ohm load. Logic levels for the PCM output are plus 7 ( $\pm 1$ ) volts dc for a binary ONE and 0 ( $\pm 0.5$ ) volts dc for a binary ZERO.

1-59. The acceptance of external digital data by the P/S converter is dependent upon the presence of a positive control bit in the nine-bit digital word. The control bit is NEEDED with the plus two-volt reference output of buffer strobe module A15-9, and applied to the timer section. (The two-volt reference output of the buffer strobe module is used to establish an accept/reject voltage reference level for the incoming control bit. Control bits less than plus two volts are not accepted by the P/S converter.) The timer gates the control bit with the trailing edge of each eighth data rate timing pulse, and routes the resultant output pulse back to the P/S converter as a digital dump signal. The external digital data is transferred to the P/S converter's shift/storage register upon occurrence of the digital dump signal via eight AND gates (A15-25 through A15-17). Serialization of this data is accomplished in the same manner as described previously for a digitized analog input to the P/S converter.



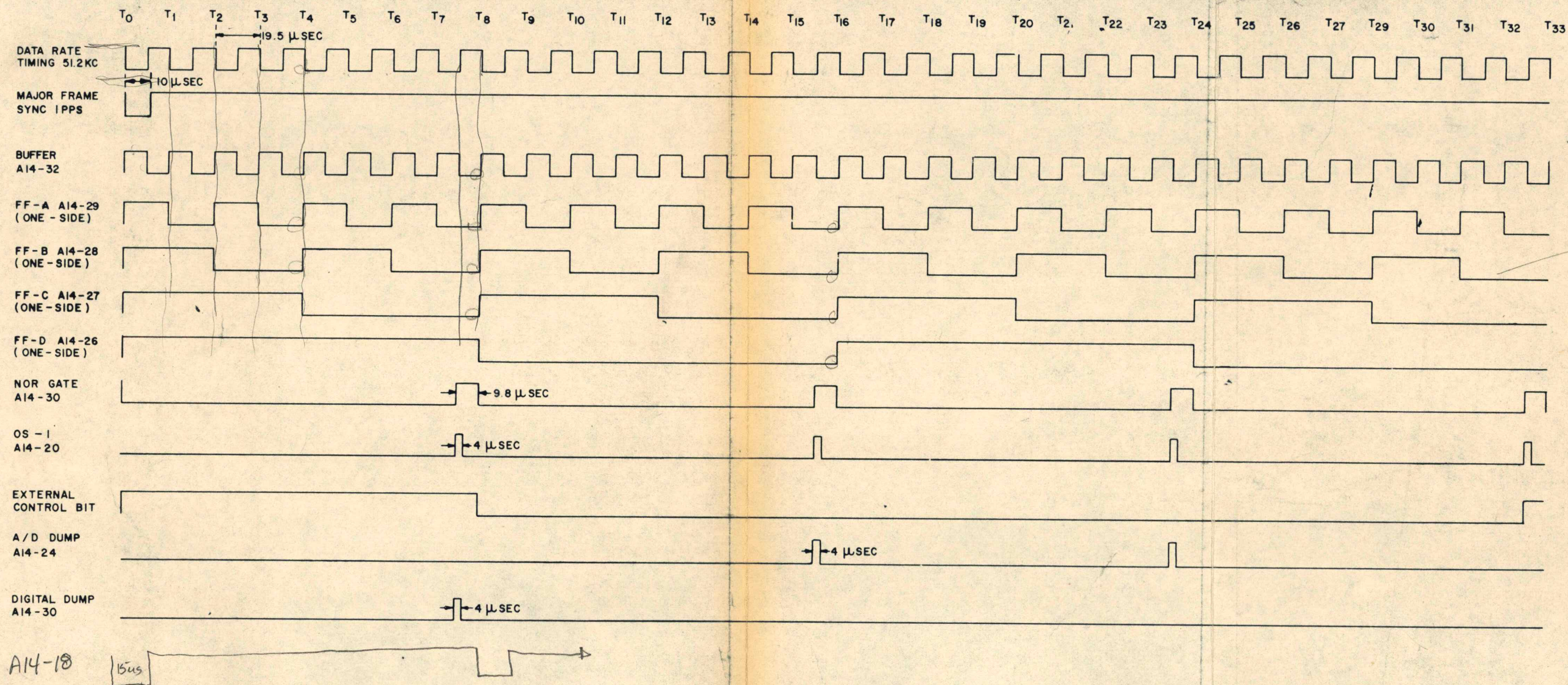


Figure 1-4. Timer Section, Waveform Diagram



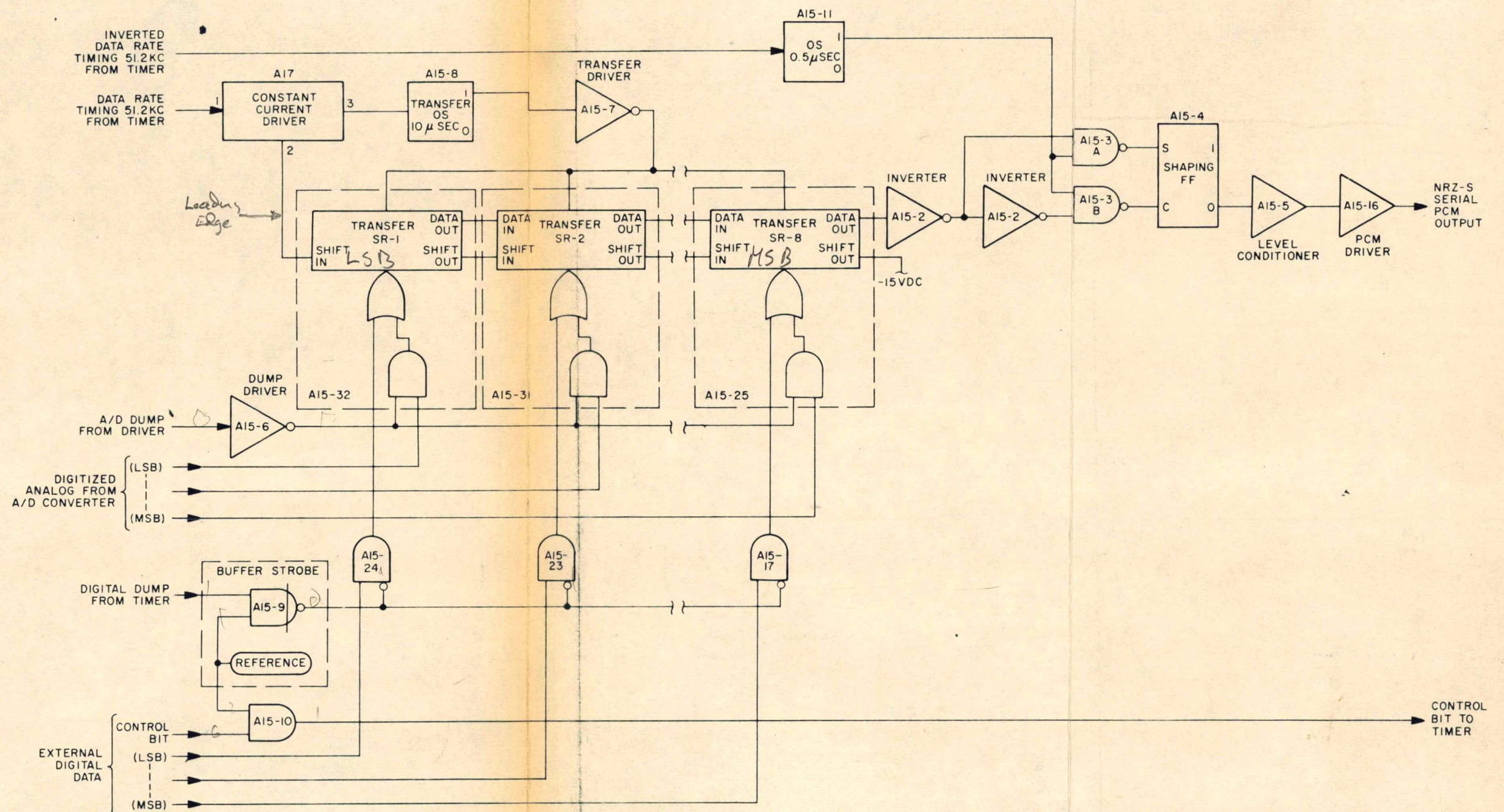
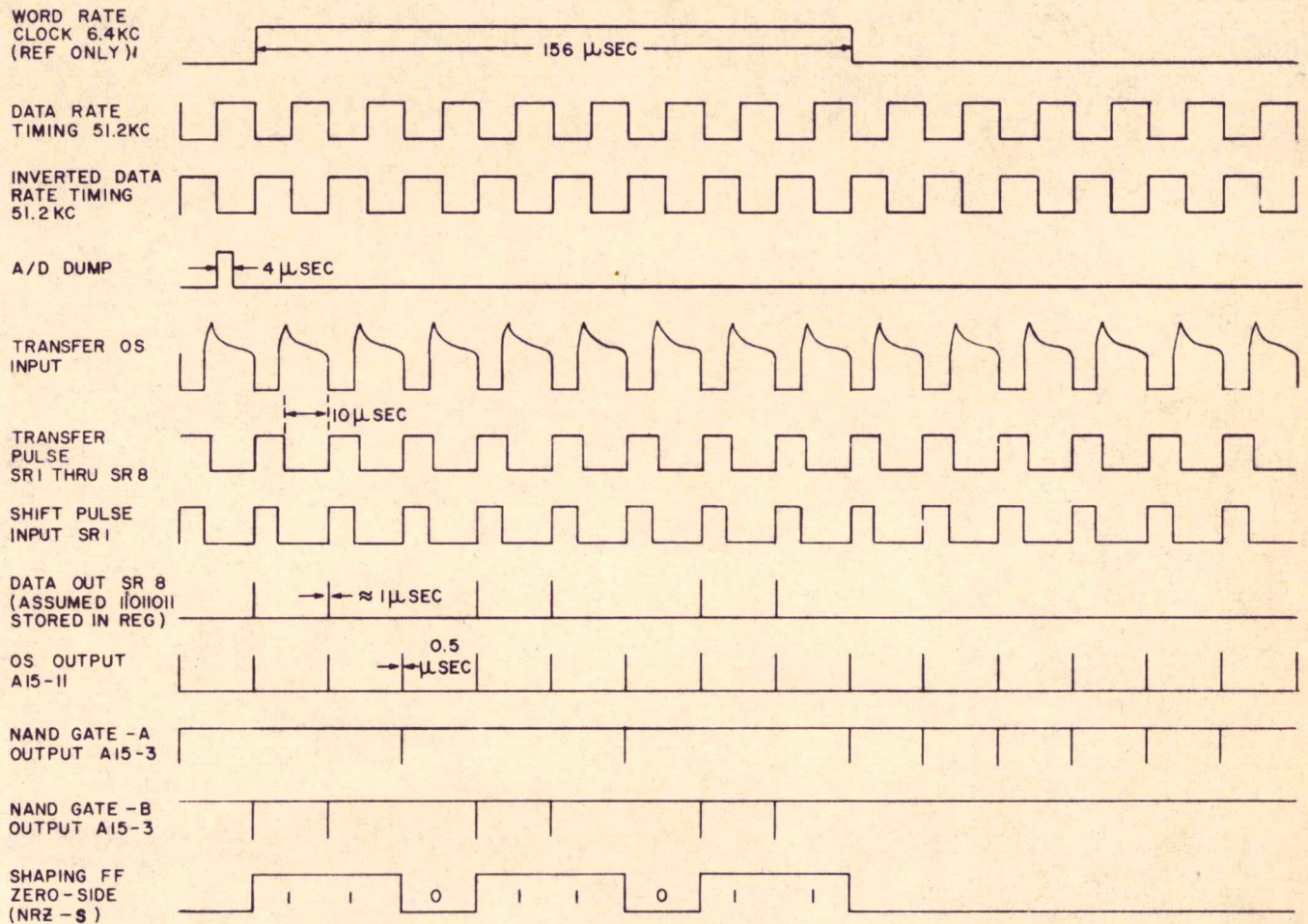


Figure 1-12. Parallel-to-Serial Converter, Simplified Logic Diagram





M1509-13

Figure 1-13. Parallel-to-Serial Converter,  
Waveform Diagram



## SECTION II

## FUNCTIONAL TEST

2-1. SCOPE.

2-2. This section contains test instructions for bench checkout of the C14-210-0003. Acceptable tolerances for test results are provided to indicate minimum performance standards. Corrective maintenance procedures for malfunctions observed during checkout are given in Section III, Trouble Analysis. The corrective action is identified in Section III by the associated step number of the functional test procedure contained in this section.

2-3. INPUT/OUTPUT SIGNAL CHARACTERISTICS.

2-4. Technical specifications for the input/output signals of the C14-210-0003 are as follows:

## a. Input Requirements

## 1. Timing Signals

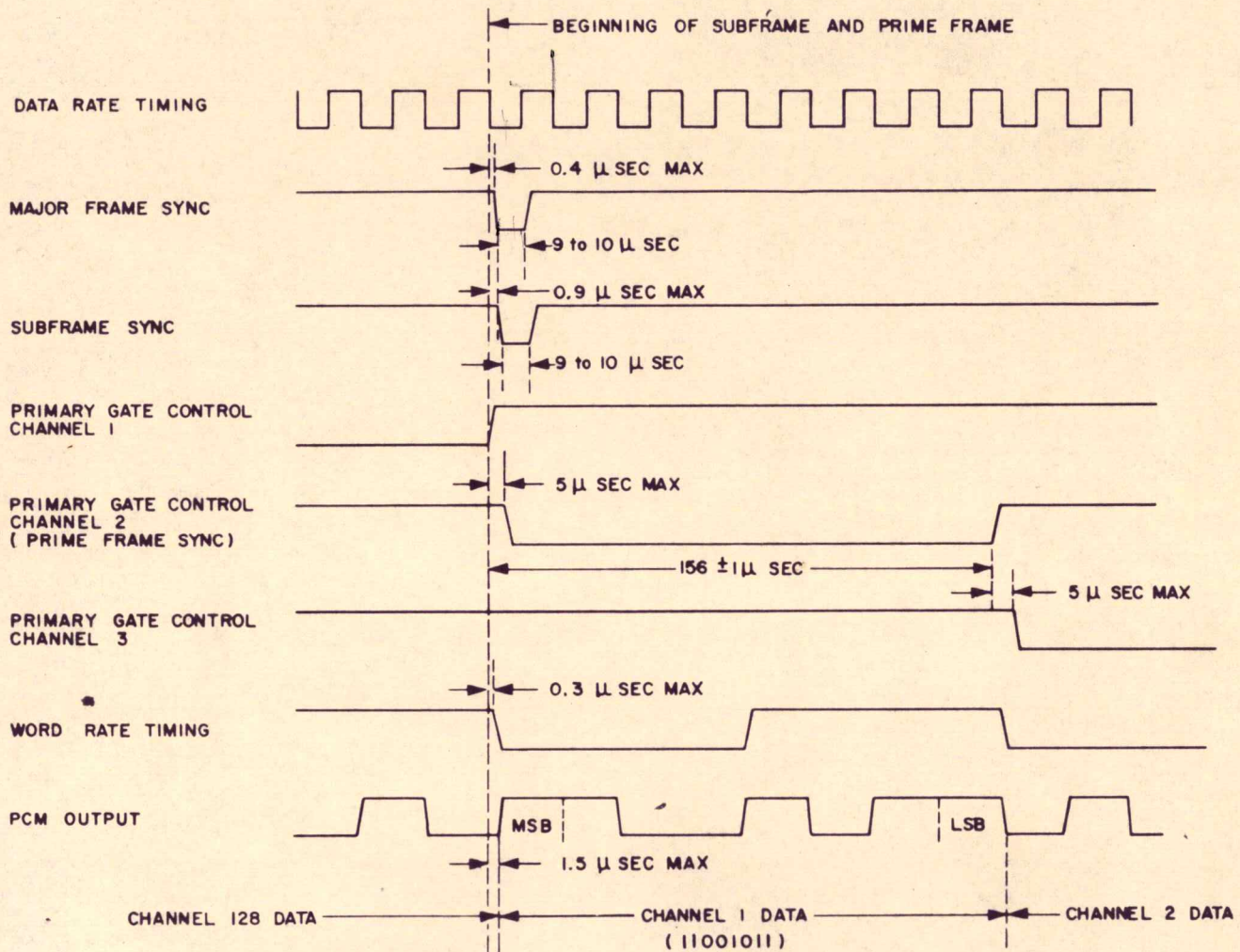
## (a) Data Rate Timing

- |                          |   |
|--------------------------|---|
| (1) Format:              | Negative square wave with a 50 ( $\pm 10$ ) percent duty cycle                          |
| (2) Frequency:           | 51,200 pulses per second  |
| (3) Source impedance:    | 95 ( $\pm 5$ ) ohms   |
| (4) Amplitude level:     | 0 ( $\pm 0.5$ ) vdc and -2.7 to -6.5 vdc  |
| (5) Jitter:              | $< \pm 1\%$ of bit period   |
| (6) Rise and fall time:  | $< 0.5$ microsecond   |
| (7) Frequency stability: | Long term, better than one part in $10^7$ ; short term, $\pm 0.1$ percent of bit period |

## (b) Major Frame Synchronization

- |                         |  |
|-------------------------|--|
| (1) Format:             | Negative pulse                           |
| (2) Width:              | 9 to 10 microseconds                     |
| (3) Frequency:          | 1 pulse per second                       |
| (4) Source impedance:   | 95 ( $\pm 5$ ) ohms                      |
| (5) Amplitude level:    | 0 ( $\pm 0.5$ ) vdc and -2.7 to -6.5 vdc |
| (6) Rise and fall time: | $< 0.5$ microsecond                      |
| (7) Synchronization:    | $< 0.4$ microsecond; see figure 2-1      |
|                         | (referenced to data rate timing)         |





M1509-14

Figure 2-1. C14-210-0003 Timing Diagram



## 2. Data

- (a) Gated Analog: Up to 48 high-level (0 to 5 volts), unipolar inputs
- (b) Subcommutated Analog: One high-level (0 to 5 volts), unipolar PAM wavetrain
- (c) Digital
  - (1) Format: 9 parallel bits per sample, consisting of 8 data bits and 1 control bit
  - (2) Amplitude level
    - a) Binary ONE: +3.5 to +10 vdc
    - b) Binary ZERO: 0 ( $\pm 0.5$ ) vdc
  - (3) Source Impedance: <5000 ohms
  - (4) Pulse width: One word time (156 ( $\pm 1$ ) microseconds)

## b. Output Characteristics

## 1. Control Signals

## (a) Subframe Synchronization

- (1) Format: Negative pulse
- (2) Width: 9 to 10 microseconds
- (3) Frequency: 1 pps
- (4) Output impedance: 45 to 165 ohms
- (5) Amplitude level (10K load): 0 ( $\pm 0.5$ ) vdc and -6 ( $\pm 0.5$ ) vdc
- (6) Jitter: < $\pm 0.1$  microsecond
- (7) Load impedance: 95 to 10,000 ohms to ground
- (8) Rise time: <0.2 microsecond
- (9) Fall time: <0.3 microsecond
- (10) Delay: See figure 2-1
- (11) Amplitude stability: Signal amplitude constant to within 0.2 volt peak-to-peak, dc to 1 megacycle, measured from  $T + 2$  microseconds to the next rise (or fall) time.  $T + 2$  microseconds is the 2 microseconds immediately after the previous rise (or fall) time.
- (12) Overshoot, undershoot, and ringing: <0.35 volt in amplitude and 2 microseconds in duration.
- (13) Current drive: 15 milliamperes dc,  $\pm 40$ -milliampere transient for 3 microseconds.



## (b) Data Inhibit

- (1) Format: Negative pulse train comprised of 58 PGC channels per prime frame.
- (2) Pulse width: 156 ( $\pm 1$ ) microsecond (one word time), including delay time
- (3) Frequency of occurrence: See table 1-1.
- (4) Output impedance: 45 to 165 ohms
- (5) Amplitude level (10K load): 0 ( $\pm 0.5$ ) vdc and -6 ( $\pm 0.5$ ) vdc
- (6) Load impedance: 95 to 10,000 ohms to ground
- (7) Pulse delay: <10 microseconds, measured between 90 percent levels of data inhibit pulse and corresponding primary gate control channel which generated the pulse
- (8) Rise time: <0.5  $\mu$ second
- (9) Fall time: <1  $\mu$ second
- (10) Current drive: 3 milliamperes dc,  $\pm 10$ -milliampere transient, for 3 microseconds

## (c) Primary Gate Control Channels (PGC)

- (1) Format: 70 sequenced outputs; refer to starred PGC signals in table 1-1.
- (2) Width: 156 ( $\pm 1$ ) microseconds (one word time), including delay time.
- (3) Frequency: 50 pulses per second for each output.
- (4) Output impedance: 45 to 165 ohms
- (5) Amplitude level (10K load): 0 ( $\pm 0.5$ ) vdc to -6 ( $\pm 0.5$ ) vdc
- (6) Rise time: <0.5 microsecond
- (7) Fall time: <1.0 microsecond
- (8) Load impedance: 95 to 10,000 ohms to ground
- (9) Delay: See figure 2-1.
- (10) Amplitude Stability: Signal amplitude constant to within 0.3 volt peak-to-peak, dc to 1 megacycle, measured from T+3 microseconds to the next rise (or fall) time. T+3 microseconds is the 3 microseconds immediately after the previous rise (or fall) time.
- (11) Overshoot, under-shoot, and ringing: <0.75 volt in amplitude and 3 microseconds in duration.
- (12) Current drive: 3 milliamperes dc



## 2. Data

## (a) PCM Output.

- (1) Format: 50 prime frames consisting of 128 words each.
- (2) Word length: Eight bits, straight binary; MSB first.
- (3) PCM type: NRZ-S
- (4) Bit rate: 51,200 bits per second
- (5) Delay: See figure 2-1.
- (6) Amplitude levels (95-ohm load): Binary ONE, +7 ( $\pm 1$ ) vdc; binary ZERO, 0 ( $\pm 0.5$ ) vdc.
- (7) Jitter:  $< \pm 0.1$  microsecond
- (8) Rise and fall times:  $< 0.3$  microsecond
- (9) Output impedance: 95 ( $\pm 5$ ) ohms
- (10) Frequency stability: Long term, better than one part in  $10^7$ ; short term,  $\pm 0.1$  percent of bit period.
- (11) Amplitude stability: Signal amplitude constant to within 0.3 volt peak-to-peak, dc to 1 megacycle, measured from T+2 microseconds to the next rise (or fall) time. T+2 microseconds is the 2 microseconds immediately after the previous rise (or fall) time.
- (12) Overshoots, undershoot, and ringing:  $< 0.35$  volt in amplitude and 2 microseconds in duration.

2-5. STANDARD TEST EQUIPMENT REQUIRED.

2-6. Table 2-1 lists the standard test equipment required to perform a functional test of the C14-210-0003.

Table 2-1. Standard Test Equipment Required for Functional Test

Description	Manufacturer	Application
Oscilloscope, cathode ray, delayed sweep with four-trace preamplifier	Tektronix, Model 545A or equivalent with a Tektronix, Type M plug-in unit or equivalent.	Monitor signals generated during test.
Power supply, 0 to 50 vdc, 0 to 1.5 amperes	Power Designs, Model 5015 or equivalent.	Provide +28 vdc input power to C14-210-0003.



Table 2-1. Standard Test Equipment Required for Functional Test (cont.)

Description	Manufacturer	Application
Reference supply, precision millivolt, 0 to $\pm 10$ vdc.	Electronic Development Company, Model MV-100 or equivalent.	Provide calibrated analog or digital input voltages.
Decade box, power resistor, 0 to 10,000 ohms.	Clarostat Model 240C or equivalent.	Provide 95- and 10,000 ohm loads during test.
Resistor, carbon composition, 5,000 ohms, 1/4 watt, 5 percent.	Allen Bradley or equivalent.	Provide proper output impedance for reference supply.
Counter, electronic frequency, six-digit.	Hewlett Packard, Model 523C or equivalent.	Used to initially set up frequency and time relationship of data rate timing and major frame sync pulse.
Voltmeter, digital, three-digit.	Hewlett Packard, Model 405BR or equivalent.	Used to measure voltages during functional test.

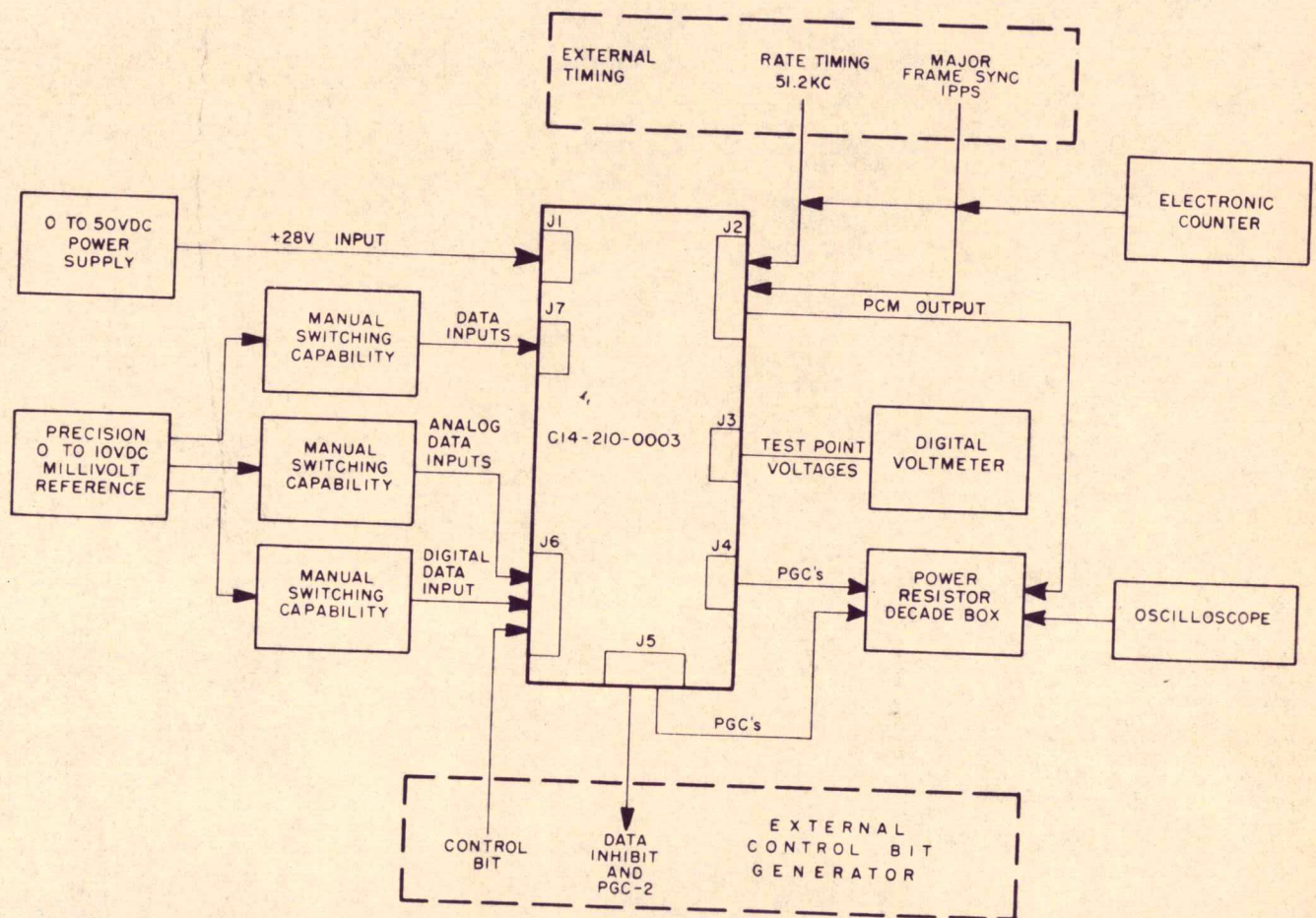
2-7. TEST EQUIPMENT SETUP.

2-8. Figure 2-2 illustrates the bench test setup for the test equipment used during functional test of the C14-210-0003. Specific test equipment interconnection points are identified in the functional test procedure. Table 2-2 is provided to serve as a convenient reference for input/output connector pin assignments and corresponding functional names.

Table 2-2. Connector Pin Assignments

Pin	Functional Assignment	Pin	Functional Assignment
J1	Bendix 71-74720-15P	J2	Bendix PTO7E-22-7S/103
A	+28-volt input	A	Data rate timing
B	+28-volt input	B	Spare
C	Case ground	C	Major frame sync
D	Power return	D	Spare
E	Power return	E	PCM output
F	Case ground	F	Spare
G	Spare	G	Spare





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Figure 2-2. Bench Test Setup for C14-210-0003



Table 2-2. Connector Pin Assignments (cont )

Pin	Functional Assignment	Pin	Functional Assignment
<del>X</del> J3 Bendix PTO7H-18-32S <del>X</del>			
A	Data rate timing	T	A/D dump
B	Major frame sync	U	Control bit
C	Subframe sync	V	End A/D conversion
D	A/D trigger	W	Analog ground
E	PCM output	X	Digital ground
F	Word rate	Y	Analog +10 vdc
G	A/D analog in	Z	Analog -10 vdc
H	A/D bit 1	a	Digital +15 vdc
J	A/D bit 2	b	Digital +10 vdc
K	A/D bit 3	c	Digital -10 vdc
L	A/D bit 4	d	Digital -15 vdc
M	A/D bit 5	e	Spare
N	A/D bit 6	f	Spare
P	A/D bit 7	g	Spare
R	A/D bit 8	h	Spare
S	Digital dump	j	Spare
J4 Bendix PTO7H-20-41S			
A	PGC channel 1	Y	PGC channel 40
B	PGC channel 4	Z	PGC channel 41
C	PGC channel 6	a	PGC channel 43
D	PGC channel 8	b	PGC channel 46
E	PGC channel 9	c	PGC channel 48
F	PGC channel 11	d	PGC channel 49
G	PGC channel 14	e	PGC channel 50
H	PGC channel 16	f	PGC channel 52
J	PGC channel 17	g	PGC channel 54
K	PGC channel 18	h	PGC channel 56
L	PGC channel 20	i	PGC channel 57
M	PGC channel 22	j	PGC channel 59
N	PGC channel 24	k	PGC channel 62
P	PGC channel 25	m	Logic signal return
R	PGC channel 27	n	PGC channel 64
S	PGC channel 30	p	Logic signal return
T	PGC channel 32	q	Logic signal return
U	PGC channel 33	r	PGC channel 65
V	PGC channel 34	s	Logic signal return
W	PGC channel 36	t	Logic signal return
X	PGC channel 38		



Table 2-2. Connector Pin Assignments (cont )

Pin	Functional Assignment	Pin	Functional Assignment
J5 Bendix PTO7H-20-41SW			
A	PGC channel 66	Y	PGC channel 107
B	PGC channel 68	Z	PGC channel 110
C	PGC channel 70	a	PGC channel 112
D	PGC channel 72	b	PGC channel 113
E	PGC channel 73	c	PGC channel 114
F	PGC channel 75	d	PGC channel 116
G	PGC channel 78	e	PGC channel 118
H	PGC channel 80	f	PGC channel 120
J	PGC channel 81	g	PGC channel 121
K	PGC channel 82	h	PGC channel 123
L	PGC channel 84	i	PGC channel 126
M	PGC channel 86	j	PGC channel 128
N	PGC channel 88	k	Data inhibit
P	PGC channel 91	m	Logic signal return
R	PGC channel 94	n	Subframe sync
S	PGC channel 96	p	Logic signal return
T	PGC channel 97	q	Logic signal return
U	PGC channel 98	r	Prime frame sync (PGC channel 2)
V	PGC channel 100	s	Logic signal return
W	PGC channel 102	t	Logic signal return
X	PGC channel 104		
J6 Bendix PTO7H-20-41P			
A	Analog gate input 29	Y	Analog signal return
B	Analog gate input 30	Z	Analog signal return
C	Analog gate input 31	a	Analog signal return
D	Analog gate input 32	b	Analog signal return
E	Analog gate input 33	c	Analog signal return
F	Analog gate input 34	d	Analog signal return
G	Analog gate input 35	e	Analog signal return
H	Analog gate input 36	f	Analog signal return
J	Analog gate input 37	g	Analog signal return
K	Analog gate input 38	h	Analog signal return
L	Analog gate input 39	i	Analog signal return
M	Analog gate input 40	j	Control bit
N	Analog gate input 41	k	Digital input 1 (MSB)
P	Analog gate input 42	m	Digital input 2
R	Analog gate input 43	n	Digital input 3
S	Analog gate input 44	p	Digital input 4
T	Analog gate input 45	q	Digital input 5
U	Analog gate input 46	r	Digital input 6
V	Analog gate input 47	s	Digital input 7
W	Analog gate input 48	t	Digital input 8 (LSB)
X	Analog signal return		



Table 2-2. Connector Pin Assignments (cont )

Pin	Functional Assignment	Pin	Functional Assignment
J7 Bendix PTO7H-20-41PW			
A	Analog gate input 1	Y	Analog signal return
B	Analog gate input 2	Z	Analog signal return
C	Analog gate input 3	a	Analog signal return
D	Analog gate input 4	b	Analog signal return
E	Analog gate input 5	c	Analog signal return
F	Analog gate input 6	d	Analog signal return
G	Analog gate input 7	e	Analog signal return
H	Analog gate input 8	f	Analog signal return
J	Analog gate input 9	g	Analog signal return
K	Analog gate input 10	h	Analog signal return
L	Analog gate input 11	i	Analog signal return
M	Analog gate input 12	j	Analog signal return
N	Analog gate input 13	k	Analog gate input 21
P	Analog gate input 14	m	Analog gate input 22
R	Analog gate input 15	n	Analog gate input 23
S	Analog gate input 16	p	Analog gate input 24
T	Analog gate input 17	q	Analog gate input 25
U	Analog gate input 18	r	Analog gate input 26
V	Analog gate input 19	s	Analog gate input 27
W	Analog gate input 20	t	Analog gate input 28
X	Subcommutator input (PAM)		

2-9. TEST PROCEDURE.

2-10. Whenever the operation of the C14-210-0003 is suspected as being faulty, the functional test procedure contained in table 2-3 should be performed. Malfunctions observed during this test can be isolated using the trouble analysis procedure contained in Section III.

Table 2-3. Functional Test Procedure

Step	Test Description and Procedure	Test Results
1	<p style="text-align: center;">NOTE</p> <p style="text-align: center;">To avoid ground loops, terminate all external grounds at a common point.</p>	
	Provide data rate timing and major frame sync input signals as per specifications given in paragraph 2-3.	



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results
------	--------------------------------	--------------

## NOTE

Data rate timing and major frame sync signals are referenced to logic signal return (J5-m).

- 2 Connect 51.2 kc data rate timing signal input to J2-A.
- 3 Connect 1 pps major frame sync signal input to J2-C.

## NOTE

Data inhibit, primary gate controls, and control bit signals are referenced to logic signal return (J5-m).

- 4 Connect J5-k (data inhibit signal) to control bit generator input.
- 5 Connect J5-r (primary gate control channel -2) to control bit generator input.
- 6 Connect J6-j (control bit) to control bit generator output.
- 7 Turn on 0 to 50 vdc power supply and adjust output voltage to +28 ( $\pm 1.5$ ) vdc; set maximum power supply output current limit to 1.5 amperes; turn off 0 to 50 vdc power supply.

## WARNING

To avoid injury to personnel, verify that 0 to 50 vdc power supply is turned off before performing step 8.

- 8 Connect output 0 of 50 vdc power supply to C14-210-0003 under test. (Positive lead connects to J1-A & -B; negative lead connects to J1-D & -E.); turn on 0 to 50 vdc power supply and verify that power supply output voltage is still at +28 ( $\pm 1.5$ ) vdc; readjust power supply output voltage slightly if necessary.

## NOTE

Wait 15 minutes before proceeding with step 9.



Table 2-3. Functional Test Procedure (cont )

Step	Test Description and Procedure	Test Results
INTERNAL VOLTAGE TEST		
<p style="text-align: center;">NOTE</p> <p>Power supply output voltages are nonadjustable. The final output voltage is obtained at test by selection of certain power supply resistors. The output voltages listed in the following step are nominal values and should closely approximate those obtained during measurement to within <math>\pm 1</math> volt of nominal. Power supply regulation should be within the percentage indicated for a particular power supply output nominal voltage.</p>		
9	Use digital voltmeter to measure internal voltages generated by system under test. Vary 0 to 50 vdc power supply output from +26.5 to +29.5 vdc.	<p>Internal voltages measured should be as follows:</p> <p>a. J3-Y (+) +10 vdc nominal J3-W (-) (<math>\pm 2</math> percent of nominal voltage)</p> <p>b. J3-W (+) -10 vdc nominal J3-Z (-) (<math>\pm 2</math> percent of nominal voltage)</p> <p>c. J3-a(+) +15 vdc nominal J3-X (-) (<math>\pm 10</math> percent of nominal voltage)</p> <p>d. J3-b (+) +10 vdc nominal J3-X (-) (<math>\pm 10</math> percent of nominal voltage)</p> <p>e. J3-X (+) -10 vdc nominal J3-c (-) (<math>\pm 5</math> percent of nominal voltage)</p> <p>f. J3-X (+) -15 vdc nominal J3-d (-) (<math>\pm 5</math> percent of nominal voltage)</p>



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results
SUBFRAME SYNCHRONIZATION OUTPUT TEST		
10	Set decade box to 10,000 ohms and connect across subframe sync output (J5-n to J5-m).	
11	Using oscilloscope, observe subframe sync output signal (J5-n) with respect to major frame sync signal (J2-C). Reference oscilloscope to logic signal return J5-m.	Subframe sync signal should have following characteristics: a. Format: negative pulse b. Pulse duration: 9 to 10 $\mu$ sec c. Frequency: 1 pps d. Rise time: 0.2 ( $\pm 0.1$ ) $\mu$ sec e. Fall time: < 0.3 $\mu$ sec f. Delay: See figure 2-1. g. Amplitude: 0( $\pm 0.5$ ) to -6 ( $\pm 0.5$ ) vdc h. Jitter: < 0.1 $\mu$ sec
12	Vary amplitude of major frame sync input signal from -6 vdc to -1.5 vdc while observing subframe sync output (J5-n) on oscilloscope.	Subframe sync output should be present when major frame sync amplitude is between -6 and -2.7 vdc and drop out when major frame sync amplitude is lowered to -1.5 vdc.
PRIMARY GATE CONTROL CHANNEL TEST		
13	Synchronize oscilloscope to leading edge of major frame sync input (J2-C). Reference oscilloscope to logic signal return (J5-m).	
14	Set decade box to 10,000 ohms and connect it across PGC channel 2 output (J5-r and J5-m).	
15	Using oscilloscope, observe PGC channel 2 output signal (J5-r) with respect to major frame sync signal (J2-C).	PGC channel 2 output should have the following characteristics: a. Format: negative b. Pulse duration: 156 ( $\pm 1$ ) $\mu$ sec, including delay time c. Frequency: 50 pps



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure			Test Results
15 (cont)				d. Rise time: < 0.5 μ sec e. Fall time: < 1.0 μ sec f. Delay: See figure 2-1 g. Amplitude: 0(±0.5) to -6 (±0.5) (10,000 vdc. ohm load)
16	Vary amplitude of data rate timing input signal from -6 vdc to -1.5 vdc while observing PGC channel 2 output at J5-r.			PGC channel 2 output should be present when data rate timing amplitude is between -6 and -2.7 vdc and drop out when data rate timing amplitude is lowered to -1.5 vdc.
NOTE				
In the following step, synchronize oscilloscope with PGC channel output pulse preceding the PGC channel pulse to be observed. Oscilloscope should be referenced to logic signal return.				
17	Repeat steps 14 and 15 for following 69 PGC outputs: PGC channel 2 has been included in this list for purposes of scope synchronization.			As specified in step 15. Pulse delay to be as specified in figure 2-1 for adjacent PGC channel. Non-adjacent PGC channel output delays may be measured with respect to data rate timing. Delay should be as shown in figure 2-1 for leading edge of PGC channel 2 with respect to beginning of subframe and prime frame.
	PGC Channel Output	Connector Pin	Scope Sync & Comparison Input	
	1	J4-A	PGC 128	
	2	J5-r	PGC 1	
	4	J4-B	PGC 2	
	6	J4-C	PGC 4	
	8	J4-D	PGC 6	
	9	J4-E	PGC 8	
	11	J4-F	PGC 9	
	14	J4-G	PGC 11	
	16	J4-H	PGC 14	
	17	J4-J	PGC 16	
	18	J4-K	PGC 17	
	20	J4-L	PGC 18	
	22	J4-M	PGC 20	



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure			Test Results
17 (cont)	PGC Output	Connector Pin	Scope Sync & Comparison Input	
	24	J4-N	PGC 22	
	25	J4-P	PGC 24	
	27	J4-R	PGC 25	
	30	J4-S	PGC 27	
	32	J4-T	PGC 30	
	33	J4-U	PGC 32	
	34	J4-V	PGC 33	
	36	J4-W	PGC 34	
	38	J4-X	PGC 36	
	40	J4-Y	PGC 38	
	41	J4-Z	PGC 40	
	43	J4-a	PGC 41	
	46	J4-b	PGC 43	
	48	J4-c	PGC 46	
	49	J4-d	PGC 48	
	50	J4-e	PGC 49	
	52	J4-f	PGC 50	
	54	J4-g	PGC 52	
	56	J4-h	PGC 54	
	57	J4-i	PGC 56	
	59	J4-j	PGC 57	
	62	J4-k	PGC 59	
	64	J4-n	PGC 62	
	65	J4-r	PGC 64	
	66	J5-A	PGC 65	
	68	J5-B	PGC 66	
	70	J5-C	PGC 68	
	72	J5-D	PGC 70	
	73	J5-E	PGC 72	
	75	J5-F	PGC 73	
	78	J5-G	PGC 75	
	80	J5-H	PGC 78	
	81	J5-J	PGC 80	
	82	J5-K	PGC 81	
	84	J5-L	PGC 82	
	86	J5-M	PGC 84	
	88	J5-N	PGC 86	
	91	J5-P	PGC 88	



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure			Test Results
17 (cont)	PGC Output	Connector Pin	Scope Sync & Comparison Input	
	94	J5-R	PGC 91	
	96	J5-S	PGC 94	
	97	J5-T	PGC 96	
	98	J5-U	PGC 97	
	100	J5-V	PGC 98	
	102	J5-W	PGC 100	
	104	J5-X	PGC 102	
	107	J5-Y	PGC 104	
	110	J5-Z	PGC 107	
	112	J5-a	PGC 110	
	113	J5-b	PGC 112	
	114	J5-c	PGC 113	
	116	J5-d	PGC 114	
	118	J5-e	PGC 116	
	120	J5-f	PGC 118	
	121	J5-g	PGC 120	
	123	J5-h	PGC 121	
	126	J5-i	PGC 123	
	128	J5-j	PGC 126	
ANALOG-TO-DIGITAL CONVERTER TEST				
18	Connect 600 feet of RG-180 B/U coaxial cable terminated with a 95-ohm resistor across PCM output and logic signal return (J2-E and J4-m, respectively).			
19	Connect variable 0 to ±10 vdc millivolt reference (5,000 ohms output impedance) to sub-commutator input (J7-X positive and J6-X return).			
20	Connect jumpers from all analog gate input lines to analog signal return. Refer to table 2-2 for analog gate connector pin letters.			



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results
21	Connect PCM output (J2-E) to vertical input of oscilloscope. Reference oscilloscope to logic signal return (J5-m).	
22	Vary millivolt reference output from 0 to 5 vdc while observing PCM output on oscilloscope.	Bit content of PCM output should continuously change as millivolt reference output is varied.
23	Adjust millivolt reference output to 0.000 vdc.	
24	Observe PCM output (J2-E) on oscilloscope with respect to PGC channel 2 output (J5-r).	<p>PCM code should be 00000001. Waveform characteristics should be as follows:</p> <ul style="list-style-type: none"> <li>a. Format: NRZ-S</li> <li>b. Word length: 8 bits straight binary</li> <li>c. Bit rate: 51,200 bits per second</li> <li>d. Amplitude: Binary ONE +7 (<math>\pm 1</math>) vdc Binary ZERO 0 (<math>\pm 0.5</math>) vdc</li> <li>e. Rise time: <math>&lt; 0.3 \mu \text{ sec}</math></li> <li>f. Fall time: <math>&lt; 0.3 \mu \text{ sec}</math></li> <li>g. Jitter: <math>&lt; \pm 0.1 \mu \text{ sec}</math></li> <li>h. Delay: One word time (156 <math>\mu \text{ sec}</math>) from trailing edge of PGC pulse originating PCM output.</li> </ul>
<p style="text-align: center;">NOTE</p> <p>In steps 25 and 26, the mean threshold voltage is the average value of the upper and lower threshold voltages. The threshold voltage is the point at which either a dropout or addition of a single bit occurs.</p>		
25	Adjust output of millivolt reference to obtain threshold levels of PCM output. Record mean threshold levels.	Recorded mean voltage should be within $\pm 15$ millivolts of 0.000 vdc.



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results
26	<p>Adjust millivolt reference to obtain threshold levels for following PCM codes. Record mean threshold levels.</p> <p>a. 00011011 b. 00110101 c. 01001101 d. 01100111 e. 10000000 f. 10011001 g. 10110011 h. 11001100 i. 11100101 j. 11111110</p>	<p>Recorded mean threshold voltages for PCM codes should be as follows:</p> <p>a. 0.514 (<math>\pm 0.015</math>) vdc b. 1.028 (<math>\pm 0.015</math>) vdc c. 1.502 (<math>\pm 0.015</math>) vdc d. 2.016 (<math>\pm 0.015</math>) vdc e. 2.510 (<math>\pm 0.015</math>) vdc f. 3.004 (<math>\pm 0.015</math>) vdc g. 3.518 (<math>\pm 0.015</math>) vdc h. 4.012 (<math>\pm 0.015</math>) vdc i. 4.506 (<math>\pm 0.015</math>) vdc j. 5.000 (<math>\pm 0.015</math>) vdc</p>
ANALOG GATE TEST		
<p>NOTE</p> <p>In steps 27 through 30, remove input signal short from particular analog gate being tested. Replace short at completion of test.</p>		
27	Disconnect millivolt reference from J7-X and connect it to analog gate 1 input J7-A.	
28	Adjust output of millivolt reference to +2.510 vdc.	
<p>NOTE</p> <p>PCM output is delayed one PGC channel time from PGC channel originating PCM output.</p>		
29	Observe PCM output on oscilloscope with respect to PGC channel 4 output.	PCM code associated with PGC channel 3 should be 10000000.



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure			Test Results	
30	NOTE				
	Analog gates 43 through 48 are spares and, therefore, are not required to be functionally tested in the following step.				
	Repeat steps 27 through 29 for following 41 analog gates:			All PCM codes for analog gates should be 10000000.	
	Analog Gate Number	Input Connector Pin	Associated PGC	Comparison Delay PGC	Remarks
	2	J7-B	5	6	Coincident
	3	J7-C	7	8	Coincident
	4	J7-D ✓	10 & 74	11 & 75	Coincident
	5	J7-E	12 & 76	14 & 78	Delayed 156 μ sec
	6	J7-F	13 & 77	14 & 78	Coincident
	7	J7-G ✓	15 & 79	16 & 80	Coincident
	8	J7-H ✓	19	20	Coincident
	9	J7-J ✓	21	22	Coincident
	10	J7-K	23	24	Coincident
	11	J7-L	26 & 90	27 & 91	Coincident
	12	J7-M	28 & 92	30 & 94	Delayed 156 μ sec
	13	J7-N	29 & 93	30 & 94	Coincident
	14	J7-P	31 & 95	32 & 96	Coincident
	15	J7-R	35	36	Coincident
	16	J7-S	37	38	Coincident
	17	J7-T	39	40	Coincident
	18	J7-U	42 & 106	43 & 107	Coincident
	19	J7-V	44 & 108	46 & 110	Delayed 156 μ sec
	20	J7-W	45 & 109	46 & 110	Coincident
	21	J7-k	47 & 111	48 & 112	Coincident
	22	J7-m	51	52	Coincident
	23	J7-n	53	54	Coincident
	24	J7-p	55	56	Coincident
	25	J7-q	58 & 122	59 & 123	Coincident
	26	J7-r	60 & 124	62 & 126	Delayed 156 μ sec
	27	J7-s	61 & 125	62 & 126	Coincident
	28	J7-t	63 & 127	64 & 128	Coincident
29	J6-A	67	68	Coincident	



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure			Test Results	
30 (cont)	Analog Gate Number	Input Connector Pin	Associated PGC	Comparison Delay PGC	Remarks
	30	J6-B	69	70	Coincident
	31	J6-C	71	72	Coincident
	32	J6-D	83	84	Coincident
	33	J6-E	85	86	Coincident
	34	J6-F	87	88	Coincident
	35	J6-G	89	91	Delayed 156 $\mu$ sec
	36	J6-H	99	100	Coincident
	37	J6-J	101	102	Coincident
	38	J6-K	103	104	Coincident
	39	J6-L	105	107	Delayed 156 $\mu$ sec
	40	J6-M	115	116	Coincident
	41	J6-N	117	118	Coincident
	42	J6-P	119	120	Coincident
	43	J6-R	} Spares		
	44	J6-S			
	45	J6-T			
	46	J6-U			
	47	J6-V			
	48	J6-W			
DATA INHIBIT TEST					
31	Set decade box to 10,000 ohms and connect it across data inhibit output (J5-k and J5-m).			Data inhibit output should have following characteristics: a. Format: Negative pulse train comprised of 58 PGC channels per prime frame.(Refer to table 1-1.) b. Pulse width: Each pulse 156 ( $\pm 1$ ) $\mu$ sec c. Rise time: < 0.5 $\mu$ sec d. Fall time: < 1.0 $\mu$ sec	
32	Observe data inhibit output signal (J5-k) with respect to PGC channel 1 (J4-A) for format and with respect to data rate timing (J3-A) for pulse delay. Reference oscilloscope to logic signal return (J5-m).				



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results																		
32 (cont)		<p>e. Amplitude 0 (<math>\pm 0.5</math>) vdc to -6 (10,000 (<math>\pm 0.5</math>) vdc ohm load):</p> <p>f. Pulse delay: &lt; 10 micro-seconds, measured between 10 and 90 percent levels of data inhibit pulse and data rate timing.</p>																		
DIGITAL DATA TEST																				
33	<p>Disconnect millivolt reference from analog gate input and connect positive lead of millivolt reference in parallel with the following points:</p> <table><tr><td>Digital Data Bit</td><td>Connector Pin</td></tr><tr><td>1 (MSB)</td><td>J6-k</td></tr><tr><td>2</td><td>J6-m</td></tr><tr><td>3</td><td>J6-n</td></tr><tr><td>4</td><td>J6-p</td></tr><tr><td>5</td><td>J6-q</td></tr><tr><td>6</td><td>J6-r</td></tr><tr><td>7</td><td>J6-s</td></tr><tr><td>8 (LSB)</td><td>J6-t</td></tr></table>	Digital Data Bit	Connector Pin	1 (MSB)	J6-k	2	J6-m	3	J6-n	4	J6-p	5	J6-q	6	J6-r	7	J6-s	8 (LSB)	J6-t	
Digital Data Bit	Connector Pin																			
1 (MSB)	J6-k																			
2	J6-m																			
3	J6-n																			
4	J6-p																			
5	J6-q																			
6	J6-r																			
7	J6-s																			
8 (LSB)	J6-t																			
34	Connect negative lead of millivolt reference to logic signal return (J5-m).																			
35	Adjust millivolt reference output to +10.000 vdc.																			
36	Observe PCM output (J2-E) on oscilloscope. Reference oscilloscope to logic signal return (J5-m).	PCM output for all digital data times (refer to table 1-1) should be 11111111.																		



Table 2-3. Functional Test Procedure (cont)

Step	Test Description and Procedure	Test Results
37	Lower output of millivolt reference from +10.000 to +2.000 volts while observing PCM output (J2-E) on oscilloscope.	PCM output should be present when millivolt reference is between +10.000 and +3.500 vdc and drop out when millivolt reference is lowered to +2.000 vdc.
38	Adjust millivolt reference output to +10.000 vdc.	PCM output should be 11111111.
39	Switch digital data input lines (one line at a time) from +10.000 vdc to logic signal return while observing PCM output (J2-E) on oscilloscope.	PCM output should change in accordance with switching of digital data input. Plus 10.000 volts on digital data input should provide a binary ONE in PCM output and zero volts on digital data input should provide a binary ZERO in PCM output.
40	Open circuit all input lines to digital data bits 1 through 8.	
41	Observe PCM output (J2-E) on oscilloscope. Reference oscilloscope to logic signal return (J5-m).	PCM output should be 11111111.



## SECTION III

### TROUBLE ANALYSIS

#### 3-1. SCOPE.

3-2. This section contains trouble analysis data for use with the functional test procedure given in Section II. The basic troubleshooting approach is described, major test points are identified, and a detailed trouble analysis procedure is provided to aid maintenance personnel in the isolation and correction of a C14-210-0003 malfunction.

3-3. Additional troubleshooting aids in the form of logic and wiring diagrams are contained in Section VIII.

#### 3-4. APPROACH.

3-5. The basic troubleshooting approach adopted for the C14-210-0003 is to localize the indicated malfunction to one or two suspect plug-in circuit boards by using techniques which require a minimum of equipment disassembly. Each suspect plug-in circuit board is then replaced, one at a time, with a known-good board until the malfunction is corrected.

3-6. In many cases, the malfunction isolation process is readily apparent by logical deduction. More difficult malfunctions are isolated to the suspect board or boards through the use of 27 major test points provided at connector J3.

#### 3-7. TEST POINTS.

3-8. Twenty-seven major system test points are provided at external connector J3 to facilitate maintenance and troubleshooting of the carry-on system. Each test point contains a 10,000-ohm, series resistor to provide current-limiting protection for internal circuitry. Because of the series limiting resistance, it is recommended that high-input impedance test equipment be connected to the test points in order to provide accurate measurements. Table 3-1 illustrates typical waveforms and/or voltages present at each test point during normal system operation.

#### 3-9. TROUBLE ANALYSIS PROCEDURE.

3-10. A trouble analysis procedure for the C14-210-0003 is given in table 3-2. This table is developed on a single-failure basis and is keyed to the functional test procedure contained in Section II.



Table 3-1. Idealized Test Point Waveforms/Voltages

Major Test Point	CONNECTOR PIN		Waveform/Voltages	
TP1	J3-A	Data Rate Timing	0V -2.7V TO -6.5V	
TP2	J3-B	Major Frame Sync	0V -2.7V TO -6.5V	
TP3	J3-C	Subframe Sync	0V -6V	
TP4	J3-D	A/D Trigger	+10V 0V	
TP5	J3-E	PCM Output (Typical)	+7V 0V	
TP6	J3-F	Word Rate	+10V 0V	
TP7	J3-G	A/D Analog In (Typical)	+5V 0V	
TP8	J3-H	A/D Bit 1 (MSB)	<p>Voltage level is dependent upon state of flip-flop at time of measurement. A logical ONE is <math>\approx +8</math> vdc and a logical ZERO is <math>\approx -5</math> vdc.</p>	<p>NOTES</p> <p>1. Waveforms shown are idealized; actual waveforms observed may have rounding of corners, overshoot, etc., due to capacitive loading of test equipment and 10-kilohm series limiting resistor in C14-210-0003.</p> <p>2. Test point waveforms do not necessarily show related time bases. Voltage levels and time measurements differ for each test point.</p>
TP9	J3-J	A/D Bit 2		
TP10	J3-K	A/D Bit 3		
TP11	J3-L	A/D Bit 4		
TP12	J3-M	A/D Bit 5		
TP13	J3-N	A/D Bit 6		
TP14	J3-P	A/D Bit 7		
TP15	J3-R	A/D Bit 8 (LSB)		

312  
3.2  
6.24  
936  
796.4



Table 3-1. Idealized Test Point Waveforms/Voltages (Cont)

Major Test Point	CONNECTOR PIN	FUNCTION	Waveform/Voltages	
TP16	J3-S	Digital Dump (Typical)	+10V 0V	
TP17	J3-T	A/D Dump (Typical)	+10V 0V	
TP18	J3-U	Control Bit (Typical)	+2V TO +10V 0V	
TP19	J3-V	End A/D Conversion	+10V 0V	
TP20	J3-W	Analog Ground	Reference point for TP22 & TP23.	
TP21	J3-X	Digital Ground	Reference point for TP24, TP25, TP26, & TP27.	
TP22	J3-Y	Analog +10 vdc	+10 (±0.2) vdc	9.87
TP23	J3-Z	Analog -10 vdc	-10 (±0.2) vdc	10.17
TP24	J3-a	Digital +15 vdc	+15 (±0.72) vdc	+14.73
TP25	J3-b	Digital +10 vdc	+10 (±0.5) vdc	9.69
TP26	J3-c	Digital -10 vdc	-10 (±0.5) vdc	10.34
TP27	J3-d	Digital -15 vdc	-15 (±0.75) vdc	15.32

## NOTES

1. Waveforms shown are idealized; actual waveforms observed may have rounding of corners, overshoot, etc., due to capacitive loading of test equipment and 10-kilohm series limiting resistor in C14-210-0003.
2. Test point waveforms do not necessarily show related time bases. Voltage levels and time measurements differ for each test point.



Table 3-2. Trouble Analysis Procedure

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
9	One or more internal power supply voltages incorrect.	Power supply defective	Replace power supply board A17.
11	Subframe sync output missing or out of tolerance.	Input buffer or driver 71 defective.	Replace board A14 or A1.
12	Subframe sync output does not respond properly to level changes of major frame sync.	Input buffer defective.	Replace board A14.
15	PGC channel 2 output missing.	1. Programmer one-shot-1 defective.	Replace board A14.
		2. Driver 70 defective.	Replace board A1.
		3. Channel 1 trigger circuitry inoperative.	Replace board A14.
		4. Down-counter defective.	Replace board A14.
	PGC channel 2 output out of tolerance.	1. Driver 70 defective.	Replace board A1.
		2. Programmer one-shot -1 defective.	Replace board A14.
	PGC channel 2 output present only once per format (50 prime frames).	1. Ring counter defective.	Monitor other 69 PGC channel outputs to isolate where operation ceases. Replace defective program one-shot board A10, A11, A12, A13, or A14 depending upon which board contains inoperative one-shot.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
15 (cont )			<p>A14 contains one-shots 1 - 8.  A13 contains one-shots 9 - 38.  A12 contains one-shots 39 - 68.  A11 contains one-shots 69 - 98.  A10 contains one-shots 99 - 128.</p>
		2. Phase B, 3.2 kc drive signal missing.	Replace board A14.
16	PGC channel -2 output does not respond properly to level changes of data rate timing signal.	Input buffer defective.	Replace board A14.
17	PGC channels -4, -6, -8, or -9 missing or out of tolerance.	<p>1. Associated program one-shot defective.</p> <p>2. Associated driver defective.</p>	<p>Replace board A14.</p> <p>Replace board A3.</p>
	PGC channels -11, -14, -16, -17, -18, -20, -22, -24, -25, -27, -30, -32, -33, -34, -36, or -38 missing or out of tolerance.	<p>1. Associated program one-shot defective.</p> <p>2. Associated driver defective.</p>	<p>Replace board A13.</p> <p>Replace board A3.</p>
	PGC channels -40, -41, or -43, missing or out of tolerance.	<p>1. Associated program one-shot defective.</p> <p>2. Associated driver defective.</p>	<p>Replace board A12.</p> <p>Replace board A3.</p>



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
17 (cont )	PGC channels -46, -48, -49, -50, -52, -54, -56, -57, -59, -62, -64, -65, -66, or -68 missing or out of tolerance.	1. Associated program one-shot defective.	Replace board A12.
		2. Associated driver stage defective.	Replace board A2.
	PGC channels -70, -72, -73, -75, -78, -80, -81, -82, -84, or -86 missing or out of tolerance.	1. Associated program one-shot defective.	Replace board A11.
		2. Associated driver stage defective.	Replace board A2.
	PGC channels -88, -91, -94, -96, or -98 missing or out of tolerance.	1. Associated program one-shot defective.	Replace board A11.
		2. Associated driver stage defective.	Replace board A1.
	PGC channels -100, -102, -104, -107, -110, -112, -113, -114, -116, -118, -120, -121, -123, -126, or -128 missing or out of tolerance.	1. Associated program one-shot defective.	Replace board A10.
		2. Associated driver stage defective.	Replace board A1.
	PGC channel -1 missing or out of tolerance.	1. Associated program one-shot defective.	Replace board A10.
		2. Associated driver stage defective.	Replace board A3.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
22	No PCM output	<ol style="list-style-type: none"> <li>1. Time share gate, series gate D, or series gate E inoperative.</li> <li>2. Control bit signal missing.</li> <li>3. A/D dump signal missing.</li> <li>4. A/D converter inoperative.</li> <li>5. +5 vdc reference supply defective.</li> <li>6. P/S converter inoperative.</li> <li>7. Constant current driver defective.</li> <li>8. Output resistor A17R2 open.</li> </ol>	<p>Replace board A8.</p> <p>Monitor control bit at TP18 (J3-U). If signal is absent, replace board A15.</p> <p>Monitor A/D dump signal at TP17 (J3-T). If signal is absent, replace board A14.</p> <p>Monitor content of MSB storage register at TP8 (J3-H). If voltage remains constant, replace boards A8 and/or A16. If voltage changes, refer to next probable cause.</p> <p>Replace board A8.</p> <p>Replace board A15.</p> <p>Replace power supply A17.</p> <p>Monitor PCM output at TP5 (J3-E). If signal is present, replace power supply board A17.</p>



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
22 (cont )	All PCM output bits do not change as analog input voltage is varied.	1. A/D converter card B or P/S converter inoperative.	Monitor content of A/D register at TP8 thru TP15 with oscilloscope. If voltages at these points vary, replace board A15; if voltages remain constant, replace board A16.
24	No PCM output or incorrect number of bits.	1. A/D converter card A out of adjustment. 2. A/D converter defective.	Readjust board A8 as described in Section VI. Replace boards A8 and/or A16.
	PCM output wave-train out of tolerance.	PCM level conditioner or driver defective.	Replace board A15.
25 & 26	Mean threshold levels out of tolerance.	1. A/D converter card A out of adjustment. 2. A/D converter defective.	Readjust board A8 as described in Section VI. Replace boards A8 and/or A16.
29	No PCM output.	1. Program one-shot -2 No. 2 output missing. 2. Analog gate 1 or series gate A inoperative.	Replace board A14. Replace board A7.
	Incorrect number of bits in PCM output.	Analog gate 1 or series gate A defective.	Replace board A7.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
30	No PCM output for analog gate -2 or -3.	1. Associated program one-shot number 2 output missing.	Replace board A14.
		2. Analog gate -2, -3, or series gate A inoperative.	Replace board A7.
	Incorrect number of bits in PCM output for analog gate -2 or -3.	Analog gate -2, -3, or series gate A defective.	Replace board A7.
	No PCM output or incorrect number of bits for analog gate -4, -5, -6, or -7.	Analog gate -4, -5, -6, -7, or series gate A defective.	Replace board A7.
	PCM output for analog gate -4, -5, -6, or -7 occurs only once per prime frame.	Associated program one-shot number 2 output missing.	Replace board A13 if output associated with PGC channel 10, 12, 13, or 15 is missing. Replace board A11 if output associated with PGC channel 74, 76, 77, or 79 is missing.
	No PCM output for analog gate -8, -9, or -10.	1. Associated program one-shot number 2 output missing.	Replace board 13.
		2. Analog gate -8, -9, -10, or series gate A defective.	Replace board A7.
	Incorrect number of bits in PCM output for analog output -8, -9, or -10.	Analog gate -8, -9, -10, or series gate A defective.	Replace board A7.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
30 (cont )	No PCM output or incorrect number of bits for analog gate -11, -12, -13, or -14.	Analog gate -11, -12, -13, -14, or series gate A defective.	Replace board A7.
	PCM output for analog gate -11, -12, -13, or -14 occurs only once per prime frame.	Associated program one-shot number 2 output missing.	Replace board A13 if output associated with PGC channels 26, 28, 29, or 31 is missing. Replace board A11 if output associated with PGC channel 90, 92, 93, or 95 is missing.
	No PCM output for analog gate -15 or -16.	1. Associated program one-shot number 2 output missing.  2. Analog gate -15, -16, or series gate A defective.	Replace board A13.  Replace board A7.
	Incorrect number of bits in PCM output for analog gate -15 or -16.	Analog gate -15, -16, or series gate A defective.	Replace board A7.
	No PCM output for analog gate -17.	1. Associated program one-shot number 2 output missing.  2. Analog gate -17 or series gate B defective.	Replace board A13.  Replace board A6.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
30 (cont )	Incorrect number of bits in PCM output for analog gate -17.	Analog gate -17 or series gate B defective.	Replace board A6.
	No PCM output or incorrect number of bits for analog gate -18, -19, -20, or -21.	Analog gate -18, -19, -20, -21, or series gate B defective.	Replace board A6.
	PCM output for analog gate -18, -19, -20, or -21 occurs only once per prime frame.	Associated program one-shot number 2 output missing.	Replace board A12 if output associated with PGC channel 42, 44, 45, or 47 is missing. Replace board A10 if output associated with PGC channel 106, 108, 109, or 111 is missing.
	No PCM output for analog gate -22, -23, or -24.	1. Associated program one-shot number 2 output missing.  2. Analog gate -22, -23, -24, or series gate B defective.	Replace board A12.  Replace board A6.
	Incorrect number of bits in PCM output for analog gate -22, -23, or -24.	Analog gate -22, -23, -24, or series gate B defective.	Replace board A6.
	No PCM output or incorrect number of bits for analog gate -25, -26, -27, or -28.	Analog gate -25, -26, -27, -28, or series gate B defective.	Replace board A6.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
30 (cont)	PCM output for analog gate -25, -26, -27, or -28 occurs only once per prime frame.	Associated program one-shot number -2 output missing.	Replace board A12 if output associated with PGC channel 58, 60, 61, or 63 is missing. Replace board A10 if output associated with PGC channel 122, 124, 125, or 127 is missing.
	No PCM output for analog gate -29 or -30.	1. Associated program one-shot number 2 output missing. 2. Analog gate -29, -30, or series gate B defective.	Replace board A12. Replace board A6.
	Incorrect number of bits in PCM output for analog gate -29 or -30.	Analog gate -29, -30, or series gate B defective.	Replace board A6.
	No PCM output for analog gate -31 or -32.	1. Associated program one-shot number 2 output missing. 2. Analog gate -31, -32, or series gate B defective.	Replace board A11. Replace board A6.
	Incorrect number of bits in PCM output for analog gate -31 or -32.	Analog gate -31, -32, or series gate B defective.	Replace board A6.
	No PCM output for analog gate -33, -34, -35, or -36.	1. Associated program one-shot number 2 output missing.	Replace board A11.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
30 (cont)		2. Analog gate -33, -34, -35, -36, or series gate C defective.	Replace board A5.
	Incorrect number of bits in PCM output for analog gate -33, -34, -35, or -36.	Analog gate -33, -34, -35, -36, or series gate C defective.	Replace board A5.
	No PCM output for analog gate -37, -38, -39, -40, -41, or -42.	1. Associated program one-shot number 2 output missing.	Replace board A11.
		2. Analog gate -37, -38, -39, -40, -41, -42, or series gate C defective.	Replace board A5.
	Incorrect number of bits in PCM output for analog gate -37, -38, -39, -40, -41, or -42.	Analog gate -37, -38, -39, -40, -41, -42, or series gate C defective.	Replace board A5.
32	Data inhibit output missing completely.	1. Inverter inoperative.	Replace board A4.
		2. Level conditioner or driver 72 inoperative.	Replace board A1.
		3. Output resistor A17R22 open.	Replace power supply board A17.
	Data inhibit output wavetrain out of tolerance.	Level conditioner or driver 72 defective.	Replace board A1.



Table 3-2. Trouble Analysis Procedure (cont )

Referenced Step, Table 2-3	Abnormal Indication	Probable Cause	Remedy
36	No PCM output for all digital data times.	Digital dump signal missing.	Monitor digital dump signal at TP16 (J3-S). If signal is present, replace board A15. If signal is absent, replace board A14.
	Incorrect PCM output.	Buffer amplifier defective.	Replace board A15.
37	PCM output does not respond properly to level changes of digital data input.	Buffer amplifier defective.	Replace board A15.
39	No change in PCM output for a given change of digital input data.	Buffer amplifier defective or serial/shift register input gate defective.	Replace board A15.
41	Incorrect PCM output.	Buffer amplifier defective.	Replace board A15.



## SECTION IV

### REMOVAL AND INSTALLATION

4-1. SCOPE,

4-2. This section contains the necessary instructions for removal and installation of the major components of the C14-210-0003.

4-3. COMPONENT REMOVAL (See figures 4-1 and 4-2).

4-4. PLUG-IN BOARDS (A1 thru A16).

#### NOTE

Figure 4-1 shows the location and identification of each plug-in board.

4-5. Plug-in board removal is accomplished as follows:

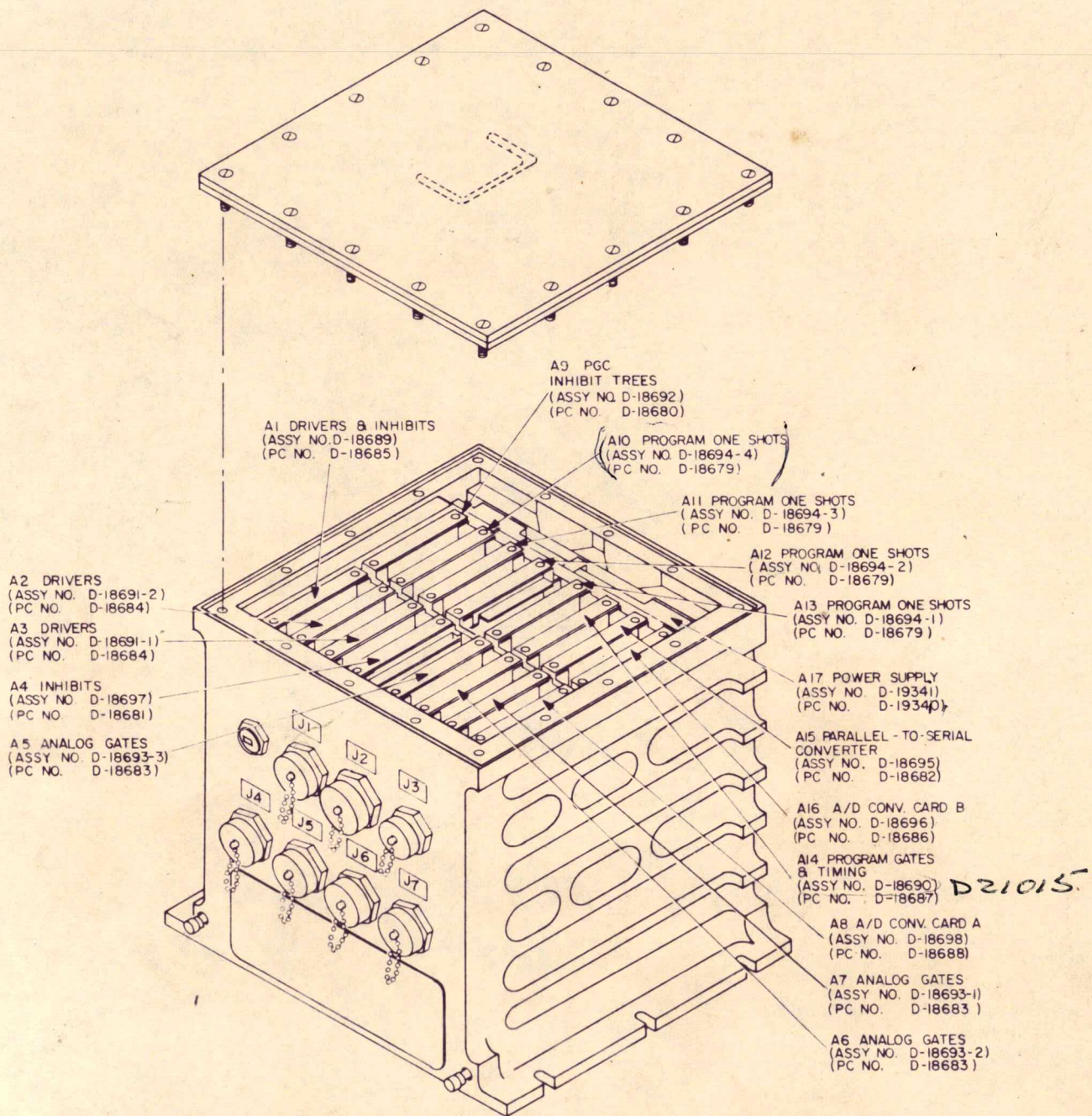
- a. Disconnect input power to C14-210-0003.
- b. Loosen 16 captive screws (Vector Part No. C-19186-1) securing top cover to housing.

#### CAUTION

In the following step, do not use tools to pry off the top cover of the C14-210-0003 as possible damage could result to the frame seal gasket contained on the underside of this cover. The top cover can be easily removed by hand.

- c. Carefully lift top cover from housing.
- d. Identify location of particular plug-in board to be removed using figure 4-1 as a guide.
- e. Loosen two captive screws (Vector Part No. C-19186-7) securing board to housing.





M1509-16

Figure 4-1. Board Identification and Location



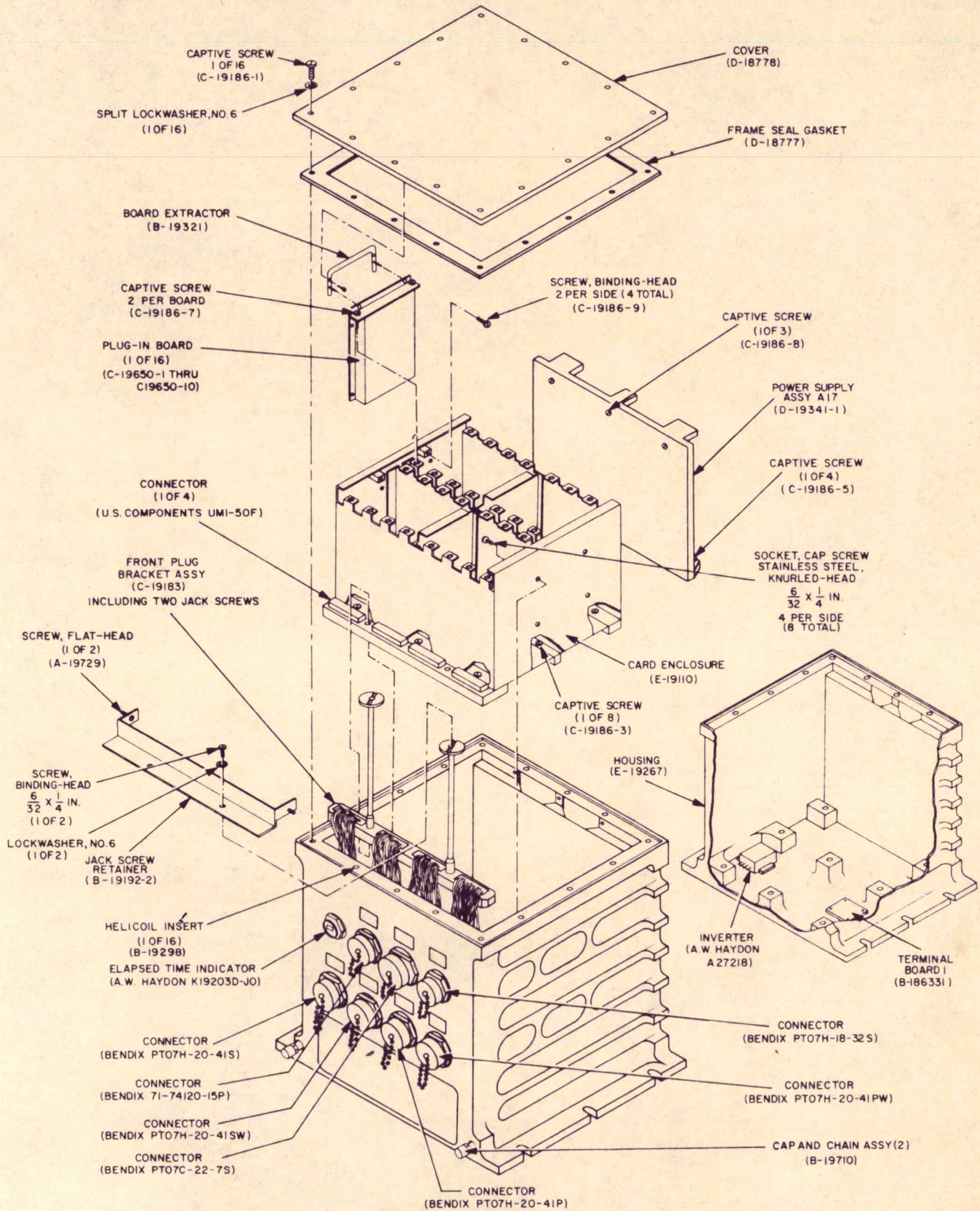


Figure 4-2. Major Components of C14-210-0003

M1509-17



NOTE

Each plug-in board is provided with two holes at the top of the board to accept the board extractor pins.

- f. Use board extractor (Vector Part No. B-19321) attached to bottom side of top cover to remove board from housing.

4-6. POWER SUPPLY ASSEMBLY (A17).

NOTE

Figure 4-1 shows the location of the power supply assembly.

4-7. The plug-in power supply assembly is removed as follows:

- a. Disconnect input power to C14-210-0003.
- b. Loosen 16 captive screws (Vector Part No. C19186-1) securing top cover to housing.

CAUTION

In the following step, do not use tools to pry off the top cover of the C14-210-0003 as possible damage could result to the frame seal gasket contained on the underside of this cover. The top cover can be easily removed by hand.

- c. Carefully lift top cover from housing.
- d. Identify location of plug-in power supply assembly using figure 4-1 as a guide.
- e. Loosen three captive screws (Vector Part No. C19186-8) securing top portion of power supply assembly to side of housing.
- f. Loosen four captive screws (Vector Part No. C19186-5) securing bottom of power supply assembly to base of housing.
- g. Withdraw power supply assembly from housing.



4-8. FRAME SEAL GASKET.

4-9. The frame seal gasket shown in figure 4-2 is removed by backing off the 16 captive screws (Vector Part No. C19186-1) securing the top cover to the housing until the screws are completely free from the top cover.

4-10. CARD ENCLOSURE AND/OR HOUSING.

NOTE

Figure 4-2 identifies the major components of the C14-210-0003.

4-11. Card enclosure and/or housing removal is accomplished as follows:

- a. Disconnect input power to C14-210-0003.
- b. Loosen 16 captive screws (Vector Part No. C19186-1) securing top cover to housing.

CAUTION

In the following step, do not use tools to pry off the top cover of the C14-210-0003 as possible damage could result to the frame seal gasket contained on the underside of this cover. The top cover can be easily removed by hand.

- c. Carefully lift top cover from housing.
- d. Remove two 6/32 by 1/4-inch binding-head screws and two No. 6 lock washers securing jack screw retainer (Vector Part No. B19192-2) to housing.
- e. Remove two flat-head screws (Vector Part No. A19729) securing sides of jack screw retainer to housing.
- f. Remove jack screw retainer from housing.
- g. Remove all 16 plug-in boards by loosening two captive screws (Vector Part No. C19186-7) securing each board to housing; use board extractor (Vector Part No. B19321) to facilitate board removal.
- h. Loosen three captive screws (Vector Part No. C19186-8) securing top portion of power supply to side of housing.



- i. Loosen four captive screws (Vector Part No. C19186-5) securing bottom of power supply assembly to base of housing.
- j. Withdraw power supply assembly from housing.

#### CAUTION

To avoid possible damage to front plug bracket assembly connectors, alternate loosening of each front plug bracket assembly jackscrew in following step.

- k. Loosen two front plug bracket assembly jackscrews (alternate loosening approximately one turn per jackscrew) until they turn freely.
- l. Loosen eight captive screws (Vector Part No. C19186-3) securing bottom of card enclosure to base of housing.
- m. Remove four binding-head screws, two per side, (Vector Part No. C19186-9) securing top portion of card enclosure sides to housing.
- n. Remove eight, 6/32 by 1/4-inch, knurled-head, socket cap screws (four per side) securing sides of card enclosure to housing.
- o. Lift up and position front plug bracket assembly away from front of card enclosure.
- p. Slide card enclosure towards area vacated by removal of power supply assembly, then carefully withdraw card enclosure from housing.

#### NOTE

At this point of disassembly, all internal wiring, connectors, etc., are accessible for replacement, if required.

#### 4-12. COMPONENT INSTALLATION.

4-13. Installation of C14-210-0003 components is essentially the reverse of the procedures described in paragraph 4-3; however, for plug-in board installation, the board extractor is not required. All plug-in components can be replaced individually without requiring board matching, calibration, or adjustment after installation of a new plug-in component. Refer to figure 4-1 for proper location when installing plug-in boards. Stamped on each plug-in board is the board name and either a printed circuit board part number or an assembly part number. Both of these numbers are shown in figure 4-1.



## SECTION V

### REPAIR INSTRUCTIONS

#### 5-1. GENERAL.

5-2. Repair of the C14-210-003, with the exception of simple repairs, is limited to the replacement of defective components authorized for field-level maintenance, and performing the adjustment procedures contained in Section VI. Instructions for removal/installation of C14-210-0003 major components are contained in Section VI. Periodic maintenance routines are described in Section VII.

5-3. C14-210-0003 systems requiring repair beyond the authorized level of field maintenance should be returned to the manufacturer.

#### 5-4. STORAGE.

5-5. Prepare the C14-210-0003 for temporary storage as follows:

- a. Purge coolant passage with gaseous nitrogen.
- b. Seal inlet and outlet ports with captive threaded protective caps.
- c. Install metal protective caps on all seven external electrical connectors.
- d. Enclose C14-210-0003 in a polyethylene film bag and seal bag.



## SECTION VI

## CALIBRATION AND ADJUSTMENT

6-1. SCOPE.

6-2. This section contains adjustment instructions for the C14-210-0003. These instructions are provided as supplemental information and are to be used on an as - required basis, rather than at prescheduled intervals.

6-3. ADJUSTMENT REQUIREMENTS.

6-4. The only component of the C14-210-0003 requiring field adjustment is the analog-to-digital converter, card A mounted in reference designation area A8. (See figure 4-1.)

6-5. Two slightly different types of analog-to-digital converter card A's are used in the C14-210-0003. The earlier C14-210-0003 systems contain a Type 1 A/D converter card A, while later systems are provided with a Type 2 A/D converter card A. Both types of cards are shown in figure 6-1. For either type card, however, the field adjustment procedure is identical. The two additional potentiometers provided on the Type 1 card are for manufacturing convenience and under no circumstances should they be adjusted in the field. These potentiometers are factory set and do not require any further adjustment for the life of the card.

6-6. EQUIPMENT REQUIRED.

6-7. Since the A/D converter card A is adjusted while the C14-210-0003 is processing an analog input signal, all of the equipment listed in table 2-1 is required for adjustment purposes. Additionally, a board extender (Vector Part No. C-19762) is necessary to gain access to the potentiometers during the adjustment procedure.

6-8. ADJUSTMENT PROCEDURE.

6-9. Adjustment of the A/D converter card A is performed as follows:

a. Provide required external inputs to C14-120-0003 as described in steps 1 through 7 of table 2-3.

b. Remove top cover of C14-210-0003 and locate A/D converter card A in reference designation area A8. (See figure 4-1.)



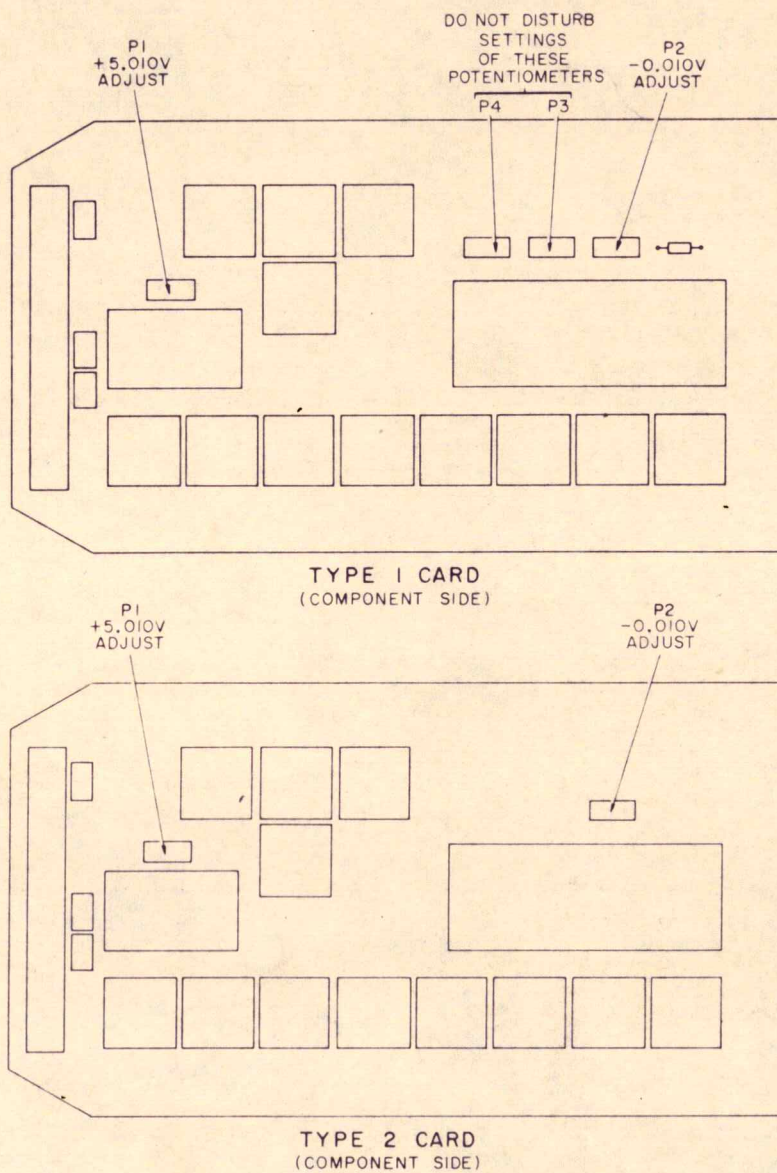


Figure 6-1. Location of Adjustments on A/D Converter Card A



- c. Remove A/D converter card A.
- d. Remove metal heat sink cover surrounding components on A/D converter card A and identify board type using figure 6-1 as a guide.
- e. Obtain board extender (Vector Part No. C-19762) and insert in slot vacated by removal of A/D converter card A.
- f. Insert A/D converter card A into board extender.
- g. Connect 600 feet of RG-180 B/U coaxial cable terminated with a 95-ohm resistor across PCM output and logic signal return (J2-E and J4-m, respectively).
- h. Connect PCM output (J2-E) to vertical input B of oscilloscope.
- i. Connect PGC channel 2 output (J5-r) to vertical input A of oscilloscope.
- j. Turn on 0 to 50 vdc power supply and adjust supply output to plus 28 ( $\pm 1.5$ ) vdc.
- k. Synchronize oscilloscope to major frame sync input (J2-C) and reference oscilloscope to logic signal return (J5-m).
- l. Except for analog gate 1, connect jumpers from all analog gate input lines to analog signal return. Refer to table 2-2 for analog gate connector pin letters.
- m. Connect variable 0 to  $\pm 10$  vdc millivolt reference (5,000 ohms output impedance) to analog gate 1 input (J7-E positive and J7-Y return).
- n. Adjust output of millivolt reference to -0.010 vdc.

## NOTE

Do not disturb settings of P3 and P4 on Type 1 A/D converter card A while performing step o.

- o. On A/D converter card A (figure 6-1), adjust P2 while observing PCM output on oscilloscope. A correct P2 adjustment is obtained when the least significant bit (last bit) of PCM wavetrain flickers from a binary ONE to a binary ZERO. (The other seven bits of the PCM output word should be binary ZEROES.)
- p. Adjust output of millivolt reference to +5.010 vdc.

## NOTE

Do not disturb settings of P3 and P4 on Type 1 A/D converter card A while performing step q.



q. On A/D converter card A (figure 6-1), adjust P1 while observing PCM output on oscilloscope. A correct P1 adjustment is obtained when the least significant bit (last bit) of PCM wavetrain flickers from a binary ONE to a binary ZERO. (The other seven bits of the PCM output word should be binary ONES.)

r. Adjust output of millivolt reference to -0.010 vdc.

s. Verify that least significant bit of PCM wavetrain still flickers from a binary ONE to a binary ZERO. Readjust P2 if necessary.

t. Adjust output of millivolt reference to +5.010 vdc.

u. Verify that least significant bit of PCM wavetrain still flickers from a binary ONE to a binary ZERO. Readjust P1 if necessary.

v. Repeat steps r through u until there is no interaction between adjustments.

w. Turn off 0 to 50 vdc power supply.

x. Remove A/D converter card A and board extender.

y. Reassemble heat sink cover to A/D converter card A.

z. Install A/D converter card A in reference designation area A8.

aa. Perform straight line linearity check of A/D converter as outlined in steps 18 through 26 of functional test procedure in table 2-3.



## SECTION VII

## PERIODIC INSPECTION AND SERVICE

7-1. SCOPE.

7-2. This section contains periodic inspection and servicing requirements for the C14-210-0003.

7-3. PERIODIC INSPECTION.

7-4. Since the C14-210-0003 is a hermetically-sealed unit, there are no scheduled inspection requirements for the interior components. Table 7-1 lists the inspection routines for the frame seal gasket and items of the C14-210-0003 exposed to the exterior.

Table 7-1. Periodic Inspection

Item	Inspection Procedure	Preventive Maintenance
Complete unit	Check for excessive dirt or dust, chipped paint, or corrosion.	Clean and refinish as required.
Connectors (external)	Check for damaged pins, distorted barrels, and cracked inserts.	Replace defective connector.
Frame seal gasket	Check o-ring for signs of excessive wear such as cracks, splits, etc. Check r-f gasketing for signs of excessive wear.	Replace gasket.
Pressure ports	Check for dust accumulation and obstructions. Check tightness of protective cap seals.	Clean or tighten as required.
Elapsed time indicator	Check for cracked or damaged indicator window.	Replace.



7-5. CLEANING.

7-6. The following procedure should be used to clean the exterior of the C14-210-0003:

- a. Remove loose dirt by vacuuming, or by dusting with a lint-free cloth.
- b. Wash case with a mild soap and water solution, rinse, and wipe dry.

WARNING

Some solvents are toxic and/or flammable. To prevent injury to personnel, avoid inhalation of fumes and extended contact. Keep solvent away from heat or open flame. Use in a well-ventilated area.

c. Clean stubborn dirt on metallic parts with a lint-free cloth dampened with cleaning solvent Federal Specification P-S-661, Type II.

7-7. LUBRICATION.

7-8. The C14-210-0003 does not require lubrication.

7-9. SURFACE REFINISHING.

7-10. Refinishing of painted surfaces is performed as specified in the following steps.

- a. Use sandpaper and/or wire brush to abrade damaged finish and remove paint and primer from metal surface.
- b. Feather edges of damaged area to prevent adjacent point from chipping.
- c. Rinse abraded surface with clean water and dry thoroughly.
- d. Apply one coat of epoxy polyimide primer No. 162W59 (W. P. Fuller Co.) or equivalent and allow to air dry.
- e. Apply two coats of Class A semi-gloss enamel, Federal Specification TT-E-529, Federal Standard 595, Color No. 26251 (gray).



## SECTION VIII

### DIAGRAMS

#### 8-1. SCOPE.

8-2. This section contains logic diagrams, wiring diagrams, and associated data required for reference purposes when performing maintenance of the C14-210-0003.

#### 8-3. LOGIC SYMBOLS.

8-4. The graphic symbols used to represent logic functions in the diagrams for the C14-210-0003 are individually discussed in paragraphs 8-5 through 8-18. The symbology is based upon a positive logic system; that is, a logical ONE is defined as a voltage more positive than that used to represent a logical ZERO. The following symbols are used in the C14-210-0003 logic diagrams:

- a. AND/OR functions
- b. NOT function
- c. Amplify function
- d. Flip-flop function
- e. One-Shot function
- f. General function

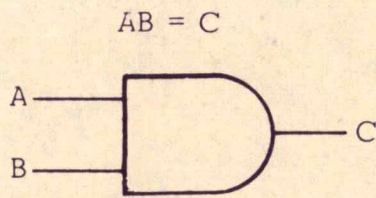
#### 8-5. AND/OR FUNCTIONS.

8-6. Basic AND/OR symbols used in the C14-210-0003 are shown in figure 8-1 with associated truth tables.

8-7. The AND circuit is used to detect coincidence of two or more input signals. The output of the AND circuit is at a logical ONE when all inputs are at a logical ONE.

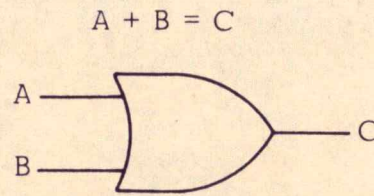
8-8. The OR circuit is an inclusive device that is used to mix or combine the input signals. The output of the OR circuit is at a logical ONE when one or more of its inputs are at a logical ONE.





AND CIRCUIT

INPUT		OUTPUT
A	B	C
0	0	0
1	0	0
0	1	0
1	1	1



OR CIRCUIT

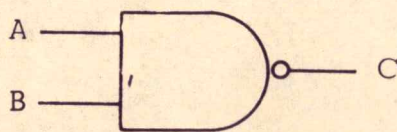
INPUT		OUTPUT
A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

M1509-19

Figure 8-1. AND/OR Functions

## 8-9. NAND/NOR FUNCTIONS.

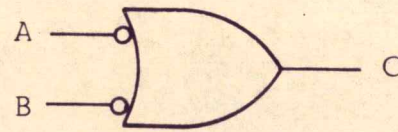
8-10. Basic NAND/NOR symbols used in the C14-201-0003 logic diagrams are shown in Figure 8-2 with associated truth tables. A small circle is used at the output of each device to indicate inversion. A NAND gate is simply an AND gate followed by an inverting amplifier, and a NOR gate is an OR gate followed by an inverting amplifier.



$$\overline{C} = AB$$

NAND CIRCUIT

INPUT		OUTPUT
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



$$C = \overline{A + B}$$

NOR CIRCUIT

INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

M1509-20

Figure 8-2. NAND/NOR Functions



## 8-11. AMPLIFY FUNCTION.

8-12. The amplify function, shown in figure 8-3, represents a device which may or may not have linearity, gain, or inversion. Only three symbols are used for amplify functions in this manual. Symbol A in figure 8-3 represents a non-inverting amplifier or emitter follower, symbol B represents an inverting amplifier, and symbol C represents a solid-state switch (single-pole, single-throw analogy). The solid-state switch is activated only by a logical ONE at the input and when activated, the output is connected to ground (logical ZERO).

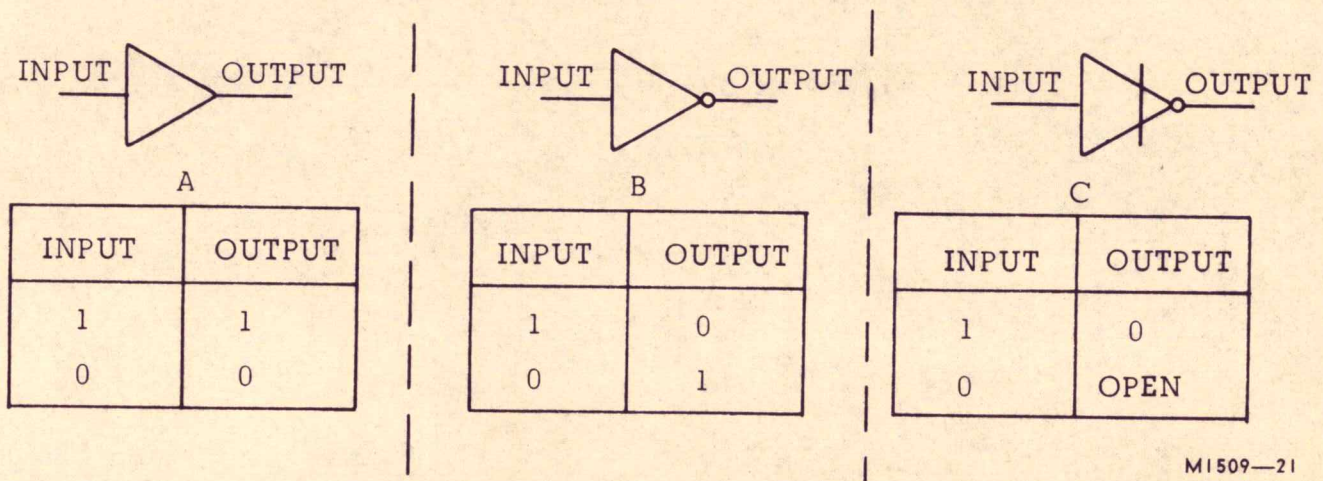


Figure 8-3. Amplify Functions

## 8-13. FLIP-FLOP FUNCTION.

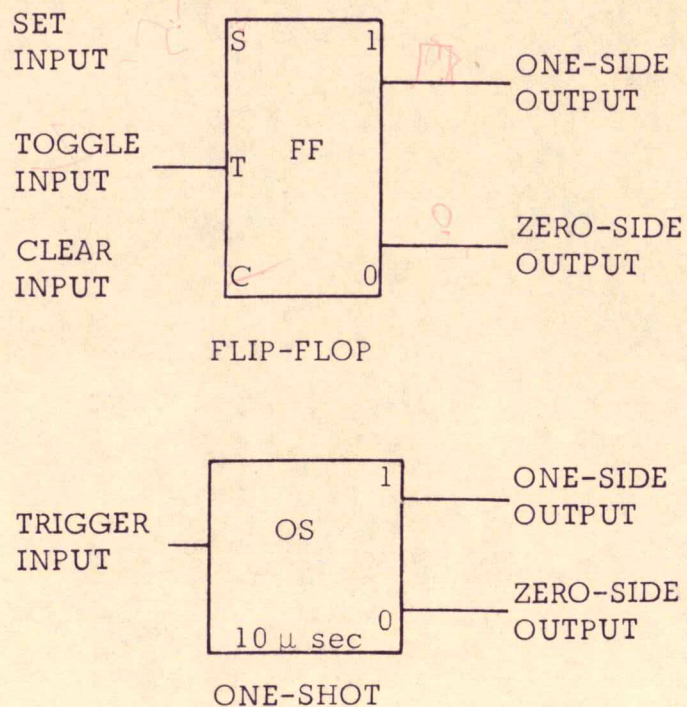
8-14. The flip-flop is a device used to store a single bit of information. It has three inputs, set (S), clear (C), and toggle (T), and two outputs, one-side and zero-side. The flip-flop symbol used in the logic diagrams and shown in figure 8-4 is a rectangle with inputs and outputs appropriately identified.

8-15. The one-side output of the flip-flop assumes the ONE state when a trigger pulse of the correct polarity is applied to the set (S) input. The zero-side output assumes a logical ZERO level when a trigger pulse of the correct polarity is applied to the clear (C) input. The flip-flop outputs reverse their states when a trigger pulse is applied to the toggle (T) input.

8-16. ONE-SHOT FUNCTION. One-shot functions are represented in the logic diagrams by a square block. As shown in figure 8-4, the pulse duration (or delay) of



the one-shot output is identified within the symbol. When activated by a trigger pulse input of the proper polarity, the output of the one-shot changes state (logical level) and remains at this new level for the duration of the active time of the device. At the end of the delay, the one-shot output returns to its original state.



M1509-22

Figure 8-4. Flip-Flop and One-Shot Functions

#### 8-17. GENERAL FUNCTIONS.

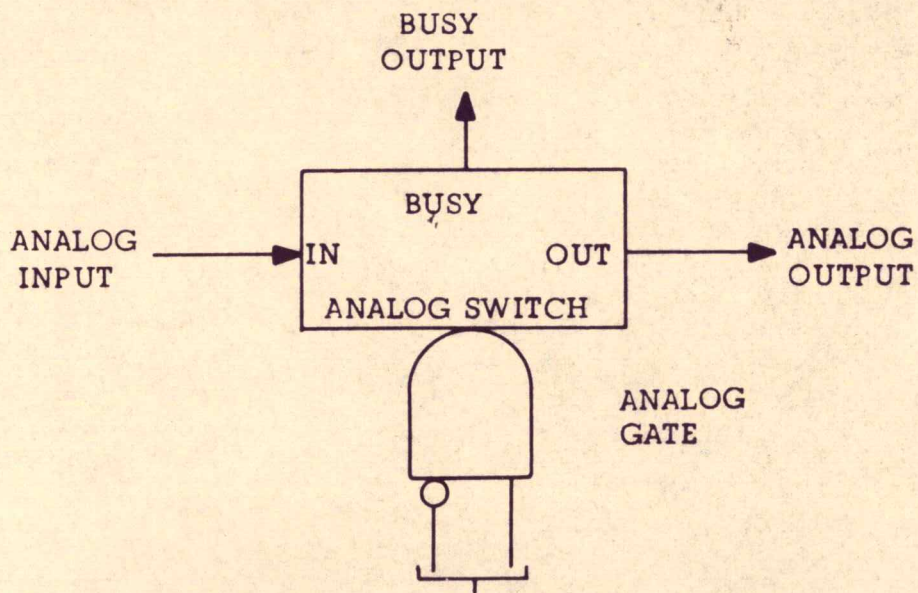
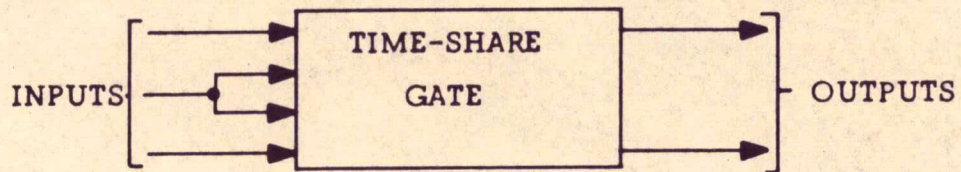
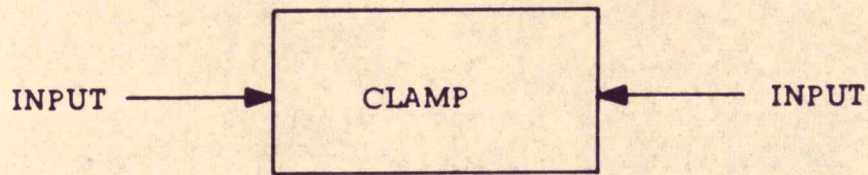
8-18. All functions for which logic symbols are not specified are symbolized by a rectangle. Each rectangle is labeled so as to easily identify the function performed and input/output pin letters. Figure 8-5 illustrates several examples of general functions.

#### 8-19. LOGIC DIAGRAMS.

8-20. Detailed logic diagrams for the C14-210-0003 are presented in figures 8-6 through 8-17. Inputs and outputs of each figure are appropriately labeled by signal name and connector pin designation to identify where the signal originated or its destination.

8-21. Individual circuit modules are represented in the diagrams by logic symbols. Each circuit module is identified by a reference designation (such as A8-2) and the corresponding Vector part number. The first portion of the reference designator indicates the plug-in board of which the module is a part and the last portion indicates





GATING SIGNAL INPUTS

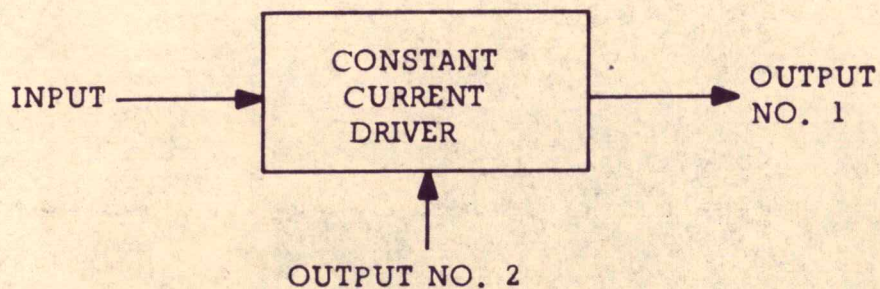


Figure 8-5. General Functions



the physical location of the module on the board. For example, reference designation A8-2 identifies the second module contained on plug-in board A8.

8-22. Major system test points are identified in the diagrams by a star-encircled arabic number. Twenty-seven major test points are electrically accessible at connector J3.

8-23. WIRING DIAGRAMS.

8-24. Wiring diagrams for the C14-210-0003 are presented in figures 8-18 and 8-19.



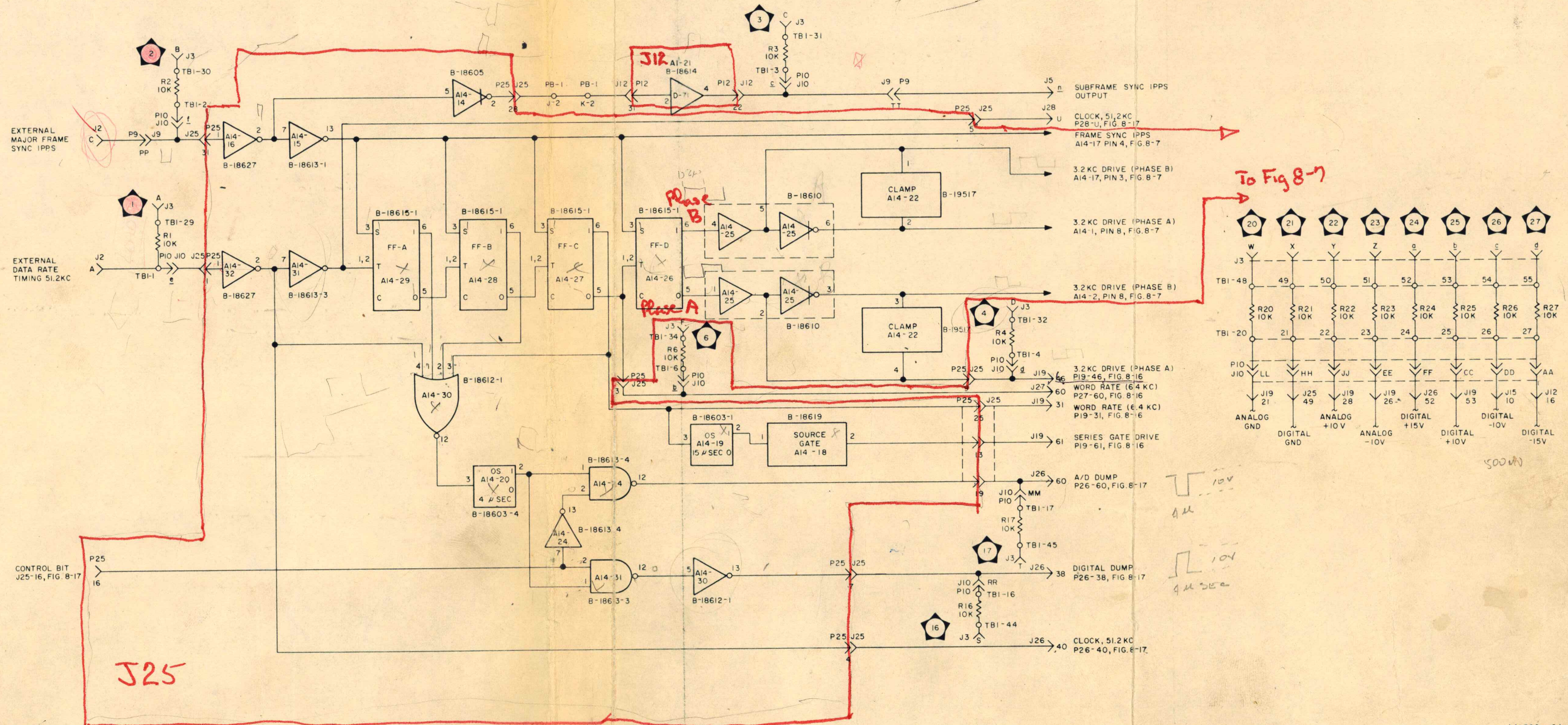


Figure 8-6. Timer Section, Detailed Logic Diagram



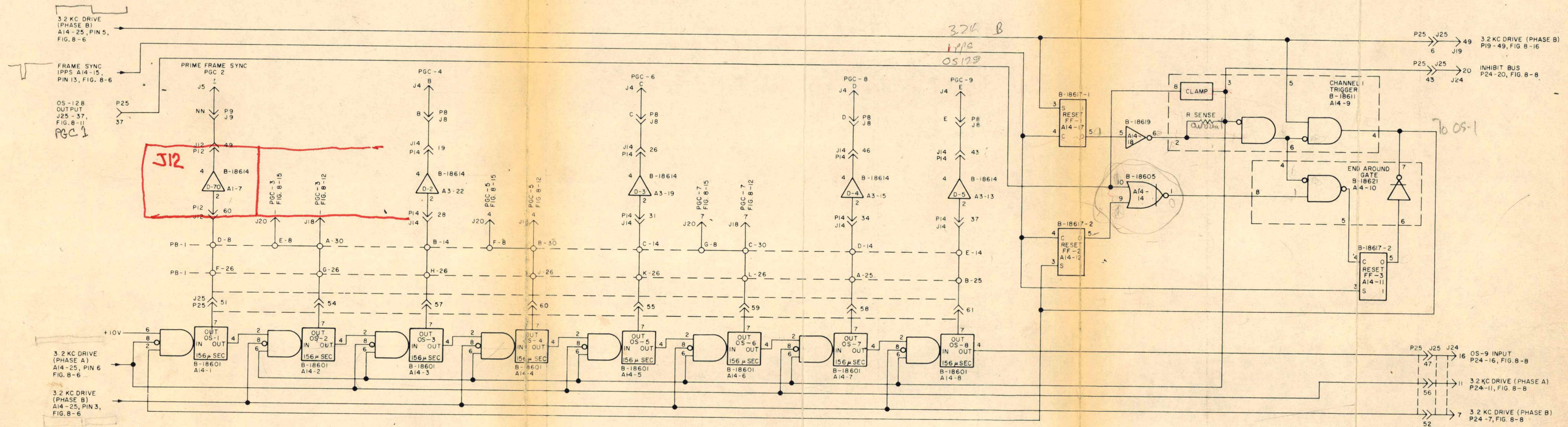


Figure 8-7. Programmer One Shots 1-8 &amp; Timing Gates, Detailed Logic Diagram



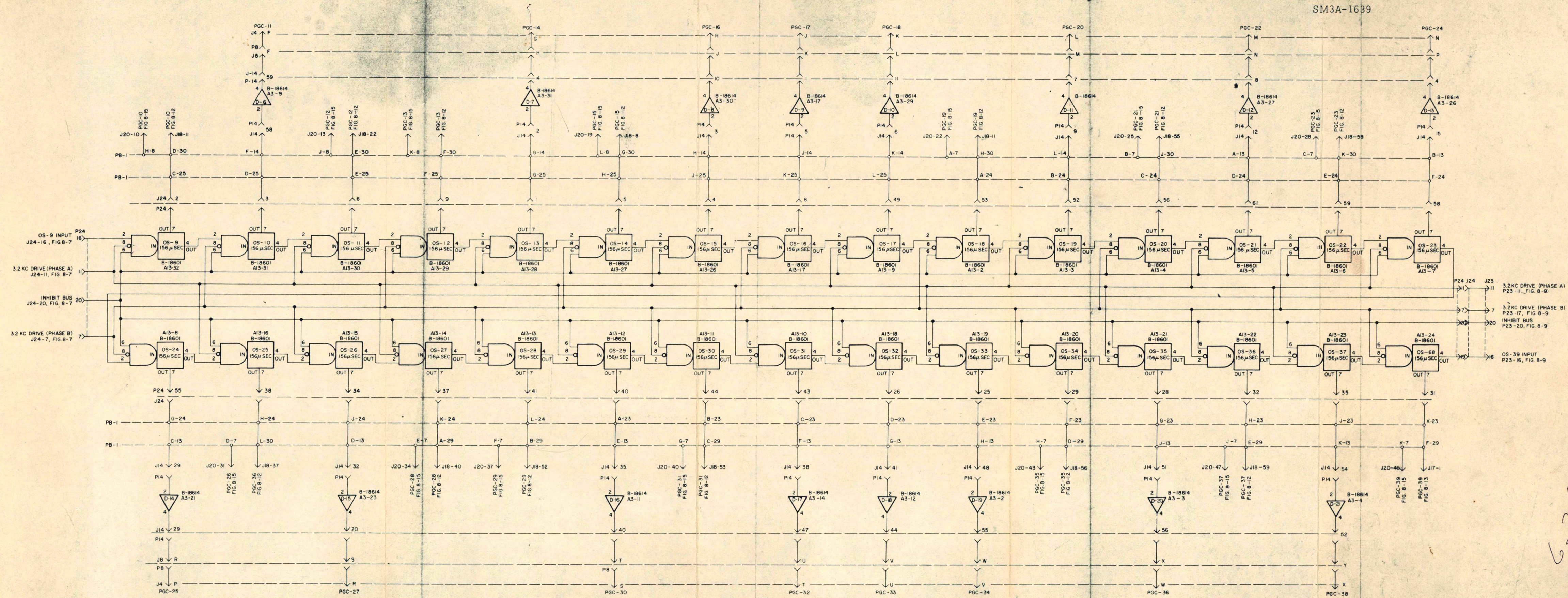


Figure 8-8. Programmer One Shots 9-38, Detailed Logic Diagram

M1509-26



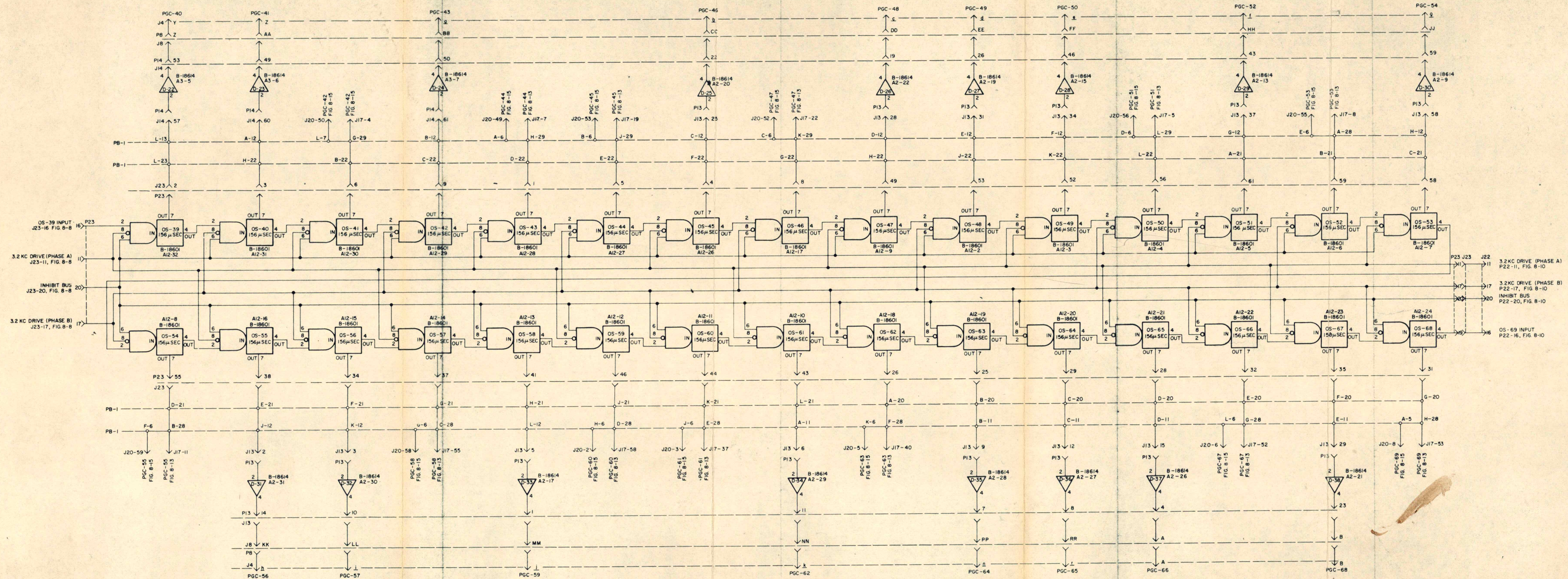
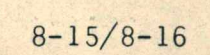


Figure 8-9. Programmer One Shots 39-68, Detailed Logic Diagram







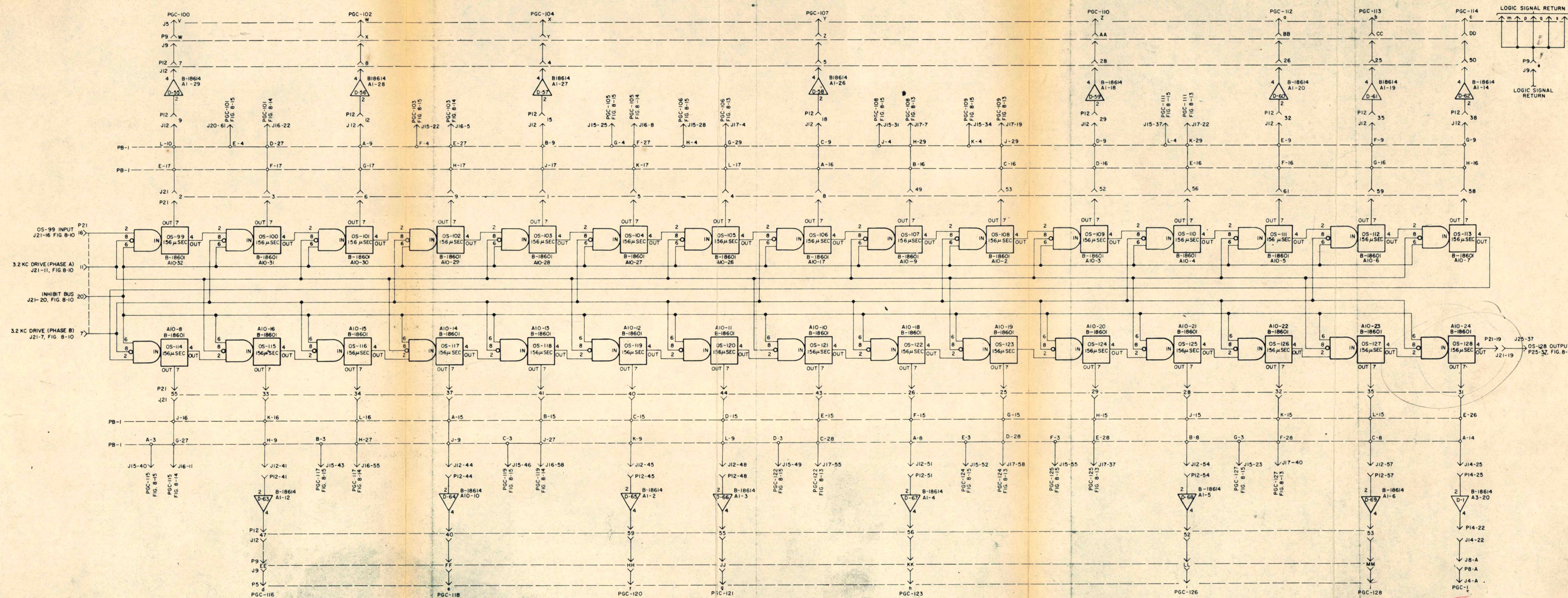
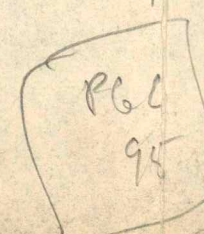


Figure 8-11. Programmer One Shots 99-128, Detailed Logic Diagram





MI 509—30



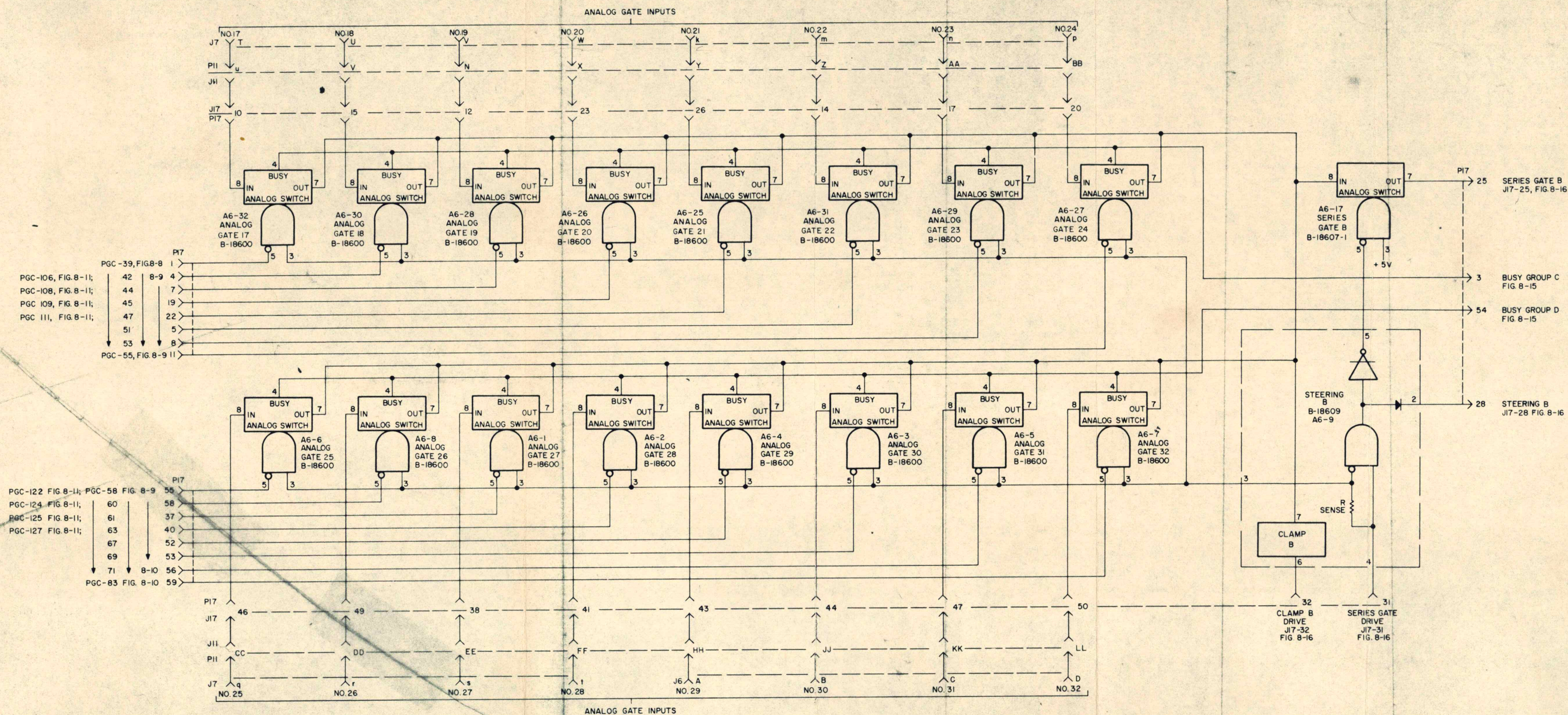
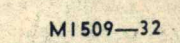


Figure 8-13. Analog Gates 17-32, Detailed Logic Diagram





8-23/8-24



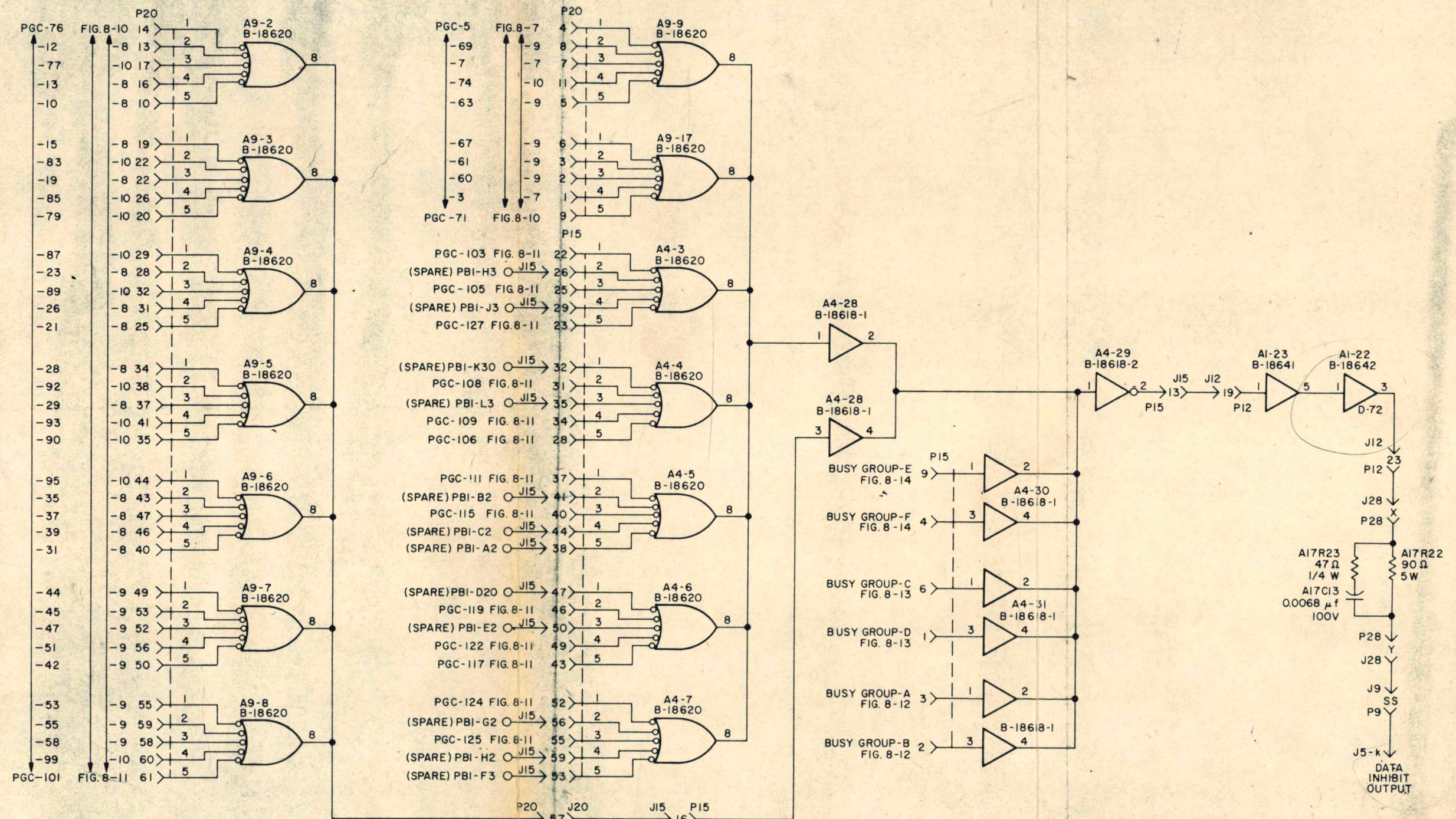
170  
128  
2

Figure 8-15. Data Inhibit Circuitry, Detailed Logic Diagram



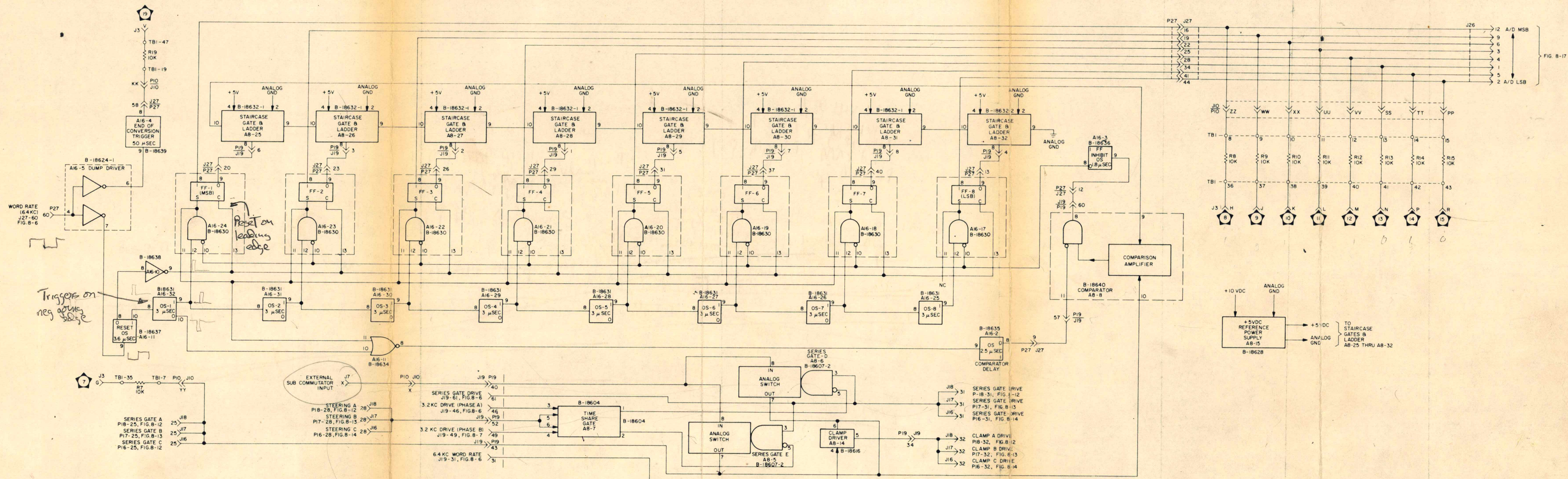


Figure 8-16. Analog-to-Digital Converter, Detailed Logic Diagram



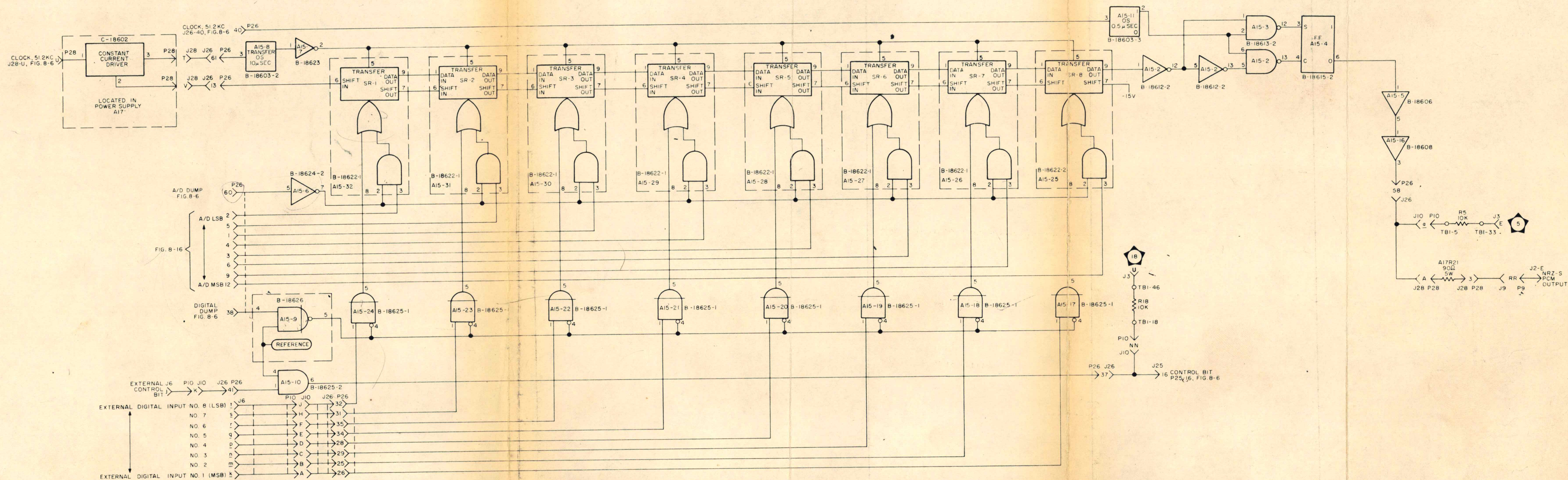


Figure 8-17. Parallel-to-Serial Converter, Detailed Logic Diagram



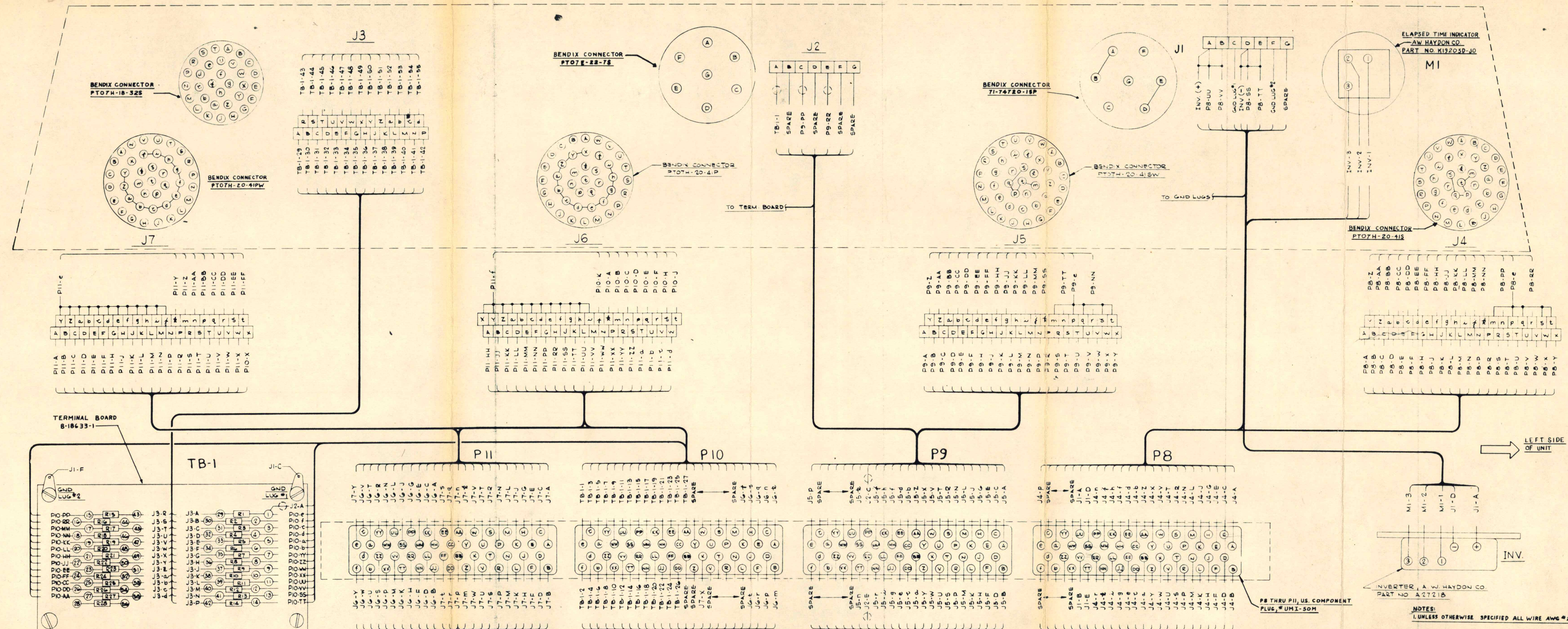


Figure 8-18. C14-210-0003 Wiring Diagram



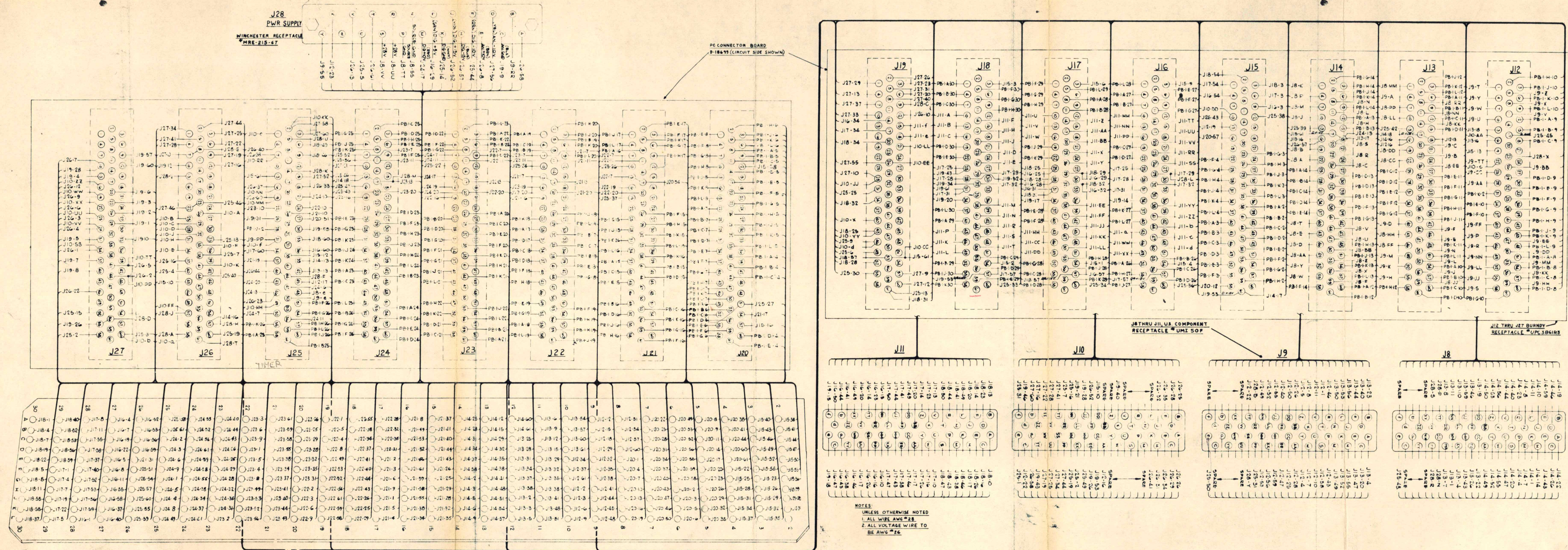


Figure 8-19. C14-210-0003 Interconnection Diagram



## APPENDIX A

## SOURCE DATA

A-1. GENERAL.

A-2. This appendix provides a complete listing of the source data used in the preparation of this manual.

A-3. ENGINEERING DRAWINGS.

A-4. Table A-1 contains a listing of the top assembly drawings for major items of the C14-210-0003. All engineering change notices are incorporated in the latest drawing revision.

Table A-1. Applicable Engineering Drawings

Drawing No.	Revision	Title	Date
B-19130	K	North American Carry-On PCM List of Materials and Data	11-5-65
D-19521	D	NAA Carry-On PCM System Assembly 7765	9-17-65
D-18689	A	Driver & Inhibit Output Card, Wiring Diagram & Assembly	11-4-65
D-18691-2	A	Driver Card, Wiring Diagram & Assembly	11-4-65
D-18691-1	A	Driver Card, Wiring Diagram & Assembly	11-4-65
D-18697	A	Inhibit Card, Wiring Diagram & Assembly	11-4-65
D-18693-3	A	Analog Gate Card, Wiring Diagram & Assembly	11-5-64



Table A-1. Applicable Engineering Drawings (cont )

Drawing No.	Revision	Title	Date
D-18693-2	A	Analog Gate Card, Wiring Diagram & Assembly	11-4-65
D-18693-1	A	Analog Gate Card, Wiring Diagram & Assembly	11-4-65
D-18698	A	A/D Converter, Card A, Wiring Diagram & Assembly	3-1-65
D-18698	B	A/D Converter, Card A, Wiring Diagram & Assembly	11-3-65
D-18692	A	PGC Inhibit Tree Card Wiring Diagram & Assembly	11-4-65
D-18694-4	A	Program One-Shot Card, Wiring Diagram & Assembly	11-4-65
D-18694-3	A	Program One-Shot Card, Wiring Diagram & Assembly	11-4-65
D-18694-2	A	Program One-Shot Card, Wiring Diagram & Assembly	11-4-65
D-18694-1	A	Program One-Shot Card, Wiring Diagram & Assembly	11-4-65
D-18690	D	Program Gates & Timing Board, Wiring Diagram & Assembly	11-4-65
D-18695	B	Parallel-to-Serial Converter Card, Wiring Diagram & Assembly	11-4-65
D-18696	A	A/D Converter, Card B, Wiring Diagram & Assembly	11-3-65
D-19341	E	Power Supply, Card Assembly	11-4-65
C-19129	A	Power Supply Schematic	11-4-65



Table A-1. Applicable Engineering Drawings (cont )

Drawing No.	Revision	Title	Date
C-18602	B	Constant Current Pulse Driver, Module Assembly	11-4-65
B-18600	A	High Level Gate Assembly	12-16-64
B-18601	C	Program One-Shot Assembly	12-28-64
B-18603	E	One-Shot Assembly	3-3-65
B-18604	A	Time Share Gate Assembly	12-16-64
B-18605	C	Inverters Assembly	11-4-65
B-18606	D	Level Conditioner Assembly	3-3-65
B-18607	B	Series Gate Assembly	12-16-64
B-18608	B	Power Output Assembly	12-10-64
B-18609	D	Clamp & Steering Assembly	3-4-65
B-18610	C	Dual Buffer Inverter Assembly	3-5-65
B-18611	D	Channel 1 Trigger Assembly	11-4-65
B-18612	A	NOR Gate & Inverter Assembly	12-4-64
B-18613	C	NAND Gate Inverter Assembly	1-7-65
B-18614	C	Driver Assembly	3-5-65
B-18615	A	Universal Flip-Flop Assembly	1-7-65
B-18616	F	Clamp Driver Assembly	3-3-65
B-18617	B	Reset Flip-Flop Assembly	12-16-64
B-18618	B	Dual Inhibit Gate Assembly	1-4-65
B-18619	D	Source Gate Assembly	3-2-65



Table A-1. Applicable Engineering Drawings (cont )

Drawing No.	Revision	Title	Date
B-18620	A	PGC Inhibit Tree Assembly	12-16-64
B-18621	B	End Around Gate Assembly	2-22-65
B-18622	A	Shift Register Assembly	1-4-65
B-18623	A	Transfer Driver Assembly	11-4-65
B-18624	B	Dump Driver Assembly	11-3-65
B-18625	C	Input Buffer Assembly	11-4-65
B-18626	B	Input Buffer Strobe Assembly	12-16-64
B-18627	D	Input Buffer Assembly	11-4-65
B-18628	B	+5V Reference Supply Assembly	11-3-65
B-18630	A	Flip-Flop Assembly	12-16-64
B-18631	A	One-Shot Assembly	12-16-64
B-18632	B	Staircase Gate & Ladder Network Assembly	12-16-64
B-18634	A	Comparator Delay One-Shot Trigger Assembly	12-16-64
B-18635	A	Comparator Delay One-Shot Assembly	12-16-64
B-18636	B	Flip-Flop Inhibit One-Shot Assembly	11-3-65
B-18637	B	Reset One-Shot Assembly	11-3-65
B-18638	A	Reset Switch Assembly	11-3-65
B-18639	A	End of Conversion Trigger	12-16-64
B-18640	--	Comparator Assembly	10-19-64



Table A-1, Applicable Engineering Drawings (cont )

Drawing No.	Revision	Title	Date
B-18640	A	Comparator Assembly	3-16-65
B-18641	C	Level Conditioner Assembly	3-3-65
B-18642	A	Power Output Assembly	12-16-64
B-19517	A	Clamp Assembly	1-21-64
E-18629	B	North American PCM Inter-connection Diagram	11-4-65
E-18651	--	North American PCM Harness Assembly	12-18-64
B-19321	A	Card Extractor PCM 7765	1-20-65
C-19762	--	PC Extender Assembly	12-30-64

A-5. SPECIFICATIONS

A-6. Table A-2 contains a listing of the specifications applicable to the C14-210-0003.

Table A-2. Applicable Specifications

Specification No.	Revision	Title	Date
MC901-0141 (3)	Deviations identified in ME901-0141-0003.	Carry-On Pulse Code Modulation System Spec Control Drawing.	Basic document 8-3-63; deviations 9-2-65.

A-7. MISCELLANEOUS DOCUMENTATION.

A-8. Table A-3 contains a listing of miscellaneous documentation directly related to the C14-210-0003.



Table A-3. Miscellaneous Documentation

Document No.	Revision	Title	Date
Test Plan 2-730-97	B	Acceptance Test Procedure for Carry-On Pulse Code Modu- lation System, Vector Model 7765.	1-19-65

A-9. MODIFICATION DATA.

A-10. Table A-4 contains a listing of the modification kits applicable to the C14-210-0003.

Table A-4. Modification Data

Drawing No.	Title	Date
B-20914	Modification Kit, PCM System	10-1-65