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TECHNICAL MANUAL

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(S-IU-204 Thru 212/501 Thru 515)

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LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES, DESTROY SUPERSEDED PAGES

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

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S-IU-209 Tab			
5-18A Added	1 April 68		
5-18B Blank Added	1 April 68		
S-IU-210 Tab			
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5-18D Blank Added	1 April 68		

* The asterisk indicates pages changed, added, or deleted by the current change.

Original	Revision	Change No.1	Change No.2					
1 June 1966	1 Mar 1967	1 Apr 1968	1 Aug 1969					

CIRCUIT DESCRIPTION

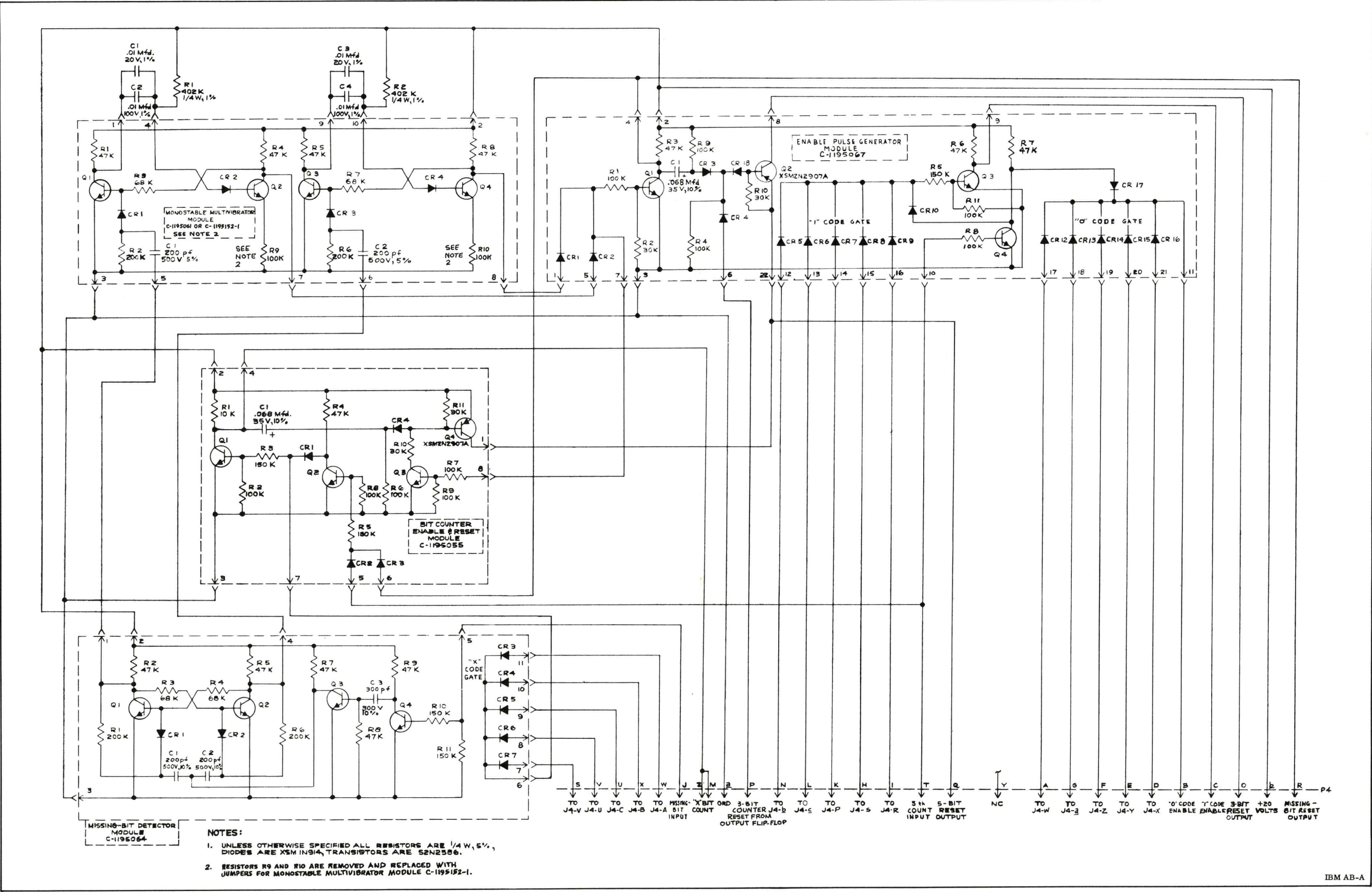
The missing-bit input pulse is amplified by Q4(064) and differentiated by C3. The resulting positive trailing edge of the pulse turns ON Q3 driving its collector to ground. The resulting negative-going voltage triggers the bistable multivibrator Q1 and Q2. The set and reset outputs of the flip-flop are coupled to two monostable multivibrators Q1(061) and Q2, and Q3 and Q4 (MVB1 and MVB2, Figure 2-5). The MVB's will alternately trigger as the flip-flop is set and reset. Each multivibrator's output pulse width is set to 5.4 milliseconds. This is a slightly longer period than the pulse repetition time interval (5.0 milliseconds). The outputs from the collector Q2 and the collector Q4 are coupled to an OR gate (OR5, Figure 2-5) consisting of CR1(067), CR2(067) and Q1(067). The collector of Q1 is driven to ground by the positive output pulse from the MVB's. In normal operation, the collector is held to ground, as it always has at least 1 input. The first "X" bit detected therefore starts the missing-bit clock consisting of the MVB1, MVB2, and OR5.

The output of Q1 is used to drive several other gates. The first of these is the OR gate (OR6, Figure 2-5) consisting of CR2(055), CR3(055) and Q2(055). The other input to the OR gate is the fifth-count input from the 5-bit counter. If either of the diodes CR2 or CR3 is forward biased by a positive voltage, the collector of Q2 is grounded enabling an "X" bit count. Therefore, the "X" bit count pulse from the collector of Q1 is present when (1) either the output of the missing-bit OR gate, Q1(067), or the fifth-count input pulse is positive, and (2) the output of the "X" code gate is at a low voltage, [junction of R3 and CR1(055).] Other conditions at the first "X" bit are: (1) Q3(055) is OFF because the missing-bit clock is not running, i. e., there is a low voltage at the base of Q3, and (2) Q4 is conducting because of the bias voltage formed by R11, CR4, and R6. When CR4 is prevented from conducting by the positive "X" bit pulse from C1, Q4 ceases conduction causing a negative pulse at the col-

lector. This pulse is used to reset the 5-bit counter. Thereafter, as long as either missing-bit MVB is at a high voltage, Q3 is biased ON, hence biasing Q4 ON by the voltage across R11 and preventing any further reset pulses to the 5-bit counter. In summation, the first "X" bit starts the missing-bit clock providing a positive voltage is on the base of Q3 inhibiting further reset pulses to the 5-bit counter. This is possible because the 5-bit counter resets itself as discussed earlier.

The 3-bit counter is reset at the time of the 5-bit counter reset, i. e., by the first "X" bit count. This is accomplished through an OR gate (OR7, Figure 2-5) consisting of CR3(067), CR4(067) and Q2(067). Transistor Q2 is normally ON, due to the bias from CR18 and R4. When the 5-bit (negative) reset pulse occurs at the collector of Q4(055), it is directly coupled to the emitter of Q2(067), thereby providing a reset to the 3-bit counter. The 3-bit counter can also be reset through Q1 and C1 by the positive pulse from the monostable multivibrator. The pulse reverse biases CR18, turning OFF Q2 and producing a negative pulse. A positive pulse (computer reset) from the output flip-flop through CR4 will also reset the counter in a similar manner at the completion of data transfer to the LVDA.

The "1" code AND gate (AND6, Figure 2-5) is composed of diodes CR5(067) through CR10, Q3 and Q4. The fifth-count input pulse turns ON Q4 allowing the AND gate, CR5 through CR9, to control Q3. The collector of Q3 is at ground at all times except when all anodes of the diodes are at a low voltage and this occurs precisely when the correct "1" code is written into the 5-bit shift register. At this time Q3 turns OFF, providing a positive "1" data pulse. Therefore, a "1" is generated if the correct code is written into the 5-bit shift register and if the pulse count from the 5-bit counter is present. Q4 also enables the "0" code gate to provide a "0" code enable to module (058) of Figure 2-9.



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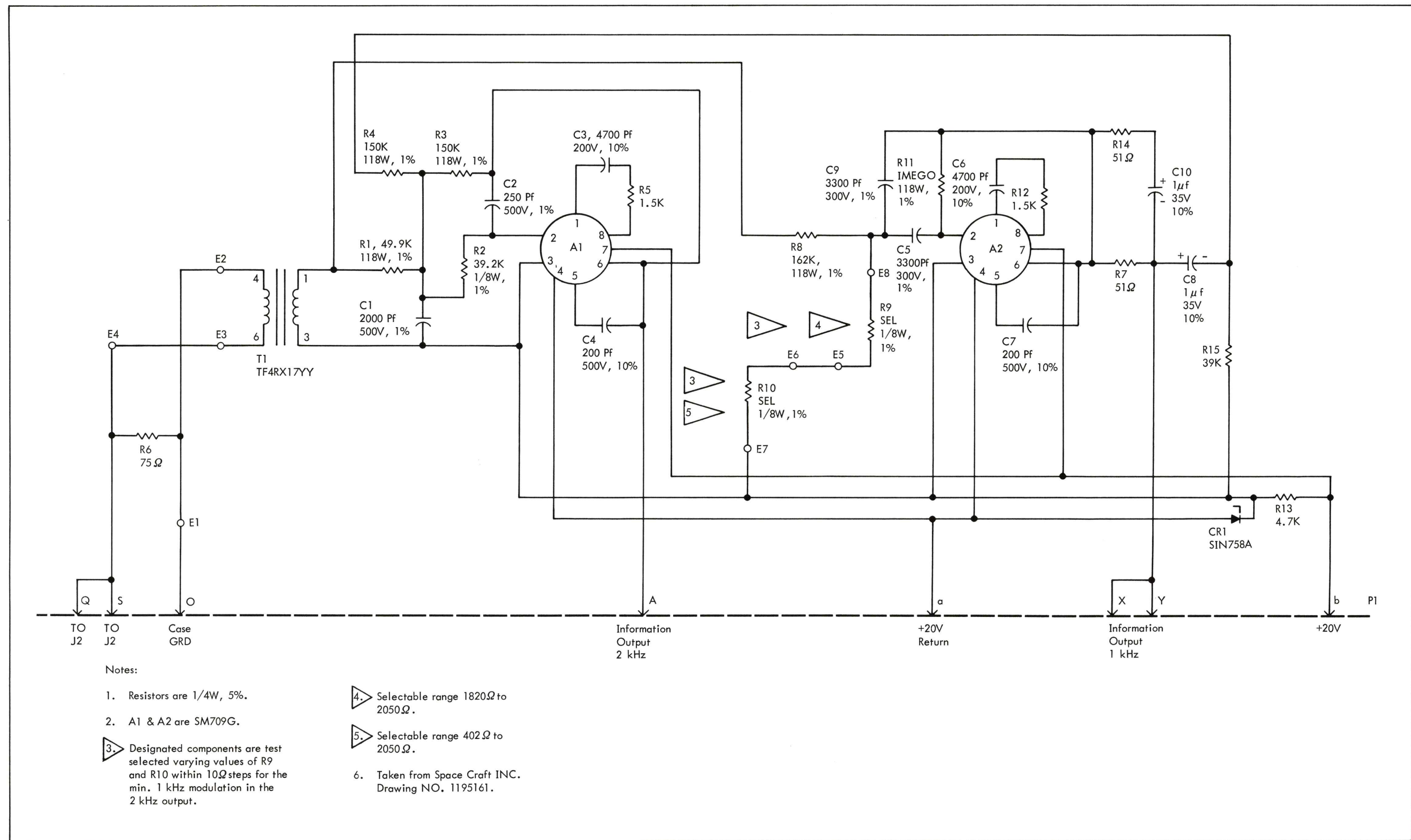
Figure 2-10
Missing-Bit Detector Schematic
2-23/2-24

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

- 1** The differences specified on the S-IU-206 and S-IU-208 Data Sheets also apply to S-IU-506.
- 2** Figure 506-1 replaces the PSK filter schematic, Figure 2-7.
- 3** Figure 506-2 and 506-3 replace the sub-bit detector schematic, Figure 2-19.

CIRCUIT DESCRIPTION

The function of the filter circuit is to separate the 1 kHz reference signal and 2 kHz data signal from the PSK signal waveform. The PSK signal is applied at at connector J2 and then transformer coupled through T1 to two active filters. One active filter is a band-pass filter centered on 1 kHz; the remaining filter is a low-pass filter with a cutoff just above 2 kHz and having a notch at 1 kHz to suppress the reference signal. The output of the bandpass filter is a 1 kHz sine wave which is in-phase with the 1 kHz component of the composite PSK signal. The output of the low-pass filter is a 2 kHz data signal which is phase shifted -28.8° from the 2 kHz component of the composite PSK signal.

Figure 506-1
PSK Filter Schematic

LOGIC DESCRIPTION**PSK FILTER**

The PSK composite signal (waveform (A)) is applied to two active filter circuits; a low-pass filter and a bandpass filter. The low-pass filter removes all signals above approximately 2 kHz and removes nearly all of the 1 kHz signal, thus the output (waveform (B)) of this filter is essentially 2 kHz PSK data (a phase shift of -28.8° occurs with respect to the input signal). The bandpass filter is centered on 1 kHz, and the output (waveform (C)) from this circuit becomes the 1 kHz reference frequency (F_r).

SUB-BIT DETECTOR

The PSK filter outputs are applied to the sub-bit detector to generate "1" and "0" sub-bit outputs and to shift the outputs to the 5-bit counter. The sub-bit detector also supplies count pulses to the missing-bit detector circuit.

F_r is applied to a 28.8° phase-shift amplifier which introduces an approximate -28.8° phase shift in F_r , bringing this signal back in phase coherence with the 2 kHz PSK data signal (waveform (D)). F_r is also applied to a 118.8° phase-shift amplifier which introduces a -118.8° ($28.8^\circ + 90^\circ$) phase shift in F_r (waveform (E)), thus making this signal lag waveform (D) by 90° .

$F_r - 28.8^\circ$ and $F_r - 118.8^\circ$ are applied to an exclusive "OR" circuit which has 2 outputs $2F_r$ and $2\overline{F_r}$ (waveforms (F) and (G) respectively). These outputs are 180° out-of-phase with each other and are phase coherent with F_r .

The transformerless demodulator (synchronous detector) uses the $2F_r$ and $2\overline{F_r}$ signals in comparing the phase of the 2 kHz data signal to detect a sub-bit "1" or "0". When the 2 kHz data signal is in-phase with $2F_r$, a "1" will be detected, out-of-phase, a "0" will be detected.

The output of the transformerless demodulator is applied to the integrator and dump circuits. The integrator is used to accumulate the detector output during the sub-bit time interval; at the end of this period, the dump circuit discharges the integrator in preparation for the next sub-bit integration. The steering circuits condition the "1" and "0" sub-bits to the logic levels required to gate data to the 5-bit counter circuits.

$F_r - 28.8^\circ$ and $F_r - 118.8^\circ$ are also used for generating timing signals for the integrator circuit, the steering circuits, and for generating shift output pulses for the 5-bit shift register, in addition to count output pulses for the 5-bit counter circuit.

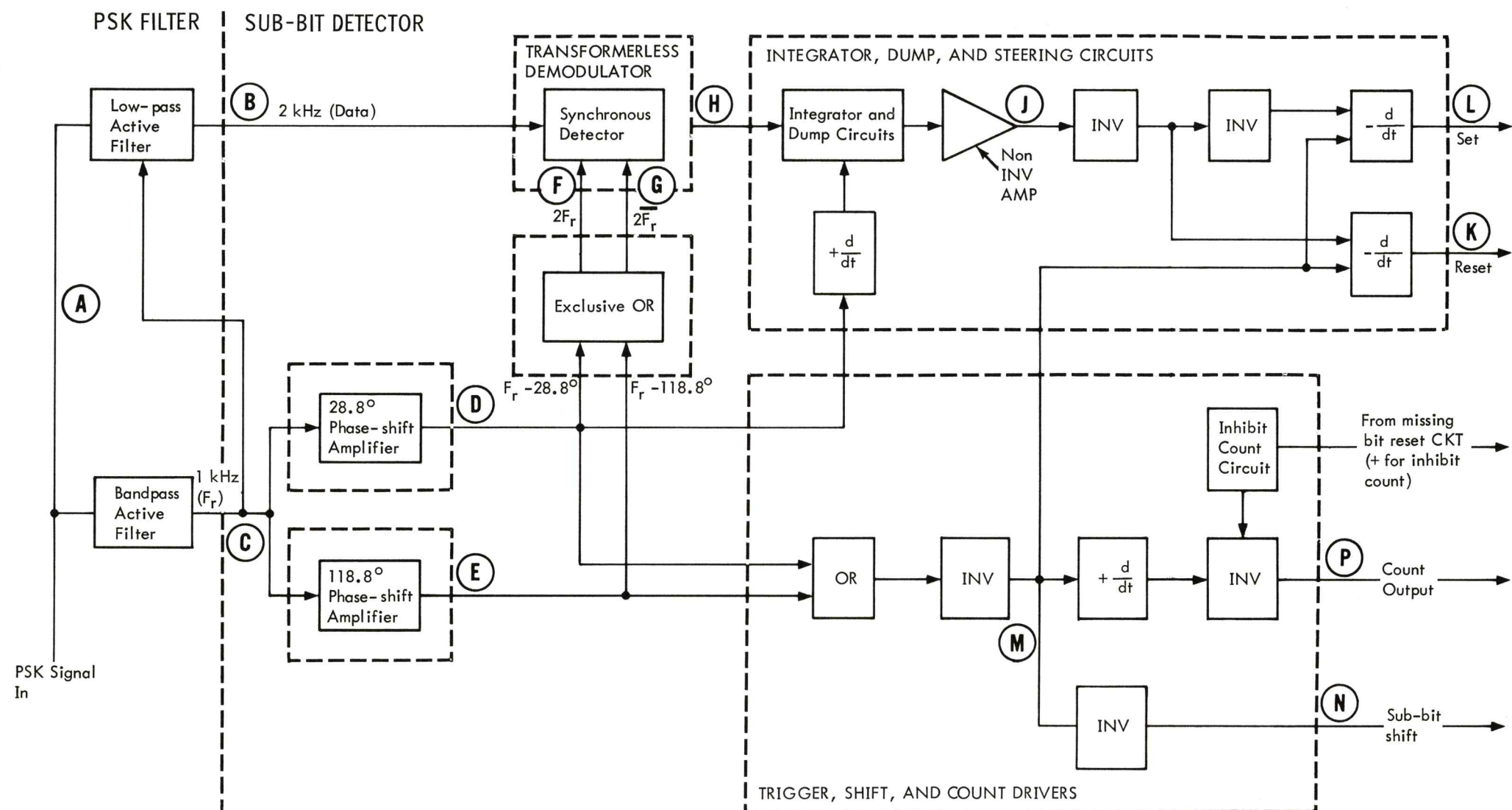
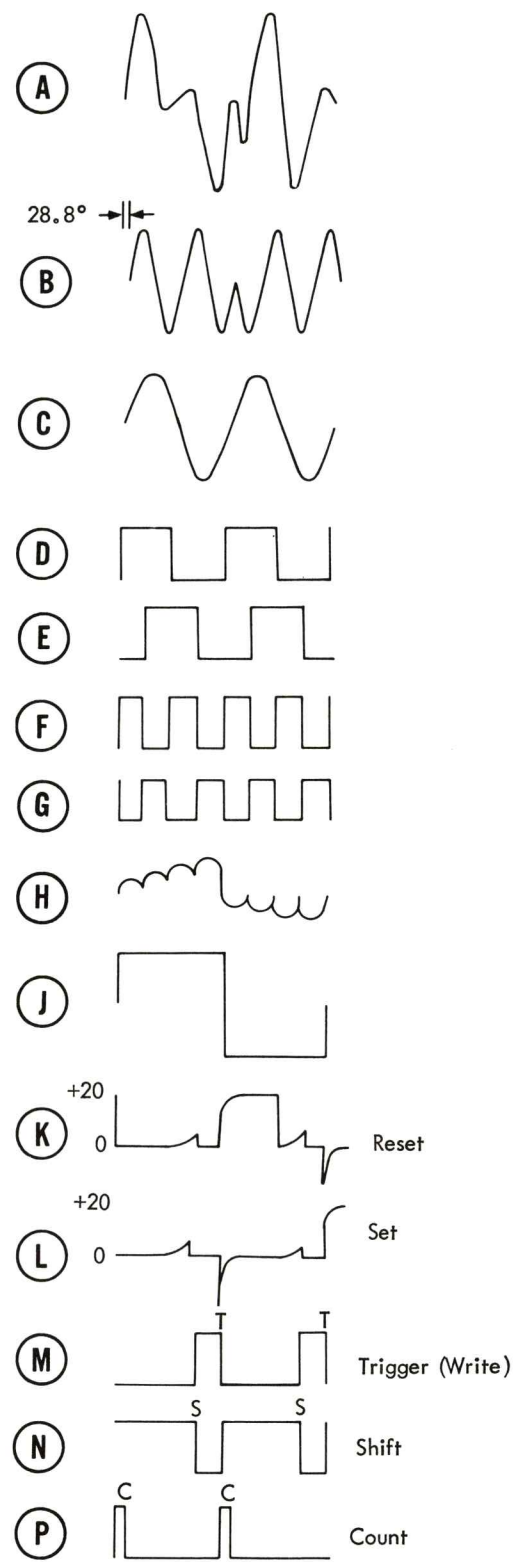


Figure 506-2
PSK Filter and Sub-Bit Detector Logic Diagram

CIRCUIT DESCRIPTION

The 1 kHz input is applied to two phase-shift amplifiers which shift the phase -28.8° and -118.8° ($90^\circ + 28.8^\circ$) respectively.

The IC3 circuitry, shown in the 28.8° phase-shift amplifier, delays the signal -28.8° and also provides a square-wave output.

The IC4 and IC5 circuitry provides a function similar to the IC3 circuitry except that the phase shift is -118.8° .

The outputs from the -28.8° and -118.8° phase-shift amplifiers (designated $F_r -28.8^\circ$ and $F_r -118.8^\circ$) are applied to an exclusive "OR" logic circuit. The output from this circuit will be a 2 kHz square wave which is lagging -28.8° from the incoming 1 kHz component of the PSK signal. This output is designated as $2F_r$ and the inverse function as $2F_r$.

The transformerless demodulator (synchronous detector) uses the 2 kHz data signal and the $2F_r$ and $2F_r$ signals to demodulate the 2 kHz data signal into a series of positive or negative going pulses depending upon the phase relationship of the data with respect to $2F_r$ and $2F_r$. The demodulator consists of a dual chopper circuit followed by a differential amplifier. When the 2 kHz data signal is in-phase with $2F_r$, the output will be a series of positive-going, sine-shaped pulses. When data is out-of-phase with $2F_r$, negative going pulses are generated. Note waveform (H), Figure 506-2 which seems to disagree, this is created by the integrator function in the following circuit.

The demodulator output is next applied to the integrator circuit (R12 and C3). The integrator accumulates the voltage output from the demodulator during the sub-bit period. At the end of the sub-bit period, the dump circuit (Q3 and Q4) will be turned ON briefly to discharge C3 in preparation for the next sub-bit detection. This dump function is turned ON by differentiating the positive-going edge of the $F_r -28.8^\circ$ signal (waveform (D)) Figure 506-2. The output of the dump circuit connects to IC2, an operational amplifier wired as a non-inverting amplifier. This circuit amplifies the serial binary sub-bit waveform and drives an inverter stage (Q5) which translates the signal to a +20 return reference voltage and provides the reset level. This level also feeds another inverter (Q6), which provides the set output level. The set and reset levels are connected to two differentiator circuits (R22, C7) and (R25, C8) which are fed by a square-wave pulse timed to

transfer the serial binary data on the negative-going edge of this pulse (waveforms (M), (K), and (L)), Figure 506-2. The set and reset signals are then applied to the 5-bit shift register steering inputs.

In addition to the data handling circuits described above, the sub-bit detector contains the trigger, shift, and count driver circuits which supply timing and control pulses. The 2 signals ($F_r -28.8^\circ$ and $F_r -118.8^\circ$) are used to generate the necessary timing (waveforms (D) and (E)), Figure 506-2. These signals are applied to an "OR" circuit followed by an inverter which creates the waveform (M), Figure 506-2. Waveform (M) is a strobe pulse for the set and reset outputs. It is also inverted by Q13 becoming waveform (N), Figure 506-2, which is the shift output pulse. In addition, the positive-going edge of waveform (M) is differentiated and applied to an inverter (Q11) which, if not inhibited by Q12, will create an output pulse called the count output signal. Examination of waveforms (M), (N), (P), (K), and (L) will reveal that the following sequence occurs during a sub-bit period.

1. The shift pulse is generated (negative-going shift in waveform (N)).
2. The write pulse is generated next (the negative pulse superimposed on the set or reset levels (waveforms (K) and (L)).
3. The count output pulse is generated (negative shift in waveform (P)). Note that this pulse occurs in the following bit period.

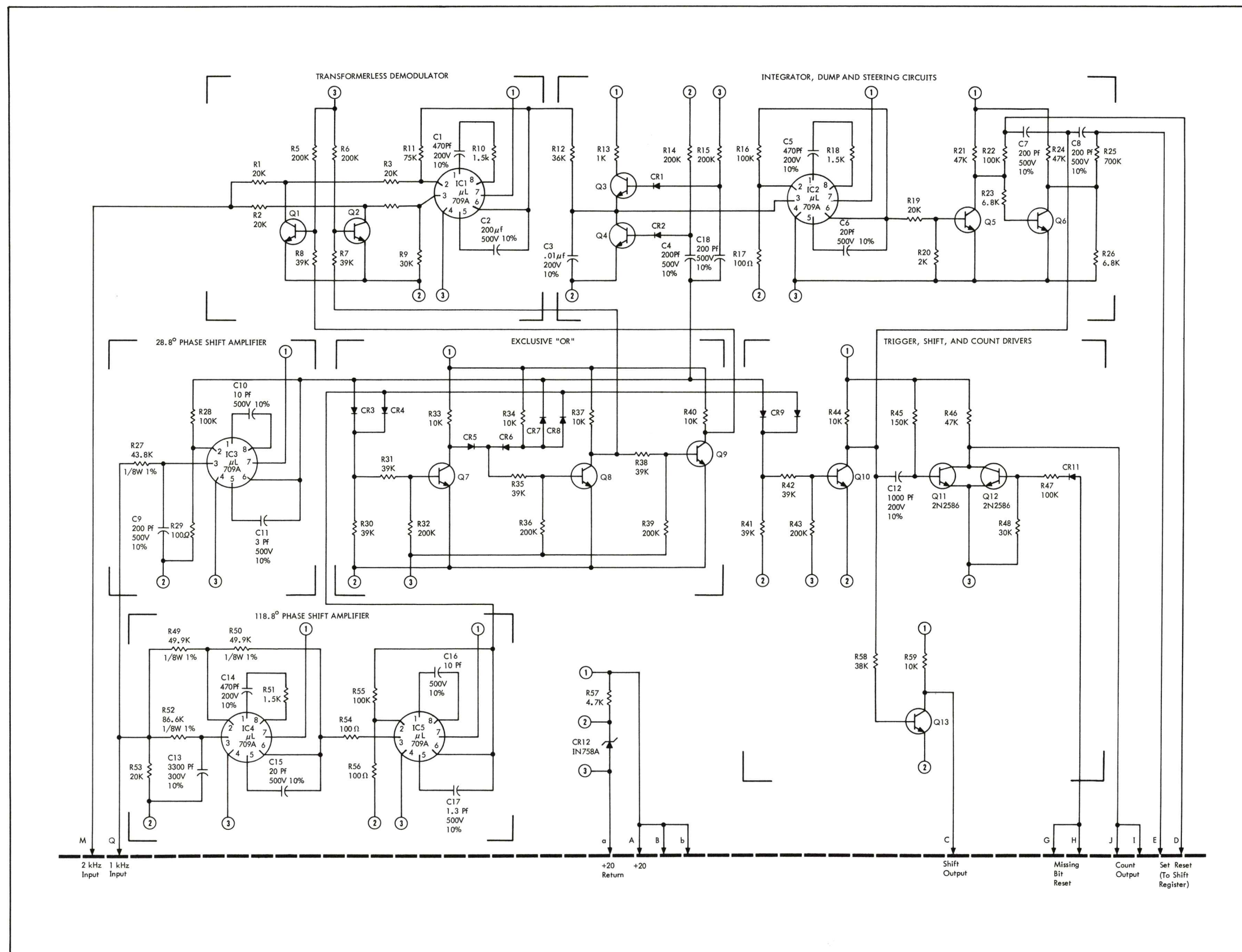


Figure 506-3
Sub-Bit Detector Schematic

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE
VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

1 The differences specified on the S-IU-206,
S-IU-208, and S-IU-506 Data Sheets also apply to
S-IU-507.

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE
VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

- 1** The differences specified on the S-IU-206, S-IU-208, and S-IU-506 Data Sheets also apply to S-IU-508.

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE
VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

- 1** The differences specified on the S-IU-206, S-IU-208, and S-IU-506 Data Sheets also apply to S-IU-509.

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE
VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

1 The differences specified on the S-IU-206,
S-IU-208, and S-IU-506 Data Sheets also apply to
S-IU-510.

NOTE

The above Data Sheet changes also
apply to S-IU-511 thru S-IU-515.
Data Sheet changes for these effec-
tivities will be included with future
manual change activities.

NOTICE

The enclosed pages comprise Change NO. 2 to the following technical manual:

Command Decoder

IBM NO. 66-966-0019

Before inserting these change pages, your manual title page must reflect the following dates:

Basic date	1 March 1967
Change date	1 April 1968

Should these dates on your manual be incorrect, direct inquiries to:

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The enclosed pages change, delete, or supplement the information in your technical manual. Insert these pages (See page A, "List of Effective Pages", contained in the change pages) and destroy the pages they replace. The level of each page is noted by the date at the bottom of the page; original pages are not dated.

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