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FINAL REPORT
INTEGRATED CIRCUIT APPLICATION TO APOLLO UDL

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SECTION I

1. INTRODUCTION

This report contains a description of the design, performance, manufacturing and background information derived in the development of the Engineering Model Integrated Circuit Up-Data Link for NASA Manned Spacecraft Center, Houston, Texas under NASA Contract NAS 9-3458.

Delivery of the Integrated Circuit Up-Data Link and an accompanying adapter drawer from Motorola to NASA/MSC was made on July 12, 1965. The adapter drawer permits UDL operation with existing Apollo UDL Test Equipment.

The Integrated Circuit UDL consists of a Sub-Bit Detector, an I/C Decoder, an Interface Assembly, a Voltage Regulator, a mounting base with internally contained wiring harness, and a cover. Figure 1-1 illustrates the configuration of the delivered Integrated Circuit UDL.

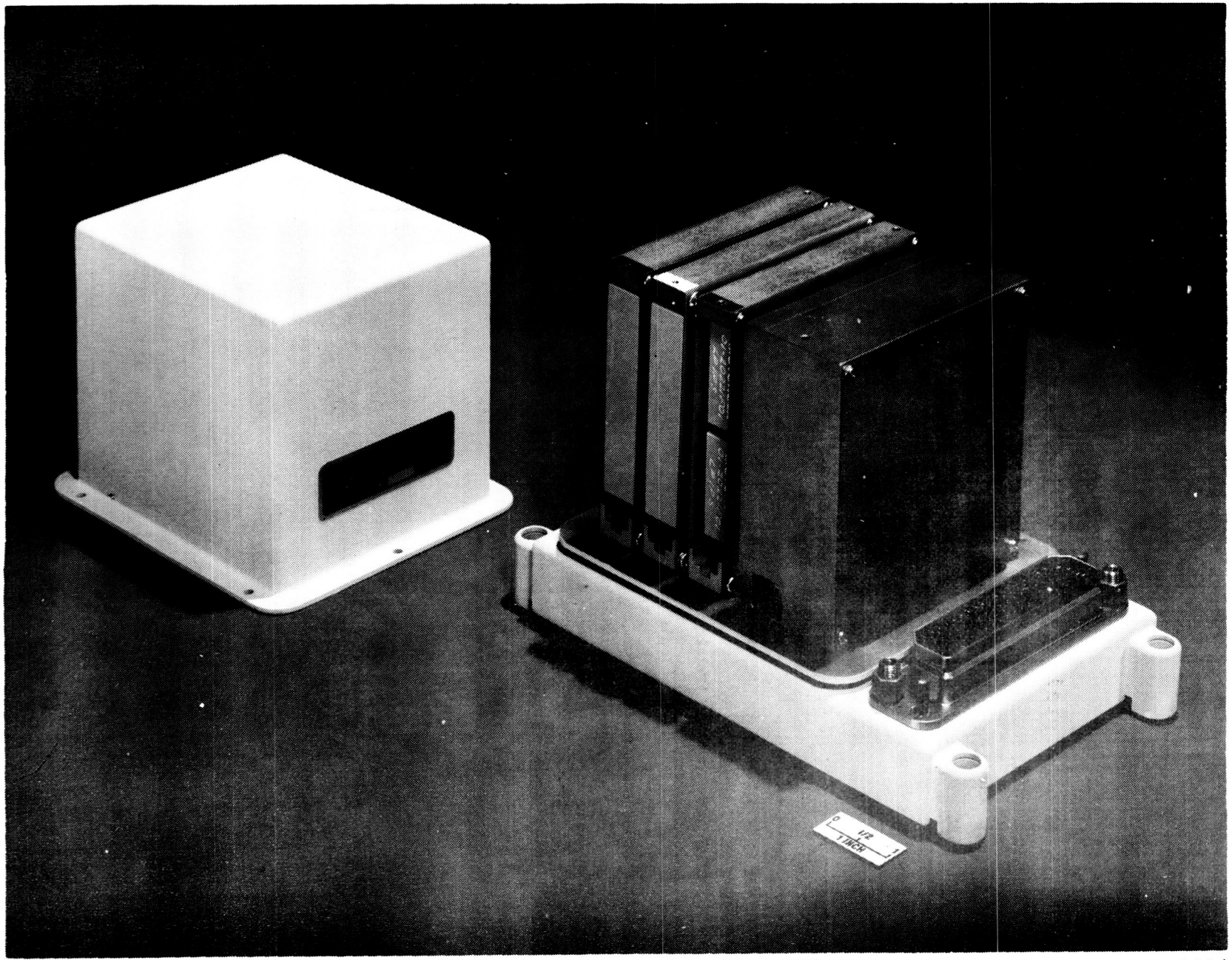

Figure 1-1. Integrated Circuit UDL

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SECTION II

2. PROGRAM OBJECTIVES

The primary objective of this program was to design and develop an integrated circuit decoder for the Apollo Up-Data Link system and to build and test a complete UDL engineering model, less receiver, incorporating the new decoder. The package form factors were to be compatible with Apollo Block II packaging as of November 9, 1964.

2.1 INTEGRATED CIRCUITS

Selection of the appropriate monolithic integrated circuit family for use in future command links was of significant importance because there is an operational need to reduce equipment size and at the same time increase reliability and decrease production costs. An integrated circuit family which has continuing usage will provide the maximum opportunity for these improvements.

The Apollo UDL Decoder was an excellent vehicle to test the selection of an I/C family because it represented a modest, yet significant, equipment size and its present implementation is entirely digital in nature. The practical effects on hardware such as circuit count, interconnection techniques, and system performance can be directly compared with the discrete component equivalent, both on a design basis and finally on a finished hardware basis.

2.2 APOLLO BLOCK II PACKAGING

The UDL equipment was to be packaged in a form factor compatible with the Apollo Block II electronic equipment compartment. This constrained the packaging investigations to techniques most applicable to manned space applications.

2.3 FABRICATION OF THE ENGINEERING MODEL

The fabrication of an integrated circuit decoder provided a live evaluation of integrated circuit package techniques for high

density equipment. Because dimensions are greatly diminished with I/C hardware, unforeseen problems could occur. Interconnections must be well controlled. Interface with discrete input and output functions had to be examined. The packaging of the complete engineering model provided further insight into possible problem areas. Finally, compatibility testing of both an electrical and mechanical nature permitted evaluation of possible weak areas caused by the incorporation of integrated circuits in an existing system.

2.4 SPECIAL TASKS

Reliability, parts procurement, and fabrication process control required to produce high reliability spare hardware for manned vehicles using discrete circuitry have been thoroughly evaluated on the Gemini and Apollo programs. The use of integrated circuits adds a new dimension to the requirements, in that long parts histories and fabrication techniques must be re-examined for applicability to I/C hardware. Rather than delay the development of the engineering model while these areas were being evaluated, a parallel study effort was conducted which should enable future command systems to change to digital integrated circuits with a minimum of problems in specification and purchase of upgraded integrated circuits for installation in well designed, reliable equipments.

SECTION III

3. ELECTRICAL DESIGN

The primary electrical design objective for the I/C UDL was to implement all digital functions of the Apollo Decoder with monolithic integrated circuits. The functional characteristics of the UDL have been retained, except that the UHF receiver has been removed. Input option for receiver audio from an external source as well as S-Band audio has been provided.

A system block diagram for the I/C UDL is shown in Figure 3-1. The four major subdivisions are the I/C Decoder, Sub-Bit Detector, Interface, and Voltage Regulator. Digital integrated circuits are used exclusively in the I/C Decoder. The digital portions of the Sub-Bit Detector and Interface Subassemblies also use monolithic circuits. The remaining portions of these subassemblies use discrete components packaged in cordwood modules, similar to those in the Apollo UDL.

An extensive study of the monolithic integrated circuit families was conducted prior to design of the separate subassemblies. Appendix I, TM 3030-2, describes this evaluation. The selected family is the 930 series diode-transistor circuitry (DTL), operating with a 4-volt supply.

3.1 I/C DECODER

The I/C decoder was designed to satisfy the set of logic functions performed in the Apollo Block I Decoder with maximum utilization of the integrated circuit family. The boundary between the I/C Decoder and the output interface circuitry was not emphasized on the Apollo Decoder. Accordingly, a separation for the I/C UDL was made which minimized interconnection between the two units. Two output functions which could be packaged conveniently in I/C module form were included as part of the decoder.

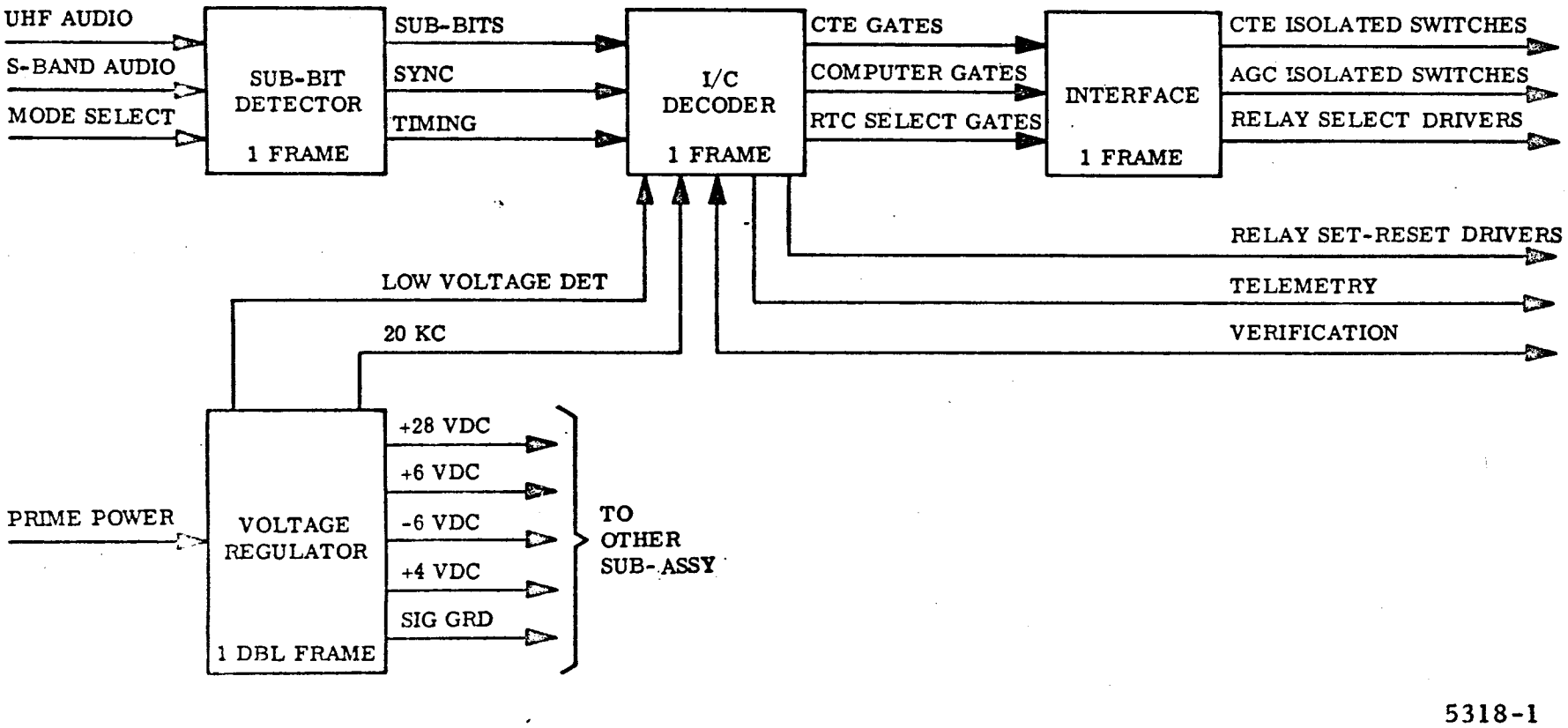

Figure 3-1. I/C UDL Block Diagram

These were the telemetry interface circuits and the RTC set-reset drivers. The remaining output functions will be discussed as part of the interface subassembly.

Figure 3-2 shows a block diagram of the I/C Decoder and the main signal paths. Each block corresponds to one of the nine I/C modules used to package the decoder. The characteristics of the inputs and outputs for the I/C decoder were well defined. To achieve a reasonable implementation efficiency, the internal logic was synthesized from these terminal requirements, rather than a direct translation from the discrete component (25 kc) logic family to the I/C family.

3.1.1 Flip-Flops

The most significant difference in changing from the 25-kc family to the I/C family is the flip-flop triggering mode. The 25-kc family flip-flop is transient-triggered on the negative going transition to the side with low steering. Set and reset functions are also transient-triggered on the negative-going transition. Hence, a signal can be held at either low or high level until triggering is desired. The 930 series flip-flop is a dual-rank, direct-coupled unit operating from a single-phase clock. A clock transition from low to high sets the master stage to the side with high steering. The clock transition back to the low level transfers from the master to the slave which drives the output terminals. Set and reset functions are direct-coupled to the slave flip-flop. A low signal on one of these lines holds the respective output at the high level; hence both set and reset lines must be continuously kept at the high level for triggering operations. A truth table for the two flip-flop types is shown in Figure 3-3.

The most important effect from the difference in flip-flop operation is the requirement to keep the d-c set and reset lines high at all times, except during the operation. With transient triggering, one edge of a signal can be used to set up data and

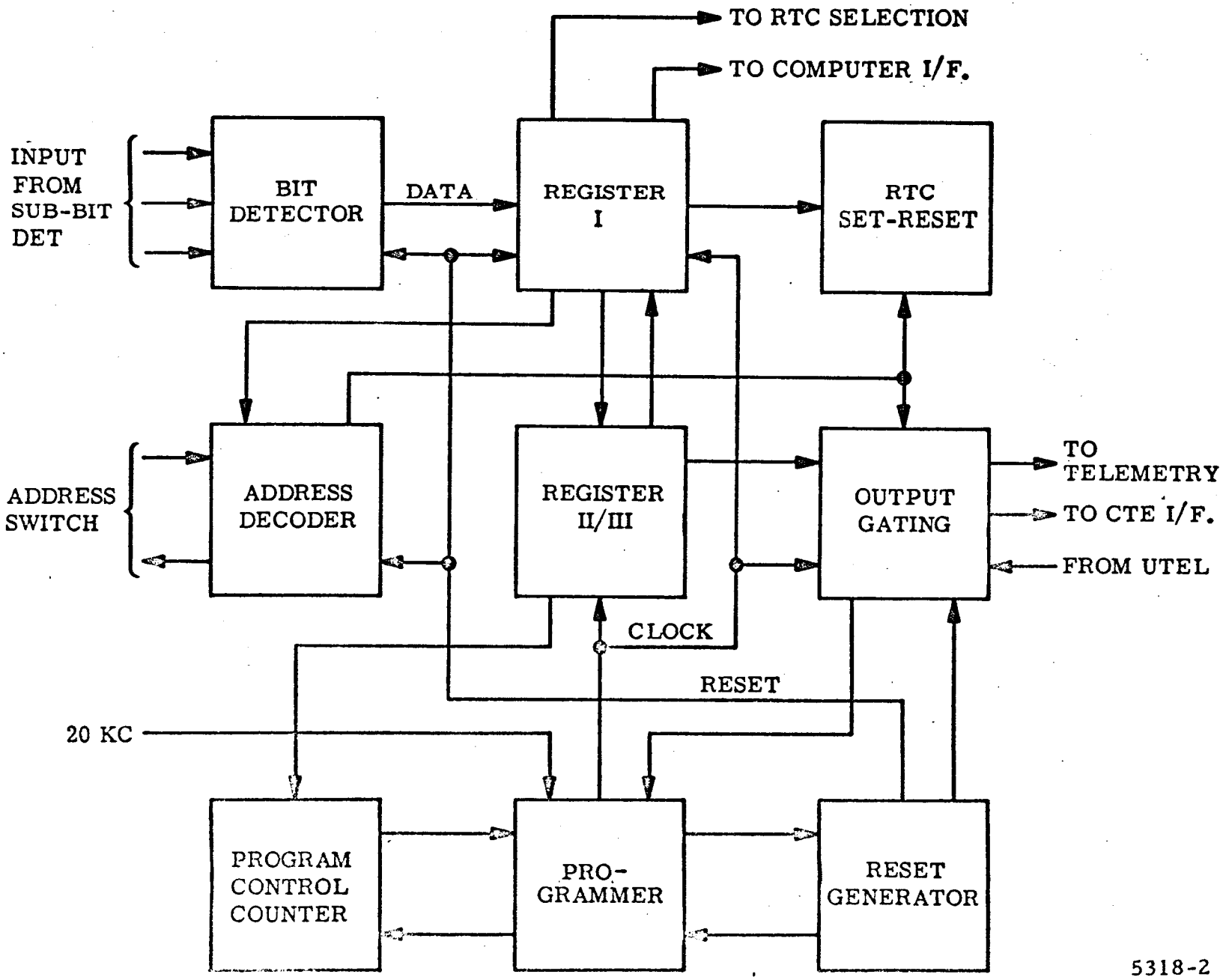

Figure 3-2. I/C Decoder Block Diagram

the complement of the same signal can be used on the trigger line. This would cause a signal race condition on the 945 flip-flop and must be avoided. Some additional logic circuits are thus required, but noise immunity is improved.

25-KC Flip/Flop

T = high going to low

S	R	T	TS1	TS2	Q(t = n)	Q(t = n + 1)
		T	H	H	Q^n	Q^n
		T	L	H	Q^n	H
		T	H	L	Q^n	L
		T	L	L	Q^n	Not Defined
T	T				Q^n	Not Defined
T					Q^n	H
	T				Q^n	L

945 I/C Flip/Flop

S_D	C_D	T	S_1	S_2	C_1	C_2	Q(t = n)	Q(t = n + 1)
H	H	T	L	-	L	-	Q^n	Q^n
H	H	T	L	-	H	H	Q^n	L
H	H	T	H	H	L	-	Q^n	H
H	H	T	H	H	H	H	Q^n	Not Defined
H	H	O	-	-	-	-	Q^n	Q^n
H	L	-	-	-	-	-	Q^n	L
L	H	-	-	-	-	-	Q^n	H
L	L	-	-	-	-	-	Q^n	Both Q & $\overline{Q}$ H

Figure 3-3. Flip-Flop Truth Tables

3.1.2 Loading Rules

The 930 series DTL family is specified for operation with a 4- to 6-volt power supply range. Fanout is slightly reduced for both 4-volt and 6-volt operation as compared with 5 volts. For spaceborne applications, minimum power level is needed; hence, the reduction in fanout for 4-volt operation is warranted. The power differential would be

$$\frac{V_2^2}{V_1^2} = 25/16 \approx 65\%$$

Table III-1 gives the loading rules which were used in the I/C Decoder design for -40°C operation.

TABLE III-1. Loading Rules (Fanout)

	(-55°C) +5 VDC Mfgr Rating	(-55°C) 4 VDC Mfgr Rating	(-40°C) 4 VDC Rating Used
930 Gate	FO = 8	FO = 5	FO = 6
932 Buffer	FO = 25	FO = 18	FO = 20
933 Expander	FO = --	FO = --	FO = --
945 Flip Flop	FO = 10	(Not Available)	FO = 6
946 Gate	FO = 8	FO = 5	FO = 6

The -55°C, 6-vdc rating agrees with those chosen for this system. The only logic circuits requiring a 6-volt supply are the telemetry, computer, and CTE output circuits which are all 930 or 946 gate circuits.

3.1.3 Special Circuits

Two special logic circuits are used in the Apollo decoder, a 50-millisecond monostable multivibrator and a 20-KHz astable

multivibrator. Each circuit requires one cordwood module. Because of the high impedance levels in the 25-kc family, all timing components are a reasonable physical size. The 50-ms monostable is required to sustain the telemetry verification outputs after the program has been completed. Hence no signals are available for stop pulses.

The standard monostable multivibrator for the 930 series I/C family is useful for pulse widths of a few microseconds. The timing capacitor is large at 30 microseconds and a polarized capacitor would be required for 50 milliseconds. The I/C implementation used is a four-stage counter started by the end of program (EOMR pulse). The counter resets after ten 5-millisecond intervals. This implementation requires less than 1/2 an I/C module and is not subject to the noise problems of an MSMV.

No standard astable multivibrator exists for the 930 series I/C family. A dual gate can be interconnected with capacitors but the resulting circuit is sensitive to both supply voltage and temperature. Further, it has no special provision for self-starting. A more stable signal source for the 20-kc used in CTE data transfer has been obtained by using the chopped output from the voltage regulator which operates at 10 kc. A buffer gate directly drives the logic family.

3.1.4 Decoder Implementation

Implementation of the decoder logic diagram into I/C modules was accomplished on a functional basis to minimize interconnections. The final logic design requires 115 FEB's which are packaged in 9 I/C modules. Expansion capabilities can be accommodated by addition of a tenth I/C module. Table III-2 lists the 9 I/C modules and the FEB complement of each. Logic diagrams of each module are included in Appendix 4.

Two printed circuit boards are used for the decoder. The first holds the bit detector, Register I, Register II/III, and

TABLE III-2. Decoder Components

	930	932	933	945	946	Dual 2N956	Discrete Resistors
Bit Detector	5	0	2	8	1	0	0
Register I	1	2	0	8	1	0	0
Reg II/III	0	0	0	16	0	0	0
RTC Set-Reset	2	0	0	0	0	4	16
Address Decoder	4	1	0	8	2	0	0
Programmer	4	1	0	5	4	0	0
Prog.Control CTR	1	0	1	6	6	0	0
Output Gating	6	0	0	5	3	0	1
Reset Generator	2	1	0	4	1	0	0
Total	25	5	3	60	18	4	17

RTC set-reset modules. The second board holds the five remaining modules. The 30 leads between the two boards are accommodated at the top of the boards by flexible cabling. Dual 30-pin Hughes pin-type connectors accommodate 27 outputs from one board and 25 outputs from the other.

3.2 SUB-BIT DETECTOR

The sub-bit detector receives the modulated PSK audio signal from either an S-band or uhf receiver and provides outputs in digital form for decoder operation. The implementation used in the Apollo Block I design will be used directly, except in the switching from the different inputs (mode switching). A sub-bit detector block diagram is shown in Figure 3-4.

The Apollo sub-bit detector requires 23 cordwood module spaces including 7 digital circuit modules, 5 equivalent module spaces

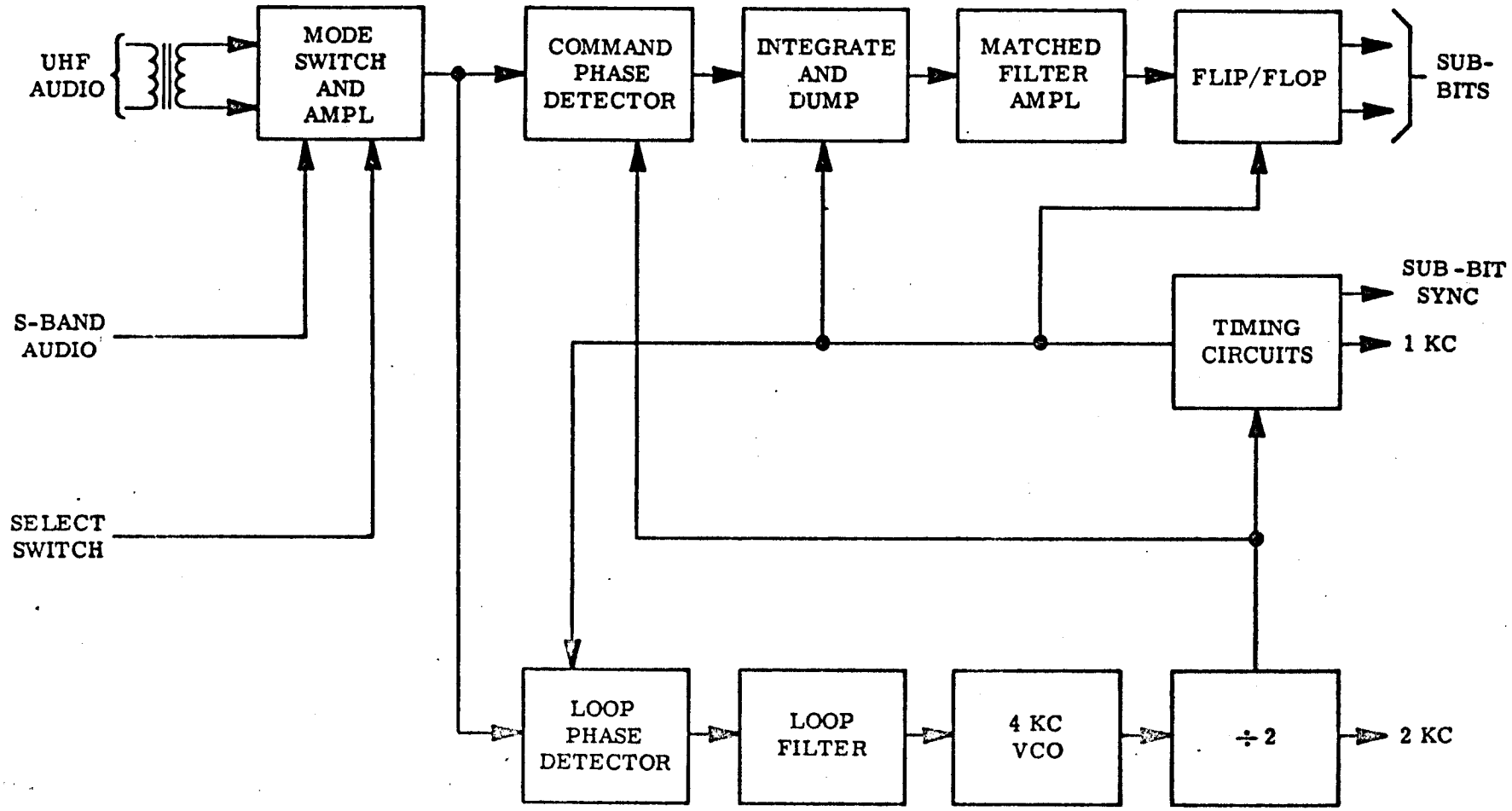

Figure 3-4. Sub-Bit Detector Block Diagram

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for two-phase detector transformers, and 11 special cordwood modules. A detector packaged in this manner would require twice the volume of the I/C decoder. Several design modifications have been accomplished which allow the detector to be packaged in a single frame.

3.2.1 Digital Circuits

Digital functions performed by the sub-bit detector include the following:

(a) Division of the 4-kc voltage controlled oscillator output to 2 kc and 1 kc for use as phase detector reference signals.

(b) Sub-bit synchronization

(c) Sample pulses for the integrate and dump and matched filter amplifier in the data channel

(d) Sub-bit flip-flop storage

The outputs to the I/C decoder can be directly satisfied by substituting 930 series integrated circuits for the equivalent 25-kc circuits. Interface changes in the vco output, matched filter amplifier (mfa) output, phase detector driver inputs, and sample pulses inputs had to be examined to determine whether design changes or special interface circuits would be required to change logic families.

3.2.1.1 VCO Output

The vco output has a buffer stage capable of driving a 930 gate. The output high level exceeds +6 v, the breakdown limit of a 930 input diode. A 15-K resistor to ground will limit the positive excursion and allow direct interfacing.

3.2.1.2 Matched Filter Amplifier Output

The mfa will be driving the steering S_1 and C_1 terminals of a 945 flip-flop (2/3 unit load). This load is three times the steering load of the 25-kc flip-flop. The additional loading

will somewhat desensitize the mfa differential amplifier by reducing stage gain. Bit error tests run with the breadboard subbit detector and limit voltage conditions showed equal performance with either flip-flop, so the mfa design was not altered. A change in the differential amplifier collector resistors from 1500 ohms to 1780 ohms would restore the voltage gain.

3.2.1.3 Phase Detector Driver Inputs

The driver inputs contain a logic level conversion stage from the 25-kc logic family to a 28-volt swing suitable for driving the phase detectors. To minimize loading, these stages use 1 per cent resistors throughout. The 945 I/C flip-flop provides drive capability for heavier loading, but only a 4-volt OFF voltage as opposed to 6 volts in the 25-kc family. The drivers were redesigned using 5 per cent resistors and heavier loading to reduce size and OFF voltage requirements. The revised phase detector drivers use the dual 2N956 in a flat package which is used in the I/C decoder. Accordingly, both drivers have been packaged in a single I/C module while accommodating interface with the I/C family.

3.2.1.4 Sample Pulse Inputs

The 10-μs and 30-μs sample pulses used for the integrate and dump and matched filter amplifiers can be derived from I/C monostables. The load requirements and transition times are satisfactory so no additional buffering is needed. The DTμL 951 Monostable was not available during the design period. The SE160 monostable proved satisfactory for the application, except that a -2 vdc bias supply is required. This has been provided by a voltage divider from the -6 vdc supply. The monostables were found to have an 0.058%^{o}C temperature coefficient over the range from -40^{o}C to 85^{o}C which is easily satisfactory.

3.2.2 Mode Switch

The mode switch module provides switching circuitry to accept either uhf audio signals or S-band audio signals. The mode switch

output is a low impedance linear signal suitable for driving the synchronization and command phase detector transformers. The Apollo Block I contains the uhf receiver and supplies receiver voltages. Mode switching is provided by disabling the S-band input and turning power on the receiver. The mode switch operates from receiver supply voltages and uses the phase detector transformer for d-c isolation.

The mode switch for the I/C UDL must operate with a separate uhf receiver running from its own supply voltages. Direct current isolation is required at the uhf signal input to the switch. All mode switch circuitry must operate from UDL supply voltages. The mode switch design is given in Appendix III.

3.2.3 Phase Detector Transformer

The Apollo Sub-Bit Detector contains two phase detector transformers, both driven from the output of the mode switch. One transformer is chopped at a 1-kc rate to determine the phase relationship for the synchronization signals in the phase-locked loop. The second operates at 2 kc for recovery of data in the command channel. The most critical requirement on the transformers is a linear, minimal phase shift in the band from 250 cps to 4 kc.

A single transformer with four secondaries can be used to perform this function, if sufficient isolation is provided from one set of secondaries to the other pair, and if the reflected source impedance can be held sufficiently low. Transformer size must be compromised to minimize the phase shift which appears as a signal loss. The transformer developed for this program has a 1:5:5:5:5 turns ratio as compared to two 1:10:10 transformers. The difference in signal gain is provided by the mode switch. Each pair of secondaries is bi-filar wound with a split coil form used to separate the pairs.

The final transformer was tested with the new mode switch in the sub-bit detector breadboard. Bit error tests showed a

difference of less than 0.2 db between performance of the single transformer and the double transformer designs. The single transformer is approximately the size of one of the two previous transformers. By eliminating one core, one primary, and several connections, calculated reliability is substantially improved. The salient characteristics for the transformer are as follows:

Primary Inductance	500 mh at 1 kc
Turns Ratio	1:5:5:5:5
Capacitance (Secondaries 1 and 2 to 3 and 4)	100 pf maximum
Phase Shift (250 cps to 4 KC)	5^{o} maximum
Source Impedance	50 ohms maximum
Load Impedance	50 K ohms each secondary (switched)

3.2.4 Sub-Bit Detector Implementation

The detector miniaturization efforts allowed the sub-bit detector to be packaged in one frame size equivalent to the I/C decoder. The uhf input transformer has been placed in the base of the UDL as a portion of the wiring harness due to probable future elimination of this transformer. The remaining circuitry is mounted on two printed circuit boards using the sandwiching technique. Table III-3 summarizes the detector modules.

3.3 VOLTAGE REGULATOR

The voltage regulator supplies the DC voltages required for operation of the sub-bit detector, I/C decoder, and interface subassemblies. Additional outputs are a 20-kc square wave signal used in the I/C decoder, and a low output voltage indication which is used to inhibit system outputs. The voltage regulator input is nominally +28 vdc with a +2 volt and -4 volt tolerance.

The basic voltage regulator design is a pulse width modulated supply with a 10-kc chopping frequency. Power requirements for the I/C UDL are similar to the Apollo UDL, except that the -18

TABLE III-3. Sub-Bit Detector Modules

Modules	Discrete Components	Integrated Circuits
Mode Switch	Yes	0
Phase Detector Transformer	Yes	0
Dual Phase Det Driver	Yes	4 Dual 2N956
Command Phase Detector	Yes	0
Loop Phase Detector	Yes	0
Loop Filter	Yes	0
Voltage Control Oscillator	Yes	0
Integrate and Dump	Yes	0
Matched Filter Amp.	Yes	0
Detector Timing	3 Resistors	1 DTUL932 Buffer
		3 DTUL 945 Flip-Flop
		1 DTUL 946 Gate
		2 SE160 Monostable
	3 Timing Capacitors on PC Board	

volt supply for the uhf receiver is not provided. Since the Apollo UDL power supply is a pulse width modulated design, direct application of this design to the I/C UDL was originally proposed. Implementation of this design would require a package larger than the remainder of the I/C UDL and would enlarge the size of the entire unit.

The power supply used for the LEM Transponder was a modified version of the Apollo UDL supply using a 10-kc chopping frequency (7-kc on Apollo) and a single transformer in the modulator. Other parts changes resulted in a design which would meet reliability requirements comparable to Apollo with a physically smaller package. This design has been used for the I/C UDL. A new power transformer and regulator-filter circuitry was developed to meet the requirements for the I/C UDL.

The d-c output requirements are shown in Table III-4. Nominal power delivered is 4.00 watts with 4.56 watts peak power used during relay set-reset operation (30-millisecond pulses). Parts selections are required in the following circuits to optimize performance:

1. Astable multivibrator - square wave symmetry
2. Astable multivibrator - 10-kc output frequency
3. Differential Amplifier - set nominal output voltage
4. Low Voltage Detector - indicate +6 vdc failure when output is below 5.6 vdc.

TABLE III-4. Power Output, Voltage Regulator

Voltage	Current	Wattage
+28 vdc	47 ma and 67 ma	1.32 and 1.88
+6 vdc	45 ma	.27
+4 vdc	550 na	2.20
-6 vdc	35 na	.21
Total		4.00 and 4.56 watts

3.3.1 Breadboard Tests

A complete voltage regulator breadboard was required to design the power transformer (select the turns ratios) and the filter networks. Output requirements were regulation, line and load, ±5% maximum over temperature, and ripple of 1.0% rms maximum. The completed breadboard was tested over a temperature range of -20°C to 85°C for regulation versus line (20 vdc to 30 vdc), regulation versus load (50% load to 150% load, audio susceptability with 1.2v rms superimposed on the input voltage, and the ripple on each d-c output monitored. The trigger level of the low voltage detector was checked and the filter time constants for each d-c voltage were evaluated to assure that extraneous outputs could be avoided. Test results for the breadboard were similar to test results on the unit discussed in subsection 5.1.3.

3.3.2 Voltage Regulator Implementation

The voltage regulator is fabricated entirely from discrete components. Two printed circuit boards are used in a back-to-back mounting configuration. The PC board assembly is mounted in a completely enclosed nickel-plated chassis with only one connector. All outputs pass through feed through RFI filters to minimize radiated interference. Table III-5 summarizes the voltage regulator modules.

3.4 INTERFACE

The interface unit receives inputs from the I/C decoder and provides buffered outputs for RTC (relay) selection, guidance computer data, and central timing equipment update signals. Both the computer and CTE interfaces are performed with cordwood modules identical to those used in the Apollo UDL. Two computer driver modules and five isolated pulse switch modules are required for these functions.

3.4.1 Relay Selection

Relay operation is performed by use of a 4 x 16 selection matrix. This matrix is used to set and reset 32 dual coil

TABLE III-5. Voltage Regulator Modules

Function	Size
Input Filter	1 x 1 x 0.63 in.
Astable Multivibrator	Standard Cordwood Module
Monostable Multivibrator	Standard Cordwood Module
Differential Amplifier	Standard Cordwood Module
Low Voltage Detector	Standard Cordwood Module
Power Driver	Standard Cordwood Module
Power Amplifier	1 x 2 x 0.73 in.
Transformer-Rectifier	1.8 x 1.8 x 0.73 in.
Trimming Resistors	4 1/8w, 1%
Isolation Resistors	8 1.4w, 5%
Filter Capacitors	5 Miscellaneous

magnetic latching relays. Sixteen relay selection lines are used, each of which is connected to two sides of two relays. Two set and two reset drivers are provided to complete the selection by providing a signal source to operate the selected relay coil.

The Apollo UDL uses 8 cordwood modules to perform the selection function, each module containing two selection circuits. The relay selection function has been implemented in one I/C module containing 8 dual 4-input 932 buffers and 8 dual - 2N956 transistors. The implementation for one relay coil is shown in Figure 3-5. The selection output is required to sink up to 22 ma when the output is turned on (saturated). When the output is off, an open circuit voltage of +28 volts is present. The 932 buffer can sink a load of 35 ma, but is limited to 8 volts open circuit. The 2N956 is connected in a common base mode which provides isolation

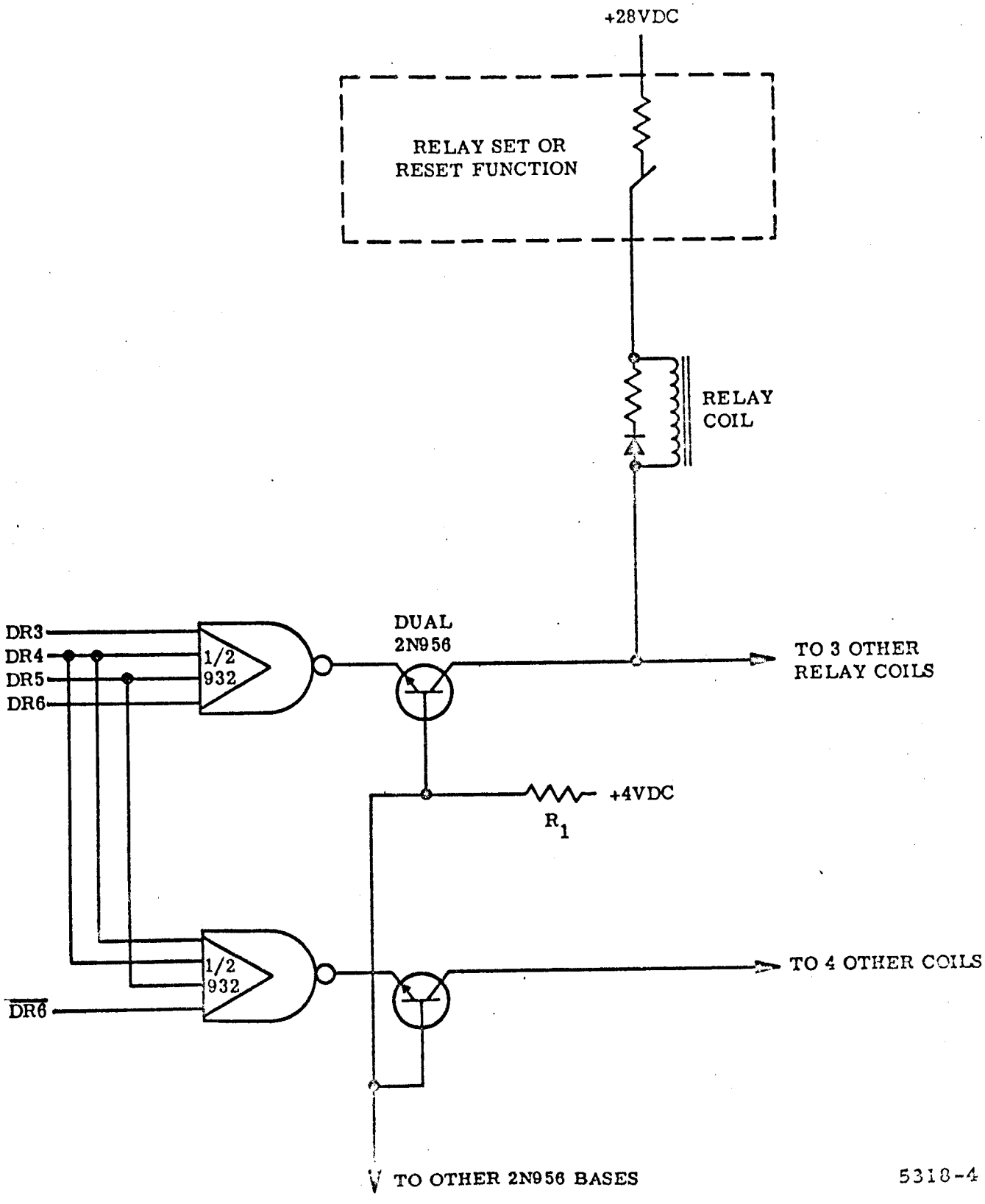

Figure 3-5. Relay Selection

in the open circuit condition. One base resistor is used for base drive to all the 2N956's. Since one output is always turned on, the remaining fifteen 2N956 transistors are back-biased and cannot turn on. The resistor selection assures a saturated output for a "worst case" load.

3.4.2 Interface Implementation

The interface unit consists of seven cordwood modules and one I/C module packaged in the sandwich configuration with all seven cordwood modules on one motherboard. Considerable room for expansion exists in the interface unit which could accommodate up to ten cordwood modules and 2 I/C modules.

SECTION IV

4. MECHANICAL DESIGN

4.1 PHYSICAL DESCRIPTION

The Integrated Circuit Up Data Link package consists of a base, electronic subassemblies, and a cover as shown in Figure 1-1. The base is made up of a subassembly mounting shell and a heat transferring flat plate.

The package is designed to be hermetically sealed by welding the cover and the flat plate to the subassembly mounting shell. If access to the interior is required, material is available for the package to be resealed twice.

The Engineering Model Up Data Link will be fastened with screws instead of welding to allow customer access to the electronic subassemblies.

Physical dimensions for the package were constrained by North American Aviation (NAA) Control Drawing ME-470-0101 for Apollo Block II equipment. Table IV-1 compares the dimensional limits with the actual I/C UDL. A maximum weight of 7 pounds was established by NASA-Motorola at the system design review. The completed engineering model weighed only 5 pounds 6 ounces, a saving of 1 pound 10 ounces over the specified limit and 10 pounds 12 ounces over an Apollo Block I UDL without the uhf receiver.

TABLE IV-1. I/C UDL Dimensions

	Specified Maximum	I/C UDL
Height	6.000 inches	6.000
Width	9.65 inches	4.70
Length	18.3 inches	8.58
Mounting Centers	4.000 inches	4.000
Flatness	.010 inches	.005

The external system connector is as recommended for Block II packaging by North American. The external test connector and the voltage regulator connector are available in a high reliability version. The test connector is also available in a hermetically sealed version.

The electronic subassembly connectors wholly contained within the package are of the same type used on the Apollo Block I Up Data Link.

The electronic subassemblies are designated as follows:

Sub-bit Detector

Decoder

Interface

Voltage Regulator

The detector, decoder, and interface subassemblies consist of two printed circuit boards with encapsulated modules and aluminum attaching spacers as shown in Figure 4-1. The two printed circuit board-module assemblies are bonded together (back to back) to create a panel similar in concept to a honeycomb panel. The encapsulated modules act as the core and the circuit boards as the shear plates. Electrical connection is made to the subassembly through connectors fastened to each of the printed circuit boards. Additional printed circuit board interconnections are provided by folded flat flexible jumpers across the top.

The size of the integrated circuit modules was chosen so as to be compatible with the cordwood modules used on the Gemini, Apollo and Mariner programs. The internal construction of the I/C module is shown in Figure 4-2. Refinements to the module design originally proposed have taken place during the I/C UDL development program. The connector has been replaced by individual solid pins, the molded cover has been eliminated, and the module solidly encapsulated. Future equipment will incorporate smaller diameter pins to aid in interconnect P/C board layout and to change the material thickness ratio between pin and microharness for improved welded joints.

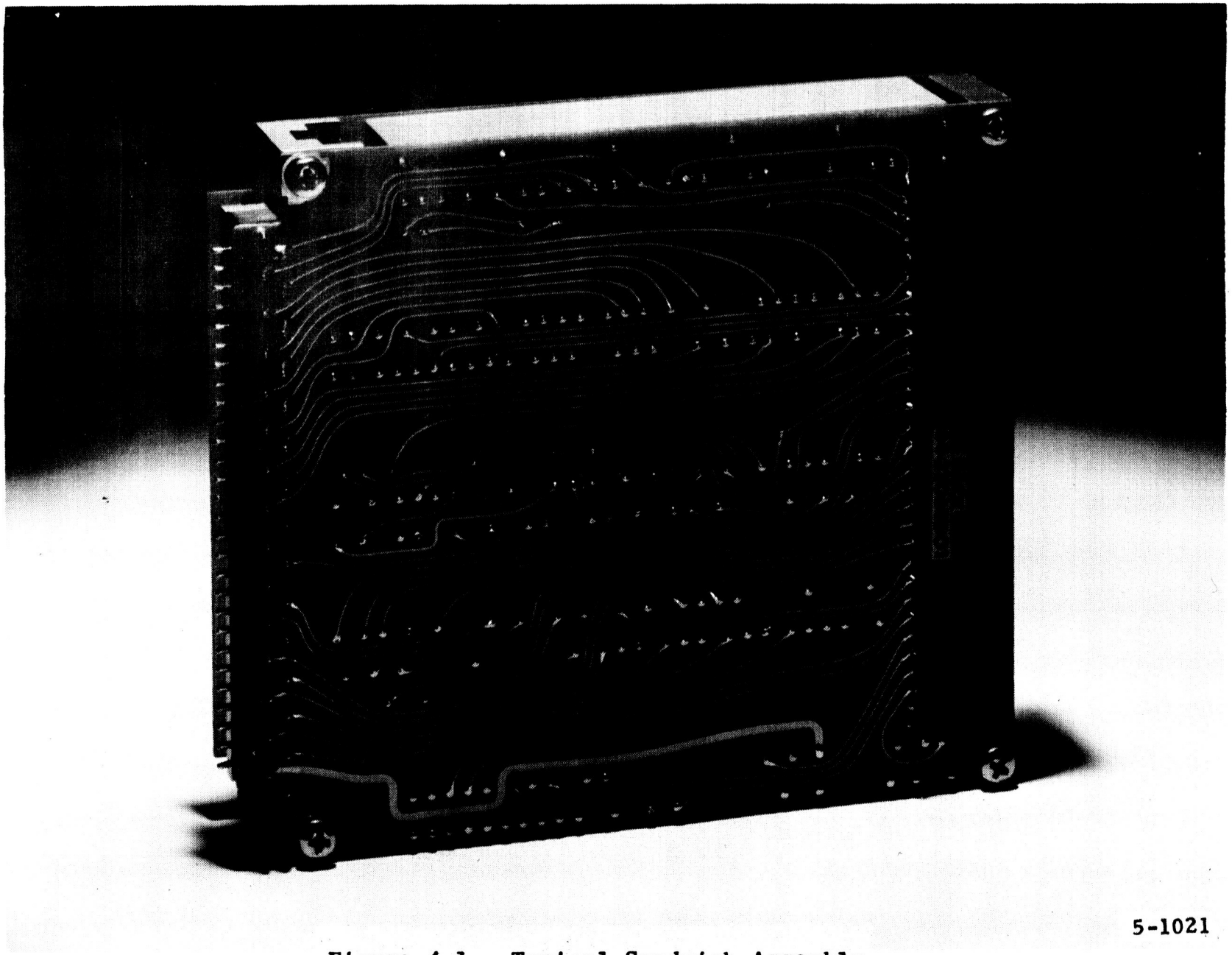

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Figure 4-1. Typical Sandwich Assembly

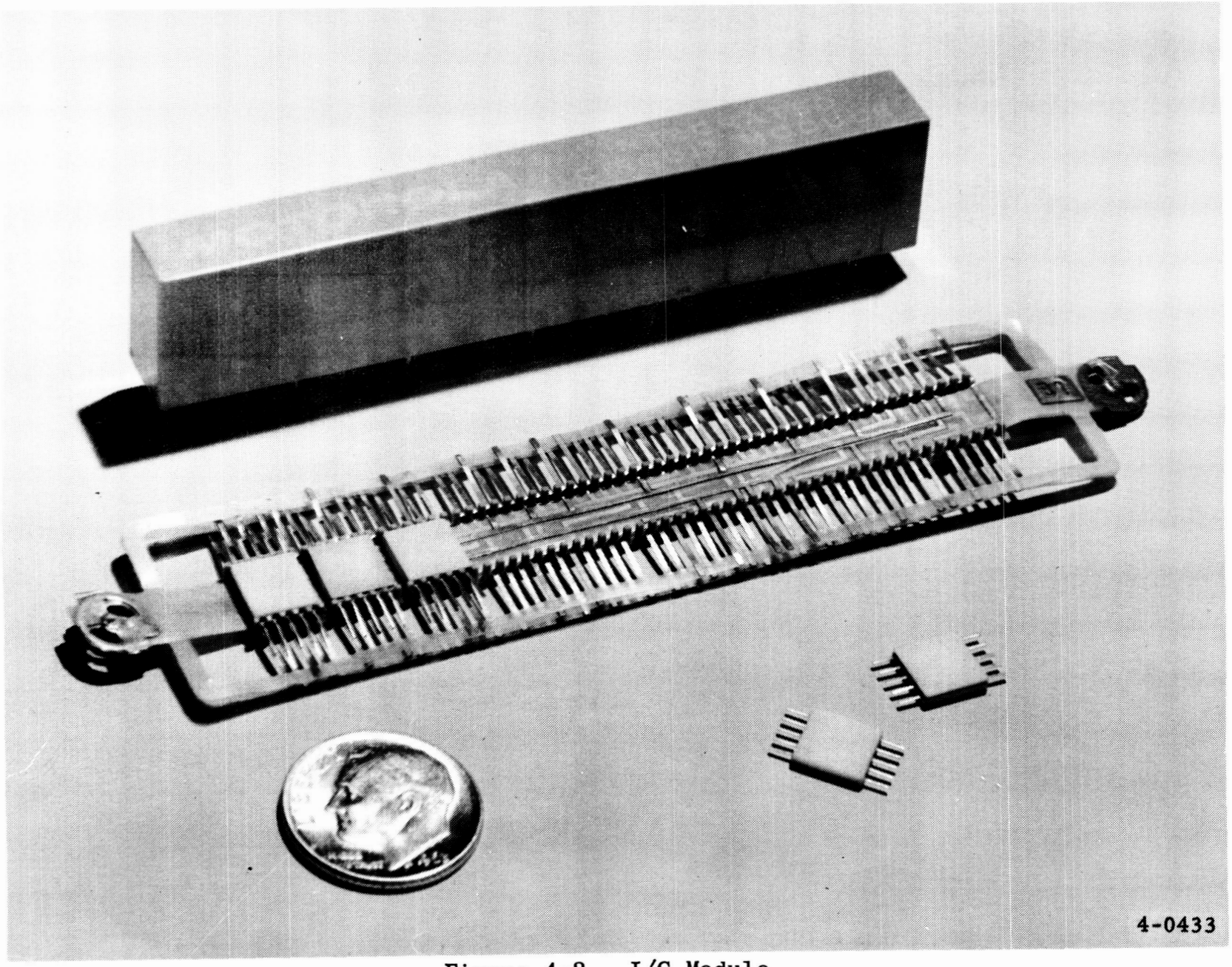


Figure 4-2. I/C Module

A rigorous test was performed to demonstrate the capability of the I/C module to withstand the environmental stresses which will be encountered in aerospace applications. The results of this test were published in Motorola Telecommunications Laboratory Technical Memorandum No. 3030-1-3. A comparable test was conducted with a live 14 FEB I/C module with concurring results. This test was referenced in progress report 3030-1-6. A continuing effort is being exerted to insure that the encapsulating medium used is the best available for the application.

The voltage regulator consists of two subassemblies contained in an aluminum housing. The housing is nickel plated to provide magnetic shielding and corrosion protection for the aluminum. The subassemblies consist of a printed circuit board, encapsulated modules, and an aluminum plate which functions as the sandwich shear plate, and with the housing to provide adequate electrical shielding and heat transfer. The voltage regulator is shown in Figure 4-3. Electrical connection is made to the power supply through a 37-pin connector fastened to the housing. An electrically isolated compartment at the bottom of the regulator mounts rfi filters for both input power and all d-c voltages.

4.2 SUBASSEMBLY REMOVAL AND REPLACEMENT

4.2.1 Subassembly Removal

Each electronic subassembly can be removed independently of the others by performing the following sequential steps.

1. Remove cover.
2. Remove screws from top tie plate.
3. Starting at an edge apply finger pressure to remove top tie plate. As bonding adhesive starts to stretch, cut strands of adhesive. To remove residual adhesive, use ball of adhesive, do not use solvents.
4. Remove two fastening screws from appropriate subassembly.
5. Unplug and lift subassembly directly away from base.

NOTE: ALL DIMENSIONS ARE IN INCHES

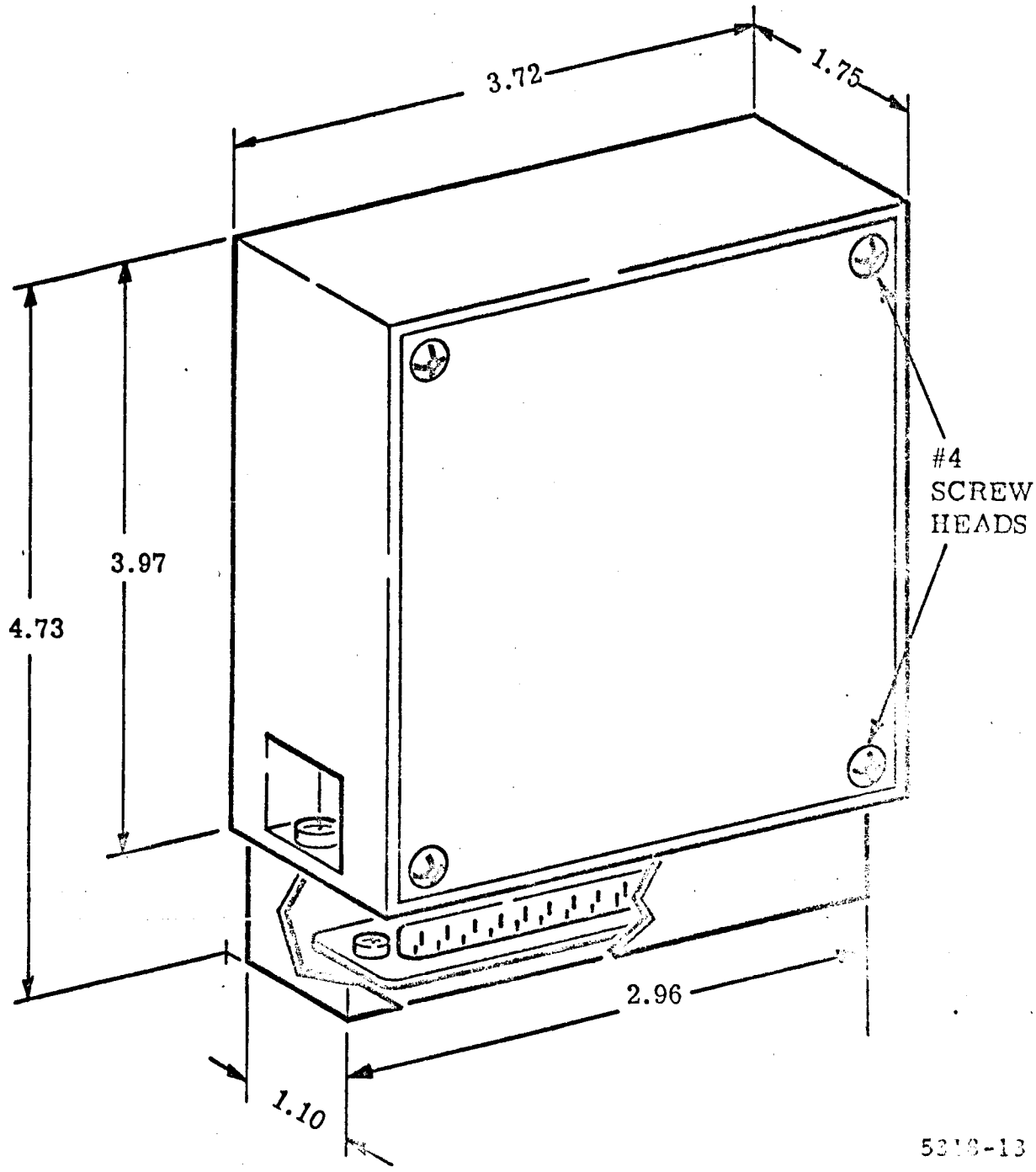


Figure 4-3. Voltage Regulator

4.2.2 Subassembly Reassembly

To reassemble, reverse this procedure. The top tie plate can be reassembled by performing the following steps:

1. Remove all oil and dirt from surfaces to be mated.
2. Cover all contact areas with a thin even coat of GE adhesive, No. 585.
3. Condition adhesive for 30 minutes at 160°F.
4. Assemble mating parts.

NOTE

Adhesion takes place at contact; therefore, considerable care must be exercised in the initial positioning of the mating parts.

5. Install screws.

4.3 ELECTRONIC SUBASSEMBLY DISASSEMBLY

4.3.1 Detector, Decoder, Interface Subassembly Disassembly

For detector, decoder, interface proceed with the following steps.

1. Remove eight attaching spacer screws.
2. Proceed as in paragraph 4.2.1, Item 3, to separate individual printed circuit boards.

4.3.2 Voltage Regulator Disassembly

The voltage regulator can be disassembled as follows:

1. Remove eight attaching spacer screws.
2. Proceed as in paragraph 4.2.1, Item 3, to remove aluminum shield cover.
3. Pivot top (portion opposite connector) out of power supply housing.

4.3.3 Reassembly Procedure

To reassemble, reverse procedure, applying adhesive per paragraph 4.2.2, Items 1 through 5.

To facilitate examination of the unit, the I/C UDL will be supplied without the contact adhesive.

4.4 MODULE REMOVAL

Encapsulated modules can be removed by individually melting each solder joint and removing the molten solder with a vacuum probe.

SECTION V

5. TEST PROGRAM

A comprehensive test program was established for the engineering model I/C UDL to prove electrical compatibility with the Block I Apollo UDL. Environmental tests and analyses were used to show the I/C UDL would be mechanically compatible with Apollo Block II requirements.

First electrical testing was conducted at the component level. Dynamic tests were conducted on 100 per cent of the integrated circuits as a part of incoming inspection. Further electrical tests were conducted at the cordwood module and I/C module levels. These modules were then installed in one of the four major subassemblies and subassembly tests were conducted. Finally, the system was assembled and tested in two modes using the I/C UDL adapter drawer. One set of tests used the interconnecting cabling of the drawer and tested the subassemblies separated from each other. This is called the "sandwich test mode". The second system test operated the four subassemblies through the output connectors as an intact unit. This test mode was used for all qualification tests.

5.1 SUBASSEMBLY AND SYSTEM TESTS

Subassembly tests were conducted to check out the components, interconnections, and detailed design of each subassembly. Tests at this level facilitated location of deficiencies of any type and permitted corrective action more easily than in subsequent system tests. While these tests were conducted primarily for checkout, some measurements were made that would be difficult at a system level. Adjustment and check of regulation of the voltage regulator is an example.

5.1.1 I/C Decoder Tests

The I/C decoder consists entirely of logic circuits divided into 9 I/C modules. The extensive interconnection from module-to-module indicates the difficulty of running comprehensive tests on a single module. Static tests were conducted on each I/C module prior to welding and encapsulation. The ability to make design changes in the completed decoder with all the modules potted is very limited; hence a fabrication and checkout sequence was initiated which tested some complex modules before welding and potting with other modules which had been tested, completed, and installed on the motherboards. This quasi-system test approach facilitated two necessary design changes in the "Output Gating" I/C Module. A short wire jumper on the motherboard was required to complete one change.

Since the I/C decoder was the last subassembly to be completed, the sub-bit detector and interface subassemblies were used to supply stimuli and output load terminations. Tests of the completed decoder subassembly were limited to full electrical tests and measurement of input power required. Separate temperature tests of the I/C decoder were not conducted because the logic circuits were specified to operate from $-55^{o}C$ to $+125^{o}C$, well in excess of the system temperature requirements. The input power levels were as follows:

+6 vdc	29 ma
+4 vdc	495 ma
+28 vdc	15 ma
-6 vdc	none
Total Power	2.534 watts

5.1.2 Sub-Bit Detector Tests

Each module from the sub-bit detector was tested after encapsulation. The entire detector was then assembled and operated

with a command modulator. Performance of the detector was comparable to the breadboard unit except that the sub-bit output was inverted. This was corrected by reversing the matched filter amplifier outputs into the sub-bit flip-flop, requiring two jumper wires on the motherboard.

The detector subassembly was temperature tested from -25°C to +85°C with no noticeable degradation in performance. The input power levels were measured as follows:

+6 vdc	8.6 ma
+4 vdc	42 ma
+28 vdc	31.5 ma
-6 vdc	33 ma
Total Power	1.332 watts

5.1.3 Voltage Regulator Tests

The voltage regulator design requires selection of several resistor values to optimize the output frequency, symmetry of the chopping signals, output voltage, efficiency, and low voltage detector trigger level. The resistor selection for output symmetry and frequency are located in the astable multivibrator module, all others are on power supply motherboard one.

The voltage regulator was assembled on the two motherboards with all modules encapsulated except the astable multivibrator. Resistor selection for symmetry of 69.8 K and a fine frequency adjust (R8) of 220 ohms were made for this module. The ASMV was then encapsulated and installed. Final resistor selections were made for the remaining functions using the dummy loads shown in Table V-1. Subsequent measurements of the remaining subassemblies show that both the +4 vdc and +28 vdc outputs were loaded heavier than the dummy load. As a result all outputs were within ±1.5% of nominal. The low voltage detector selection, which depends on the +6 vdc supply was made so that the detector output was marginal at 5.6 vdc and always indicated failure at 5.5 vdc.

TABLE V-1. Power Supply Dummy Loads

Nominal Output	Load Current	Actual Output	Deviation
+ 6 vdc	50 ma	6.1 vdc	+ 1.6%
+ 4 vdc	500 ma	4.2 vdc	+ 5%
+28 vdc	35.0 ma	28.6 vdc	+ 2.2%
- 6 vdc	33 ma	6.0 vdc	--
Output Power With Dummy Load = 3.58 Watts			

The completed voltage regulator was temperature tested from $-25^{o}C$ to $+85^{o}C$. Table V-2 shows the effect of temperature and input voltage on the power supply input power and efficiency. The efficiency for a constant load varies from 58 per cent at high temperature, high voltage to 64 per cent at low temperature, low voltage. These values agree with breadboard results and are comparable to the Block I Apollo design.

TABLE V-2. Input Power with Dummy Load

Input Voltage (v)	$T = -25^{o}C$		$T = 25^{o}C$		$T = 85^{o}C$	
	Input Current (ma)	Input Power (w)	Input Current (ma)	Input Power (w)	Input Current (ma)	Input Power (w)
20	282	5.65	297	5.95	305	6.10
25	223	5.60	236	5.90	240	6.00
28	206	5.75	211	5.90	217	6.05
30	195	5.85	199	5.95	207	6.20

All power supply outputs were monitored for change in output voltage (regulation) and output ripple with input supply voltage and temperature using the nominal d-c outputs shown in Table V-1 as the reference. The maximum change over the input range of 22 vdc to 30 vdc and $-25^{o}C$ to $+85^{o}C$ was -2%, +2.5% with the maximum occurring at high temperature, high supply voltage and the minimum occurring at low supply voltage.

The ripple voltage on the d-c outputs was specified at 1 per cent rms maximum. Filter designs on all voltages except the +4v supply provided much lower ripple; the +4v is used only on logic circuits which can tolerate larger ripple voltages. Ripple outputs are a direct function of input supply voltage. Table V-3 shows the ripple measurements with a dummy load and a 28-v input supply.

TABLE V-3. D-C Voltage Ripple Measurements

Output Voltage	T = -25°C		T = 25°C		T = 85°C	
	Output Ripple	% of Output	Output Ripple	%	Output Ripple	%
+6 vdc	18.6 MV rms	0.31	15 MV rms	0.25	14 MV rms	0.23
+4 vdc	39	0.97	35	0.87	30	0.75
+28 vdc	21.5	0.08	18	0.07	18	0.07
-6 vdc	7	0.12	7	0.12	8	0.13

Voltage regulator audio susceptibility was measured with 1.2 volts rms coupled into the +28 vdc line. Maximum sensitivity occurred with a 350-cycle audio tone. The sharpest peak occurs on the 28-vdc output at 125 millivolts rms, or 0.45% ripple. The +4 vdc output was essentially unchanged with an audio input from 30 cps to 10 kc.

Other voltage regulator tests included a check of output frequency versus temperature, minimum voltage at which the regulator would operate (15 vdc), and a review of all test points for anomalies. Two differential amplifier test points provided to check the voltage adjustment were sensitive to the chopping output and produced an undesirable but nondestructive oscillation. These test points were eliminated, so that voltage adjustment can only be checked by direct probing on the motherboard.

Other test points provide internal monitoring points where the I/C UDL is tested in the sandwich mode.

5.1.4 Interface Unit Tests

The Interface Subassembly was tested by operating the circuits from the respective decoder outputs. Since all circuits were previously tested in module form, checkout consisted of an operational test to assure both motherboards and connectors were wired correctly.

5.1.5 System Tests

The system test program was designed to prove that the I/C UDL was ready for subsequent qualification and acceptance tests. The primary test sequence was to follow the acceptance test procedure and record all test results. These tests are directly related to the Apollo Block I UDL and are intended to prove comparable performance.

System checkout of the I/C UDL with the bench maintenance equipment (BME) revealed two logical differences which give no-go's in BME testing but do not affect the desired output to the using system. The first difference is in the CTE reset output. The equipment requirement is at least one reset output for CTE up date with each CTE transmission. The Apollo UDL supplies 24 full pulses and one half pulse. The I/C UDL supplies 24 full pulses but, due to a timing difference, does not supply the half pulse. The BME counts pulses and treats the half pulse as a 25th pulse. A simple change in the checking circuitry accommodates this variation.

The second change is in the agc data outputs. The I/C UDL has an additional one millisecond delay before starting agc outputs. The number of pulses, pulse width, and pulse amplitudes are the same as the Apollo UDL. Since this variation does not affect the user, a one millisecond delay was inserted in the BME to give valid data sample times on the I/C UDL.

5.1.5.1 System Power Requirements

The I/C UDL input power was measured at limit input voltages against a specified limit of 15 watts. The typical dissipation of a Block I UDL without receiver is 7.84 watts. Table V-4 summarizes the power used in the Detector, Decoder, and Interface Subassemblies. Table V-5 shows the power levels at each input voltage.

TABLE V-4. Subassembly Power Requirements

	+6 VDC	+4 VDC	+28 VDC	-6 VDC	Total
Detector	8.6 ma	42 ma	31.5 ma	33 ma	
Decoder	29	486	15	--	
Interface	13	14	0.1	3.4	
Total Current	50.6 ma	541 ma	46.6 ma	37.4 ma	
Total Power	303.6 mw	2164 mw	1305 mw	224.4 mw	3997 mw

TABLE V-5. System Power Requirements

Input Voltage	Current	Power	Efficiency
24 vdc	285 ma	6.84 w	58.5%
28 vdc	240 ma	6.72 w	59.5%
30 vdc	225 ma	6.75 w	59.2%

5.1.5.2 Message Error Rate

The message error rate for the Apollo UDL is measured using the UHF receiver. Since the I/C UDL does not include a receiver, the signal-to-noise ratio at the UHF or S-band input terminals must be defined to permit error rate testing. The input level at the Apollo receiver for acceptance test is -99 dbm. Data taken from receiver #1 at a -99 db input gives a signal level of 0.6v

rms and a noise level of 0.05v rms. These levels have been established for the I/C UDL as representative limits.

The indicated threshold for S/N testing can be derived as follows:

S = SIGNAL = $\sqrt{S_N^2 - N_Q^2}$ where

SN = SIGNAL + NOISE

N_Q = NOISE

From the receiver specification with S removed,

N_Q must be 6 db below S_N and

$$S/N = 20 \log_{10} \frac{S_N^2 - N_Q^2}{N_Q} \geq 10 \text{ db}$$

hence $S \geq 3.16\ N_Q$ or for

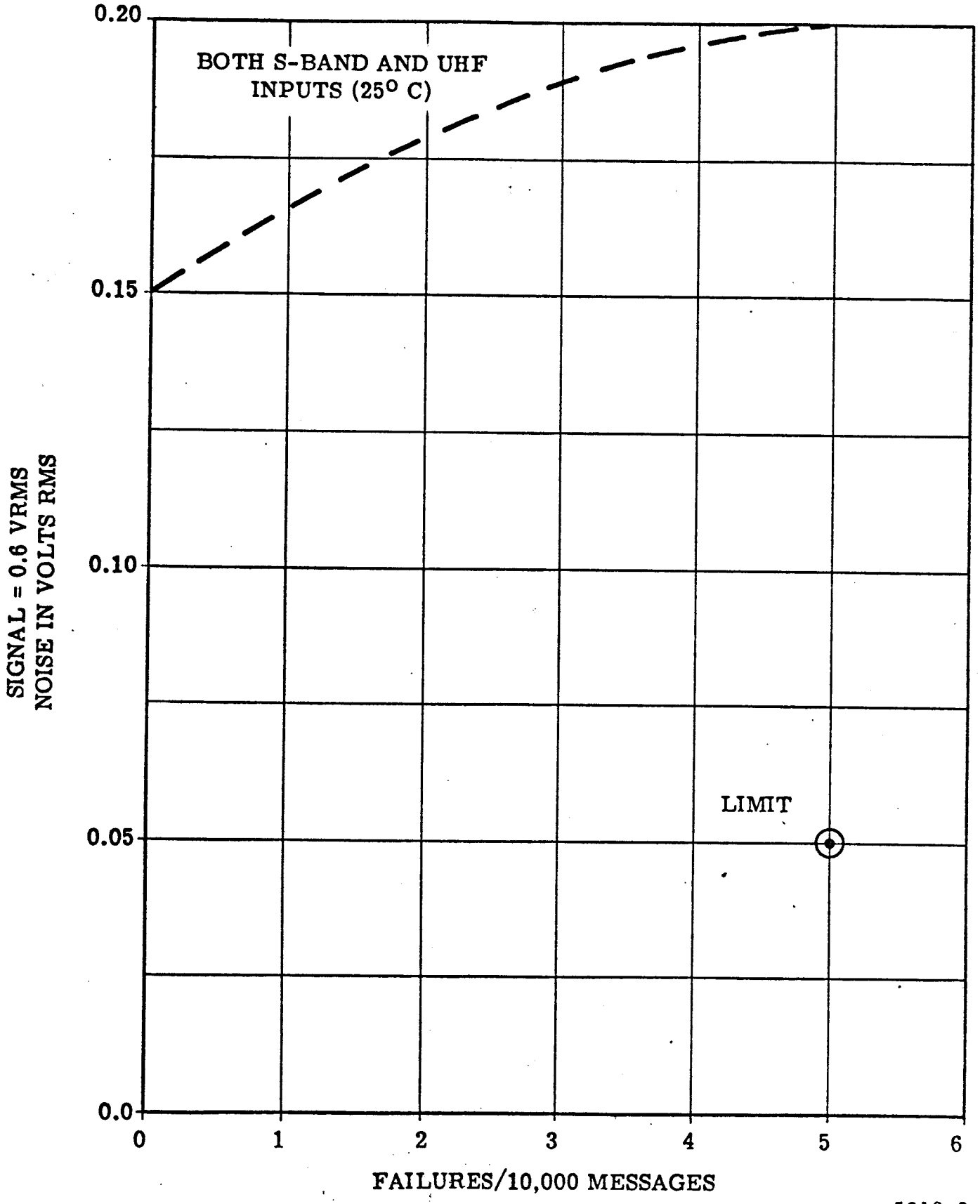
S = 0.6v rms

N_Q = 0.19v rms maximum

Error rate tests using various signal-to-noise ratios are shown in Figure 5-1, which provides a 12 db margin in the I/C UDL. This level is comparable to Apollo UDL's.

5.1.5.3 Grounding and Isolation Measurements

The ATP requires a check of grounding and isolation from ground on all pins of the access connector and the output connector which are used for interface circuits. The test instrument is a digital voltmeter which uses 36 volts as a test voltage. Due to the likelihood of damaging intergrated circuits which have an 8- to 10-volt breakdown this test was run with a vom with a 3-volt battery. It is recommended that this test be changed, because inadvertent measurement to a wrong pin could degrade or permanently damage an operating circuit.



5318-8

Figure 5-1. Message Error Rate, I/C UDL

5.2 QUALIFICATION TESTS

The qualification tests for the I/C UDL were a series of environmental tests made with the unit electrically operating. The environmental requirements for high and low temperature were taken from North American Apollo UDL Specification MC-470-0014 Rev. B for Block II equipment. To allow customer access to the unit, the package has not been welded shut and the connectors have not been encapsulated. Therefore, the vibration test has been limited to a 2 g resonant search over the frequency 20 cps to 2000 cps. Other tests such as salt spray, shock, and humidity could not be evaluated due to the lack of sealing; although related equipments have previously passed these requirements. A 10-foot extension cable was used to couple the I/C UDL to the BME for all environmental tests.

5.2.1 High Temperature Test

The qualification test procedure requires a temperature test run of 8 hours with a cold plate temperature of 48°C and an ambient of 66°C. Electrical tests could not be started until two hours after the unit stabilized at high temperature. Figure 5-2 shows the Test Specimen mounted in the Tenney temperature chamber for this test. Figure 5-3 shows the temperature cycle for this test. The unit was turned on and operating throughout the test program so realistic temperature rises in the equipment could be measured.

5.2.1.1 Thermal Analysis

The temperature rise shown in Figure 5-3 is worse than that to be expected in system performance. The cover was not used on the unit so that thermocouple mounting could be simplified. Since the unit was not welded, the thermal paths to the cold plate were dependent on the screws and the mounting feet. The base of the unit would be milled flat after welding to meet the 5/1000 flatness requirement. This provides uniform contact over the entire unit base.

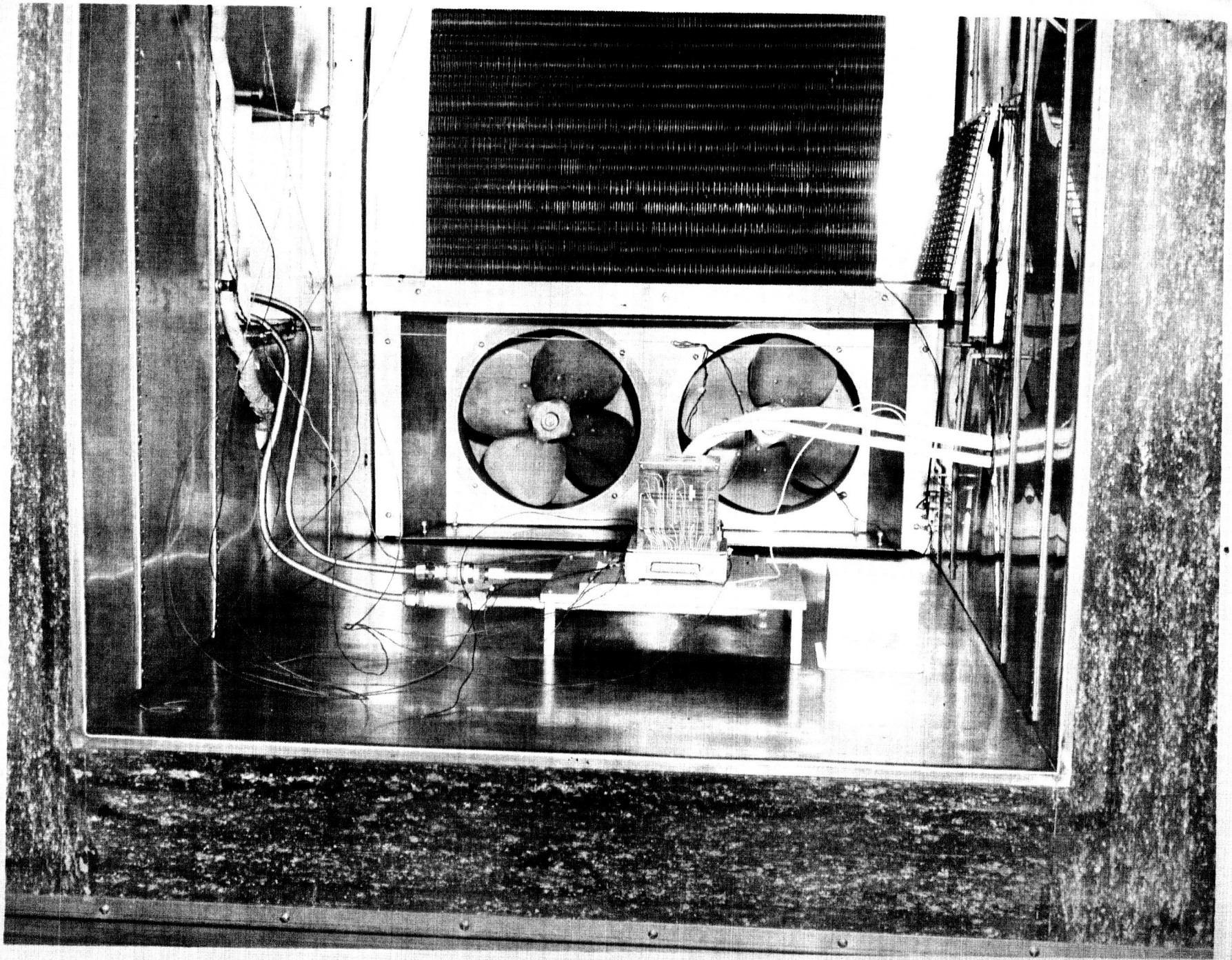


Figure 5-2. Test Specimen in Tenney Temperature Chamber

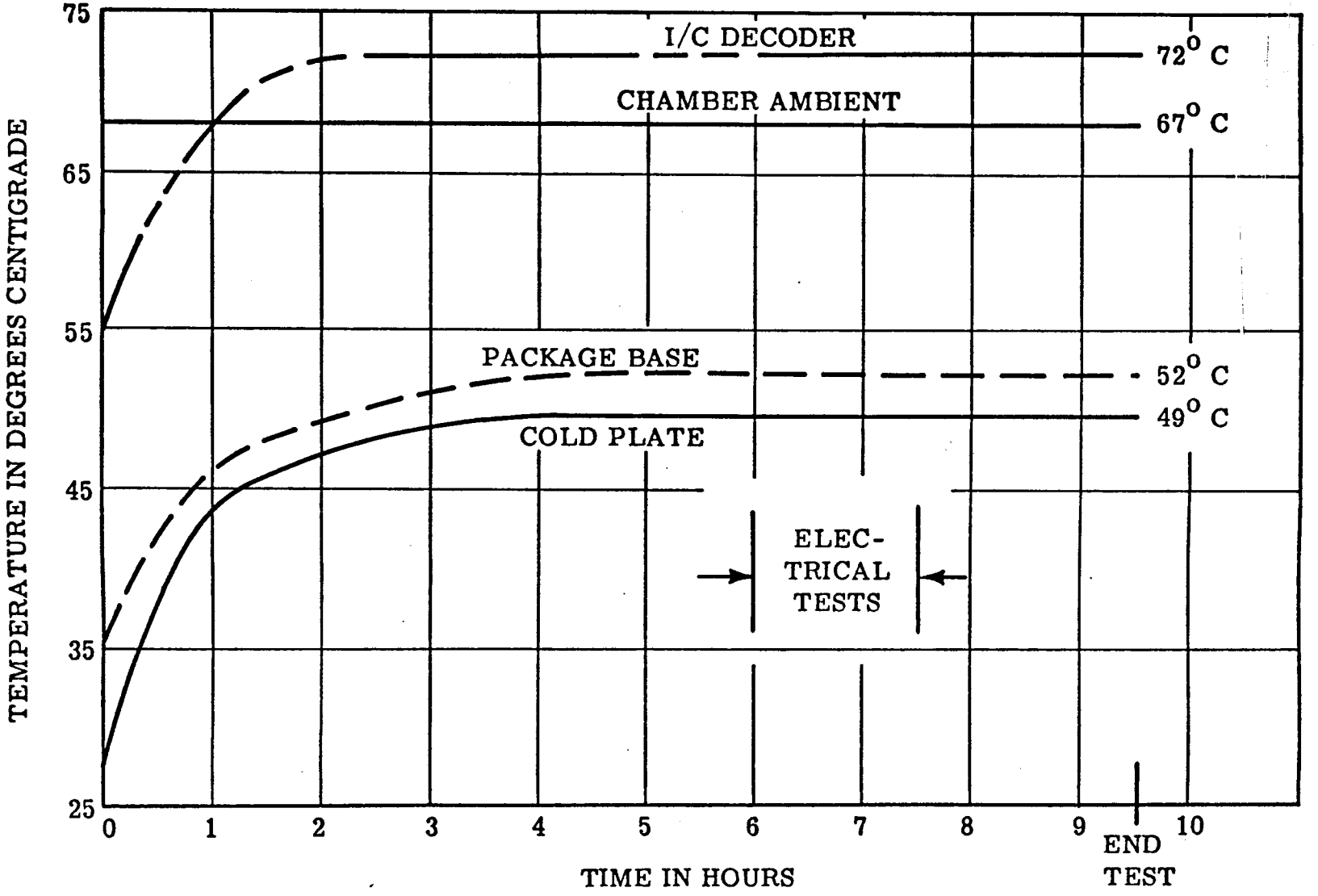


Figure 5-3. Qualification Test, High Temperature

The I/C decoder dissipates the highest power and has the highest temperature rise of any subassembly. The decoder rise of 20°C over the package base is well within design expectancy. Actual rise in a completely sealed unit would be approximately 10°C.

5.2.1.2 Electrical Tests

The electrical tests on the I/C UDL were the same as those called out in the acceptance test procedure for both operational and comprehensive tests. The input power requirements increased approximately 225 milliwatts at all input voltage ranges as expected from paragraph 5.1.3, voltage regulator temperature tests. All electrical tests were passed satisfactorily and the unit was returned to room temperature.

5.2.2 Low Temperature Test

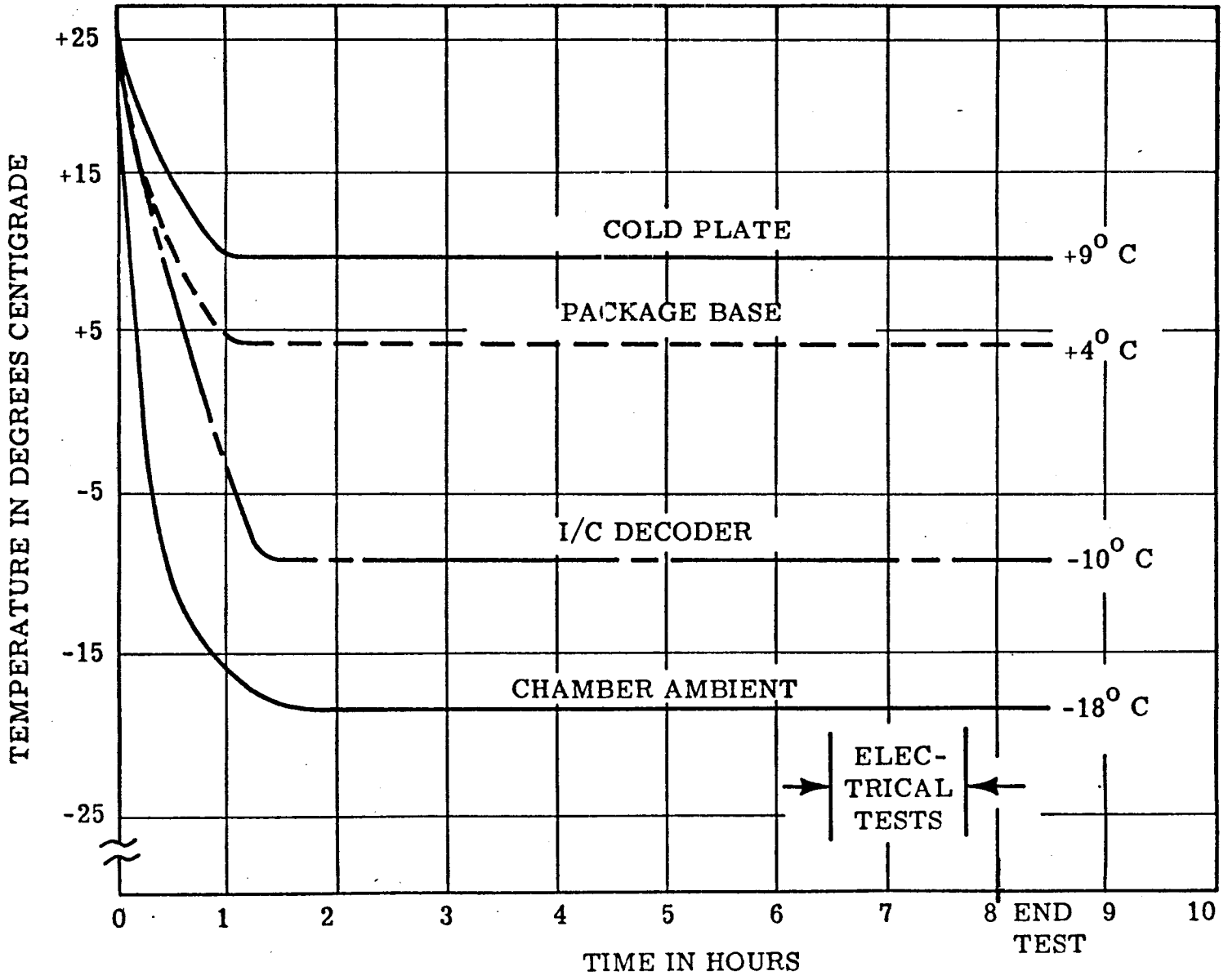
The low temperature test requires a run of 8 hours with a cold plate temperature of 13°C and an ambient of -18°C. The test specimen mounting and test program are the same as the high temperature test. Figure 5-4 shows the temperature cycle for this test.

5.2.2.1 Thermal Analysis

The absence of the cover and welded thermal paths resulted in much lower equipment temperatures than would normally be expected for this test. The I/C decoder shows a 19°C change from cold plate temperature. The expected difference in a completely sealed unit is approximately 5°C.

5.2.2.2 Electrical Tests

A failure occurred in the I/C decoder at low temperature which gave erroneous output for agc, CTE, and test messages. The unit operated normally in all other modes so the test sequence was completed. The power requirements decreased approximately 225 milliwatts (3.3%) at all input voltage ranges. Error rate tests, vehicle and system address, and all real time command messages were passed satisfactorily.



5318-10

Figure 5-4. Qualification Test, Low Temperature

5.2.3 Failure Analysis and Re-Test

The circuit which worked satisfactorily at room termperature but failed at low temperature was traced to a 945 flip-flop located in DR7 of Register 1 I/C module which had an internal race problem. Special extension cables were required to temperature test the decoder alone and in the process of temperature cycling to locate the failure, a 946 Quad Two Gate used in telemetry interface was damaged. The potting in the area of each specific FEB was dissolved, new integrated circuits were installed and the modules were re-encapsulated. Temperature testing to verify correct system operation resulted in an additional integrated circuit failure of a 946 quad gate in the program control counter. This failure occurred because of a bad wire bond inside the integrated circuit. A discussion of quality assurance steps to avoid I/C failures may be found in subsection 6.2.

The completely repaired I/C decoder was retested over the temperature range of $-35^{o}C$ to $+90^{o}C$. Complete BME test tapes were run with the decoder at $-35^{o}C$ and $+80^{o}C$ and the remainder of the system at $25^{o}C$. All operations were satisfactory.

5.2.4 Requalification Testing

The I/C UDL was requalified using a Delta 6545A Temperature Chamber and no cold plate. These tests were intentionally more severe than the original qualification requirements to show design margin. An ambient temperature profile is shown in Figure 5-5. The electrical tests were all passed satisfactorily after stabilization at $-20^{o}C$ and $+80^{o}C$.

5.2.5 Vibration Test

The vibration tests were designed to determine, through low level search sweep, the basic resonances of the I/C UDL package. Unfortunately, some of the final package characteristics are dependent upon the package being sealed. The results of these tests therefore may not track in total those of a similar package completely sealed.

The tests were conducted using a Ling 275 shake table controlled by a Ling R-1003 Sinusoid Console. Resonance of the mounting

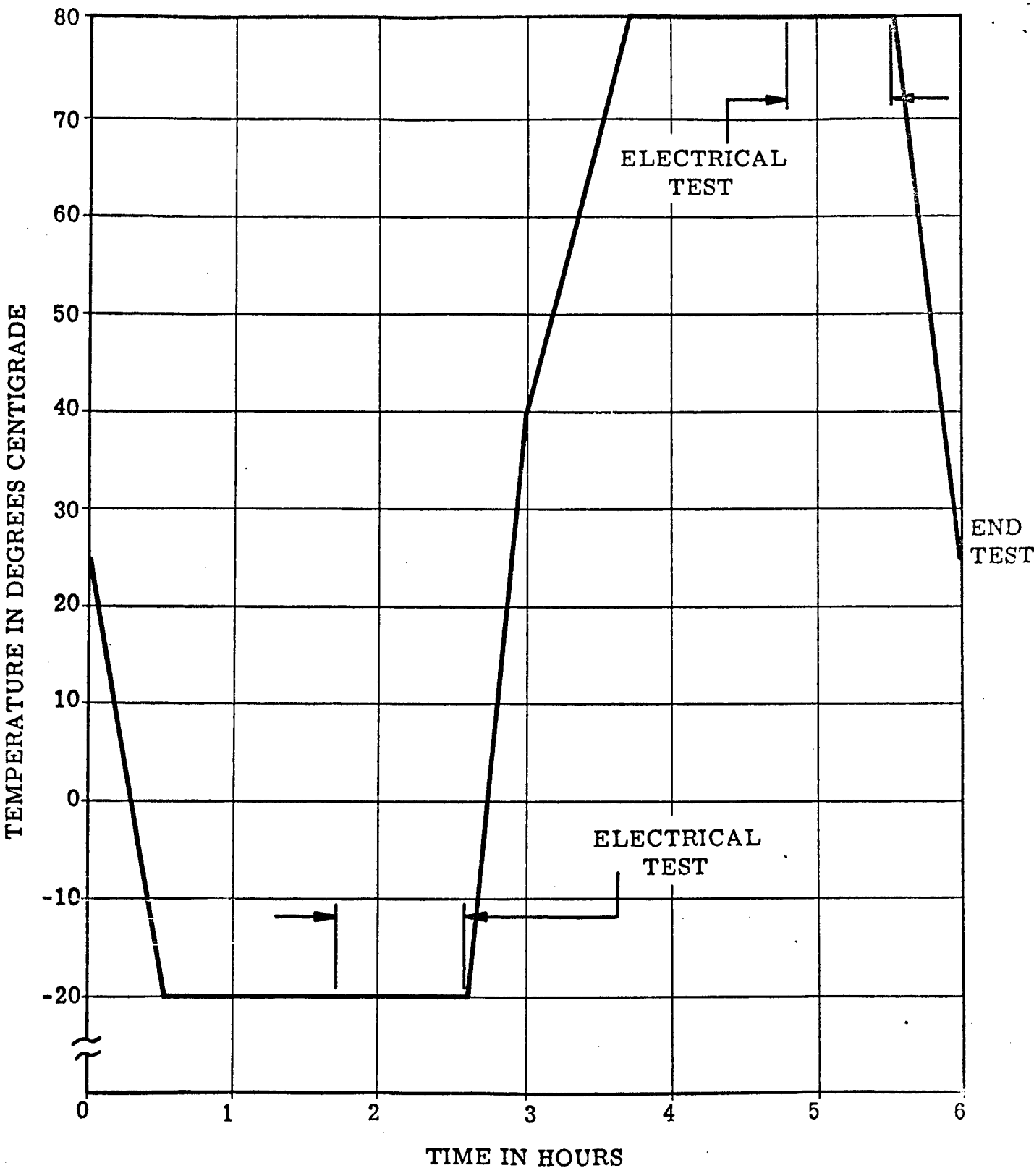


Figure 5-5. Requalification Temperature Test 5318-12

fixture was determined to be outside the frequency range encompassed by the test. Data was recorded using a CEC 11 channel recording oscillograph.

The unit under test was subjected to a 2 g resonance search from 20 cps to 2000 cps at a sweep rate of 2 octaves per minute.

5.2.5.1 Vibration Analysis

Figures 5-6 through 5-8 are plots of the transmissibility versus frequency for the three shake planes, A, B, and C. In each of the first two tests, planes A and B, inordinately high transmissibilities were encountered at resonance. Because of the low input g level, visual observations with a strobe light proved inconclusive.

In order to verify the mode of excursion suspected, a 545 Tektronic dual trace scope was employed along with accelerometers No. 1 and 8 in shake plane B. An "in phase" display throughout the frequency range indicated the excursion mode pictured in Figure 5-9 was correct.

Since the requirement was one of determining resonance of this particular package and not one of obtaining any particular result, no further tests were scheduled. As a matter of speculation, it is felt that with the cover in place and an elastomer energy absorber positioned between the subassemblies and the cover, transmissibilities can be reduced to a satisfactory limit. Figure 5-10 illustrates the proposed damper.

5.2.5.2 Electrical Tests

The operational tests from the acceptance test procedure were conducted while the unit was vibrated in each plane. All system outputs were verified and no failures occurred.

5.3 ACCEPTANCE TESTS

The acceptance test procedure was patterned after Motorola Document 12-28402D, ATP for the Apollo UDL using the special test equipment. The actual acceptance test was conducted at NASA/MSC

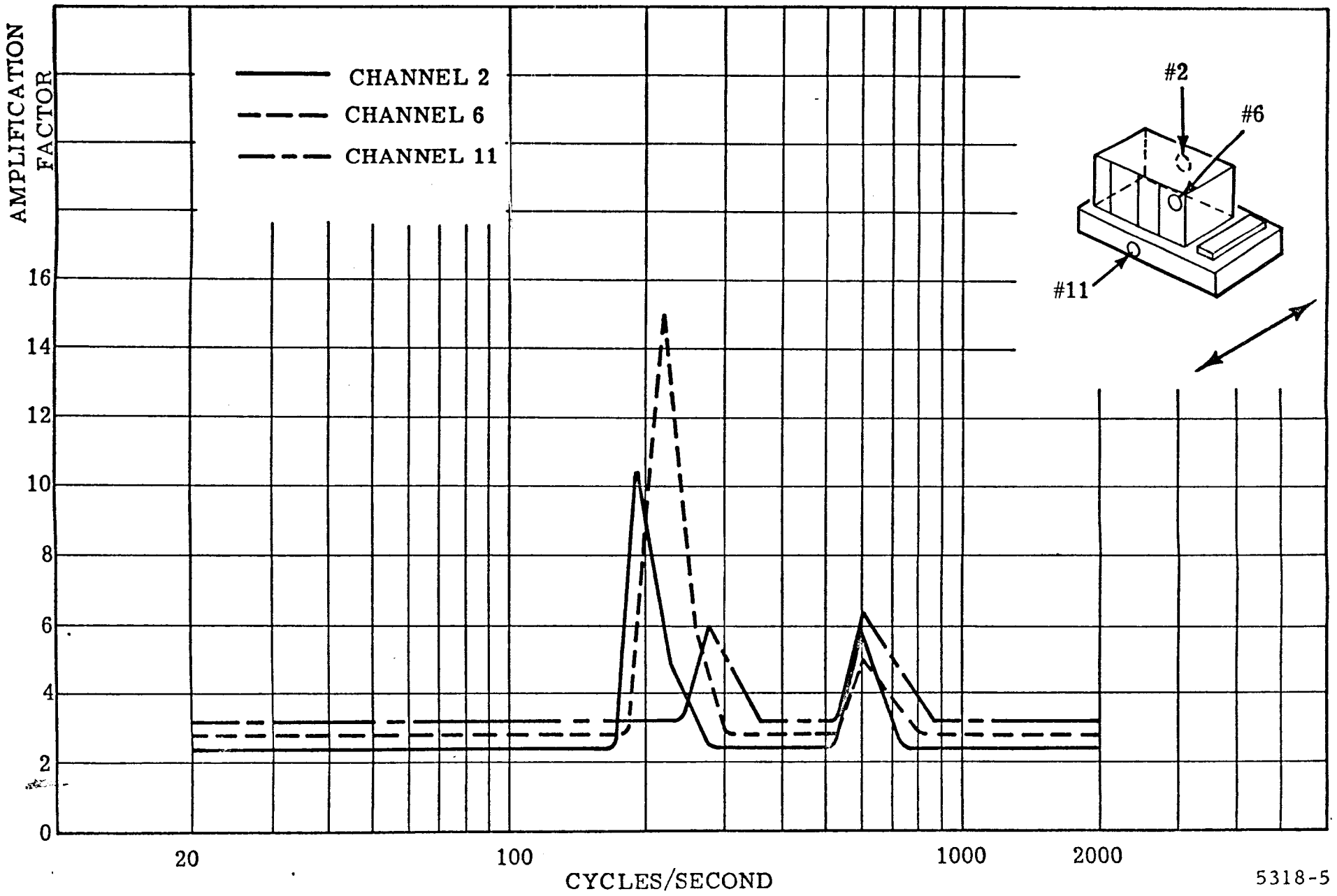


Figure 5-6. Shake Plane A

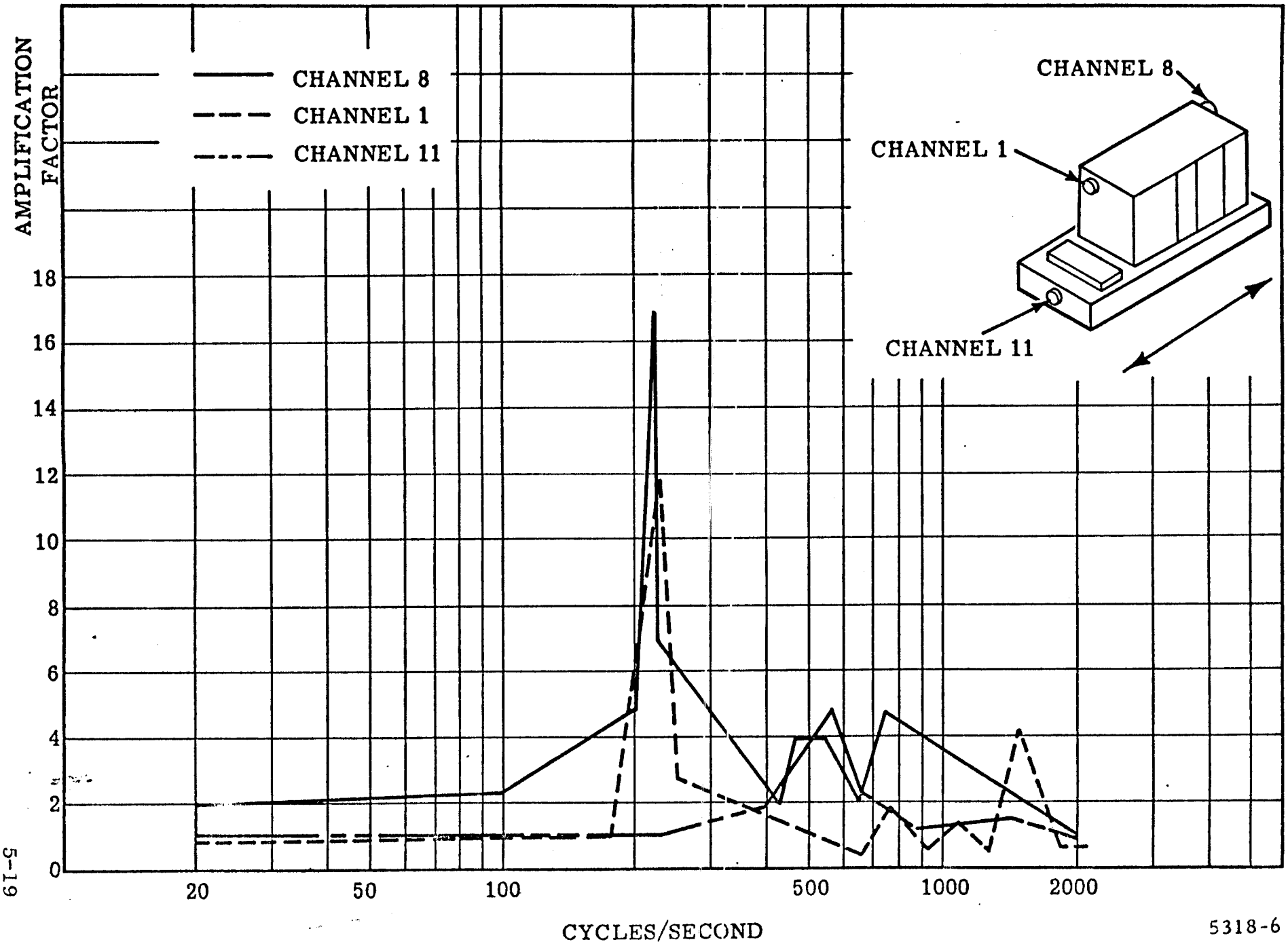


Figure 5-7. Shake Plane B

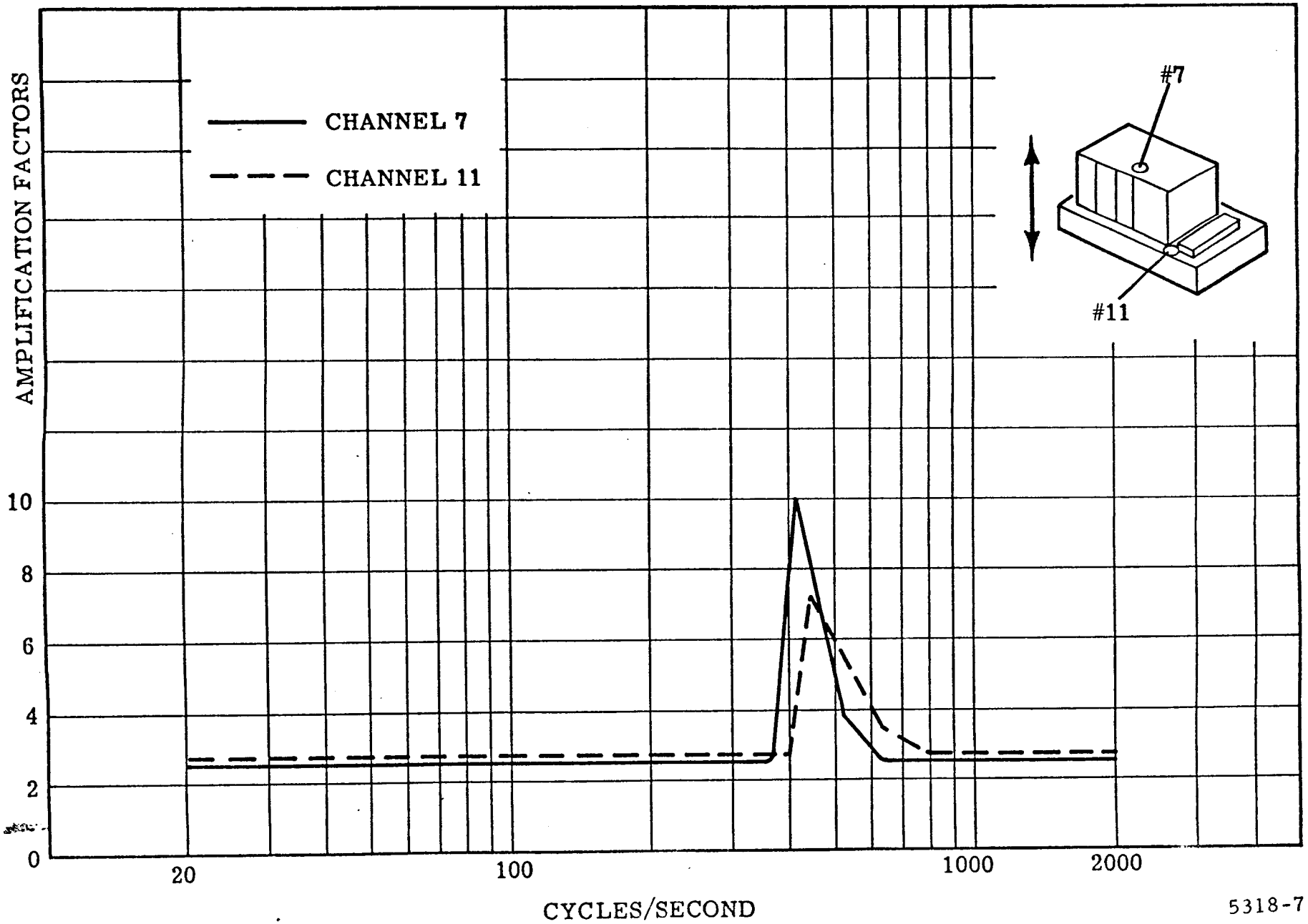


Figure 5-8. Shake Plane C

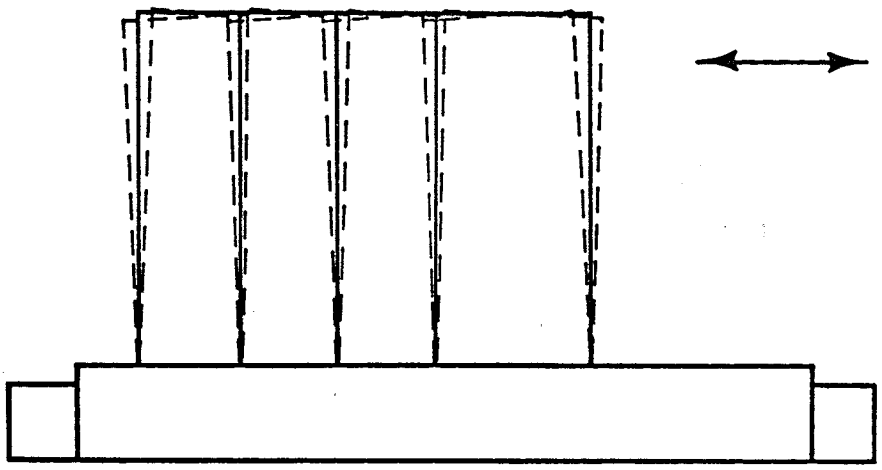


Figure 5-9. "B" Plane Excursion (Exaggerated)

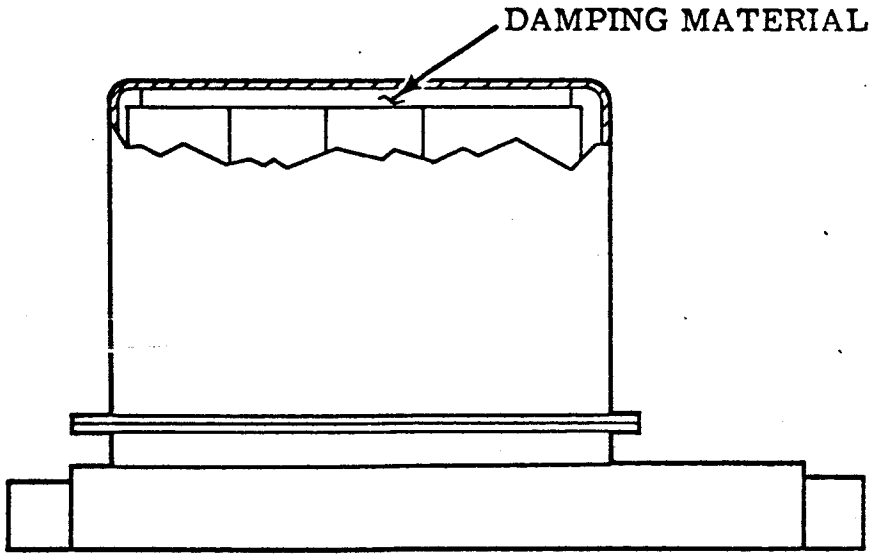


Figure 5-10. Positioning of Damping Material 5318-11

using the CSTS - Bench Test Set with I/C UDL Adaptor Drawer. The BTS was modified to accept both the 24 and 25 CTE reset pulses and the one millisecond delay in agc outputs as discussed previously. The complete operational and comprehensive operational test programs were conducted in both the "sandwich test mode" and the system test mode. The I/C UDL passed all tests.

SECTION VI

6. RELIABILITY STUDIES

To back up the design of an integrated circuit UDL, studies were instituted to determine if integrated circuit application would provide the reliability improvements which have been anticipated by both semiconductor manufacturers and many equipment manufacturers. These studies have been separated into the categories of reliability prediction, procurement of integrated circuits, and fabrication of a system containing integrated circuits. The reliability prediction will be based on the I/C UDL using best known failure rates on I/C. The procurement section will pertain to I/C which could be successfully used for a flight-worthy I/C UDL. The fabrication studies will discuss process steps and controls to assure that flat pack integrated circuits packaged in microharness modules will result in the best possible system reliability.

6.1 RELIABILITY PREDICTION

Determination of the failure rate of a given set of integrated circuits produced by a given manufacturer requires a test program of hundreds of millions of device hours. The logic family selected for the I/C UDL, namely the 930 series DTL, is a relatively new family and does not currently have this history. Integrated circuit manufacturers have attempted to lump all circuits built with planar epitaxial processes in order to accumulate data faster. This concept should give results within an order of magnitude, but it does not delineate between packaging processes such as TO-5 and various flat packages nor does it account for internal bonding such as gold-aluminum or all aluminum systems. Specific reliability assurance for the 930 series family must be developed through controls inserted in the procurement document and through additional life test data.

Appendix II, TM 3030-1-1 Reliability Comparison of the Apollo UDL and the I/C UDL shows the effect of integrated circuits using

an industry wide average failure rate for the integrated circuits. This report, generated early in the I/C UDL program, shows a 2:1 reliability improvement for I/C used in the digital portion only. Minor changes in the sub-bit detector and interface units should show additional improvement.

Up-dated reliability information on the 930 series family indicates the pre-screened units should have a lower failure rate than that cited in the report (0.002%/1000 hours). The implementation of the I/C decoder provides minimum component stress by using low fanout, low frequencies, and an encapsulated, ruggedized package technique.

A second reliability advantage for integrated circuits is that the significant size reduction makes redundancy on a subsystem level much more practical than with discrete components. For the I/C UDL, redundancy of the sub-bit detector and the majority of the I/C decoder could be accommodated with a minimum of selection circuitry. A triply redundant unit with voting circuits feeding the interface modules could also be used. The fully redundant I/C UDL was estimated to have a mission reliability of 0.999966 for 336.5 hours.

6.2 PROCUREMENT OF HIGH RELIABILITY INTEGRATED CIRCUITS

The factors involved in procurement of integrated circuits can best be defined by development of a procurement document which limits vendor selection, specifies inspection levels and criteria, defines an initial qualification and periodic requalification, and provides test limits which meets all program requirements. These factors are discussed independently in the following paragraphs.

6.2.1 Parts Selection

The selection of a set of digital integrated circuits to be used in high reliability spacecraft equipment must initially be based on circuits which best meet the system design requirements.

Where a choice of circuit families exists, the circuits should be readily available from several sources. The individual part history, as ascertained from manufacturer's test data and from other programs which are using the parts, should be reviewed for possible design deficiencies and latent failures. The part design, both electrically and structurally, must be basically sound if reliable circuits are to be the result.

6.2.2 Vendor Selection

Several steps can be taken to assure the selection of the vendor with the most reliable product. The vendor's history with previous high reliability programs should be examined in detail. A plant survey is needed to verify that the vendor has the capability for processes and process controls necessary to continue producing high reliability circuits. The survey should also show whether these controls are applicable and are being applied to the selected circuit family. The vendor must be willing to discuss any weak areas in both design and processing and to provide corrective action to eliminate these shortcomings.

6.2.3 Qualification

A survey should be made to determine whether a prospective vendor can be initially qualified on the basis of having been qualified by other NASA and/or military organizations on the same or similar parts.

Only if the reliability requirements of the mission justify the expense should a qualification program be initiated on each specific device type.

6.2.4 Lot Qualification

The definition of a lot is extremely important. Both the number of units and elapsed time period must be controlled for adequate lot definition. Lot size and determination of the sample size (LTPD) should be a balance between the system reliability requirements and the cost of the system. The LTPD should be decided

by carefully weighing the parts cost against the cost of replacing devices during the manufacturing operation.

A significant change in the process would also automatically start a new lot. For example, a lot of integrated circuits could be defined as a family of related devices manufactured with the same process and equipment, over a period of two weeks, with a maximum lot size of 1000 units. Manufacturers have been reluctant to accept this double definition on the basis that it exposes yield data; however, product control necessitates the limit.

6.2.5 Traceability, Failure Reporting, and Corrective Action

Traceability of a device is used to relate device and lot failures to specific fabrication steps. Traceability back to wafer diffusion is sufficient to provide the data, because failures induced prior to diffusion are either random or affect yield which can be evaluated directly.

A failure reporting and corrective action system is required to protect device quality. The vendor should be requested to report lot failures within two days by telephone and follow up with a written report within a week from that date. Device failures should be carefully analyzed to determine whether a systematic weakness exists in the processing. Corrective action can be taken, subject to forming new lots if the change is major.

6.2.6 Visual Inspection

The simplest visual inspection is an x-ray taken after package sealing and any mechanical tests. X-ray photographs contribute very little to the reliability of most I/C because neither silicon nor aluminum shows up on x-ray. For those circuits which use gold wires, the x-ray will show up lead paths.

The best visual inspection is one conducted, just before final sealing, with high power microscopes. Representatives of the buyer's QA department could perform this inspection; however, it is probable that this approach is unacceptable to the vendor.

Buyer inspections have been used where an entire assembly line has been set aside as has been the case in some Minuteman programs. A mutually acceptable workmanship standard can be prepared and enforced by the vendor's QC department.

The visual inspection criteria are qualitative and therefore difficult to define. Examples of good and marginal parts can be demonstrated with sketches. As a minimum, the criteria should include scratch marks in interconnect patterns, wedge bond appearance, bond positioning, chips or particles, and lead placement.

6.2.7 Mechanical Tests

After the production final electrical tests are performed, all I/C's should be subjected to a series of mechanical tests. Suggested tests include:

Temperature Cycling	-55° to 125°C
Centrifuge	20,000 g's minimum
Hermetic Seal Test	10^{-8} cc/sec
Burn-in	100 hours minimum

Additional tests or tighter requirements on these tests can be provided if the reliability requirements justify the expense.

6.2.8 Electrical Tests

The electrical tests for each device type depend on the specific application. It is suggested that all other criteria be developed for the entire family of circuits, but that separate data sheets calling out only the significant parameters be used for electrical test limits. Delta criteria have become common for high reliability transistors to show the stability of a device before and after burn-in. The primary problem in this type data is correlation of test equipment. Delta parameter tests are not presently recommended for integrated circuits because the secondary effects involved in circuit test limits have not been fully evaluated.

6.2.9 Procurement Document

The preparation of the final procurement document should be approved in advance by prospective vendors so that parts can be purchased. Documents containing most of the criteria above have been submitted to Fairchild, Motorola Semiconductor, and Philco for their comments. Primary objections have occurred in lot definition, visual inspection criteria, and written reports on lot failures. These areas can be negotiated on future contracts.

6.2.10 Effect on I/C UDL

Two parts failures occurred on the I/C UDL, one a low temperature failure and the second a faulty bond. The unit which failed at low temperature was from the first run of the new 945 type flip-flop. A subsequent design change should have eliminated this failure from future lots.

The bond failure is normally revealed by temperature cycling followed by centrifuge. Three steps can be taken to prevent this type failure on high reliability equipment. The first is the 100% visual inspection which detects marginal bonds. A second is a higher level centrifuge which places more stress on the light aluminum wires. Finally, a 100-200 hour 125°C burn-in will provide bond stressing. Had this circuit been subjected to these tests, it would most probably have been discovered prior to installation in finished equipment.

6.3 FABRICATION OF HIGH RELIABILITY I/C EQUIPMENT

The fabrication of high reliability equipment using discrete components in cordwood modules has been developed as part of the Mariner, Gemini, and Apollo programs. The selection of the Microharness integrated circuit module as a packaging medium for flat pack integrated circuits utilizes the cordwood module background in installation of modules on the motherboard. Subsequent subassembly packaging and tests are independent of whether the modules are I/C or discrete.

The assembly process for standard high-rel welded cordwood modules as used on the Apollo UDL is listed so that differences between a cordwood module and an I/C module can be emphasized.

6.3.1 Cordwood Module

1. Parts are inspected by Incoming Inspection
2. Parts are kitted. Part number and Serial number are recorded for traceability
3. Module is assembled by qualified operator
4. Module is inspected prior to welding for proper placement of parts, etc by QA
5. Module is welded by NASA certified welder
6. Module is given a pre-encapsulation electrical test
7. Module is inspected for weld defects by QA
8. Module is encapsulated, identified, and serialized
9. Module is given final electrical test
10. Module is inspected by QA.

6.3.2 Micro-harness Module

The differences in assembly processes are as follows:

1a. Micro-harness is fabricated by printed circuit facility
1b. Micro-harness is inspected by QA
3a. Module is electrically tested prior to welding

The microharness module is approximately the same size as a cordwood module. Handling techniques, weld inspections, and other process steps can be accomplished by the same operator.

6.3.3 Process Control Documents

The integrated circuit modules for the I/C UDL were fabricated without formal documentation such as assembly drawings, Workmanship Inspection Standards, Manufacturing Process Specifications,

and a complete flow diagram. The various process steps were closely evaluated on this program so that these control documents could be readily prepared for future UDL's.

6.3.4 Tooling

The primary tooling limitation for the I/C UDL integrated circuit modules was the holding of FEBs and microharness during FEB to microharness welding. This tooling has been developed and will be available for subsequent programs.

The pins used in the I/C modules were made of 0.030 diameter tin-plated nickel wire which when welded to 0.002 Kovar interconnect gave a thickness ratio of 15:1. A true weld nugget is formed when the ratio is no greater than 4:1. The pin size has been reduced to 0.015 and flattened to 0.008 for all future I/C modules.

No other fabrication areas have been identified which limit the reliability of integrated circuit equipment using flat pack integrated circuits.

SECTION VII

7. CONCLUSIONS AND RECOMMENDATIONS

Integrated circuits have been applied to approximately 65% of the electronic hardware from the Apollo UDL including all digital circuits. Some further miniaturization has been achieved in the voltage regulator and the sub-bit detector. A comparison of the Apollo UDL and the I/C UDL is shown in Table VII-1.

TABLE VII-1. UDL Comparisons

Parameter	Apollo UDL W/O Rcvr	I/C UDL
Electrical Performance	Specified	Identical
Size	560 cu in.	214 cu in.
Weight	16.2 pounds	5.6 pounds
Power	7.8 watts	6.8 watts

While the stress on the I/C UDL has been in reduction of size and weight, the unit was constrained to form factors dictated by Apollo Block II specifications. It is estimated that the equivalent electronic functions could have been packaged in 150 cubic inches and less than 5 pounds without these constraints.

7.1 PACKAGING

The equipment design permitted an evaluation of Apollo Block II specifications. The constraint of 4-inch mounting centers represents a hardship for small equipments, because the useful area inside the package is so limited. This constraint affects discrete component equipment even more than integrated circuit equipment. The requirement for welding shut the package also constrains a small package because weld seams consume volume which could be used for equipment. Neither of these constraints existed on Block I equipment.

The integrated circuit interconnect used for this program proved satisfactory for miniaturizing equipment using flat-pack integrated

circuits. The module pin size has been reduced because the large (0.030 diameter) pin resulted in some inconsistency in the micro-harness-to-pin weld, and made interconnection of several I/C modules on a two-sided printed circuit board difficult. Fabrication and encapsulation processes are now comparable to discrete component equipment.

7.2 INTEGRATED CIRCUITS

The application of integrated circuits reflects a potential for higher reliability than discrete component equipment because of a reduction in number of interconnects (joints) per set of circuits by approximately 10 to 1.

Advanced screening techniques have shown that extremely reliable equipment can be fabricated with discrete components by extensive testing of each part prior to installation and by subsequent testing of the completed module. A similar program using integrated circuits should result in equal reliability at significantly lower cost, because the screening techniques would be applied once per circuit rather than on each component.

Two integrated circuit failures were experienced during the I/C UDL program. These failures indicate that screening tests of I/C for high reliability applications are required to reduce the infant mortality rate. It is not believed that these particular failures are indicative of poor long-term reliability of the circuit family. Subsequent testing by NASA/Houston should confirm this.

7.3 RECOMMENDATIONS

To obtain some quantitative measure of the reliability of the equipment, it is recommended that NASA/MSC conduct an operating life test of the delivered equipment. Operating the equipment at elevated temperature (+65^{o}C) will accelerate the failure mechanisms and provide more meaningful data in a shorter period of time.

The use of integrated circuits for the digital equipment has significantly reduced equipment size with no degradation in performance. A similar program in the linear circuitry, and particularly in the voltage regulator, will further reduce size and weight by one-half. The voltage regulator is now 40% of the total electronic equipment.

The integrated circuits selected for the digital functions use approximately two watts. While lower power digital integrated circuits could have been chosen, the 930 series represents a practical power level to achieve the desired noise immunity. Another two watts are used in the linear and interface circuitry. Redesign of the linear circuits using I/C techniques should combine power reduction with size and weight reduction. Since the voltage regulator efficiency should remain about 60%, a one-watt reduction in linear circuit power would provide a 1.67-watt reduction in input power.

APPENDIX 1

TELECOMMUNICATIONS LABORATORY

TECHNICAL MEMORANDUM

No. 3030-1-2

24 November, 1964

SELECTION OF DIGITAL INTEGRATED CIRCUIT FAMILY FOR USE ON THE I/C APPLICATION TO APOLLO UDL

By: R. Herring and F. Jones

ABSTRACT

This report discusses the desired characteristics for a digital circuit family to be used in the Apollo UDL. The available standard I/C families are then compared against the design requirements. The major comparisons are based on reliability, package design, electrical performance, power levels, and package count. The final conclusion is that the 930 Series DTL family, as produced by Fairchild, best meets these requirements.

MOTOROLA INC.

WESTERN MILITARY ELECTRONICS CENTER

INTRODUCTION

The incorporation of digital integrated circuits is a logical starting point in the conversion of a discrete component system to a miniaturized integrated circuit version. In the Apollo UDL, the digital circuitry comprises 65% of the electrical component volume. The approach used in selection of a logic family was to define the logical requirements and compare these with the capabilities of I/C families. Once the basic logical requirements can be satisfied, other criteria such as reliability, size, weight, and power dissipation can be used in the selection of a preferred type.

BASIC LOGIC FAMILY REQUIREMENTS

The logic requirements for the Apollo Decoder were established by a general analysis of the logic, re-designed without the constraints of the original logic implementation. This was accomplished in two parts. First, the fan-in requirements were established by re-designing parts of the logic where the original implementation was constrained by the 25 kc high rel discrete component logic family. A complete tabulation was made of the actual fan-in requirements. Second, the fan-out requirements were established by re-designing the logic so that the loading was obtained on each logic signal. That is, drivers were removed or treated as gates where necessary to accurately determine the real logical loading on signals from gates and flip-flops. The results of this analysis are tabulated in Tables 1, 2, and 3.

From the results of this analysis, any logic family can be evaluated as to logic suitability to the UDL and an estimated number of circuits required for implementation. This allows all logic families to be evaluated without developing a complete logic design for each logic family. For application to a small system such as the UDL, the chosen logic family should closely fit the requirements to avoid size, weight and power penalties. The fan-in, fan-out requirement of the UDL were found to closely agree with those from other spaceborne, airborne and ground equipments which Motorola has produced.

An analysis of the fan-in and fan-out vs function tables shows that the logic requirements dictate a family with the following characteristics:

TABLE 1. DECODER LOGIC CIRCUITS

Quantity	Type
23	Flip-Flop (Shift Register, no parallel entry)
28	Flip-Flop (Shift Register, AC set and/or reset)
7	Flip-Flop (Shift Register, controlled AC set and/or reset)
4	7-Input Gate
1	5-Input Gate
2	4-Input Gate
23	3-Input Gate
28	2-Input Gate
24	1-Input Gate
5	3-Input Driver
7	2-Input Driver
18	1-Input Driver
1	55 Millisecond Monostable
1	30 Microsecond Monostable
1	10 Microsecond Monostable
1	20 K H_Z Astable

TABLE II UDL GATE SIGNALS
LOADING REQUIREMENTS

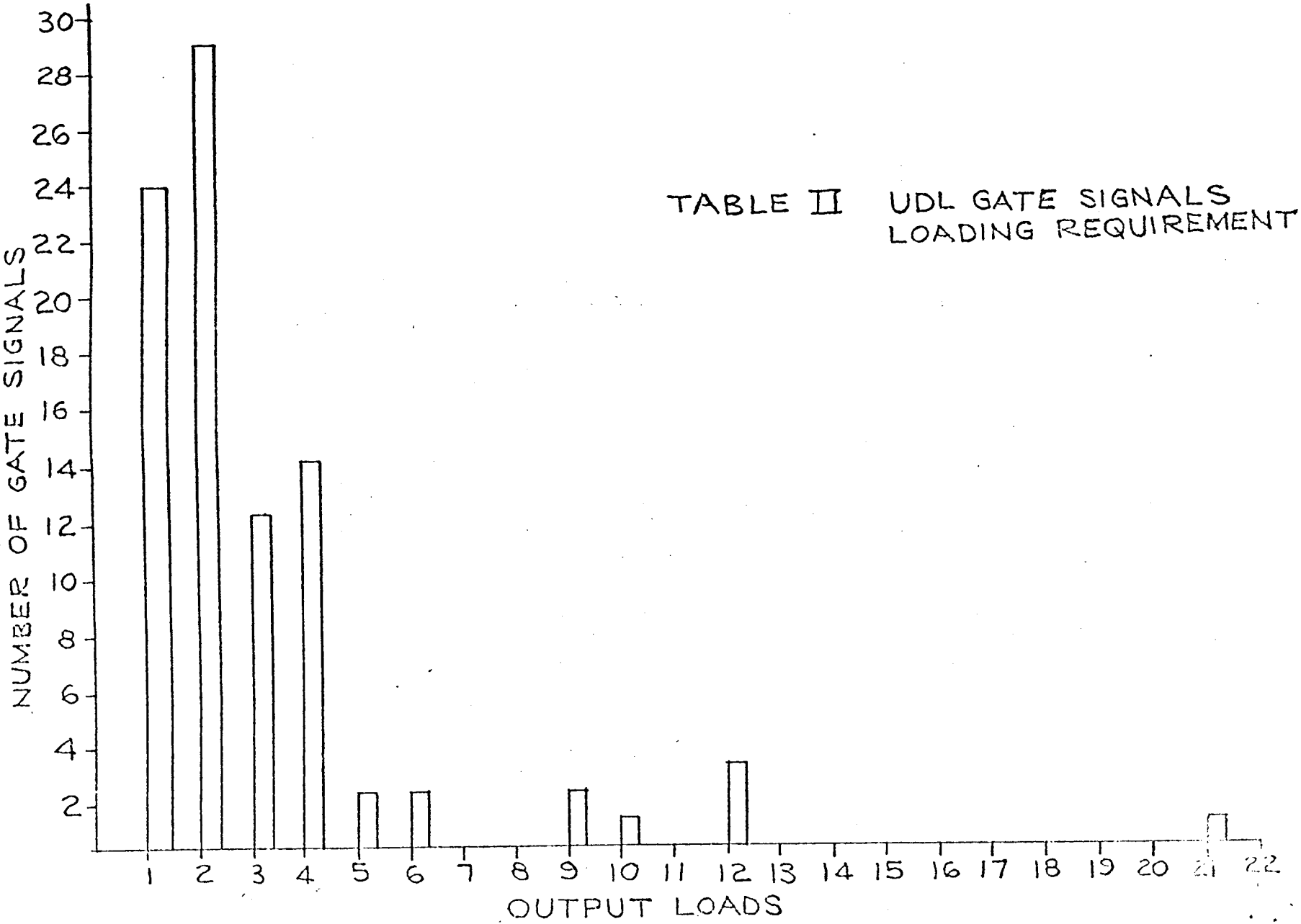
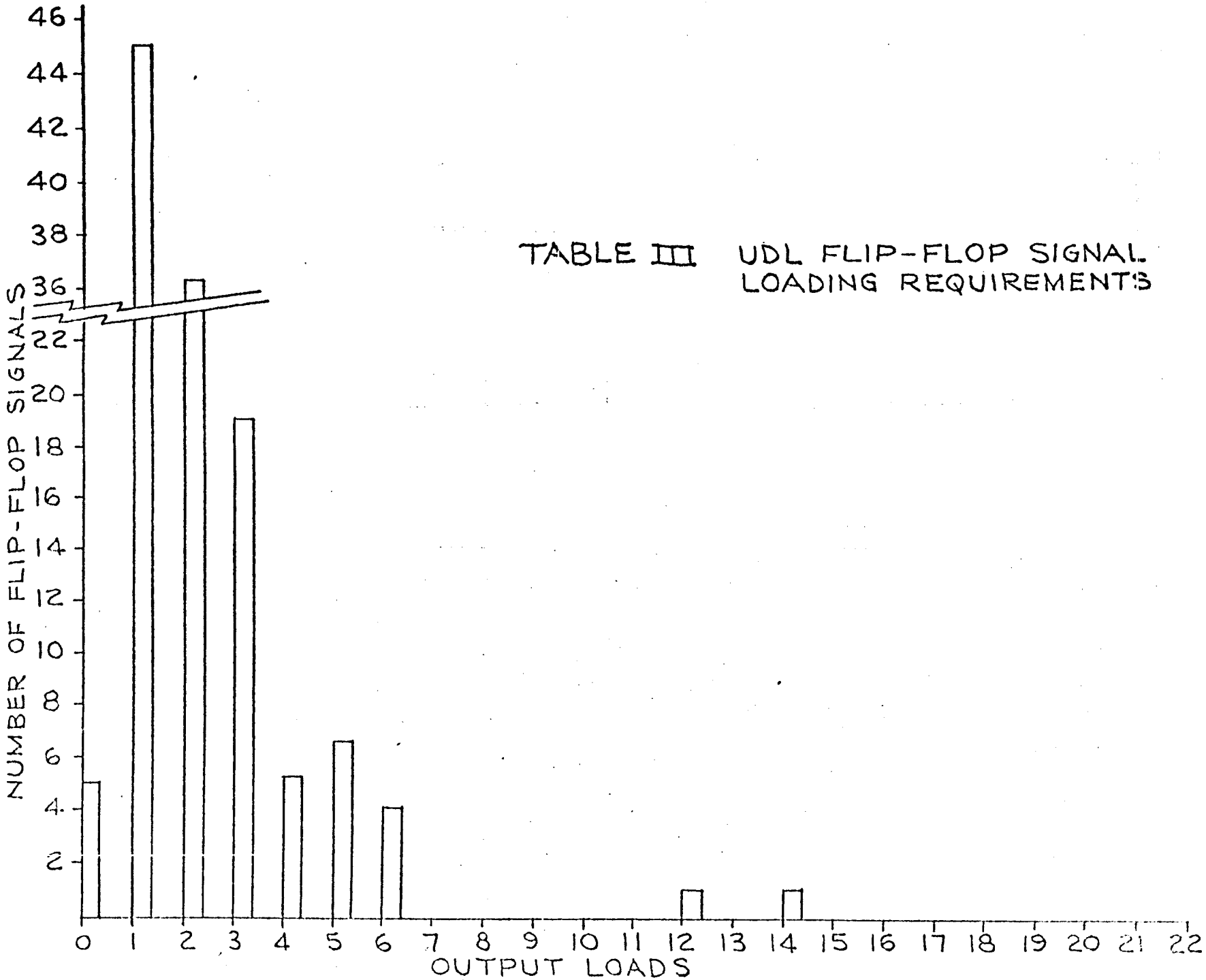


TABLE III UDL FLIP-FLOP SIGNAL LOADING REQUIREMENTS



All circuits 25 K H_Z operation

3 Gate expandable		fan-out 6
2 Gate	Compromise on one of these	fan-out 6
1 Gate		fan-out 6
Gate expander to 7		
3 Input Buffer		fan-out 14
JKT F/F (Register) W/AC Set and Reset		fan-out 6

CHARACTERISTICS OF THE DESIRED I/C FAMILY

The logical requirements developed in the previous section can best be met by development of a custom integrated circuit family which would also consume little power and optimally package the circuits into the smallest volume. Use of a custom family would be costly because the circuit designs and mask sets would have to be developed for each circuit element. Further, the reliability requirements would necessitate a large number of qualification units. Finally, either a large quantity of circuits would have to be built and stock piled, or provision made for periodic re-order of the circuits which would be a constraint on the semiconductor manufacturer. These limitations can be solved on a program requiring a large volume of circuits, but are beyond the scope of this program. Thus, a standard logic family, available on the open market, will be selected.

A prime objective in using integrated circuits for the Apollo UDL and other spaceborne equipment is reliability enhancement. The selected circuit family must be well designed and manufactured to provide an inherent low failure rate for this type application. Manufacturers with proven capability in production of hi-rel devices will be emphasized.

The basic integrated circuit package (FEB) must also be a reliable design. Those packages which have established reliability at the present time include the TO-5, TO-18, and the flat package. Many more exotic packaging techniques are in the development phase, but are not presently ready for incorporation in space hardware. Of the three acceptable packages, the flat package (either 1/4" by 1/8" or 1/4" by 1/4") has been chosen because it will allow a smaller system volume using a reliable welded interconnect.

The temperatures imposed on the Apollo UDL are modest for monolithic integrated circuits. Many manufacturers make circuits which meet the full military temperature range (-55°C to +125°C) as well as reduced temperature versions. The full range devices should be specified for all spaceborne digital applications to insure obtaining the best possible product and to provide additional performance margins.

Power requirements for the digital circuits should be minimized. High power dissipation requires additional spacecraft weight in power supplies, energy sources (such as batteries or solar cells) and in heat sinks and cooling systems. High power dissipation will also raise the circuit ambient temperatures and affect system reliability.

A low module (FEB) count is also important for reducing size, weight, and power dissipation. Reduction in interconnections due to decreased number of circuits will upgrade the system reliability.

A desired characteristic for the Apollo UDL is easy interface with the Sub-Bit Detector and other circuitry. The logic family being replaced is a NAND type. The associated circuits present a current source type load to these logic elements, as does the NAND family itself. The

simplest interface would thus be an I/C family which is compatible with this loading requirement.

TYPES OF DIGITAL INTEGRATED CIRCUIT FAMILIES

The basic I/C logic types to be considered for this program are as follows:

RTL = Resistor - Transistor Logic - each load is a current sink. The major characteristics are simple and easy to fabricate, small voltage swings, marginal noise immunity.

RCTL = Resistor - Capacitor Transistor Logic - similar to RTL except that a capacitor is used across each resistor to remove transistor stored base charge (speed up). The capacitors allow use of larger resistors which increases voltage swings but makes fabrication more difficult. Noise immunity may be marginal.

DTL = Diode - Transistor Logic - each load is a current source. The major characteristics are large voltage swings with unequal rise and fall times. Fan-in is easily expandable and good noise immunity can be provided.

TTL = Transistor - Transistor Logic - the logic form is the same as DTL except that the input diodes are replaced by multiple-emitter transistors.

ECL = Emitter Coupled Logic - the circuits are operated in the linear range (off ground) which provides fast operation, small voltage swing, and good noise immunity. Interface with circuits using a ground reference is a problem.

AVAILABLE STANDARD LOGIC FAMILIES

The logic families listed in this section all meet the 25 K H_Z operating frequency and required temperature range. These families are available in the flat package. Because so many families meet these constraints they have been ordered in terms of power dissipation per basic gate element. The most promising types will be given further evaluation in succeeding sections.

1. Micropower RTL - This family introduced by CBS provides the lowest power. Its construction depends on very large resistors which means a combination of monolithic circuits with compatible thin film on a large (80 x 80 mil) chip. Because of the limited elements available, the family would result in a high module count and is not compatible with the required interface.

2. Series 51 RCTL - This basic TI logic family has a long history, low power, and reasonable package count. It will be considered in succeeding sections.

3. Milliwatt RTL - Versions of this family are produced by Amelco, Fairchild, GME, Philco and others. These simple circuits have low fan-out and a resulting high package count. There are no interface advantages over the Series 51. The higher power coupled with questionable noise immunity eliminates these elements.

4. Series 930 DTL - This DTL family introduced by Fairchild provides lowest power per circuit of presently available DTL and low package count. It will be studied further.

5. Series SE 100 DTL and MC 200 DTL - These families are offered by Fairchild, GME, Motorola, and Signetics. Considerable history is available for this family and it will also be considered further.

6. Other DTL families - Siliconix, TI Series 53, and Westinghouse DTL families provide similar circuits to the above DTL families but have the disadvantage of higher power levels. Since no significant advantages are offered, these families will not be considered.

7. Micrologic - The Fairchild micrologic family is a high power version of the milliwatt RTL and thus, is not suited for this application.

8. TTL families - The Sylvania TTL is the most prominent, but it features high speed with resulting high power. Package count and reliability should not be appreciably better than DTL families.

9. ECL - The Motorola MECL family is representative of this class. These circuits are extremely fast but require high power. As such, they are not suited to this application.

RELIABILITY COMPARISONS - STATISTICAL DATA

The circuit families which merit further consideration have been reduced to a manageable level, namely:

TI Series 51

Fairchild Series 930

Signetics Series SE 100

Motorola Series MC 200

These four companies have been producing digital I/C for several years in volume. Further, each has accepted high reliability programs on their devices, although Signetics would have the least total experience because they do not make transistors.

Basic I/C reliability data has been compiled by the Arinc Research Corporation, based on field failure data of digital I/C as compared with semiconductor components used in digital applications. The graph of figure 1 summarizes their findings. The basic conclusions are as follows:

A. The observed failure rate for digital integrated circuits is the same as that for a single transistor used in a digital application.

B. There is no observed wear out mechanism.

C. The mean failure rate of a microelectronic computer using 3000 digital I/C (made before July, 1963) is 6 months.

D. Diodes used in digital applications are still the most reliable semiconductors.

Reliability data from the four manufacturers was compared to determine the relative merits of each manufacturer. Absolute comparisons are very difficult because the manufacturers have run most tests at high

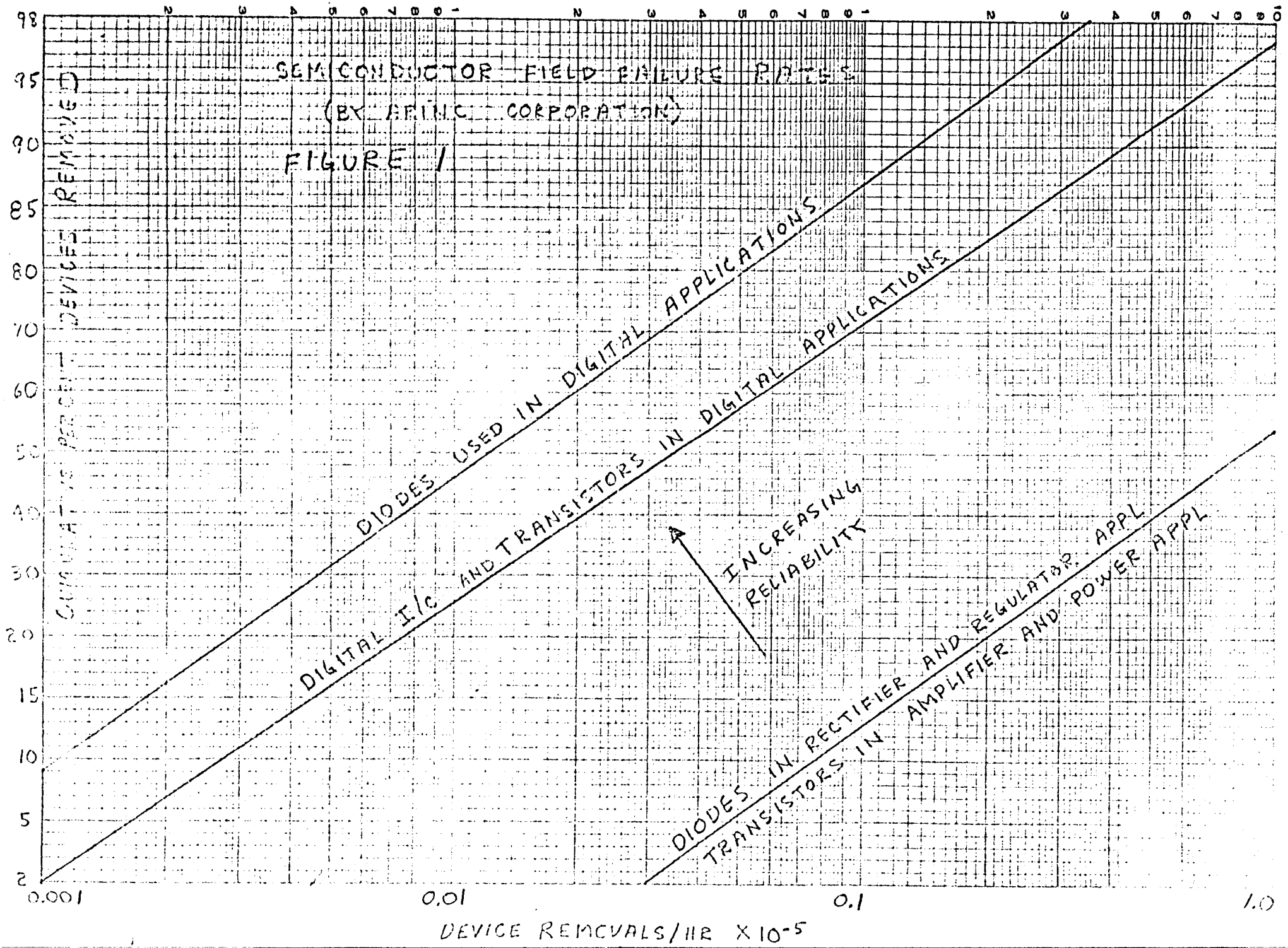
temperatures and used varying acceleration factors. Further, the tests have lumped widely varying circuit types and in the case of one manufacturer (Motorola) included hybrid I/C as well as monolithic I/C. Some failures have been catastrophic, others degradation. It is not apparent that all degradation failures would cause an equipment failure and some accepted usint might cause equipment failure. Thus, only a general observation will be attenpted. Most of the reliability data lumps TO-5 and flat packages, so a separate analysis of flat packages will be made. The listing below summarizes the available data.

Fairchild - Fairchild shows the lowest quoted failure rate, based only on Micrologic (RTL) family - no data was available on the 930 DTL to confirm this failure rate.

Motorola - Motorola data is based primarily on the MECL family and also includes hybrid circuits. Data on the MC 200 DTL was not separately available.

Texas Instruments - TI data includes all Series 51 units including early packaging seal problems. TI also has degradation failures which might not cause system failure.

Signetics - Signetics has experienced no failures on the SE 100 DTL at room temperature. High temperature failures, accountable primarily to "purple plague" at the Al-Au interface give these circuits the highest observed failure rate. Screening steps have been added to recent units to reduce this problem.


SEMICONDUCTOR FIELD FAILURE RATES
(BY AERONAUTICAL CORPORATION)
FIGURE 1
CUMULATIVE % OF DEVICES REMOVED
98
95
90
85
80
70
60
50
40
30
20
15
10
5
2
2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 10
0.001
0.01
0.1
1.0
DEVICE REMOVALS/HR X 10⁻⁵
DIODES USED IN DIGITAL APPLICATIONS
DIGITAL I/C AND TRANSISTORS IN DIGITAL APPLICATIONS
INCREASING RELIABILITY
DIODES IN RECTIFIER AND REGULATOR APPL
TRANSISTORS IN AMPLIFIER AND POWER APPL

RELIABILITY COMPARISONS - PACKAGE ANALYSIS

The basic flat packages made by each manufacturer were examined under a high power microscope. These packages were then dissected so that internal construction could be evaluated. Color photos were taken on the internal details for a permanent record. All units were supplied as representative of the manufacturer's current productions.

Motorola - The Motorola unit is an all aluminum system with a high temperature (500°C) seal in a ceramic package. Metalization and bonds appear to be good. Large bonding pads are spaced around the edge of the die. The package leads are gold plated only on the outside of the case. The package is sealed with a flat ceramic lid.

Fairchild - The Fairchild unit is also an all aluminum system with a high temperature seal. The package is sealed at the plane of the leads line and when opened the leads lift out rather easily. The gold coating on the leads extends through the package, giving rise to a possibility of a package sealing problem. The coating material does not appear to bond firmly to the leads. Large bonding pads are spaced around the edge of the die and metalization and bonds appear to be good.

Texas Instruments - The TI unit is a gold-aluminum system in a solder-sealed case (also stitch welded version). Bonds are made directly to the narrow metalized stripes rather than to bonding pads. The die is large and is positioned higher than the external leads, requiring the gold leads to be bent down past the edge of the die in order to make contact with the external lead. Internal interconnections are made both by metalization and by wire bonding. In the unit examined, two wire bonds were placed one on top of the other (wedge

bond and ball bond). Varnish is used around the bonding areas and leads to hold them in place.

Signetics - The Signetics unit is a clear glass package sealed with a flat kovar lid. The seal is quite good; however, the glass case fractured instead of the seal when the unit was opened. This indicates a possibility of internal glass strains with resultant case fractures when exposed to thermal stress. The die of the unit was smaller than the metal die bonding area (other circuits use the entire metal area). The die was attached with what appeared to be gold paste. Globs of this material were visible on the metal area and one glob was large enough to come dangerously close to an internal lead. None of the globs seemed to be loose. Aluminum metalization and gold ball bonds appeared to be good. All bonds were to bonding pads around the edge of the die.

RELIABILITY COMPARISONS - ELECTRICAL ANALYSIS

There are three significant electrical parameters which could have direct influence on system reliability when using integrated circuits. These are the circuit power level, noise immunity, and design margin. The circuits being considered are constrained to low power so no significant thermal problem should exist with any family.

The noise immunity (and noise generation) will be higher with these particular DTL families because of the larger voltage swings and relatively higher power than the Series 51 RCTL. The digital I/C will operate from a separate voltage in this system which will minimize problems in noise generation. Thus, the DTL families should have a net advantage.

The design margins are best evidenced by the fan-out and noise immunity characteristics. The RCTL circuits with emitter followers have the highest fan-out, but no better noise immunity than the regular RCTL. The Fairchild DTL circuits represent a newer circuit design and have higher fan-out and greater specified noise immunity than the Signetics and Motorola DTL's. The test data conducted on the program confirms this. Somewhat more noise is generated by the faster, larger voltage swing DTL's, but the overall design margins are better for the DTL than for the RCTL (TI) family.

The implementation of the Decoder Logic Circuits from Table 1 can be accomplished with each of the standard families. Table 4 shows the basic circuit elements available with each family in flat packages. No I/C manufacturer presently makes the Shift Register Flip-Flop with

the AC Set and/or AC Reset capability. This limitation will somewhat alter the logic design so that the DC Set-Reset terminals can be used. The Fairchild flip-flop which has both J-K and RR-SS capability is probably the most versatile. All Fairchild elements are in 14 pin packages; the other elements are in 10 pin packages except as noted. The larger number of pins will require more volume per package, but will generally reduce the total package count a corresponding amount, while reducing the total number of interconnections required.

The circuit elements were then compared with the existing 25 kc cordwood family. This comparison is very important because it gives the effect of size, weight, and power with respect to the existing design. While the size and weight improvements with I/C are obvious, the power levels for these circuit families show little change from the 25 kc family. This data is summarized in Table 5. The relative power figures are taken with all circuits in the maximum power dissipation levels and do not represent estimated power consumed in a final system. Numerous other options exist, such as operating the 930 Series at +5V supply which provides increased power dissipation and somewhat greater noise immunity. The Series 51 is specified for possible operation with a 3V supply; however, tests indicate that noise margins are undesirably low at that operating level. The 4 volt level gives minimum power; however, if the Series 51 is operated at 6 volts, this would eliminate the need for a 4 volts (special) logic supply.

The conclusion is that the Series 51 circuits represent the best power, module count tradeoff. The Series 930 circuits consume approximately the same power as the cordwood circuits with the lowest circuit count. The other logic series are less desirable either on a circuit count or power level basis.

TABLE 4 - CIRCUIT ELEMENTS IN THE I/C FAMILIES

Type	Series 930 (FCHLD)	Series MC200 (MOT)	Series SE100 (Sig)	Series 51(TI)
Flip-Flop	Clocked JK or Clocked RR-SS	Clocked JK Asynch JK	Clocked JK Asynch JK	Clocked RS Clocked RS W/EF
Gates	Dual 4-Input (1) Quad 2-Input	4-Input (1) Dual 2-Input	4-Input (1) Dual 2-Input Quad 2-Input (2) Triple 3-Input (2) Dual 4-Input (2)	6-Input (3) Dual 3-Input (3) Triple 2-Input (3)
Drivers	Dual 4 Buffer (1)	Power Gate Gated Line Driver	Power Gate Gated Line Driver Dual 4 Buffer (1) (2)	Clock Driver 6-Input Gate with EF
Input Expander	Dual 4-Input	60Input	6-Input Dual 3-Input	Note 3
Monostable	Yes	No	Yes	Yes

NOTE: 1. Input Expander NODE available.

2. These elements in new 1/4" x .35" package, require higher power than standard elements and use 14 pins.

3. Input expansion available by collector paralleling.

TABLE 5 - DECODER COMPARISONS

Family	Supply Voltage	Module Count	Relative Power
25 KC Cordwood	±6 VDC	106	1687 mw
Series 51 (TI)	+6 VDC	111	1246 mw
	+4 VDC	105	600 mw est.
Series MC200 (MOT)	+4V, -2V	160	2536 mw
Series SE100 (SIG)	+4V, -2V	160	2536 mw
(using new elements)	+4V, -2V	95	4450 mw
Series 930 (FCHLD)	+4 VDC	95	1660 mw

CONCLUSION AND SELECTION OF THE LOGIC FAMILY

No one I/C family has all the desired characteristics, yet each family will adequately meet the requirements of the I/C Decoder. Table 6 is a final summary of the four families. The most advantages accrue to the Series 930 DTL family as produced by Fairchild. This circuit family will be used for the program.

TABLE 6 - SUMMARY OF FAMILY CHARACTERISTICS

Parameter Rated	Series 51	Series SE100	Series MC200	Series 930
Reliability (a) Statistical Data	3	4	2	1
(b) Package Analysis	3	4	1	2
(c) Electrical Analysis	3	2	2	1
Power Dissipation	1	3, 4	3	2
Module Count	2	4, 1	4	1
Interface with Discrete Detector and Outputs	4	2	2	1

NOTE:

1. The preferred relative rating is the lowest number (1).
2. The summary does not imply that the various parameters have equal importance.
3. Dual ratings are given Signetics Series SE100 depending on whether the new higher power circuits are used.

APPENDIX 2

TELECOMMUNICATIONS LABORATORY

TECHNICAL MEMORANDUM

No. 3030-1-1 19 October, 1964

RELIABILITY COMPARISON OF THE APOLLO, UDL SYSTEM AND THE PROPOSED I/C UDL SYSTEM

Prepared by:

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R&C Group

Approved by:

R. F. Martin
R&C Group

ABSTRACT

A comparison of the reliabilities of the existing Apollo UDL system and the proposed I/C UDL system was made with the receiver eliminated from each system as well as a reliability estimate of a completely redundant I/C UDL system with the receivers eliminated.

MOTOROLA INC.

WESTERN MILITARY ELECTRONICS CENTER

INTRODUCTION

A reliability comparison was made of the Block Diagram I/C APP to UDL and the Apollo Up Data Link (UDL). The comparison was made considering the decoder, interface, sub-bit detector, power supply, cable assembly and connectors. A summary of the equipment and system reliabilities utilizing Block Diagram I/C APP to UDL is shown in Table I, for launch and orbiting environments.

The following list of assumptions and conditions were used to make this analysis.

1. Failure rates were determined from Motorola's Special Memorandum No. 188, dated 1 July 1964, at an ambient temperature of 70°C and calculated stress ratings except for integrated circuits which are assumed to operate at 10% of their power rating.
2. The failure rate was constant.
3. Part failure rates account for both catastrophic and performance degradation failures, and include solder joint failures associated with each component.
4. All parts were considered in series and a failure of any part results in system failure.
5. All parts were considered to be Hi-Rel and require screening (burn-in).
6. An environmental use factor of 10.0 was used for the launch environment and 1.0 for the orbital environment.
7. The time duration of the launch was assumed to be one-half hour, with an orbital mission time of 336 hours.
8. The receiver was eliminated from the original and proposed UDL systems' reliability estimates.

ESTIMATE OF THE I/C APP TO UDL

In Tables 2 thru 5 the failure rates for the power supply, sub-bit detector and Decoder/Interface are tabulated by modules and miscellaneous parts. The module and part failure rates, the number of modules and part types per subassembly are given for each module. The failure rates for the cable assembly and connectors are given in Table 6.

The environmental use factors were applied to the failure rate totals from Tables 2 thru 5. The resultant failure rates for each unit in its environment are given in Table 1. The reliability for each unit was determined by applying mission times for each environment to the expression:

$$R = \exp(-\lambda t)$$

where λ = the failure rate of the unit

t = mission time

The resultant reliabilities R_O (orbiting reliability) and R_L (launch reliability) were multiplied to determine the mission reliability ($t = 336.5$ hours) for each unit. The mission reliabilities for each unit were multiplied to determine the system reliability of 0.994223.

COMPARISON

A comparison of the previous Apollo/UDL reliability with the above system follows:

	Reliability ($t = 336.5$ Hours)
UDL System (original)	0.989390
I/C UDL System	0.994223

The reliability of the proposed I/C UDL system is higher than the previous system due to the replacement of discrete parts with integrated circuits in the Decoder and Sub-Bit Detector.

Table 1

Failure Rates and Reliabilities Comparison

Unit	Orbit Envir. Failure Rate %/1000 Hrs.	Launch Envir. Failure Rate %/1000 Hrs.	Orbit Reliability (R_O) t = 336 Hrs.	Launch Reliability (R_L) t = 0.5 Hrs.	Mission Reliability ($R_O \times R_L$) t = 336.5 Hrs.
Decoder/Interface	.665	6.65	0.997765	0.999967	0.997732
Sub-Bit Detector	.1564	1.564	0.999476	0.999993	0.999469
Power Supply	.3959	3.959	0.998670	0.999981	0.998651
Harnass & Connector	.477	4.77	0.998398	0.999977	0.998365
Proposed I/C UDL System (Without Receiver)	1.6943	16.943	0.994308	0.999916	0.994223
Original UDL (Without Receiver)	3.1687	31.687	0.98942	0.999984	0.98939
Redundant New System					0.999966

REDUNDANT ESTIMATE

An estimate for a manually switched redundant system was obtained by the following expression:

$$R_{Redundant} = 1 - (1 - R_{system})^2$$

Where R_{system} is the system reliability ($R_O \times R_L$) for t = 336.5 hours.

$$R_{Redundant} = 1 - (1 - 0.994233)^2$$

$$R_{Redundant} = 0.999966$$

Table 2

Power Supply
01-28282D02

Module	Part No.	Qty	Module F.R. %/1000 Hrs	Total Module F.R. %/1000 Hrs
Driver Module	01-27325D02	1	.0041	.0041
Input Filter	01-27329D02	1	.0745	.0745
Rectifier No. 1	01-27333D02	1	.0791	.0791
Rectifier No. 2	01-27337D02	1	.044	.044
Power XMFR	25-27341D02	1	.061	.061
Power Ampl.	01-27345D02	1	.0666	.0666
Astable MV	01-27349D02	1	.0046	.0046
Monostable MV	01-27353D02	1	.0031	.0031
Diff. Ampl.	01-27357D02	1	.01007	.01007
Low Volt Det	01-27385D02	1	.0030	.0030
Low Volt Det Fltr	01-27393D02	1	.0242	.0242
Capacitor Assy	23-27383D02	1	.0216	.0216
			Total	.3959

Table 3

Sub-Bit Detector

Module	Part No.	Qty	Module F.R. %/1000 Hrs	Total Module F.R. %/1000 Hrs
Integrated Circuits		8	.002	.016
Capacitor (Tant)		1	.0006	.0006
Phase Det DVR	01-27263D02	2	.00449	.00898
Phase Det	01-27267D02	2	.00273	.00546
Volt Cont OSC	01-27321D02	1	.01319	.01319
Matched Filter Amp	01-27365D02	1	.00967	.00967
Integrate & Dump	01-27369D02	1	.0144	.0144
Mode Switch/Emitter Fol	01-27401D02	1	.0228	.0228
10:10:1 XMFR	25-28317D01	2	.030	.0600
Loop Filter	01-27389D02	1	.00531	.00531
			Total	.1564

Table 4

Decoder/Interface

Module	Part No.	Qty	Module F.R. %/1000 Hrs	Total Module F.R. %/1000 Hrs
Relay Sel Dvr	01-27227D02	8	.00403	.03224
Relay Set Dvr	01-27231D02	4	.0046	.0184
Computer Driver	01-27307D02	2	.0689	.1378
IP Switches*		5	.0472	.236
Integrated Circuits		120	.002	.24
Resistor		2	.000012	.000024
Capacitor		2	.000275	.00055
			Total	.665

* Addition to present UDL for the CTE Interface

Table 5

Cable Assemblies and External Connectors

Part Type	Part No.	Qty	F.R. %/1000 Hrs	Total F.R. %/1000 Hrs
Wiring Harness		1	.315	.315
External Connectors		3	.54	.162
			Total	.477

APPENDIX 3

Mode Switch Design

GENERAL CONSIDERATIONS

The mode switch is to operate from a PSK modulated signal supplied by either a UHF or S-band receiver. The receiver output must be isolated at a high impedance level; transformer coupling seems most feasible. The S-band output is transformer coupled. To assure adequate passage of the PSK spectrum with minimal degradation, the maximum allowed phase shift has arbitrarily been set at 5^{o}.

A 5^{o} phase shift corresponds to a signal degradation (δ) of

$$\delta = 20 \log \frac{1}{\cos 10^{o}} = 0.172 \text{ DB}$$

The general mode switch configuration is shown in Figure A3-1.*

INPUT TRANSFORMER

The UHF signal source is specified at 1 volt rms from a 19.6K ohm source impedance. Using a 1:1 transformer, the transfer ratio

$$\left|\frac{eo}{es}\right| = \frac{R'}{R_S \left[1 + \left(\frac{R'}{\omega L}\right)^2\right]^{1/2}} \qquad \text{(See Figure A3-2)}$$

$$\text{Phase shift} = \arg \frac{eo}{es} = -\tan^{-1} \left(\frac{R'}{\omega L_p}\right)$$

$$\text{where } R' = \frac{R_S R_L}{R_S + R_L}$$

and $R_L = 6.2K$ as determined in the next section.

*Referenced figures will be found at the end of this Appendix.

Then $R' = \frac{19.6 \times 6.2}{19.6 + 6.2} = 4.7K$ ohms.

For $\arg \frac{eo}{es} \leq 5^o$ at f = 250 cps,

$$\frac{\omega L_p}{R'} \geq 6 \text{ and } L_p \text{ minimum} = 18 \text{ henries}$$

$$\left|\frac{eo}{es}\right| \geq \frac{4.7K}{19.6K\left[1 + \frac{1}{36}\right]^{1/2}} = 0.232$$

Thus the transformer mismatch results in a signal loss which must be recovered in the mode switch amplifier.

SWITCH SELECT CIRCUITRY

The configuration for the switch select circuitry can take many forms, but the one in Figure A3-3 was chosen because it provides excellent input isolation between channels and does not require any flow of dc through the input transformer. The isolation was measured to be greater than 55 db.

When UHF output is desired, the mode control switch is grounded placing a +4v on the cathode of CR2 and +0.1 volt at one side of R2. This allows CR1 to conduct with approximately 230 ohms resistance (taken from diode curve). The voltage at the anode of the diodes is approximately 2.4 volts dc which back biases CR2. The extremely high back biased impedance of CR2 effectively blocks any current transfer from the S-band input.

Resistor selections R2 and R3 are chosen to provide sufficient current through CR1 to bias the diode in a linear range. The resistor ratio is determined by back biasing requirements for the alternate input. Resistor R2 represents a signal loss on the UHF channel and must be as large as practical.

Capacitor selection for C1 has been based on minimum capacitor physical size to obtain negligible phase shift.

$$\arg \frac{eo}{es} = \tan^{-1} \left[\frac{X_C}{R_S + R_L} \right]$$

for f = 250 cps and C = 4.7 μf

$$\arg \frac{eo}{es} = \tan^{-1} \left[\frac{1}{6.28 \times 4.7 \times 10^{-6} \times (19.6K + 4.7K)} \right] \approx 0.35^{o}$$

$$\text{gain change } \left| \frac{eo}{es} \right| = \frac{19.6K + 4.7K}{19.6K + 4.7K + .16K} \approx 1$$

thus a 4.7 μf capacitor is sufficient.

The measured output of the switch select circuit with a 1 v rms input on the UHF channel is 0.23 volts rms. An equivalent output is required for S-band audio. The ratio of R9 and R10 provides a signal loss so that the output when using S-band input is also 0.23 volts rms.

AMPLIFIER CIRCUITRY

The output of the mode switch drives the dual phase detector transformer. A 1:5:5:5:5 transformer is used to step up the phase detector input to 12 volts peak or $\frac{12}{1.72} = 7.0$ volts rms. The amplifier output must then be $\frac{7.0}{5} = 1.4$ volts rms for maximum signal. Maximum input signal is 1.2 volts rms into the mode switch; hence maximum gain is $\frac{1.4}{1.2} = 1.16$. Mode switch gain will be designed for 1.07 to prevent phase detector saturation under worst case component tolerances. Amplifier input is 0.28 volts maximum; amplifier gain is set at 4.8.

To avoid gain changes due to loading effects on the input transformer by the amplifier, a Darlington configuration was used. This resulted in a minimum input impedance of 64.8K. Gain stabilization is achieved by using degenerative feedback in the form of an unbypassed emitter resistor in the inverting stage Q2

of Figure A3-4. Calculated and measured gain changes over the temperature range of -40°C to +85°C were less than 2%. Gain variation due to limit 8 units was calculated as less than 6%.

PHASE SHIFT

Because of the rigid phase shift tolerances, capacitors were selected to produce minimal shift. All capacitors are derated and used at 50% or less of the nominal d-c voltage rating. A computer analysis of the amplifier was used to plot the effect of various capacitor sizes in the output circuitry. A 20 μf output capacitor introduced 4.5° of phase shift at 250 cps and approximately 1° at 1K cps. A 10 μf capacitor introduces 6° and a 5 μf introduces 10° of phase shift at 250 cps. Further increase in capacitance did little to improve phase shift at 250 cps, primarily because the transformer inductance dominated. Table AIII-1 shows the measured phase shift with temperature for the mode switch and transformer. The current lead at high frequencies has been attributed to distributed capacitance in the transformer windings.

TABLE AIII-1. Mode Switch Phase Shift

	250 cps	4K cps
-40°C	-6°	+1.9°
+25°C	-3°	+3°
+85°C	-4°	+6°

The mode switch module has a power dissipation of 280 milliwatts. This value could be reduced in future equipment by a minor redesign based on a 12-v power supply.

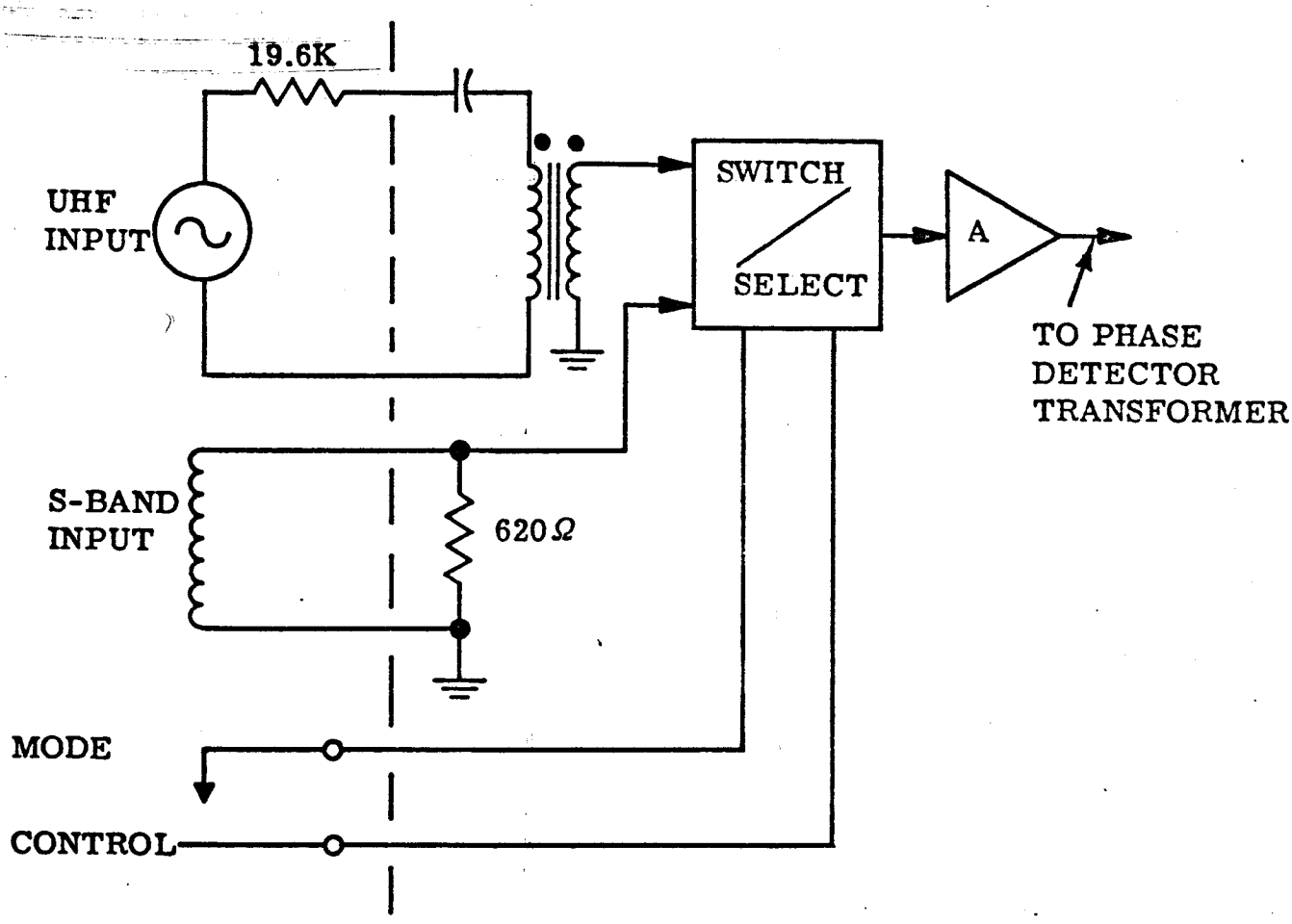
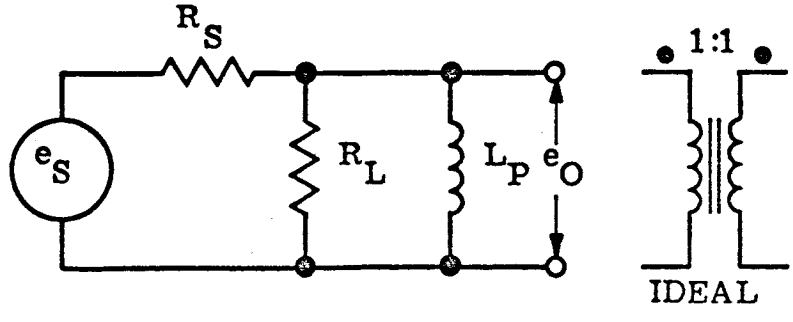


Figure A3-1. Mode Switch Block Diagram



5318-16

Figure A3-2. Input Transformer Circuit

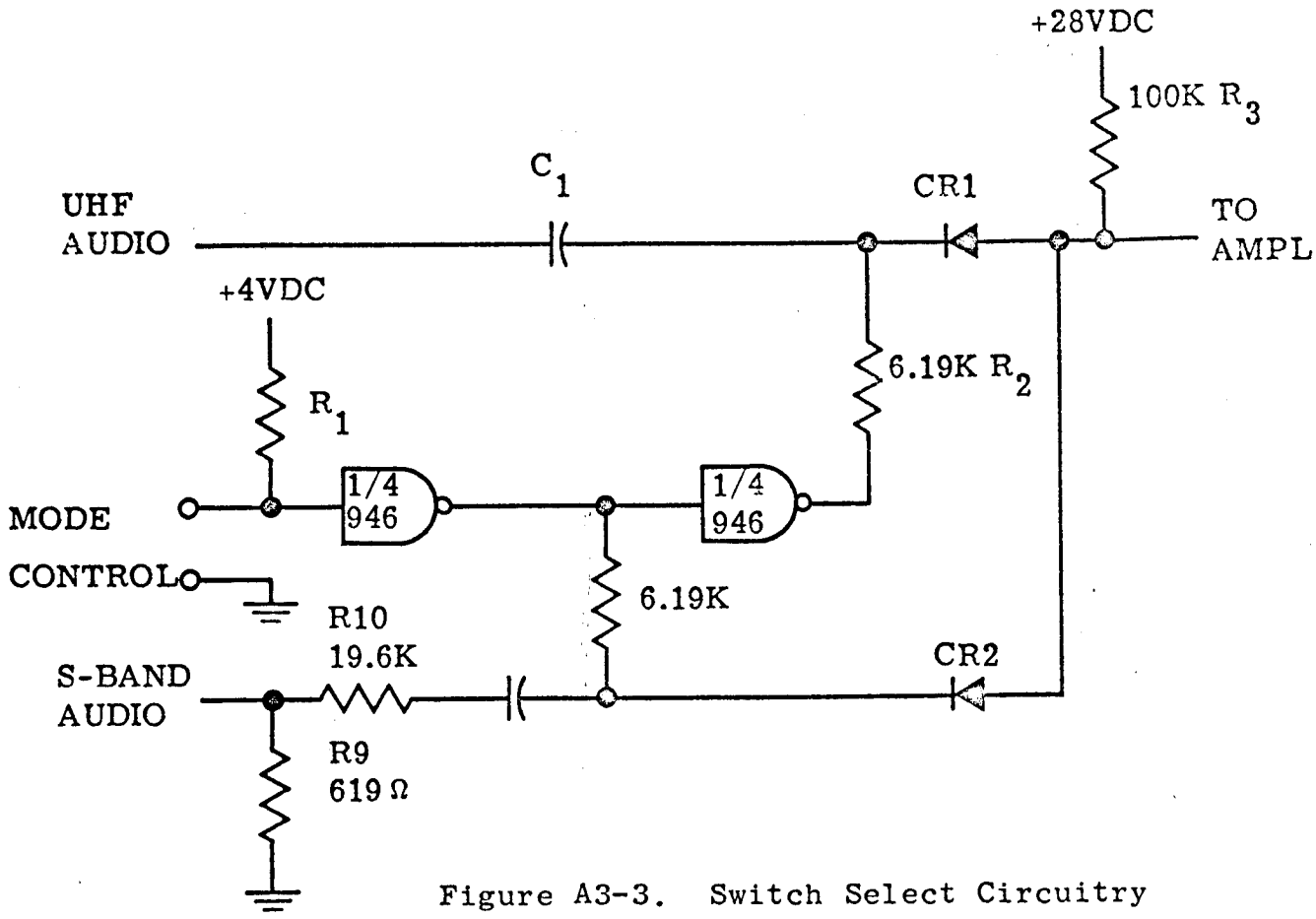


Figure A3-3. Switch Select Circuitry

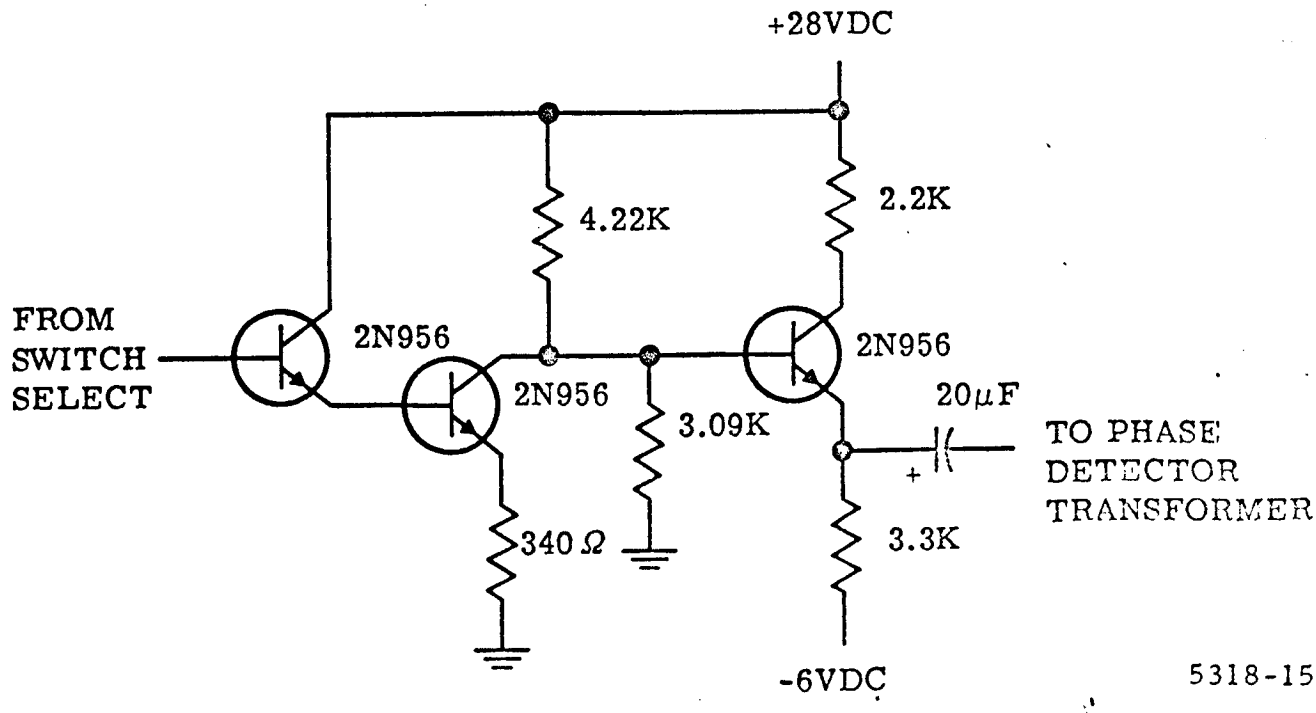
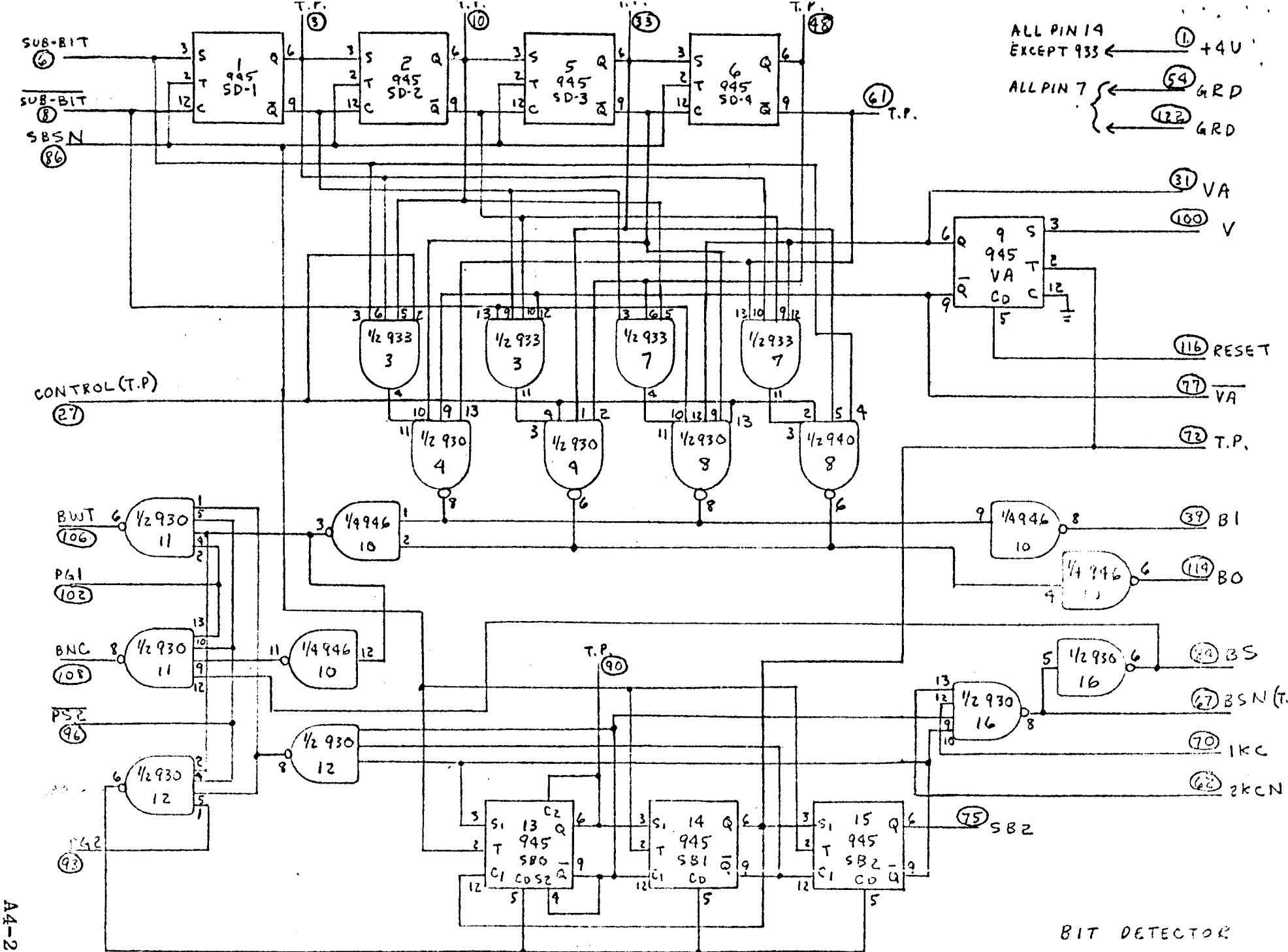


Figure A3-4. Amplifier Circuitry

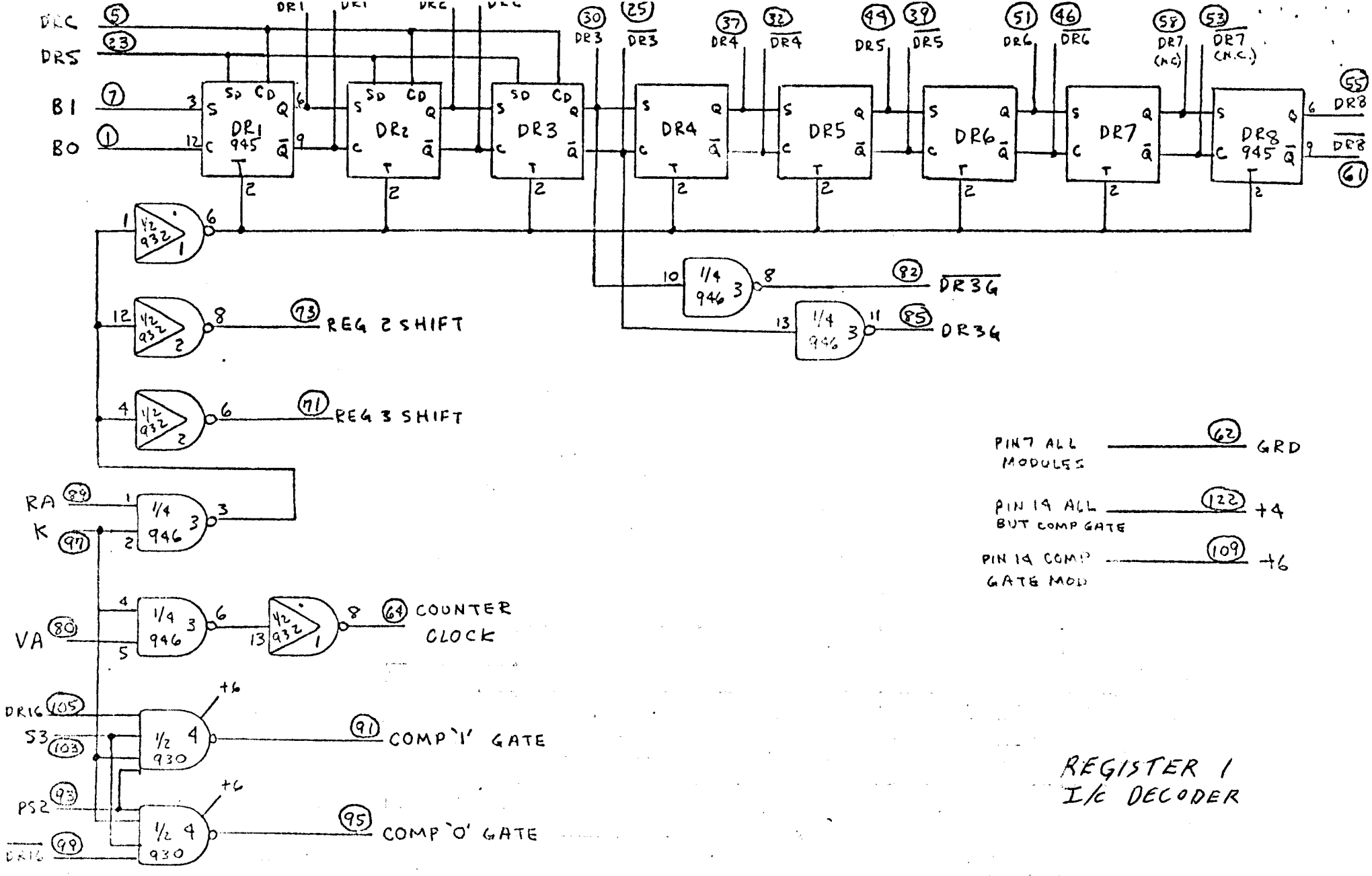
APPENDIX 4

List of Drawings used in the program:

1. Bit Detector Module, Logic Diagram
2. Register 1 Module, Logic Diagram
3. Register 2/3 Module, Logic Diagram
4. RTC Set-Reset Module, Logic Diagram
5. Address Decoder Module, Logic Diagram
6. Program Control Counter Module, Logic Diagram
7. Programmer Module, Logic Diagram
8. Reset Generator Module, Logic Diagram
9. Output Gating Module, Logic Diagram
10. RTC Selection Module, Logic Diagram
11. Detector Timing Module, Logic Diagram
12. Phase Detector Driver Module, Logic Diagram
13. Sub-Bit Detector, Block Diagram
14. Interface Subassembly, Block Diagram
15. Voltage Regulator, Schematic Diagram
16. Base Wiring Assembly, Wire List
17. Base Pin Connection Diagram
18. I/C UDL Chassis Diagram
19. Adapter Drawer, Test Point List

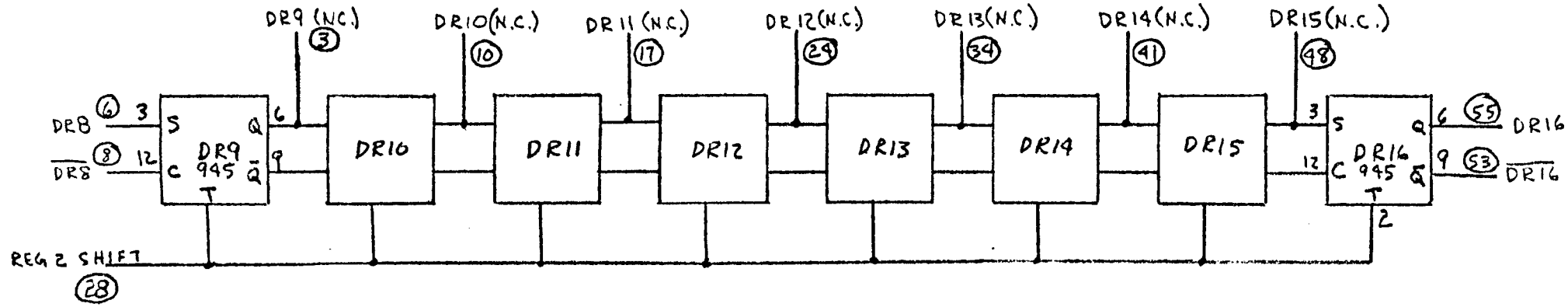

SUB-BIT
SUB-BIT
SBSN
1 945 SD-1
2 945 SD-2
5 945 SD-3
6 945 SD-4
T.P.
ALL PIN 14 EXCEPT 933
+4U
ALL PIN 7
GRD
GRD
9 945 VA CD
VA
V
RESET
VA
T.P.
CONTROL (T.P)
1/2 933 3
1/2 933 3
1/2 933 7
1/2 933 7
1/2 930 4
1/2 930 9
1/2 930 8
1/2 940 8
BWT
PGI
BNC
PSZ
1/2 930 11
1/2 930 11
1/2 930 12
1/2 930 12
1/4 946 10
1/4 946 10
1/4 946 10
1/4 946
T.P
1/2 930 16
1/2 930 16
13 945 SBO
14 945 SBI
15 945 SBZ
BI
BO
BS
BSN (T.
IKC
2KCN
SBZ
BIT DETECTOR
I/C DECODER
31 MAR 65

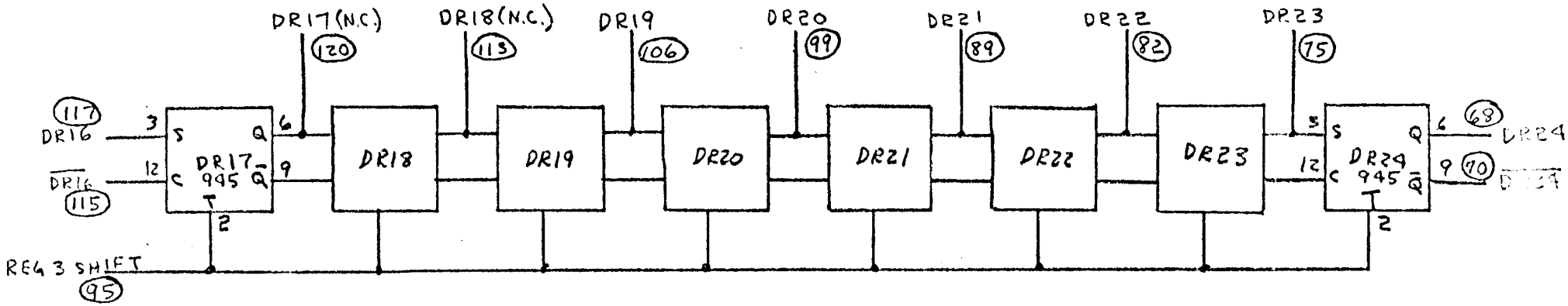
A4-2



REGISTER 1
I/c DECODER

REGISTER 1
I/c DECODER



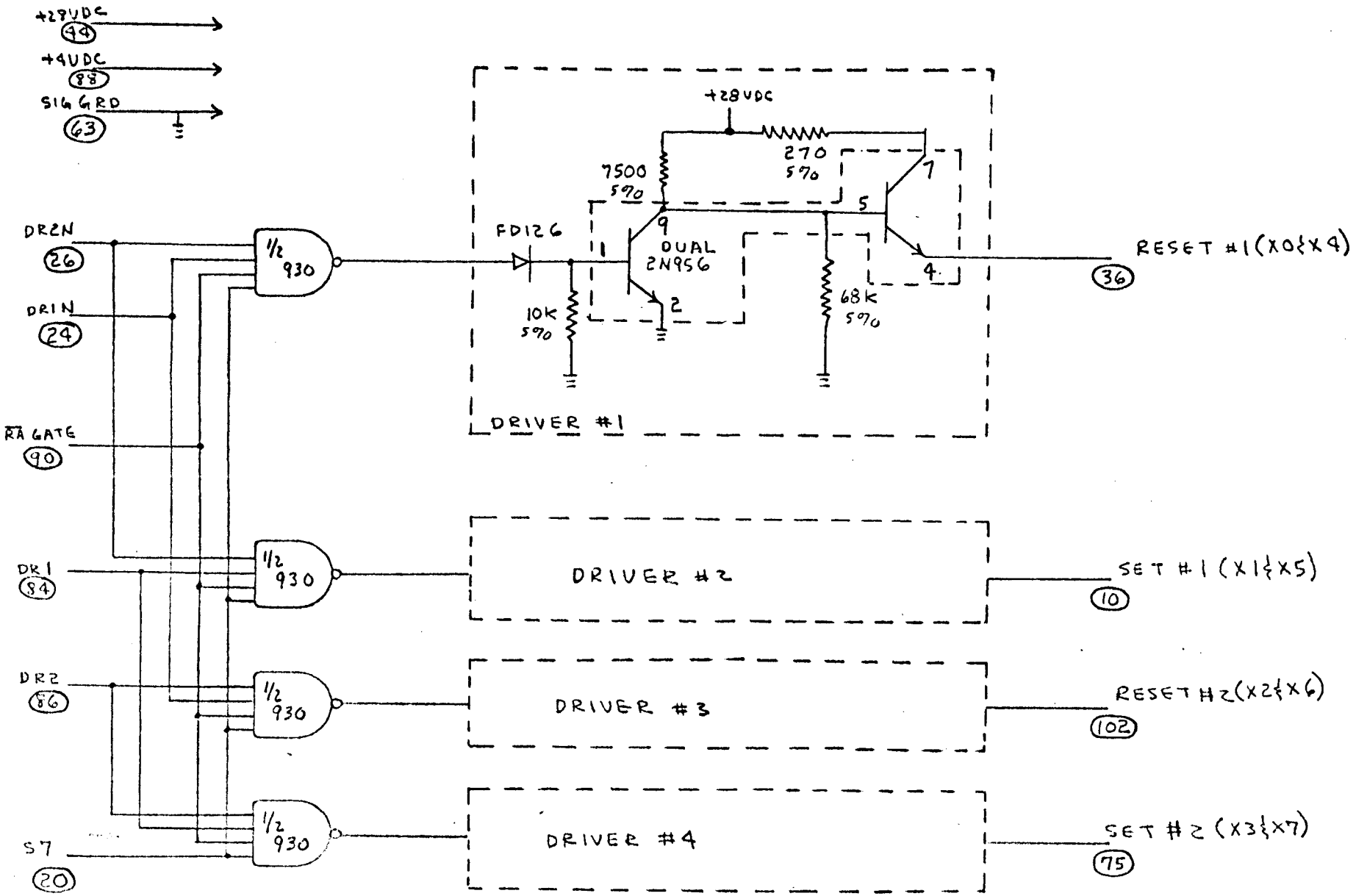


+4V (61)(62) all pin 14

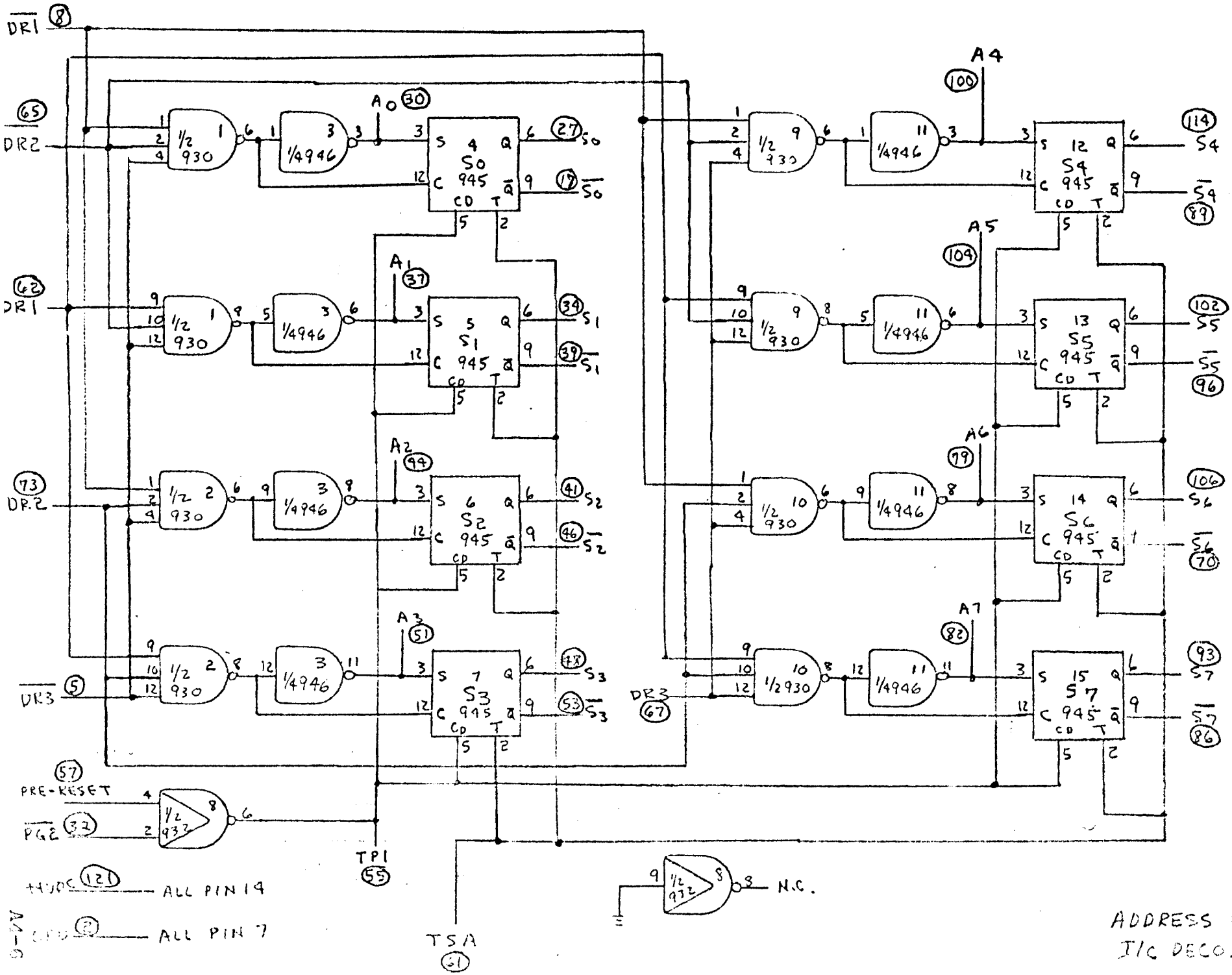
GRD (1)(122) all pin 7

REGISTER 2/REGISTER I/C DECODER

5 JAN 65



RTC SET-RESET
I/C DECODER
31 MAR 1965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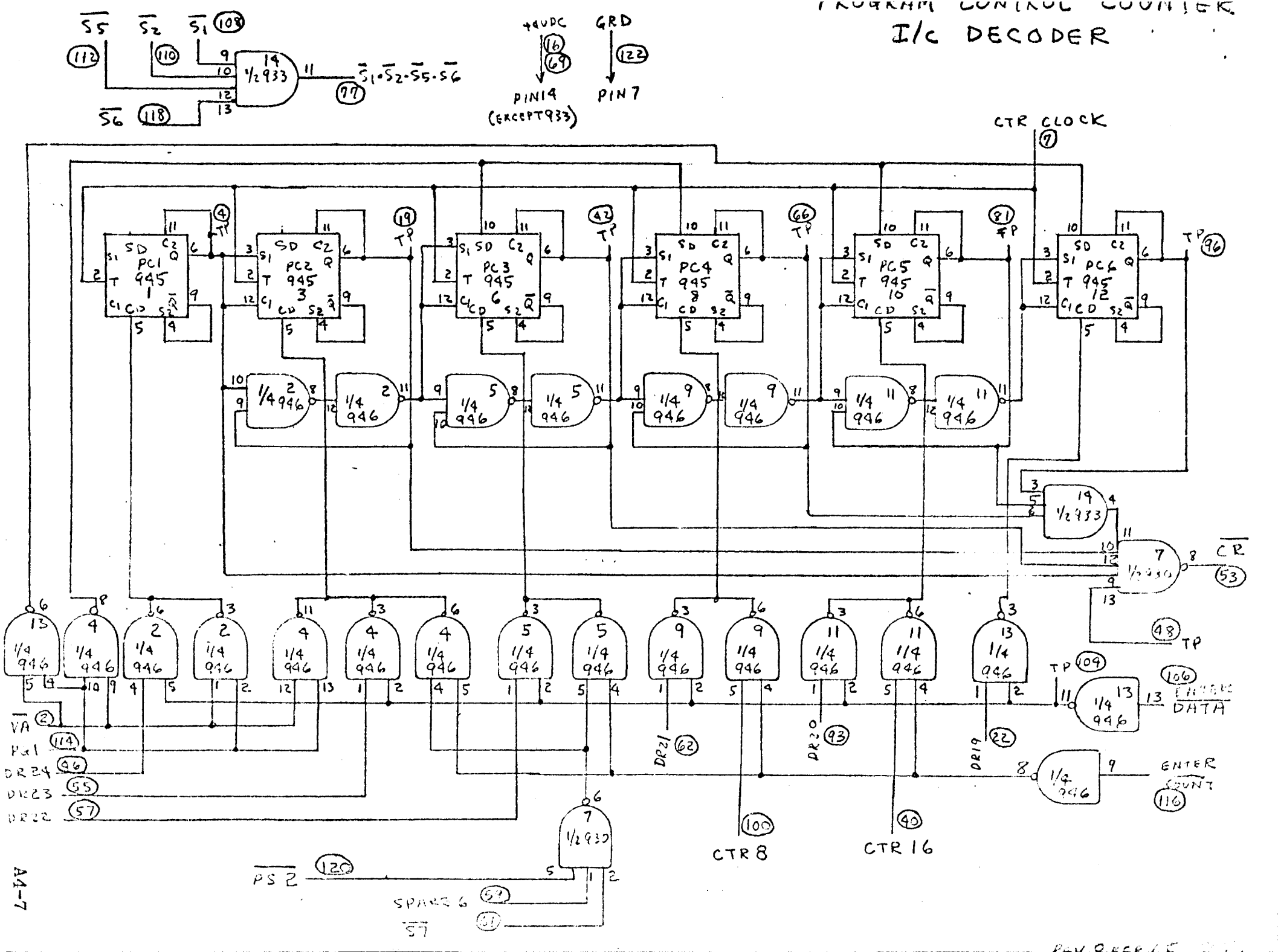
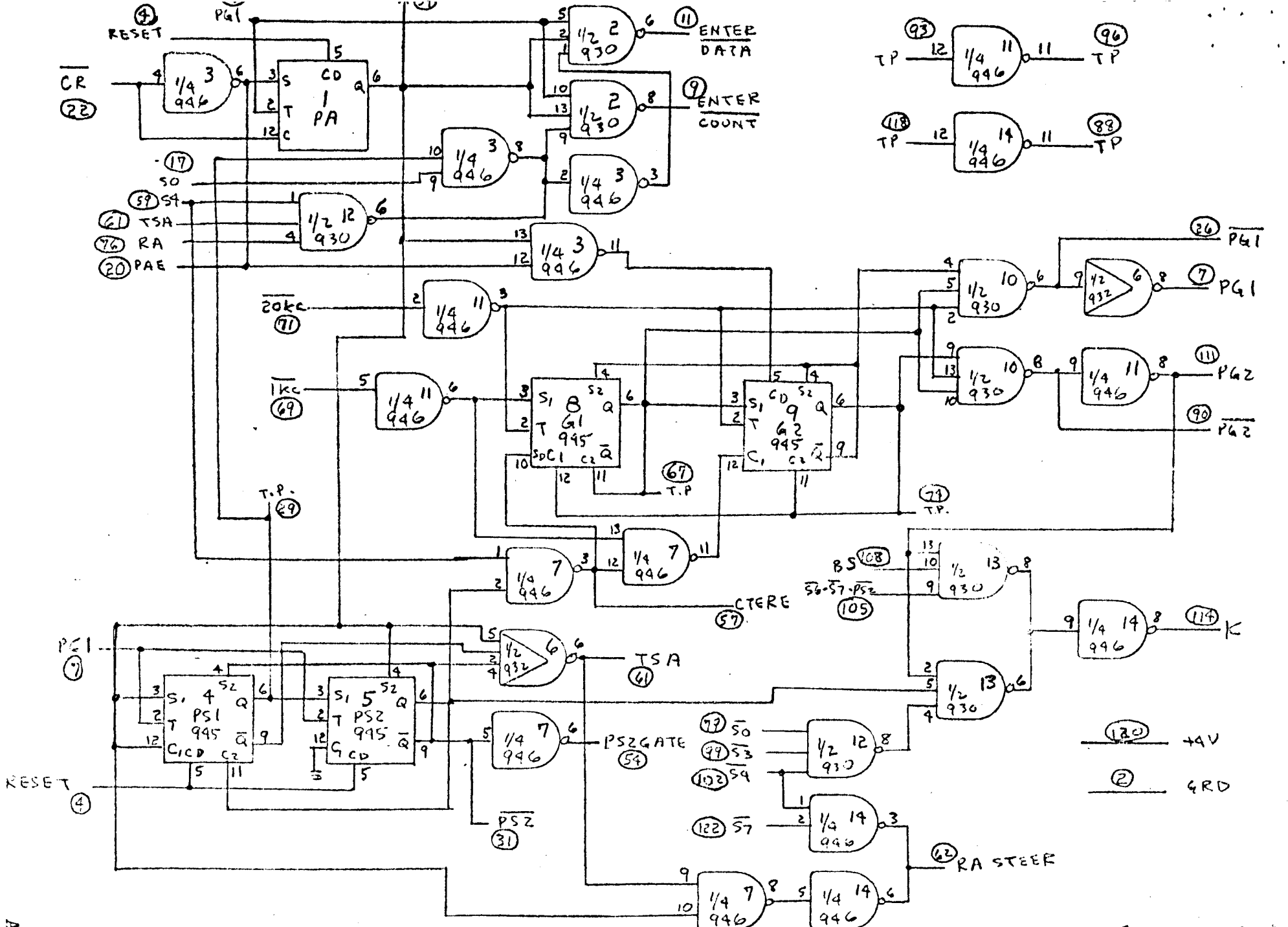
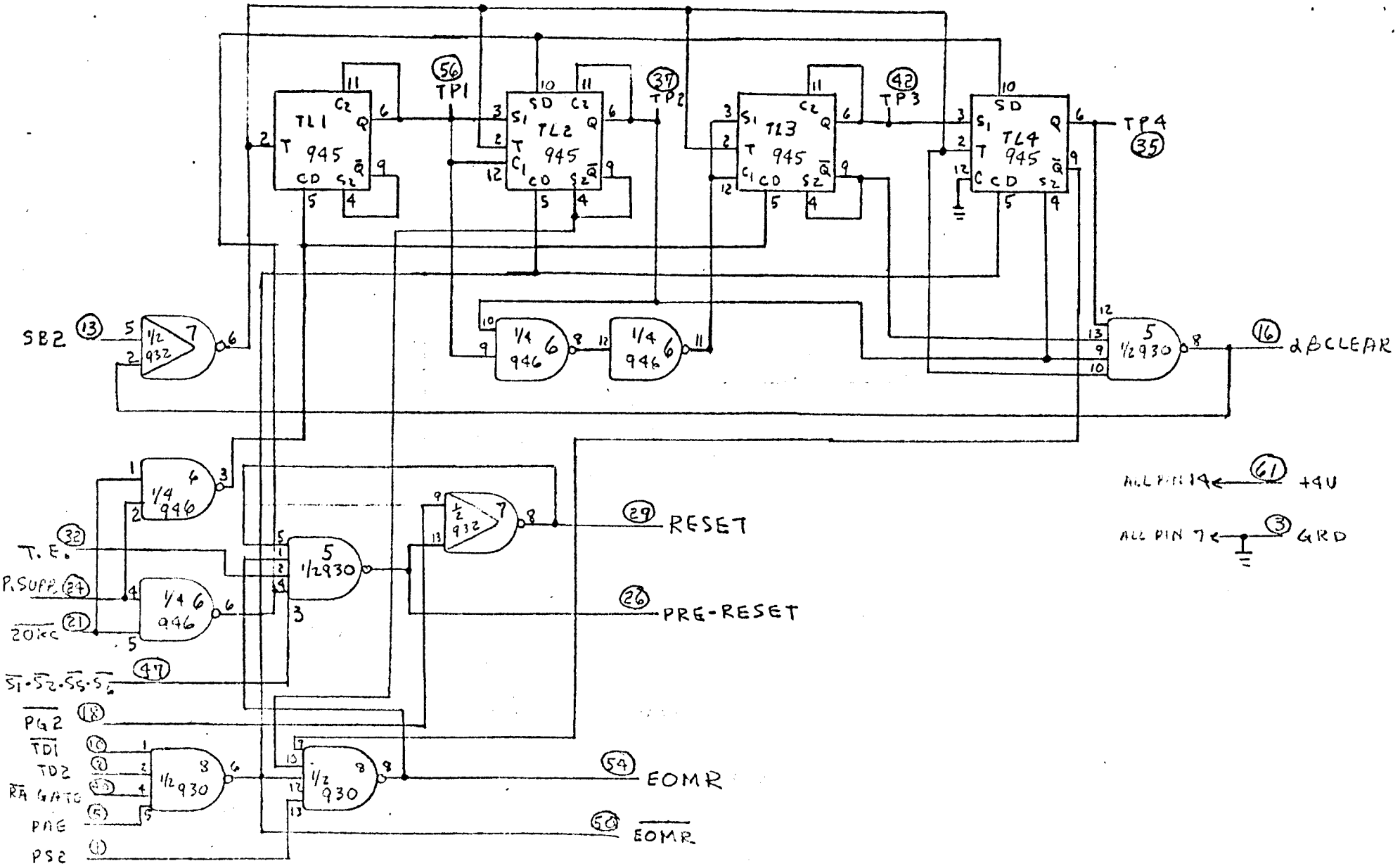
DR2
DR1
DR2
DR3
DR3
PRE-RESET
PGE
TPI
TSA
A0
A1
A2
A3
A4
A5
A6
A7
S0
S1
S2
S3
S4
S5
S6
S7
ALL PIN 14
ALL PIN 7
N.C.
ADDRESS DECODER
I/C DECODER

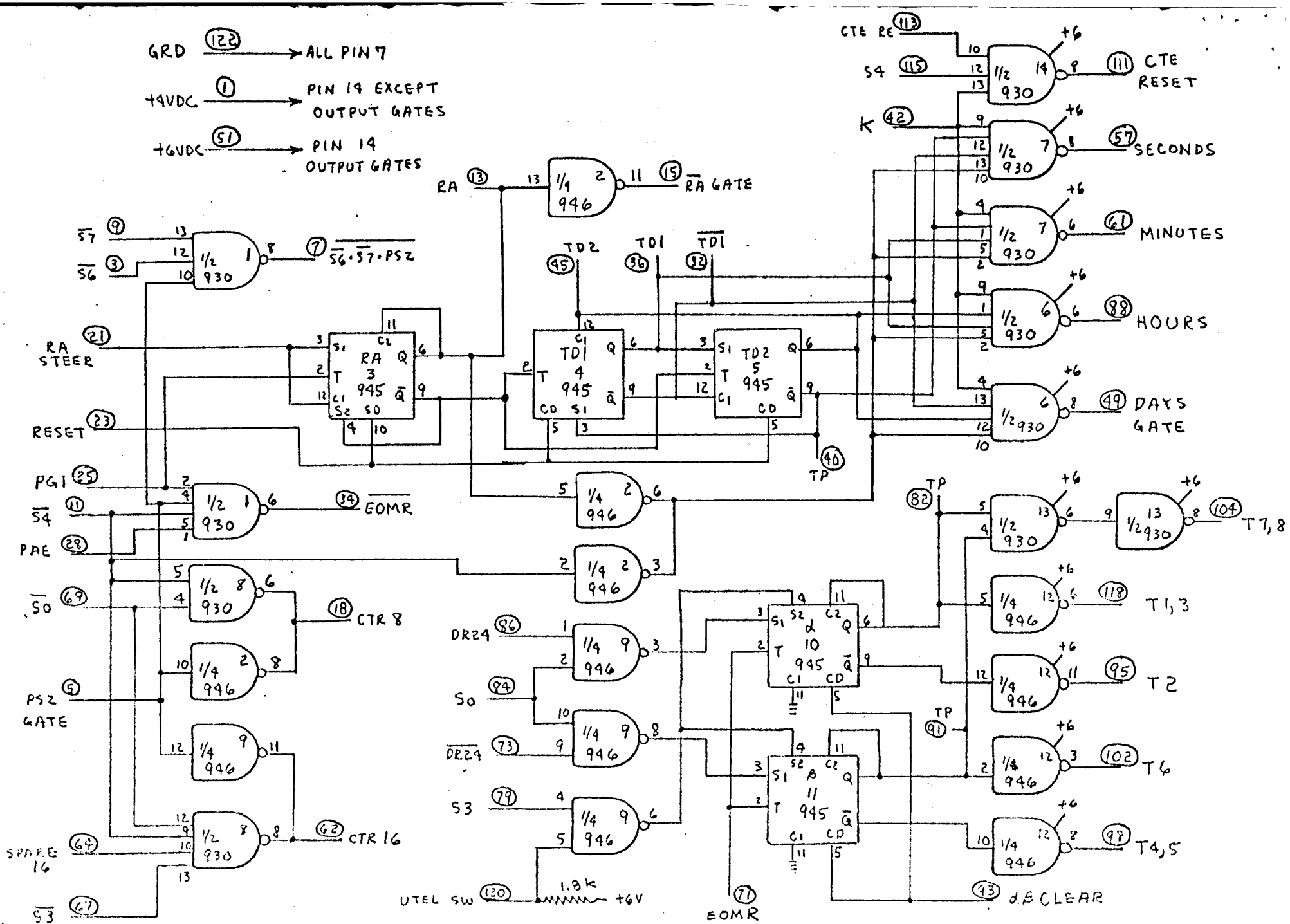
PROGRAM CONTROL COUNTER
I/c DECODER



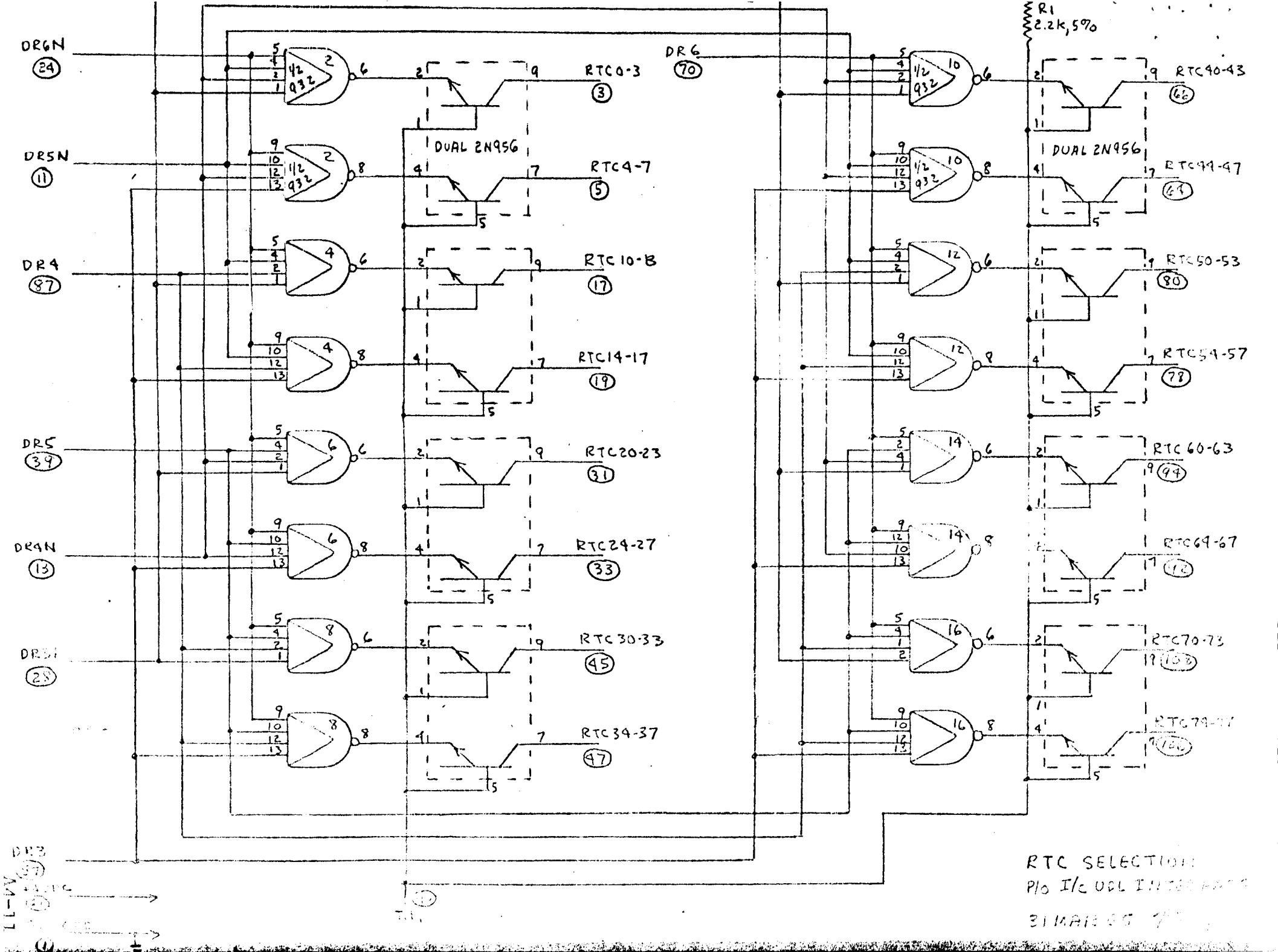

RESET
PG1
CR
ENTER DATA
ENTER COUNT
TP
TP
TP
TP
SO
SS
TSA
RA
PAE
20kc
1kc
T.P.
T.P
T.P.
PG1
PG1
PG2
PG2
BS
CTERE
TSA
PSZGATE
PSZ
RESET
RA STEER
+4V
GRD
PROGRAMMER
I/C DECODER
15 APR 65

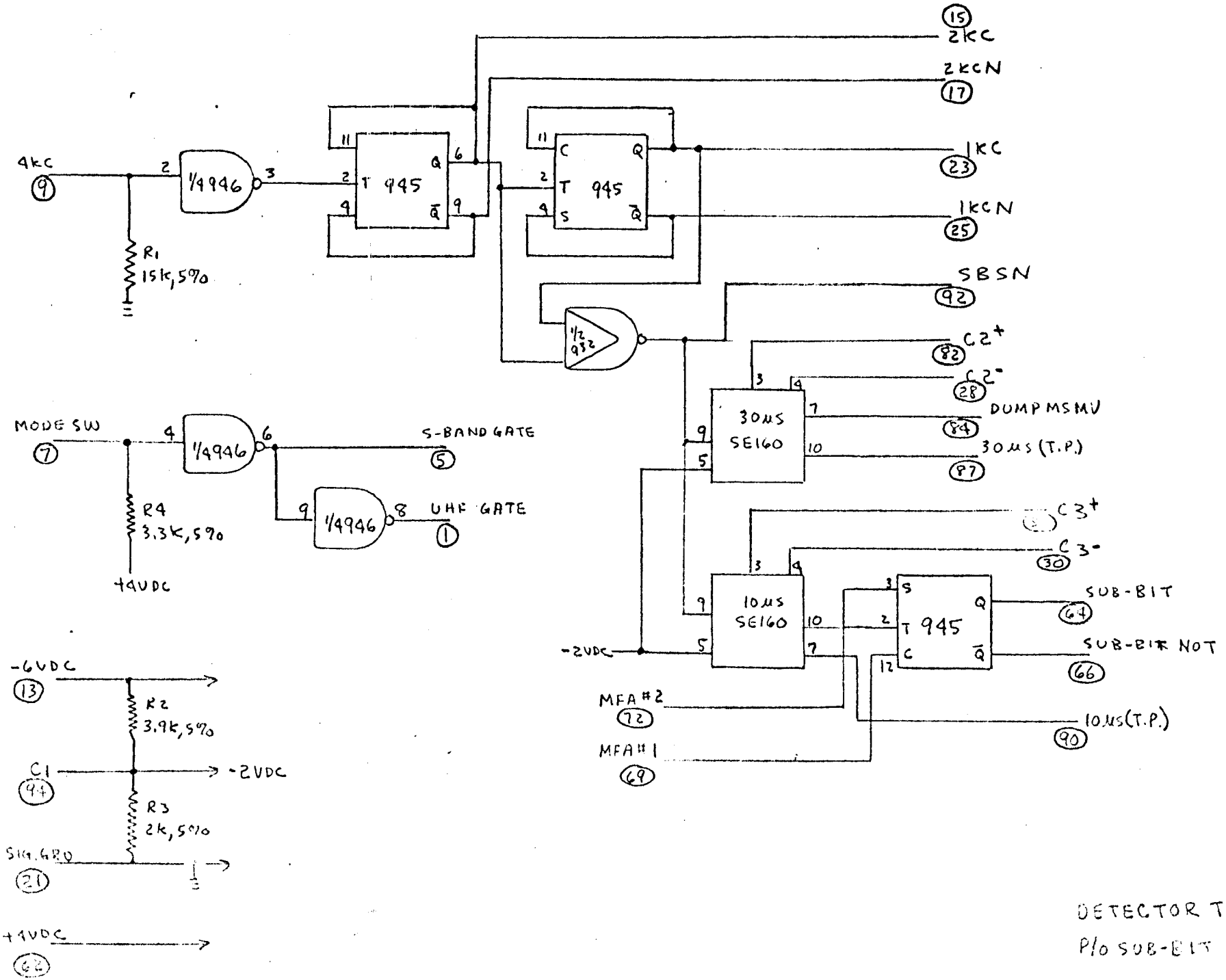


RESET GEN... I/C DECO...
REV. 1A MAR 1967



OUTPUT GATING
I/C DECODER


DR6N
(24)
DR5N
(11)
DR4
(87)
DR5
(39)
DR4N
(13)
DR3
(25)
DR3
(59)
DR6
(70)
R1
2.2k, 5%
DUAL 2N956
DUAL 2N956
RTC 0-3
(3)
RTC 4-7
(5)
RTC 10-13
(17)
RTC 14-17
(19)
RTC 20-23
(31)
RTC 24-27
(33)
RTC 30-33
(45)
RTC 34-37
(47)
RTC 40-43
(66)
RTC 44-47
(68)
RTC 50-53
(80)
RTC 54-57
(78)
RTC 60-63
(94)
RTC 64-67
(92)
RTC 70-73
(103)
RTC 74-77
(101)
RTC SELECTION
P/O I/C UDL
3 MAR 65

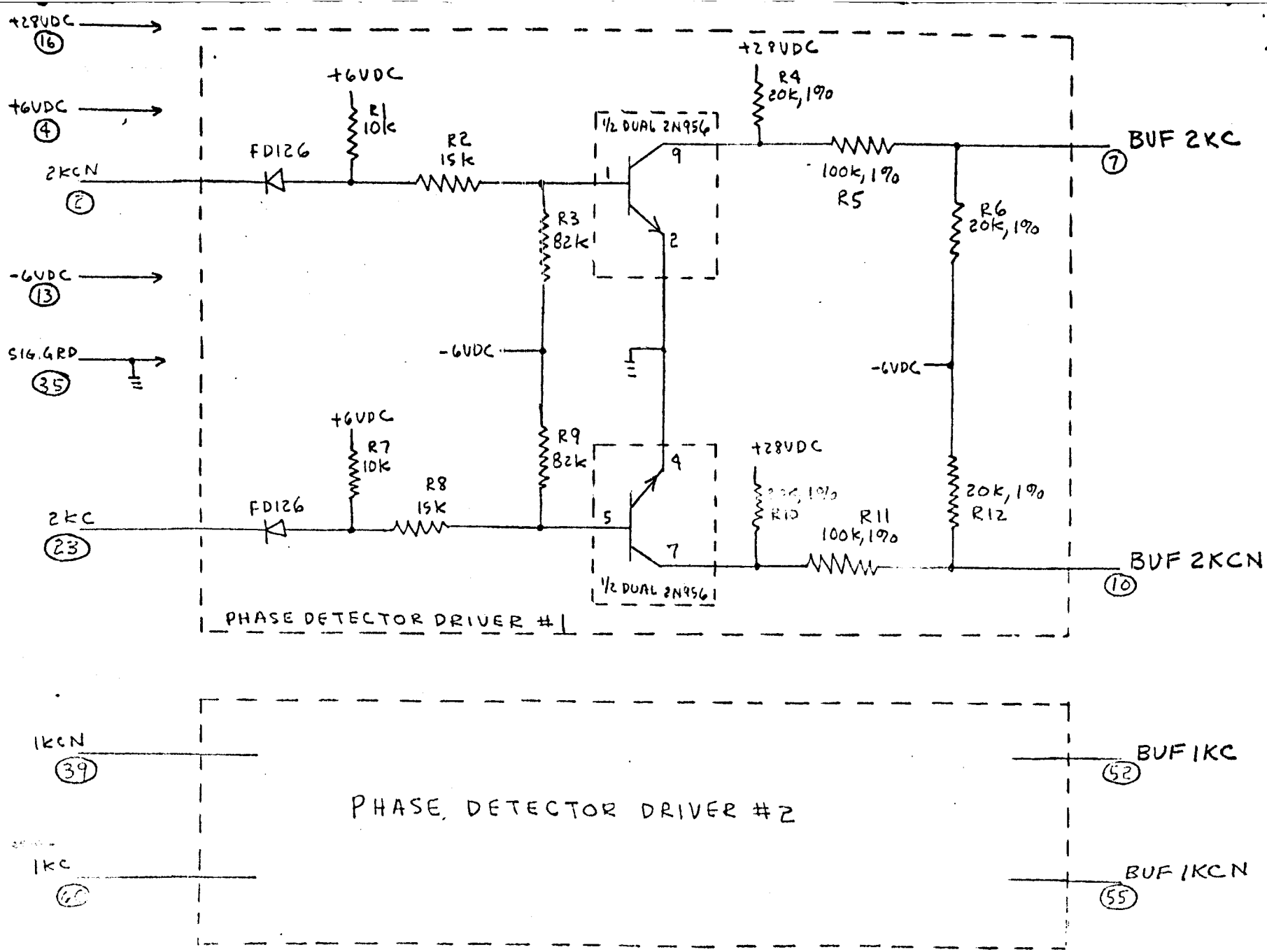


DETECTOR TIMING

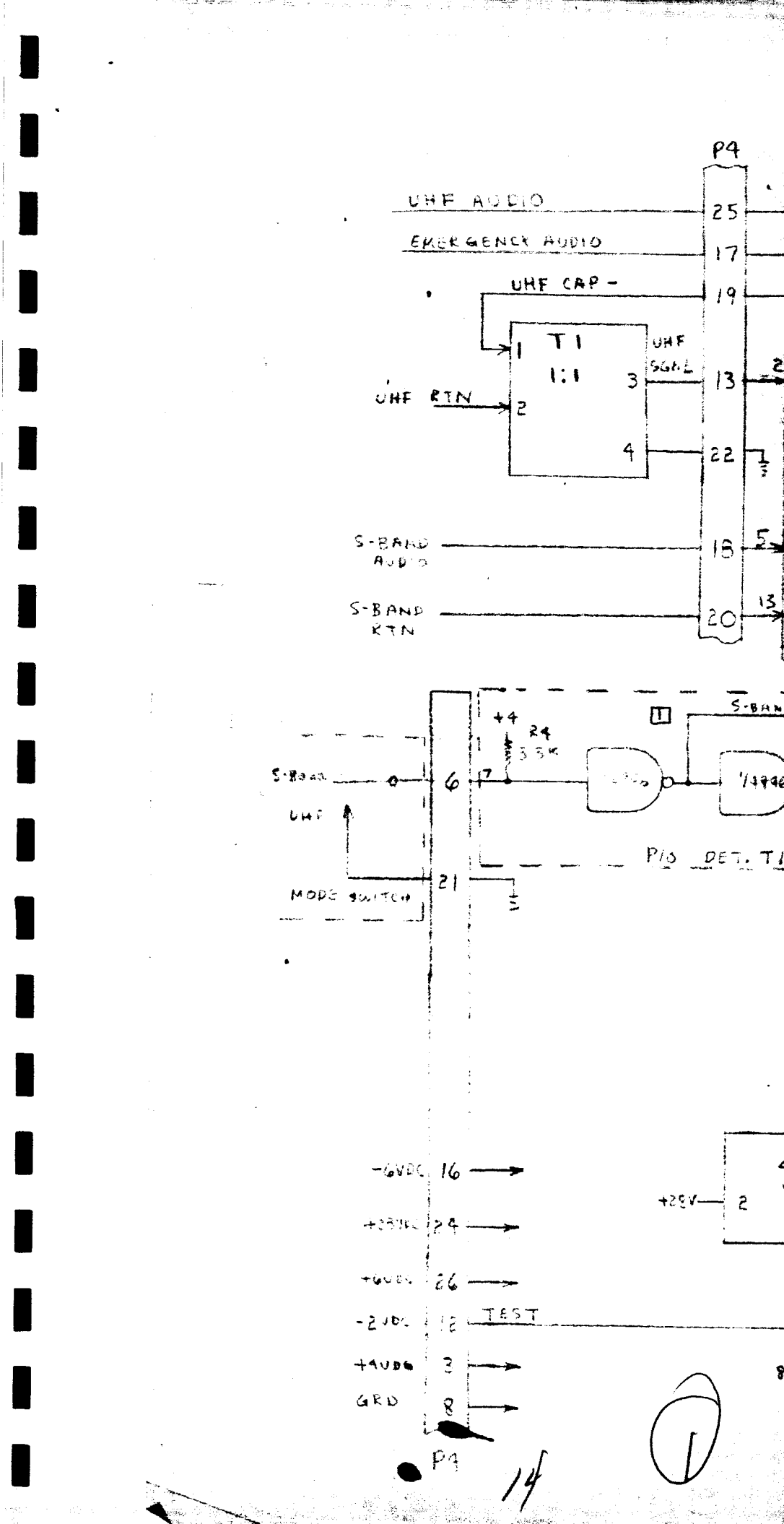
P/O SUB-BIT DETECTOR

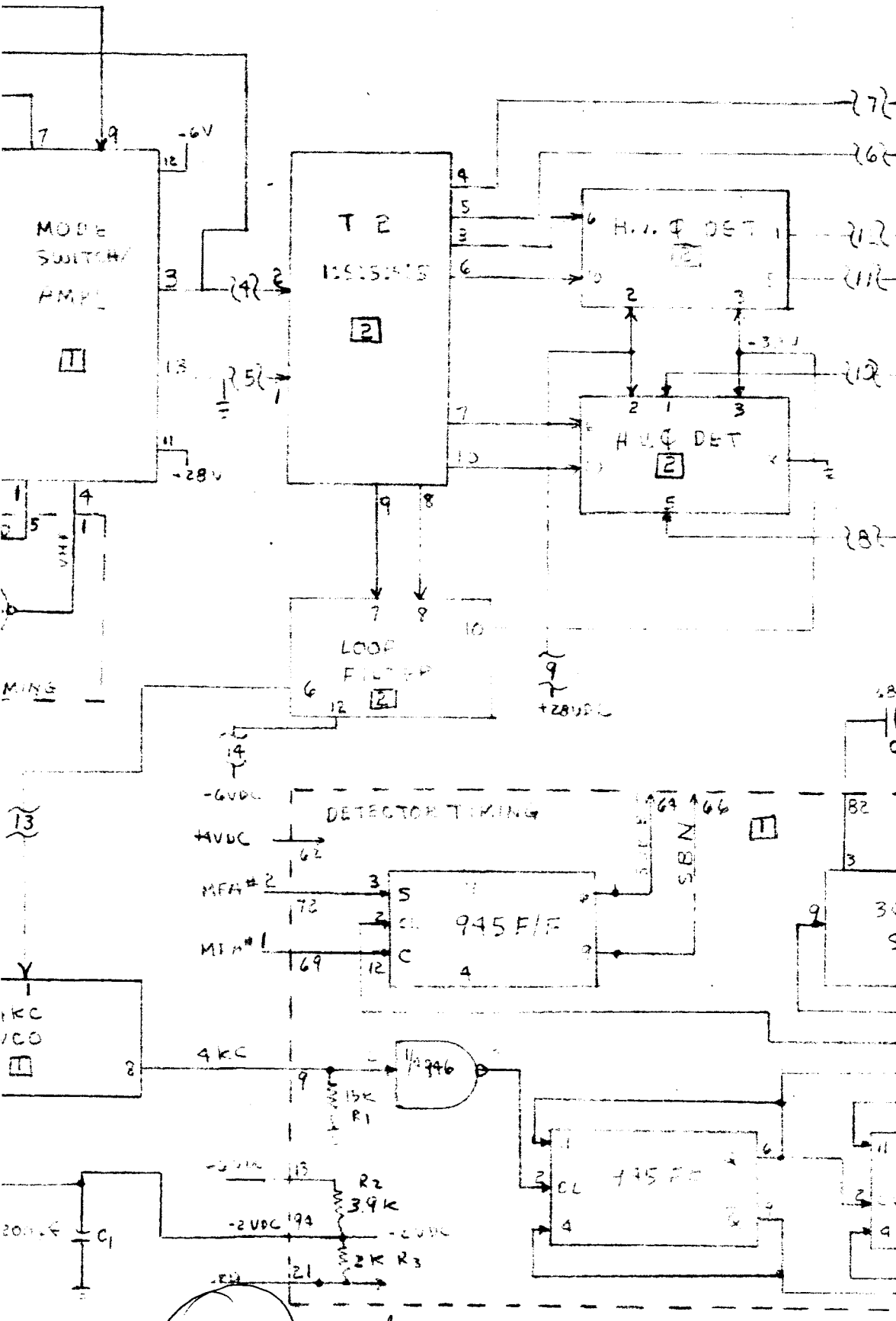
31 MAR 65

A4-12

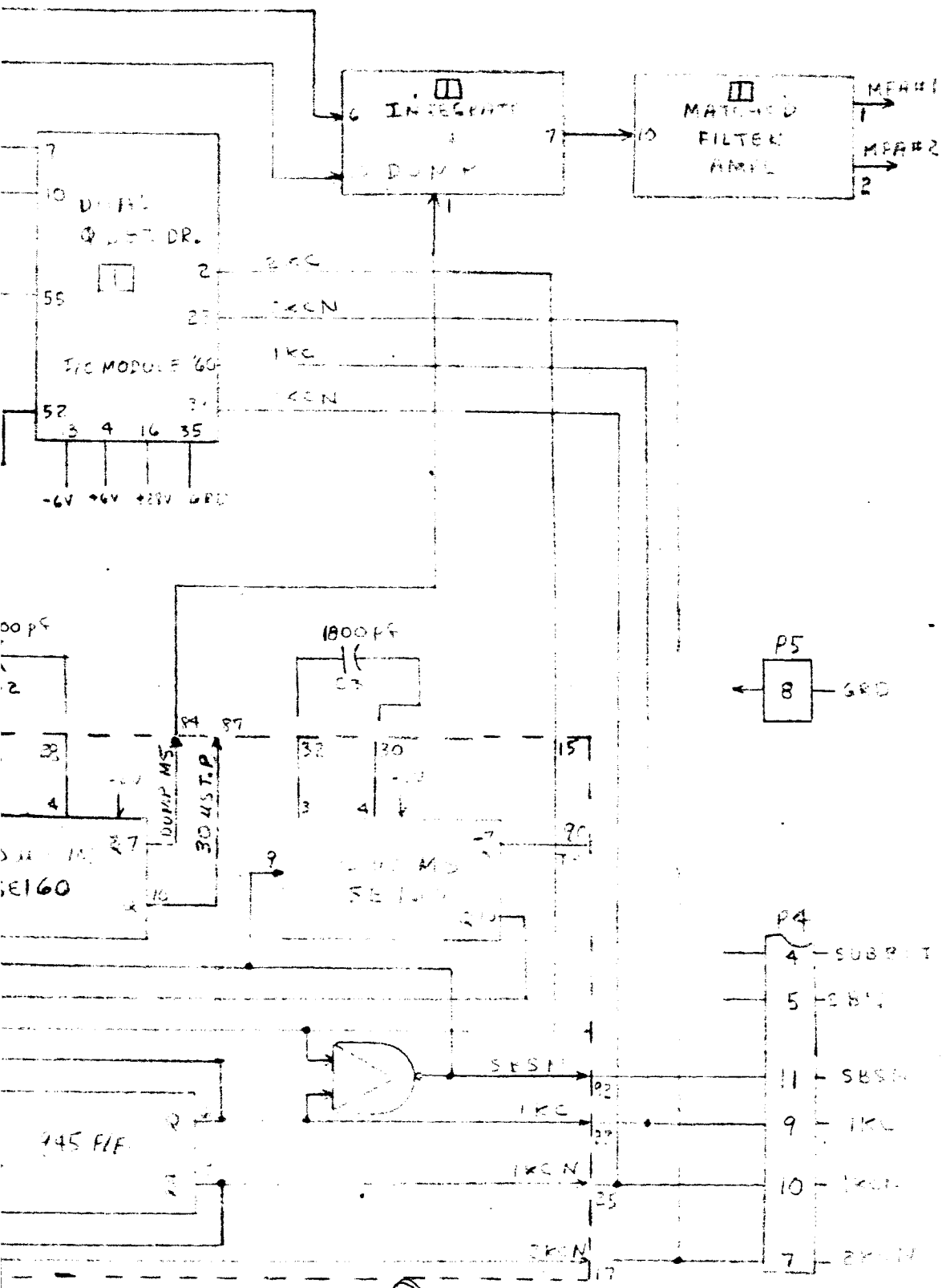


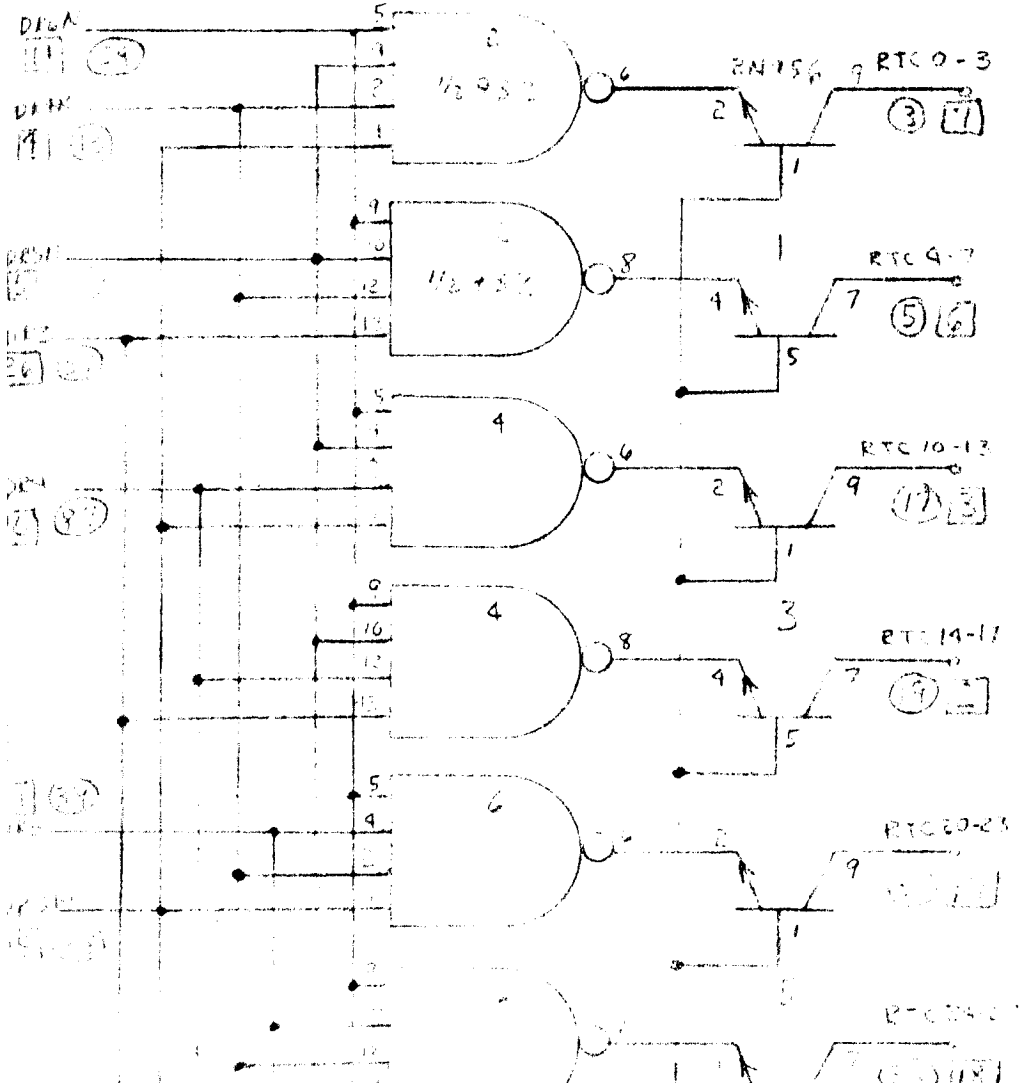
PHASE DETECTOR
P/O SUB-BIT


P4
UHF AUDIO
25
EMERGENCY AUDIO
17
UHF CAP -
19
T1
1:1
1
2
3
4
UHF RTN
UHF SGNL
13
22
S-BAND AUDIO
18
S-BAND RTN
20
+4
24
33K
S-BAND
6
7
UHF
21
MODE SWITCH
P10 DET. T
-6VDC
16
+28VDC
24
+6VDC
26
-2VDC
12
TEST
+9VDC
3
GRD
8
+28V
2
P1
14

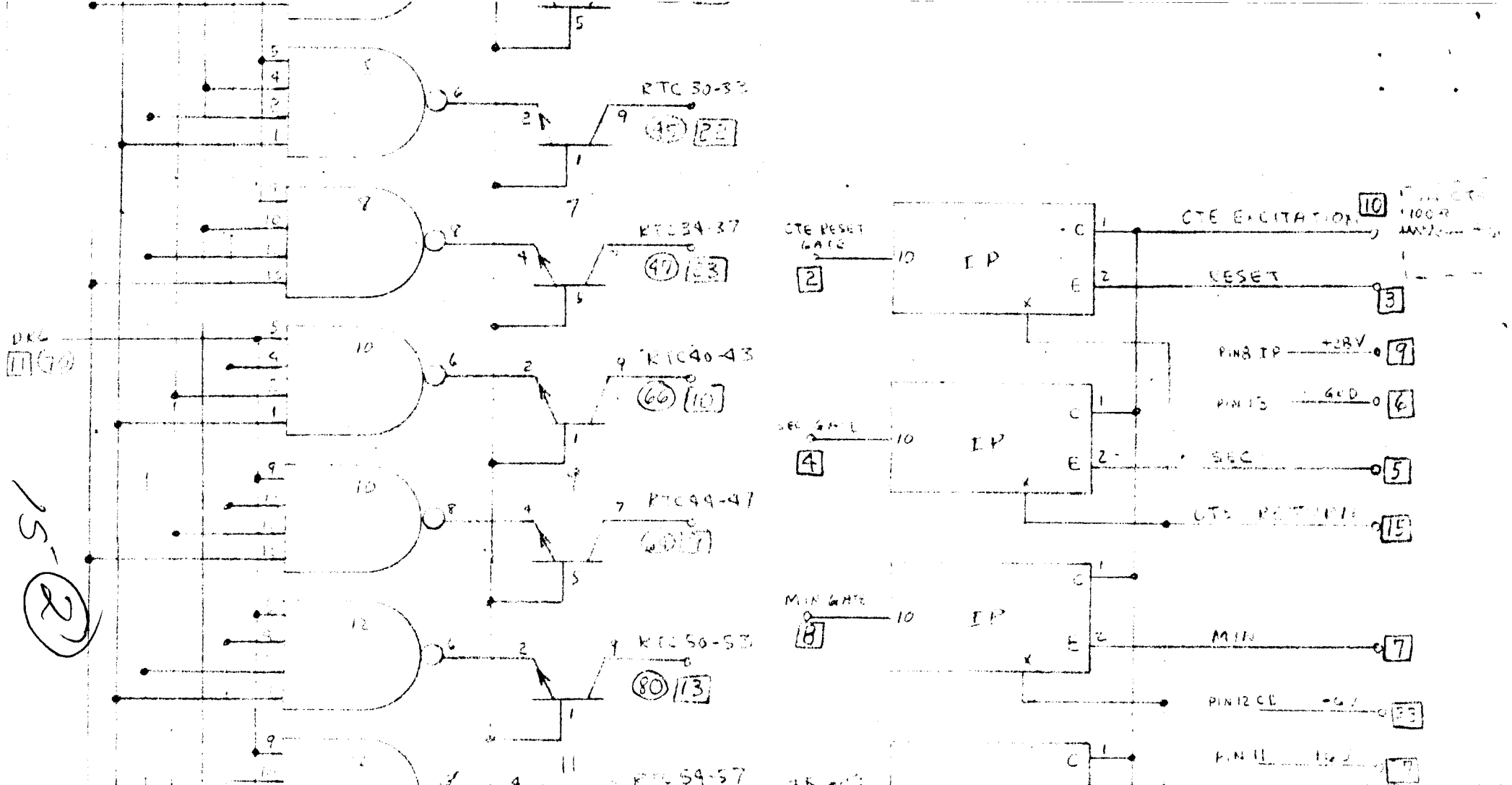

MODE SWITCH/ AMPL
T 2
H.V. F DET
H.V. C DET
LOOP
DETECTOR TIMING
945 F/F
946
4 KC
-6V
-28V
+28VDC
-6VDC
+4VDC
MEM#2
MEM#1
15K R1
R2 3.9K
2K R3
C1

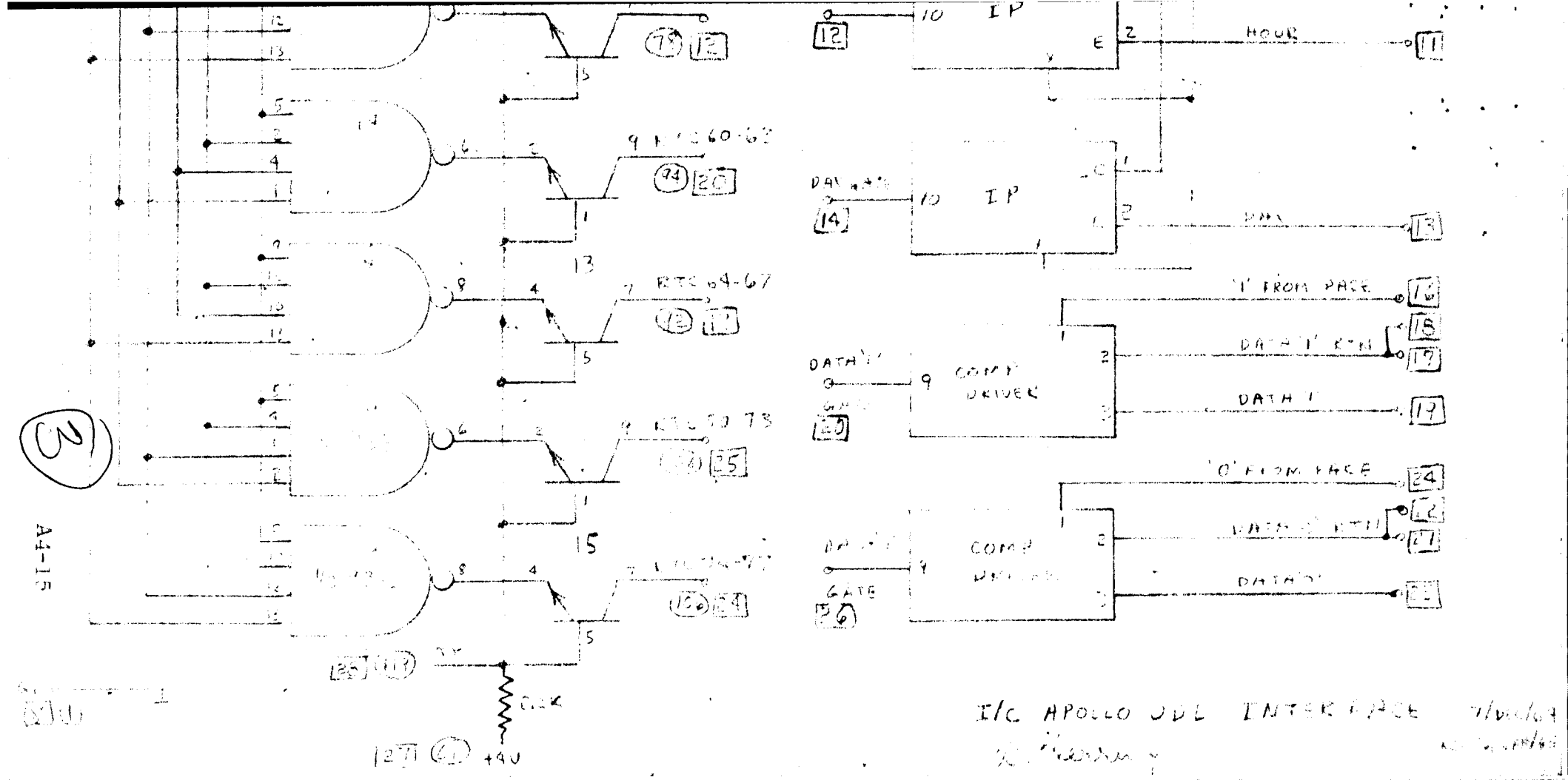
2 14

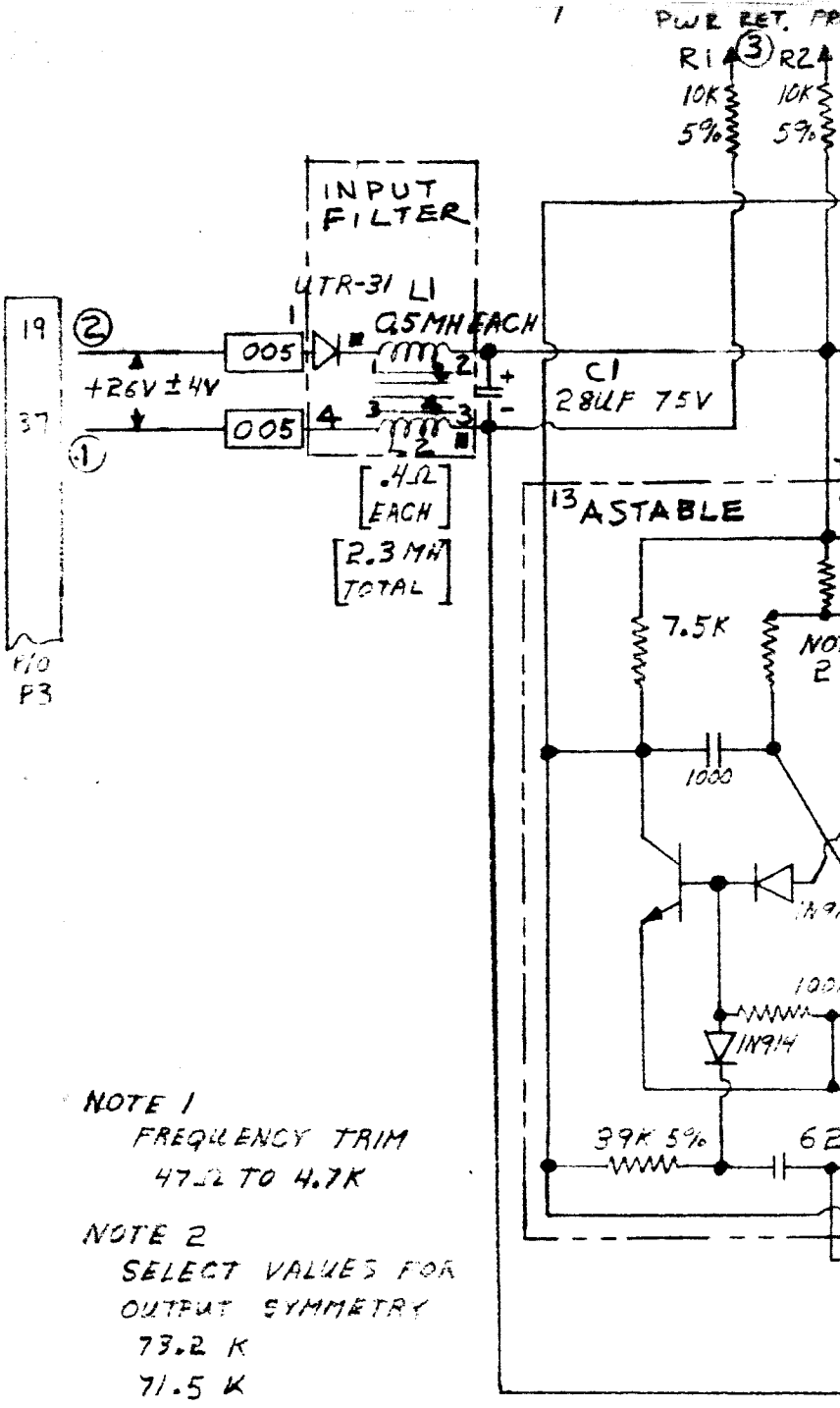

INTEGRATE
DUMP
MATCHED
FILTER
MFA#1
MFA#2
DIGITAL
DR.
I/C MODULE 160
-6V
+6V
+28V
GRD
1800PF
C3
P5
8
GRD
DUMP MS
30 MS T.P
SE160
145 F/F
P4
SBSY
IKC
IKCN
SBSYN



D-51


RTC 50-53
RTC 54-57
RTC 40-43
RTC 44-47
DRC
CTE RESET GATE
MIN GATE
SEC GATE
CTE EXCITATION
RESET
MIN
SEC
PIN 8 TP +28V
PIN 13 GND
PIN 12 CD
PIN 11
TP
C
E
X


IP
HOUR
IP
DAY
'1' FROM PACE
DATA '1' RTN
COMP DRIVER
DATA '1'
'0' FROM PACE
COMP
DATA '0'
GATE
+9V
(3)
A4-15

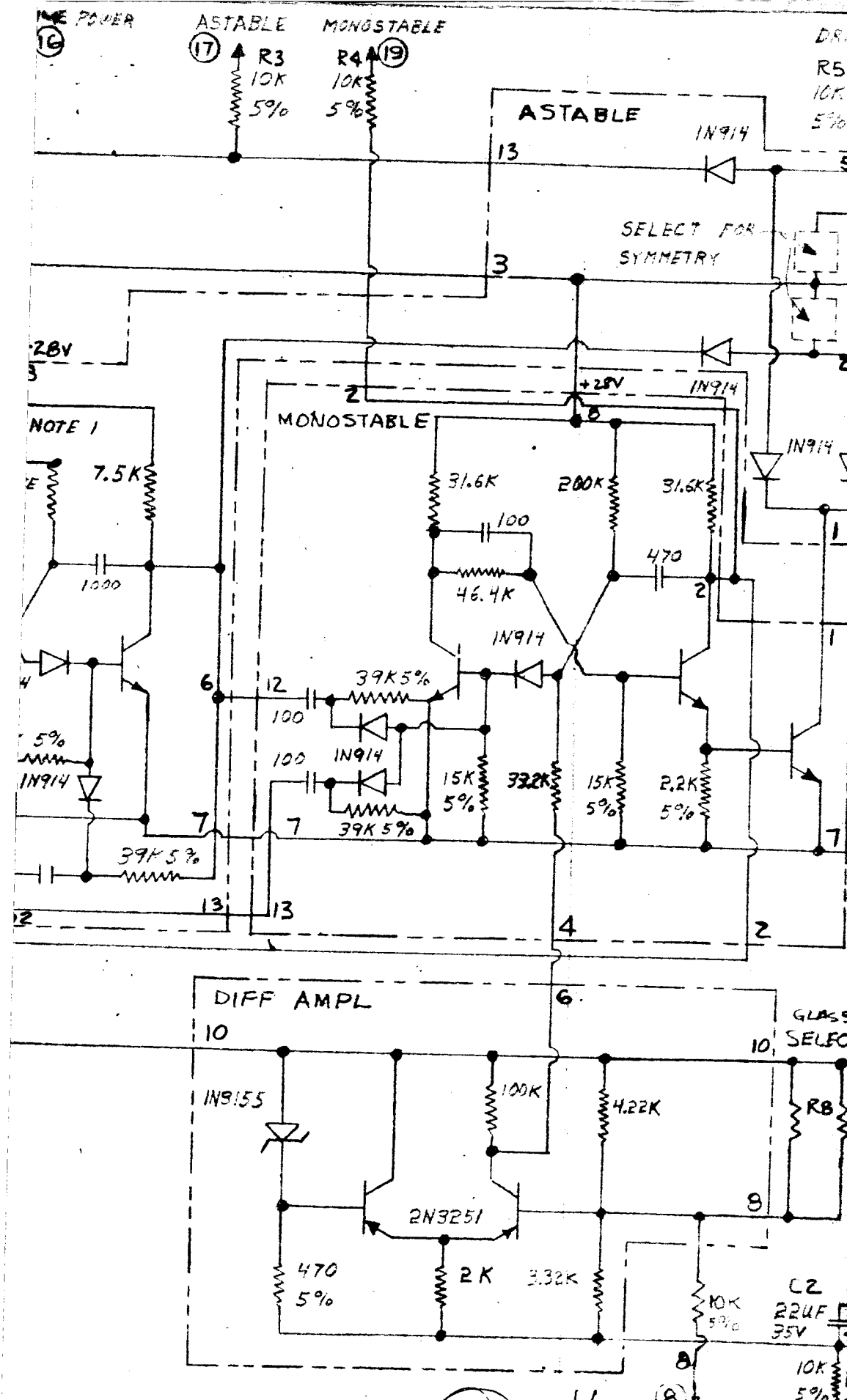


NOTE 1
FREQUENCY TRIM
47Ω TO 4.7K

NOTE 2
SELECT VALUES FOR
OUTPUT SYMMETRY
73.2 K
71.5 K
69.8 K
68.1 K

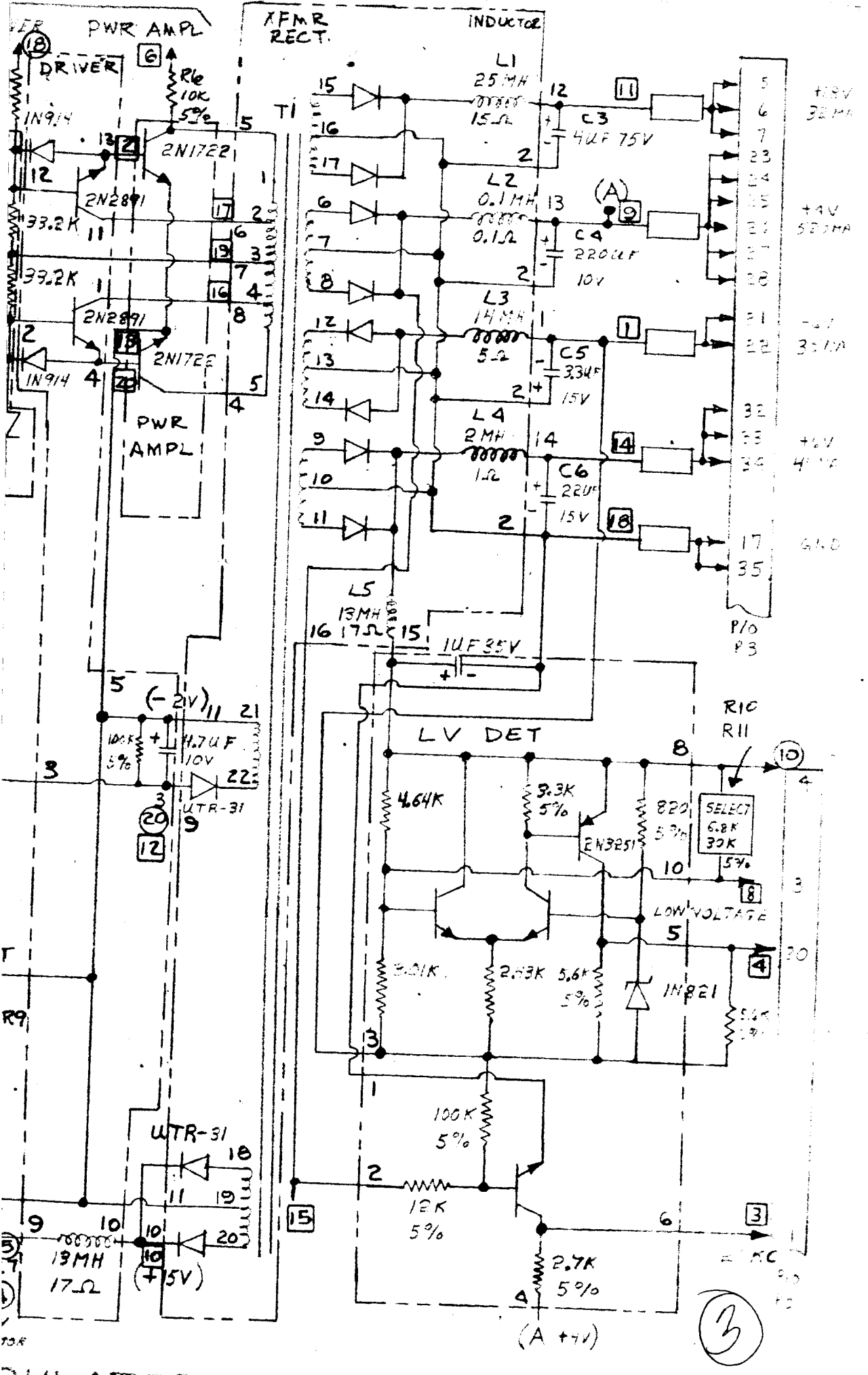
RESISTORS - TI-CG 1/8 W 1%
RESISTORS - 5% A-B 1/4W
CAPACITORS - CORNING GLASS (PF)
TRANSISTORS - 2N956
RECTIFIERS - UTR-31
FILTERS - ERIE 1200-005
- ERIE 1200-

160



2 16

APOLLO I/C VOLTAGE RE


PWR AMPL
DRIVER
R16
10K
5%
IN914
2N1722
2N2891
33.2K
2N2891
2N1722
IN914
PWR
AMPL
T1
XFMR
RECT.
INDUCTOR
L1
25 MH
15Ω
C3
4UF 75V
L2
0.1MH
0.1Ω
C4
220UF
10V
L3
1MH
5Ω
C5
3.3UF
15V
L4
2MH
1Ω
C6
22UF
15V
L5
13MH
17Ω
1UF 35V
+18V
32 MA
+4V
52 MA
-4V
35 MA
+6V
41 MA
GND
P/O
P3
(-2V)
10K
5%
4.7UF
10V
UTR-31
LV DET
R10
R11
4.64K
3.3K
5%
2N3251
820
5%
SELECT
6.8K
30K
5%
LOW VOLTAGE
3.01K
2.43K
5.6K
5%
IN821
5.6K
5%
100K
5%
12K
5%
2.7K
5%
(A +4V)
UTR-31
13MH
17Ω
(+15V)
R9
3

I/C UDL BASE WIRING ASSEMBLY WIRE LIST

Project 3030-1 Date

Location

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	P8		4	DR4N	P7		20
	P8		5	DR3N	P7		18
	P8		11	DR6	P7		15
	P8		14	DR6N	P7		16
	P8		15	DR3N	P7		25
	P8		16	DR4	P7		19
	P8		21	DR5	P7		17
	P8		26	DR3	P7		26
	P9		2	CTE Reset Gate	P6		25
	P9		4	SEC Gate	P6		17
	P9		8	Min Gate	P6		16
	P9		12	Hour Gate	P6		19
	P9		14	Day Gate	P6		18
	P9		20	Data '1' Gate	P7		24
	P9		26	Data '0' Gate	P7		23

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date _____

Location _____

Item	Connect Wire From Col. (Con)	Row	Pin	Signal	Connect Wire To Col. (Con)	Row	Pin
	P6		13	1KCN	P4		10
	P7		4	SB	P4		4
	P7		5	1KC	P4		9
	P7		6	SBN	P4		5
	P7		7	SKCN	P4		7
	P7		4	SBSN	TB1		23
	P7		10		P4		11
	P3		5	+28 VDC	P4		24
	P3		6	+28 VDC	P7		9
	P3		7	+28 VDC	P9		9
	P3		11	Prime Pwr	TB1		16
	P3		12	Prime Pwr	TB1		19
	P3		17	Signal Grd.	Term. Strip		
	P3		19	+28 VDC In.	P1		101
	P3		20	Lo Volt Det	P6		28
	P3		21	-6 VDC	P4		16

SPECIAL INSTRUCTIONS

Indicates two wires at one connection

Signal ground term strip on connector P5 pins 8 to 15.

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date _____

Location _____

Item	Connect Wire From Col. (Con)	Row	Pin	Signal	Connect Wire To Col. (Con)	Row	Pin
	P3		22	-6 VDC	P9		23
	P3		23	+4 VDC	TB1		1,2,3
	P3		24	+4 VDC	P4		3
	P3		25	+4 VDC	P6		2
	P3		26	+4 VDC	P7		29
	P3		27	+4 VDC	P8		27
	P3		32	+6 VDC	P4		26
	P3		33	+6 VDC	P7		8
	P3		34	+6 VDC	P9		27
	P3		35	Sig Grd	P1		53
	P3		37	+28 V in, Rtn	P1		100
	P1		100	+28 V in, Rtn	P1		99
	P1		99	+28 V in, Rtn	P1		98
	P3		1	20 KCN	P6		27

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date

Location

Item	Connect Wire From Col. (Con)	Row	Pin	Signal	Connect Wire To Col. (Con)	Row	Pin
	XFMR1		1	UHF CAP -	P4		19
	XFMR1		2	UHF Audio R	P1		82
	XFMR1		3	UHF Signal	P4		13
	XFMR1		4	UHF Sig Rtn	P4		22
	J2		1	Sig. Grd	Term Strip		
	TB1		8	T1,3	P1		88
	P1		88	T1,3	P6		21
	TB1		5	T2	P1		89
	P1		89	T2	P6		23
	TB1		6	T4,5	P1		90
	P1		90	T4,5	P6		22
	TB1		9	T6	P1		91
	P1		91	T6	P6		20
	TB1		15	T7,8	P1		92
	P1		92	T7,8	P6		24

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Page _____

Location _____

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	TB1		18	Comp Data '1'	P1		40
	P1		40	Comp Data '1'	P9		19
	TB1		21	Data '1' Rtn	P1		41
	P1		41	Data '1' Rtn	P9		17
	TB1		24	Comp Data '0'	P1		42
	P1		42	Comp Data '0'	P9		25
	TB1		17	Data '0' Rtn	P1		43
	P1		43	Data '0' Rtn	P9		21
	TB1		27	Chassis Grd	Ground Term		
	TB1		14	CTE Reset	P1		32
	P1		32	CTE Reset	P9		3
	TB1		4	CTE Excit	P1		56
	P1		56	CTE Excit	P9		10
	TB1		7	CTE Days	P1		36
	P1		36	CTE Days	P9		13

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1

Date _____

Location _____

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	TB1		11	CTE Hours	P1		35
	P1		35	CTE Hours	P9		11
	TB1		10	CTE Min.	P1		34
	P1		34	CTE Min.	P9		7
	TB1		13	CTE Sec.	P1		33
	P1		33	CTE Sec	P9		5
	TB1		22	UHF Audio	XFMR1		3
	TB1		25	S-Band Audio	P1		83
	P1		83	S-Band Audio	P4		18
	TB1		26	S-Band Audio (Emerg)	P1		69
	P1		69	S-Band Audio (Emerg)	P4		17
	TB1		3	TLM Norm Pwr	P1		68
	P1		1	RTC SEL 0-3	P8		8
	P1		2	RTC SEL 4-7	P8		6
	P1		3	RTC SEL 10-13	P8		3

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date _____

Location _____

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	P1		4	RTC SEL 14-17	P8		2
	P1		5	RTC SEL 20-23	P8		17
	P1		6	RTC SEL 24-27	P8		18
	P1		7	RTC SEL 30-33	P8		22
	P1		8	RTC SEL 34-37	P8		23
	P1		9	RTC SEL 40-43	P8		10
	P1		10	RTC SEL 44-47	P8		9
	P1		11	RTC SEL 50-53	P8		13
	P1		12	RTC SEL 54-57	P8		12
	P1		13	RTC SEL 60-63	P8		20
	P1		14	RTC SEL 64-67	P8		19
	P1		15	RTC SEL 70-73	P8		25
	P1		16	RTC SEL 74-77	P8		24
	P1		18	RTC RES 0 & 4	P7		11
	P1		19	RTC SET 1 & 5	P7		13

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date _____

Location _____

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	P1		20	A0	P6		6
	P1		21	A1	P6		5
	P1		22	A2	P6		4
	P1		23	A3	P6		3
	P1		24	A4	P6		7
	P1		25	A5	P6		8
	P1		26	A6	P6		11
	P1		27	A7	P6		10
	P1		28	V	P7		3
	P1		29	Reset	P7		2
	P1		30	Preset 1	P7		22
	P1		31	Preset 0	P7		21
	P1		38	RTC RES 2 & 6	P7		12
	P1		39	RTC SET 3 & 7	P7		14

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1 Date _____

Location _____

Item	Connect Wire From Col. (Con)	Row	Pin	Signal	Connect Wire To Col. (Con)	Row	Pin
	P1		44	Pace '1'	P9		16
	P1		45	Pace '1' Rtn	P9		18
	P1		46	Pace '0'	P9		24
	P1		47	Pace '0' Rtn	P9		22
	P1		51	UTEL SW	P6		26
	P1		52	UTEL SW Rtn Sig Grd	Term Strip		
	P1		55	CTE Rtn	P9		15
	P1		62	Chassis Grd	P1		63
	P1		63	Chassis Grd	P1		64
	P1		64	Chassis Grd	P1		65
	P1		65	Chassis Grd	P1		66
	P1		66	Chassis Grd	P1		67
	P1		67	Chassis Grd	Ground Term		
	P1		84	S-Band Audio R.	P4		20
	P1		86	Mode Switch	P4		6

SPECIAL INSTRUCTIONS

I/C UDL BASE WIRING ASSEMBLY WIRE LIST (cont)

Project 3030-1

Date _____

Location _____

Item	Connect Wire From			Signal	Connect Wire To		
	Col. (Con)	Row	Pin		Col. (Con)	Row	Pin
	P1		87	Mode Sw. Rtn	P4		21
	P1		93	Telem Rtn (Sig Grd)	Term Strip		
	P1		81	UHF Audio	P4		25
	P4		8	Sig Grd	Term Strip		
	P5		8	Sig Grd	Term Strip		
	P6		9	Sig Grd	Term Strip		
	P7		28	Sig Grd	Term Strip		
	P8		7	Sig Grd	Term Strip		
	P9		6	Sig Grd	Term Strip		

SPECIAL INSTRUCTIONS

P3

Pin	Signal
19	INPUT
18	—
17	SIG GRD
16	—
15	—
14	—
13	+15V
12	P.PWR RTN
11	P.PWR
10	ASMV
9	DRIVER
8	MSMV
7	+28V
6	+28V
5	+28V
4	LOW VOLTS
3	TRIM
2	PWR AMP
1	20KC
37	INPUT RTN
36	—
35	SIG GRD
34	+6V
33	+6V
32	+6V
31	—
30	—
29	VOLT TRIM
28	+4V
27	+4V
26	+4V
25	+4V
24	+4V
23	+4V
22	-6V
21	-6V
20	LOW VOLTS

P4

Pin	Signal
1	—
2	—
3	+4V
4	SB
5	SBN
6	MODE SW
7	2KCN
8	SIG GRD
9	1KC
10	1KCN
11	SBSN
12	-2V
13	UHF SIG
14	—
15	—
16	-6V
17	EM.AUD.
18	S-B
19	UHF CAP
20	S-B GRD
21	MS GRD
22	GRD
23	—
24	+28V
25	UHF AUD
26	+6V
27	—
28	—
29	—
30	—

P5

BLUE

Pin	Signal
8	SIG.GRD

P6

Pin	Signal
1	+4V
2	A3
3	A2
4	A1
5	A0
6	A4
7	A5
8	GRD
9	A7
10	A6
11	—
12	1KCN
13	—
14	—
15	MIN
16	SEC
17	DAYS
18	HRS
19	T6
20	T1,T3
21	T4,T5
22	T2
23	T7,T8
24	CTE R.
25	UTEL SW
26	20KC
27	LOW VOLTS
28	T.P. RESET
29	—

P7

WHITE

Pin	Signal
30	+4V
29	GRD
28	—
27	DR3G
26	$\overline{DR3G}$
25	COMP'1'
24	COMP'0'
23	DRS
22	DRC
21	$\overline{DR4}$
20	DR4
19	$\overline{DR5}$
18	DR5
17	$\overline{DR6}$
16	DR6
15	SET 2
14	SET 1
13	RESET 2
12	RESET 1
11	SBSN
10	+28V
9	+6V
8	2KCN
7	SBN
6	1KC
5	SB
4	V
3	RESET
2	—

P8

Pin	Signal
1	RTC 14-17
2	RTC 10-13
3	DR4N
4	DR5N
5	RTC 4-7
6	RTC 0-3
7	GRD
8	RTC 40-43
9	RTC 44-47
10	RTC 54-57
11	DR6
12	DR6N
13	RTC 50-53
14	DR4
15	DR3N
16	RTC 24-27
17	RTC 20-23
18	RTC 60-63
19	RTC 64-67
20	RTC 30-33
21	DR5
22	RTC 74-77
23	RTC 34-37
24	DR3
25	RTC 70-73
26	+4VDC
27	—
28	—
29	—

P9

RED

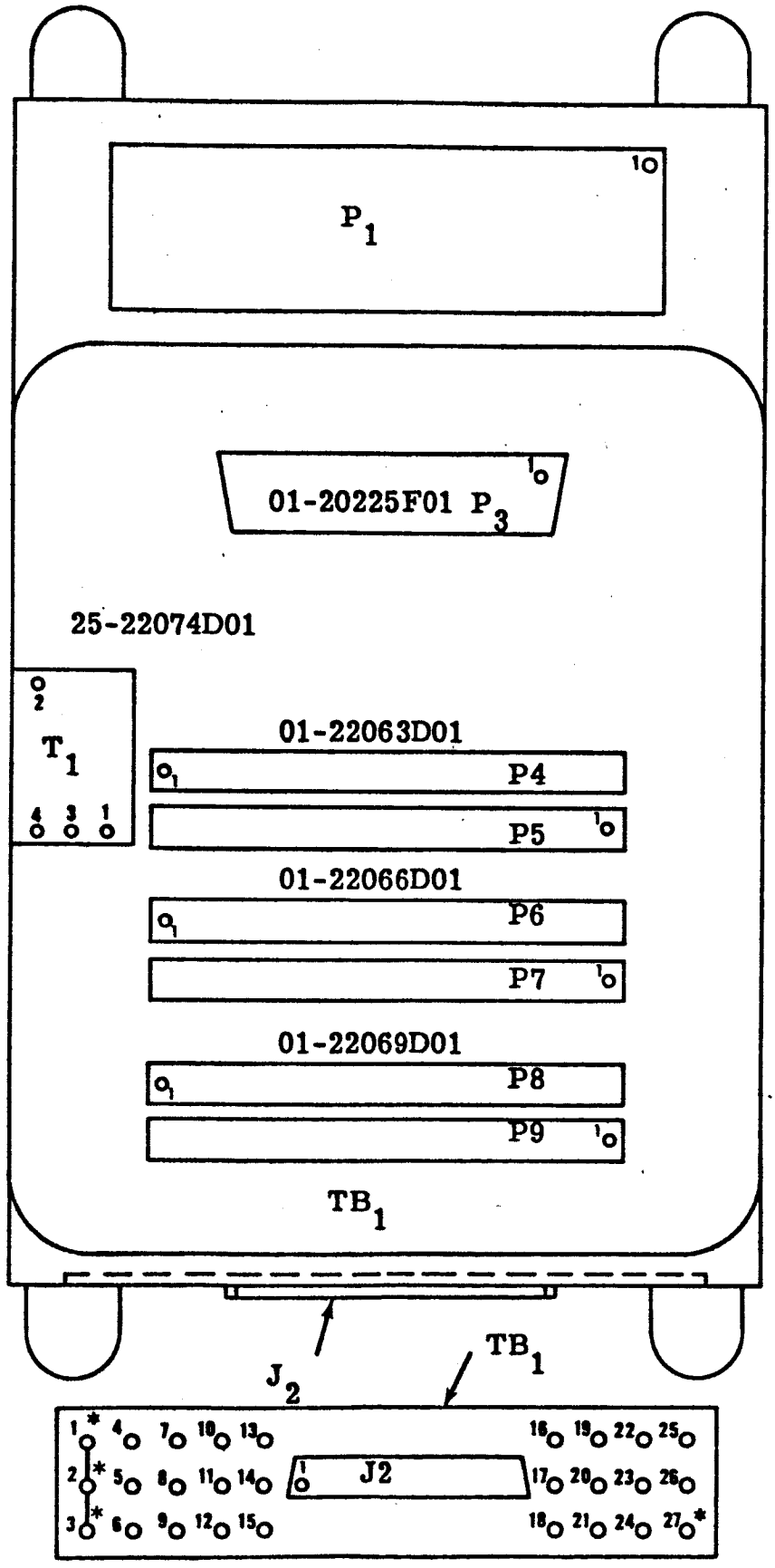
Pin	Signal
30	—
29	—
28	+6VDC
27	'O' GATE
26	DATA 'O'
25	PACE 'O'
24	-6VDC
23	'O' RTN
22	'O' RTN
21	'1' GATE
20	DATA '1'
19	'1' RTN
18	'1' RTN
17	PACE '1'
16	CTE RTN
15	DAY GATE
14	DAYS
13	HR GATE
12	HOURS
11	CTE EV.
10	+28VDC
9	MIN GATE
8	MIN.
7	GRD
6	SEC
5	SEC GATE
4	CTE RESET
3	RESET GATE
2	—

P2

Pin	Signal
20	—
21	—
22	—
23	CTE RESET
24	CTE EXC.
25	CTE DAYS
26	CTE HRS
27	CTE MIN
28	CTE SEC
29	—
30	CH GRD
31	+28V IN
32	+28V RTN
33	UHF AUD
34	S-BAND AUDIO
35	EM AUD
36	SUB BITS
37	CH.GRD
1	GRD
2	+4V
3	T1,3
4	T2
5	T4,5
6	T6
7	T7,8
8	—
9	—
10	—
11	—
12	DATA '1'
13	'1' RTN
14	DATA 'O'
15	'O' RTN
16	CH GRD
17	—
18	CH.GRD
19	—

APOLLO I/C UDL PIN CONNECTION DIAGRAM

6-30-65



5318-1

Chassis Diagram

I/C UDL ADAPTER DRAWER TEST POINT LIST

FROM	TEST POINT	REMARKS
J2-1	TP1	UDL Signal Ground
2	TP2	TLM Normalized PWR. T.P.
3	TP3	Validity Bit 1 and 3 T.P.
4	TP4	Validity Bit 2 T.P.
5	TP5	Validity Bit 4 and 5 T.P.
6	TP6	Validity Bit 6 T.P.
7	TP7	Validity Bit 7 and 8 T.P.
10	TP8	Rcvr. Sig. Strength (No. Conn.)
11	TP9	Rcvr. Sig. Strength RTN (No. Conn.)
12	TP10	Apollo Guid. Comp. Data 1 T.P.
13	TP11	Apollo Guid. Comp. Data 1 RTN T.P.
14	TP12	Apollo Guid. Comp. Data 0 T.P.
15	TP13	Apollo Guid. Comp. Data 0 RTN T.P.
16	TP14	Box Ident - Chassis GRD.
18	TP15	Box Ident - Chassis GRD.
22	TP16	Box Ident - Open
23	TP17	CTE Reset T.P.
24	TP18	CTE Excitation T.P.
25	TP19	CTE Days T.P.
26	TP20	CTE Hours T.P.
27	TP21	CTE Minutes T.P.
28	TP22	CTE Seconds T.P.
29	TP23	Box Ident - Open
30	TP24	Box Ident - Chassis GRD.
31	TP25	Prime Power (+28 VDC) T.P.
32	TP26	Prime Power RTN T.P.
33	TP27	UHF Audio T.P.
34	TP28	S-Band Audio T.P.
35	TP29	Sub-Bit Detector Audio T.P.
36	TP30	Sub-Bits T.P.

FROM	TEST POINT	REMARKS
J8-8	TP31	RTC Selection 0 - 3
J9-21	TP32	Data "0" RTN
J9-25	TP33	Data "0"
J9-17	TP34	Data "1" RTN
J9-19	TP35	Data "1"
J6-26	TP36	UTEL Switch
J9-10	TP37	CTE Excitation
J9-13	TP38	CTE Days
J9-11	TP39	CTE Hours
J9-7	TP40	CTE Minutes
J9-5	TP41	CTE Seconds
J9-3	TP42	CTE Reset
J7-11	TP43	Reset X0 and X4
J6-10	TP44	A7
J6-7	TP45	A4
J6-11	TP46	A6
J6-8	TP47	A5
J7-15	TP48	DR6
J7-17	TP49	DR5
J7-19	TP50	DR4
J7-26	TP51	DR3
J7-3	TP52	V
J7-2	TP53	Reset
J6-3	TP54	A3
J6-4	TP55	A2
J6-5	TP56	A1
J6-6	TP57	A0
J6-24	TP58	T7,8
J6-20	TP59	T6
J6-21	TP60	T1
J6-22	TP61	T4,5
J6-23	TP62	T2
J7-22	TP63	DRS

FROM	TEST POINT	REMARKS
J7-21	TP64	DRC
J4-11	TP65	SBSN
J4-6	TP66	Mode Switch
J4-9	TP67	1 KC
J4-7	TP68	2 KC N
J4-4	TP69	Sub-Bits
J4-18	TP70	S-Band Audio
XFMR-P3	TP71	UHF Signal
XFMR-P2	TP72	UHF Audio RTN
J4-17	TP73	Emergency Audio
J4-19	TP74	UHF Cap.
J4-25	TP75	UHF Audio
J4-8	TP76	Signal Ground
J3-11	TP77	Prime Power T.P.
J3-12	TP78	Prime Power RTN T.P.
J3-20	TP79	Low Voltage Det.
J3-29	TP80	Voltage Trim (Diff. Amp.) T.P.
J3-13	TP81	+15 VDC T.P.
J3-10	TP82	ASMV T.P.
J3-9	TP83	PWR Driver T.P.
J3-8	TP84	MSMV T.P.
J3-2	TP85	PWR AMP T.P.
J3-1	TP86	20 KC N
J3-28	TP87	+4 VDC
J3-32	TP88	+6 VDC
J3-22	TP89	-6 VDC
J3-5	TP90	+28 VDC
J3-25	TP91	Signal Ground
	TP92	-
	TP93	-
	TP94	-
	TP95	-
	TP96	-