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GUIDANCE, NAVIGATION AND CONTROL

E-2462

SIMFAM: DESCRIPTION AND OPERATION

by

John F. McKenna, Jr.

MARCH 1970

MIT

CHARLES STARK DRAPER

CAMBRIDGE MASSACHUSETTS 02139

LABORATORY

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GUIDANCE, NAVIGATION AND CONTROL

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E-2462

SIMFAM:
DESCRIPTION AND OPERATION

ABSTRACT

A fixed test memory for ground use with an Apollo Guidance Computer has been designed and fabricated. The unit, called SIMFAM, uses a Braid Memory with an adapter to operate via the AGC's rope connector, thus simulating operation with rope-memory modules.

This report contains a description of the SIMFAM unit and its operation.

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March 1970

DESCRIPTION AND OPERATION

1. INTRODUCTION

SIMFAM is a fixed ground test memory (FGTM) designed to operate with a Block II Apollo Guidance Computer via the rope connector. A SIMFAM unit (Fig. 1.1, 1.2, and 1.3) contains a Braid Memory, a Braid Adapter, power supplies, harnesses, and extenders for mating with the AGC.

The Braid Memory used is of the million-bit "Easy Boat" configuration and may contain single AGC programs of up to 36,864 sixteen-bit words.

The Braid Adapter interfaces with both the AGC and the Braid, deriving timing pulses and a 16-bit address from the AGC rope signals. The address and control pulses are applied to the Braid, and the Braid output word is stored and transmitted to the AGC fixed-memory sense amplifiers at the proper time through a transformer interface.

2. BRAID MEMORY

2.1 Description

The SIMFAM Braid Memory stores 589,824 bits arranged for parallel readout of 36,864 words of 16 bits each. The Braid accepts a 16-bit parallel address equivalent to the AGC'S fixed-memory address (FMA) and reads the contents of the location specified when a READ command occurs.

The SIMFAM Braid is of the "Easy Boat" configuration, and consists of an assembly of a "boat", a sense board, a core array, and an electronics section. The boat contains the potted braid bundle, wire terminations, and the diodes used for wire selection. The sense coils, sense amplifiers, sense group-selection circuitry, and an output register are mounted on the sense board which in turn is fastened to the completed boat. Ferrite cores (144 altogether) are inserted through the sense board and potted braid and capped with I-cores to form transformers at all sense positions.

The electronics section contains the word-line selection logic, word-line driving circuits, and a timing generator. The electronics section mates with the boat-core-sense board assembly to form a complete package measuring 15-7/8"x14-1/2"x2".

2.2 Organization

The SIMFAM Braid information field consists of an array of 144 sense positions (cores with sense windings and amplifiers) threaded by a word-line bundle of 4096 wires. A "one" is stored at the intersection of a given word line and sense position if the word line passes through the core at that sense position. When current is passed through a word line, a current is induced in the sense coils on all cores threaded by the word line. Hence, binary "ones" are represented electrically by current in the same windings, and "zeros" by the absence of coupled current.

A single word is read by passing current through a single word line and enabling a set of sixteen sense positions. Word-line selection is done with a double-ended selection system having 32 top switches (drivers), 128 bottom switches (receivers), and a diode in series with each word line (see Fig. 2.1). The receivers act as single-pole double-throw switches: all unselected receiver bundles are connected to +5Vdc, and the single selected bundle is connected to ground. An "off" driver acts as an open circuit, while an "on" driver presents a low impedance to current from the pulsed current source. When a single driver and receiver are selected, a current path is formed through a single word line.

Each receiver is a parallel connection of two SUHL 2-input NAND gates (Fig. 2.2a); each driver is a discrete circuit using one transistor and one resistor (Fig. 2.2b).

The sense circuit used is shown in Fig. 2.3. Transistor Q1 acts as an inhibiting switch by shunting the sense-coil output current to ground when "on". The sense position is enabled by turning Q1 "off" so that, if a coil output current appears (representing a "one"), Q2 will saturate.

The organization of the sensing circuitry is shown in Fig. 2.4. The collectors of all sensing transistors representing the same bit are wired together to perform the logical OR function. The output circuitry is completed by a pullup resistor and RTL Flip-Flop for each bit. Grounding any single "inhibit" line will enable 16 sense positions.

2.3 Braid Addressing

The address field and its segmentation for selection are illustrated in Fig. 2.5. Address bits A_0 to A_6 are used to select one of the 128 receivers; bits A_7 to A_{11} select one of the 32 drivers; and bits A_{12} to A_{15} select one of the 9 sense groups.

2.4 Timing and Pulse Circuits

The SIMFAM Braid Memory contains pulse-generating circuits to control the sequencing and timing of the operations necessary to perform the read function. The signals involved are shown in Fig. 2.6.

The current source (Fig. 2.7) provides drive-current pulses of controlled amplitude and risetime. A 1:4 transformer in the output lead provides a current pulse having the same shape as the drive-current pulse but one-fourth the amplitude; this current pulse is applied to a special wire threading all cores in a reverse direction to improve signal-to-noise ratio.

3. BRAID ADAPTER

The Braid Adapter collects address information from the signals appearing at the AGC rope connector, regenerates the Fixed-Memory Address (FMA) for presentation to the Braid Memory, and generates a READ signal when a fixed-memory cycle is being done. The word read from the Braid is held in a data register and gated to the AGC rope-sense amplifiers at the time they are being strobed.

The Adapter may be used in a manual mode to read the contents of a specified location in the Braid by setting an address in a front-panel switch bank and pressing a button. The manual mode is useful for check and test purposes.

The Braid Adapter electronics (with the exception of indicator drivers) occupies a single DGE (digital ground equipment) tray. Twelve of the twenty-four module positions are occupied by discrete-circuit modules, and twelve by T-headers containing 8 dual 3-input nor gates each. The module assignments are shown in Fig. 3.1 and the tray pin-numbering convention is shown in Fig. 3.2. The front panel layout appears in Fig. 3.3, and its operation is described in a later section.

3.1 Interfaces

The signals available at the AGC rope connector for determining address and timing are listed in Table 3.1. The driving circuits are of two types: current

sources that draw current to ground or +4Vdc from +14V when "on", and AND networks of PNP transistors whose output is a positive voltage when "on". When a selection function is "1", the corresponding driving circuit is "on".

The SIMFAM circuits for interfacing with these signals are shown in Fig. 3.4. The output of either the V or the I circuit is a positive voltage (1) when the selection function is "1".

The transformer output circuit for driving AGC sense amplifiers is illustrated in Fig. 3.5. A transmitted "1" is represented by a one-microsecond pulse of approximately 65mV amplitude.

3.2 Addressing

The appearance times of the various rope-select signals are shown in Fig. 3.6. FMA bits 1 to 7 are determined from the inhibit signals, and are available shortly after the inhibits appear; bit 8 is determined from the set-time resets; bit 9 from the set-time sets; and bits 10 to 16 are determined by strand and module functions, which are available at strand-gate time. Note that the FMA bits are numbered 1 to 16 (for compatibility with the AGC numbering), while the corresponding address bits in the Braid are numbered 0 to 15 (for convenience).

The following logical functions are performed in the conversion of rope-select functions; here FMA bits 1 to 16 are designated F_1 to F_{16} .

First, three special strand functions are generated for use in the decoding:

$$\begin{aligned}\phi_1 &= \text{STR01} + \text{STR02} + \text{STR03} + \text{STR04} \\ \phi_2 &= \text{STR05} + \text{STR06} + \text{STR07} + \text{STR08} \\ \phi_3 &= \text{STR09} + \text{STR10} + \text{STR11} + \text{STR12}\end{aligned}$$

Then

$$\begin{aligned}F_{16} &= (\phi_2 + \phi_3) \text{MODT2} \\ F_{15} &= \phi_3 \text{MODS1} + \text{MODS2} + \text{MODT1} + \phi_1 \text{MODT2} \\ F_{14} &= (\phi_2 + \phi_3) \text{MODR2} + (\phi_1 + \phi_2) \text{MODS1} + \text{MODT1} \\ &\quad + \phi_1 \text{MODT2} \\ F_{13} &= \phi_1 (\text{MODR2} + \text{MODS1} + \text{MODT2}) + \phi_2 (\text{MODS1} + \text{MODS2}) \\ &\quad + \phi_3 (\text{MODR1} + \text{MODS2} + \text{MODT1}) \\ F_{12} &= \phi_2 (\text{MODR1} + \text{MODS1} + \text{MODT1}) + (\phi_1 + \phi_3) (\text{MODR2} \\ &\quad + \text{MODS2} + \text{MODT2})\end{aligned}$$

$F_{11} = \text{STR03} + \text{STR04} + \text{STR07} + \text{STR08} + \text{STR11} + \text{STR12}$
 $F_{10} = \text{STR02} + \text{STR04} + \text{STR06} + \text{STR08} + \text{STR10} + \text{STR12}$
 $F_9 = \text{SETCD}$
 $F_8 = \text{XRSTAN} + \text{XRSTCN}$
 $F_7 = \text{X07FN}$
 $F_6 = \text{X06FN}$
 .
 .
 .
 $F_1 = \text{X01FN}$

4. SIMFAM OPERATION

4.1 Set Up

1. Connect AGC-SIMFAM cable to Braid Adapter "AGC" connector.
2. Remove AGC power.
3. Install six (6) dummy-rope modules (numbered B1 to B6) in correct positions in AGC baby tray, open sides facing tray A.
4. Connect six (6) connectors (numbered B1 to B6) at free end of AGC-SIMFAM cable to the corresponding dummy-rope modules.
5. Connect SIMFAM power cord to 115V, 60 Hz source.

4.2. Operate with AGC

1. Apply power to AGC and set SIMFAM power switch to "ON" (order not critical).
2. Set SIMFAM "AGC-MAN" switch to "AGC".

4.3. Manual-Mode Operation

1. Set "AGC-MAN" switch to "MAN". SIMFAM will then ignore AGC inputs and accept addresses from the front panel controls.
2. Set "BANK-FMA" switch to type of manual address selection desired. With the switch in the "FMA" position, the 16-bit FMA set into the address switch bank specifies the location to be read. With the switch in the "BANK" position, the 10 least-significant bits of the address switch bank have the same meaning as the 10 least-significant bits of the S register in the AGC, while the 6 higher-order switches are ignored; the six high-order address bits are determined from the settings of the "SREG", "BANK", and "FEXT" switches, all of which have the same meaning as the AGC registers whose name they carry. The FMA bits decoded from these switch settings are displayed in lamps located above the six inactive address switches.

3. Depress "CYCLE" button. The contents of the location specified will appear in the "DATA" register with the parity bit leftmost in the display and bit 1 rightmost.

NOTE: If SIMFAM is connected to the AGC in manual-mode operation, the AGC power must be on to provide +14V to the Braid's current driver. If SIMFAM is to be operated without connection to an AGC, +14 Vdc must be applied from an external power supply to pin 118 of the adapter's "AGC" connector.

5.0. NOTES ON ADDRESS CONVERSIONS

In the AGC, the unique fixed-memory address is determined from the settings of the S register, the FBANK register, and the Fixed Extension channel (FEXT); in octal program listings the address is specified by either "ADDR" (where $4000_8 \leq \text{ADDR} \leq 7777_8$), or "BANK, ADDR" (where $00_8 \leq \text{BANK} \leq 43_8$ and $2000_8 \leq \text{ADDR} \leq 3777_8$). The address presented to the Braid (the FMA) is a straightforward 16-bit binary number ($000000 \leq \text{FMA} \leq 107777_8$). An attempt is made here to present the manner of converting from one representation to another.

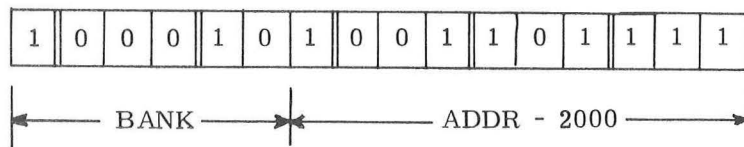
5.1. BANK, ADDR to and from FMA

The bank number (6 binary bits) occupies the 6 high-order bits of the FMA (F_{16} to F_{11}), and the low 10 bits of ADDR occupy the low 10 bits of the FMA (F_{10} to F_1). The most-significant bit of ADDR is taken care of in one of two ways, both of which have the same result: 1) subtract octal 2000 from ADDR, or 2) discard the most-significant bit of ADDR. Note that it is improper to prefix the octal ADDR by the octal bank number, because one octal digit of the FMA is formed by bits from both ADDR and BANK.

Example:

42,3157

is FMA 105157:



To convert a given FMA to the BANK, ADDR representation: write out the FMA in binary; the top 6 bits are the bank number, and ADDR is obtained by prefixing the bottom 10 bits of FMA by 1 (or by adding 2_{10}).

5.2. "ADDR" to and from FMA

If the contents of the S register (ADDR) are between octal 4000 and octal 7777, the address is in "fixed-fixed" memory, where the FMA is equal to ADDR.

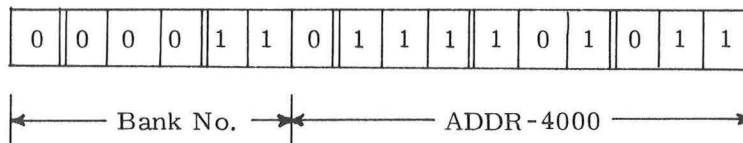
5.3. ADDR(FF) to and from "BANK, ADDR"

A "fixed-fixed" address (between 4000 and 7777) may, of course, be represented by "BANK, ADDR", where $2000 \leq \text{ADDR} \leq 3777$ and BANK is 02 or 03.

Example:

6753

is FMA 006753:



and may be written as 03,2753.

5.4 FEXT, FBANK, SREG to and from FMA

$$2000 \leq S \leq 7777$$

$$0 \leq \text{FEXT} \leq 7 \quad (\text{Note that FBANK is not necessarily equal to BANK.})$$

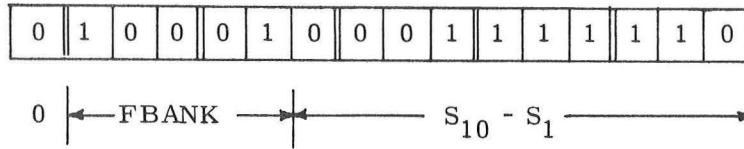
$$0 \leq \text{FBANK} \leq 37$$

- a. The ten low-order bits of the FMA are always equal to the 10 low-order bits of S.
- b. If $4000 \leq S \leq 7777$, fixed-fixed memory is specified, regardless of the contents of FEXT and FBANK, and the FMA is equal to S. The following cases assume $2000 \leq S \leq 3777$.
- c. If $0 \leq \text{FBANK} \leq 27$, the most-significant bit of the FMA (F_{16}) is zero, bits F_{15} through F_{11} are occupied by the number in FBANK, and bits F_{10} through F_1 are occupied by the 10 low-order bits of S:

Example:

FBANK = 21, S = 2176

is FMA 042176:



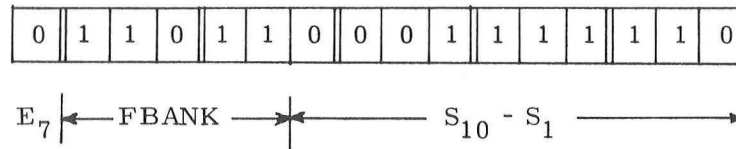
which may also be written 21,2176.

- d. If $30 < \text{FBANK} < 37$, then bit 16 of the FMA is no longer zero but is equal to the high-order bit (designated E_7) of the fixed extension channel FEXT. Bits F_{15} through F_{11} are equal to the number in FBANK if E_7 (hence F_{16}) is zero; if E_7 (hence F_{16}) is 1, subtract 30 (octal) from FBANK to obtain the number to be placed in bits F_{15} to F_{11} . (This rule does not apply if $\text{FEXT} > 4$.)

Example 1:

FBANK = 33, FEXT = 2, S = 2176

$E_7 = 0$, so $F_{16} = 0$.

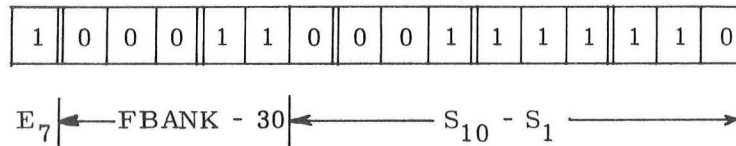


The FMA is 066176; it may also be written 33,2176.

Example 2:

FBANK = 33, FEXT = 4, S = 2176

$E_7 = 1$, so $F_{16} = 1$, and $(F_{15} \rightarrow F_{11}) = 33 - 30 = 3$



the FMA is 106176; the address may also be written 43,2176.

6. OPERATING MARGINS

Operation of SIMFAM has been verified at ambient temperatures from +15°C to + 55°C.

Permissible power-supply voltage variations are :

- + 3.3V (internal): $\pm 10\%$
- + 5.0V (internal): $\pm 10\%$
- + 14Vdc (from AGC): 12V to 17V.

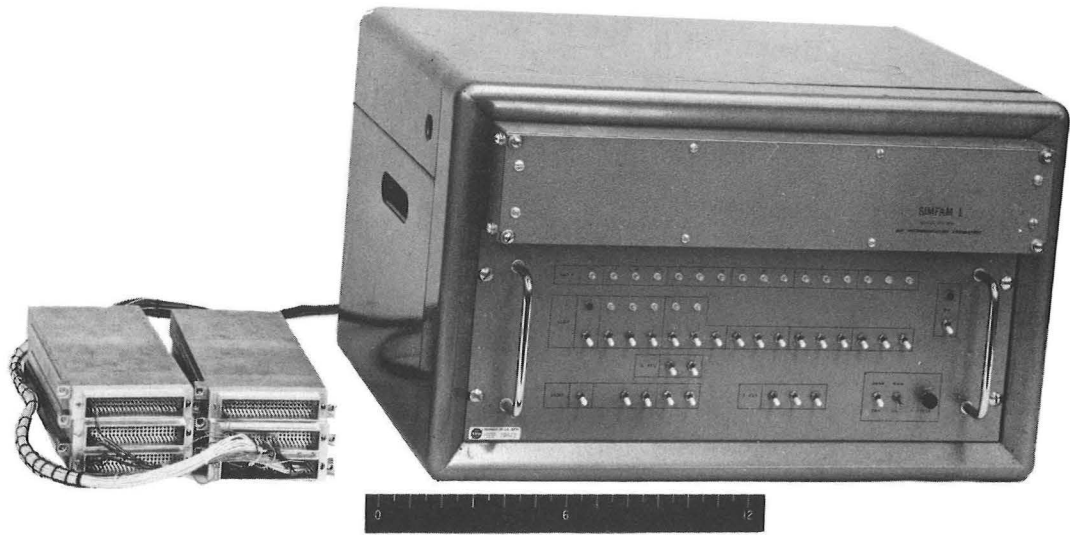


Fig. 1.1 SIMFAM assembly.

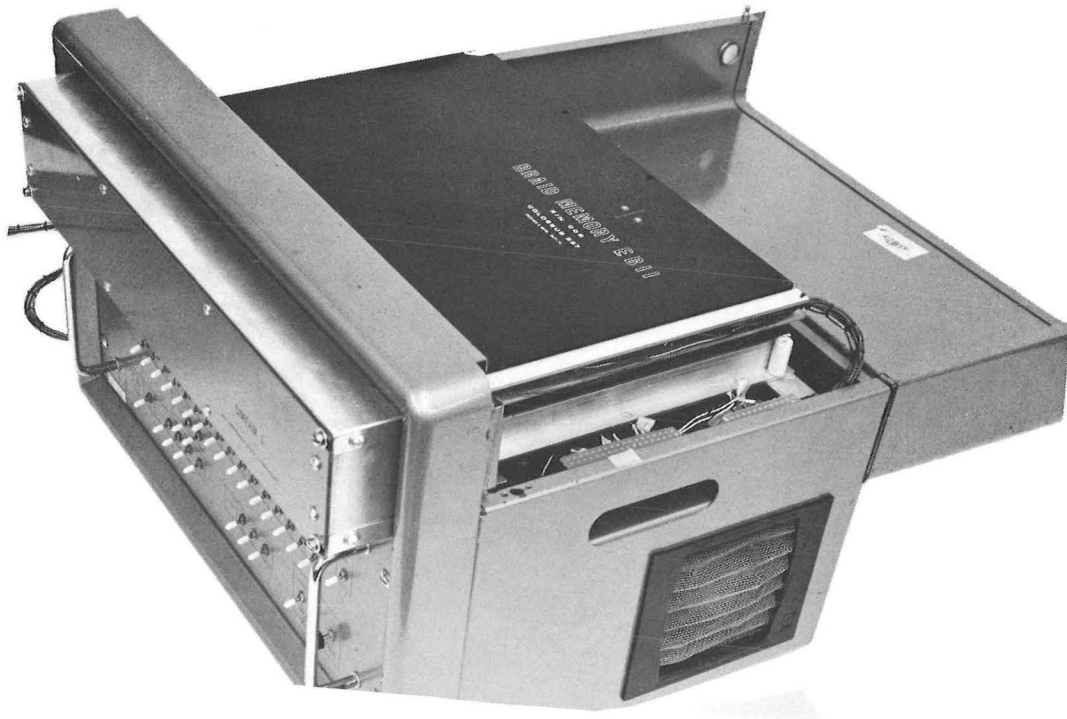


Fig. 1.2 SIMFAM showing braid memory installed.

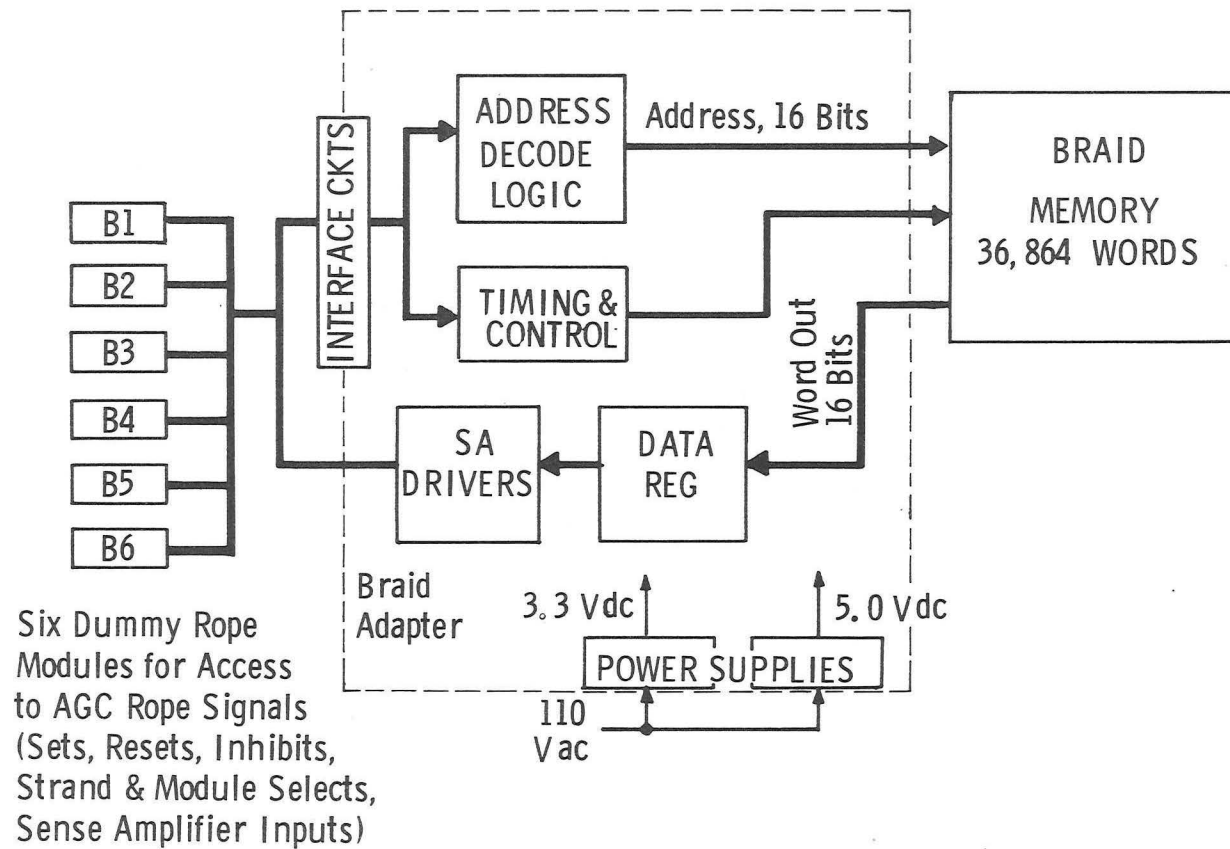


Fig. 1.3 SIMFAM organization.

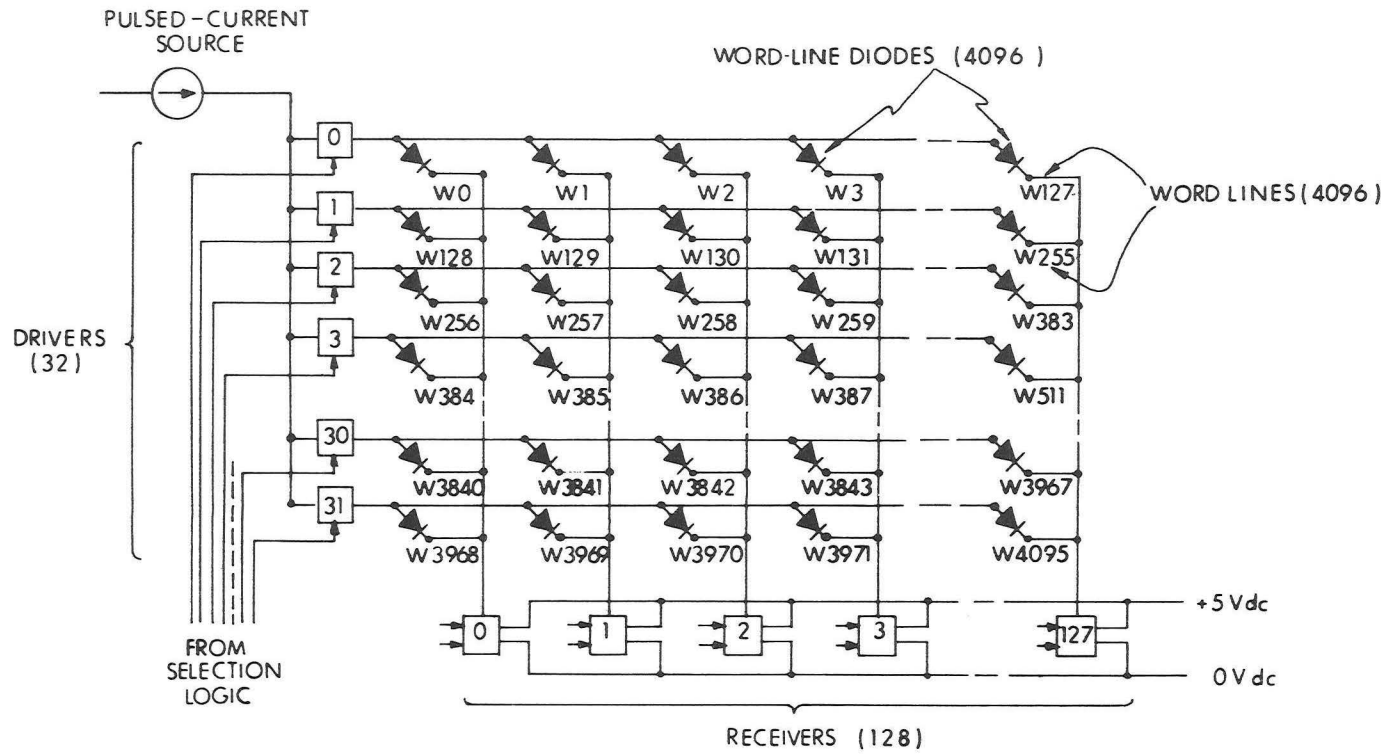


Fig. 2.1 Word-line selection.

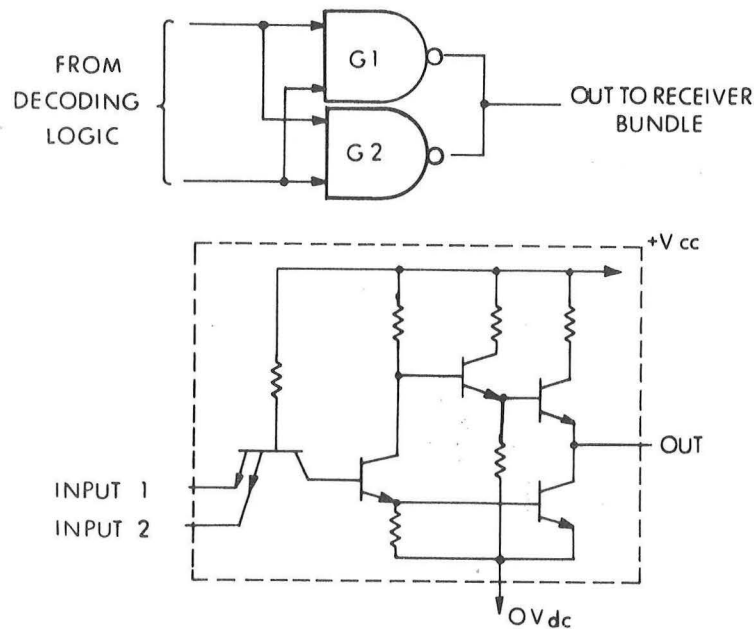


Fig. 2.2a Receiver (top) and equivalent circuit of single gate (bottom).

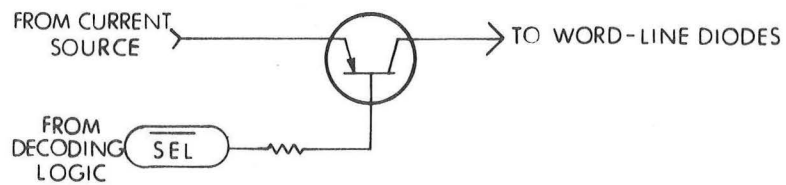
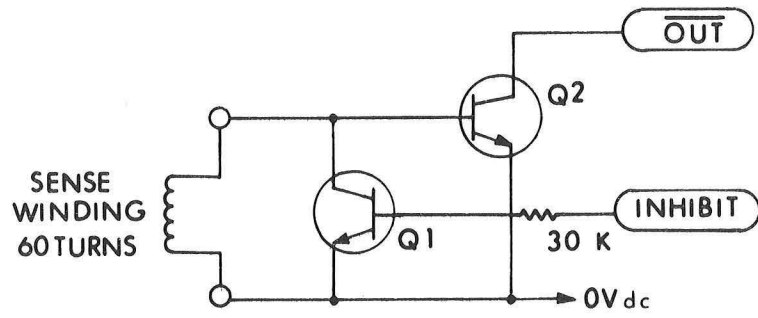


Fig. 2.2b Driver (transmitter) circuit.

SCHEMATIC



SYMBOL

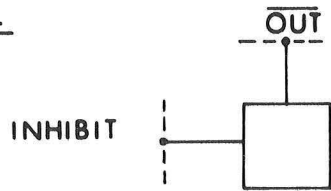


Fig. 2.3 Sense circuit.

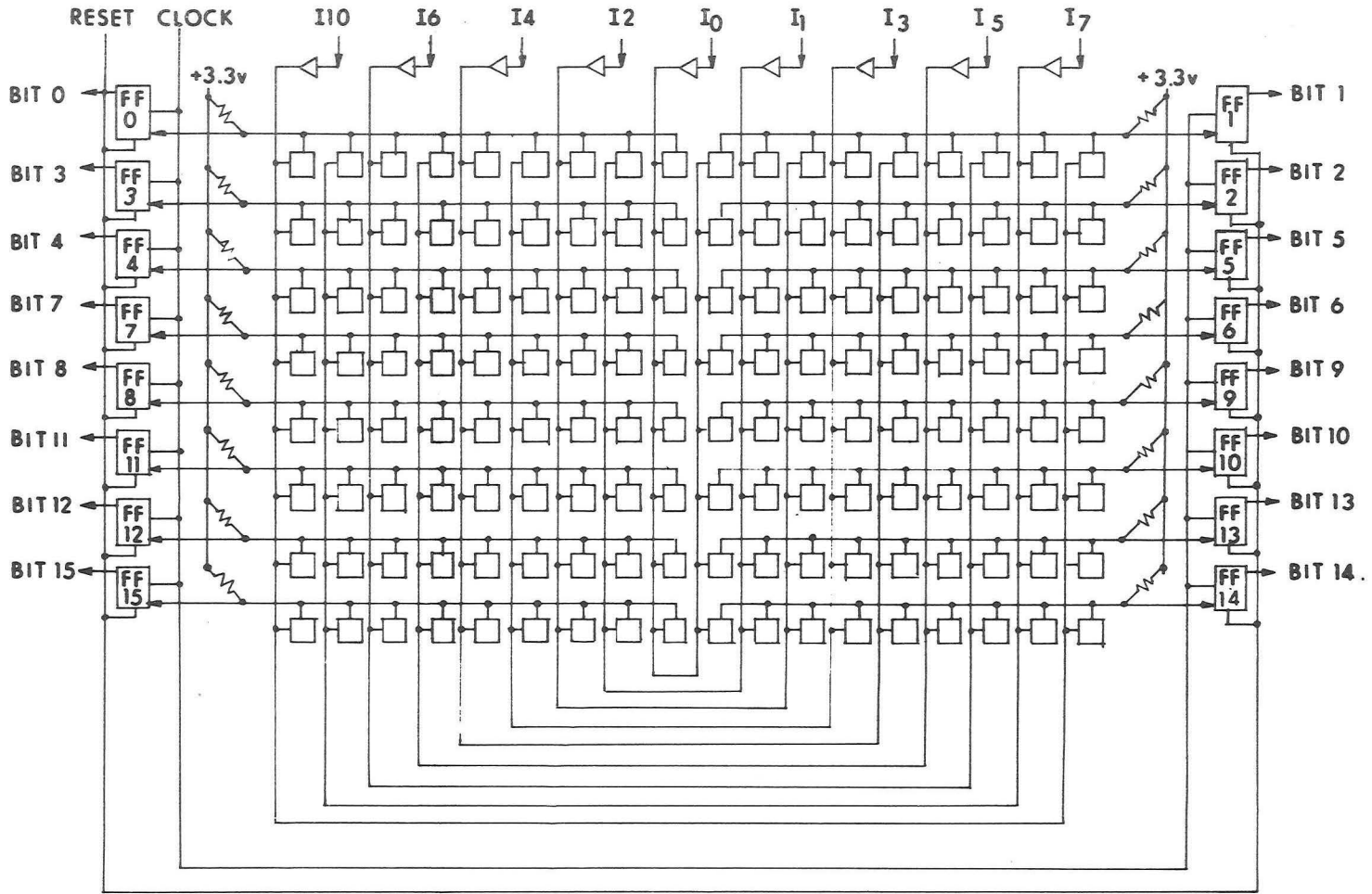
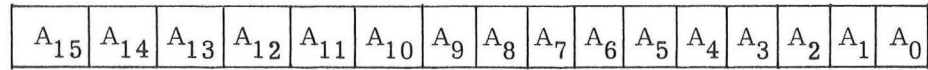
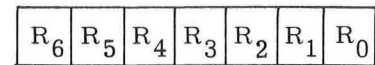


Fig. 2.4 Sense-board organization.

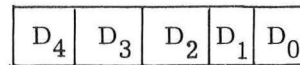
Address
(FMA)



Receiver
Number



Driver
Number



Sense Group
Number

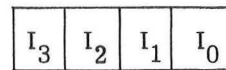


Fig. 2.5. Braid Address Field.

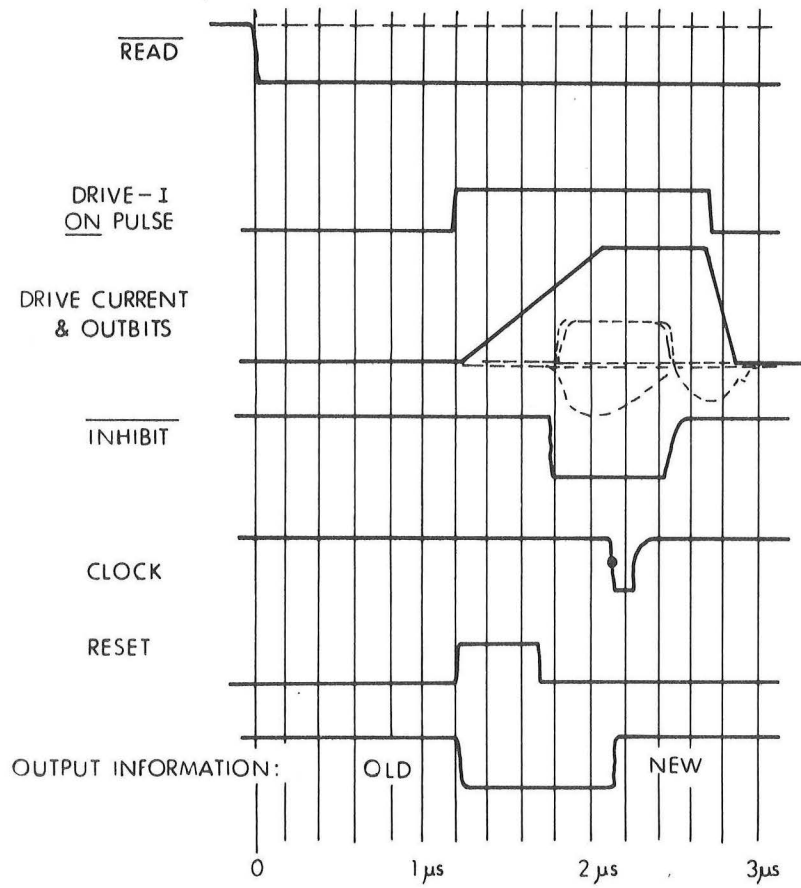
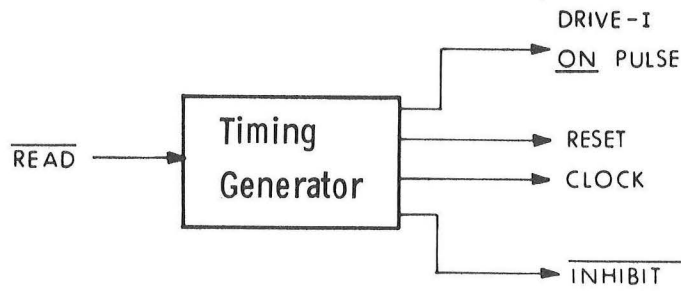


Fig. 2.6 Braid timing.

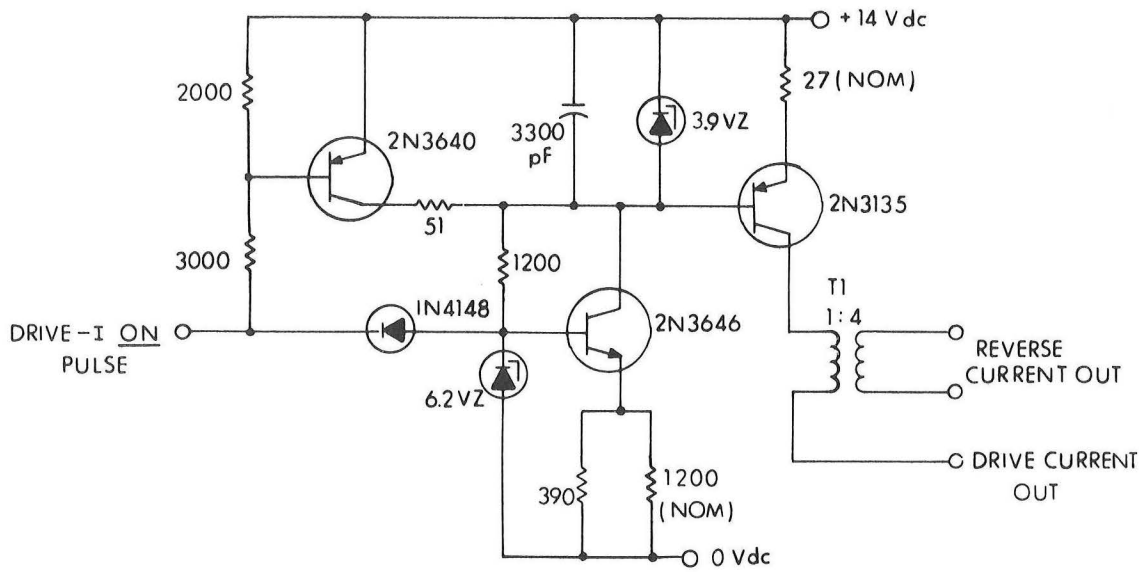


Fig. 2.7 Current source.

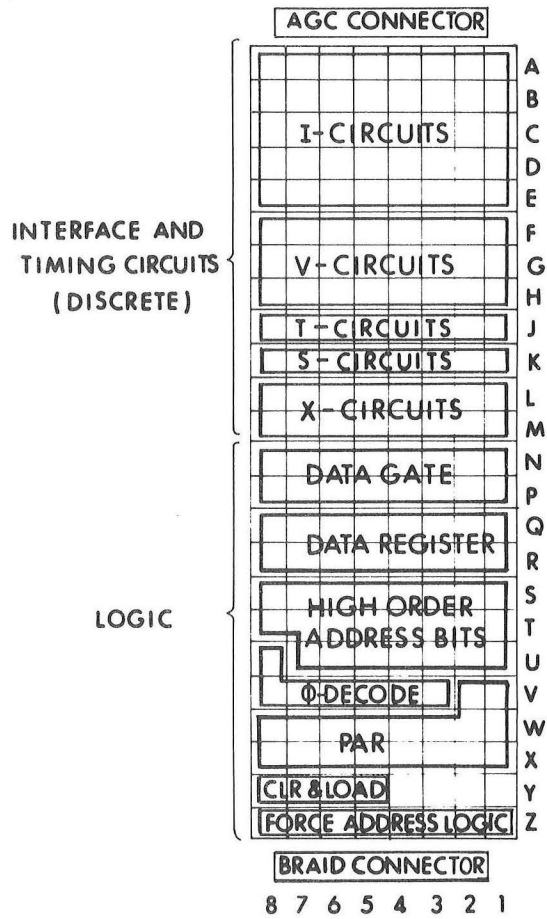
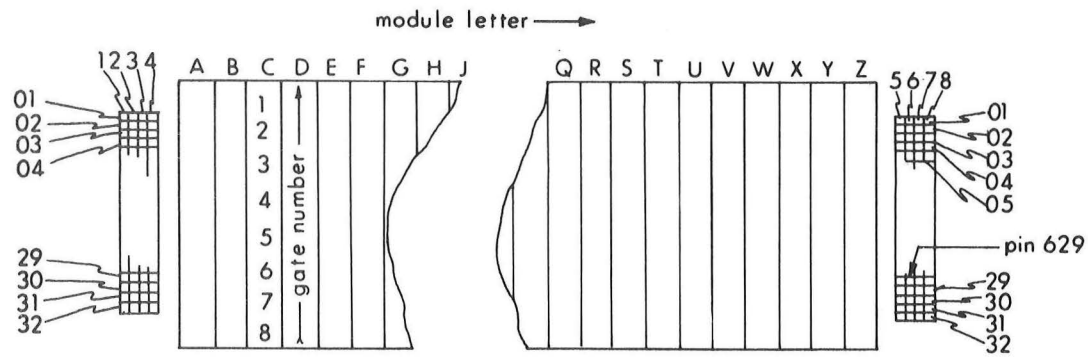


Fig. 3.1 Braid adapter module assignments.



pin configuration

		H	K		
A	O	O	O	O	V
B	O		O	O	W
C	O			O	X
D	O			O	Y
E	O	O	O	O	Z
		J	L		

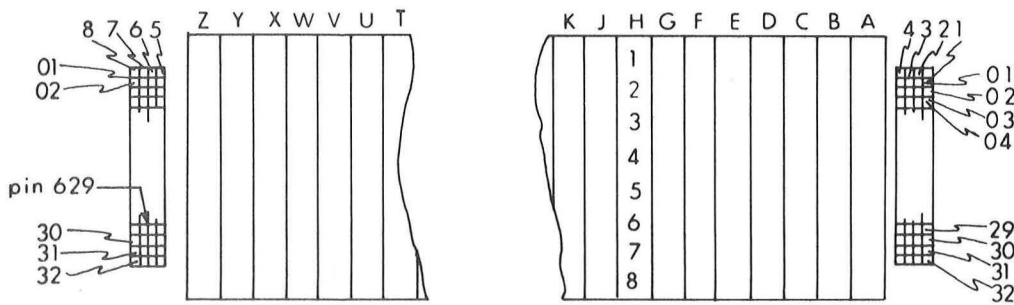
MODULE SIDE

WIRELIST DESIGNATION

A 2 B

is

module A, gate 2, pin B



WIRINGSIDE

		K	H		
V	O	O	O	O	A
W	O		O	O	B
X	O		O	O	C
Y	O		O	O	D
Z	O	O	O	O	E
		L	J		

Fig. 3.2 DGE-tray pin-numbering convention.

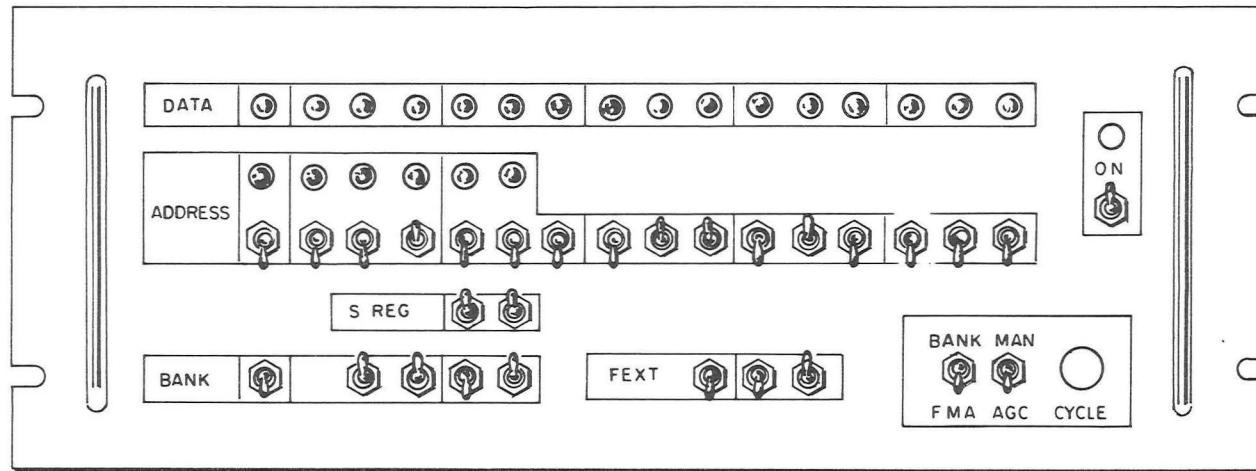


Fig. 3.3 Braid adapter panel.

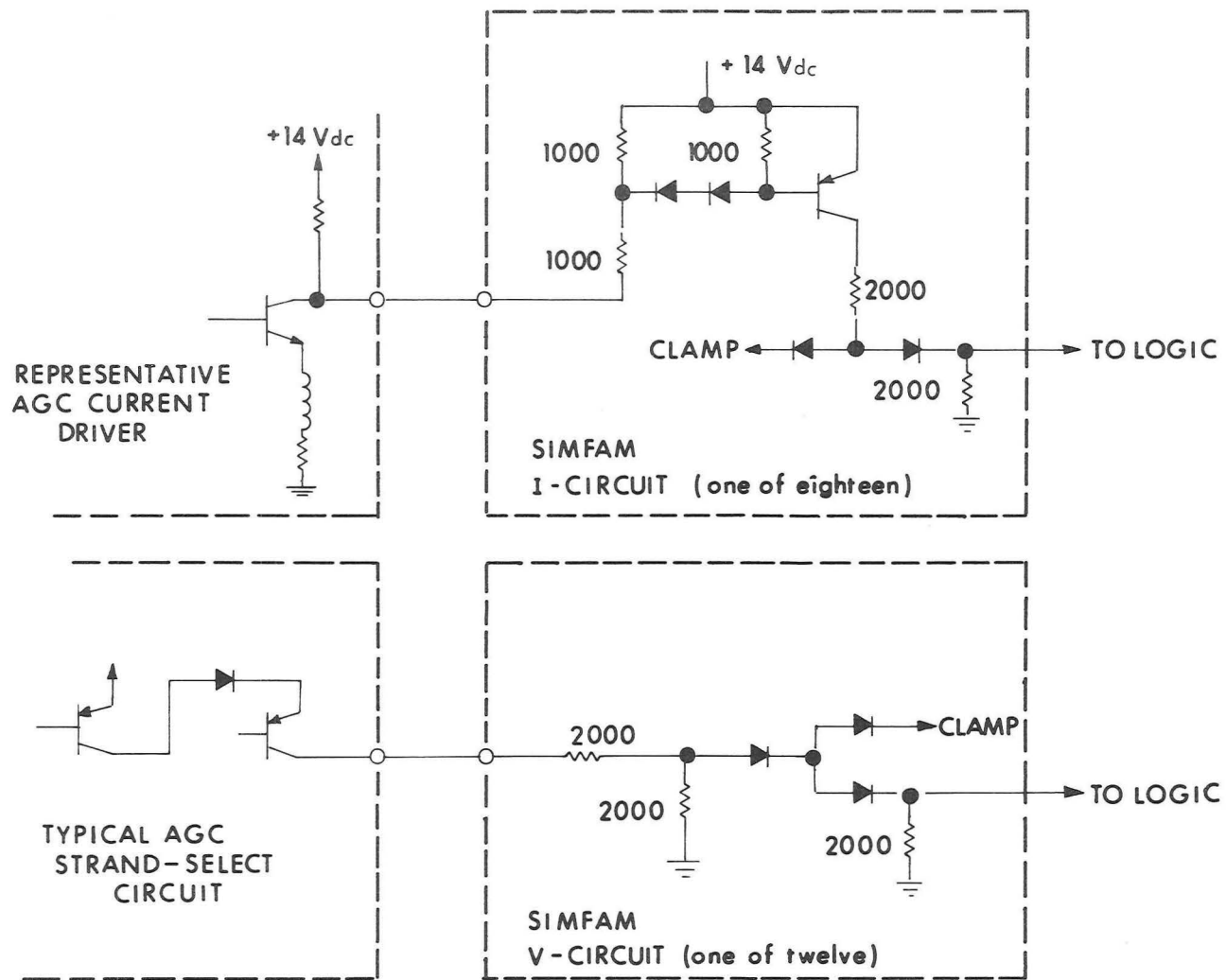


Fig. 3.4 AGC-SIMFAM interface.

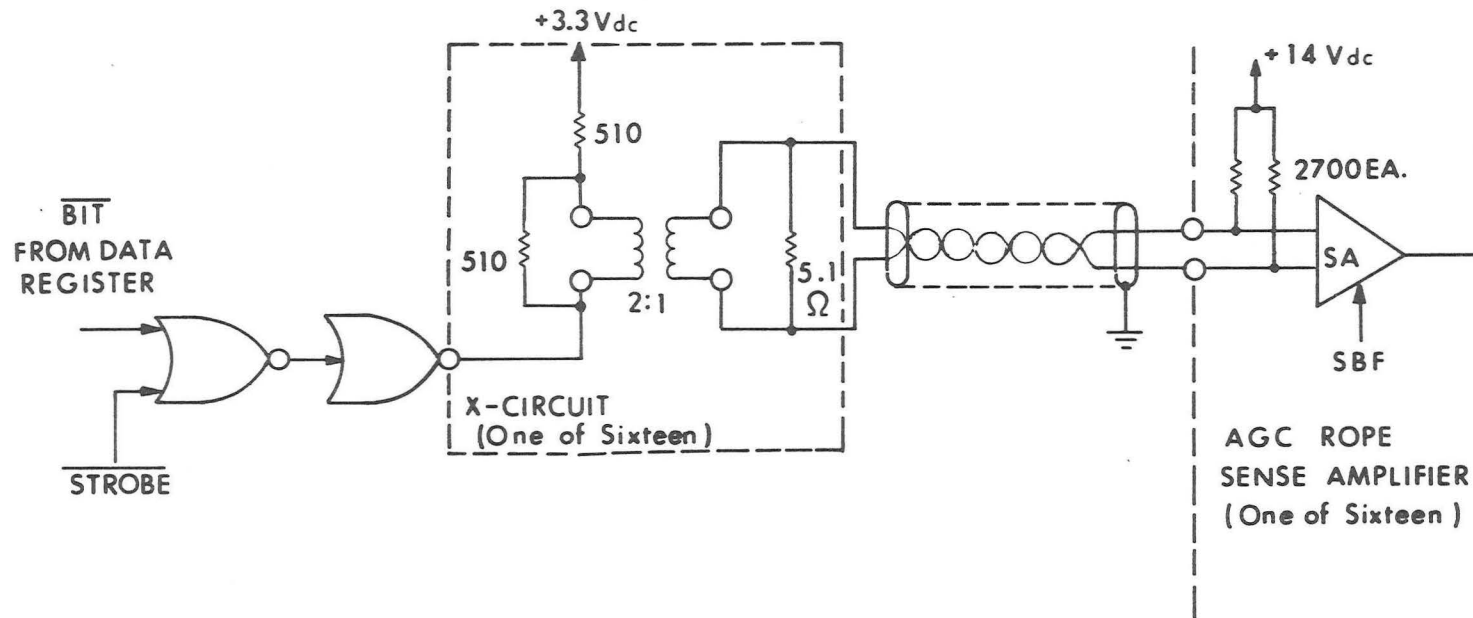


Fig. 3.5 SIMFAM-AGC sense amplifier interface.

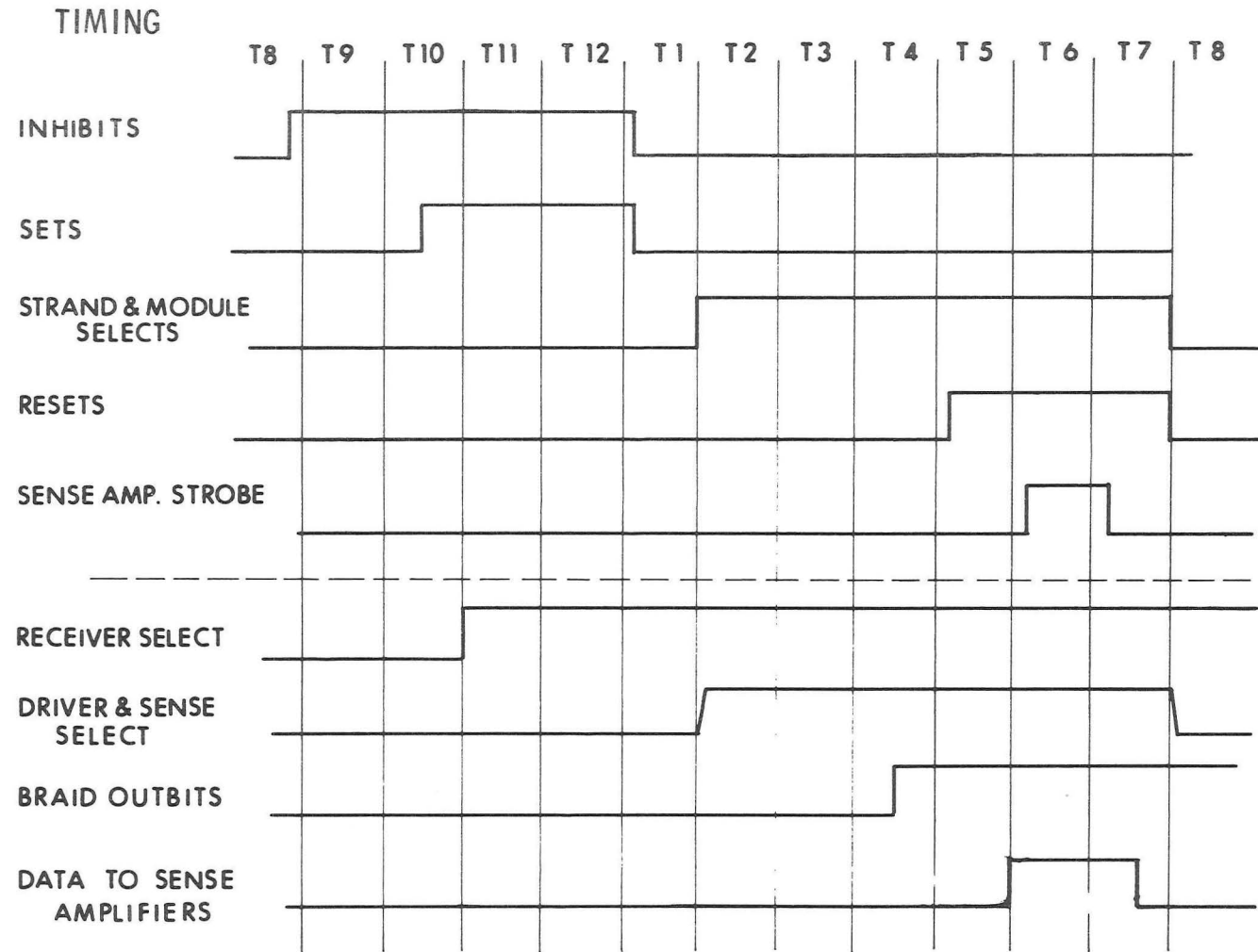


Fig. 3.6 AGC and SIMFAM timing.

TABLE 3.1
AGC Rope-Driver Signals

NAME	AGC CKT TYPE	SIGNALS	SIMFAM CKT TYPE
Inhibits	I-Drivers	X01CN	I
		X02CN ↓ X07CN XPCN	Not Used
		X01FN ↓ X07FN	I
		XPFN	Not Used
Sets	I-Drivers	XSETAB XSETCD	I
Resets	I-Drivers	XRSTAN	I
		XRSTBN	Not Used
		XRSTCN	I
		XRSTDN	Not Used
Clear	I-Driver	CLRROPR CLRROPS CLRROPT	Not Used
Module Select	I-Drivers	MODR1 MODR2 MODS1 MODS2 MODT1 MODT2	I
Strand Select	Saturated Switch to BPLSSW	STR01 ↓ STR12	V

E-2462

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