Apollo Study Report Volume II

Apollo Study Report

Volume II

Contract No. NAS 8-5296
and NAS 8-5276

CLASSIFICATION AND CONTENTS
APPROVED BY: M. M. Dickinson

PROJECT OFFICE APPROVAL: R. E. Kuehn

IBM NO.: 63-928-130

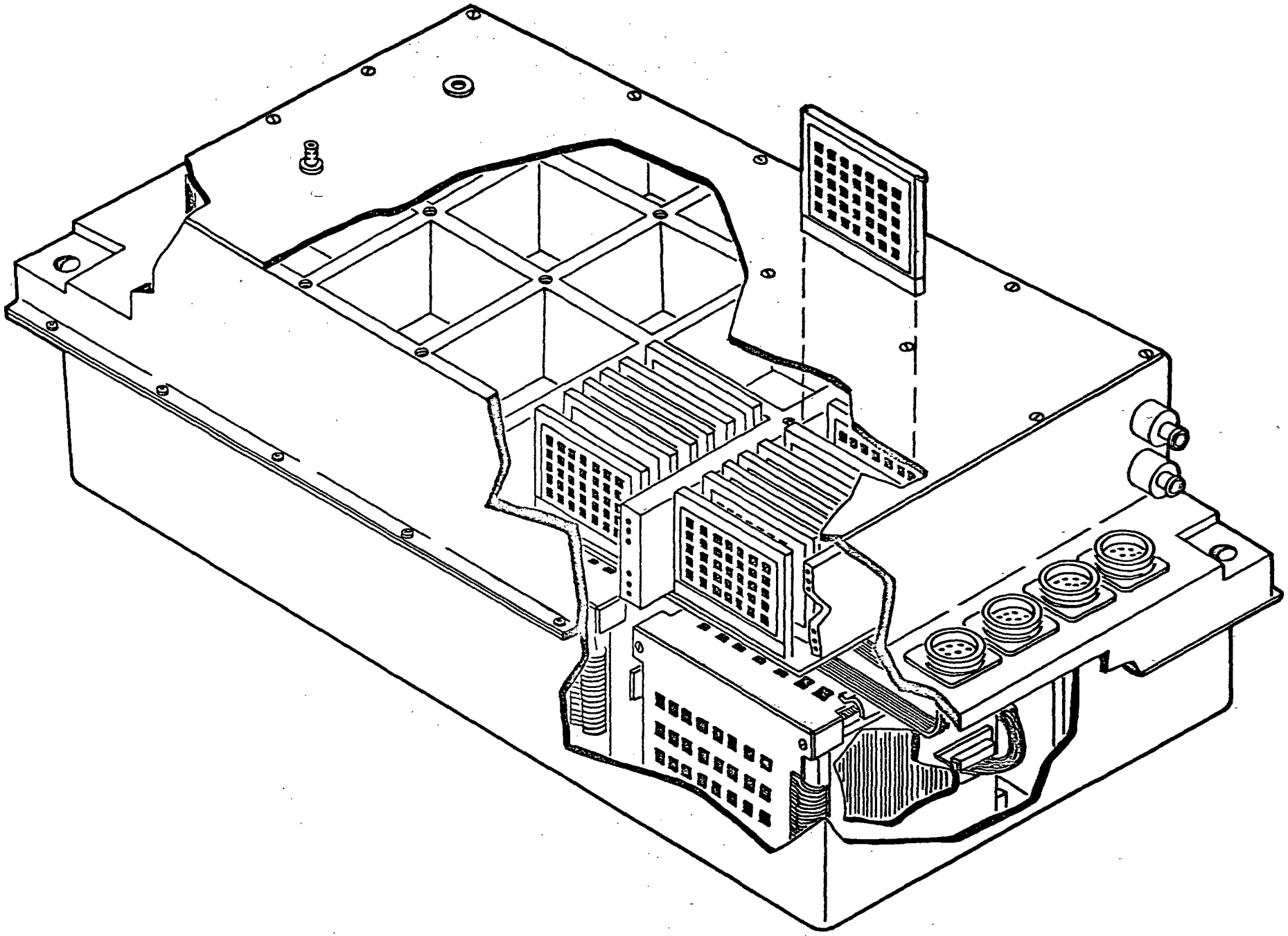
Prepared for the
GEORGE C. MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

IBM Space Guidance Center, Owego, New York

FOREWORD

The feasibility of adapting the Saturn V Guidance Computer, Data Adapter, and Laboratory Test Equipment to the Apollo application was studied by IBM under NASA Contract NAS 8-5296.

This report presents the results of the study effort. In order to publish this report as soon as possible, it is being submitted without prior NASA review. However, discussions with NASA personnel contributed significantly to the compilation of this report. Volume I describes equipment that will successfully fulfill the requirements of the Apollo mission. Volume II describes the equipment currently being developed for Saturn V. The essential similarities of Apollo and Saturn V equipment can provide significant time and dollar savings during the Apollo development program.



Saturn V Guidance Computer

CONTENTS

Contents (cont)

Contents (cont)

ILLUSTRATIONS

Illustrations (Cont)

TABLES

Section I

SYSTEM CONFIGURATION

Section I

SYSTEM CONFIGURATION

A. GENERAL

The Saturn V Guidance Computer and Data Adapter (DA) is integrated into the Saturn V vehicle guidance system. To meet the requirements imposed by a variety of missions, flexible and highly reliable computer and DA equipment was designed. High computing speed and a random-access core memory are combined in a microminiature design approach achieving low power dissipation and minimum size and weight.

The guidance computer is the primary computing element in the complex Saturn guidance system. It provides sufficient speed to meet all anticipated computing needs and has a memory large enough to store all programs to be performed in the various phases of the mission. The computer uses microminiature packaging technology, a random-access magnetic core memory, triple modular redundancy, and duplex memory modules to achieve the very high reliability required for the Saturn missions. The computer is interconnected with the DA which contains input and output conversion electronics and power control equipment. The DA also connects the guidance computer with the ground control computer, the telemetry equipment, and the guidance system sensors used during the mission.

High computational speed is obtained by operating the computer at a 500-kilocycle bit rate and using a logical organization that permits both addition and multiplication operations to take place simultaneously. Program instructions are conserved in this mode of operation by allowing the programmer control over whether one-word-time operations (and advancing of the instruction counter) are permitted during multiplication. One option uses a multiply operation that allows concurrent one-word-time operations, while the other results in a sequential multiply mode by prohibiting one-word-time operations in the adder. Although this type of organization requires more components than a machine organized to permit only sequential, nonconcurrent operation, it allows a computational speed up to 40 percent greater than that of the conventional machine.

An instruction storage capacity of up to 32,768 14-bit instructions (in the duplex memory mode) is provided to store the programs associated with pre-launch check-out, injection guidance, orbital check-out and lunar trajectory injection. Data words, using two instruction words for a word length of 28 bits, may be intermixed with instructions in any proportion. Each word comprises two instructions or one data word. Memory modules may be used singly or duplex in pairs, and up to eight magnetic core memory modules of 4,096 words may be mounted in the computer.

The Saturn V Guidance Computer and DA can perform a variety of space booster and orbital missions, including injecting the Apollo lunar spacecraft into lunar trajectory. In view of the importance of these missions, the need to protect the lives of the astronauts involved, the expense of the vehicles, and the safety of launch equipment, reliability is of paramount importance. For maximum reliability, triple modular redundancy (TMR) is used in the central computer electronics. The highly reliable central computer may then be used to provide for the reading of memory, the use of the input/output instrumentation, and for operation of system check-out functions with a high probability of having no malfunction in the vital central computer. TMR subdivides the computer logic into modules; the modules are triplicated and a voter establishes an output based on a majority decision. One of the modules in each trio may fail (and in some circumstances, more than one), and the computer will continue to function.

The Saturn V DA contains power supplies for itself and for the computer and its memories. It also contains all input/output (I/O) equipment necessary for communication between the guidance system and the Instrument Unit sensors and telemetry equipment. It provides registers and sampling circuits for discrete outputs and inputs, including error monitoring of the computer and data adapter. A delay line buffers interrupt signals, which cause normal computer processing to stop, so that a high priority function may be handled. A storage register also holds information intended for the RCA-110 Ground Control Computer, telemetry transmitter, and orbital check-out system Computer Interface Unit (CIU). Gating circuits are provided for system inputs from the RCA-110, command receiver, and CIU. Analog-to-digital circuits convert two-speed resolver inputs to digital form. (The resolvers indicate platform gimbal angles, horizon scanner sensor angles, and other angular inputs.) Optisyn inputs indicate velocity from the accelerometers. Ladder networks convert digital attitude error and other information to analog form.

The computer memory is organized to permit either simplex or duplex operation. In simplex operation, the memory module to be used is specified, and reading and writing takes place in this module only. For duplex operation, memory modules are used in pairs with identical information stored in

each member of the pair. Each memory is read out, but information from only one of them is used. If checking shows the information to be in error, the other memory output is used. Verified information is simultaneously written into both memories. This duplexing provides a very high reliability memory system, which is able to correct errors by its unique employment of two memory modules. Noncritical portions of the mission, such as ground pre-launch check-out, may be carried out using a simplex memory configuration. Where very high reliability is required during the flight, duplex memory operation would be used; thus, duplex memory organization provides large capacity during short and noncritical mission phases and less capacity and greater reliability for long and critical mission phases. The DA also contains redundant features for high reliability.

Redundancy leads to unique possibilities for the maintenance of the computer and DA. Each channel of the TMR central computer can be operated in turn under control of data adapter relays. Simple test problems then indicate whether the channel is functioning properly. The ground equipment can also switch modules in the TMR configuration to determine if individual modules (of which each simplex channel has seven) are malfunctioning. The inputs to the voters used in the TMR logic are monitored to determine when they do not agree. The disagreement detectors associated with each page of logic are OR'd together to isolate malfunctions to a trio of triplicated pages. In a like manner, two duplexed logic functions may be compared for disagreement and test programs and special detection circuits used to localize malfunctions. Parity checking is used in the memories to detect reading and writing errors. Addressing currents are monitored to ensure that they are within specified magnitude and timing limits. Test programs are used to periodically check memory operation.

The Saturn V Computer Manual Exerciser (ACME) laboratory test equipment was designed to test the guidance computer. It contains data displays, memory loading and verification, a test stand for mounting the computer during test, and can exercise the computer-DA interface for testing. The Saturn V Data Adapter Processor Tester (ADAPT) tester performs similar functions for the DA. It can also exercise the interfaces between the DA and external sensors.

ASTEC laboratory test equipment can test either the computer or the DA in the same manner as the ACME and the ADAPT testers. The Saturn V Test and Evaluation Console (ASTEC) can also test the combined computer-DA, using a computer test program. Other functions of the ASTEC include the capability to check operational programs by simulating system inputs in real time and recording computer and DA outputs. In addition, it can assist in diagnosing of prime equipment malfunctions by analyzing information available at test points and automating the check-out procedure.

B. SYSTEM BLOCK DIAGRAM

The Saturn V Guidance System consists of the equipment shown in Figure I-1. The DA is the focal point for interfaces among system equipment. It interconnects with input sensors, ground command and telemetry equipment, ground support and checkout equipment, and the guidance computer. The DA also contains analog-to-digital and digital-to-analog converters, power supplies and voltage sequencing, mode switching, and telemetry addressing.

The guidance computer, with its associated memory units, interconnects with the DA to perform all the required computation in the guidance system. The computer, through the use of an I/O instruction in its order code, controls the interchange of information between computer and the DA. The PIO instruction transfers one data word between the accumulator or memory and the DA.

The computer-DA interface consists of signal and control lines of various types. Computer timing signals are supplied to the DA to synchronize I/O quantities. Eight lines select the I/O device or circuit in the DA from which a computer input is read or to which a computer output is delivered. The devices or circuits include delay lines, counters, and static signal buffers. An additional control line indicates whether an input or an output function is to be performed. A computer interrupt signal consisting of discrete inputs OR'd together permits external signaling and interruption of the program both for normal mission operation and for operation with ground check-out equipment. A timed interrupt is also generated within the DA.

Computer starting and initialization are controlled by computer-DA interconnections. I/O data are serialized and transmitted to and from the DA over single I/O lines. The DA interprets the equipment selection signal and directs the data to the proper location. Discrete inputs and outputs are combined into words and handled like other I/O data. The flexibility of the computer-DA interface and the operation codes provided permit a wide variety of input and output devices to be attached as dictated by various mission requirements.

C. MODES OF OPERATION

To assist in establishing computer speed and storage requirements and to define typical mission I/O functions, which must be handled for a Saturn V application, four operating modes or states have been outlined. Some of these modes contain major submodes which are significant within themselves, but the list has been restricted for preliminary consideration. Throughout the discussion of the modes, the guidance computer is assumed to be mounted in the main Apollo mission booster.

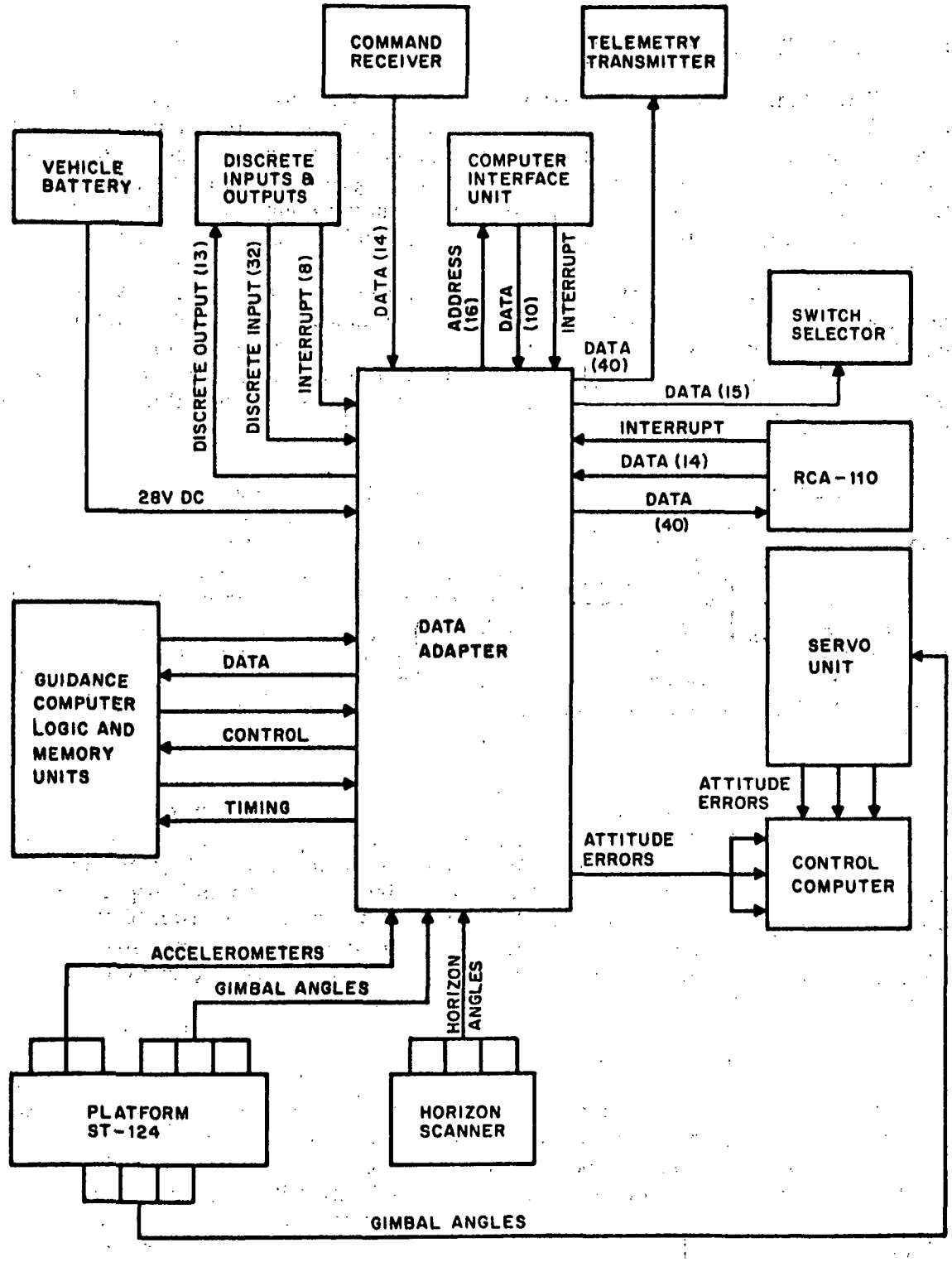


Figure I-1. Guidance Subsystem

The guidance computer is placed at the top of those propulsion systems which are responsible for carrying a "payload" into orbit. In the Apollo configuration, shown in Figure I-2, the first two stages are used to boost the systems above stage two into an earth orbit. The third stage injects the devices attached above it into a lunar transfer trajectory. The third stage is discarded after the lunar injection burning is completed; thus the computer has completed its functions at that point. Lunar orbit rendezvous of the Apollo spacecraft and a lunar excursion module is assumed.

The modes to be discussed are:

- Mode 1 - Pre-launch Check-out
- Mode 2 - Boost Guidance
- Mode 3 - Orbital Check-out
- Mode 4 - Lunar Trajectory Injection

Orbital check-out processes may be required at any point after injection into earth orbit and the problem of communicating between the vehicle data sensors and computer is discussed in the description of mode 3. The other modes are discussed briefly. Figure I-3 shows a flow diagram for the modes of operation for the orbital launch vehicle mission.

1. MODE 1 - GROUND CHECK-OUT

After the guidance computer is installed in the vehicle, all ground communication is handled through the ground control computer. The vehicle telemetry system is used to address data for sensor and vehicle check-out. Test variables are sent to the guidance computer, which will perform operations using these quantities, and results are sent back to the ground check-out complex for verification. Guidance constants are loaded in the same manner (read in and read back out for verification). Test programs are contained in the guidance computer for each mode, and a sequence similar to that followed for the actual mission is carried out so that parts of each program are checked. The platform stabilization servos may be checked by injecting a pulse into each loop and observing the transient response. All interfaces are tested by the guidance computer and the DA for proper operation before the flight.

All check-out is controlled by the ground control center and by the ground control computer. Check-out can be under direct control of the ground equipment, with results monitored through the telemetry system, or it can be carried out by the guidance computer (through command of the ground

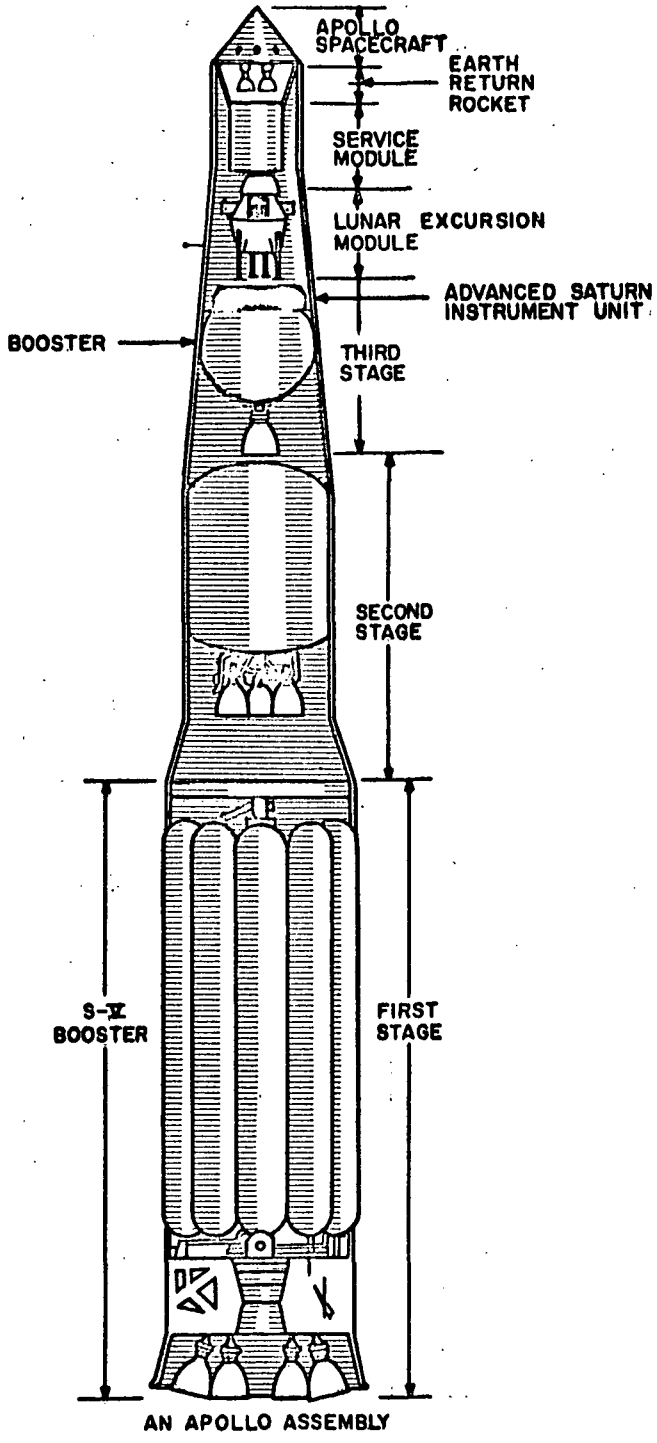


Figure I-2. Apollo Vehicle S-V

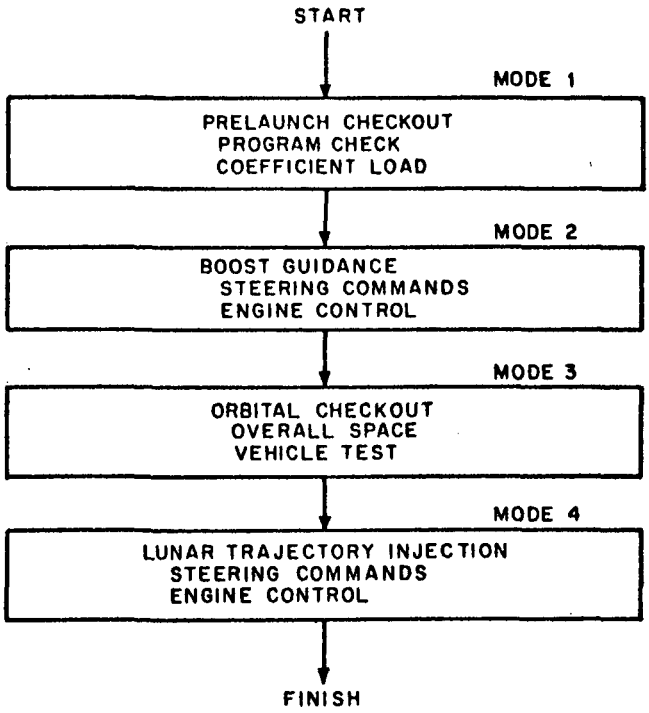


Figure I-3. Mode Flow Diagram

control computer) and results sent to the ground. The routines performed consist of Load, Verify, and Test Launch Constants; Computer Self-Test; Self-Contained Mission Simulation; System Test; Mode Control; Inertial Element Performance Monitor; Telemetry Check; Delayed Launch Condition Computation; and Delayed Launch Coefficient Modification.

2. MODE 2 - BOOST GUIDANCE

During the period from liftoff to burnout of the final boost stage the computer inputs and outputs consist of the following (Figure I-4):

(a) Inputs

- Accelerometer outputs, in the form of optisyn encoders, representing velocity.
- Discrete inputs indicating liftoff, stage 1 cutoff, separation, stage 2 ignition, stage 2 cutoff, engine out, etc.

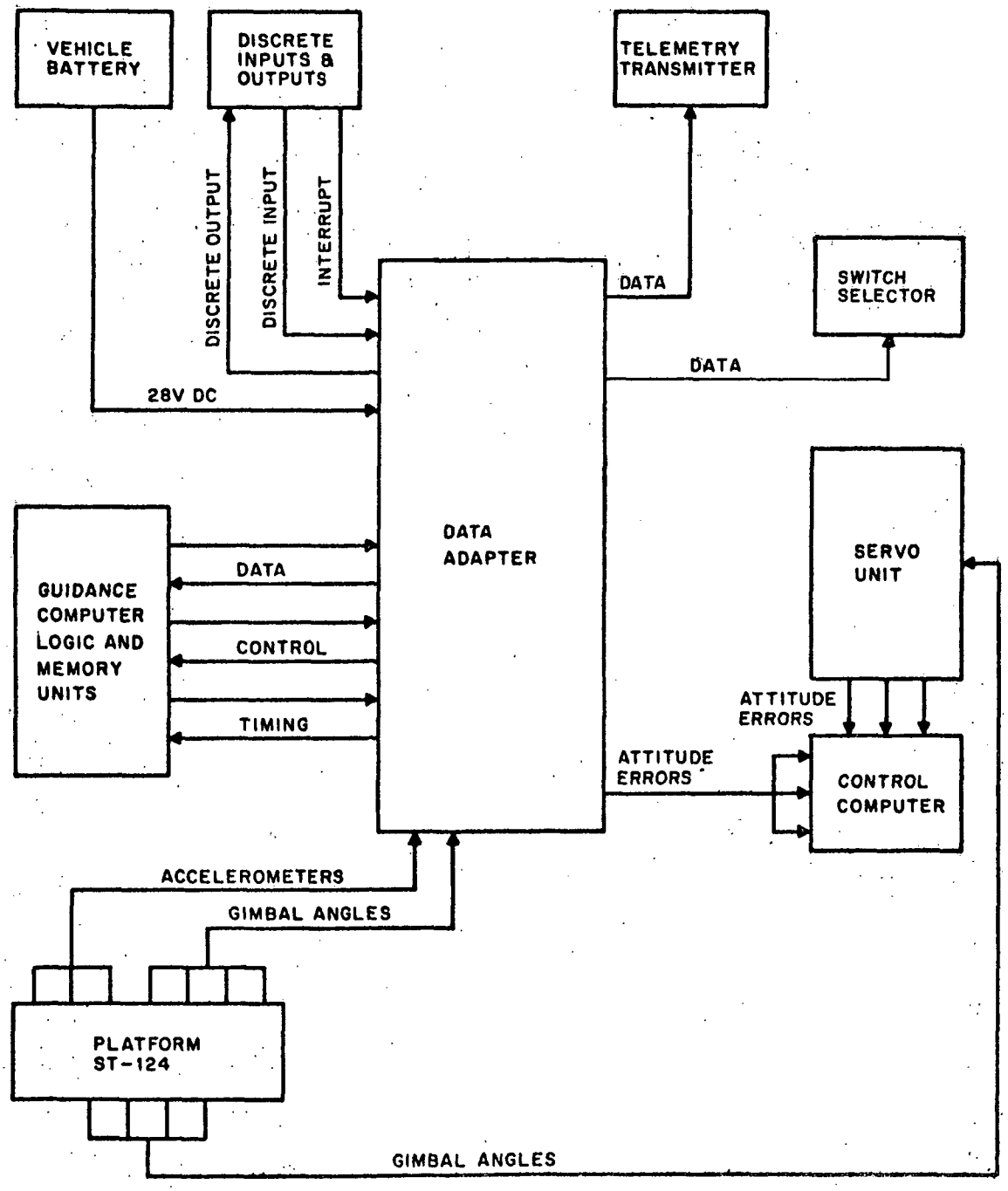


Figure I-4. Boost Guidance

- Platform gimbal angles in the form of two-speed resolver signals.

(b) Outputs

- Attitude error signals, which are resolved in computer.
- Telemetry data words, at a maximum rate of 240 per second, to monitor computer and DA operation.
- Discrete outputs commanding second and third stage cutoff, stage separation, etc.

The computer routines executed during the boost guidance mode consist of the following:

- Navigation - The velocity vector is determined, coordinate transformation is performed, present position is calculated, and the gravity vector is projected into the guidance coordinate frame.
- Steering - Projections of required velocity are computed through a polynomial path-adaptive scheme, and steering commands are computed.
- Logic - Timed vehicle functions and logical decisions are made.
- Cutoff - A polynomial is used to compute cutoff time.
- Reasonableness Testing - All navigation and steering parameters are checked for reasonableness.

Corrections resulting from gyro drift-rate data are carried out in this mode if necessary.

Computations in Mode 4, Lunar Transfer Trajectory Injection, are similar to this mode.

3. MODE 3 - ORBITAL CHECK-OUT (See Figure I-5)

The Saturn V computer is needed to check out all vehicle systems while in orbit, prior to launching the Apollo spacecraft into a lunar trajectory. This is the last point at which the operational capability of the system can be checked and an abort initiated before the spacecraft is committed to its trip to the moon. Propulsion, attitude control, radio command, guidance, telemetry, and radar systems require check-out. The Saturn Instrument Unit must also be checked out. These systems are activated to the greatest

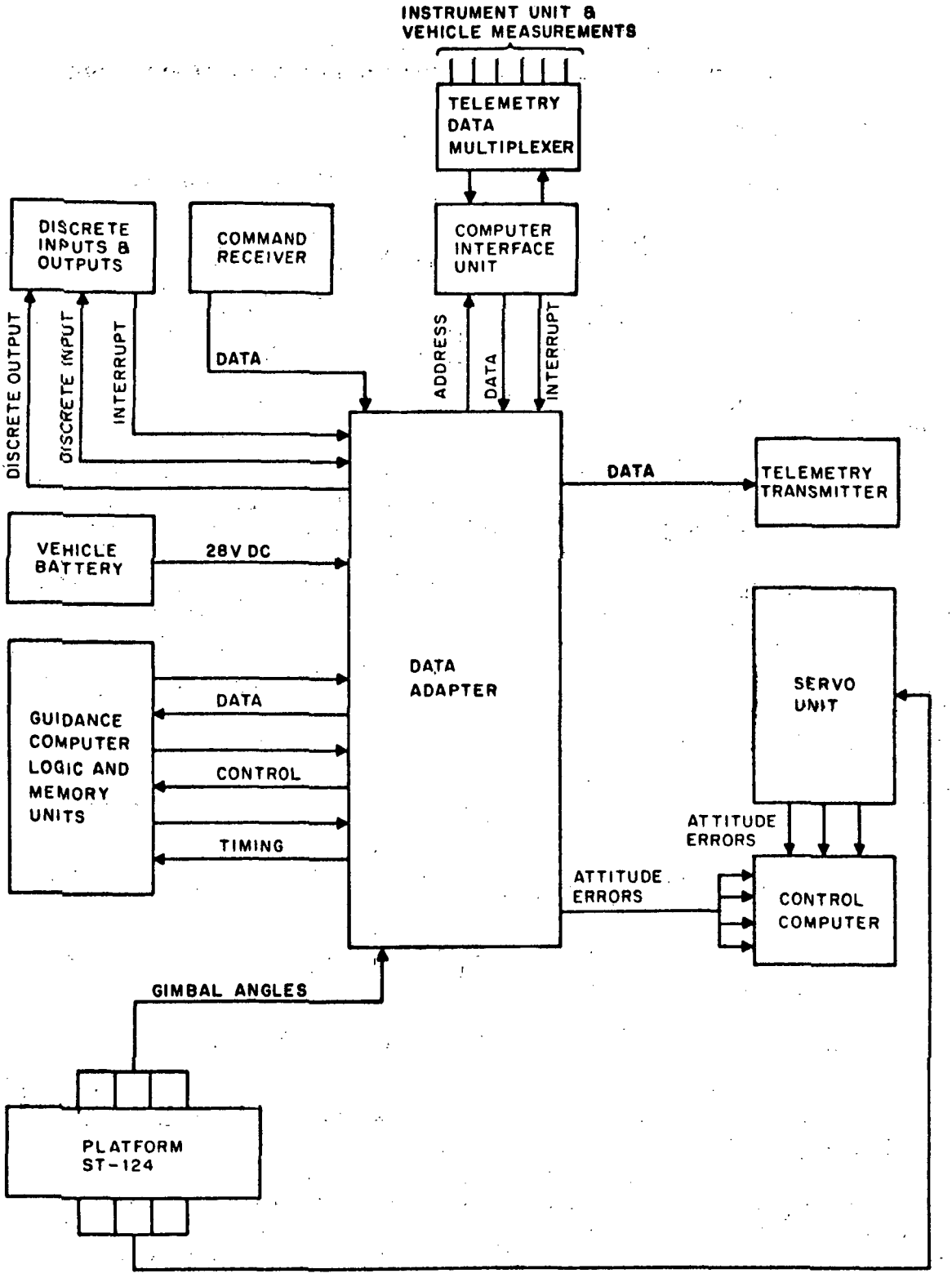


Figure I-5. Orbital Check-out

extent possible and the computer sequentially initiates stimuli to each system and evaluates its response via feedback from the telemetry analog-to-digital converter. The computer is able to identify the telemetry data and has go, no-go limits stored for each parameter it monitors as well as certain dynamic response characteristics. Up to 2,000 different parameters are evaluated either statically, dynamically, or both.

When dynamic response is checked, a few standard characteristic equations can be stored in the computer, with sets of reference coefficients for the various parameters being tested. One of the major reasons for performing the orbital checkout is to save telemetry power, so only the results of the tests are transmitted to the ground. Since the tests might be performed while the vehicle is in an unfavorable orientation or location for telemetry transmission, there is a need to store and transmit, at a later time, certain test results and selected data which were questionable and required further analysis on the ground.

Data Adapter inputs and outputs during this mode are as follows:

(a) Inputs

- Platform gimbal angles in the form of two-speed resolver signals.
- Quantities measured through the telemetry multiplexer and Computer Interface Unit, which are checked in the computer.
- Commands and data from the command receiver.
- Discrete inputs indicating status of Instrument Unit and vehicle equipment and responses to tests performed.

(b) Outputs

- Attitude error signals which were resolved in computer.
- Telemetry data words, at a maximum rate of 240 per second, to monitor computer and DA operation, and report orbital check-out information to the ground.
- Discrete outputs to initiate tests and stimuli to IU and vehicle equipment.
- Address information to the Computer Interface Unit to select quantities for checking.

4. OTHER COMPUTATIONS

In addition to the basic modes of operation and computations previously outlined, certain other computations, described in the following paragraphs, must logically be performed by the on-board computer in the orbital launch vehicle.

Load and Verify Data - Data from the vehicle radio command system are loaded in the computer memory and verified. Synchronization signals must be properly decoded and precautions taken to ensure that the correct memory locations are used.

Malfunction Isolation Tests - When a malfunction in the vehicle system is detected, several alternate means of handling it are available. The airborne computer can be placed under control of the ground control complex to carry out detailed commands within the system; the ground control computer can load appropriate test routines into the memory of the airborne computer, which would then carry out the testing functions; or the test routines can be stored in the airborne computer memory, and carried out on command from the ground. These tests are very extensive, particularly in the case of redundant equipment where the malfunctioning element must be identified. These tests also include decisions which initiate alternate modes of operation where other inputs are available.

Data Transmission - A special routine is used to transmit selected data during checkout modes or during certain other modes of operation. This data is in addition to normally-transmitted flight data.

Computer Self-Test - A portion of each routine is devoted to computer self-test. This testing continuously monitors computer performance, and is in addition to a pre-flight test routine.

DA Test - The computer conducts tests to indicate the performance of the DA and to localize malfunctions. The DA delay lines are written into and read from. Sample quantities are converted through the ladder decoders to test their operation. If duplexed logic outputs do not agree, tests are originated to localize the malfunction to either one of the pair.

Other Mission Equations - Numerous other programs are part of the computer requirements for various space booster missions. For example, practice rendezvous missions are executed in earth orbit to test all systems and operational concepts before attempting a lunar orbit rendezvous. Rendezvous sensors then become part of the overall system and the Saturn V Guidance Computer plays a role in such missions. Rendezvous equation programs are stored in the computer memory along with other mission equations. All functions discussed previously are not necessarily part of every mission, however, so the computer memory does not have to store all possible programs simultaneously.

D. COMPUTER AND DATA ADAPTER CONSIDERATIONS

1. MEMORY STORAGE CAPACITY

To determine the total memory storage requirement for a mission, the storage requirement for each routine which is used on the mission was estimated.

A breakdown of each major computer function with a crude estimate of the memory storage requirements for each is presented in the following paragraphs. This list of functions is presented as a typical example of the type of operations to be performed. Both the complexity and the types of functions to be performed vary considerably with changes in mission concepts and with the system configuration. It is presented as a reasonable estimate, however, which is used for estimating the memory requirements for the type of vehicle in question. Because the final mission definition is not complete and is subject to a considerable amount of change, the memory configuration was selected for maximum flexibility by permitting from one to eight memory modules to be used.

Compilations of gross estimates for the orbital launch vehicle computer functions are presented in Table I-1. These estimates are in terms of equivalent instruction words, where an instruction word may consist of 13 bits, and a constant is considered to be the equivalent of two instruction words.

2. MEMORY STORAGE CHARACTERISTICS

Although the degree of complexity of each of the listed functions will vary considerably, depending upon the exact implementation to be used, one significant characteristic of each is that they are performed sequentially. The order in which the functions are executed may vary from mission to mission, and may even change during a mission; but their sequential nature does not change. During each phase of the mission, only a limited number of routines are used. Furthermore, there are long time periods between certain functions and, if properly organized, there should be no need for rapid change-over from one set of routines to another.

Because of program storage requirements, the computer memory contains 4 modules of 4,096 28-bit words each. This capacity provides 16,384 duplexed instructions (14-bits each) which are adequate for most missions. Where less storage is needed all of the memory modules need not be carried. Where greater storage capacity is required, up to eight memory modules are used, increasing the capacity to 32,768 duplex instructions.

Table I-1

STORAGE REQUIREMENT FOR COMPUTER

Routine	Storage Requirement in Equivalent Instruction Words			
	Estimated Minimum		Estimated Maximum	
Ground Prelaunch				
Load, Verify, and Test Launch Constants	400		600	
Computer Self-Test	100		200	
Self-Contained Mission Simulation	400		800	
System Test	100		200	
Mode Control	100		200	
Inertial Performance Monitor	100		200	
Telemetry Check	100		200	
Delayed Launch Condition Computation	200		400	
Launch Coefficient Modification	100		200	
Subtotal		1,600		3,000
Orbit Injection and Orientation				
Navigation	800		1,200	
Steering	800		1,200	
Logic Decisions	400		600	
Cutoff	400		600	
Orientation	200		400	
Reasonableness Tests	400		800	
Subtotal		3,000		4,800
Orbital Checkout	800		4,000	
Load and Verify Data	200		400	
Orbital Transfer Computations	400		800	
Malfunction Isolation Tests	1,600		16,000	
Data Transmission	200		2,000	

Table I-1. Storage Requirement For Computer (cont)

Routine	Storage Requirement in Equivalent Instruction Words	
	Estimated Minimum	Estimated Maximum
Lunar Injection Guidance Using Orbital Injection Guidance with:		
Different Constants	400	800
Different Logic	400	800
Total Mission Requirement For All Phases	4,000	24,800
	8,600	32,600

3. COMPUTATIONAL SPEED

Since the missions and programs for Saturn V have not yet been completely defined, it is difficult to determine the required speed. The Saturn I injection guidance equations have been examined since they will likely be the longest computing loop and require the highest computational speed. For the equations defined, the Saturn V Computer will have a solution time of from 0.25 to 0.40 seconds. The computations include navigation and guidance and all program logic required. The speed capability of the computer provides for growth in problem complexity for a given maximum computation interval and augments the growth capability provided in memory capacity.

The inclusion of digital resolution computations for four gimbal angles, performed at the rate of 25 per second, requires less than 25 percent of the available computing time. This should allow a major loop (other low-speed computations) computation cycle of from one to two per second. A reduction in speed required for the resolutions or a simplification in their complexity through the use of various constraints and approximations yields a substantially higher major loop iteration rate.

4. DATA ADAPTER DESIGN

The DA design permits considerable flexibility in both the addition of larger numbers of existing functions and the addition of other types of I/O devices. Spare capacity in discrete inputs and outputs and in the interrupt register is provided, for example, to ensure that future mission requirements

will be satisfied. The design permits the inclusion of an increased number of electronic pages to increase the capacity from the normal mission requirement to the maximum design limit.

Both digital and analog interfaces have been identified for the DA. The digital interface uses static registers and sampling gates, and serializers for I/O transmission. The analog interface uses dual-speed resolvers for angular inputs, optisyns for accelerometer pickoffs, and processes analog outputs through ladder network digital-to-analog decoders. The resolver inputs and analog outputs are multiplexed, and additional capacity is provided for future growth.

Because of this interface definition, a strong attempt has been made to standardize the I/O devices so that they mate with the appropriate interface. This standardization limits the amount of unit redesign to permit the incorporation of new types of sensors and other equipment.

Section II

RELIABILITY

Section II

RELIABILITY

Mathematical analyses have shown that the operational reliabilities of the guidance computer and the data adapter will exceed the design goal of 0.99 which was set for each during a 250-hour mission with the units operating at 60°C. In addition, the mathematical reliability model of the guidance computer — data adapter system was exercised to derive reliability estimates for various other mission lengths and operating conditions, using both redundant (duplex) and nonredundant (simplex) computer modes.

A block diagram of the system model is shown in Figure II-1. The ground rules for redundant-mode reliability calculations are as follows:

(1) The oscillator contains no redundancy; the failure of any component causes system failure.

(2) The basic oscillator signal is subdivided in the Timing Generator (TG). As depicted in Figure II-1, the TG is operated in triplicate. A failure in a TG results in failure of the TMR channel with which it is associated. (Actually, this is a pessimistic assumption made to simplify formulation of the mathematical model.)

(3) The computer TMR logic block consists of seven triplicated modules (trios). All outputs of each trio are voted upon; there is one set of triplicated voters for each trio output. The reliability model recognizes that failure in a TG block results in a requirement that both of the other channels must work for mission success.

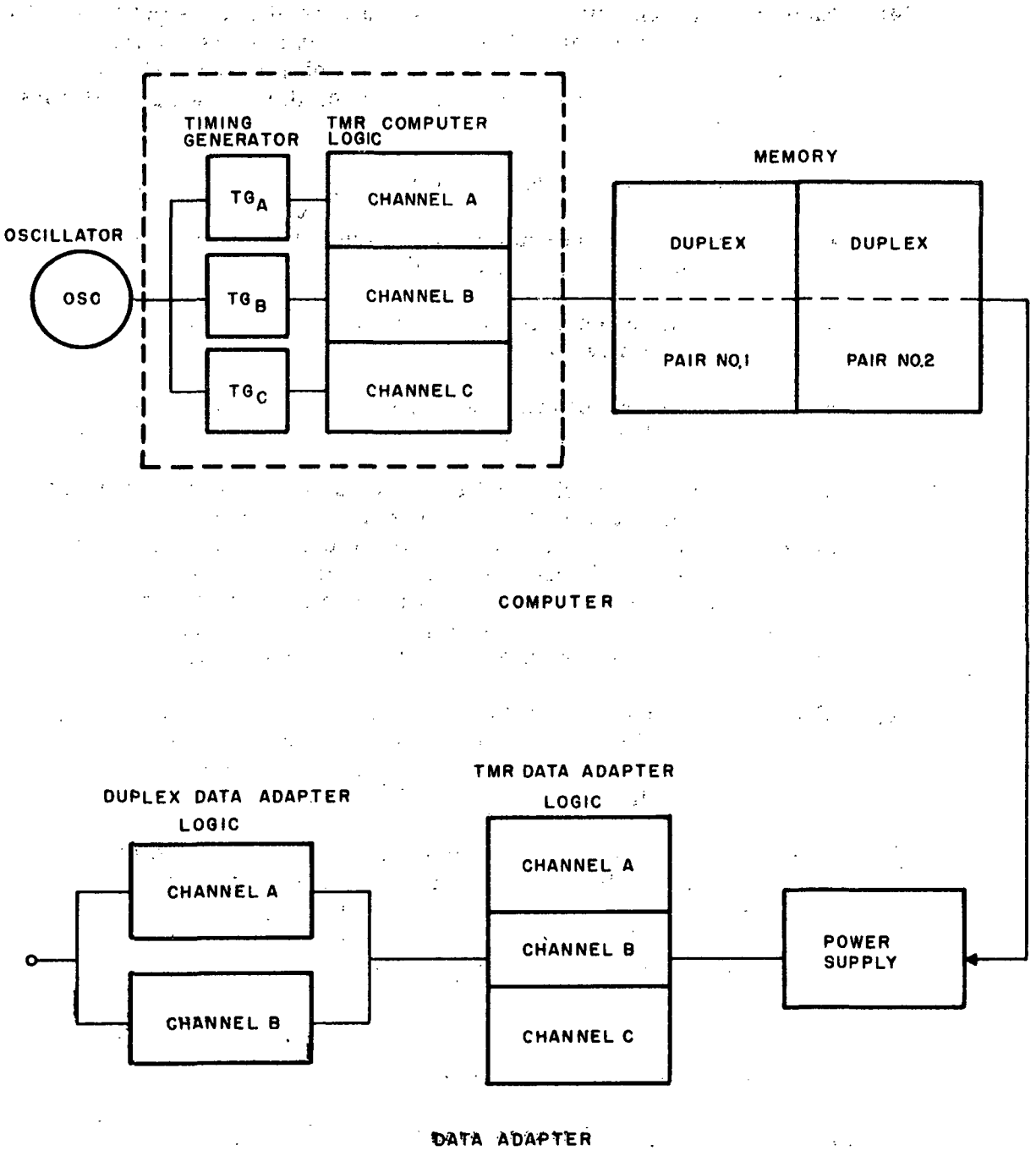


Figure II-1. Block Diagram of System Model

(4) Each duplex memory pair consists of a pair of arrays (64 x 128x14 cores) and its associated drivers. A duplex pair cannot be accurately described as two blocks in parallel (i.e. $R \neq 1-(1-R)^2$). For a duplex pair to cause system failure, the following conditions must exist:

- An error of an undetectable nature, or
- An error of a detectable nature and concurrent failure of the detection circuitry, or
- A simultaneous error in the same word location in each memory array, or
- Combinations of failures in elements external to memory (i. e., induced failure).

(5) The power supply block supplies six voltages to the data adapter and computer. Each voltage is generated by a duplex redundant power supply. The output of each voltage branches into separate power lines for each channel in the machines. The duplex arrangement is such that either of the two supplies can fall to a low voltage state without affecting system operation. However, if either supply falls to a high voltage state, mission failure results.

(6) The TMR portion of the data adapter is similar in design to the computer TMR logic. In view of the relative crudeness of the definition of this portion of the system, reliability is computed on the basis of the $R_{tmr} = (3R^2 - 2R^3)^n$ approximation.

(7) The data adapter duplex electronics are only crudely defined. The analysis of this portion of the system is made by using the two blocks in parallel approximation (i. e. $R_{duplex} = 1-(1 - R)2$). This is extremely pessimistic in that one set of duplex blocks is assumed, while in practice there will be several duplex blocks which are much smaller, thus resulting in greater reliability gain.

The resultant mathematical equation is:

$$R_{system} = (R_{osc})\ (R_{c1})\ (R_{mem})\ (R_{ps})\ (R_{datmr})\ (R_{dadup})$$

where

R_{osc} = reliability of oscillator

R_{c1} = reliability of computer logic; includes TMR computer logic and timing generation.

R_{mem} = reliability of memory

R_{ps} = reliability of power supply

R_{datmr} = reliability of data adapter TMR circuitry

R_{dadup} = reliability of data adapter duplex circuitry

Simplex (nonredundant) calculations assume that any component failure causes system failure. These were computed by summing the failure rates of all elements and applying the conventional $R = e^{-\lambda t}$ formula.

In the following tables, the power supply is included in the computer, rather than in the data adapter package. This is only to present a unified computer package without interface equipment. In the redundant equipment actually being developed, the reliability of the power supply is so high as to be negligible. If the power supply unreliability were significant, it would actually be assessed against the data adapter reliability goal, since it is physically packaged in the data adapter unit.

Table II-1

NONREDUNDANT (SIMPLEX) MODE RELIABILITY
WHEN OPERATING AT 100°C

Unit	Failures per Million Hours ($\lambda \times 10^6$)	Reliability		
		Mission Time (hours)		
		100	250	500
Oscillator	0.537	0.999946	0.999866	0.999731
Timing Generator	11.511	0.998851	0.997129	0.994267
Logic	196.384	0.980554	0.952089	0.906475
Subtotal - Computer	208.432	0.979375	0.949228	0.901036
8000-Word Memory	198.850	0.98031	0.95150	0.90536
Subtotal - Computer and 8000-Word Memory	407.282	0.960091	0.903190	0.815762
Power Supply	4.141	0.99752	0.99378	0.98764
Subtotal - Computer Package	411.423	0.957710	0.89753	0.805679
Data Adapter	378.500	0.9628	0.9097	0.8275
TOTAL SYSTEM	789.923	0.922083	0.816522	0.666700

Table II-2

REDUNDANT (DUPLEX) MODE RELIABILITY
WHEN OPERATING AT 100°C

Unit	Reliability		
	Mission Time (hours)		
	100	250	500
Oscillator	0.999946	0.999866	0.999731
Timing Generator and TMR Logic	0.999253	0.997770	0.991300
Subtotal - Computer	0.999199	0.997636	0.991033
8000-Word Memory	0.99898	0.996785	0.991440
Subtotal - Computer and 8000-Word Memory	0.998180	0.994429	0.982550
Power Supply	$\cong 1$	$\cong 1$	≥ 0.999975
Subtotal - Computer Package	0.998180	0.994429	0.982526
Data Adapter (TMR)	0.9999	0.9996	0.9985
Data Adapter (Duplex)	0.9993	0.9960	0.9850
TOTAL - SYSTEM	0.997381	0.990055	0.966336

Table II-3

NONREDUNDANT (SIMPLEX) MODE RELIABILITY
WHEN OPERATING AT 75°C

Unit	Failures per Million Hours ($\lambda \times 10^6$)	Reliability		
		Mission Time (hours) 100	250	500
Oscillator	0.532	0.999947	0.999867	0.999734
Timing Generator	10.217	0.998979	0.997449	0.994906
Logic	181.079	0.982056	0.955740	0.913438
Subtotal - Computer	191.828	0.981001	0.953175	0.908543
8000-Word Memory	181.138	0.98205	0.95573	0.91341
Subtotal - Computer and 8000-Word Memory	372.966	0.963392	0.910978	0.829872
Power Supply	3.441	0.99794	0.99485	0.98972
Subtotal - Computer Package	376.407	0.961408	0.906287	0.821341
Data Adapter	346.300	0.9660	0.9170	0.8410
TOTAL - SYSTEM	722.707	0.928720	0.831065	0.690748

Table II-4

REDUNDANT (DUPLEX) MODE RELIABILITY
WHEN OPERATING AT 75°C

Unit	Reliability		
	Mission Time (hours)		
	100	250	500
Oscillator	0.999947	0.999867	0.999734
Timing Generator and TMR Logic	0.999380	0.99798	0.99219
Subtotal - Computer	0.999327	0.997847	0.991826
8000-Word Memory	0.999123	0.99725	0.99271
Subtotal - Computer and 8000-Word Memory	0.998451	0.995103	0.984695
Power Supply	$\cong 1$	$\cong 1$	$\cong 1$
Subtotal - Computer Package	0.998451	0.995103	0.984695
Data Adapter (TMR)	0.9999	0.9997	0.9988
Data Adapter (Duplex)	0.9994	0.9966	0.9873
TOTAL - SYSTEM	0.997752	0.991422	0.971023

Table II-5

NONREDUNDANT (SIMPLEX) MODE RELIABILITY
WHEN OPERATING AT 60°C

Unit	Failures per Million Hours ($\lambda \times 10^6$)	Reliability		
		Mission Time (hours) 100	250	500
Oscillator	0.528	0.999947	0.999868	0.999736
Timing Generator	9.427	0.999057	0.997644	0.995294
Logic	175.211	0.982632	0.957147	0.916122
Subtotal - Computer	185.166	0.981653	0.954766	0.911570
8000-Word Memory	170.548	0.98309	0.95826	0.91826
Subtotal - Computer and 8000-Word Memory	355.714	0.965054	0.914914	0.837058
Power Supply	3.054	0.99817	0.99542	0.99085
Subtotal - Computer Package	358.768	0.963288	0.910724	0.829399
Data Adapter	330.500	0.9674	0.9207	0.8476
TOTAL - SYSTEM	689.268	0.931884	0.838503	0.702999

Table II-6

REDUNDANT (DUPLEX) MODE RELIABILITY
WHEN OPERATING AT 60°C

Unit	Reliability		
	Mission Time (hours)		
	100	250	500
Oscillator	0.999947	0.999868	0.999736
Timing Generator and TMR Logic	0.999493	0.99825	0.99297
Subtotal - Computer	0.999440	0.998118	0.992708
8000-Word Memory	0.999233	0.99758	0.99357
Subtotal - Computer and 8000-Word Memory	0.998673	0.995703	0.986325
Power Supply	≅ 1	≅ 1	≅ 1
Subtotal - Computer Package	0.998673	0.995703	0.986325
Data Adapter (TMR)	0.99	0.9997	0.9989
Data Adapter (Duplex)	0.9995	0.9970	0.9885
TOTAL - SYSTEM	0.998074	0.992418	0.973910

Table II-7

SUMMARY OF SYSTEM RELIABILITY CALCULATIONS

a. Nonredundant (Simplex) Mode

Mission Time (hours)	Operating Temperature (°C) 100		75		60	
	R	MTBF (hours)	R	MTBF (hours)	R	MTBF (hours)
100	0.9221	1265.95	0.9285	1383.69	0.9319	1450.82
250	0.8165	1265.95	0.8311	1383.69	0.8385	1450.82
500	0.6667	1265.95	0.6907	1383.69	0.7030	1450.82

b. Redundant (Duplex) Mode

Mission Time (hours)	Operating Temperature (°C) 100		75		60	
	R	MTBF (eff. hours)*	R	MTBF (eff. hours)*	R	MTBF (eff. hours)*
100	0.9974	38,462.	0.9978	45,455.	0.9981	52,632
250	0.9901	25,253.	0.9914	29,070.	0.9924	32,895.
500	0.9664	14,881.	0.9710	17,241.	0.9739	19,157.

*Effective MTBF is defined as the MTBF required of a nonredundant machine to achieve the same reliability as the redundant machine for the mission length under consideration.

Section III

SATURN V COMPUTER

Section III

SATURN V COMPUTER

A. GENERAL DESCRIPTION

The Saturn V computer is a serial machine using a random access magnetic core memory. It uses microminiature packaging techniques, developed under the Advanced Saturn Technology program; triple modular redundancy in the central computer; and multiple duplex memory modules for high reliability. Glass delay lines are used for the serial arithmetic registers and for the storage of the instruction counter. The characteristics of the computer are summarized in Table III-1.

The Saturn V computer provides general purpose computing capability characterized by high internal computing speed and variable capacity random access core memory. The internal arithmetic structure employs both adder and multiplier units which may operate concurrently with a single program control unit. This arrangement provides operating speeds up to 40 percent greater than for a more conventional nonconcurrent arithmetic section at essentially no additional cost in components. To provide flexibility to the programmer and to conserve instruction words during the multiply process, an option is provided which permits or prohibits addition during multiplication under control of the programmer.

Memory words are 28 bits in length, (including two parity bits). The memory is arranged so that one data word or two instructions may occupy one 28-bit memory word. The memory uses fourteen 64 by 128 (4,096 words) magnetic core planes plus the required drive and sensing circuits. From one to eight memory modules may be used in the computer, providing flexibility in memory size for different Saturn missions. Independent memory modules may be used in duplex fashion for high reliability on long missions. This report assumes the use of 32,768 instruction words, or four modules. This memory space permits duplex operational capability, thus providing very high memory reliability.

Reliability of the central computer is ensured by the use of triple modular redundancy (TMR). The computer is divided into seven modules (defined in Table III-2), which are triplicated. Redundancy at this level provides reliability superior to the duplex equipment approach and raises fewer design problems than the use of quad components. Calculations and simulation show that by using TMR central computer logic and duplex memory operation for the mission phases, reliability of 0.9957 for 250 hours for the computer logic, memory and power supply is achieved.

Table III-1

SATURN V COMPUTER CHARACTERISTICS

Type	Stored program, general purpose, serial fixed point, binary
Clock	512 kilobits per second, 2.048 mc clock
Speed	Add-subtract and multiply-divide simultaneously:
Add Time, Accuracy	82 usec, 26 bits
Multiply Time, Accuracy	328 usec, 24 bits
Divide Time, Accuracy	656 usec, 24 bits
Storage capacity (4 memory modules)	16,384 26-bit words plus two parity bits expandable in 4,096-word modules to 32,768 words total. The memory modules may be used in simplex or duplex operation. Memory can be divided between program and data as desired, typically: 2,000 data words (25 bits and sign) 28,768 instructions (each 13 bits)
Input/Output	External - computer programmed I/O control
Component count (including 4 memory modules)	40,800 silicon semiconductors and cermet resistors; 458,752 ferrite cores
Temperature	60°F inlet coolant temperature; 100°C maximum junction temperature allowable
Reliability	0.996 probability of success for 250-hour mission using TMR logic and multiple duplex memory modules

Table III-1. Saturn V Computer Characteristics (cont)

Packaging	78 electronic page assemblies, four 4,096-word (28 plane) memory assemblies. Integral liquid cooling.
Weight	80 pounds (dry weight) including four 4,096-word memory assemblies
Volume	2.10 cubic feet
Power	138 watts

Table III-2

TMR COMPUTER MODULE BREAKDOWN

Module Number	Pages per Module	Module Name or Description
1	1	Computer Timing
2	2	Transfer Register
3	1	Arithmetic Unit
4	3 plus delay line	Multiply and Divide
5	1	Operation Code
6	3	Memory Address Register and Decoder
7	3	Memory Timing and Parity Check

The TMR system uses three identical simplex computer logic channels and subdivides each channel into seven functional modules. The outputs from each channel are voted upon in voter circuits before the signal is sent to another module. The output of the voter circuit is equal to the majority of the inputs to the circuit. Thus, even if one of the three inputs is incorrect, the output to the next module will be correct. Figure III-1 is an example of TMR voter signal outputs.

The voter circuits prevent the failure of one functional module from causing computer failure, because the computer modules are not dependent upon single modules for correct inputs.

Correct computations can be obtained, even with several malfunctions in the computer, through the use of the modularized computer and module output voting providing two identical modules are not in error.

This method will provide greater reliability than using three independent computers. If the outputs from three independent computers were compared, any malfunction in two of the computers would cause the computation to be in error.

An average of 13 output signals from each module are voted on. The voter circuit outputs may go to any of the other subdivided modules of the computer.

The Saturn V microminiature packaging permits the 40,800 components in the machine to be packaged into an 80-pound unit occupying 2.10 cubic feet.

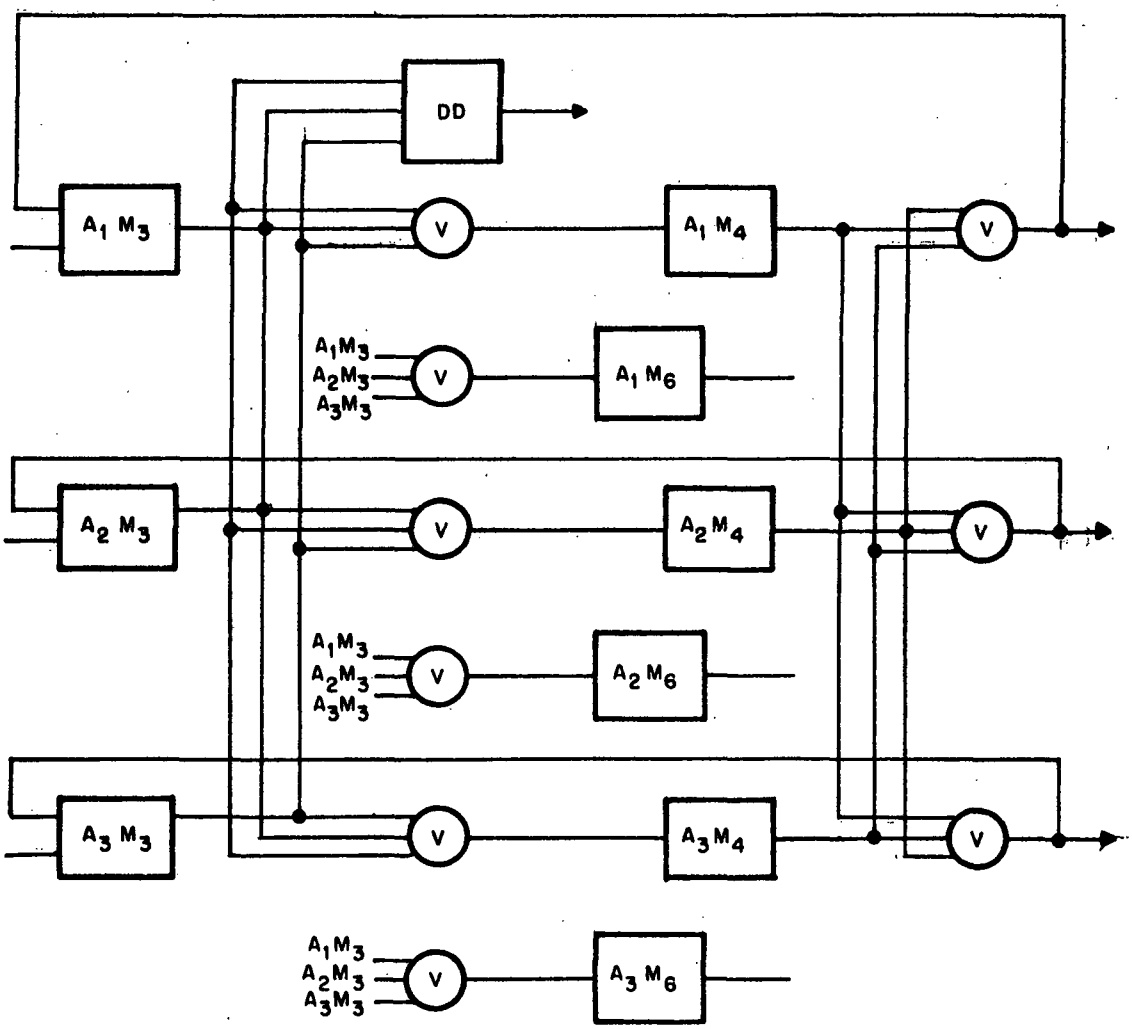


Figure III-1. TMR Voter Signal Outputs

Electronic circuits are mounted on 0.3 in. square wafers on which interconnection wiring and film resistors (cermet) have been deposited by silk screen printing and subsequent firing operations. These are known as Unit Logic Devices (ULD). They are attached to Multilayer Interconnection Boards (MIB) by solder reflow techniques. Each MIB has a capacity of 35 ULD's.

Two MIB's are bonded back-to-back to a supporting metal frame. This assembly comprises a page. Pages are interconnected by back panel multilayer printed circuit boards.

The central computer electronics units are packaged on 78 pages. A welded compartmentized liquid cooled structure houses the computer electronics units and delay line registers. Memory electronics units are mounted on MIB-type boards where possible. Each memory module is a self-contained unit with individual timing, control, drive, address, sense and inhibit circuitry.

TMR permits the subdivision of the computer into three simplex machines for testing purposes. Significant machine register signals are brought out to laboratory test equipment for troubleshooting during ground testing. The maintenance equipment will have the capability of observing register contents by use of panel lights, and will also be able to control the voltage connection of the voter circuits in each TMR module. This will permit using test programs to isolate malfunctions on a simplex level. Further malfunction isolation will make use of module switching, test lights, and maintenance probes.

Details of the computer design are discussed in the following sections, including aspects of logical organization, circuit design, maintainability, packaging design, and laboratory test equipment.

B. COMPUTER FUNCTIONAL DESCRIPTION

The computer information flow is illustrated in Figure III-2. This simplified block diagram depicts the major data flow paths and associated register level logic. The timing logic and I/O section are not shown, but are described in this section under the Instruction Sequencing and Computer I/O Capability portions.

1. CHARACTERISTICS

The computer is a serial, fixed point, stored program, general purpose machine which processes data using two's complement arithmetic. Two's complement arithmetic obviates the recomplementation cycle required

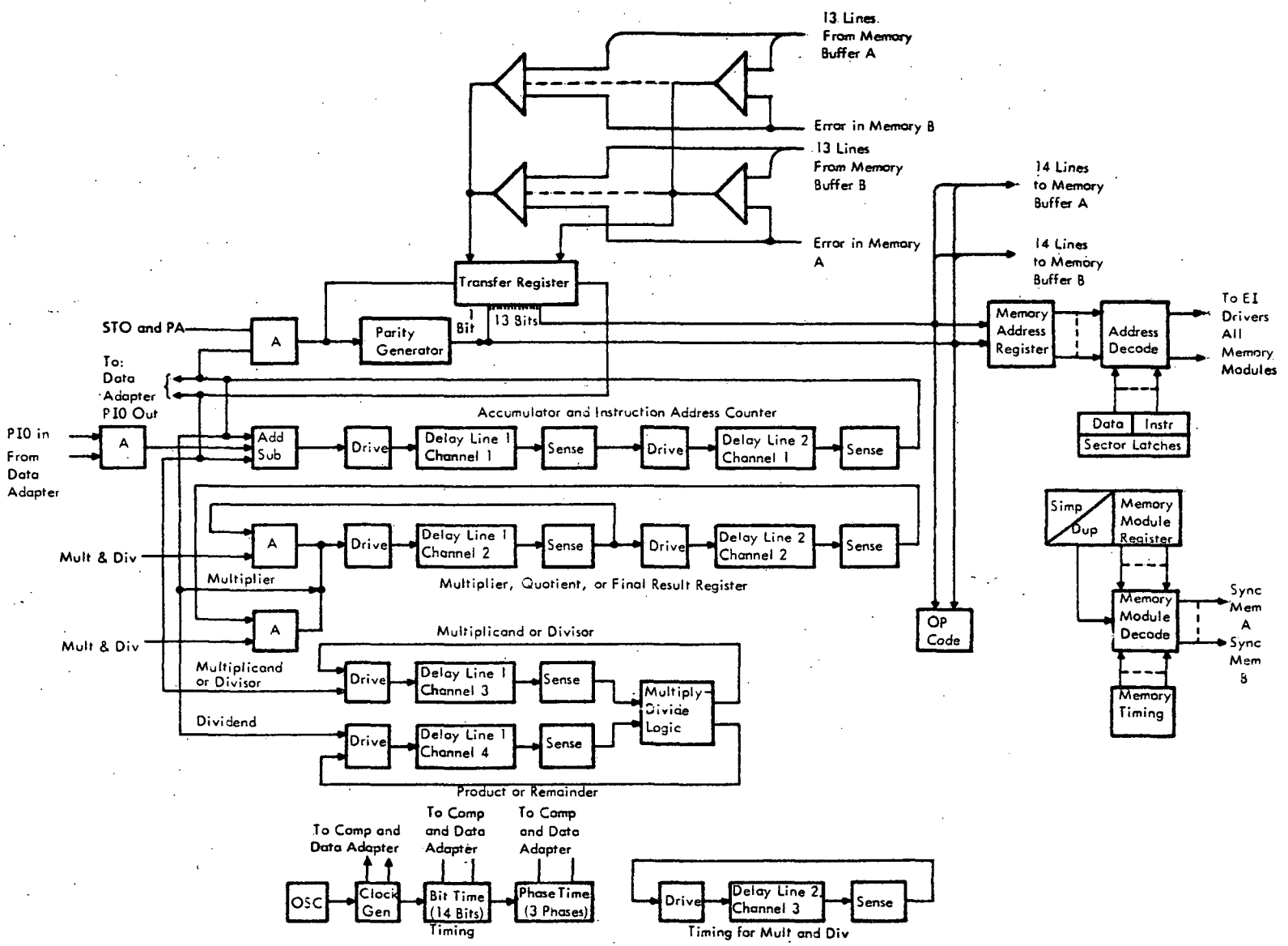


Figure III-2. Saturn V Guidance Computer Simplified Diagram

when using sign plus magnitude arithmetic. Special algorithms have been developed and implemented for multiplication and division of two's complement numbers. Multiplication is done four bits at a time and division two bits at a time. These algorithms are treated separately in the Arithmetic portion of this section.

A random access magnetic core memory is used as the computer storage unit. A serial data rate of 512 kilobits per second is maintained by operating the memory units in a serial by byte, parallel by bit operating mode. This allows the memory to work with a serial arithmetic unit. The parallel read-write word length of 14 bits includes one parity bit to allow checking of the memory operations.

Storage external to the memory is located predominantly in the shift register area. High reliability in this area is achieved by using glass delay lines for arithmetic registers and counters. Delay lines are the best choice when the number of transistors which would be required for the various registers is considered.

2. ORGANIZATION

Each instruction is comprised of a four-bit operation code and a nine-bit operand address. The nine-bit address allows 512 locations to be directly addressed. The total memory is divided into sectors of 256 words, and contains a residual memory of 256 words. The nine-bit address specifies a location in either the previously selected sector (data sector latches) or in the residual memory. If the operand address bit (R) is a binary 0, then the data will come from the sector specified by the sector register. If R is a 1 the data comes from residual memory.

Instructions are addressed from an eight-bit instruction counter which is augmented by a four-bit instruction sector register. Sector memory selection is changed by special instructions which change the contents of the sector register. Sector size is large enough so that this is not a frequent operation.

Data words consist of 26 bits. Instruction words consist of 13 bits and are stored in memory two instructions per data word. Hence, instructions are described as being stored in syllable one or syllable two of a memory word. Two additional bits are used in the memory to provide parity checking for each of the two syllables. (Refer to Table III-3.)

The computer is programmed by means of single-address instructions. Each instruction specifies an operation and an operand address. Instructions are addressed sequentially from memory under control of the instruction counter. Each time the instruction counter is used, it is incremented by one to develop the address of the next instruction. After the instruction is read from memory and parity checked, the operation code is sent from the transfer register to the OP code register, a static register which stores the operation code for the duration of the execution cycle.

Table III-3

DATA AND INSTRUCTION WORD FORMAT

Memory Plane	Syllable 2	1	2 ----------	13 14
	Syllable 1	15	16 ----------	27 28
Data Word	Syllable 2	S	2^{-1} ----------	2^{-12} P
	Syllable 1	2-13	2^{-14} ----------	2^{-25} P
Instruction Word	Syllable 1 or 2	A8	A7 --------	A1 R OP4 OP3 OP2 OP1 P

S . . . . . Sign Position
A8, A7, etc., ... Operand Address
R. . . . . Residual Bit
OP1, OP2, etc., ... Operation Codes
P. . . . . Parity Bit

The operand address portion of the instruction is transferred in parallel (9 bits) from the transfer register (TR) to the memory address register. The TR is then cleared.

If the operation code requires reading the memory, the contents of the operand address are read 14 bits at a time (including parity) from the memory into the buffer register where a parity check is made. Data bits are then sent in parallel to the TR. This information is then serially transferred to the arithmetic section of the computer. If the operation code is a store (STO), the contents of the accumulator are transferred serially into the TR and stored in two 14-bit bytes. A parity bit is generated for each byte.

Upon completion of the arithmetic operation, the contents of the instruction counter are transferred serially into the TR. This information is then transferred in parallel (just as the operand address had previously been transferred) into the memory address register. The TR is then cleared and the next instruction is read, thus completing one computer cycle.

The data word is read from the memory address specified by the memory address register and from the sector specified by the sector register. Data from the memory goes directly to the arithmetic section of the computer where it is operated on as directed by the OP code.

The arithmetic section contains an add-subtract element, a multiply-divide element, and storage registers for the operands. Registers are required for the accumulator, product, quotient, multiplicand, multiplier, positive remainder and negative remainder. The add-subtract and the multiply-divide elements operate independently of each other. Therefore, they can be programmed to operate concurrently if desired; i.e., the add-subtract element can do several short operations while the multiply-divide element is in operation.

No dividend register is shown in Figure III-2 because it is considered to be the first remainder. The divisor is read from the accumulator during the first cycle time and can be regenerated from the two remainders on subsequent cycles. As indicated, both multiply and divide require more time for execution than the rest of the computer operations. A special counter is used to keep track of the multiply-divide progress and stop the operation when completed. The product-quotient (PQ) register has been assigned an address and is addressable from the operand address of any instruction. The answer will remain in the PQ register until another multiply-divide is initiated.

3. TIMING

The three levels of computer timing are illustrated in Figure III-3. Basically, the computer is organized around a four clock system. The width of each clock is approximately 0.4 usec and the pulse repetition frequency is 512 kilocycles. The bit time (four clock pulses) is 1.95 microseconds. Fourteen bit times occur in one phase time, resulting in a phase time of 27.3 microseconds. Three-phase times, P_A, P_B, and P_C are required to perform a complete computer operation cycle. Phase A (P_A) makes up the instruction cycle and phases B and C (P_B and P_C) make up the data cycle.

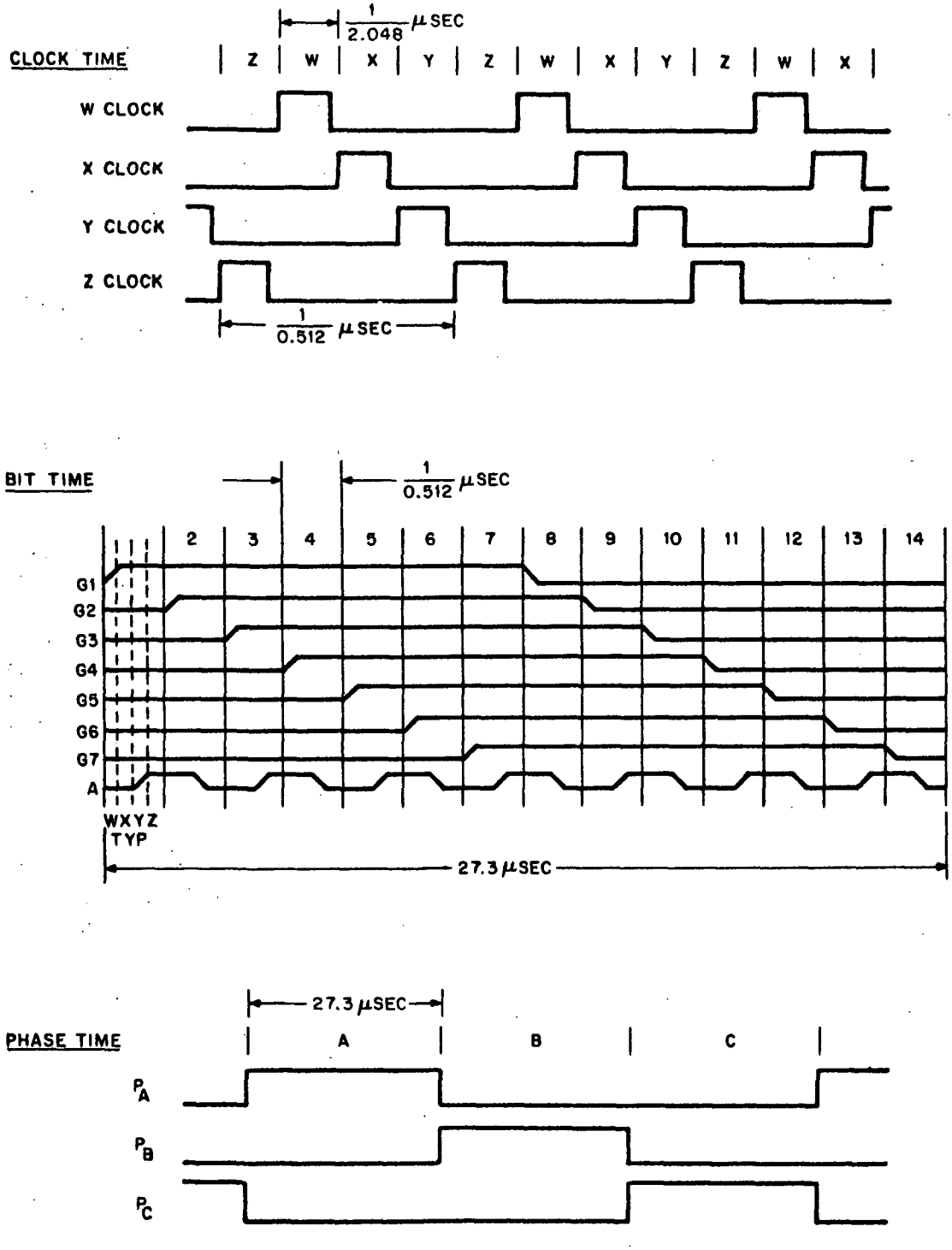


Figure III-3. Computer Timing

C. COMPUTER CONTROL

1. INSTRUCTION LIST

The instruction bit assignment for the operation codes is shown in Table III-4.

Table III-4

OPERATION CODE MAP

OP1 \ OP2				
	MPY		STO	DIV
	MPH	XOR	CLA	ADD
	TNZ	TMI	SHF	AND
	HOP	TRA	PIO	SUB

OP3

OP4

HOP (82 usec) 0000 — The contents of the memory address specified by the operand address specify the next instruction address and data sector. Four bits identify the next instruction sector, eight bits are transferred to the instruction address counter, one bit conditions the syllable control, four bits identify the next data sector, three bits identify the next memory module, one bit defines either simplex or duplex memory operation, and one bit resets the memory error latch when specifying a new memory module.

TRA (82 usec) 1000 — The eight-bit operand address is transferred to the instruction counter. The residual bit in the operand address is used to specify the instruction syllable latch. The sector register remains unchanged.

TMI (82 usec) 1100 — A transfer occurs on the minus accumulator sign. If the sign is positive (zero is considered positive), the next instruction in sequence is chosen (no branch); if the sign is negative, the eight bits of operand address become the next instruction address (perform branch), and a TRA operation is executed.

TNZ
(82 usec)
0100

A transfer occurs when the accumulator contains a nonzero number. If the accumulator is zero, the next instruction in sequence is chosen; if the accumulator is not zero (either negative or positive), the eight bits of the operand address become the next instruction address, and a TRA operation is executed.

SHF
(82 usec)
1110

The SHF instruction shifts the accumulator contents right or left one or two places as specified by the operand address.

A1 Right Shift 1	A5 Left Shift 1
A2 Right Shift 2	A6 Left Shift 2

AND
(82 usec)
0110

The contents of the memory location specified by the operand address are logically AND'ed, bit-by-bit, with the accumulator contents. The result is retained in the accumulator.

CLA
(82 usec)
1111

The contents of the location specified by the operand address are transferred to the accumulator.

ADD
(82 usec)
0111

The contents of the location specified by the operand address are added to the accumulator contents. The result is retained in the accumulator.

SUB
(82 usec)
0010

The contents of the location specified by the operand address are subtracted from the accumulator contents. The result is retained in the accumulator.

STO
(82 usec)
1011

The contents of the accumulator are stored in the location specified by the operand address. The contents of the accumulator are retained.

DIV
(656 usec)
0011

The contents of the accumulator are divided by the contents of the register specified by the operand address. The 24-bit quotient is in the product-quotient delay line. Concurrent use of the adder-subtracter element is required.

MPY
(328 usec)
0001

The contents of the memory location specified by the operand address are multiplied by the accumulator contents. The 24 high-order bits of the multiplier and multiplicand are multiplied together to form a 24-bit product. Concurrent use of the add-subtract element is required. The product is stored in the product-quotient register.

MPH (410 usec) 0101	This is the multiply and hold operation. It is the same as the MPY operation except concurrent use of the add-subtract element is not permitted and the product is stored in the accumulator.
XOR (82 usec) 1101	The contents of the memory location specified by the operand address are exclusively OR'd, bit-by-bit, with the contents of the accumulator. The result is retained in the accumulator.
PIO (82 usec) 1010	The low order address bits, A1 and A2, determine whether the operation is an input or output instruction. The high order address bits, A8 and A9, determine whether the data contents are transferred from the main memory, residual memory or accumulator.

2. MULTIPLY AND DIVIDE TIMING

All operations except MPY, MPH and DIV require one operational cycle (82 microseconds) for execution. The MPY and DIV instructions must be executed concurrently with any of the other instructions (except MPH). Three instructions can be executed between the start on the MPY and the time when the product is available; similarly seven instructions can be executed between the start and finish of DIV.

More one-word-time instructions can be inserted before the product or quotient is addressed if maximum efficiency is not required since multiplication or division is stopped automatically and the result retained until addressed. Figure III-4 illustrates the timing of the MPY and DIV operations.

The MPH instruction inhibits further access to memory until completed, and cannot be operated concurrently with other operations.

3. INTERRUPT

A limited program interrupt feature is provided to aid the input/output processing. An external signal can interrupt the computer program and cause a transfer to a subprogram. Interrupt occurs when the instruction in progress is completed. The instruction counter, sector and module registers, and syllable latch are stored automatically in a reserved residual memory location (octal address 777). A HOP constant is retrieved from a second reserved residual memory location (octal address 776). The HOP constant designates the start of the subprogram. Automatic storage of the accumulator and product-quotient registers is not provided. This must be accomplished by the subprogram. Protection against multiple interrupts and interrupts during MPY and DIV operations is provided.

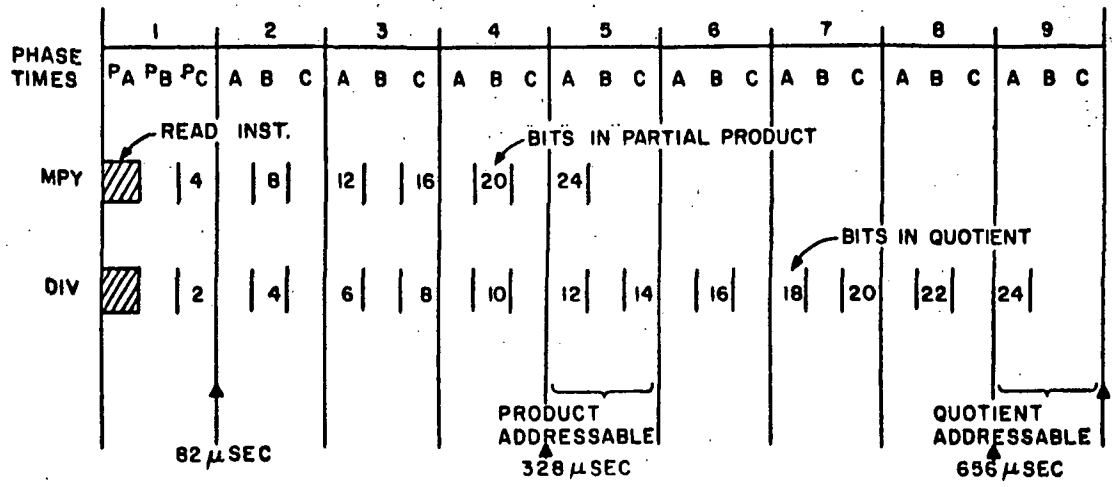


Figure III-4. MPY-DIV Timing Chart

The interrupt signal may be generated by a timed source. The rate at which it is generated is controlled by changing the magnitude of a number which is being continually summed. When the summed number reaches a predetermined value, the interrupt signal is generated. This is accomplished in the Saturn V Data Adapter (DA) equipment.

The main program can be resumed by addressing the contents of residual memory word 777 with a HOP instruction.

Certain discrete input signals are allowed to cause interrupt. These are useful in causing the I/O subprogram to give immediate attention to an input or output operation.

4. PROGRAMMING CONSIDERATIONS

The Saturn V Guidance Computer uses a conventional complement of arithmetic instructions including add, subtract, multiply, and divide. Two multiply instructions are included. MPY requires that one-word-time operations be performed in the adder unit during the multiplication process because the instruction counter advances each word-time. This procedure speeds up the computer operation by permitting simultaneous multiplication and one-word operations. Trial programming has shown a speed increase of up to 40 percent over a conventional sequential computer.

When the program is multiply-limited, and a sufficient number of useful one-word operations cannot be located in the portion of the flow diagram being executed, the MPH instruction is used. This instruction inhibits advance of the instruction counter so no new instructions are read from memory until the operation is completed. This feature conserves program steps. Having both types of multiply instructions permits the increased speed of concurrent operation without sacrifice in the number of program steps required, and permits a programming tradeoff of speed and number of instructions required.

TRA, TMI, and TNZ instructions provide flexibility in programming unconditional transfers; in branch instructions, through transfer of the contents of the accumulator; and in easy handling of discrete inputs, which are obtained in the accumulator through masking with an AND instruction.

The HOP instruction is used for transfers outside of the sector currently being used. HOP permits jumping to another portion of the flow diagram and to subroutines. To return from a subroutine, the last instruction in the routine is a HOP. The HOP constant causes a return to the original program sequence. Since each use of a subroutine in the program results in return to a different place in the flow diagram, the HOP constant is loaded prior to entering the subroutine. An automatic program compiler is used to generate the correct HOP constants.

An exclusive OR operation, XOR, is provided to permit the rapid checking of changes in discrete inputs, which are grouped into data-word inputs. Discrete output words may be generated by masking out the bit to be changed with an AND instruction and adding the discrete output into the selected position.

The product-quotient (P-Q) register can be addressed (by Octal 775) with the operations CLA, ADD, SUB, STO, AND and XOR.

The interrupt feature in the guidance computer facilitates the timing of input-output operations by causing a transfer to an input-output subprogram. The interrupt signal is generated in the DA and may be set to interrupt at the highest rate at which any I/O quantity must be handled. This method avoids the necessity of keeping track of time expired since last entering the I/O subprogram.

The automatic interrupt also makes it possible to permit certain discrete inputs to cause interrupt. Allowing discrete inputs to interrupt makes it possible to demand that the program give attention to an important discrete input. Communications between the guidance computer and the vehicle telemetry monitoring system are thus facilitated.

The vehicle monitor system is selected by an address code from the computer. The definition of which vehicle parameter is to be monitored is given over the output lines to the DA and stored in a buffer register. When the monitor has acquired the desired parameter, an interrupt is generated causing the computer I/O subprogram to read the value of the parameter as an input. This scheme permits computing to continue while waiting for the monitor system to acquire the parameter.

The data sector register permits considerable flexibility in the handling of data and constants. Instructions indicate whether data is located in the residual sector or the sector referred to by the data sector register. By confining data to the residual register and a limited number of memory sectors, the changing of the data sector register can be minimized. The residual sector is then made more readily usable for data referred to by instructions stored in many sectors. The small size of each sector, achieved by concentrating instructions rather than both data and instructions in each sector, reduces the size of the instruction word and conserves memory core planes. The programmer is free to move between separate parts of the program without frequently changing instruction or data sector registers.

The data sector register is also useful in addressing sets of constants stored for use with polynomial injection guidance equations. The instructions necessary to compute the polynomials are stored once. Sets of coefficients for the many different polynomials are each stored in different memory sectors. The coefficients can be readily retrieved by use of the data address register, which is set to select a given set of coefficients in the evaluation of the polynomial. Thus, the location of the polynomial number is set in the sector register and the coefficients are selected.

The separate instructions and data sector register feature eliminates the need for indexing, since it accomplishes the same end result in polynomial evaluation, the chief application of indexing. Hardware and instruction bits are saved by omitting indexing.

Upper and lower limits for orbital checkout parameters are stored in the two halves of a data word. Addressing of the parameter through the monitoring system is related to the storage location of the limits in memory. A simple, regular sequence of addresses makes programming easy by the use of address modification techniques.

D. ARITHMETIC SECTION

1. GENERAL

The Saturn V Computer has two independent arithmetic elements, the add-subtract element and the multiply-divide element. Although both operate

independently, they are serviced by the same program control circuits and may be operated concurrently. During each program cycle-time, the add-subtract element can perform any one of the computer instructions, except MPY, MPH, and DIV. Also during each program cycle-time, the results of the simple arithmetic operations are circulated through the accumulator delay line and through the accumulator sync delay line channel to prevent precessing of the results.

The multiply-divide element uses three channels of a delay line as shown in Figure III-3. One channel of the instruction counter delay line is used as a counter to stop the multiply or divide operations. Another channel of the instruction counter delay line is used to synchronize the product or quotient when the operation is completed. This is controlled automatically by the counter.

The product-quotient register is addressable as a residual memory word and has the octal address 775. The product or quotient can be obtained on any subsequent operation cycle after completion of the multiply or divide operation, but must be used before initiation of another multiply or divide operation. The product of the MPH operation is stored in the accumulator.

The recursion formulas for implementing multiply and divide instructions with two's complement numbers are explained in the following paragraphs:

2. MULTIPLY

The multiply element operates in a two-phase cycle, serial-by-four parallel, and requires 15 phase times, including instruction access time. The program initiates a multiply by placing the 24 high-order bits of the contents of the memory location specified by the operand address into the multiplicand delay line. The multiplier delay line contains the 24 high-order bits of the contents of the accumulator. The phase counter terminates a multiply instruction.

The instrumentation of the multiply algorithm requires three delay line channels. Two of the channels contain the partial product and the multiplier. These channels shift both the partial product and the multiplier four places to the right every two-phase cycle. The third channel contains the multiplicand. The accumulator portion (fourth channel) of this delay line is not involved in the multiply operation and can be used concurrently with the multiply operation.

Upon initiation of a multiply and during every other phase time thereafter, the five low-order bits of the multiplier (MR_1, MR_2, MR_3, MR_4, and MR_5) are placed in latches or tratches and are used to condition addition or subtraction of multiples of the multiplicand to the partial product.

The following algorithm is utilized for multiply:

$$P_i = 1/16 \left[P_{(i-1)} + \Delta 1 + \Delta 2 \right]$$

P_i is the new partial product, and $\Delta 1$ and $\Delta 2$ are formed according to the rules:

MR_1	MR_2	MR_3	$\Delta 1$	
MR_3	MR_4	MR_5		$\Delta 2$
0	0	0	0	0
1	0	0	+2M	+8M
0	1	0	+2M	+8M
1	1	0	+4M	+16M
0	0	1	-4M	-16M
1	0	1	-2M	-8M
0	1	1	-2M	-8M
1	1	1	0	0

M represents the multiplicand. For the first multiplication cycle $P_{(i-1)}$ and MR_1 are made zeros.

3. DIVIDE

The divide element operates in a two-phase cycle, serial-by-two-parallel, and requires 27 phase times per divide, including instruction access time. The program initiates a divide by transferring the 26 bits of the addressed memory location (divisor) and the 26 bits of the accumulator (dividend) to the divide element. The phase counter terminates a divide operation.

The following algorithm is instrumented to execute divide:

$$Q_i = R_{is} \cdot DV_s + \overline{R_{is}} \cdot \overline{DV_s} \quad (1)$$

and

$$R_{i+1} = 2R_i + (1 - 2Q_i)\, DV \quad (2)$$

where:

i = 1, 2, 3, ...24

Q_i = The i^{th} quotient bit

R_{is} = The sign of the i^{th} remainder

DV_s = The sign of the divisor

R_i = The i^{th} remainder

R_1 = The dividend

DV = The divisor

Equation (1) states that the i^{th} quotient bit is equal to a "1" if the sign of the i^{th} remainder is identical to the sign of the divisor. The high-order quotient bit (sign bit) is the only exception to this rule. Q_i as determined by equation (1) is used to solve equation (2) but must be complemented before it is stored as the sign bit of the quotient.

The instrumentation of the divide algorithm requires three channels of a delay line. One channel contains the quotient; one the divisor; and one the dividend. These three channels are used during multiply to contain the multiplier, the multiplicand, and the partial product respectively. The quotient and the remainder channels of the delay line have been lengthened by latches to shift two places to the left each two-phase cycle. The divisor circulates once each two-phase cycle.

In the two's complement number system, the high-order bit determines the sign of the number. Since this is the last bit read from memory, it is impossible to solve Equations (1) or (2) until the entire divisor has been read from memory. However, Equations (1) and (2) can have only two possible solutions.

Either,

$$Q_i = 1$$

and,

$$R_{(i+1)} = 2R_i - DV$$

or,

$$Q_i = 0$$

and,

$$R_{(i+1)} = 2R_i + DV$$

Both the borrow of $2R_i - DV$ and the carry of $2R_i + DV$ are generated as the dividend and divisor registers are loaded. When the sign bits of these quantities are finally entered into their respective registers, Equation (1) is solved for the first quotient bit. If this quotient bit is a one, the borrow is examined to determine the second quotient bit. If the first quotient bit is a zero, the carry is examined to determine the second quotient bit. The following truth table is solved to determine the second quotient bit if the first quotient bit is a one.

R_i	DV_S	B	$R_{(i+1)_S}$	Q
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Where

R_i = The first remainder bit to the right of the sign bit

DV_S = The divisor sign

B = The borrow into the R_i, DV_S position

$R_{(i+1)_S}$ = The sign of the new remainder

Q = The quotient bit as determined by comparing DV_S with $R_{(i+1)_S}$ according to Equation (2).

$$Q = \overline{R}_i \overline{DV}_S \cdot \overline{B} + \overline{R}_i DV_S \overline{B} + R_i \cdot \overline{DV}_S \cdot B + R_i \cdot DV_S \cdot B$$

$$= \overline{R}_i \cdot \overline{B} (\overline{DV}_S + DV_S) + R_i \cdot B (\overline{DV}_S + DV_S)$$

$$= \overline{R}_i \cdot \overline{B} + R_i \cdot B$$

The equation used in generating the new remainder, R_{i+2}, is obtained by expanding Equation (2)

$$R_{(i+2)} = 2R_{(i+1)} + (1 - 2Q_{(i+1)})\ DV$$

$$R_{(i+2)} = 2\left[2R_i + (1 - 2Q_i)\ DV\right] + (1 - 2Q_{(i+1)})\ DV$$

$$R_{(i+2)} = 4R_i + 2\ (1 - 2Q_i)\ DV + (1 - 2Q_{i+1})\ DV$$

As $R_{(i+2)}$ is being generated, the next iteration of divide is started by generating, as already described, the borrow and carry for $2R_{i+2} \pm DV$.

E. MEMORY

The memory for the Saturn V Guidance Computer uses conventional toroidal cores in a unique self-correcting duplex system for achieving a memory reliability of 0.9976 for 250 hours of duplex operation or 0.958 for 250 hours when operating simplex (for 8000 words of memory). The memory consists of four identical 4096-word memory modules which may be operated in simplex for increased storage capability or in duplex pairs for high reliability. The basic computer program is loaded at electronic speeds into the instruction and constants sectors of the memory on the ground just prior to launch. Thereafter, the information content of constants and data can be electrically altered, but only under control of the computer program.

The self-correcting duplex system uses an odd-even parity bit detection scheme in conjunction with memory drive current error detection circuitry for malfunction indication and correction. Unlike conventional toroid random access memories, the self-correcting extension of the basic duplex approach permits regeneration of correct information after transients or intermittent failures which otherwise would result in destructive read-out of the memory.

F. BASIC MEMORY SYSTEM OPERATION

Figure III-5 is a simplified block diagram of the computer memory system. The configuration consists of a pair of memories providing storage for 8192 14-bit memory words when operating duplex, or 16,384 14-bit memory words when simplex operation is desired. Each of the simplex memories includes independent peripheral instrumentation consisting of timing, control, address drivers, inhibit drivers, sense amplifiers, error detection circuitry and I/O connections to facilitate failure isolation. Computer functions common to these simplex units consist of the following:

- Memory address register outputs
- Memory transfer register input-output
- Store gate command
- Read gate command
- Syllable control gates

Computer functions, which are separate for each simplex memory, consist of the synchronizing gates, which provide conversion of the serial data rate of 512 kilobits per second required by the computer to generate a start memory unit command at 128 kilobits per second. These gates also provide selection of multiple simplex memory units for storage flexibility and permit partial or total duplex operation throughout the mission profile for purposes of extending the mean-time-before-failure for long mission times. Each of the simplex units can operate independently of the others or in a duplex manner.

Memory modules are divided into two groups, one group consisting of even numbered moduled (0-6), the other consisting of odd numbered modules (1-7). A buffer register associated with each group is set by the selected modules.

For duplex operation, as shown in Figure III-5, each memory is under control of independent buffer registers when both memories are operating without failure. Both memories are simultaneously read and updated in parallel (14 bits). A single cycle is required for reading instructions (13 bits plus 1 parity bit per instruction word). Two memory cycles are required for reading and updating data (26 bits plus 2 parity bits).

The parallel outputs of the memory buffer registers are serialized at a 512-kilobit rate at the memory transfer register under control of the memory select logic. Initially, the outputs of only one buffer register are being used with simultaneous parallel parity checking being performed on both register outputs. When an error is detected in the memory being used, operation immediately transfers to the other memory. Both memories are then regenerated by the buffer register of the "good" memory, thus correcting transient errors.

After the parity-checking and error detection circuits have verified that the erroneous memory has been corrected, operation returns to the condition where each memory is under control of its own buffer register. Operation is not transferred to the previously erroneous memory until the "good" memory develops its first error. Consequently, instantaneous switching from one memory output to another permits uninterrupted computer operation until simultaneous failures at the same location in both memories cause complete system failure.

Proper operation of the memory system during read cycles is indicated by each 14-bit word containing an odd number of "one's" and a logical "one" output of the error detecting circuitry. If either or both of these conditions are violated, operation is transferred to the other memory.

During regenerate or store cycles parity checking cannot be performed. Failure detection is accomplished by the error detection circuitry only. Parity checking is performed during subsequent read cycles.

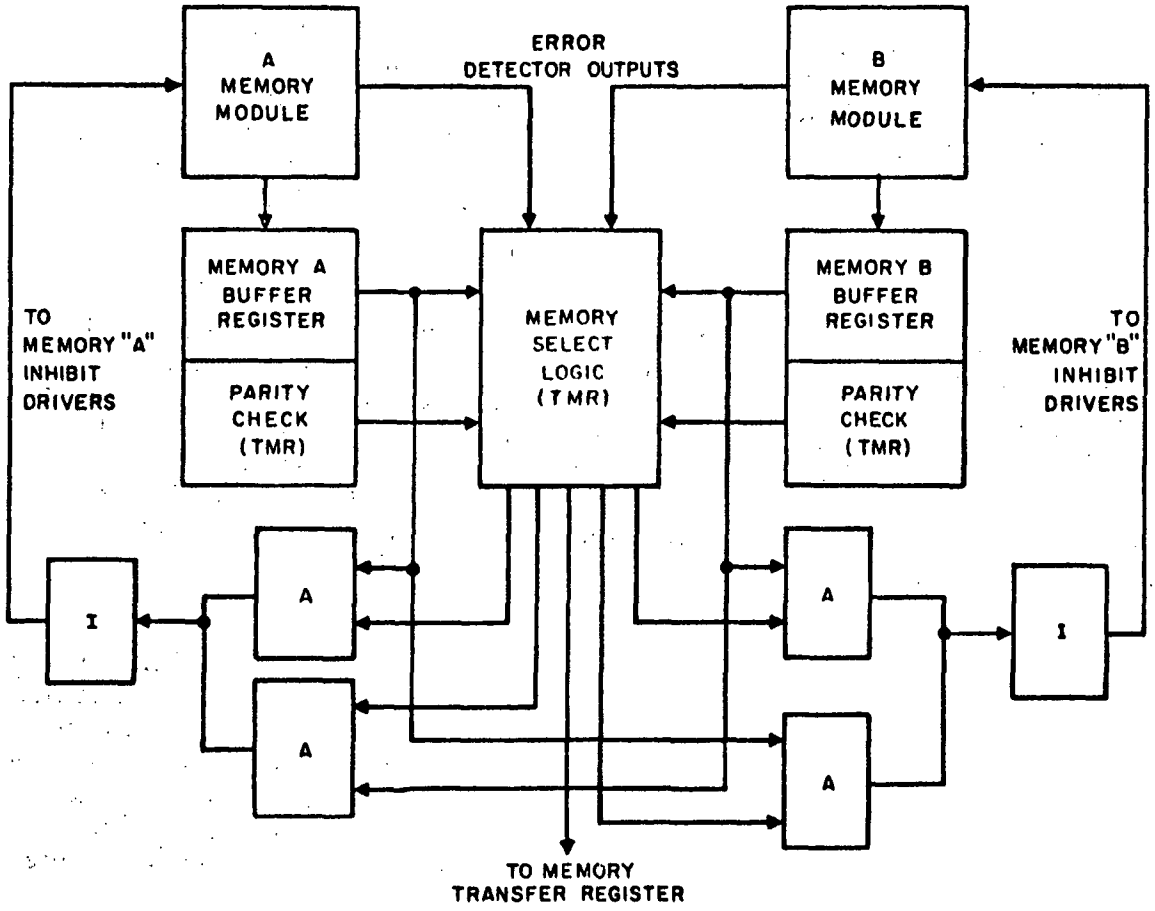


Figure III-5. Self-Correcting Duplex-Toroid Memory System

Intermittent addressing of memory between normal cycles is detected by the error detecting circuitry producing a logical "one" output at the improper time. Figure III-6 indicates the system connection of the error detector circuits for a simplex memory.

The control latch circuits are packaged with the buffer register circuitry in the computer. The output latch is in a logical "zero" state for normal operation. If the error detector output is a logical "zero" at normal cycle times, or a logical "one" at the improper time, the output latch is set to the "one" state indicating an error. Conditions which will result in an error output are as follows:

Address without voltage source

Address without current sink

No address

Dual source-single sink address

Single source-dual sink address

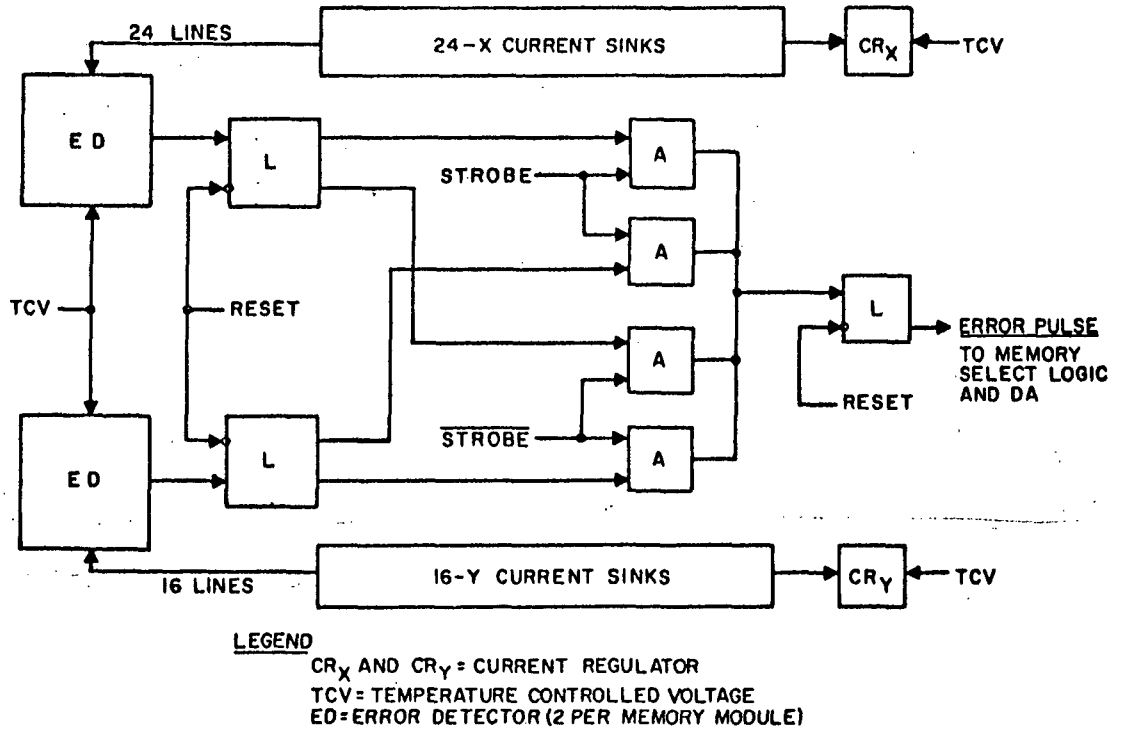


Figure III-6. X-Y Coordinate Half-Select Current Error Detection

G. COMPUTER INPUT/OUTPUT CAPABILITY

1. GENERAL

The computer input/output capabilities are characterized by the input/output instruction and the interrupt feature. The Process Input/Output (PIO) instruction provides for transferring of a single word into or out of the accumulator or out of the memory.

The primary input/output interface will be between the computer and the DA. The DA will perform all conversion (analog-to-digital and digital-to-analog) required by the system.

2. PIO INSTRUCTION

The PIO instruction transfers data between the accumulator or memory and one-word registers and delay lines located in the DA or other subsystem. The operand address is used to select the desired register.

Discrete inputs and outputs can be processed by this instruction. It is possible to pack 26 discrete signals into one word. The XOR instruction will determine if any of the 26 discrete inputs has changed state. The AND instruction is used to set or reset any of the discrete outputs.

3. INTERRUPT

Interrupt signals can be generated within the DA. These signals will stop the computer program and cause a branch to a subprogram. The location of the subprogram is program-controlled and is dependent upon the HOP constant stored in a specific memory location. This subprogram will normally be used to process a block of input-output data on a periodic basis. The rate at which the timed interrupt occurs is also program-controlled and can be adjusted as dictated by the various modes of operation during a given mission.

The main program can be resumed after completion of the subprogram by executing a HOP operation from another specified memory location. This location will contain the contents of the instruction counter, sector register, and syllable latch, which were stored there when the interrupt occurred.

H. LOGIC CIRCUITS

1. DESIGN

Many different logic circuit techniques were evaluated before the final circuit configuration was chosen. The circuit configuration, a form of current switching diode logic, was found to have these advantages (listed in order of importance):

- Reliability: The circuits are inherently simple and are capable of yielding large component drift allowances in a large percentage of logical applications.
- Low Power: The circuit is designed to minimize power by sacrificing only the very high speeds. Also, many of the AND resistors are clocked and, hence, need power only when they are interrogated.

- Speed: Signal voltage levels are kept as low as possible to achieve relatively high speeds without sacrificing power.

Most of the computer circuits use ultra-high-speed silicon planar epitaxial transistors and dual silicon planar diodes.

Simultaneous worst-case design was used for all of the circuits. This takes into account supply voltages, input responses and levels, environmental conditions, and component drift with life. The end-of-life component conditions are determined from environmental and operating life testing. Circuits are designed, where applicable, such that input signal noise, power supply noise, and output signal noise, may all occur simultaneously without causing circuit failure.

Release of a circuit for production was made only after laboratory evaluation verified circuit performance of a circuit breadboard consisting of selected worst-case components.

The number of different circuit types utilized has been minimized. One standard inverter circuit serves the logical inversion function and, in conjunction with standard AND-OR diode logic circuits, is instrumented to serve as a latch, the equivalent of a flip-flop. Buffer storage circuits of the latch type have the advantages of being d-c coupled, and relatively insensitive to noise. In addition, these circuit types do not require critical input signal response times.

2. BASIC LOGIC CIRCUITS

The basic logic circuits consist of an AND-OR-INVERT circuit family which uses diode logic and a transistor, operated in the saturated and cut-off modes. The logic circuits are designed to operate at 512 kilocycles in a four clock-per-bit system. The computer clocks synchronously gate logic signals by applying a six volt pulse to the AND resistors. Clocking the AND resistor, together with proper selection of the clock down level, allows increased capability of the inverter through time-sharing of loads and also eliminates the need for an AND diode for each clocked AND.

The logic ground rules provide that an AND may have up to ten logic inputs in addition to a clock; an OR may have up to four inputs. Since the inverter load is phased with respect to the inverter drive, there are two values available for the AND resistor. When the inverter is driven by a 2.5k AND, it may drive five 2.5k ANDS or three 1.5k ANDS. When the inverter is driven by a 1.5k AND, it may drive 16 2.5k ANDS or ten 1.5K ANDS. The AND loads may be a mixture of two AND resistor values where a 2.5K AND is equivalent to three-fifths of a 1.5K AND in terms of

loading. The availability of two AND resistor values has the net effect of allowing one inverter to perform functions which would normally require two inverters. The inverter AND loads, in addition to being phased with respect to the drive, may occur at different clock times and may then be time-shared. This results because an AND with its clock input in the down state presents no loading on an inverter. The principle of time-sharing may also be used to extend the number of allowable OR inputs. Also, a 2.5k AND is equivalent to half a 1.5k AND in terms of OR fan-in. Thus, the OR fan-in may be as high as eight at any one clock time.

The layout of the logic circuits was limited by basic design needs. The choice of a 0.3 inch ULD substrate dictated that only 12 of the available ULD connections could be used. The number of different types of ULD's has been minimized and all logical connective functions are satisfied with a minimum of ULD's.

Examples of the two highest usage blocks are shown in Figures III-7 and III-8. Figure III-7 shows an INV module which contains an inverter with a permanently connected 1.5k AND and an extra 2.5k AND. Two INV modules are required to form a latch. The AA module of Figure III-8 is used to obtain AND and OR diodes and AND resistors. For example, the AA module may be used to obtain two three-input 2.5k AND's with two OR diodes, a seven-input 2.5k AND with one OR diode, or just to obtain eight AND diodes. The versatility of these modules allows just two modules to satisfy all logic connections with minimum waste of unused components.

I. SPECIAL CIRCUITS

1. GENERAL

In addition to the basic logic circuits, several other special circuits are required by the computer. These circuits are associated with delay lines, timing generation, memory, and input and output functions. They are referred to as special since they are designed for a unique function, and usually have only limited usage.

2. VOTER CIRCUIT

A voter circuit is required to instrument triple modular redundancy. The following requirements are imposed on the voter circuit by TMR:

- The voter output must represent the majority of three inputs.
- The voter reliability must be as high as possible because of the influence of voter reliability on overall computer reliability.

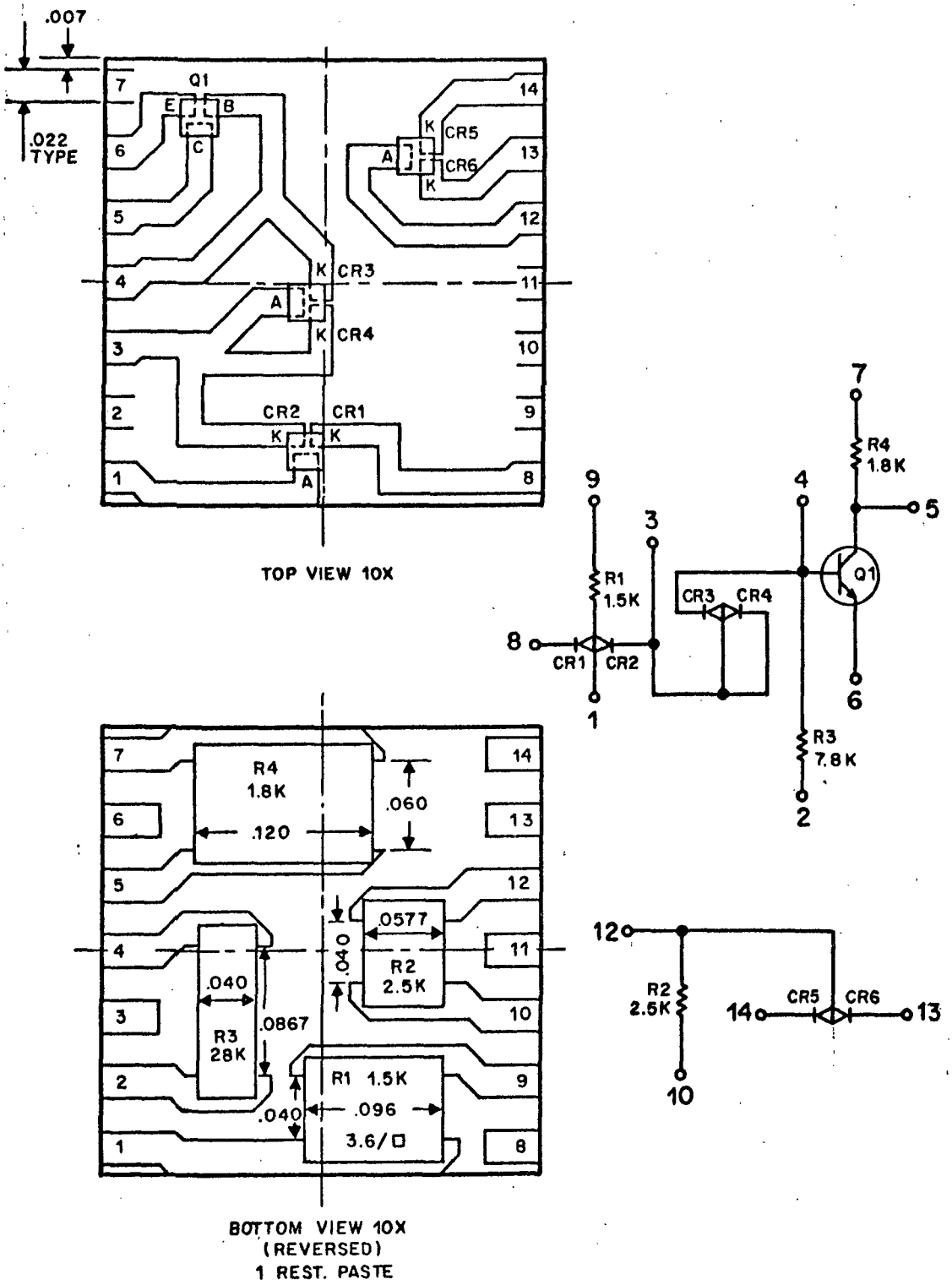


Figure III-7. INV Module

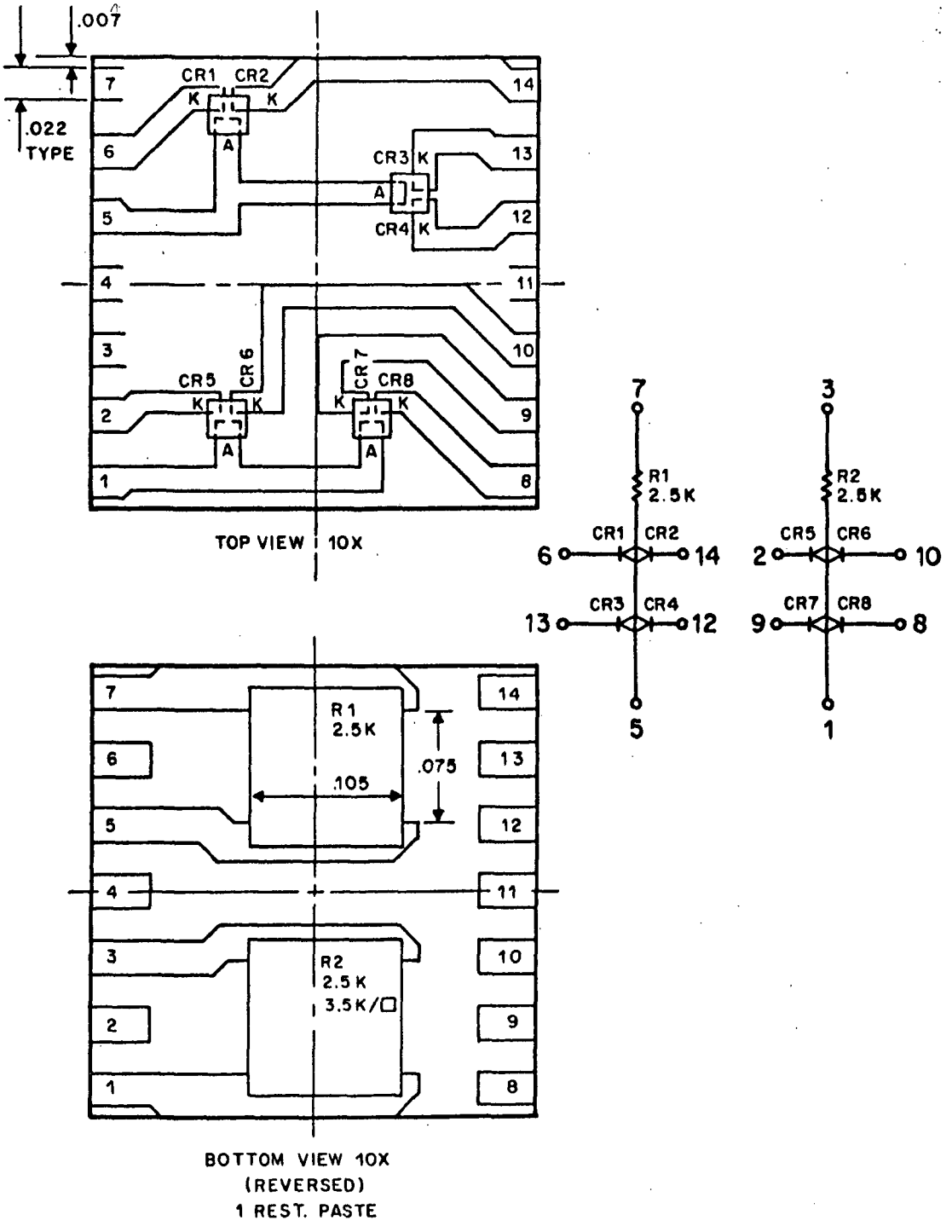


Figure III-8. AA Module

- The signal delay through the voter circuit must be small enough so that the complexity of the nonredundant module is not increased when the voter is added.

- The voting circuit requires a juncture of the three module outputs. This juncture must be so constructed that a failure of one module cannot possibly affect either of the other two modules. Also, the failure of a voter component must not cause failure of a module and thus cause failure of other outputs of that module.

- The voter circuit must be capable of operating in simplex mode, in the interest of computer checkout.

The voter circuit consists of a current summing network which is sensed by an inverter. The output of the inverter is then amplified with an additional inverter to supply an output capable of driving ten 1.5k AND's. A power voter is also available which amplifies the inverter output to a capability of twenty 1.5k AND's. The delay through the voter circuits is less than one clock time by the amount of allowable skew between clocks of the three clock channels.

3. DISAGREEMENT DETECTOR

Disagreement detectors provide an output if any of the triplicated modules fail. The disagreement detector consists of a three-way exclusive OR, which is connected to each set of outputs of each trio of modules. There are approximately two-hundred disagreement detectors in the Saturn V Guidance Computer. The outputs of several disagreement detectors are OR'd together to provide fewer outputs to the DA where a register stores disagreement detector outputs for transmission over telemetry. The inputs to the disagreement detectors are clocked to allow time for the inputs to reach steady state conditions before sampling.

4. DELAY LINE CIRCUITS

Ultrasonic delay lines are utilized for short term storage. The delay medium is zero temperature-coefficient glass. One bit of information is a 0.2 microsecond pulse which propagates through the delay medium at the speed of sound in the medium. Ceramic transducers are used for energy conversion. Glass delay lines provide very reliable and stable short-term storage along with simple instrumentation.

The maximum data rate of the delay line in this computer is 2 megacycles. Thus, only one delay line, delay line driver, and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier, is easily implemented by gating the driver input and sense amplifier output with the four computer clocks.

The delay line input is actually provided by the delay line clock output of the clock generator and the delay line driver acts only as a logic gate. This scheme helps to increase the read-out timing margin and greatly simplifies the delay line driver circuitry.

5. CLOCK GENERATOR

The clock generator provides four sequential nonoverlapping 0.4 microsecond clock pulses and the corresponding reciprocals every bit-time. The clock pulses are synchronized with the 2.048 megacycle signal which drives the delay line drivers. Clock drivers provide the power gain necessary for driving up to 216 AND's on any clock output.

The clock pulses are derived by decoding the outputs of four latches driven by the 2.048 megacycle oscillator. Three clock generators are used in the TMR system. Voting is used as a means of automatically synchronizing the three clock generator channels when the computer is first turned on.

The clock generator also provides clock pulse signals to the DA. These signals must be powered by clock driver circuits in the DA. The delay line clock outputs are also available to the DA from the computer clock generator.

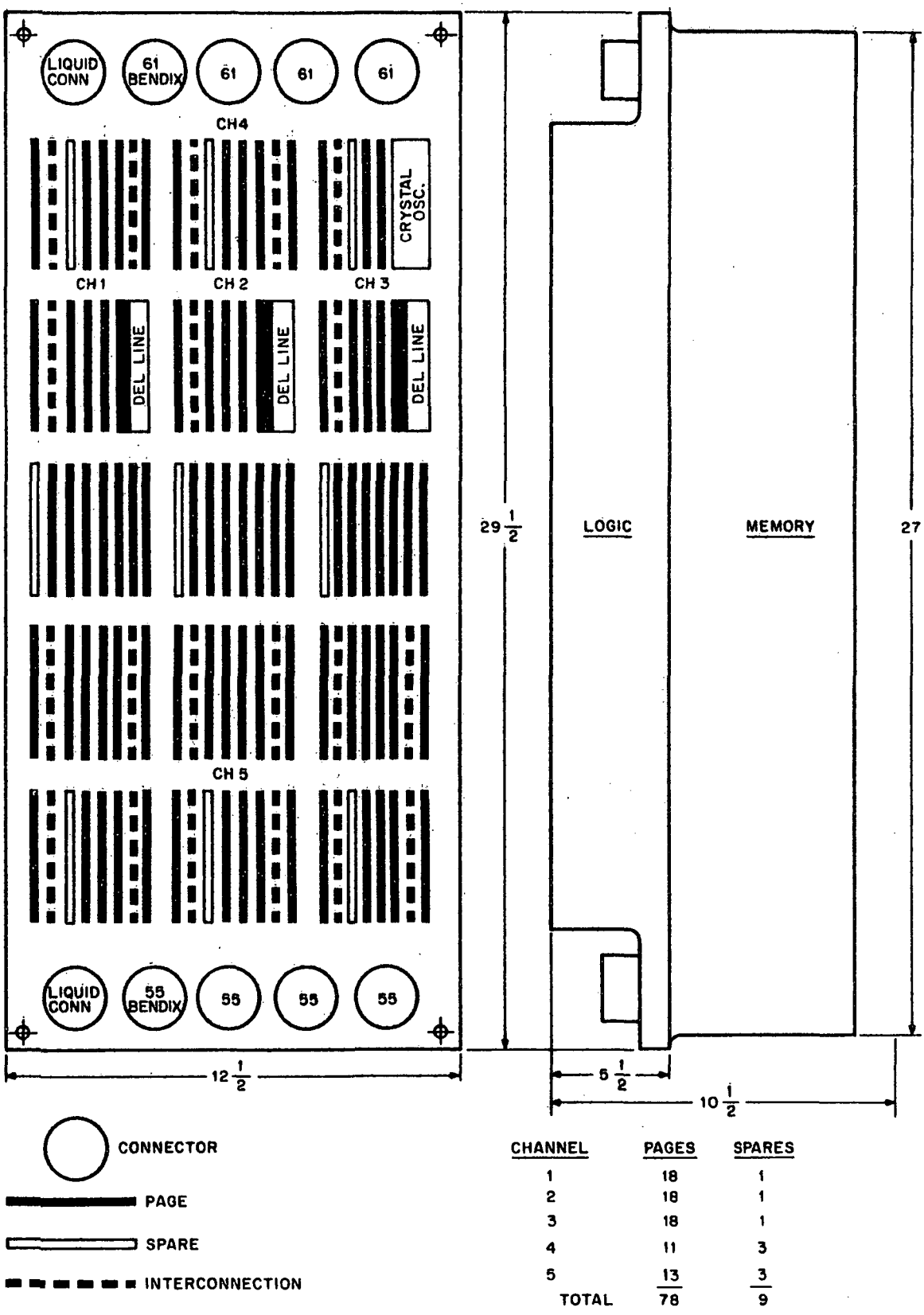
J. TEMPERATURE CHARACTERISTICS

All circuits are designed to operate with a minimum semiconductor junction temperature of 0°C and a maximum junction temperature of 100°C. The logic circuits must have a differential temperature between semiconductor junctions of less than 20°C on a page and 50°C throughout the computer.

K. COMPUTER PACKAGING AND ENVIRONMENTAL REQUIREMENTS

1. CONFIGURATION

The general design of the Saturn V Guidance Computer is shown in Figures III-9 and III-10. The computer package is arranged to contain a logic section with space for 87 pages and a memory section with space for eight memory modules. The unitized structure of the computer is designed to support the logic pages, interconnection back panels, external electrical connectors, and memory modules and to provide for "hard" mounting of the entire assembly to a structural framework within the vehicle.



CHANNEL	PAGES	SPARES
1	18	1
2	18	1
3	18	1
4	11	3
5	13	3
TOTAL	78	9

Figure III-9. Memory and Logic Assembly

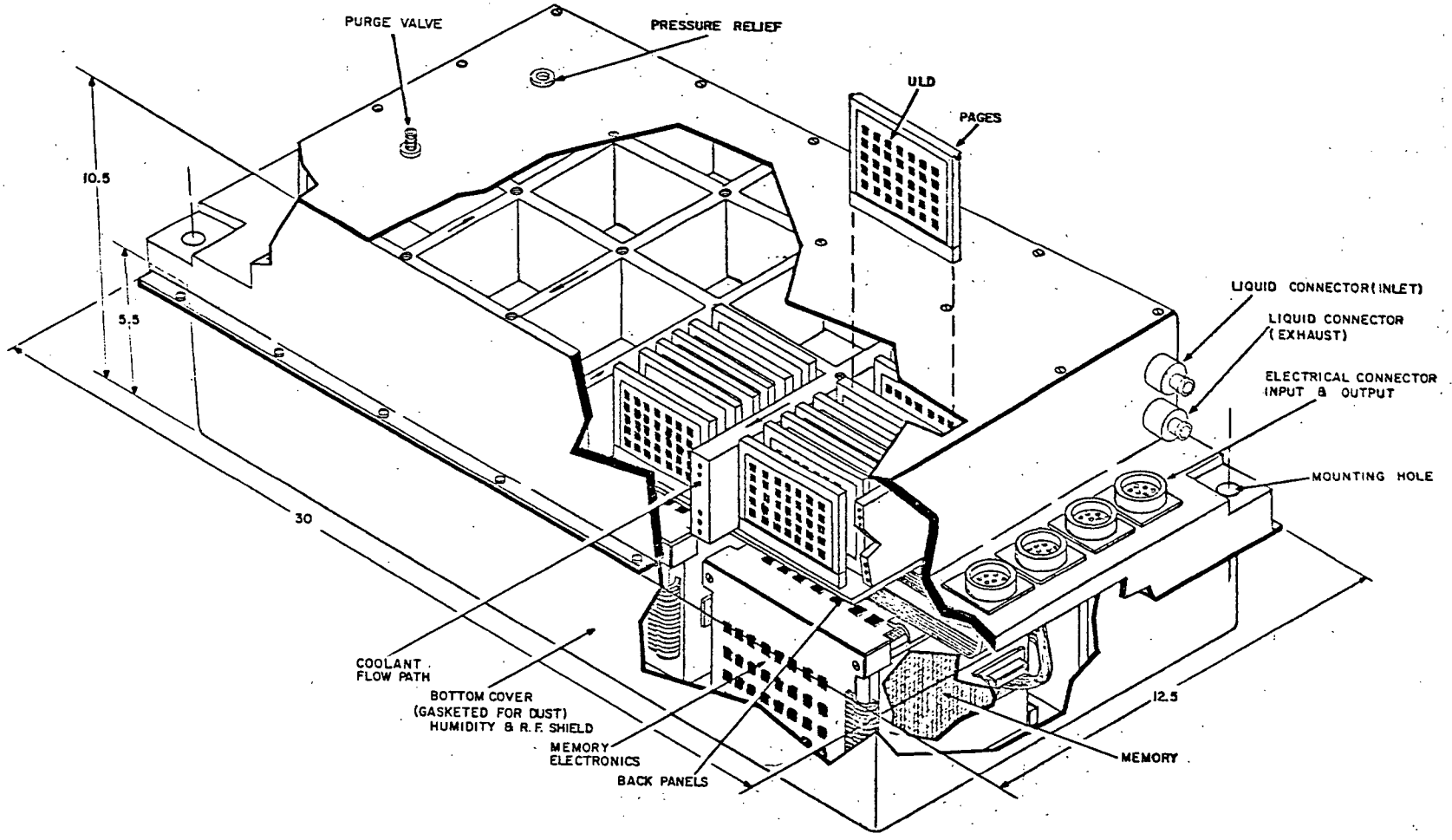


Figure III-10. Saturn V Guidance Computer General Design

Logic pages and memory modules can be easily removed and replaced after removal of the protective covers. The external electrical connectors are located on the framework to allow for the convenient connecting or disconnecting of mating connectors and to minimize possible interference with adjacent units. Heat generated by the logic pages and memory modules is absorbed by cooling fluid circulating through passages in the structural walls of the computer package.

2. MATERIAL

Light-weight magnesium-lithium alloy is used to fabricate the structural gridwork. The structure is designed to a safety factor equal to or less than 1.5. Material used in the fluid passages is compatible with a water-menthanol cooling solution in order to enhance heat transfer effectiveness and to resist corrosion.

3. SEALING DESIGN

The sealing design of the computer provides RF shielding and dust exclusion. In addition, the computer is sealed to the extent that 1 psig will leak off to atmospheric or ambient pressure within a 2-minute minimum period when the unit is pressurized to 5 psig.

4. SIZE AND WEIGHT

The dimensions of the computer are approximately 30 inches long, 12 inches wide and 10.5 inches high. The mounting bosses are positioned so that 5 inches of the vertical dimension of the computer are located on one side of the plane defined by the mounting surfaces, and 5.5 inches on the other side.

A computer with four memory modules and 78 logic pages will weigh approximately 80 pounds and occupy a volume of approximately 2.10 cubic feet. The estimated weights of the computer sections are as follows:

Logic	Weight (lbs)
Pages (occupying 78 page spaces)	11.1
Connectors	13.4
Supporting Structure	22.6
Wiring	3.6

Memory	Weight (lbs)
Assembly and Mounting Structure	22.0
Electronics	3.3
Growth Factor	6.5

These weight estimates exclude the weight of the cooling fluid.

5. COOLING

Those electronic items which dictate the overall thermal design of the Saturn V Computer are as follows:

- Allowable ULD transistor junction temperature...100°C.
- Allowable temperature differential per machine page...20°C.
- Allowable temperature differential within any one machine...50°C.
- Allowable temperature level of memory array...70°C.
- Allowable temperature differential over entire array...10°C.

An integral cooling system is incorporated within the computer design. The operating specifications for the coolant are as follows:

- Maximum input coolant temperature = 60°F
- Maximum allowable flow rate = 12 lb/min.
- Maximum allowable pressure drop (including one main liquid disconnect) = 3.5 psi

The coolant is channelled through the frame as shown in Figure III-10. In addition, the liquid channels are drilled or cast into the magnesium-lithium structure in order to obtain satisfactory distribution of the liquid and the highest possible heat transfer coefficient.

The transfer path for the heat generated by the ULD's is:

- From the ULD to the MIB board and metallic page structure, then

- From the page structure to the metallic clip attached on the page extremities, and finally

- From the clip to the fluid passing through the machine frame structure.

Heat transfer coefficients in the range of 50-70 BTU/Hr. - Ft^2 - F^o are obtained in the vicinity of the clip mounting structure. A temperature differential of 2 degrees Fahrenheit/watt of page dissipation exists at each clip interface. Summing all the temperature differentials, the maximum expected transistor junction temperature is 140°F (60°C).

L. ENVIRONMENTAL REQUIREMENTS

The Saturn V Computer is designed to operate without malfunction when subjected to the following environmental conditions:

- The computer will be operated for 1 hour at 200,000 ft altitude followed by 4 hours of operation at 100°F chamber radiation wall temperature. The emissivity of the radiation chamber wall will not be less than 0.8.

- The chamber wall temperature will then be reduced to minus 40°F in a period not to exceed 1 hour and the computer will be operated for 4 hours.

- The computer will be placed in a vacuum chamber and the pressure reduced to 10^{-4}mm Hg (Torrs). The chamber wall temperature will be stabilized at 80°F and the computer will be operated for not less than 500 hours after temperature stabilization within the computer.

- The computer will be subjected to humidity and explosive atmosphere in accordance with paragraph 4.41 of MIL-E-5272C and paragraph 4.13.4 of MIL-E-5272C.

- The computer will be operated at 15g sustained acceleration in the horizontal plane normal to the 30-inch mounting dimension for a minimum of 6 minutes.

- The computer will be subjected to three 50g shock saw-tooth waves having a 6 millisecond rise time and a 0.5 millisecond decay time. This shock will be imposed in the horizontal plane normal to the 30-inch mounting dimension of the computer.

- The computer will be subjected to a 140 db over-all acoustic noise level in a bandwidth of 37.5 cps to 10 kc.

- The computer will be subjected to an acceptance test vibration level of 3G RMS sine in the three principal axes at a sweep rate of 1 octave/min in the direction of increasing frequency only.

- The computer will be subjected to a qualification test of 0.057 g^2/cps random noise in a 40 to 1800 cps band with a 6 db per octave roll off below 40 cps. Above 1800 cps, the roll-off is 12 db/octave. This energy will be applied for 3 minutes after which the general spectrum will be reduced to 0.032 g^2/cps. This energy will be applied for 7 minutes. This test will be applied to the computer in the three principal axes.

- The computer will be designed for fuel compatibility for an exposure time consistent with mission requirements.

The thermal operating design requirements will be met by the following coolant requirements:

Fluid:	60 percent by weight methanol and 40 percent by weight water solution
Quantity:	12 lb/min
Pressure Drop:	$\Delta P_{max} = 3.5$ psi
Inlet Temperature:	$50^{o}F$ to $60^{o}F$

The vibration requirements will be met by hard mounting the computer to channels within the missile.

M. ELECTRONIC PACKAGING

1. UNIT LOGIC DEVICE (ULD)

The basic circuit module is a ceramic substrate with deposited resistors and uncased semiconductor devices. The alumina substrate is 0.300 inch square. Resistors are formed on the surface of the substrate by silk-screen deposition of cermet resistor materials. Metallic conductors are also formed by the same process. Transistors and diodes are attached by reflow of solder-coatings previously applied to conductor surfaces. An encapsulation material is applied to protect the components.

Connections with external circuitry and between opposite surfaces of the substrate are made through 14 wrap-around conductor lands and metal clips on the edges of the substrate. Figure III-11 shows a ULD before and after encapsulation.

2. MULTILAYER INTERCONNECTION BOARD (MIB)

Interconnections among ULD's are accomplished by the Multilayer Interconnection Board. The MIB is composed of multiple layers of etched circuits which are bonded together under heat and pressure to form a single unit. Connections between circuit layers and to the outer surfaces are provided by plated-through holes. Circuit layers are arranged for optimum circuit isolation.

Each MIB contains 12 layers of copper assigned as shown in Figure III-12. Several layer patterns are shown in Figures III-13, III-14 and III-15. All plated holes and conductors are located on a 0.020 inch grid. Conductors are nominally 0.010 inch wide. Nominal separation of adjacent conductors is 0.010 inch. The MIB has mounting area for 35 ULD's on 0.400 inch centers. Figure III-16 shows front and rear views of a MIB before trimming.

3. PAGE

ULD's and MIB's in the computer logic are combined in page form. The page includes two MIB's bonded to both faces of a magnesium-lithium alloy frame. A 98-pin connector is fastened to the lower edge of the frame and wire leads from the connector are soldered in plated holes on the edge of both MIB's. Feed-through connections between the two MIB's are provided by insulated pins fastened in holes in the frame. Pin ends are soldered in plated holes of both MIB's. Test point lands are provided along the upper edge of each MIB.

Mechanical support for the page is provided on the lower end by the connector shell and guide pins and on the upper end by clamping two lugs on the page frame to the computer structure. Spring clips which grip both sides of the page provide additional mechanical support and provide the principal thermal path from the page to the computer structure.

Electrical and mechanical attachment of ULD's to MIB's is by solder fillet connections. Both MIB and ULD land surfaces are pre-coated with solder. The solder is re-flowed by infra-red heating to form solder fillets. After page assembly and test, a coating is applied for protection in a high humidity environment. A page mockup is shown in Figure III-17.

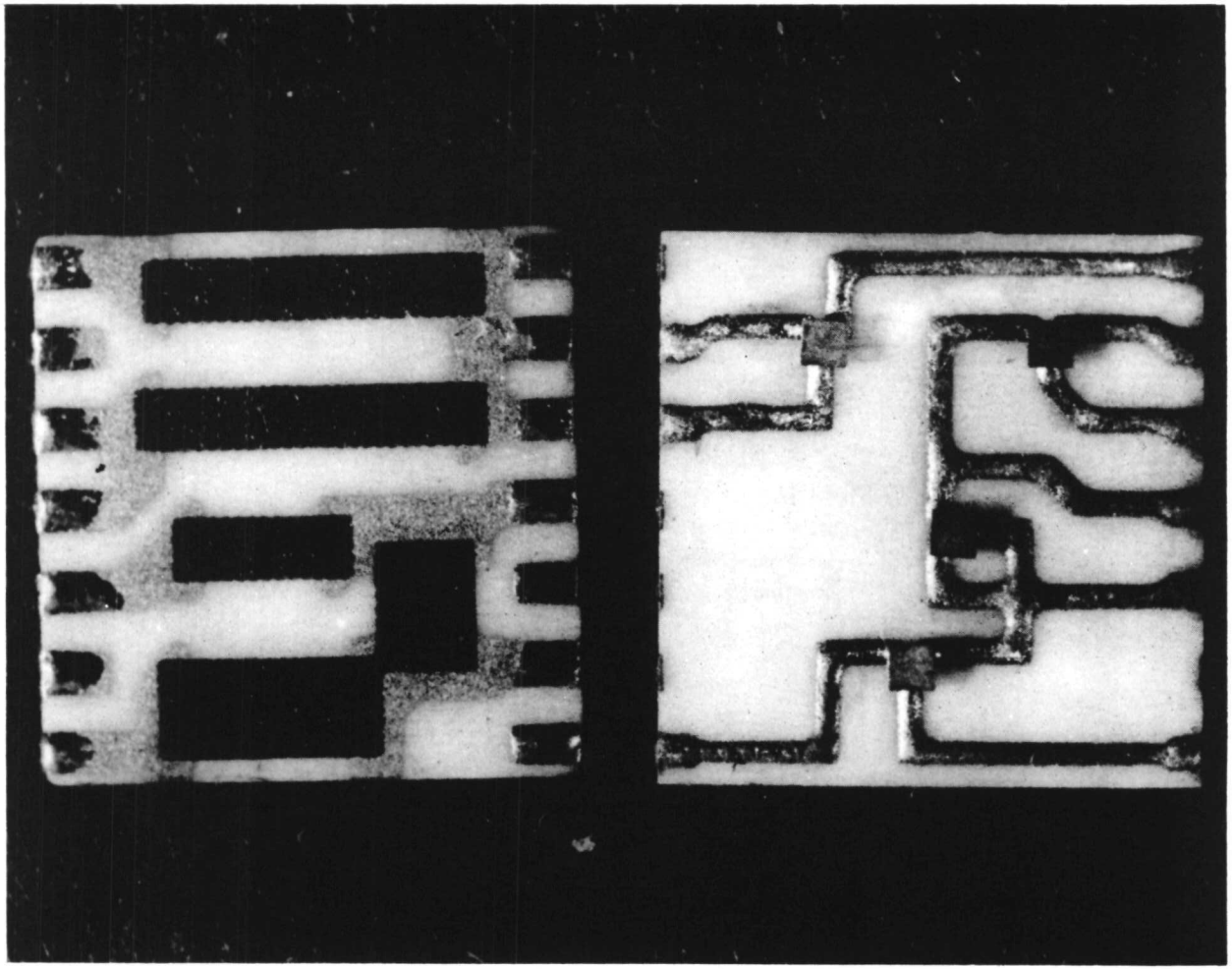


Figure III-11. ULD Before and After Encapsulation

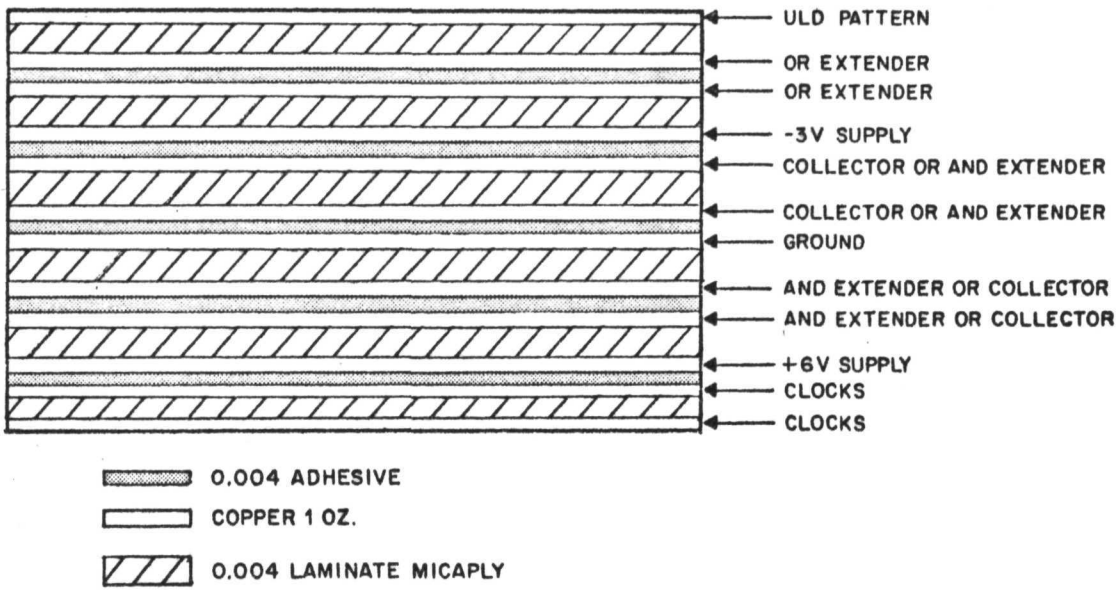


Figure III-12. MIB Cross Section

4. BACK PANEL

Interconnections among pages of the logic section are made through back panels. The back panel consists of a MIB, receptacles for pages and a metal plate for mechanical support. The MIB is bonded to the plate and the leads of the receptacle are soldered to plated holes in the MIB.

5. MEMORY

The toroid memory module contains 14 core planes stacked between mechanical supports. Each plane has 8192 toroids 64 by 128 in a frame approximately 5.5 inches long by 3.5 inches wide by 0.150 inches thick. Interconnections between planes are made with printed wiring strips, soldered to the plane edge terminals.

The mechanical supports on each end contain diode matrices and termination resistors. These supports also provide mounting surfaces on four sides for MIB's, mounting surfaces across one end for a discrete component connector and panel, and pads for mounting the memory module into the computer frame.

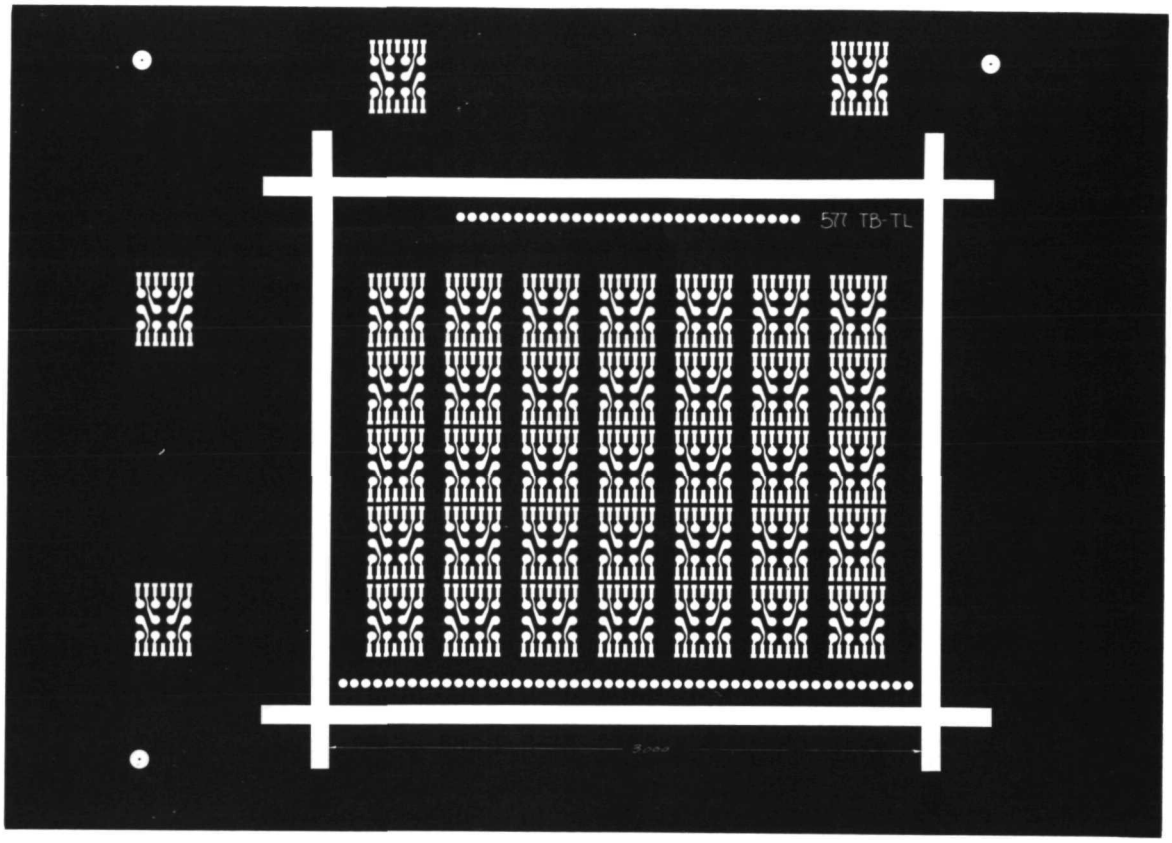


Figure III-13. MIB Top Land Pattern

The four MIB's mounted to the end supports contain memory circuit ULD's. The discrete components panel has a 98-pin input-output connector for interconnections between the memory module and the computer logic. Flat cable wiring is used to make electrical connections between MIB's and the core planes within the array.

The memory module volume is approximately 110 cubic in. and the weight 6.43 pounds. Memory configuration is shown in Figure III-18.

6. INTERCONNECTIONS

The logic pages are grouped in five channels in the computer. These channels contain space for 16 to 20 pages. Interconnections within each channel are provided by a back panel. Connections among channels are through etched flexible flat cables. Adjacent areas on the five back panels are interconnected by cables made in a few basic sizes and connected to conventional 98-pin page connectors. Figure III-19 shows the flat cable artwork.

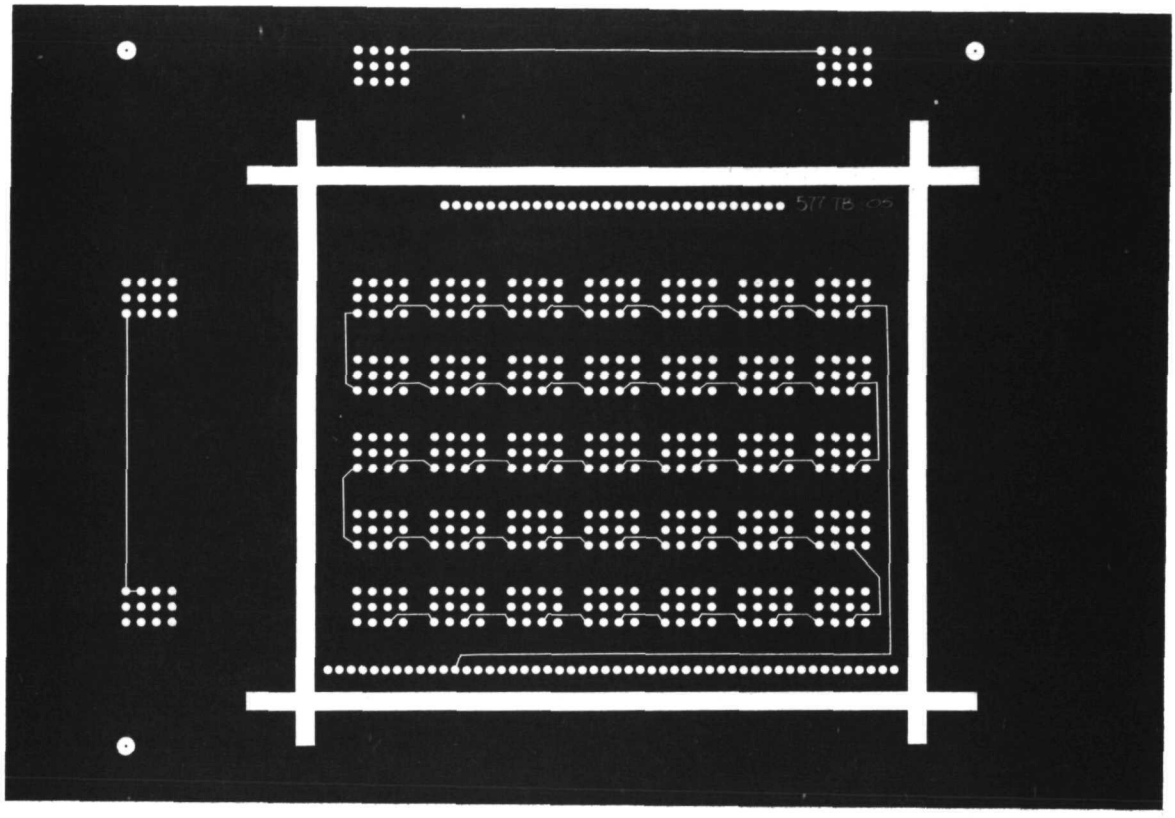


Figure III-14. MIB Circuit Layer

Connections from back panels to external connectors are made through a harness which is attached at one end to terminal blocks on the back panels and at the other end to the connector pins.

Memory modules are connected to the computer through flat cables which are permanently fastened to the computer back panels at one end and have a pluggable connection to the memory module on the other end.

A diagram of computer interconnection wiring is shown in Figure III-20. Figure III-21 shows the physical arrangement of elements of the interconnection system.

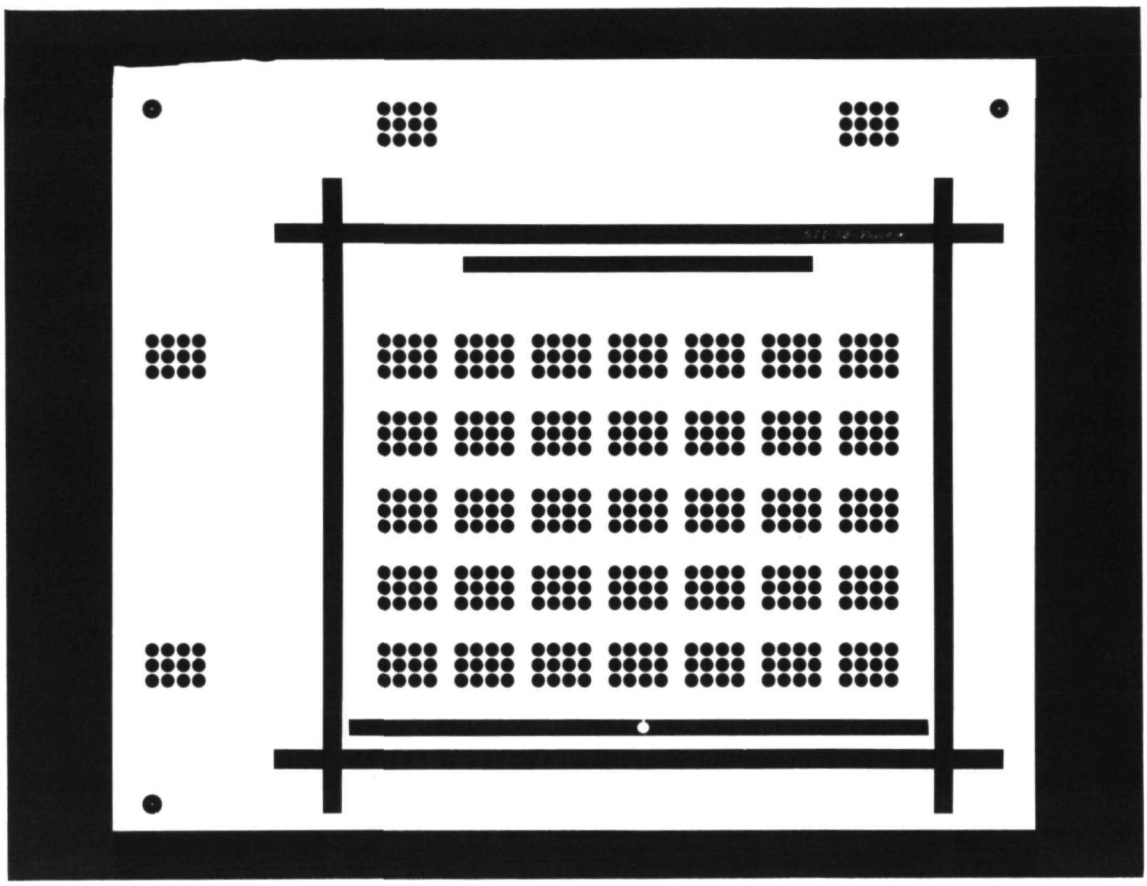


Figure III-15. MIB Ground Plane

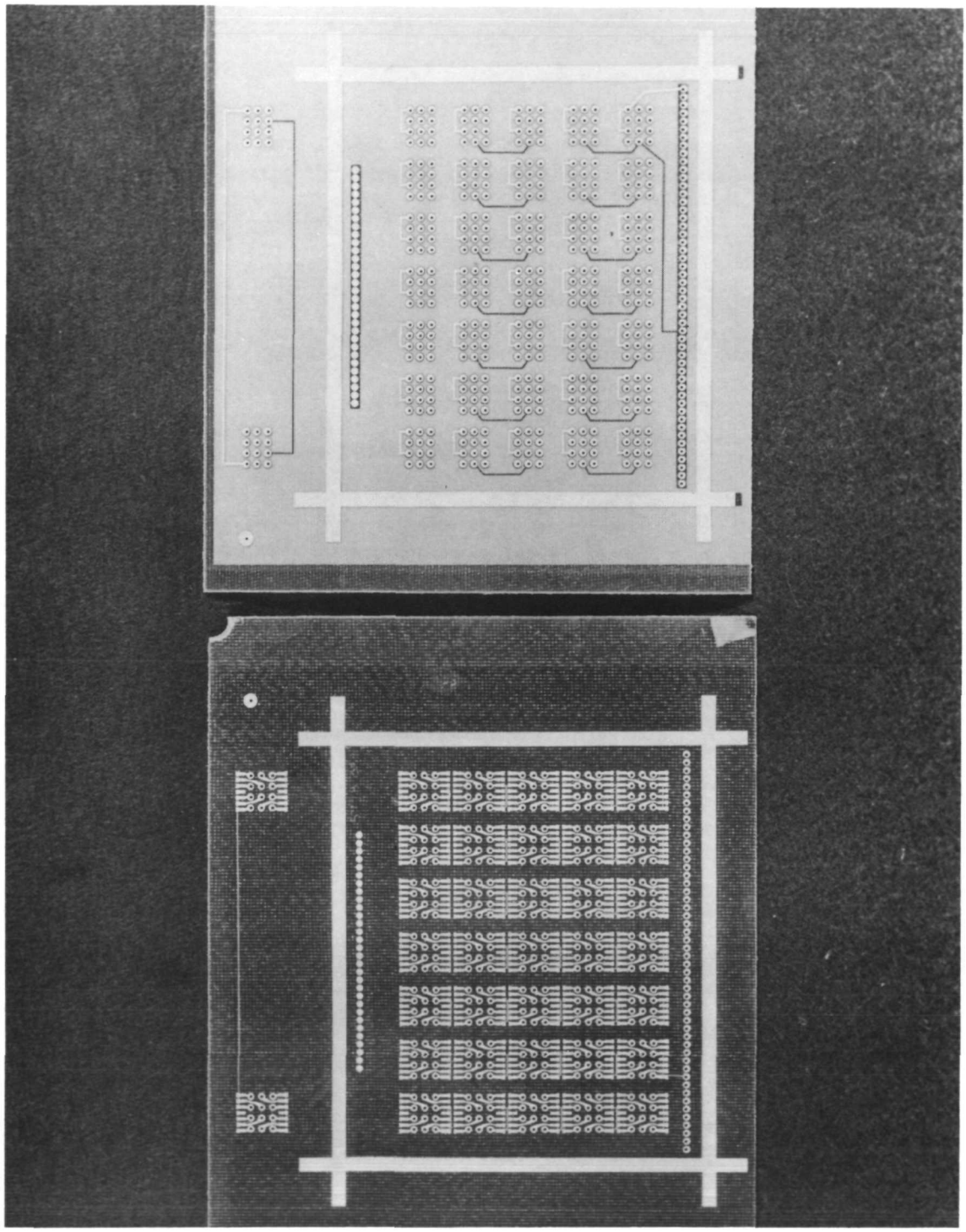


Figure III-16. MIB Front and Rear Before Trimming

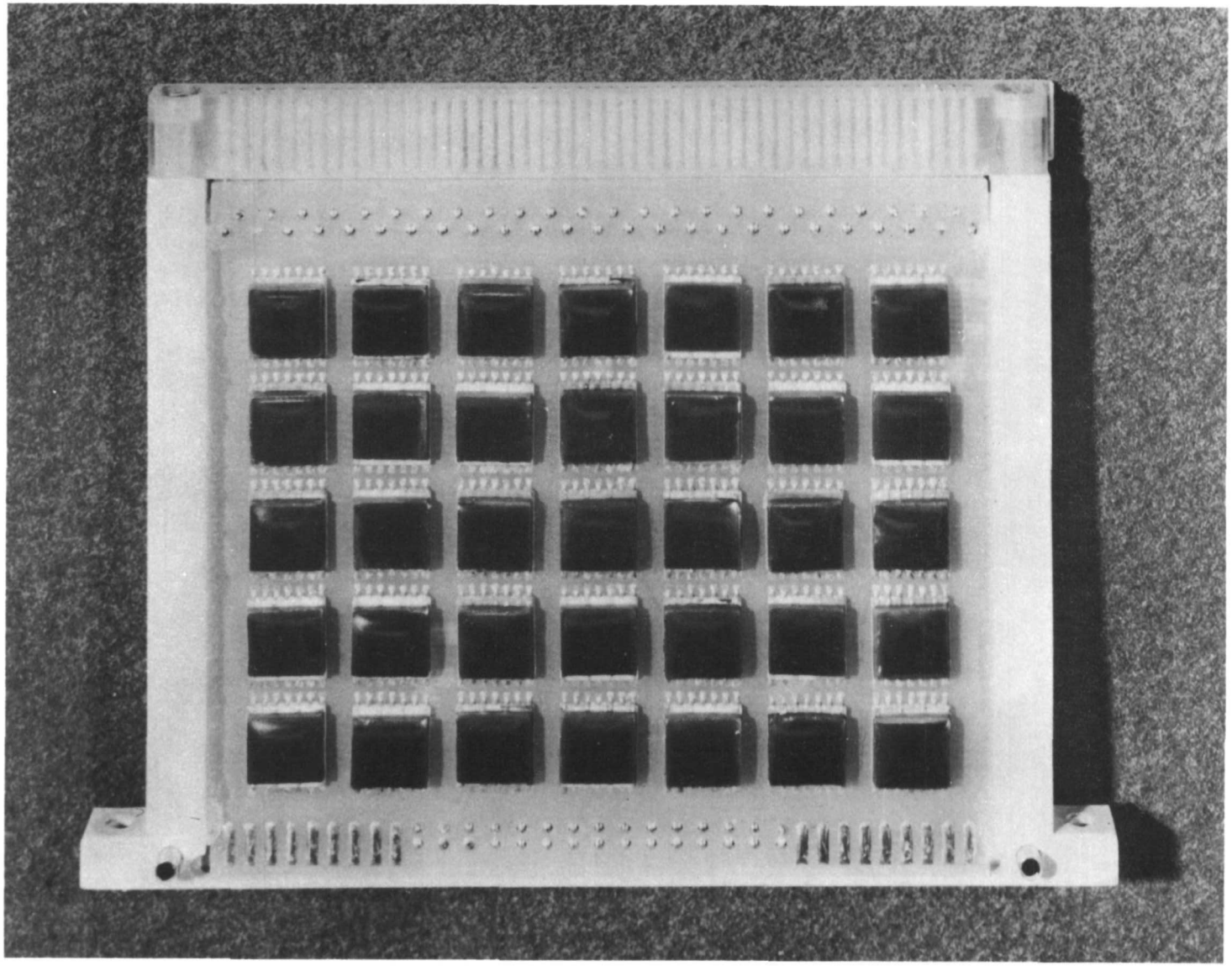


Figure III-17. Page Mockup

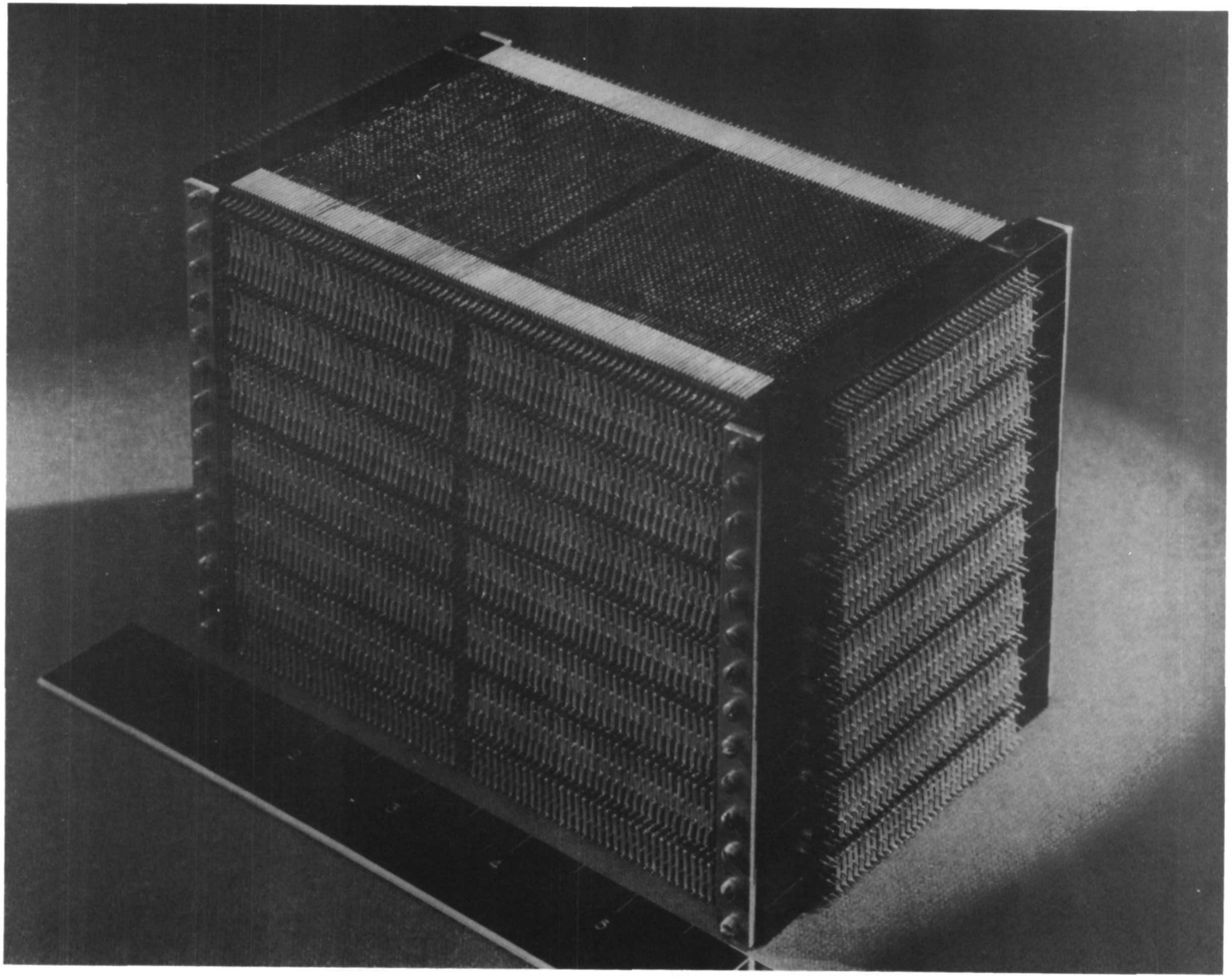


Figure III-18. Memory Configuration

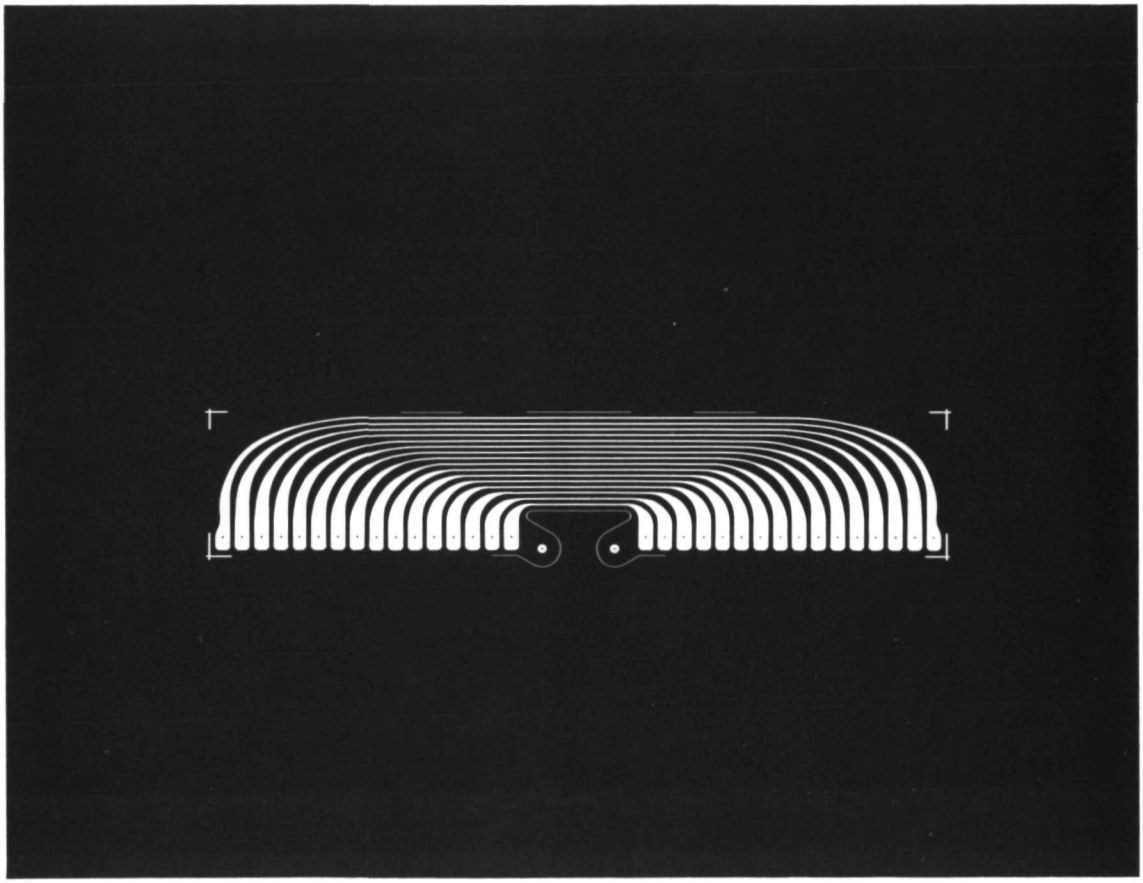


Figure III-19. Flat Cable Artwork

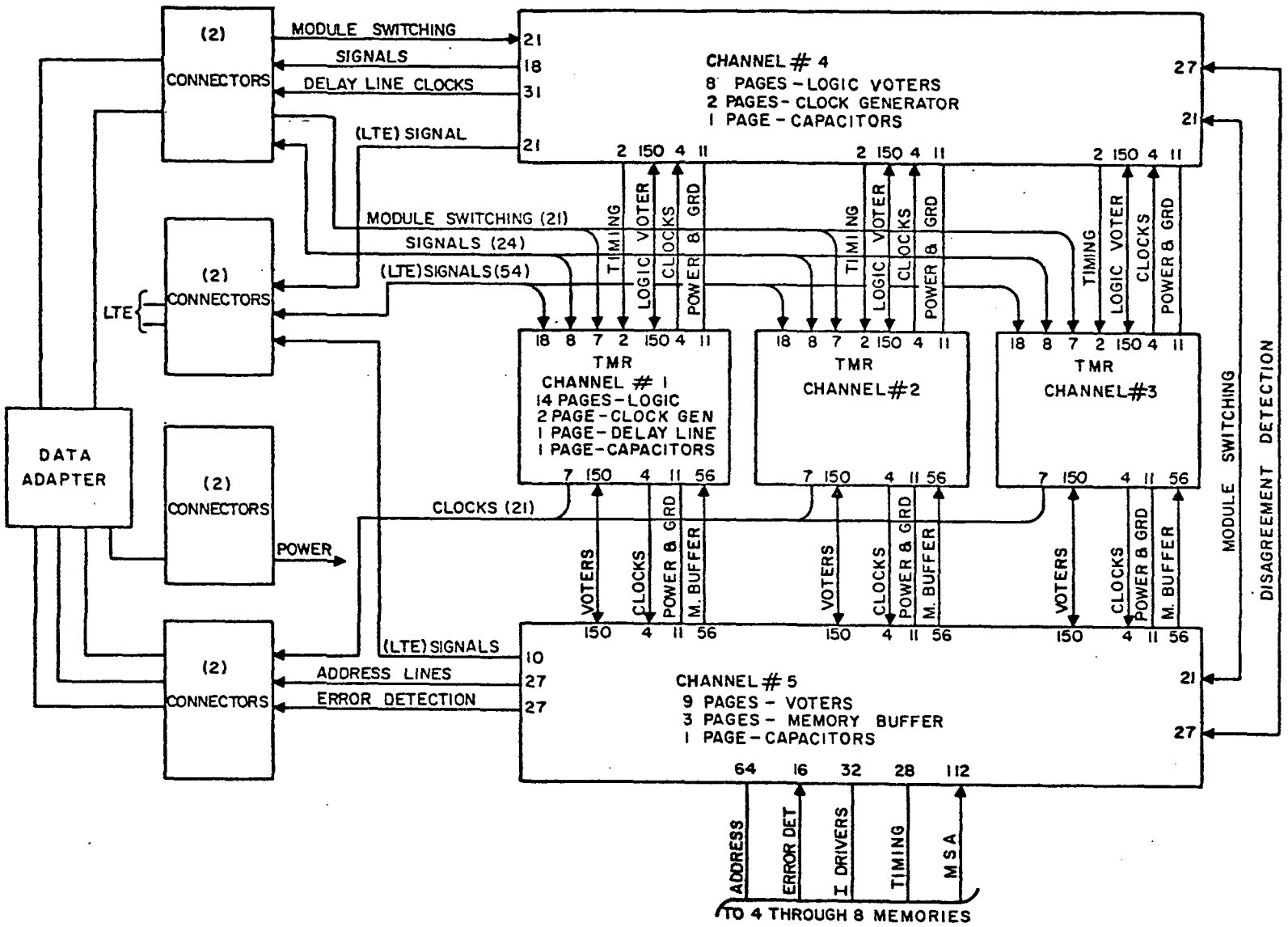


Figure III-20. Computer Interconnection Wiring Diagram

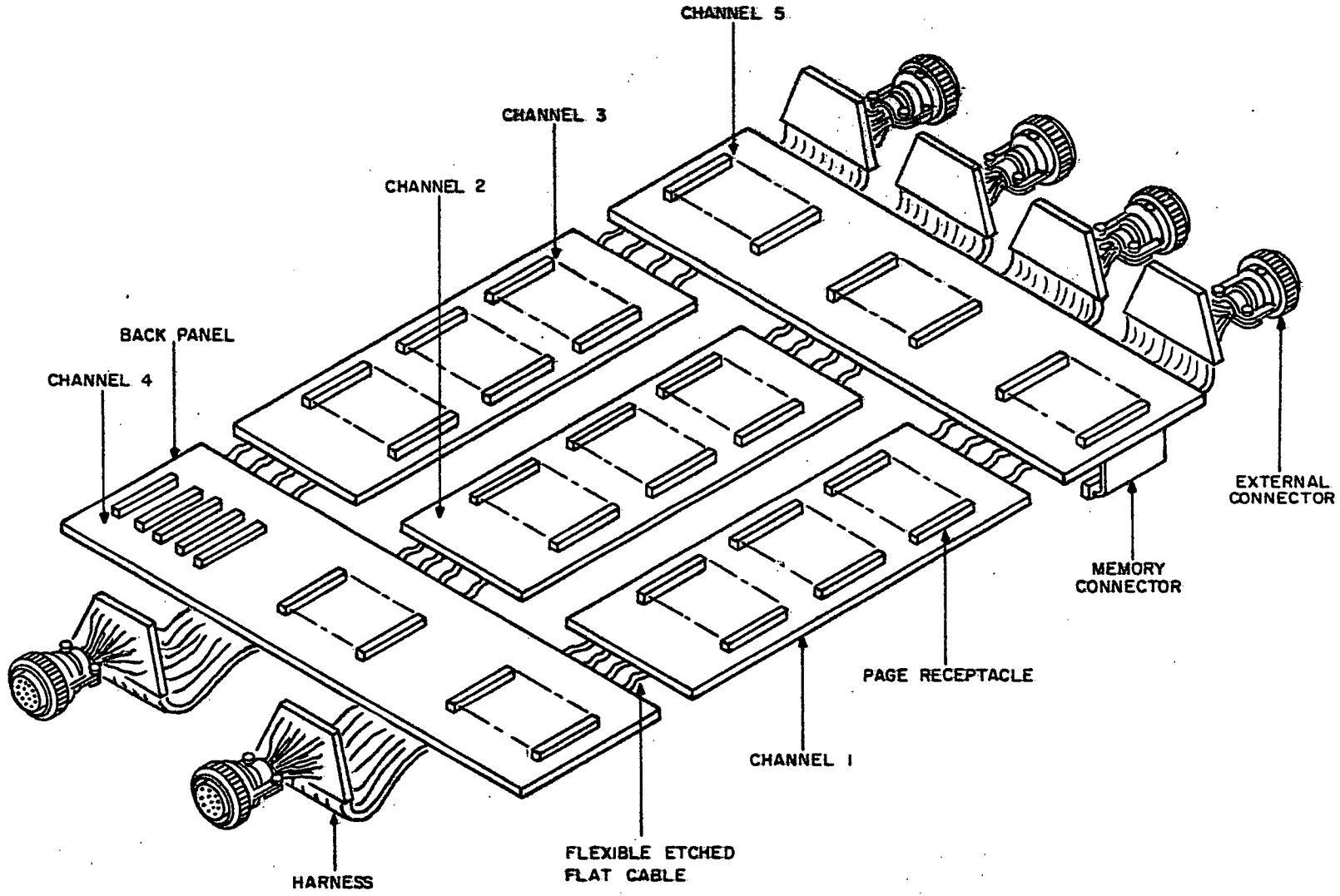


Figure III-21. Interconnection System

Section IV

SATURN V DATA ADAPTER

Section IV

SATURN V DATA ADAPTER

A. GENERAL DESCRIPTION

The data adapter (DA) is the input-output unit which will accompany the Saturn V guidance computer. Common technology (in terms of component types, circuit module fabrication and multilayer interconnection boards (MIB)) is used in the computer and DA. The DA can perform a variety of input-output functions and is compatible with the information rate and interface requirements of Instrument Unit equipment with which it must interconnect. It also has a growth capability to handle larger numbers of existing types of inputs and outputs, and to incorporate new types of functions. (See block diagram, Figure IV-1.) The DA is divided into the following distinct parts:

- A digital section which buffers digital quantities such as discretes
- An analog section which converts analog-to-digital and digital-to-analog.

The power supplies which serve the DA, computer and memory are contained in the DA. These power supplies are duplexed for reliability; thus each supply must be capable of supplying the full current load for that voltage. Voltage sequencing is provided where required, and power supply lines can be switched to permit single channel computer operation.

Communication with the computer is carried out through 512-kilobit-per-second serial transmission. The PIO instruction permits the specification of either input or output operations, and addresses the device to be affected. A single 26-bit word is transferred to the computer accumulator or from the accumulator or memory.

The DA employs ULD circuit modules and MIB's for circuit interconnections. Technology which is adapted from that used in the guidance computer will be employed. Where low-power logic circuits are used, leadless semiconductors will be mounted on ULD's. For those applications where high power dissipation is required, where precision components are needed, or where leadless devices are not available, standard discrete components packaged in encapsulated modules will be used. This will apply particularly in the case of power supplies, ladder networks, and cross-over detectors.

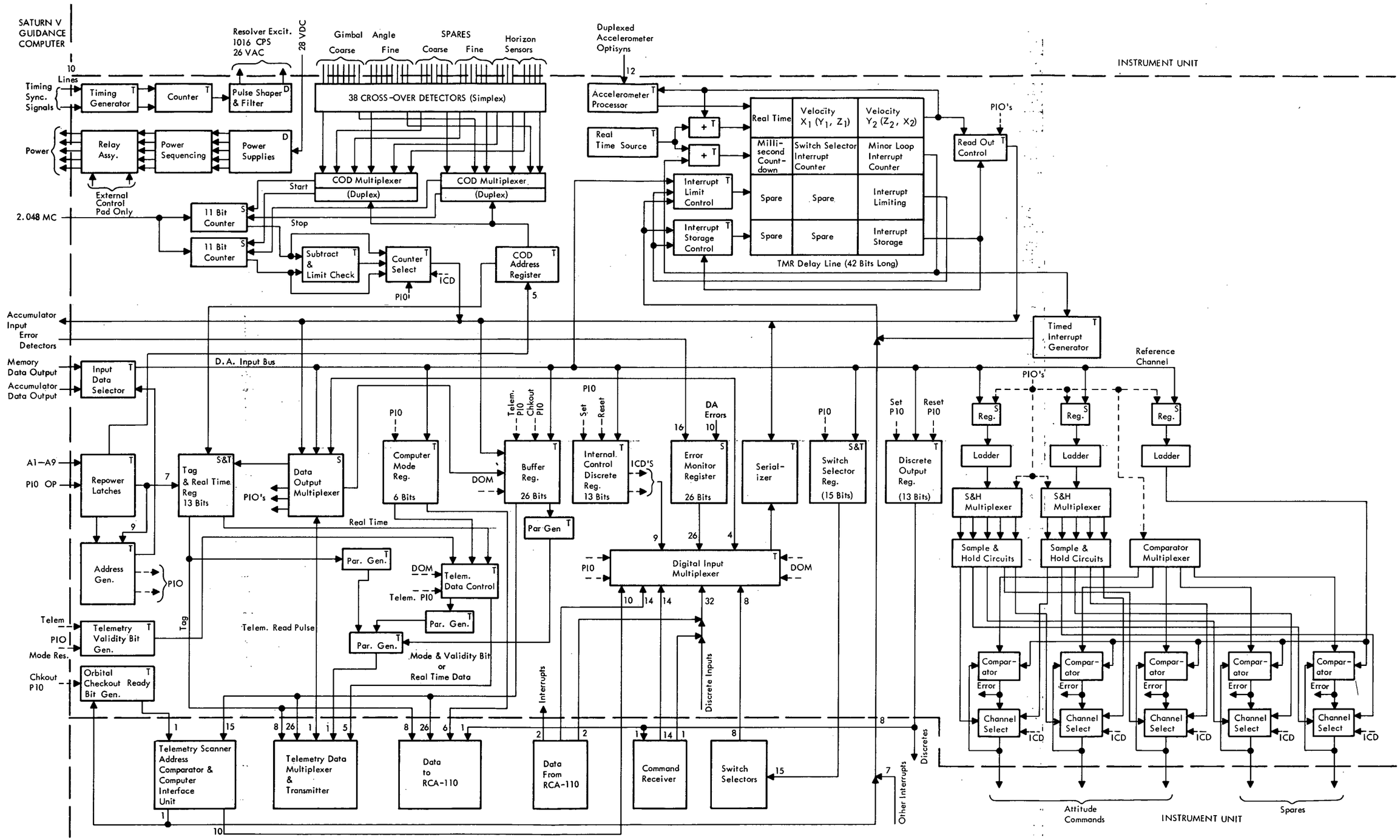


Figure IV-1. Saturn V Data Adapter Block Diagram

A complete listing of DA characteristics is presented in Table IV-1.

Table IV-1

DATA ADAPTER CHARACTERISTICS

Item	Description
Computer Input/Output Rate	512-kc serial
Power Supplies	6 pairs of duplexed supplies
Switch Selector	8-bit switch-selector input 15-bit switch-selector output
Discretes	13 discrete outputs 32 discrete inputs
Buffer Register Interrupt Register Mode Register	26-bit 8-bit 6-bit provides communication with the RCA-110 Ground Control Computer, Telemetry Transmitter, and the Computer Interface Unit
Digital-to-Analog Converter	8-bit, 2-msec operation
Analog-to-Digital Converter	3 attitude commands, 2 spare outputs. Equivalent of 16 bits from a 2-speed resolver
Platform	4 2-speed gimbal angle resolver inputs
Horizon Scanner	4 single-speed resolver inputs
Spares	6 resolver inputs
Delay Lines	3 4-channel Delay Lines for normal I/O operations 2 4-channel Delay Lines for Telemetry operations
Telemetry	
Command Receiver	14 bits for input data
Data Transmitter	38 data and identification bits plus validity bit and parity bit
Telemetry Scanner	15 bits address plus validity bit for output data, 10 bits for input data

Table IV-1. Data Adapter Characteristics (cont)

Item	Description
RCA-110	39 data and identification bits plus validity bit for output data, 14 bits for input data plus interrupt
Component Count	37,000 silicon semiconductors, cermet resistors and other special components
Temperature	60°F coolant inlet temperature, 100°C maximum junction temperature allowable
Reliability	0.99 probability of success for 250 hrs; uses TMR logic, duplex special circuits, duplex power supplies
Packaging	100 electronic page assemblies, plus special electronic assemblies
Weight Volume Power	94 pounds 2.6 cubic feet 400 watts

B. FUNCTIONAL DESCRIPTION

1. DATA ADAPTER INTERNAL FUNCTIONS

Although the routing of data is an important DA function, the DA must also process much of the data it transmits. The internal operation of the DA may be broken down into three main categories:

- Control data flow, including temporary storage
- Transform data into a form which is compatible with the characteristics of the receiving equipment
- Perform certain simple computational and logical operations on the data.

The following functions are typical of those included in the first category:

- The storage of telemetry data from the computer and DA in the buffer registers

- The temporary storage of telemetry scanner addresses during orbital checkout.

- The transmission of guidance data from the computer to the analog control computer.

Operations which require a change in the form of the data include: (Typical of those in the second category)

- Digital-to-analog, analog-to-digital, and signal level conversions

- The formation of 40-bit RCA-110 and telemetry words from 26-bit computer words

- Buffering of communications between the computer and the ground-based RCA-110 to reconcile the difference in clock rates.

The DA contributes to the efficient operation of the computer by performing many simple, though time-consuming, logical and computational tasks such as: (Typical of those functions performed in the third category)

- Keeping track of real time

- Decoding of operand addresses in PIO operations

2. POWER SUPPLIES

The DA contains the power supplies to drive the circuitry of the DA and the computer. To a limited extent, power may also be furnished to interface circuitry in other equipment where good grounding practices dictate the need. The power is isolated from the +28 volt battery supply of the vehicle by a dc-to-dc static converter. DC output voltages will be determined by the circuit requirements of the DA and the computer. The power supplies contain relays to operate the computer on the ground. These relays permit ground check-out of the redundant circuits to verify that all redundant functions are operating.

3. ADDRESS GENERATOR AND TAG REGISTER

During I/O operations, the computer must select a register in the DA which contains or will receive the I/O data. The address of the selected register and the correct data are determined by the operand bits of the instruction

word along with the PIO control lines from the computer. These functions are performed by the Address Generator.

4. SWITCH SELECTOR REGISTER

This register is loaded by the computer whenever the computer wishes to give commands to specific vehicle devices such as fuel valve controls. The register has a 15-bit storage capacity and is loaded by a PIO instruction. The register also controls the outputs of five switch selectors located within the stages of the vehicle.

The 15 bits are used as follows:

- Eight bits make up a relay tree code which is distributed in parallel to each of the five switch selectors.
- Five bits determine which switch selector will be activated. (No more than two selectors may be addressed at once.)
- One bit commands the assigned switch selector to activate the device selected by the relay tree.
- One bit resets all switch selector relays which were turned on by the previously described bits.

5. DISCRETE OUTPUT REGISTER

Certain functions within the vehicle, excluding those controlled by the Switch Selector Register, are controlled by a 13-bit Discrete Output Register. An example of one function which is controlled by the Discrete Output Register is a signal to the RCA-110 and Command Receiver indicating that data has been read by the computer.

To ease programming requirements for changing specific discretes while not affecting others, the Discrete Output Register is not loaded in the same way as the other registers. If certain discretes are to be activated, a PIO is set up to address the "set" side of all latches in the register. Conversely, if certain discretes are to be deactivated, another PIO selects the opposite or "reset" side of all latches in the register. The desired bits in the register are changed by placing "ones" in the corresponding bit locations of the data word transferred to the register from the computer while the unchanged bit positions have "zeros" in the data word.

6. DISCRETE INPUTS

Discrete inputs are signals which do not require storage within the DA. The DA is designed to handle 32 of these inputs. Groups of these discrete inputs are treated as words by the computer — one 26-bit word and one 8-bit word. Each word is read by the computer as requested by a PIO address. The computer reads the discretes periodically and performs the necessary program steps.

Examples of discretes are:

- A "data ready" signal from the RCA-110 or the Command Receiver.
- A "source of data" signal from the RCA-110. (If this signal is not present, the "data ready" discrete is interpreted as coming from the Command Receiver.

7. SWITCH SELECTOR FEEDBACK INPUTS

When the Switch Selectors are operated as previously described, the relay tree feedback lines must be tested to assure that the tree was set properly by the DA. Eight lines from a separate set of contacts on the relay tree contain the complement of the data word used to set the tree. These lines are inputs to the DA which do not require storage and are addressed by the DA in the same manner as other discrete inputs. This feedback word is separated from the other discrete inputs so that the word may be processed more easily in the computer when comparing it with the word used to "set" the relay tree.

8. INTERRUPT REGISTER

As a means of notifying the computer that immediate attention be given to an external operation, an interrupt line is wired from the DA to the computer. The Interrupt Register (Delay Line) is capable of accepting 13 different signals and storing them until the computer has acted upon them. Presently, there are requirements for only eight interrupt signals. The signals are OR'ed together so that only one interrupt line to the computer is required. After an interrupt, the computer branches to a subroutine to read the Interrupt Register by means of a PIO operation. A computer analysis is then made, testing the highest priority bit positions first in case more than one interrupt signal is stored in the register. During this testing, the computer stores the contents of the memory address register and the instruction counter and branches to an interrupt subroutine. While in this subroutine, the computer will not recognize further interrupts. The next to last instruction of the interrupt

subroutine is a PIO addressed to the Interrupt Register to reset the particular bit causing the interrupt. The hardware provides a time delay to prevent further immediate interrupts from the same source. The source must disappear and return before another interrupt will be honored from that source. This will prevent slow-acting devices such as relays from regenerating interrupts while they are being activated by discrete outputs which occur during the interrupt subroutine. Each interrupt signal must be at least 84 us. duration to assume storage in the delay line.

The computer is also capable of inhibiting the interrupt, as commanded by the program, with PIO instructions whenever the function of the subroutine warrants this precaution. However, a few of the inputs will bypass this inhibit control; these latter inputs will be caused by functions which require the highest priority of attention. The TM Scanner Address Comparator and the RCA-110 each have one input to the Interrupt Register.

9. BUFFER REGISTER

The Buffer Register provides storage for a 26-bit word and is loaded by PIO operations or the Data Output Multiplexer for DA data telemetry operations. It provides part of the interface required for transferring data to the telemetry transmitter and/or RCA-110. It also stores addresses to be compared in the Telemetry Scanner Address Comparator during orbital or ground check-out. It provides parallel outputs to all of these external systems simultaneously. These systems read data from this register asynchronously with respect to computer timing.

10. MODE REGISTER

The Mode Register is similar to the Buffer Register and other one-word registers loaded by the computer. It provides storage for a 6-bit computer word which defines the computer mode of operation. While communicating with the RCA-110 these six outputs are read in parallel by the RCA-110. The Telemetry Data Multiplexer reads four of these outputs when transmitting computer telemetry words, but real time information data will be substituted for these bits when DA data is transmitted.

11. VALIDITY BIT GENERATOR

Since the Telemetry Data Multiplexer addresses the DA asynchronously with respect to computer timing, it is possible for telemetry words to be read while they are being changed by PIO operations. However, data read at this time is invalid. Also, since the Buffer Register is used to store addresses of other telemetry system parameters during orbital check-out, this data would be invalid as telemetry outputs from the DA.

Therefore a signal must be included in the telemetry word which indicates the validity of the word. The Validity Bit Generator performs this function. Data will be invalid any time the Computer Mode Register, Tag Register and Buffer Register are being loaded. It will also be invalid when the Buffer Register contains orbital check-out address information.

12. READY-BIT GENERATOR

During orbital check-out the computer examines various parameters which are monitored by the telemetry system. The computer obtains one of these inputs by sending a Telemetry Scanner address to the Buffer Register. This 15-bit address is compared in the Telemetry Scanner Address Comparator. When comparison occurs the telemetry word is stored in a 10-bit register which is read by the DA. Another line interrupts the computer to notify it that data is available.

Since the Buffer Register is continuously connected to the Telemetry Scanner Address Comparator as well as the Telemetry Data Multiplexer and RCA-110 interface, it is necessary to indicate to the Address Comparator when the Buffer Register data is ready for comparison. This is the function of the Ready Bit Generator. The "ready" bit is turned on after the 15-bit address is loaded into the Buffer Register, under control of a special PIO instruction. The bit remains on until after the address has been compared and the 10-bit data word has been stored; it is turned off by the line causing the computer interrupt.

13. PARITY GENERATOR

To help ensure that computer data sent out over the RF telemetry link to ground equipment is received without error, a parity bit is included in each 40-bit data word sent out by the DA.

The telemetry data word is formed from three subwords plus a validity bit. The validity bit however, is not included in the parity check. Odd parity is used. This means that, excluding the validity bit, all the "ones" in the three subwords plus the parity bit will add up to an odd number. The easiest way to generate total parity is to generate an individual parity bit for each subword. The three parity bits are then checked for total parity and a resultant parity bit is generated.

14. INTERNAL CONTROL DISCRETE REGISTER

Certain functions within the DA must be controlled by the computer. A 13-bit register, very similar to the Discrete Output Register, is included to provide these controls.

Some of the functions of these discretes are:

- Control switching of duplex delay line channels
- Selection of the duplex analog output channels to be used
- Control to inhibit certain interrupts.

15. PIO DIGITAL INPUT MULTIPLEXER AND SERIALIZER

Excluding the computer, all digital input words except accelerometer inputs occur in parallel form. Since the computer can read only one group of inputs (one word) at a time, the group of inputs selected by the PIO request is switched to a single Serializer which converts the parallel inputs to the 512-kc serial bit rate. The output of this Serializer is fed to the accummulator input data bus. The PIO Multiplexer provides the necessary switching for the input word selected by the computer.

Data from the RCA-110 and the Command Receiver have the same address. If the RCA-110 is connected to the system, a discrete input indicates this and provides a control gate to inhibit inputs from the Command Receiver while allowing inputs to come from the RCA-110. The converse of this is true if the RCA-110 is not connected into the system.

16. TMR DELAY LINE

The use of glass delay lines in a TMR configuration has effected significant component savings and resultant reliability improvements in the DA. They replace several latch registers that would otherwise be required for the functions being implemented.

This TMR delay line has been organized around computer timing such that the information it contains remains synchronized with the computer operation cycle. The total circulation time of the delay line and its associated electronics will be equal to the basic computer instruction cycle time of 82.03 microseconds (42 bit times). The delay line will be divided into three 14-bit word times corresponding to the three computer phase times. Furthermore, the four clock times into which each computer bit time is divided will be used to time-share the delay line among four "channels" of 512-kilocycle serial information. Hence, a total of 12 14-bit words can be stored in a single delay line by operating the line at 2.048 megacycles per second. Figure IV-2 illustrates how these word locations will be used.

In performing a PIO operation, the computer sends out or looks for information only during phase-times "B" and "C." Real time has been assigned to a phase "A" word time. This is done to facilitate the use of real time information in the Data Output Multiplexer (DOM). However, real time will be made available to the computer during phase "B" via the multiplexer register and the serializer latch.

The velocity accumulations, which are the processed outputs of the accelerometer optisyns, are arranged in such a manner as to provide duplex redundancy, matching the duplexed optisyns, in the TMR delay line. One line will contain outputs X_1 and Y_2, another will accumulate Y_1 and Z_2, while still another will process Z_1 and X_2. When the computer calls for a given velocity accumulation, it will receive the processed output of one of the optisyns on the selected accelerometer in phase "B" and the output of other optisyn on the same accelerometer during phase "C." These two values will be processed separately in the computer such that any one of the delay lines or any optisyn could fail without failing the system.

No initialization has been provided for this delay line. The real time accumulation is voted upon in TMR voters during every circulation, so the values in all three lines will always agree. The duplex operation of the accelerometer processors does not allow voting, so there is no guarantee that the absolute value of the two readings will agree. Inasmuch as it is the change in velocity between readings that is of interest, and since the duplexed outputs are processed separately in the computer, it is assumed that the extra circuitry required for initialization is unnecessary. Real time is accumulated in 246.1-microsecond increments, while the least significant bit in the velocity measurement has a weight of 0.05 meters per second.

The delay channel whose bits are written at Y time is used to time three functions in the data adapter/computer system. In phase "A," a time delay of approximately 1 millisecond duration for use in the D/A converter is generated by counting 12 circulations of the delay line. In phase "B," time to go until the next computer interrupt for the switch selector function is counted down, while the time remaining before the next minor loop is counted down in phase "C." These two countdowns occur at the rate of one count every 0.4922 millisecond, and they generate an interrupt when they pass through zero. The length of the count is determined by the computer, which loads a value of time-to-go to indicate each count.

	Phase A	Phase B	Phase C	
W Clock	Spare	Spare	Interrupt Storage	Read Channel
X Clock	Spare	Spare	Interrupt Limiting	Write Channel
Y Clock	Millisecond Countdown	Switch Selector Interrupt Countdown	Minor Loop Interrupt Countdown	Write Channel
Z Clock	Real Time Accumulation	Velocity Accumulation $X_1 (Y_1, Z_1)$	Velocity Accumulation $Y_2 (Z_2, X_2)$	Read Channel

Figure IV-2. Use of Word Locations

Computer interrupts are stored in phase "C" of channel "W." Once the computer recognizes an interrupt, it sets the corresponding bit in phase "C" of channel "X" and resets this bit in channel "W." The associated circuitry prevents a new interrupt from being recognized in this bit position until the previous interrupt has disappeared. The only constraint, therefore, on the length of the interrupt signal is that it lasts for at least 82.03 microseconds.

In Figure IV-2 it can be seen that four spare words are left in channels "W" and "X." Channel "W" may be conveniently read by the computer, while channel "X" may be conveniently written into from the computer. As many as three of the normal 14 bits may have to be sacrificed if it is desired to use either of these two channels in the opposite manner.

17. TELEMETRY MONITORING OF DATA

a. Digital Data Monitoring

The PCM telemetry system to be used for monitoring digital data will accept 40-bit words at an asynchronous rate of 240 words per second. Special buffering and control logic must be provided in the data adapter to temporarily store input and output data occurring at instantaneous rates greater than 240 words per second.

The telemetry monitoring system will telemeter all significant data adapter inputs and outputs read or written by PIO operations. In addition, other important data available only in the computer will be telemetered. This data will also be transferred by PIO operations. The only PIO operations that will not be telemetered are those caused by the timed interrupt operations.

It is assumed that the computer will not send out telemetry data during the minor loop of the operational program nor will its telemetry output exceed 100 words per second.

Assuming four gimbal angle inputs, each at a rate of 25 per second, and three attitude command outputs at the same rate could mean an additional 175 PIO's per second. Added together, these would exceed the allowable telemetry rate of 240 words per second. However, since gimbal angles and attitude commands are short words of less than one syllable, they can be combined in a delay line register so that two PIO words make up one telemetry word. This would reduce the effective number of inputs and outputs of this type to 87-1/2 telemetry words per second.

Other PIO's have been assumed to occur at the following rates:

Computation Mode Register	0.2/sec
Real Time	5/sec
COD Error Inputs	1/sec
Command Receiver	4/sec
Switch Selector (Normal Operation)	20/sec
Discrete Inputs	8/sec
Error Monitor Register	1/sec

Internal Control Discretes	0.2/sec
Optisyn Inputs	6/sec
Discrete Outputs	0.2/sec
Horizon Sensors	8/sec
Minor Loop Interrupts (Timed)	25/sec
Switch Selector Interrupts (Timed)	20/sec
Other Interrupts	1/sec
Total	99.6/sec

Of this total, time interrupts account for 45/sec. Excluding these, which will not be telemetered, the total reduces to 54.6/sec.

In summary, the estimated number of telemetry words generated each second is as follows:

Computer	100/sec
Gimbal Angles and Attitude Commands	87.5/sec
Other PIO's, excluding Timed Interrupt	54.6/sec
Total telemetry operations	242.1/sec

For digital outputs, data will be monitored at the interface of the data adapter to determine whether the correct signals were sent to the external equipment. This applies to the switch selector and discrete output registers. Each have serial inputs and parallel outputs. The switch selector register has 13 address bits, one read command, and one reset bit, while the discrete output register has 13 bits. The read command and reset bits of the switch selector are eliminated from telemetry making the outputs of both registers one-syllable words. This allows the formation in a delay line of a 26-bit word containing the serial input to one of these registers and the output of the register, and in turn requires loading the data output register and the address bits of the switch selector register during phase "B" of the PIO operation. The parallel outputs will then be serialized through the digital input multiplexer and stored in the delay line during phase "C" of the PIO operation. The internal control discrete register, which has no external interface, will be monitored in the same way.

A data output monitor (DOM) (Figure IV-3) provides the additional delay line buffer storage and control logic needed to handle all digital telemetry words except the computer telemetry words previously mentioned.

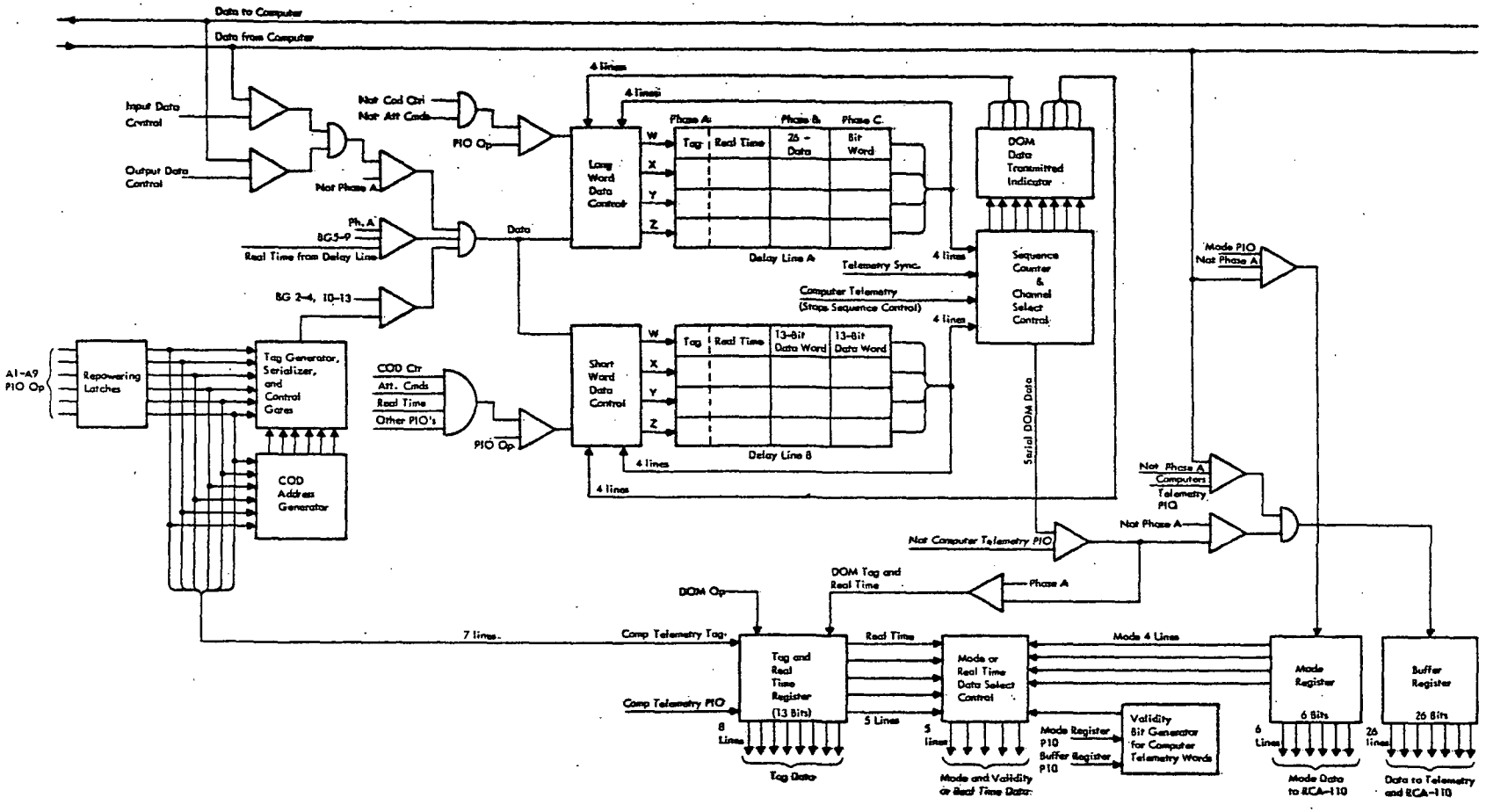


Figure IV-3. Proposed Digital Data Control for Telemetry Transfers from the Saturn Data Adapter

Computer telemetry words will be loaded directly into the 26-bit buffer register in the DA by PIO's and, along with four bits from the mode register and eight bits from the tag register, a validity bit and a parity bit will be transmitted in parallel to another 40-bit core buffer in the telemetry equipment. The DOM also shares this hardware, except for the mode register and the validity bit generator. When a synchronizing pulse occurs, indicating that a word has been read by the telemetry equipment, a new word is transferred from the DOM buffer into these registers in preparation for the next telemetry "read" operation. If a computer telemetry PIO takes place before the DOM word has been read, it will have priority and computer data will be substituted for DOM data. The DOM will reload the same data for transmission as soon as the computer word has been transmitted. (Refer to the timing chart, Figure IV-4.)

To provide a meaningful tag for those telemetry words assembled from two PIO words, a fixed format must be established for the assembled words. A special delay line buffer will be used to provide this function thus, data sorted in this delay line might be as follows:

	Phase A	Phase B	Phase C
Channel W	Tag A / Tag B — Real Time	Attitude Command A	Fine Pitch / Coarse Pitch
Channel X	Tag C / Tag D Real Time	Attitude Command B	Fine Yaw / Coarse Yaw
Channel Y	Tag E / Tag F Real Time	Attitude Command C	Fine Roll / Coarse Roll
Channel Z	Tag G / Tag H Real Time	Spare	Fine Redun. Yaw / Coarse Redun. Yaw

In addition to the gimbal angles shown, horizon sensor and other COD inputs may be added. Tags will always be generated from the address stored in the COD address generator, which is required to select the resolver input. Unique groups of tags will not only define the COD input but also the attitude command stored in the same channel.

There is no problem in tagging the following input and output PIO words:

Command Receiver
Switch Selector Register
Discrete Inputs
Discrete Outputs
Error Monitor Register
Internal Control Discretes
Optisyn Inputs
Interrupt Register

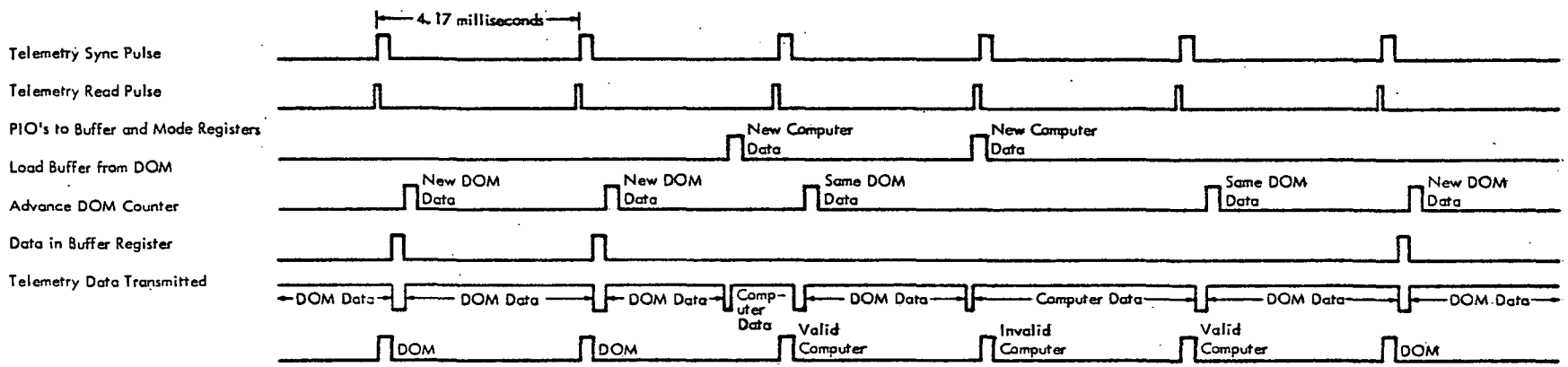


Figure IV-4. Data Adapter Telemetry Timing

Therefore, another delay line buffer will store these parameters. Channels of this delay line will not be allocated to certain parameters, but will be loaded as available after previously loaded data has been transmitted. The parameter tags will be formed partially from the operand address of the PIO operation and will be stored in the phase "A" portion of the delay line as before.

Two delay lines will provide storage for eight 26-bit telemetry words, plus tag and real time data. When the computer is not generating telemetry data, these words will be selected in sequence by delay line channel for transmission. If there are no valid data in a selected channel, the counter will advance until valid data are located. A 3-bit sequence counter will be required to select channels. The counter will be advanced by a synchronizing pulse from the telemetry equipment every 1/240 second (4. 17 millisecond) if the computer did not load a telemetry word since the last sync pulse. If the latter occurs, the counter does not advance and the same data are reloaded for transmission.

With eight words of storage, some data words will be buffered 8×4.17 milliseconds (33. 4 milliseconds) or longer if the DOM is interrupted by computer telemetry operations. It is therefore desireable to include additional data along with the tag information to indicate when the data was loaded in the buffer delay line. Five bits from the real time counter in the D. A. will be added to phase "A" data. The low order bit represents an increment of 2 milliseconds so real time can be expressed over a range of 64 milliseconds. These real-time increments, when correlated with timing information generated by the telemetry system, will pin-point data generation time to within 2 milliseconds. To add these five bits of time information, it is necessary to delete other data making up the 40-bit telemetry word. To prevent any ambiguity of associating real time with the short data words in the special delay line, this line might be limited to minor loop data such as platform gimbal angles and attitude commands. Telemetry transmissions from this line could then be inhibited during the minor loop and allowed only in the major loop. The four mode bits and one validity bit used with computer telemetry words will be deleted. This would be done for DOM telemetry operations only.

When processing this data on the ground, it is possible to distinguish between DOM and computer telemetry words by looking at tag bit 8. The presence of a bit in this position indicates that the data originated in the computer. Otherwise the data was DOM-generated. Tables IV-2 and IV-3 present details on PIO and tag bit coding.

A special circuit will monitor the constant-amplitude, phase-shifted input to the COD's. If, due to a malfunction, the signal level exceeds established limits in the positive or negative direction, the output of this circuit will be a logical "1." There are presently 18 pairs of COD's that must be monitored by these circuits, and their outputs must be telemetered. This will be done by one telemetry word. The best means of controlling the DOM to provide this function is to provide an additional PIO address to serialize the parallel outputs of these circuits so they are read by the computer and stored in the DOM. As a program consideration, this would probably be done once during the major loop, i. e., once or twice a second. There is no storage capability in the individual monitoring circuits, so if an intermittent malfunction occurs and clears between PIO samples, it will not be detected.

Table IV-2

DEFINITION OF USE OF ADDRESS LINE BITS TO THE DATA ADAPTER FOR PIO OPERATIONS

Group	A8	A2	A1	Function
1	X	0	0	Not used
2	See Below	1	0	Input to Data Adapter (Load Registers and Delay Lines)
3	See Below	0	1	Input to Data Adapter (Computer Telemetry operations)
4	0	1	1	Output from Data Adapter (Register and Delay Line Read)
5	1	1	1	Output from Data Adapter (COD CTR READ and set up new COD using address lines)

Table IV-2. Definition of Use of Address Line Bits
To The Data Adapter For PIO Operations (cont)

	Group 1	Group 2	Group 3	Group 4	Group 5
A3 A4 A5 A6 A7 A8 A9	Not Used	Address See Below	Address See Below	Address 0 Not Used	Address 1 Not Used
		A8 A9 0 0 M MEM 0 1 ACC 1 0 1 1 R MEM 64 ACC 32 RES MEM 32 MAIN MEM	A8 A9 0 0 0 1 ACC 1 0 1 1 RES MEM 96 ACC 32 RES MEM	Bit A8 is used to recognize COD group.	

Table IV-3

DEFINITION OF TAG CODE TO BE USED WITH TELEMETRY

	PIO Group 2	PIO Group 3	PIO Group 4	PIO Group 5
Tag Bit 1	0	A8	1	0
2	1	A9	0	0
3	A3	A3	A3	A3
4	A4	A4	A4	A4
5	A5	A5	A5	A5
6	A6	A6	A6	A6
7	A7	A7	A7	A7
8	0	1	0	0

A1, A2, and A8 are decoded in the DA to determine what goes into tag bit 1, 2, and 8 positions. A "1" in tag bit 8 position indicates that the computer is the source of data. For a "0", the DOM is the source. For DOM data, tag bits 3 through 7 identify the word or registor addressed in the DA and are the corresponding operand address bits of a PIO instruction. Tag bits 1 and 2 identify whether the data is an input, output, or COD word. Computer telemetry words are identified by operand address bits A3 through A9.

be a logical "1". There are presently 18 pairs of COD's that must be monitored by these circuits, and their outputs must be telemetered. This will be done by one telemetry word. The best means of controlling the DOM to provide this function is to provide on additional PIO address to serialize the parallel outputs of these circuits so they are read by the computer and stored in the DOM. As a program consideration, this would probably be done once during the major loop, i. e. once or twice a second. There is no storage capability in the individual monitoring circuits, so if an intermittent malfunction occurs and clears between PIO samples, it will not be detected.

b. Analog Data Monitoring

Certain data in the data adapter will be monitored by the analog input channels to the PCM telemetry system. These include the following:

(1) Unfiltered 28 VDC input to the DA
(2) Filtered 28 VDC output from the DA
(3) +6 V from power supply No. 1
(4) +6 V from power supply No. 2
(5) +12 V
(6) +20 V
(7) -3 V
(8) Attitude command "A"
(9) Attitude command "B"
(10) Attitude command "C"
(11) Spare ladder output "A"
(12) Spare ladder output "B"
(13) Computer thermistor output "A"
(14) Computer thermistor output "B"
(15) DA thermistor output "A"
(16) DA thermistor output "B"
(17) Optisyns
(18) Resolver excitation

For 1 through 12 of the previous list, these signals must be scaled down in most cases to be compatible with the full scale range of 0 to 5 VDC for the telemetry system inputs. No interface circuits are required to connect the thermistor outputs into the telemetry system. Each thermistor will provide two output lines to telemetry. In addition, all computer thermistor circuits will be routed to telemetry through the DA.

C. ANGLE MEASUREMENT

The instrumentation used is capable of measuring shaft angles in digital form to an accuracy of approximately one part in two thousand. This requires an analog-to-digital conversion of eleven bits. To accomplish measurements and conversion of the shaft angles, a time-duration measurement is used. This is accomplished by connecting a resolver in such a manner that two signals will be generated to switch a high-frequency counter on and off. The resultant count, after a measurement cycle, represents the angle in binary form.

The basic principle of operation can be seen by considering the sum of the constant amplitude and frequency sine wave modulated by the cosine and sine respectively of the variable of interest. This is:

$$e_r = (E \sin \omega t) \cos \theta + (E \sin \omega t) \sin \theta \ .$$

The sum can be modified to a useful trigonometric form by shifting one of the waves by 90 deg. Thus

$$e_r = (E \sin \omega t) \sin \theta + E \sin (\omega t + \tfrac{\pi}{2}) \cos \theta$$

where, by a standard identity,

$$e_r = E \cos (\omega t - \theta).$$

These operations are carried out by the resolver and its associated circuitry by feeding an excitation signal to the resolver as shown in Figure IV-5. The input sinusoid is multiplied by the sine and cosine of the angular rotation of the rotor with respect to the stator of the resolver. A phase shifting network connected to the two rotor windings causes their outputs to differ in phase by 90 deg.

Addition takes place within the network and the resultant output is a sinusoid, shifted by an amount proportional to θ plus a constant shift which can be calibrated out. Thus, the ratio of the amount of phase shift due to the rotation of the resolver relative to 2π, gives a direct measure of the angles.

Assuming a 2.048 mc clock for the counter and a 1016 cps reference supply, the resolution of a single phase-shifted input is

$$\frac{1016 \times 2\pi}{2.048 \times 10^6} = 0.178 \text{ deg/binary bit.}$$

System requirements dictate angle measurement accuracies of one minute of arc. This is achieved by using two-speed resolvers with a coarse-to-fine ratio of 32:1. Coarse and fine inputs are each measured to a resolution of 11 bits. The combined resolution is 16 bits.

D. POWER SUPPLY CONFIGURATION

The block diagram of a pulse-width-modulated power supply module is shown in Figure IV-6.

The timing oscillator provides an unregulated d-c voltage for the driver stages to ensure power ground isolation. It also provides a square-wave output which determines the switching rate of the power inverter. Integrators in the predriver stage convert this square wave into a triangular drive signal whose average d-c value is a function of the control input from the d-c feedback amplifier. The biased triangular signal determines the degree of modulation. The shaped output from the driver stage is transformer-coupled to the power inverter to maintain ground isolation.

The push-pull power inverters switch the +28-V dc source to the primary of the power transformer. The full-wave rectified output of the transformer constitutes a unipolar pulse train whose on-off ratio is proportional

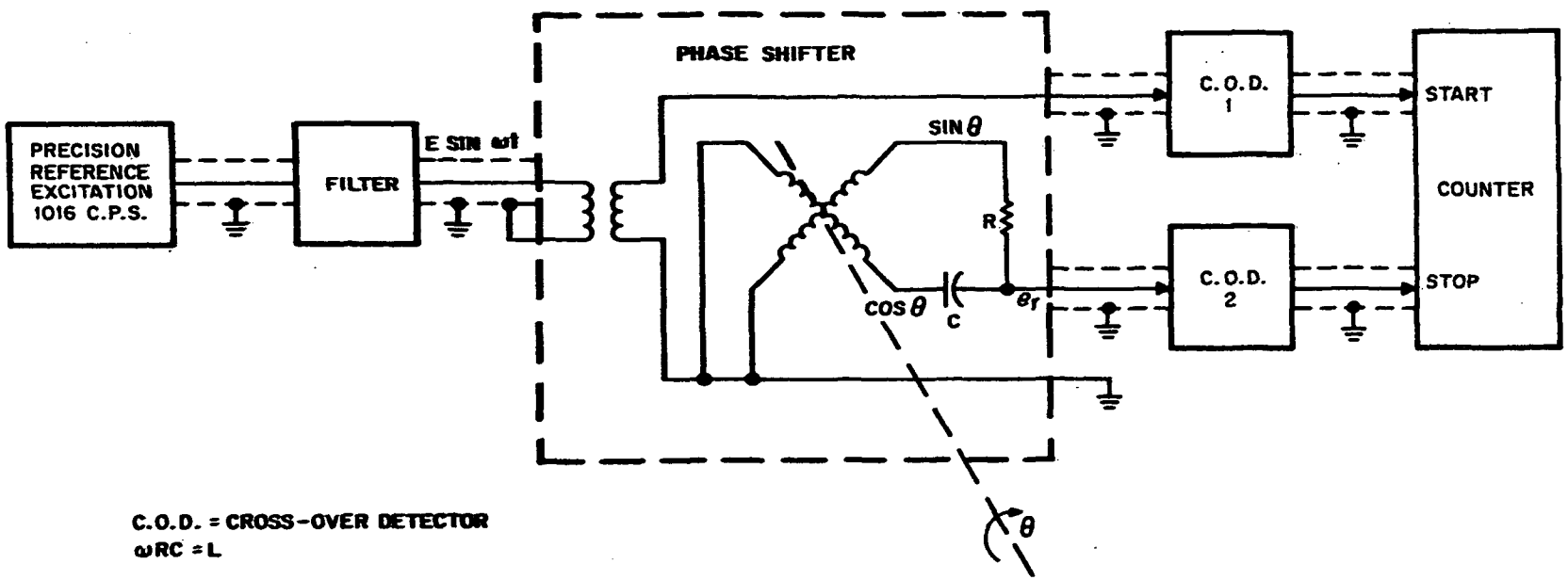


Figure IV-5. Angle Digitizer

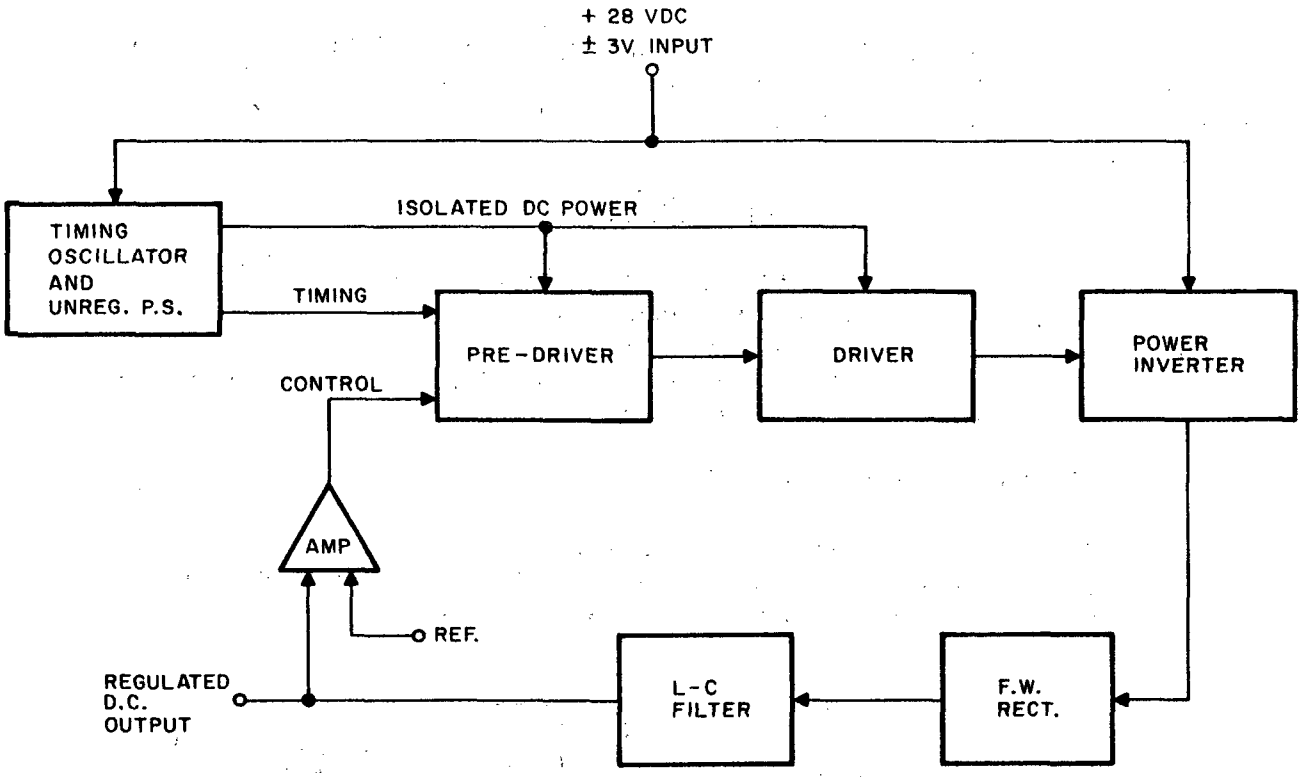


Figure IV-6. Pulse-Width-Modulated Power Supply Module Block Diagram

to the circuit losses and inversely proportional to the +28-V dc line voltage variations. The single section LC filter smoothes the modulated pulses into a low-ripple, regulated d-c voltage. Any variation in the average value of the output voltage is sensed by the feedback amplifier, and the error signal is used to control the power inverter pulse width.

The Saturn V guidance computer and data adapter require five d-c supply voltages. To handle the large current requirements of one of these supplies (+6 volts) with available high-quality components, this load is split and is furnished by two independent sources. The power supply subsystem consists of 12 power converter modules and 24 feedback amplifiers arranged to furnish 6 highly reliable power sources.

The efficiency of the complete d-c power system which uses duplexed modules will be approximately 60 percent. The efficiency of a comparable dual series-regulator power supply is estimated to be about 30 percent. The better efficiency of the pulse-width-modulated regulator is due primarily to the absence of any linear elements in series with the power source.

E. SPECIAL CIRCUIT DESIGN

Most of the digital circuits used in the DA are identical to those used in the computer. Some special circuits are needed to accommodate the interfaces to external equipment. Two special circuit designs are discussed in the following paragraphs.

1. 28-VOLT BUFFER INTERFACE CIRCUIT

A buffer circuit is used to convert the 28-volt digital input signals to 6-volt ground referenced signals, compatible with the DA logic circuitry. Since an input noise of 4 volts is expected, an inverter with input noise rejection of at least 7 or 8 volts is used. Either component redundant or TMR techniques can be used to obtain reliability.

2. RESOLVER FREQUENCY SOURCE

The 1016 cps frequency needed to drive the resolvers is obtained by counting down from computer timing pulses. This is accomplished with a three-stage ring counter followed by a latch. (See Figure IV-7.)

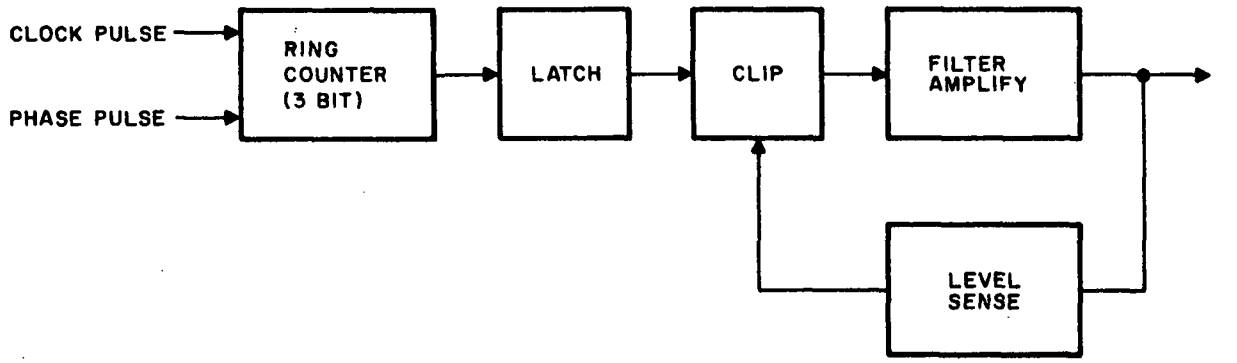


Figure IV-7. Resolver Frequency Source-Block Diagram

A variable clipper controls the amplitude of the 1016 cps square wave obtained from the counter. The clipping level is set by level-sensing detector-amplifier circuitry. The fundamental component of the square wave is obtained by filtering, and is amplified to a 26-volt level which is adequate to drive the resolvers. The 26-volt level is maintained by an amplitude sensitive feedback circuit. The harmonic content is reduced by filtering. This filtering is accomplished by incorporating frequency selective feedback techniques in the amplifier circuitry.

The resolver frequency source is duplexed in a sense, i.e., each source will supply power for half of the resolver inputs in such a manner that fine and coarse resolver excitation for any input parameter is not supplied by the same source. Since fine and coarse inputs serve as a backup for each other (under the proper program control), duplex redundancy is used for the excitation source.

F. PACKAGING

A packaging design similar to that employed for the computer is used for the data adapter. ULD's mounted on pages contain the majority of the digital circuits. Potted cordwood-type Circuit Modules mounted on MIB's are used where high-dissipation circuits or circuits requiring large precision components are needed, Figure IV-8. Ten CM's are mounted on a page which contains electronics on one side only. The CM pages require the mounting space of three ULD pages. The area under the cantilevered CM pages is used for interconnection between backpanels. The layout of the DA package is shown in Figure IV-9.

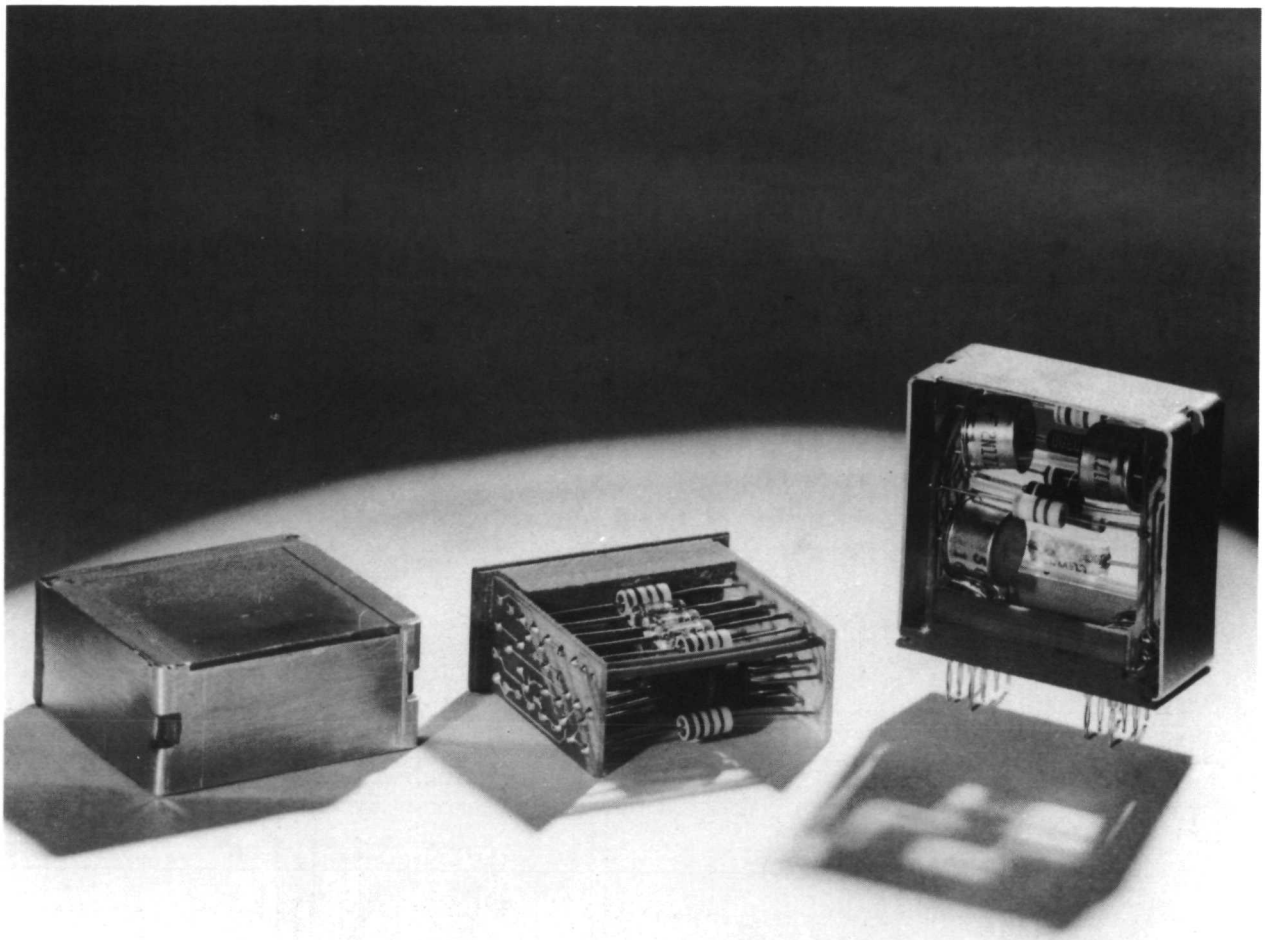


Figure IV-8. Data Adapter Circuit Module

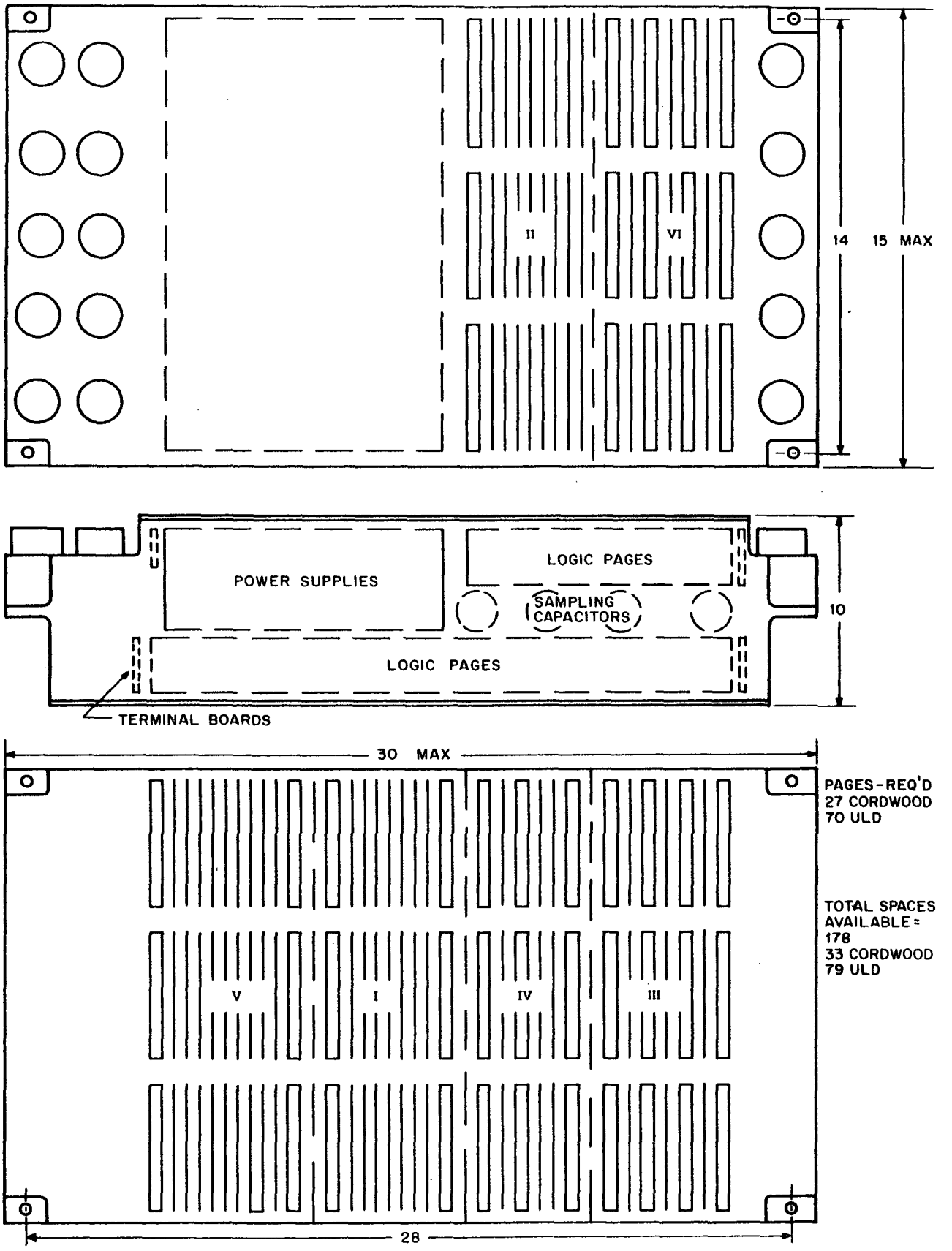


Figure IV-9. Data Adapter Packaging Layout

Section V

LABORATORY TEST EQUIPMENT

Section V

LABORATORY TEST EQUIPMENT

A. GENERAL

Four machine types are used to test the computer and data adapter. These machine types are as follows:

- Saturn V Computer Manual Exerciser (ACME)
- Saturn V Data Adapter Processor Tester (ADAPT)
- Saturn V Test and Evaluation Console (ASTEC)
- Saturn V Test and Operational Monitor (ATOM)

The ACME tests the computer as a unit, monitoring the computer as it runs a special program that exercises the hardware to the maximum possible extent. The ACME is not designed to be used with computer operational programs, but is used in conjunction in hardware acceptance and qualification testing.

The ADAPT tests the DA. It is capable of (1) exercising the interface between the computer and DA, and (2) simulating the inputs to the DA and accepting its outputs, both digital and analog. The ADAPT will be used in production build-up, acceptance testing and qualification testing of the DA.

The ASTEC can test the computer alone, the DA alone, and the computer/DA combination. The ASTEC is used for computer and DA hardware check-out and for operational program check-out and acceptance tests. The ASTEC is also used in troubleshooting the computer and DA by implementing malfunction isolation techniques.

The ATOM facilitates analysis of the computer and DA. It enables an operator to observe either the contents of the accumulator or the memory register at a particular instruction address time and perform control operations on the computer. The ATOM will be used in an Instrument Unit breadboard for operational testing.

B. MACHINE CONFIGURATION

The ACME tester (see Figure V-1) consists of two standard IBM double-cube modules bonded together and a single-cube module. One of the double-cube modules contains a high-speed paper-tape reader and its controls. The reader is used for computer memory loading and verification. The other double-cube module contains control switches and visual displays of computer registers and test points. The electronics and power supplies for ACME,

as well as the power supplies for the Saturn V computer under test, are contained in the lower sections of these two modules. The single-cube module is a test stand on which the computer is mounted during test. Auxiliary cooling cart must be used with the ACME, ADAPT and ASTEC testers when liquid cooling is to be provided to the computer; cooling equipment is located in the test stands in each test equipment.

The ADAPT tester is similar in appearance to the ACME (see Figure V-2). A pair of double-cube modules are bonded together, one containing a high-speed tape reader for loading the internal test processor memory and the other containing controls and displays. A test stand for mounting the DA during test is composed of a single-cube module containing tester electronics. An IBM electric typewriter is used for printing the test results.

The ASTEC installation configuration is shown in Figure V-3. The two single-cube modules supporting the computer and DA are bonded together as a single test stand unit, and the display and processor modules are bonded together as a single unit. The printer is a separate unit; it may be installed remotely from the other ASTEC units if desired. A double-cube module containing a high-speed tape reader is also part of the tester.

Figure V-4 shows the installation configuration of the ATOM. The control panel is mounted on a 19-inch relay rack provided by MSFC, and the electronics module is positioned as close to the computer in the breadboard instrument unit as is practicable.

C. DETAILED DESCRIPTION

1. ACME

The ACME consists of three basic sections: Memory Core Loader (MCL), Data Display (DD), Interface Exerciser (IE), and Power Control and Distribution.

The MCL is capable of loading and verifying both diagnostic and operational programs. A photoelectric tape reader which operates at 500 characters-per-second is used for loading. The MCL modes of operation are as follows:

- Primary mode — initially places the computer memory to "hard zero".
- Lamp test mode — self-check for all of the MCL lamps.
- Automatic mode — automatic loading and verification of the computer memory.
- Manual mode — manual operation of the MCL.

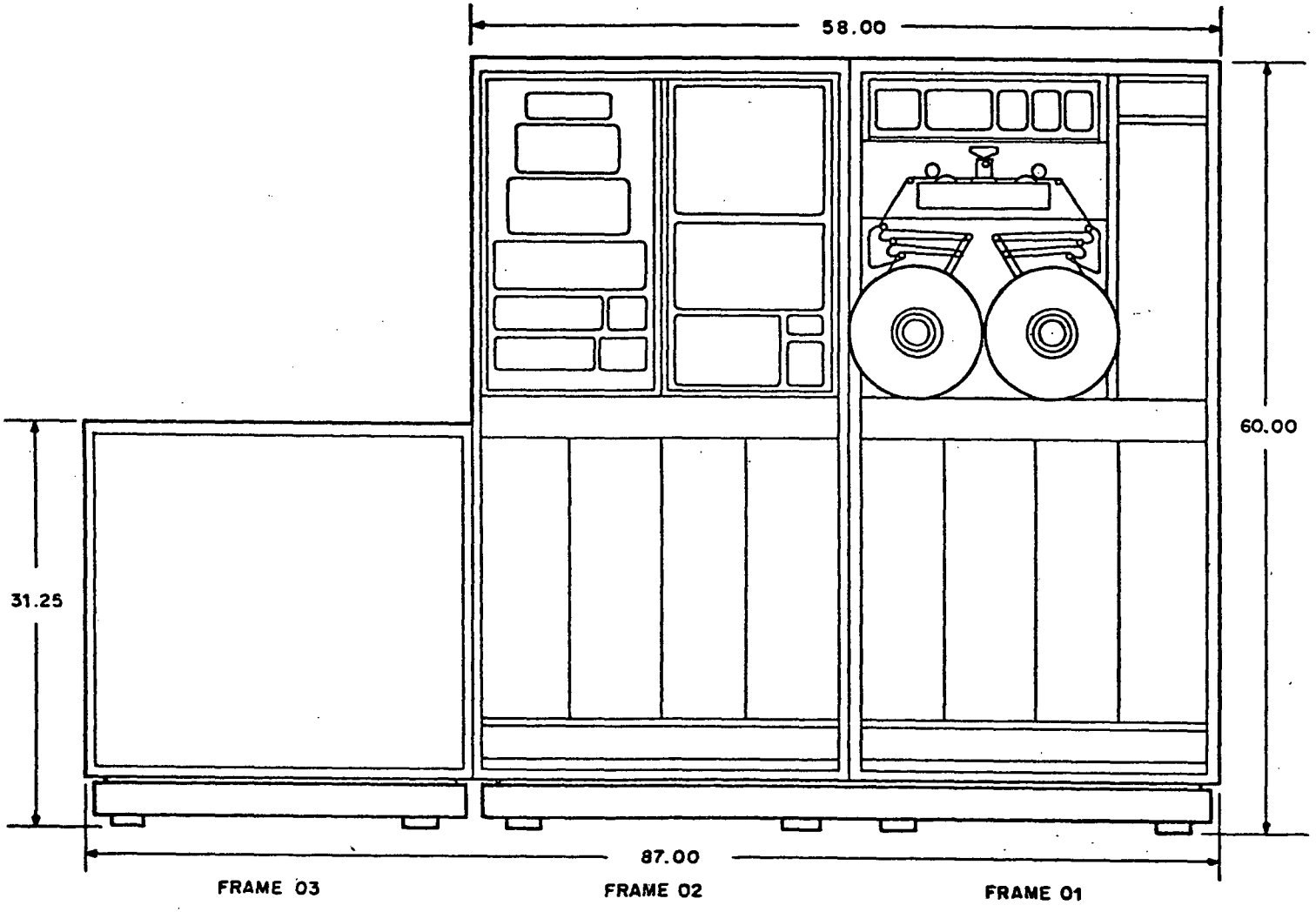


Figure V-1. ACME Installation Outline Drawing

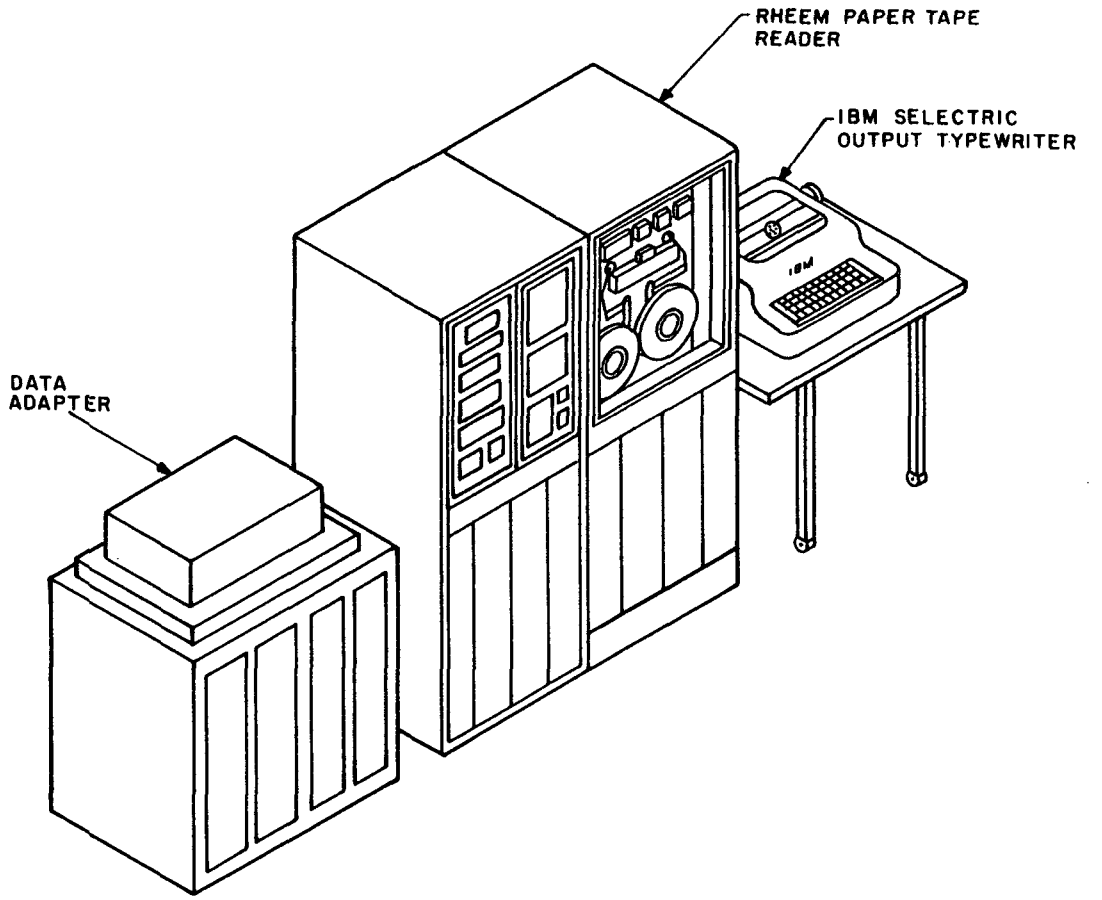


Figure V-2. ADAPT Installation Outline Drawing

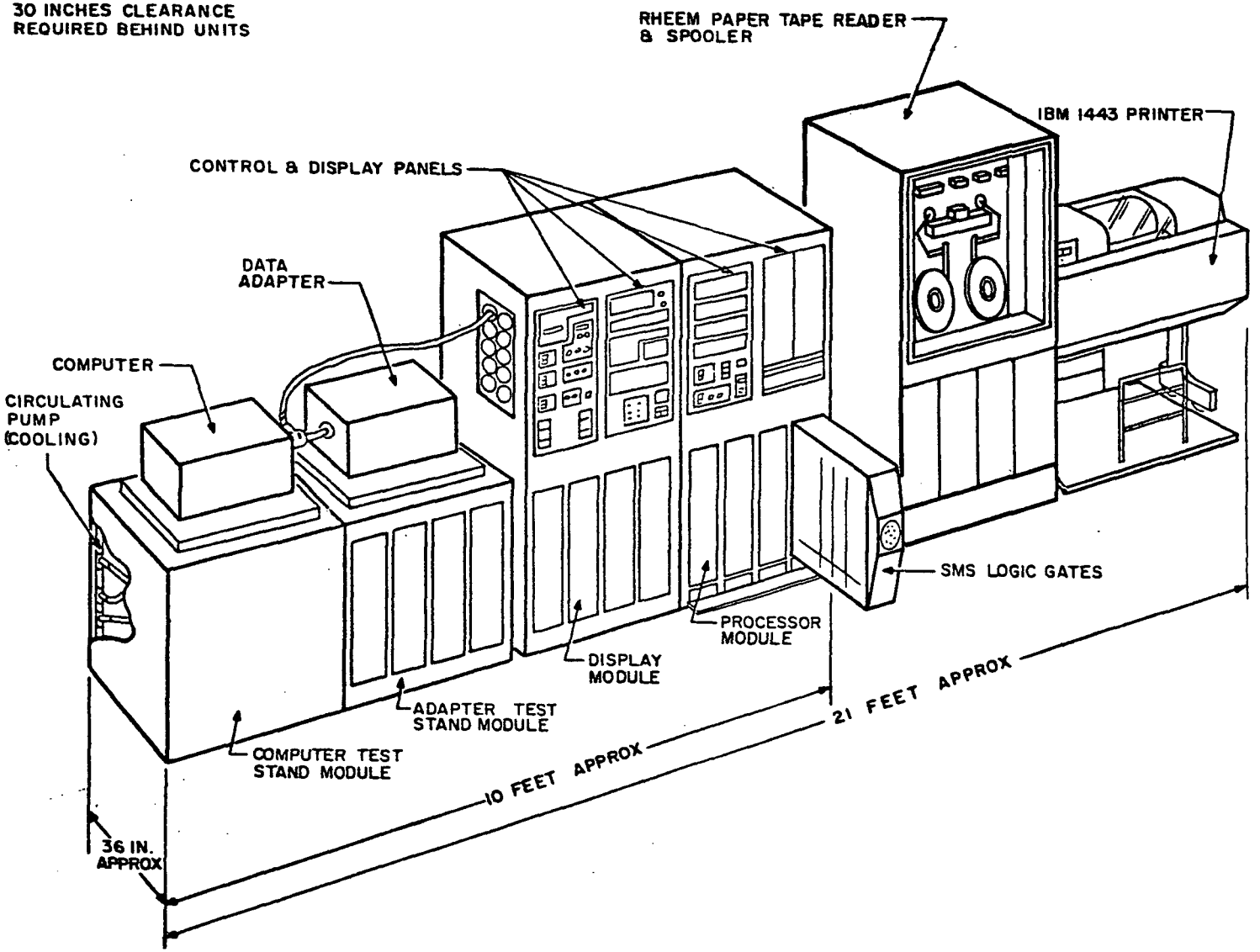


Figure V-3. ASTEC Installation Outline Drawing

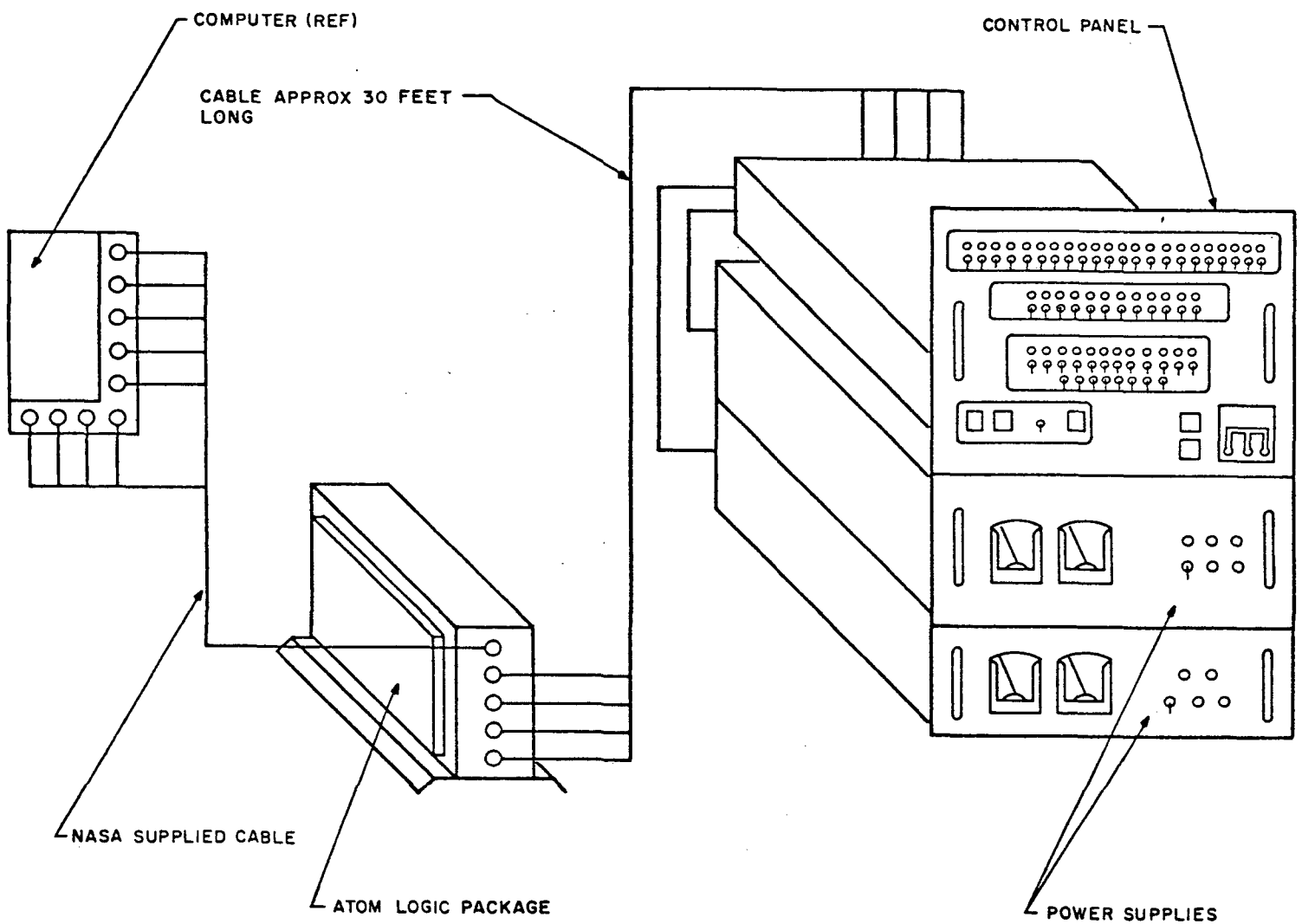


Figure V-4. ATOM Installation Outline Drawing

The basic modes of operation of the DD are as follows:

- Switch-selected data input
- Spare data probe data input
- Repeat-display
- Single-display
- Single-step
- Automatic/manual restart
- External oscilloscope synchronization
- External oscilloscope marker
- Lamp test

The IE provides signal inputs to the data adapter-computer interface. With these inputs, the internal demonstration program exercises the computer hardware to the maximum extent. However, the IE is not used with operational programs.

2. ADAPT

The ADAPT contains circuits which interface with all DA external connections. It provides stimuli to DA inputs via a multiplex and distributor, and receives data and control pulses from DA outputs. Testing is controlled by a digital processor which has a magnetic core memory and a simplified instruction set.

The processor directs the tests to be performed by reading out digital information from its memory for DA inputs, and comparing DA outputs with prestored results. Data may also be recorded in the memory for later printout and analysis if desired.

The processor is a serial binary machine which operates with a clock frequency of 2.048 mc in a four-clock-pulse logical organization.

A description of the processor manual and program control follows.

a. Manual Control – Console Lights and Switches

Lamps are used on all the processor data paths, registers, parity and error latches, including the timing unit generator, the output distributor and input multiplexer registers. The following manual switch controls are used:

- MAR Compare
- Buffer Load
- Transfer Register Load
- Instruction Register Load
- Multiplexer Load
- Distributor Load

- Reset – on-off power and timing
- Single Cycle
  1) Multiple instruction
  2) Single instruction
  3) Single phase
- Interrupt by-pass
- Internal- external timing source

b. Program Control – Stored Program - Instruction Repertoire

The following processor instructions are the minimum required; all instructions take a maximum of 82 usec for execution.

HOP	SUB
TRA	STO
TNZ	PI0
TMI	CLA
SHF	CI0 – Control Input/Output
AND	BIO – Branch if Indicator On
ADD	

3. ASTEC

The ASTEC performs the combined functions of the ACME and ADAPT machines, and in addition, is capable of checking out operational programs on the computer, and operating the computer and DA in combination. ASTEC uses the same processor that is used in ADAPT and has a printer attachment for recording output results, telemetry data and processor memory dumps. The ASTEC is intended for field use while ACME and ADAPT are basically factory-oriented equipment.

4. ATOM

The ATOM can force the computer to operate in single operation increments (Single-Step Mode). When this mode of operation has been selected by the operator, the computer is stopped immediately after performing either of the following:

- The instruction whose address has been set into the appropriate switches on the ATOM Control and Display Panel, or

- The instruction in process at the time of operating the "STOP" button on the ATOM Control and Display Panel.

The computer is run in single instruction increments by pressing the "ADVANCE" button on the Control and Display Panel. As each computer operation is performed, the ATOM displays either the data read out of memory or the contents of the accumulator and either the current instruction or its address, as selected by the operator. Although the ATOM can control all channels of a TMR computer, it can monitor only one such channel.

In addition, the operator can force the application of the computer control signal HLT (instead of entering Single-Step Mode) by either of the two procedures previously described. With the computer stopped, any location in its memory can be loaded or verified manually. When all desired program alterations have been completed, the operator can load a HOP instruction at the starting address and a HOP constant at the operand address specified by the HOP instruction. This constant causes a HOP to any desired point in the program, from which point the computer either resumes normal operation or is placed in Single-Stop Mode, as decided by the operator.