270 Clock Ckt.

÷5, ÷6, ÷10, Sync

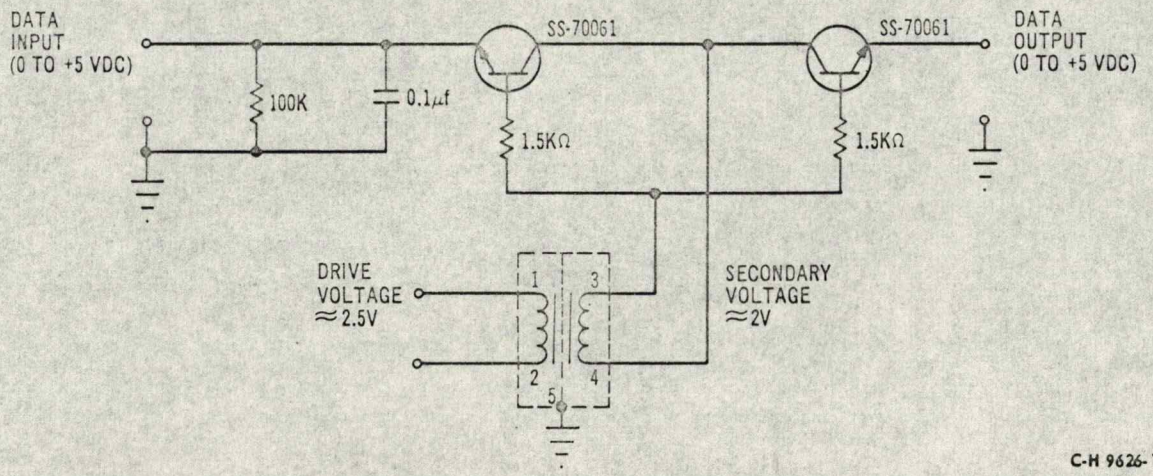

FIGURE 2-1. SELECTOR SWITCH SCHEMATIC

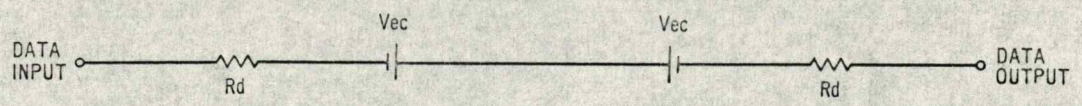

FIGURE 2-2. SELECTOR SWITCH EQUIVALENT CIRCUIT

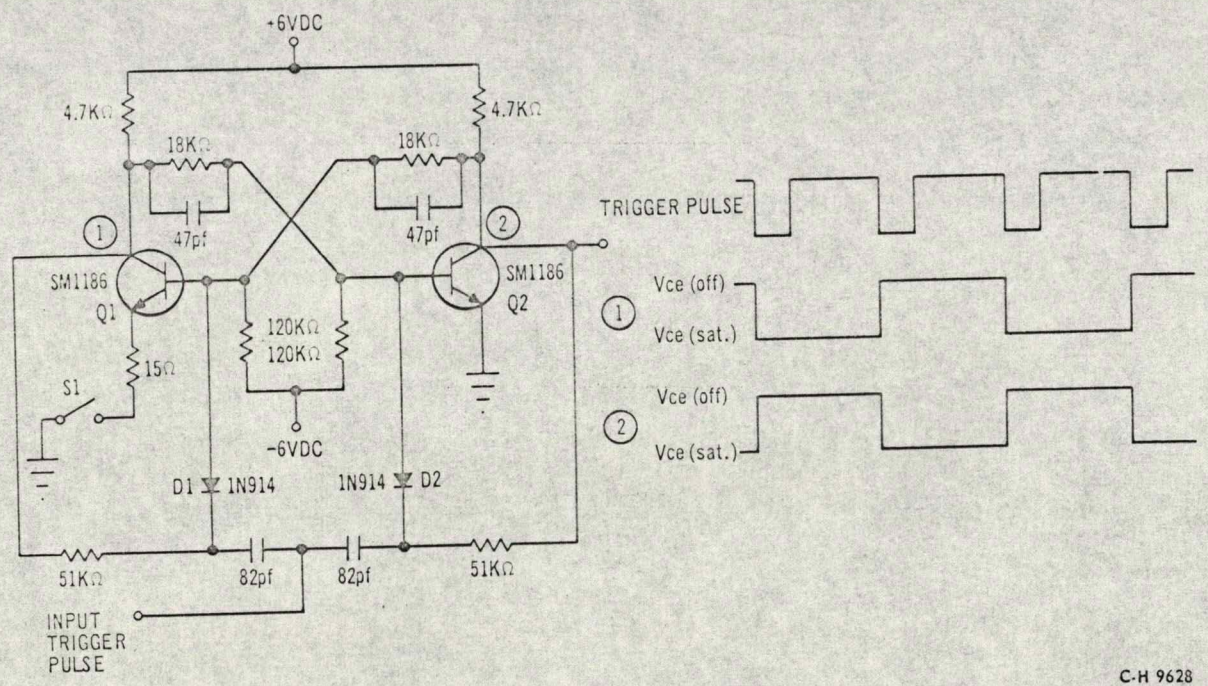

FIGURE 2-3. COUNTER SCHEMATIC

The flip-flop operates as follows: Assuming initially that S1 has been opened and then closed (that is, a reset state exists where Q1 is off and Q2 is on) approximate Q2 voltages are

$V_{ce\,(sat.)} \approx 0.3$ v

$V_{be\,(sat.)} \approx 0.7$ v

Approximate Q1 voltages are

$V_{ce\,(off)} \approx 5.0$ v

$V_{be\,(off)} \approx 0.5$ v

NOTE: The Vce (off) magnitude depends on the external load connected to the flip-flop.

Under the above conditions, the cathode of D1 is at approximately +5 volts and D2 at approximately +0.3 volts. A negative going input trigger pulse (CP, F5, or AT) of

approximately 5 volts then switches the flip-flop to the stable state, i.e., Q1 on and Q2 off. The negative pulse passes through D2 and reverse-biases the base-emitter junction of Q2, thus switching Q2 off. (The negative pulse will not pass through D1 since the cathode is already at a +5-volt level.) Switching Q2 off applies a positive base voltage to Q1, forward-biasing the base-emitter junction and switching Q1 on. Upon application of the next trigger pulse, the process repeats itself, switching the transistors back to the original stable state.

The collector of Q2 is the trigger input line to the next stage of the counter. Since the collector of Q2 (or Q1) will have a negative going pulse condition occurring with every other input trigger pulse, the flip-flop is operating in a normal divide-by-two manner and this will be propagated to the next stage whose output will be a divide-by-four (of the original trigger input pulses).

2.4 GATE OPERATION

One type of gate used in the model 270 multiplexer is shown schematically in figure 2-4 and is used on the five counter board to decode the count of one, F1.

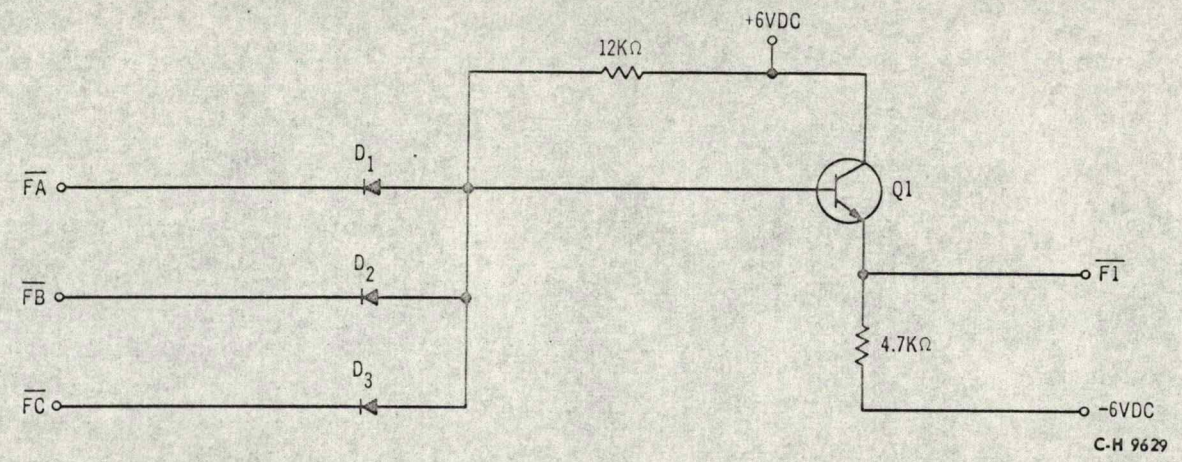

FIGURE 2-4. GATE SCHEMATIC

Circuit operation is as follows: If one of the inputs ($\overline{FA}$, $\overline{FB}$, or $\overline{FC}$) is low, the diode connected to that particular

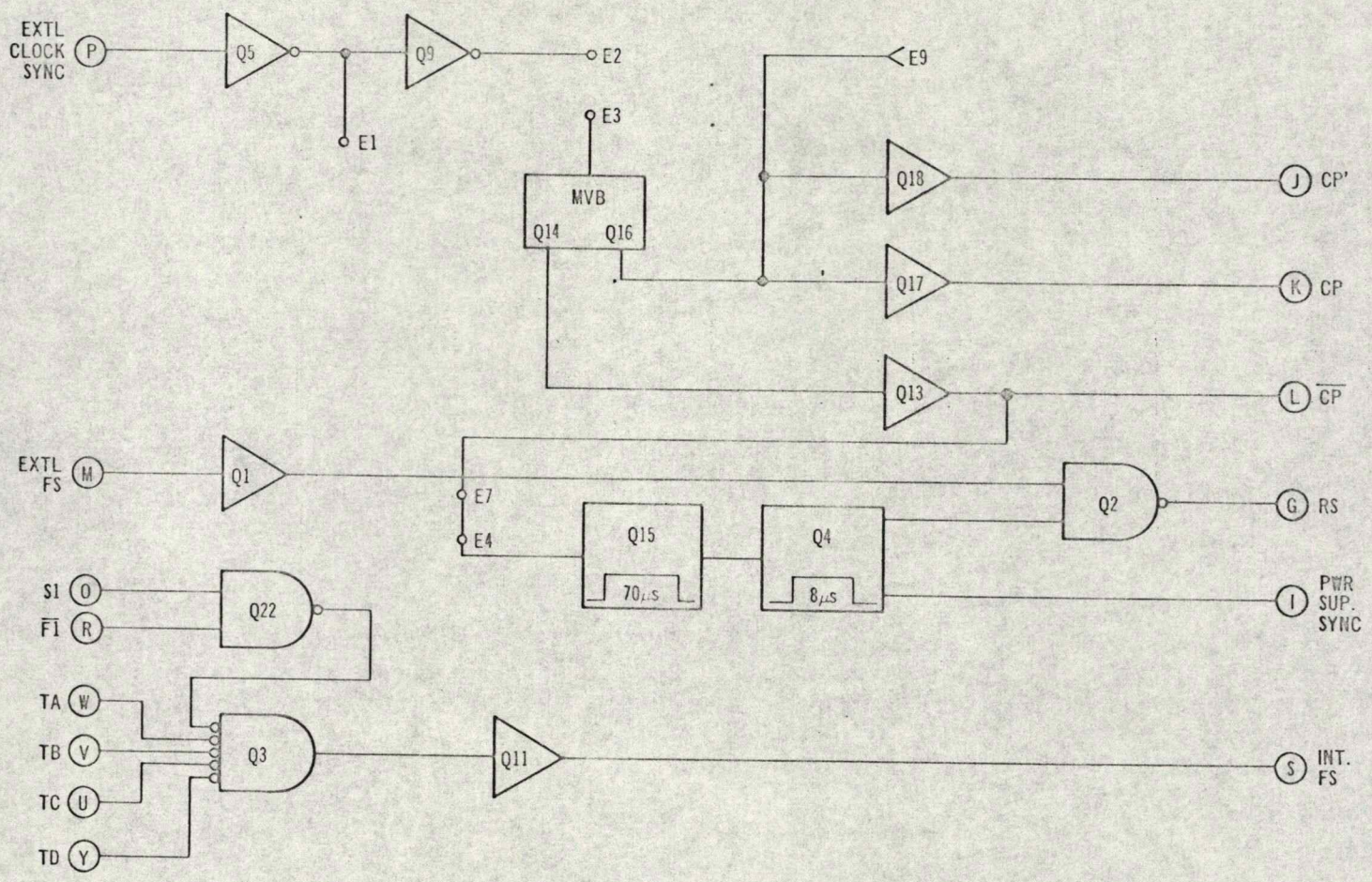

FIGURE 5-1. CLOCK AND FRAME SYNCHRONIZER LOGIC DIAGRAM

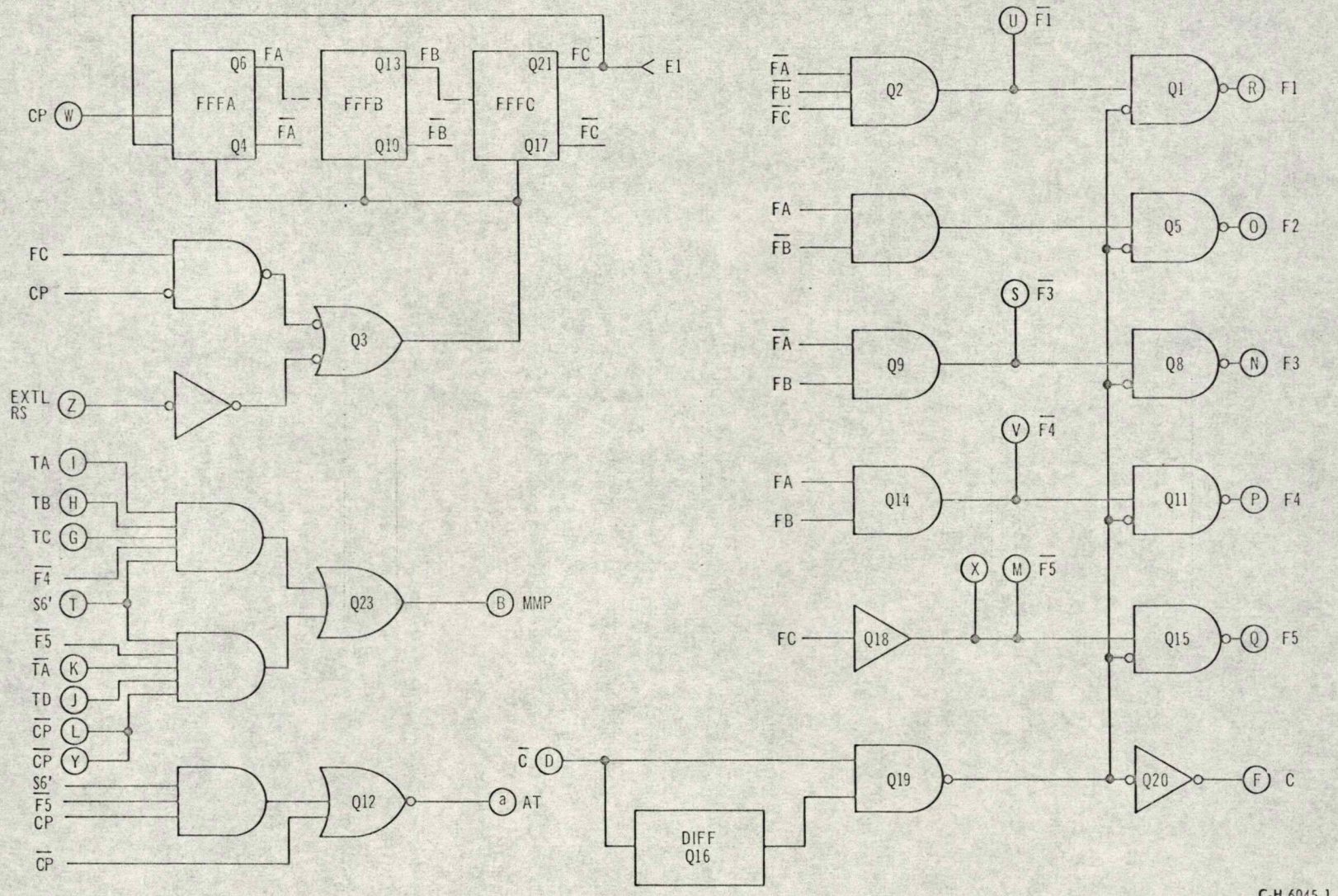

FIGURE 5-2. "F" COUNTER AND DECODER LOGIC DIAGRAM

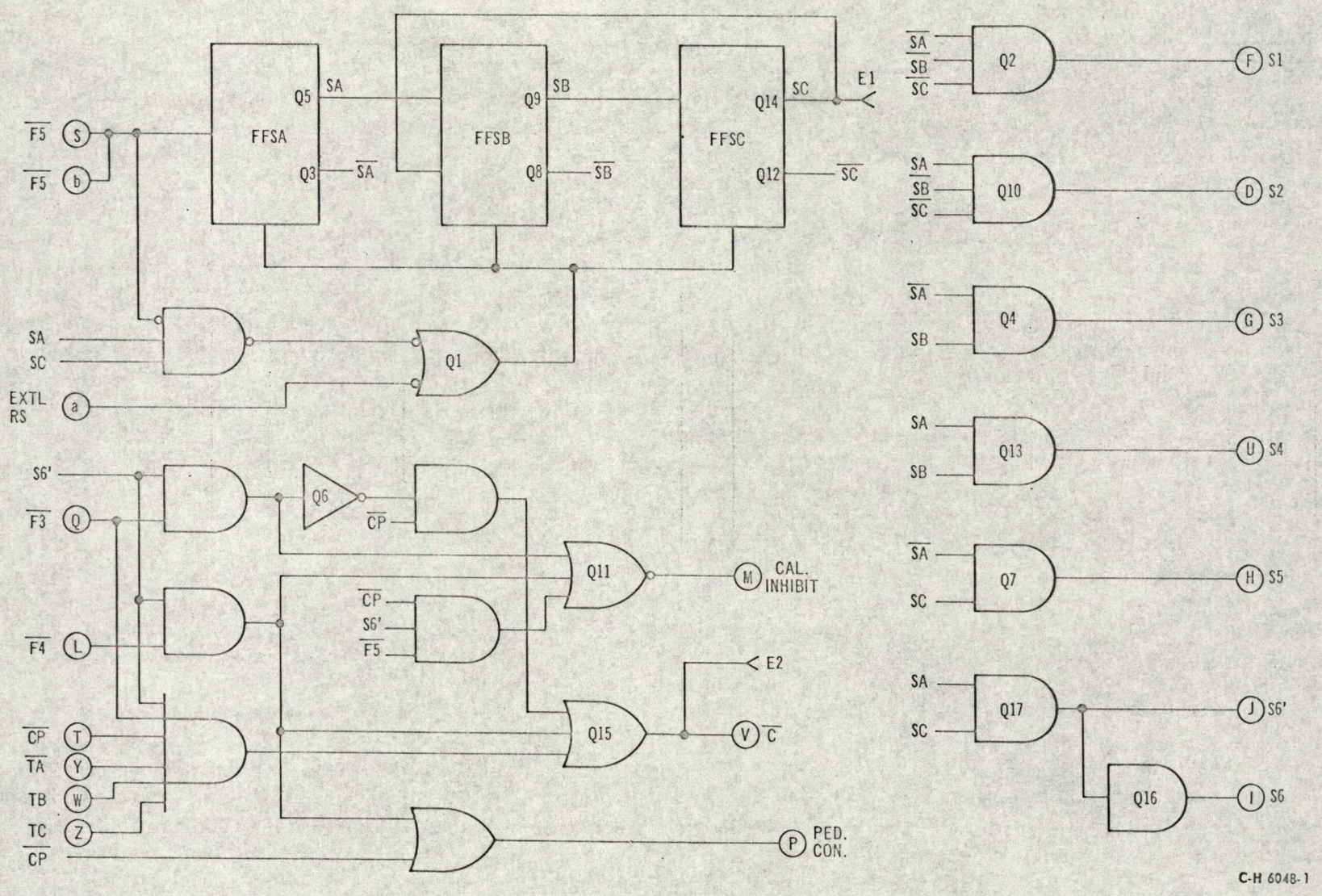

FIGURE 5-3. "S" COUNTER AND DECODER LOGIC DIAGRAM

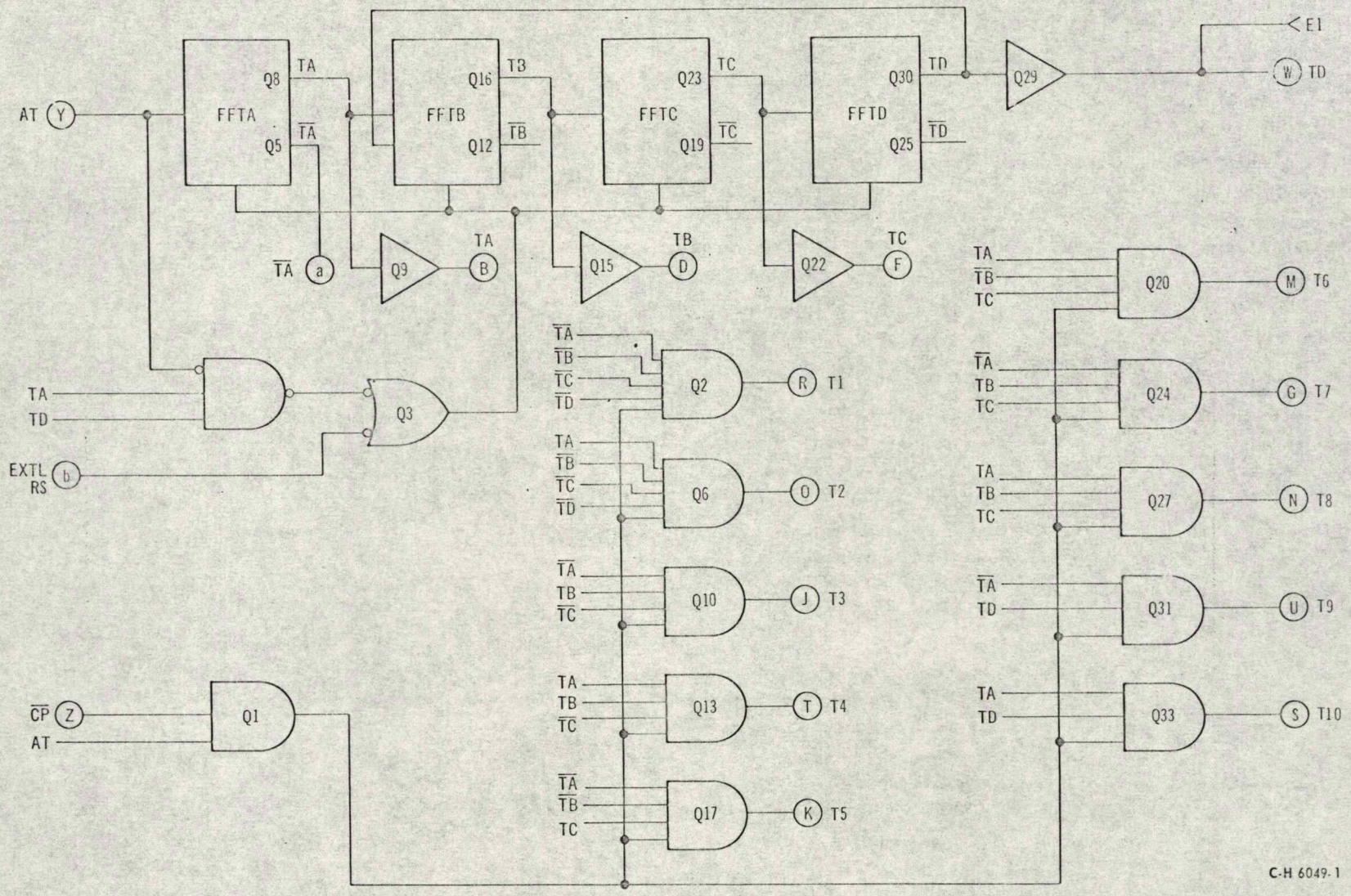

FIGURE 5-4. "T" COUNTER AND DECODER LOGIC DIAGRAM

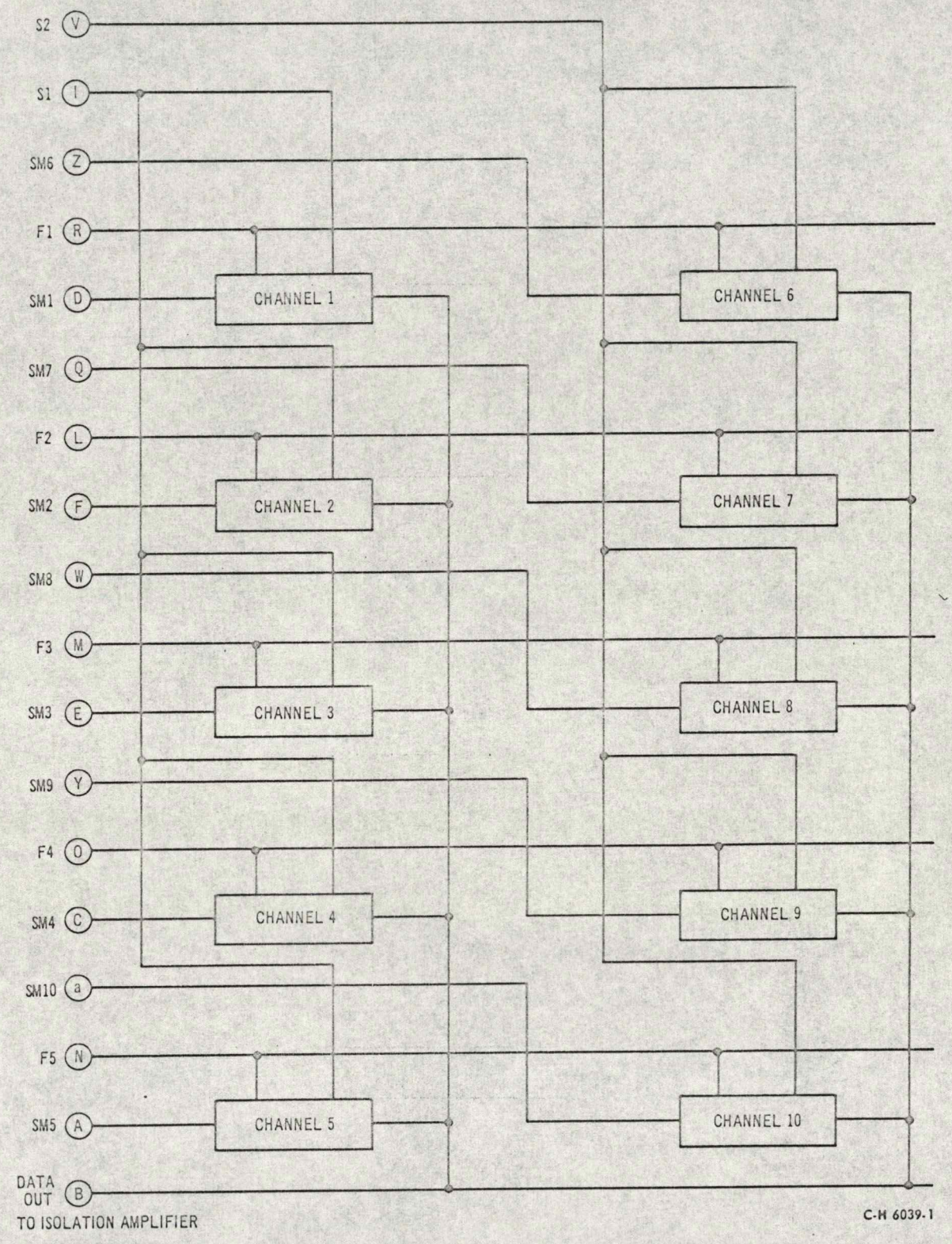

FIGURE 5-5. MAIN MULTIPLEXER CHANNELS 1 THROUGH 10 LOGIC DIAGRAM

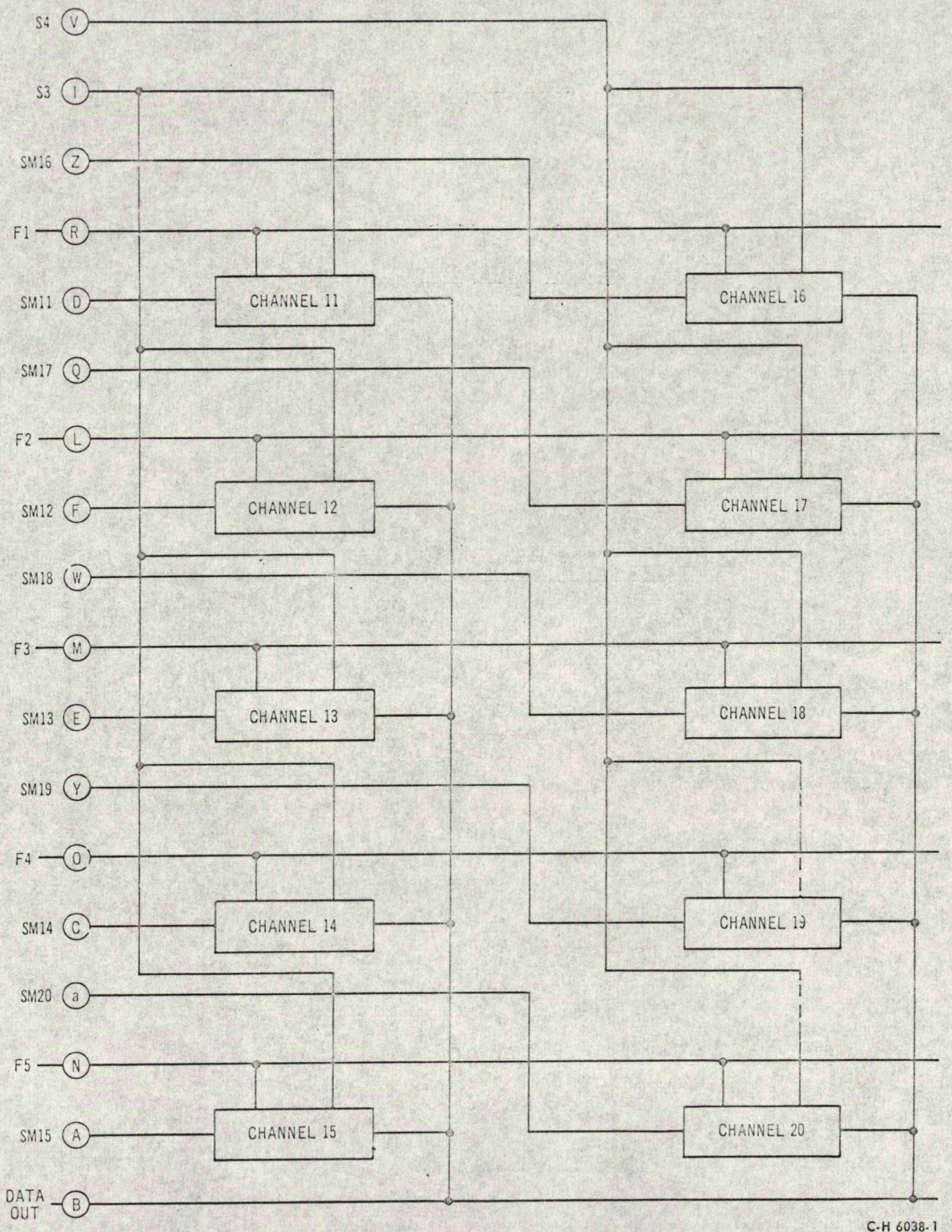

FIGURE 5-6. MAIN MULTIPLEXER CHANNELS 11 THROUGH 20 LOGIC DIAGRAM

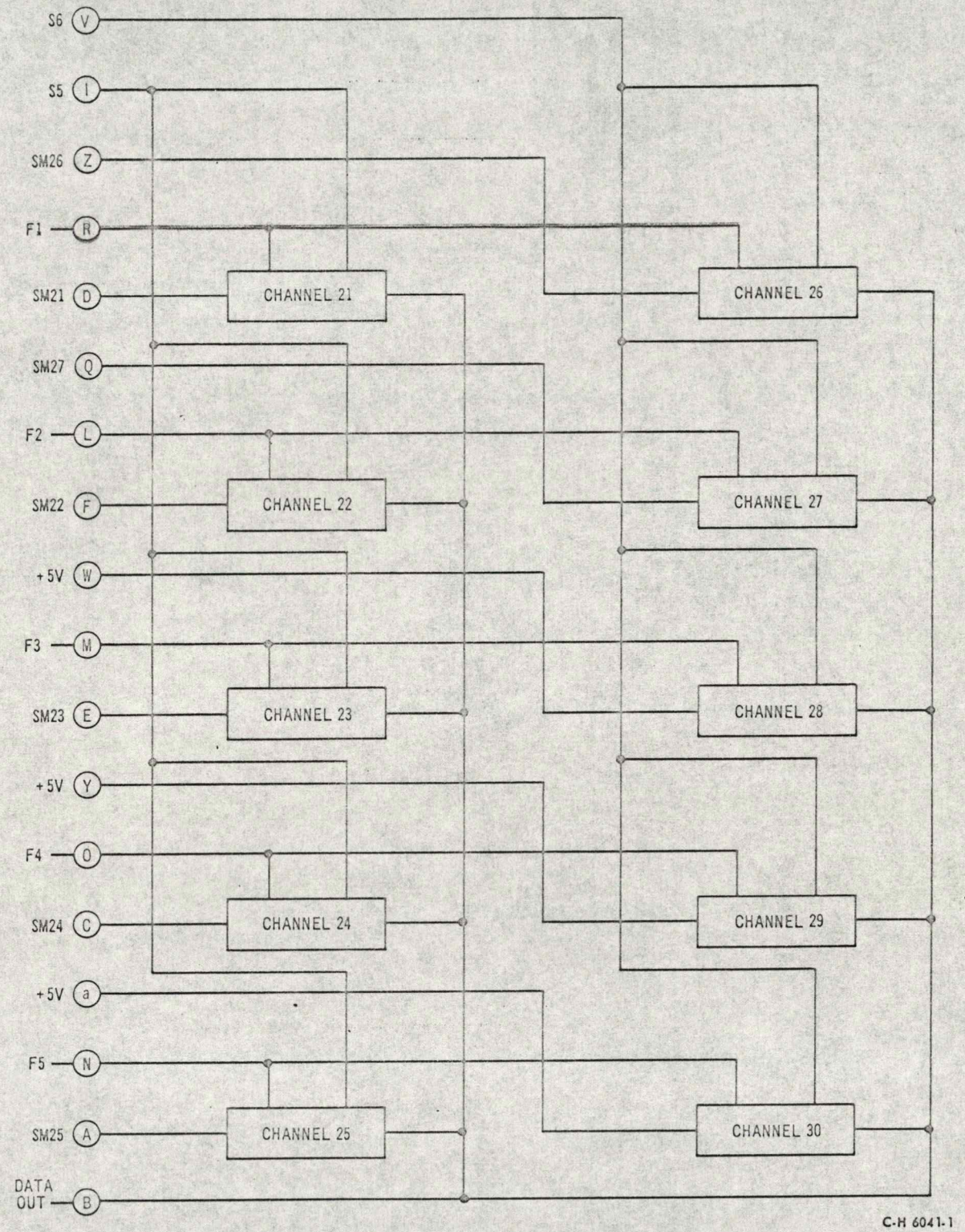

FIGURE 5-7. MAIN MULTIPLEXER CHANNELS 21 THROUGH 30 LOGIC DIAGRAM

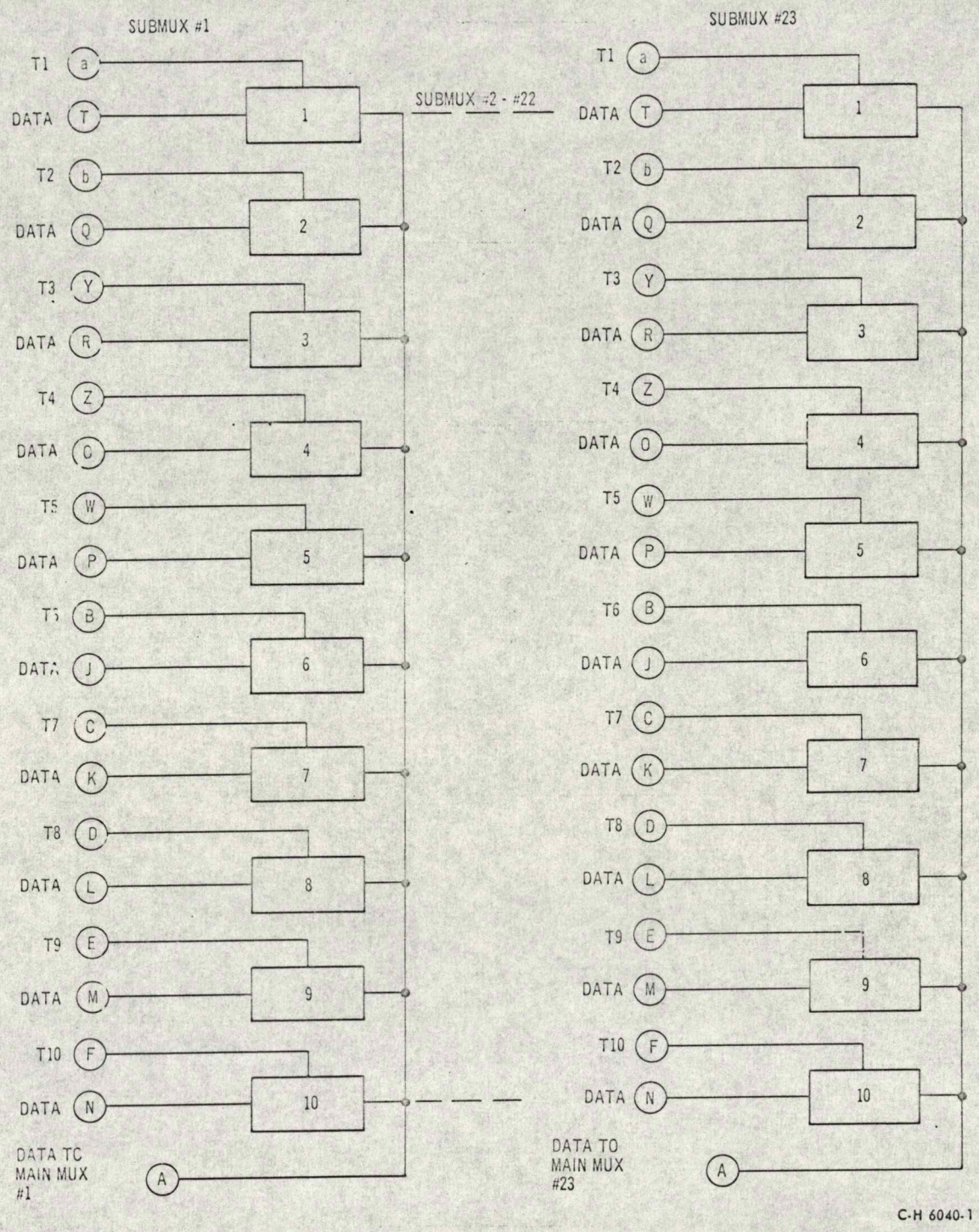

FIGURE 5-8. SUBMULTIPLEXERS 1 THROUGH 23 LOGIC DIAGRAM

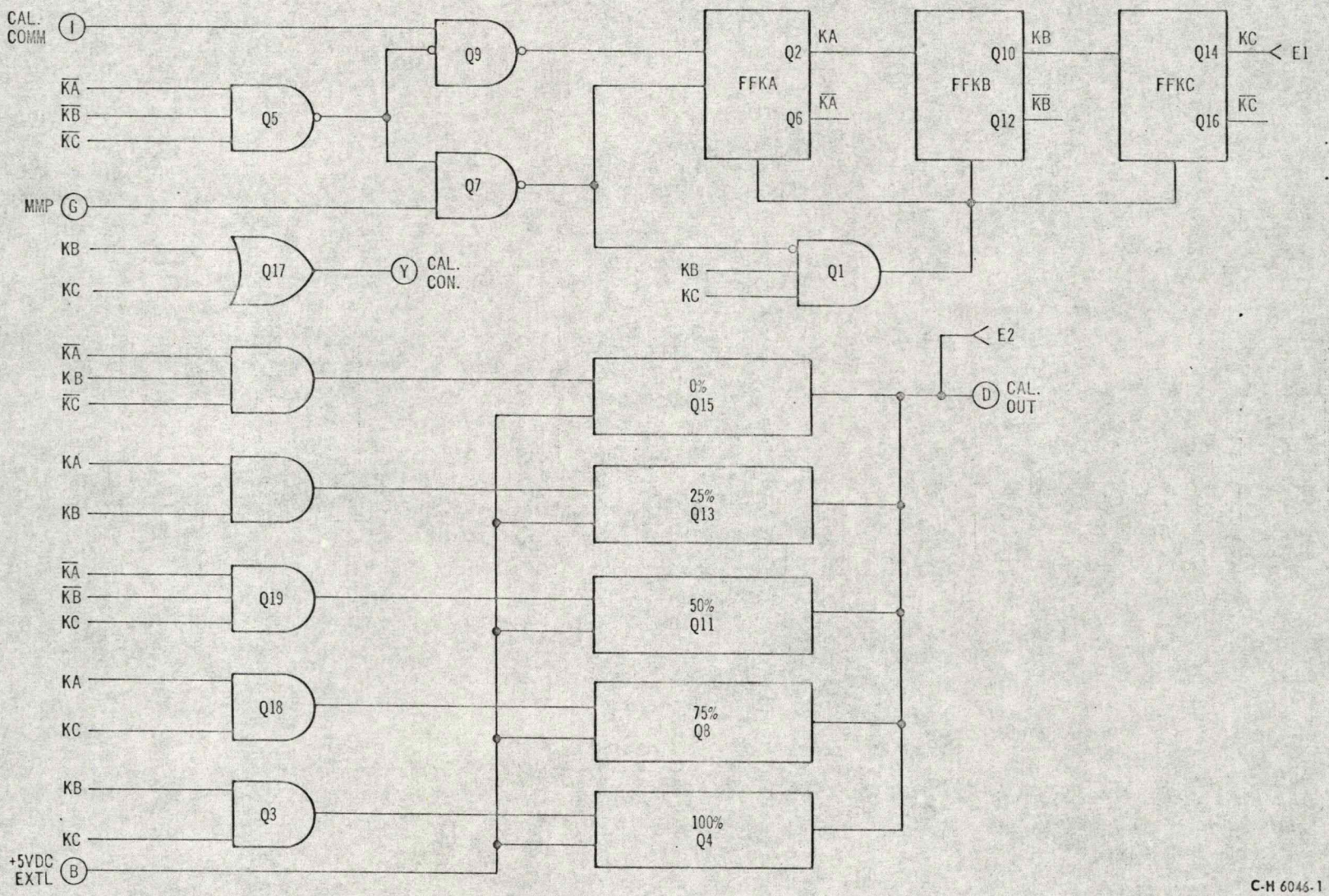

FIGURE 5-9. CALIBRATOR LOGIC DIAGRAM

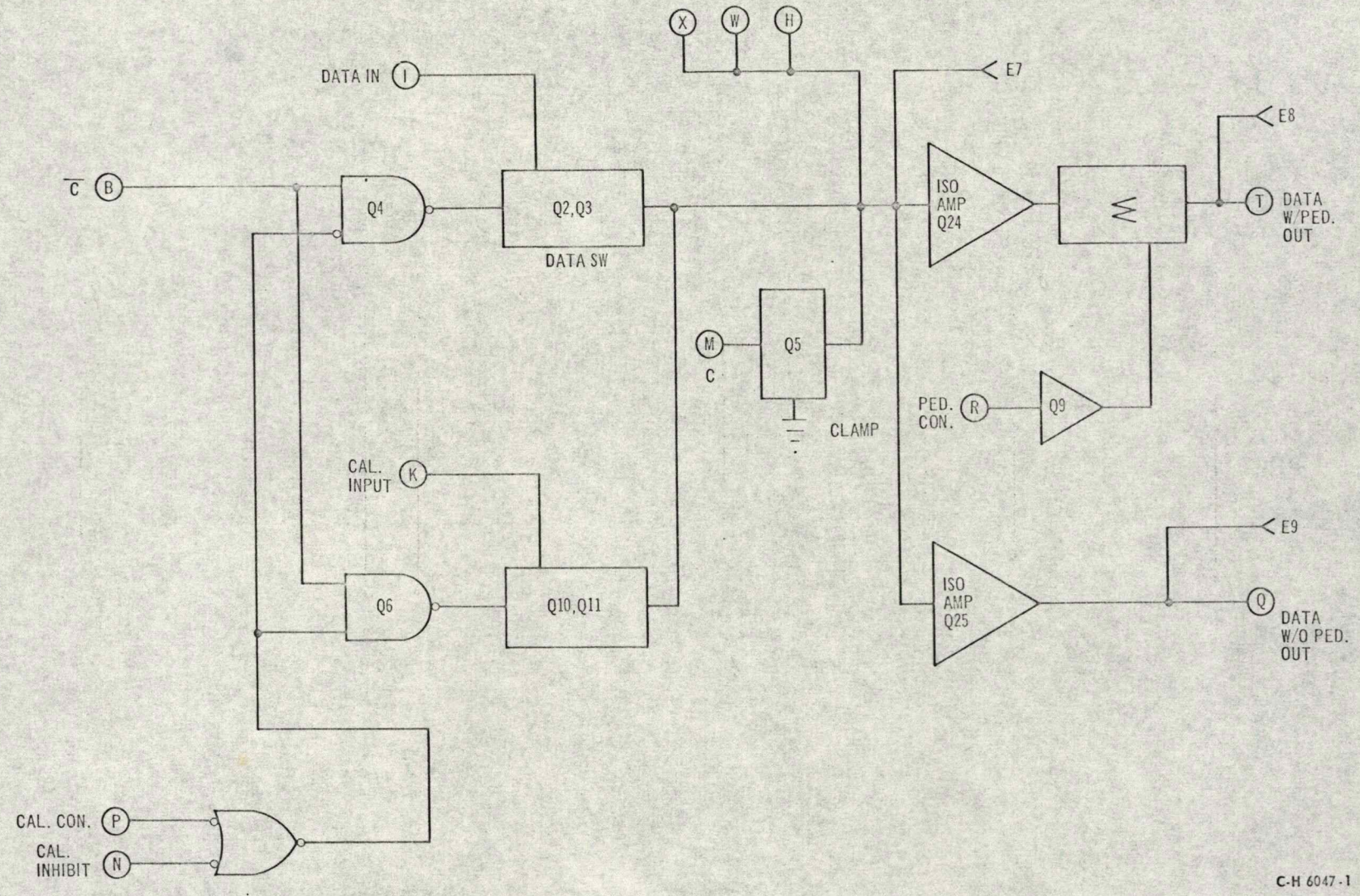

FIGURE 5-10. ISOLATION AMPLIFIER LOGIC DIAGRAM