

APOLLO
GUIDANCE & NAVIGATION
EQUIPMENT
FAMILIARIZATION MANUAL
CHAPTER 5
COMPUTER SUBSYSTEM

RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION

RAYTHEON

APOLLO

GUIDANCE & NAVIGATION

EQUIPMENT FAMILIARIZATION MANUAL

CHAPTER 5

COMPUTER SUBSYSTEM

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Chapter 5

COMPUTER SUBSYSTEM

5-1 INTRODUCTION

Chapter 5 contains descriptions of the functional and physical configurations of the Computer Subsystem portion of the Apollo Guidance and Navigation System. Interface, machine instructions, and programs are described also.

5-2 GENERAL THEORY

5-2.1 COMPUTER SUBSYSTEM INTERFACE. The relationship of the Computer Subsystem to the Spacecraft and the Inertial and Optical Subsystems is shown on figure 5-1. The Computer Subsystem consists of two Display and Keyboards (DSKY's) and the Apollo Guidance Computer (AGC). The DSKY's provide outputs to the AGC, Spacecraft, and Inertial Subsystem. The AGC accepts and processes inputs from, and provides outputs to, the Spacecraft and the Inertial and Optical Subsystems.

The DSKY's allow the astronauts to load information into the AGC, to initiate various program functions, and to perform tests on the Computer and other subsystems of the Guidance and Navigation System. In addition, the DSKY's indicate failures in the AGC, display the program functions being executed by the AGC, and can display specific data selected by the keyboard input. The DSKY's function also to route data from the AGC to the Inertial and Optical Subsystems and the Spacecraft. Commands for switching operation to different modes are supplied to the Inertial Subsystem, and data is supplied to the Spacecraft Telemetry System. A block uplink signal can be applied to the Spacecraft Telemetry System to prevent uplink words from being entered into the AGC. In conjunction with the AGC, the DSKY's supply alarm indications to the Spacecraft and the Inertial Subsystem.

The AGC is the control and processing center of the Guidance and Navigation System. It processes data and issues discrete bit and control signals both for the Guidance and Navigation System and the other Apollo Spacecraft Systems. The AGC is a control computer with many features of a general purpose computer. As a control computer, the AGC aligns the Inertial Measurement Unit (IMU) in the Inertial Subsystem, positions optical subsystem components, and issues control commands to the Spacecraft. As a gen-

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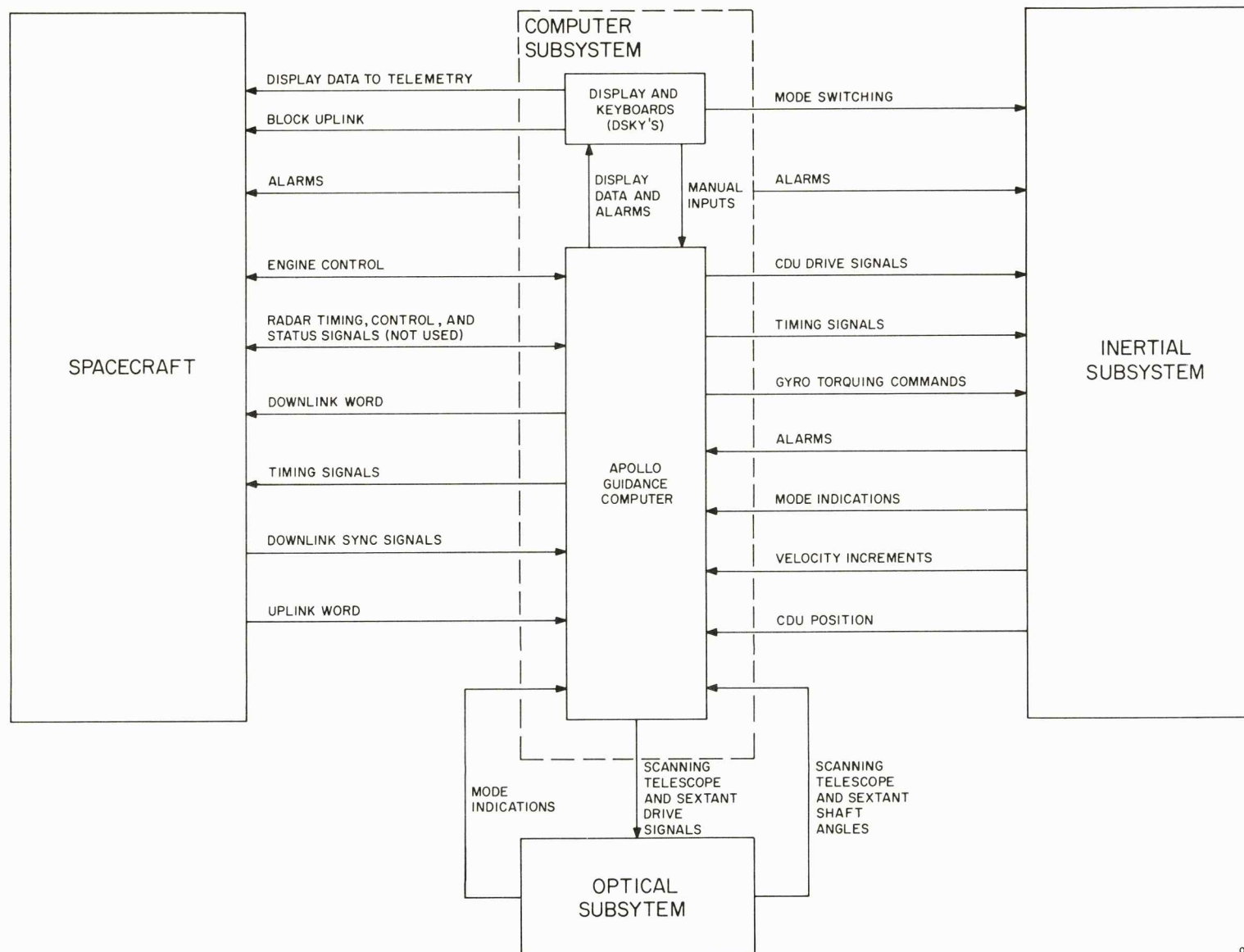


Figure 5-1. Computer Subsystem, General Interface

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eral purpose computer, the AGC solves guidance and navigation problems required for the round trip to the moon. In addition, the AGC monitors the operation of the Guidance and Navigation System.

The AGC stores data pertinent to the flight profile that the Spacecraft must assume in order to complete its mission. This data, consisting of position, velocity, and trajectory information, is used by the AGC to solve the flight and steering equations during orbital injections and midcourse velocity corrections. The results determine the required magnitude and direction of thrust, noted as engine control signals on figure 5-1. Corrections to be made are established automatically by the AGC. The spacecraft engines are turned on at the correct time, and steering signals are generated by the AGC to re-orient the Spacecraft to a new trajectory, if required. The Inertial Subsystem senses velocity changes and supplies these changes to the AGC for calculating the total velocity. Drive signals are supplied from the AGC to Coupling and Display Units (CDU's) in the Inertial Subsystem to set the gimbal angles in the IMU. CDU position signals are fed to the AGC to indicate gimbal angles and to cause the generation of drive signals, if required. The AGC receives mode indications and shaft angles from the Optical Subsystem during optical sightings. This information is used by the AGC to calculate present position and refine trajectory information. Optical subsystem components can also be positioned automatically by drive signals supplied from the AGC. The radar timing, control, and status signals are not used at present.

The uplink word from the Spacecraft Telemetry System originates in ground based stations and is supplied to the Computer Subsystem. This word provides ground based operators with a computer control capability similar to that available with the DSKY's.

Data specifically selected by program functions is used to compose downlink words which are supplied to the Spacecraft Telemetry System for transmission to ground based stations. The entire operation is synchronized by signals supplied to the AGC from the Telemetry System. The DSKY's provide display data to the Telemetry System that indicates operational conditions of the Computer Subsystem. This information is displayed on ground based equipment.

5-2.2 COMPUTER SUBSYSTEM OPERATION. The Computer Subsystem (figure 5-2) consists of eight functional areas: the Timer, Sequence Generator, Central Processor, Input and Output sections, Priority Control, Memory, Power, and the DSKY's. The following general functional theory of the

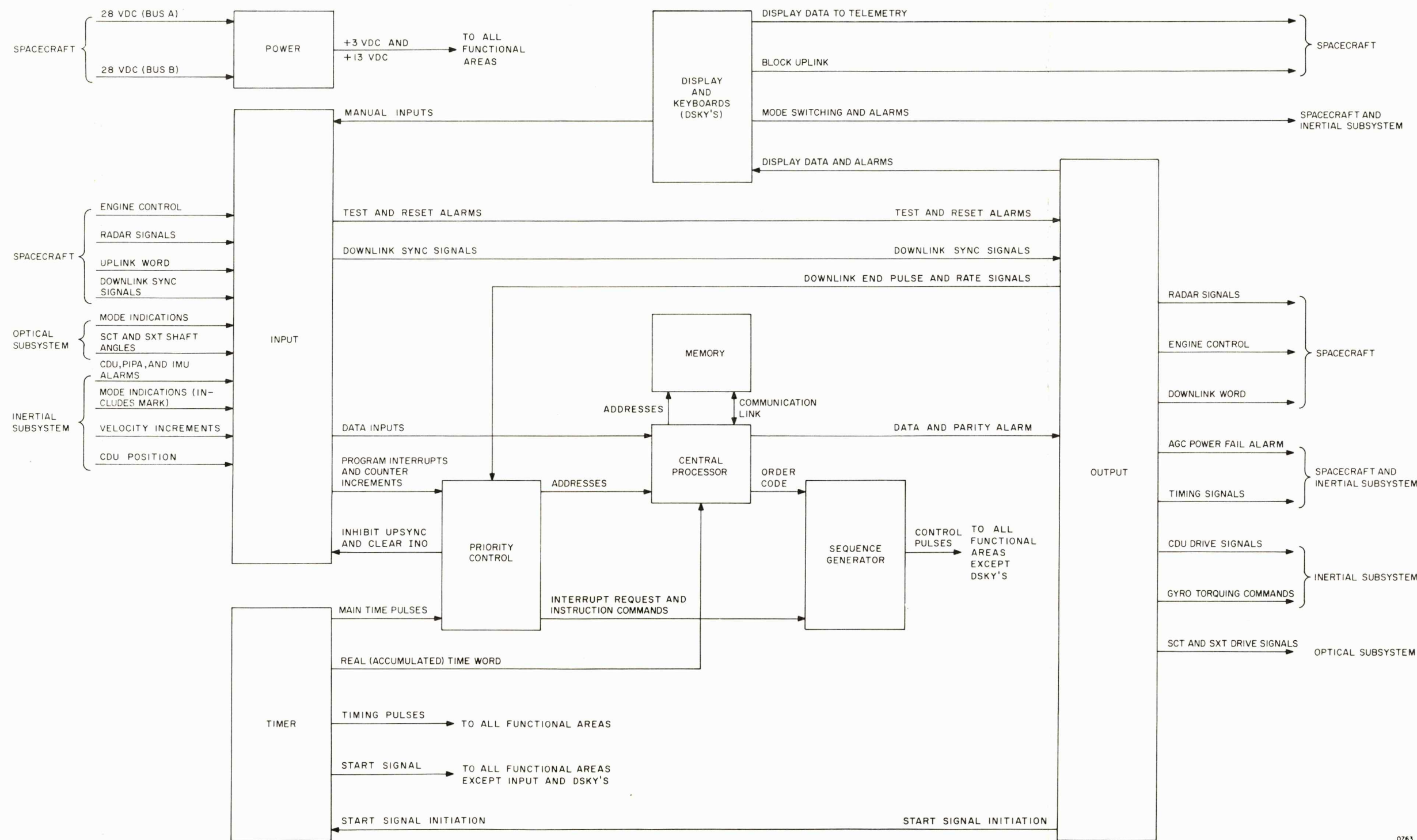


Figure 5-2. Computer Subsystem, Block Diagram

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Computer Subsystem involves data flow and operations within these areas; discussions on the individual areas are presented later.

The Input section, consisting of interface circuits and input registers, accepts all inputs to the AGC from the DSKY's, Spacecraft, Optical Subsystem, and Inertial Subsystem. Manual inputs from the DSKY's include the keycodes which allow information to be read out and displayed or loaded into the AGC and initiate certain program operations. Other manual inputs include an uplink blocking signal and alarm test and reset signals. Uplink data can be prevented from entering the AGC by the blocking signal. The alarm test and reset signals are applied from the DSKY's through the Input section to the Output section.

Planned engine control inputs will indicate occurrences in the Spacecraft. These include thrust, possible abort, and an indication that the Spacecraft is under manual control. Planned inputs from the rendezvous and landing radars will include radar power on, failure indications of either radar, lock-on conditions, and pertinent data which is to be applied to the Central Processor. The uplink word from the Spacecraft Telemetry System is fed to the Central Processor to allow ground control operation and checkout of the AGC during flight. The downlink sync signals also originate in the Spacecraft Telemetry System. These signals are applied through the Input section to the Output section to synchronize transmission of the downlink words.

The Optical Subsystem provides mode indications and data inputs representing scanning telescope (SCT) and sextant (SXT) shaft angles. The data inputs from the Input section are applied to the Central Processor and are used in the solution of guidance equations.

Velocity increments, sensed by the pulse integrating pendulous accelerometers (PIPA's) in the Inertial Subsystem, are used also in the solution of the guidance equations and are fed to Priority Control in the form of counter increments. The CDU position input indicates the angles that the CDU assumes as a result of commands from the AGC during thrust sequences. Mode indications include manual or automatic control exerted by the AGC on the Inertial Subsystem. The various modes involve alignment, zeroing, etc and are each indicated as individual bit inputs to the input registers within the Input section. Failure of the IMU, the CDU, or any one of the PIPA's causes a program interrupt input to Priority Control. Priority Control then causes the AGC to perform an associated interrupt program.

The main function of the AGC is to execute the programs stored in Memory. Programs are written in a machine language expressed in basic instruc-

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tions. A basic instruction contains an operation (order) code and a relevant address. The order code defines the operation to be performed and the relevant address selects the data that is to be used. Data flow is controlled by the Sequence Generator. An order code is entered into the Sequence Generator which then produces a specific sequence of control pulses. The instructions are usually stored in consecutive memory locations to specify the sequence in which instructions are to be executed. The location of the instruction to be executed next is defined by adding the quantity one to the address of an instruction presently being executed. Execution of an instruction is complete when the order code of the next instruction is transferred to the Sequence Generator and the relevant address is in the Central Processor.

Priority Control determines the priority of program interrupt requests and counter increment requests. Program interrupt requests include signals from the Input section, the downlink end pulse from the Output section, and signals from the Sequence Generator. Counter increments include signals from the Input section, main time pulses from the Timer, and rate signals from the Output section. During program interrupt requests, Priority Control produces an interrupt request signal which is sent to the Sequence Generator. This signal causes the execution of an instruction that transfers sufficient information from the Central Processor to Memory to permit later resumption of the interrupted program. In addition, control pulses transfer the interrupt program address in Priority Control to the Central Processor and then to Memory. As a result, the first basic instruction word of the interrupt program is entered into the Central Processor from Memory, and execution of the interrupt program is begun. The interrupt program transfers AGC control to an interrupting program. The last instruction of each interrupting program returns the information stored in Memory at the time of interruption.

Counter increment requests are processed by Priority Control for the counters in Memory which contain data pertaining to the Spacecraft used in the solution of guidance and navigation problems. This data includes real (accumulated) time, acceleration, and position information; all are continuously updated as new data becomes available. The contents of the counters are changed through an incrementing process which is implemented by Priority Control. Each counter increment request to Priority Control produces a counter address and an instruction command. The instruction command is sent to the Sequence Generator to initiate the proper instruction. The control pulses produced by the Sequence Generator transfer the counter address through the Central Processor to Memory. In addition, the control pulses enter the contents of the addressed counter into the Central Processor for

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incrementing. After the incrementing operation, the control pulses transfer the new data in the Central Processor back to its assigned storage location in Memory via the communication link.

Continuous drive pulses, originating as timing pulses in the Timer, are gated in the Output section. The resulting continuous drive pulses are sent to the Spacecraft and are used as timing signals, discrete carrier signals, and control signals. The rate signals, which are bursts of drive pulses, originate in the Output section and are sent to the gyros, CDU's, sextant, and tracker. Rate signals also control the attitude of the Spacecraft. The number of pulses in each burst and occurrence of each burst are controlled by a program function. The program function is dependent on incremental pulse feedback to Priority Control from the gyros, CDU's, sextant, and tracker. The destination, as well as the type of rate signal (incremental or decremental), is also selected by program function.

The downlink operation of the AGC is asynchronous to the Spacecraft Telemetry System. The Telemetry System supplies all of the timing signals necessary for the downlink operation. These signals include start, end, and bit sync pulses. The end pulse is also sent to the Priority Control from the Input section. The end pulse initiates a telemetry interrupt program. An interrupting program is then executed which provides more data for the downlink operation. Downlink data is sent to the Output section from the Central Processor. Downlink operation is performed within the AGC by the downlink converter.

With a DSKY keyboard, the astronaut can load information into the AGC, retrieve and display information contained in the AGC, and initiate any program function stored in Memory. The Computer Subsystem contains two DSKY's. A keycode is assigned to each keyboard pushbutton. When a pushbutton on either DSKY is depressed, keycodes are produced and sent to the Input section. The same keycodes are also sent to Priority Control where they produce an interrupt request signal and the address of an interrupt program stored in Memory. The address is supplied to the Central Processor, and the interrupt request signal is sent to the Sequence Generator. The interrupt request initiates an instruction for interrupting the program in progress and the interrupt program stored in Memory is executed. An interrupting program is then executed which transfers the keycodes, temporarily stored in the Input section, to the Central Processor, where they are decoded and processed. A number of keycodes are required for a basic instruction word, an address, or a data word. The interrupting program also converts DSKY information to a coded display format. The coded display information is

transferred from the Central Processor to the Output section for storage. The information is then sent to the display portion of the DSKY's, which indicates to the astronaut that the keycodes were received, decoded, and processed properly by the AGC.

The AGC power circuits receive +28 volts dc from spacecraft fuel cells on two buses. Two voltage outputs, +3 and +13 volts, are generated for all functional areas. The +13 voltage output and the +28 source voltage energize power supplies in the DSKY's.

5-3 FUNCTIONAL DESCRIPTIONS

5-3.1 TIMER. The Timer (figure 5-3) generates timing pulses required for AGC operation, timing pulses for the Spacecraft and Inertial Subsystem, and start and stop signals. The Timer consists of a clock countdown circuit, two scalers, a time pulse generator, and start-stop logic. The source frequency for the Timer is generated by a 2.048 megacycle oscillator.

The clock countdown circuit consists of two binary dividers and a ring counter. The first binary divider divides the source frequency by two to produce 1.024 megacycle timing pulses, the master clock frequency. This divider also receives two stop signals from the start-stop logic. If either stop signal A or B is present, timing pulses from the divider to the time pulse generator are inhibited and AGC operation is stopped. The second binary divider and the ring counter divide the 1.024 megacycle timing pulses to produce 512 kilocycle and 102.4 kilocycle timing pulses, respectively. The 102.4 kilocycle timing pulses from the clock countdown circuit drive scaler A.

Scaler A contains 17 identical binary divider stages and generates timing pulses at various rates between 51.2 kilocycles and 0.78125 cycles per second. The output from the last stage in scaler A, 0.78125 cps timing pulses, drives scaler B.

Scaler B contains 16 binary divider stages and is similar to scaler A except that each stage in scaler B can be read out, and the resultant real time word is sent to the Central Processor. The last stage indicates time intervals of 23.3 hours.

The time pulse generator is driven by 1.024 megacycle timing pulses received from the clock countdown circuit. These timing pulses step a Gray code counter. The Gray code counter outputs (A, B, C, and D) drive a de-

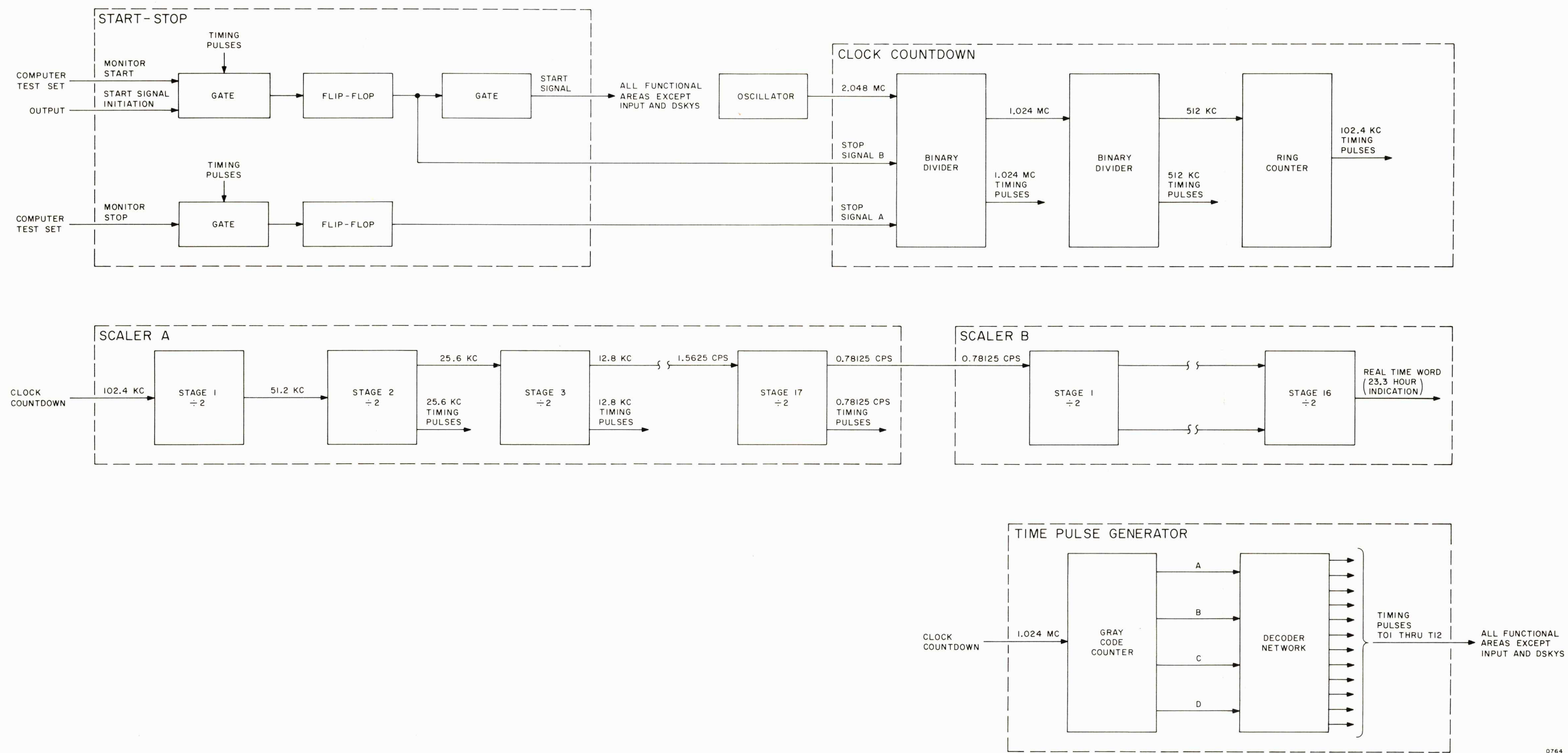


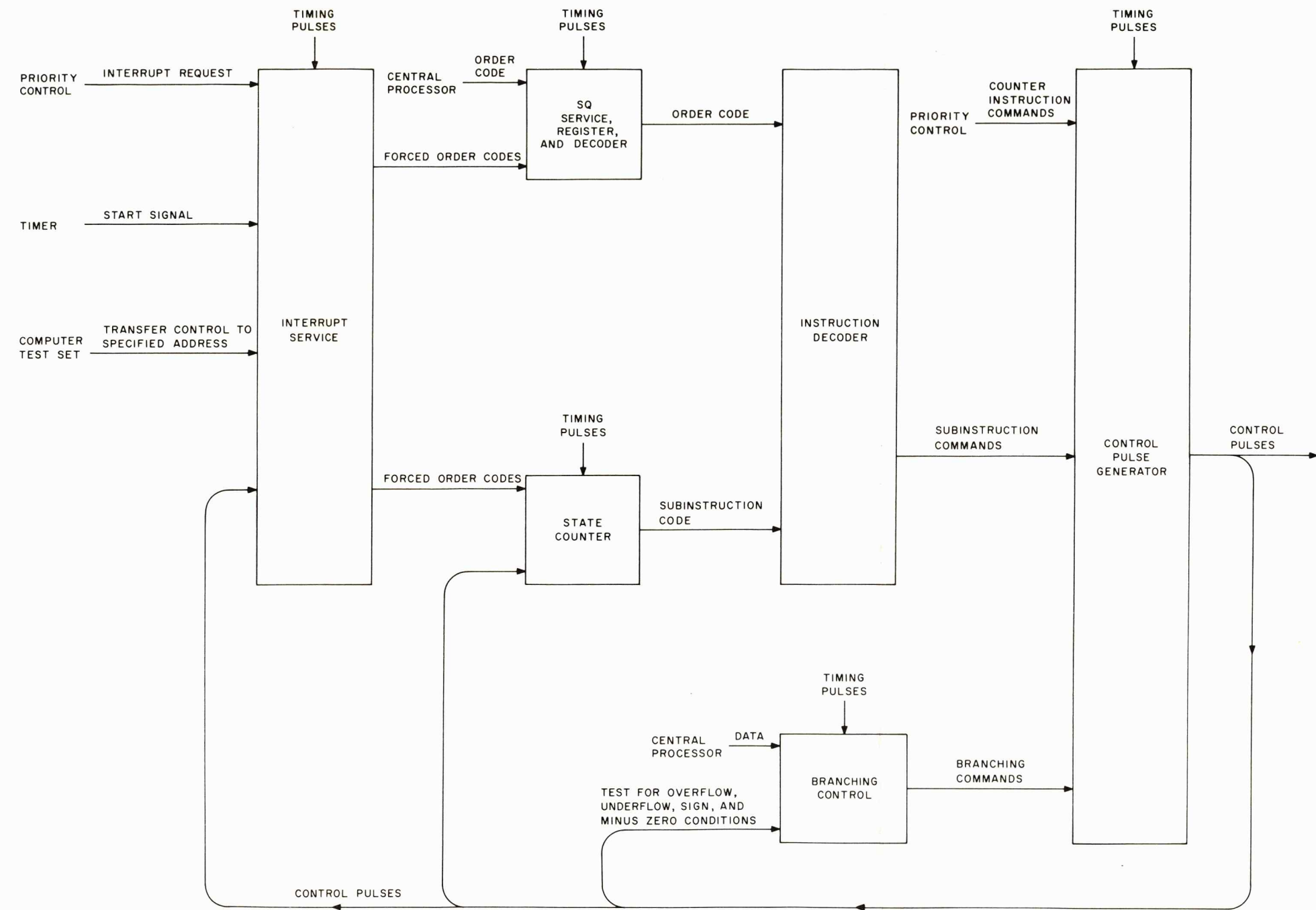
Figure 5-3. Timer, Functional Diagram

coder network which provides timing pulse outputs T01 through T12. These timing pulses, generated for use throughout the AGC, define a 12-action cycle which is referred to as a memory cycle time within the AGC.

The start-stop logic generates stop signals A and B and a start signal. Either stop signal, applied through the first binary divider in the clock count-down circuit, inhibits the time pulse generator at the end of a memory cycle time. This is accomplished so that AGC operation begins at the start of a memory cycle time when the start signal sets initial conditions. The start signal and stop signal A are generated when either a monitor start signal is received from the Computer Test Set (CTS) or a start signal initiation is received from the AGC Output section. Monitor stop from the CTS produces stop signal B and AGC operation is inhibited until the CTS removes monitor stop. The AGC start signal initiation is produced when AGC alarms that require a fresh start are detected.

5-3.2 SEQUENCE GENERATOR. The Sequence Generator (figure 5-4) consists of an interrupt service; SQ register, service, and decoder; state counter; instruction decoder; branching control; and a control pulse generator. The Sequence Generator permits 21 different logical operations, called machine instructions, to be performed on data within the AGC. A machine instruction is executed by control pulses from the Sequence Generator. The control pulses regulate the flow of data through all functional areas except the DSKY's. Machine instructions require from 1 to 16 memory cycle times for execution and contain as many subinstructions as there are distinct operations in the instruction. For example, the multiply instruction requires 8 memory cycle times to be executed but contains only three distinct operations. The first and last operations are executed once; the second operation is executed six times.

The AGC contains 28 different operations; each requires one memory cycle time for execution. A subinstruction command is produced by the Sequence Generator or an instruction command is sent to the Sequence Generator for each of the 28 operations. These commands cause control pulses which execute the associated operation to be produced. Twenty-two of the command signals are produced by the instruction decoder in the Sequence Generator. The six instruction commands are received from Priority Control. Each of the 22 subinstruction commands (representing 15 machine instructions) has an order code and a subinstruction code. The 15 order codes identify the instruction which is being executed. There are 4 subinstruction codes which identify the subinstruction to be executed. For example, the multiply instruction has one order code and three subinstruction codes. An



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Figure 5-4. Sequence Generator, Functional Diagram

instruction with two subinstructions has one order code and two subinstruction codes. Twelve of the order codes are under program control and are produced in the Central Processor. Three order codes, called involuntary or forced order codes, are produced in the interrupt service by the start signal from the Timer, the interrupt request from the Priority Control, and the transfer-control-to-specified-address signal from the CTS. The order codes are stored by the SQ service, register, and decoder during the entire execution of a machine instruction. The subinstruction codes are produced in the state counter. When the Sequence Generator is under program control, the state counter is reset and advanced in a logical sequence by control pulses to produce the subinstruction codes. Otherwise, the counter is forced into a predetermined state by the forced order code signals to produce subinstruction codes.

One or more control pulses can be generated every microsecond. The control pulse or pulses generated are called an action. During an action, data flows between two or more logic elements or the state of any single logic element, such as a register, is changed. Examples of actions are clearing a register of its contents by a single control pulse or transferring data from one register to another by read and write control pulses. The AGC is designed such that 12 actions may occur within one memory cycle time. Each action time is regulated by a timing pulse. Eleven timing pulses (T01 through T11) from the Timer are applied to the control pulse generator for the execution of subinstructions. The 12th timing pulse (T12) is used to produce the next order code or subinstruction code.

A subinstruction can be modified by branch commands from the branching control. A branch in a subinstruction means that one out of as many as four possible actions may occur during a given time pulse period. A subinstruction may contain more than one branch. The action that occurs in a branch is determined during execution of the subinstruction by tests made by the branching control on data brought into the Sequence Generator from the Central Processor. The data can be tested for sign, overflow, underflow, plus zero, and minus zero. The use of branching functions by program is unlimited. Branching functions are used to determine if a computation is complete, to adjust the execution of programs dealing with overflow or underflow quantities, and to determine if certain operations are occurring at the proper rate.

5-3.3 CENTRAL PROCESSOR. The Central Processor (figure 5-5) performs all arithmetic operations and other data manipulations in the AGC. The Central Processor consists of the flip-flop registers, write amplifiers, memory buffer register, and parity block.

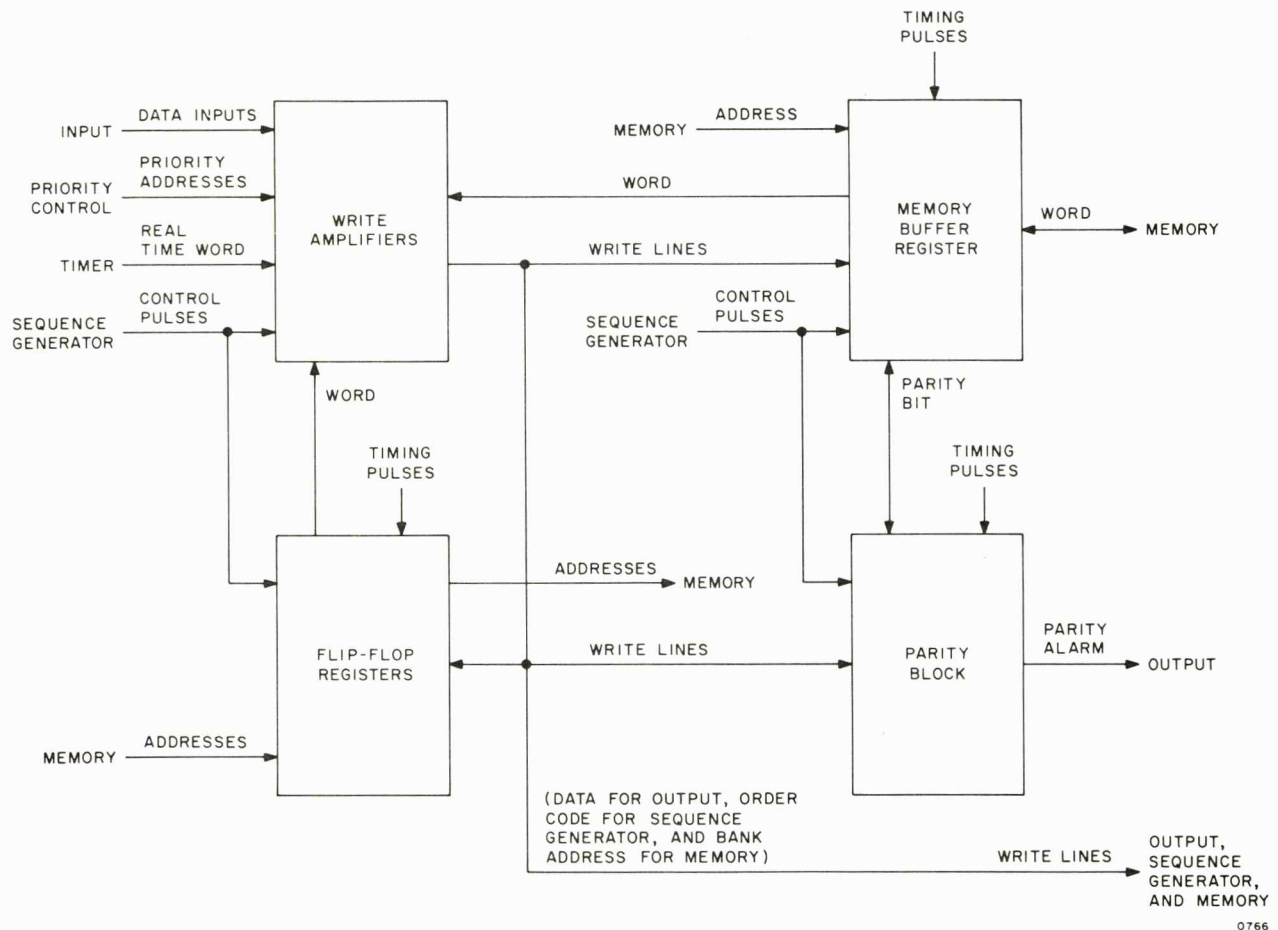


Figure 5-5. Central Processor, Functional Diagram

Data and word flow within the Central Processor is through the write amplifiers, the outputs of which are designated as write lines. Words read-out from Memory (through the memory buffer register) are routed to specific destinations through the write amplifiers. Likewise, information that is to be written into Memory is placed on the write lines and applied through the memory buffer register.

Primarily, information on the write lines consists of words which are transferred between the flip-flop registers. This is accomplished by reading the output of one register through the write amplifiers onto the write lines, and writing this same information into another register. Information placed on the write lines is available not only to flip-flop registers but also to other

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functional areas. Control pulses from the Sequence Generator determine the destination(s) of the information placed on the write lines. Certain inputs are placed directly on the write lines, not from a flip-flop register. These inputs include data inputs used during the execution of programs, interrupt program addresses, and the real time word which updates the main time counter in Memory.

The memory buffer register buffers all information read out of Memory and all information written into erasable memory. Words read out of Memory are deposited directly in the buffer register. On command of the control pulses from the Sequence Generator, the word is read out of the buffer register and placed on the write lines. Simultaneously, the word is entered through the write amplifiers into the parity block for a parity check and into another register for further processing. All words in Memory contain an odd number of binary ONE's. A parity alarm registers if an even number of binary ONE's are detected in the memory buffer word after a word is received from Memory. A word being written into erasable memory (only erasable can be written into) is placed on the write lines, entered into the memory buffer register, and simultaneously entered into the parity block, where a parity bit for the word is generated. The word is then read out of the buffer register directly into Memory.

The memory buffer register also functions during certain programs to shift or cycle information as required. This is accomplished by entering specific memory addresses into the buffer circuits. Information then entered into the buffer register is shifted or cycled as dictated by the memory address.

The parity block, as indicated previously, checks for correct parity on words read out of fixed and erasable memory and controls a parity bit for all words being written into erasable memory. A binary ONE can be written into the parity bit so that each word has correct parity when in Memory. The parity bit is never placed on the write lines. During read-out from Memory, the parity bit of the word is fed directly to the parity block. During write-in, the generated parity bit is fed directly to the buffer register.

There are eight flip-flop registers in the Central Processor, each consisting of 16 bit positions. All operations involving the flip-flop registers, whether arithmetic functions or manipulation of data, are accomplished by the control pulses from the Sequence Generator. These control pulses, in conjunction with the timing pulse inputs, control data flow. The flow of data between registers is accomplished by enabling read gates of the register

containing data and write gates of the other register into which the data is to be inserted. Data flow between certain registers can be controlled also by specific memory addresses. The addresses are determined under program control.

5-3.4 INPUT-OUTPUT. Input-Output consists of the input-output registers (including the interface circuits), downlink converter, alarm circuits, and rate control circuits. Information is transferred between the Computer Subsystem and the other spacecraft systems through the Input-Output.

5-3.4.1 Input-Output Registers. The input registers (figure 5-6) are flip-flop registers that are identical to the flip-flop registers of the Central Processor. Each register consists of 16 bit positions with clear and read service. There is no write service for the input registers. The input data from the interface circuits is applied directly to each flip-flop. The read and clear control signals are generated under program control by associated memory addresses and control pulses through the Central Processor from the Sequence Generator. Priority Control clears the IN0 register of previous inputs when the mark signal or keycodes are received for storage in the IN0 register.

The discrete bit inputs consist of mode indication signals, alarm conditions, etc. Manual inputs from the DSKY's, such as the keycodes and discrete bit inputs from the Spacecraft, Inertial Subsystem, and Optical Subsystem, are entered into the input registers from the input interface. These data inputs are subsequently transferred to the write amplifiers in the Central Processor. Positive and negative incremental inputs are applied directly to Priority Control from the input interface. These inputs include uplink information, velocity increments, etc and are subsequently transferred to associated counter locations in erasable memory. Other inputs applied directly from the input interface are the downlink sync signals for the downlink converter and test and reset alarm signals from the DSKY's for the alarm circuits.

The output registers are also functionally identical to the flip-flop registers of the Central Processor. Each register, with one exception, has associated write, clear, and read pulses which are enabled under program control by specific memory addresses coincident with control pulses from the Sequence Generator. The output register associated with the downlink converter does not have associated read pulses. The output registers receive data words from the Central Processor, supply data inputs to the Central Processor, and supply signals through the output interface to the DSKY's, the rate control circuits, and the downlink converter.

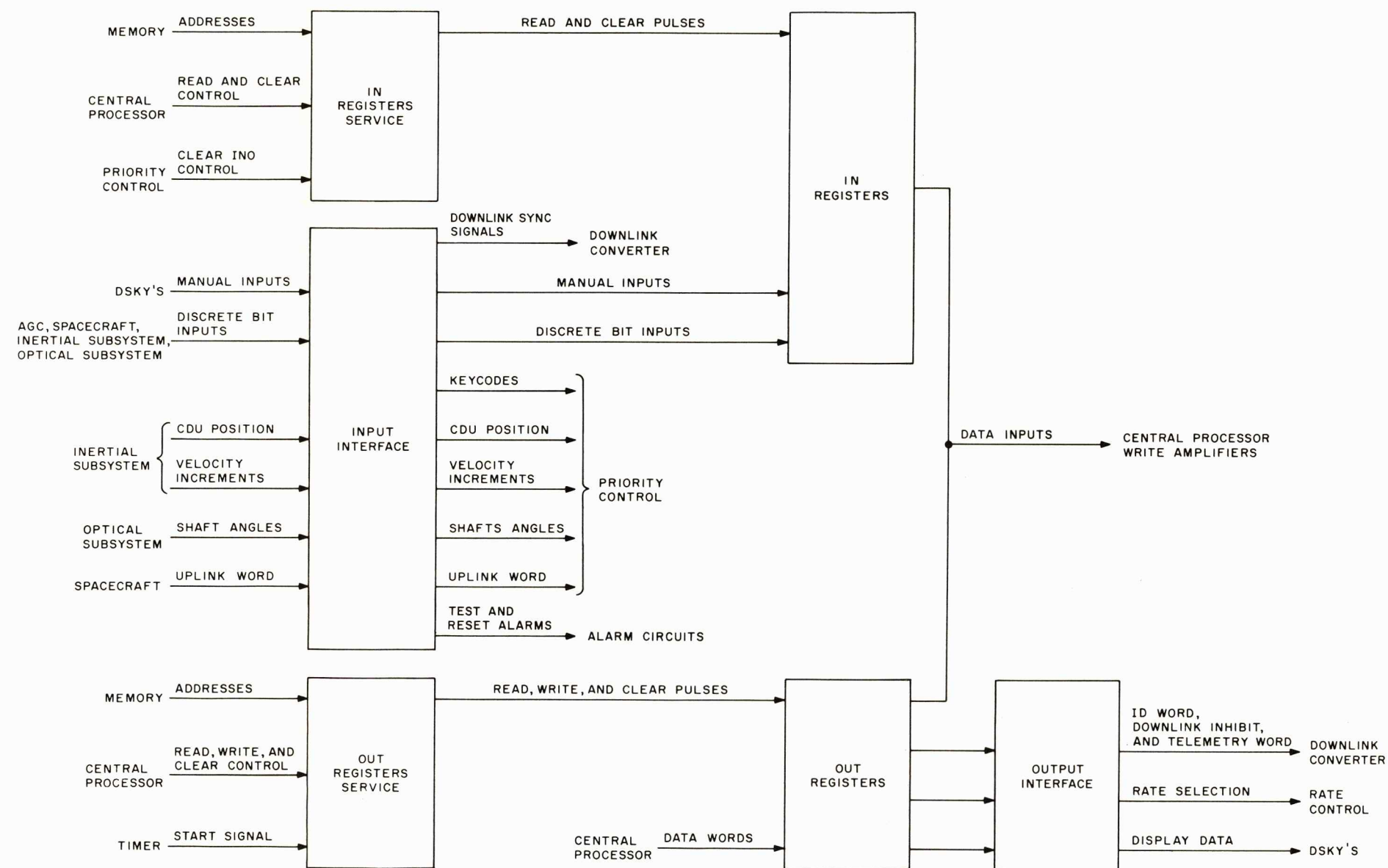
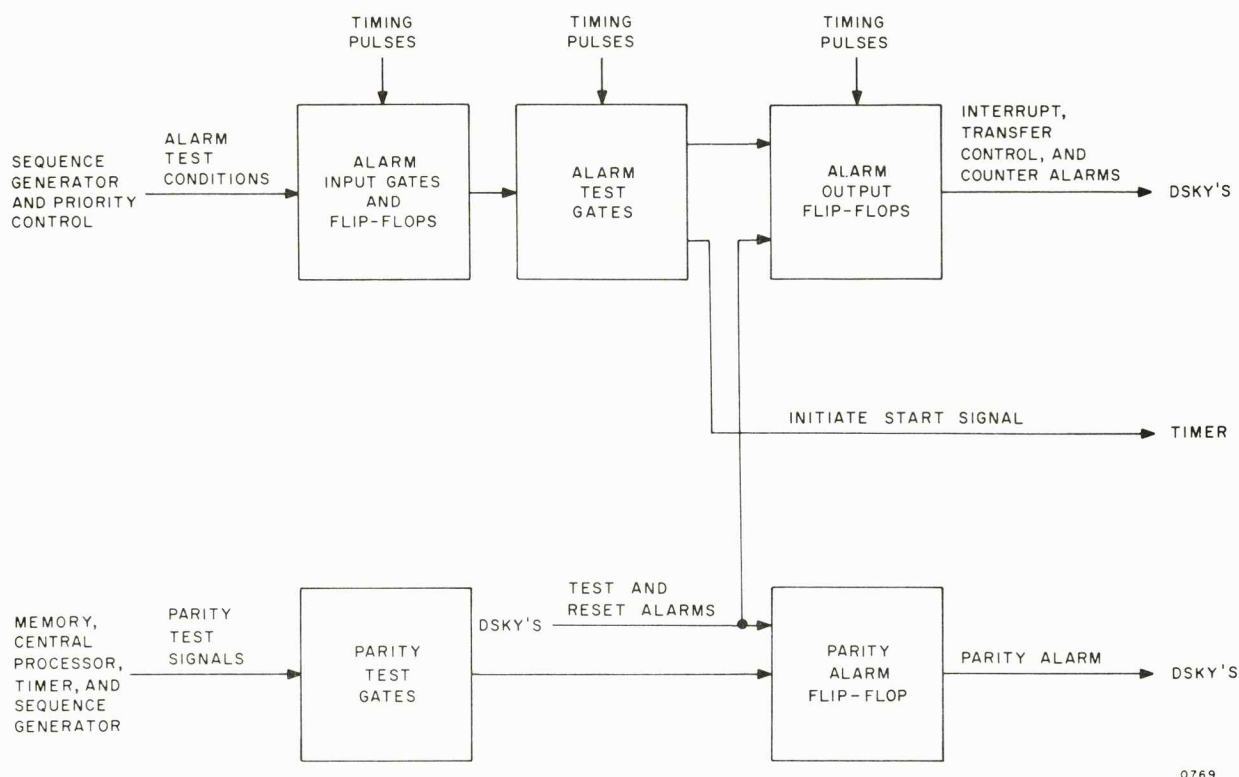


Figure 5-6. Input-Output Registers, Functional Diagram



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Figure 5-7. Alarm Circuits, Functional Diagram

5-3.4.2 Alarm Circuits. The alarm circuits (figure 5-7) provide outputs to the DSKY's which are indicative of conditions in the AGC. These alarms are the interrupt, transfer control, counter, parity, and scaler fail. Any one of the alarms, with the exception of the scaler fail alarm, produces the initiate start signal which is sent to the Timer. A start signal from the Timer then restarts the AGC. Three additional alarms; the program, telemetry, and check fail alarms, are detected by program operations.

The interrupt, transfer control, and counter alarms are dependent on specific occurrences within a given period of time. For example, an interrupt alarm is generated if an interrupt has been in progress longer than a predetermined period or if an interrupt has not occurred during a specific period of time. A transfer control alarm is generated if transfer control instructions have been continuously in progress longer than a given period or if no transfer control instruction is executed within a given period. A counter

alarm is generated if counter increment operations (counter priority control) have been continuously in progress longer than a given period or if a counter increment operation is requested and does not take place at the proper time. A parity alarm occurs if a word has been incorrectly read out of Memory and indicates a flip-flop or core malfunction. The scaler fail alarm circuit monitors the output of one stage of scaler A in the Timer. Failure of the scaler is indicated by loss of this signal, and the alarm subsequently appears on a DSKY display. Alarm output and DSKY display circuits are checked for proper operation by a test alarm signal applied from a DSKY. This causes the corresponding alarm displays to illuminate.

5-3.4.3 Rate Control. The rate control circuits (figure 5-8) provide drive pulses to the Spacecraft, Inertial Subsystem, and Optical Subsystem. Counter increment pulses are sent to Priority Control so that rate counter counters will be incremented. The drive pulses are divided into two basic categories: those which are generated under program control by the content of specific bit positions of register OUT 2, and those which are generated continuously as a function of timer outputs. The bit positions of register OUT 2 are divided into three groups. Each group is associated with a rate counter in erasable memory, which results in three groups of rate signals. Initially, a rate counter is preset to some value by a program and is then incremented until overflow occurs. Drive pulses are gated out until overflow occurs. The bit positions associated with the rate counter are then cleared and the drive pulses cease.

The gating rate for the rate control signals is 3200 pps established by inputs from the Timer. The rate 1 control logic generates drive pulses for the gyros and the CDU in the Inertial Subsystem and supplies counter increments for the associated rate counter. Two bit positions of OUT 2 are used to differentiate to which unit the rate 1 drive signals are to be sent; two other bit positions differentiate whether positive or negative incremental pulses are to be sent. The rate 2 control logic generates drive pulses for the spacecraft engines and the Optical Subsystem, and supplies counter increments for the associated rate counter. The rate 3 control logic generates drive pulses for the Rendezvous and LEM radars and supplies counter increments for the associated rate counter. At present, the drive pulses controlled by the rate 3 control logic are not used. However, the facility exists for generating drive pulses to these units.

Continuous drive pulses, generated as a function of inputs from the Timer, are supplied to the Spacecraft and the Inertial Subsystem. The engine control signals, supplied to the spacecraft, are selected by program and are continuous outputs until terminated by program control.

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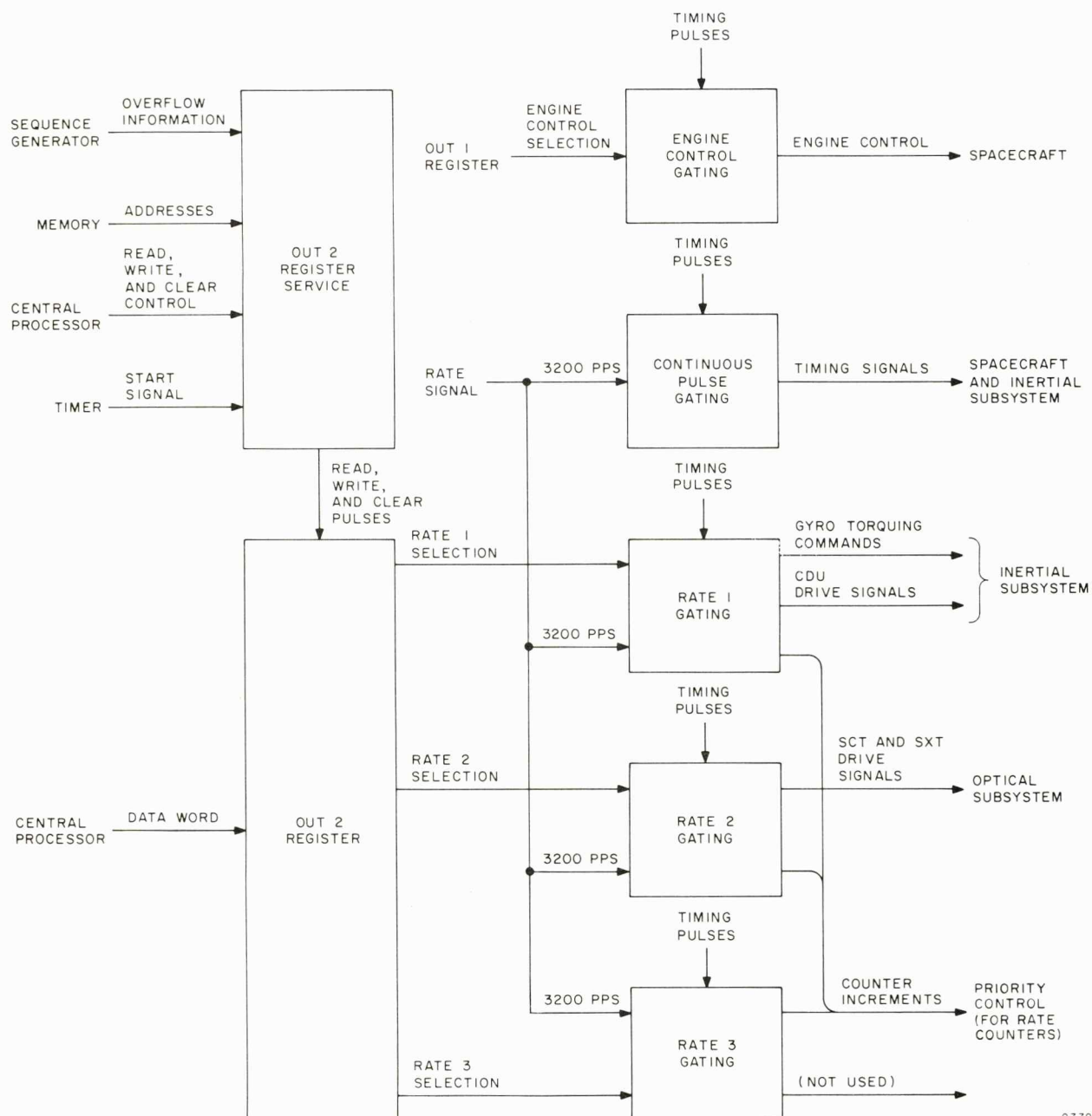
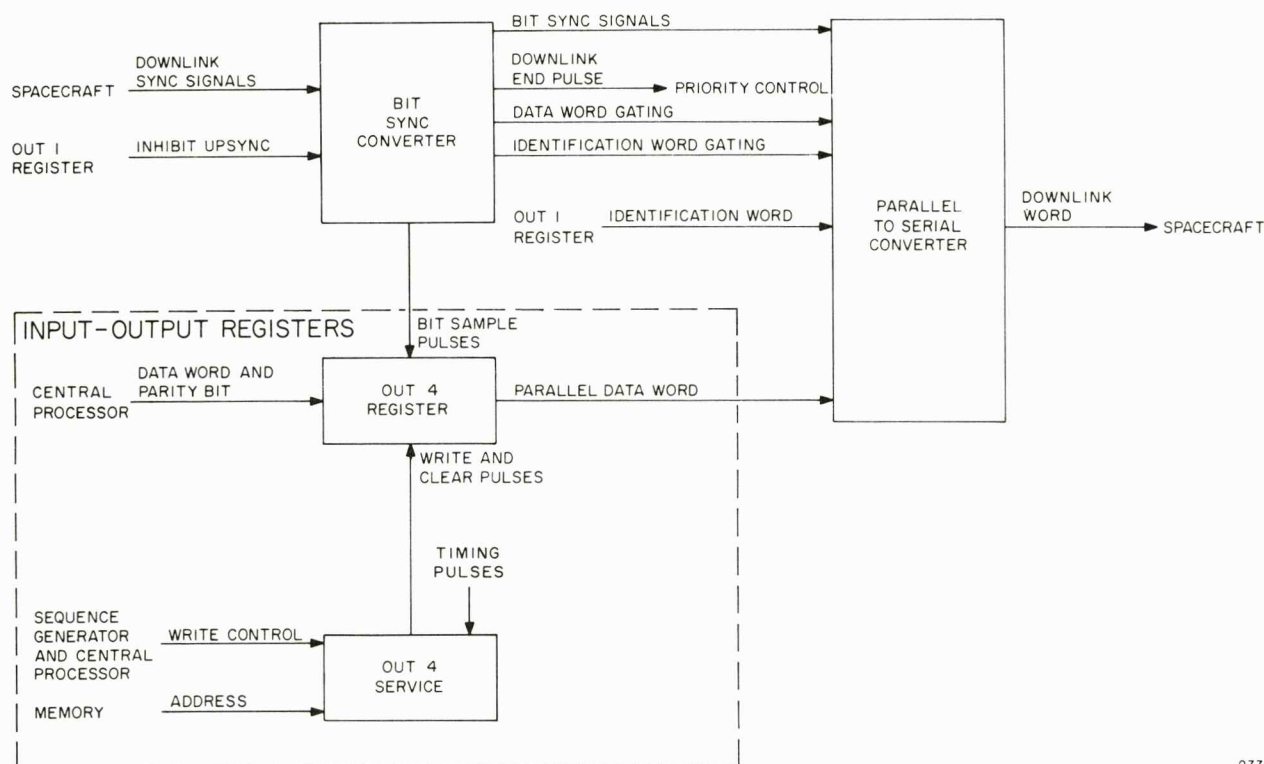


Figure 5-8. Rate Control, Functional Diagram

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Figure 5-9. Downlink Converter, Functional Diagram

5-3.4.4 Downlink Converter. The downlink converter (figure 5-9) transforms parallel AGC data, selected by program control, into serial data for transmission by the Spacecraft Telemetry System. Register OUT 4 stores the data to be transmitted.

Data to be transmitted downlink is written into the OUT 4 register under program control. The register bit positions are then enabled (strobed) one at a time by the bit sample pulses causing the parallel word to be read through the parallel to serial converter to the Telemetry System. The downlink converter operation is synchronized by the downlink sync signals from the Spacecraft. The downlink sync signals for one transmission consist of a start pulse, 40 bit sync pulses, and a downlink end pulse. During a transmission 32 bit sync pulses cause the bit sync converter and parallel-to-serial converter to transmit the contents of register OUT 4 twice. The remaining 8 bit sync pulses cause all logical ZERO's or all logical ONE's to be transmitted, depending on the identification word bit in the OUT 1 register. The

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downlink end pulse then initiates program operation to reload the OUT 4 register. Downlink converter operation can be inhibited by an inhibit upsync signal from the OUT 1 register which is controlled by a program operation.

5-3.5 PRIORITY CONTROL. There are two types of priority control operations within the AGC; counter and interrupt. Counter priority control updates counters in erasable memory and during test functions implements display and load requests from the CTS. Interrupt priority control transfers AGC control to one of six interrupt programs that initiate programs which deal with conditions such as alarms or keycode inputs from the DSKY's.

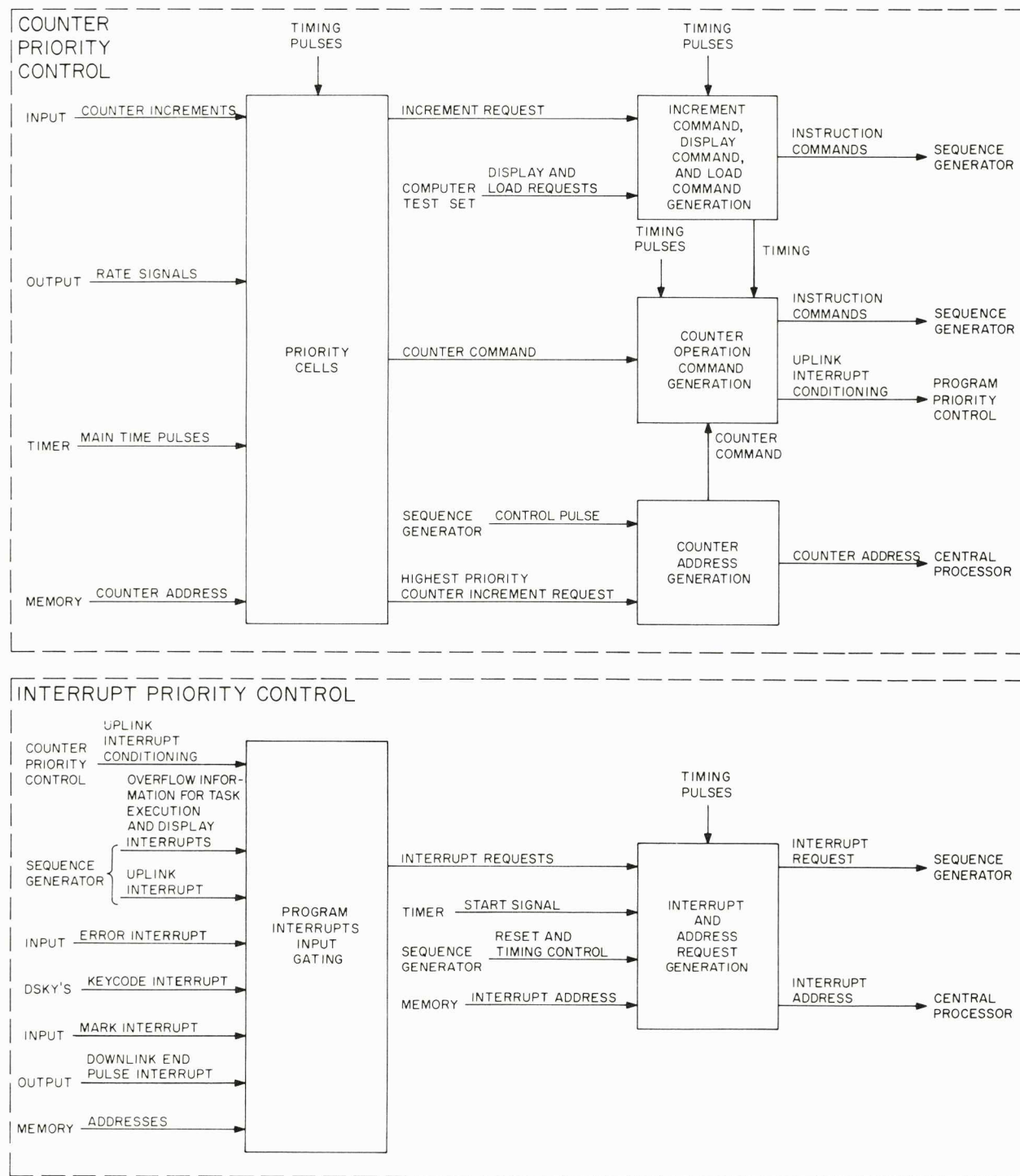
5-3.5.1 Counter Priority Control. Counter priority control (figure 5-10) updates applicable counters when counter increment requests are received through the Input section, when main time pulses are received from the Timer, and when rate signals are received from the Output section. Only one counter is updated at a time. However, pulses for several counters may be received simultaneously. When this occurs the counters are updated in order of preassigned priority. The counter increments are associated with elements such as the PIPA's, CDU's, and timing. The main time pulses are associated with two counters that store real (accumulated) time. To time program operations, a counter is set to a specific value and then incremented. Rate signal inputs from the rate control circuits in the Output section initiate these counter increment operations. When the counter reaches capacity, overflow occurs and indicates that the required time interval has passed. Counter priority control determines the type of counter instruction command inputs and produces the address of the counter to be updated. The Sequence Generator receives these commands and implements increment, decrement, shift, or shift and add one operations within the Central Processor.

When a display or load request is received from the CTS, counter priority control commands the Sequence Generator to execute a display or load instruction. The display instruction causes the contents of a CTS-addressed memory location to be displayed on the CTS. The load instruction allows the CTS to load data into a CTS-addressed location in Memory.

There are 20 priority cells in counter priority control. These cells receive input signals from the Input section, Output section, and Timer. A cell is set when it receives an input signal. Priority is tested to determine if this cell is the highest priority cell that is set. If so, an increment request is sent to the increment command, display command, and load command generation circuit. A counter increment request signal is also applied to the counter address generation circuit. Either the priority cells or the counter

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Figure 5-10. Priority Control, Functional Diagram

address generation circuit produces the applicable counter command signal for the counter operation command generation circuit. This counter command signal indicates increment, decrement, shift, or shift and add one operations. If there is no display or load request from the CTS, an instruction command signal which indicates that a counter increment operation must be performed is applied to the Sequence Generator. The Sequence Generator provides a control pulse which enables the counter address generation circuit and sends the applicable counter address to the Central Processor. The counter address enables the Central Processor to obtain the proper counter word from Memory in preparation for updating the word. Timing pulses then enable the counter operation command generation circuit, and the instruction command is applied to the Sequence Generator which implements the proper operation: increment, decrement, shift, or shift and add one. While a counter is being updated, the counter address, supplied from Memory to the priority cell, is used in conjunction with a timing pulse to reset the applicable priority cell. Counter priority control then processes the next highest priority cell that is set.

Display or load requests from the CTS inhibit counter operations until after the display or load instruction is accomplished. When the display request or the load request is applied to the Sequence Generator, the timing signal applied to the counter operation command generation circuit is inhibited. When the Sequence Generator receives the display or load instruction command, it inhibits the control pulse sent to the counter address generation circuit. Without this pulse the counter address cannot be transferred to the Central Processor. Timing pulses, in conjunction with internal signals, reset the increment command, display command, and load command generation circuit after the display or load instruction has been implemented.

5-3.5.2 Interrupt Priority Control. Interrupt priority control (figure 5-10) initiates transfers to the following interrupt programs: task execution, error, display, keyrpt, uplink, and telemetry. These interrupt programs are listed in the order of priority. Program interrupt inputs are applied to the program interrupt input gating circuit. This circuit stores all interrupt requests until they are processed and supplies available interrupt requests to the interrupt and address request generation circuit. Priorities are then tested, and the highest priority interrupt request is sent to the Sequence Generator. When the Sequence Generator can process the specified interrupt request, a timing control signal from the Sequence Generator enables the interrupt address which is then sent to the Central Processor. This interrupt address is the address of the first instruction of an interrupt program. The interrupt address, in conjunction with a reset signal from the Sequence Generator, resets

the interrupt request after the interrupt program has been initiated. Timing pulses are applied to enable the requests at the proper times. The timer start signal clears all requests that are present.

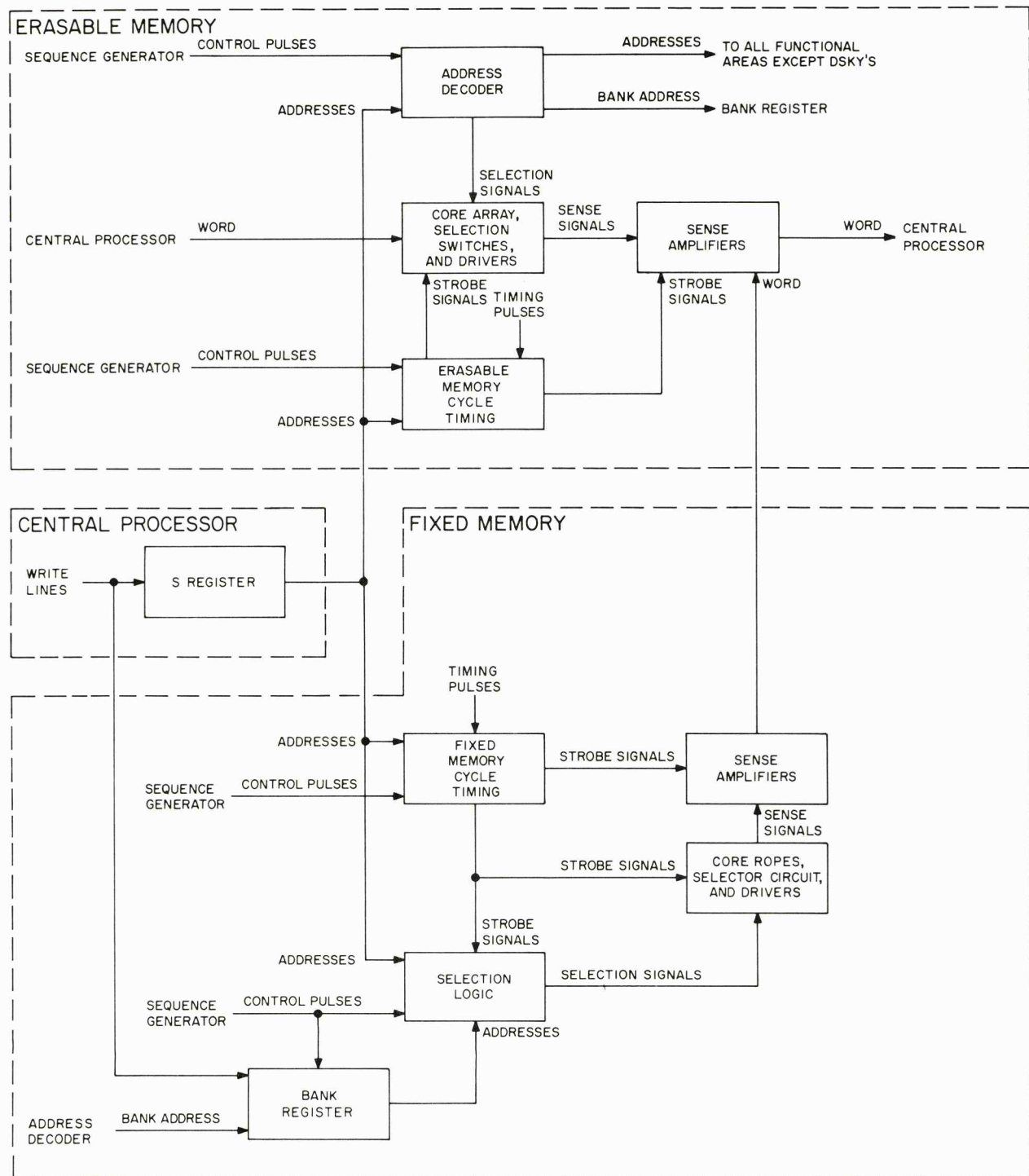
Task execution, display, and uplink interrupt requests are controlled by operations within counter priority control. Counters associated with the task execution and display interrupt programs are incremented until overflows are detected by the Sequence Generator. The counter operation command generation circuit within counter priority control produces an uplink interrupt conditioning signal when a complete uplink word has been received and stored in the uplink counter.

The addresses from Memory indicate if the task execution or display counter is being incremented when overflow occurs. The address of the uplink counter is required in conjunction with the uplink interrupt conditioning signal to specify an interrupt request for the uplink priority program. The error interrupt input occurs when engine control signals are received from the Spacecraft or when a CDU, PIPA, or IMU fail alarm is received from the Inertial Subsystem. (The engine control signals are not used at present.) The keycode and mark interrupt inputs both cause a keyrupt interrupt request. The keycode interrupt input occurs when any keys on the DSKY's are operated. The mark interrupt input from the Input section occurs when the mark signal is received from the Inertial Subsystem. The downlink end pulse interrupt input initiates a telemetry interrupt request. The downlink end pulse occurs after a complete downlink word has been sent to the Spacecraft Telemetry System.

5-3.6 MEMORY. Memory (figure 5-11) consists of an erasable memory and a fixed memory and has an effective capacity of 25,584 sixteen-bit words. Both memories contain magnetic-core storage elements. In erasable memory the storage elements form a core array; in fixed memory the storage elements form core ropes. Erasable memory is a coincident-current ferrite core array with a total capacity of 1,024 sixteen-bit words, although only 1,008 locations are used. Information stored in erasable memory can be altered or updated. Readout of erasable memory is destructive in that word locations are cleared when they are read. Fixed memory consists of six magnetic core rope modules, each with a capacity of 4,096 sixteen-bit words, with a total capacity of 24,576 sixteen-bit words. The words stored in fixed memory cannot be altered electrically. Fixed memory words are wired in and readout is nondestructive.

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Figure 5-11. Memory, Functional Diagram

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When a program is written, addresses are assigned to instructions to specify the sequence in which they are to be executed and blocks of addresses are reserved for data such as constants and tables. Information is put into fixed memory by particular wiring patterns through the magnetic cores. Information is put into assigned locations in erasable memory from the Computer Test Set, the DSKY's, uplink, or program control.

Both memories use a common address register in the Central Processor. When the address register, register S, contains an address pertaining to erasable memory, the erasable memory cycle timing is energized. Timing pulses sent to the erasable memory cycle timing then produce strobe signals for the write, read, and sense functions. The address decoder receives addresses from the S register and produces selection signals for the core array. The address decoder also sends addresses to the bank register and to all functional areas except the DSKY's. Before the selection signals are applied to the core array, they are modified by the selection switches. The selection switches perform a decoding function and permit information to be written into, or read from, the selected storage location. When a word is taken from a storage location in erasable memory, the location is cleared. This is destructive read out. The word, sometimes modified, is always put back into its storage location through the write process so that it may be used again. When information is being written into a storage location, the word comes from the memory buffer register in the Central Processor and is written into the selected location by the write drivers. When information is being read from a storage location, the information is strobed by the read driver outputs and applied to the sense amplifiers. The sense amplifiers are strobed also and the information is entered into the memory buffer register in the Central Processor. The buffer register receives information from both memories.

Fixed memory contains selection logic, timing circuits, and sense amplifiers, and has an additional address register, register bank. Fixed memory has two divisions; fixed-fixed and fixed-switchable. This additional address register is necessary to address locations in fixed-switchable memory. Only register S is required to address fixed-fixed memory. The S register addresses energize the fixed memory cycle timing when a location in fixed memory is addressed. The timing pulses sent to the fixed memory cycle timing produce the strobe signals for the read and sense functions. The selection logic receives addresses from the bank and S registers and produces selection signals for the core ropes. The bank register receives its contents from the Central Processor write lines when the register is addressed and

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the proper control pulses from the Sequence Generator are present. The content of a storage location in the core rope is strobed from the fixed memory sense amplifiers through a buffer stage in the erasable memory sense amplifiers and then entered into the memory buffer register.

5-3.7 POWER. Two switching-regulator power supplies (figure 5-12) furnish the voltage required for AGC operation. One power supply provides +3 volts and the other provides +13 volts. Both power supplies are energized by power received from fuel cells in the Spacecraft Power System on the A and B voltage buses. The input voltage is applied to a power switch and chopped at a variable duty cycle. The resulting signal is filtered to produce the required +3 and +13 output voltages. Functional operation of the +13 volt power supply is described and is typical of both power supplies.

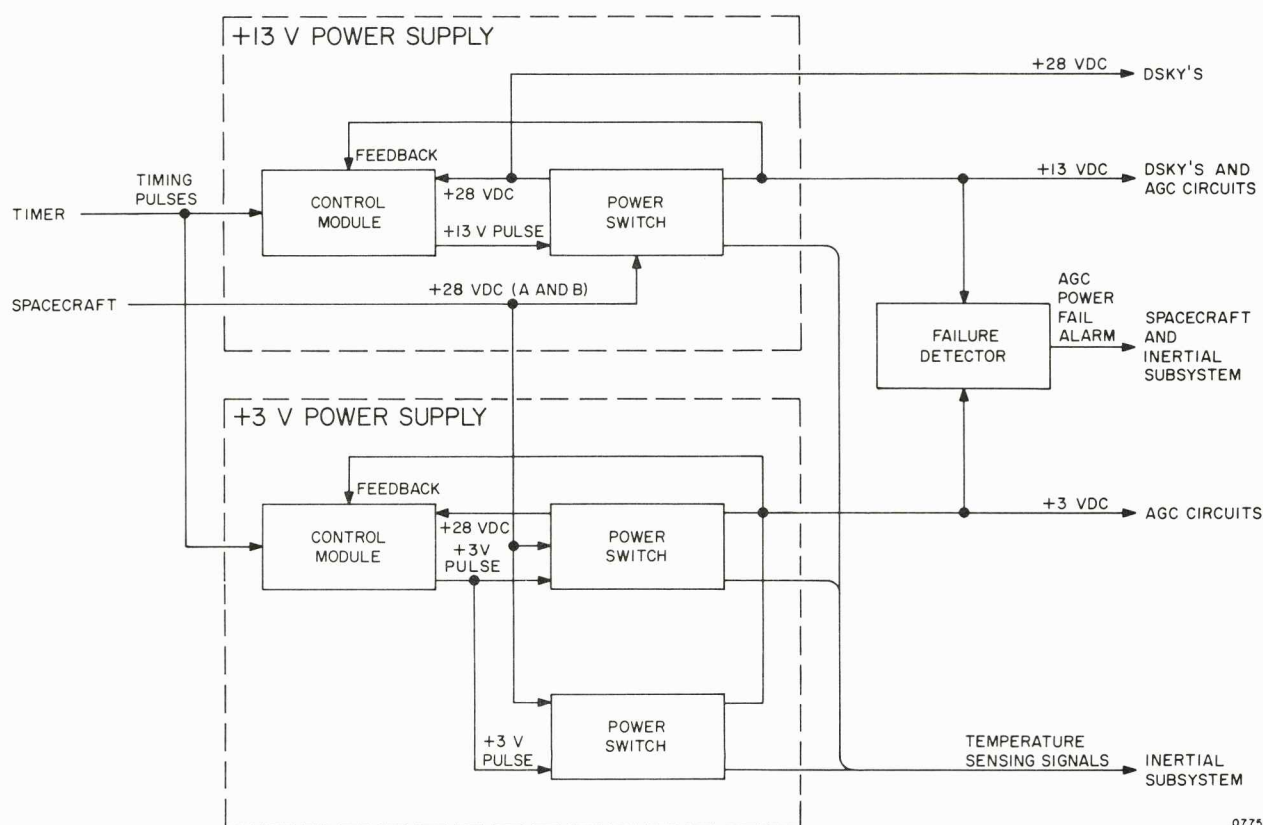


Figure 5-12. Power, Functional Diagram

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The power switch receives input voltage on both buses. Either voltage is supplied to the control module. This voltage and the +13 volt output energize the DSKY power supplies. The control module compares feedback from the power supply output with a reference voltage. A differential amplifier within the control module then detects any change in the output voltage from the reference voltage. The differential amplifier output and timing pulses from the Timer drive and sync a one-shot multivibrator in the control module. The differential amplifier output determines the multivibrator pulse width. The +13 volt pulse from the multivibrator is applied to the power switch. This pulse is increased in width to compensate for a decrease in output voltage and is decreased in width to compensate for a rise in output voltage. The power switch filters the control module pulse output to produce the desired dc voltage. Input filtering protects the Spacecraft Power System from wide load variations caused by the chopping action.

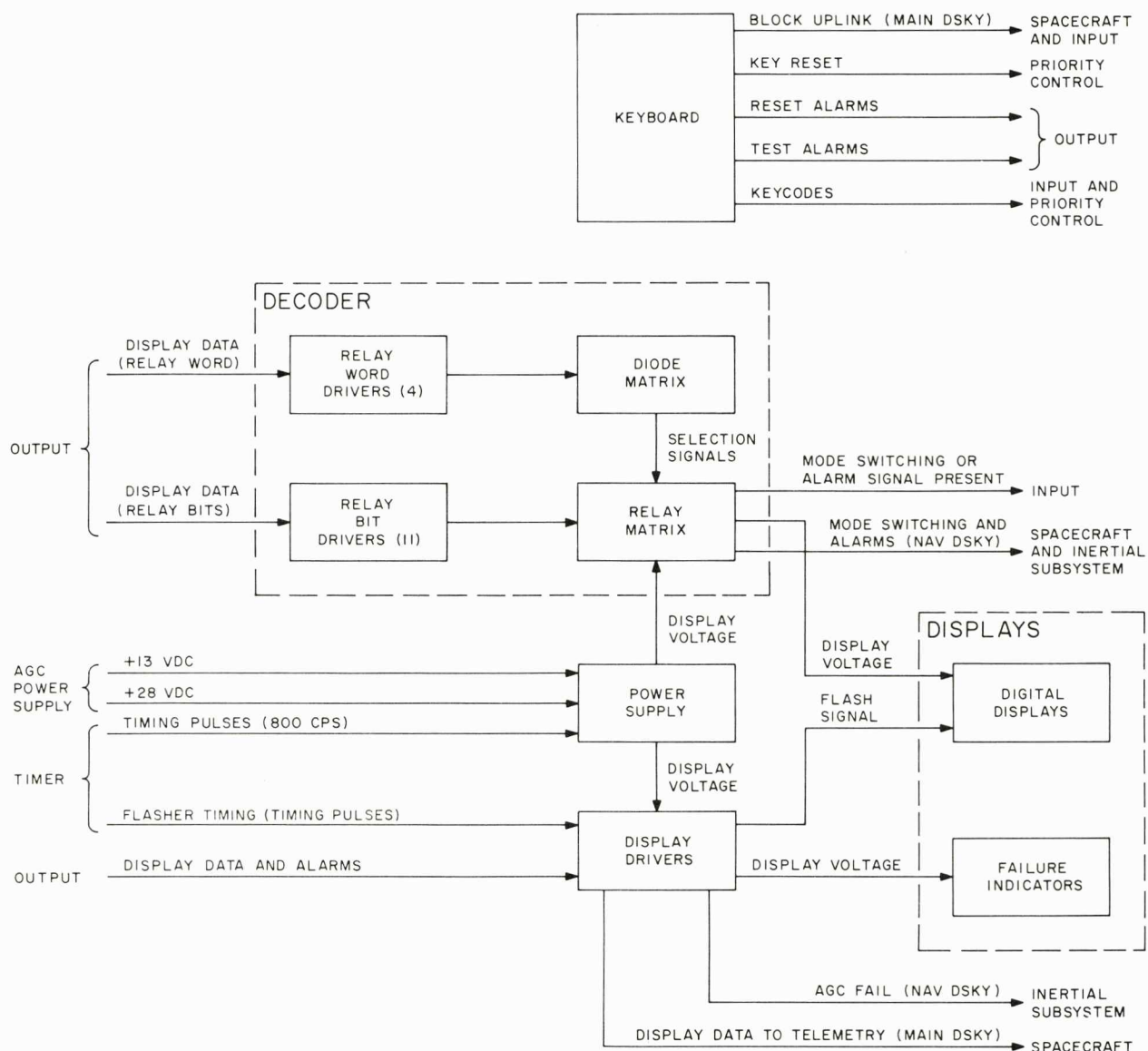
Because of load requirements, the +3 volt power supply requires two power switches. Each power switch contains a temperature sensing circuit; temperature sensing signals are supplied to the Inertial Subsystem. The +3 and +13 volt outputs are monitored by a failure detector. An AGC power fail alarm signal is supplied to the Spacecraft and to the Inertial Subsystem if an overvoltage or undervoltage condition exists.

5-3.8 DISPLAY AND KEYBOARDS. The DSKY's (figure 5-13) provide man-machine communication and provide alarm and operation signals to the Spacecraft and Inertial Subsystem. The astronauts can load information into the AGC with the DSKY's, request information from the AGC, initiate various programs stored in fixed memory, and initiate tests on the Apollo Guidance and Navigation subsystems. The DSKY's also display alarm indications and operational changes which may occur within the AGC. There are two DSKY's in the Computer Subsystem: the Main Panel DSKY and the Navigation Panel DSKY. The Main Panel DSKY is located on the Main Display and Control Panel; the Navigation Panel DSKY is located on the Lower Display and Control Panel. Each DSKY consists of a keyboard, a decoder, display drivers, displays, and a power supply.

Each keyboard contains controls with which the DSKY's are operated to generate the manual inputs. Manual inputs, applied to the Input section and Priority Control, consist of keycodes and the block uplink signal. The main panel DSKY keyboard contains a switch that controls the block uplink signal. Depressing any key generates a keycode which initiates an interrupt request. The subsequent interrupting program enters the keycode through the Central Processor to Memory. A keycode is followed by a key reset signal when the

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Figure 5-13. DSKY's, Functional Diagram

key is released. The test alarms signal and the reset alarms signal are generated by keys and are applied through the Input section to alarm circuits in the Output section. These two signals control AGC alarms that are detected by alarm circuits. (Other AGC alarms are detected by program operations.)

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The block uplink signal, sent to the Spacecraft and to the Input section, causes the uplink words sent to the AGC to be inhibited.

The decoder receives display data from the Output section in the form of a four-bit relay word and eleven relay bits. This display data is decoded to select the proper digital indicators for display. The drivers, the diode matrix, and the relay matrix perform the decoding. The drivers amplify the input bits and supply signals to the diode matrix and the relay matrix. The diode matrix produces a single selection signal for each set of inputs. This signal, in conjunction with the relay bits, selects which latching relays in the relay matrix energize. Selected relays then apply the display voltage to the proper digital indicators.

Relays within the relay matrix also provide mode switching and alarms to the Spacecraft and the Inertial Subsystem and provide an indication to the Input section that a mode switching or alarm signal is present. The mode switching signals specify zero encoder, coarse align, lock CDU, fine align, and roll re-entry conditions. The alarm signals light CDU, PIPA, and IMU fail indicators on the Inertial Subsystem Guidance and Navigation Panel. The CDU, PIPA, and IMU alarm conditions are not determined within the AGC; they are signaled by inputs received from the Inertial Subsystem.

The display drivers receive display data and alarm signals from the Output section and receive a flasher timing signal from the Timer. Eight of the display drivers initiate a failure indication when they receive an alarm signal. The other four have separate functions: one causes a computer activity operation indicator to light, another generates a flash signal which indicates an action request, and two are spares.

The display drivers in the Main Panel DSKY provide display data to the Telemetry System in the Spacecraft. The display drivers in the Navigation Panel DSKY provide an AGC fail indication to the Inertial Subsystem. The display data sent to the Spacecraft includes all AGC alarms, a computer activity indication, a key release indication, and the block uplink signal. The computer activity indication specifies that a test is being performed. The key release indication is produced by the AGC when the AGC requires control of the DSKY displays. When the operator depresses the corresponding key, the AGC obtains control and the key release indication is removed. The AGC fail indication from the Navigation Panel DSKY is present if any AGC alarm is detected.

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The displays consist of digital (operational and data display) and failure indicators. The digital indicators allow an astronaut to observe the data entered or requested via the keyboard. The failure indicators present an indication of any failures that occur.

The power supply utilizes +13 volts and +28 volts from the AGC power supply and 800-cps timing pulses to generate a 275-volt 800-cps display voltage. This display voltage is applied to the displays via the relay matrix.

5-4 MACHINE INSTRUCTIONS

Each machine instruction is a distinct operation such as add, increment the addressed counter, or multiply. The machine instructions are defined by order codes or command signals in the Sequence Generator. Order codes are supplied from the Central Processor or generated within the Sequence Generator. Each machine instruction consists of one or more subinstructions. The subinstructions are defined by subinstruction codes or by command signals within the Sequence Generator. Each subinstruction requires one memory cycle time for execution. One memory cycle time is defined by timing pulses T01 through T12. There are three functional divisions of machine instructions; regular, involuntary, and miscellaneous.

5-4.1 REGULAR MACHINE INSTRUCTIONS. Regular machine instructions identify distinct operations during program executions and consist of basic instructions and extra code instructions. Each basic instruction word in Memory contains a three-bit order code which identifies a basic instruction. This three-bit order code is converted to a four-bit order code within the Central Processor and then is supplied to the Sequence Generator. The three-bit order code identifies eight basic instructions. Three additional regular machine instructions, the extra code instructions, are identified by order codes obtained within the Central Processor by indexing. Indexing adds selected quantities to quantities specified by the three-bit order code. Therefore, the four-bit order code sent to the Sequence Generator is not limited to identifying eight instructions. Eleven regular machine instructions, consisting of eight basic instructions and three extra code instructions, are identified. The eight basic instructions are as follows:

- | | |
|----------------------------|------------------------|
| 1. Transfer control | 5. Clear and subtract |
| 2. Count, compare and skip | 6. Transfer to storage |
| 3. Index | 7. Add |
| 4. Exchange | 8. Mask. |

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The extra code instructions consist of the multiply, divide, and subtract instructions.

The transfer control instruction changes AGC control to an instruction word in a given location. The address of the instruction word that was to be executed next is stored, and a transfer control instruction can later be used to return AGC control to this stored instruction word.

The count, compare, and skip instruction selects one of four new instruction words, depending on the magnitude and sign of a quantity at a given location. This branching control allows program options depending on the results of selected computations.

The index instruction modifies basic instruction words to obtain order codes of extra code instructions and to obtain other basic instruction words. If a basic-instruction-word result is desired, either the order code or the order code and relevant address can be changed. The relevant address can not be changed when an order code of an extra code instruction is obtained.

The exchange instruction exchanges the contents of the Central Processor accumulator with the contents at a given location. If a location in fixed memory is given, its contents are copied into the accumulator after the former accumulator contents are cleared.

The clear and subtract instruction enters the complement of the contents at a given location into the accumulator. If the given location is the accumulator, the accumulator contents are complemented.

The transfer to storage instruction copies the accumulator quantity into a memory location or into another flip-flop register. If one memory location is not sufficient to store the quantity, other instructions which copy part of the quantity into a second location may be initiated.

The add instruction copies the contents of a given location into the accumulator if the accumulator was initially cleared. If the accumulator contained a number, the add instruction adds the contents of the given location to the number in the accumulator. If the given location is the accumulator, the accumulator contents are doubled.

The mask instruction detects individual-bit conditions of the binary word contained in the accumulator. The results are used to determine program execution options.

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The multiply instruction multiplies the accumulator contents by the contents of a given location. The result, because of its length, is stored in the accumulator and another register. The contents of the accumulator are squared if the given location is the accumulator.

The divide instruction divides the contents of a given location into the accumulator contents. The quotient is stored in the accumulator; any remainder is stored separately.

The subtract instruction subtracts the contents of a given location from the accumulator contents. The result is stored in the accumulator. If the accumulator was initially cleared, the subtract instruction copies the complement of the contents of a given location into the accumulator. If the given location is the accumulator, the result is a minus zero.

5-4.2 INVOLUNTARY MACHINE INSTRUCTIONS. Involuntary machine instructions do not obtain order codes from the Central Processor and consist of interrupt and counter instructions. These instructions are initiated by program interrupt and resume condition signals and by counter instruction commands. The interrupt request and counter instruction commands are generated by Priority Control. Resume conditions are detected by the Sequence Generator when an interrupting program is finished. Order and subinstruction codes for the two interrupt involuntary instructions are generated within the Sequence Generator. These are the interrupt and resume instructions that allow an interrupting program to be executed. The counter instruction commands from Priority Control inhibit program executions and initiate the counter instructions. There are four counter instructions; increment, decrement, shift, and shift and add one. The counter instruction commands control the Sequence Generator outputs and also prevent the stored order and subinstruction codes from affecting Sequence Generator outputs. Therefore, the counter instructions do not require order and subinstruction codes.

The interrupt instruction accomplishes transfer operations necessary to initiate an interrupt program. Instruction information and computation results of the current program are stored so that later the current program can be resumed at the point of interruption. Also, the address of the first instruction word of the interrupt program is brought into the Central Processor.

The resume instruction occurs at the end of an interrupting program. This instruction restores the instruction information and computation results. Execution of the interrupted program is then resumed.

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The counter instructions are initiated in the counter priority control circuits which also supply the address of the applicable counter to the Central Processor. A counter word is then brought into the Central Processor, and the counter operation is performed. The increment instruction adds one to the counter word; the decrement instruction subtracts one from the counter word; the shift instruction shifts the contents one place to the left; and the shift and add one instruction shifts the contents one place to the left and adds one. The shift instructions accomplish serial-to-parallel conversions of inputs to the AGC.

5-4.3 MISCELLANEOUS MACHINE INSTRUCTIONS. The miscellaneous instructions consist of the go, start at specified address, display, and load instructions. The Sequence Generator generates order and subinstruction codes for the go and start at specified address instructions. The Timer supplies the start signal which initiates the start instruction. The CTS supplies the start at specified address signal. The display and load initiation signals are instruction commands received from priority control circuits and are initiated by the CTS. As with the counter instructions, the display and load instructions have no order or subinstruction code.

The go instruction occurs in conjunction with the start signal. This instruction transfers AGC control to an instruction word that begins a program operation which places the AGC in an idle mode. The program being performed when the start signal occurs is displayed on the DSKY's. Through DSKY operation, the AGC can be returned to the original program or any other selected program. Other programs might be selected to perform tests if the start signal was generated as a result of an alarm. (The start signal can also be generated by the CTS.)

The start at specified address instruction enables the CTS to transfer AGC control to selected instruction words. An address is received from the CTS and copied into the Central Processor when the instruction is performed.

The display and load instructions are initiated by the CTS. The display instruction obtains a word from Memory that is addressed by the CTS and provides this word to the CTS for display and other uses. The load instruction loads data from the CTS into memory locations that are addressed by the CTS.

5-5 PROGRAMS

A program written for the AGC may perform such functions as solving guidance and navigation problems, testing the operation of the Guidance and Navigation System, and monitoring the entire operation of the Spacecraft. These programs are classified into utility programs, computer subsystem test programs, system test programs, and mission programs.

5-5.1 UTILITY PROGRAMS. The focal point of all program operations is the utility programs which manage operation of the AGC. These programs schedule the execution of jobs according to their preassigned priorities and perform similar functions for tasks within the real-time requirements of the Apollo mission. Interrupt programs, described in Priority Control, are also part of the utility programs. The utility programs also provide such complex mathematical operations as matrix multiplications, vector addition and dot product computations, using double or triple precision quantities (two or three words per quantity). Another function of the utility programs is to detect alarm conditions within other programs of the AGC and to provide indications to the operator when an error situation exists.

5-5.2 COMPUTER SUBSYSTEM TEST PROGRAMS. The AGC is designed such that, with the rest of the Guidance and Navigation System disconnected from the AGC, the outputs of the AGC can be connected to the inputs with a test connector. The computer subsystem test programs are then used to check the proper transmission of signals through the output circuits to the input circuits. The programs permit the AGC to run for long periods of time to compile data on component reliability and transient errors. These programs are used for checking the AGC and diagnosing possible malfunctions. The computer subsystem test programs check the AGC micrologic and core memory as exhaustively as possible. Certain computer subsystem test programs accomplish an AGC self-check during preinstallation and post-installation testing. During these phases of testing, all program inputs are supplied through the DSKY keyboard and all outputs are available on the DSKY displays.

5-5.3 SYSTEM TEST PROGRAMS. The system test programs exercise the Guidance and Navigation System in all of its operational modes. These programs are used for isolating malfunctions to a particular subsystem, including the Computer Subsystem. When the AGC is in subsystem test, some of the system test programs, in addition to the computer subsystem test programs, can be used to test the AGC. The system test programs are initiated through the DSKY keyboard. Each of the system test programs is

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identified by a code. When the code of a program is entered through the DSKY's, the utility programs schedule the execution of the system test program. Data for the system test programs is also entered through the DSKY's. Failures detected in any subsystem by the system test programs produce alarm indications on the DSKY's and other display panels of the Guidance and Navigation System. The system test programs also produce data for display on the DSKY registers. This information is compared with precalculated results to determine the operational capability of the Guidance and Navigation System.

5-5.4 MISSION PROGRAMS. The mission programs are the largest and most complex programs stored in fixed memory. These programs are the guidance and navigation programs and are initiated through the DSKY's. Information from other Guidance and Navigation subsystems is converted by these programs to quantities and coordinate systems which are used in solving the guidance and navigation equations. The guidance programs are executed during all powered phases of the mission. These programs control the spacecraft engines as well as the attitude of the spacecraft. The navigation programs compute the position and velocity of the spacecraft during all non-powered phases of the mission. These programs are executed when the spacecraft is in orbit or in a trajectory between the earth and the moon.

5-6 PHYSICAL CONFIGURATION

The Computer Subsystem consists of the AGC, the Main Panel DSKY, and the Navigation Panel DSKY.

5-6.1 APOLLO GUIDANCE COMPUTER. The AGC (figure 5-14) is approximately 24 inches wide, 19 inches deep, and 6 inches high and is located in the lower center of the Navigation Display and Control Panel below the Power and Servo Assembly. The AGC consists of three plug-in tray assemblies, an end connector assembly, and a toe plate. The three tray assemblies are mounted vertically on the coldplate, are plugged into the end connector assembly, and are secured to the toe plate on the edge of the coldplate. There is one memory tray assembly, one logic tray assembly, and one harness tray assembly. The end connector assembly is bolted to the coldplate and provides support for the tray assemblies. The coldplate is an aluminum-alloy, liquid-cooled, honeycombed structure.

The memory tray assembly (figure 5-15) consists of two panels which are mounted vertically on the coldplate and bolted back to back. The right hand panel contains 11 horizontally-mounted and 2 vertically-mounted sticks.

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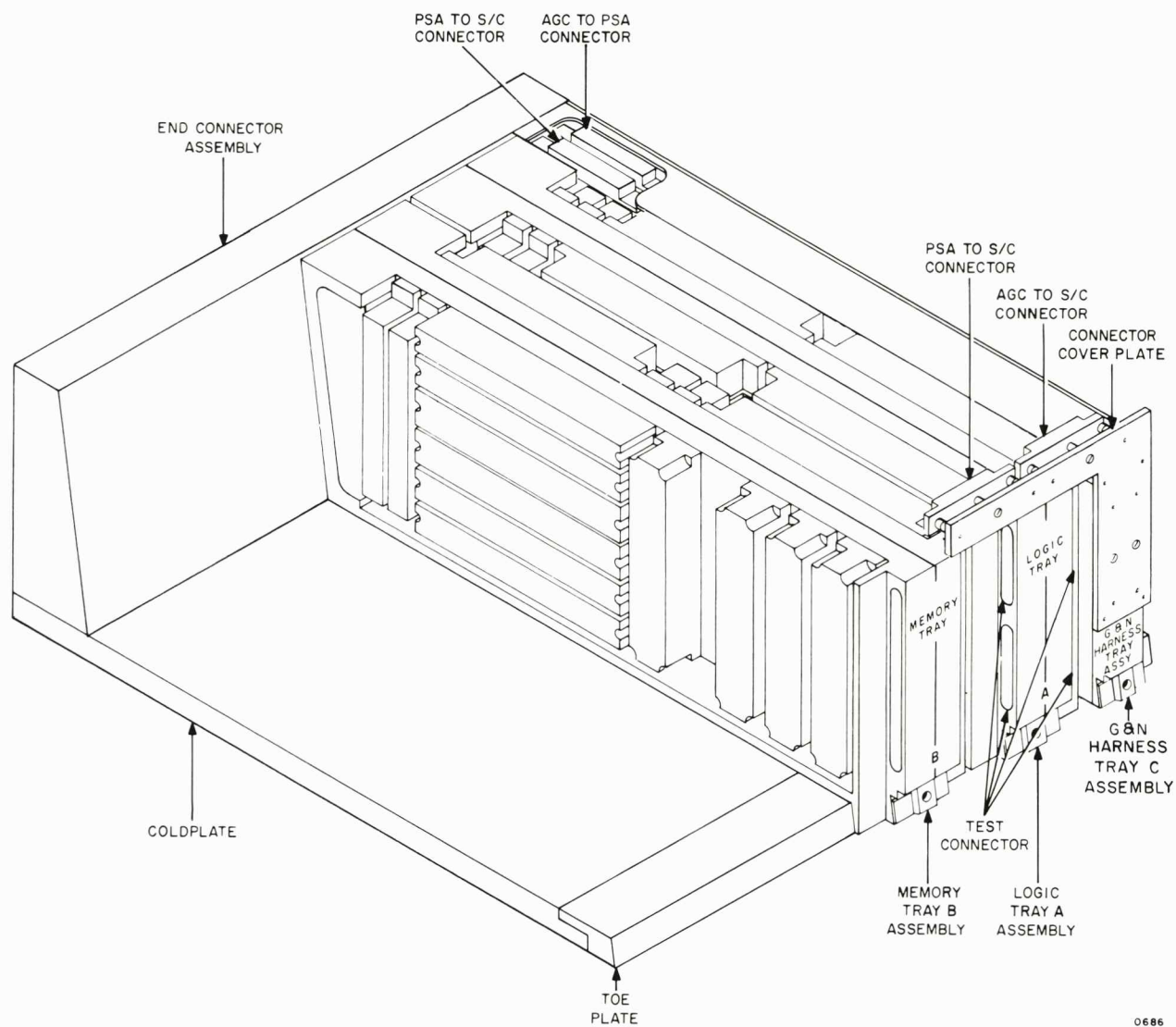
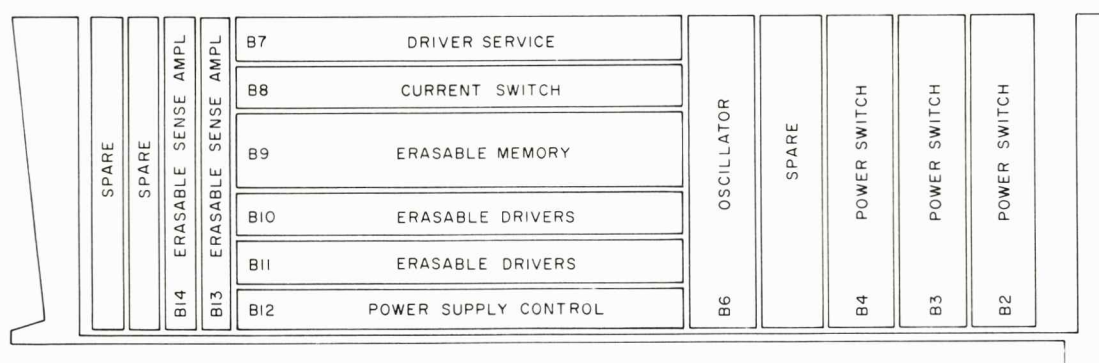


Figure 5-14. Apollo Guidance Computer

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LEFT PANEL



RIGHT PANEL

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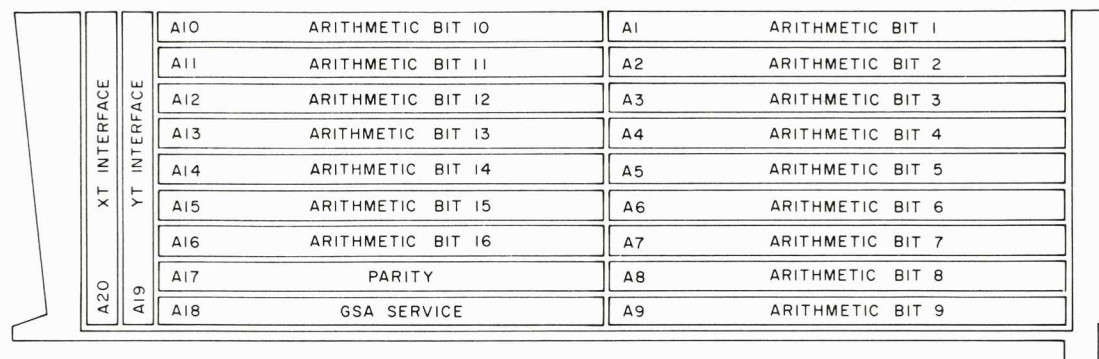
Figure 5-15. Memory Tray Assembly

The left hand panel contains 6 horizontally-mounted and 9 vertically-mounted sticks.

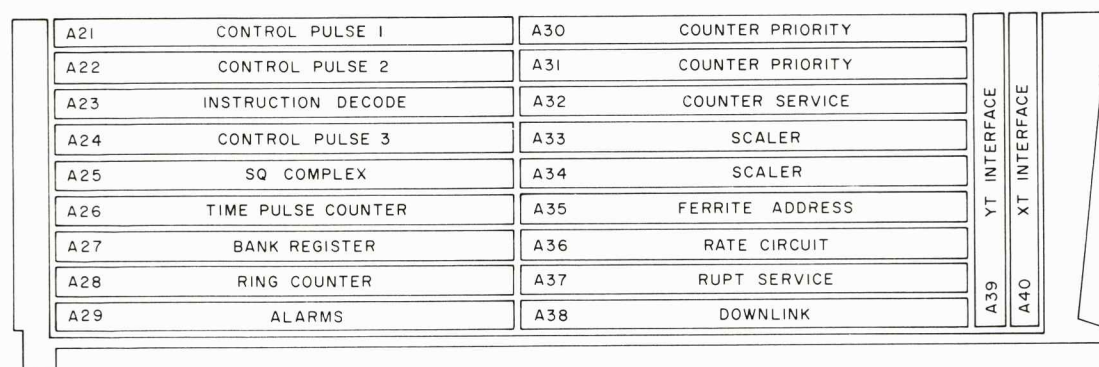
The logic tray assembly (figure 5-16) consists of two panels. Each panel contains 18 horizontally-mounted and 2 vertically-mounted sticks. Two test connectors, located on the logic tray assembly, provide connection between the AGC and Ground Support Equipment (Computer Test Set).

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LEFT PANEL

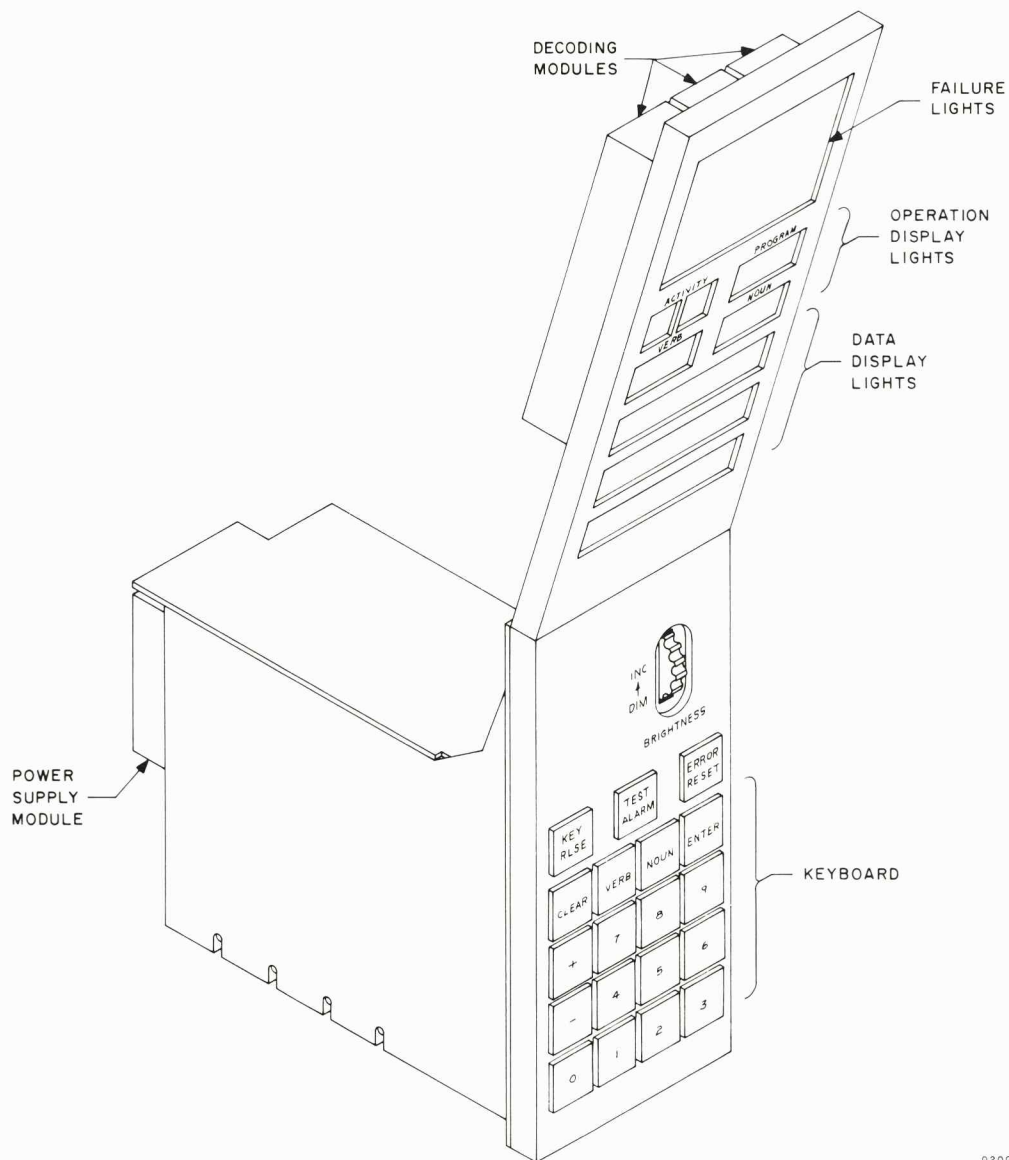


RIGHT PANEL

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Figure 5-16. Logic Tray Assembly

5-6.2 NAVIGATION PANEL DSKY. The Navigation Panel DSKY (figure 5-17) is located on the Lower Display and Control Panel. It is rectangular in shape and divided into two sections; one for the display and one for the keyboard. The display section contains failure lights, operation display lights, and data display lights. Mounted in the rear of the display section are three interchangeable decoding modules. The keyboard section contains keys and a brightness control. Mounted on the rear of the keyboard is a case containing four interchangeable relay trays and a power supply module. Each relay tray consists of seven sticks, each of which contains six relays. The power supply module furnishes the voltage to light the various displays.



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Figure 5-17. Navigation Panel DSKY

5-6.3 MAIN PANEL DSKY. The Main Panel DSKY (figure 5-18) is located on the Main Display and Control Panel. It is square in shape and differs from the Navigation Panel DSKY in the placement of front panel controls, the absence of one key and all but two failure lights, and the addition of a

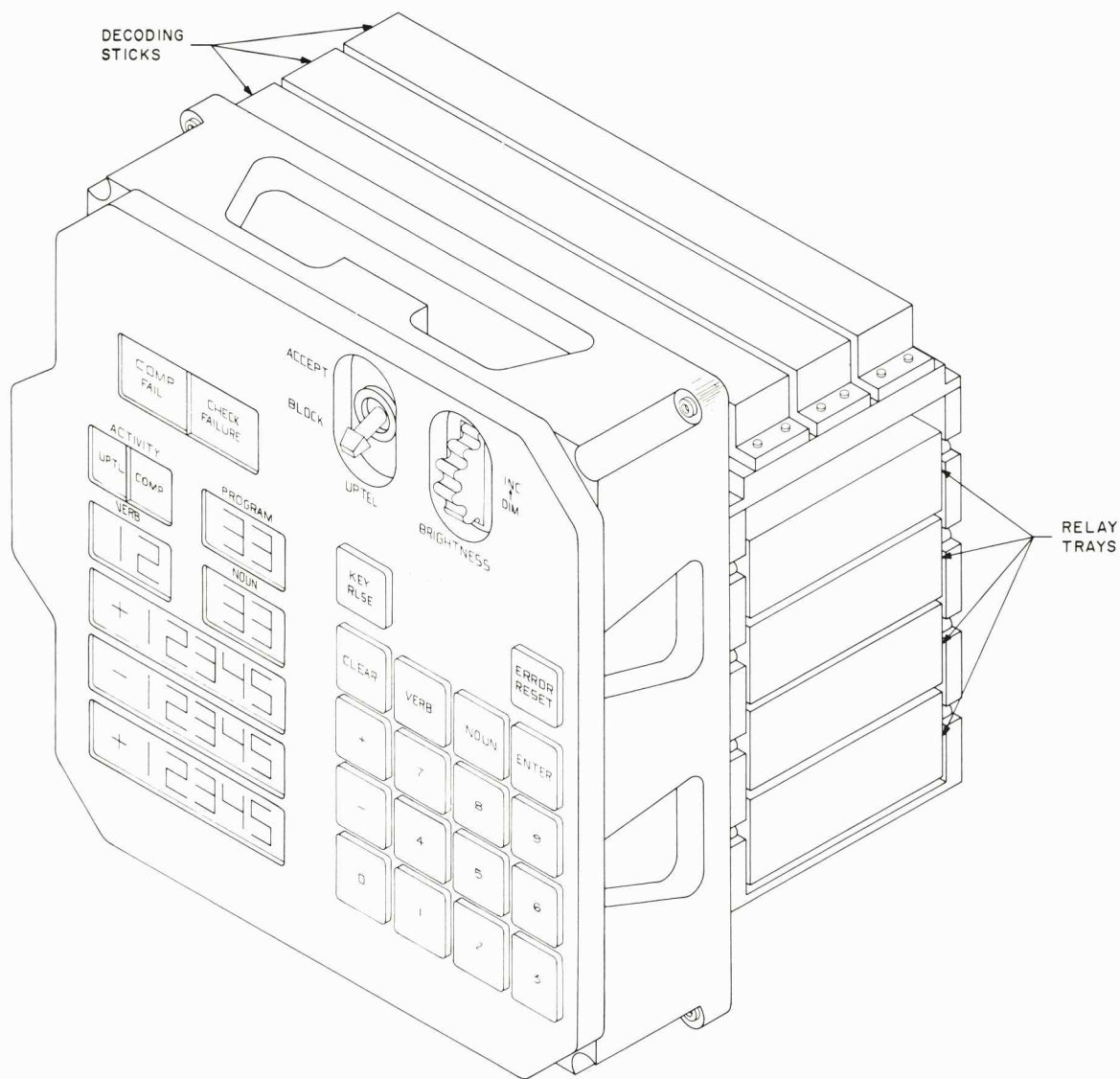


Figure 5-18. Main Panel DSKY

toggle switch. The functions of the operating controls and indicators located on both DSKY's are listed in table 5-1.

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Table 5-I. DSKY Operating Controls and Indicators

Control or Indicator	Applicable DSKY	Function
Failure lights	Navigation Panel	Indicate which of 12 possible alarms has occurred
ACTIVITY lights	Navigation Panel Main Panel	Indicate information is being received via uplink and/or that a test condition is in progress
PROGRAM lights	Navigation Panel Main Panel	Indicate which program is being processed
VERB lights	Navigation Panel Main Panel	Indicate verb code entered at keyboard
NOUN lights	Navigation Panel Main Panel	Indicate noun code entered at keyboard
Data display lights	Navigation Panel Main Panel	A plus or minus sign signifies data displayed is decimal; no sign signifies data is octal
COMP FAIL light	Main Panel	Indicates failure has occurred
CHECK FAILURE light	Main Panel	Indicates failure resulting from program control
TEST ALARM key	Navigation Panel	Tests several failure lights to ensure operation
KEY RLSE key	Navigation Panel	Releases displays initiated by the keyboard so that information supplied by program action may be displayed

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Table 5-I. DSKY Operating Controls and Indicators (cont)

Control or Indicator	Applicable DSKY	Function
UPTL switch	Main Panel	Controls reception of uplink information
BRIGHTNESS control	Navigation Panel Main Panel	Controls brightness of operation and data display lights
ERROR RESET key	Navigation Panel Main Panel	Clears failure lights after alarms are detected or after TEST ALARM key is used
CLEAR key	Navigation Panel Main Panel	Clears data contained in data registers. Clears whichever display register is currently in use
VERB key	Navigation Panel Main Panel	Conditions the AGC to interpret the next two numerical characters as an action request
NOUN key	Navigation Panel Main Panel	Conditions the AGC to interpret the next two numerical characters as an address code
ENTER key	Navigation Panel Main Panel	Informs AGC that assembled data is complete, execute the requested function
+ key	Navigation Panel Main Panel	Enters positive sign for decimal data
- key	Navigation Panel Main Panel	Enters negative sign for decimal sign
0 through 9 keys	Navigation Panel Main Panel	Enters data, address code, or action request code into AGC

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