

*Cape*

*I*

IBM HUNTSVILLE LIBRARY

MSFC No. III-5-510-17

IBM No. 66-966-0019

TECHNICAL MANUAL

SATURN IB/V INSTRUMENT UNIT  
COMMAND DECODER

(S-10-204 THRU 212/501 THRU 515)

Prepared under Contract

NAS 8-14000

by

International Business Machines Corporation

Federal Systems Division

Huntsville, Alabama

IBM HUNTSVILLE LIBRARY

*60 Pages*

1 June 1966

LIST of RELATED DOCUMENTS

The following manuals have been published under NASA contracts as source and reference information on IU systems and/or components.

Title	Number		Published Date	Changed Date
	IBM	MSFC		
Saturn IB/V Instrument Unit Structure Repair Manual	65-966-0011H	III-5-510-1	1 September 1965	
Auxiliary Power Distributors	65-966-0013H	III-5-510-2	1 October 1965	
Power Distributor	65-966-0014H	III-5-510-3	1 October 1965	
Emergency Detection System Distributor	65-966-0015H	III-5-510-4	1 October 1965	
Control Distributor	65-966-0016H	III-5-510-5	1 October 1965	
Measuring Distributors	65-966-0017H	III-5-510-6	1 October 1965	
56 Volt Power Supply	65-966-0018H	III-5-510-7	1 October 1965	1 May 1966
5 Volt Measuring Voltage Supply	65-966-0019H	III-5-510-8	1 October 1965	
Saturn IB/V Instrument Unit Switch Selector, Model II	66-966-0001	III-5-510-9	1 February 1966	
Saturn IB/V Instrument Unit Component Handling Equipment Description and Operating Instructions	66-966-0005	III-5-510-10	1 February 1966	
Saturn IB/V Instrument Unit C-Band Radar Transponder Set SST-135C	66-966-0008	III-5-510-11	31 July 1964	1 March 1966
Saturn IB/V Instrument Unit Control Accelerometer	66-966-0012	III-5-510-12	1 March 1966	
Saturn IB/V Instrument Unit Control-FDS Rate Gyro Package	66-966-0013	III-5-510-13	1 March 1966	
Saturn IB/V Instrument Unit Control Signal Processor	66-966-0014	III-5-510-14	1 March 1966	
Saturn IB/V Instrument Unit Flight Control Computer	66-966-0015	III-5-510-15	15 March 1966	
Saturn IB/V Instrument Unit Instrumentation System Description	65-966-0021	III-5-509-1	1 June 1966	

INSERT LATEST CHANGED PAGES, DESTROY SUPERSEDED PAGES

# LIST OF EFFECTIVE PAGES

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

Page	Issue
Title.....	Original
A.....	Original
1 thru 1v.....	Original
1 thru 7.....	Original
8 Blank.....	Original
9.....	Original
10 Blank.....	Original
11 thru 15.....	Original
16 Blank.....	Original
17.....	Original
18 Blank.....	Original
19.....	Original
20 Blank.....	Original
21 thru 23.....	Original
24 Blank.....	Original
25 thru 27.....	Original
28 Blank.....	Original
29 thru 31.....	Original
32 Blank.....	Original
33.....	Original
34 Blank.....	Original
35 thru 37.....	Original
38 Blank.....	Original
39.....	Original
40 Blank.....	Original
41.....	Original
42 Blank.....	Original
43.....	Original
44 Blank.....	Original
45.....	Original
46 Blank.....	Original
47.....	Original
48 Blank.....	Original
49.....	Original
50 Blank.....	Original
51 thru 53.....	Original
54 Blank.....	Original

\* The asterisk indicates pages changed, added, or deleted by the current change.

LIST of RELATED DOCUMENTS (Cont)

Title	Number		Published Date	Changed Date
	IBM	MSFC		
Saturn IB/V Instrument Unit Navigation, Guidance, and Control System Description	66-966-0003	III-5-509-2	1 February 1966	
Saturn IB/V Instrument Unit System Test Reference Manual Volume I Control System Volume II Guidance System Volume III ST-124M-3 Inertial Stabilizer System	66-966-0004	III-5-509-3	1 March 1966	
Saturn IB/V Instrument Unit System Description and Component Replacement Data	66-966-0006	III-5-509-4	1 March 1966	
Saturn IB/V Instrument Unit Environmental Control System Description	66-966-0009	III-5-509-5	15 March 1966	
Apollo-Saturn Emergency Detection System Description	66-966-0010	III-5-509-6	1 March 1966	
Saturn IB/V Instrument Unit Command Decoder	66-966-0019	III-5-510-17	1 June 1966	

# CONTENTS

Section	Page	Section	Page
<b>I</b>	<b>INTRODUCTION AND DESCRIPTION</b>		
1-1	Introduction.....	1	
1-2	Description.....	1	
1-3	General.....	1	
1-4	Mechanical Design.....	3	
1-5	Physical Characteristics.....	5	
1-6	Electrical Characteristics.....	5	
1-7	Connector Pin Assignments...	5	
<b>II</b>	<b>PRINCIPLES OF OPERATION</b>		
2-1	General Operation.....	11	
2-2	Data Verification.....	12	
2-3	Program Capabilities.....	15	
2-4	Detailed Operation.....	15	
		<b>III</b>	<b>PREPARATION FOR USE AND SHIPMENT</b>
		2-5	Detailed Logic Discussion..... 15
		2-6	Detailed Schematic Discussion. 25
		3-1	Preparation For Use..... 51
		3-2	Preparation for Shipment..... 51
		3-3	Packaging..... 51
		3-4	Marking..... 51
		<b>IV</b>	<b>PREVENTIVE MAINTENANCE AND REPAIR</b>
		4-1	Preventive Maintenance..... 53
		4-2	Repair..... 53

# ILLUSTRATIONS

Number	Page	Number	Page
1-1	Command Decoder.....	1-12	Wiring Side of Typical Printed Circuit Board Without Damper Board..... 7
1-2	Removed.....	3	
	Command Decoder Motherboard....	4	1-13 Command Decoder Outline Drawing..... 9
1-3	PSK Filter Printed Circuit Card...	6	
1-4	PSK Detector Printed Circuit Card.....	6	2-1 IU Command System Data Flow..... 11
1-5	5-Bit Counter and Shift Register Printed Circuit Card.....	6	2-2 Command Message Format..... 12
1-6	Missing Bit Detector Printed Circuit Card.....	6	2-3 Generation of PSK Data Signal..... 13
1-7	Shift Out and 32-Bit Counter Printed Circuit Card.....	6	2-4 Command Decoder Block Diagram... 14
1-8	Shift Register Printed Circuit Card.....	6	2-5 Command Decoder Logic Diagram (2 Sheets)..... 17
1-9	Monostable Multivibrator Printed Circuit Card.....	7	2-6 Command Decoder Flow Diagram.... 23
1-10	Power Supply Printed Circuit Card.	7	2-7 Encoded PSK Data..... 25
			2-8 PSK Filter Schematic..... 26
			2-9 PSK Detector Schematic..... 27
			2-10 5-Bit Counter and Shift Register Schematic..... 31
			2-11 Missing Bit Detector Schematic..... 33

## ILLUSTRATIONS (Cont)

Number		Page	Number		Page
2-12	Shift Out and 32-Bit Counter Schematic.....	37	2-16	Monostable Multivibrator Schematic..	45
2-13	Shift Register "A" Schematic .....	39	2-17	Power Supply Schematic .....	47
2-14	Shift Register "B" Schematic .....	41	2-18	Motherboard Interconnection Schematic .....	49
2-15	Shift Register "C" Schematic .....	43	3-1	Packaging Instructions for IU Command Decoder .....	52

## SECTION I

# INTRODUCTION AND DESCRIPTION

### 1-1 INTRODUCTION

The purpose of this manual is to provide the principles of operation, packaging procedures, and maintenance and repair instructions for the Saturn IB/V Instrument Unit Command Decoder (see Figure 1-1). The Instrument Unit Command Decoder, hereafter referred to as the Decoder, is an integral part of the Saturn IB/V Command System. This system is used during powered and orbital phases of flight to:

- Initiate closed-loop tests in the vehicle – the Decoder instructs the Launch Vehicle Digital Computer (LVDC) which test program is to be initiated.
- Provide ground computed orbital data to the LVDC.
- Instruct the LVDC to telemeter memory information.

The Decoder is specifically designed to provide highly reliable command information to the LVDC. The probability of an undetected error in the Decoder is approximately  $1 \times 10^{-9}$ . In addition to the low error rate of the Decoder, several sophisticated techniques of data verification are utilized. These techniques are discussed in detail in Section II of this technical manual.

### 1-2 DESCRIPTION

#### 1-3 GENERAL

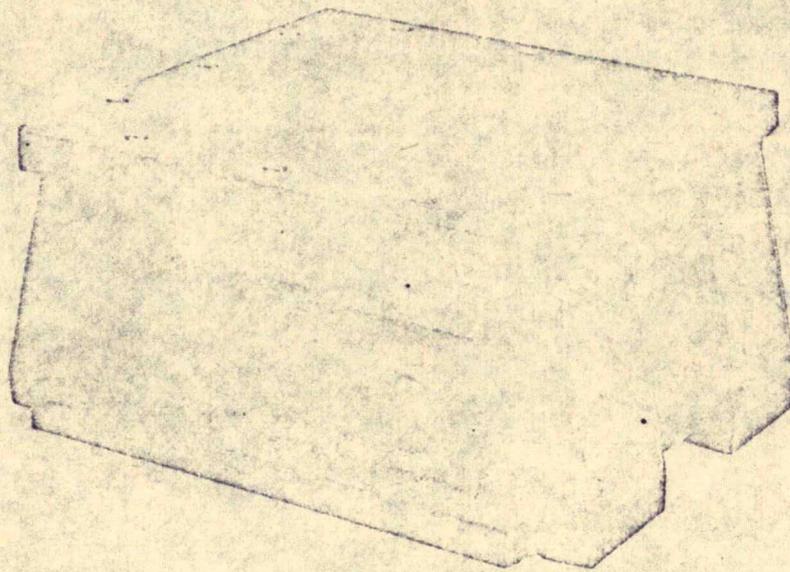
The Decoder is fabricated utilizing packaging techniques which provide maximum reliability. Some considerations are:

- Highly reliable components
- Welded modular construction
- Highly reliable printed circuit construction

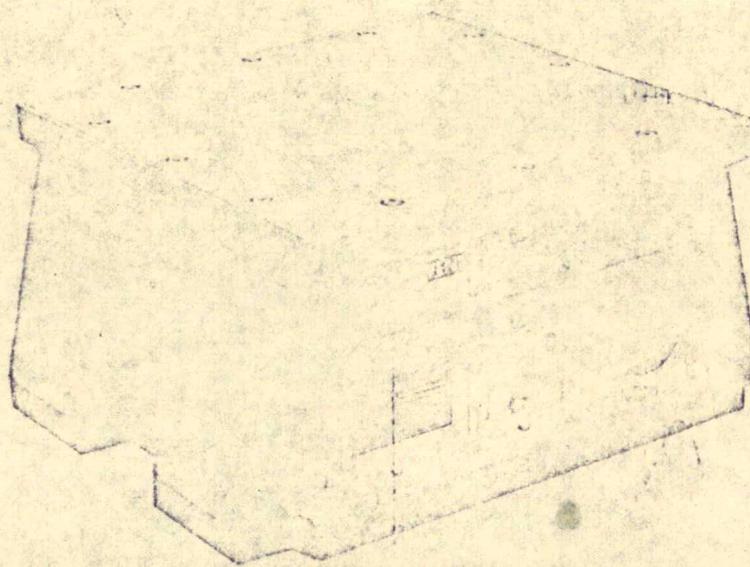
- Printed wire cabling
- Motherboard for plug-in cards
- RFI shielding
- Rugged mechanical construction

The Decoder is designed and packaged to meet all the anticipated environmental conditions of a Saturn IB/V vehicle. The package has outstanding features of ruggedness and serviceability. The assembly is modular, permitting the removal of the electronics with minimum effort (see Figure 1-2). The package consists of a housing with removable top and bottom covers. The electronics is installed from both top and bottom of the housing. This arrangement makes pre-wiring all connectors to the motherboard possible. The motherboard (see Figure 1-3) is the major board interconnect system plus a general connection and distribution point for all circuits. The pre-wired motherboard and connectors are installed into the housing from the bottom.

The motherboard rests against the inside structure of the housing. A foam rubber pad of sufficient size to cover the entire area of the motherboard is cemented to the bottom cover. The foam is of medium density. Installation of the bottom plate and rubber pad assembly applies a uniform pressure to the motherboard. The upward load from the rubber is sufficient to maintain the motherboard against the housing at all times. The electronic printed circuit cards are installed from the top of the housing. Grooves located in the side plates within the housing act as guides for the cards (see Figure 1-2). As a card is inserted in the box, the groove positions the card in line with the connector mounted on the motherboard. The semi-floating motherboard acts as an adjustment member in the mechanical system. After all cards are installed, the top cover is put in place. The top cover has two rubber strips cemented to the inside surface. These strips are of a higher density than the foam pad located under the motherboard. Only the edge of the cards contact the rubber resulting in small area contact; therefore, a more dense



FRONT VIEW



REAR VIEW

IBM AB

Figure 1-1. Command Decoder

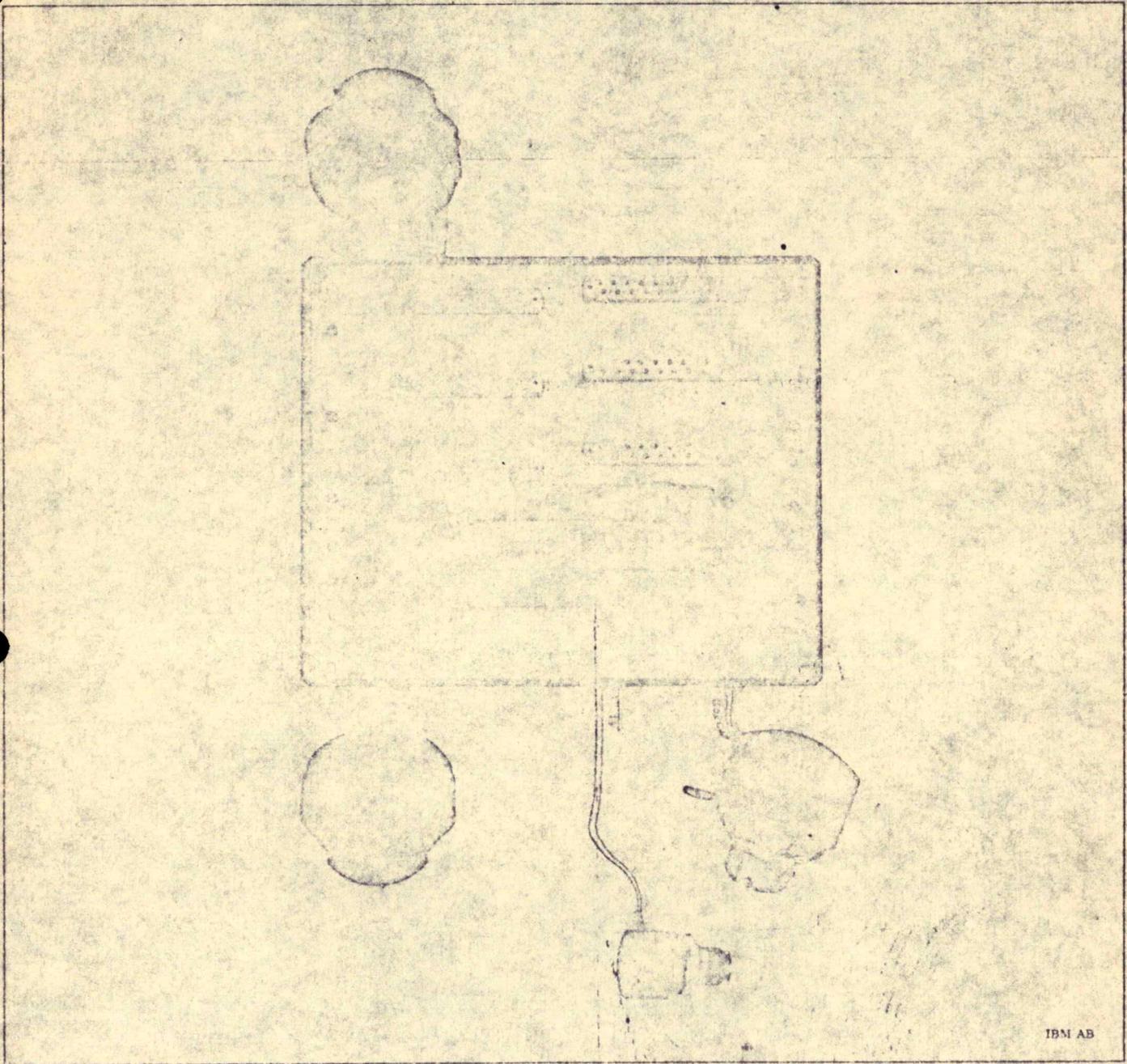


Figure 1-3. Command Decoder Motherboard

The side guides are aluminum plates with grooves that position the printed circuit cards in line with the motherboard connectors. The additional slot width accommodates a wave-type beryllium-copper spring that is installed and runs the length of the slot. The advantages of the wave spring include ease of inserting the printed circuit cards, positive spring pressure on card assemblies, and vibration isolation. To provide good electrical contact between the housing and the cover, the housing and cover are nickel plated per MIL-C-26074A. A RFI braided metal gasket is also used to further improve electrical contact between the covers and the housing. An O-ring groove is machined in the flange area of the housing to accommodate an O-ring seal. The O-ring provides protection against humidity and moisture and offers a seal against excessive leaking of the purge gas. A purge fitting is provided.

Module and Printed Circuit Card Construction

Welded electronic modules are sub-miniature electronic subassemblies produced by "cordwood" stacking of components between parallel films. The components are welded between the parallel welding films and then another film is placed on both sides of the "cordwood" stacking and the welding operation repeated. The double welding provides a highly reliable welded module. These modules are then cast in an epoxy compound. A freeze coat is applied to the welded modules prior to embedding for ruggedization and improved moisture protection. The encapsulated component assemblies are then placed on a printed circuit card. The leads from the module pass through the holes in the card and are soldered to printed pads. The surface of the card accommodates the modules. The modules are cemented in place and the clad side of the board is covered with a polyurethane coating. A viscoelastic vibration damping board is affixed to the rear of the printed circuit card. The damper board is specially designed for the Decoder and is shown in Figure 1-2. Figures 1-4 through 1-11 show the Decoder printed circuit cards. Figure 1-12 shows the wiring side of a typical circuit card without the damper board.

1-5 PHYSICAL CHARACTERISTICS

A detailed mechanical drawing is shown in Figure 1-13 providing all finished machined dimensions.

Other physical characteristics are:

Weight:	3.85 kg	(8.5 pounds)
Height:	10.79 cm	(4.25 inches)
Length:	22.60 cm	(8.90 inches)
Width:	18.39 cm	(7.24 inches)

1-6 ELECTRICAL CHARACTERISTICS

The electrical characteristics of the Decoder are as follows:

Primary Voltage .....	+28	+10 Vdc
		- 6 Vdc
Operating Current .....	80 ± 10	ma
Audio Input .....	1.9	+0.35 Vrms
		-1.25 Vrms
Input Impedance .....	75	ohms (resistive)
Binary Output Functions		
"One" .....	28	+0
		-3 Vdc
"Zero" .....	0 ± 0.5	Vdc
Data Output Impedance .....	Less than 1000	ohms
Telemetry Output Functions		
"One" .....	5 ± 1	Vdc
"Zero" .....	0 ± 0.5	Vdc
Telemetry Output Impedance ..	270 K	ohms

1-7 CONNECTOR PIN ASSIGNMENTS

The Decoder connector pin assignments are listed in Figure 1-13.

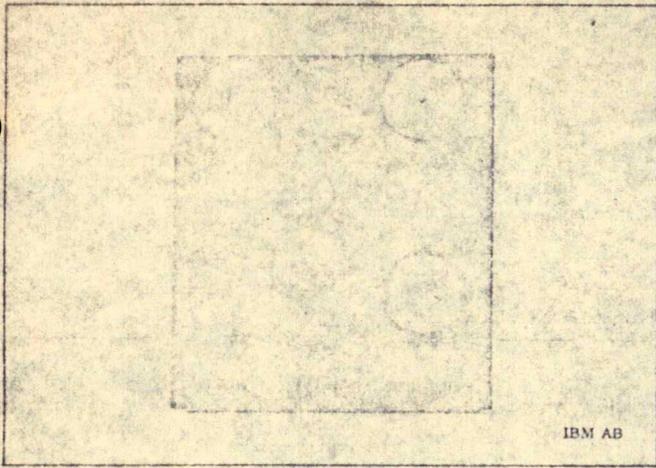


Figure 1-4. PSK Filter  
Printed Circuit Card

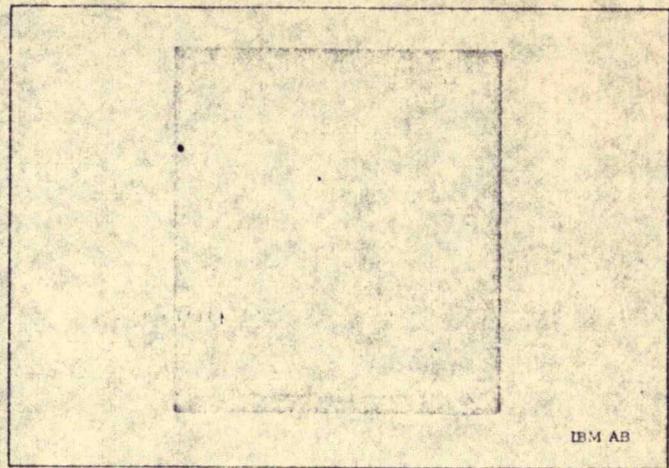


Figure 1-7. Missing Bit Detector  
Printed Circuit Card

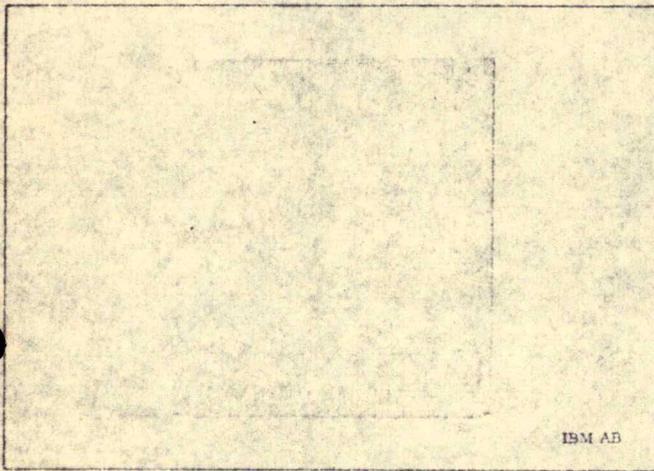


Figure 1-5. PSK Detector  
Printed Circuit Card

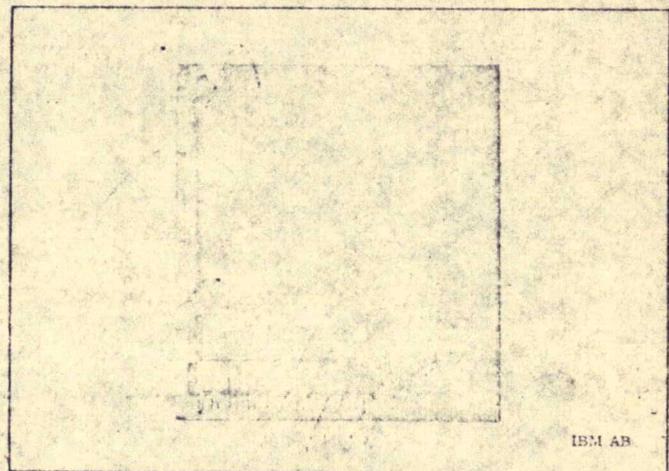


Figure 1-8. Shift Out and 32-Bit Counter  
Printed Circuit Card

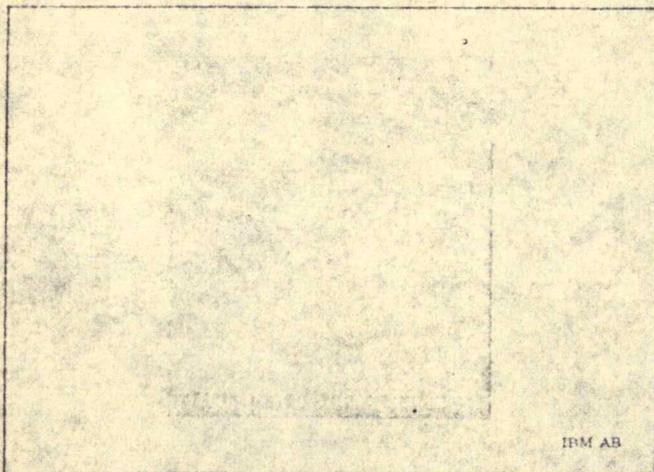


Figure 1-6. 5-Bit Counter & Shift Register  
Printed Circuit Card

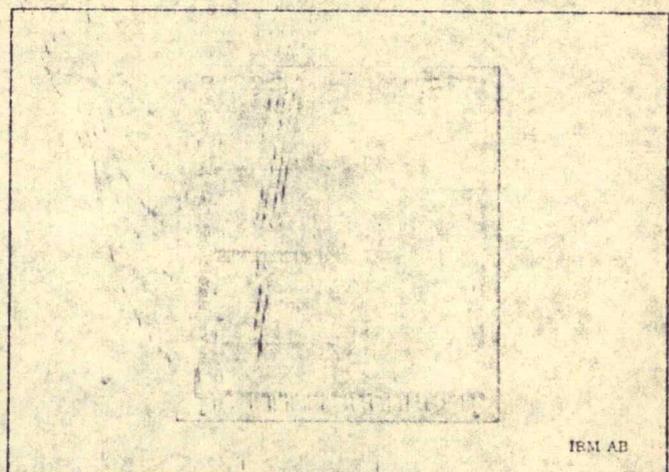


Figure 1-9. Shift Register  
Printed Circuit Card

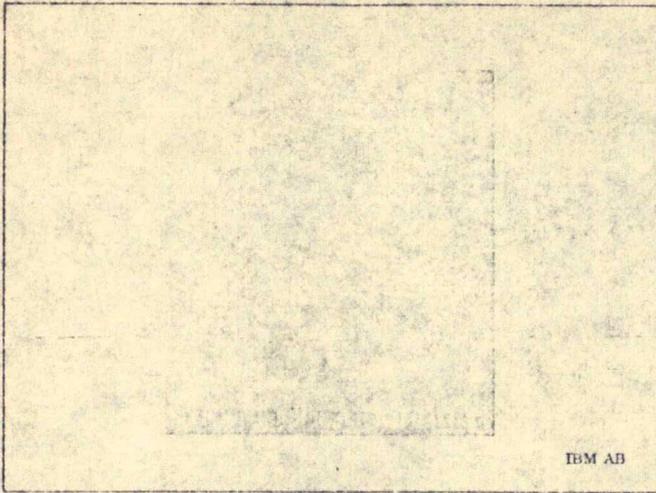


Figure 1-10. Monostable Multibrator  
Printed Circuit Card

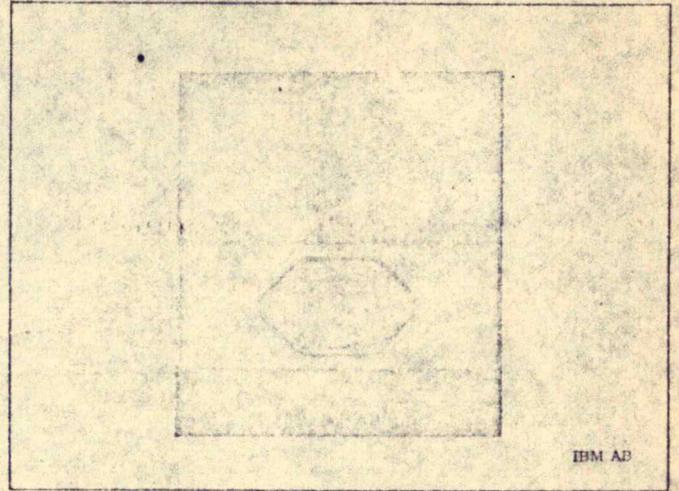


Figure 1-11. Power Supply  
Printed Circuit Card

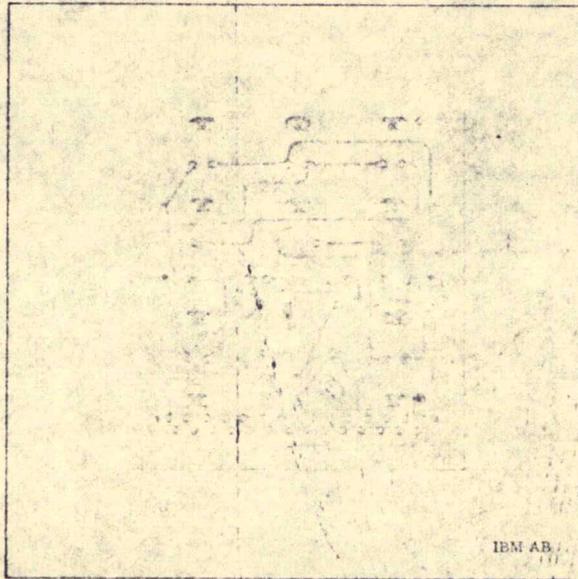
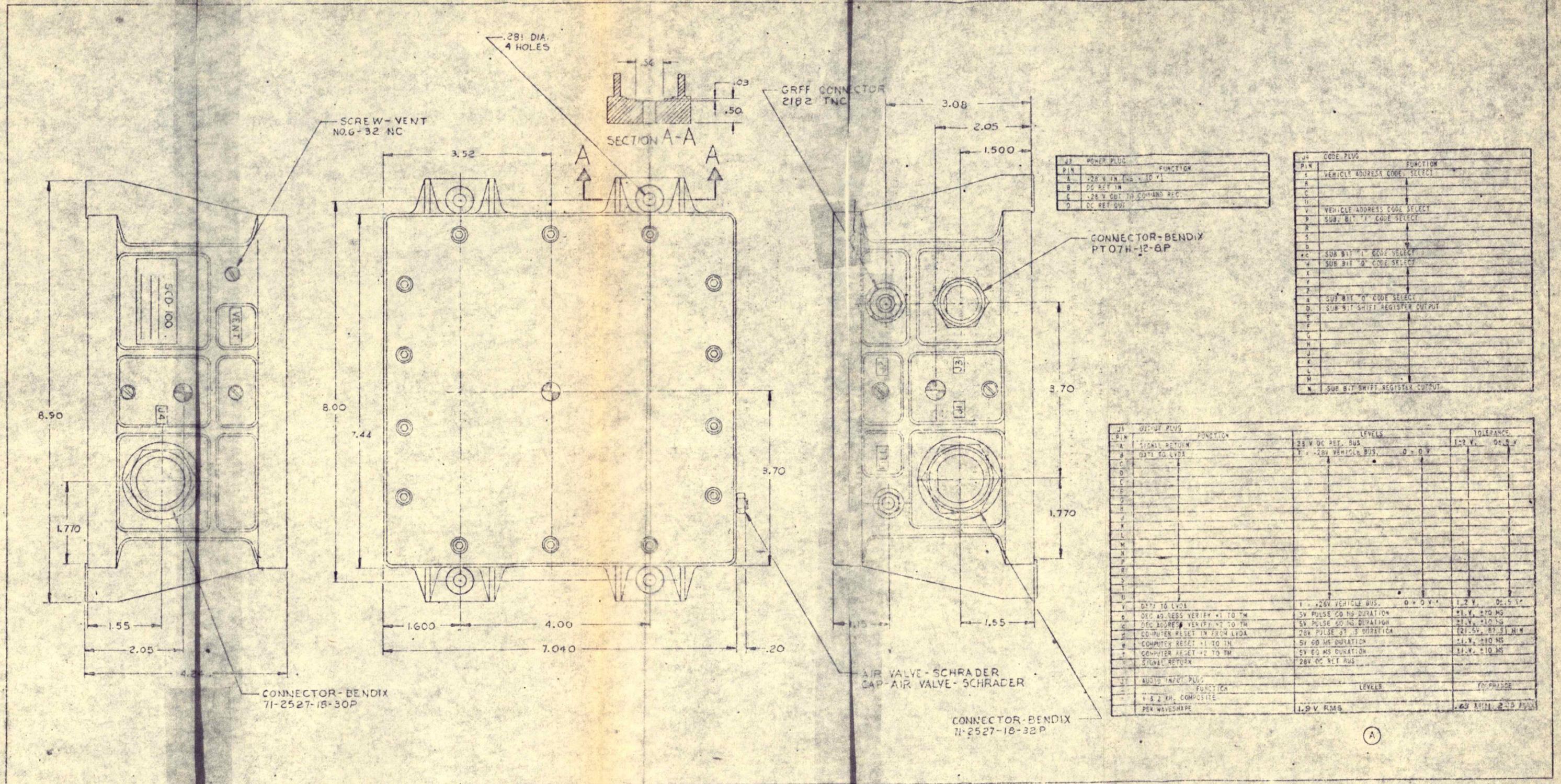


Figure 1-12. Wiring Side of Typical Printed  
Circuit Board Without Damper Board



J3 POWER PLUG	FUNCTION
A	+28 V IN (+5 - 10 V)
B	DC RET IN
C	+28 V OUT TO COMMAND REC.
D	DC RET OUT

J4 CODE PLUG	FUNCTION
S	VEHICLE ADDRESS CODE SELECT
A	
C	
U	
V	VEHICLE ADDRESS CODE SELECT
R	SUB BIT "1" CODE SELECT
S	
D	
*C	SUB BIT "1" CODE SELECT
*V	SUB BIT "0" CODE SELECT
X	
Y	
Z	
A	SUB BIT "0" CODE SELECT
D	SUB BIT SHIFT REGISTER OUTPUT
E	
F	
G	
H	
J	
K	
L	
M	
N	SUB BIT SHIFT REGISTER OUTPUT

J1 OUTPUT PLUG	FUNCTION	LEVELS	TOLERANCE
A	SIGNAL RETURN	28 V DC RET. BUS	1.2 V. 0.5 V
B	DATA TO LVDA	1 = +28V VEHICLE BUS, 0 = 0 V	
C			
D			
E			
F			
G			
H			
J			
K			
L			
M			
N			
P			
R			
S			
T			
V	DATA TO LVDA	1 = +28V VEHICLE BUS, 0 = 0 V	1.2 V. 0.5 V
W	DEC ADDRESS VERIFY #1 TO TM	5V PULSE 60 MS DURATION	±1 V. ±10 MS
X	DEC ADDRESS VERIFY #2 TO TM	5V PULSE 60 MS DURATION	±1 V. ±10 MS
Y	COMPUTER RESET IN FROM LVDA	28V PULSE 37.5 DURATION	(21.5V. 87.5 NIM)
Z	COMPUTER RESET #1 TO TM	5V 60 MS DURATION	±1 V. ±10 MS
A	COMPUTER RESET #2 TO TM	5V 60 MS DURATION	±1 V. ±10 MS
B	SIGNAL RETURN	28V DC RET BUS	
J2 AUDIO INPUT PLUG <td> <td> <td> </td></td></td>	<td> <td> </td></td>	<td> </td>	
	FUNCTION <td>LEVELS <td>TOLERANCE </td></td>	LEVELS <td>TOLERANCE </td>	TOLERANCE
	1 & 2 CH. COMPOSITE		
	PKW WAVESHAP	1.9 V. RMS	±.63 MIN. 2.35 MAX

Figure 1-13. Command Decoder Outline Drawing

## SECTION II

# PRINCIPLES OF OPERATION

### 2-1 GENERAL OPERATION

Figure 2-1 illustrates the data flow for the Saturn IB/V Command System. A Ground Station associated with the Manned Space Flight Network (MSFN) transmits a Command Message to the IU Command Receiver. The information is routed from the Receiver to the Decoder for decoding. If an error occurs during transmission, the message is rejected; if not, the following functions are performed by the Decoder:

- Address verification
- Logical combination of the address-verification and control bits allowing information transfer to the Launch Vehicle Data Adapter.

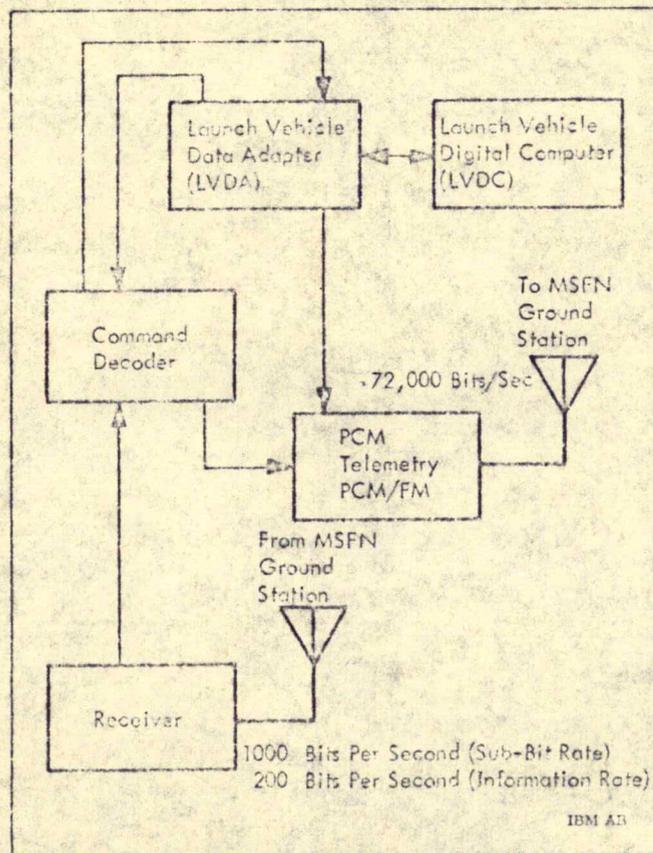


Figure 2-1. IU Command System Data Flow

- Generation of output signals to telemetry indicating the above functions have occurred.

Upon successful completion of decoding, the information is routed through the Launch Vehicle Data Adapter (LVDA) to the Launch Vehicle Digital Computer (LVDC). Verification that the LVDC has received the Command Message is transmitted via IU PCM Telemetry.

The characteristics of the Command Message are:

- Message length - 175 sub-bits
- Sub-bit rate - 1000 bps
- Encoding scheme - 5 sub-bits per data bit
- Effective data bit rate - 200 bps
- Effective Command Message length - 35 bits
- Modulation scheme - Phase Shift Keyed/  
Frequency Modulation (PSK/FM)

The 175 sub-bit Command Message after decoding is 35 data bits in length. The 35 data bits are recovered in the Decoder by decoding the sub-bits into 5 sub-bit groups to make up each data bit. A data bit may be defined as:

- "X" code - A coded pattern of 5 sub-bits; there are 3 "X" bits which are used to address the required vehicle.
- "1" code - A coded pattern of 5 sub-bits that determine the "1" data bit.
- "0" code - A coded pattern of 5 sub-bits that determine the "0" data bit.

The Command Message format is shown in Figure 2-2. The message is comprised of the following: 1) Vehicle address. The 3 "X" bits (15 sub-bits)

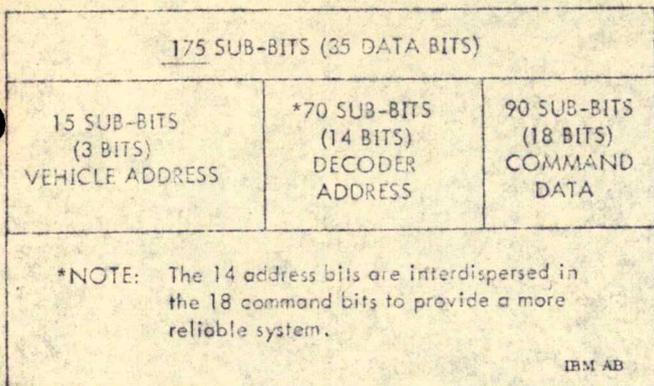


Figure 2-2. Command Message Format

are coded for the particular vehicle addressed to receive the command. 2) Decoder address. The address has 14 bits (70 sub-bits) which are compared with a prewired address in the decoder. The bits are interspersed in the message and are used to perform error checking. 3) Command data. The 18 bits (90 sub-bits) of command data conveyed to the LVDC via the LVDA.

The Command Message is encoded at the MSFN ground station transmitting to the vehicle. The encoding is accomplished by the algebraic addition of a 1 kHz reference sine wave to a coherent 2 kHz sine wave. The "O" sub-bit is generated by the addition (at the zero crossing) of the positive-going 1 kHz signal to the negative-going 2 kHz signal (-270° phase shift of the 2 kHz. Refer to Figure 2-3). The "1" sub-bit is generated by the addition (at the zero crossing) of the positive-going 1 kHz signal and positive-going 2 kHz (0° phase shift of 2 kHz). The algebraic addition of the 1 kHz and the 2 kHz signals result in waveform © of Figure 2-3.

The Decoder block diagram is shown in Figure 2-4. A description of Decoder operation is given below.

The PSK data from the Command Receiver is routed to the filter. The filter consists of two sections. 1) A low pass filter to reduce the noise and harmonics on the PSK data and 2) a narrowband 1 kHz filter to recover the original 1 kHz reference signal from the PSK data.

The outputs from the filter drive the sub-bit detector. The function of the detector is to determine the sub-bit "1's" and "0's". The detector also provides a shift pulse and count pulse at the sub-bit rate of 1000 bps.

The sub-bit "1's" and "0's" are written into a 5-bit shift register in the 5-bit counter and shift register. The 10 outputs (2 for each stage) from the 5-bit shift register are compared in parallel with prewired codes that determines the "X" data bit, "1" data bit, and "O" data bit. The prewired codes are established by 5 jumpers for each code in the code plug J4.

The "X" data bit, "1" data bit and "O" data bit are generated in the missing bit detector circuitry. The "X" data bit is the output of an AND gate whose 5 inputs are from the code plug (J4). The same is true of the "1" data bit and the "O" data bit. The outputs of the above gates are returned to the 5-bit counter and shift register where the "X" bit occurrences are counted and the "1's" and "0's" are inhibited until the third "X" bit count.

At this time the decoded data bits are written into a 32-bit shift register, the first 2 stages of which are located in the 32-bit counter and shift register. The shift pulses are counted in a 32-bit counter and an output provided at the count of 32. If the correct bits are written into the 32-bit shift register, an address verify pulse is sent to the output monostable multivibrators. Two monostables are used for redundancy. The monostable outputs are buffered to obtain the correct voltage levels and then sent to telemetry. The 18 lines of data in the 32-bit shift register are buffered and sent to the LVDA.

Upon receipt of the information, the LVDA generates a reset pulse preparing the Decoder for the next message. The reset pulse from the LVDA triggers 2-redundant monostable multivibrators allowing the computer return pulse to be buffered and sent to telemetry (denoting receipt of the computer reset pulse).

The missing bit detector insures correct Decoder operation by detecting the absence of any data bit (i. e. an error) in the pulse train of the Command Message. When this occurs the missing bit detector resets the Decoder and inhibits further processing. The "X" data bit, "1" data bit and "O" data bit are ORed in the 5-bit counter and shift register and provide the input to drive the missing bit detector.

## 2-2 DATA VERIFICATION

The application of the IU Command System and the information transmitted through the system require a high probability that a correct Command Message will be received in the vehicle. This high probability is obtained by the use of several different techniques throughout the system.

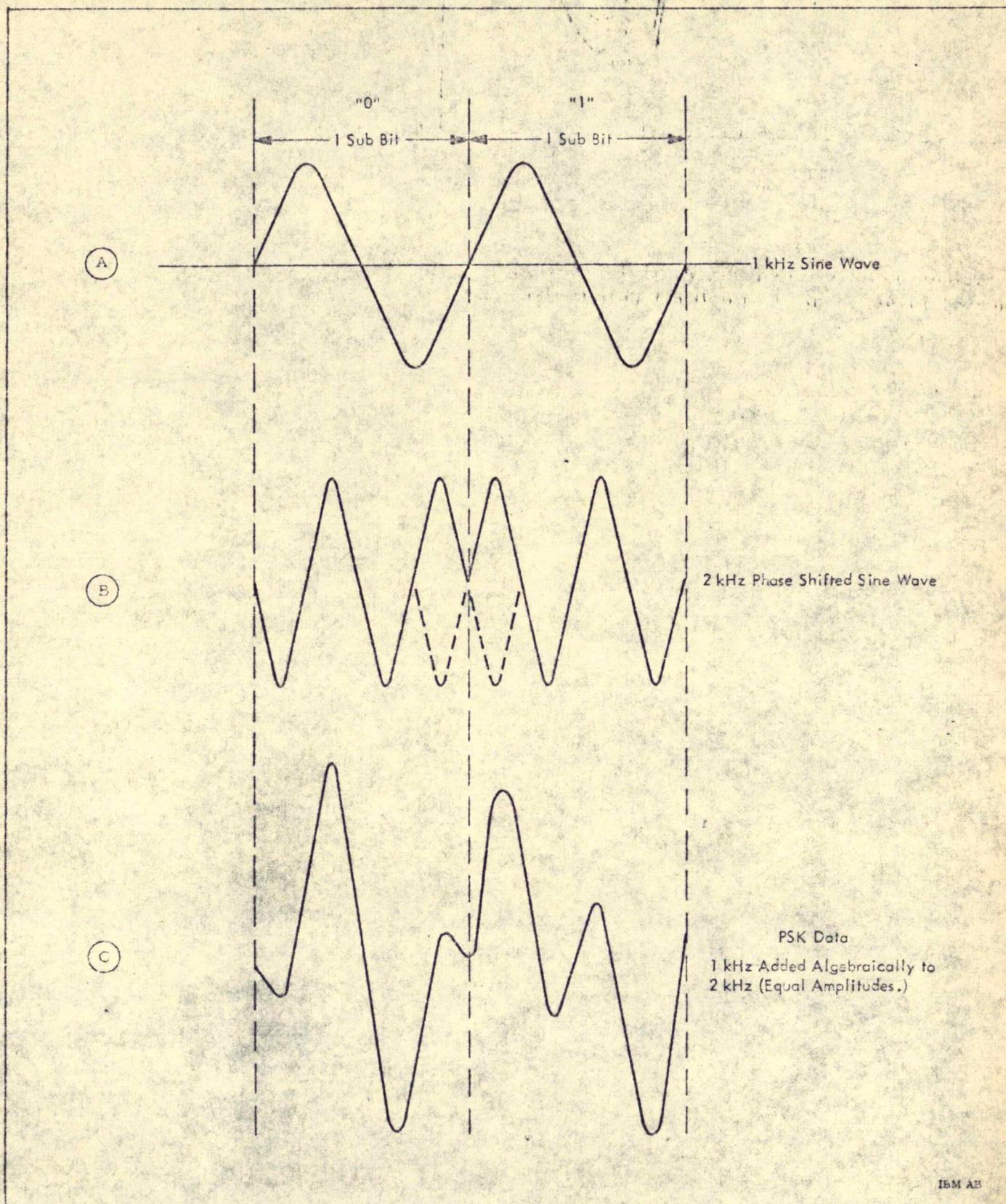
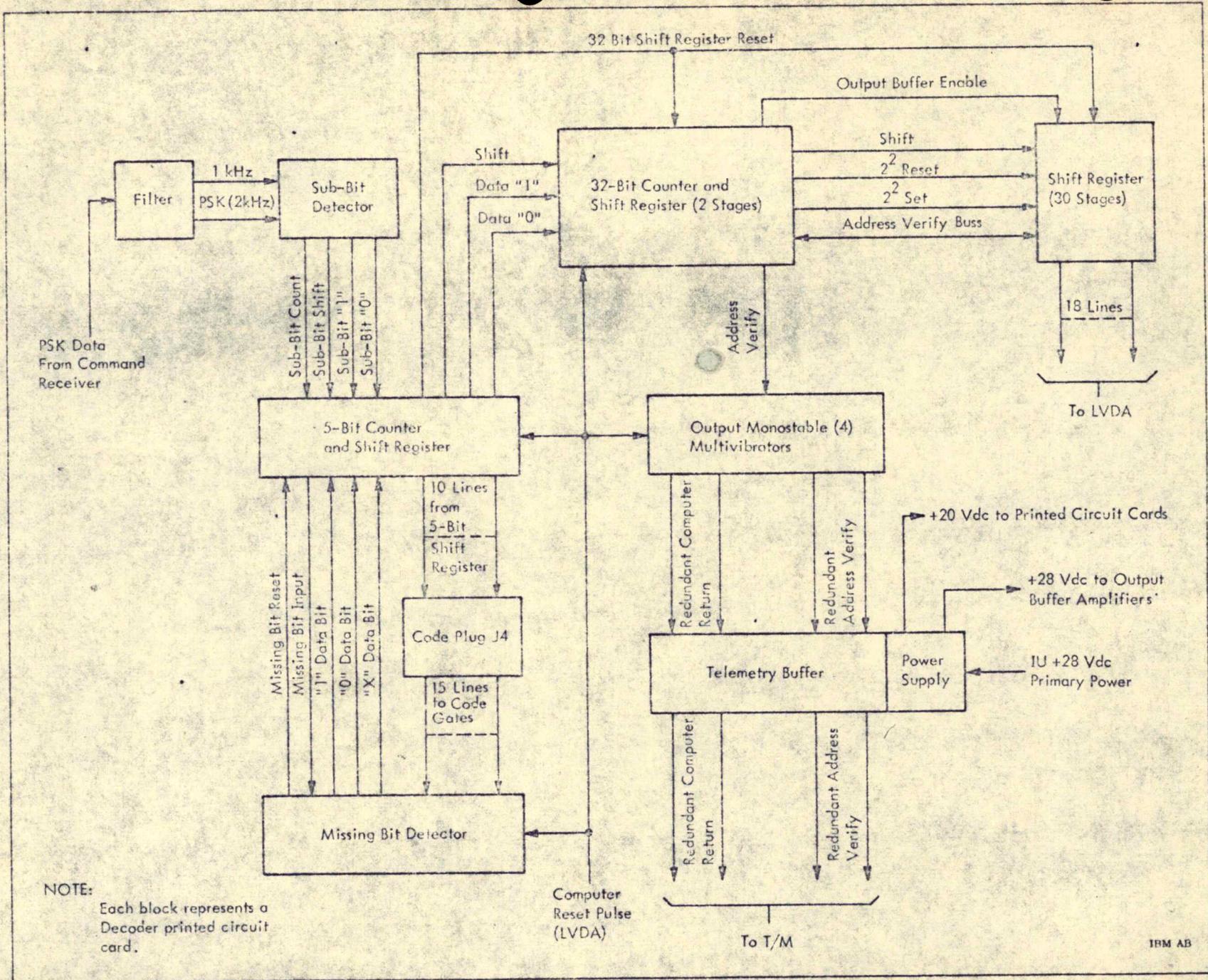


Figure 2-3. Generation of PSK Data Signal

Figure 2-4. Command Decoder Block Diagram



First, the Manned Space Flight Network is designed to provide a high degree of data transmission accuracy from the originating station in Houston, Texas, to the MSFN Digital Command System (DCS) which actually transmits the message to the vehicle. Secondly, to transpose a "1" bit to a "0" bit or vice-versa, every 1 of the 5 sub-bits of an update bit must be transposed to its complement; and this must be done in multiples of 5 in synchronism with the bit rate (200 bits per second) or the message will be rejected. Thirdly, 17 bits of each 35-bit transmission must be correct (there is no possibility of an undetected error here) before the 18 information bits are presented to the LVDA. Last of all, a verification loop utilizing telemetry as a downlink is employed to verify the 18 information bits for critical commands (the LVDC update commands).

The verification loop works as follows. If the 14-bit address is correct, an address verification pulse is sent to telemetry. This pulse is decommutated in real time at the ground station and presented to the message acceptance pulse circuitry. A second pulse is also derived in the vehicle and sent to telemetry. This is the LVDC reset pulse which signifies that the LVDC has received the 18 information bits. The pulse is also decommutated in real time and routed to the message acceptance pulse circuitry. The address verification pulse triggers a bistable multivibrator to the ON state. The LVDC reset pulse will occur a short time thereafter and trigger a 20-microsecond monostable multivibrator to the ON state. If the LVDC reset pulse does not appear during the ON time of the address verification pulse, then it will not appear at all for a given transmission. The 2 outputs are logically combined in an AND gate, which will have an output only when both multivibrators are ON at the same time.

The 20-microsecond pulse thus produced is called the message acceptance pulse and is fed to the DCS. The DCS uses this message acceptance pulse as a next-message-transmit signal. Upon receipt of this pulse, the DCS will transmit the next message (if any). If the message acceptance pulse does not appear within a certain length of time, the DCS will then retransmit the message. A dead time between messages is needed to ensure that the DCS does not retransmit prior to receipt of the message acceptance pulse. The delay takes into account all processing and loop delays, including propagation time (a maximum 2-way trip of 28,000 kilometers for the S-IVB/IU).

To complete the data verification, the LVDC stores all LVDC update messages (as many as forty

18-bit groups) and nondestructively reads out these data bits to telemetry. Upon receipt by the ground station, these bits are sent to Houston via MSFN and compared with those originally transmitted. If all bits are verified, an execute update command is sent to the DCS and thence to the vehicle. Only upon receipt of this message will the LVDC act upon the update data bits.

## 2-3 PROGRAM CAPABILITIES

The Decoder is designed so that a large number of program codes may be utilized. A description of these capabilities follows:

- "X" Bit Code - The "X" bit code is formed of 5 sub-bits and is the vehicle address designator found in the first 3 bits of the 35-bit Command Message. The code is externally programmed by the change of the code plug J4 on the Decoder.
- "1" Bit Code - The "1" bit code is a combination of 5 sub-bits to yield a data bit. The code is externally programmed by the code plug J4.
- "0" Bit Code - The "0" bit code is the "1's" complement of the "1" bit and programmed by the code plug J4.
- Address Code - The address code is derived from 14 interspersed bits of the 35-bit Command Message. The address code is used to generate an address verification for the Command Message. The code is factory set but may be changed with minor component changes. The change can be implemented for each bit by removing a diode from one side of a stage of the 32-bit shift register and placing another diode to the other side of the stage.

## 2-4 DETAILED OPERATION

### 2-5 DETAILED LOGIC DISCUSSION

During this discussion refer to Figure 2-5, Command Decoder Logic Diagram.

#### Filter

The PSK data from the Command Receiver is routed to a low pass filter. The function of this filter is to reduce the noise and harmonic content of the PSK data signal. The PSK data signal is then filtered in a narrow band filter to obtain a clean 1 kHz reference signal.

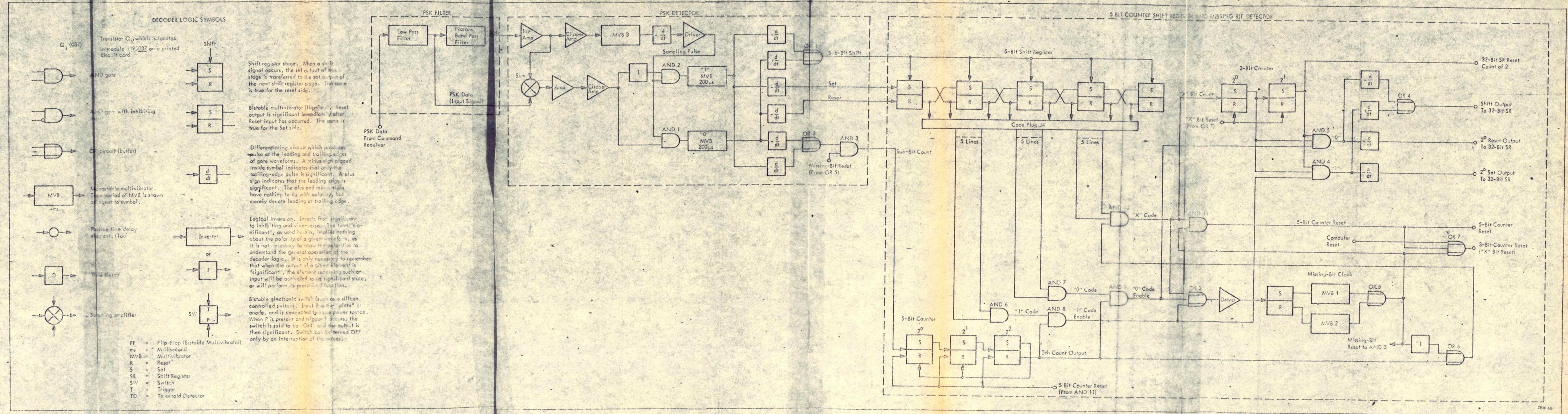


Figure 2-5. Command Decoder Logic Diagram (Sheet 1 of 2)

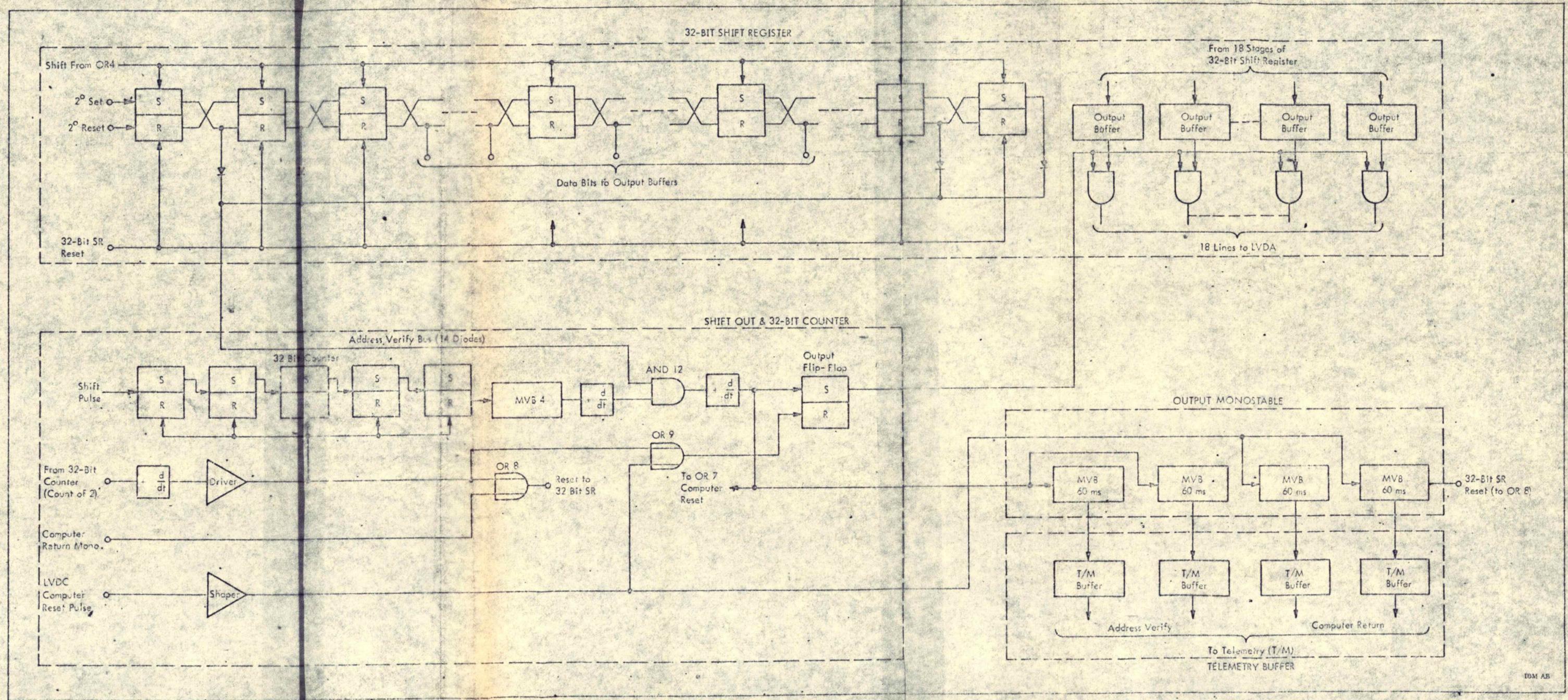


Figure 2-5. Command Decoder Logic Diagram (Sheet 2 of 2)

Detector

The PSK detector amplifies and shapes the 1 kHz and 2 kHz signals from the filter to determine the phase of the 2 kHz signal with respect to the 1 kHz signal. The relative phase of the signals determines the sub-bit "1's" and "0's" as required.

The 1 kHz signal from the filter is amplified and inverted 180° and then summed with the input signal. The output of the summing network is the relatively clean 2 kHz signal which is amplified, shaped, and applied to AND1 and inverted and applied to AND2.

The 1 kHz signal from the inverter amplifier is shaped and used to trigger monostable multivibrator MVB3. The output of MVB3 is differentiated to provide a very narrow sampling pulse appearing at a 1 kHz rate from the driver. The timing of the sampling pulse is adjusted to compensate for the phasing differences due to the RF link and the filter. The sampling pulse is applied to AND1 and AND2. AND1 and AND2, therefore, determine the phase of the 2 kHz signal with respect to the 1 kHz signal. Note that AND1 and AND2 cannot have an output at the same time.

The output from AND1 is used to trigger a 200-microsecond MVB, which is the "0" sub-bit output. The output of AND2 triggers a 200-microsecond MVB, which is the "1" sub-bit output. The leading edge of each 200-microsecond waveform is differentiated and ORed in gate OR1, and provides the shift pulse for the 5-bit shift register. The bits are written into the register by the differentiated trailing edge. The trailing edge is also ORed in OR2 and applied to gate AND3. Gate AND3 is enabled when the missing-bit clock is running. The output of AND3 is the sub-bit count pulse to the 5-bit counter.

5-Bit Counter and Shift Register

The sub-bit "1's" and "0's" from the sub-bit detector are written into the 5-bit shift register as required and routed to code plug J4.

The shift register has 10 outputs (2 for each position) resulting in  $2^5$  (32) possible sub-bit patterns. Each of 3 sub-bit comparators, "X," "1," and "0," (AND10, AND6, AND7) have 5 wires connected to the 5-bit shift register, via J4, 1 wire to each position. Hence, gate AND10 will have an output when the correct 5-bit code is written into the 5-bit shift register, thereby generating an "X" code.

The same is true for AND6 and AND7, thereby generating an "O" code or a "1" code. For example, the sub-bit code for a data "1" may be chosen as "11010", the sub-bit code for a data "0" may be chosen as the data "1's" complement, and the "X" sub-bit code may be chosen to be "11000".

During intervals when no messages are being transmitted, all sub-bit "1's" are transmitted; however, the comparators have no output. The first 3 data bits of a transmitted message are designated a "vehicle address" and are sub-bit coded as "X's." Since the message is bracketed by continuous sub-bit "1's," the "X" comparator is initially enabled by the output from OR6 through OR5, permitting an "X" comparison at any time the 5-bit shift register pattern is correct.

The "X" bits are counted in the 3-bit counter. At the second "X" bit, the set output of the  $2^1$  stage is used to reset the 32-bit shift register. The count-of-three in the 3-bit counter is applied to AND4. If the "1" code enable is true at this time, the output from the gate is the valid "1" bit. The same is true for gate AND5 if the "0" code enable is true. The positive leading edge of the "0's" and "1's" are ORed in OR4 and provide a shift pulse for the 32-bit shift register. The "0's" and "1's" are written into the register with the negative trailing edge.

As each group of 5 sub-bits is written into the 5-bit shift register, they are counted by the 5-bit counter. When the counter reaches a count of 5, a positive pulse is produced and used to open gates AND8, AND9, and AND10 (through OR6) to provide a "1" code enable, "0" code enable, or an "X" bit count pulse only when the correct 5 sub-bit pattern is written into the 5-bit shift register.

The input to the missing-bit clock is the output from OR3. The composite signal is therefore the "X" bit count, "1" code enable or "0" code enable. During normal message decoding, the pulse spacing is 5 milliseconds (200 bps). The missing-bit clock is essentially 2 monostable multivibrators (MVB1 and MVB2) which, if a proper message is being received, will provide a continuous output from OR5. This is accomplished by alternately triggering MVB1 and MVB2. The ON cycle of the multivibrators (5.4 milliseconds) is adjusted to be slightly greater than the duration of each data bit (5.0 milliseconds). Thus, the OFF multivibrator is triggered ON, 400 microseconds before the ON multivibrator completes its cycle, and OR5 will always have at least 1 input.

The output from AND11 at the first "X" bit will reset the 5-bit counter and will pass through OR7 to reset the 3-bit counter. The 3-bit counter is also reset through OR7 by the positive leading edge of the pulse from OR5 when the absence of a bit is detected by the missing-bit clock or when the computer reset pulse occurs at the completion of data transfer to the LVDA.

### 32-Bit Shift Register

The 32 bits following the three "X" bits are coded "O's" or "1's" as required. Each time a count-of-five state is reached by the 5-bit counter a comparison is made to determine if the bit is an "O" or a "1". These 32 bits are then written into a 32-bit shift register.

The decoder address is prewired and composed of 14 of the 32 bits of the shift register. These 14 bits must be true to have an output on the address verify buss. Note that the diodes of the buss may be connected to the set or reset side of each shift register stage as prescribed by the decoder address desired.

The 18 data bits are buffered and sent to the LVDA for processing.

### Shift Out and 32-Bit Counter

The second "X" bit count of the Command Message input from the 3-bit counter is differentiated and the positive pulse resets the 32-bit counter, the output flip-flop (through OR9) and the 32-bit shift register (through OR8).

The input shift pulses to the 32-bit shift register are counted by the 32-bit counter. At a count of 32, MVB4 is triggered, strobing gate AND12. At this time, the 32 data bits have been completely written into the 32-bit shift register. If the decoder address in the register is correct, gate AND12 is opened and the positive leading edge used to:

- Set the output flip-flop, thus enabling the output buffers
- Reset the 3-bit counter
- Trigger the address verify MVB.

The computer reset pulse (at the completion of data transfer to the LVDA) resets the output flip-flop through OR9, thus disabling the output buffers.

The computer reset pulse also triggers the computer return MVB's, whose output is returned to OR8 to reset the 32-bit shift register.

### Output Monostables

The address verify pulse from the address verify buss is routed to redundant MVB's. The output pulse width on the MVB's is set to 60 milliseconds, and is sent to telemetry to denote decoder address verification. The computer reset pulse from the LVDA is used to trigger another pair of redundant MVB's (60 milliseconds) which acknowledge receipt of the computer reset pulse. The outputs of the MVB's are buffered to meet the required input voltage levels of the IU PCM Telemetry System.

### Summary

The flow diagram, Figure 2-6, illustrates Decoder operation. In this summary reference is made to the logic elements of Figure 2-5.

The first "X" bit comparison in the Command Message generates a 1-millisecond pulse which is differentiated; the leading edge passes through AND11 and resets the 5-bit counter and through OR7 to reset the 3-bit counter. The trailing edge of the pulse advances the 3-bit counter 1 count and starts the missing-bit clock. When the missing-bit clock starts, the output of OR5 will: (1) open AND3, enabling the 5-bit counter, and (2) inhibit AND11, preventing the next "X" comparison from generating a reset.

As the next 5 sub-bits are written into the 5-bit shift register, they are counted by the 5-bit counter. When the counter reaches a count of 5, the output passes through OR6, thus enabling a second "X" comparison. A valid "X" comparison will generate a 200-microsecond pulse. The trailing edge of this pulse will advance the 3-bit counter to the count-of-two state and will also keep the missing-bit clock running. The count-of-two output from the 3-bit counter will (1) clear the 32-bit shift register (the cleared state of this register is when there is an "O" stored in the "O" side of all 32 stages), (2) send a reset pulse to the 32-bit counter, and (3) send a reset pulse to the output flip-flop. After the third "X" bit has been recognized, the count-of-three output from the 3-bit counter will provide a direct-coupled signal to AND4 and AND5. As long as the signal is present, AND4 and AND5 are "open"; that is, they will allow valid "O" and "1" bits to pass through.

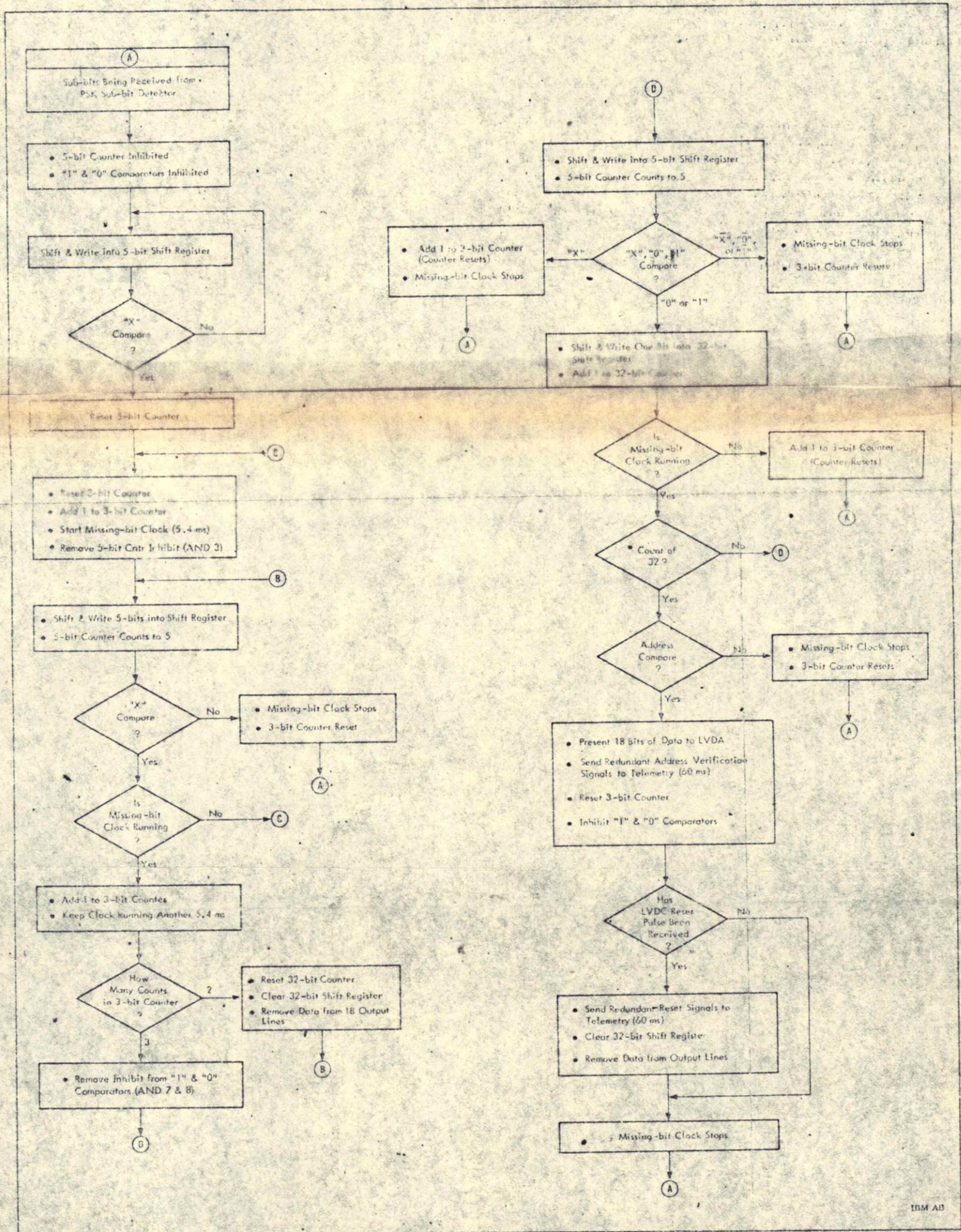


Figure 2-6. Command Decoder Flow Diagram

The next 32 bits will be coded with "0's" and "1's" as required. Each time a count-of-five state is reached by the 5-bit counter, a comparison is made to determine if the bit is an "0" or a "1". A pulse will be produced at the output of OR3, thus keeping the missing-bit clock running. These 32 bits will also be shifted and written into the 32-bit shift register and counted by the 32-bit counter. Upon the count of 32, a 1-millisecond monostable multivibrator is triggered ON. This signal opens AND12 and allows an address comparison to be made. If the address is correct, a signal will pass through AND12 and trigger the output gate flip-flop (a bistable multivibrator) to its set state. In addition, the two 60-millisecond monostable multivibrators will be triggered ON, providing an indication to telemetry that the address was valid. Two multivibrators are used for reliability.

The set output of the flip-flop also resets the 3-bit counter (through OR7) and provides an enabling voltage to the 18 data-output buffers. The binary information stored in the 18 data stages of the 32-bit shift register is thus transferred in parallel form to the LVDA. When the LVDC accepts these data bits from the LVDA, a reset pulse acknowledging receipt is sent through the LVDA to the decoder. This pulse will pass through OR9 to 1) reset the output flip-flop (thus disabling the 18 data-output buffers), 2) trigger two 60-millisecond monostable multivibrators, and 3) clear the 22-bit shift register through OR8. The outputs of these 2 multivibrators are sent to telemetry to indicate receipt of the LVDC reset pulse. If, for some reason, the LVDC reset pulse does not arrive prior to the beginning of the next message, the second "X" bit of vehicle address will provide an output from the 3-bit counter to reset the decoder circuits.

## 2-6 DETAILED SCHEMATIC DISCUSSION

During this discussion reference will be made to the Decoder logic diagram, Figure 2-5; the PSK data waveform, Figure 2-7; the IU Command Decoder Schematics, Figures 2-8 through 2-17; and the motherboard schematic, Figure 2-18.

The motherboard schematic shows the printed circuit card interconnections. A description of each card is given below.

### Note

During the following discussion reference to detail parts (with the exception of the filter circuit) will be as follows: Q1(037) will refer to transistor Q1 located in module 1195037 on a printed circuit card.

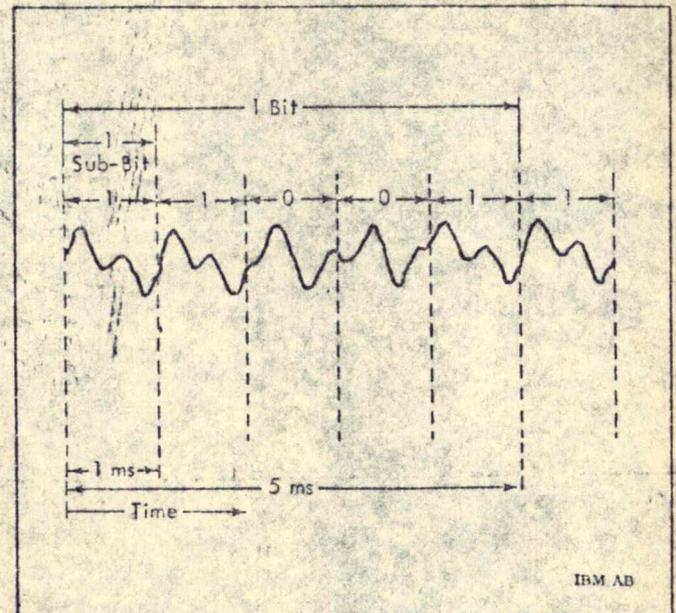


Figure 2-7. Encoded PSK Data

### Filter

The function of the filter circuitry is to separate the 1 kHz reference signal from the composite PSK data. A schematic of the filter card is shown in Figure 2-8. The PSK data (Figure 2-7) is taken from connector J2 and transformer coupled through T1 to low pass filter (L1 thru L3 and C1 thru C4). The low pass filter removes the harmonics and noise from the composite PSK data signal. This signal is further filtered in a sharply tuned 1 kHz filter (L4, L5, C5, C6, R2 and R3) to remove the 2 kHz modulating signal obtaining the pure 1 kHz reference signal. The information signals developed across R1 and R3 are used in the Detector.

### Detector

The schematic and waveforms of the detector card are shown in Figure 2-9. The 1 kHz signal from the filter is phase shifted 180° during amplification by Q1(034) and added algebraically to the 2 kHz (PSK) signal at the base of Q1(037). The 1 kc signal is coupled from the collector Q1(034) to the base of Q1(037) via C1 and R2. The signal at Q1(034) is amplified by Q2(034) and the negative half of the sine wave clipped by CR1(034) (see waveforms on Figure 2-9). The positive portion of the 1 kHz sine wave turns ON transistor Q3(034) driving the collector to ground as shown in waveform (A). The resulting pulse is differentiated by C5(034) and the trailing edge of the pulse (positive) triggers the monostable multivibrator (MVB) composed of Q4(034) and Q5(034).

NOTES:  
1. LAST REFERENCE DESIGNATORS USED ARE T1, L5, C6 AND R3.

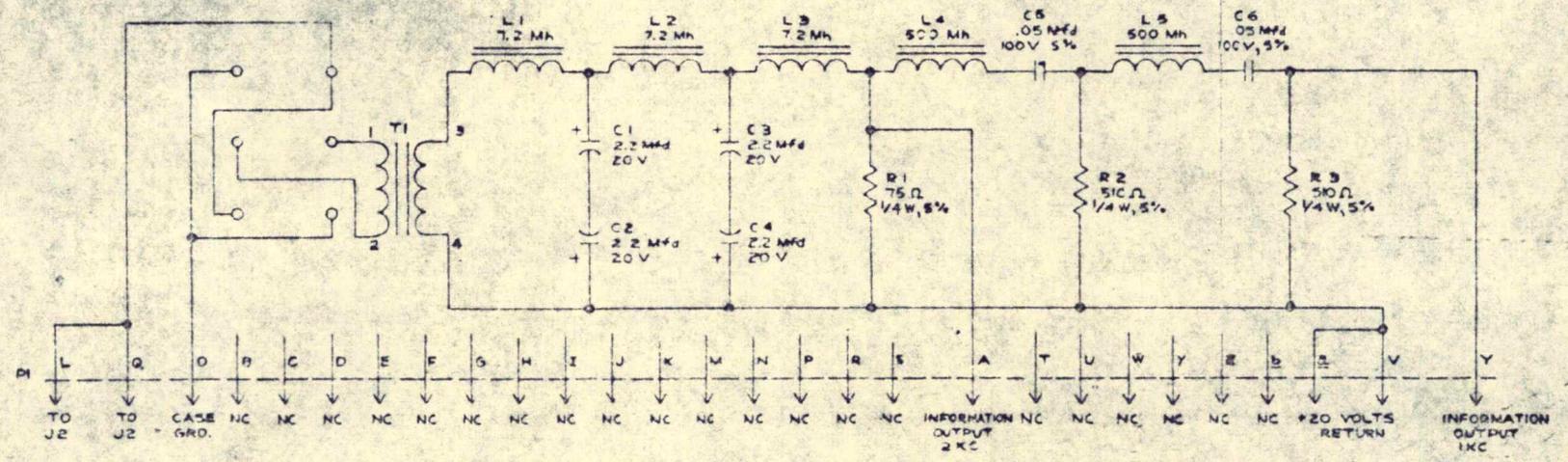


Figure 2-8. PSK Filter Schematic

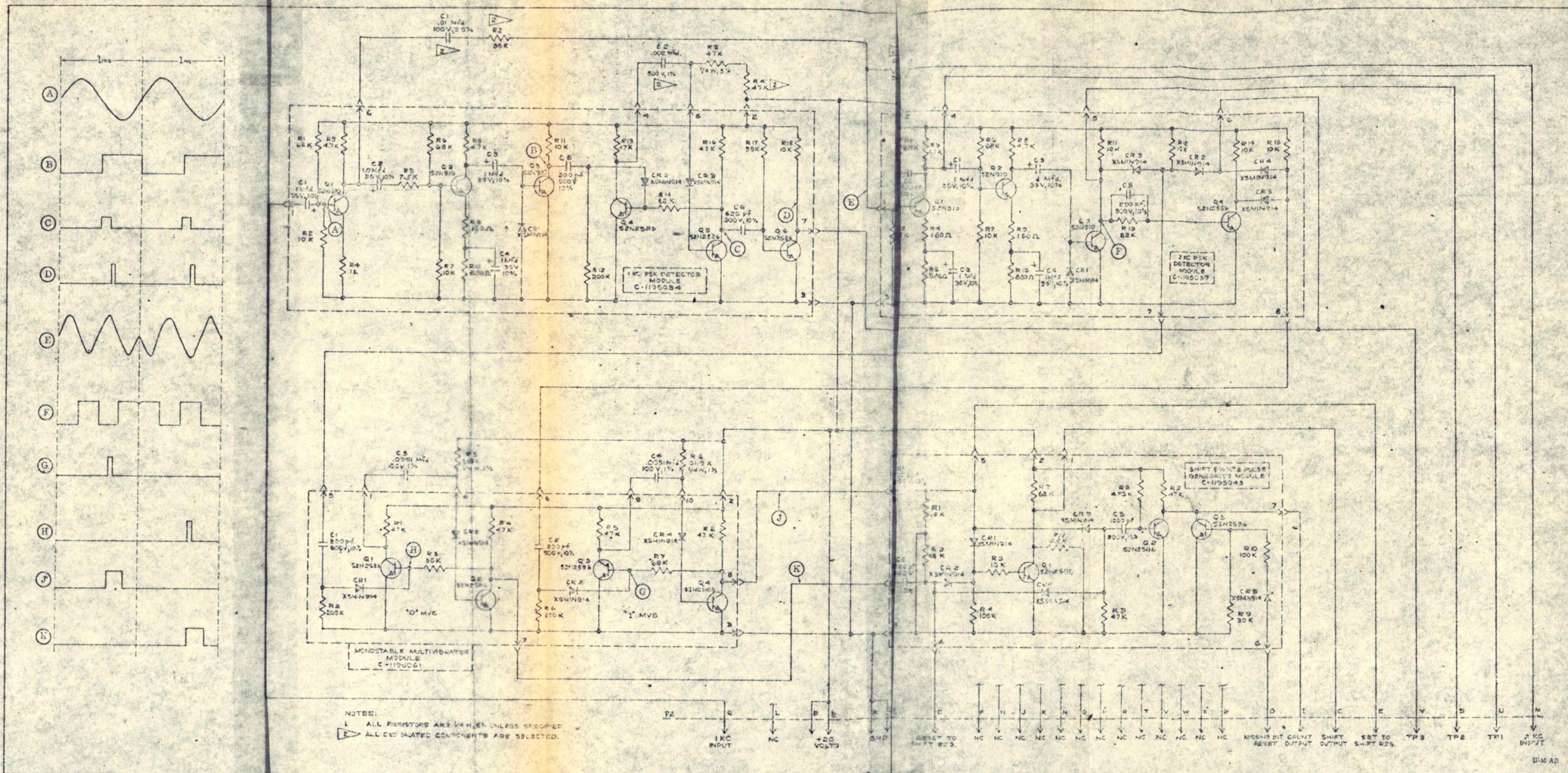


Figure 2-9. PSK Detector Schematic

The width of the pulse from the MVB is determined by the charging time constant of C2. (See waveform (C)). The positive pulse from the MVB is differentiated and the negative edge turns OFF Q6(034) yielding a narrow positive "sampling pulse" at the collector (waveform (D)).

The addition of the 180° phase shifted 1 kHz signal to the modulated 2 kHz signal produces a relatively clean 2 kHz signal at the base of Q1(037). The 2 kHz signal at the base of Q1(037) is shaped through 2 stages of amplification, Q1(037) and Q2(037), and is then clipped and shaped by CR1(037) and Q3(037). (See waveforms (E) and (F)). Diodes CR2(037) and CR3(037) form a 2-input AND gate which has an output only when the cathodes of both diodes are high. The input to diode CR3(037) of the AND gate is from the clipped 2 kHz at the collector of Q3(037) and the input to CR2(037) is the shaped 1 kHz sampling pulse from the collector of Q6(034). The output of this AND gate (AND1, Figure 2-5) shown in waveform (H) Figure 2-9, triggers a 200-microsecond MVB, Q1(061) and Q2(061), to produce the "0" sub-bit output, waveform (J). Diodes CR4(034) and CR5(034) form a second AND gate (AND2, Figure 2-5) whose inputs are the shaped 1 kHz sampling pulse at the collector of Q6(034) (Figure 2-9) and the inverted 2 kHz of Q4(034). The output of this AND gate, waveform (G), drives a 200-microsecond MVB, Q3(061) and Q4(061), to produce the "1" sub-bit output, waveform (J). Note that both AND gates cannot be on at the same time. The output from the "1" MVB is differentiated by C1(043), and the output from the "0" MVB is differentiated by C2(043). The differentiated signals are applied to the set input and the reset input respectively of the 5-bit shift register.

Transistor Q1(043) and diodes CR1(043) and CR2(043) form an OR gate, (OR1, Figure 2-5) whose output is the shift pulse for the 5-bit shift register at the sub-bit rate. The output of the gate is at B+ until either CR1(043) or CR2(043), Figure 2-9, is forward biased. The positive pulses produced by differentiating action of C1(043) or C2(043) drive the collector of Q1(043) to ground providing a negative shift pulse. Diodes CR3(043), CR4(043), and Q2(043) form an OR gate (OR2, Figure 2-5) which is the count pulse to the 5-bit counter. The transistor is biased ON by R6(043), Figure 2-9, until a negative pulse from the differentiators C1(043) and C2(043) to CR3(043) or CR4(043) reverse biases Q2(043), allowing the collector to approach B+ for the duration of the negative pulse. Transistor Q3(043) forms an AND gate (AND3, Figure 2-5) with the output of Q2(043), Figure 2-9,

to inhibit the count output pulse until the missing bit detector determines the start of the Command Message.

### 5-Bit Counter and Shift Register

The schematic and waveforms of the 5-bit counter and shift register card is shown in Figure 2-10. A description of the operation of the card follows. When the correct Command Message is being received, the sub-bit "1's" and "0's" are written into the 5-bit shift register (module 116). The trailing edge (negative) of the sub-bit pulse ("1" or "0") is coupled through CR1(116) or CR2(116) to reverse bias the appropriate side of the shift register stage to produce a "1" or "0" as required, see waveforms (A) and (B). The shift signal is applied as shown in waveform (C), and occurs at the positive edge of the "1" or "0" sub-bit pulse.

The negative edge of the "1" or "0" sub-bit pulse is used to write in the required data. Figure 2-10 illustrates the operation and timing of the shift register with a sample sub-bit pulse train of 01011. The set output waveform of the first stage of the 5-bit shift register with a sub-bit input of 01011 is shown as waveform (E). Each set and reset output (e.g. 2<sup>0</sup>, 2<sup>4</sup>) is routed to the code plug J4. There are 10 outputs from the shift register, 2 from each stage. The code plug is prewired and determines the "X" code, "0" code, and "1" code, by 5 jumpers for each code to 3 sets of 5 diodes. There are, therefore 32 possible combinations (2<sup>5</sup>) for each code. The 5-bit counter provides a positive enable pulse to the "X," "1" and "0" code gates. This counter consists of 3 bistable multivibrators (flip-flops) in a counter arrangement. The input to the counter from the PSK detector (P2-1) is shown as waveform (D). The counter triggers on the negative edge of the waveform and counts in the following manner.

	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>
Reset	0	0	0
Bit 1	0	0	1
Bit 2	0	1	0
Bit 3	0	1	1
Bit 4	1	1	1
Bit 5	0	0	0

The 5-bit counter counts normally until a count of 4, at which time the positive going pulse from the set output of the 2<sup>2</sup> stage is coupled by C4(049), to set

the first 2 stages of the counter through CR1(049) and CR2(049). The positive reset output from the 2<sup>2</sup> stage is the fifth count output to the code gates (see waveform (F)). The counter is ready to count the next set of 5 sub-bits and does not require a reset pulse.

The 3-bit counter (module 038) is 2 capacitively coupled flip-flops identical to the first 2 stages of the 5-bit counter. The function of the 3-bit counter is to count the occurrences of the "X" bit code pulses. At the second "X" code pulse the counter provides an output to reset the system thereby preparing for Command Message decoding. The third count enables the "0" and "1" inputs to the 32-bit shift register.

The operation of the remaining circuitry on the 5-bit counter and shift register card will be described with the explanation of the missing bit detector card.

#### Missing Bit Detector

Figure 2-11 shows a schematic of the missing bit detector card. The missing bit input pulse (P4-J) is amplified by Q4(064) and differentiated by C3(064). The positive trailing edge of the pulse turns ON Q3(064) driving the collector to ground and triggering the bistable multivibrator Q1(064) and Q2(064). The set and reset outputs of the flip-flop are coupled to 2-monostable MVB's (module 061). The MVB's will alternately trigger as the flip-flop is set and reset. Each multivibrator output pulse width is set to 5.4 milliseconds. This is a slightly longer period than the pulse repetition time interval (5.0 milliseconds). The outputs from the collector Q2(061) and the collector Q4(061) of the monostables are coupled to an OR gate (OR5, Figure 2-5) consisting of CR1(067), CR2(067) and Q1(067), Figure 2-11. The collector of Q1(067) is driven to ground by the positive output pulse from the monostables. In normal operation, the collector is held to ground, as it always has at least 1 input. The first "X" bit detected therefore starts the missing-bit clock consisting of the above mentioned flip-flop, MVB's and the OR gate, Q1(067).

The output of the missing-bit clock, Q1(067), is used to drive several other gates. The first of these is the OR gate (OR6, Figure 2-5) consisting of CR2(055), CR3(055) and Q2(055), Figure 2-11. The other input to the OR gate is the fifth count input from the 5-bit counter. If either of the diodes CR2(055) or CR3(055) is forward biased by a positive voltage, the collector of Q2(055) is grounded enabling an "X" bit

count. Therefore, the "X" bit count pulse from the collector of Q1(055) is present when (1) either the output of the missing bit OR gate, Q1(067) (OR5, Figure 2-5), or the fifth count input pulse are positive, and (2) the output of the "X" code gate is at a low voltage, (junction of the 150K(055) resistor and CR1(055), Figure 2-11). Other conditions at the first "X" bit are: (1) Q3(055) is OFF because the missing-bit clock is not running, i. e. there is a low voltage at the base of Q3(055), and (2) Q4(055) is conducting because of the bias voltage formed by R11(055), CR4(055) and R8(055). When CR4(055) is prevented from conducting by the positive "X" bit pulse from C1(055), Q4(055) ceases conduction causing a negative pulse at the collector. This pulse is used to reset the 5-bit counter. Thereafter, as long as either missing-bit monostable MVB is at a high voltage, Q3(055) is biased ON, hence biasing Q4(055) ON by the voltage across R11(055) and preventing any further reset pulses to the 5-bit counter. In summation the first "X" bit starts the missing-bit clock providing a positive voltage on the base of Q3(055) inhibiting further reset pulses to the 5-bit counter. This is possible because the 5-bit counter resets itself as discussed earlier.

The 3-bit counter is reset at the time of the 5-bit counter reset, i. e. by the first "X" bit. This is accomplished through an OR gate (OR7, Figure 2-5) consisting of CR3(067), CR4(067) and Q2(067), Figure 2-11. Transistor Q2(067) is normally ON, due to the bias from CR18(067) and R4(067). When the 5-bit (negative) reset pulse occurs at the collector of Q4(055), it is directly coupled to the emitter of Q2(067), thereby providing a reset to the 3-bit counter. The 3-bit counter can also be reset through C1(067) by the positive pulse from the missing bit detector. The pulse reverse biases CR18(067), turning OFF Q2(067) and producing a negative pulse. A positive pulse from the computer reset line will also reset the counter in a similar manner at the completion of data transfer to the LVDA.

The "1" code gate is composed of diodes CR5(067) through CR10(067), Q3(067) and Q4(067). The fifth count input pulse turns ON Q4(067) allowing the AND gate, CR5(067) through CR9(067), to control Q3(067). The collector of Q3(067) is at ground at all times except when all anodes of the diodes (AND6, Figure 2-5) are at a low voltage and this occurs precisely when the correct "1" code is written into the 5-bit shift register. At this time Q3(067), Figure 2-11, turns OFF, providing a positive "1" data pulse. Therefore a "1" is generated if the correct code is written into the 5-bit shift register and if the pulse

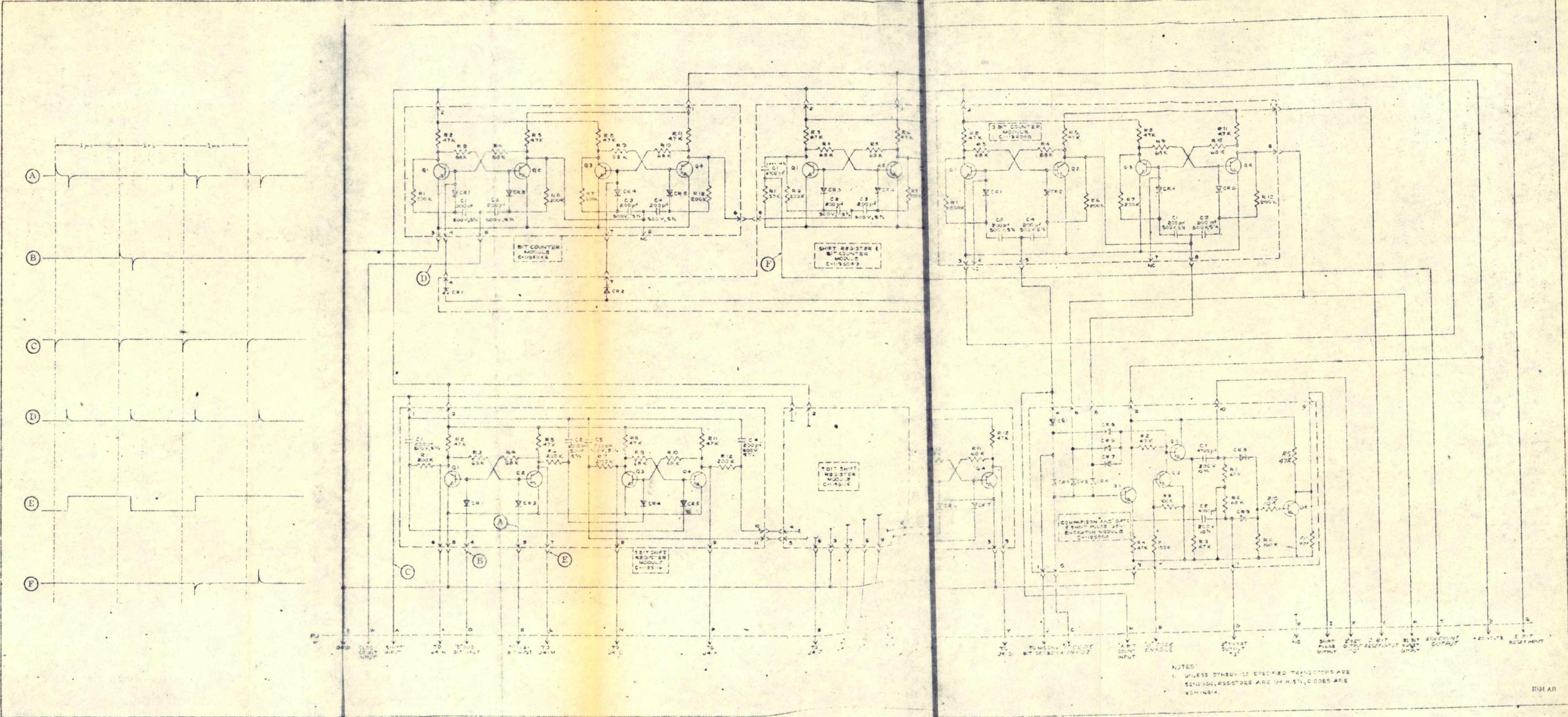


Figure 2-10. 5-Bit Counter and Shift Register Schematic

NOTES:  
1. UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE 52N100, RESISTORS ARE 1/4 W, 5%, DIODES ARE V51N1014.

ISM AB

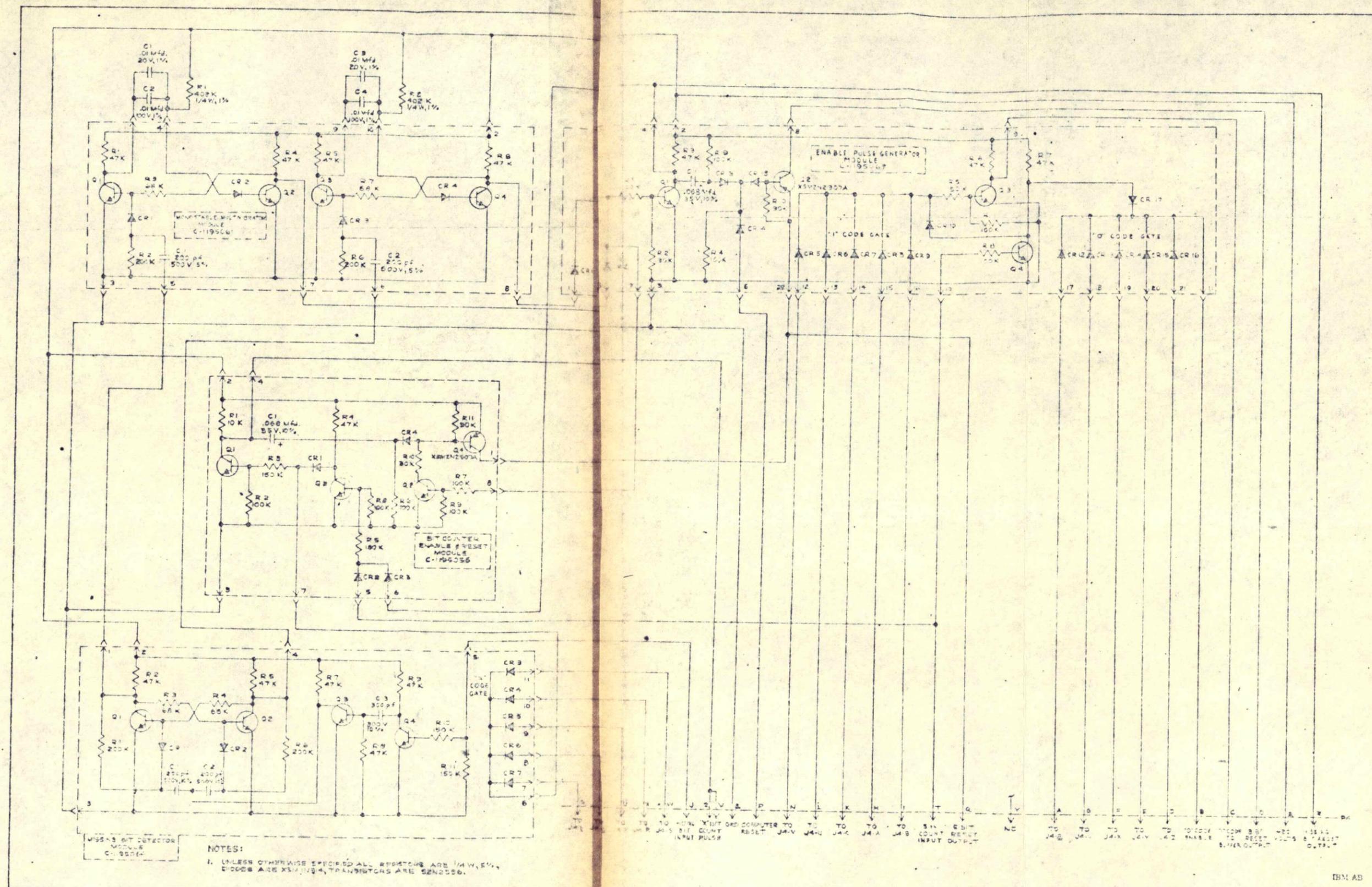


Figure 2-11. Missing Bit Detector Schematic

count from the 5-bit counter is present. Q4(067) also enables the "0" code gate to provide a "0" code enable to module (058) of Figure 2-10.

To complete the discussion of the 5-bit counter and shift register, the circuitry of Figure 2-10 provides the shift pulse, set input, and reset input to the 32-bit shift register. The operation of the circuitry follows:

- After the third "X" bit count pulse the 3-bit counter is filled with "1's" applying a positive voltage on the cathodes of diodes CR3(058), CR4(058), CR6(058) and CR7(058).
- At this time emitter follower Q3(058) will conduct if Q2(058) is non-conducting, i. e. a "0" code is present at the base of Q2(058). Therefore, when Q3(058) conducts, the positive pulse produced is differentiated by C1(058) and the negative portion of the pulse is used to set a "0" into the first stage of the 32-bit shift register. At all other times Q2(058) is conducting thereby providing insufficient base bias for Q3(058).
- Emitter follower Q1(058) will conduct if the "1" code enable is present. The positive pulse is differentiated and the resulting negative pulse is used to set a "1" into the 32-bit shift register. At all other times, Q1(058) is non-conducting.
- The differentiated output pulses from the "1" and "0" gates are applied to an OR gate in which the positive pulses turn ON Q4(058) providing a negative shift pulse for the 32-bit shift register. (Gate OR4 in Figure 2-5).
- The positive pulse generated when a "1" code is present is coupled through CR2(058), Figure 2-10, and the positive pulse generated when a "0" code is present are coupled through CR5(058) to drive the missing-bit clock. (The above pulses are inputs to OR gate OR1 of Figure 2-5).

#### Shift Out and 32-Bit Counter

The schematic and waveforms of the shift out and 32-bit counter is shown in Figure 2-12. The second "X" bit produces a positive pulse in the 2<sup>1</sup> stage of the 3-bit counter (P3-H, Figure 2-10) which is coupled to P5-M of Figure 2-12. This positive pulse is used to reset the 32-bit counter, the 32-bit

shift register, and the output flip-flop. Referring to Figure 2-12, the positive pulse is coupled through C6(082) which forward biases Q4(082). The positive pulse thus produced at the emitter of Q4(082) is coupled through C1(082) to reverse bias Q2(082), producing a negative pulse at the collector thus resetting the 32-bit counter. The positive pulse at the emitter of Q4(082) is also coupled to CR1(082) through C2(082) to reset the output flip-flop, Q3(082) and Q3(076) (waveform H). At the completion of data transfer to LVDA the output flip-flop is again reset by a positive pulse through C4(082) and CR2(082) from the computer reset monostable. (Hence, CR1(082) and CR2(082) make up the OR gate OR9, in Figure 2-5.)

The positive pulse at the emitter of Q4(082), Figure 2-12, is used to drive another OR gate which resets the 32-bit shift register by reverse biasing Q1(082) through C3(082) and CR3(082) (waveform K). The other input to this OR gate is through C5(082) and CR4(082) to reset the 32-bit shift register at completion of data transfer. (The above OR gate is OR8 of Figure 2-5.)

The output of the 32-bit counter, triggers a monostable multivibrator at a total of 32 shift pulses (refer to the waveform C of Figure 2-12). This positive pulse from the collector of Q4(079) is differentiated by C1(076) and the resulting negative pulse reverse biases Q1(076). If the address verify buss from the 32-bit shift register is at a low voltage, then Q2(076) is OFF and a positive voltage is developed across R5(076). This positive voltage is routed to the address verify monostable multivibrator producing an address verify signal to telemetry waveform E. The positive pulse at the collector of Q1(076) is differentiated by C2(076) and sets the output flip-flop (waveform D). The set output is from the collector of Q3(082) and is developed across the collector load resistor R6(076) (waveform J). When Q3(082) is OFF, Q4(076) is forward biased and drawing its collector current through R12(076) and R13(076). The voltage dropped across R13(076) forward biases Q5(076) providing 28 volts gated to the output buffers.

#### 32 Bit Shift Register

The first 2 stages of the 32-bit shift register are located on the shift out and 32-bit counter card, Figure 2-12. The remaining 30 stages are shown in Figures 2-13, 2-14, and 2-15. The 32-data bits are written into the shift register as required. Figure 2-13 shows 4 diodes CR1 through CR4 (on the printed

circuit card, pin G) of the 14 that make up the address verify buss. The diodes may be connected to either the set or the reset side of the shift register stage as required by the code desired. The output of the verify buss is ANDed with the output of the 32-bit counter and the resultant pulse differentiated to trigger the 2-redundant address verify monostable multivibrators (Figure 2-16). The address verify outputs are buffered and routed to telemetry.

Upon completion of data transfer to the LVDA, a reset pulse is generated by the LVDA and sent to the Decoder. This pulse is differentiated and the positive portion used to trigger the 2-redundant computer return monostable multivibrators (Figure 2-16). This computer return pulse is buffered by the circuitry of Figure 2-17 and routed to telemetry. This pulse is also used to reset the 32-bit shift register (through OR8 of Figure 2-5).

The 18 data-output buffers to the LVDA are shown in Figures 2-13, 2-14, and 2-15. These are required to produce the "1" level of +28 volts and the "0" level of 0 volts.

In Figure 2-13, 6 of the data output-buffer stages are shown. Assuming the data-bit output is a "1", the positive voltage at the set output of the shift register stage forward biases Q1(070), allowing the voltage drop across R2(070) to forward bias Q2(070). The conduction of Q2(070) makes available

a "1" (+28V) to the LVDA. The +28 volts supplied at the emitter of Q2(070) is switched by the output flip-flop as described above. If the data bit is a "0" then Q1(070) and Q2(070) are non-conducting, and the output is zero volts.

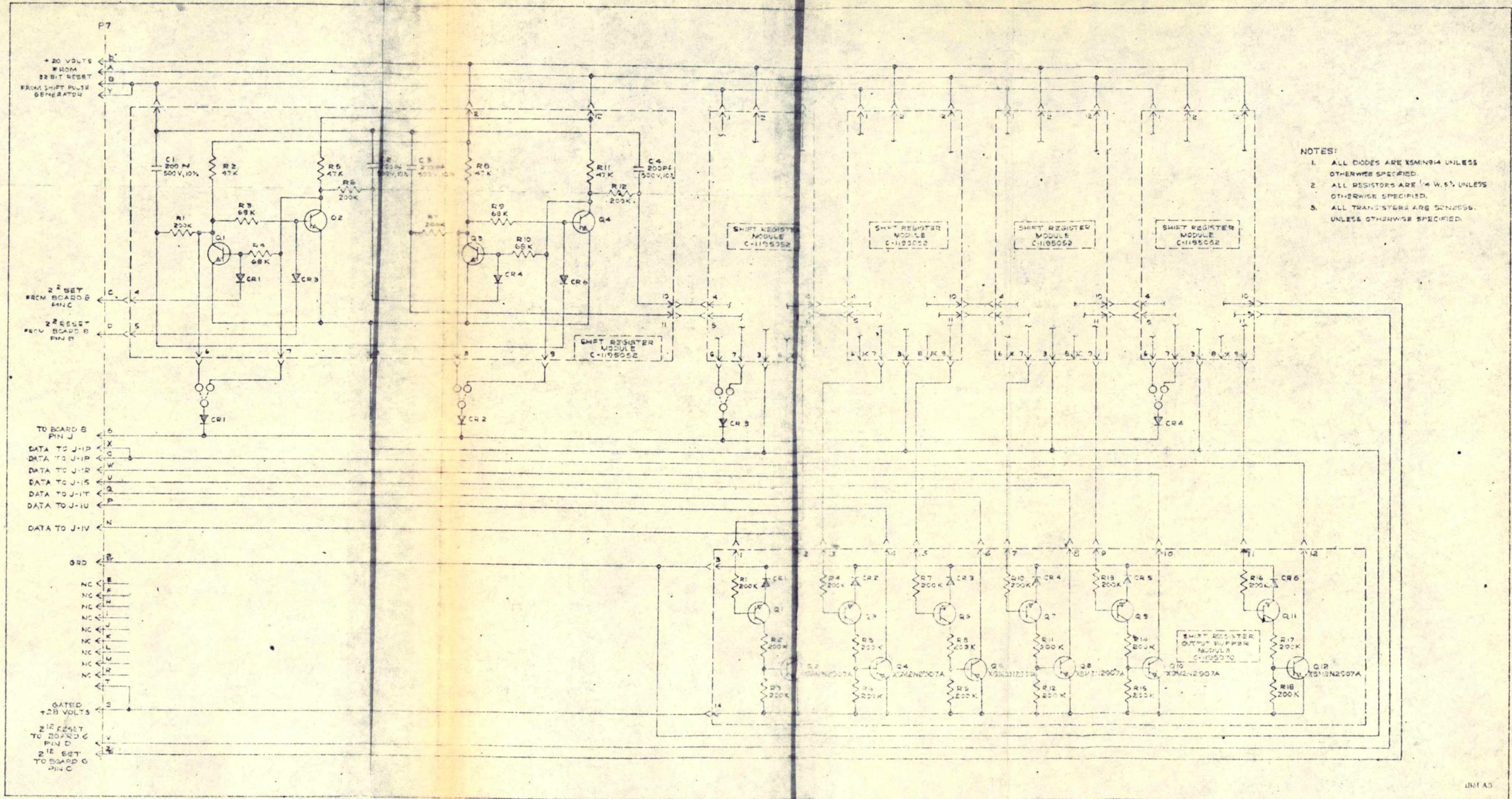
#### Telemetry Buffer

The telemetry buffer circuitry of Figure 2-17 is required to provide the required 5 volt pulses to telemetry. The pulse from the monostable multivibrators of Figure 2-16 are used to drive the buffers of Figure 2-17. Since the operation of the telemetry buffer circuits are similar only 1 buffer will be described. A negative pulse from the address verify monostable MVB turns OFF Q1(073) of Figure 2-17. The collector of Q1(073) therefore approaches B+ providing a positive base bias for Q2(073). As Q2(073) turns ON, a voltage is developed by this emitter follower across its emitter resistor R3(073). This positive pulse is coupled through R4(073) to the telemetry input.

#### Power Supply

The power supply for the Decoder is shown in Figure 2-17. The diode CR3 is provided to protect the supply from reverse polarity at the input terminals. The power supply provides a filtered +28 volts for the output-buffer amplifiers and provides the regulated +20 volts to the electronics of the Decoder.

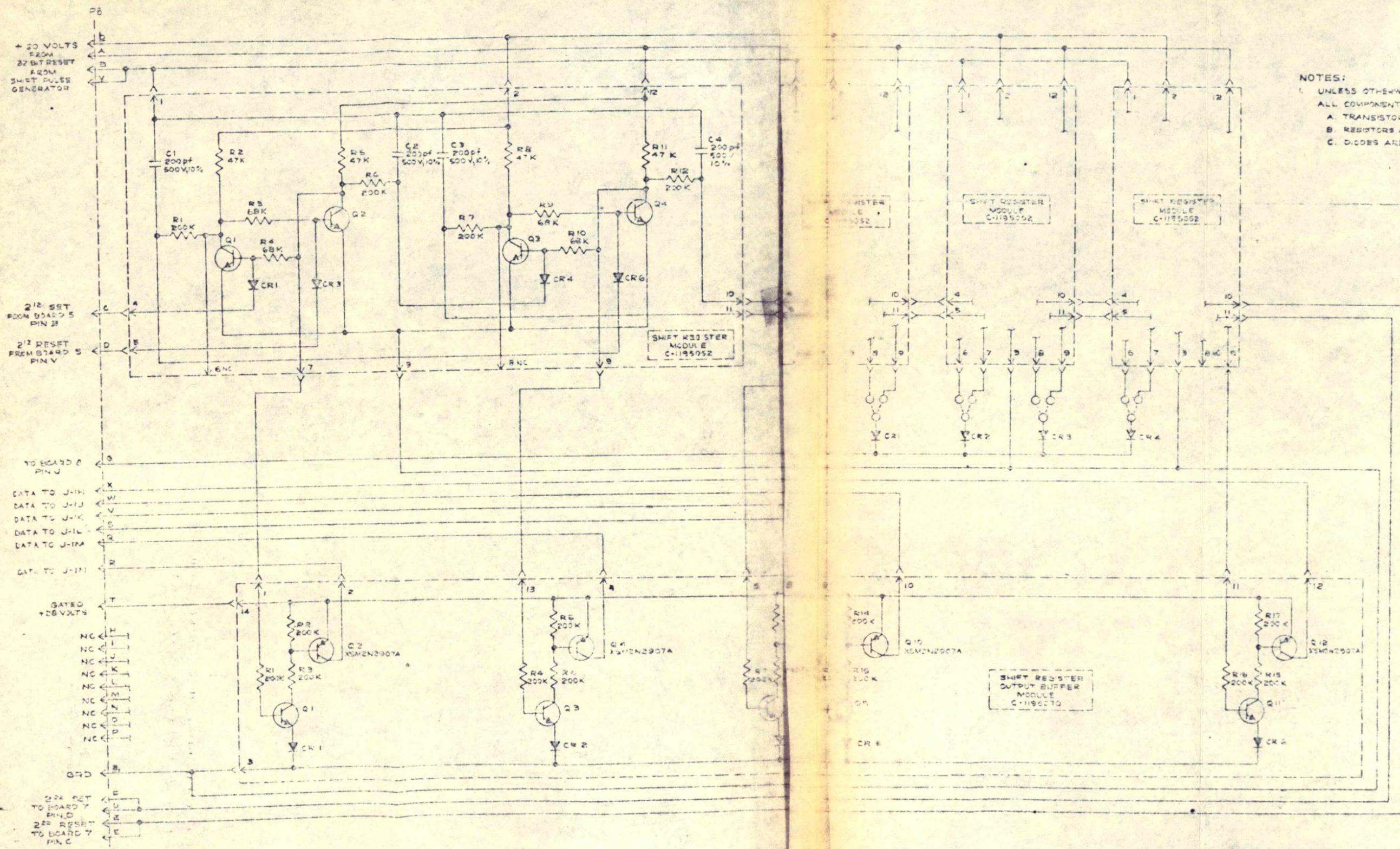




- NOTES:
1. ALL DIODES ARE XSM1914 UNLESS OTHERWISE SPECIFIED.
  2. ALL RESISTORS ARE 1/4 W. 5% UNLESS OTHERWISE SPECIFIED.
  3. ALL TRANSISTORS ARE 50N2556 UNLESS OTHERWISE SPECIFIED.

Figure 2-13. Shift Register "A" Schematic

IBM A3



- NOTES:  
 1. UNLESS OTHERWISE SPECIFIED  
 ALL COMPONENTS ARE:  
 A. TRANSISTORS ARE 52N2906.  
 B. RESISTORS ARE 1/4W, 5%  
 C. DIODES ARE 5M1N914.

Figure 2-14. Shift Register "B" Schematic

IBM AR

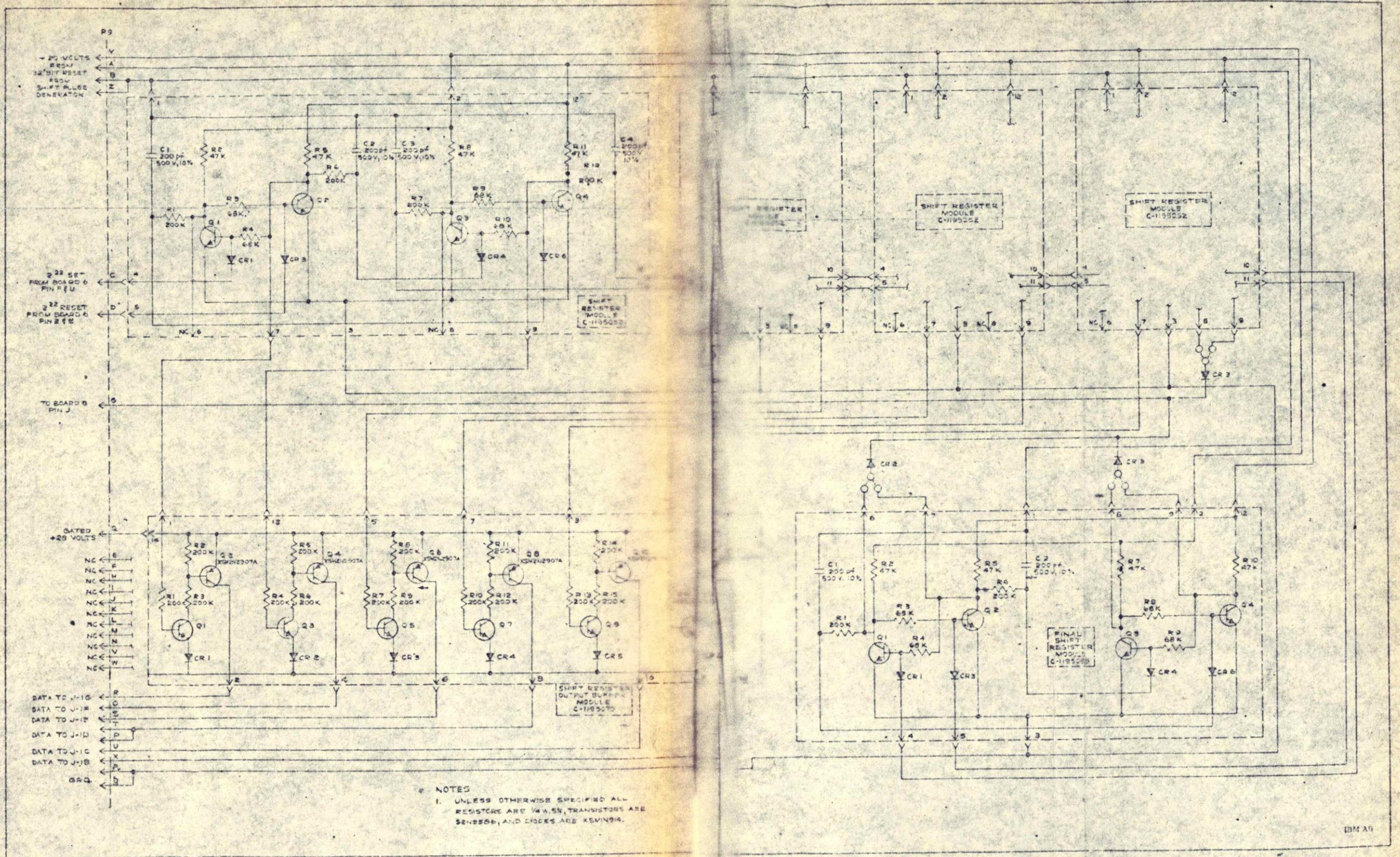
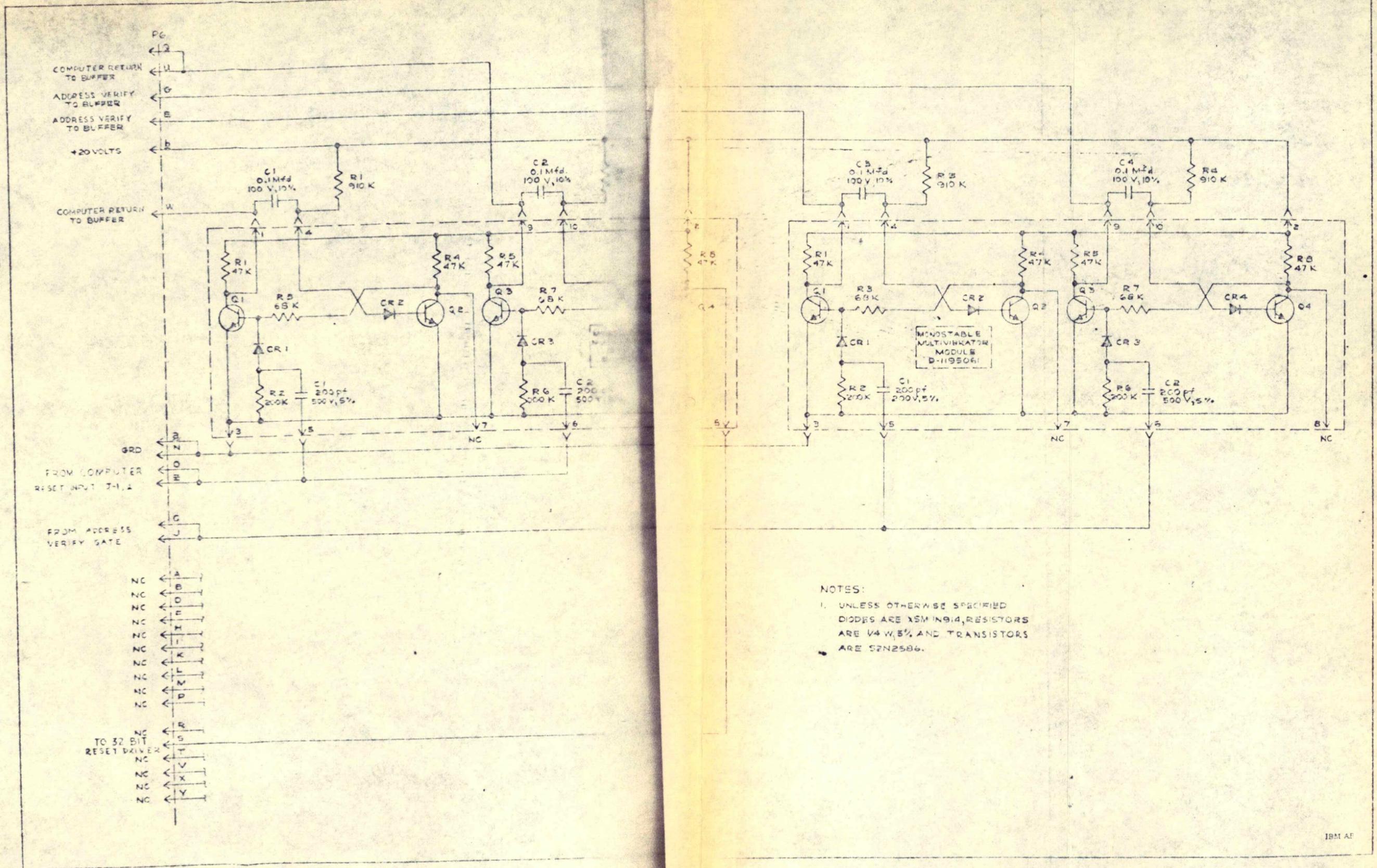


Figure 2-15. Shift Register "C" Schematic

IDM A9



NOTES:  
1. UNLESS OTHERWISE SPECIFIED  
DIODES ARE XSM1N914, RESISTORS  
ARE 1/4 W, 5%, AND TRANSISTORS  
ARE 2N2586.

Figure 2-16: Monostable Multivibrator Schematic

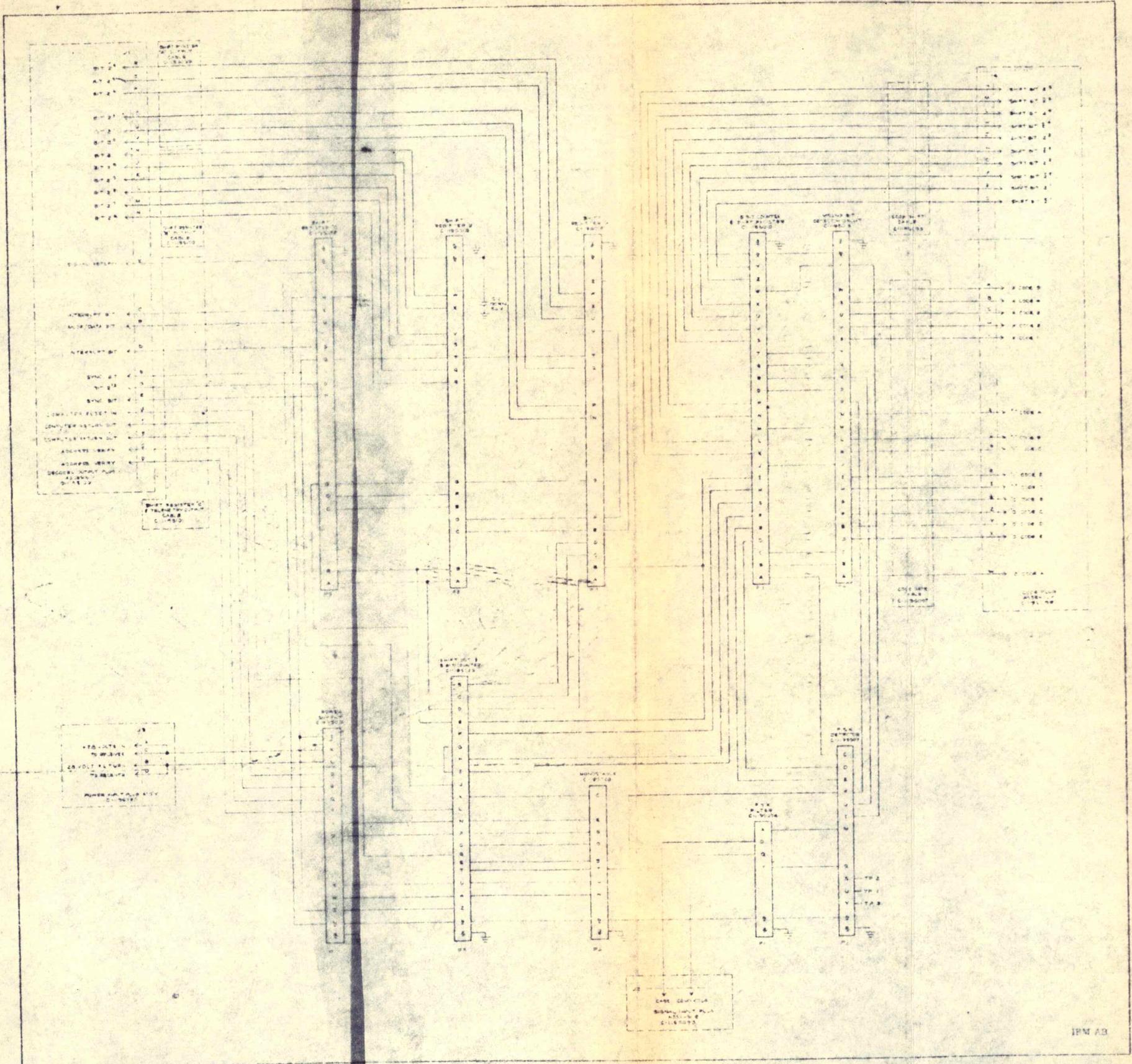
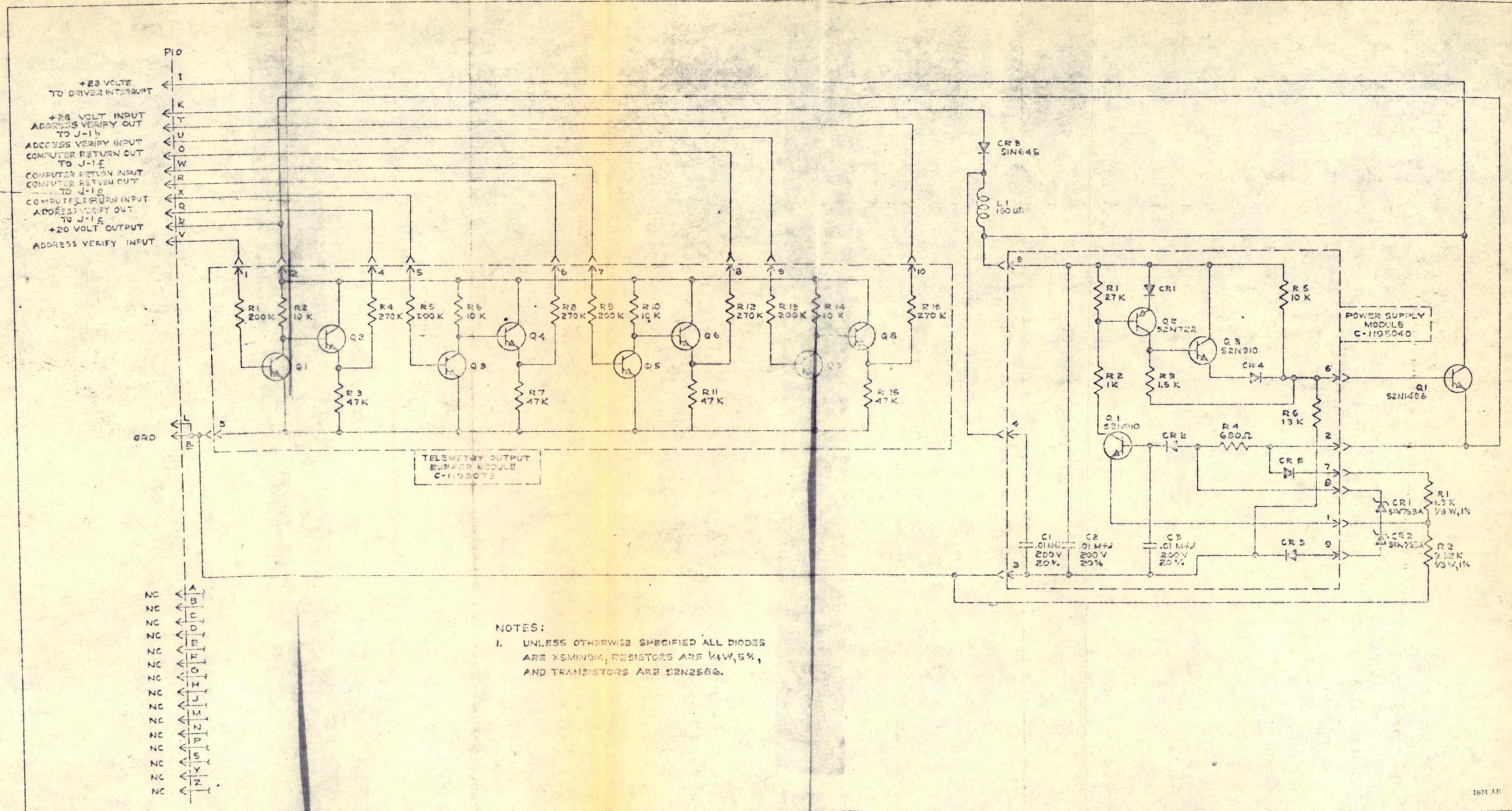


Figure 2-18. Motherboard Interconnection Schematic



NOTES:  
1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE XSMINDH, RESISTORS ARE 1/4W, 5%, AND TRANSISTORS ARE 52N258G.

Figure 2-17. Power Supply Schematic

## SECTION III

# PREPARATION FOR USE AND SHIPMENT

### 3-1 PREPARATION FOR USE

The packaged Decoder shall be opened in the following manner:

- a. Slit tape on outer carton.
- b. Cut barrier bag immediately below seal.
- c. Check humidity indicator (see following paragraph).
- d. Slit tape on inner carton.
- e. Lift out top cushioning pad.
- f. Remove component.
- g. Remove dust cover from connector.
- h. Visually inspect Decoder for physical damage and corrosion.
- i. Replace dust cover on connector.

The humidity indicator has three blue indicators graduated to indicate thirty, forty, and fifty percent humidity. These indicators will turn pink when their respective percent of humidity has been reached. A visual inspection for corrosion should always be made immediately after unpacking a Decoder. If the fifty percent indicator is pink, it is recommended the Decoder be returned to the laboratory for inspection and testing.

### 3-2 PREPARATION FOR SHIPMENT

#### 3-3 PACKAGING

The Decoder shall be packaged in accordance with Method IIb or Method III of Military Specification MIL-P-116 and marked in accordance with Military Standard MIL-STD-129. Determination of whether to use Method IIb or Method III is dependent upon the degree of protection required. Method III is to be used if the Decoder is to be shipped between plants at the Huntsville facility and there will be no storage required. Method IIb is to be used in all other cases. Refer to Figure 3-1 for packaging instructions.

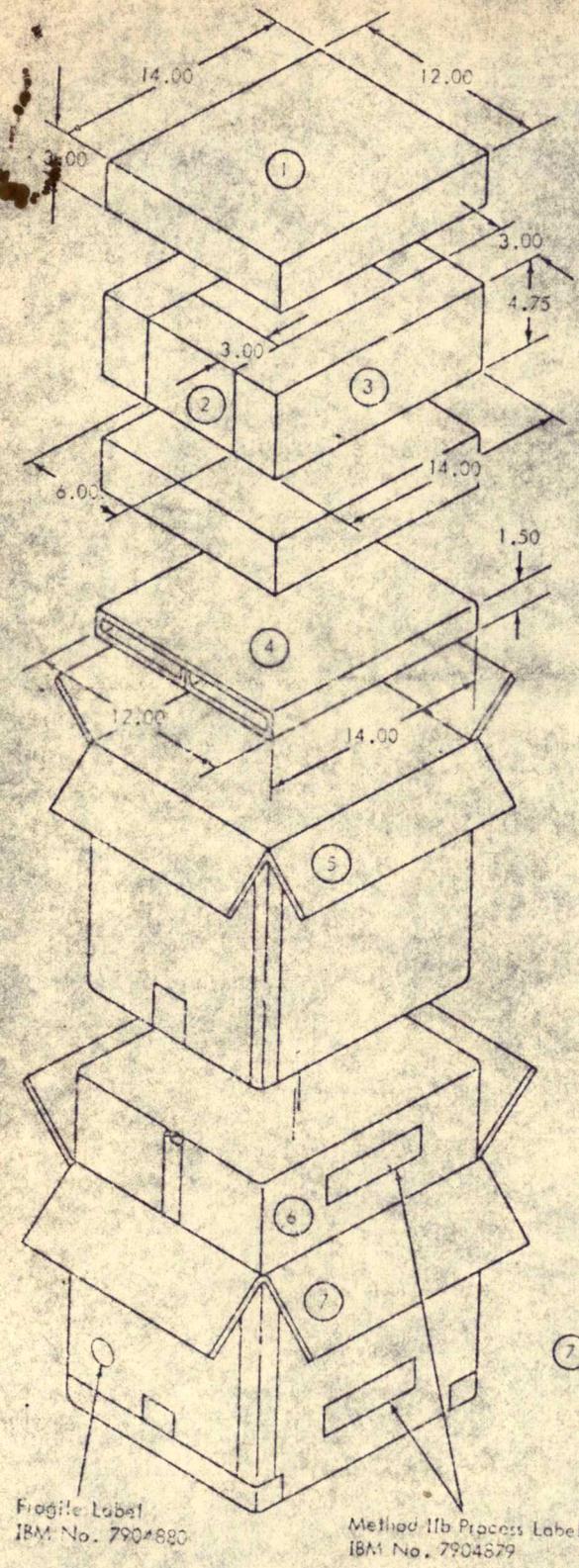
#### 3-4 MARKING

Markings containing the following information shall be applied on the inner and outer cartons.

MSFC Number  
Item Description  
Quantity  
Contract Number  
Level of Preservation and Date  
Serial Number

A Method IIb Process Label (IBM No. 7904879) shall be applied to the top of the water-vaporproof barrier bag and to the outer carton. Make certain the packaging date is recorded on these labels.

A Fragile Label (IBM No. 7904880) shall be applied to both ends of the outer carton.



Method IIb: Use items ① thru ⑦ .

Method III: Use items ① thru ⑤ . Do not include the desiccant or humidity indicator.

Items ① , ② , and ③ (2 each) to be fabricated from Polyurethane foam cushioning, 4 lb/cu ft. density, MIL-P-26514, Type 1, Class 2. IBM No. 7904R11-5

The Decoder will be surrounded by the cushioning as shown.

④ Pad  
Material: 275 lb Test, A flute, corrugated fiberboard.  
Place three 8-unit bags of desiccant,  
Part No. 7905816-003 inside pad.

⑤ Carton  
Per PPP-B-636  
Type 1, Class 1  
Style: RCS  
Material: 275 lb test, A flute

Inside Dimensions:	
Length:	14.00 inches
Width:	12.00 inches
Depth:	12.25 inches

Inner carton tube closed with pressure sensitive tape and corners are to be blunted so as not to damage barrier bag, item ⑥ .

⑥ Water-vaporproof Barrier Bag  
Material: MIL-B-131G, Class I  
Style: Bag  
Dimensions: 28 inches high x 30 inches wide.

After inner carton has been inserted in barrier bag, place humidity indicator on top of inner carton. When barrier bag is sealed, the humidity indicator will be between inner carton and barrier bag. The barrier bag originally is heat sealed, however, when packaging a defective decoder, waterproof tape may be used.

After barrier bag has been inserted in outer carton, apply a Method IIb process label on top of the barrier bag. Record the packaging date on the label.

⑦ Carton  
Per PPP-B-636  
Type 1, Class 1  
Style: RCS  
Material: 275 lb test "A" flute  
IBM Stock No. 7904770

Inside Dimensions	
Length:	14.75 inches
Width:	12.75 inches
Depth:	13.50 inches

Outer Carton to be closed with 3-inch Kraft Tape.

Fragile Label  
IBM No. 7904880

Method IIb Process Label  
IBM No. 7904879

Figure 3-1. Packaging Instructions for IU Command Decoder