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GEORGE C. MARSHALL  
SPACE FLIGHT CENTER  
Huntsville, Alabama

## Worst-Case Circuit Analysis of the Switch Selector MOD II

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CLASSIFICATION AND CONTENT APPROVAL

F. A. Ford

PROGRAM OFFICE APPROVAL

C. R. Crebar

**IBM** Space Guidance Center, Huntsville, Alabama

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## ABSTRACT

This report presents the results of a worst-case circuit analysis considering single and multiple component failures, performed on the circuits of the Switch Selector Mod II, IBM Part No. 6101400, (50M67864). The analysis was performed for operating conditions over the temperature range of  $-25^{\circ}$  to  $+125^{\circ}$  C. The piece-part tolerances include initial purchase tolerance and aging based on a 10,000 hour end-of-life.

A statistical worst-case analysis was performed on the two principal circuits, the IP and IN switching circuits using a statistical analysis computer program, ASAP. A transient analysis was performed on the Automatic Reset Circuit, using a transient analysis computer program PREDICT.

A detailed description of the analysis and results, including worst-case variations and statistical distributions of the circuit parameters is given. It was found that the Switch Selector circuits will meet the electrical design requirements of IBM Specification No. 6009026 under worst-case conditions for any simplex component failure.



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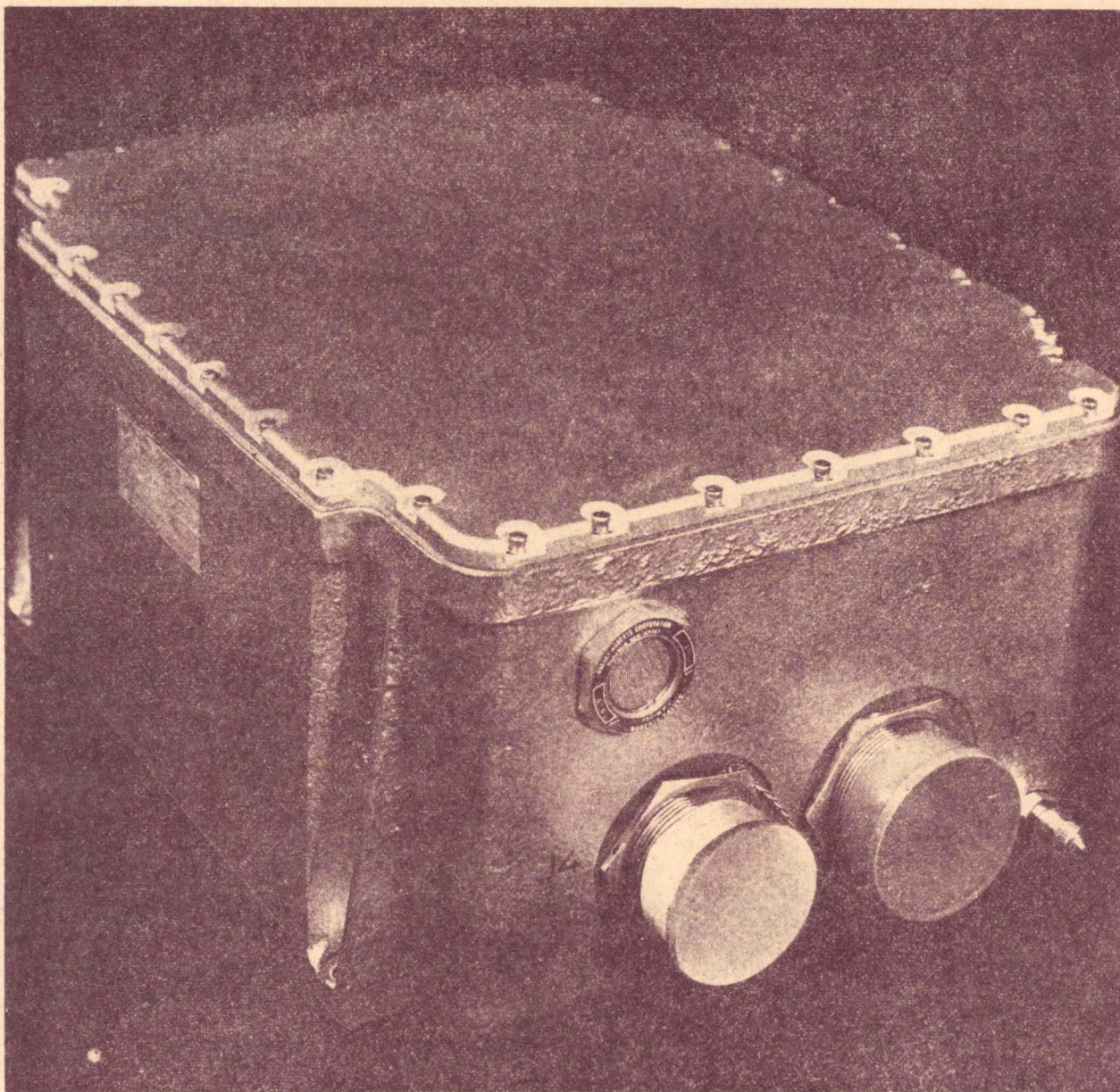
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Switch Selector Mod II



## SECTION 1

### INTRODUCTION

The purpose of this report is to present the results of the Switch Selector Mod II worst-case circuit analysis as required by the Switch Selector Mod II Statement of Work, Item 8B, page 5, under Contract NAS 8-14000, Attachment I, Modification No. 39. The analysis does not include the relay logic since this logic is straightforward and the only factor to be considered is reliability. A discussion of reliability is beyond the scope of this report.

The Switch Selector, IBM part No. 6101400, is used to decode an eight-bit binary word into one of 112 possible outputs and to switch power to that output for use in particular control mechanisms. The IP and IN switching circuits are the two principal circuits in the Switch Selector. The IP circuit is used as a driver to switch power for various functions within the Switch Selector and to switch power at each of the 112 outputs. The IN circuit is used with AND logic circuits to decode the eight-bit input word. With the exception of some relay logic, these circuits are the basic building blocks for the entire Switch Selector.

An IP switching circuit is a logic inverter using PNP switching transistors. Similarly, an IN switching circuit is a logic inverter using NPN transistors. The purpose of these circuits is to provide a low impedance path to a power source to complete a function, or conversely, a high impedance path to block the function. Thus, each circuit is called a switching circuit since it is a controlled switch.

There are 24 relays in the Switch Selector; 19 latching type and 5 conventional. The latching relays require a reset pulse to return the relays to the normal position. Eight of these relays, verify relays, are set or reset depending on the position of eight other relays, the Bit Register relays. The eight Bit Register relays and the three Stage Select relays are reset by a pulse which is generated by an Automatic Reset Circuit contained in the Switch Selector. There is an externally controlled forced reset pulse that will reset the relays in the event a component failure causes an incorrect verification and the complement word must be used. This forced reset pulse will also perform the reset function in the event the Automatic Reset Circuit fails.

The IP and IN switching circuits were designed using a quad-redundant principle which permits each circuit to have a number of component failures with negligible effects on practical circuit operation. One hundred and thirty-four circuits of the Switch Selector are of the IP type. One hundred and twelve of these circuits are used as output drivers. The remaining 22 are modified and are used to switch power within the Switch Selector. Twenty-five IN circuits with associated AND logic circuitry are also contained in the Switch Selector. Each IN circuit which is "Flight Critical" has redundant AND circuits (that is, two AND circuits). These AND circuits are connected logically to permit each Switch Selector output to be turned on either by a given word



or the complement of that word, should any component or interface failures prevent normal insertion with the desired word. All of these factors contribute to the Switch Selector reliability, i.e., being able to operate normally with component failures. The IP and IN circuits are shown in Section 5 along with a detailed description of the dc analyses and circuit operations.

The overall objective of the analysis was to determine whether the Switch Selector would meet design specifications as depicted in the Switch Selector Specification, IBM No. 6009026, when subjected to worst-case end-of-life component tolerances, operating temperature extremes of  $-25^{\circ}$  to  $+125^{\circ}\text{C}$ , and the most detrimental component failure modes. To accomplish this objective, the analysis was performed in two parts: (1) dc steady-state worst-case analyses of the IP and IN circuits, (2) transient analysis of the Automatic Reset Circuit.

A second objective of the dc analysis was to determine by statistical analysis whether a circuit with a component failure could be detected by external testing such as measuring the output voltage with a given input and a given load. The failure modes analyzed were those considered to be most detrimental to circuit operation without causing complete circuit failure.

The Automatic Reset Circuit provides the pulse for the reset of the eight Bit Register latch-type relays, and the three Stage Select latch-type relays. The Automatic Reset Circuit, which uses three quad-redundant IP circuits, employs redundancy for all other components as well. The object of the analysis of this circuit was to determine if worst-case conditions of component tolerances, temperature extremes, and component failure modes would cause the reset pulse duration to be less than or greater than the allowable pulse width. The Automatic Reset Circuit is shown in Section 6 along with a detailed description of the analysis and circuit operation.

The Switch Selector performance is summarized using the results of each circuit analysis. It should be noted here that after the original analysis had been completed, various design changes were made. The changes were in the configuration and application of several IP circuits and in the addition of two IP circuits. This resulted in more stringent requirements on all IP circuits. Considering these new requirements, a worst-case analysis was performed on the modified IP circuit, utilizing as much as possible the previous analytical results. The changes and results will be discussed in the appropriate sections of the report.

The statistical worst-case dc analysis computer program, ASAP, is designed to perform a Monte Carlo statistical analysis on a set of equations which completely describe the circuit under consideration. The equations are solved repeatedly several thousand times using a random selection of component values for each solution, thereby producing a statistical distribution of the desired output parameters. Also the worst-case values of the desired output parameters are calculated using the same set of equations



and component parameters. The values and characteristics of all components are defined along with the specified tolerance giving a range of values from which the component parameters are selected for each solution. A general description of the ASAP computer program is given in Appendix IV-A.

The transient analysis computer program, PREDICT, is designed to compute the time dependent responses of a given circuit. All components have fixed values and worst-case conditions must be determined by the analyst. A general description of the PREDICT program is given in Appendix IV-B.



## SECTION 2

### CONCLUSIONS

Conclusions drawn from the Switch Selector worst-case studies are:

A. The Switch Selector will meet the electrical design requirements of IBM Specification No. 6009026 in its entirety under worst-case conditions for any simplex component failure.

B. The IP and IN inverter circuits will meet the Switch Selector requirements under absolute worst-case failure mode conditions.

C. All flight critical components have a steady-state power dissipation of less than 50 percent of rated power.

D. For both the IP and IN circuits, the variations in transistor parameters are the major factors in causing variations in saturation voltage drop.

E. The normal and failure mode statistical distributions of the saturation voltage drop for both the IP and IN circuits overlap in such a manner as to prevent any attempt to establish fixed acceptance criteria for circuit modules. Any such attempt would result in the acceptance of circuits which contained faults, and/or the rejection of good circuits. However, tests at the system level may possibly be established since a worst-case component failure will cause a significant change in circuit characteristics.

F. The Automatic Reset Circuit will generate a pulse capable of resetting the relays under worst-case failure mode conditions.

G. All power dissipation transients in the reset circuit are of a duration such that the average power dissipation is well below the rated power and no damage to circuit components will result.



## SECTION 3

### RESULTS

#### 3-1 IP AND IN CIRCUIT REQUIREMENTS

The eight-bit input word to the Switch Selector is decoded by diode logic circuits (AND circuits), IN inverter circuits, and IP inverter circuits. The block diagram of Figure 3-1 shows the typical interconnection of these circuits when a word has been decoded and any one of the 112 outputs is on. Each of the 112 outputs is provided by an identical combination of other identical circuits within the Switch Selector. The complete logic schematic, IBM Drawing No. 6101534, can be seen in Appendix III. The individual circuits are shown on this logic schematic and are described in Section 5 along with a detailed description of the analysis. A detailed description of the Switch Selector theory of operation is given in the Description Manual of the Saturn Switch Selector MOD II, IBM Document No. 65-529-0004.

When the analysis was first completed, IP circuits #5 and #6 (Figure 3-1) were not used and power was applied to IP circuits #3 and #4 by the read command relay as shown by the dotted line. IBM Specification No. 6009026 specifies that the Switch Selector must deliver up to 110 milliamperes output current at an output voltage not more than 3 volts below stage power. Stage power is nominally 28 volts dc with a tolerance of  $\pm 2$  volts.

The analysis was carried out for normal operation to determine the general characteristics of the circuits and for worst-case conditions of component values and failure modes at normal, high, and low temperatures.

Improvements in the design of the Switch Selector were then incorporated resulting in the addition of IP circuits #5 and #6 as shown in Figure 3-1. The read command relay was then used to control IP #5 and #6 rather than as shown by the dotted line. Also, a modified IP circuit was employed at several locations. The 112 output drivers represented by IP #1 were unchanged. The remaining 22 IP circuits were modified by removing four diodes. The circuit configurations and the analysis of each are discussed in detail in Section 5.

The addition of the two IP circuits placed more stringent requirements on the IP circuits. With the original design only two IP circuits were connected in series between stage power and the output. This allowed a maximum average of 1.5 volts drop per circuit. With the addition of another IP circuit in series, the maximum average voltage drop per circuit is decreased to one volt. However, the modification provided more base drive so that the requirements are easily met.

Because of these design changes, some of the test conditions used are not pertinent to the worst-case analysis but are included here to show typical characteristics and behavior of the circuits. Based on the original analysis, the modified IP circuit was analyzed for worst-case conditions only.



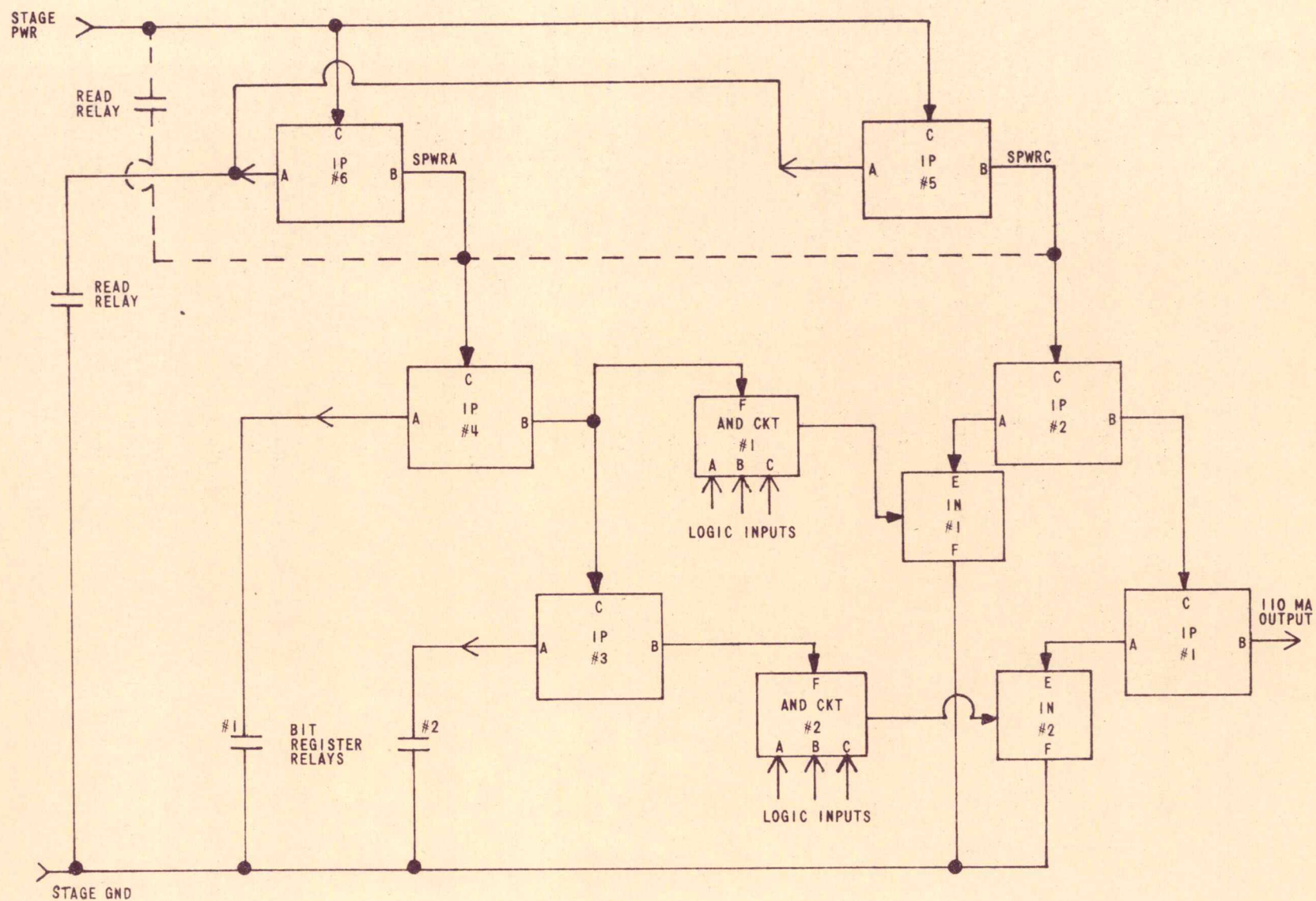


Figure 3-1. Typical Power Flow Diagram for Switch Selector Outputs



### 3-2 IP CIRCUIT RESULTS

The most important circuit parameter for the IP circuit is the saturation voltage drop across the circuit when driving the required load. Since the circuit is acting as a switch, it is desirable to have the saturation voltage as low as possible.

The output driver, IP circuit with all the diodes, was analyzed for normal operation at all three temperatures and for worst-case failure modes at all three temperatures. The worst-case input voltage was considered to be 24 volts and the load current was 110 milliamperes. The results of the worst-case and statistical analysis are tabulated in Table 3-1, showing the characteristics of the circuit. A component failure causing one side of the circuit to be inoperative caused only a small increase in the circuit saturation voltage drop even under worst-case conditions. The condition of one transistor being shorted was tested for the second objective, to detect failures. Therefore, this failure mode was simulated for only 28 volts input.

Nominal and maximum component power dissipation for steady-state operation is shown in Table 3-2. The only components operating near the rated power are the 7.5K ohm base resistors. However, the average power is less than 25 percent of rated power, since the maximum duty cycle is 25 percent for all but two IP circuits which perform a zero indicate function. These two circuits, which could have a 100 percent duty cycle are not flight critical. Also, the resistors are metal film resistors. It is not general design practice to derate metal film resistors below the rated power level because internally generated heat below the rated limit is not a contribution to premature end-of-life.

The statistical distribution of the saturation voltage drop for all cases shown in Table 3-1 can be seen in Appendix I.

Referring again to Figure 3-1, IP #2 has a load of the output current plus the base current required by IP #1. By studying Table 3-1, it can be seen that the worst-case failure mode and environmental conditions are one transistor open at low temperature and minimum input voltage as indicated by finding the maximum voltage drop for the constant load. Using these conditions, a worst-case analysis was performed to determine the limits of the IP circuit. The worst-case input voltage would be 24 volts minus the voltage drop on IN circuit #2, approximately 0.5 volts. The results are shown in Table 3-3. The load limit of the circuit for a particular input voltage can be noted by the rapid increase in the saturation voltage and the transistor power dissipation. The transistors are the only components in which the power dissipation exceeded those found in Table 3-2. Using the results shown in Table 3-3, along with the results for the IN circuit, it can be shown that the original Switch Selector design would easily meet the specification.



Table 3-1. IP Circuit Worst-Case Statistical Results

| Saturation Voltage (Volts) |         |         |                          |        |         | Temperature<br>Deg C | Operating<br>Mode                            |
|----------------------------|---------|---------|--------------------------|--------|---------|----------------------|----------------------------------------------|
| Worst-Case                 |         |         | 10,000 Cases Statistical |        |         |                      |                                              |
| Minimum                    | Nominal | Maximum | Mimimum                  | Mean   | Maximum |                      |                                              |
| 0.1603                     | 0.2991  | 0.4497  | 0.1928                   | 0.3022 | 0.4055  | +125                 | Normal Operation<br>Gated Input = 28V        |
| 0.1748                     | 0.3109  | 0.4688  | 0.2121                   | 0.3163 | 0.4184  | + 25                 |                                              |
| 0.1776                     | 0.3245  | 0.4833  | 0.2191                   | 0.3278 | 0.4323  | - 25                 |                                              |
| 0.1774                     | 0.3195  | 0.4732  | 0.2141                   | 0.3223 | 0.4247  | +125                 | Normal Operation<br>Gated Input = 24V        |
| 0.1916                     | 0.3315  | 0.4870  | 0.2325                   | 0.3363 | 0.4377  | + 25                 |                                              |
| 0.1953                     | 0.3446  | 0.5016  | 0.2400                   | 0.3475 | 0.4511  | - 25                 |                                              |
| 0.2553                     | 0.4043  | 0.5610  | 0.2795                   | 0.4060 | 0.5321  | +125                 | One Transistor Open<br>Gated Input = 28V     |
| 0.2720                     | 0.4241  | 0.5888  | 0.3000                   | 0.4267 | 0.5532  | + 25                 |                                              |
| 0.2863                     | 0.4420  | 0.6160  | 0.3187                   | 0.4455 | 0.5743  | - 25                 |                                              |
| 0.2776                     | 0.4249  | 0.5800  | 0.3006                   | 0.4267 | 0.5525  | +125                 | One Transistor Open<br>Gated Input = 24V     |
| 0.2942                     | 0.4446  | 0.6077  | 0.3211                   | 0.4472 | 0.5734  | + 25                 |                                              |
| 0.3084                     | 0.4625  | 0.7337  | 0.3397                   | 0.4697 | 0.6760  | - 25                 |                                              |
| 0.1126                     | 0.2044  | 0.3011  | 0.1294                   | 0.2038 | 0.2841  | +125*                | One Transistor Shorted<br>Gated Input = 28V. |
| 0.1213                     | 0.2117  | 0.3102  | 0.1345                   | 0.2135 | 0.2927  | + 25                 |                                              |
| 0.1229                     | 0.2236  | 0.3348  | 0.1451                   | 0.2233 | 0.3068  | - 25*                |                                              |

\*Approximately 5000 cases in statistical



Table 3-2. IP Circuit Component Power Dissipation

| Component           | Power Diss (mw) |     | Temp<br>Deg C | Operating Mode    |
|---------------------|-----------------|-----|---------------|-------------------|
|                     | Nom             | Max |               |                   |
| 7.5K Base Resistors | 95              | 105 | +125          | All Conditions    |
| R5 thru R8          | 90              | 100 | + 25          |                   |
|                     | 88              | 98  | - 25          |                   |
| 2K Bias Resistors   |                 |     | All           | All Conditions    |
| R1 thru R4          |                 | < 1 | Temps         |                   |
| IN645 Diodes        |                 | < 6 | All           | All Conditions    |
|                     |                 |     | Temps         |                   |
| 2N2907 Transistors  | 9.5             | 22  | +125          | Normal            |
| T1 thru T4          | 9.5             | 23  | + 25          |                   |
|                     | 10              | 27  | - 25          |                   |
| 2N2907 Transistors  |                 |     | All           | All Failure Modes |
| T1 thru T4          | 25              | 50  | Temps         |                   |

Maximum Rated Component Power Dissipation:

Resistors at all temperatures-----125mw

2N2907 transistor at +125-----172mw

2N2907 transistor at +25° or less-----400mw

IN645 diode at +125°-----200mw

IN645 diode at +25° or less-----600mw



Table 3-3. Normal IP Circuit Results  
With Open Failure at -25 °C

| Nominal Case            |                            |                   |                            | Maximum Worst-Case      |                            |                   |                            | Conditions             |                       |
|-------------------------|----------------------------|-------------------|----------------------------|-------------------------|----------------------------|-------------------|----------------------------|------------------------|-----------------------|
| Total Base Current (ma) | Saturation Voltage (Volts) | Load Current (ma) | Transistor Pwr. Diss. (mw) | Total Base Current (ma) | Saturation Voltage (Volts) | Load Current (ma) | Transistor Pwr. Diss. (mw) | Load Resistance (Ohms) | Input Voltage (Volts) |
| 13.6                    | 0.535                      | 153               | 43                         | 14.2                    | 1.41                       | 148               | 137                        | 180                    | 28                    |
| 13.6                    | 0.526                      | 148               | 41                         | 14.2                    | 0.989                      | 146               | 92                         | 185                    |                       |
| 13.6                    | 0.518                      | 145               | 39                         | 14.2                    | 0.818                      | 143               | 63                         | 190                    |                       |
| 13.6                    | 0.510                      | 141               | 38                         | 14.2                    | 0.795                      | 140               | 59                         | 195                    |                       |
| 12.6                    | 0.521                      | 141               | 39                         | 13.0                    | 1.70                       | 135               | 155                        | 180                    | 26                    |
| 12.6                    | 0.513                      | 138               | 37                         | 13.0                    | 1.28                       | 133.5             | 112                        | 185                    |                       |
| 12.6                    | 0.505                      | 134               | 35                         | 13.0                    | 0.871                      | 132               | 76                         | 190                    |                       |
| 12.0                    | 0.506                      | 132               | 35                         | 12.5                    | 1.45                       | 127               | 120                        | 185                    | 25                    |
| 12.0                    | 0.499                      | 129               | 34                         | 12.5                    | 1.06                       | 126               | 87                         | 190                    |                       |
| 12.0                    | 0.492                      | 126               | 33                         | 12.5                    | 0.793                      | 124               | 56                         | 195                    |                       |
| 12.0                    | 0.485                      | 122               | 32                         | 12.5                    | 0.773                      | 121               | 50                         | 200                    |                       |
| 11.5                    | 0.50                       | 127               | 33                         | 12.0                    | 1.63                       | 121               | 127                        | 185                    |                       |
| 11.5                    | 0.492                      | 124               | 32                         | 12.0                    | 1.25                       | 120               | 97                         | 190                    | 24                    |
| 11.5                    | 0.486                      | 120               |                            | 12.0                    | 0.881                      | 118               |                            | 195                    |                       |
| 11.5                    | 0.479                      | 117               |                            | 12.0                    | 0.773                      | 116               |                            | 200                    |                       |
| 11.4                    | 0.483                      | 118               | 30                         | 11.8                    | 0.985                      | 115               | 74                         | 195                    |                       |
| 11.4                    | 0.476                      | 115               | 29                         | 11.8                    | 0.774                      | 113               | 48                         | 200                    | 23.5                  |
| 11.4                    | 0.470                      | 112               | 28                         | 11.8                    | 0.756                      | 111               | 45                         | 205                    |                       |
| 11.4                    | 0.464                      | 110               | 27                         | 11.8                    | 0.739                      | 108               | 43                         | 210                    |                       |
|                         |                            |                   |                            |                         |                            |                   |                            |                        |                       |



The characteristics of the modified IP circuit differ from the original circuit in only one manner; the elimination of the four diodes provides more base drive allowing the circuits to deliver more load current without excessive saturation voltage. However, with the addition of IP #5 and #6 as shown in Figure 3-1, the load requirements change. A worst-case analysis was then performed to determine the limits of the modified IP circuit. Table 3-4 is a tabulation of the results only for those input voltages needed to determine the overall worst-case performance. As in Table 3-3, the nominal case is shown for comparison. In Paragraph 3-4, these results along with the IN circuit results are summarized in a description of the overall worst-case performance.

### 3-3 IN CIRCUIT RESULTS

The most important circuit parameter again is the saturation voltage drop. The base drive to the IN circuits is dependent upon the gated input to the AND logic circuit. Under worst-case conditions this voltage was considered to have a minimum of 23 volts.

The IN circuit load current is the IP circuit base current which has a maximum of approximately 15 milliamperes depending on the input voltage to the IP circuit. However, a 50-milliamper load current was specified for the analysis in anticipation of other applications for the IN circuit. The analysis was carried out considering the IN circuit and the AND logic circuits as one circuit with a load current of 50 milliamperes and a logic input of 23 volts. Under these conditions the IN circuit performed satisfactorily for all worst-case conditions except one failure mode at  $-25^{\circ}\text{C}$ . Under worst-case failure mode conditions at  $-25^{\circ}\text{C}$ , the maximum load current the IN circuit would carry was 30 milliamperes, or twice that required at any time in the Switch Selector. The circuit and analysis are discussed in detail in Section 5.

Table 3-5 shows the results of the worst-case and statistical analysis. The statistical distribution of the saturation voltage for each case can be seen in Appendix I.

The 16K ohm resistors used for the gated input to the logic circuits are the only components which could have a 100 percent duty cycle. However, the maximum power dissipation is less than 50 percent of rated power. Table 3-6 shows typical nominal and maximum component power dissipations.

### 3-4 REALIZING AN OUTPUT UNDER WORST-CASE CONDITIONS

Referring again to Figure 3-1, a typical output of one of the 112 outputs is realized as shown without the dotted line. The logic diagram in Appendix III shows the complete Switch Selector logic.



Table 3-4. Modified IP Circuit Results  
With Open Failure at -25 °C

| Nominal Case            |                            |                   |                            | Maximum Worst-Case      |                            |                   |                            | Conditions             |                       |
|-------------------------|----------------------------|-------------------|----------------------------|-------------------------|----------------------------|-------------------|----------------------------|------------------------|-----------------------|
| Total Base Current (ma) | Saturation Voltage (Volts) | Load Current (ma) | Transistor Pwr. Diss. (mw) | Total Base Current (ma) | Saturation Voltage (Volts) | Load Current (ma) | Transistor Pwr. Diss. (mw) | Load Resistance (Ohms) | Input Voltage (Volts) |
| 13.1                    | 0.525                      | 145               | 40                         | 13.6                    | 1.27                       | 141               | 95                         | 175                    | 26                    |
| 13.1                    | 0.516                      | 142               | 38                         | 13.6                    | 0.991                      | 139               | 61                         | 180                    |                       |
| 13.1                    | 0.508                      | 138               | 37                         | 13.6                    | 0.802                      | 136               | 58                         | 185                    |                       |
| 13.1                    | 0.500                      | 134               | 35                         | 13.6                    | 0.78                       | 132.5             | 55                         | 190                    |                       |
| 13.1                    | 0.492                      | 131               | 34                         | 13.6                    | 0.758                      | 130               | 52                         | 195                    |                       |
| 12.3                    | 0.506                      | 133               | 35                         | 12.8                    | 1.13                       | 130               | 68                         | 180                    | 24.5                  |
| 12.3                    | 0.498                      | 130               | 34                         | 12.8                    | 0.878                      | 128               | 54                         | 185                    |                       |
| 12.3                    | 0.490                      | 126               | 33                         | 12.8                    | 0.778                      | 125               | 51                         | 190                    |                       |
| 12.3                    | 0.483                      | 123               | 31                         | 12.8                    | 0.758                      | 121               | 49                         | 195                    |                       |
| 12.3                    | 0.477                      | 120               | 30                         | 12.8                    | 0.738                      | 119               | 46                         | 200                    |                       |
| 12.3                    | 0.470                      | 117               | 29                         | 12.8                    | 0.720                      | 116               | 44                         | 205                    |                       |
| 11.8                    | 0.49                       | 124               | 32                         | 12.2                    | 0.984                      | 122               | 51.5                       | 185                    | 23.5                  |
| 11.8                    | 0.484                      | 121               | 31                         | 12.2                    | 0.776                      | 120               | 49                         | 190                    |                       |
| 11.8                    | 0.477                      | 118               | 30                         | 12.2                    | 0.757                      | 117               | 47                         | 195                    |                       |
| 11.8                    | 0.471                      | 115               | 29                         | 12.2                    | 0.739                      | 114               | 45                         | 200                    |                       |
| 11.8                    | 0.465                      | 112               | 28                         | 12.2                    | 0.721                      | 111               | 42                         | 205                    |                       |
| 11.8                    | 0.459                      | 109               | 27                         | 12.2                    | 0.705                      | 109               | 40                         | 210                    |                       |



Table 3-5. IN Circuit Worst-Case and Statistical Results

| Saturation Voltage (Volts) |         |         |                       |        |         |                      |                                                                    |
|----------------------------|---------|---------|-----------------------|--------|---------|----------------------|--------------------------------------------------------------------|
| Worst-Case                 |         |         | 500 Cases Statistical |        |         | Temperature          | Operating Mode                                                     |
| Minimum                    | Nominal | Maximum | Minimum               | Mean   | Maximum | Deg C                |                                                                    |
| 0.0971                     | 0.2218  | 0.3548  | 0.1373                | 0.2175 | 0.2928  | +125                 | Normal Operation<br>Gated Input = 23V                              |
| 0.1019                     | 0.2302  | 0.3863  | 0.1452                | 0.2270 | 0.3037  | + 25*                |                                                                    |
| 0.1056                     | 0.2367  | 0.4397  | 0.1523                | 0.2421 | 0.3268  | - 25                 |                                                                    |
| 0.0634                     | 0.1400  | 0.2235  | 0.0806                | 0.1376 | 0.2010  | +125                 | One Transistor Shorted<br>Gated Input = 23V                        |
| 0.06657                    | 0.1459  | 0.2723  | 0.0843                | 0.1473 | 0.2250  | + 25*                |                                                                    |
| 0.0691                     | 0.1609  | 0.3503  | 0.09084               | 0.1637 | 0.2589  | - 25                 |                                                                    |
| 0.1569                     | 0.2886  | 0.4535  | 0.1848                | 0.2893 | 0.3929  | +125                 | One Transistor Open<br>Gated Input = 23V<br>Load Current = 50 ma   |
| 0.1635                     | 0.3084  | 0.8293  | 0.2005                | 0.3167 | 0.4799  | + 25*                |                                                                    |
| 0.1185                     | 0.2557  | 0.5196  | 0.1545                | 0.2634 | 0.3915  | - 25                 |                                                                    |
| 0.1329                     | 0.2682  | 0.5651  | 0.1675                | 0.2815 | 0.4370  | - 25                 | One Transistor Open<br>Gated Input = 24.5V<br>Load Current = 37 ma |
| 0.1579                     | 0.2948  | 0.6169  | 0.1926                | 0.3042 | 0.4609  | - 25                 |                                                                    |
| 27.998                     | 27.998  | 27.998  | 28.0                  | 28.0   | 28.0    | Typical<br>All Temps | Up Level With One<br>Zener Diode Shorted                           |

\* Approximately 5000 cases in Statistical



Table 3-6. IN Circuit Component Power Dissipation

| Component                                  | Power Diss (mw) |        | Temp<br>Deg C | Operating Mode                              |
|--------------------------------------------|-----------------|--------|---------------|---------------------------------------------|
|                                            | Min             | Max    |               |                                             |
| 16 K AND CKT Resis-<br>tors RA1 thru RA4   | 40              | 44.0   | All<br>Temps  | Up Level<br>Gated Input = 28V               |
|                                            |                 | < 30.0 | All<br>Temps  | Typical All Conditions<br>Gated Input = 23V |
| 3K Bias Resistors<br>RT1 thru RT4          |                 | < 0.5  | All<br>Temps  | Typical All Conditions                      |
| IN1753A Zener Diodes                       |                 | < 9.0  | All<br>Temps  | Typical All Conditions                      |
| IN645 Diodes                               |                 | < 2.5  | All<br>Temps  | All Conditions                              |
| 2N2222                                     | 3.5             | 6.5    | All<br>Temps  | Normal Operation                            |
| Transistors                                | 8               | 25.0   | All<br>Temps  | All Failure Modes                           |
| Maximum Rated Component Power Dissipation: |                 |        |               |                                             |
| Resistors at all temperatures-----         |                 |        |               | 125mw                                       |
| 2N2222 transistor at +125 °C -----         |                 |        |               | 167mw                                       |
| 2N2222 transistor at +25 °C or less -----  |                 |        |               | 500mw                                       |
| IN753A Zener diode at +125 °C -----        |                 |        |               | 200mw                                       |
| IN753A Zener diode at +25 °C or less ----- |                 |        |               | 400mw                                       |
| IN645 diode at +125 °C-----                |                 |        |               | 200mw                                       |
| IN645 diode at +25 °C or less-----         |                 |        |               | 600mw                                       |



A typical output channel is turned on in the following manner. The input eight-bit word is such that all logical ONE's are applied to AND circuits #1 and #2 through six of the Bit Register Relays. Bit Register Relays #1 and #2 are also set or closed. The Read Relay then turns IP #6 and #5 on. Since Stage Power is always present at the inputs of IP #6 and #5, Switch Power A (SPWRA) and Switch Power C (SPWRC) will be on. IP's #4 and #3 have been turned on by Bit Register Relays #1 and #2. Therefore, power is applied to AND circuits #1 and #2. Because all logical ONES have been applied to the AND circuits, they provide inputs to IN circuits #1 and #2 and turn the IN circuits on. The IN circuits act as switches to turn on IP's #2 and #1 which supply power at the desired output channel. IP's #6 and #5 are used for each of the 112 outputs. However, each of the outputs require different circuits to complete the remainder of the configuration. This can be seen by following the logic in Appendix III.

The operation will now be analyzed for worst-case conditions. These conditions will occur at  $-25^{\circ}\text{C}$ , the minimum specified operating temperature. A worst-case failure of one transistor open in each IP and IN circuit will be considered. The maximum current required by the AND circuits has been calculated considering ideal diodes. No failures (open resistors) are considered in the AND circuit since this would require less current. A minimum stage power voltage of 26 volts will be considered since this reduces the base drive to the IP circuits and thus increases the saturation voltage drop.

With a maximum of three volts drop between stage power and output specified, a maximum of one volt drop across each IP circuit is assumed. Then IP #3 will have 24 volts applied and will apply 23 volts in turn to AND circuit #2, which actually represents eight AND circuits in parallel. Because the drop across IP #3 will actually be less than one volt, a maximum voltage of 26 volts applied to the AND circuits will be assumed. This requires a maximum of 52 milliamperes. Then IP #3 must supply a 52 milliamperes load current with less than one volt drop when 24 volts input is applied. The load on IP #4 then consists of IP #3 load and base current of 52 milliamperes and 13 milliamperes maximum respectively, plus 52 milliamperes to AND circuit #1 which also represents eight AND circuits. The minimum input voltage to IP #4 will be 25 volts. Then IP #4 must supply  $52 + 13 + 52$  or 117 milliamperes with less than one volt drop when 25 volts input is applied. The load on IP #6 will then be the load on IP #4 plus the base current in IP #4 or  $117 + 14 = 131$  milliamperes. IP #6 must then supply 131 milliamperes with less than one volt drop when 26 volts input is applied. It was stated earlier that IP #1, #3, and #6 were all modified IP circuits. It can then be seen in Table 3-4 that the modified IP circuit will easily meet each of the requirements just described.

IN circuits #1 and #2 must be capable of carrying a current of 15 milliamperes maximum. The minimum input voltage of 23 volts to the AND circuits will be assumed, although this input voltage will be somewhat greater if the load current reaches 15 milliamperes. Table 3-5 shows that the maximum voltage drop to be expected under these conditions is approximately 0.5 volts. Since the IN circuit will carry



30 milliamperes with only 0.52 volts maximum drop when the input to the AND circuit is 23 volts, it is safe to assume that under the conditions stated above the maximum voltage drop will be 0.5 volts.

Again assuming one volt drop per IP circuit, IP #1 will have a minimum of 24 volts input. However, considering 0.5 volts across IN #2, the conditions correspond to 23.5 volts input with base input "A" grounded. IP #1 must then supply 110 milliamperes maximum load current with less than one volt drop when 23.5 volts input is applied. IP #1 is a normal IP circuit and Table 3-3 shows that it will easily meet these requirements.

IP #2 must supply 110 milliamperes plus the base current for IP #1, which is approximately 12 milliamperes. The input to IP #2 is 25 volts minimum or 24.5 volts when the drop across IN #1 is considered. IP #2 must then supply  $110 + 12 = 122$  milliamperes with less than one volt drop when 24.5 volts input is applied. IP #5 has a load of IP #2 load and base current. IP #5 must be capable of supplying  $122 + 14 = 136$  milliamperes at less than one volt drop with 26 volts input. IP's #2 and #5 are both modified IP circuits. Table 3-4 shows that the modified IP will easily meet each of these requirements.

It is apparent that the worst-case voltages and currents assumed could not all occur simultaneously, thus making worst-case conditions somewhat better than assumed. Having worst-case failures in all of the IP and IN circuits is very improbable but not impossible. Although assuming multiple failures is outside the scope of the design ground rules, it is appropriate for a worst-case analysis. However, the preceding discussion clearly shows that the Switch Selector will meet requirements under worst-case multiple failure mode conditions.

In a similar manner it can be shown that as the stage power and/or temperature increases, the safety margin for satisfactory operation increases.

### 3-5 DETECTING DEFECTIVE CIRCUIT MODULES

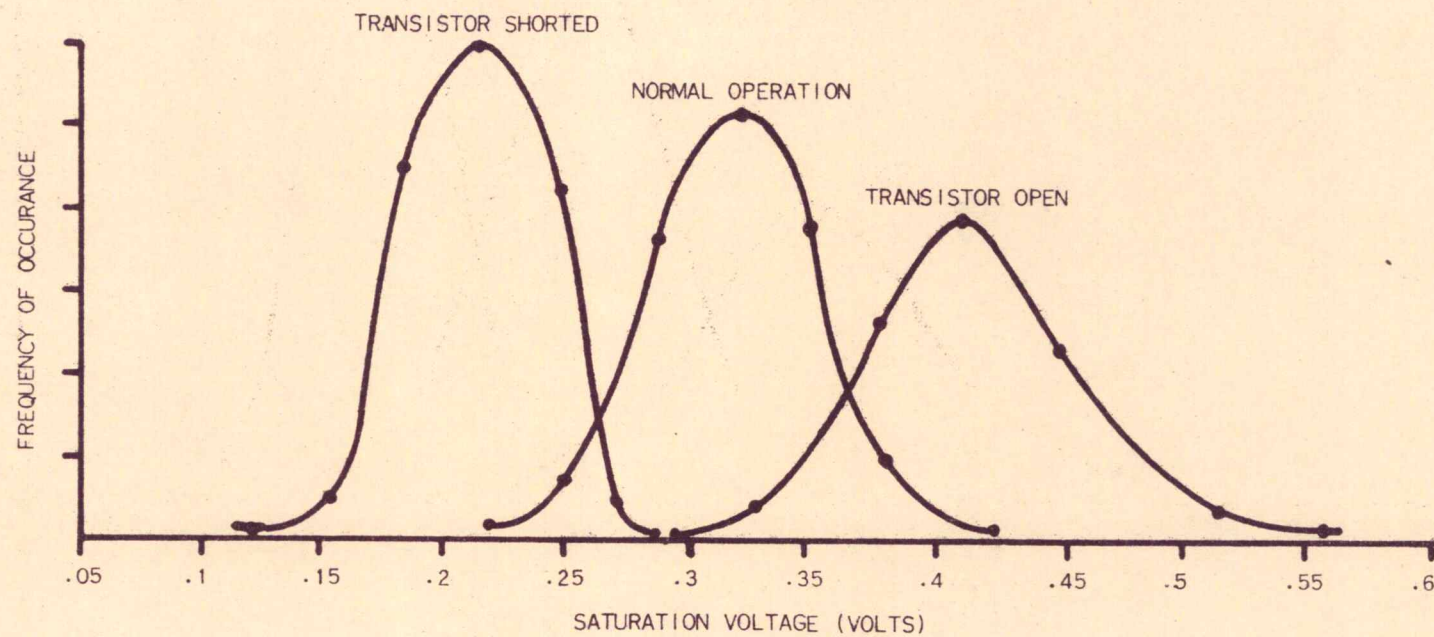
This section presents the result of an effort to evaluate the saturation characteristics of the inverter circuits under three conditions:

1. All components normal
2. A short failure mode
3. An open failure mode.

The possibility of establishing test criteria for circuit modules was investigated by comparing the statistical distributions of the saturation voltages of the failure modes to the distribution for normal operation. The comparison was made for conditions at +25 °C, since testing would most likely be carried out at +25 °C. The normalized distributions are shown in Figure 3-2 and Figure 3-3 for the IP and IN



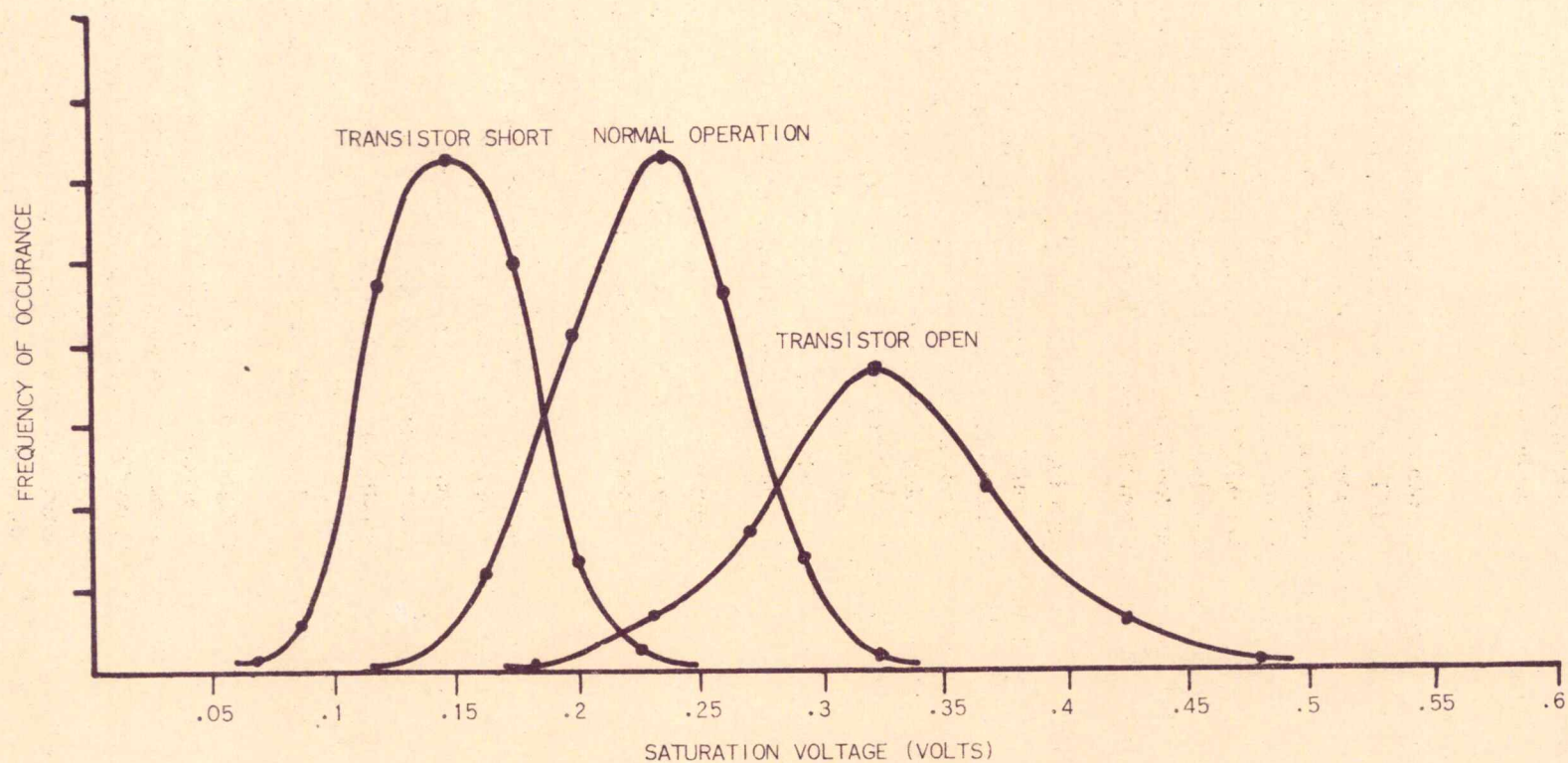
Figure 3-2. Comparison of IP Circuit Statistical Distributions



NORMALIZED STATISTICAL DISTRIBUTIONS BASED ON 10000 CASES FOR EACH MODE OF OPERATION:  
 THE 10000 CASES WERE GROUPED INTO 50 CLASS INTERVALS WITH THE AVERAGE SHOWN HERE.  
 THE MEAN AND 1,2, & 3 SIGMA POINTS ARE SHOWN.



Figure 3-3. Comparison of IN Circuit Statistical Distributions



NORMALIZED STATISTICAL DISTRIBUTIONS BASED ON 5578 CASES FOR EACH MODE OF OPERATION:  
 THE 5578 CASES WERE GROUPED INTO 50 CLASS INTERVALS WITH THE AVERAGE SHOWN HERE.  
 THE MEAN AND 1,2, & 3 SIGMA POINTS ARE SHOWN.



circuits respectively. It can be seen from the distributions (and also Tables 3-1 and -5) that the severe failure modes tested caused only a small change in the saturation voltage drop.

The statistical analysis was carried out using a rectangular distribution for component values and characteristics. This means that all values within the tolerances are equally likely to occur. Although the rectangular distribution is better for worst-case results, a normal distribution of component values may be more realistic for the statistical distributions. This would result in the saturation voltage distributions having less deviation from the mean while the mean would be the same as shown in this analysis and would improve the possibility of establishing criteria for testing without degrading the circuit. However, it should not be assumed that a normal distribution will always represent the range of values found in a given group of components.

Each curve is normalized and represents the worst-case distribution of saturation voltage given a particular operating mode, showing the possible range of saturation voltages for a normal circuit, a circuit with a short mode failure and a circuit with an open mode failure. If an attempt were made to establish fixed limits beyond which a circuit would be considered defective, there would be a certain risk or probability of accepting a defective circuit. The probability of a defective circuit meeting the requirements for a good circuit is calculated for the three selected limits of  $\pm\sigma$ ,  $\pm 1.5\sigma$ , and  $\pm 2\sigma$  deviation from the mean of the distribution for a good circuit. This information is tabulated in Tables 3-7 and 3-8.

The probability of actually accepting a defective module during tests would depend upon the probability of defects existing in the individual components and in the fabrication of the circuits. To obtain and interpret this data is beyond the scope of this report.

It was originally hypothesized that the saturation voltage distributions of circuits operating under the three unique conditions listed previously would exhibit characteristics which were distinctive and not overlapping. However, the analysis proved that this was not the case. Furthermore, any attempt to establish fixed acceptance criteria would result in the acceptance of circuits which contained faults or the rejection of good circuits. Therefore, measurement of the saturation characteristics and the resulting variables data cannot be used as an acceptance criteria.

The analysis did reveal a usable insight to tests at the system level. There was a significant change in these saturation characteristics for similar circuits which contain similar component parameters, yet are in different categories (that is, one of the circuits has a component failure). When this fact is considered, it can be seen that once a distinct level for a given circuit is established, subsequent difference from this level are grounds to suspect that some loss of redundancy has occurred. Furthermore, significantly different characteristics of initial measurements of similar circuits used in similar applications should cause doubt as to the status of the redundancy, and further evaluation should follow.



Table 3-7. Probability for IP Circuit Tests

| Probability of a defective IP circuit module exhibiting a saturation voltage between limits shown when input = 28V and load current = 110 ma. |                        |                              |                          |
|-----------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------------|--------------------------|
| IP BASED ON<br>10,000 CASES                                                                                                                   | $-\sigma$ to $+\sigma$ | $-1.5\sigma$ to $+1.5\sigma$ | $-2\sigma$ to $+2\sigma$ |
| Voltage                                                                                                                                       | 0.285 to 0.348         | 0.269 to 0.364               | 0.253 to 0.379           |
| Probability<br>for Open<br>CKT                                                                                                                | 0.0388                 | 0.0844                       | 0.1883                   |
| Probability<br>for Short<br>CKT                                                                                                               | 0.0012                 | 0.0132                       | 0.0523                   |

Table 3-8. Probability for IN Circuit Tests

| Probability of a defective IN circuit module exhibiting a saturation voltage between limits shown when gated input to AND CKT = 23V and load current = 50 ma. |                        |                              |                          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------------|--------------------------|
| IN BASED ON<br>5578 CASES                                                                                                                                     | $-\sigma$ to $+\sigma$ | $-1.5\sigma$ to $+1.5\sigma$ | $-2\sigma$ to $+2\sigma$ |
| Voltage                                                                                                                                                       | 0.1996 to 0.2594       | 0.185 to 0.274               | 0.170 to 0.289           |
| Probability<br>for Open<br>CKT                                                                                                                                | 0.126                  | 0.231                        | 0.315                    |
| Probability<br>for Short<br>CKT                                                                                                                               | 0.019                  | 0.063                        | 0.186                    |



It should not be construed that the use of this measurement technique is a foolproof method of redundancy loss detection. However, it is an effective tool that can help isolate failures that occur after initial detailed testing, because after a module is installed, all the required test points are not accessible for detailed testing.

### 3-6 AUTOMATIC RESET CIRCUIT RESULTS

The results of the Automatic Reset Circuit analysis are summarized in Table 3-9 showing the critical points of the reset pulse. The results are for normal operation at  $-25^{\circ}$ ,  $+25^{\circ}$ , and  $+125^{\circ}\text{C}$  and for worst-case conditions which result in the minimum and maximum pulse widths. The most important circuit parameter is the reset coil current. IBM Specification No. 608207 for the relay states that the minimum relay operating voltage at  $+25^{\circ}\text{C}$  is 11 volts. Under these conditions the maximum operating time is 5 milliseconds which includes 2 milliseconds for bounce. Then the relay first makes contact in a maximum time of 3 milliseconds under worst-case operating conditions. Laboratory testing revealed that the inductance to be expected in the coil is 0.8 henries. Then using the nominal coil resistance of 725 ohms at  $+25^{\circ}\text{C}$  and applying a step voltage of 11 volts, simple calculations will show that the coil current will increase to 14.2 milliamperes in 3 milliseconds.

Neglecting any changes in mechanical characteristics due to temperature changes, the magnetic field required to operate the relay is constant. Since the magnetic field is directly proportional to the coil current, it can be concluded that the minimum coil current pulse required is independent of temperature. Therefore, if the reset circuit provides a current pulse equal to or greater than the current pulse described above, the relay will operate satisfactorily. Resorting to a current pulse rather than a voltage pulse is a convenient way to establish fixed minimum operating requirements over a temperature range. Since coil resistance varies approximately 10 percent per 25-degree change in temperature, the required voltage pulse would vary proportionally.

It is stated in the Description Manual of the Saturn Switch Selector MOD II, IBM No. 65-529-0004, that the reset pulse width must be from 3.5 to 12 milliseconds. However, the method of measuring the pulse width is not defined. Pulse width is generally defined as that time interval from the time the amplitude has increased to a certain level to the time the amplitude has decreased to a certain level. These levels may be certain percentage points or fixed levels. Therefore, whether a pulse is within the specification is a matter of definition. Considering the relay characteristics and specifications, the pulse width is defined in this report as the time interval from the beginning of the pulse to the time at which the relay coil current has decreased to 14.1 milliamperes. The pulse width limits are also defined as a minimum of 3 milliseconds as limited by the relay characteristics and a maximum of 12 milliseconds to prevent inhibition of subsequent Switch Selector operations.



Table 3-9. Reset Pulse Characteristics

| Pulse Width<br>(ms) | Complete<br>Cutoff<br>(ms) | Maximum Reset<br>Coil Current<br>(ma) | Maximum<br>Transistor<br>Power Diss.<br>(mw) | Condition                                                                                             |
|---------------------|----------------------------|---------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------|
| 6.9                 | 9                          | 29.7                                  | 430                                          | Normal at +25 °C                                                                                      |
| 4.9                 | 11.2                       | 28.2                                  | 480                                          | Normal at -25 °C                                                                                      |
| 7.9                 | 10.7                       | 23.0                                  | 290                                          | Normal at +125 °C                                                                                     |
| 9.6                 | 12.4                       | 25.5                                  | 390                                          | Worst-Case Conditions<br>for Longest Pulse With<br>No IP Circuit Compon-<br>ent Failure (+125 °C)     |
| 11.4                | 14.1                       | 25.5                                  | 390                                          | Worst-Case Conditions<br>for Longest Pulse<br>Including IP Circuit<br>Component Failure<br>(+125 °C)  |
| 3.7                 | 9.5                        | 25.5                                  | 415                                          | Worst-Case Conditions<br>for Shortest Pulse With<br>No IP Circuit Compon-<br>ent Failure (-25 °C)     |
| 2.2                 | 10.5                       | 18.2                                  | 910                                          | IP Circuit Component<br>Failure Causing<br>Shortest Pulse With<br>Other Components<br>Normal (-25 °C) |



There are actually three distinct worst-case failure mode conditions in the Automatic Reset Circuit which can be tolerated due to redundancy. The Automatic Reset Circuit is required to meet specification for any one of these three worst-case modes over the operating temperature range and for worst-case conditions of stage power tolerances. In most cases, the analysis considered simultaneous failures to determine the circuit limits. The most critical conditions are at low temperature when considering worst-case conditions for minimum pulse width. Under these conditions, all three simultaneous component failures cannot be tolerated. The failure modes are discussed in Section 6 along with a detailed description of the analysis. Graphs of the reset pulse and circuit conditions for all test cases are shown in Appendix II.

The transistor power dissipation in some cases has a peak of over 150 percent of rated power and is greater than rated power for several milliseconds. This is due to the long period of time required for the transistors to turn off. The capacitance in the base circuit increases the base voltage at a relatively slow rate preventing the transistors from turning off fast. However, average power dissipation is less than 25 percent of the rated power at the particular temperature in all cases.

The characteristics of the reset circuit oppose the effects of changes in input voltage on the pulse width, holding the pulse width relatively constant.

A severe change in the load on one of the three IP circuits will affect only the width of the pulse at the output of that circuit having a negligible effect on the pulse at the output of the other two circuits.



## SECTION 4

### TOLERANCES AND TEST CONDITIONS

#### 4-1 TOLERANCES

Three factors were considered in determining the component tolerances used for the analysis of the IP and IN circuits: (1) initial purchase tolerance, (2) aging based on 10,000 hours end-of-life, (3) changes in temperature.

All resistors used in the circuits were type RN60C. The total tolerance for all resistors at all temperatures was  $\pm 3$  percent. This consisted of  $\pm 1$  percent initial purchase tolerance and  $\pm 2$  percent aging tolerance which included a change of 50 parts per million per degree change in temperature from  $+25^{\circ}\text{C}$ .

The equivalent circuits used for the transistors require that two characteristic curves and Beta be given. The range used for Beta was found by using the minimum Beta of 100 at purchase for  $+25^{\circ}\text{C}$  and determining a maximum of 250 by testing a random selection of transistors. These values were then degraded by 20 percent for aging. A temperature coefficient of 0.6 percent per degree change from  $+25^{\circ}\text{C}$  was applied for temperatures differing from  $+25^{\circ}\text{C}$ .

The  $I_e$  versus  $V_{be}$  curve was determined by the manufacturer's specifications and by laboratory testing. A  $\pm 50$  millivolt spread was applied to the curve to include purchase tolerance and aging. It may be noted here that aging causes very little change in the characteristic curves. The  $I_c$  versus  $V_{bc}$  curve was determined by laboratory testing and using the minimum and maximum curves. This curve was not held to a  $\pm 50$  millivolt spread since this characteristic varies with collector current. For conditions other than  $+25^{\circ}\text{C}$  the curves were varied by a -2 millivolts per degree Centigrade change from  $+25^{\circ}\text{C}$ .

The SIN645 diode curve was determined by laboratory testing and applying a  $\pm 50$  millivolt spread to include purchase tolerance and aging. Again, for conditions other than  $+25^{\circ}\text{C}$ , the curve was varied by -2 millivolts per degree Centigrade change from  $+25^{\circ}\text{C}$ .

The IN753A zener diode curve was determined by laboratory testing of a random selection and the minimum and maximum curves were used. The temperature coefficient used was specified by the manufacturer to be 0.045 percent per degree Centigrade.

The tolerances for components in the reset circuit were used as depicted on respective IBM source control drawings Nos. 6082103, 6082104, and 6082078 for the thermistors, capacitors, and relays respectively. The actual tolerances and values are stated in Section 5 for the derivation of the equivalent circuit used in the analysis.



It was stated in Section 1 that with the quad-redundant configuration of the IP and IN switching circuits, the circuits will continue to function although various components in the circuit may have failed. As can be seen, there are many possible combinations of component failures. This analysis was intended to cover only those failure modes that are most detrimental to circuit operation without causing the circuit as a whole to fail.

Considering the circuits as symmetrical, it can be seen that two shorted transistors on one side of the circuit, or one open transistor on each side of the circuit would cause complete failure. It is very unlikely to have either one of these two combinations of failures. However, even considering high reliability components, it is quite possible to have a component failure or a mechanical defect which would cause one transistor to be permanently on or shorted or one transistor to be permanently off or open.

For both the IP and IN circuits, two failure modes which were considered to be the most severe were used for the analysis: (1) a component failure or open connection which would open one side of the circuit and force the other side of the circuit to carry all of the load current, (2) one transistor shorted which would cause the other transistor on the same side of the circuit to carry nearly all of the load. These conditions were simulated as discussed in Section 5. To simulate worst-case test conditions for all modes of operation, the maximum required load current, 110 milliamperes for the IP circuit and 50 milliamperes for the IN circuit, was used. The last condition considered was that the circuits be analyzed with the minimum available base drive.

The number of component failures considered in the Automatic Reset Circuit was limited to one capacitor opening or shorting, one thermistor opening, and a worst-case failure in one IP circuit. The reset circuit was analyzed for worst-case combinations of these failures and extreme operating temperatures to determine if the reset pulse would be within the required range of 3 to 12 milliseconds.



## SECTION 5

### DETAILED DESCRIPTION OF IP AND IN CIRCUIT ANALYSES

A steady-state dc analysis was performed on the quad-redundant IP and IN switching circuits. The most important parameter was the saturation voltage drop (VCESAT) across the circuit for each condition of component failure and temperature. Therefore, the loads and inputs were held constant to better determine the effects of circuit component variations on circuit operation. For the IP circuit the base drive is dependent upon the input voltage (gated-input) and the analysis was performed for the nominal input voltage and 2 volts below the minimum input voltage. In the case of the IN circuit which is associated with the AND logic circuit, the base drive was dependent upon the gated input to the AND circuit which was held at its minimum value for worst-case.

Equivalent circuits were used for the analyses. In each circuit, open conditions were simulated by increasing the resistance (to 10 megohms) of 0.001 ohm resistors connected in series with the emitters, collectors, and bases of the transistors. Shorting conditions were simulated by decreasing the resistance (to 0.001 ohm) of 10-megohm resistors between the emitters and adjacent collectors of the transistors. This method of simulating open and short circuits for failure modes greatly simplifies the mechanics of programming when more than one mode of operation is to be analyzed. Several possible failure modes could have been simulated. It was found that for normal operation, the resistors caused a negligible amount of unbalance in the circuits.

A diode connected between the base and collector of each transistor is part of the equivalent circuit for a saturated transistor condition as discussed in Appendix IV.

The current sources connected to the collectors of both circuits maintained a constant load. While this may not be as realistic as a resistive load, it is better for a worst-case analysis. Obviously, the current source could be used only when the circuit was turned on. When the circuit was turned off or the transistors became unsaturated, the current source required replacement with a passive load.

#### 5-1 IP CIRCUIT ANALYSIS

The IP switching circuit as shown in Figure 5-1 is used as a driver to supply power at the outputs of the Switch Selector. The circuit is turned on by grounding the base input and thus causing the PNP transistors to be turned on when a gated input is applied. The maximum load current specified for the analysis was 110 milliamperes. The current was analyzed using tolerances as explained in Section 3 for each of the following conditions at  $-25^{\circ}$ ,  $+25^{\circ}$ , and  $+125^{\circ}\text{C}$ :

1. Normal operation with input of 28V
2. Normal operation with input of 24V



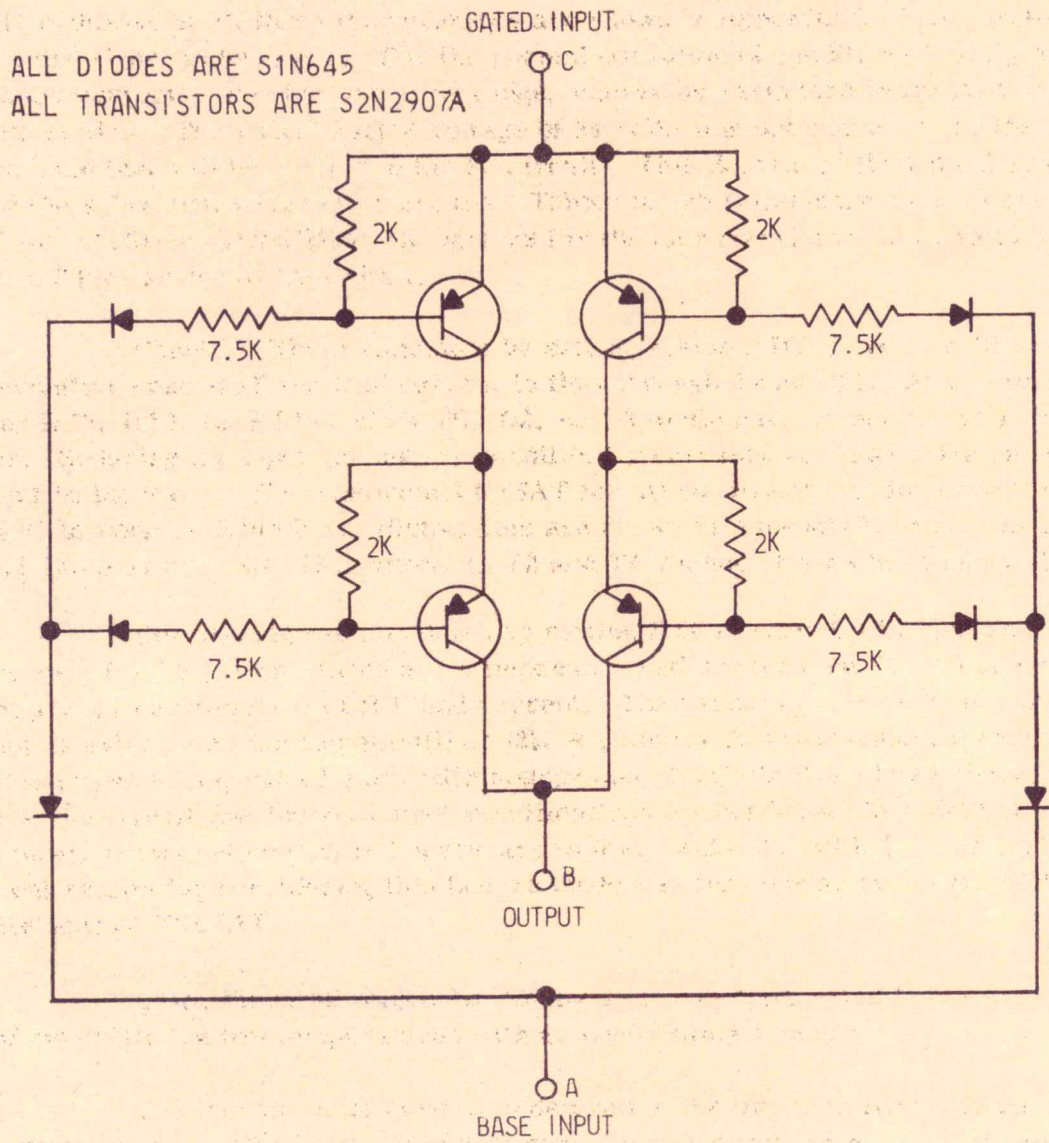


Figure 5-1. Normal IP Switching Circuit



3. One side of the circuit open with input of 28V
4. One side of the circuit open with input of 24V
5. Collector to emitter short on one transistor (Input of 28V).

The circuit was programmed as shown in Figure 5-2 to be run using the ASAP computer program. Histograms of the saturation voltage drop (VCESAT) for all conditions at all three temperatures are shown in Appendix I. The worst-case results are shown in Section 3. For the normal operation of condition (1) or (2), the transistor currents varied over a wide range, caused by variations in transistor characteristics. The reduced input voltage of 24 volts was determined to be the worst-case voltage that will be applied to the IP circuit. This decreased the base drive and caused the saturation voltage to increase. Tables for 25 worst-case parameters for +25 °C for conditions (1) and (2) and histograms for the four transistor currents for condition (1) are shown in Appendix I.

Condition (3) was simulated by setting resistor RT11 equal to 10 megohms. This condition caused all the load current to flow through T2 and T4. As can be seen, opening RT3, RT4, or RT8 or diode D1, D2, or D3 would have caused the same conditions. Reducing the input voltage for condition (4) decreased the base drive and caused VCESAT to increase. The maximum VCESAT for all conditions was for condition (4) at -25 °C as seen in Table 3-1. Histograms are shown in Appendix I. Since the load current had only one path, the current in T2 and T4 did not vary as in condition (1) or (2).

Condition (5) was simulated by setting RT6 equal to 0.001 ohm and setting beta to zero for T3. This caused a low impedance path through the T1 - T3 side of the circuit and T1 carried most of the load current. The variation in transistor currents was not as extreme as for condition (1) or (2). A table for 25 worst-case parameters at +25 °C is shown in Appendix I along with histograms of VCESAT as stated above. Because the circuit was found to meet specifications for conditions (2) and (4) with 24 volts gated input, it was not considered necessary to test condition (5) with 24 volts input. The principal reason for considering this failure mode was for comparison of the statistical distributions of VCESAT.

Using the results thus far obtained, it was determined that worst-case conditions existed at low temperatures with an open failure mode.

This condition was tested to determine the limits as input voltage and load current varied. The limit for satisfactory operation was set at one volt drop across the circuit. The results are shown in Table 3-3.

The modified IP circuit as shown in Figure 5-3 was analyzed in a similar manner to determine the worst-case limits. The design changes can be seen by comparing Figure 5-1 to Figure 5-3. The results for this circuit are shown in Table 3-4. These worst-case limits of the two circuits are used in Section 3 to show that the Switch Selector will meet specifications under extreme worst-case conditions.



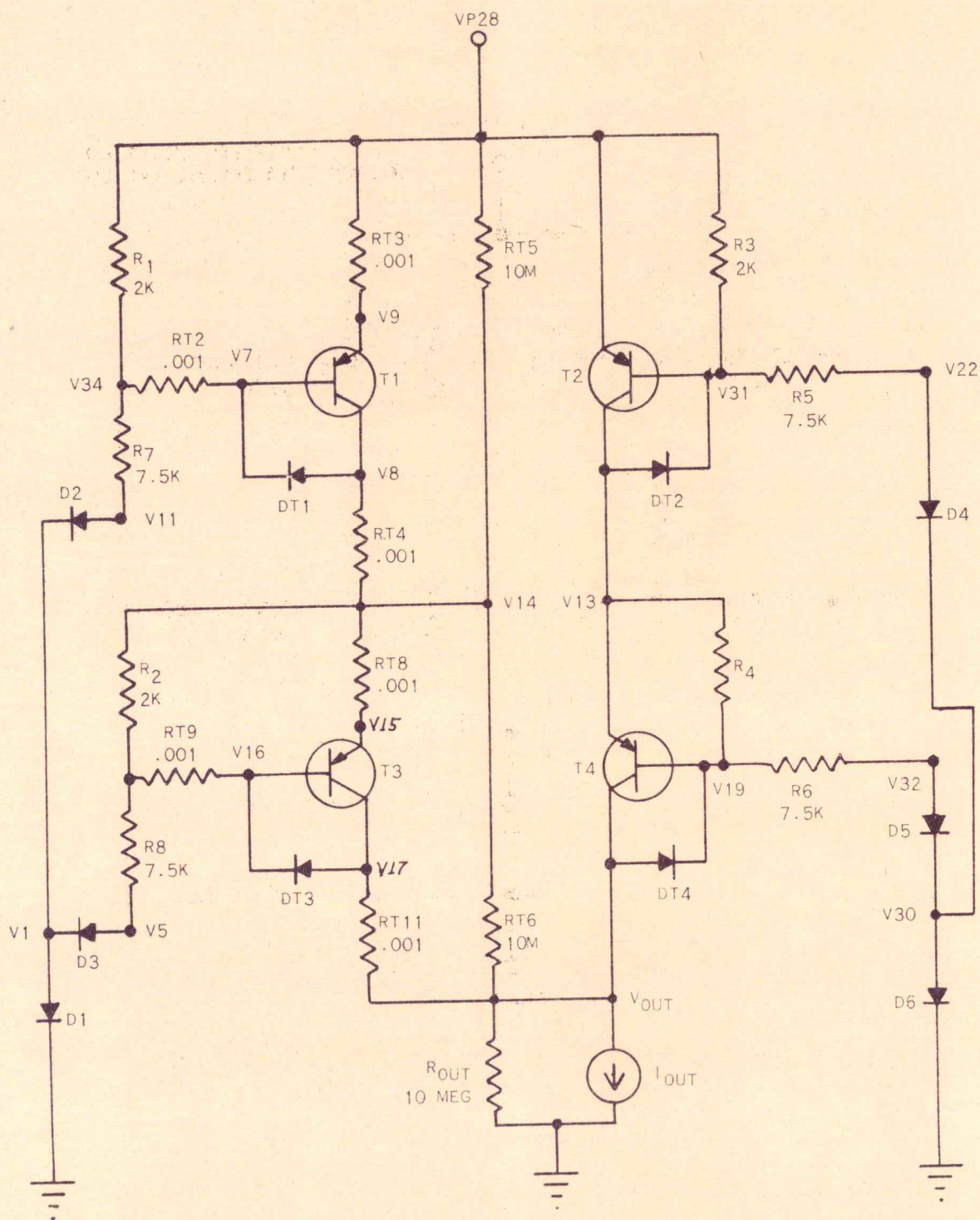


Figure 5-2. IP Equivalent Switching Circuit



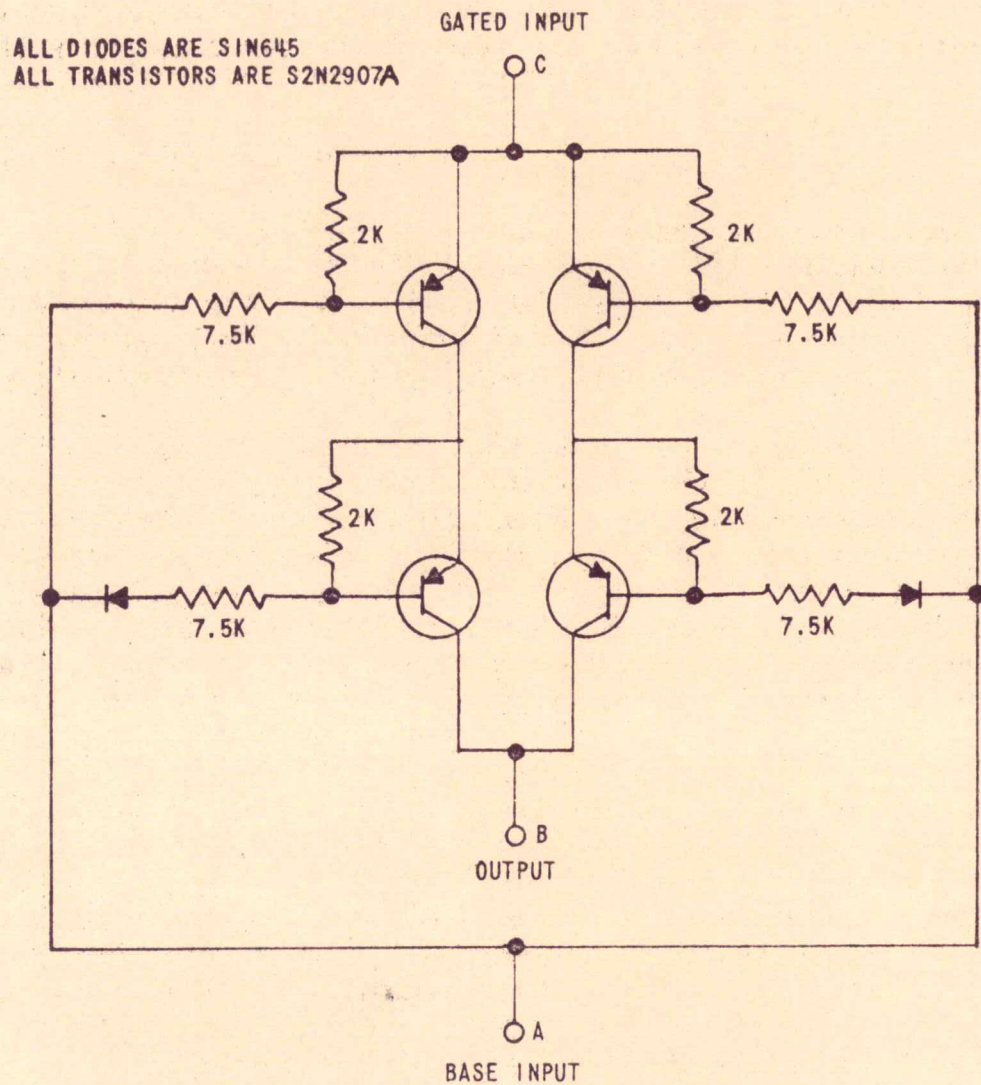


Figure 5-3. Modified IP Switching Circuit



The IP switching circuit was found to meet specifications for all worst-case conditions tested.

The steady-state power dissipation for each component was calculated using the worst-case results, or for some components was calculated as part of the computer program. Since the power level in most components was much less than the rated power, only the maximum is tabulated in most cases. Table 3-2 shows the results.

## 5-2 IN CIRCUIT ANALYSIS

The IN switching circuit is used as a decoder and provides the base input signal to the IP circuits within the Switch Selector. The base input to the IN circuit is provided by a gated input voltage controlled by diode logic. Two identical diode logic circuits, AND circuits, are used so that the IN circuit may be controlled with either the given binary word or the complement of that word.

The IN switching circuit with the associated AND circuits is shown in Figure 5-4. The gated input is a positive voltage with respect to ground. When all the logic inputs are open, or ungrounded, the gated input provides base drive to the transistors and the IN circuit is turned on, causing the output B to approach ground potential. If one of the logic inputs is grounded, the current will see a low impedance path to ground. Thus, no base drive will be provided for the transistors, and the IN circuit is off, allowing no current to flow in the load at output B. The zener diodes prevent the transistors from turning on due to noise at the logic inputs or due to the voltage drop across the diodes in the AND circuit.

To permit the use of the computer program, ASAP, for the analysis, the circuit had to be simplified so that the number of diodes would not exceed the limit of the program. Therefore, the logic circuit was reduced as shown in the equivalent circuit of Figure 5-5 with negligible effects on the steady-state circuit parameters. With the exception of DA1 through DA4 all of the diodes could have been eliminated except for the condition of turning the circuit off.

The maximum load current specified for the analysis was 50 milliamperes. For worst-case conditions, the gated input (VARN) was held constant at 23 volts for minimum base drive. The voltage applied to the load was held at 28 volts for all conditions. The circuit was analyzed using tolerances as explained in Section 4 for each of the following conditions at  $-25^{\circ}$ ,  $+25^{\circ}$ , and  $+125^{\circ}\text{C}$ :

1. Normal operation
2. One side of the circuit open
3. Collector to emitter short on one transistor
4. Zener diode short with the circuit turned off.



ALL TRANSISTORS ARE S2N2222.  
 ALL ZENER DIODES ARE S1N753A.  
 ALL DIODES IN AND CIRCUIT ARE S1N645.

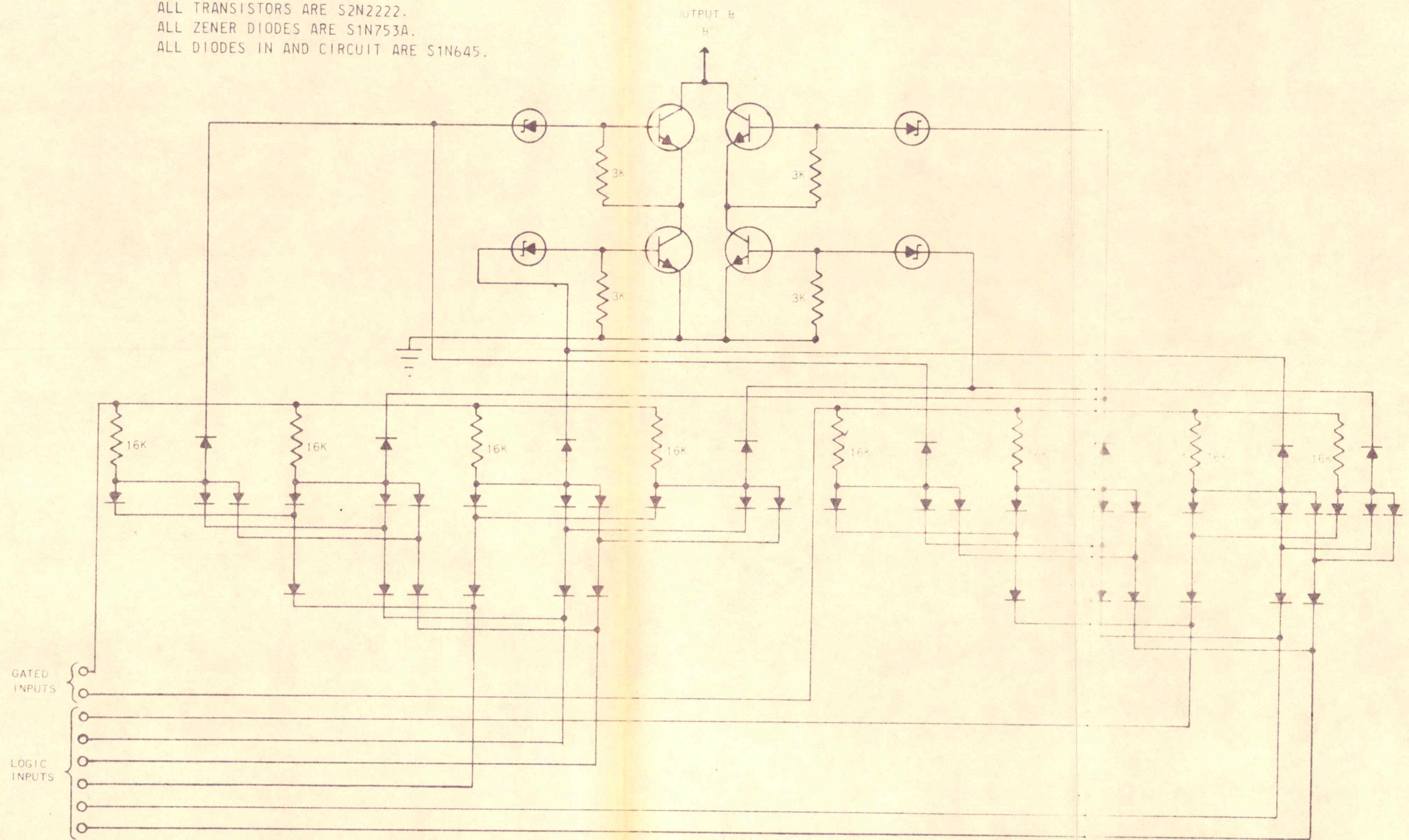


Figure 5-4. IN Switching Circuit



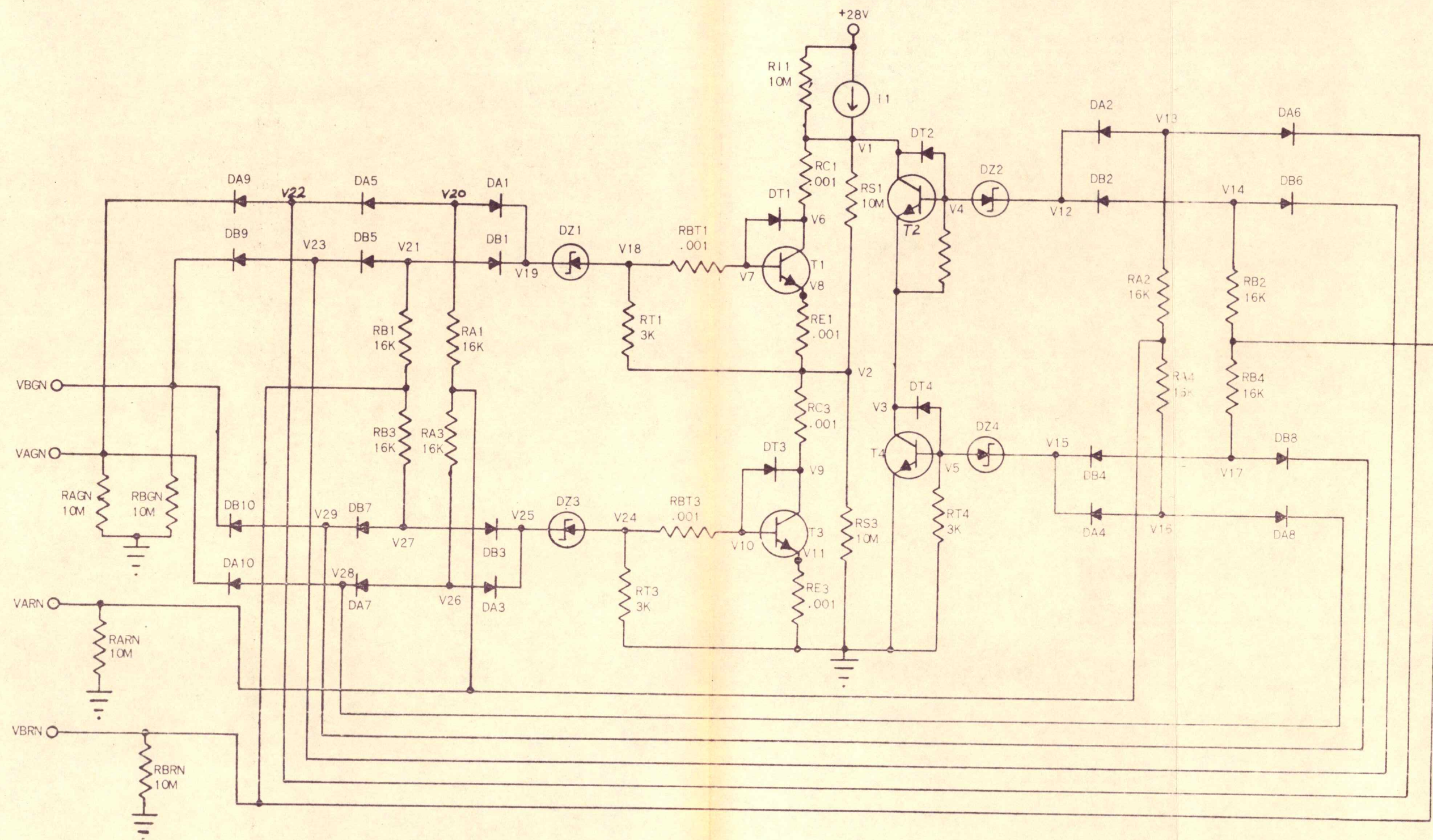


Figure 5-5. IN Equivalent Switching Circuit



The circuit was programmed as shown in Figure 5-5 to be run using the ASAP computer program. Histograms of the saturation voltage drop for all test conditions except(4) are shown in Appendix I. The worst-case results are shown in Section 3.

For the normal operation of condition(1), the transistor currents varied over a wide range as for the IP circuit. Histograms of the four currents at +25 °C and a table of 25 worst-case parameters are shown in Appendix I.

Condition(2) was simulated by increasing resistor RC1 to 10 megohms effectively opening the resistor to simulate an open solder connector or an open transistor. This forced all of the load current to flow through T2 and T4 resulting in an increased voltage drop across the circuit. Preliminary calculations showed that at -25 °C, T2 and T4 would become unsaturated with a load current of 50 milliamperes. To prevent the current source I1 from causing erroneous voltages, I1 was set to zero and RI1 was set to  $\frac{V_{p28}-V_1}{50 \text{ ma}} = 555 \text{ ohms}$ , where VP28 = 28 volts, V1 is the nominal V1 for normal operations. With RI1 = 555 ohms and I1 = 0, at -25 °C it was found that the currents IDT2 and IDT4 through DT2 and DT4 were negative at worst-case indicating that T2 and T4 did pull out of saturation. This caused V1max to be 9.45 volts and the load current to drop to approximately 35 milliamperes, T2 emitter current (IT2).

IBM Test Specification No. 6101451, Type 1 Decoders, specified that the IN circuit can have a maximum voltage drop of 1.5 volts at a load current of 15 milliamperes with a minimum of 23 volts at VARN. Also IBM Test Specification No. 6101457, Type 7 Decoders, specifies a maximum voltage drop of 1.5 volts with 37 milliamperes load current and a minimum of 24.5 volts at VARN.

The circuit was then tested to find the limits of the operation at -25 °C with one transistor open. After preliminary calculations, a worst-case and statistical analysis was performed to verify satisfactory operation for three conditions at which the circuit operated near the limits: (a) VARN = 28 volts and load current = 50 milliamperes, (b) VARN = 24.5 volts and load current = 37 milliamperes, (c) VARN = 23 volts and load current = 30 milliamperes. The results are tabulated in Table 3-5, and histograms of the statistical distributions are shown in Appendix I. With the worst-case conditions of 23 volts at VARN, the gated input to the AND circuit, the IN switching circuit was capable of carrying 30-milliamperes load current, or two times the maximum current required, with approximately 0.5 volts drop.

Condition(3) was simulated by decreasing RS3 to 0.001 ohm and setting beta 3 to zero. This created a low impedance path in one side of the circuit causing T1 to carry most of the load current. This resulted in a decrease in saturation voltage. With a load current of 50 milliamperes and a gated input at VARN of 23 volts, the transistors remained in saturation at all temperatures.



Condition(4) was simulated by removing DZ1 and letting  $RAGN = 322$  ohms, which resulted in VAGN being approximately 2 volts to represent noise. VARN was set at 28 volts to increase the possibility of the circuit turning on. The current source I1 had to be removed and RI1 set to 555 ohms. The voltage at V1 was essentially 28 volts with less than a millivolt change due to temperature extremes. No histograms are shown.

Because of the large number of diodes in the equivalent circuit of Figure 5-5, excessive computer time would have been required to run a statistical analysis of 10,000 cases for every test condition. Therefore, only approximately 500 cases were run at  $+25^{\circ}\text{C}$  to provide a better comparison between the statistical distributions for the second objective of this analysis.

All steady-state power dissipated in each component was much less than the rated power and was calculated similarly to that in the IP circuit. The results are shown in Table 3-6.



## SECTION 6

### ANALYSIS OF AUTOMATIC RESET CIRCUIT

#### 6-1 CIRCUIT DESCRIPTION

The eight Bit Register relays and the three Stage Select relays are latching-type relays which require a pulse to be applied to the reset coils when it is desired to reset the contacts. The reset circuit, which generates the bit reset pulse, and the reset coils of the relays are shown in Figure 6-1.

Operation of the circuit is as follows. With the capacitors discharged and K17 in the position shown, the base inputs of the three IP circuits are essentially at ground potential and the IP switching circuits are turned on hard, applying power to the relay reset coils. The 200-ohm resistors in series with the 18-volt coils are used to drop the 28-volt output of the IP circuit. As the capacitors are charged, due to the base circuit current, the capacitor voltage reaches a level at which the IP circuit transistors become unsaturated and turn off. This generates a pulse which must have a duration of 3 to 12 milliseconds. When a Read Command is received in the Switch Selector, K17 is energized and shunts the capacitors with the four parallel 680-ohm resistors, discharging the capacitors. The three IP circuits will remain off since the base input is now open. At the completion of the Read Command the Bit Register relays and the Stage Select relays must be reset. K17 is a nonlatching relay which drops out at the end of the Read Command, applying a base input to the three IP circuits which apply power to the reset coils and the cycle repeats.

#### 6-2 DETAILED DESCRIPTION OF ANALYSIS

The reset pulse width is determined by the RC time constant of the capacitors, thermistors, transistor base resistors, diode resistances, and the emitter-base resistances of the transistors. When the transistors are saturated the nonlinear resistances of the transistors and diodes change very little. Then the base circuit can be represented by a single differential equation and the time that the transistors are saturated can be easily calculated. However, when the transistors become unsaturated, the nonlinear resistance must be considered. The capacitance in the base circuit causes the transistor turn off time to be several milliseconds and this turn off time must be calculated. Since the nonlinear characteristics of the transistors and diodes cannot be conveniently represented by equations, a piecewise linear method must be used for calculating the turn off time. Performing the calculations by hand would be very cumbersome and the results would be subject to error. It was decided to employ the PREDICT transient analysis computer program to perform a piecewise linear analysis and determine the total reset pulse width.



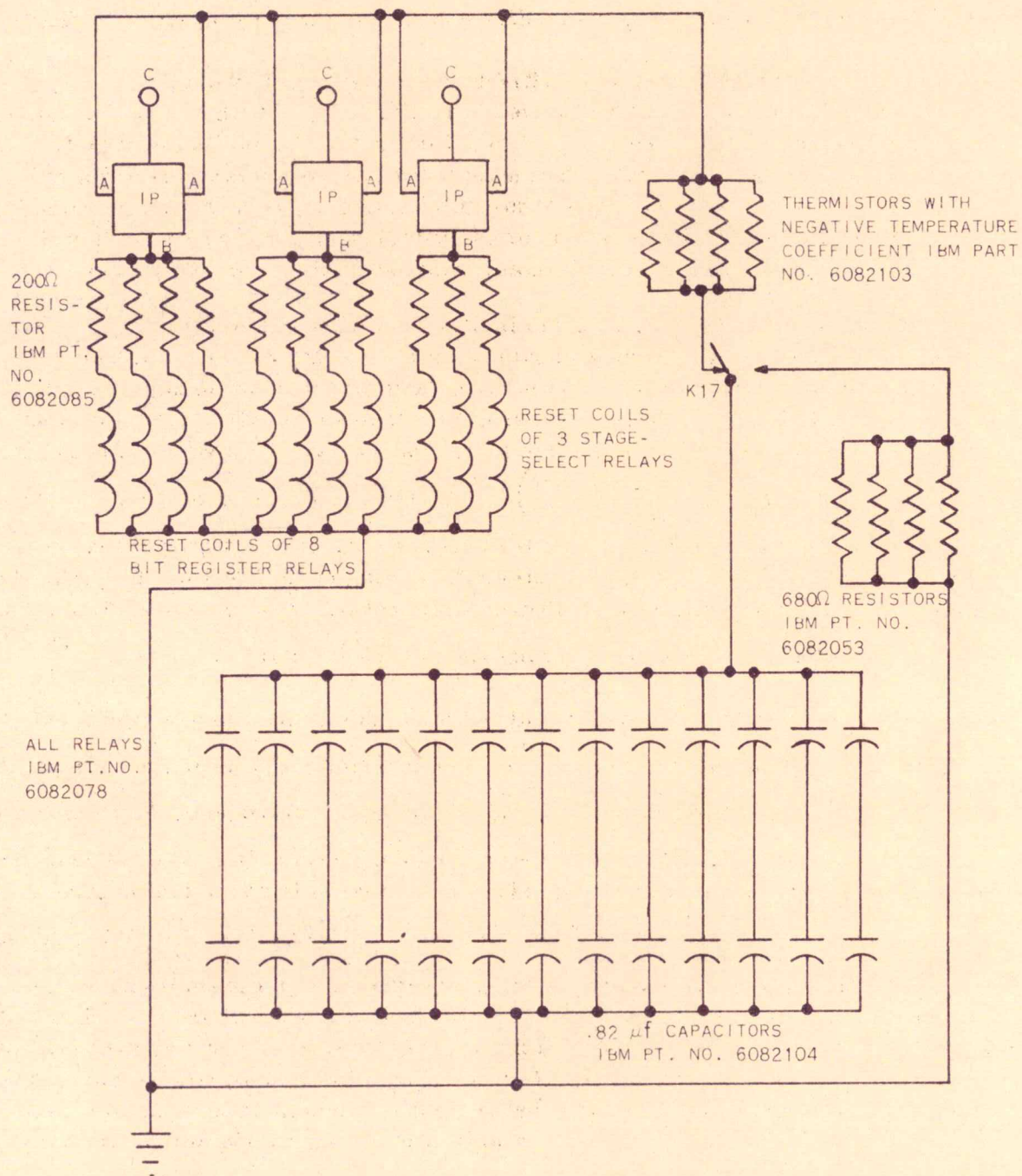


Figure 6-1. Automatic Reset Circuit



The IP circuits used in the reset circuit are of the configuration shown in Figure 5-3 with the addition of a 0.82 microfarad capacitor connected from emitter to base of each transistor. This capacitance provides a necessary delay in the turn on of the IP circuits to prevent interference with other operations in the Switch Selector.

To permit the use of the PREDICT computer program, the reset circuit had to be reduced to a smaller equivalent circuit. As seen in Figure 6-1, the three IP circuits all do not have equal loads. Therefore, it was assumed that since the S2N2907A transistors are saturated for a major portion of the on time and exhibit a high beta during turn off, the small difference in the loads will have a negligible effect on the base circuit which determines the pulse width. Thus, a load of four parallel reset coils and series resistors was assumed for each IP circuit.

With this assumption the total circuit can now be reduced to an equivalent circuit consisting of only one side of an IP circuit with all other circuit components adjusted to maintain the same proportional collector load and the same RC time constant in the base circuit. The equivalent circuit is shown in Figure 6-2. The load resistance, load inductance, thermistors and capacitors are all reduced to equivalent single components. The load resistance is  $R_D + R_L = \left( \frac{200}{4} + \frac{rL}{4} \right)$  ohms, where  $R_D$  is the total parallel dropping resistance and  $R_L$  is the total parallel coil resistance. The load inductance  $L_1 = 0.8/4$  henries, where  $L_1$  is the total parallel coil inductance. To maintain the same proportional load for one-half the IP circuit, the load resistance is  $2 \left( \frac{200}{4} + \frac{rL}{4} \right) = \left( 100 + \frac{rL}{2} \right)$  ohms and the inductance  $L_1$  is  $2 (0.8/4) = 0.4$  henries.

$R_L$  is temperature dependent and is not combined with the voltage dropping resistors.

The equivalent thermistor resistance is  $R_T = \frac{R_t}{4}$ , where  $R_t$  is the individual thermistor resistance and the equivalent capacitance  $C_t = \frac{13C}{2}$ , where  $C$  is the individual

capacitance. The base current which charges the capacitors is now only one-sixth of the current in the actual reset circuit. Therefore, to maintain the same RC time

constant,  $R_T = \frac{R_t}{4} \times 6 = \left( \frac{3R_t}{2} \right)$  ohms and  $C_t = \frac{13C}{2} \times \frac{1}{6} = \frac{13C}{12}$  microfarads.

Unlike the ASAP program, all components are held to a zero percent tolerance for PREDICT. The nonlinear components, transistors and diodes, vary according to the characteristic curves. The reset pulse width was determined for five different operating modes; normal operation at  $-25^\circ$ ,  $+25^\circ$ , and  $+125^\circ\text{C}$  and for two worst-case failure modes to determine the minimum and maximum pulse widths. Each of the failure modes was also investigated to determine the effects of variations in input voltage.



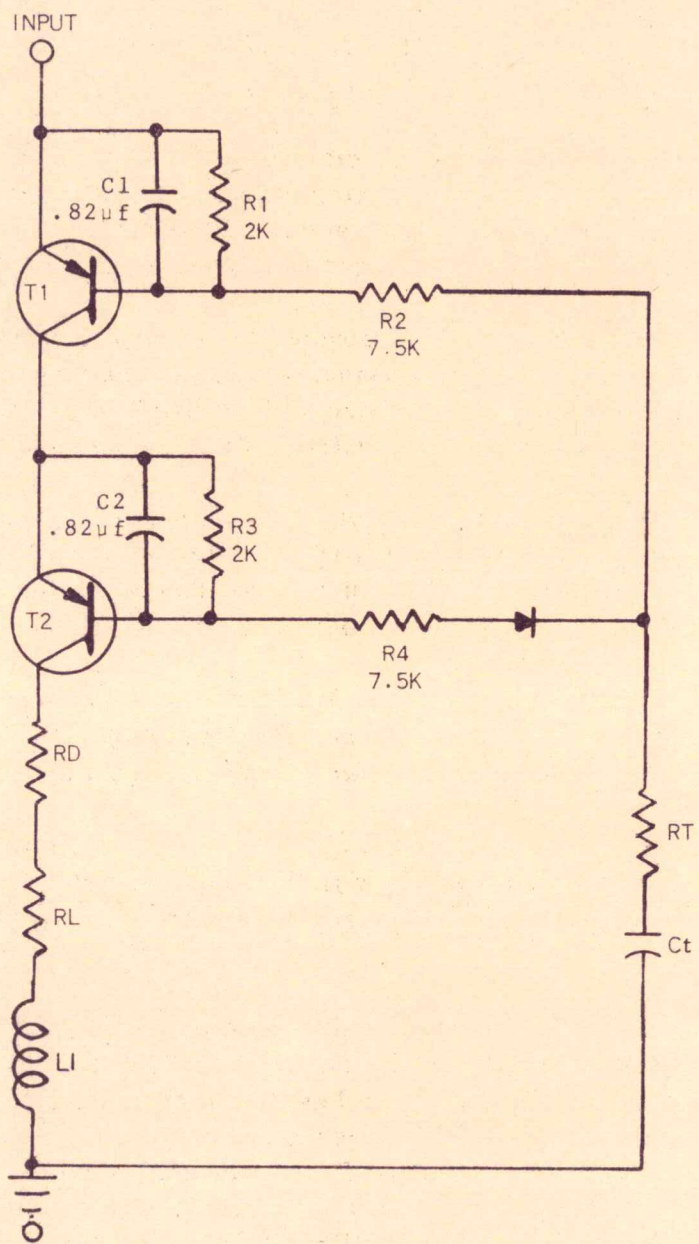


Figure 6-2. Equivalent Automatic Reset Circuit



The following table gives individual component values and tolerances in Figure 6-1 as given in the specifications referenced in Section 3:

|    | <u>-25 °C</u>         | <u>+25 °C</u>         | <u>+125 °C</u>         |
|----|-----------------------|-----------------------|------------------------|
| C  | $0.82 \pm 10\% \mu f$ | $0.82 \pm 10\% \mu f$ | $0.82 \pm 10\% \mu f$  |
| Rt | $3200 \pm 5\% \Omega$ | $333 \pm 10\% \Omega$ | $15.2 \pm 13\% \Omega$ |
| rL | $596 \pm 5\% \Omega$  | $725 \pm 5\% \Omega$  | $1010 \pm 5\% \Omega$  |

In all but one of the failure modes, Ct and RT in the equivalent circuit of Figure 6-2 were set either at the maximum or minimum value. Referring again to Figure 6-1, the total capacitance, Ct, in the capacitor bank will be maximum when one capacitor is shorted and all the remaining capacitors are increased by 10 percent. Ct will be minimum when one capacitor is open and all the remaining capacitors are decreased by 10 percent.

The total thermistor resistance, RT, will be maximum when one thermistor is open and the other thermistors are increased to the given tolerance at the particular temperatures. RT will be minimum when all thermistors are good and decreased to the given tolerance at the particular temperature.

The maximum and minimum load resistance, RL, is calculated using the tolerance specified. The input voltage is  $28 \pm 2$  volts at all temperatures giving a minimum of 26 volts or a maximum of 30 volts. The above methods were followed when calculating the equivalent circuit component values for the failure modes.

Although small changes in RL were considered negligible when deriving the equivalent circuit, changes in RL are considered here to determine the maximum load current and the maximum transistor power dissipation.

The tolerances on components in the IP circuits are very small and were considered negligible when considering worst-case conditions of the reset circuit. Therefore, all modes of operation were analyzed with the components in the IP circuits held at the nominal value.

The nominal reset pulse width was determined at -25°, +25°, and +125 °C for normal operation. Figures II-1, II-2, and II-3 in Appendix II show the relay coil voltage and current, capacitor voltage, and transistor power dissipation with respect to time. The power dissipation shown is for each of the transistors with common collectors. The transistors with common emitters have less than 50-milliwatt maximum power dissipation and the curve is not shown. The rated maximum steady-state power dissipation for the S2N2907A transistor is 400 milliwatts at +25 °C or less and 172 milliwatts at +125 °C. It can be seen in Figure II-3 that at +125 °C the transistor peak power dissipation is approximately 150 percent of rated power and is greater than rated power for approximately 2 milliseconds. At -25 °C power dissipation is greater than rated power for approximately 3 milliseconds. The figures show that the relay coil current is more than sufficient to operate the relay in the allotted time for normal operation at all three temperatures.



The first failure mode considered was worst-case conditions which would cause the reset current pulse width to be maximum. Excluding failures within the IP circuit, the maximum pulse width will occur at  $+125^{\circ}\text{C}$  with maximum  $C_t$ , maximum  $R_T$  and maximum input voltage.  $R_L$  is set at the minimum value to determine the maximum coil current and transistor power dissipation. This tends to decrease the pulse width by causing the transistors to begin cutting off earlier due to the increased load. However, this change is negligible since the tolerance on  $R_L$  is only  $\pm 5$  percent. It will be shown later that even large changes in the load have a negligible effect on the base circuit and the time at which the transistor will be completely cut off. Figure II-4 shows that the maximum reset pulse width under the specified worst-case conditions is within the specified limits. Figure II-5 shows the results of reducing the input voltage to the minimum of 26 volts with all other conditions the same.

Varying the input voltage from one extreme to the other causes less than 0.7-millisecond change in the pulse width. An increase in the input voltage will cause the voltage across the capacitor to increase faster trying to cut the transistors off earlier while the increased input voltage requires the capacitor voltage to be greater for cutoff, tending to keep the transistors on for a longer period of time. A decrease in the input voltage will work in the reverse manner. This self-cancelling effect of the reset circuit tends to minimize the effects of changes in the input voltage at all temperatures.

The same failure mode is now considered except that a worst-case failure in one IP circuit is simulated (by opening  $R_5$  or  $R_7$  in Figure 5-2). This results in less current being available to charge  $C_t$ , causing an increase in the reset pulse width. Since there are now only five charge paths to the capacitor bank, the RC time constant is maintained in the equivalent circuit by using a factor of 5 rather than a factor of 6 as previously shown. Then the worst-case conditions giving the longest reset pulse are still maximum  $C_t$ , maximum  $R_T$  and maximum input voltage with one charge path open. The results are shown in Figure II-6. Curves A, B, and D are characteristic of the two IP circuits without the open diode. As seen the total pulse exceeds the 12-millisecond specification. However, the coil current is less than the minimum operating current at 12 milliseconds.

It will be shown later that the IP circuit with the failure will generate a shorter pulse. Due to the increased load the transistors begin turning off before the normal time. However all three circuits will turn completely off at approximately the same time.

The second failure mode considered was worst-case conditions for the minimum pulse width. Excluding IP circuit component failures, minimum  $C_t$ , minimum  $R_T$  and minimum input voltage at  $-25^{\circ}\text{C}$  will result in the pulse width being minimum. The results are shown in Figure II-7. As seen the pulse width is well within the limits. Figure II-8 shows the results on increasing the input voltage to 30 volts. The pulse width increases by approximately 0.7 milliseconds.



The same worst-case conditions at  $-25^{\circ}\text{C}$  with 26 volts input voltage were again considered with an open resistor in one IP circuit. This condition will increase the charge time of  $C_t$ , increasing the reset pulse width of the two IP circuits without the failure. However, the IP circuit with the failure will begin turning off earlier due to the effective increase in the load current. Figure II-9 shows the characteristics for the circuit with the failure and Figure II-10 for the circuit without the failure.

All of the failure modes thus far tested were considering simultaneous failures. While this is violating ground rules, the reset circuit will still function satisfactorily with these multiple failures.

However, the IP circuit failure which results in the maximum pulse width at  $+125^{\circ}\text{C}$  does not give rise to the minimum pulse width at  $-25^{\circ}\text{C}$ .

Again referring to Figure 5-2, opening the collector of T3 or T4 will double the load on the good side of the circuit while the base circuit and consequently the charge time of  $C_t$  is unchanged. Simulating this circuit failure decreased the pulse width for the failed circuit such that simultaneous failures in RT and  $C_t$  could not be considered. As stated before, however, the Automatic Reset Circuit is required to withstand only one component failure. Figure II-11 shows the results of this failure. The pulse width by definition is less than that required as stated in Section 3. Figure II-12 shows the largest current pulse required to pick any relay which meets the minimum specification requirements. Comparing the rise time and peak currents of the two current pulses, the pulse of Figure II-11 is considered adequate to operate the relays.

It should be noted at this point that as transistor collector current decreases and VCE increases, beta increases. In the case of the 2N2907A, beta increases significantly. Since this change in beta cannot be simulated in the PREDICT computer program, beta was held constant as calculated at the knee of the curve, i.e., for the point at which the transistor begins to saturate. Therefore, the results of the analysis are somewhat pessimistic.

Since Figures II-9 and II-10 represent simultaneous characteristics for different IP circuits, the voltage transient on  $C_t$  is the same as is expected since  $C_t$  is a common component. However, considering the equivalent circuit used for the analysis, it is obvious that the data for both figures were not obtained simultaneously. The conditions were analyzed by changing only the load while holding all other circuit components constant. The fact that the voltage transient on  $C_t$  is the same in both cases supports the original assumption that due to the high beta, the load has a negligible effect on the base current. It can then be concluded that a change in the load on one IP circuit will affect the pulse width at the output of that circuit only.



The capacitors are discharged during the Read Command as stated earlier. The Read Command has a duration of 25 milliseconds. K17 is operated by the Read Command and will close at the latest 6.5 milliseconds after the beginning of the Read Command. It can be considered for worst-case that the relay will drop immediately at the end of the Read Command giving a minimum time of 18.5-millisecond discharge time. Actually, K17 will not drop until several milliseconds after the termination of the Read Command depending on the operating voltage.

Again letting worst-case failures be a maximum of only one 680-ohm resistor opening and a maximum of only one capacitor shorting,  $R = \frac{680}{3} = 227$  ohms and  $C_t = \left( \frac{.82 \times 12}{2} + .82 \right) 1.10 = 6.3$  microfarads. Then for  $C_t$  and  $R$  in parallel and with  $C_t$  initially charged  $V_c = V_i \frac{-t}{RC_t}$ , where  $V_c$  is the time dependent voltage on the capacitors and  $V_i$  is the initial voltage which has a maximum value of 30 volts. Then after 18.5 milliseconds,

$$V_c = 30e^{-\frac{.0185}{227 \times 6.3 \times 10^{-6}}} = 30e^{-12.9} \approx 0. \quad (1)$$

Therefore, the capacitor bank will always have sufficient time to discharge so that the next reset pulse can be properly generated.

The maximum power dissipation in each of the 680-ohm resistors will be  $\frac{(V_i)^2}{R} = \frac{(30)^2}{680} = 1.32$  watts or more than 10 times the rated power dissipation of 125 milliwatts. The time required for the power dissipation to decrease to the rated power is given by:

$$t = \frac{RC}{2} \ln \frac{(V_i)^2}{.125R} = \frac{227 \times 6.3 \times 10^{-6}}{2} \ln \frac{900}{.125 \times 680} = 1.69 \text{ ms} . \quad (2)$$

Now, considering only the 18.5 milliseconds that the 680-ohm resistors are shunting the capacitors, the average power is given by:

$$\begin{aligned} P_{\text{ave}} &= \frac{1}{T} \int_0^T \frac{\left( V_i e^{-\frac{t}{RC_t}} \right)^2}{R} dt , \\ &= \frac{900}{.0185 \times 680} \int_0^{.0185} e^{-\frac{2t}{227 \times 6.5 \times 10^{-6}}} dt , \\ &= 51 \text{ mw} . \end{aligned} \quad (3)$$

$P_{\text{ave}}$  equals 51 milliwatts per resistor for the 18.5-millisecond time period. It should be noted here that K17 will then switch the resistors out of the circuit for the next 15 to 20 milliseconds, making the average power dissipation approximately 25 milliwatts.



In a similar manner the absolute maximum power dissipation in each of the thermistors is 43 milliwatts with the average power being much less. Rated power dissipation is 1 watt.

The 200-ohm voltage dropping resistors in series with the relay coils will have a maximum power dissipation of 240 milliwatts. Average power dissipation will be less than 50 milliwatts in all cases, well below the rated power of 125 milliwatts.

In several cases the transistor power dissipation in the transistors with common collectors have a peak power dissipation greater than rated power. For the worst-case failure mode at  $-25^{\circ}\text{C}$ , the peak power dissipation is 225 percent of rated power and is greater than rated power for approximately 6 milliseconds. Although the average power cannot be calculated directly, it can be estimated with reasonable accuracy and found to be less than 50 percent of rated power for all test cases and less than 25 percent of rated power for most test cases.



## APPENDIX I

### HISTOGRAMS AND WORST-CASE TABULATIONS OF DC ANALYSIS

The following histograms are the statistical distributions of the saturation voltage for all test conditions of the IP and IN circuit dc analysis. The cases in the histograms grouped into 50 class intervals. The left scale indicates the center value of each class interval and is read directly in volts, milliamps, or milliwatts, as applicable. The right scale indicates the number of cases which occurred in each class interval. The scale factor is the approximate number of cases represented by each asterisk.

The following tables of worst-case parameters show the minimum and maximum values of each current, power, and node voltage with respect to ground. These minimum and maximum parameters are the worst-case results for any combination of extreme variations within the tolerance of every component. A component value may be at the minimum or maximum for either the minimum or maximum parameter value. The nominal parameter shown is the result of all components being held at the nominal value. The tables are read by multiplying the number by the power of ten following that number (e.g.,  $2.768910E01 = 27.68910$  or  $2.768910 E-01 = 0.278910$ ) and are read in volts, milliamps or milliwatts as applicable.

The nodes correspond to the respective equivalent circuits of Figure 5-2 and Figure 5-5. The tables for all test conditions are not included.

The histograms and tables are reproductions of the computer printout using the computer notation.



# DISTRIBUTION OF PERFORMANCE PARAMETER T1 FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|           |       |     |
|-----------|-------|-----|
| 14.25177  |       | 1   |
| 16.10782  | *     | 6   |
| 17.96387  | *     | 8   |
| 19.81991  | **    | 13  |
| 21.67596  | **    | 19  |
| 23.53201  | ***   | 27  |
| 25.38805  | ****  | 37  |
| 27.24410  | ***** | 54  |
| 29.10015  | ***** | 73  |
| 30.95619  | ***** | 82  |
| 32.81224  | ***** | 114 |
| 34.66828  | ***** | 148 |
| 36.52433  | ***** | 144 |
| 38.38038  | ***** | 188 |
| 40.23642  | ***** | 230 |
| 42.09247  | ***** | 256 |
| 43.94852  | ***** | 311 |
| 45.80456  | ***** | 326 |
| 47.66061  | ***** | 348 |
| 49.51665  | ***** | 354 |
| 51.37270  | ***** | 440 |
| 53.22875  | ***** | 500 |
| 55.08479  | ***** | 463 |
| 56.94084  | ***** | 439 |
| 58.79689  | ***** | 484 |
| 60.65293  | ***** | 467 |
| 62.50898  | ***** | 468 |
| 64.36502  | ***** | 477 |
| 66.22107  | ***** | 447 |
| 68.07712  | ***** | 436 |
| 69.93316  | ***** | 352 |
| 71.78921  | ***** | 352 |
| 73.64525  | ***** | 329 |
| 75.50130  | ***** | 254 |
| 77.35734  | ***** | 238 |
| 79.21339  | ***** | 201 |
| 81.06944  | ***** | 176 |
| 82.92548  | ***** | 130 |
| 84.78153  | ***** | 140 |
| 86.63757  | ***** | 92  |
| 88.49362  | ***** | 55  |
| 91.34966  | ***** | 41  |
| 92.20571  | ***** | 40  |
| 94.06176  | ***** | 38  |
| 95.91780  | ***   | 27  |
| 97.77385  | **    | 19  |
| 99.62989  | **    | 19  |
| 101.48594 | *     | 9   |
| 103.34198 | *     | 5   |
| 105.19803 |       | 3   |

Figure I-1. Histogram, IP Ckt Transistor Current,  
Normal Operation at +25°C  
for Transistor T1



# DISTRIBUTION OF PERFORMANCE PARAMETER I<sub>T2</sub> FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|           |       |     |
|-----------|-------|-----|
| 17.23448  |       | 3   |
| 19.08792  | *     | 5   |
| 20.94135  | *     | 7   |
| 22.79478  | **    | 17  |
| 24.64822  | **    | 19  |
| 26.50165  | ***   | 26  |
| 28.35508  | ****  | 33  |
| 30.20851  | ***** | 40  |
| 32.06195  | ***** | 42  |
| 33.91538  | ***** | 48  |
| 35.76881  | ***** | 90  |
| 37.62225  | ***** | 132 |
| 39.47568  | ***** | 130 |
| 41.32911  | ***** | 163 |
| 43.18254  | ***** | 197 |
| 45.03598  | ***** | 238 |
| 46.88941  | ***** | 254 |
| 48.74284  | ***** | 304 |
| 50.59627  | ***** | 350 |
| 52.44971  | ***** | 366 |
| 54.30314  | ***** | 425 |
| 56.15657  | ***** | 426 |
| 58.01000  | ***** | 476 |
| 59.86344  | ***** | 475 |
| 61.71687  | ***** | 463 |
| 63.57030  | ***** | 470 |
| 65.42373  | ***** | 460 |
| 67.27717  | ***** | 458 |
| 69.13060  | ***** | 487 |
| 70.98403  | ***** | 448 |
| 72.83747  | ***** | 415 |
| 74.69090  | ***** | 369 |
| 76.54433  | ***** | 329 |
| 78.39776  | ***** | 310 |
| 80.25120  | ***** | 299 |
| 82.10463  | ***** | 234 |
| 83.95806  | ***** | 158 |
| 85.81149  | ***** | 143 |
| 87.66493  | ***** | 146 |
| 89.51836  | ***** | 124 |
| 91.37179  | ***** | 87  |
| 93.22522  | ***** | 73  |
| 95.07866  | ***** | 61  |
| 96.93209  | ***** | 41  |
| 98.78552  | ****  | 30  |
| 100.63896 | **    | 17  |
| 102.49239 | **    | 13  |
| 104.34582 | *     | 10  |
| 106.19925 | *     | 6   |
| 108.05269 |       | 3   |

Figure I-2. Histogram, IP Ckt Transistor Current,  
Normal Operation at +25 °C  
for Transistor T2



# DISTRIBUTION OF PERFORMANCE PARAMETER IT3 FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|           |       |     |
|-----------|-------|-----|
| 10.53966  |       | 1   |
| 12.40032  | *     | 5   |
| 14.26098  | *     | 7   |
| 16.12165  | **    | 16  |
| 17.98231  | **    | 15  |
| 19.84297  | ***   | 26  |
| 21.70363  | ****  | 34  |
| 23.56429  | ***** | 53  |
| 25.42496  | ***** | 72  |
| 27.28562  | ***** | 82  |
| 29.14628  | ***** | 115 |
| 31.00694  | ***** | 142 |
| 32.86761  | ***** | 132 |
| 34.72827  | ***** | 195 |
| 36.58893  | ***** | 221 |
| 38.44959  | ***** | 279 |
| 40.31025  | ***** | 323 |
| 42.17092  | ***** | 314 |
| 44.03158  | ***** | 354 |
| 45.89224  | ***** | 405 |
| 47.75290  | ***** | 427 |
| 49.61356  | ***** | 498 |
| 51.47423  | ***** | 474 |
| 53.33489  | ***** | 442 |
| 55.19555  | ***** | 482 |
| 57.05621  | ***** | 474 |
| 58.91687  | ***** | 468 |
| 60.77753  | ***** | 483 |
| 62.63820  | ***** | 436 |
| 64.49886  | ***** | 438 |
| 66.35952  | ***** | 359 |
| 68.22018  | ***** | 358 |
| 70.08084  | ***** | 332 |
| 71.94150  | ***** | 254 |
| 73.80217  | ***** | 248 |
| 75.66283  | ***** | 197 |
| 77.52349  | ***** | 178 |
| 79.38415  | ***** | 128 |
| 81.24481  | ***** | 143 |
| 83.10547  | ***** | 92  |
| 84.96614  | ***** | 93  |
| 86.82680  | ***** | 49  |
| 88.68746  | ***** | 39  |
| 90.54812  | ****  | 35  |
| 92.40878  | ***   | 26  |
| 94.26944  | ***   | 21  |
| 96.13010  | **    | 17  |
| 97.99077  | *     | 10  |
| 99.85143  | *     | 5   |
| 101.71209 |       | 3   |

Figure I-3. Histogram, IP Ckt Transistor Current  
Normal Operation at +25 °C  
for Transistor T3



# DISTRIBUTION OF PERFORMANCE PARAMETER IT4 FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|           |       |     |
|-----------|-------|-----|
| 13.84867  |       | 3   |
| 15.70280  | *     | 5   |
| 17.55694  | *     | 7   |
| 19.41107  | **    | 18  |
| 21.26521  | ***   | 20  |
| 23.11934  | ***   | 25  |
| 24.97347  | ****  | 34  |
| 26.82761  | ***** | 41  |
| 28.68174  | ***** | 39  |
| 30.53588  | ***** | 51  |
| 32.39001  | ***** | 51  |
| 34.24414  | ***** | 135 |
| 36.09828  | ***** | 131 |
| 37.95241  | ***** | 163 |
| 39.80655  | ***** | 200 |
| 41.66068  | ***** | 242 |
| 43.51481  | ***** | 249 |
| 45.36895  | ***** | 307 |
| 47.22308  | ***** | 358 |
| 49.07722  | ***** | 359 |
| 50.93135  | ***** | 434 |
| 52.78548  | ***** | 423 |
| 54.63962  | ***** | 474 |
| 56.49375  | ***** | 476 |
| 58.34789  | ***** | 465 |
| 60.20202  | ***** | 474 |
| 62.05615  | ***** | 454 |
| 63.91029  | ***** | 468 |
| 65.76442  | ***** | 480 |
| 67.61856  | ***** | 445 |
| 69.47269  | ***** | 425 |
| 71.32682  | ***** | 360 |
| 73.18096  | ***** | 328 |
| 75.03509  | ***** | 314 |
| 76.88922  | ***** | 290 |
| 78.74336  | ***** | 231 |
| 80.59749  | ***** | 192 |
| 82.45162  | ***** | 152 |
| 84.30576  | ***** | 139 |
| 86.15989  | ***** | 125 |
| 88.01403  | ***** | 89  |
| 89.86816  | ***** | 71  |
| 91.72229  | ***** | 57  |
| 93.57643  | ***** | 39  |
| 95.43056  | ****  | 28  |
| 97.28469  | **    | 18  |
| 99.13883  | **    | 13  |
| 100.99296 | *     | 9   |
| 102.84709 | *     | 6   |
| 104.70123 |       | 3   |

Figure I-4. Histogram, IP Ckt Transistor Current  
Normal Operation at +25 °C  
for Transistor T4



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.19282 |       | 1   |
| 0.19716 |       | 0   |
| 0.20150 |       | 1   |
| 0.20584 |       | 2   |
| 0.21018 | *     | 5   |
| 0.21452 | *     | 10  |
| 0.21886 | **    | 14  |
| 0.22320 | ***   | 26  |
| 0.22754 | ****  | 31  |
| 0.23188 | ***** | 54  |
| 0.23622 | ***** | 54  |
| 0.24056 | ***** | 92  |
| 0.24490 | ***** | 108 |
| 0.24924 | ***** | 140 |
| 0.25357 | ***** | 166 |
| 0.25791 | ***** | 218 |
| 0.26225 | ***** | 244 |
| 0.26659 | ***** | 301 |
| 0.27093 | ***** | 339 |
| 0.27527 | ***** | 371 |
| 0.27961 | ***** | 464 |
| 0.28395 | ***** | 438 |
| 0.28829 | ***** | 529 |
| 0.29263 | ***** | 501 |
| 0.29697 | ***** | 516 |
| 0.30131 | ***** | 525 |
| 0.30565 | ***** | 519 |
| 0.30999 | ***** | 512 |
| 0.31433 | ***** | 515 |
| 0.31867 | ***** | 478 |
| 0.32301 | ***** | 440 |
| 0.32735 | ***** | 389 |
| 0.33169 | ***** | 357 |
| 0.33603 | ***** | 354 |
| 0.34037 | ***** | 256 |
| 0.34471 | ***** | 210 |
| 0.34905 | ***** | 216 |
| 0.35339 | ***** | 173 |
| 0.35773 | ***** | 120 |
| 0.36206 | ***** | 82  |
| 0.36640 | ***** | 76  |
| 0.37074 | ***** | 53  |
| 0.37508 | ***** | 43  |
| 0.37942 | ***   | 25  |
| 0.38376 | **    | 17  |
| 0.38810 | *     | 7   |
| 0.39244 |       | 2   |
| 0.39678 | *     | 4   |
| 0.40112 |       | 0   |
| 0.40546 |       | 2   |

Figure I-5. Histogram, IP Ckt Saturation Voltage, Normal Operation at +125 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.21213 |       | 1   |
| 0.21634 |       | 2   |
| 0.22055 |       | 0   |
| 0.22475 | *     | 4   |
| 0.22896 | *     | 11  |
| 0.23317 | **    | 16  |
| 0.23738 | ***   | 27  |
| 0.24159 | ****  | 33  |
| 0.24580 | ***** | 43  |
| 0.25000 | ***** | 62  |
| 0.25421 | ***** | 74  |
| 0.25842 | ***** | 114 |
| 0.26263 | ***** | 116 |
| 0.26684 | ***** | 168 |
| 0.27104 | ***** | 198 |
| 0.27525 | ***** | 253 |
| 0.27946 | ***** | 252 |
| 0.28367 | ***** | 302 |
| 0.28788 | ***** | 377 |
| 0.29209 | ***** | 408 |
| 0.29629 | ***** | 453 |
| 0.30050 | ***** | 460 |
| 0.30471 | ***** | 491 |
| 0.30892 | ***** | 505 |
| 0.31313 | ***** | 484 |
| 0.31733 | ***** | 517 |
| 0.32154 | ***** | 514 |
| 0.32575 | ***** | 496 |
| 0.32996 | ***** | 489 |
| 0.33417 | ***** | 435 |
| 0.33838 | ***** | 421 |
| 0.34258 | ***** | 358 |
| 0.34679 | ***** | 348 |
| 0.35100 | ***** | 321 |
| 0.35521 | ***** | 266 |
| 0.35942 | ***** | 199 |
| 0.36362 | ***** | 194 |
| 0.36783 | ***** | 144 |
| 0.37204 | ***** | 133 |
| 0.37625 | ***** | 81  |
| 0.38046 | ***** | 68  |
| 0.38467 | ***** | 55  |
| 0.38887 | ***** | 47  |
| 0.39308 | ***   | 27  |
| 0.39729 | **    | 17  |
| 0.40150 | *     | 6   |
| 0.40571 | *     | 5   |
| 0.40991 |       | 3   |
| 0.41412 |       | 0   |
| 0.41833 |       | 2   |

Figure I-6. Histogram, IP Ckt Saturation Voltage, Normal Operation at +25 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.21919 |       | 1   |
| 0.22354 |       | 0   |
| 0.22789 |       | 1   |
| 0.23224 |       | 2   |
| 0.23658 | *     | 7   |
| 0.24093 | *     | 8   |
| 0.24528 | ***   | 22  |
| 0.24963 | ***   | 26  |
| 0.25398 | ***** | 37  |
| 0.25833 | ***** | 52  |
| 0.26267 | ***** | 68  |
| 0.26702 | ***** | 81  |
| 0.27137 | ***** | 113 |
| 0.27572 | ***** | 149 |
| 0.28007 | ***** | 204 |
| 0.28442 | ***** | 212 |
| 0.28876 | ***** | 258 |
| 0.29311 | ***** | 296 |
| 0.29746 | ***** | 335 |
| 0.30181 | ***** | 412 |
| 0.30616 | ***** | 455 |
| 0.31051 | ***** | 484 |
| 0.31485 | ***** | 492 |
| 0.31920 | ***** | 526 |
| 0.32355 | ***** | 531 |
| 0.32790 | ***** | 521 |
| 0.33225 | ***** | 495 |
| 0.33660 | ***** | 535 |
| 0.34094 | ***** | 501 |
| 0.34529 | ***** | 456 |
| 0.34964 | ***** | 418 |
| 0.35399 | ***** | 390 |
| 0.35834 | ***** | 359 |
| 0.36269 | ***** | 332 |
| 0.36703 | ***** | 264 |
| 0.37138 | ***** | 200 |
| 0.37573 | ***** | 186 |
| 0.38008 | ***** | 161 |
| 0.38443 | ***** | 111 |
| 0.38878 | ***** | 86  |
| 0.39313 | ***** | 79  |
| 0.39747 | ***** | 42  |
| 0.40182 | ***** | 44  |
| 0.40617 | ***   | 23  |
| 0.41052 | *     | 10  |
| 0.41487 | *     | 7   |
| 0.41922 |       | 3   |
| 0.42356 |       | 3   |
| 0.42791 |       | 1   |
| 0.43226 |       | 1   |

Figure I-7. Histogram, IP Ckt Saturation Voltage, Normal Operation at -25°C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER $V_{CESAT}$ FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.21418 |       | 1   |
| 0.21848 |       | 0   |
| 0.22277 |       | 1   |
| 0.22707 |       | 3   |
| 0.23137 | *     | 4   |
| 0.23566 | *     | 11  |
| 0.23996 | **    | 19  |
| 0.24425 | ***   | 24  |
| 0.24855 | ***** | 37  |
| 0.25284 | ***** | 54  |
| 0.25714 | ***** | 55  |
| 0.26144 | ***** | 90  |
| 0.26573 | ***** | 111 |
| 0.27003 | ***** | 153 |
| 0.27432 | ***** | 169 |
| 0.27862 | ***** | 224 |
| 0.28291 | ***** | 255 |
| 0.28721 | ***** | 291 |
| 0.29150 | ***** | 333 |
| 0.29580 | ***** | 365 |
| 0.30010 | ***** | 473 |
| 0.30439 | ***** | 455 |
| 0.30869 | ***** | 504 |
| 0.31298 | ***** | 507 |
| 0.31728 | ***** | 512 |
| 0.32157 | ***** | 538 |
| 0.32587 | ***** | 499 |
| 0.33016 | ***** | 505 |
| 0.33446 | ***** | 515 |
| 0.33876 | ***** | 465 |
| 0.34305 | ***** | 444 |
| 0.34735 | ***** | 379 |
| 0.35164 | ***** | 359 |
| 0.35594 | ***** | 355 |
| 0.36023 | ***** | 253 |
| 0.36453 | ***** | 221 |
| 0.36882 | ***** | 213 |
| 0.37312 | ***** | 167 |
| 0.37742 | ***** | 121 |
| 0.38171 | ***** | 85  |
| 0.38601 | ***** | 72  |
| 0.39030 | ***** | 52  |
| 0.39460 | ***** | 49  |
| 0.39889 | ***   | 24  |
| 0.40319 | **    | 17  |
| 0.40749 | *     | 8   |
| 0.41178 |       | 2   |
| 0.41608 | *     | 4   |
| 0.42037 |       | 1   |
| 0.42467 |       | 1   |

Figure I-8. Histogram, IP Ckt Saturation Voltage, Normal Operation at +125°C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.23254 |       | 1   |
| 0.23672 |       | 2   |
| 0.24091 |       | 0   |
| 0.24509 | *     | 4   |
| 0.24928 | *     | 10  |
| 0.25346 | **    | 17  |
| 0.25765 | ***   | 25  |
| 0.26183 | ***** | 36  |
| 0.26602 | ***** | 44  |
| 0.27020 | ***** | 62  |
| 0.27439 | ***** | 73  |
| 0.27857 | ***** | 109 |
| 0.28276 | ***** | 123 |
| 0.28695 | ***** | 164 |
| 0.29113 | ***** | 200 |
| 0.29532 | ***** | 253 |
| 0.29950 | ***** | 248 |
| 0.30369 | ***** | 298 |
| 0.30787 | ***** | 382 |
| 0.31206 | ***** | 394 |
| 0.31624 | ***** | 454 |
| 0.32043 | ***** | 466 |
| 0.32461 | ***** | 489 |
| 0.32880 | ***** | 510 |
| 0.33298 | ***** | 468 |
| 0.33717 | ***** | 531 |
| 0.34136 | ***** | 511 |
| 0.34554 | ***** | 483 |
| 0.34973 | ***** | 502 |
| 0.35391 | ***** | 437 |
| 0.35810 | ***** | 413 |
| 0.36228 | ***** | 363 |
| 0.36647 | ***** | 352 |
| 0.37065 | ***** | 318 |
| 0.37484 | ***** | 267 |
| 0.37902 | ***** | 202 |
| 0.38321 | ***** | 198 |
| 0.38739 | ***** | 143 |
| 0.39158 | ***** | 133 |
| 0.39577 | ***** | 80  |
| 0.39995 | ***** | 70  |
| 0.40414 | ***** | 55  |
| 0.40832 | ***** | 49  |
| 0.41251 | ***   | 25  |
| 0.41669 | ***   | 20  |
| 0.42088 | *     | 6   |
| 0.42506 | *     | 5   |
| 0.42925 |       | 3   |
| 0.43343 |       | 0   |
| 0.43762 |       | 2   |

Figure I-9. Histogram, IP Ckt Saturation Voltage, Normal Operation at +25 °C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 9200 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.24001 |       | 1   |
| 0.24432 |       | 0   |
| 0.24862 |       | 1   |
| 0.25293 |       | 2   |
| 0.25724 | *     | 4   |
| 0.26154 | *     | 10  |
| 0.26585 | **    | 18  |
| 0.27016 | ***   | 26  |
| 0.27446 | ***** | 37  |
| 0.27877 | ***** | 40  |
| 0.28308 | ***** | 74  |
| 0.28739 | ***** | 74  |
| 0.29169 | ***** | 103 |
| 0.29600 | ***** | 144 |
| 0.30031 | ***** | 197 |
| 0.30461 | ***** | 199 |
| 0.30892 | ***** | 236 |
| 0.31323 | ***** | 277 |
| 0.31753 | ***** | 311 |
| 0.32184 | ***** | 376 |
| 0.32615 | ***** | 407 |
| 0.33046 | ***** | 439 |
| 0.33476 | ***** | 454 |
| 0.33907 | ***** | 491 |
| 0.34338 | ***** | 476 |
| 0.34768 | ***** | 463 |
| 0.35199 | ***** | 461 |
| 0.35630 | ***** | 483 |
| 0.36060 | ***** | 445 |
| 0.36491 | ***** | 419 |
| 0.36922 | ***** | 396 |
| 0.37353 | ***** | 366 |
| 0.37783 | ***** | 324 |
| 0.38214 | ***** | 302 |
| 0.38645 | ***** | 245 |
| 0.39075 | ***** | 196 |
| 0.39506 | ***** | 168 |
| 0.39937 | ***** | 158 |
| 0.40367 | ***** | 107 |
| 0.40798 | ***** | 77  |
| 0.41229 | ***** | 71  |
| 0.41660 | ***** | 37  |
| 0.42090 | ***** | 40  |
| 0.42521 | ***   | 20  |
| 0.42952 | **    | 12  |
| 0.43382 | *     | 7   |
| 0.43813 |       | 3   |
| 0.44244 |       | 1   |
| 0.44674 |       | 1   |
| 0.45105 |       | 1   |

Figure I-10. Histogram, IP Ckt Saturation Voltage, Normal Operation at -25 °C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.27951 |       | 1   |
| 0.28466 |       | 3   |
| 0.28981 |       | 1   |
| 0.29497 | **    | 13  |
| 0.30012 | **    | 18  |
| 0.30528 | ****  | 34  |
| 0.31043 | ***** | 51  |
| 0.31559 | ***** | 72  |
| 0.32074 | ***** | 85  |
| 0.32590 | ***** | 98  |
| 0.33105 | ***** | 152 |
| 0.33621 | ***** | 144 |
| 0.34136 | ***** | 168 |
| 0.34652 | ***** | 220 |
| 0.35167 | ***** | 257 |
| 0.35683 | ***** | 277 |
| 0.36198 | ***** | 293 |
| 0.36714 | ***** | 307 |
| 0.37229 | ***** | 316 |
| 0.37744 | ***** | 347 |
| 0.38260 | ***** | 364 |
| 0.38775 | ***** | 428 |
| 0.39291 | ***** | 427 |
| 0.39806 | ***** | 453 |
| 0.40322 | ***** | 465 |
| 0.40837 | ***** | 449 |
| 0.41353 | ***** | 448 |
| 0.41868 | ***** | 425 |
| 0.42384 | ***** | 390 |
| 0.42899 | ***** | 406 |
| 0.43415 | ***** | 351 |
| 0.43930 | ***** | 332 |
| 0.44446 | ***** | 348 |
| 0.44961 | ***** | 276 |
| 0.45477 | ***** | 260 |
| 0.45992 | ***** | 211 |
| 0.46507 | ***** | 209 |
| 0.47023 | ***** | 197 |
| 0.47538 | ***** | 160 |
| 0.48054 | ***** | 135 |
| 0.48569 | ***** | 103 |
| 0.49085 | ***** | 111 |
| 0.49600 | ***** | 75  |
| 0.50116 | ***** | 46  |
| 0.50631 | ***   | 27  |
| 0.51147 | ***   | 21  |
| 0.51662 | *     | 11  |
| 0.52178 | *     | 11  |
| 0.52693 |       | 2   |
| 0.53209 |       | 2   |

Figure I-11. Histogram, IP Ckt Saturation Voltage, Transistor Open at +125 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.30007 |       | 1   |
| 0.30524 |       | 3   |
| 0.31040 |       | 3   |
| 0.31557 | *     | 10  |
| 0.32073 | ***   | 20  |
| 0.32590 | ****  | 34  |
| 0.33106 | ***** | 51  |
| 0.33622 | ***** | 72  |
| 0.34139 | ***** | 89  |
| 0.34655 | ***** | 105 |
| 0.35172 | ***** | 152 |
| 0.35688 | ***** | 146 |
| 0.36204 | ***** | 158 |
| 0.36721 | ***** | 226 |
| 0.37237 | ***** | 264 |
| 0.37754 | ***** | 278 |
| 0.38270 | ***** | 271 |
| 0.38787 | ***** | 322 |
| 0.39303 | ***** | 327 |
| 0.39819 | ***** | 337 |
| 0.40336 | ***** | 374 |
| 0.40852 | ***** | 406 |
| 0.41369 | ***** | 434 |
| 0.41885 | ***** | 464 |
| 0.42402 | ***** | 462 |
| 0.42918 | ***** | 469 |
| 0.43434 | ***** | 429 |
| 0.43951 | ***** | 419 |
| 0.44467 | ***** | 388 |
| 0.44984 | ***** | 394 |
| 0.45500 | ***** | 381 |
| 0.46016 | ***** | 322 |
| 0.46533 | ***** | 351 |
| 0.47049 | ***** | 266 |
| 0.47566 | ***** | 247 |
| 0.48082 | ***** | 213 |
| 0.48599 | ***** | 217 |
| 0.49115 | ***** | 191 |
| 0.49631 | ***** | 158 |
| 0.50148 | ***** | 143 |
| 0.50664 | ***** | 99  |
| 0.51181 | ***** | 115 |
| 0.51697 | ***** | 61  |
| 0.52214 | ***** | 54  |
| 0.52730 | ***   | 22  |
| 0.53246 | ***   | 25  |
| 0.53763 | *     | 10  |
| 0.54279 | *     | 10  |
| 0.54796 | *     | 5   |
| 0.55312 |       | 2   |

Figure I-12. Histogram, IP Ckt Saturation Voltage, Transistor Open at +25 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORIGINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.31877 |       | 2   |
| 0.32398 |       | 3   |
| 0.32920 | *     | 6   |
| 0.33441 | *     | 11  |
| 0.33962 | ***   | 20  |
| 0.34484 | ***** | 40  |
| 0.35005 | ***** | 57  |
| 0.35526 | ***** | 66  |
| 0.36048 | ***** | 92  |
| 0.36569 | ***** | 119 |
| 0.37091 | ***** | 145 |
| 0.37612 | ***** | 153 |
| 0.38133 | ***** | 186 |
| 0.38655 | ***** | 209 |
| 0.39176 | ***** | 262 |
| 0.39698 | ***** | 292 |
| 0.40219 | ***** | 283 |
| 0.40740 | ***** | 306 |
| 0.41262 | ***** | 341 |
| 0.41783 | ***** | 358 |
| 0.42304 | ***** | 369 |
| 0.42826 | ***** | 400 |
| 0.43347 | ***** | 461 |
| 0.43869 | ***** | 451 |
| 0.44390 | ***** | 483 |
| 0.44911 | ***** | 452 |
| 0.45433 | ***** | 447 |
| 0.45954 | ***** | 383 |
| 0.46476 | ***** | 395 |
| 0.46997 | ***** | 376 |
| 0.47518 | ***** | 404 |
| 0.48040 | ***** | 329 |
| 0.48561 | ***** | 310 |
| 0.49082 | ***** | 291 |
| 0.49604 | ***** | 222 |
| 0.50125 | ***** | 214 |
| 0.50647 | ***** | 220 |
| 0.51168 | ***** | 178 |
| 0.51689 | ***** | 143 |
| 0.52211 | ***** | 134 |
| 0.52732 | ***** | 107 |
| 0.53254 | ***** | 102 |
| 0.53775 | ***** | 55  |
| 0.54296 | ***** | 40  |
| 0.54818 | ****  | 35  |
| 0.55339 | **    | 19  |
| 0.55860 | *     | 11  |
| 0.56382 | *     | 11  |
| 0.56903 | *     | 4   |
| 0.57425 |       | 3   |

Figure I-13. Histogram, IP Ckt Saturation Voltage, Transistor Open at -25 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.30065 |       | 1   |
| 0.30579 |       | 3   |
| 0.31093 |       | 1   |
| 0.31607 | **    | 13  |
| 0.32121 | **    | 16  |
| 0.32635 | ****  | 35  |
| 0.33149 | ***** | 50  |
| 0.33662 | ***** | 74  |
| 0.34176 | ***** | 84  |
| 0.34690 | ***** | 102 |
| 0.35204 | ***** | 152 |
| 0.35718 | ***** | 147 |
| 0.36232 | ***** | 163 |
| 0.36746 | ***** | 221 |
| 0.37259 | ***** | 264 |
| 0.37773 | ***** | 273 |
| 0.38287 | ***** | 294 |
| 0.38801 | ***** | 314 |
| 0.39315 | ***** | 312 |
| 0.39829 | ***** | 352 |
| 0.40343 | ***** | 350 |
| 0.40857 | ***** | 435 |
| 0.41370 | ***** | 427 |
| 0.41884 | ***** | 448 |
| 0.42398 | ***** | 478 |
| 0.42912 | ***** | 454 |
| 0.43426 | ***** | 438 |
| 0.43940 | ***** | 417 |
| 0.44454 | ***** | 409 |
| 0.44968 | ***** | 394 |
| 0.45481 | ***** | 358 |
| 0.45995 | ***** | 322 |
| 0.46509 | ***** | 346 |
| 0.47023 | ***** | 275 |
| 0.47537 | ***** | 259 |
| 0.48051 | ***** | 219 |
| 0.48565 | ***** | 199 |
| 0.49078 | ***** | 199 |
| 0.49592 | ***** | 159 |
| 0.50106 | ***** | 136 |
| 0.50620 | ***** | 99  |
| 0.51134 | ***** | 113 |
| 0.51648 | ***** | 78  |
| 0.52162 | ***** | 45  |
| 0.52676 | ***   | 26  |
| 0.53189 | ***   | 20  |
| 0.53703 | **    | 12  |
| 0.54217 | *     | 10  |
| 0.54731 |       | 2   |
| 0.55245 |       | 2   |

Figure I-14. Histogram, IP Ckt Saturation Voltage, Transistor Open at +125°C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.32113 |       | 1   |
| 0.32828 |       | 3   |
| 0.33143 |       | 3   |
| 0.33857 | *     | 10  |
| 0.34172 | ***   | 21  |
| 0.34687 | ***** | 34  |
| 0.35202 | ***** | 51  |
| 0.35717 | ***** | 71  |
| 0.36231 | ***** | 90  |
| 0.36746 | ***** | 107 |
| 0.37261 | ***** | 154 |
| 0.37776 | ***** | 146 |
| 0.38291 | ***** | 160 |
| 0.38805 | ***** | 224 |
| 0.39320 | ***** | 270 |
| 0.39835 | ***** | 272 |
| 0.40350 | ***** | 281 |
| 0.40865 | ***** | 317 |
| 0.41379 | ***** | 328 |
| 0.41894 | ***** | 334 |
| 0.42409 | ***** | 371 |
| 0.42924 | ***** | 412 |
| 0.43439 | ***** | 429 |
| 0.43953 | ***** | 466 |
| 0.44468 | ***** | 458 |
| 0.44983 | ***** | 472 |
| 0.45498 | ***** | 431 |
| 0.46013 | ***** | 420 |
| 0.46527 | ***** | 385 |
| 0.47042 | ***** | 397 |
| 0.47557 | ***** | 378 |
| 0.48072 | ***** | 325 |
| 0.48587 | ***** | 338 |
| 0.49102 | ***** | 266 |
| 0.49617 | ***** | 255 |
| 0.50131 | ***** | 215 |
| 0.50646 | ***** | 214 |
| 0.51161 | ***** | 186 |
| 0.51676 | ***** | 163 |
| 0.52190 | ***** | 146 |
| 0.52705 | ***** | 90  |
| 0.53220 | ***** | 119 |
| 0.53735 | ***** | 60  |
| 0.54249 | ***** | 55  |
| 0.54764 | ***   | 20  |
| 0.55279 | ***   | 26  |
| 0.55794 | *     | 9   |
| 0.56309 | *     | 10  |
| 0.56823 | *     | 5   |
| 0.57338 |       | 2   |

Figure I-15. Histogram, IP Ckt Saturation Voltage, Transistor Open at +25 °C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.33973 |       | 2   |
| 0.34649 | *     | 4   |
| 0.35324 | **    | 12  |
| 0.35999 | ***   | 27  |
| 0.36674 | ***** | 52  |
| 0.37349 | ***** | 79  |
| 0.38024 | ***** | 111 |
| 0.38699 | ***** | 137 |
| 0.39374 | ***** | 181 |
| 0.40049 | ***** | 223 |
| 0.40724 | ***** | 257 |
| 0.41399 | ***** | 333 |
| 0.42074 | ***** | 367 |
| 0.42750 | ***** | 372 |
| 0.43425 | ***** | 395 |
| 0.44100 | ***** | 475 |
| 0.44775 | ***** | 513 |
| 0.45450 | ***** | 561 |
| 0.46125 | ***** | 573 |
| 0.46800 | ***** | 575 |
| 0.47475 | ***** | 573 |
| 0.48150 | ***** | 460 |
| 0.48825 | ***** | 517 |
| 0.49500 | ***** | 491 |
| 0.50175 | ***** | 428 |
| 0.50850 | ***** | 401 |
| 0.51525 | ***** | 326 |
| 0.52200 | ***** | 273 |
| 0.52875 | ***** | 279 |
| 0.53550 | ***** | 246 |
| 0.54225 | ***** | 174 |
| 0.54900 | ***** | 166 |
| 0.55575 | ***** | 127 |
| 0.56250 | ***** | 91  |
| 0.56925 | ***** | 52  |
| 0.57600 | ***** | 46  |
| 0.58275 | ***** | 39  |
| 0.58950 | ***   | 21  |
| 0.59625 | *     | 8   |
| 0.60300 | **    | 14  |
| 0.60975 | *     | 10  |
| 0.61650 |       | 3   |
| 0.62325 |       | 0   |
| 0.63000 |       | 3   |
| 0.63675 |       | 1   |
| 0.64350 |       | 0   |
| 0.65025 |       | 0   |
| 0.65700 |       | 1   |
| 0.66375 |       | 0   |
| 0.67050 |       | 1   |

Figure I-16. Histogram, IP Ckt Saturation Voltage, Transistor  
Open at -25°C, Gated Input = 24 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 6720 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|         |       |     |
|---------|-------|-----|
| 0.12946 |       | 1   |
| 0.13262 | *     | 3   |
| 0.13577 | *     | 3   |
| 0.13893 | *     | 3   |
| 0.14208 | **    | 8   |
| 0.14524 | ***   | 11  |
| 0.14839 | ***** | 26  |
| 0.15155 | ***** | 40  |
| 0.15470 | ***** | 80  |
| 0.15786 | ***** | 81  |
| 0.16101 | ***** | 100 |
| 0.16417 | ***** | 147 |
| 0.16733 | ***** | 133 |
| 0.17048 | ***** | 198 |
| 0.17364 | ***** | 192 |
| 0.17679 | ***** | 244 |
| 0.17995 | ***** | 217 |
| 0.18310 | ***** | 238 |
| 0.18626 | ***** | 273 |
| 0.18941 | ***** | 272 |
| 0.19257 | ***** | 270 |
| 0.19572 | ***** | 271 |
| 0.19888 | ***** | 270 |
| 0.20204 | ***** | 262 |
| 0.20519 | ***** | 274 |
| 0.20835 | ***** | 316 |
| 0.21150 | ***** | 264 |
| 0.21466 | ***** | 271 |
| 0.21781 | ***** | 231 |
| 0.22097 | ***** | 285 |
| 0.22412 | ***** | 238 |
| 0.22728 | ***** | 250 |
| 0.23044 | ***** | 232 |
| 0.23359 | ***** | 179 |
| 0.23675 | ***** | 167 |
| 0.23990 | ***** | 145 |
| 0.24306 | ***** | 125 |
| 0.24621 | ***** | 109 |
| 0.24937 | ***** | 77  |
| 0.25252 | ***** | 63  |
| 0.25568 | ***** | 52  |
| 0.25883 | ***** | 40  |
| 0.26199 | ***** | 23  |
| 0.26515 | ***   | 10  |
| 0.26830 | ***   | 11  |
| 0.27146 | *     | 4   |
| 0.27461 | *     | 3   |
| 0.27777 | *     | 5   |
| 0.28092 |       | 1   |
| 0.28408 | *     | 2   |

Figure I-17. Histogram, IP Ckt Saturation Voltage, Transistor Shorted at +125°C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 10000 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.13457 |       | 1   |
| 0.13780 |       | 0   |
| 0.14103 |       | 1   |
| 0.14425 | *     | 6   |
| 0.14748 | *     | 6   |
| 0.15070 | *     | 11  |
| 0.15393 | ***   | 22  |
| 0.15716 | ****  | 33  |
| 0.16038 | ***** | 60  |
| 0.16361 | ***** | 97  |
| 0.16683 | ***** | 114 |
| 0.17006 | ***** | 165 |
| 0.17329 | ***** | 199 |
| 0.17651 | ***** | 204 |
| 0.17974 | ***** | 277 |
| 0.18296 | ***** | 306 |
| 0.18619 | ***** | 351 |
| 0.18942 | ***** | 330 |
| 0.19264 | ***** | 405 |
| 0.19587 | ***** | 409 |
| 0.19909 | ***** | 395 |
| 0.20232 | ***** | 409 |
| 0.20555 | ***** | 422 |
| 0.20877 | ***** | 447 |
| 0.21200 | ***** | 373 |
| 0.21523 | ***** | 442 |
| 0.21845 | ***** | 456 |
| 0.22168 | ***** | 409 |
| 0.22490 | ***** | 407 |
| 0.22813 | ***** | 381 |
| 0.23136 | ***** | 389 |
| 0.23458 | ***** | 379 |
| 0.23781 | ***** | 337 |
| 0.24103 | ***** | 306 |
| 0.24426 | ***** | 291 |
| 0.24749 | ***** | 233 |
| 0.25071 | ***** | 240 |
| 0.25394 | ***** | 183 |
| 0.25716 | ***** | 129 |
| 0.26039 | ***** | 100 |
| 0.26362 | ***** | 88  |
| 0.26684 | ***** | 74  |
| 0.27007 | ***** | 43  |
| 0.27329 | ***   | 24  |
| 0.27652 | **    | 16  |
| 0.27975 | **    | 14  |
| 0.28297 | *     | 6   |
| 0.28620 | *     | 7   |
| 0.28942 |       | 1   |
| 0.29265 |       | 2   |

Figure I-18. Histogram, IP Ckt Saturation Voltage, Transistor Shorted at +25 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER VCESAT FOR 4675 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|         |       |     |
|---------|-------|-----|
| 0.14513 |       | 1   |
| 0.14843 |       | 1   |
| 0.15173 | *     | 3   |
| 0.15503 | *     | 3   |
| 0.15833 | *     | 5   |
| 0.16163 | ***   | 12  |
| 0.16493 | ****  | 14  |
| 0.16822 | ***** | 18  |
| 0.17152 | ***** | 49  |
| 0.17482 | ***** | 57  |
| 0.17812 | ***** | 64  |
| 0.18142 | ***** | 98  |
| 0.18472 | ***** | 94  |
| 0.18802 | ***** | 136 |
| 0.19131 | ***** | 128 |
| 0.19461 | ***** | 139 |
| 0.19791 | ***** | 169 |
| 0.20121 | ***** | 175 |
| 0.20451 | ***** | 184 |
| 0.20781 | ***** | 182 |
| 0.21111 | ***** | 174 |
| 0.21441 | ***** | 187 |
| 0.21770 | ***** | 206 |
| 0.22100 | ***** | 190 |
| 0.22430 | ***** | 210 |
| 0.22760 | ***** | 200 |
| 0.23090 | ***** | 189 |
| 0.23420 | ***** | 194 |
| 0.23750 | ***** | 209 |
| 0.24079 | ***** | 182 |
| 0.24409 | ***** | 155 |
| 0.24739 | ***** | 172 |
| 0.25069 | ***** | 170 |
| 0.25399 | ***** | 147 |
| 0.25729 | ***** | 123 |
| 0.26059 | ***** | 86  |
| 0.26389 | ***** | 78  |
| 0.26718 | ***** | 66  |
| 0.27048 | ***** | 49  |
| 0.27378 | ***** | 49  |
| 0.27708 | ***** | 43  |
| 0.28038 | ***** | 22  |
| 0.28368 | ***** | 13  |
| 0.28698 | **    | 6   |
| 0.29028 | **    | 9   |
| 0.29357 | *     | 4   |
| 0.29687 | **    | 6   |
| 0.30017 |       | 0   |
| 0.30347 | *     | 3   |
| 0.30677 |       | 1   |

Figure I-19. Histogram, IP Ckt Saturation Voltage, Transistor Shorted at -25 °C, Gated Input = 28 V



# DISTRIBUTION OF PERFORMANCE PARAMETER IT1 FOR 5578 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|          |       |     |
|----------|-------|-----|
| 0.50268  |       | 1   |
| 1.53362  | *     | 2   |
| 2.56456  |       | 0   |
| 3.59551  | **    | 8   |
| 4.62645  | ***   | 11  |
| 5.65739  | ***** | 22  |
| 6.68833  | ***** | 30  |
| 7.71927  | ***** | 47  |
| 8.75021  | ***** | 50  |
| 9.78115  | ***** | 64  |
| 10.81210 | ***** | 75  |
| 11.84304 | ***** | 111 |
| 12.87398 | ***** | 125 |
| 13.90492 | ***** | 151 |
| 14.93586 | ***** | 180 |
| 15.96680 | ***** | 143 |
| 16.99774 | ***** | 157 |
| 18.02869 | ***** | 184 |
| 19.05963 | ***** | 157 |
| 20.09057 | ***** | 188 |
| 21.12151 | ***** | 214 |
| 22.15245 | ***** | 217 |
| 23.18339 | ***** | 214 |
| 24.21433 | ***** | 219 |
| 25.24528 | ***** | 228 |
| 26.27622 | ***** | 211 |
| 27.30716 | ***** | 237 |
| 28.33810 | ***** | 218 |
| 29.36904 | ***** | 210 |
| 30.39998 | ***** | 178 |
| 31.43093 | ***** | 207 |
| 32.46187 | ***** | 173 |
| 33.49281 | ***** | 176 |
| 34.52375 | ***** | 168 |
| 35.55469 | ***** | 180 |
| 36.58563 | ***** | 180 |
| 37.61657 | ***** | 141 |
| 38.64752 | ***** | 123 |
| 39.67846 | ***** | 84  |
| 40.70940 | ***** | 82  |
| 41.74034 | ***** | 50  |
| 42.77128 | ***** | 46  |
| 43.80222 | ***** | 44  |
| 44.83316 | ***** | 27  |
| 45.86411 | ***** | 19  |
| 46.89505 | ***   | 12  |
| 47.92599 | **    | 7   |
| 48.95693 | **    | 6   |
| 49.98787 |       | 0   |
| 51.01881 |       | 1   |

Figure I-20. Histogram, IN Transistor Current Normal Operation at +25 °C for Transistor T1



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|          |       |     |
|----------|-------|-----|
| 0.49144  |       | 1   |
| 1.52168  |       | 0   |
| 2.55191  | **    | 6   |
| 3.58215  | **    | 7   |
| 4.61239  | ****  | 14  |
| 5.64263  | ***** | 20  |
| 6.67287  | ***** | 24  |
| 7.70311  | ***** | 44  |
| 8.73334  | ***** | 46  |
| 9.76358  | ***** | 52  |
| 10.79382 | ***** | 82  |
| 11.82406 | ***** | 86  |
| 12.85430 | ***** | 124 |
| 13.88454 | ***** | 137 |
| 14.91477 | ***** | 184 |
| 15.94501 | ***** | 178 |
| 16.97525 | ***** | 169 |
| 18.00549 | ***** | 173 |
| 19.03573 | ***** | 178 |
| 20.06597 | ***** | 210 |
| 21.09620 | ***** | 175 |
| 22.12644 | ***** | 207 |
| 23.15668 | ***** | 222 |
| 24.18692 | ***** | 235 |
| 25.21716 | ***** | 210 |
| 26.24739 | ***** | 230 |
| 27.27763 | ***** | 218 |
| 28.30787 | ***** | 215 |
| 29.33811 | ***** | 218 |
| 30.36835 | ***** | 209 |
| 31.39859 | ***** | 189 |
| 32.42882 | ***** | 159 |
| 33.45906 | ***** | 179 |
| 34.48930 | ***** | 164 |
| 35.51954 | ***** | 141 |
| 36.54978 | ***** | 175 |
| 37.58001 | ***** | 154 |
| 38.61025 | ***** | 125 |
| 39.64049 | ***** | 110 |
| 40.67073 | ***** | 74  |
| 41.70097 | ***** | 63  |
| 42.73120 | ***** | 50  |
| 43.76144 | ***** | 46  |
| 44.79168 | ***** | 31  |
| 45.82192 | ***** | 22  |
| 46.85216 | ***   | 11  |
| 47.88240 | **    | 8   |
| 48.91263 |       | 0   |
| 49.94287 | *     | 2   |
| 50.97311 |       | 1   |

Figure I-21. Histogram, IN Transistor Current Normal  
Operation at +25 °C for Transistor T2



# DISTRIBUTION OF PERFORMANCE PARAMETER IT3 FOR 5578 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|          |       |     |
|----------|-------|-----|
| 1.49117  |       | 1   |
| 2.52175  | *     | 2   |
| 3.55233  |       | 0   |
| 4.58291  | **    | 7   |
| 5.61348  | ***   | 12  |
| 6.64406  | ***** | 22  |
| 7.67464  | ***** | 30  |
| 8.70522  | ***** | 47  |
| 9.73579  | ***** | 50  |
| 10.76637 | ***** | 63  |
| 11.79695 | ***** | 76  |
| 12.82753 | ***** | 110 |
| 13.85810 | ***** | 123 |
| 14.88868 | ***** | 153 |
| 15.91926 | ***** | 180 |
| 16.94984 | ***** | 139 |
| 17.98041 | ***** | 162 |
| 19.01099 | ***** | 183 |
| 20.04157 | ***** | 156 |
| 21.07214 | ***** | 194 |
| 22.10272 | ***** | 208 |
| 23.13330 | ***** | 215 |
| 24.16388 | ***** | 217 |
| 25.19445 | ***** | 217 |
| 26.22503 | ***** | 227 |
| 27.25561 | ***** | 214 |
| 28.28619 | ***** | 235 |
| 29.31676 | ***** | 222 |
| 30.34734 | ***** | 207 |
| 31.37792 | ***** | 180 |
| 32.40850 | ***** | 201 |
| 33.43907 | ***** | 178 |
| 34.46965 | ***** | 176 |
| 35.50023 | ***** | 167 |
| 36.53081 | ***** | 182 |
| 37.56138 | ***** | 179 |
| 38.59196 | ***** | 138 |
| 39.62254 | ***** | 125 |
| 40.65311 | ***** | 84  |
| 41.68369 | ***** | 84  |
| 42.71427 | ***** | 50  |
| 43.74485 | ***** | 47  |
| 44.77542 | ***** | 42  |
| 45.80600 | ***** | 26  |
| 46.83658 | ***** | 20  |
| 47.86715 | ***   | 13  |
| 48.89773 | **    | 7   |
| 49.92831 | **    | 6   |
| 50.95889 |       | 0   |
| 51.98946 |       | 1   |

Figure I-22. Histogram, IN Transistor Current Normal Operation at +25 °C for Transistor T3



DISTRIBUTION OF PERFORMANCE PARAMETER IT<sub>4</sub> FOR 5578 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|          |       |     |
|----------|-------|-----|
| 1.44462  |       | 1   |
| 2.47550  |       | 0   |
| 3.50637  | **    | 6   |
| 4.53724  | **    | 7   |
| 5.56812  | ***   | 12  |
| 6.59899  | ***** | 20  |
| 7.62987  | ***** | 25  |
| 8.66074  | ***** | 42  |
| 9.69161  | ***** | 49  |
| 10.72249 | ***** | 51  |
| 11.75336 | ***** | 81  |
| 12.78423 | ***** | 86  |
| 13.81511 | ***** | 123 |
| 14.84598 | ***** | 140 |
| 15.87686 | ***** | 183 |
| 16.90773 | ***** | 176 |
| 17.93860 | ***** | 168 |
| 18.96948 | ***** | 177 |
| 20.00035 | ***** | 175 |
| 21.03122 | ***** | 204 |
| 22.06210 | ***** | 179 |
| 23.09297 | ***** | 209 |
| 24.12384 | ***** | 220 |
| 25.15472 | ***** | 238 |
| 26.18559 | ***** | 211 |
| 27.21646 | ***** | 228 |
| 28.24734 | ***** | 220 |
| 29.27821 | ***** | 213 |
| 30.30908 | ***** | 218 |
| 31.33996 | ***** | 207 |
| 32.37083 | ***** | 191 |
| 33.40170 | ***** | 160 |
| 34.43258 | ***** | 180 |
| 35.46345 | ***** | 161 |
| 36.49432 | ***** | 142 |
| 37.52520 | ***** | 176 |
| 38.55607 | ***** | 153 |
| 39.58694 | ***** | 128 |
| 40.61782 | ***** | 106 |
| 41.64869 | ***** | 78  |
| 42.67956 | ***** | 63  |
| 43.71044 | ***** | 51  |
| 44.74131 | ***** | 43  |
| 45.77218 | ***** | 33  |
| 46.80306 | ***** | 22  |
| 47.83393 | ***   | 10  |
| 48.86480 | **    | 9   |
| 49.89568 |       | 0   |
| 50.92655 | *     | 2   |
| 51.95742 |       | 1   |

Figure I-23. Histogram, IN Transistor Current Normal Operation at +25 °C for Transistor T4



DISTRIBUTION OF PERFORMANCE PARAMETER V1 FOR 361 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 4

|         |       |    |
|---------|-------|----|
| 0.13732 | ****  | 1  |
| 0.14049 |       | 0  |
| 0.14366 |       | 0  |
| 0.14684 | ***** | 2  |
| 0.15001 |       | 0  |
| 0.15318 | ****  | 1  |
| 0.15636 | ***** | 2  |
| 0.15953 | ****  | 1  |
| 0.16270 | ***** | 6  |
| 0.16588 | ***** | 5  |
| 0.16905 | ***** | 4  |
| 0.17222 | ***** | 6  |
| 0.17540 | ***** | 6  |
| 0.17857 | ***** | 6  |
| 0.18175 | ***** | 15 |
| 0.18492 | ***** | 8  |
| 0.18809 | ***** | 11 |
| 0.19127 | ***** | 9  |
| 0.19444 | ***** | 9  |
| 0.19761 | ***** | 13 |
| 0.20079 | ***** | 13 |
| 0.20396 | ***** | 13 |
| 0.20713 | ***** | 11 |
| 0.21031 | ***** | 16 |
| 0.21348 | ***** | 12 |
| 0.21665 | ***** | 19 |
| 0.21983 | ***** | 10 |
| 0.22300 | ***** | 11 |
| 0.22617 | ***** | 19 |
| 0.22935 | ***** | 15 |
| 0.23252 | ***** | 12 |
| 0.23569 | ***** | 12 |
| 0.23887 | ***** | 8  |
| 0.24204 | ***** | 12 |
| 0.24522 | ***** | 5  |
| 0.24839 | ***** | 9  |
| 0.25156 | ***** | 5  |
| 0.25474 | ***** | 11 |
| 0.25791 | ***** | 8  |
| 0.26108 | ***** | 9  |
| 0.26426 | ***** | 5  |
| 0.26743 | ***** | 4  |
| 0.27060 | ***** | 4  |
| 0.27378 | ***** | 2  |
| 0.27695 | ****  | 1  |
| 0.28012 | ****  | 1  |
| 0.28330 | ***** | 3  |
| 0.28647 | ***** | 4  |
| 0.28964 | ****  | 1  |
| 0.29282 | ****  | 1  |

Figure I-24. Histogram, IN Ckt Saturation Voltage,  
Normal Operation at +125°C



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 4

|         |       |     |
|---------|-------|-----|
| 0.12659 |       | 1   |
| 0.13055 |       | 0   |
| 0.13450 |       | 1   |
| 0.13846 |       | 0   |
| 0.14241 |       | 1   |
| 0.14637 | *     | 3   |
| 0.15033 | **    | 9   |
| 0.15428 | **    | 8   |
| 0.15824 | ***** | 21  |
| 0.16219 | ***** | 20  |
| 0.16615 | ***** | 38  |
| 0.17010 | ***** | 36  |
| 0.17406 | ***** | 61  |
| 0.17801 | ***** | 77  |
| 0.18197 | ***** | 79  |
| 0.18592 | ***** | 108 |
| 0.18988 | ***** | 119 |
| 0.19383 | ***** | 163 |
| 0.19779 | ***** | 167 |
| 0.20175 | ***** | 182 |
| 0.20570 | ***** | 221 |
| 0.20966 | ***** | 253 |
| 0.21361 | ***** | 260 |
| 0.21757 | ***** | 246 |
| 0.22152 | ***** | 316 |
| 0.22548 | ***** | 303 |
| 0.22943 | ***** | 257 |
| 0.23339 | ***** | 285 |
| 0.23734 | ***** | 290 |
| 0.24130 | ***** | 270 |
| 0.24525 | ***** | 254 |
| 0.24921 | ***** | 217 |
| 0.25317 | ***** | 178 |
| 0.25712 | ***** | 174 |
| 0.26108 | ***** | 173 |
| 0.26503 | ***** | 156 |
| 0.26899 | ***** | 125 |
| 0.27294 | ***** | 138 |
| 0.27690 | ***** | 94  |
| 0.28085 | ***** | 61  |
| 0.28481 | ***** | 45  |
| 0.28876 | ***** | 47  |
| 0.29272 | ***** | 38  |
| 0.29667 | ***** | 25  |
| 0.30063 | ***** | 20  |
| 0.30459 | ***** | 16  |
| 0.30854 | ***** | 13  |
| 0.31250 | *     | 4   |
| 0.31645 | *     | 4   |
| 0.32041 |       | 1   |

Figure I-25. Histogram, IN Ckt Saturation Voltage,  
Normal Operation at +25 °C



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 2

|         |       |    |
|---------|-------|----|
| 0.15233 | ****  | 2  |
| 0.15589 |       | 0  |
| 0.15945 |       | 0  |
| 0.16301 |       | 0  |
| 0.16657 | ***** | 3  |
| 0.17013 |       | 0  |
| 0.17369 | ***** | 5  |
| 0.17725 | ***** | 4  |
| 0.18081 | ****  | 2  |
| 0.18437 | ***** | 7  |
| 0.18794 | ***** | 4  |
| 0.19150 | ***** | 11 |
| 0.19506 | ***** | 11 |
| 0.19862 | ***** | 14 |
| 0.20218 | ***** | 10 |
| 0.20574 | ***** | 16 |
| 0.20930 | ***** | 22 |
| 0.21286 | ***** | 13 |
| 0.21642 | ***** | 16 |
| 0.21998 | ***** | 21 |
| 0.22354 | ***** | 21 |
| 0.22711 | ***** | 22 |
| 0.23067 | ***** | 19 |
| 0.23423 | ***** | 26 |
| 0.23779 | ***** | 19 |
| 0.24135 | ***** | 23 |
| 0.24491 | ***** | 33 |
| 0.24847 | ***** | 28 |
| 0.25203 | ***** | 30 |
| 0.25559 | ***** | 17 |
| 0.25915 | ***** | 20 |
| 0.26271 | ***** | 19 |
| 0.26627 | ***** | 19 |
| 0.26984 | ***** | 12 |
| 0.27340 | ***** | 20 |
| 0.27696 | ***** | 13 |
| 0.28052 | ***** | 13 |
| 0.28408 | ***** | 9  |
| 0.28764 | ***** | 13 |
| 0.29120 | ***** | 11 |
| 0.29476 | ***** | 6  |
| 0.29832 | ***** | 9  |
| 0.30188 | ***** | 3  |
| 0.30544 | ***** | 4  |
| 0.30901 | ***** | 3  |
| 0.31257 | ***** | 4  |
| 0.31613 | ***** | 4  |
| 0.31969 |       | 0  |
| 0.32325 | ****  | 2  |
| 0.32681 | **    | 1  |

Figure I-26. Histogram, IN Ckt Saturation Voltage,  
Normal Operation at +25 °C



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 2

|         |       |    |
|---------|-------|----|
| 0.18498 | **    | 1  |
| 0.18913 | **    | 1  |
| 0.19237 | ***** | 5  |
| 0.19762 | ****  | 2  |
| 0.20196 | ***** | 3  |
| 0.20611 | ***** | 5  |
| 0.21035 | ***** | 9  |
| 0.21460 | ***** | 11 |
| 0.21884 | ***** | 9  |
| 0.22309 | ***** | 11 |
| 0.22733 | ***** | 10 |
| 0.23158 | ***** | 7  |
| 0.23582 | ***** | 17 |
| 0.24007 | ***** | 15 |
| 0.24431 | ***** | 15 |
| 0.24856 | ***** | 20 |
| 0.25280 | ***** | 14 |
| 0.25705 | ***** | 25 |
| 0.26129 | ***** | 22 |
| 0.26554 | ***** | 11 |
| 0.26978 | ***** | 14 |
| 0.27403 | ***** | 19 |
| 0.27827 | ***** | 15 |
| 0.28252 | ***** | 15 |
| 0.28676 | ***** | 26 |
| 0.29101 | ***** | 15 |
| 0.29525 | ***** | 27 |
| 0.29950 | ***** | 22 |
| 0.30374 | ***** | 23 |
| 0.30799 | ***** | 13 |
| 0.31223 | ***** | 17 |
| 0.31648 | ***** | 22 |
| 0.32072 | ***** | 11 |
| 0.32496 | ***** | 14 |
| 0.32921 | ***** | 22 |
| 0.33345 | ***** | 20 |
| 0.33770 | ***** | 14 |
| 0.34194 | ***** | 21 |
| 0.34619 | ***** | 5  |
| 0.35043 | ***** | 10 |
| 0.35468 | ***** | 11 |
| 0.35892 | ***** | 13 |
| 0.36317 | ***** | 10 |
| 0.36741 | ***** | 9  |
| 0.37166 | ***** | 4  |
| 0.37590 | ***** | 3  |
| 0.38015 | ***** | 4  |
| 0.38439 | ****  | 2  |
| 0.38864 |       | 0  |
| 0.39288 | ****  | 2  |

Figure I-27. Histogram, IN Ckt Saturation Voltage,  
Transistor Open at +125 °C



DISTRIBUTION OF PERFORMANCE PARAMETER V1 FOR 7395 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8

|         |       |     |
|---------|-------|-----|
| 0.17742 |       | 1   |
| 0.18406 | *     | 4   |
| 0.19069 | *     | 6   |
| 0.19733 | **    | 13  |
| 0.20396 | ***   | 22  |
| 0.21059 | ****  | 35  |
| 0.21723 | ***** | 40  |
| 0.22386 | ***** | 70  |
| 0.23050 | ***** | 112 |
| 0.23713 | ***** | 133 |
| 0.24376 | ***** | 149 |
| 0.25040 | ***** | 170 |
| 0.25703 | ***** | 201 |
| 0.26367 | ***** | 252 |
| 0.27030 | ***** | 244 |
| 0.27693 | ***** | 260 |
| 0.28357 | ***** | 295 |
| 0.29020 | ***** | 328 |
| 0.29684 | ***** | 372 |
| 0.30347 | ***** | 381 |
| 0.31010 | ***** | 411 |
| 0.31674 | ***** | 388 |
| 0.32337 | ***** | 372 |
| 0.33001 | ***** | 370 |
| 0.33664 | ***** | 355 |
| 0.34327 | ***** | 333 |
| 0.34991 | ***** | 314 |
| 0.35654 | ***** | 259 |
| 0.36318 | ***** | 234 |
| 0.36981 | ***** | 258 |
| 0.37645 | ***** | 209 |
| 0.38308 | ***** | 187 |
| 0.38971 | ***** | 131 |
| 0.39635 | ***** | 125 |
| 0.40298 | ***** | 71  |
| 0.40962 | ***** | 79  |
| 0.41625 | ***** | 64  |
| 0.42288 | ***** | 45  |
| 0.42952 | ****  | 34  |
| 0.43615 | **    | 15  |
| 0.44279 | **    | 18  |
| 0.44942 | *     | 10  |
| 0.45605 | *     | 5   |
| 0.46269 | *     | 5   |
| 0.46932 | *     | 6   |
| 0.47596 |       | 3   |
| 0.48259 |       | 3   |
| 0.48922 |       | 2   |
| 0.49586 |       | 0   |
| 0.50249 |       | 1   |

Figure I-28. Histogram, IN Ckt Saturation Voltage, Transistor Open at +25 °C



DISTRIBUTION OF PERFORMANCE PARAMETER V<sub>I</sub> FOR 486 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 4

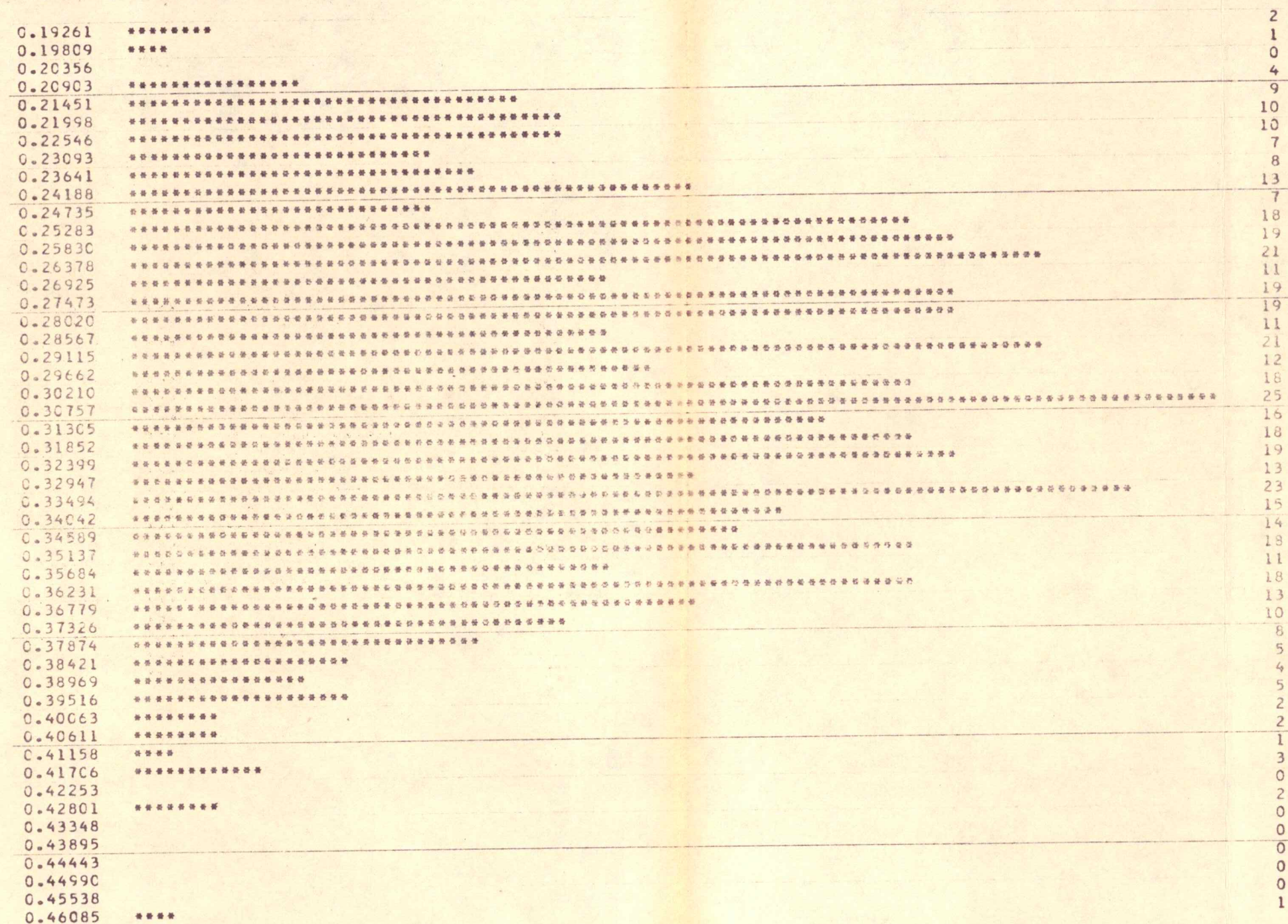


Figure I-29. Histogram, IN Ckt Saturation Voltage, Transistor Open at -25°C, Gated Input = 24.5 V, Load Current = 37 ma



DISTRIBUTION OF PERFORMANCE PARAMETER V<sub>I</sub>

FOR 1114 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1

|         |       |    |
|---------|-------|----|
| 0.16751 | ***** | 5  |
| 0.17300 |       | 0  |
| 0.17850 | **    | 2  |
| 0.18400 | ***** | 9  |
| 0.18950 | ***** | 14 |
| 0.19500 | ***** | 12 |
| 0.20049 | ***** | 23 |
| 0.20599 | ***** | 18 |
| 0.21149 | ***** | 15 |
| 0.21699 | ***** | 22 |
| 0.22248 | ***** | 15 |
| 0.22798 | ***** | 40 |
| 0.23348 | ***** | 47 |
| 0.23898 | ***** | 31 |
| 0.24447 | ***** | 34 |
| 0.24997 | ***** | 42 |
| 0.25547 | ***** | 38 |
| 0.26097 | ***** | 41 |
| 0.26646 | ***** | 51 |
| 0.27196 | ***** | 42 |
| 0.27746 | ***** | 46 |
| 0.28296 | ***** | 47 |
| 0.28846 | ***** | 46 |
| 0.29395 | ***** | 40 |
| 0.29945 | ***** | 44 |
| 0.30495 | ***** | 39 |
| 0.31045 | ***** | 47 |
| 0.31594 | ***** | 33 |
| 0.32144 | ***** | 30 |
| 0.32694 | ***** | 41 |
| 0.33244 | ***** | 38 |
| 0.33793 | ***** | 35 |
| 0.34343 | ***** | 25 |
| 0.34893 | ***** | 25 |
| 0.35443 | ***** | 18 |
| 0.35992 | ***** | 18 |
| 0.36542 | ***** | 13 |
| 0.37092 | ***** | 8  |
| 0.37642 | ***** | 6  |
| 0.38192 | ***   | 3  |
| 0.38741 | **    | 2  |
| 0.39291 | **    | 2  |
| 0.39841 | ***   | 3  |
| 0.40391 | *     | 1  |
| 0.40940 |       | 0  |
| 0.41490 | *     | 1  |
| 0.42040 | *     | 1  |
| 0.42590 |       | 0  |
| 0.43139 |       | 0  |
| 0.43689 | *     | 1  |

Figure I-30. Histogram, IN Ckt Saturation Voltage, Transistor  
Open at -25 °C, Gated Input = 24.5 V, Load Current = 37 ma



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 4

|         |       |    |
|---------|-------|----|
| 0.15456 | ***** | 2  |
| 0.15940 |       | 0  |
| 0.16424 | ***** | 2  |
| 0.16907 | ***** | 4  |
| 0.17391 | ***** | 6  |
| 0.17874 | ***** | 5  |
| 0.18358 | ***** | 9  |
| 0.18841 | ***** | 14 |
| 0.19325 | ***** | 5  |
| 0.19808 | ***** | 11 |
| 0.20292 | ***** | 10 |
| 0.20775 | ***** | 5  |
| 0.21259 | ***** | 15 |
| 0.21742 | ***** | 22 |
| 0.22226 | ***** | 22 |
| 0.22709 | ***** | 17 |
| 0.23193 | ***** | 12 |
| 0.23676 | ***** | 19 |
| 0.24160 | ***** | 15 |
| 0.24643 | ***** | 20 |
| 0.25127 | ***** | 19 |
| 0.25610 | ***** | 10 |
| 0.26094 | ***** | 18 |
| 0.26577 | ***** | 21 |
| 0.27061 | ***** | 17 |
| 0.27544 | ***** | 22 |
| 0.28028 | ***** | 16 |
| 0.28511 | ***** | 17 |
| 0.28995 | ***** | 14 |
| 0.29478 | ***** | 15 |
| 0.29962 | ***** | 16 |
| 0.30445 | ***** | 18 |
| 0.30929 | ***** | 14 |
| 0.31412 | ***** | 17 |
| 0.31896 | ***** | 14 |
| 0.32380 | ***** | 12 |
| 0.32863 | ***** | 13 |
| 0.33347 | ***** | 11 |
| 0.33830 | ***** | 7  |
| 0.34314 | ***** | 7  |
| 0.34797 | ***** | 4  |
| 0.35281 | ***** | 2  |
| 0.35764 | ***** | 3  |
| 0.36248 | ***** | 2  |
| 0.36731 | ***** | 3  |
| 0.37215 | ***** | 2  |
| 0.37698 | ****  | 1  |
| 0.38182 |       | 0  |
| 0.38665 |       | 0  |
| 0.39149 | ****  | 1  |

Figure I-31. Histogram, IN Ckt Saturation Voltage, Transistor  
Open at -25 °C, Gated Input = 23 V, Load Current = 30 ma



DISTRIBUTION OF PERFORMANCE PARAMETER V1 F2R 500 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 4

|         |       |    |
|---------|-------|----|
| 0.08063 | ****  | 1  |
| 0.08309 |       | 0  |
| 0.08554 | ***** | 4  |
| 0.08800 | ***** | 3  |
| 0.09045 | ***** | 7  |
| 0.09291 | ***** | 5  |
| 0.09536 | ***** | 9  |
| 0.09782 | ***** | 6  |
| 0.10028 | ***** | 14 |
| 0.10273 | ***** | 13 |
| 0.10519 | ***** | 13 |
| 0.10764 | ***** | 11 |
| 0.11010 | ***** | 12 |
| 0.11255 | ***** | 12 |
| 0.11501 | ***** | 13 |
| 0.11746 | ***** | 16 |
| 0.11992 | ***** | 16 |
| 0.12237 | ***** | 13 |
| 0.12483 | ***** | 23 |
| 0.12729 | ***** | 16 |
| 0.12974 | ***** | 16 |
| 0.13220 | ***** | 14 |
| 0.13465 | ***** | 8  |
| 0.13711 | ***** | 7  |
| 0.13956 | ***** | 7  |
| 0.14202 | ***** | 18 |
| 0.14447 | ***** | 25 |
| 0.14693 | ***** | 16 |
| 0.14938 | ***** | 5  |
| 0.15184 | ***** | 15 |
| 0.15430 | ***** | 18 |
| 0.15675 | ***** | 15 |
| 0.15921 | ***** | 13 |
| 0.16166 | ***** | 11 |
| 0.16412 | ***** | 17 |
| 0.16657 | ***** | 9  |
| 0.16903 | ***** | 9  |
| 0.17148 | ***** | 12 |
| 0.17394 | ***** | 10 |
| 0.17640 | ***** | 10 |
| 0.17885 | ***** | 12 |
| 0.18131 | ***** | 6  |
| 0.18376 | ***** | 7  |
| 0.18622 | ***** | 4  |
| 0.18867 | ***** | 5  |
| 0.19113 | ****  | 1  |
| 0.19358 | ****  | 1  |
| 0.19604 |       | 0  |
| 0.19849 | ****  | 1  |
| 0.20095 | ****  | 1  |

Figure I-32. Histogram, IN Ckt Saturation Voltage,  
Transistor Shorted at +125 °C



THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 2

|         |       |     |
|---------|-------|-----|
| 0.08215 | *     | 1   |
| 0.08520 | ***   | 5   |
| 0.08825 | ***** | 16  |
| 0.09130 | ***** | 16  |
| 0.09435 | ***** | 32  |
| 0.09740 | ***** | 57  |
| 0.10046 | ***** | 65  |
| 0.10351 | ***** | 69  |
| 0.10656 | ***** | 86  |
| 0.10961 | ***** | 122 |
| 0.11266 | ***** | 128 |
| 0.11571 | ***** | 122 |
| 0.11876 | ***** | 130 |
| 0.12181 | ***** | 139 |
| 0.12486 | ***** | 154 |
| 0.12791 | ***** | 153 |
| 0.13096 | ***** | 130 |
| 0.13401 | ***** | 184 |
| 0.13706 | ***** | 147 |
| 0.14011 | ***** | 161 |
| 0.14316 | ***** | 158 |
| 0.14621 | ***** | 175 |
| 0.14926 | ***** | 147 |
| 0.15231 | ***** | 188 |
| 0.15536 | ***** | 167 |
| 0.15841 | ***** | 178 |
| 0.16146 | ***** | 164 |
| 0.16452 | ***** | 163 |
| 0.16757 | ***** | 170 |
| 0.17062 | ***** | 173 |
| 0.17367 | ***** | 142 |
| 0.17672 | ***** | 115 |
| 0.17977 | ***** | 108 |
| 0.18282 | ***** | 88  |
| 0.18587 | ***** | 94  |
| 0.18892 | ***** | 68  |
| 0.19197 | ***** | 55  |
| 0.19502 | ***** | 43  |
| 0.19807 | ***** | 24  |
| 0.20112 | ***** | 25  |
| 0.20417 | ***** | 16  |
| 0.20722 | ***** | 14  |
| 0.21027 | ***** | 17  |
| 0.21332 | **    | 3   |
| 0.21637 | **    | 3   |
| 0.21942 | **    | 4   |
| 0.22247 | **    | 4   |
| 0.22553 |       | 0   |
| 0.22858 |       | 0   |
| 0.23163 | *     | 1   |

Figure I-33. Histogram, IN Ckt Saturation Voltage , Transistor Shorted at +25 °C



DISTRIBUTION OF PERFORMANCE PARAMETER VI FOR 344 CASES TESTED

THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 1 / 4

|         |       |    |
|---------|-------|----|
| 0.09087 | ***** | 2  |
| 0.09430 |       | 0  |
| 0.09773 |       | 0  |
| 0.10115 | ***** | 4  |
| 0.10458 | ***** | 2  |
| 0.10801 | ***** | 7  |
| 0.11144 | ***** | 5  |
| 0.11486 | ***** | 2  |
| 0.11829 | ***** | 7  |
| 0.12172 | ***** | 9  |
| 0.12515 | ***** | 11 |
| 0.12857 | ***** | 9  |
| 0.13200 | ***** | 11 |
| 0.13543 | ***** | 8  |
| 0.13886 | ***** | 6  |
| 0.14228 | ***** | 14 |
| 0.14571 | ***** | 12 |
| 0.14914 | ***** | 7  |
| 0.15257 | ***** | 14 |
| 0.15599 | ***** | 10 |
| 0.15942 | ***** | 17 |
| 0.16285 | ***** | 18 |
| 0.16628 | ***** | 15 |
| 0.16970 | ***** | 16 |
| 0.17313 | ***** | 12 |
| 0.17656 | ***** | 14 |
| 0.17999 | ***** | 14 |
| 0.18341 | ***** | 9  |
| 0.18684 | ***** | 11 |
| 0.19027 | ***** | 9  |
| 0.19370 | ***** | 12 |
| 0.19712 | ***** | 8  |
| 0.20055 | ***** | 11 |
| 0.20398 | ***** | 9  |
| 0.20740 | ***** | 3  |
| 0.21083 | ***** | 6  |
| 0.21426 | ***** | 4  |
| 0.21769 | ***** | 3  |
| 0.22111 | ***** | 3  |
| 0.22454 |       | 0  |
| 0.22797 | ***** | 3  |
| 0.23140 | ****  | 1  |
| 0.23482 | ***** | 2  |
| 0.23825 | ***** | 2  |
| 0.24168 | ****  | 1  |
| 0.24511 |       | 0  |
| 0.24853 |       | 0  |
| 0.25196 |       | 0  |
| 0.25539 |       | 0  |
| 0.25882 | ****  | 1  |

Figure I-34. Histogram, IN Ckt Saturation Voltage, Transistor Shorted at -25°C



Table I-1. Worst-Case Tabulation, IP Circuit at +25 °C with  
No Component Failures (Gated Input = 28 V)

| PARAMETER | MINIMUM      | NOMINAL      | MAXIMUM      |
|-----------|--------------|--------------|--------------|
| VOUT      | 2.753493E 01 | 2.768910E 01 | 2.782943E 01 |
| V31       | 2.709785E 01 | 2.718881E 01 | 2.727696E 01 |
| V13       | 2.772717E 01 | 2.784298E 01 | 2.794947E 01 |
| V19       | 2.688525E 01 | 2.703481E 01 | 2.717408E 01 |
| V14       | 2.773270E 01 | 2.784492E 01 | 2.795024E 01 |
| V30       | 5.557674E-01 | 6.078406E-01 | 6.600260E-01 |
| V7        | 2.710373E 01 | 2.718842E 01 | 2.728371E 01 |
| V16       | 2.689391E 01 | 2.703681E 01 | 2.717948E 01 |
| V5        | 1.081131E 00 | 1.184047E 00 | 1.287139E 00 |
| V11       | 1.081415E 00 | 1.184231E 00 | 1.287230E 00 |
| PT1       | 1.102958E 00 | 9.610208E 00 | 2.074734E 01 |
| PT2       | 1.622274E 00 | 9.671568E 00 | 2.276931E 01 |
| VCEsat    | 1.747987E-01 | 3.109043E-01 | 4.688008E-01 |
| IT1       | 4.018550E 00 | 6.197056E 01 | 1.156477E 02 |
| IT2       | 4.280381E 00 | 6.159540E 01 | 1.184920E 02 |
| IT3       | 8.437455E-01 | 5.799473E 01 | 1.146510E 02 |
| IT4       | 9.273786E-01 | 5.812956E 01 | 1.149045E 02 |
| IC1       | 6.661923E 00 | 6.914257E 00 | 7.182385E 00 |
| PT3       | 9.703776E-01 | 9.037161E 00 | 2.124971E 01 |
| PT4       | 1.240320E 00 | 8.945358E 00 | 2.208953E 01 |
| IC4       | 3.341888E 00 | 3.467277E 00 | 3.599950E 00 |
| IC5       | 3.314854E 00 | 3.446768E 00 | 3.585448E 00 |
| IC6       | 6.661057E 00 | 6.914043E 00 | 7.180908E 00 |
| ICT3      | 1.184703E 00 | 2.537248E 00 | 2.918536E 00 |
| ICT4      | 1.503291E 00 | 2.630378E 00 | 3.188795E 00 |



Table I-2. Worst-Case Tabulation, IP Circuit at +25 °C with  
No Component Failures (Gated Input = 24 V)

| PARAMETER | MINIMUM      | NOMINAL      | MAXIMUM      |
|-----------|--------------|--------------|--------------|
| VOUT      | 2.351296E 01 | 2.366854E 01 | 2.380841E 01 |
| V31       | 2.309860E 01 | 2.318974E 01 | 2.327794E 01 |
| V13       | 2.371686E 01 | 2.383299E 01 | 2.393883E 01 |
| V19       | 2.287461E 01 | 2.302529E 01 | 2.316408E 01 |
| V14       | 2.371962E 01 | 2.383465E 01 | 2.394023E 01 |
| V30       | 5.463377E-01 | 5.981323E-01 | 6.500187E-01 |
| V7        | 2.310303E 01 | 2.318941E 01 | 2.328453E 01 |
| V16       | 2.288093E 01 | 2.30270CE 01 | 2.316998E 01 |
| V5        | 1.066986E 00 | 1.169477E 00 | 1.272122E 00 |
| V11       | 1.067282E 00 | 1.169675E 00 | 1.272226E 00 |
| IDT1      | 7.171035E-01 | 2.199354E 00 | 2.408070E 00 |
| IDT2      | 9.812169E-01 | 2.101677E 00 | 2.631241E 00 |
| VCEsat    | 1.915872E-01 | 3.314588E-01 | 4.870439E-01 |
| IT1       | 3.331990E 00 | 6.083273E 01 | 1.166200E 02 |
| IT2       | 3.731351E 00 | 6.052827E 01 | 1.169302E 02 |
| IT3       | 8.297628E-01 | 5.746171E 01 | 1.137834E 02 |
| IT4       | 9.083935E-01 | 5.759271E 01 | 1.138900E 02 |
| ID1       | 5.628912E 00 | 5.850298E 00 | 6.085759E 00 |
| ID2       | 2.826611E 00 | 2.935964E 00 | 3.053213E 00 |
| ID3       | 2.798263E 00 | 2.914335E 00 | 3.037277E 00 |
| ID4       | 2.826034E 00 | 2.936007E 00 | 3.052306E 00 |
| ID5       | 2.797447E 00 | 2.914109E 00 | 3.036354E 00 |
| ID6       | 5.627665E 00 | 5.850113E 00 | 6.084219E 00 |
| IDT3      | 8.121756E-01 | 2.022530E 00 | 2.419716E 00 |
| IDT4      | 1.000870E 00 | 2.101757E 00 | 2.640027E 00 |



Table I-3. Worst-Case Tabulation, IP Circuit at +25 °C  
With Shorted Transistor

| PARAMETER | MINIMUM      | NOMINAL      | MAXIMUM      |
|-----------|--------------|--------------|--------------|
| VOUT      | 2.769354E 01 | 2.778826E 01 | 2.788151E 01 |
| VCESAT    | 1.212609E-01 | 2.117419E-01 | 3.101950E-01 |
| V31       | 2.714604E 01 | 2.723024E 01 | 2.729580E 01 |
| V13       | 2.779183E 01 | 2.789172E 01 | 2.798043E 01 |
| V19       | 2.701778E 01 | 2.712652E 01 | 2.722754E 01 |
| V14       | 2.770497E 01 | 2.779856E 01 | 2.788943E 01 |
| V7        | 2.709059E 01 | 2.714927E 01 | 2.723312E 01 |
| V16       | 2.703525E 01 | 2.714111E 01 | 2.725575E 01 |
| IT1       | 3.783103E 01 | 1.069177E Q2 | 1.173985E 02 |
| IT2       | 3.781724E 00 | 1.601699E 01 | 8.615584E 01 |
| IT3       | 5.062650E-01 | 7.110629E-01 | 9.129111E-01 |
| IT4       | 5.087674E-01 | 1.254994E 01 | 8.256395E 01 |
| ID1       | 6.674526E 00 | 6.922912E 00 | 7.188368E 00 |
| ID2       | 3.340772E 00 | 3.462002E 00 | 3.593940E 00 |
| ID3       | 3.333701E 00 | 3.460914E 00 | 3.596370E 00 |
| ID4       | 3.348153E 00 | 3.472772E 00 | 3.602677E 00 |
| ID5       | 3.332004E 00 | 3.458961E 00 | 3.592709E 00 |
| ID6       | 6.685779E 00 | 6.931729E 00 | 7.191256E 00 |
| PT1       | 9.238534E 00 | 2.153761E 01 | 3.492039E 01 |
| PT2       | 6.118285E-01 | 1.734334E 00 | 9.241876E 00 |
| PR7       | 8.621683E 01 | 8.989089E 01 | 9.396695E 01 |
| IDT1      | 1.375599E 00 | 2.395679E 00 | 2.712995E 00 |
| IDT2      | 1.781705E 00 | 2.975001E 00 | 3.178615E 00 |
| IDT3      | 1.923929E 00 | 2.288337E 00 | 2.457738E 00 |
| IDT4      | 2.015122E 00 | 2.987362E 00 | 3.273720E 00 |



Table I-4. Worst-Case Tabulation, IN Circuit at +25 °C  
With No Component Failure

| PARAMETER | MINIMUM      | NOMINAL      | MAXIMUM      |
|-----------|--------------|--------------|--------------|
| V1        | 1.018261E-01 | 2.302793E-01 | 3.865856E-01 |
| V2        | 2.074802E-02 | 1.157292E-01 | 2.420990E-01 |
| V3        | 2.076739E-02 | 1.157278E-01 | 2.421017E-01 |
| V4        | 7.213329E-01 | 8.497989E-01 | 9.945196E-01 |
| V5        | 6.526912E-01 | 7.352404E-01 | 8.116737E-01 |
| VI2       | 6.389623E 00 | 6.822491E 00 | 7.271872E 00 |
| V7        | 7.213072E-01 | 8.497782E-01 | 9.945092E-01 |
| VI0       | 6.526700E-01 | 7.352194E-01 | 8.116595E-01 |
| VI5       | 6.320717E 00 | 6.708061E 00 | 7.089505E 00 |
| IT1       | 3.564330E-01 | 2.572555E 01 | 5.115632E 01 |
| IT2       | 3.566335E-01 | 2.574409E 01 | 5.115624E 01 |
| IT3       | 1.266767E 00 | 2.671108E 01 | 5.219549E 01 |
| IT4       | 1.265448E 00 | 2.672875E 01 | 5.219533E 01 |
| IDT1      | 5.725094E-02 | 5.507866E-01 | 8.198051E-01 |
| IDT2      | 5.727441E-02 | 5.506555E-01 | 8.197686E-01 |
| IDT3      | 4.908394E-02 | 5.505365E-01 | 7.944834E-01 |
| IDT4      | 4.909675E-02 | 5.504193E-01 | 7.944908E-01 |
| IDZ1      | 9.194536E-01 | 9.779127E-01 | 1.038961E 00 |
| IDZ2      | 9.193641E-01 | 9.778994E-01 | 1.038978E 00 |
| IDZ3      | 9.303816E-01 | 9.850444E-01 | 1.043460E 00 |
| IDZ4      | 9.303749E-01 | 9.850510E-01 | 1.043437E 00 |
| PDZ1      | 5.420033E 00 | 5.840772E 00 | 6.277008E 00 |
| PT2       | 4.247679E-02 | 2.949022E 00 | 5.545641E 00 |
| PT3       | 8.860163E-02 | 3.090560E 00 | 5.719564E 00 |
| PRA3      | 1.426511E 01 | 1.552546E 01 | 1.689856E 01 |



Table I-5. Worst-Case Tabulation, IN Circuit at +25 °C  
With Shorted Transistor

| PARAMETER | MINIMUM      | NOMINAL      | MAXIMUM      |
|-----------|--------------|--------------|--------------|
| V1        | 6.656852E-02 | 1.458592E-01 | 2.723461E-01 |
| V2        | 9.186923E-06 | 4.853364E-05 | 5.216865E-05 |
| V3        | 1.305857E-02 | 7.400828E-02 | 1.731801E-01 |
| V4        | 6.832482E-01 | 7.705941E-01 | 8.942425E-01 |
| V5        | 6.512843E-01 | 6.986541E-01 | 7.816830E-01 |
| V12       | 6.351903E 00 | 6.743369E 00 | 7.171613E 00 |
| V13       | 6.832997E 00 | 7.274237E 00 | 7.752179E 00 |
| V18       | 6.888106E-01 | 7.604168E-01 | 8.139619E-01 |
| V19       | 6.357681E 00 | 6.733205E 00 | 7.091892E 00 |
| V20       | 6.838798E 00 | 7.264096E 00 | 7.672778E 00 |
| V24       | 5.922053E-01 | 6.160103E-01 | 6.325647E-01 |
| IDT1      | 6.812596E-02 | 3.967622E-01 | 7.530433E-01 |
| IDT2      | 2.075721E-01 | 7.244964E-01 | 8.519456E-01 |
| IDZ1      | 9.294400E-01 | 9.832043E-01 | 1.040977E 00 |
| IDZ2      | 9.252392E-01 | 9.824583E-01 | 1.041272E 00 |
| IDZ3      | 9.405768E-01 | 9.924678E-01 | 1.046799E 00 |
| IDZ4      | 9.315221E-01 | 9.871961E-01 | 1.043593E 00 |
| IT1       | 8.642641E 00 | 4.784814E 01 | 5.134919E 01 |
| IT2       | 2.018283E-01 | 3.640926E 00 | 4.285347E 01 |
| IT3       | 2.570017E-01 | 3.579946E-01 | 4.587919E-01 |
| IT4       | 1.082619E 00 | 4.627366E 00 | 4.389320E 01 |
| IDT3      | 2.858143E-01 | 4.320194E-01 | 5.881128E-01 |
| IDT4      | 2.002636E-01 | 7.215288E-01 | 7.955811E-01 |
| IRA3      | 9.413116E-01 | 9.924907E-01 | 1.046817E 00 |
| IRA4      | 9.322044E-01 | 9.873418E-01 | 1.043612E 00 |



## APPENDIX II

### AUTOMATIC RESET CIRCUIT CHARACTERISTICS

The following graphs show the significant Automatic Reset Circuit parameters with respect to time during generation of the reset pulse. The waveforms are labeled as follows: Curve A is the voltage dropped by the relay; Curve B is the current per relay; Curve C is the voltage across the capacitor bank; Curve D is the power dissipation in each of the two transistors which have common collectors. The peak power dissipation in the two common emitter transistors is never more than 50 milliwatts and is not shown on the graphs.

The test conditions are stated on each graph.





Figure II-1. Normal Operation at +25 °C



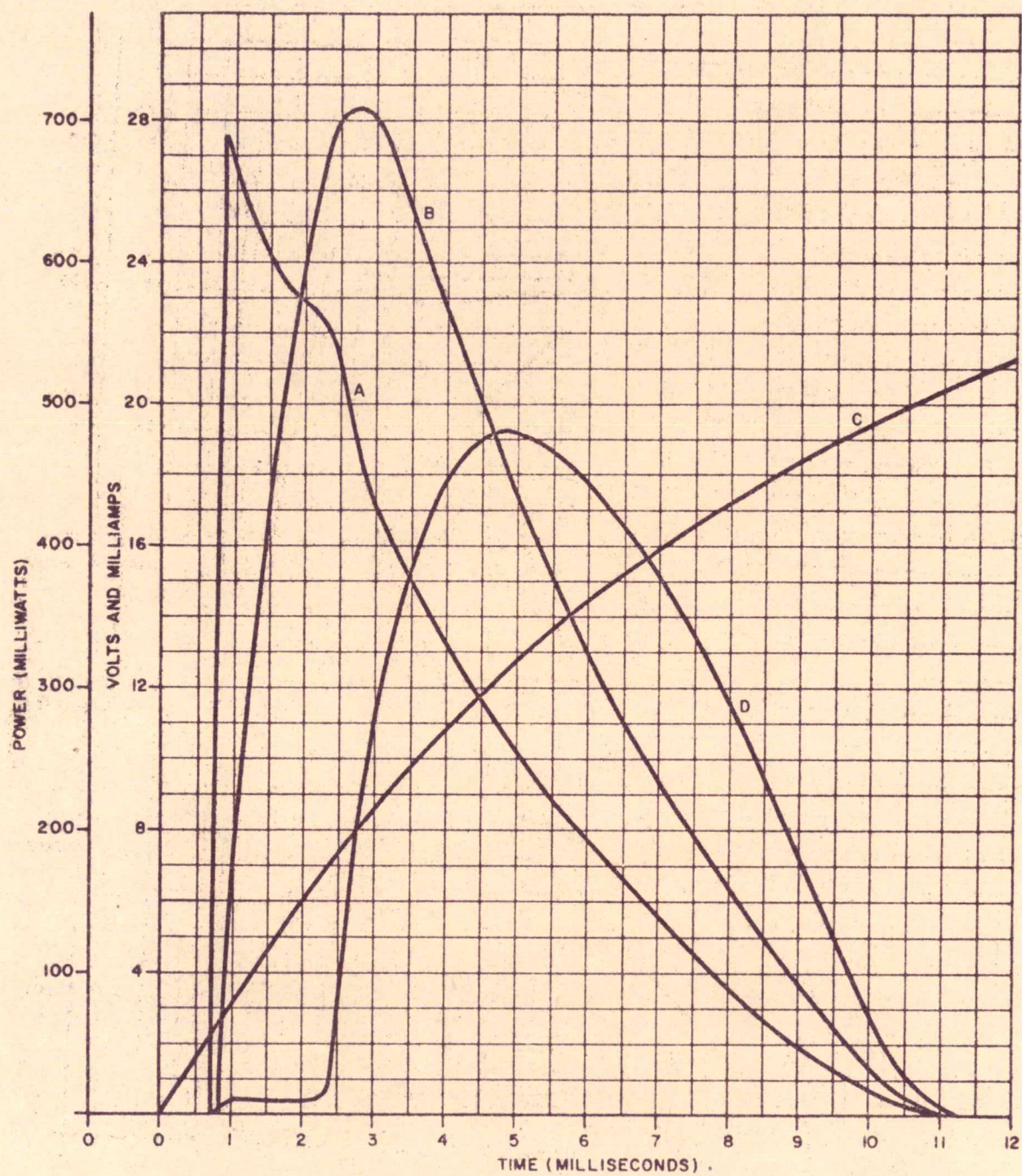


Figure II-2. Normal Operation at  $-25^{\circ}\text{C}$





Figure II-3. Normal Operation at +125°C





Figure II-4. Maximum Pulse Width With No IP Circuit Failure:  
Cmax, RTmax, RLmin, and Maximum Input Voltage (30V) at +125 °C



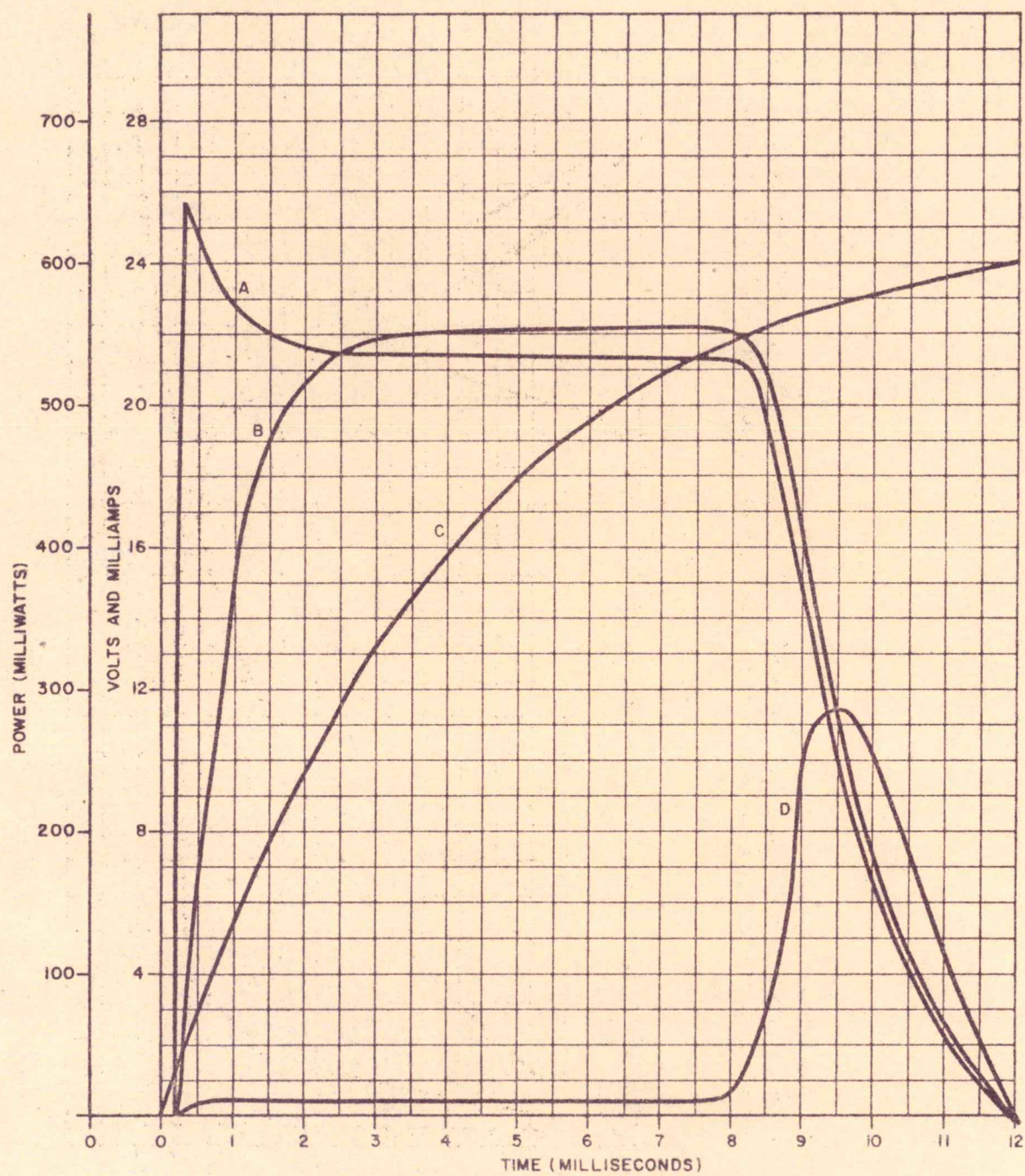
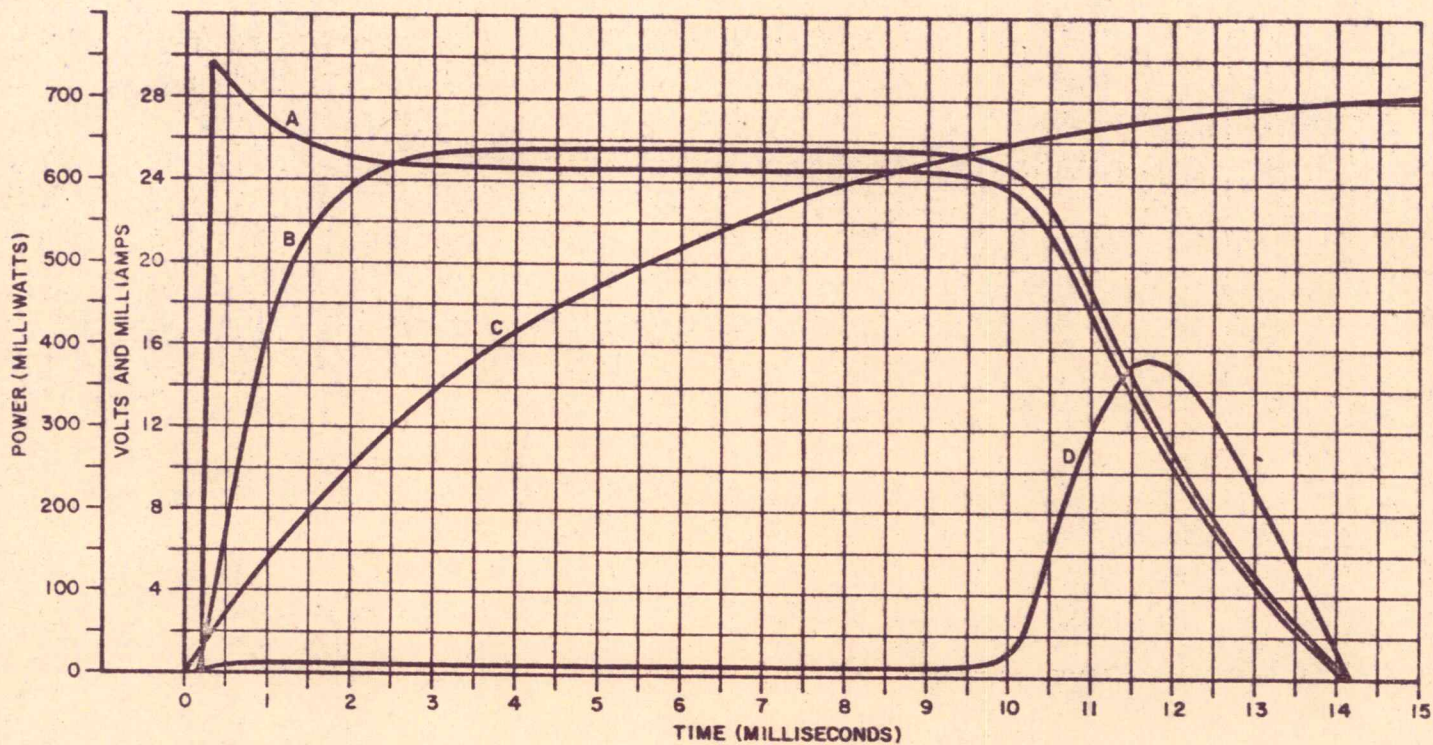


Figure II-5. IP Circuit Normal With  $C_{max}$ ,  $R_{Tmax}$ ,  $R_{Lmin}$ , and Minimum Input Voltage (26V) at  $+125^{\circ}\text{C}$





Maximum Pulse Width With IP Circuit Failure: C<sub>max</sub>, R<sub>Tmax</sub>, R<sub>Lmin</sub>, And Maximum Input Voltage (30V) at +125°C. Curves A, B, and D Are for the IP Circuits Without Failure.

Figure II-6. Maximum Pulse Width With IP Circuit Failure: C<sub>max</sub>, R<sub>Tmax</sub>, R<sub>Lmin</sub>, and Maximum Input Voltage (30V) at +125°C



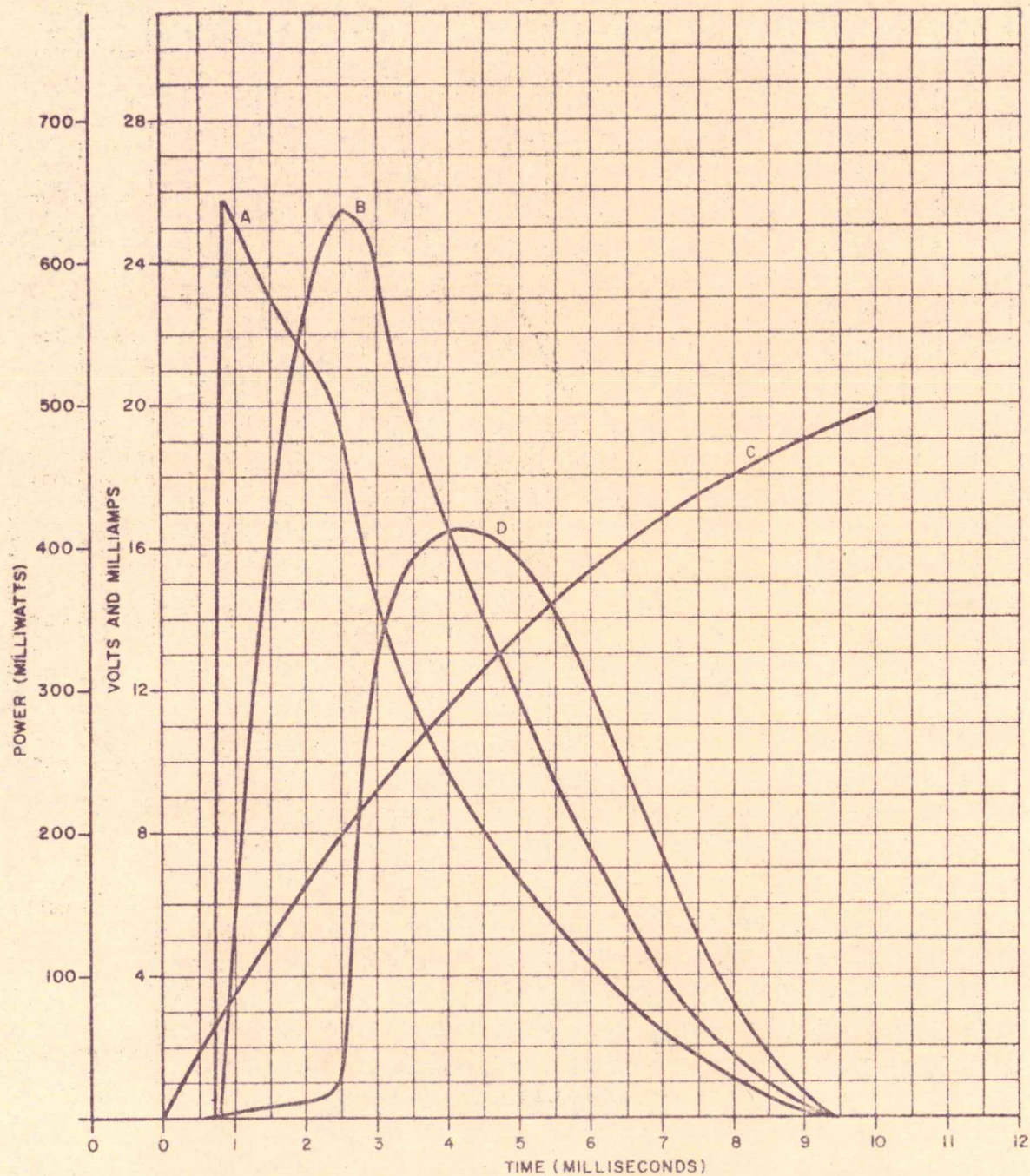


Figure II-7. Minimum Pulse Width With Normal IP Circuits:  
Cmin, RTmin, and Minimum Input Voltage (26V) at -25 °C



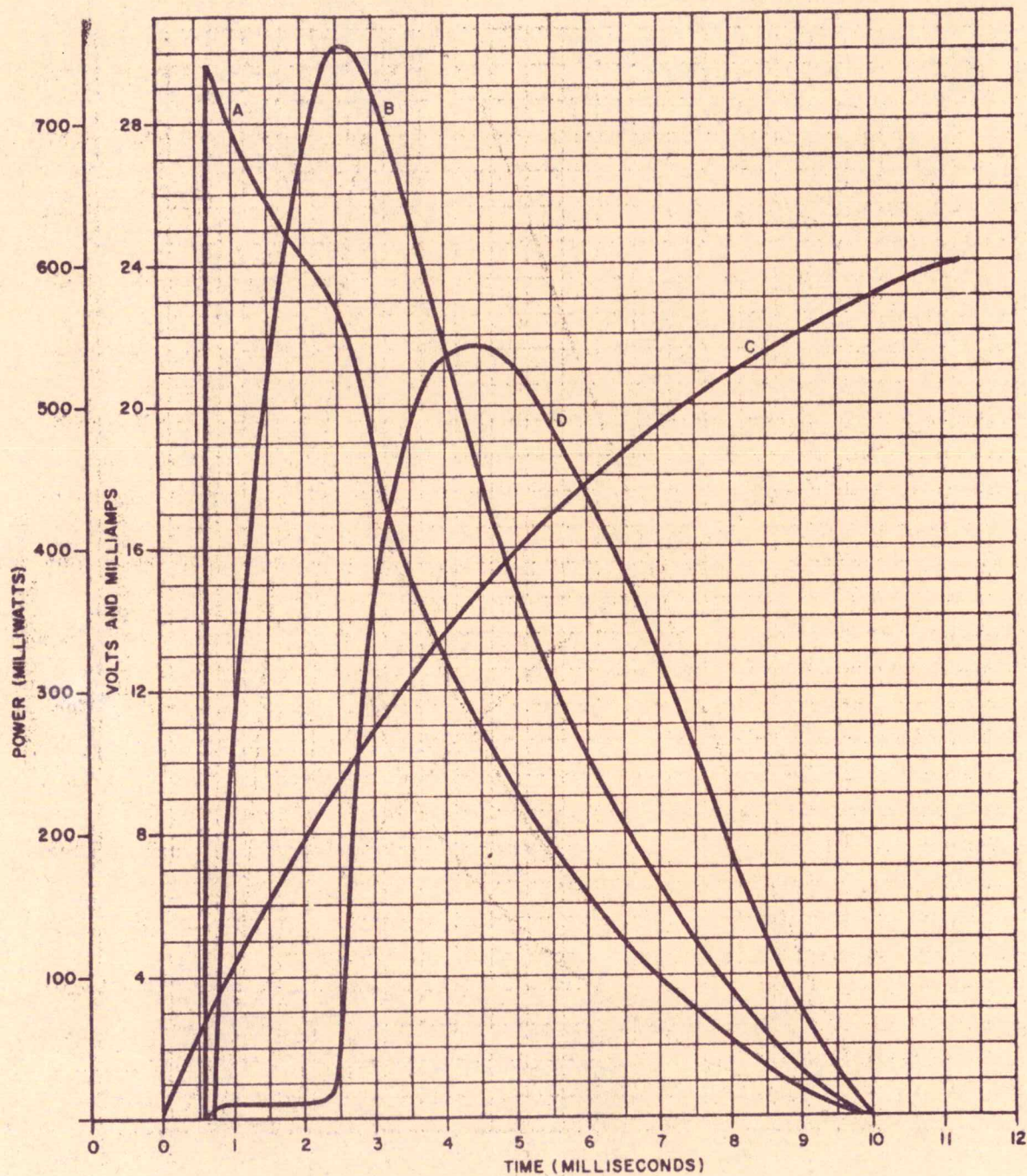
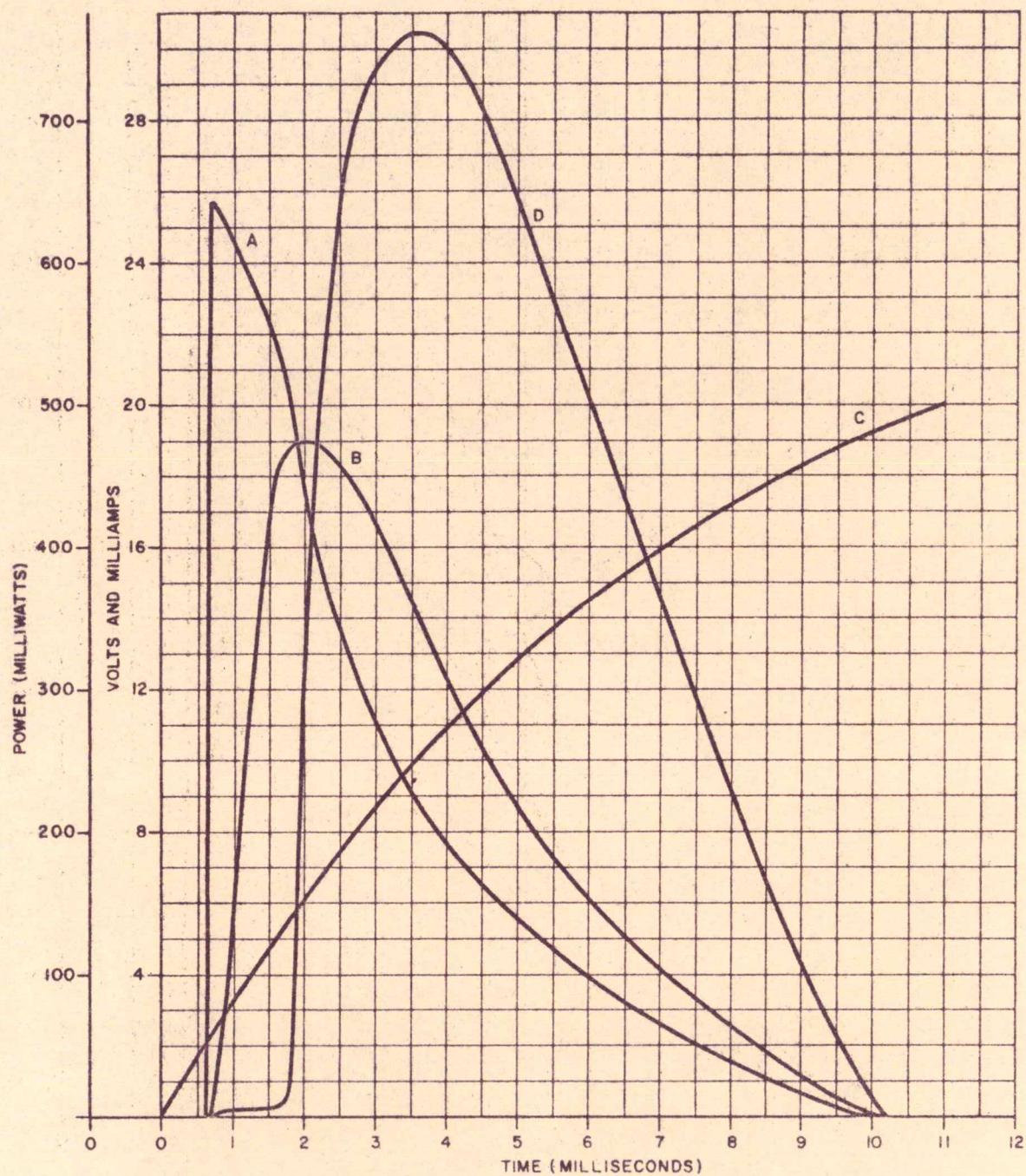


Figure II-8. IP Circuit Normal at  $-25^{\circ}\text{C}$ :  $C_{\min}$ ,  $R_{T\min}$ , and Maximum Input Voltage (30V)

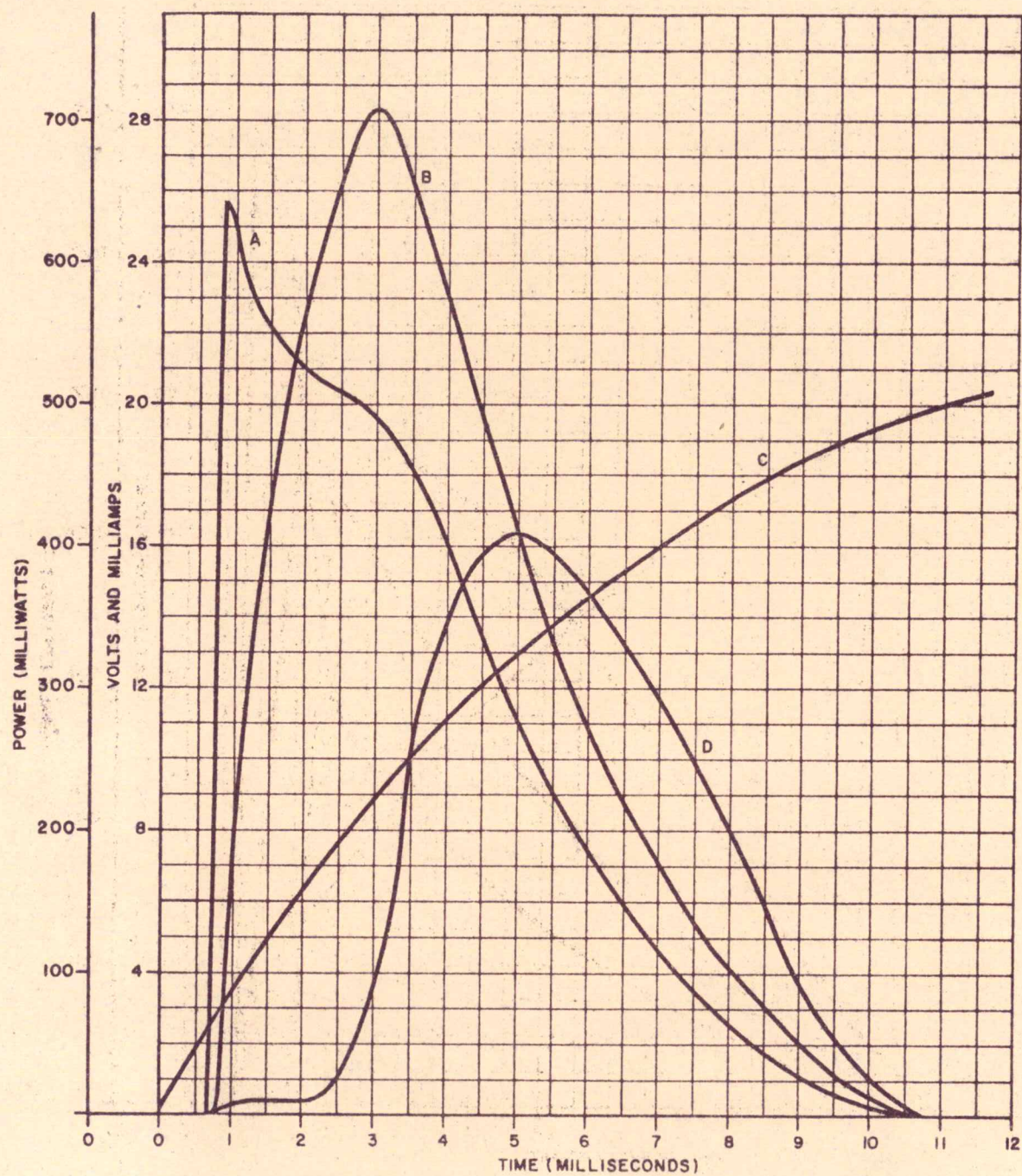




IP Circuit Failure of Open Base Resistor With  $C_{min}$ ,  $R_{Tmin}$ , and Minimum Input Voltage (26V) at  $-25^{\circ}\text{C}$ . Curves A, B, & D Are For IP Circuit With Failure.

Figure II-9. IP Circuit Failure of Open Base Resistor With  $C_{min}$ ,  $R_{Tmin}$ , and Minimum Input Voltage (26V) at  $-25^{\circ}\text{C}$





IP Circuit Failure of Open Base Resistor With  $C_{min}$ ,  $R_{Tmin}$  and Minimum Input Voltage (26V) at  $-25^{\circ}\text{C}$ . Curves A, B, & D Are For IP Circuits Without Failure.

Figure II-10. IP Circuit Failure of Open Base Resistor With  $C_{min}$ ,  $R_{Tmin}$ , and Minimum Input Voltage (26V) at  $-25^{\circ}\text{C}$



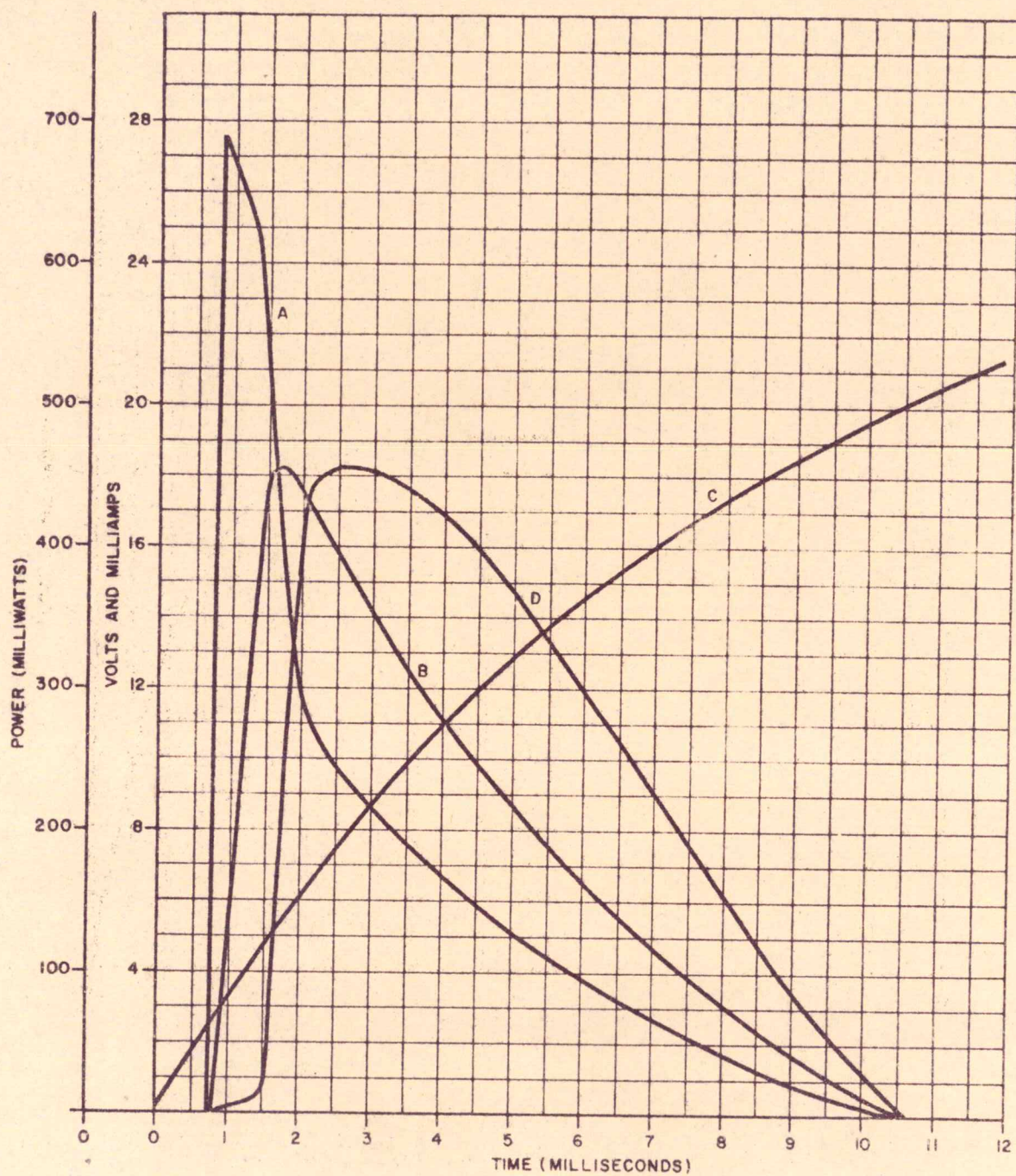
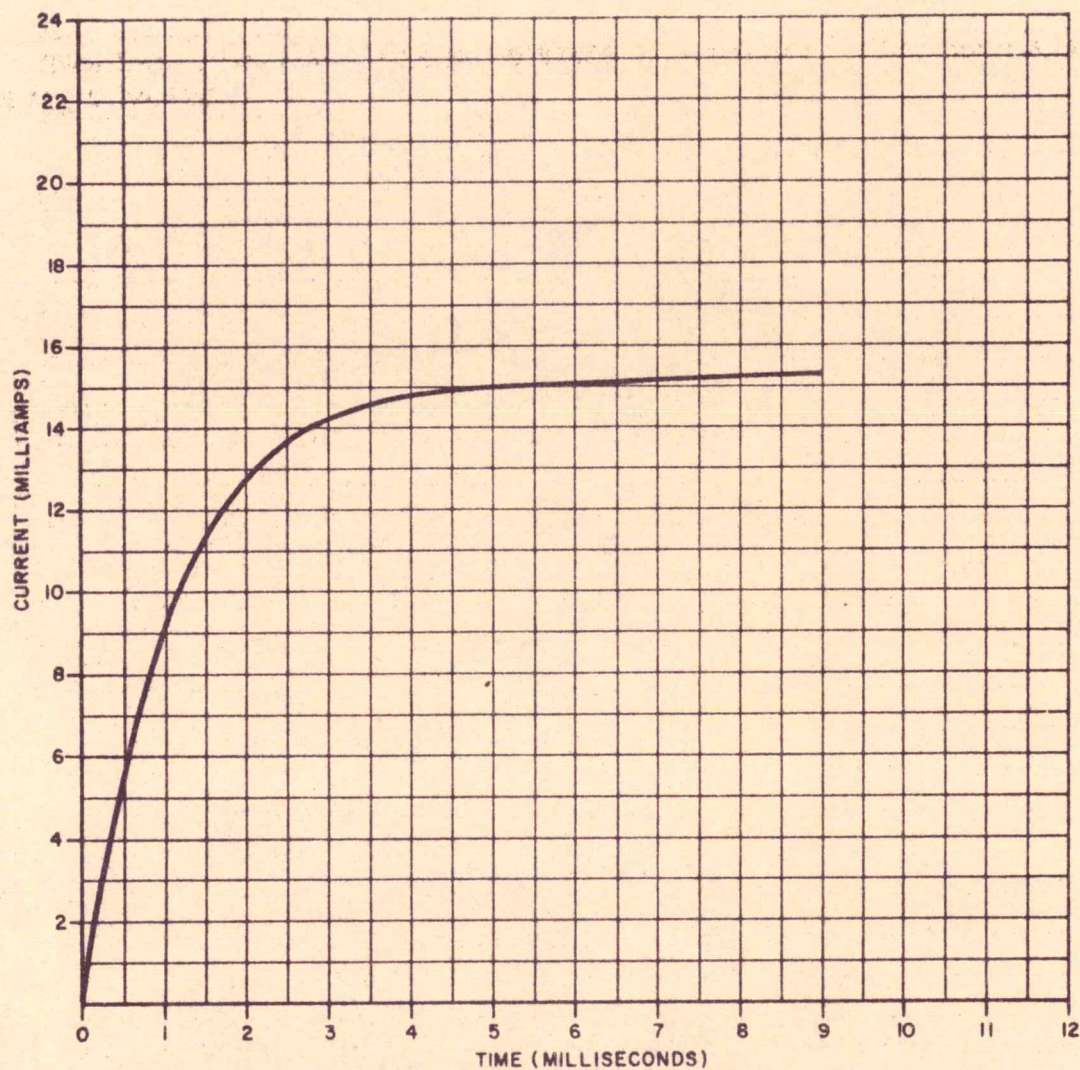


Figure II-11. Minimum Pulse Width With IP Circuit Failure of Open Transistor Collector at  $-25^{\circ}\text{C}$





Relay Coil Current Vs Time with 11 Volts Applied at 25 °C. This current pulse will operate any relay which meets the minimum spec requirements.

Figure II-12. Relay Coil Current Vs Time With 11 Volts Applied at +25 °C

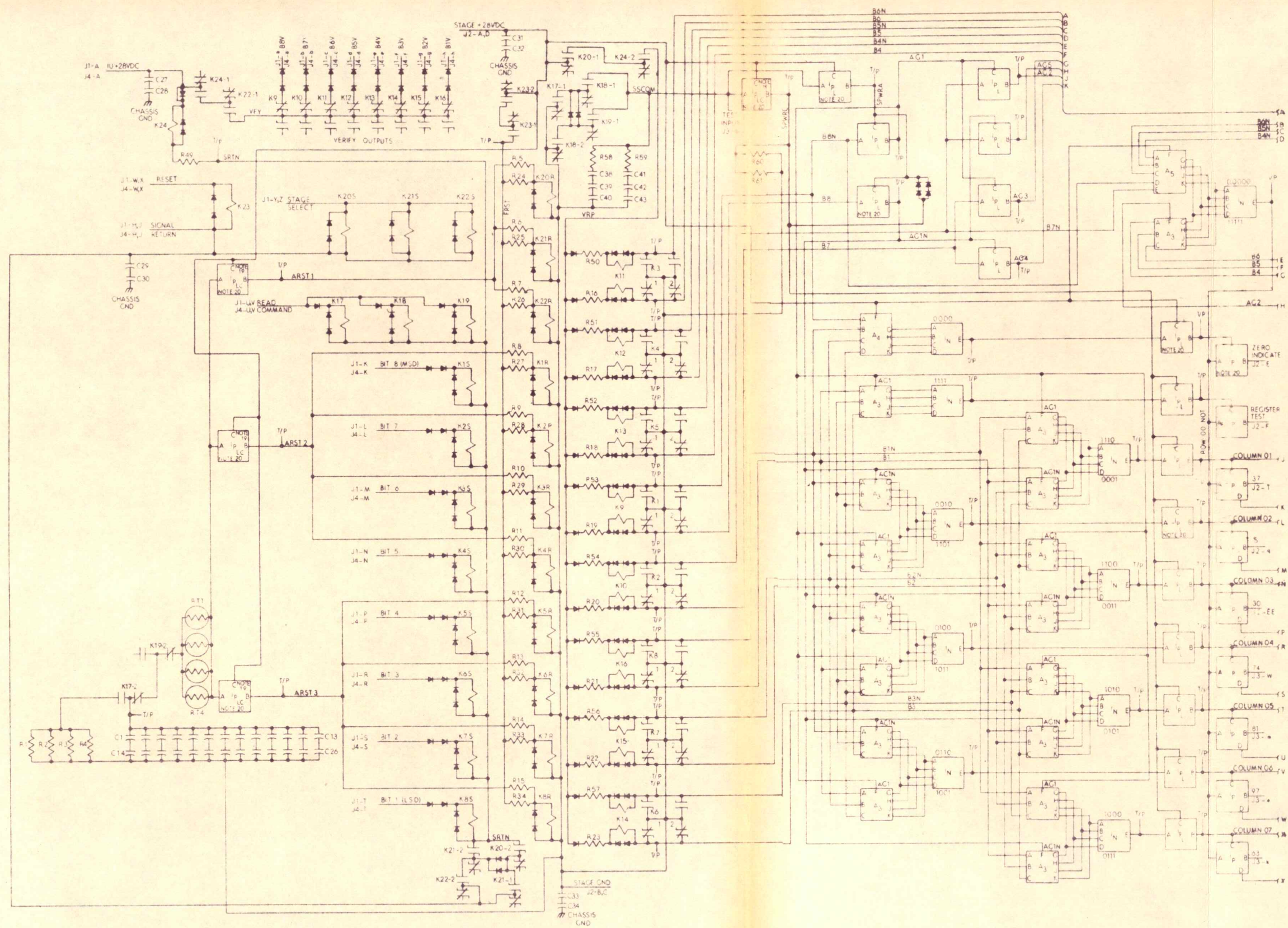


### APPENDIX III

#### SATURN SWITCH SELECTOR MOD II LOGIC SCHEMATIC

This logic schematic is IBM No. 6101534, Revision D as of December 9, 1965,  
NASA No. 50M69053.





NOTES:  
 1. CIRCUIT MODIFIED BY A 0.02 MFD CAPACITOR CONNECTED FROM THE BASE TO EMITTER OF EACH TRANSISTOR.  
 2. CIRCUIT MODIFIED BY THE ELIMINATION OF BASE ISOLATION DIODES CR1, CR2, CR3 AND CR4.

# Switch Selector Schematic (Sheet 1 of 2)

III-3/III-4







## APPENDIX IV

### A. ASAP DESCRIPTION

#### AUTOMATED STATISTICAL ANALYSIS PROGRAM (ASAP)

The statistical worst-case circuit analysis for the system under consideration was accomplished by employing an automated circuit analysis computer program. This program is designed to perform a Monte Carlo statistical analysis of a set of equations which completely describe the system under investigation. The set of real or complex algebraic equations (which are determined by the type of analysis being performed) when solved simultaneously will always yield a unique solution for the given parameter values. The task of generating these equations and the solution process may become difficult and error prone, especially with large number of circuit components. A particular difficulty arises when nonlinear components such as diodes and transistors are introduced.

A scientific computer can easily perform the mechanics and produce the solution more rapidly, economically, and more reliably than manual techniques. However, a computer always requires a well-defined algorithm capable of processing the general case. Such an algorithm has been developed for the program used for this analysis.

The input to the computer program is a description of the circuit components and their interconnection. The values of all components and sources are also defined. In addition, all components defined in the description also include the appropriate tolerances for the statistical analysis (these tolerances may include purchase, temperature and component aging tolerances depending on the application). A density function, which defines the statistical distribution for each component is also given. From this information, the program generates the set of Kirchoff current equations which define the network. These equations are then solved repeatedly using random selection of parameter values, according to the statistical distribution specified, thereby producing a statistical variation for the desired output quantities.

The program is able to determine the effects of component variation on the output parameters. Two types of sensitivity are computed by the program. The first considers the assigned spread of each circuit parameter about its mean value to determine the effect of each parameter variation on the output parameters separately. The second sensitivity is computed when each component value is varied only by 1 percent from its nominal values. This information is particularly useful in reducing the instability of a network whose operation is critically dependent on a circuit parameter. This type of information is generally unobtainable from a "breadboard" simulation.



## The Monte Carlo Method

The Monte Carlo method of treating system analysis is a scheme by which the performance of a large number of simulated samples (usually 10,000) of a system can be evaluated when the system is comprised of elements with values that may vary between tolerance limits. By repeatedly selecting random combinations of these parameters and computing the variables of the system, a valuable indication of the probability of meeting specific performance criteria can be derived for the system.

The first step of the Monte Carlo process consists of computing a random number  $X$ , which has a value between 0 and 1, by means of a uniform random number generator built into the program. The cumulative density function gives the probability of the random variable being less than or equal to a given specified value. From this function  $F$ , as shown in Figure IV-1, for the normal distribution and Figure IV-2 for the uniform distribution, the component parameter values to be used in each simulation can be selected randomly.

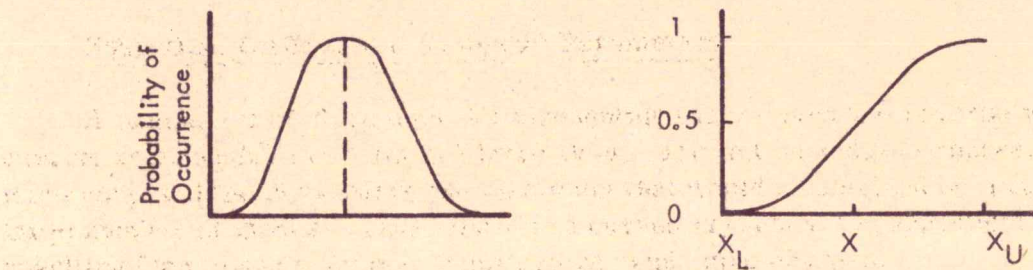


Figure IV-1. Density and Cumulative Probability Function for a Normal Distribution

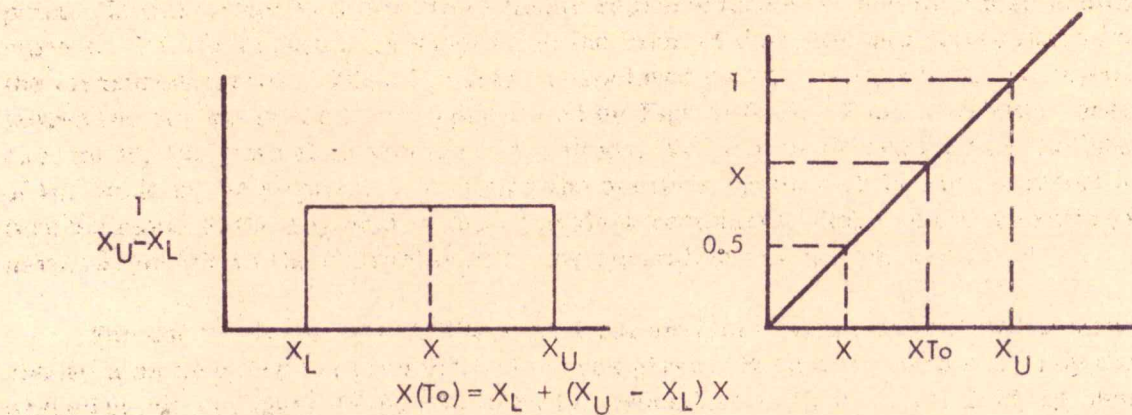


Figure IV-2. Density and Cumulative Probability Function for the Uniform Distribution



In general, the frequency distribution for each component may be obtained by measuring a sample lot of components, plotting their histograms in discrete intervals, as in Figure IV-3, then smoothing the histograms and normalizing so that the total area under the curve is equal to 1. This arrangement makes it possible to generate random component values for all circuit components using a single uniform random number generator and a different cumulative density function for every component. These cumulative density functions range from the simple first-order polynomial for the uniform distribution, to higher-order polynomials. The order of these equations is based on the number of points supplied to describe the function.

The second step of the Monte Carlo process is to simulate the circuit performances by substituting the generated random component values into the Kirchoff current equations generated by the program.

The most commonly encountered statistical distributions are those that closely approximate a common class of physical variation. These distributions are the normal, uniform or rectangular, and the exponential distribution. Each of these and two others which are defined by the analyst for his application are permitted in this program.

#### Equivalent Circuits for Nonlinear Parameters

A typical set of diode curves representing the forward and reverse voltage-current relationship is shown in Figure IV-4. The left hand curve represents the minimum, and the right curve the maximum that would be obtained by measuring a large number of diodes. Thus, these two curves represent the statistical limits resulting from manufacturing, temperature, and aging changes.

A diode, for example, may be represented by the equivalent circuit of Figure IV-4 provided the values of  $V_d$  and  $R_d$  are obtained from the diode curves at each operating point. In this program a piecewise linear representative is used for these nonlinear curves. This information is supplied in the form of discrete data points taken from the measured curves. When linearly interpolated between data points, the computer stores the curves in the form represented by Figure IV-5. For a particular operating current  $I_d$ , the equivalent voltage of the diode,  $V_d$ , can be determined as the intercept of the diode curve segment, containing the operating point and the zero-current axis. The inverse slope of the segment is the equivalent resistance,  $R_d$ . As the operating point moves up and down the characteristic, the equivalent voltage and resistance values change.

For each of the cases for the statistical analysis, a random number is used to choose a diode curve between the two curves given. Such a curve is shown by the dashed curve in Figure IV-5. An iterative procedure is then used to find the operating point. As a first estimate, a current for the diode is assumed. From this, the  $V_d$  and  $R_d$  are computed. Using this data the Kirchoff current equations may be solved for the circuit node voltages. The diode current is now computed in terms of these node voltages. When the newly calculated current lies on the same segment as the previous one, the



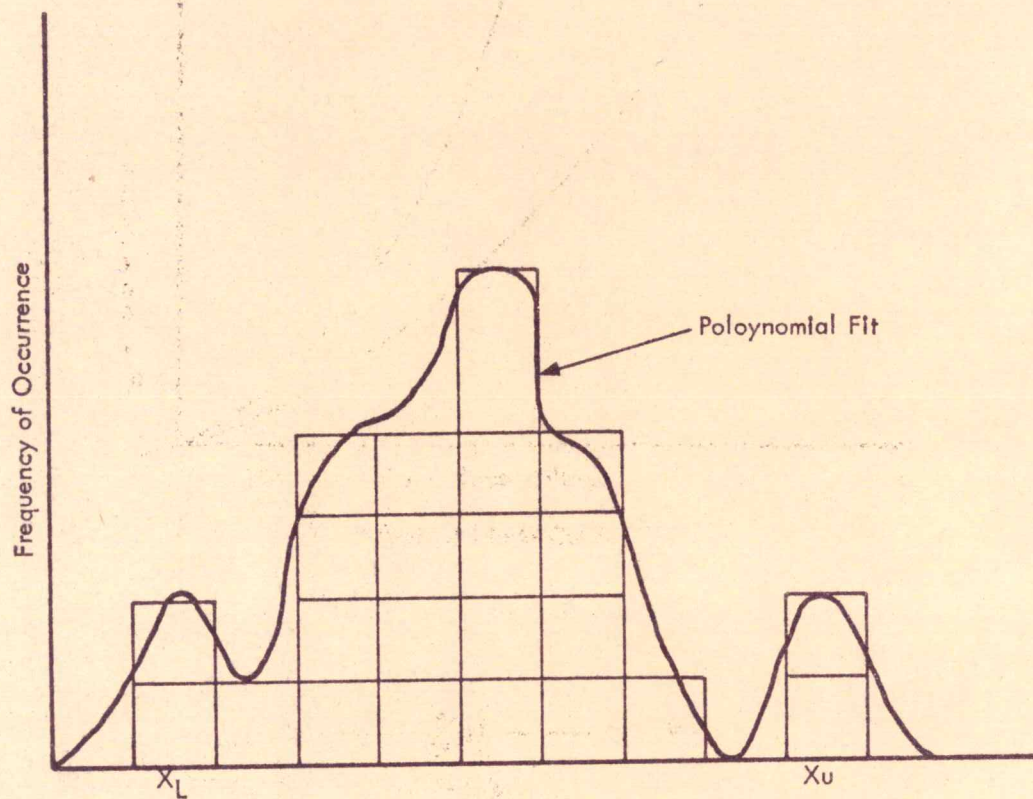


Figure IV-3. Histogram of Empirical Frequency Distribution of Component Parameter Values, Smoothed by Polynomial Curve Fitting



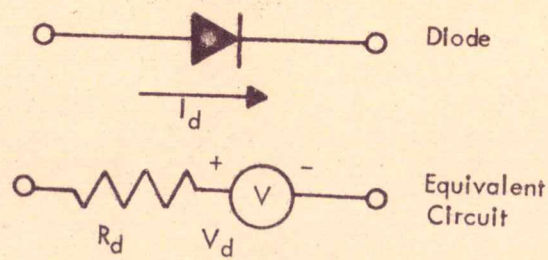
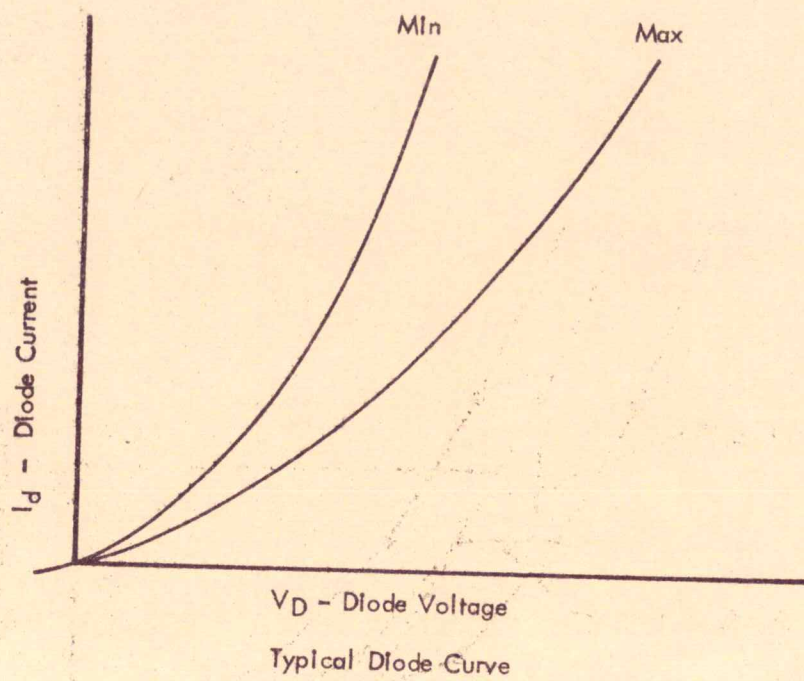


Figure IV-4. Diode Characteristic Curves and Equivalent Circuit for DC Analysis



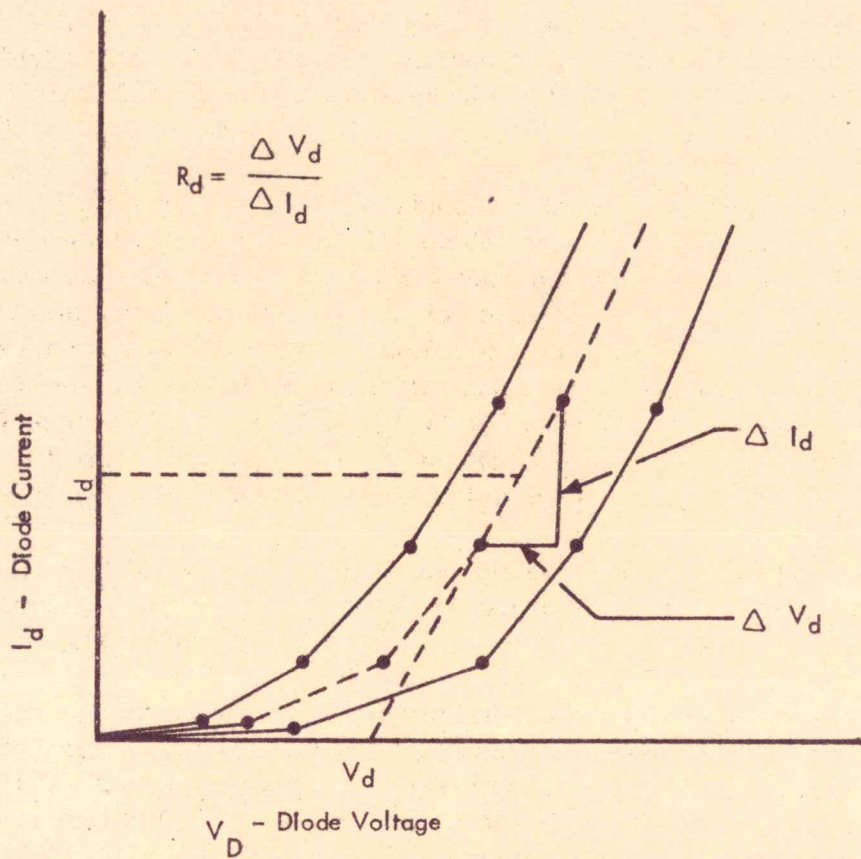


Figure IV-5. Segmented Diode Curves



solution is found. If the circuit is composed of more than one diode, each diode curve must satisfy this convergence criterion before a solution is produced. The accuracy of this diode model is dependent on the number of segments supplied for the nonlinear characteristic.

In the case of a zener diode the curve representation and the solution for the operating point is the same. The only difference is that the reverse characteristic is the one of primary interest since it describes the zener breakdown region as shown in Figure IV-6.

The transistor equivalent circuit which was found to be most useful is the large signal model shown in Figure IV-7. The diode between the base and emitter junction describes the input characteristics of the device under consideration. Similarly, the diode between the base and collector junction describes the output characteristic. Each of these diode curves may include the same variations used for a normal diode. A dependent current source between collector and base completes the piecewise linear large signal equivalent circuit. This model will properly define the operation of a transistor in all three regions of operation. The iteration procedure used to obtain the operating point is the same as discussed for the diode.

In the present form the statistical analysis program will produce solutions for circuits of size up to 50 dependent nodes, 40 diodes or 20 transistors, 5 distribution shapes and 75 input parameters.

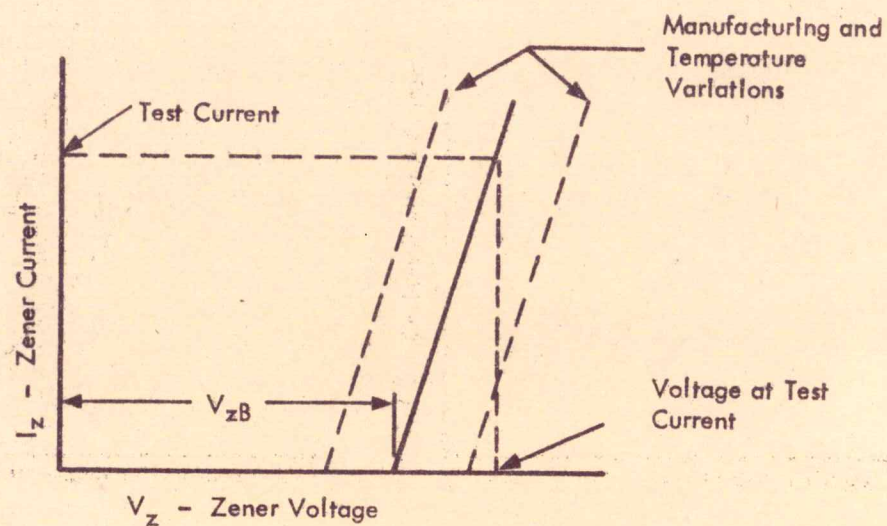
Although circuit breadboards will be needed for preliminary design, it has been shown that statistical circuit analysis of the type discussed in this report have produced more information for a particular circuit than breadboard testing. In a laboratory test, only one set of parameter values for a circuit may be tested at a time. In the program, however, 10,000 cases are simulated in the same test environment. This simulation then produces the effect of the test environment on the circuit for all combinations of circuit parameters for the given distribution of values. In addition, the automated analysis is more reliable, more economical and usually requires less time than breadboard testing.

## B. PREDICT DESCRIPTION

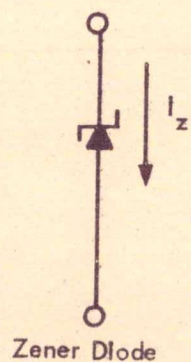
### TRANSIENT CIRCUIT ANALYSIS COMPUTER PROGRAM

PREDICT is an automated digital computer program for determining circuit transient responses. The program is primarily intended to determine the transient response to a nonperiodic forcing function. It is possible, however, to use PREDICT for ac and dc steady-state analysis. The analysis is of a nonstatistical nature.

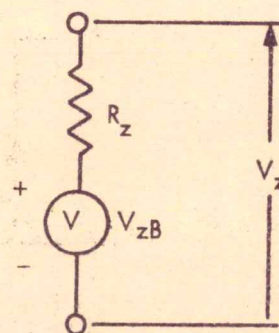




Typical Zener Characteristics



Zener Diode



Zener Diode  
Equivalent CKT

Figure IV-6. Zener Diode Characteristic Curves and  
Equivalent Circuit for DC Analysis



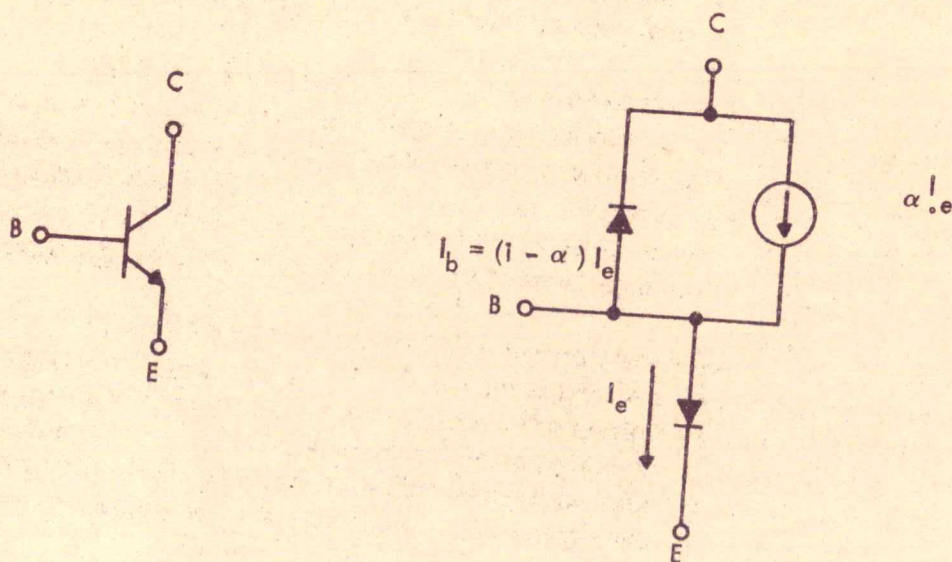
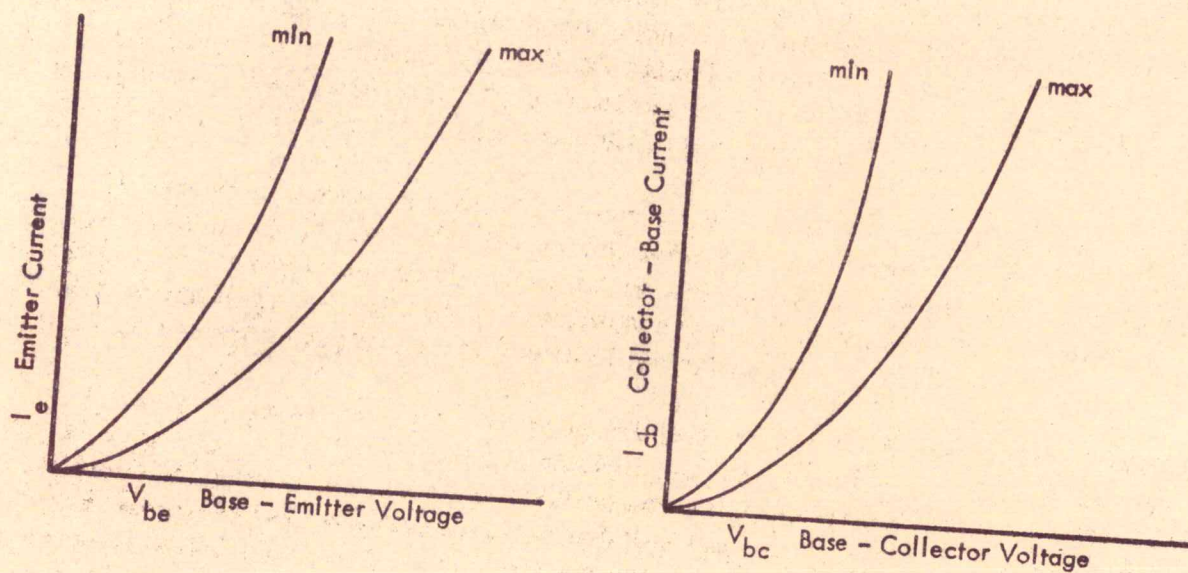


Figure IV-7. Transistor Characteristics and Equivalent Circuit, DC Analysis



The input to the program consists of a description of the circuit elements and the interconnections written in a language compatible with the program. Passive elements are defined as invariant with respect to time. If components were permitted to vary statistically as in ASAP (see ASAP description of this appendix) the time solution would be meaningless. Any combination of finite valued voltage or current sources is permitted as driving functions. These sources may be defined by mathematical expressions or by piecewise linear functions in the form of tables.

All variables vary with respect to time but may be dependent upon circuit conditions and parameters. This gives rise to equivalent transistor models. These models are inserted in the program as a network of active and passive elements. Thus, the analyst can derive and simulate any high or low frequency equivalent transistor model to satisfy his requirements within the limits of the program.

From the input description, the program generates a set of differential equations. These equations are evaluated using numerical integration methods. The integration time step size, and consequently the solution accuracy, is controlled with direct input instructions by limiting the step size and solution error. Various integration routines are available depending on the accuracy desired. The most common routine used has an accuracy of approximately  $\pm 1$  percent while other routines can attain an accuracy of  $\pm 0.01$  percent. As would be expected, the greater the accuracy desired, the more real machine time required. However, in the interest of saving machine time, the program varies the integration step size within the limits specified to use the largest possible step size and still maintain the desired accuracy.

The program output is a time history of the requested network quantities such as branch currents, branch voltages, and source values. These outputs are tabulated at each integration step time interval and can be obtained in the form of machine plotted graphs if desired. Any circuit parameter such as power dissipations which depend on more than one basic circuit parameter may be obtained by inserting a branch and defining that branch with a mathematical expression containing the appropriate circuit parameters.

The results of the PREDICT computer program can be only as accurate as the information inserted, i.e., only as accurate as components, such as transistors, can be mathematically represented. Since the components are invariant, the worst-case conditions must be determined by the analyst. In most cases, the computer program is faster and more efficient than breadboard testing. The Program is considered much more accurate and reliable than performing a hand analysis.



## ADDENDUM TO WORST-CASE CIRCUIT ANALYSIS OF SWITCH SELECTOR MOD II

### WORST-CASE TIMING

The Switch Selector will operate as described by IBM Specification No. 6009026 in all respects with regards to timing with the exception of two instances. These are associated with the implied continuity of voltage levels from the unselected output channels while under the influence of or just after the Read Command and the zero (up level) verification output levels when the stage is selected. In particular, an unselected output channel may produce an accumulated discontinuity of up to 300 microseconds duration in any 10-millisecond period. Similarly, the verification outputs may exhibit an accumulated discontinuity of up to 125 microseconds in any 2-millisecond period.

The unselected output discontinuity can occur under the following conditions:

1. The unit must be exposed to a vibration environment that is sufficient to cause relay contact motion. These levels are approximately equal to the qualification levels in Specification No. 6009026.
2. The unit must be exposed to a worst-case temperature environment (cold).
3. The stage supply voltage must be toward the upper specified limit, i.e., 30 volts.
4. The internal power switching circuitry exhibits near limit timing characteristics as built and a short mode fault develops in one of six capacitors in the control integration circuitry.

If all of these conditions simultaneously occur and the Switch Selector is operated, the mechanism is present to cause an unselected channel to turn on in a transient fashion.

The verification discontinuity can occur when the unit is in a relatively severe random vibration environment. This is caused by the relay contact motion which may occur in this environment and causes the contact to momentarily open.

It is generally assumed that even if these discontinuities are produced, there will be no serious effect on the intended mode and sequence control of a Saturn vehicle.