410-TM(700) REVISION No. 4

KW Smith

# TRAINING MANUAL

ACE-S/C
DATA ACQUISITION SYSTEM
(PCM DECOMMUTATOR)

CONTRACT NASW-410

TECHNICAL TRAINING UNIT

APOLLO SYSTEMS DEPARTMENT

MISSILE AND SPACE DIVISION

GENERAL ELECTRIC COMPANY

DAYTONA BEACH, FLORIDA

410-TM(700)

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DATA ACQUISITION SYSTEM
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Contract NASw-410

1 April 1969

Technical Training Unit Apollo Systems Department Missile and Space Division General Electric Company Daytona Beach, Florida

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#### FOREWORD

Throughout this manual many references are made to figures that are not a part of this manual. These figures are logic diagrams in a separately bound document. The callouts for these diagrams are recognizable in this text by the word "figure" being in all lower case letters. Callouts for illustrations that are a part of this manual are referred to with an upper case (Figure \_\_) designation.

#### SECTION 1

#### INTRODUCTION

#### 1.1 GENERAL

The purpose of the series 540 PCM decommutator is two fold. First, to decommutate serial PCM telemetry data from the Apollo spacecrafts, assign routing addresses and drive digital and analog displays such as meters, lights, and recorders in the ACE-S/C control room. Second, to decommutate serial PCM telemetry data from the Apollo spacecrafts, perform preprocessing, storage assignment, and route to the ACE-S/C downlink computer for further processing and display.

The decommutator is a programmable device; therefore, many variables could be introduced if presented as a general-purpose system. However, this manual will describe only the usage as it applies to the ACE-S/C present programmed equipment configuration. But, bear in mind that as a result of the evolution of the ACE-S/C programming philosophy, certain inconsistencies between this written description and actual programs may exist.

## 1.2 FUNCTIONAL DESCRIPTION

The PCM decommutator (Figure 1-1) is capable of operating over a wide range of input telemetry data and can also accept a variety of types of PCM coding and various arrangements of parameter data specified by the telemetry system. To meet the demands of versatility in operating range and the requirements of recording, display, and data processing systems, the decommutator operates under program control. In the ACE-S/C configuration, both the interleaved and the airborne decommutation programs can be stored by the decommutator memory simultaneously. This gives the capability of rapid acquisition for each type of input available.

To obtain synchronization on the incoming data, the decommutator must be programmed with the criteria for bit synchronization, prime frame synchronization, and major cycle synchronization. Bit synchronization exists when the decommutator defines the exact same period of time as was generated by the telemetry system and decodes the weighted digit in its true form. Prime frame synchronization exists when the decommutator recognizes the beginning of a repetitive group of coded bits which divide a given amount of time into equal parts. In the ACE-S/C telemetry system this code

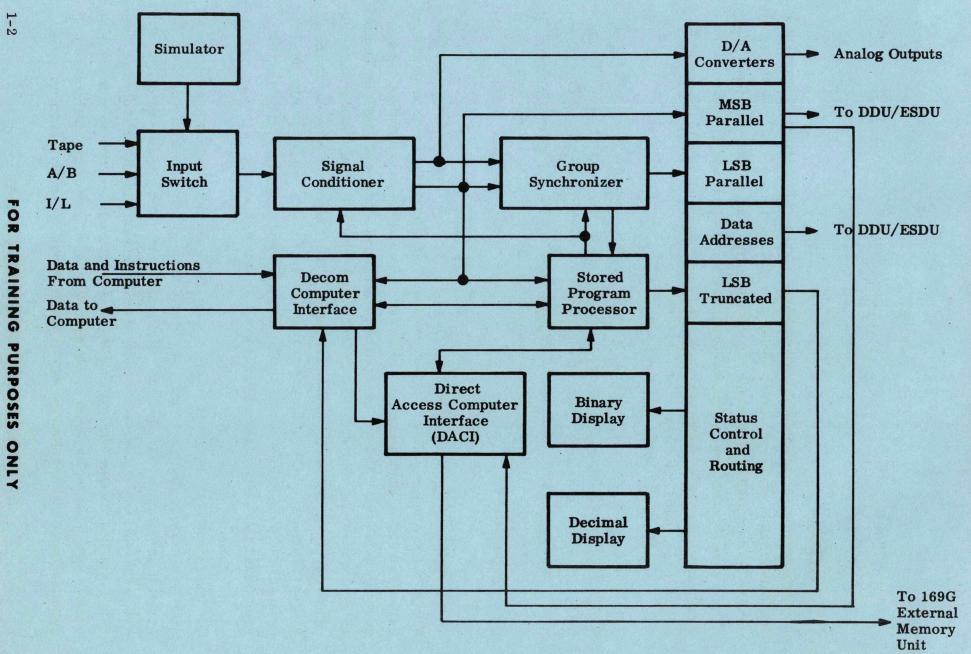


Figure 1-1. PCM Decommutator

appears 50 times per second; therefore, the system divides a one-second time span into 50 equal units. Major cycle synchronization is when the decommutator recognizes a specific prime frame and can then define the same real-time second as generated by the telemetry system. After completing these three steps of synchronization the decommutator memory is synchronous with the input data; therefore, the decommutation process can be initiated.

The basic parts of the decommutator are the signal conditioner, the group synchronizer, the stored program processor (memory), the output rack, and the decom/computer interface (normal and DACI). All operate under program control of the particular program in operation.

#### 1.3 SIGNAL CONDITIONER

The PCM signal conditioner (Figure 1-2) accepts the incoming split-phase pulse code modulated telemetry signal, conditions the pulses, and synchronizes with each bit to control the decommutator timing. The signal conditioner acts upon the incoming PCM signal to restore the data to a ground level and provide a stable output for the entire decom. This is performed to enable more efficient decommutation by the remaining sections of the decommutator.

Decommutation of the incoming PCM data can only be performed if the decommutator timing is synchronized with the bit rates of the commutation processes. Therefore, various time slots containing discrete words can be processed or decommutated to reproduce the exact data used in modulation during the commutation of the spacecraft parameters. The input signal to the decommutator when used in the ACE-S/C capacity is split-phase-C PCM data. This input signal is then converted to NRZ-C and NRZ-M with the NRZ-C being sent to the group synchronizer.

The signal conditioner consists of three principal subsystems:

- a. A dc restorer.
- b. A bit synchronizer.
- c. A bit detector.

The dc restorer accepts the serial data train as an input and supplies level-restorer signal to the bit synchronizer and bit detector. The bit synchronizer outputs are a clock at the bit rate of the data and timing signals for the system. The bit detector accepts the clock timing signals from the bit synchronizer and the data train from the

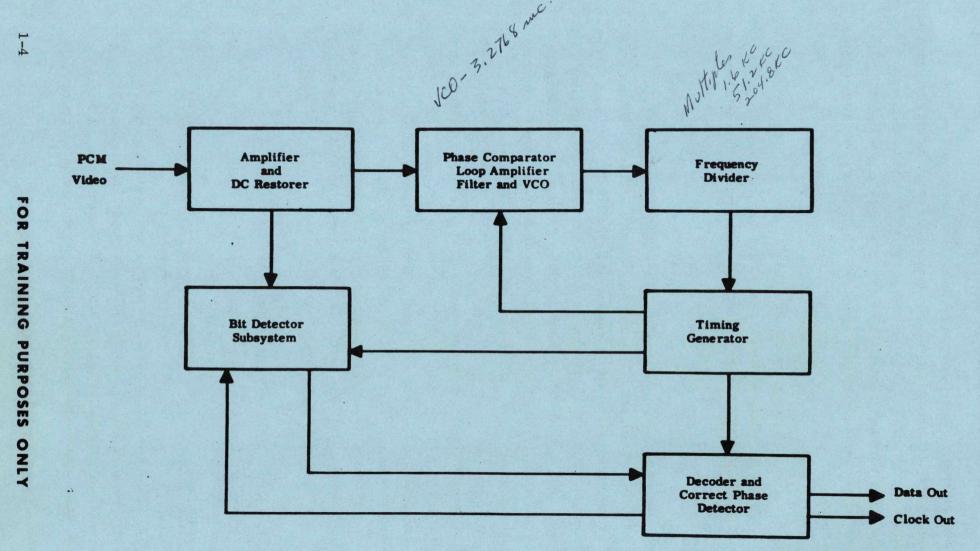


Figure 1-2. PCM Signal Conditioner

dc restorer. It then produces reconstructed serial NRZ-C digital data as an output. Thus, the bit detector performs the basic decision of whether a binary "one" or "zero" exists for each bit.

For split-phase data, the clock defines only the carrier frequency, for the bit location is subject to an ambiguity. The bit detector resolves this ambiguity, locates the bit position, and makes the bit polarity decision. The phase decision is made on the basis of several bits to reduce the probability of an error as a result of noise and uses as criteria the definition of SP-C data where two adjacent half cycles of a bit period are never equal.

#### 1.4 GROUP SYNCHRONIZER

The group synchronizer performs two different types of synchronization. First, it must establish prime frame synchronization and then major cycle or ID synchronization. The information used as criteria to perform these functions must be programmed in memory and called up as instructions for the synchronizer as follows:

- a. Prime frame length.
- b. Prime frame pattern.
- c. D counts up or down.
- d. Location of ID word.
- e. Number of errors accepted in synchronization.
- f. Number of prime frames to be checked.
- g. ID MSB/LSB first.

The serial data from the signal conditioner is shifted through a shift register (accumulator) of the frame synchronizer (Figure 1-3) where a bit-by-bit comparison of the input data is made with the pattern and length placed in storage after memory callup. When the pattern of the prime frame sync word (32 bits in ACE-S/C) matches the stored pattern, a first prime frame sync signal is generated and enables the check mode of operation. Heretofore, the synchronizer has been in the search mode looking for a correlating pattern. This first prime frame sync signal not only enables the check mode but informs memory that a pattern has been found. Since it is highly possible that a sync pattern can be found any place in a prime frame with an arbitrary group of data bits, memory must instruct the frame synchronizer where the next pattern is located. To do this, it generates a signal call aperture which enables a prime frame sync pulse to be checked the next time it should appear. If the first sync pulse was a valid one, then the next prime frame sync pulse should fall within the aperture; however,

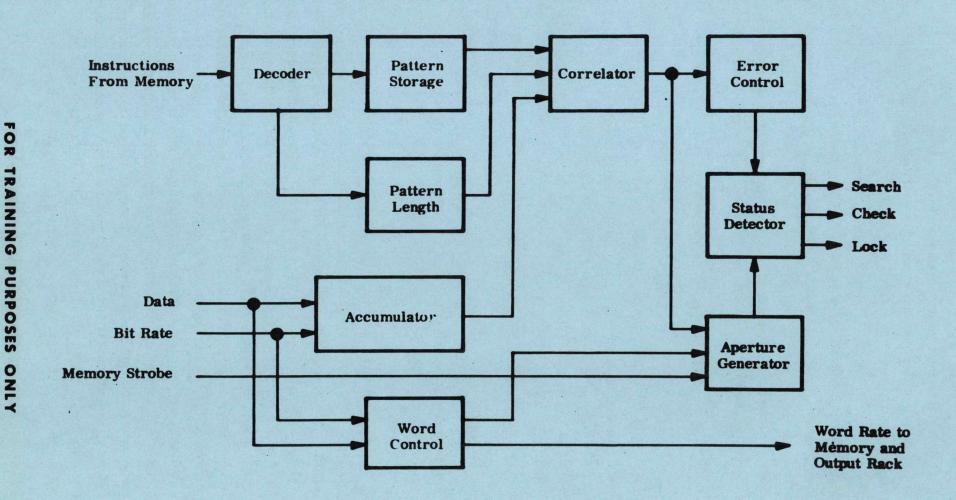


Figure 1-3. Prime Frame Synchronizer

if the first sync pulse was invalid, it is extremely unlikely that at the same time in the next frame an arbitrary group of 32 bits will match the pattern and generate a sync pulse; therefore, the pulse would not fall within the aperture and would generate an error. If this exceeds the number of errors allowed, then the system returns to the search mode to obtain the proper sync word.

After the proper sync word is obtained and the check mode entered, the synchronizer checks the sync word with the pattern a predetermined number of times to establish that proper synchronization has been obtained. During this mode, the ID synchronizer is enabled.

The function of the ID synchronizer (Figure 1-4) is to enable the unit to begin decommutation as readily as possible. Memory instructs the group synchronizer where the ID word occurs and enables the ID word to be detected. This detected word is sent to memory control where it jumps the memory sequence to the prime frame detected. At this point, major cycle sync has been obtained. Each prime frame contains an ID word and during this time slot the new ID is checked against the updated contents of the synchronizer. If these two do not correlate, the ID synchronizer returns to search.

## 1.5 STORED PROGRAM PROCESSOR

The stored program processor (Figure 1-5) provides storage for key instruction words used by the group synchronizer, DACI and the output rack for processing data under program control. It also stores synchronized code information that enables the group synchronizer to get in step with the data train and to reacquire synchronization with a minimum of words if synchronization is lost. The stored program processor consists of random-access core-memory, input/output devices for formatting, control logic for loading and unloading instructions, and a memory control panel for entering or selecting data manually. The core-memory has a storage capability for 8192, 40-bit words.

The stored program processor is capable of operating on one decommutation program while loading another into the memory on a priority basis (from tape and control panel only). This is accomplished by arbitrarily dividing the core memory into eight program stored sections designated 1 through 8. If this arbitrary division is adhered to, each section of memory is capable of storing 1024, 40-bit words. Of course, it is entirely possible to have only one or two programs take up the entire 8192, 40-bit storage locations.

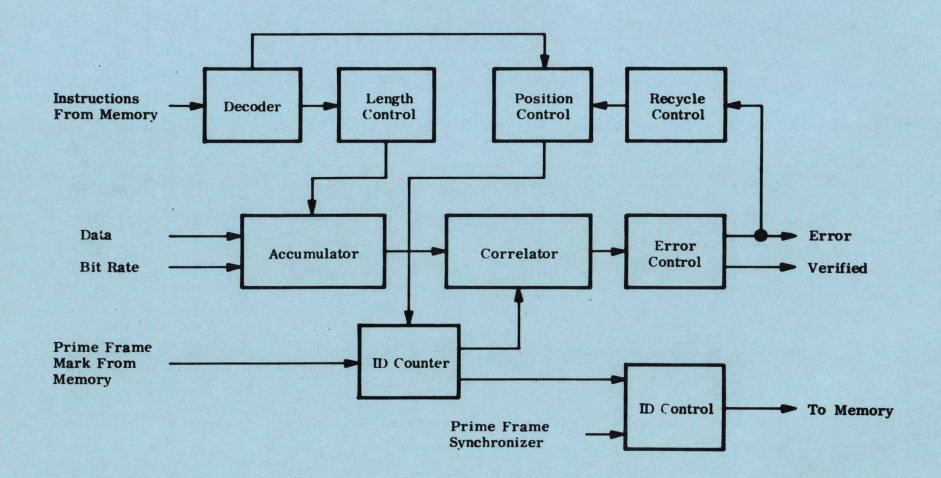


Figure 1-4. ID Synchronizer

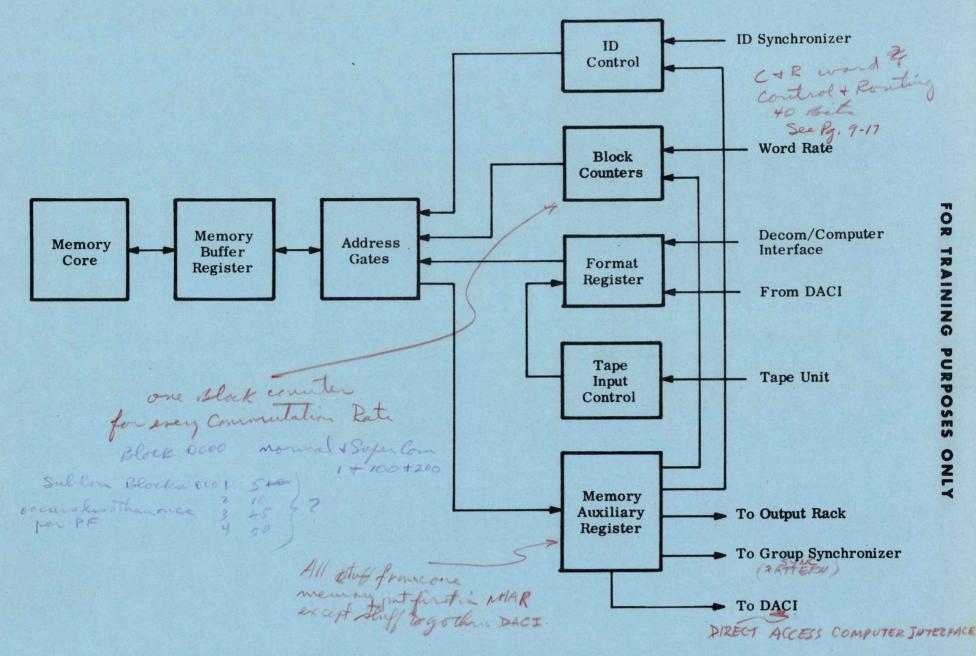


Figure 1-5. Stored Program Processor

A program can be loaded into the stored program processor from a digital computer, the paper tape reader, or manually from the program control panel. For the program entry, a 13-bit address for starting the loading is the first word in a given program. Thereafter, the stored program processor updates the address for sequential loading of memory slots. A program can be loaded into one program section of memory, while the stored program processor is operating from another program section, provided the word being decommutated has a word length of at least seven bits.

Program instruction words from a computer and the paper tape reader are formatted into the instruction word format used by the stored program processor. If the instruction word is from a computer, it is furnished in the form of four words or characters. one 4-bit and three 12-bit words or characters. The words or characters are formatted into a 40-bit word by the formatting gates and the 40-bit word is loaded into the data register. Word formatting is controlled by the format counter and decoder. This functional area loads the correct set of formatting gates based upon the number of words or characters transferred. For the first four-bit word or character transferred from the computer, the format counter loads the first four most significant bit formatting gates. It notes the fact that a word has been transferred and when another word is ready, loads the next set of formatting gates (corresponding to the 12 next most significant bits of the instruction word). Upon completion of word formatting, the word is transferred to the core-memory register by the master load gates. The word is subsequently stored in the address designated by the program. When this word is stored, the computer sends another program word, and the counter address is updated, and another word is stored in the next sequential address of the memory. The process continues until a complete program is loaded.

A similar process is required for loading instruction words from the paper tape reader. The starting address for program loading is the first word on the tape. The tape reader furnishes input words in the form of one 4-bit word or character and six 6-bit words or characters. These input words are formatted and stored in the memory by the same process described for computer inputs. The process continues until a completed program is loaded. Instruction words entered from the program control panel do not require formatting. The starting address for storing the words is manually entered at the program control panel. Thereafter, the load/unload counter updates the address for sequential loading of the memory. No manual loading can be performed during decommutation; however, the address of stored instruction words can be changed using controls on the program control panel.

The stored program processor operates in two basic modes—preacquisition and decommutation. In the preacquisition mode, all the criteria is called out of memory and is the criteria for memory control in the same manner discussed in the synchronizer. Memory is controlled during the decommutation process by block counters which are jammed to the starting addresses of the data contained in prime frame one of the telemetry input format for a particular program. These block counters fall into two categories—ID and control and routing. When the ID word is verified, the ID block counter causes the block counters used for control and routing to be jammed to the address of the prime frame when major cycle synchronization is found. At this time, the exact location of every word is known in the major cycle.

The control and routing format contains instructions for memory control and the formatting process performed by the output rack. The next block instruction causes the block counters to access the next memory location applicable to the incoming data word. The instructions contained in a memory location are for the next incoming word. Therefore, the decommutator operates one word time ahead of the incoming data.

## 1.6 OUTPUT RACK

The output format devices (Figure 1-6) are used to convert the NRZ-C data into the proper format determined by the equipment to receive the data word. The gating of the data word into the proper output register is determined by the program in the stored program processor. The output format control unit receives serial reconstructed NRZ-C data from the output of the PCM signal conditioner, timing from the group synchronizer, and program control instructions from the memory. The output format control unit provides analog and digital data outputs to the external units. Parallel binary and binary-coded-decimal (BCD) data are also provided to data displays on the system control panel, which gives the operator the capability of displaying any incoming data word in its time binary or decimal value.

The outputs of the digital-to-analog converter circuit are routed to the event distribution and recorder patching unit to be distributed to the analog recorders located in the computer room. The data routed to the downlink computer comes from the least significant bit truncated register or DACI where they are transferred as 12-bit and 30-bit parallel data words respectively. The data transmitted to the decommutator distribution and event storage and distribution unit, in the control room, are routed through the MSB parallel register. The addresses (from memory) applied to the data of the

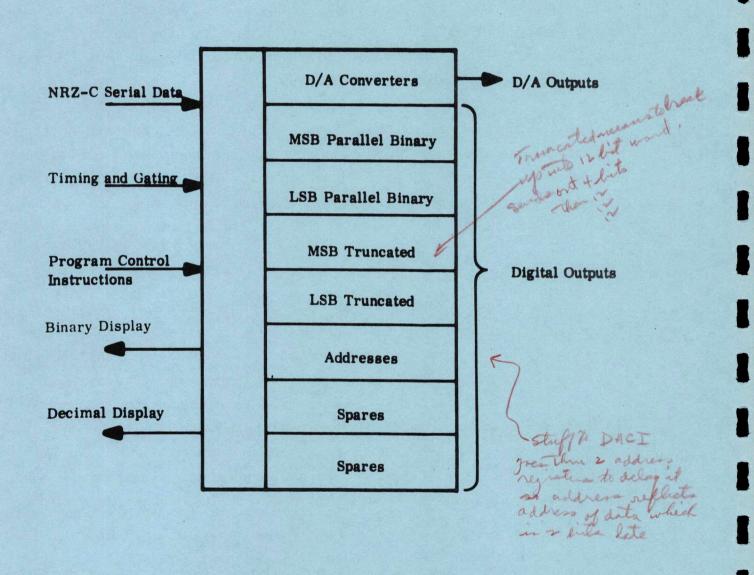


Figure 1-6. Output Devices

MSB parallel register are routed through the data address register. The remaining output devices are not used in the application with ACE-S/C.

#### 1.6.1 DIGITAL-TO-ANALOG CONVERTERS

The digital-to-analog (D/A) converters convert the incoming digital data to analog voltages to be distributed to the event distribution and recorder patching unit. The decommutator contains a total of 60 D/A converters of which 40 are used in the transmission of data to the recording and patch unit. The D/A converters are selected by the stored program processor. The memory instruction performs three functions in controlling the D/A devices:

- a. Controlled designation of which D/A will convert the incoming data word.
- b. When the D/A will be selected.
- c. Synchronization of gating the incoming data into the converter.

#### 1.6.2 MSB/LSB PARALLEL OUTPUTS

The function of this group is to provide as an output all data words in both MSB and LSB first formats at the same time. Any data word may be from 4 to 64 bits long. The different conditions under which the registers can accept data are:

- a. No parity or word synchronization code bits in the data word and either MSB or LSB first.
- b. Parity and word synchronization code bits present in the data word either at the beginning or the end of the word and either MSB or LSB first.

The program of the system being monitored dictates the mentioned conditions. The data is serial when received and is converted to parallel by a formatting process.

After the entire word has been formatted, the new data word is shifted left the number of places corresponding to the number of parity and word synchronization code pulses contained in the word. The action takes place if word parity and word sync are used. In the ACE-S/C application, word parity and word sync are not used.

The MSB formatting and parallel registers are composed of 33 stages while the LSB formatting and parallel registers are composed of 64 stages. The reason for this is that it is only necessary to acquire one more MSB bit than half the word length to determine the value of the measurand while the entire word in LSB form must be gathered to determine which bits are the MSB of the word.

Also contained in the MSB/LSB parallel registers logic is the 12-bit display address register which feeds the ESDU and the console control logic circuits. This address with a read pulse is gated out in parallel with the contents of the MSB parallel register. The LSB parallel drives the decom binary display.

#### 1.6.3 MSB/LSB TRUNCATED OUTPUTS

Truncate means to cut up or cut off. Truncation circuitry is used when the decommutator operates in conjunction with 160G computer. If the incoming data word is too large, the truncated output will be in characters whose lengths are compatible with the computer input. This allows the decommutator to maintain its versatility and still allow the remaining units of the ACE-S/C system to function at their specific capability. The MSB/LSB truncated unit operates basically identical to the MSB/LSB parallel unit with the exception of a calculator which divides the incoming word by a factor of two until a remainder is obtained. This remainder is outputted as the first truncated character which will vary in length with varying lengths of incoming data. However, the remaining characters will all be the same dependent upon the initial size of the incoming data word.

The ACE-S/C application utilizes the least significant truncated circuits and outputs the data words to the decommutator/computer interface unit.

#### 1.6.4 DECIMAL AND BINARY DISPLAYS

Three decimal displays and one binary display provide the capabilities for selecting and displaying the decimal and binary values of words from registers in the output rack.

The three decimal displays operate independently; that is, all three can be used concurrently to select and display one word or three different words. Any word in the data train up to octal 7777 (decimal 4095) can be selected on any one display. The decimal displays are wired for word values up to 999, 999; however, the displays only contain modules for word values up to 999.

The binary display provides the capabilities for selecting and displaying any of 4095 data words. A 64-bit word plus parity can be displayed. In addition, word synchronization can also be displayed.

The decimal and binary displays function identically, except for the fact that the decimal displays must decode the BCD inputs. The decoding operation performed for decimal displays can be ignored when evaluating the operation of the binary display.

## 1.7 DECOMMUTATOR/COMPUTER INTERFACE

The computer interface unit is designed so that a free interchange of data and instructions can be carried on between the Radiation Series 540 PCM acquisition and stored program decommutation system and a digital computer. The unit converts the logic level of the decom to that required by the computer. The unit also decodes the various instructions from the computer and causes the decommutator to comply with them. In addition, the unit provides a path through which a complete program can be inserted into the decommutator memory or an existing program can be modified or checked. All interchange between the computer and the computer interface unit is performed by parallel transfer.

The decommutator sends two types of words to the computer through the computer interface unit. Both types of words are sent upon request of the computer. The two types are truncated data words (characters) with a maximum of 12 bits per character and a status word. The truncated characters are routed from the decommutator LSB truncated character register through the computer interface unit which converts the logic levels to be compatible with that required by the computer. The status word is partially generated within the decommutator and tells the computer the status of the decommutator at the time of receiving the request from the computer.

All data transferred into the computer memory from the decommutator and all data transferred from the computer into the decommutator memory must be under the direct and complete control of the computer program. The decommutator can be synchronized on the incoming data train and, in effect, to the entire decommutation process. However, no data is transferred through the interface unit until requested by the computer. Initiation of this transfer is effected by control words and control functions generated by the computer.

# 1.8 DIRECT ACCESS COMPUTER INTERFACE (DACI)

The DACI is essentially in parallel with the decommutator normal interface circuitry (Figure 1-7) and enables the ACE-S/C decommutator to input addressed data directly into the 169G external memory unit. The decommutator output circuitry (normal or

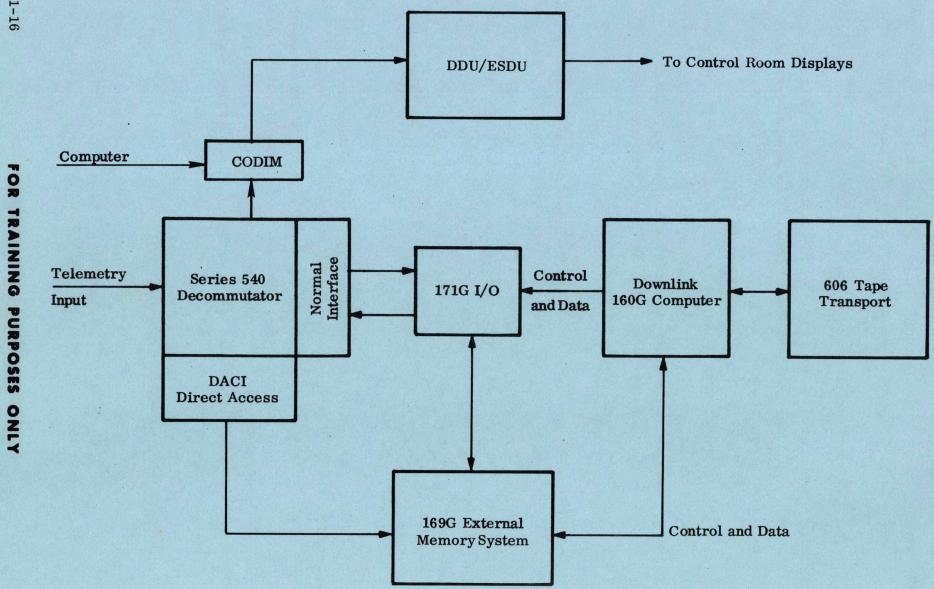


Figure 1-7. Interconnection Diagram

DACI) will be selected by the preacquisition block of the decom program. The DACI is then enabled by the 160G downlink computer. The decommutator control and routing words define which PCM words are to be transferred to the 169G. The information transfer from DACI to the 169G will be as follows:

a. 17 address bits: 4 Memory bank select

13 Memory address

b. 13 data bits: 8 Data

2 Blank

3 Flags

The decommutator also has the capability to perform parameter limit checks, floating point checks, and event transition checks (Figure 1-8). The limit checks are performed on the upper and lower parameter values for each PCM word determined by the loaded decommutator program. The values for the upper and lower limits are predetermined and are preprogrammed into the decommutator memory prior to testing. Thus, the values provide unique checking for each telemetry word input into the PCM decommutator system.

The floating point check is performed on those parameters where the change is of significance rather than the exact upper or lower values. In this capability the last known value of a parameter is used as the next point of reference, thus the floating point technique. The event transition checking is performed in the same manner as the floating point technique in that the last event word input from the telemetry system is used as the next reference.

A flag is sent to the computer as part of the data word to tell the computer any time the limit check or floating point check was out of tolerance.

## 1.9 PHYSICAL DESCRIPTION

The stored program decommutator is housed in four equipment cabinets, each 84 inches high, 21 inches wide, and 30 inches deep (Figures 1-9 and 1-10). In addition to the Radiation-built equipment, the stored program decommutator includes a number of modified vendor equipments and off-the-shelf vendor items.

The individual cabinets are assigned assembly reference designations 1A, 2A, 3A, and 4A, from left to right. Cabinets 1A and 2A house various-sized rigid-mounted assemblies and sliding drawer assemblies, on which are mounted the operating controls of the

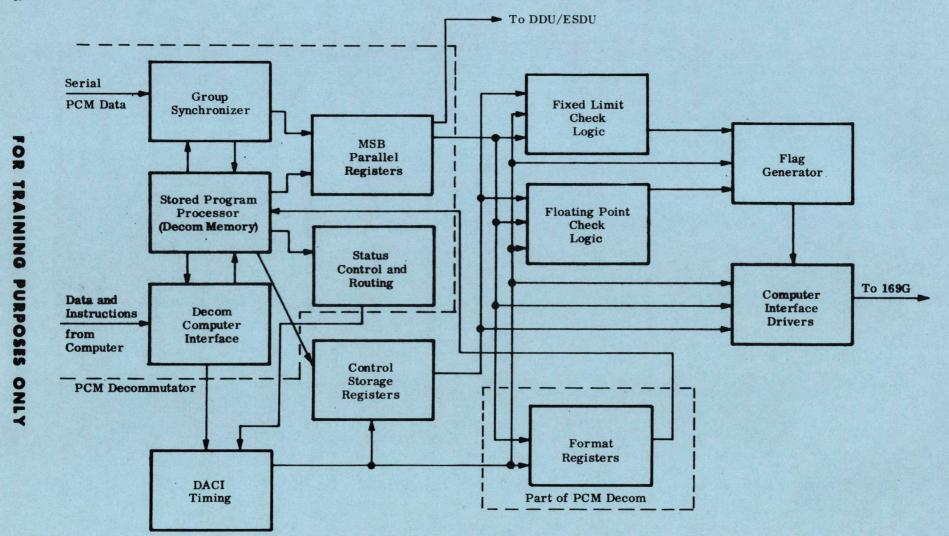


Figure 1-8. DACI/Decommutator Interface

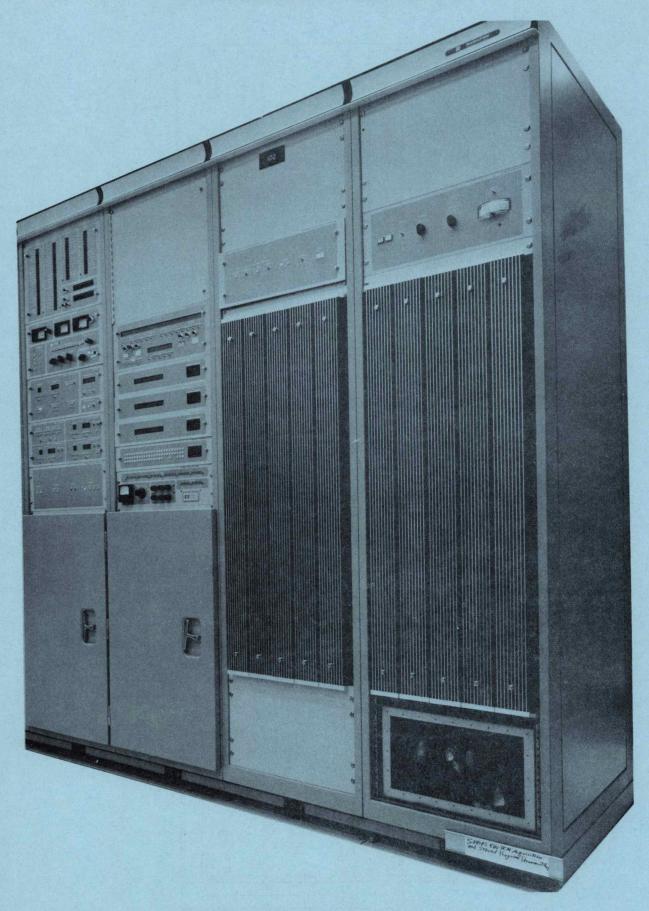


Figure 1-9. Series 540 PCM Acquisition and Stored Program Decommutator

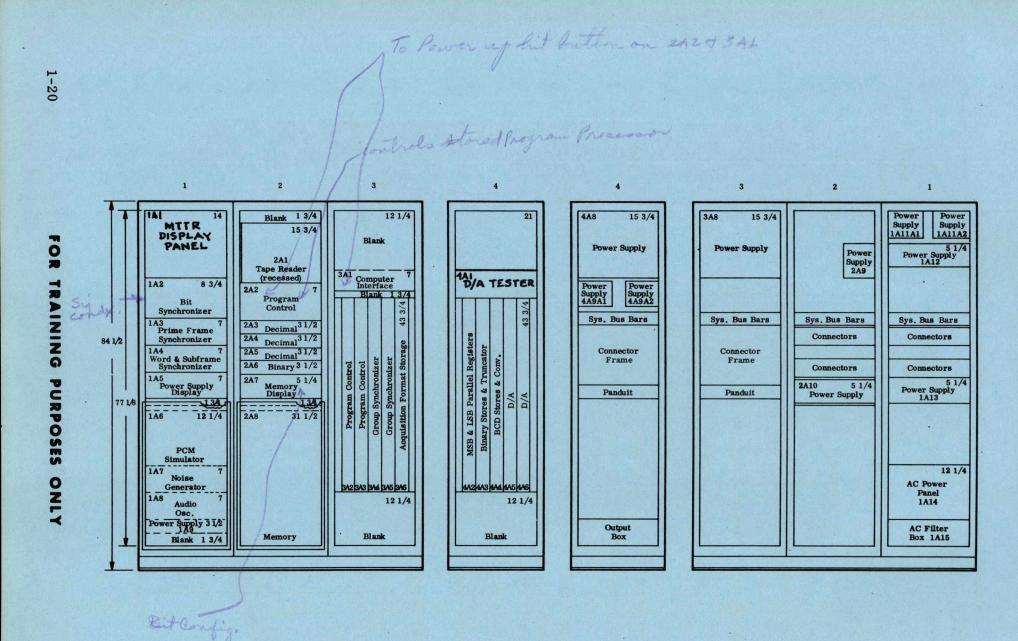


Figure 1-10. Stored Program Decommutator Equipment Location

system. Cabinet 2A also contains a core memory. Cabinet 3A contains five module panel assemblies, each capable of housing 1000 modules. Cabinet 4A also contains five module panel assemblies, each capable of housing 1000 modules. The module panel assemblies are cable-connected to terminal boards at the rear of each cabinet. They are mounted on slides for easy access to the modules, test points, and wiring.

Within the cabinets the major components (rigid-mounted assemblies, sliding drawer, and module panel assemblies) are assigned reference designations composed of the cabinet designation plus an arabic number. For example, 3A2 is a module panel assembly in cabinet number 3 drawer 2 and the modules are assigned a letter of the alphabet A through Z. These blocks are further divided into ten rows (assigned arabic number 1 through 10 and five columns, assigned A through E).

The stored program decommutator uses repairable printed circuit cards and low-cost, transfer-molded, throwaway modules. The printed circuit cards are Radiation standard printed circuit cards. The modules are assembled into 4-inch by 6 3/4-inch contact blocks, 50 modules per block. Four of these blocks are mounted into 7 1/2 by 17-inch castings, and these castings are assembled into drawers or panels. Further explanation is given under the section pertaining to Radiation logic.

## 1.10 LEADING PARTICULARS

The leading characteristics of the stored program decommutator are listed in Table 1-1.

## 1.11 CAPABILITIES AND LIMITATIONS

The pertinent data for determining the capabilities and limitations of the stored program decommutator are listed in Table 1-2. Types of PCM modulation are shown in Figure 1-11.

Table 1-1 Leading Particulars

Dimensions	
(Each cabinet)	84 inches high 21 inches wide 30 inches deep
Weight	
(Total of four cabinets with full complement)	3200 pounds (approximately)
Primary Power	
Voltage Frequency Phase Current Total Power	110 volts ± 10 percent 60 ± 3 cps Single-phase, 2-wire 40 amps, maximum 5 kw, maximum
Temperature	
Operating Non-operating Room Ambient	60° to 125°F -30° to 125°F 30° to 110°F
Heat Dissipation	
Cabinet 1A Cabinet 2A Cabinet 3A Cabinet 4A	1200 watts (approximately) 1500 watts (approximately) 500 watts (approximately) 800 watts (approximately)
Cabinet Cooling Conditions	
Inlet	60°F, +3.0°, and -0.0° Dry bulb temperature
	58°F maximum dew point (approximately 90 percent relative humidity)
Outlet	15°F expected temperature rise through cabinets.

# Table 1-2 Condensed Data

Input	
Bit Frequency	1 to 1,000,000 bits per second, NRZ; 0.5 to 500,000 bits per second; SP and RZ.
Amplitude Range	0.5 to 30 volts peak-to-peak.
DC Offset	60 percent of input amplitude.
Dynamic Range	15 to 1 without adjustment.
Input Impedance	Greater than 10,000 ohms, shunted by not more than 30 $\mu\mu$ f. May be reduced by external shunt to 120 ohms.
Codes (See Figure 1-3)	
RZ	In RZ modulation a logic "one" is represented by a pulse half of a bit-period wide; a logic "zero" is represented by lack of pulse during a bit period.
NRZC	In NRZC modulation a logic "one" is represented by one level and a "zero" is represented by another level.
NRZM	In NRZM modulation a logic "one" is represented by a change in level; a logic "zero" is represented by no change in level.
NRZS	In NRZS modulation a logic "one" is represented by no change in level; a logic "zero" is represented by a change in level.
SP	In split-phase modulation a logic "one" bit is represented by a "one-zero" code element combination. A logic "zero" bit is represented by a "zero-one" code element combination.
SPM	In split phase-M modulation a logic "one" bit is represented by a change from a "one-zero" code element to a "zero-one" code element or vice-versa. A logic "zero" bit is represented by no change in code element.
Arrangement Word-Bit	MSB first or LSB first.
Polarity	Reversible.
Connection	Three single-ended inputs and one balanced input.
Bit Synchronization	
Bit Error Rate	Within 1 db of theoretical. Maintains synchronization with a 3 percent bit jitter frequency or jitter of ± 25 percent of a bit period at frequencies up to the bit rate with a signal-to-noise ratio of 15 db.

Table 1-2
Condensed Data (Cont.)

Bit Synchronization (Cont.)	
Tracking Range	Follows variations in the bit rate of ±20 percent, with 50 percent transitions at a signal-to-noise ratio of 15 db.
Sensitivity	Bit slippage threshold of 8 db or better. (Bit slippage threshold is defined as the signal-to-noise ratio in an FM receiver IF, normalized to a bandwidth equal to the bit rate, at which the bit synchronizer slips one or more bits in one of 10,000 bit frames on the average.)
Synchronization Mainte- nance of Bit	The system maintains bit synchronization within ±25 percent of a bit period with a signal-to-noise ratio of -4 db and a noise bandwidth equal to the bit rate.
Acquisition Range	The system will lock onto the incoming bit rate at ±10 percent of the predetermined bit rate with 50 percent transitions at a signal-to-noise ratio of 15 db or greater with the noise bandwidth equal to the bit rate.
Clock Outputs	Two-phase clock corresponding to 0 and 180 phase displacement.
Data Output	Regenerated serial NRZ; "Zero" level is 0 volt; and "One" level is -10 volts.
Monitors	Meter provided for input amplitude level, sync status (quality), and fine tuning.
Input Switching	Front panel selector switch for four input sources.
Automatic Mode	Stored program or manual selection of up to eight predetermined bit rates and other associated parameters. Automatic switch-over takes place in approximately 2 milliseconds.
Prime Frame Synchronization	
Prime Channels	512 words per prime frame or greater, depending on format stored in memory.
Sync Word	7 to 33 bits. Can be expanded to 64 bits by the addition of logic modules.
Modes of Operation	Search, check, and lock.
Aperture	Width is programmable for 1 to 3 bits.

# Table 1-2 Condensed Data (Cont.)

<b>新聞的表現的社會是否的特別的表現的地區的基礎的意思的</b>	
Prime Frame Synchronization (Cont.)	
Search Mode	Sync word error bits are programmable for 0 to 15. (Only 8 displayed.)
Check Mode	Sync word error bits are the same as in the lock mode. "Quality Test - Words Sampled" is programmable for 1 to 4. "Quality Test - Allowable Words" in error is programmable for 0 to 2.
Lock Mode	Sync word bits in error are programmable for 0 to 15.
Status Indicators	Search, check, and lock.
Programming	All of the above quality parameters are controlled by programming or may be controlled manually from the front panel controls.
Subframe Recycle Synchronization	
Number	One subframe recycle synchronizer is provided; expansion to three can be made by addition of logic modules.
Subchannels	512 or more, depending on program stored in memory.
Sync Word	7 to 33 bits. Can be expanded to 64 bits by the addition of logic modules.
Modes of Operation	Search and lock.
Search Mode	Sync word bits in error are programmable for 0 to 8.
Lock Mode	Sync word bits in error is 0 to 15.
Status Indicators	Search and lock.
Programming	Each of the quality parameters listed above can be controlled by the memory program or manually for each synchronizer.
Major Cycle ID Synchronization	
Number	One major cycle ID synchronizer is provided.
ID Code Words	Maximum code length is 9 binary bits and is programmable. Can accept MSB or LSB arrangement.

Table 1-2
Condensed Data (Cont.)

Major Cycle ID Synchroniza- tion (Cont.)	
Location	An ID word may appear in any position in either a data word or a sync word.
Status Indication	ID error and ID verified. An ID ON indicator lights when an ID code is included in the format.
Word Synchronization	
Sync Word	Up to three bits programmable.
Modes of Operation	Search, check, and lock.
Aperture	Width is one bit wide and remains constant for all modes.
Search Mode	Sync word bits in error are programmable for 0 or 1.
Check Mode	Sync word bits in error remain the same as in the Search mode. "Quality Test - Words Sampled" is programmable from 0 to 4.
Lock Mode	Sync word bits in error is 0 or 1 bit.
Status Indicators	Search, check, lock, and an ON indicator.
Programming	Each of the parameters listed above can be controlled by program or manually.
Supercommutation	Programming capability is provided to accommodate any number of supercommutated channels at any rate.
<u>Parity</u>	The start of an ODD or EVEN parity count sequence is programmed or manual. A decimal display indicates up to 999 parity errors in 1 to 99 frames. Manual or remote reset capability is provided.
Stored Program Decommutation	
Word Length	Any length up to 64 bits.
Word Rate	Prime or subcommutated word rates up to 200,000 per second can be accommodated by the basic system.
Prime Frame Length	512 or more, depending on arrangement of memory.
TOP TRAINI	NG BURBOSES ONLY

Table 1-2
Condensed Data (Cont.)

HEARING WATER TO THE PARTY OF T	
Stored Program Decommutation (Cont.)	
Subframe Length	Up to four independent subframe ratios can be accommodated with lengths to 512 words or greater. Subframe synchronizers may be set up to provide decommutation for subsubchannels.
Programming	Accepts programs from computers, punched paper tapes, or manually from the system control panel. One memory word is required for each word in the program.
	In operation, only one memory cycle is required for each prime frame or subframe word.
Channel Stripping	Any number of channels may be stripped from the total multiplex by stored program instructions.
Program Selection	Selection of any of the stored programs may be made manually or remotely.
Digital Data Output Capability	
MSB Parallel Binary	8 bits per word; can be expanded to 64 bits by the addition of logic modules.
LSB Parallel Binary	32 bits per word; can be expanded to 64 bits by the addition of logic modules.
BCD Storage	Wired capability of 5 BCD stores of 6 digits each exists by the addition of logic modules.
Binary Storage	Wired expansion capability for 5 binary stores of 33 bits each by the addition of logic modules.
LSB Truncated	4 to 15 bits per character.
MSB Truncated	4 to 15 bits per character.
Miscellaneous	Bits per word numbering: 6 binary bits. Sync status signals for all synchronizers. Word Numbering: 9 binary bits and 11 BCD bits. Readout commands: as required with each system output.
	End of prime frame pulse.
	Data flag to indicate good or bad data.
	Data addresses: 12 binary bits.
	Clock: two-output phases.

Table 1-2 Condensed Data (Cont.)

Digital Data Output Capability (Cont.)	
Serial Digital Data	NRZ-C and NRZ-M.
Output Waveform Characteristics	"One" level is -10 volts; "Zero" level is -0 volt; rise and fall time is less than 100 nanoseconds; and the output impedance is less than 93 ohms.
Data Displays	
Binary	One 32-bit plus word sync code and parity bit indicators provided with thumbwheel channel selector switch, expandable to 64 bits by addition of modules to display unit and LSB parallel binary unit.
BCD	Three 3-digit decimal displays are provided for BCD data with thumbwheel channel selector switches. Expandable to 6 digits by addition of modules to display units and the BCD unit.
Analog Data Output Capability	
Channels	40 digital-to-analog converters with expansion capability to 60 channels by addition of modules.
Voltage	0 to -5 volts.
Output Impedance	1000 ohms.
Resolution	One part in 256.
Linearity	Better than 0.1 percent.
Long Term Stability	Better than 0.1 percent over temperature range from 25 to 50°C.
Direct Access Computer Interface (Data Edit)	
Fixed Upper Limit	Provides capabilities for checking upper limits of measurands and flagging output to computer denoting out-of-limit measurands. Programmable from 0 to 255 in binary increments.
Fixed Lower Limit	Provides capabilities for checking lower limits of measurands and flagging output to computer denoting out-of-limit measurands.  Programmable from 0 to 255 in binary increments.  NG PURPOSES ONLY
PORTRAINII	ALO PLIKPUSES UNIT

Table 1-2
Condensed Data (Cont.)

Direct Access Computer Interface (Data Edit) (Cont.)	
Floating Limit	Provides capabilities for checking last floating point data against measurand and event words and then checking result against a programmed tolerance of 0 to 63. Flags output to computer when out-of-tolerance words are detected.
Transfers to Computer	Provides direct access capabilities to the computer memory for transfer of 13-bit words. Provides computer storage address for word sorting functions.
Interface with Computer	Provides differential input and output termination and logic level conversion that is compatible with computer input and output circuits. Differential voltage of -0.5 to +0.6 volts with drive capabilities for 50 feet of balanced transmission line.
Restrictions	Limits word rate usage to $18  \mu  \text{sec.}$ (Maximum of three memory access cycles.) Prevents loading of programs during use. No parity checks on data edit instructions.

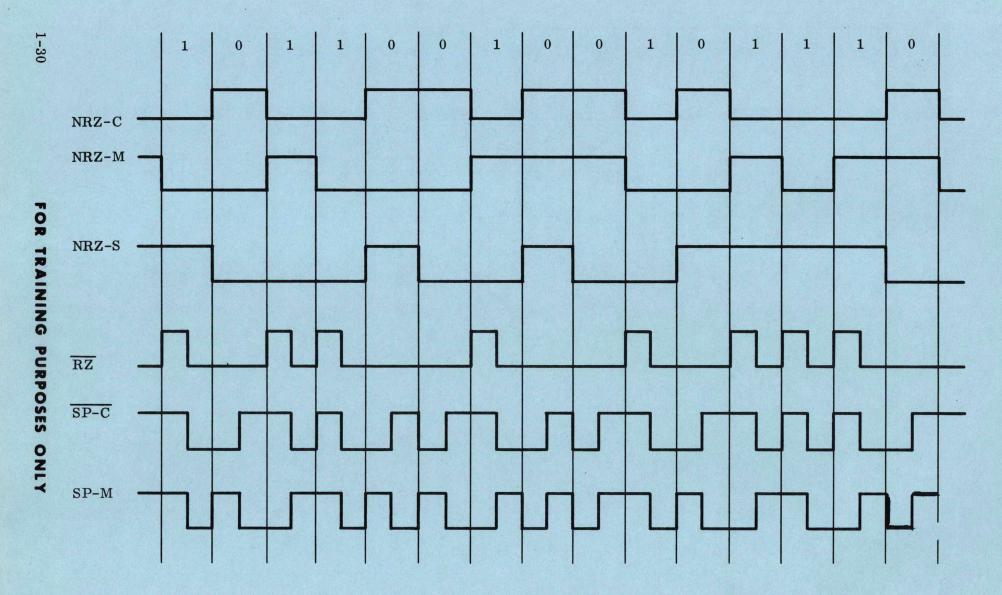


Figure 1-11. Types of PCM Modulation

#### SECTION 2

#### RADIATION LOGIC

#### 2.1 INTRODUCTION

The PCM decommutator is a digital machine, and its logic circuits are composed of rectangular molded modules (see Figure 2-1) and rectangular cards (see Figure 2-2). Only the signal conditioner and PCM simulator contain cards.

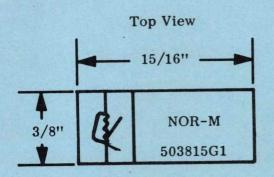
The cards and modules are discussed independently and are concerned with only the logic function of a particular card or module. The schematic of a particular card or module is available and may be examined if so desired. The only basic difference between a module and a card is that modules are set by a positive going pulse and cards by a negative going pulse. The logic function of both, along with the logic symbol are identical. Radiation represents a logic "one" by a  $-10^{V}$  level and a logic "zero" by a  $0^{V}$  level.

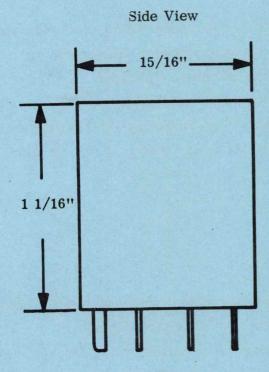
#### 2.2 MODULES

#### 2.2.1 GENERAL

The rectangular molded modules that form most of the logic circuits in the Series 540 PCM Decommutator are mounted in a connector panel, 50 modules per panel. The physical dimensions of the panel are 4 inches by 6 3/4 inches. Four of these panels are mounted vertically on a 7 1/4 inch by 17 inch casting. Five castings vertically mounted, side on side, make up a logic slide-out panel. There are 5 logic slide panels in racks 3 and 4.

The connector panels are designated by a lettering system (see Figure 2-3). Starting at top left corner of a logic slide-out panel, the first connector panel is panel "A," the second "B," the third "C" and the fourth "D." The next casting will contain connector panels "E" through "H." Casting 3 connector panels are "K," "L," "M," and "N." Casting 4 has "R," "S," "T," "U," and casting 5 contains "W," "X," "Y," and "Z."





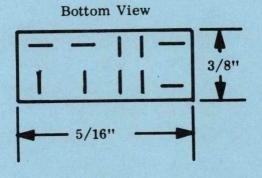


Figure 2-1. Molded Modules
FOR TRAINING PURPOSES ONLY

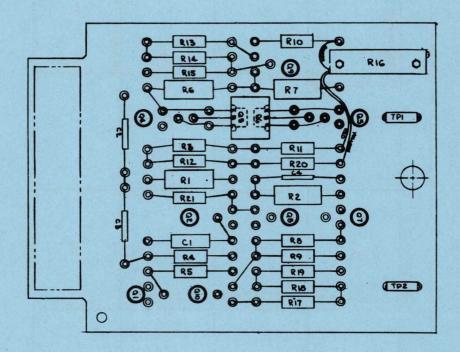


Figure 2-2. Rectangular Card
FOR TRAINING PURPOSES ONLY

# eat. 1 A2/ A/1A # Bandre

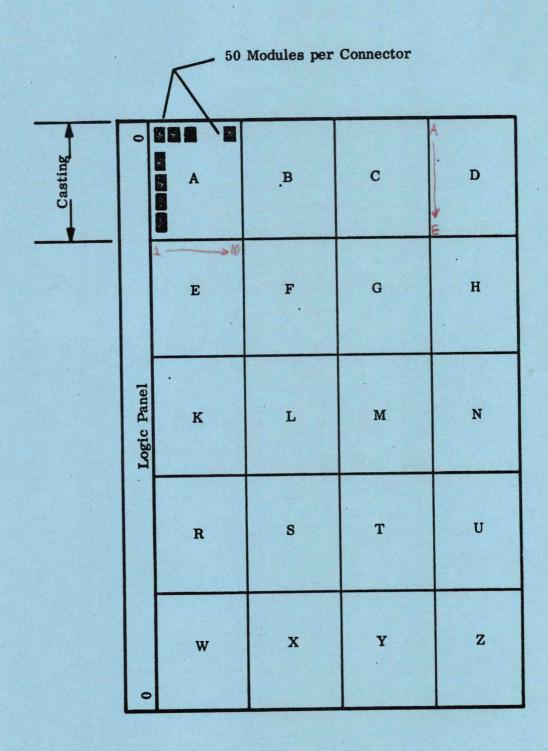


Figure 2-3. Connector Panel Representation

A single connector panel identifies each individual module by a letter-number code. The horizontal row containing 10 modules is numbered 1 through 10 (see Figure 2-4) and the vertical row is lettered "A," "B," "C," "D," and "E." The individual modules are also color coded, and any module fits any connector. They are keyed in that they can be inserted only one way, but an AND module could be inserted into a location occupied by a power inverter and vice versa.

The individual components are welded to flat contact pins. Contact pins are then inserted into slots in plastic blocks; individual connections are made by welding and trimming off the excess wire. Components not going to contact pins are welded as a final step in assembly. The component assembly is transfer molded in filled epoxy. The plastic block is then pulled off, leaving the contact pin exposed. Figure 2-5 shows the steps just described.

#### 2.2.2 LOGIC MODULES

#### 2.2.2.1 NOR Gates

# 1 A 3 B 4 C 5 D

Note

Logic Symbol

The numbers in the drawing are the input and output pins. The gate can be used as a two-input NOR gate. The letters are the input and output signal.

#### 2.2.2.1.1 Explanation

The NOR module performs the OR-NOT function for negative-true inputs and the AND-NOT for positive-true inputs as indicated below:

- a. OR-NOT
  - (1) Input

$$A + B + C + D$$

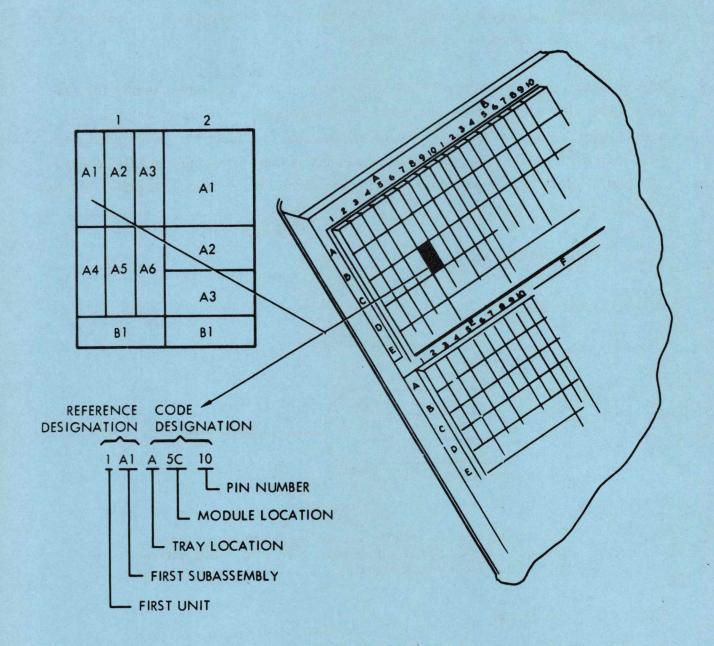


Figure 2-4. Reference/Code Designation

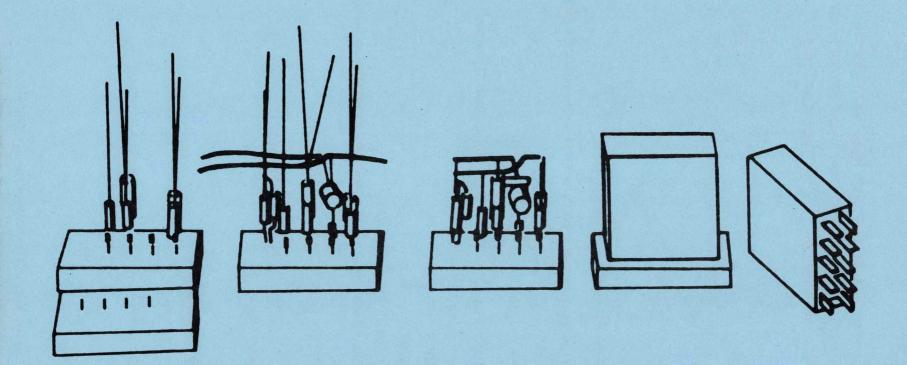


Figure 2-5. Typical Module at Successive Stages of Construction

(2) Output

If one of the four inputs is a logic "one," the output will be a logic "zero." The waveshapes below are the inputs if "A" is a logic "one" and "B," "C," "D" are logic "zeros."

With these inputs, the output "F" will appear as follows:

At time input "A" goes false (logic "one"), output "F" goes to  $0^{\frac{V}{2}}$  (logic "zero").

b. AND-NOT

- (1) Input  $\overline{A}$  .  $\overline{B}$  .  $\overline{C}$  .  $\overline{D}$
- (2) Output F

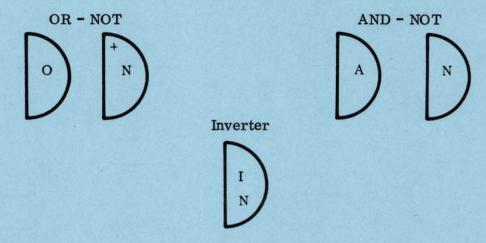
The waveshapes of these inputs will appear as follows:

$$\begin{array}{ccccc}
\hline{A} & -10^{\underline{Y}} & \\
\hline{B} & -10^{\underline{Y}} & \\
\hline{C} & -10^{\underline{Y}} & \\
\hline{C} & -10^{\underline{Y}} & \\
\hline{D} & -10^{\underline{Y}} & \\
\hline
\end{array}$$

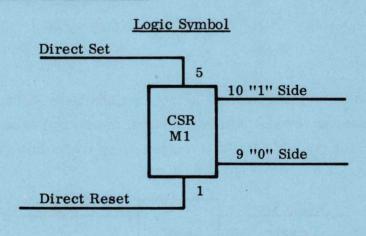
If all the inputs are NOT signals (logic "zeros"), the output "F" will be a true signal (logic "one") and appear as follows:

#### 2.2.2.1.2 Summary

The NOR gate is used for both the OR-NOT and AND-NOT function in the PCM decommutator logic. In addition, it is used as an inverter-single input, since the output, as in the AND-NOT function, is the reverse of the input signals. The circuit is the same; only the logic function changes. The logic symbol may also change, as noted below.



#### 2.2.2.2 Counter Shift Register (CSR)



A CSR is a flip-flop that is used in two basic circuits in the decommutator logic. The name CSR is derived from the function it performs—a binary counter or a shift register.

Note

## 2.2.2.1 Explanation

The output levels may be switched by either the direct set or direct reset inputs. The relationship between the direct set and the reset inputs is shown in the truth table below:

Input		Outp	ut
Direct Set_	Direct <u>Reset</u>	<u>"1" Side</u>	<u>"0" Side</u>
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	Undefined	Undefined

The waveshapes for this operation are as follows:

Direct Set	Direct Reset	<u>"1" Side</u>	"0" Side
0 <u>v</u> ——		No Change	No Change
-10 <u>\tilde{V}</u>			
0 <u>v</u>			7
-10 <u>V</u>			
$0_{\overline{\Lambda}}$		7	
-10 <sup><u>v</u></sup>			
0₫		Undefined	Undefined
-10 <sup><u>v</u></sup>			

If a trigger is used in conjunction with the logic set and logic reset inputs, the output of either the "1" side or "0" side will remain until the arrival of another trigger pulse. The logic symbols for the M1CSR with a trigger pulse are as follows:

	10 "1" Side
CSR	
M 1	
,	9 "0" Side

A truth table for its operation is as follows:

Logic Set	Logic Reset	Trigger	<u>"1" Side</u>	"0" Side
0	0	0	No Change	No Change
1	0	1	1	0
0	1	1	0 .	1
0	0	1	Undefined	Undefined
1	1	1	No Change	No Change

Note

A "0" is equal to  $0^{\frac{V}{4}}$  and a "1" is equal to  $-10^{\frac{V}{4}}$ .

The waveshapes for the operation as listed in the truth table are shown in Figure 2-6.

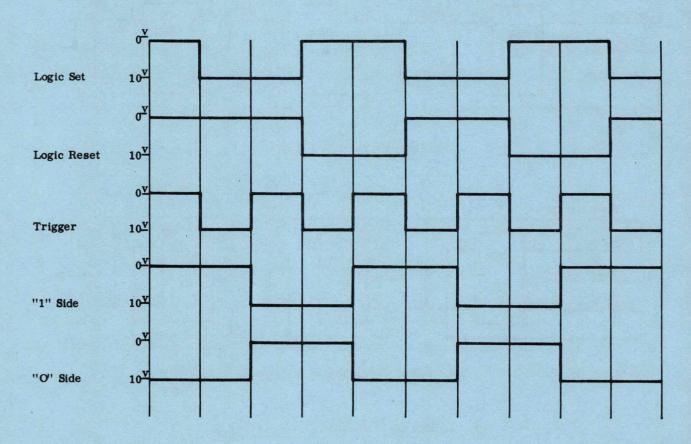


Figure 2-6. CSR Waveshapes

In this example, the CSR is presumed to be in the reset state before the arrival of the first logic set pulse. The trigger pulse does not effect a change in the CSR until it goes positive. At this time the logic set, or reset, depending upon which has a logic "1" on line, will be clocked through the CSR, and either the "1" side or the "0" side will change state.

#### 2.2.2.1.1 CSR Counters

A CSR counter can be either an up counter or a down counter. The direction it counts is dependent upon how it is wired externally. (See Figures 2-7 and 2-8)

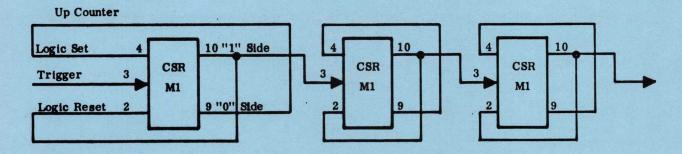


Figure 2-7. CSR Up Counter

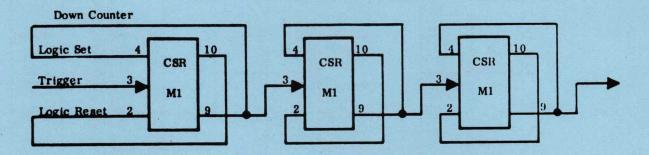


Figure 2-8. CSR Down Counter

#### 2.2.2.1.2 CSR Shift Register

The shift register uses a CSR with the logic set/reset and trigger pulses as its inputs. The input is shifted from the first CSR to the second CSR at the rate that the trigger pulse occurs. See Figure 2-9.

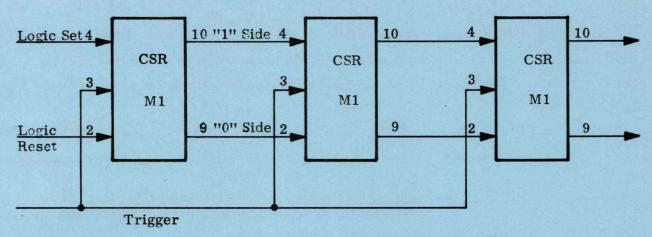


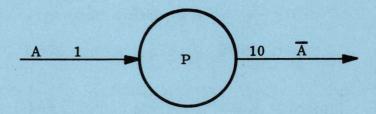
Figure 2-9. CSR Shift Register

#### 2.2.2.2 Summary

The CSR may use the direct/indirect set or logic set/reset combined with a trigger pulse to change states. The particular method used will depend upon the logic circuit itself. A trigger pulse will not effect a change until its positive-going edge is felt by the CSR module.

#### a. Power Inverter

(1) Logic Symbol

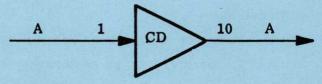


#### (2) Explanation

Power inverter modules perform a logic inversion and are capable of driving ten CSR or NOR modules and three complementary drivers.

#### b. Complementary Driver

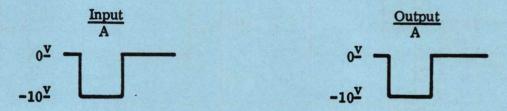
#### (1) Logic Symbol



#### (2) Explanation

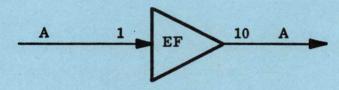
The complementary driver is a complementary emitter-follower and performs no logic function. The complementary driver has

the capability of driving the trigger pulse to 40 CSR. It is capable of driving 50 dc loads. A complementary driver may be driven by an unloaded NOR or a differentiator.



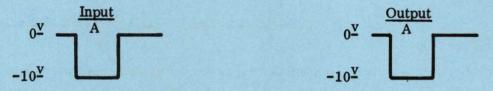
#### c. Emitter-Follower

#### (1) Logic Symbol



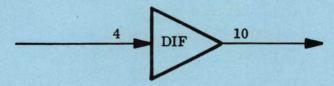
#### (2) Explanation

The emitter-follower module is noninverting and performs no logic function. It is capable of driving 10 dc loads. A CSR or an unloaded NOR may drive an emitter follower. A power inverter may drive two emitter-followers.



#### d. Differentiator (DIFF)

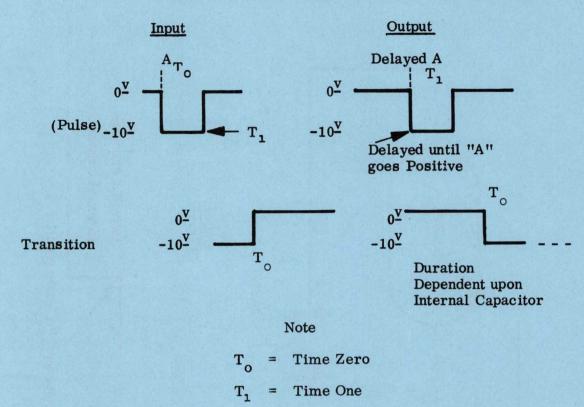
#### (1) Logic Symbol



#### (2) Explanation

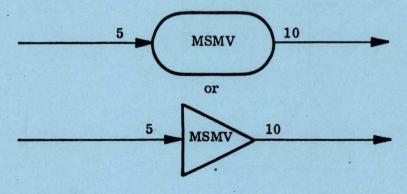
The differentiator module may be used to obtain a negative pulse in applications where the pulse duration is not critical and relatively long rise and fall times can be tolerated. A positive transsistion is required to trigger a DIFF. However, if the DIFF is triggered by a pulse, the output pulse can never exceed the duration of the input pulse. If the trigger is not a pulse but only a

positive transition signal, the output duration will depend upon the differentiating capacitor at the input of pin 4. The DIFF can drive four dc loads and may be driven by all circuits.



#### e. Monostable Multivibrator (MSMV)

#### (1) Logic Symbol



#### (2) Explanation

The MSMV circuit consists of two modules (see Figure 2-10). One is designated MSMV and the other DIFF. In addition to the two modules, an external timing capacitor is required. The output of the complete circuit is a negative pulse occurring when a positive transition is applied to the input and having a duration

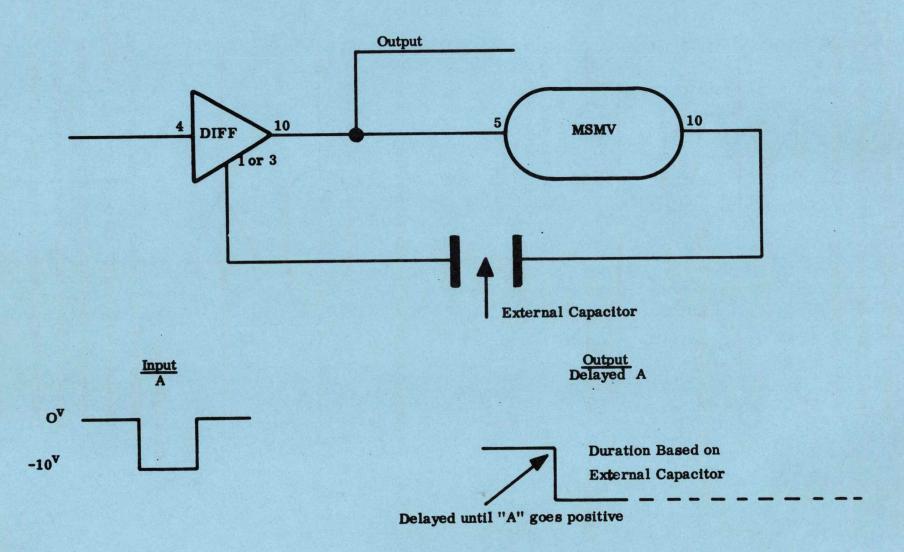
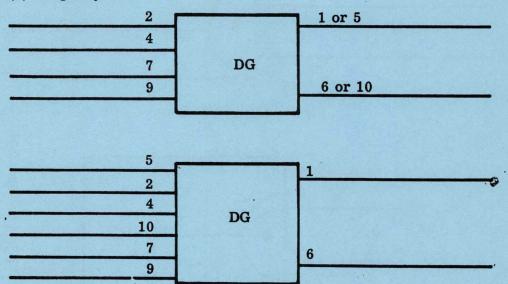


Figure 2-10. Complete MSMV Circuit

determined by the value of the external capacitor. Output pulses from 1.5 microsecond to 50 microseconds can be obtained. The MSMV can drive three dc loads, a single DIFF, or another MSMV.

#### f. Diode Gate

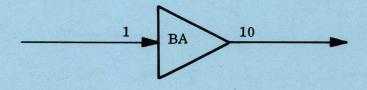
#### (1) Logic Symbol



#### (2) Explanation

The diode gate is a combination of several logic functions, dependent upon the circuit it is used in. The input can be two 2-input AND gates with the outputs OR, either together or used as independent outputs. The module can be used as two 3-input AND gates or a single 6-input AND gate. If used as a two 3-input AND gate circuit, the output can be used independently or their outputs tied together to form the 6-input AND gate. These changes in the gate function are accomplished by external jumpers. From a logic functional standpoint, the gates appear as shown in Figures 2-11 through 2-14.

- g. Latching Module (L-2)
- h. Indicator Driver (ID-6)
- i. Buffer Amplifier
  - (1) Logic Symbol



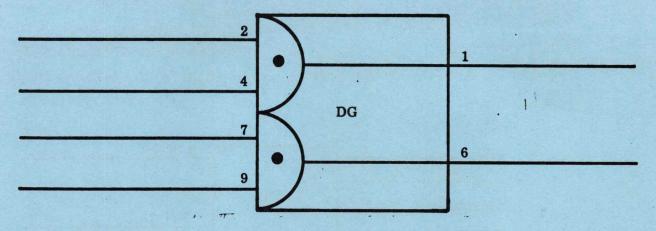


Figure 2-11. Two 2-Input AND Gates

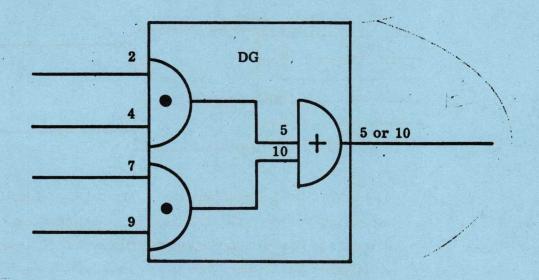


Figure 2-12. Two 2-Input AND with an OR Gate

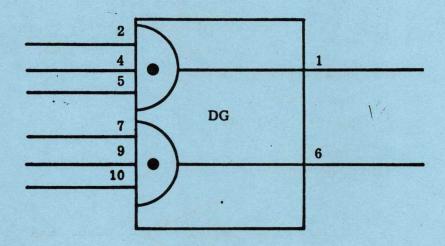


Figure 2-13. Two 3-Input AND Gates

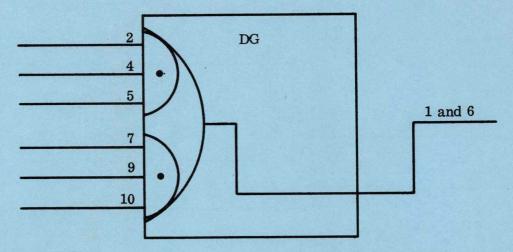


Figure 2-14. Two 3-Input AND Gates Functioning as One 6-Input AND Gate

## (2) Explanation

The buffer amplifier is essentially a complementary emitterfollower with a low output impedance that performs no logic function.

#### 2.3 CARDS

All of the module circuits used in the decommutator are also found on card circuits. Cards and their logic are identical in function and symbol. The pin numbers are not the same since more than one circuit may be found on a particular card. Figure 2-15 shows the mounting procedures for the cards in the decommutator.

#### 2.4 DIAGRAMS

Diagrams of the CSRM module, low and medium speed NOR, NOR switching characteristics, CSR M1 module, and diode gate module are shown in Figures 2-16 through 2-20.

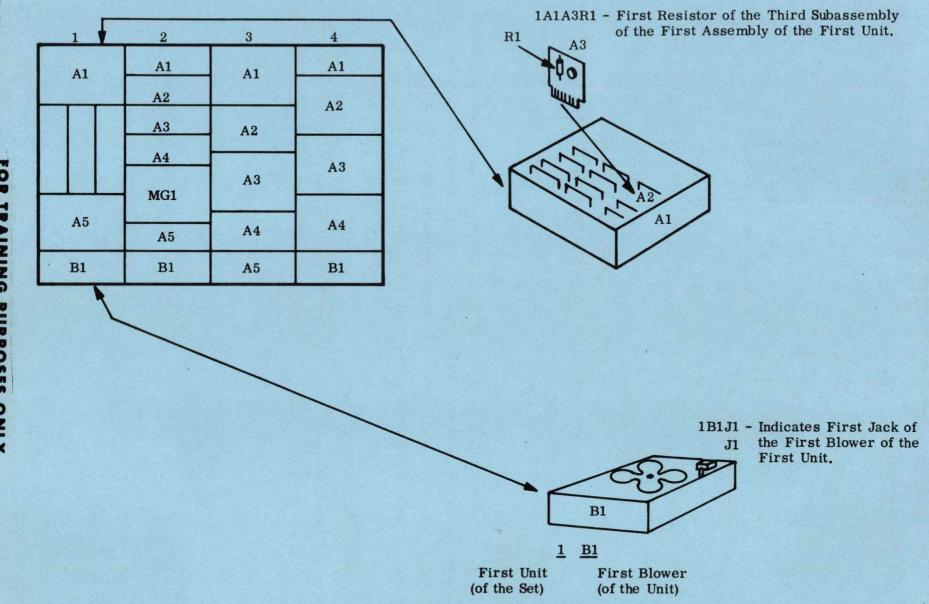


Figure 2-15. Reference Designation Assignment

Figure 2-16. Schematic and Assembly of CSRM Module

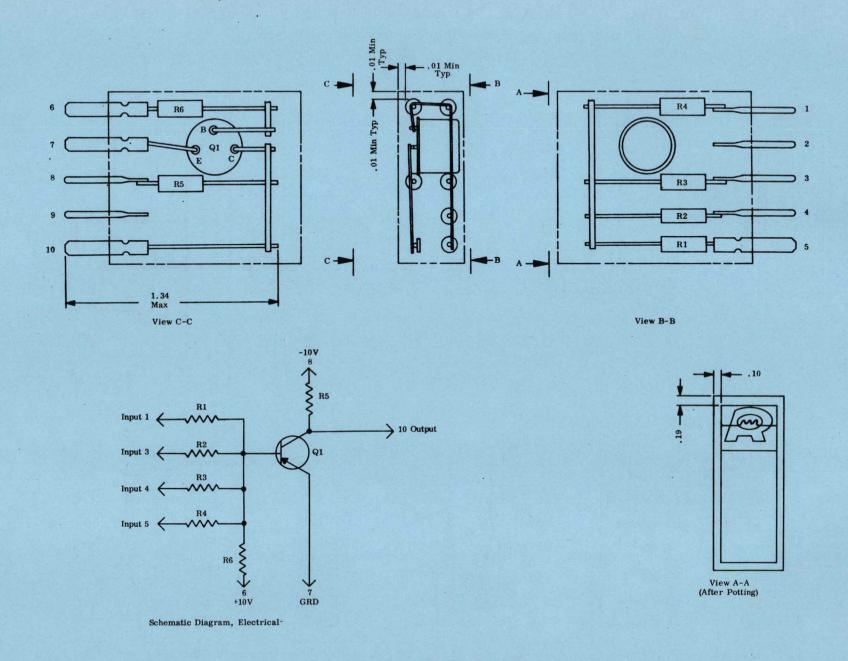


Figure 2-17. Schematic and Assembly of Low and Medium Speed NOR

		Low Speed	Medium Speed	
Rise Time (t <sub>r</sub> )	TAVE	0.289	0.068	μs
	S	0.033	0.003	μs
	TAVE + 3S	0.388	0.077	μs
- 11 - 4 3				
Fall Time (t <sub>f</sub> )	TAVE	0.353	0.058	μs
	S	0.033	0.004	μs
	T <sub>AVE</sub> + 3S	0.452	0.074	μs
Storage Time (t )	Т			
Storage Time (t <sub>s</sub> )	TAVE	0.331	0.030	μs
	S	0.043	0.001	μs
	TAVE + 3S	0.460	0.033	μs
-1 - 4	_			
Delay Time (t <sub>d</sub> )	TAVE	0.108	0.039	μs
	S	0.009	0.001	μs
	TAVE + 3S	0.126	0.042	μs

# Test Conditions (after encapsulation)

Power	Nominal
Load	Worst Case
Temperature	
Sample Size	

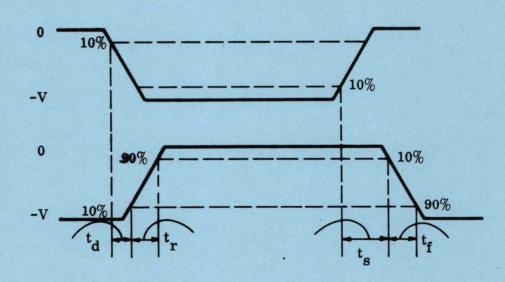


Figure 2-18. Low and Medium Speed NOR Switching Characteristics

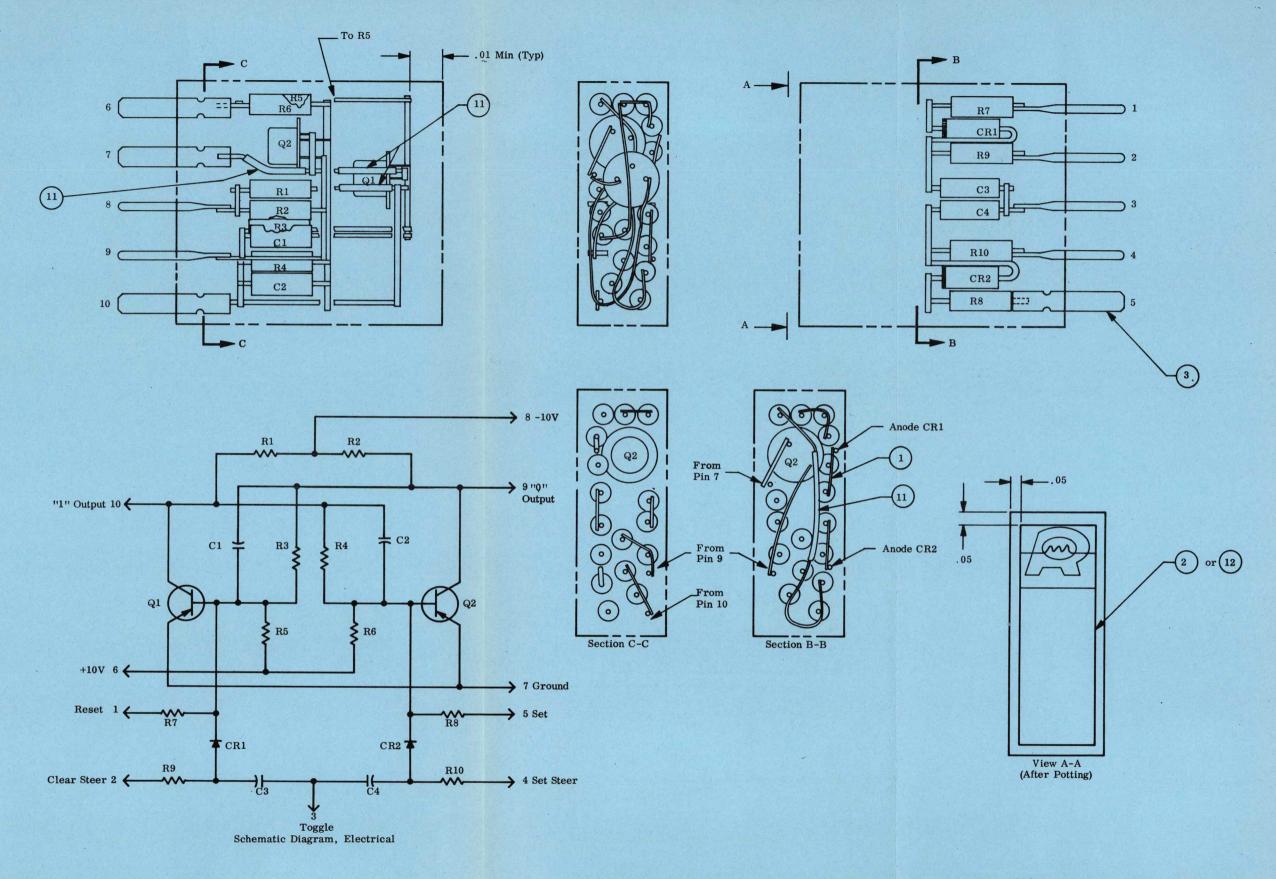


Figure 2-19. Schematic and Assembly of CSR M1 Module - 506030

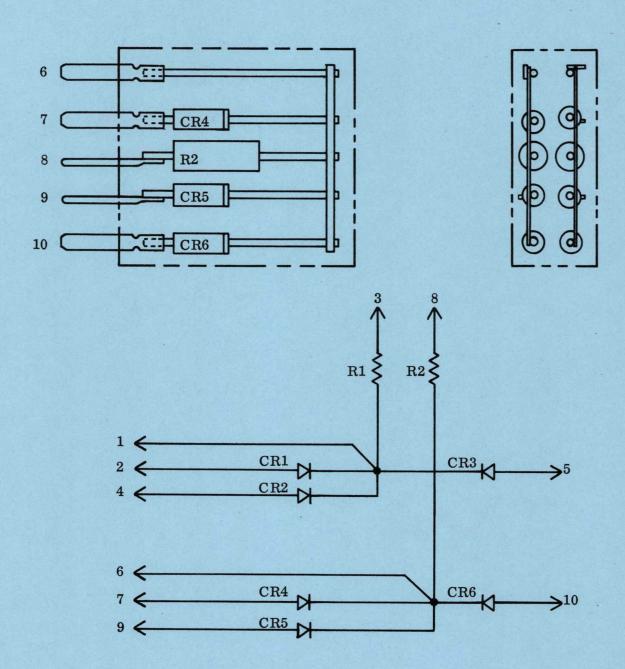


Figure 2-20. Schematic of Diode Gate Module

#### SECTION 3

#### PCM SIGNAL CONDITIONER

#### 3.1 DESCRIPTION

The controls and indicators for PCM signal conditioner 1A2 (commonly called the bit synchronizer) are shown in Figure 3-1. Table 3-1 lists the controls and indicators and their functions. The associated logic prints consist of pages 6-34 through 6-43 of the logic diagram book.

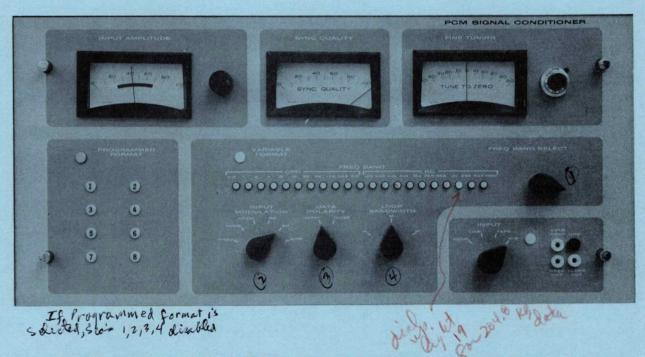


Figure 3-1. PCM Signal Conditioner 1A2 Front Panel

The serial PCM input is connected to the amplifier and dc level restorer circuits which provide the gain necessary for the remainder of the system (Figure 3-2). The level-restored signal is connected to the bit synchronizer subsystem and the bit detector subsystem. The bit synchronization subsystem utilizes a voltage-controlled oscillator (VCO) operating at a frequency directly dependent on the input bit rate. The VCO output is counted down in the binary counter chain of the frequency divider to develop the bit rate clock. The output of the frequency divider is connected to the timing generator circuits which provide the correct timing signals for the system. The bit detector and the decoder and correct phase detector circuits accept the video signal and clock signal,

Table 3-1
Bit Synchronizer Controls and Indicators

Control/Indicator	Function
INPUT AMPLITUDE meter	Displays the amplitude of the data at the output of the input amplifier.
INPUT AMPLITUDE control	Adjusts the amplitude of the PCM signal as required.
SYNC QUALITY meter	Displays whether the synchronizer is in or out of lock.
FINE TUNING meter	Aid in adjustment of the correct bit frequency.
Fine Tuning control	Fine adjustment of the correct bit frequency.
FREQ BAND SELECT control	Coarse selection of the desired frequency.
Input/Output Test Points	Jacks for observing input and output signals.
DATA IN NRZC OUT CLOCK OUT GRD	
INPUT selector switch	
RCVR (receiver) LINE TAPE SIM (simulator)	Selects input from receiver. Selects input from video line. Selects input from tape recorder. Selects input from PCM signal simulator.
Simulator Indicator	Indicates that the PCM signal simulator input is selected.
LOOP BANDWIDTH selector switch N (narrow) M (medium) W (wide)	Selects bandwidth of phase lock loop for variable format. Narrow position is normally used; medium and wide positions are for input signals with considerable bit rate jitter.

Table 3-1
Bit Synchronizer Controls and Indicators (Cont.)

Control/Indicator	Function
DATA POLARITY selector switch NORM (normal) INVER (inverted)	Selects polarity of incoming signal for variable format.
INPUT MODULATION selector switch	Selects type of input modulation for the variable format.
NRZC	Selects non-return-to-zero change (NRZC) input modulation.
NRZS	Selects non-return-to-zero shift (NRZS) input modulation.
NRZM	Selects non-return-to-zero mark (NRZM) input modulation.
RZ	Selects return-to-zero (RZ) input modu- lation.
SP	Selects split-phase (SP) input modulation.
SPM	Selects split-phase mark (SPM) input modulation.
VARIABLE FORMAT indicator	Indicates that variable format has been selected.
FREQ BAND indicators	Displays frequency band selected in variable format.
PROGRAMMED FORMAT indicators	
Yellow	Denotes a programmed format is being used.
1, 2, 3, 4, 5, 6, 7 and 8	Denotes which programmed format is being used.

perform a polarity decision each bit time, and supply a reconstructed NRZ-C waveform as the data output.

The signal conditioner consists of three principal subsystems (Figure 3-2):

- a. A dc restorer.
- b. A bit synchronizer (or phase lock loop).
- c. A bit detector.

The dc restorer accepts the serial data train as an input and supplies a level-restored signal to the bit synchronizer and bit detector. The bit synchronizer outputs are a clock at the bit rate of the data and timing signals for the system. The bit detector accepts the clock timing signals from the bit synchronizer and the data train from the dc restorer. It then produces reconstructed serial digital data as an output. Thus, the bit detector performs the basic decision of whether a binary one or zero exists for each bit.

For RZ and NRZ data, the clock from the bit synchronizer defines the bit period, and the decision is based on the polarity of the signal during this period. For bit decisions of RZ and NRZ data, a pulse integrating detector is used.

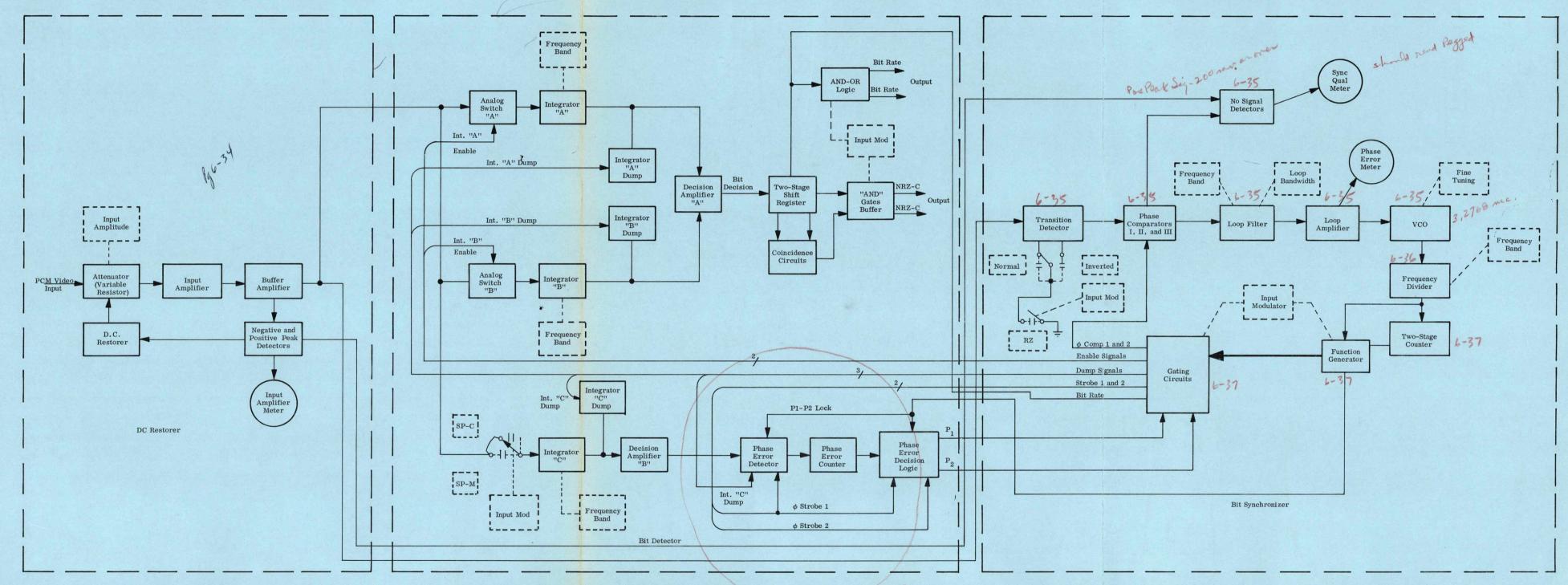
For split-phase data, the clock defines only the carrier frequency; the bit location is subject to an ambiquity. The bit detector resolves this ambiquity, locating the bit position and making the bit polarity decision. For bit decisions of split-phase data, a full-wave integrate and dump circuit is used. The phase decision is made on the basis of several bits to reduce the probability of an error resulting from noise.

Decommutation of the incoming PCM data can be performed only if the decommutator timing is synchronized with the bit rates of the incoming data. Therefore, data words can be identified and routed properly by virtue of their time slot within a serial train of commutated data.

Since the series 540 decommutator can accept six different PCM codes, the appropriate circuitry must be selected within the bit synchronizer, via the front panel modulation switch, which corresponds to the input PCM code. Also, incorporated in the system is a programming unit that is prewired for standard frequencies and code types used. This unit, through relay action, automatically establishes all the parameters necessary for the incoming formats, such as frequency, data type, and data polarity (Table 3-2).

Bit Detector

Bit Synchronizer



used only in SPM in Phones in 180° and
SP-e on SPM in Phones in 180° and

Figure 3-2. PCM Signal Conditioner

The program selected is indicated by the appropriate PROGRAMMED FORMAT light on the front panel. When programmed format is being used, the following switches are disabled: Frequency Band Select, Input Modulation, Data Polarity, and Loop Bandwidth.

Table 3-2
Parameters for Incoming Formats

Program	Frequency (kc)	Data Type	Data Polarity	
1	1.6	NRZC	Inverted	
2	5.12	SP	Inverted	
3	28.8	NRZC	Inverted	
4	51.2	SP	Inverted	
5	51.2	NRZC	Inverted	
6	102.4	SP	Inverted	
7	112.64	NRZC	Inverted	
8	204.8	SP	Inverted	

#### Note

All fixed programs employ narrow bandwidths. These programs are applicable for the program select cards as provided. If programs are modified, card parameters will be changed.

The input signal to the decommutator, when used in the ACE-S/C capacity, is split-phase-C PCM data. After determination of whether the incoming bits are "ones" or "zeros," the serial data train is converted to NRZ-C and NRZ-M modulation. Independent of the incoming PCM code format, the output of the signal conditioner is always NRZ-C and NRZ-M format. The NRZ-C serial data train is sent to the group synchronizer, where prime frame synchronization is established. The NRZ-C and NRZ-M data trains are also made available on output jacks for recording on magnetic tape recorders. This data is transferred to the recorders via the video distribution and tape transport control unit and recorded simultaneously with the PCM raw data.

### 3.2 DC RESTORER

A simplified block diagram of the dc restorer is shown in Figure 3-3. The data is connected to the input attenuator, a front panel control which is adjusted to provide proper system operation over the input voltage range of 0.5 to 30 volts, peak-to-peak.

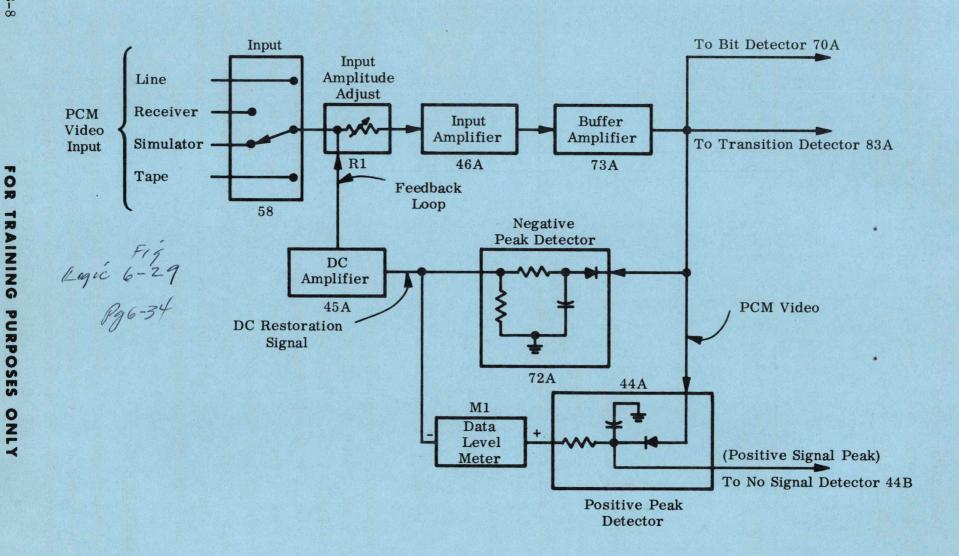


Figure 3-3. DC Restorer, Simplified Block Diagram

The attenuator output is connected to the input amplifier, which provides the gain necessary to develop a standardized signal amplitude for the remainder of the system. The video signal is applied through the buffer amplifier to the positive and negative peak detectors. The outputs of the peak detectors are mixed to provide a signal proportional to the difference in positive and negative peak values. The mixed signal is amplified by the dc amplifier and added to the data waveform at the input attenuator. This forms a feedback loop that is phased to force the summed output of the peak detectors toward zero. The result is equal amplitude positive and negative signal peaks; thus the video signal is level-shifted to form a symmetrical signal about ground.

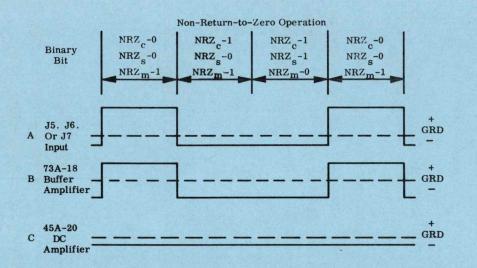
The logic diagram for the dc restorer is shown in the upper half of Figure 6-29 of the logic prints. The serial PCM input signal (waveform A, Figure 3-4) is applied through J5, J6, or J7 to the input attenuator R1 (Figure 6-29 logic print), a 10-kilohm variable resistor. The input attenuator is a front panel control which is adjusted to provide proper system operation over the input voltage range of 0.5 to 30 volts, peak-to-peak. The attenuated signal is connected to differential amplifier 46A, whose output is applied to buffer amplifier 73A. A large current load is handled by the buffer amplifier since its output (waveform B, Figure 3-4) is supplied to six circuits: (1) positive peak detector, (2) negative peak detector, (3) transition detector, (4) analog switch A, (5) analog switch B, and (6) integrator C.

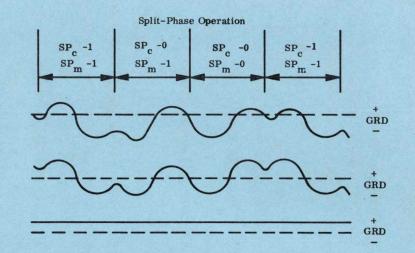
The positive and negative peak detectors supply a dc voltage level that is proportional to the difference in positive and negative peak values. A summing network for both detectors is contained on negative peak detector 72A. The output of the summing network is connected to dc amplifier 45A. Positive peak detector 44A also contains the no-signal detector. The input amplitude meter on the front panel is also connected to the positive peak detector. This meter indicates relative signal amplitude.

The dc amplifier input is applied to a differential amplifier. The output is applied to the input attenuator (waveform C, Figure 3-4). This forms a feedback loop that is phased to force the summed output of the peak detectors toward zero. The video signal is thus level shifted until it is symmetrical about ground.

## 3.3 BIT SYNCHRONIZER

A simplified block diagram of the bit synchronizer is shown in Figure 3-5. The level-restored signal is connected to the transition detector circuit, which generates a standardized pulse for each data transition. However, during RZ data reception relay





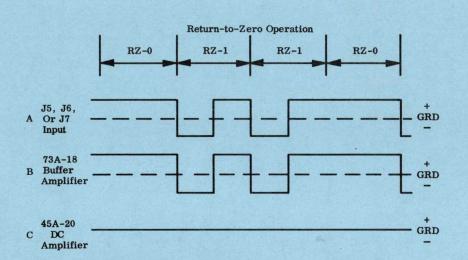


Figure 3-4. DC Restorer, Timing Diagram

Figure 3-5. Bit Synchronizer (Sheet 1 of 3)

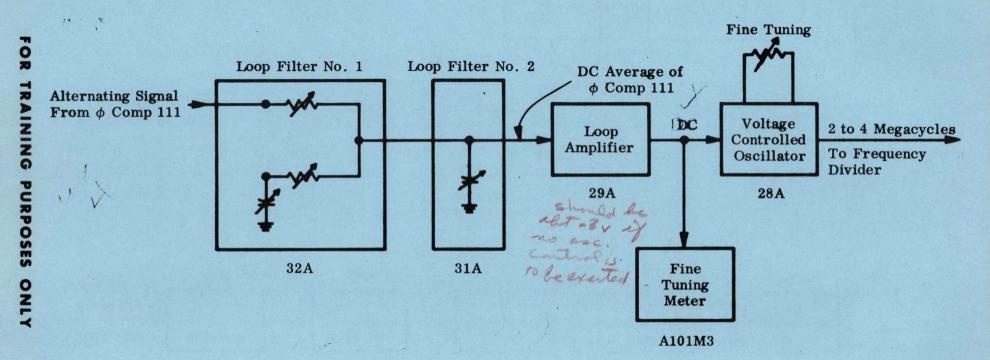
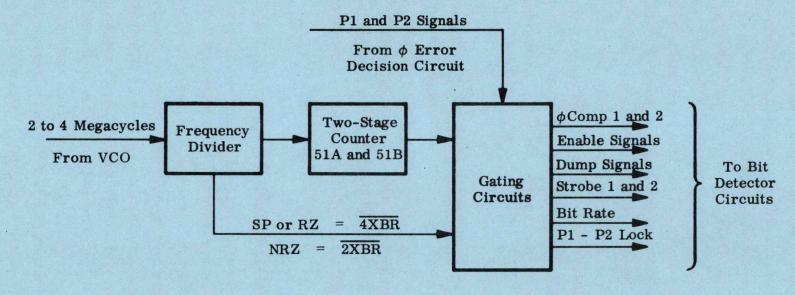


Figure 3-5. Bit Synchronizer (Sheet 2 of 3)

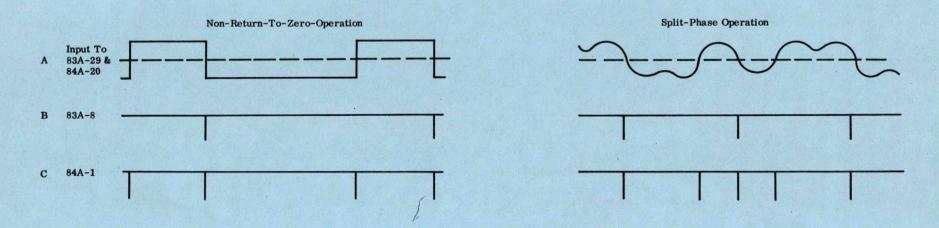


action or the INPUT MOD and POLARITY, switches connect the circuits such that transition pulses for one polarity of transition are inhibited. The transition pulses form the input to the bit synchronizer which generates the bit rate clock. The transition and the local clock pulses are applied to the phase comparators, which produce an output voltage proportional to the phase difference between the two signals. The phase error signal is passed through the loop filter, a lag-lead network controlled by relays, or from the front panel by the FREQ BAND and LOOP BANDWIDTH switches. The filtered phase error signal is amplified by the loop amplifier and is used to control the frequency of the VCO. The VCO output of 2 to 4 megacycles is counted down by the binary counter chain in the frequency divider to provide an inverted output of twice the bit rate for NRZ inputs or four times the bit rate for RZ and split-phase inputs. The output of the frequency divider is connected to a two-stage counter and to the function and gating circuits. The outputs from the function and gating circuits provide the refence signal to the phase comparator and the control and timing signals necessary to operate the bit detector.

The positive peak detector also supplies the signal to the front panel input amplitude meter. An output from the phase comparator and positive peak detector is used to operate the no-signal detectors. The output of these circuits is connected to the sync quality meter on the front panel. An output from the loop amplifier is used to indicate phase error on the front panel fine tuning meter. Fine tuning of the VCO is provided by the variable resistor control on the front panel. The logic diagram for the bit synchronizer is shown in Figure 6-30.

## 3.4 TRANSITION DETECTOR CIRCUITS

The transition detector timing diagram is shown in Figure 3-6. One output from the buffer amplifier is connected to negative transition detector 83A (figure 6-30). This signal (waveform A, Figure 3-6) is applied to the negative slicer circuit on the same card and to the positive slicer circuit on positive transition detector 84A. The inverted output of the negative slicer is amplified and applied to a differentiating network. The differentiator output is coupled to a diode rectifier, which passes only the negative pulses (waveform B). The output of the positive slicer is also applied to a differentiating network and a diode rectifier. The output of this rectifier is then combined with the output of the negative transition detector and coupled through a buffer amplifier to provide the data transition signal (waveform C) for the phase comparators. During RZ operation, relay action or the INPUT MOD switch applies a ground potential to the POLARITY switch common point. In turn, it applies the ground potential to either the



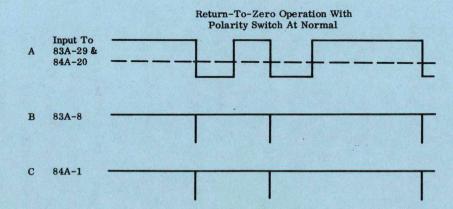


Figure 3-6. Transition Detector, Timing Diagram

positive or negative transition detector, inhibiting the output of the selected detector. Thus, the transition detectors provide an RZ output for either positive-going signal transitions or negative-going signal transitions, but not for both transitions.

## 3.5 PHASE COMPARATOR, LOOP AMPLIFIER, AND VCO CIRCUITS

The phase comparators consist of two bistable multivibrators connected in special circuits and a resistive mixing network (Figure 3-7). The first bistable (Phase Comp. 1, 59A) is set by the incoming data transitions (waveform A, Figure 3-8A) and reset by either phase of the clock (waveforms B and C). The resets at the negative-going edge of either phase of the clock pulses are obtained by coupling differentiator outputs through a diode OR pair to the reset terminals of the bistable. Thus the data transitions that occur during the first half of the clock pulse period generate a positive pulse on the -6-volt baseline of phase comparator 1 (waveform D). When a data transition occurs simultaneously with the negative going edge of either clock, as in the case of in-phase operation, the data transition will take priority at BSMV 59A. The reset signal for BSMV 58A consists of  $\overline{\phi}$  COMP 1 ANDed with CLOCK. This AND gate is true only when coincident negative pulses are present at the inputs.\* BSMV 58A is set by the CLOCK pulse. The purpose of phase comparator 2 (58A) is to provide the negative signal necessary to develop a phase error signal of the correct sense, when added to phase comparator 1. After BSMV 58A is reset by the AND gate, it is set one-half period later by the clock pulse, resulting in the generation of the required correction signal (waveform F). The signals from the two bistables are inverted and resistively added in phase comparator 3 (30A) to produce an average value of zero to the VCO for a zero phase error (waveform G). Circuit operations with a leading clock are shown in Figure 3-8B; operations with a lagging clock are shown in Figure 3-8€.

The summed output of phase comparator 3 is connected to loop filters 32A and 31A. The loop filter is a lag-lead type RC network with the capacitance controlled by relay closure or the FREQ BAND switch and the resistance controlled by relays or the LOOP BANDWIDTH switch. The loop filter output is connected to loop amplifier 29A, which provides the voltage gain required for the bit synchronizer. The output is coupled directly to the VCO (28A). The output of the loop amplifier is also connected to the phase error or FINE TUNING meter on the control panel. This meter provides a visual indication of the VCO input voltage or effectively, the amplitude of the phase error signal.

\*NOTE: Pin 23 must be negative prior to clock.

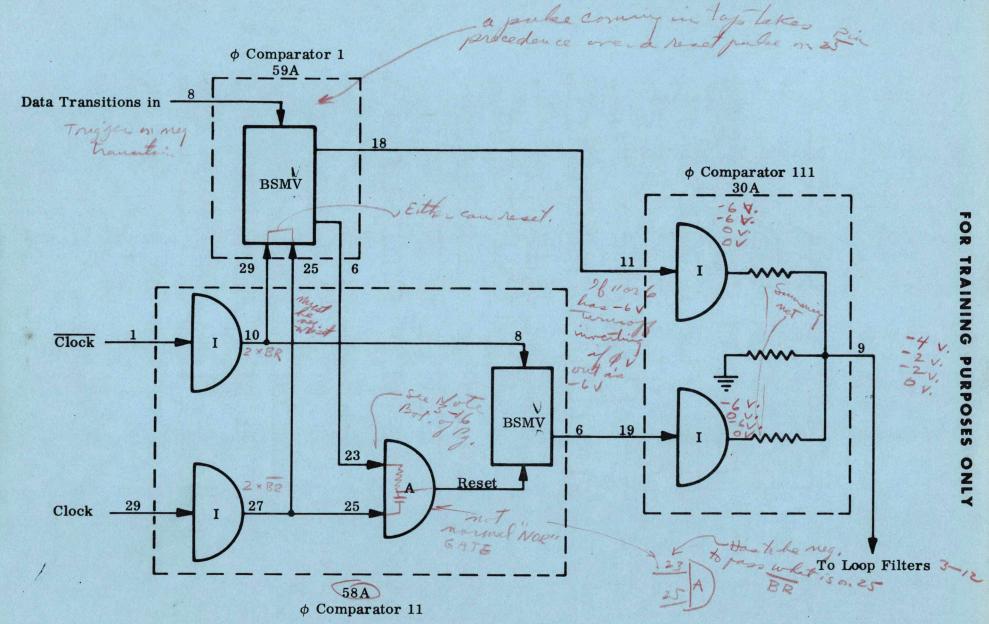


Figure 3-7. Phase Comparator Logic

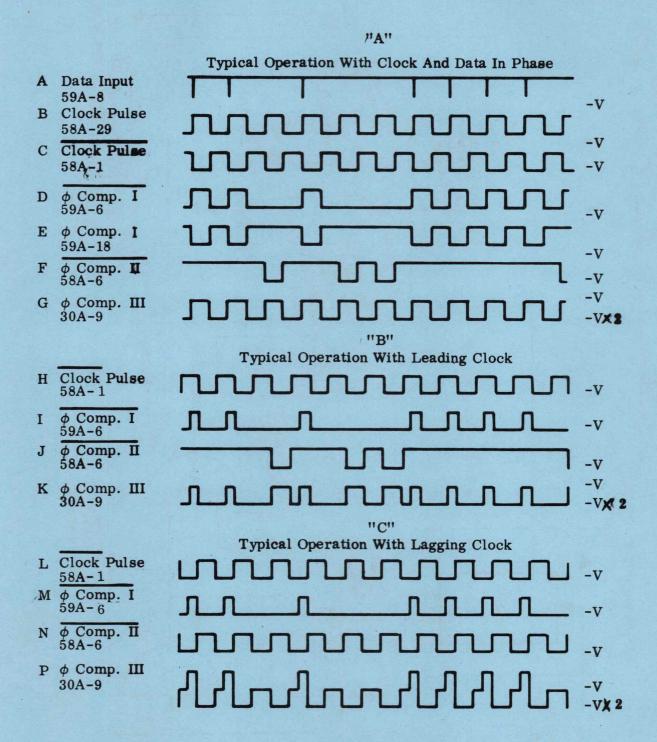


Figure 3-8. Phase Comparator Timing Diagram

The loop amplifier output is connected to the control terminal of the VCO, which produces an output frequency proportional to its control voltage input. The VCO is essentially a current-controlled switching circuit, utilizing a tunnel diode to sense the switching point. The switch output is differentiated and coupled through a dual amplifier to the frequency divider. The quiescent frequency of the VCO is adjusted by the FINE TUNING control on the front panel.

## 3.6 SYNC QUALITY CIRCUITS

The sync quality meter is driven by signals derived from phase comparator 1 and the positive peak detector. A timing diagram for typical operation of the sync quality circuits is shown in Figure 3-9.

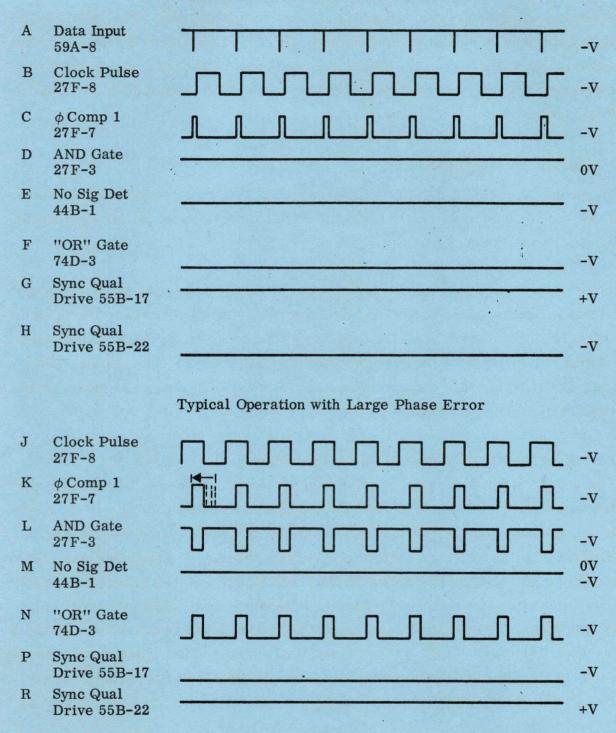
When the bit synchronizer is in lock, the output of phase comparator 1 (59A) is predominantly negative (waveforms C and K, Figure 3-9) since the phase error is small at this time. When lock is lost, the data transitions occur randomly throughout the bit period and the output of phase comparator 1 (figure 6-30) is less negative. Thus the average value of phase comparator 1 output can be interpreted as an indication of the quality of synchronization.

The output of no-signal detector 44B is a ground level voltage (waveforms E and M, Figure 3-9) as long as peaks of at least 0.25 volt occur. However, when the minimum peaks do not occur, the no-signal detector supplies a signal to OR gate 74D. AND gate 27F is enabled only during the first half of the bit period; thus the input to sync quality drive 55B is a dc signal (waveform F), except during leading clock operation. The positive-going pulses (waveform N) from the OR gate are then integrated at the sync quality drive input and cause the meter to read downscale. For the case of no data transitions, the input to the sync quality drive also causes a downscale reading of the meter. The sync quality circuitry is not used as a precision indication of synchronization, but is used in conjunction with the FINE TUNING meter as an aid in determining proper signal conditioner operation.

## 3.7 FREQUENCY DIVIDER

The output of the VCO is applied to a 20-stage binary counter. The ONE output of counter stage 56A is connected to the trigger input of counter stage 56B and to one input of a two-input NOR used as an AND gate (57B). This gate is inhibited except when switched in by relay closure or the FREQ BAND switch; its output is then connected through power inverter 57A to provide an inverted clock pulse to the timing generator.

Typical Operation with Small Phase Error



The ZERO outputs of the remaining counter stages are used as inputs to the AND gates. Selection of the AND gate outputs to be applied to special three-and four-input NOR circuits is controlled by relay action or the FREQ BAND switch. The output of NOR circuits is an inverted clock pulse for the frequency selected. The frequency divider output for NRZ operation is an inverted clock at twice the input rate; for RZ or split phase, it is an inverted clock at four-times-bit rate.

## 3.8 TIMING GENERATOR

The timing generator utilizes the VCO output through the frequency divider to produce the gating and timing pulses for proper operation of the signal conditioner. The logic diagram for the timing generator is shown in Figure 6-32. The timing diagram is shown in Figure 3-10.

Control voltages are produced by resistive networks and switching action of relays or of the INPUT MOD selector switch. The gating and timing pulses are produced by using the dc control voltages and the frequency divider pulses to gate the action of special DIODE AND-OR circuits. Each circuit contains two 3-input AND gates and a single 4-input AND gate which drive a 3-input OR gate. The output of the OR gate is connected through a power inverter to produce the final output of the special circuit. The AND gates are enabled by negative levels of 5 to 10 volts on all inputs.

The inverted clock pulse from the frequency divider is connected to counter stage 51A and power inverter 27A. The output of 51A (waveform C) is utilized only during RZ or SP operation. This counter input to AND-OR gate 26A (figure 6-32) is inhibited by a ground-level voltage from K23P4 during NRZ operation. This discussion will be concerned only with SP operation. The inverted clock at 51A-27 is four times bit rate (waveform B). The output of 51A is two times bit rate and is applied to AND-OR 26A, where the signal is inverted. This signal acts as the trigger for 51B. The output of 51B-10 is BIT RATE, which is applied to AND-OR 26B, where the proper gate has been enabled by P2. The P1 and P2 inputs to AND-OR gate 26B are set inhibit and enable dc voltages during NRZ and RZ operation; during split-phase operation, the P1 and P2 inputs are controlled by the correct phase selector to obtain correct phase lock for the bit rate output. BIT RATE output of 26B is applied to 47B. AND gate 8-10-12 is inhibited by a ground level applied at K25P3 while AND gate 2-4-6 is enabled. The output of 47B-1 is INTEGRATOR "B" ENABLE, which occurs at bit rate.

VCO Output

Counter Out

Out 26A-29

Counter Out

Out 26B-1 Diode "AND-OR"

Out 47A-29

( Comp 1)

Out 47B-1

φ Comp. 2 Out 94K-1

Diode "AND-OR"

(Int. B Enable)

Int. A Dump

Int. B Dump 48F-3

Diode "AND-OR"

Diode "AND-OR"

Diode "AND-OR"

Out 26A-29

Counter Out

Out 26B-1

Out 47A-29 (0 Comp. 1) 0 Comp. 2 Out 94K-1 Diode "AND-OR" Out 47B-1 (Int. B Enable) Int. A Dump 94J-2 Int. B Dump 48F-3 RZ Enable K24P4

51B-10

94J-2

Freq. Divider Out A52-2

Diode "AND-OR"

Diode "AND-OR"

(4 MC)

51A-28

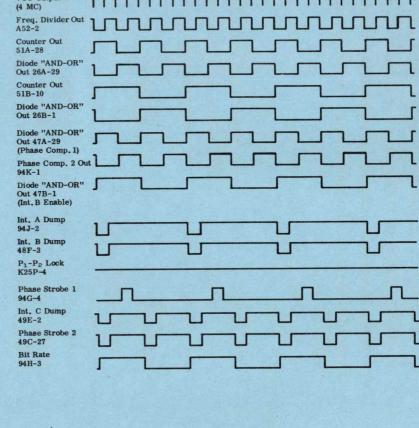
51B-10

-V

-V

PURPOSES

ONLY



Split-Phase Operation

-V

Non-Return-To-Zero Operation

Return-To-Zero Operation

Figure 3-10. Timing Generator, Timing Diagram

VCO Output

The output of AND-OR gate 50A is inverted INTEGRATOR "A" DUMP. This signal occurs at the beginning of the bit period and is one-eighth bit period wide. AND gate 17-19-21 on 50A is inhibited. The DUMP signal is obtained by ANDing BIT RATE,  $\overline{4XBR}$ , and  $\overline{2XBR}$  at pins 22, 24, and 26 respectively. Pin 20 is at a constant negative level. INTEGRATOR "B" DUMP is obtained in a similar manner from AND-OR gate 50B.

Phase comparator 2 and 1 signals are obtained in the following manner. As stated before, the output of 26A-29 is 2XBR inverted. This signal is again inverted at 27D and applied as 2XBR to pin 27 of 47A. AND gate 17-19-21 is inhibited while AND gate 23-25-27 is enabled. The output 47A-29 is inverted at 94K, and the resulting 2XBR signal is phase comparator 1.

Phase strobe 1 is the result of ANDing BR, 4XBR, and 2XBR at 49D pins 17, 18, and 19 respectively.

Integrator "C" Dump and Phase Strobe 2 are identical signals obtained by ANDing 2XBR and 4XBR at 49E and 49C.

For correct phase lock, the output of AND-OR gate 26B is an inverted bit-rate pulse at all times, except in RZ.

## 3.9 BIT DETECTOR

A simplified block diagram of the bit detector is shown in Figures 3-11 and 3-12. During RZ and NRZ operation, the buffer amplifier output is connected simultaneously to analog switches A and B. However, only the A circuits are used for polarity decisions; the B circuits are switched to a continuous dump and disable condition. After integrator A is discharged by the dump circuit, the output of analog switch A charges the integrating circuit according to the polarity of the input signal. The output of decision amplifier A is the bit decision for all six modulation types. The bit decision is connected to a two-stage shift register that is triggered at the bit rate. Outputs from the shift register are applied to the coincidence and gating circuits. The circuits are controlled by the INPUT MOD relays or switch settings as required for the particular modulation being received. The signal is then connected to the buffer and inverter stages to provide the normal and inverted NRZC outputs of the signal conditioner.

To decrease errors for any given amount of noise during split-phase operation, both the A and B integrating circuits are used to provide a large signal voltage difference

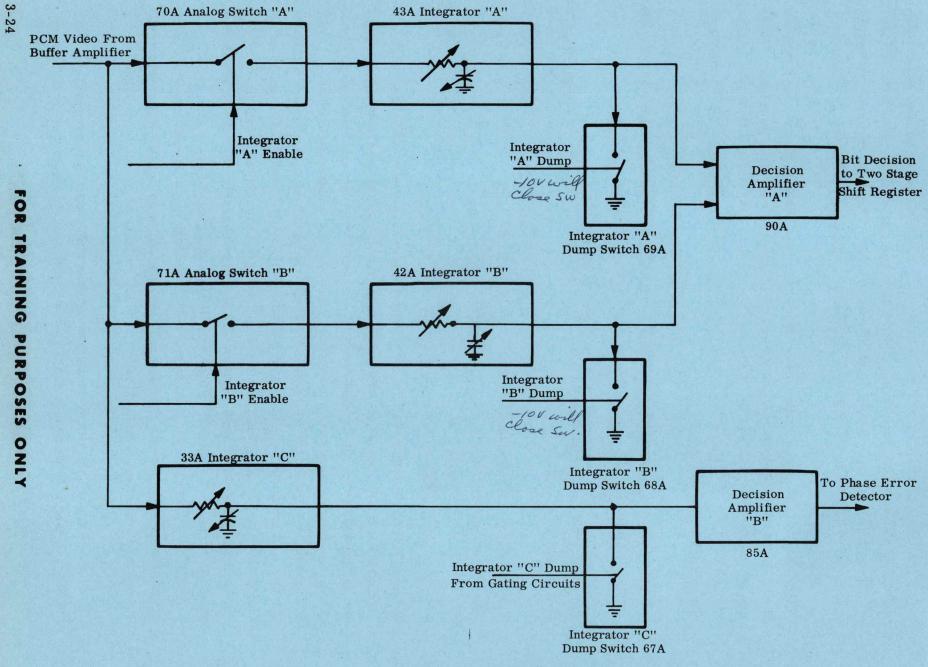


Figure 3-11. Bit Detector

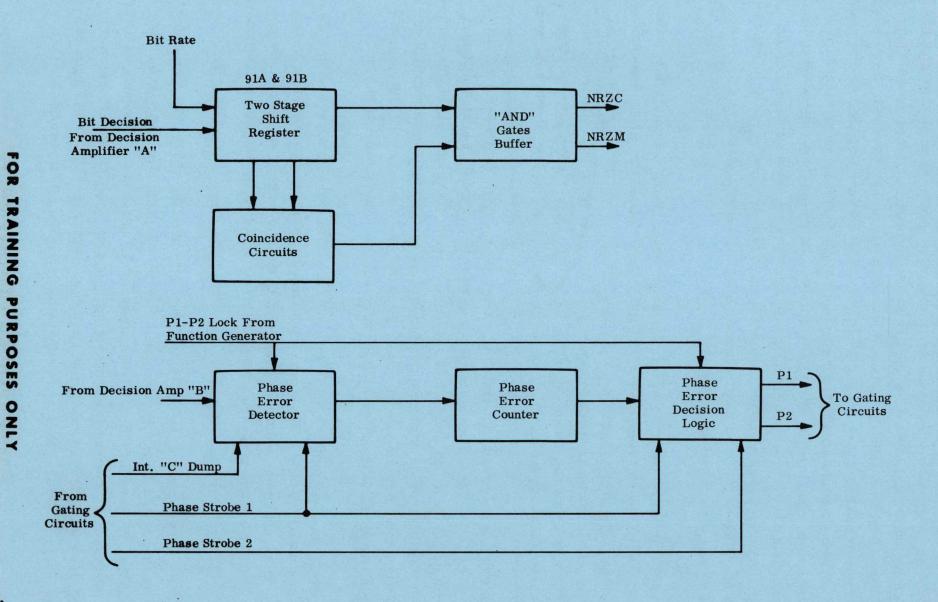


Figure 3-12. NRZ Decoder and Phase Detector

for the bit polarity decisions of decision amplifier A. The buffer amplifier output is also connected to the C circuits, which are used to resolve the bit location ambiquity. The output of decision amplifier B is connected to the phase error detector, a two-stage shift register and gating circuit similar to that used by decision amplifier A. The error signal is connected to the phase error counter, which supplies an output to the phase-error decision logic circuits. Whenever the error count exceeds the allowed maximum, the output signals to the bit synchronizer gating circuits are reversed in phase, and correct phase lock is acquired for the system. The bit rate clock for the six modulation types is applied to "AND-OR" logic circuits, which provide the normal and inverted clock outputs of the signal conditioner.

The logic diagram for the pulse integrating detectors and decision amplifiers is shown in the lower portion of Figure 6-32. The logic diagram for all data - NRZ decoder and phase detector is shown in Figure 6-33. A timing diagram for the entire decoder and correct phase detector is shown in Figure 3-13. The timing diagram illustrates operation with NRZ inputs of one megacycle or RZ and SP inputs of 500 kilocycles. The waveforms not shown for RZ and SP operation are the same as those for NRZ operation.

The buffer amplifier output is applied to analog switch A (70A, Figure 6-29) and analog switch B (71A). These circuits contain a gate pair driving a balanced diode bridge; the video from the buffer amplifier is applied to one side of the bridge. Enable and inhibit voltages from the timing generator are applied to a three-stage gate control circuit, which turns the gate pair on or off. When the gate pair is on, the video output from the diode bridge is connected to the integrator circuits (43A and 42A).

The integrator dump switches (69A, 68B, 67A) are connected between ground and the output of each integrator. The dump switch circuits are similar to the analog switch circuits, except for the addition of capacitors to the gate pair. These capacitors provide an initial current surge when the gate pair is turned on, discharging the integrators more rapidly.

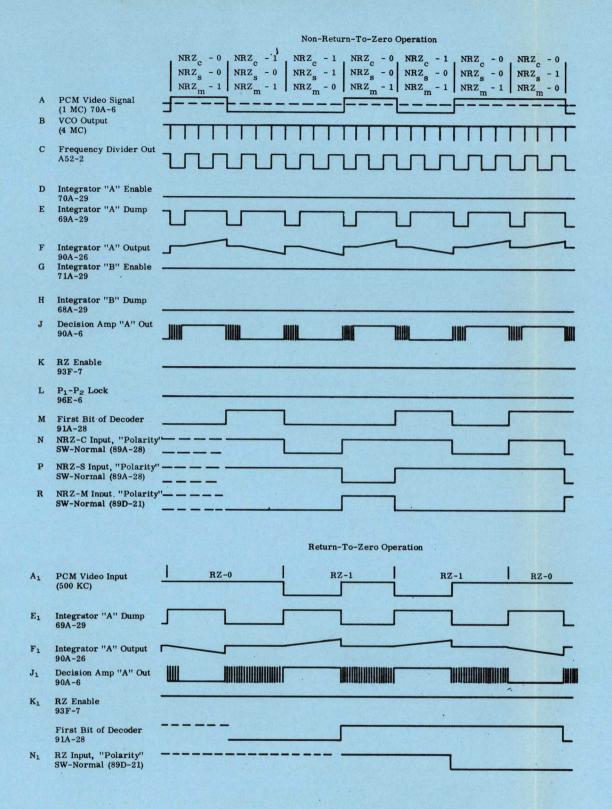
Integrator A is dumped at the beginning of each bit period for NRZ and SP operation; it is dumped at mid-bit for RZ operation, since the first half of the bit contains the information required for a bit decision. Integrator B is dumped continuously for NRZ and RZ operation; it is dumped at the beginning of each bit period for SP operation. Integrator C (33A) is used only during split phase operation; it is dumped every half bit period to provide isolation of the two distinct halves of SP bit periods.

After the integrators are dumped, the integrating capacitor begins to charge with a polarity determined by whether the incoming data bit is a "one" or "zero." The outputs of integrators A and B are connected to the inputs of decision amplifier A(90A). Each decision amplifier contains a high-gain, current and temperature stabilized, compound-pair differential amplifier whose output drives a tandem-operated amplifier. The output of decision amplifier A is a reconstructed digital version of the input waveform at the analog switch; this output is connected to the data decoder logic circuits. The output of integrator C is connected to decision amplifier B (85A), which compares the integrated signal with a ground potential and provides an output to the correct phase detector logic circuits.

The output of decision amplifier A (J, Figure 3-13) is connected directly to one steer input of shift register (91A, Figure 6-33) and through inverter 92A to the other steer input. Both shift register 91A and 91B are triggered by the integrator A dump signal. The outputs of shift register 91B are true data and inverted data for NRZC, RZ and SPC data. With the polarity relay (K33) closed or the front panel switch in NORMAL position, AND gate 92C is enabled for NRZC type modulation. The output of this gate is applied through OR gate 74B to supply true NRZC data through the line driver 89A to J1AB. AND gates 92B, 92D, and 93A are inhibited during NRZC operation by switching action of the POLARITY and INPUT MOD and relays or front panel switches.

During NRZS operation, these relays or switches inhibit AND gates 92B, 92C and 92D (Figure 6-33). The data outputs of both shift registers are supplied to AND gate 92F; the inverted data outputs are supplied to AND gate 92E. The output of the comparator formed by these AND gates is connected to OR gate 92G. These three gates provide a logical conversion of NRZS type modulation to inverted NRZC. The true NRZC output (P, Figure 3-13) is obtained through inverter 92H to AND gate 93A. The output of AND gate 93A is connected to OR gate 74B and the signal then follows the same circuitry as for NRZC modulated inputs.

Operation with NRZM modulation inputs is the same as that for NRZS except AND gate 92D is enabled. The output of OR gate 92G is now a logical conversion of NRZM type modulation to true NRZC data (R, Figure 3-13) NRZM data may be obtained at J1-AE if desired. The NRZC code obtained at OR gate 74B is applied to conversion circuitry similar to the initial incoming conversion circuitry to perform the reconversion.



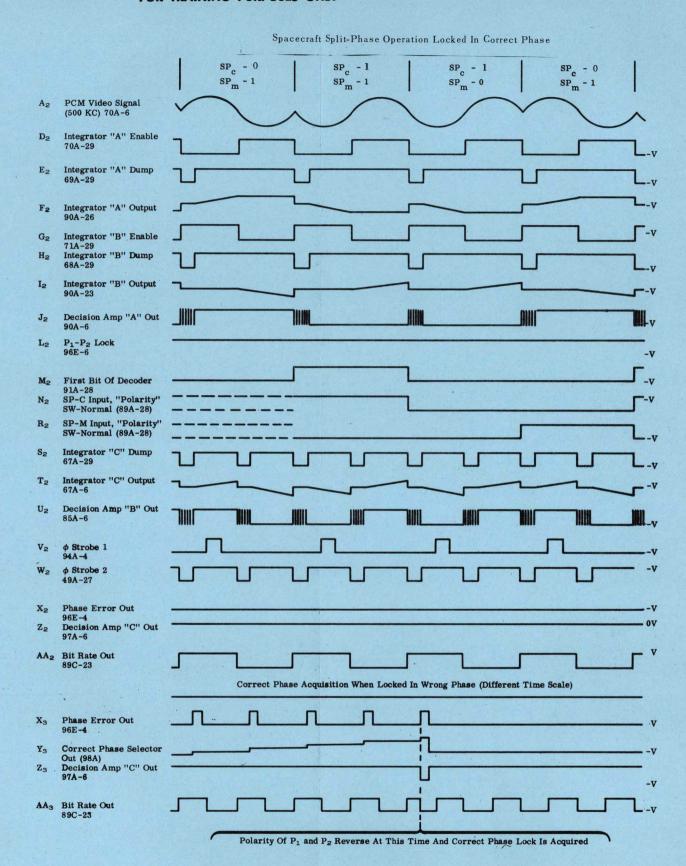


Figure 3-13. All-Data-NRZ Decoder and Correct Phase Detector Timing Diagram

Operation with RZ modulation inputs is the same as that for NRZC. However, shift register 91A is triggered at mid-bit by the integrator A dump signal; this delays the output of shift register 91B by one and one-half rather than one bit period. Refer to waveforms  $A_1$  through  $N_1$  of Figure 3-13 for comparison.

Operation with SPC modulation inputs is the same as that for NRZC; operation with SPM modulation inputs is the same as that for NRZM. However, bit location for split phase modulation is subject to an ambiquity which is resolved by the correct phase detector circuitry. Refer to waveforms  $A_2$  through  $R_2$  of Figure 3-13 for comparison of operation.

The bit rate clock pulse is developed by the same circuitry for all types of inputs. The local clock pulse from the timing generator is connected to AND gate 93F and inverter 93E. The AND gate is enabled only during RZ operation. The output of inverter 93E is applied through AND gate 93D to OR gate 93B. The output of the OR gate is inverted bit rate pulses for all types of input. This output is applied through power inverter 94B and line driver 89C to supply true bit rate at J1AD.

When a split-phase signal is being received, the bit synchronizer locks onto the carrier signal and produces an output at two times the bit rate of the incoming signal. This output can be counted down by the frequency divider to produce bit rate in two possible phases. The function of the correct phase detector is to select the correct phase position for the bit rate from the two possible values.

The edges of bit times in the split-phase signal can be identified by the presence of two adjacent half cycles of the same polarity. In a noise-free situation, this can only occur at bit edges. When the signal is noisy, occasional half cycles of the same polarity will occur within a single bit period because of the noise. The correct phase detector must ignore those noisy areas to the maximum extent possible.

The output of decision amplifier B is a reconstructed digital version of the input waveform with polarity decisions of each input half cycle made independently ( $U_2$ , Figure 3-13). The resulting reconstructed waveform is connected to a two-stage shift register (95A and 95B). The adjacent half cycle outputs of the shift registers are compared with phase strobe 1 timing signal ( $V_2$ , Figure 3-13) by AND gates 74A and 74C. The AND gates produce an output pulse through OR gate 96B when two adjacent half cycles of identical polarity occur in phase with the timing signal.

Assume the phasing is such that an output pulse from the AND gates is applied through the OR gate to AND gate 96E,  $(X_3, Figure 3-13)$ . This pulse is now loaded into the nine-stage shift register. When five error bits are loaded into the nine stages, an output is produced by correct phase selector 98A  $(Y_3, Figure 3-13)$  that triggers decision amplifier C (97A). The output or decision amplifier C  $(Z_3, Figure 3-13)$  is a command to bistable multivibrator 95C to change the phasing of its outputs. The change of phase for the  $P_1$  and  $P_2$  signals is applied to DIODE AND-OR 26B, (Figure 6-32) which then provides the opposite phase of the bit rate signal as its output. This means that no further error bits are loaded into the shift registers (Figure 6-33), since the bit rate signal is of the correct phase. The required noise immunity is satisfied, since random error bits loaded into the shift registers because of noise will not produce an output from the correct phase selector.

## 3.10 PROGRAMMING SYSTEM

A programming system is provided in the PCM signal conditioner to allow rapid, externally controlled switching between different input signals. This allows the switching between any one of eight standard formats by a control signal. Eight plug-in printed circuit cards are pre-programmed with the parameters for coarse and fine frequency, input modulation, polarity, and loop bandwidth. It is possible to select a "variable" format which allows the front panel controls to be employed to set up the signal conditioner.

#### 3.10.1 BLOCK DIAGRAM ANALYSIS

The selection of format is controlled by nine input lines (Figure 3-14), one of which is switched to a logical "1" (-10 volts) to select a format. Unselected lines should be at logical "0" (0 volts).

The following discussion presents the selection of plug-in card number one as a typical example. The remaining seven cards are selected in the same manner as the example presented. Any variable format is also selected in the same manner, except that each parameter must be established from the front panel switches. Take for example the case where format number 1 is selected by applying a "1" to relay driver A87 (Figure 6-34). The relay driver operates such that when a -10 volts is applied as an input, the output is forced to zero volts or ground. One output of relay driver A87 is applied to one side of the coil of K 40. The other side of the coil is tied to -24 volts. With the application of ground, the coil energizes and closes the four sets of contacts associated with the relay.

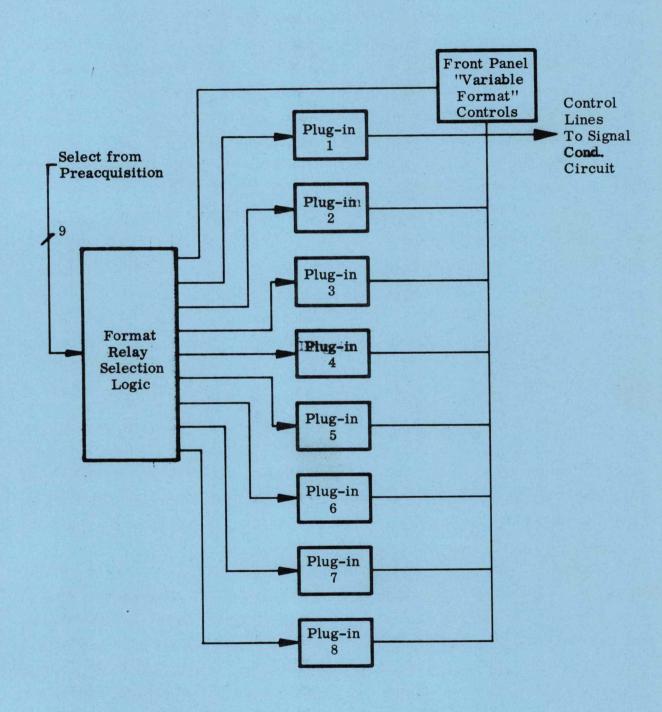


Figure 3-14. Programmer System Simplified Block Diagram

Contacts 2B/1T close to ground and provide a complete circuit for the UNIT 1 indicator to light. It is also applied to pre-programmed card number one, pin 13. Contacts 3B/2T close and apply a -10 volts to A41-17 (Z) (Sheet 2) contacts 4B/3T close and apply one of the tuning legs of the VCO to A41-10 (Y) (Sheet 2). The last set of contacts 5B/4T close and apply a second leg of the VCO tuning control to A41-12 (X) (Sheet 2).

Sheet 2 shows the wiring for each card or plug-in unit. Pin 11 is provided as an input to the VCO frequency adjust (Figure 6-34). The variable resistor on each of the eight pre-programmed cards is preset so that when its output is applied to the VCO, it forces the VCO to establish the basic frequency that is applied to the first stage of a frequency counter chain. An example of this is if the frequency selected by card number one is 500 kc, and this is to be picked off the second stage of the frequency counter, then the VCO must be forced to apply 1 mc to the first stage in the counter chain. As previously stated, this is accomplished by applying a given amount of voltage from the present center tap of the variable resistor.

The input to pin 13 on pre-programmed card one applies a ground to the anode of three diodes whose cathodes are connected to pins 2, 7, and 8. This ground level of pin 2 provides a complete path for K21 and K27 to energize. The contacts of K27 (Figure 6-33) close and activate the correct phase detector logic. The two sets of contacts (Figure 6-32) associated with K21 (Figure 6-34), close to activate the timing generator logic which establishes the basic timing for the type code that is selected by this card. Providing the ground potential at pin 7 of card number one allows K33 to energize. This relay has two sets of contacts which close to connect loop filter 1 into the circuit. Providing the ground on pin 8 applies a ground to one side of K37 and with a -24 volts applied to the other side allows the relay coil to energize. The contacts of this relay close to connect the correct phase detector in the circuit (Figure 6-34).

The input to pin 17 on pre-programmed card number one applies a -10 volts on the cathode of CR 4, 5, 6, 7, and 8. The anodes of these diodes are connected to pins 18, 21, 22, 29 and 27 respectively. The function of these five diodes is to select which stage of the frequency counter is selected to give the required frequency output. These five diodes are applied to matrix drivers on sheets 3 and 4 of Figure 6-34. The matrix drivers function as a six input AND gate. With any voltage input applied to any one of the six inputs, the relay associated with that particular matrix driver is not energized because a -24 volts is applied to both sides of the coil. With further tracing of the five diode connections, it can be seen that the only matrix driver not connected to or affected

by them is B63. With no input applied to B63 it produces its zero volt output. This provides a zero volt potential to one side of K11. The other side is tied to -24 volts; hence, the relay is energized. The relay associated with matrix driver B63 is K11. The contacts of K11 close to ground which is one input needed to true AND gate 54C (Figure 6-34). The other input to the AND gate is from the reset side of frequency counter stage 79B. These two inputs select a frequency within the 1.02 to 2.05 kc range. The actual frequency within this range is selected by the action of the variable resistor on each of the eight pre-programmed cards.

#### Note

The front panel FREQ BAND indicators do not light when one of the eight pre-programmed cards is selected by memory. They light only when the variable format is used.

## 3.11 <u>INDICATOR CIRCUIT</u>

With S6 or S7 in position 1 through 8, a -24 volt level is applied to relay driver B88-24. This voltage makes B-88-18 appear as an open circuit; hence, no indicators light. When either S6 or S7 are in position, -10 volts is applied as an input to relay driver B88. This causes B-88-18 to look like ground. With a -10 volts applied to the other side of the lights, the lights come on corresponding to the setting of S1. A schematic of the indicator circuit is shown in Figure 6-35.

### SECTION 4

#### GROUP SYNCHRONIZER

## 4.1 GENERAL DESCRIPTION

#### 4.1.1 OPERATING CONCEPTS

The group synchronizer insures that the stored program decommutator's operation is in proper synchronization with the incoming data. To accomplish this, the synchronizer examines the input data for proper prime frame sync, and ID sync, and generates outputs that enable the stored program processor to operate in synchronization with the data train.

Prime frame synchronization is achieved by comparing a programmed sync code pattern with the data train until a matching sync pattern is found, then determining if bit errors within the incoming sync pattern are within preset limits. When synchronization occurs, a prime frame sync pulse is generated and the prime frame sync check mode is initiated.

In the prime frame sync check mode, the prime frame synchronizer continues the examination of the data train for valid patterns and supplies memory with word rate pulses. The memory, using the first sync pulse as a starting point, notifies the prime frame synchronizer when to expect the next sync pattern. If the proper sync pattern is found during the time specified by memory, the prime frame synchronizer generates a second sync pulse output. It continues checking until the proper number of sync words have been sampled and initiates the lock mode. If the proper number of sync pulses are not found, the prime frame synchronizer continues checking until the number of misses allowed exceeds the programmed value, after which it returns to the search mode.

In the lock mode, the prime frame synchronizer generates word rate pulses that enable the balance of the stored program decommutator to be synchronized with the data train input. In this mode, a different number of bit errors may be programmed for sync pattern checks. If the number of bit errors in the data train exceeds the programmed number of bit errors allowed, no prime frame sync pulse is generated. The number of sync words containing excessive bit errors, in turn, is recorded. When the number

of sync words containing errors exceeds the programmed number of misses allowed, the prime frame synchronizer returns to the search mode and attempts to re-acquire sync by the method previously discussed.

Prime frame identification (ID) characters appear in a PCM data train as a prime frame count designating the number of prime frames cycled from the start of a major cycle. For example, if there are 50 prime frames cycled from the start of a major cycle, each prime frame can be identified by a count from 1 to 50. Provided the location of the ID word within the prime frame is known and the number and position of ID characters within the word are known, the prime frame number from 1 through 50 can be established and checked for validity.

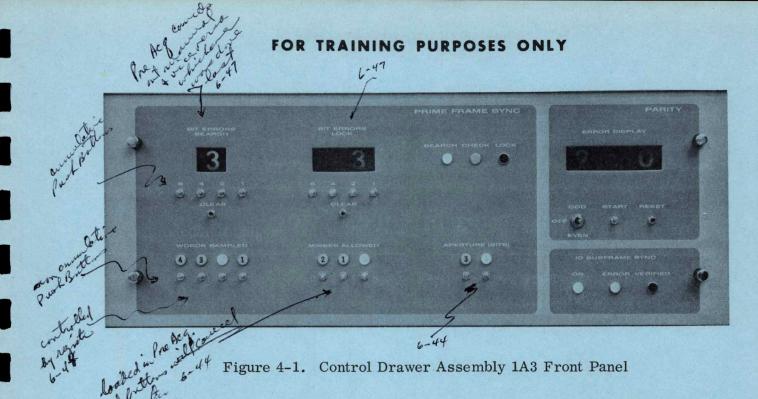
For ID sync operation, the program parameters for checking the accuracy of the ID are stored during preacquisition mode. When the decom memory sends a signal to the ID synchronizer specifying the next word in the data train is the ID word, the ID characters are extracted from the incoming data and shifted into a register. The ID characters are then loaded into a counter. The contents of the ID shift register and ID counter are made available to the comparator and the first comparison is made. The ID counter is incremented by 1 at the end of each prime frame. The updated ID code is now compared with the ID code in the data train each prime frame. When two successive comparisons are made between counter ID and incoming ID, the synchronizer goes into the ID verified mode. After ID has been verified, a signal is generated in the ID synchronizer and sent to decom memory. This signal tells the decom memory that the prime frame number has been established and verified and that the processing of incoming data can begin.

### 4.1.2 CONTROLS AND INDICATORS

There are five parameters that can be changed from the front of the control drawer assembly 1A3 (see Figure 4-1). These controls are: Bit Errors Search, Bit Errors Lock, Words Sampled, Misses Allowed, and Aperture Bits. Indicators are: Prime Frame Sync; Search, Check, Lock, and ID Subframe Sync; On and Error or Verified.

#### 4.1.3 CAPABILITIES

- a. Operates at bit rates from 0.5 cps to 1 Mc.
- b. Operates at word length from 4 to 64 bits (variable from word to word).
- c. Operates at prime frame length from 4 to 512 words.
- d. Provides rapid prime frame and word synchronization through the use of automatic search, check, and lock modes of operation.



- Provides subframe synchronization for up to three subframes. e.
- f. Provides manual override for part of programmed criteria.
- Provides display indicators for modes of operation and parts of prog. grammed criteria.

# PRIME FRAME SYNCHRONIZER

#### 4.2.1 BLOCK DIAGRAM ANALYSIS (Figure 4-2)

The prime frame synchronizer consists of the following major groups of logic:

- Preacquisition program storage.
- b. Data register.
- B seiner 6-58, 59, 40 and last 2 bit registers 18+28 Pg6-61 6-54, 55, 56 and Car Drivers on 6-58,59,68, 61(4 Series) c. Correlation logic.
- Word length counter. 10-60 6-63
- Aperture generator.
- f. Aperture-sync pulse comparator.
- Misses allowed counter. g.
- 68-78-88 1-63 h. Words sampled counter.
- i. Prime frame sync status control logic.

The preacquisition program parameters are loaded into storage registers in the prime frame synchronizer during sequence Nos. 1, 3, and 5 of the preacquisition mode of the stored program processor. Once these parameters are loaded, they will remain unchanged until another program is selected and preacquisition is again initiated. For

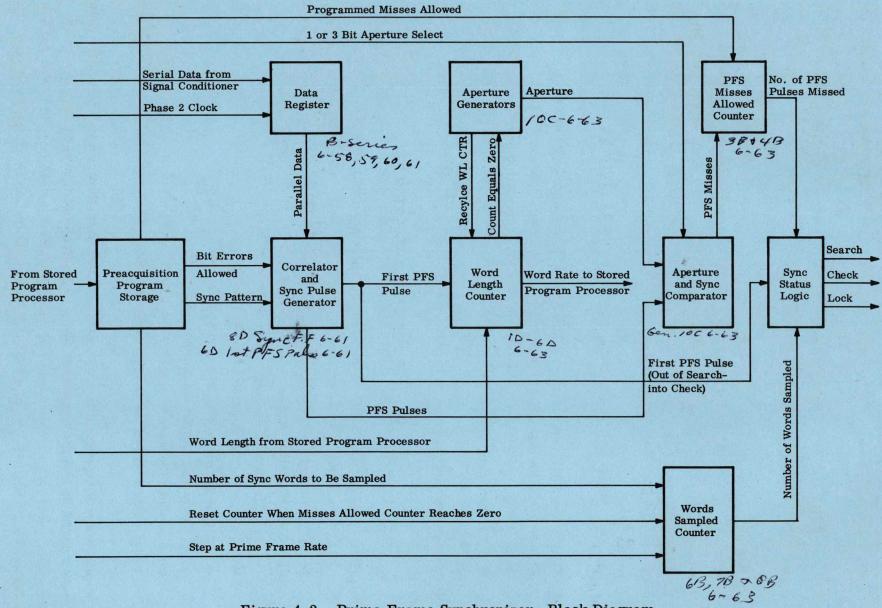


Figure 4-2. Prime Frame Synchronizer, Block Diagram

a block diagram analysis, the significant parameters are:

- a. Bit errors allowed between sync pattern and sync word.
- b. Prime frame sync pattern.
- c. Number of allowable misses of prime frame sync pulses. 3B+4B 6-63
- d. Number of sync words sampled to check the quality of sync. 68,78488 6-63

When the preacquisition mode of the stored program processor is complete, data can be shifted serially into a data register; then it is made available in parallel form to the correlator and sync pulse generator logic. When the prime frame sync pattern was loaded during sequence No. 1 of preacquisition mode, it was immediately made available to the correlator. Conditions are now set to generate a first prime frame sync pulse when the sync word in the data train matches the stored sync pattern within the allowable bit errors specified by program.

When the first prime frame sync pulse is generated, three major functions occur:

(1) First memory timing cycle is initiated, (2) the word length counter is loaded with the length of the data word following the sync word, which is eight bits in ACE and (3) the sync status logic switches the mode of the prime frame synchronizer from SEARCH to CHECK mode. In the CHECK mode, prime frame sync pulses are checked for accuracy, and if all conditions are satisfactorily met, the prime frame synchronizer will go into the LOCK mode.

The next step in the CHECK mode is for the word length counter to count down to zero. When this occurs, a word rate pulse is generated and sent to the stored program processor to initiate decom memory timing cycles. Word rate is also used as the <u>basic</u> timing pulse for logic functions in the prime frame and ID synchronizers. The zero count in the word length counter is also used to trigger the aperture generators.

The output of the aperture generators is a one-bit gate and a three-bit gate. Only one is used for a given program and is selected during sequence No. 5 of the preacquisition mode. Aperture gates can be considered as a time window that sets the limits wherein the second and succeeding prime frame sync pulses must occur. The aperture and sync pulses are compared in the aperture-sync comparison logic, and if the prime frame sync pulses are present during aperture time, no errors are generated. If the sync pulse is not present during aperture, an error signal will stop the misses allowed counter which has been programmed for a maximum of two misses.

It is necessary at this point in the analysis to examine the function of the words sampled counter. The number of prime frames that will be used to check the validity of the sync pulses is loaded into storage registers in the prime frame synchronizer during sequence No. 5 of the preacquisition mode. A maximum count of four can be loaded from the storage registers into the counter. After the first prime frame sync pulse is generated, the words sampled counter will be decremented at the end of each prime frame. The basic condition for going into prime frame LOCK mode is for the words sampled counter to reach a zero count before the misses allowed counter reaches zero. This condition will prevail if the prime frame sync pulses missed have not exceeded the programmed misses allowed.

The sync status logic monitors the outputs of the misses allowed and words sampled counters. If the misses allowed have been exceeded (zero count from misses allowed counter), the prime frame synchronizer will go out of CHECK mode and back to SEARCH mode. If the allowable misses have not been exceed during the programmed number of words sampled, the synchronizer will go from CHECK to prime frame LOCK mode.

The prime frame synchronizer will remain in the LOCK mode until synchronization with the incoming data is lost. If a sync pulse does not occur, each prime frame, the synchronizer will return to the SEARCH mode and wait for another first prime frame sync pulse. The events previously described will be repeated until the system is again in the prime frame LOCK mode.

### 4.2.2 PHASE 1 AND PHASE 2 CLOCK PULSES

Inverter 3B, sheet D, Figure 6-37 receives the serial NRZ-C data from the signal conditioner. This data passes through NOR gates 4B (if not in test), 3D, 4D, 1A upper, and 1A lower (all on sheet D) thus providing "data" and "Data:" to the serial-to-parallel shift register. Phase 1 (pin 3 of 3B sheet D, Figure 6-37) also comes from the signal conditioner and is termed "Bit Rate" at the output of the signal conditioner. The phase 1 passes through 3B, 4B, 3D, and 4D (sheet D); this phase 1 then feeds the clocking logic modules 10A through 2A, sheet C, Figure 6-37. Clocking logic provides two-phase-clock output, called phase 1 and phase 2. Phase relationship is as shown in Figure 4-3.

## 4.2.3 MEMORY STORAGE LOGIC

Storage of program criteria is accomplished by use of many flip-flops, which are loaded at preacquisition time. Loading signals (called sequence 1 to sequence 5) are

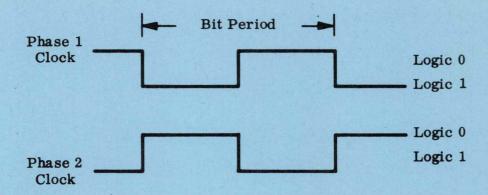


Figure 4-3. Phase Relationship, Phase 1 and Phase 2 Clock

generated by memory bits 2 through 6 of the preacquisition words. These preacquisition bits are decoded by logic located in 3A6A1A to 3A6B9A. See Figure 6-37, sheet A, modules 1A to 10A, and sheet B, modules 1A to 9A. Because of nomenclature changes by Radiation, the following bit association is necessary to understand the decoding logic:

Memory bit number	2	3	4	5	6
Associated logic bit number	M35	M36	M37	M38	M39

During preacquisition and at sequence 1 time, the decoder logic will operate as follows: First, memory bit 2 will be a logic "1." Therefore,  $\overline{M35}$ , M36, M37, M38, and M39 will be a logic 0 (o volts). Also, a strobe signal generated by memory will be "0" at sequence 1 time. NOR gate 1A will be enabled by all zeros on the inputs therefore the logic 1's pass through inverters 3A (upper) and 4A enabling NOR gate 5A (upper) to generate a sequence 1 (logic 1) at pin 10 of 6A. Sequence 1 is the triggering line for 32 flip-flops, which store 32 bits of the PFS pattern. These flip-flops are located in row B of sheets A, B, C, and two flip-flops on D. (See Figure 6-37.) Sequence 2 will enable the storage of the other 32 bits of the PFS pattern. This PFS pattern is originally part of preacquisition memory and will be stored in these 64 flip-flops only when a preacquisition start is initiated. Sequences 3 and 4 will trigger 64 flip-flops for the storage of the PFS length. Sequence 5 will enable other storage flip-flops, such as WORDS SAMPLED, MISSES ALLOWED (located sheet A, Figure 6-36), APERTURE, etc.

#### NOTE

Using module type logic, flip-flops triggered by Phase 2 will set (or reset) at the START of a bit period and flip-flops triggered by Phase 1 will set (or reset) in the middle of a bit period.

#### 4.2.4 SHIFT REGISTER

The prime frame synchronizer has a 64-stage register for storing and converting to parallel the serial NRZ-C data from the signal conditioner. Sixty stages of the register are located on sheets K, L, and M of Figure 6-37, and four stages are located on sheet N of Figure 6-37.

Data is shifted serially into CSR 1B on sheet K by Phase 2 clock. Only 32 of the 64 stages are used in ACE since the longest word in the incoming data is 32 bits (sync pattern for interleave format). The parallel outputs from the CSR's in the register are connected directly to the correlator logic on sheet E, F, G, and H of Figure 6-37.

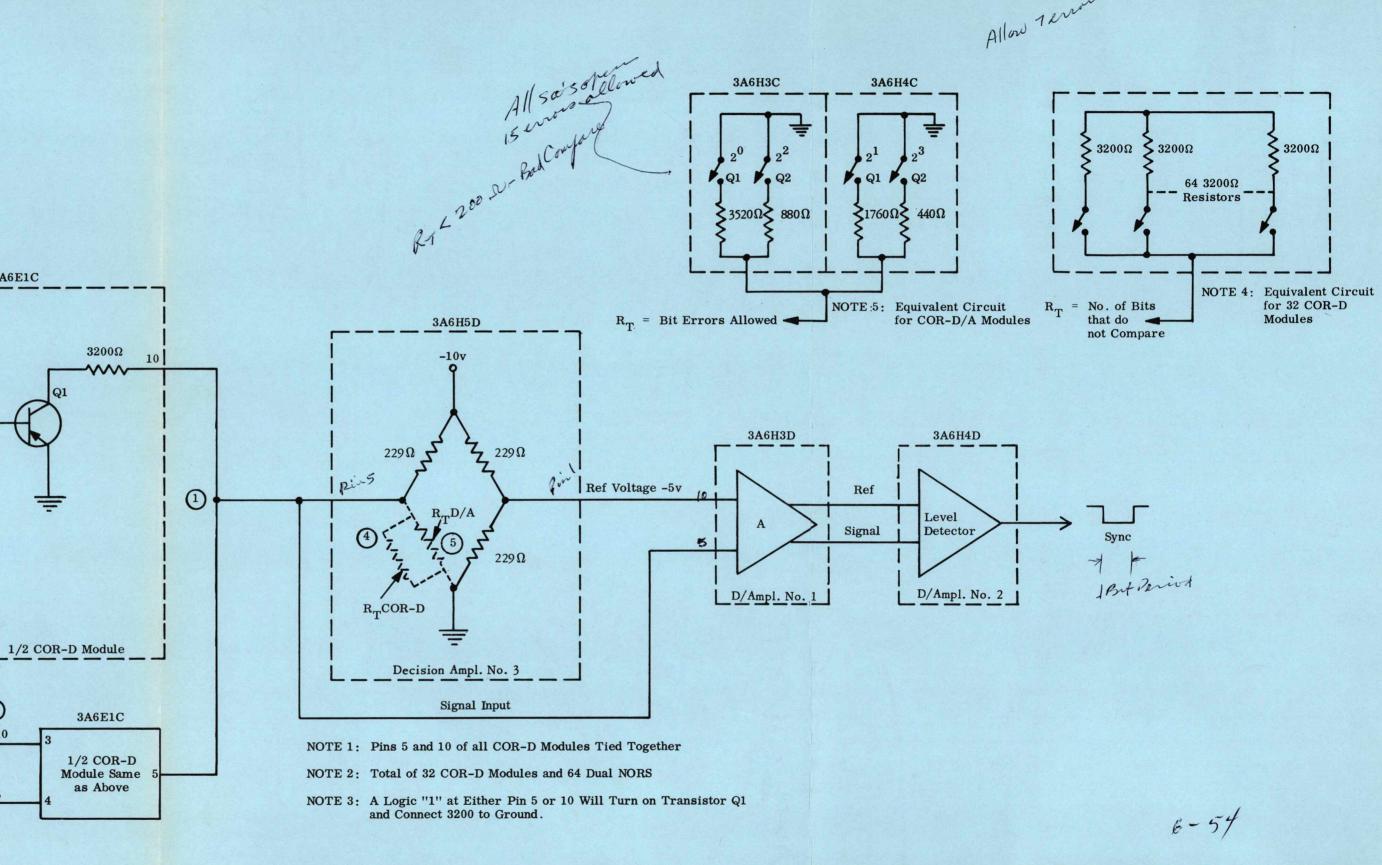
# 4.2.5 PFS CORRELATION LOGIC (Figure 4-4)

Prime frame sync occurs when the sync word in the data train matches the stored sync pattern within the limits of programmed allowable bit errors. Dual NOR 3A6E1A will have logic 0's at pins 5 and 10 when the stored pattern and sync word correlate. If the pattern bit is a logic 1 and sync word bit is a logic 1, the output of E1A is a logic 0 on both pins 5 and 10. If the pattern bit is a logic 1 and the sync word bit is a logic 0 the pattern bit NOT term is ANDed and the output at pin 5 is a logic 1. A logic 1 on the base of Q1 turns on the transistor and connects 3200 ohms to ground.

The outputs of all COR-D (correlator driver) modules are connected together at a common bus (see note 1, Figure 4-4). Therefore the maximum resistance that can be obtained from the COR-D modules is infinite resistance when all bits correlate (see note 4, Figure 4-4). If one bit did not correlate, then 3200 ohms would be the total resistance from the COR-D modules, two bits would be 1600 ohms, etc.

As discussed in paragraph 4.2.1, the number of bit errors (non-correlation) allowed is loaded into storage registers (1A3 sheet F) during sequence No. 5 of preacquisition mode. This four-bit code is applied to correlator D/A modules 3A6H3C and 3A6H4C. The logic 1 bits in the code turn on transistors in the modules and connect parallel resistances in the circuit (see note 5, Figure 4-4). Once the bit errors allowed have been decoded, a fixed resistance will be connected into a resistance bridge in module 3A6H5D.

Module 3A6H5D is one of three modules of a decision amplifier. It consists of three resistors that form three legs of a resistance bridge. The fourth leg is formed by the parallel resistances of the COR-D modules and COR-D/A modules. Assuming that all



3A6E1C

+10v

3A6E1B

Sync Bit 33

Enable I 33

Pat Bit 33

Sync Bit 33

3A6E1A

0

0

Stored Pattern Bit 1

Stored Pattern Bit 1

Sync Word Bit 1

Sync Word Bit 1

Enable II

Figure 4-4. Prime Frame Sync Correlation Logic, Simplified Schematic

bits of the sync word correlate with the stored pattern, the total resistance would be the resistance of the COR-D/A. Assuming also that zero bit errors allowed had been programmed, the COR-D/A resistance would be approximately 200 ohms. In this condition the bridge is balanced and the signal input to H3D would be a minimum of -5 volts. With -5 volts or greater on the input to H3D, module H4D generates a sync pulse of one bit period duration.

With two non-correlations occurring and no bit errors allowed, the resistance connected in parallel with the COR-D/A resistance by the COR-D modules would be 1600 ohms. The total resistance would then drop from approximately 200 ohms to around 177 ohms. This causes the signal input to H3D to decrease to less than a -5 volts. These conditions, where the number of bit errors detected exceed the bit errors allowed, prevent a sync pulse from being generated for that particular prime frame. When a sync pulse is not generated, it is considered as a "miss" and is used to step the misses allowed counter (refer to Figure 4-2).

# 4.2.6 WORD LENGTH COUNTER

The word length counter is composed of six down-counting flip-flops located at 1D through 6D on sheet S, Figure 6-37. Loading of these CSR's is enabled via NOR gates 1E through 6E, with the common loading signal (ground at load time) generated by NOR gate 7D, sheet S. (Output of 7D feeds 1E through 6E via comp driver 2D on sheet M). Initial loading of word length counter is enabled by the FIRST PRIME FRAME SYNC pulse at pin 1 of NOR gate 7D. If an eight-bit word were to be loaded into the counter, then M4 (program bit 10) will be logic 1. Therefore, the output of module 4E, pin 5, will be logic 0, setting CSR 4D, and resetting the other CSR's.

The following truth table explains the function for the word length counter.

Module	1D	2D	3D	4D	5D	6D
Initial condition	1	1	1	0	1	1
First phase 2 trigger (at CSR 1D)	0	0	0	1	1	1
Second phase 2	1	0	0	1	1	1
Third phase 2	0	1	0	1	1	1
Fourth phase 2	1	1	0	1	1	1
Fifth phase 2	0	0	1	1	1	1
Sixth phase 2	1	0	1	1	1	1
Seventh phase 2	0	1	1	1	1	1
Eighth phase 2	1	1	1	1	1	1

At the eighth count the word length counter will reload itself with a count (4 to 64 bits) which memory will designate for the next word. This self-reloading is accomplished by "END OF WORD" gates 6C and 7C (lower). These gates sample the inverted reset outputs of the six-word-length flip-flops. When the count of "0" is reached, the output of 7C pin 10 goes positive, resetting 8C. CSR-8C pin 9 then directly sets 8D. The output of 8D, pin 9, then enables gate 9D (upper) along with phase 2. The output of 9D, called "1 Aperture Start" then enables gate 7D, which loads the word length counter. Other inputs to 7D are the comparison of  $\overline{PFS}$  and  $\overline{Aperture}$  at 1A pin 10, and the first word sync pulse (not used in ACE operation).

#### 4.2.7 APERTURE 1 GENERATOR AND WORD RATE GENERATOR

The word length counter counts to zero and generates an end-of-word gate (Figure 4-5). End-of-word triggers CSR S8C to the reset state which, in turn, direct sets S8D and S8E. The reset outputs of these two CSR's now enable phase 1 and phase 2 clock pulses to pass through dual NOR S9D (Figure 4-6). Phase 2 direct sets CSR S10C. The trailing edge of phase 1 occurs one bit period later and triggers S10C back to the reset state generating No. 1 aperture.

When "No. 1 aperture start" is generated, the output of S7D goes to logic 0 for 1/2 bit period and reloads the word length counter. When "No. 1 aperture stop" occurs at phase 1 time, the output of S10D becomes word rate and word rate.

The output of S9D is fed back through S5B and R9E and immediately direct sets S8C. CSR's S8D and S8E are also triggered back to the reset state by phase 2 and phase 1 respectively.

# 4.2.8 APERTURE 3 GENERATOR (Figure 4-7)

The 3-bit aperture generator utilizes a two-stage counter that is started by the No. 3 Aperture Start pulse. This start pulse is generated by gates 4C and 5C, at next to the last bit time of the word length counter. A logic 1 at Aperture 3 Start sets CSR-10B and resets CSR-9C. Output of 10B provides the aperture gate (true Boolean term is aperture). With the reset of CSR-9C, gate 9C, gate 9B (upper) allows phase 1 clock to set CSR-9A, which, in turn, triggers CSR-10A. At a count of three, CSR-9A and CSR-10A will both be set, their reset outputs enabling gate 9B (lower) which resets CSR-10B ending the 3-bit aperture pulse. Thus, CSR-10B provides a pulse for 3-bit periods.

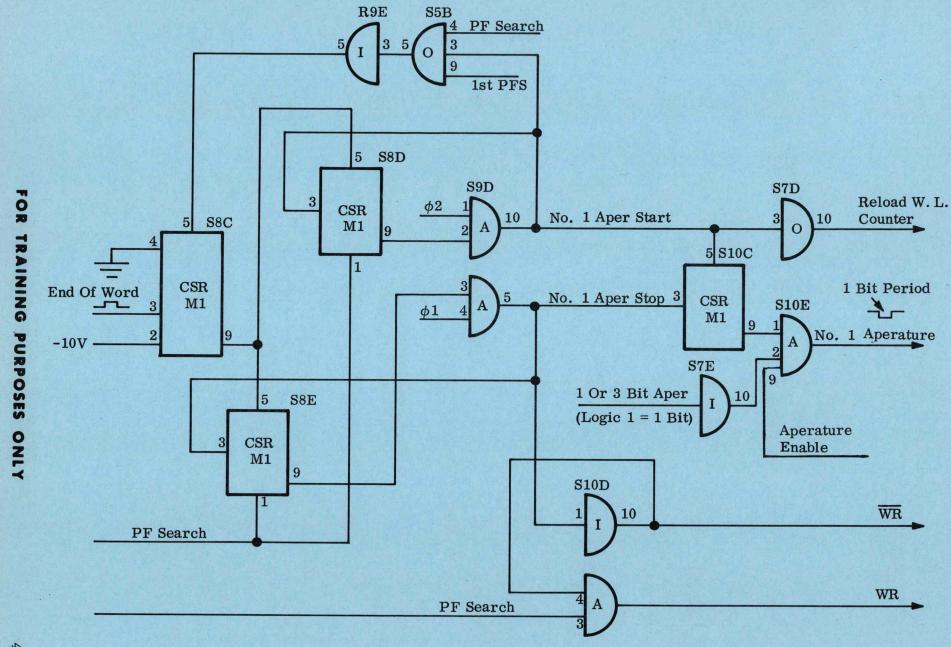


Figure 4-5. Aperture 1 Generator and Word Rate Generator

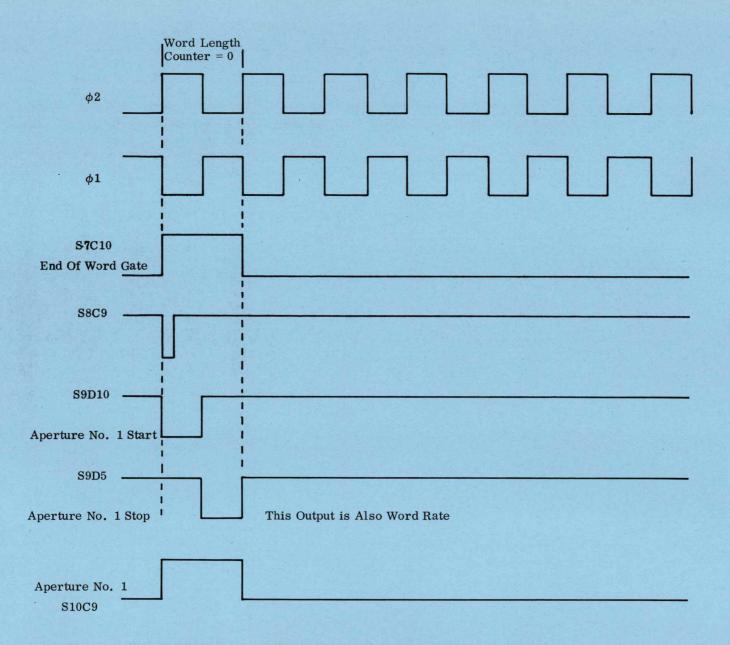


Figure 4-6. Aperture 1 and Word Rate, Synchrogram

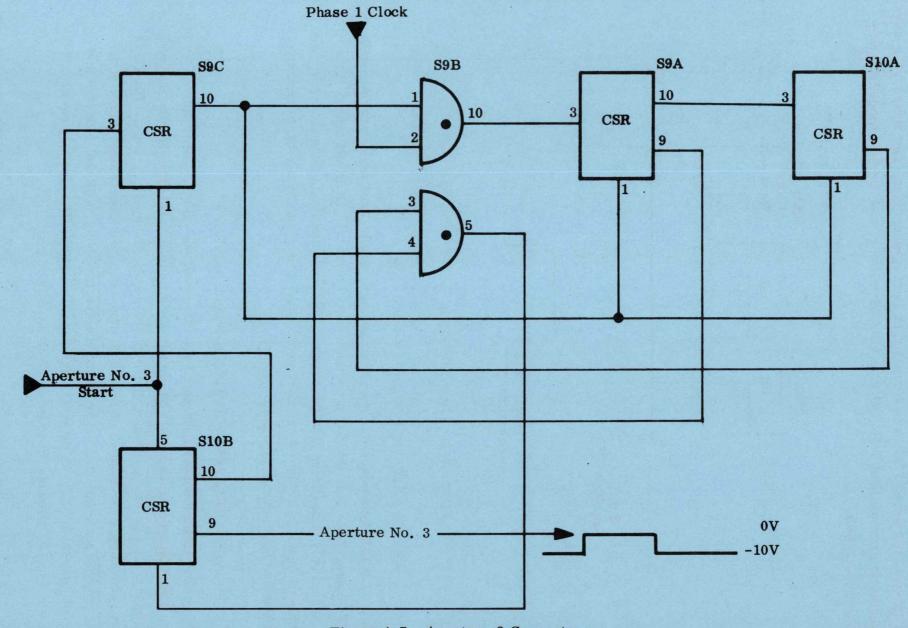


Figure 4-7. Aperture 3 Generator

Test logic for the PFS pulse is composed of 1-bit aperture generator or 3-bit aperture generator, comparison logic, misses allowed counter, and words sampled counter (see Figure 4-8).

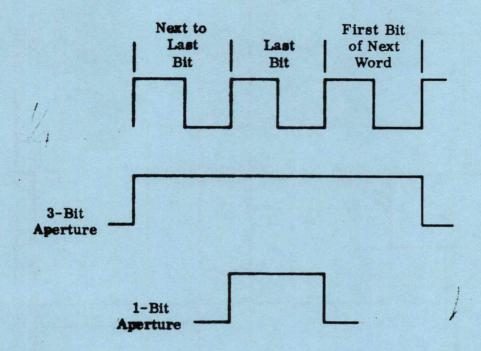


Figure 4-8. Timing Diagram, 1- and 3-Bit Apertures

# 4.2.9 APERTURE GATING (Figures 4-9 and 4-10)

NOR gate 10E determines if a 3 or 1 bit aperture will be used for comparison with the PFS pulse. Gate 10E also has a common enable signal which allows the aperture to be sampled only once during a prime frame. This Aperture Enable signal is generated in CSR-8E (sheet L). The PF member occurs during the last bit period of the prime frame and is generated by memory logic.

# 4.2.10 APERTURE/PFS COMPARISON (Figure 4-11)

The prime frame member first sets CSR-2B and resets CSR-2A, providing a "1" on pin 4 of NOR gate 1B and a "0" on pin 3. When the aperture signal is present, nothing happens. If a prime frame sync pulse occurs during the aperture time, CSR-2A is set, providing a "1" at pin 3 of 1B and no error signal is generated. But, if a prime frame sync pulse does not occur during the aperture time, CSR-2A is not set and pin 3 of 1B remains a "0." At the end of aperture time, CSR-2B is reset, providing a "0" at pin 4 of 1B, allowing 1B to generate an ERROR signal.

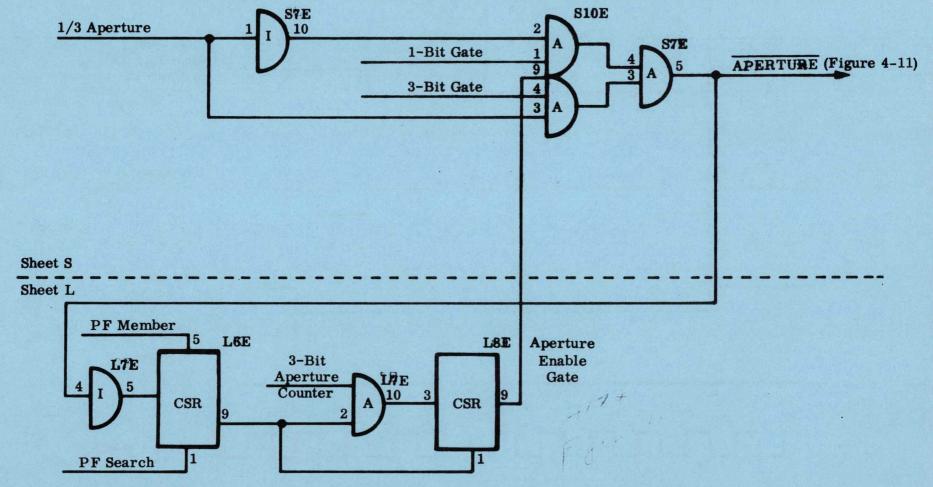


Figure 4-9. Partial Schematic for Aperture Gating

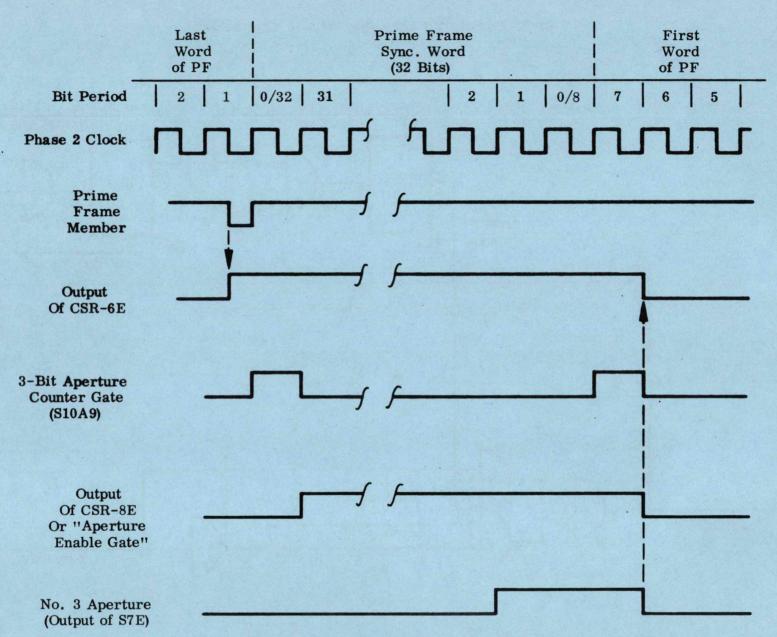


Figure 4-10. Timing Diagram for Aperture Enable Gate

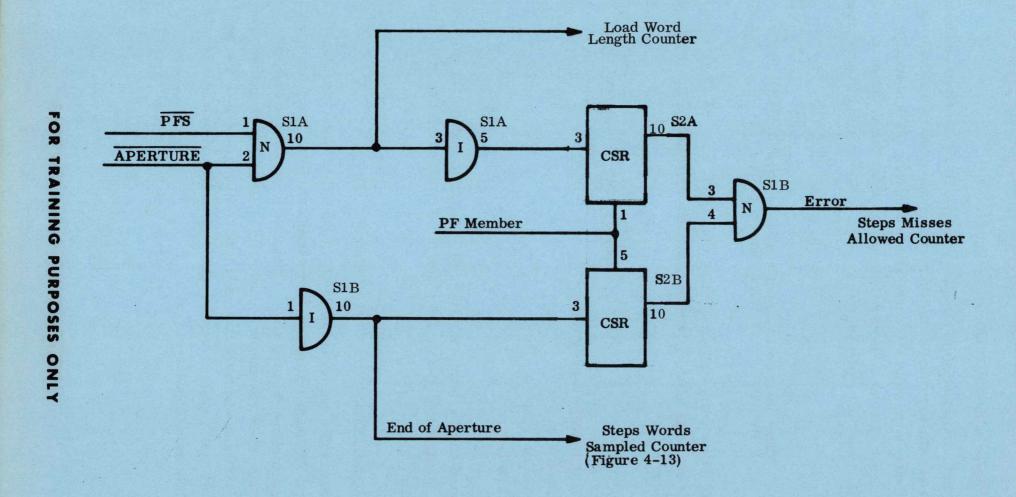


Figure 4-11. Partial Schematic of Comparison Logic

# 4.2.11 MISSES ALLOWED COUNTER (Figure 4-12)

The PFS test logic contains two sampling counters. First, the Misses Allowed counter, which is stepped every time an ERROR signal is generated; and second, the Words Sampled (better term would be Prime Frames Sampled), which is stepped by the aperture signal. Misses Allowed counter partial schematic is shown in Figure 4-12. If two misses were to be allowed, then 2<sup>1</sup> would be a logic 1 and 2<sup>0</sup> a "0" at module 3A.

#### NOTE

These bit 2<sup>1</sup> and 2<sup>0</sup> are stored, at preacquisition time in CSR's A4E and A5E. See Figure 6-36.

When the common enable trigger (ground) comes true, the CSR-3B is reset and CSR-4B is set. The following is a truth table for the counter action if two errors were allowed:

	CSR-3B Reset Output	CSR-4B Reset Output
Initial setting logic level	1	0
First error	0	1
Second error	1	1
Third error	0	0

Upon generation of a third error, the two "0" outputs enable NOR gate N9D to set CSR-S5A. Output of CSR-S5A will generate a SEARCH condition in the prime frame synchronizer.

## 4.2.12 WORDS SAMPLED COUNTER (Figure 4-13)

The words sampled counter is loaded with the stored program count for the first time by the first PFS pulse through loading gates S6A and S8A. The counter is triggered by "end of aperture" on the positive transition. Since aperture is enabled only once per prime frame, the words sampled counter will be stepped at the prime frame rate. When all set outputs from the counter is logic 0, NOR gate S7A is true and a logic 1 on pin 10 of S7A will reload the words sampled and misses allowed counter and will generate LOCK mode (Figure 4-14).

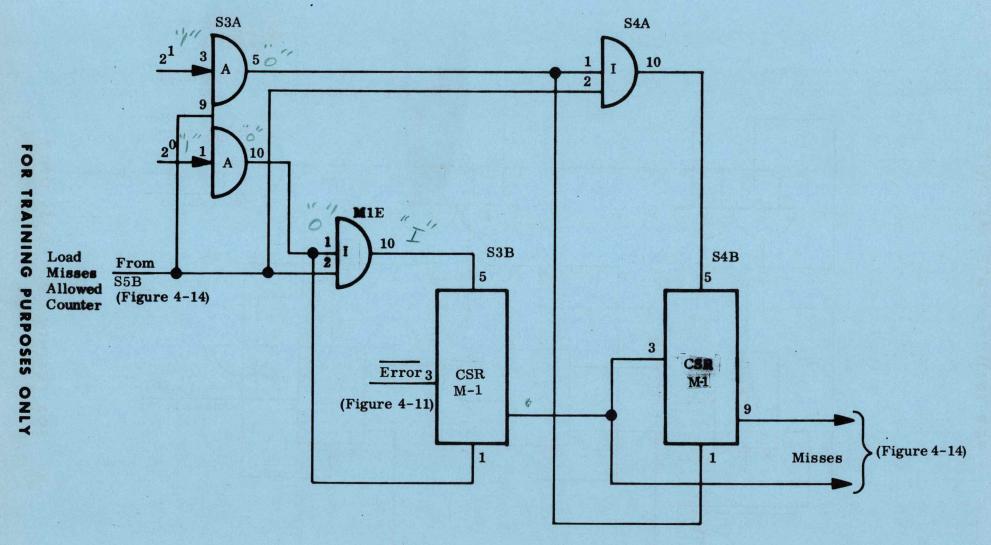


Figure 4-12. Misses Allowed Counter 3A6 Sheet S

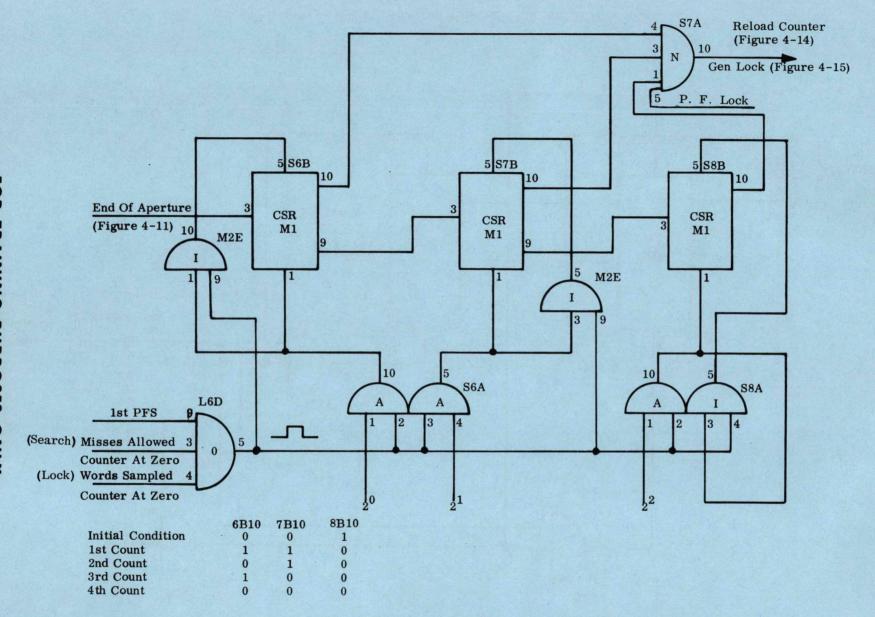


Figure 4-13. Words Sampled Counter

Figure 4-14. Partial Logic Diagram of Synchronization Control

# 4.2.13 LOADING WORDS SAMPLED AND MISSES ALLOWED COUNTERS

Loading of the Words Sampled and Misses Allowed counters comes from three sources. First, prime frame sync pulse (a logic 1) generates "0" outputs at gates S5B and L6D (see Figure 4-15). The logic 0 outputs will load both counters. When the Words Sampled counter reaches a count of zero, gate S7A resets CSR-L7D, which again will cause a logic 0 on the "Load" lines. If the Misses Allowed counter reaches its maximum count, then CSR-S5A will be set and again generate a load signal. It should be noted that the misses must exceed their allowed count within the number of words to be sampled if gate N9D is to set CSR-S5A (i.e., if two misses were allowed in four words sampled and three misses were present within the four words, then CSR-S5A would be set).

#### 4.2.14 SYNCHRONIZATION STATUS LOGIC

The sync logic receives three basic signals: preacquisition, Misses Allowed versus Words Sampled, and PFS Error (see Figure 4-14). At loading of preacquisition memory (starting of decom), output of NOR gate L1D is logic "0," which directly sets L2D providing a SEARCH signal.

With the first PFS pulse, CSR-L2D resets, providing a logic 1 for CHECK at L3E. If, during the number of prime frames sampled, the Misses Allowed count is not exceeded, then CSR-L7D is reset, which, in turn, resets CSR-L2E. Resetting of L2E generates a  $\overline{\text{LOCK}}$  function to indicate a lock condition for the synchronizer. However, if the Misses Allowed were exceeded, then CSR-S5A would be set, in turn setting CSR-L2D and generating a SEARCH condition again.

Once in a LOCK condition, one Prime Frame Sync error will allow NOR gate L3E to set CSR-L2D (via gate L1D), thus generating a SEARCH condition.

#### 4.3 ID SYNCHRONIZER

# 4.3.1 BLOCK DIAGRAM ANALYSIS (Figure 4-16)

The ID synchronizer consists of the following functional groups of logic:

- a. Program storage registers.
- b. Position counter.
- c. MSB/LSB shift register.
- d. Up-down counter.

Figure 4-15. Loading of Word and Misses Counters

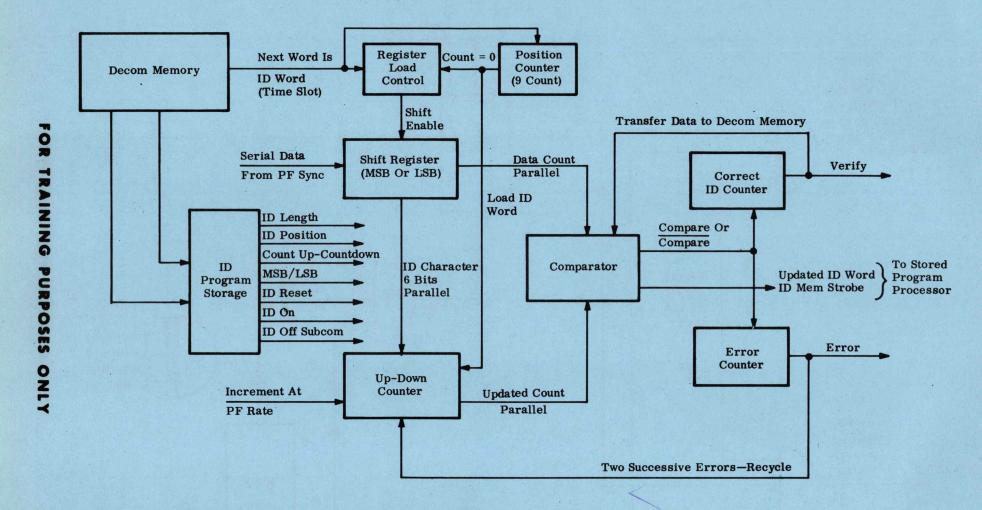


Figure 4-16. ID Synchronizer, Simplified Block Diagram

- e. ID comparator.
- f. Correct ID counter
- g. Error counter.

The program parameters for ID synchronization are loaded from the stored program processor during sequence No. 5 of preacquisition mode. These parameters are used throughout the ID sync logic and will be discussed in applicable paragraphs.

Serial data from the prime frame synchronizer is loaded into the MSB/LSB shift register when the decom memory sends a signal informing the ID sync that the next word in the data train is the ID word. This signal is called "time slot" and occurs at word rate time of the last word preceding the ID word. When "time slot" is received, the position counter (PC) is loaded with a count of 9 (ACE) and starts to count toward zero. During the time the PC is counting, a shift enable gate allows the ID word in the data train to be shifted into the MSB/LSB register. When the PC reaches zero, the shift enable gate ends and prevents any more data from entering the MSB/LSB register. The shifting of the ID word then takes place from "time slot" until PC equals zero which is the time required to shift the ID word MSB first (ACE) into the proper location in the MSB/LSB shift register.

Once the ID word is in the shift register, it is available on the input gates of the up-down counter. When the positions counter reaches a zero count, the ID characters (6 in ACE) are loaded into the up-down counter. The shift register contents are compared with the counter contents. If they compare, the correct ID counter is triggered to a count of one.

The 6 characters in the ID word contain the number of the prime frame that is presently in the group sync. At the end of the existing prime frame, the up-down counter will be incremented by one. The output of the up-down counter, which is now sitting in the comparator, is the updated ID count. On the next prime frame at "time slot," the second ID word is loaded into the shift register. The output of the shift register is also applied in parallel to the comparator. At this time, the comparator is looking at the updated count from the up-down counter and the second ID word from the next prime frame. If the two counts compare, the correct ID counter is triggered to a count of two. If the second ID word coming in compares with the updated count, the ID correct counter logic will generate a "verify" signal.

In order to generate a "verify," two successive compares must be generated by the comparator logic. Conversely, if two successive non-compares occur, the error counter counts to two and the ID sync will go out of verify and back into ID search.

On the next prime frame after "ID verify" occurs, the ID sync will send an "ID memory strobe" to the stored program processor. When the strobe is received, the stored program processor will read the contents of the up-down counter (correct ID count) into the ID adder. This establishes synchronization with the correct prime frame and enables to decom memory to start processing data.

#### 4.3.2 ID SHIFT REGISTER

Input data is received from CSR-K2B of Figure 6-37; this serial data is present at gates Z1B pin 2 and Z9B pin 4. These two gates, on sheet Z, provide the input to an MSB/LSB shift register composed of CSR's 1D through 9D. Data entry into the register is controlled by CSR-2A (sheet Z). If incoming data is "MSB first" (as in ACE), the output of 2A = 1, thus allowing NOR gate 1B to pass this data.

The data is shifted into the register from left to right or from CSR-1D to CSR-9D, leaving the LSB in CSR-1D. However, if incoming data is "LSB first," then 2A = 0, NOR gate 9B is enabled, and data is shifted from right to left or from CSR-9D to CSR-1D, again placing the LSB in 1D. It should be realized from the foregoing discussion that this register provides a standard output format (i.e., LSB in 1D). Shifting of data through the register is accomplished by a discrete number of phase 1 clock pulses. These pulses are gated by module Z4E, with pin 1 having the controlling time gate. The time gate at pin 1 starts with TIME SLOT and ends with POSITION COUNT (PC). See Figure 4-17.

TIME SLOT occurs during the last bit of the word before an ID word. This TIME SLOT sets CSR-Y10A, allowing the phase 1 clock at Z4E to shift data through the ID shift register. TIME SLOT also resets CSR-X2E, which, in turn, allows the position counter to count the number of ID bits to be entered into the ID shift register. After a discrete number of clocks the position counter resets CSR-Y10A, thus disabling further shifting of data through the ID shift register. In this manner the programming of the position counter assures that only bits of the ID Word are present in the shift register. The PC count is stored in CSR's-W5A through W10A at preacquisition time, and reloaded into the position counter when a count of zero is reached by the position counter.

#### 4.3.3 ID UP-DOWN COUNTER

The ID up-down counter consists of CSR's Y1D through Y9D (Figure 6-37). At the end of the first PC count (after first PFS pulse), a Dump Enable signal enters the contents of the ID shift register into the up-down counter.

Figure 4-17. Partial Diagram for Clocking ID Shift Register

Dump Enable NOR gates are Y1E through Y5E. Outputs of the up-down counter pass through buffer amplifier Y1C to Y9E, into the stored program processor unit for synchronization of the block counter. Loading of the up-down counter is initiated by the TIME SLOT pulse, setting CSR-Y10B (see Figure 4-18). However, not until Y10B is reset (by PC) will D1F-9A generate a 1US pulse output (see Figure 4-19). This 9A output directly sets CSR's 1D through 9D, clearing the ID storage register, and disables the COUNT ENABLE signal at 8A. When D1F-9A turns off, it turns on D1F-10C, which generates the DUMP ENABLE signal at 10E and continues disabling the COUNT ENABLE signal. When D1F-10C goes off, the loading sequence is complete and the COUNT ENABLE signal will be present again. "Load or Recycle" signal is generated by any one of three conditions (see Figure 4-20), PF SEARCH, ID ERROR, or LAST PRIME FRAME. Any of these signals reload the ID storage register with the information that is presently in the ID shift register.

#### 4.3.4 UPDATING

Incrementing the ID storage register by one count is accomplished by CSR-X10B. Prime frame MEMBER sets X10B, which, in turn, sets or resets Y1D, thus incrementing the storage register by one bit. CSR-X10B is reset by TIME SLOT, allowing the next PF MEMBER to increment the register again. In this way the count stored in the ID storage register should agree with the next ID count coming into the shift register.

Because of flexibility of the decom, the ID storage register must be able to increment up or down; that is, the incoming ID count can be either increasing or decreasing with successive prime frames. NOR gates 1B through 8B provide this flexibility.

#### 4.3.5 COMPARISON LOGIC

Comparison logic uses diode gates 1B through 9B (sheet X). If comparison does exist between ID shift register and updated ID storage register, all zeros are outputted by the diode gates. Therefore, outputs of gates 1C and 2C are 1's to diode gate 3C, whose output will be a logic 1 for correct comparison.

At pre-acquisition load CSR-X7D is set, generating an ID SEARCH signal (see Figure 4-21). If two successive compares are present, the two-stage verify counters X6C and X7C will set X10C, generating an ID VERIFY. This verify counter also resets X7D, generating ID SEARCH. CSR-X5D and X6D form a two-stage error counter, which, at two successive errors, generate ID SEARCH. It should be noted that one ERROR resets the verify counter or one VERIFY resets the error counter.

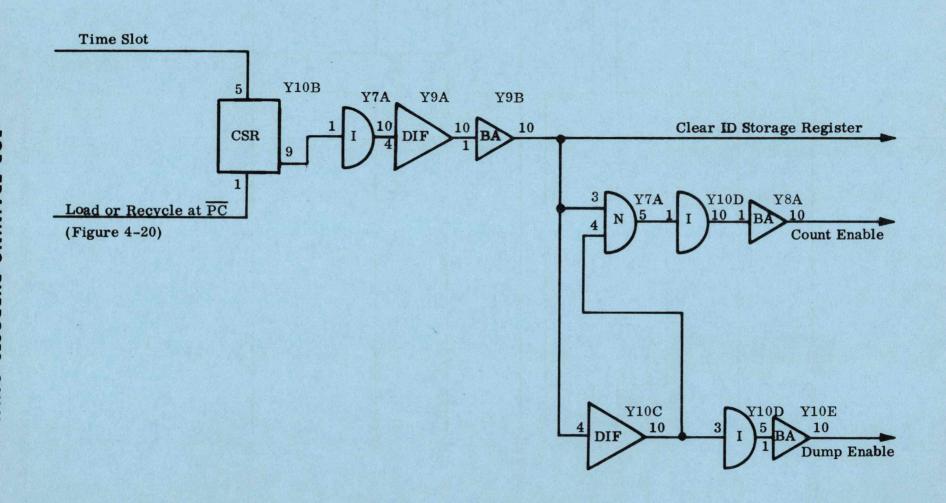


Figure 4-18. Partial Diagram for Up-down Counter Loading Signals

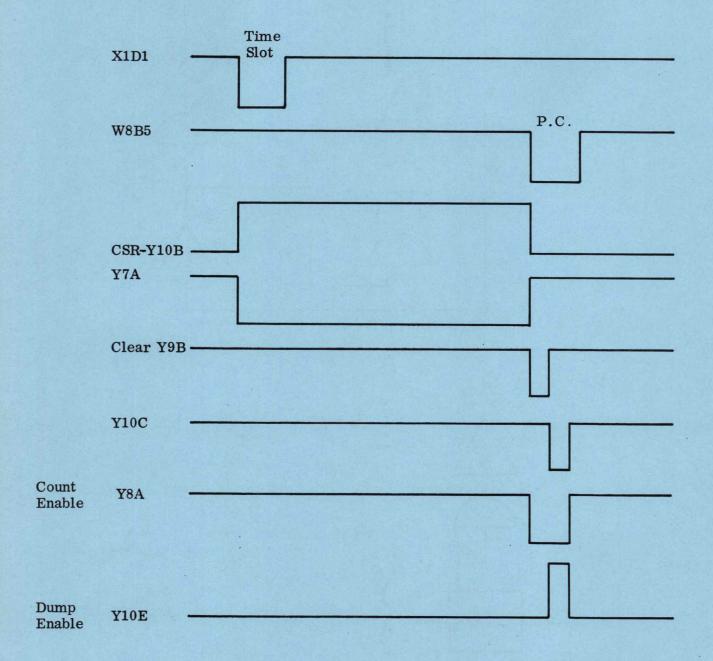


Figure 4-19. Synchrogram, Up-Down Counter Loading Signals

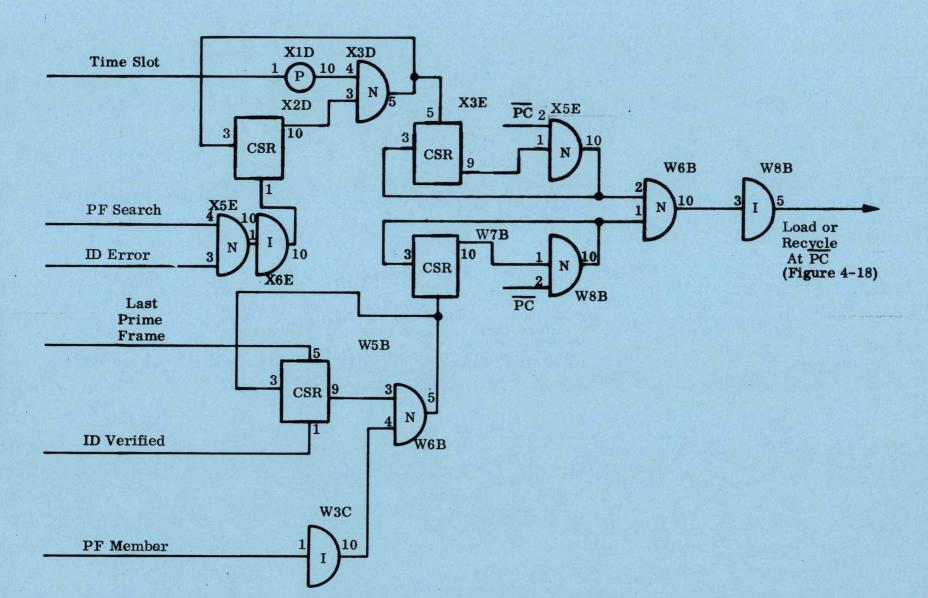


Figure 4-20. Load or Recycle Generation

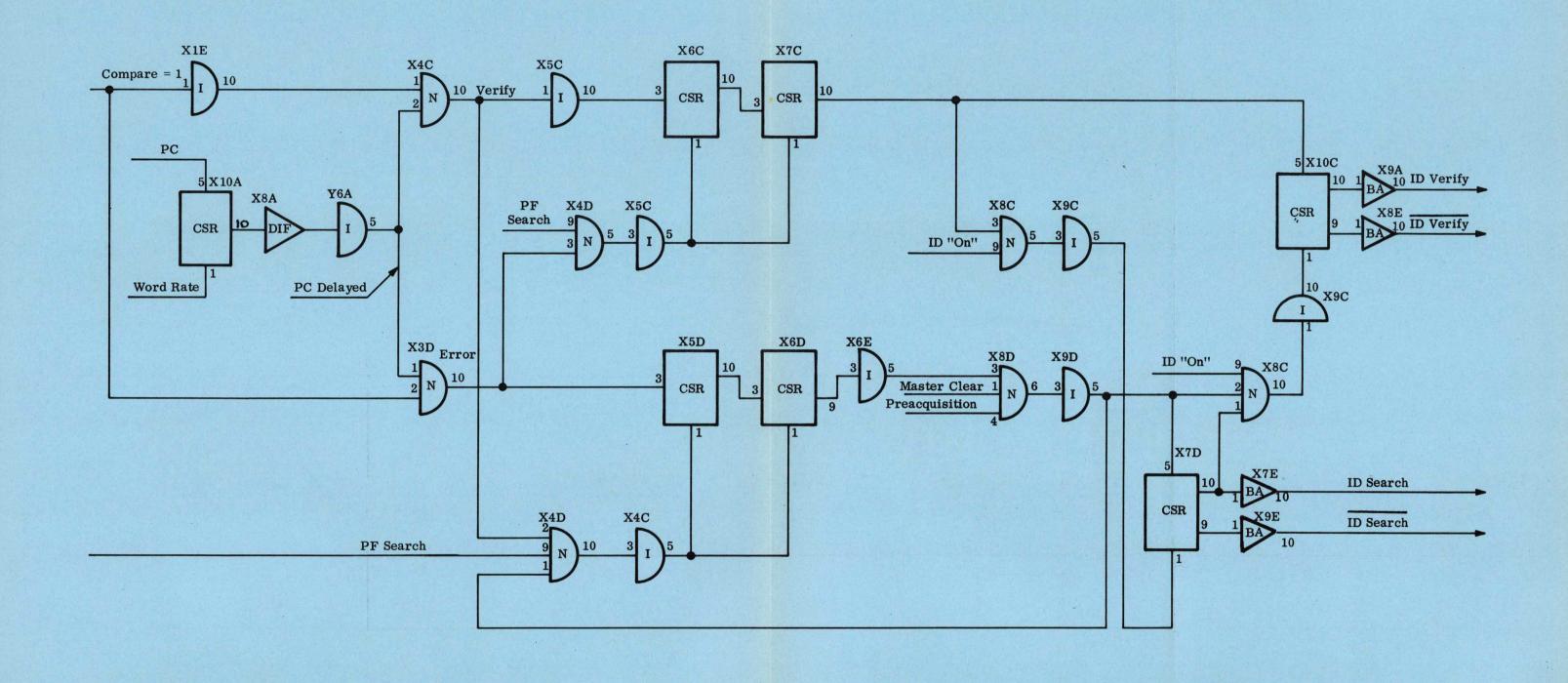


Figure 4-21. Partial Schematic of Comparison Counter

#### SECTION 5

#### STORED PROGRAM PROCESSOR

# 5.1 GENERAL

The stored program processor of the decommutator performs the function of storing the programmed instructions necessary for obtaining PCM synchronization, control and routing, and telemetry processing. The stored program processor can be divided into two basic units as shown in Figure 5-1. The memory unit consists of core storage for retention of the software necessary for operation. The memory control unit consist of decode logic and control logic necessary to maintain the memory software in sequential steps with the PCM data being input to the decommutator. The memory control also obtains the interfacing logic necessary to provide instructions and control to the remainder of the decommutator.

Section 5 will present a functional description of the control section of the stored program processor and its operation in relation to the remainder of the decommutator. Section 5A will contain a functional description of the memory unit of the stored program processor and, in addition, will present a description on Indiana General logic.

# 5.2 MEMORY CONTROL

The memory control section contains the logic necessary to control the timing of functions to be performed by the decommutator. These functions may be logically grouped under one of two operating modes, preacquisition mode and decommutation mode. Both operating modes utilize instruction words stored in the memory core. However, the type of instruction words used and the function derived therefrom are significantly different for the two modes. The loading of memory core is accomplished prior to initiating either of the operating modes. The loading operation is discussed later.

Table 5-1 indicates the contents of memory core after loading. Four types of instruction words are stored in the memory core (see programming Section 9):

- a. Preacquisition Words.
- b. Control and Routing (C&R) Words.
- c. ID Words.
- d. Second Access Words.

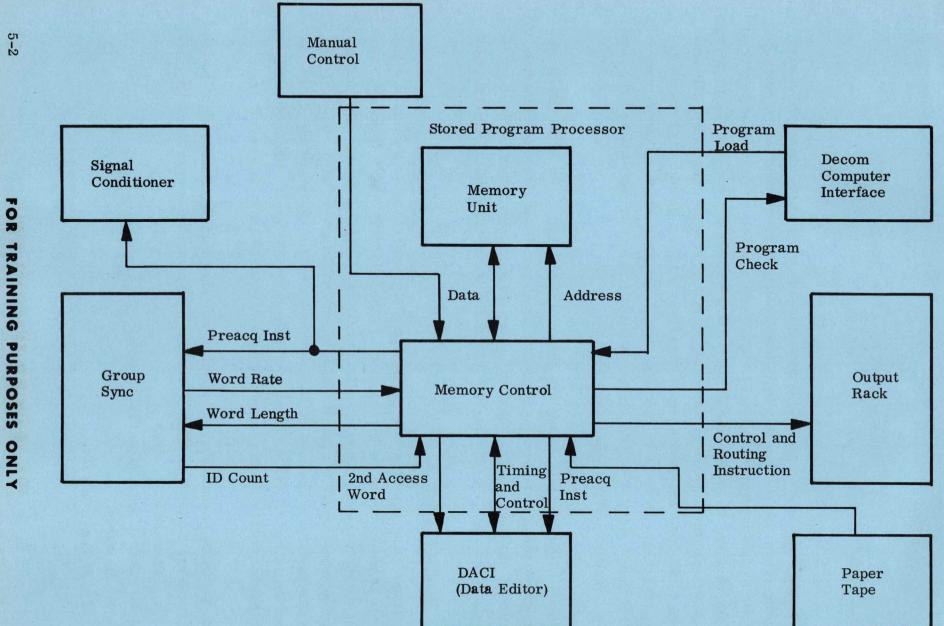


Figure 5-1. Stored Program Processor Interconnection

Table 5-1
Memory Contents

Last	17770	Sequence 0 Preacquisition Word for Program No. 8	
Eight	17771	Sequence 0 Preacquisition Word for Program No. 1	
Memory	17772	Sequence 0 Preacquisition Word for Program No. 2	
Locations	17773	Sequence 0 Preacquisition Word for Program No. 3	
	17774	Sequence 0 Preacquisition Word for Program No. 4	
	17775	Sequence 0 Preacquisition Word for Program No. 5	
	17776	Sequence 0 Preacquisition Word for Program No. 6	
	17777	Sequence 0 Preacquisition Word for Program No. 7	
One Section Preacquisition		Sequence 1 - Sequence 31 Preacquisition Words	
Per Program	Block		
One Section	Block 0	Control and Routing Instructions for Highest Sample Rate Words	
Don Duomno	-1 1		
Per Program	Block 1	Control and Routing Instructions for Next Highest Sample Rate Words	
Per Program	Block 1 Block 2	Control and Routing Instructions for Next Highest Sample Rate Words  Control and Routing Instructions for Next Highest Sample Rate Words	
Per Program			
Per Program	Block 2	Control and Routing Instructions for Next Highest Sample Rate Words	

The preacquisition words are utilized to initialize the decommutator in preparation for decommutating the incoming data stream. The Sequence 0 preacquisition words are stored in the last eight memory core slots, while Sequence 1 through Sequence 31 preacquisition words are stored in the preacquisition block. The unit is capable of storing up to eight decommutating programs, depending upon the storage requirements per program. If program storage requirements are such that more than one program can be stored in the core, each program will occupy a particular section of the blocks shown in Table 5-1. The Sequence 1 through Sequence 30 preacquisition words may be stored in any order desired, but these words will be accessed in the same order they are stored. The Sequence 31 word must be the last word in the preacquisition block. In the discussion which follows, it is assumed that these words were stored in ascending sequence number order (i.e., Sequence 1 first, Sequence 2 second, etc.). The format for the preacquisition words is shown in Section 9.

The Sequence 0 contains the program starting address, which will be used to address memory for accessing the Sequence 1 word in the selected program. The program starting address will then be incremented and used to access the Sequence 2 word, etc., until all the preacquisition words for this program have been accessed and used. If a different program number had been selected, the Sequence 0 word would have provided a different starting address, which would have directed the control section to a different portion of the memory block to access Sequence 1 through Sequence 31 words. The program starting address would, however, have been incremented in the same manner as above to provide subsequent memory access addresses. The contents of Sequence 1 through Sequence 5 preacquisition words are stored in storage registers within the group synchronizer. These contents are later used in establishing prime frame synchronization and in defining ID operation. The Sequence 6 through Sequence 20 preacquisition words are not normally used by the ACE-S/C system, and, therefore, would not normally be stored in the preacquisition block. However, Sequence 11 and Sequence 16 words may, on occasion, be coded with all zeros and stored in the preacquisition block to insure that these functions are not performed. If this were the case, these two words would occupy the two memory slots immediately following the slot containing Sequence 5.

The Sequence 29 through Sequence 31 words contain information used to initialize the block counters, which provide memory access addresses during the Decom mode. These are discussed in greater detail below. Referring again to Table 5-1, Blocks 0 through 4 contain the C&R instructions to be used during the Decom mode. The purpose

and use of these words are discussed under the decom mode operating theory. The contents of Blocks 0 to 4 are completely arbitrary in the sense that sample rate does not dictate which block will contain which particular sample rate C&R words. The example shown in Table 5-1 was chosen, since it appears to be the most logical assignment.

The initial operating conditions of the stored program processor as explained in the previous paragraphs enable the decommutator to obtain the frame synchronization needed to ultimately put the memory program in sequential step with the input data. The auxiliary counter, Figure 5-2, performs the sequential addressing of the memory to unload the preacquisition block. Each sequence is unloaded and transferred into the memory auxiliary register for distribution to the remainder of the decommutator.

The block counters are jammed to the starting addresses that are called out during the preacquisition sequence. These block counters furnish the sequential addressing for memory operation during the acquisition and decommutation modes of operation. The control of the counters are determined by the block address control which decodes the information obtained from the memory auxiliary register.

The acquisition mode timing supplies the step-by-step operations needed to get the stored program processor in sequence with the input data. The ID full adder causes the memory address, to be updated, to be coincident with the frame data so the sub-commutation counters can be jammed to the proper frame address by the ID instruction block. The signal conditioner format select block decodes the information contained in the preacquisition block and places the PCM signal conditioner in the proper format for the selected decommutator program.

The program select block contains the program number of one of the eight programs capable of being used.

The memory timing and control is used to maintain the memory core, the memory control, and the group synchronizer in sequential operation during all modes of operation.

The program control drawer provides the manual control of the stored program processor needed for certain maintenance and operational requirements. The tape and computer format control provide the interface and timing needed to load the decommutator

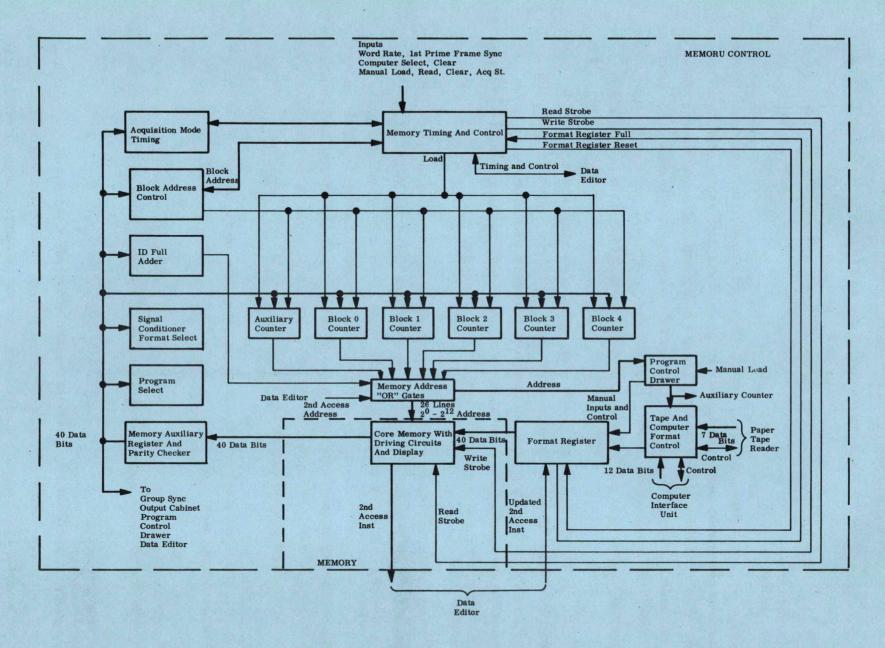


Figure 5-2. Stored Program Processor

from the paper tape reader and/or the computer. The input/output to the decom/computer interface allows the loading and checking of decommutator programs under the control of the downlink 160G computer.

The input/output functions of the DACI (data editor) provide second access instructions to the DACI, write back from the DACI, and timing and control needed to initiate and control the various memory cycles and memory advancing needed in the telemetry data processing.

The core memory and the driving circuits are discussed in Section 5A.

The step-by-step sequence of operation discussed in subsequent paragraphs will be based on the operation of the decommutator without the direct access computer interface unit enable. For this operation, refer to Section 10.

# 5.3 PROGRAM CONTROL, CONTROLS, AND INDICATORS

The controls and indicators for control and monitoring of the system and memory operation are located on program control drawer assembly 2A2, Figure 5-3. Table 5-2 contains a listing of the controls and indicators and their function.

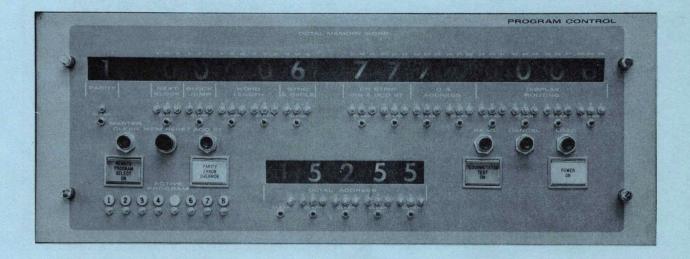


Figure 5-3. Program Control Drawer 2A2 Front Panel

Table 5-2
Program Control, Controls and Indicators

Control/Indicator	Function
POWER ON pushbutton switch and indicator (white)	Turns on system power when pressed once; turns off power when pressed a second time.
DECOMMUTATOR TEST ON pushbutton switch-indicator	Locks out the bit synchronizer and turns on the PCM signal simulator so that a known serial train of data can be applied as a system input for test purposes.
REMOTE PROGRAM SELECT ON pushbutton switch-indicator	Allows the digital computer to load a new program into memory.
PARITY ERROR OVERRIDE push- button switch-indicator	Prevents the detection of parity errors for memory.
MASTER CLEAR	Resets counter stages and storage registers throughout the stored program decommutator.
MEM RESET	Closes memory protection relay when power is turned on.
ACQ ST pushbutton switch	Starts the memory program for pre- acquisition program loading and decom- mutation.
LOAD pushbutton switch	Enters routing instructions part (all digits to the right of SYNC and CYCLE digit) of displayed word into memory.  LOAD indicator lights in display panel.
CANCEL pushbutton switch	Removes word from display panel and does not send it to memory.
READ pushbutton switch	Displays memory location accessed. READ indicator appears in display.
ACTIVE PROGRAM pushbutton switches and indicators	Switches select one of eight programs in memory to be used for decommutation. Indicators display the program used.
OCTAL ADDRESS pushbutton switches	Address selection switches for read or load operation. Arranged in five octaves for a maximum address count of 17777. CLEAR pushbutton switches reset the storage register associated with the octaves.
OCTAL ADDRESS DISPLAY	Displays the octal address selected for read or load operation.

Table 5-2
Program Control, Controls and Indicators (Cont.)

Control/Indicator	Function
OCTAL MEMORY WORD pushbutton switches	Used for the formation of memory word manual entries. Arranged in 14 octaves; each octave controls the selection of the bit configuration for the word portion specified by the legend. CLEAR switches reset the storages associated with the octaves.
OCTAL MEMORY WORD DISPLAY	
PARITY (bit 1)	Displays the parity bit value for word loaded or read.
NEXT BLOCK (bits 2-4)	Displays the value (up to 7) of the next block information loaded or read.
BLOCK JUMP (bits 5-7)	Displays the value (up to 7) of the block jump information loaded or read.
WORD LENGTH (bits 8-13)	Two octal digits that display the length of word (from 4 to 64 bits) to be decommutated. All zeros denote a word length of 64 bits.
SYNC and CYCLE (bits 14-16)	Displays ID sync and recycle information provided to the group synchronizer.
CH STRIP BIN and BCD ST (bits 17-22)	Two octal digits to designate the dumping of the word into a specified binary store, through a translator to a specified BCD store, and/or a unitary code signifying the word is to be used by some auxiliary device. The MSB may be used to select either binary or BCD storage. The LSB may be used to select only binary storage.
D/A ADDRESS (bits 23-28)	Two octal digits to signify which D/A will be used to decode the data word.
DISPLAY ROUTING (bits 29-40)	Four octal digits to designate which output device will receive incoming data word.

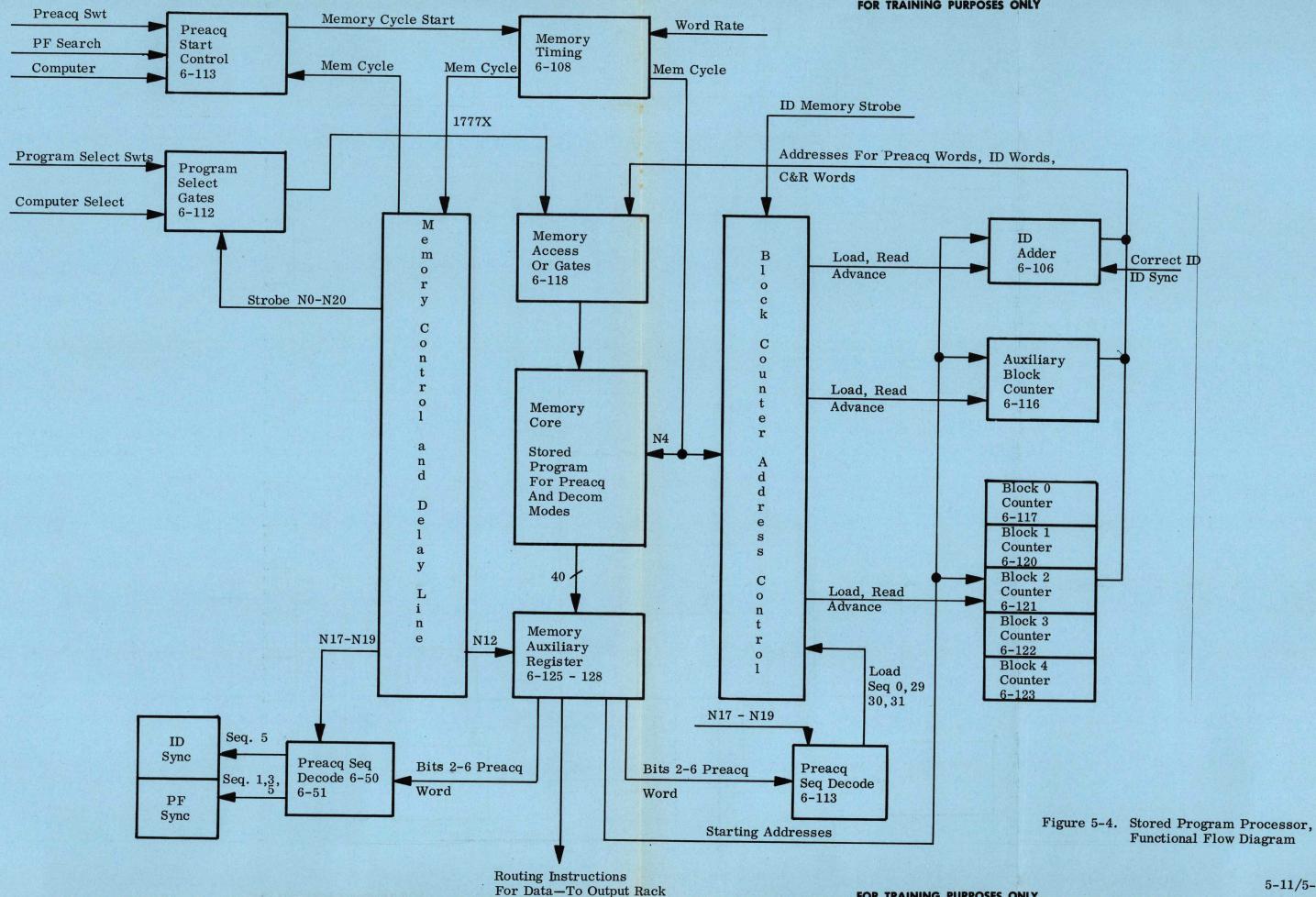
# 5.4 PREACQUISITION MODE

A simplified block diagram illustrating memory control functions performed during the preacquisition mode is shown in Figure 5-4. The preacquisition mode is initiated in one of three ways:

- a. Depressing the ACQ ST and PROGRAM NUMBER Select switches.
- b. Remote (computer) program selection.
- c. Receiving a prime frame search pulse, whenever prime frame synchronization is lost.

Depressing the ACQ ST pushbutton (or remotely selecting a program) initiates the first memory cycle trigger and enables the simulated word rate generator. This circuitry provides memory cycles at a simulated word rate of approximately 5 microseconds during the preacquisition mode. Depressing a PROGRAM NUMBER select switch (or remotely selecting a program number) completes the initiation at the preacquisition mode. The program select gates decode the program number selected and provide the least significant octave (LSO) of a memory address. The remainder of this memory address is furnished as a strobe pulse to the AND gates from the ACQ ST logic and provide all logic ones for the four most significant octaves (MSO) in the memory address. The complete address is therefore one of the last eight memory address slots in core. From Table 5-1, these slots are seen to contain the Sequence 0 preacquisition words associated with the eight programs. This memory address is gated through the memory OR gates to memory and accessed during the first memory cycle. The contents of the accessed slot (Sequence 0 word) are brought to the memory auxiliary register.

The contents of the memory auxiliary register are made available to various circuits in the decommutator unit. It is seen that particular logic functions must be satisfied, however, before these circuits may be utilized. These logic functions follow a particular order of implementation, depending upon the preacquisition block program coding. The first function performed, however, must always be associated with a Sequence 0 word, and the last function with a Sequence 31 word. Memory bits M2 to M6 in the memory auxiliary register are made available to the memory control sequence decoder and the group sync sequence decoder. The memory control sequence decoder is capable of decoding only Sequences 0, 29, 30, and 31 and will therefore perform those functions associated with these preacquisition words. The group sync sequence decoder is capable of decoding only Sequences 1, 2, 3, 4, 5, and 6 and will therefore perform those functions associated with these preacquisition words.



Upon decoding a Sequence 0 code, the memory control sequence decoder generates a Sequence 0 load pulse, which is applied to the auxiliary counter. This pulse allows the auxiliary counter to be loaded with memory bits M28 to M40 of the same preacquisition word (Sequence 0) from the memory auxiliary register. These bits are the program starting address (in the preacquisition block) for the selected program. The memory cycle trigger that initiated this memory cycle was applied to a 24-stage delay line which divides the memory cycle into 25 equal time periods, N0 through N24. At N0 time and N19 time during each memory cycle, an ADDRESS STROBE flip-flop changes state. Its output triggers the AUX CTR READ/INCR CONTROL logic. At time N0, the read gates in the auxiliary counter are enabled; while at time N19, the auxiliary counter is incremented to provide the memory access address for the next instruction in the preacquisition block. During the first memory cycle, the auxiliary counter is loaded at time N17. At time N0 of the next memory cycle, the contents (program starting address) are gated to the memory OR gates. The counter is then incremented at time N19.

Gating of the program starting address to memory accesses the first memory address slot (in the preacquisition block) associated with this program. The contents of the first memory slot for this program are brought to the memory auxiliary register (Figure 5-5). Memory bits M2 to M6 are received at the group sync sequence decoder (and the memory control sequence decoder, which is not capable of decoding Sequence 1) where Sequence 1 is decoded and a Sequence 1 load pulse is generated. This load pulse allows the first half of the prime pattern storage to be loaded with memory bits M7 to M38 of the preacquisition word (Sequence 1) from the memory auxiliary register. The auxiliary counter is again incremented at time N19 in this memory cycle.

The memory control section continues operating in this manner, accessing the instruction words in the preacquisition block by using the incrementing address in the auxiliary counter, and loading the appropriate group synchronizer storages from these words, until the contents of the Sequence 5 preacquisition word have been stored in the group synchronizer storages. The group synchronizer has thus been completely initialized to perform the synchronization function when the decom mode is entered. It is still essential, however, to synchronize the memory control section with the data stream. This is necessary so that the appropriate C&R word is accessed at the proper time in the decom mode. This synchronizing process will be accomplished during the decom mode, but requires information from the preacquisition block. It is thus necessary to access these preacquisition words during the preacquisition mode and

store the needed information. This information is contained in the Sequence 29 through Sequence 31 preacquisition words.

The point in a major cycle at which prime frame sync will be established is not known (i.e., prime frame sync could be established during any prime frame). To completely establish synchronization with the data stream, it is therefore necessary to determine which prime frame is being examined when sync occurs. The location of this prime frame within a major cycle is provided by the ID synchronizer. The ID synchronizer extracts the first ID word in the data train (after 1st prime frame sync) and updates this word each subsequent prime frame. The ID word in the data train contains a number which indicates the particular prime frame of data in which that word is contained. The ID counter starting address, contained in the Sequence 29 word, will be summed with the updated ID word from the ID synchronizer to provide an ID block (Block 5) address. This address will be used to access an instruction that will force the block counters to the proper point in the program for memory control synchronization with the data train. The synchronizing function is performed during the decom mode, but the ID counter starting address must be stored during the preacquisition mode.

At time N0 of the next memory cycle, following the Sequence 5 cycle, the seventh preacquisition word is accessed and brought to the memory auxiliary register. Since word sync and subframe sync are not used by the ACE-S/C system, the seventh preacquisition word (Figure 5-5) then becomes the Sequence 29 word. The Sequence code M2 -M6 is received at the memory control sequence decoder (and at the group sync sequence decoder, which is unable to decode Sequence 29), where it is decoded and a Sequence 29 load pulse is generated. This pulse allows the ID adder storage to be loaded with memory bits M15-M40 of the preacquisition word (Sequence 29) from the memory auxiliary register. The bits loaded into ID adder storage consist of a constant which, when summed with the incoming ID word, results in a memory address used to obtain the memory control section-data train synchronization. This is discussed in more detail in subsequent paragraphs. The bits loaded into the block 0 storage consist of the block 0 starting address corresponding to first prime frame, used in the decom mode. At N19 time of this memory cycle, the auxiliary counter is again incremented and the BLOCK 0 counter is loaded from the block 0 storage.

The auxiliary counter is gated to memory at N0 time of the following memory cycle, and the next preacquisition word, Sequence 30, is accessed and brought to the memory

Figure 5-5. Preacquisition Word Format

auxiliary register. Sequence 30 is decoded at the memory control sequence decoder, and a Sequence 30 load pulse is generated. This pulse allows the block 1 and block 2 storages to be loaded with memory bits M15-M27 and M28-M40, respectively, of the Sequence 30 preacquisition word from the memory auxiliary register. These bits are the starting addresses for Blocks 1 and 2, corresponding to first prime frame. At time N19 of this memory cycle, the auxiliary counter is incremented and the Block 1 and Block 2 counters are loaded from their respective Block 1 and Block 2 storages.

The auxiliary counter is again gated to memory at N0 time at the following memory cycle, and the Sequence 31 preacquisition word is brought to the memory auxiliary register. Sequence 31 is decoded and a Sequence 31 load pulse is generated, allowing memory bits M15-M27 and M28-M40 to be loaded into the Block 3 and Block 4 storages respectively. These bits are the starting addresses for Blocks 3 and 4, corresponding to first prime frame. At N19 time the Block 3 and Block 4 counters are loaded from the Block 3 and Block 4 storages respectively.

At this point it might be thought that the preacquisition mode is complete. This is not the case, however, since the memory, when operating in the decom mode, must remain one step ahead of the incoming data stream. That is, the control and routing instruction for the next data word must be accessed <u>prior</u> to receiving the next data word. To accomplish this, two additional memory cycles must be initiated. The first is used to access the control and routing instruction for the prime frame sync word. This word is accessed, at this time, solely to obtain the Next Block code contained in memory bits M2 to M4 of the instruction. The Next Block code allows the second additional cycle to access the control and routing instruction for the first word following the prime frame sync word in the data train. This second C&R word must be accessed at this time so that, when prime frame synchronization is achieved at the <u>end</u> of the prime frame sync word, the control and routing information for the incoming data word is known. Figure 5-6 depicts this timing.

The Sequence 31 load pulse is used to enable the two-cycle control logic (sheet 3A2L). At N22 time of the Sequence 31 memory cycle, an address strobe is generated and sent to the next block selector. This pulse is also used to disable the auxiliary counter read gates and reset the memory auxiliary register to zeros. At N0 time of the next memory cycle, the next block decoder decodes NEXT BLOCK 0 (since the memory auxiliary register was reset) and the next block selector selects Block 0. Selection of Block 0 enables the Block 0 counter read gates, allowing the contents of the Block 0 counter to

Figure 5-6. Mode/Function Timing Diagram

be gated to memory. This address is the Block 0 starting address, which contains the control and routing instruction for the prime frame sync word. This instruction is brought to the memory auxiliary register during the Sequence 31+1 memory cycle. At time N20 of this cycle, a count pulse is generated and sent to the two-stage counter (sheet 3A2L). At the trailing edge of the N20 pulse, the Block 0 counter is incremented. The NEXT BLOCK code, M2-M4, is received at the next block decoder from the memory auxiliary register. This is decoded and routed to the next block selector, which enables the read gates for the block counter selected at time N0 of the next memory cycle.

The selected block counter contents are gated to memory, accessed, and brought to the memory auxiliary register. The accessed slot contains the control and routing instruction for the first word in the data train following the prime frame sync word. At time N20 of this memory cycle (Sequence 31+2), a count pulse is generated and sent to the two-stage counter. The counter, which now contains two, generates a disable pulse which resets the ACQ ST logic which, in turn, disables the simulated word rate generator. The memory control section has been initialized under the assumption that synchronization will be achieved during prime frame number one (all block counters have been loaded with their starting address). This is not necessarily the case, however, and one of the functions of the Decom mode will be to force the Block Counters 1 through 4 to the address corresponding to the particular prime frame in which synchronization was achieved. If this occurs during prime frame number one, no forcing will be necessary, but the starting addresses must be stored in order that the block counters may be recycled to their starting addresses each major cycle. The memory control section now becomes inactive until prime frame synchronization is achieved. at which point it automatically enters the Decom mode. Between the end of the preacquisition mode and initiation of the Decom mode, the group synchronizer operates in the prime frame SEARCH mode.

### 5.5 DECOM MODE

In the Decom mode discussion it is necessary to make certain assumptions regarding the incoming data train. Here, it was assumed that data is received at the 204.8-kc rate, that the first word in the prime frame is a 32-bit prime frame sync word, and that the ID word will occupy a particular word slot in the data train, but <u>not</u> the word slot immediately following the prime frame sync word. The Mode/Function timing diagram of Figure 5-6 indicates the functions to be performed during the Decom mode and the times during which these functions are performed, as related to the incoming data

train. As indicated in this figure, the decommutating unit will also perform processing functions simultaneously with the memory control functions. A simplified block diagram depicting these functions is shown in Figure 5-7. From the Mode Function timing diagram it is seen that the memory control section will perform the function of accessing the C&R words. When these words are accessed, they are decoded and used to set the processing logic in the output circuitry for the next data word. With the processing logic preset, the next data word is properly processed and routed through the appropriate output circuitry to the external ACE-S/C unit addressed.

The Decom mode is initiated upon detection of the first prime frame sync pulse. (This pulse is also used to initiate the Group Synchronizer Check mode). In the discussion which follows it must be kept in mind that the first prime frame sync pulse occurs after the first favorable correlation between the prime frame sync word and the stored prime frame sync pattern. This may occur during any particular prime frame in the data train and not necessarily during the first prime frame. It thus becomes apparent that some means must be provided to force the block counters to a particular address in order that the program may be entered at the proper point in relation to the incoming data train. This is a secondary function performed by the memory control section and occurs only while establishing synchronization. To perform the functions mentioned above, two types of instructions are used. The first, the Control and Routing C&R instruction word, is used to:

- a. Set the memory control logic in order to access the next instruction word.
- b. Set the processing logic in order to process the next data word. This, the ID instruction word, is used to:
  - (1) Set the memory control logic to access the next instruction word.
  - (2) Force the block counters to the proper address in the program.

Table 5-1 indicates where these words are stored in the memory core.

Prior to detecting the first prime frame sync pulse, the memory auxiliary register was loaded with a C&R instruction word (last step during preacquisition mode). This word contains the information associated with processing the first word following the prime frame sync word in the data train. This information is made available to the appropriate processing circuits to set these circuits in preparation for processing that word. The processing circuits are not activated until after the first prime frame sync pulse is generated. In the case where the first word following the prime frame sync word is a subcommutated word, this word may initially be erroneously processed. The first prime frame sync pulse may occur during any particular prime frame, not necessarily prime frame number one, for which the block counters were initialized.

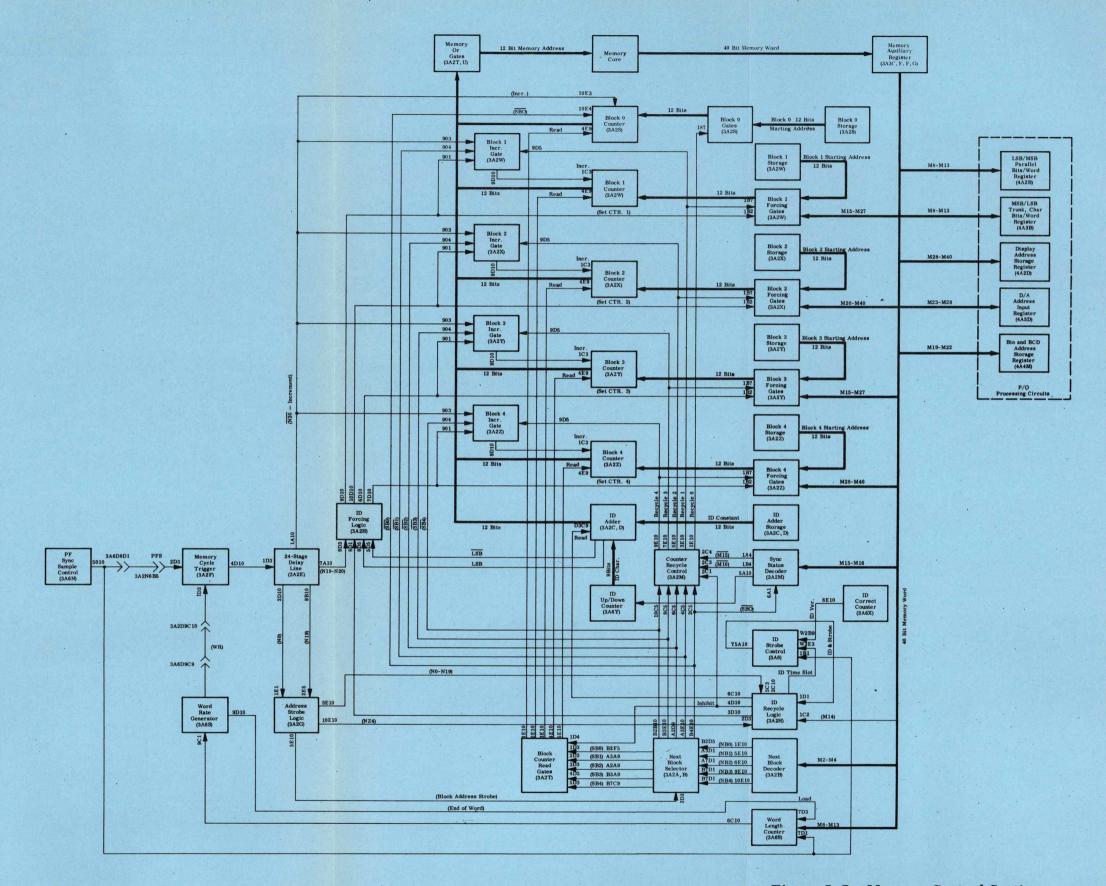


Figure 5-7. Memory Control Section - Decom Mode

14 6

Detection of the first prime frame sync pulse loads the word length counter and initiates the first memory cycle trigger. The word length counter is counted down at bit rate and, upon reaching the count of zero, generates an end-of-word pulse. This pulse is used to trigger the word rate generator. The word rate generator initiates all subsequent memory cycles at the word rate until prime frame sync is lost. At time N0 of this memory cycle, the block address strobe enables the next block selector. (Using the next block code M2-M4 of the C&R word in the memory address register, the next block decoder has set the next block selector.) The next block selector selects the block counter to be read in order to access the next C&R word, and enables the read gate for that block counter. The selected block counter is then read to memory, and the next C&R word is accessed and brought to the memory auxiliary register. At time N20 of this memory cycle, the selected block counter is incremented. Memory bits M2 to M4 of the new C&R word are decoded and set the next block selector logic. The processing logic accepts the memory bits (see Section 9 C&R) of this C&R word from the memory auxiliary register and set their processing circuits accordingly to handle the following data word. When the word length counter reaches zero, its output triggers the word rate generator, initiating a new memory cycle and reloading the word length counter with bits M8 to M12 of the new word in the memory auxiliary register. This process continues until ID verification occurs. The ID verified signal indicates that the ID counter has been loaded and updated and that the ID counter has been twice favorably correlated with the ID word in the data train. This cannot occur until at least two ID words have been processed (two prime frames), since the first ID word would be loaded into the Up/Down counter and first verify is initiated. This counter would then be incremented immediately preceding the second ID word in the data train (and immediately preceding each subsequent ID word in the data train). When the second ID word in the data train is received, it is correlated with the Up/ Down counter (incremented once after being loaded with the first ID word). Assume this correlation is favorable.

If this second correlation is favorable, the ID verified signal is generated. If two consecutive correlations are not achieved, the Up/Down counter is reloaded with the next incoming ID word and the process is repeated.

The first prime frame sync pulse, in addition to initiating the first memory cycle, sets the ID strobe control logic. When ID verification occurs, this logic is enabled. However, the C&R instruction for the ID word is no longer in the memory auxiliary register.

The operation continues as discussed above until the following prime frame. Then the C&R word for the next ID word is accessed, the ID recycle logic is enabled by the M14 bit and generates the ID time slot. This pulse, gated by the ID verified level, generates the ID phase strobe. The ID phase strobe performs two functions:

- a. Resets the ID strobe control logic.
- b. Triggers the ID recycle flip-flop.

The ID recycle flip-flop enables the read pulse generator within the recycle logic, resets the recycle trigger logic, and inhibits the block counter read gates. At N0 time of the next memory cycle (ID word time in the data train), the read pulse generator outputs a read pulse to the ID adder, the contents of which are gated to memory to access the next instruction word. The contents of the ID adder at this time consist of the sum of the ID constant (stored during preacquisition) and the contents of the ID Up/Down counter (equivalent to third ID word in the data train). This sum is the address of a particular instruction in the ID block. Which particular instruction is accessed is dependent upon the Up/Down counter contents, which, in turn, is dependent upon which prime frame the decommutator is examining. (In the foregoing, this was assumed to be the third prime frame.) This bit determines which two of the block counters will be forced. If this bit is a one (indicating the ID word was odd), counters 3 and 4 will be forced; if the bit is a zero (indicating the ID word was even), counters 1 and 2 will be forced. At time N19 of this cycle, the ID forcing logic generates the enabling pulses for two of the block counter forcing gates. Bits M28 to M40 of the ID instruction (Section 9) in the memory auxiliary register are gated to these two block counters, forcing the counters to the proper count for synchronization with the data train. At time N24 of this cycle, the ID recycle flip-flop is reset. Bits M2 to M4 are decoded, setting memory control logic to access the next C&R word. The memory control logic now continues accessing C&R words, while the processing section processes data during the remainder of this prime frame and until the next C&R word is accessed for the next ID word. When this C&R word is brought to the memory auxiliary register, bit M14 generates the ID time slot used to trigger the ID recycle flip-flop a second time. The above forcing process takes place a second time in the same manner, with two exceptions. The LSB from the ID Up/Down counter is now opposite from the previous LSB bit used, thus selecting the other two forcing gates and forcing the second two block counters to the proper count for synchronization with the data train. The recycle flip-flop output now sets the trigger logic such that forcing logic enable pulses and ID adder read pulses will not be generated by decoding a

logic one in bit M14, unless prime frame sync is lost, in which case the preacquisition mode is re-initiated and the entire process is repeated.

In order for the block counters to remain in step with the data train, they must be incremented at the proper time and periodically recycled to their starting addresses. Each block counter has an associated incrementing gate. The block zero counter is incremented at time N20, if the block zero counter was selected by decoding the NEXT BLOCK code of the C&R instruction accessed during this memory cycle. The remaining block counters are incremented at time N20 of the memory cycle only under the following conditions:

- a. This block counter was selected by decoding the NEXT BLOCK code of the C&R instruction accessed during this memory cycle.
- b. An ID forcing logic gate pulse was not generated this memory cycle.
- c. This counter was <u>not</u> selected for recycling to its starting address during this memory cycle.

The block counters are recycled to their starting address whenever the C&R instructions for that block have all been accessed. The period for the block counters thus becomes a function of the sample rate associated with the instructions in that block. Referring to Table 5-1, it will be seen that the Block 0 counter will have the shortest period (highest recycle rate), while the Block 4 counter will have the longest period (slowest recycle rate) for the example illustrated. Recycling the counters occurs upon decoding the recycle code in bits M15 to M16 of the C&R word in the memory auxiliary register. These bits will contain the proper code for recycling whenever the last C&R instruction word in that block has been accessed. Memory bits M2 to M4 of this word are also decoded, and this block is selected for recycling. The detection of the selected block pulse and the recycle code at the counter recycle control generates an enable pulse to the selected forcing gates and allows the starting address (stored during preacquisition) to be gated into the selected block counter. The remainder of this C&R word is executed by the appropriate processing and control circuits. The unit continues to operate in the Decom mode until prime frame sync is lost. If prime frame sync is lost, the unit reverts to the pre-acquisition mode and repeats the entire process.

# 5.6 PROGRAM LOADING AND CHECKING

The decommutator can be loaded from three sources—the manual pushbutton switches or the front of program control drawer (2A2), the decommutator paper tape, and the

downlink computer. The downlink computer is the only unit that is capable of checking the loaded program; however, manual callup can be made from memory control drawer 2A2.

Program loading can be accomplished during the decommutation mode if the incoming word length is of sufficient time to allow two memory cycles to be completed, one cycle for the C&R word and one for program loading. Although loading can be done by the computer during operations, it is normally not done because of the method of transfer to the computer (discussed in the decom/computer interface section).

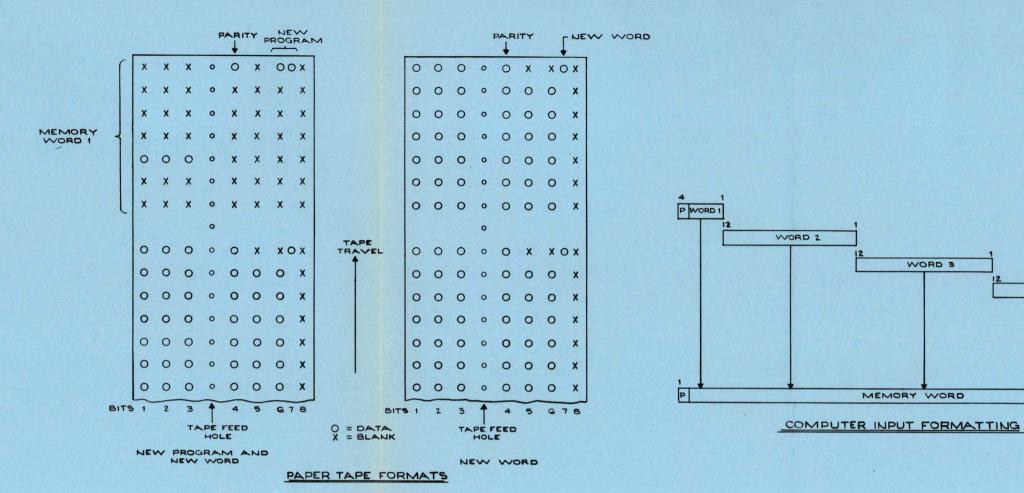
#### 5.6.1 PAPER TAPE AND COMPUTER LAYOUT FORMATTING

The paper tape reader is basically a seven level system which transfers six-bit words to the decom format register. The tape format is depicted in Figure 5-8. The tape logic recognizes bits six and seven as indication that a new program is to be loaded. The remainder of the first tape memory word defines the program starting address and loads the program beginning at this location. As shown in Figure 5-8, when a single bit is recognized in bits six and seven, this defines a new word in the loading sequence and will update the memory to the next sequential memory location. The tape input transfer to the format register is performed in seven segments (Figure 5-8). Word one contains parity plus three bits of the data. The transfer of the remaining six tape words are made by detection of the tape feed holes. After detecting that seven tape word transfers have been made to the format register, a format full pulse initiates the transfer to memory.

The computer transfers four 12-bit computer words to the decommutator when loading in a specific location. The transfer sequence shown in Figure 5-8 is a 4-bit word including the parity bit and three 12-bit words thereafter. At the end of the four word transfer, the decom generates a format register full pulse and initiates a transfer to memory.

## 5.6.2 MANUAL LOADING

The 40 pushbutton switches located on the 2A2 memory control panel allow for the individual controlling of each bit set into memory. After the proper selection has been made, the data register (Figure 5-9) of the control drawer contains the 40-bit word to be transferred to memory. The transfer is accomplished by depressing the manual load enable pushbutton, which loads the format register and generates a format full



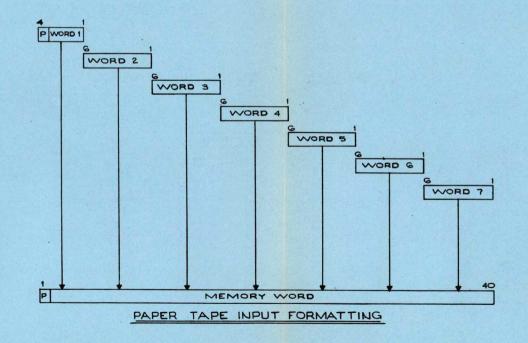


Figure 5-8. Computer and Tape Word Formats

WORD 4

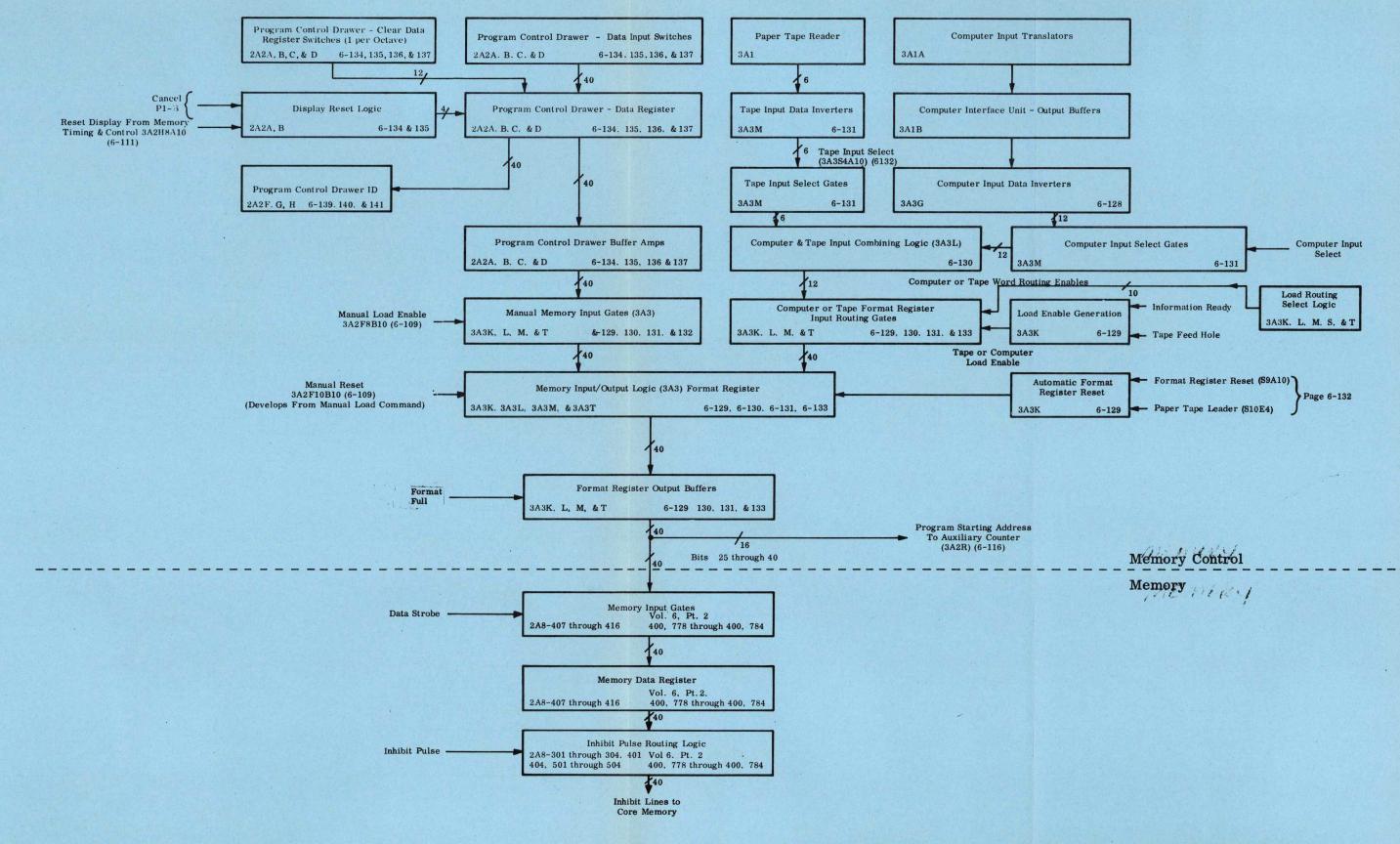


Figure 5-9. Functional Block Diagram, Decom Memory Load Logic

pulse. This full pulse initiates a memory cycle and transfers the information into the addressed memory location.

#### 5.6.3 PAPER TAPE LOADING

When the paper tape reader is initiated, this enables the logic pertaining to tape input operations and inhibits all logic related to computer input data. As the tape runs forward, 6-bit words are transferred through the tape input select gates to the computer and tape input combining logic (Figure 5-9). The tape feed holes are counted by the load enable generation logic and selects the proper input routing gates for proper loading into the format register. After seven tape words have been transferred, a format full pulse is automatically generated allowing transfer of the data word to the memory input gates. If the word is the program starting address, an output is made to the auxiliary counter to define the initial loading location. Thereafter, on each transfer, the auxiliary counter is updated to the next sequential location in memory.

### 5.6.4 COMPUTER LOADING

When loading is to be performed by the computer via the decom/computer interface, a select code (external function code) is generated by the computer, decoded by the interface, and enabled by the computer input gates (Figure 5-9). This select code is 3 X 0 2. The computer then transfers the first 12-bit word; however, the computer and tape format register input routing gates only allow four bits to be loaded into the register. The input routing gates are enabled by the load enable generation logic which counts the number of information ready signals from the computer to select the proper gating logic. After four information ready signals are received, a format full pulse is generated and the 40-bit word transferred to memory at the addressed location. This sequence continues until a total program is loaded.

#### 5.6.5 DACI LOADING

The operation of DACI Loading is given in Section 10.

#### SECTION 5A

#### **MEMORY**

## 5A.1 GENERAL

The decommutator memory (Model 8192 I 42 RS) is a random access, coincident current memory system with a capacity of 8192 x 40 words. Its function is to provide a means of storing program instructions for the decommutator operations and data words used in telemetry data processing.

There are two basic categories of memory operation. One is the reading of information from memory for use by the decom in its decommutation operations. The other is the writing or loading of new data used in data processing and/or control.

Figure 5A-1 gives the memory and decom interconnection. During the read only operations the address for the address register can be obtained from either the auxiliary counter or one of the five block counters.

During a write only operation, the address for the address register can be obtained from either the auxiliary counter or from the DACI address register. The philosophy of operation is to enable the reading or loading of memory during decommutation. The read and write signals from the memory control section define the type of operation when memory is accessed. Read is defined as read/restore, and in this mode, the contents of the core matrix is read into the data register and then restored to the core in the same addressed location. Write is defined as clear/write, and in this mode, the contents of the core matrix is cleared (destroyed) and the new data from the data register is written into the same addressed location.

Thus, the following sequential steps can be made for a read and a write operation.

#### 5A.1.1 READ

- a. An address from the auxiliary counter or block counter is loaded into the address OR gates.
- b. A read strobe initiates the memory timing cycle and loads the register.
- c. The core matrix is enabled by the contents of the address register and via the memory timing the data is read into the data register.
- d. Timing initiates a restore operation and loads the data back into the addressed cores.

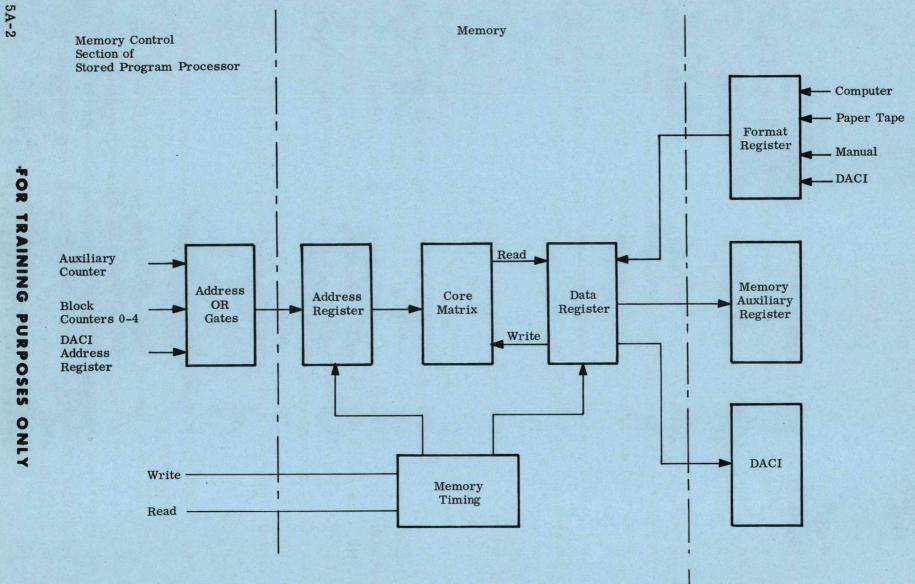


Figure 5A-1. Memory/Decom Interconnection

e. The memory cycle is complete, and the data in the data register is transferred to the using sections of the decom.

#### 5A.1.2 WRITE

- a. An address from the auxiliary counter or DACI address register is loaded into the address OR gates.
- b. A write strobe initiates the memory timing cycle and loads the address register.
- c. The core matrix is enabled by the contents of the address register.
- d. Memory timing clears the core matrix by preventing the contents of the core from being loaded into the data register and allows the contents of format register to load the data register.
- e. Timing initiates a write (basically a restore) strobe and loads the contents of the data register into the addressed memory core matrix.
- f. The memory cycle is complete and either another read or write cycle can take place.

# 5A.2 CORE MATRIX

The memory section of the decom is composed of an array of permanent or semipermanent storage devices as its primary element. In modern memories, this device
is generally the ferrite core. The ferrite core has the capability of retaining information in one of two magnetic states, making it capable of storing one bit (binary digit)
of information (see Figure 5A-2A). The magnetic properties of the core allow it to
maintain a magnetic state without the application of power (see Figure 5A-2C) and enable this state to be changed upon the application of a magnetic field of the proper intensity and direction. The core can be switched from one magnetic state to the other
very rapidly, in a matter of microseconds. Since the cores are small in size (30 mils
or so in outside diameter), a memory containing 100,000 cores or more can be built
into a package not much larger than a textbook.

A common configuration for a core memory has 4096 cores mounted in a 64 by 64 matrix on each of a number of planes; the number of planes will be equal to the number of bits (length) of the word to be stored. Each plane stores one bit of the data word in any one of 4096 locations, as determined by the address associated with that data word. A memory composed of 40 planes of 4096 cores each then could store 4096 40-bit data words. The complete memory for the decom is made up of two of these banks of memory (the remaining discussion is based upon a bank of 4096 cores).

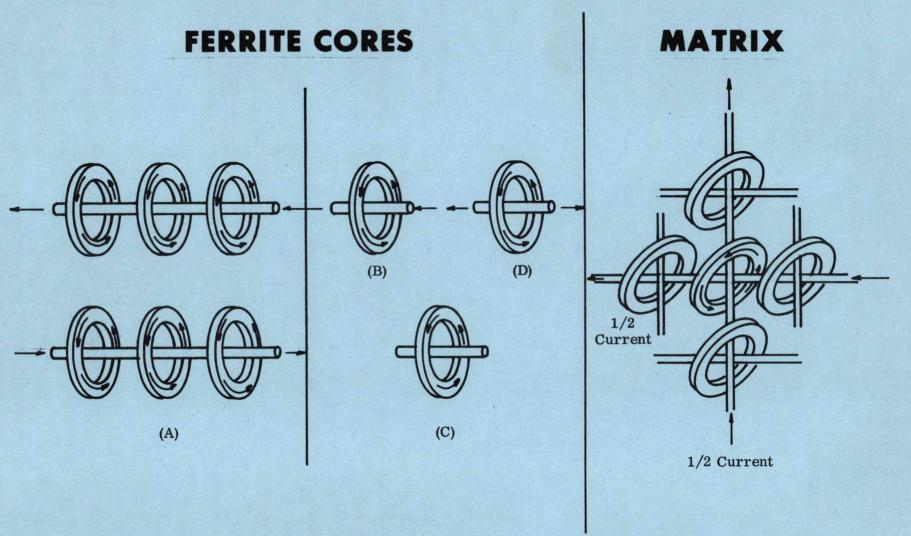


Figure 5A-2. Memory Section

Each core is threaded by five wires (Figure 5A-3): a horizontal drive line, a vertical drive line, a sense line, and two inhibit lines. For each plane of the memory described there are 64 horizontal drive lines, each threading 64 cores; 64 vertical drive lines, each threading 64 cores; a single sense line, threading all 4096 cores; and two inhibit lines threading all 4096 cores. To complete the wiring of the memory, the corresponding horizontal drive lines of each plane are connected together in series electrically, and the corresponding vertical drive lines of each plane are connected together in series.

A given memory address, specifying a single core in each of the 40 planes, is selected by translation of the output of the address register to select one horizontal drive line and one vertical drive line. Only one core in each plane threaded by the selected horizontal and vertical drive lines and is, therefore, the core selected by that memory address. When information is to be stored in memory or read out of memory, a half current (a current having only approximately one-half the amplitude required to switch a core) is applied to the selected drive lines.

All the cores that are threaded by only one of these wires will be disturbed by a current that is not sufficiently large to switch the cores, while the single core on each plane that is threaded by both of these wires will be disturbed by a current that is of sufficient amplitude to switch the magnetic state of the core.

During the readout of information from the memory, the magnetic state of each of the selected cores is switched to the zero state. If the selected core was initially in the zero state, it remains in that state and virtually no voltage is induced in the sense line. Therefore, by examining the sense line at an appropriate time after the drive lines are energized, it can be determined whether the selected core contains a zero or a one. The voltage pulses on the sense lines are amplified, shaped into standard logic pulses, and gated into a data register from which they are transmitted to the other sections of the decom as needed. This method of reading the information from a core memory is known as destructive readout.

In a memory with destructive readout, the circuitry associated with the memory automatically takes the word from the data register after readout and restores it in the selected cores in memory during the write portion of the memory reference. During the write operation, the direction of current through the selected horizontal and vertical drive lines is in a direction opposite to that during the read operation. Thus, the selected core on each plane will be set to a one state unless an inhibit current equal to

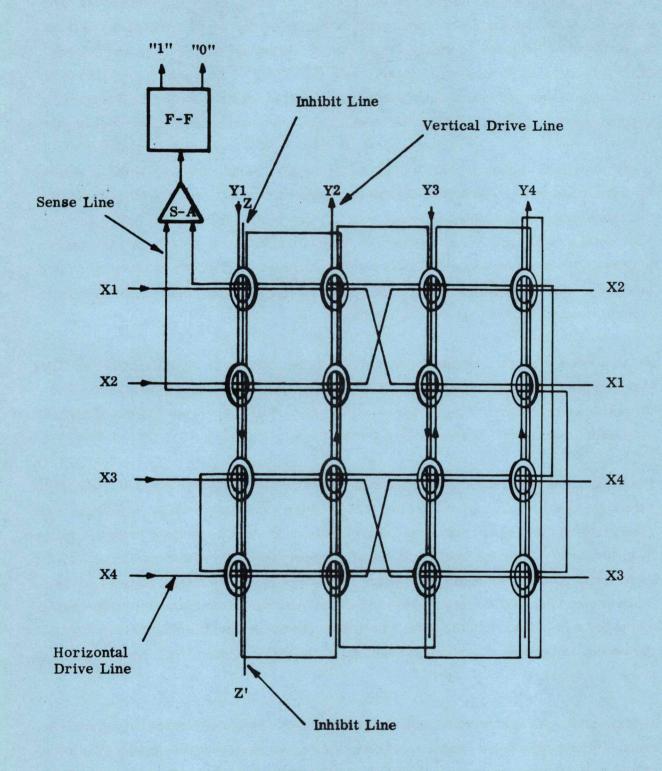


Figure 5A-3. Magnetic Core Storage Geometry

a half current and in a direction opposite to that of the write current is applied to the inhibit winding of the plane. The inhibit current is controlled by the contents of the data register, and, therefore, a zero is written into memory for those data bits of the data register that are a zero.

For a decom operation which is to write new information into memory, the memory again goes through both a read and a write cycle. During the read cycle, however, the transfer of information from the sense amplifiers to the data register is inhibited. Instead, the data register is set by a transfer of data from the format register. During the write portion of the memory reference, then, the new information is written into the selected memory location.

The memory operates in the coincident current mode, and uses currents of one direction to read, and the opposite direction to write.

When information is written into a core, the core is switched to the 1 state by two coincident currents on the X and Y drive lines. Similarly, when information is readfrom a core, it is switched to the 0 state by two coincident currents of the opposite polarity. The inhibit line carries a current parallel to one of the drive lines, but in a direction opposite to the half-write current. If the inhibit current is flowing during a write phase, it cancels the effect of one of the half currents and, thereby, prevents any core through which the inhibit current passes from being switched from a 0 to 1 state. If the drive currents were not inhibited during the write phase, all cores would be switched to a 1 state. If the write coincident X and Y currents act to switch a core from 0 to 1, and if that core is already a 1, it remains a 1. Conversely, if the read coincident X and Y drive currents act to switch a core from 1 to 0, and if that core is already a 0, it remains a 0. The sense line is connected to a differential sense amplifier. When a core switches state in either direction, the sense amplifier produces an output; however, this output is sampled only during the memory read phase.

The memory core material has an approximately rectangular hysteresis loop. The high residual magnetization of the core enables it to function as a memory element. The magnetic properties of a core are represented in Figure 5A-4 by its hysteresis loop in which magnetic flux density B is plotted as a function of field intensity H. If sufficient current flow to cause a field intensity of  $+H_{\rm m}$  is applied to the core, the flux density

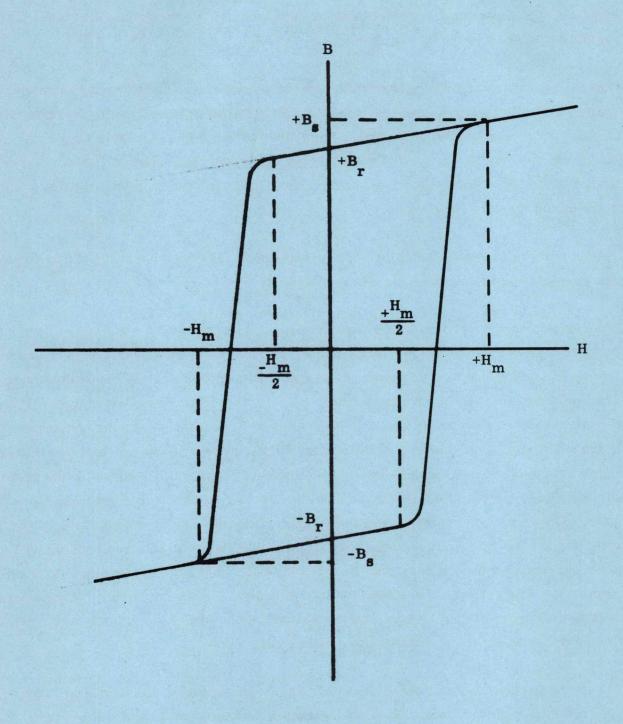


Figure 5A-4. Typical Hysteresis Loop

increases to saturation+ $B_s$ . When current is removed, the flux drops to residual value+ $B_r$  and remains there. Sufficient current flow in the opposite direction to cause a field intensity of - $H_m$  reverses the flux density to - $B_r$ .

The basic memory cycle consists of half-current pulses capable of producing a field intensity of  $\rm H_m/2$ . A half-current pulse is insufficient to switch a core; however, the coincidence of two half currents produces a net field intensity that is sufficient to switch the core.

#### 5A.2.1 INHIBIT CIRCUITS

Whenever an address is selected and the read drive is on, coincident currents are present on each core of that address. These currents attempt to switch all cores. Cores magnetized in the direction resulting from a previous 1 storage are switched, and cores magnetized in the direction resulting from a previous 0 are not switched. Inhibit currents are not used during read, those cores that switch are allowed to switch. If a core is switched, a small voltage is induced in the sense line threaded through that core and a pulse appears along the sense line (see Figure 5A-3). The readout process switches every core containing a 1 to a 0; this is a destructive readout and the memory must be restored. The output of the sense line is amplified and gated into the memory register as 1's. During the write drive, the information is written back into memory; at the end of the memory reference cycle, the contents of the particular selected address is restored.

Whenever an address is selected and the write drive is on, two coincident currents are present on each storage bit of that address. Unless the effect of one of these drive currents is cancelled out, every core in that address is switched to a 1. Because of the effect of the inhibit lines during the write phase of the memory cycle, only those bits which were 1's are switched back to 1's. In order to prevent core-switching in cores that are not to store a 1, a current flowing in opposition to one of the drive currents is generated to cancel the effect of this drive current, thereby inhibiting a core from being switched. This function is performed by the inhibit circuits consisting of inhibit generators and inhibit lines.

#### 5A.2.2 SENSE CIRCUITS

Each sense circuit consists of the sense line threaded through all cores of a quadrant of a plane, and the sense amplifier which is tied to the two ends of the sense line. Whenever a core is switched, a pulse of about 35 millivolts appears on the sense line.

This pulse may be either positive-going or negative-going depending on the direction the core was switched. The sense amplifier consists of a differential voltage amplifier and a discriminator. Regardless of the pulse polarity at the sense amplifier input, the output is always a positive-going pulse.

# 5A.2.3 DRIVE LINE SELECTION

The selection of the horizontal and vertical drive lines is controlled by the address associated with the word. Six address bits are necessary to select one of the 64 horizontal drive lines, and six address bits are necessary to select one of the 64 vertical drive lines. The time from the initiation of a memory reference cycle until the information is in the data register is known as the access time of the memory; the time required for the complete memory reference is known as the memory cycle time (see Table 5A-1).

Table 5A-1 Characteristics of Model 8192 I 42 Memory

Storage Capacity	8192 words, 40 bits per word. Memory stack contains 42 bits, 2 bits being unused.
Memory Cycle Times  Clear/Write Read/Restore Data Access Time	5 microseconds 5 microseconds 1.6 microseconds
Command Signal Characteristics	The command signals are positive pulses, -10 volts (-6 volts) to 0 volts (±1 volt). Rise/Fall time of 0.1 microsecond, of 0.3 to 0.5 microsecond duration.
Address Input Levels	Address inputs are double-ended6 volts = ONE, 0 volts = ZERO.
Data Input Level Binary ZERO Binary ONE	0 volts (±1 volt) -10 volts (-6 volts)
Data Output Levels Binary ZERO Binary ONE	-1.5 volts to 0 volts -10 volts (-6 volts)

A typical memory is constructed of two of these 4096-word banks of memory. The address is then composed of a 13-bit word. The thirteenth bit is used to determine the bank of memory to be referenced, while the lower 12 bits specify the location in the selected memory bank (memory bank being 4096).

In summary, the memory requires only three things from the memory control section of the decom. These are:

- a. A transfer into the memory address register of the number indicating which word in memory is to be selected.
- b. An indication of the direction of the transfer of the word, either into or out of the memory (read or write).
- c. A signal to start the memory cycle, which, in turn, will energize the appropriate selection and drive signals to perform the transfer.

# 5A.3 FUNCTIONAL DESCRIPTION

The timing of the memory defines, upon receipt of a clear/write or read/restore, the type of operation and the appropriate timing signals necessary to perform the operation.

# 5A.3.1 CLEAR/WRITE

A clear/write strobe into the timing logic initiates a timing cycle during which all cores of the addressed matrix are cleared to zero and new data loaded in. When the timing delay line is pulsed by the clear/write command, a reset pulse allows the data register to be reset (Figure 5A-5). Next, an address strobe enables the 13-bit address to be loaded into the two segments of the address register, and a data strobe enables the data from the format register to be loaded into the data register. When the cores are addressed by the selection of the "X"/"Y" read pulses, the data contained therein is essentially cleared because the sense amplifiers outputs are inhibited by the lack of a read strobe. This prevents the sensed data from being loaded into the data register. The remainder of the memory cycle performs a write function to place the new data into the addressed core matrix. The "X" and "Y" write pulses are generated to again enable the proper core matrix, and an inhibit pulse placed on the inhibit drivers to enable a zero to be written into memory. It is during this cycle that the contents of the data register are transferred to memory.

### 5A.3.2 READ/WRITE

The read/write cycle of memory differs from the clear/write cycle in that the contents of an addressed core matrix are read from memory, loaded into the data register, and then written back into memory. This cycle is often referred to as read/restore. The timing when strobed by a read/write command, generates a reset pulse to reset the data register. The 13-bit address is loaded into the address register by the address strobe and the "X"/"Y" read pulses are enabled thus allowing the core matrix currents to drive the sense amplifiers. The initiation of the read/write cycle generates a read strobe which enables the sense amplifiers to drive the data register. After the register is loaded, the write cycle begins and restores the data to the addressed core matrix. The write cycle of the read/write mode is the same as the write cycle of the clear/write mode.

#### 5A.3.3 INHIBIT SELECTION

The inhibit selection for writing into the memory core matrix is performed in two groups. Group A selects one-half of the memory and group B selects the other half of the memory. The 8192 memory core matrix has 64 "X" drive lines and 128 "Y" drive lines. The selection and operation works the same as explained in previous paragraphs. The 64 "X" drive lines are divided into groups A and B, and when combined with the "Y" drive lines will result in the following:

- a. Group B selection = 1 to 32 "X" drive lines and 128 "Y" drive lines.
- b. Group A selection = 33 to 64 "X" drive lines and 128 "Y" drive lines.

Therefore, when the address is loaded into the address register,  $2^5$  of the "X" decode logic (Figure 5A-5) will define which half of the  $8192 \times 40$  matrix is to be enabled.

### 5A.3.4 ADDRESS SELECTION

The memory address decoder is depicted in Figure 5A-6. The address is composed of a 13-bit address from the decom address OR gate and is divided into four groups for decoding. The "X" drive circuits are set up to form an  $8 \times 8$  matrix, thus producing a drive capability for 64 drive transformers. Bits  $2^{\circ}$  through bits  $2^{\circ}$  are decoded to enable one drive circuit and bits  $2^{\circ}$  through  $2^{\circ}$  are decoded to enable another drive circuit. The two enable one drive transformer.

The same holds true for bits 2<sup>6</sup> through 2<sup>9</sup>; however, bits 2<sup>10</sup> through 2<sup>12</sup> are decoded to enable one of 16 drive lines. The two enable one drive transformer of the 128 "Y" drive transformers.

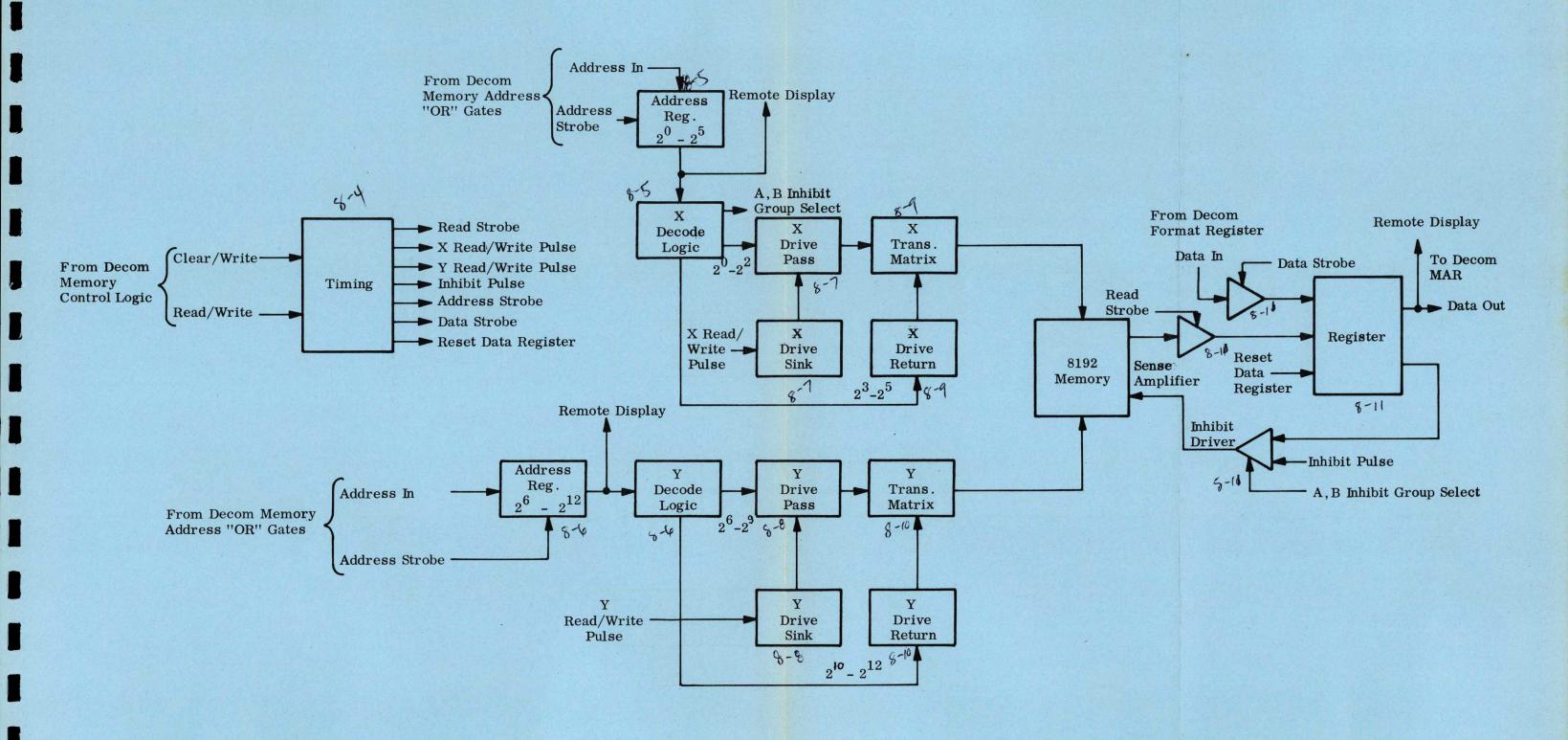


Figure 5A-5. Decom Memory

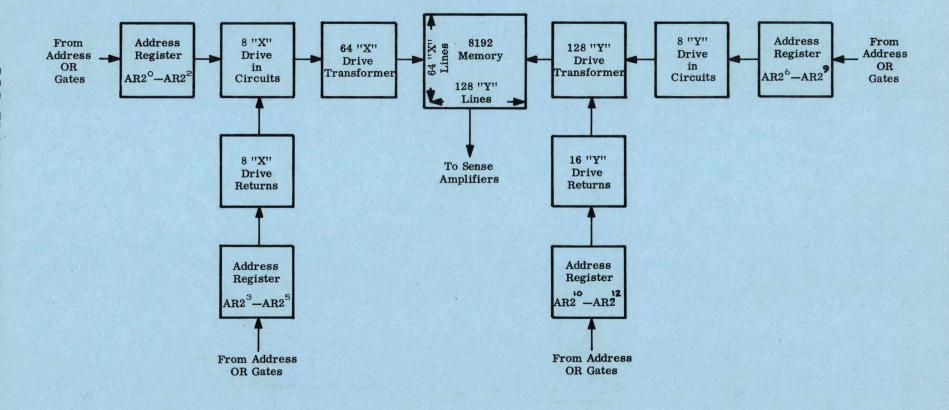


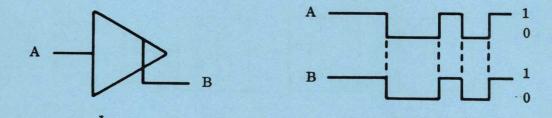
Figure 5A-6. Decom Memory Address Decoder

# 5A.4 INDIANA GENERAL LOGIC

The decommutator in using an Indiana General Memory System incorporates a different set of logic symbols and different levels of logic voltages than the Standard Radiation logic. Therefore, it is imperative that a comprehensive discussion of Indiana General logic symbology be presented. The logic levels are listed in the characteristics table. All memory logic consists of cards.

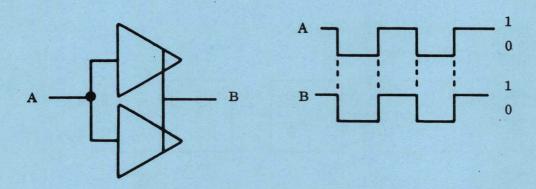
#### 5A.4.1 EMITTER FOLLOWER

The emitter follower is an impedance matching device which has a gain less than unity. It is a single input and a single output unit with no logic inversion.



## 5A.4.2 COMPLEMENTARY EMITTER FOLLOWER

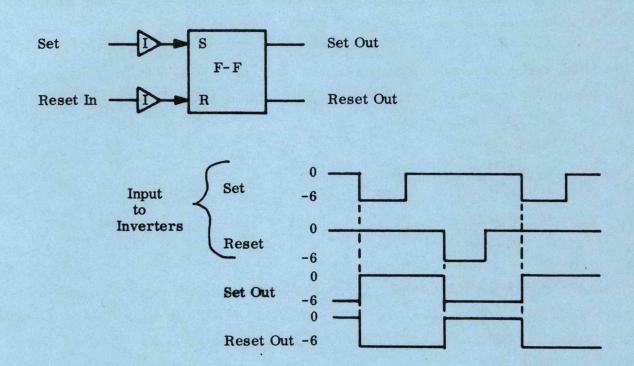
The complementary emitter follower operates the same as the emitter follower; however, it has an added capability of a higher operating speed and can drive a greater load. It also provides no logic inversion.



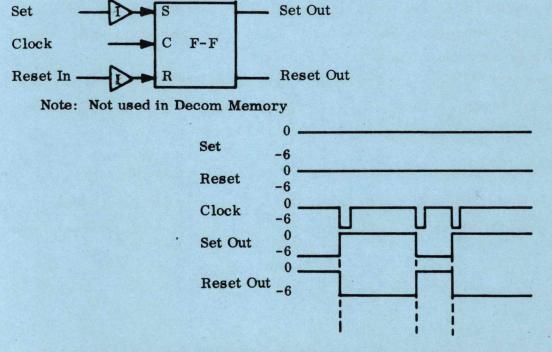
## 5A.4.3 FLIP-FLOP

The standard flip-flop card contains four identical circuits; however, the following discussion pertains to only one such circuit on a card. The basic flip-flop operates in one configuration in the memory, set and reset by direct or forced inputs. The direct control of the flip-flop is shown in the

following figure. When a set input occurs, the set out assumes a logic one or -0 volts. The opposite holds true for the reset condition.



If a clock is used to trigger the flip-flop, it changes the state to either the set or to the reset state regardless of the initial condition. Also on a flip-flop card containing four individual circuits, the clock is common to all set and reset sides.



# 5A.4.3.1 Flip-Flop Circuit Analysis

An Indiana General flip-flop consists of six transistors as shown in Figure 5A-7. Q1 and Q2 are the bistable, Q4 and Q6 are output inverters, Q5 is the set input amplifier, and Q3 is the reset amplifier.

If the assumption is made that the flip-flop is in the set condition and no input signals are present the transistors will be in the following conditions:

- a. Q1 is on.
- b. Q2 is off.
- c. Q3 is off.
- d. Q4 is off.
- e. Q5 is off.
- f. Q6 is on.

Point A is at ground potential and point  $\overline{A}$  is at a -6 volts. If a -6 volts is applied to point 4, Q3 turns on and places the cathode of CR2 at or near ground. This causes Q2 to be turned on. Q6 will turn off because the ground potential at the cathode of CR2 causes the base of Q6 to go positive. When Q3 and Q2 conduct, the positive on the base of Q1 turns off Q1 which, in turn, allows the cathode of CR1 to go negative thus turning on Q4. The result is that the flip-flop is now reset and point A is at -6 volts and  $\overline{A}$  is at ground. It may well be noted that the -6 volts applied to the base of Q3 need not be greater than the length of time needed to flip the circuit.

If the same initial conditions are assumed for a clock, the following would occur. A negative going transition applied to point 17 causes CR3 to be back biased, and the base of Q3 goes negative due to the voltage divider network of R8, R5, and R9. Q3 turns on and the circuit flips in the same manner as described for the direct input. Q5 also turns on for the same amount of time that Q3 turns on, but since Q1 is already on, Q3 has no effect upon the circuit.

# 5A.4.4 SINGLE SHOT MULTIVIBRATOR (not used in decom memory)

The single shot multivibrator provides a single pulse output for a single pulse input. When the input or set side is pulsed as shown below, the set output produces a positive

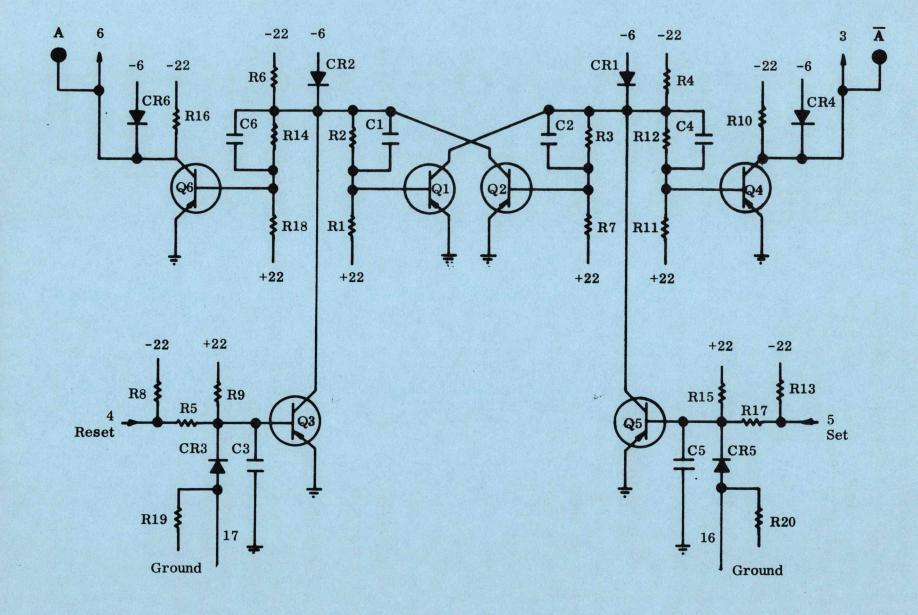
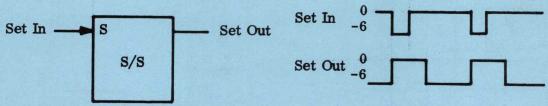


Figure 5A-7. Flip-Flop Circuit

pulse whose width is equal to the RC time constant of the circuit. The flip-flop automatically reverts to its quiescent reset state.

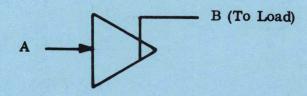


Note: Not used in Decom Memory

This type of circuit is used to generate a pulse to activate the timing delay line of memory. The pulse duration is approximately 100 nanoseconds.

#### 5A.4.5 CURRENT DRIVER

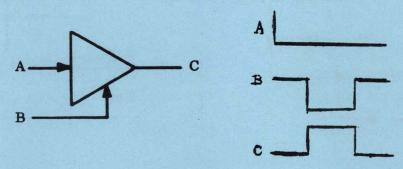
The current driver symbol is basically opposite that of an emitter follower previously discussed. The function is to control the memory transformer return circuits when a given "X" or "Y" drive line has been enabled.



A -6 volts on A turns off the driver and allows the current to be switched to the current driver load at point B.

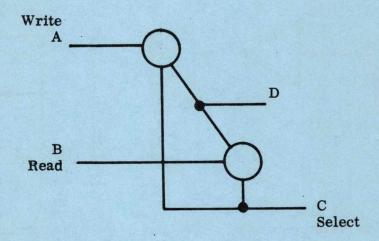
### 5A.4.6 DRIVE INPUT AMPLIFIER

The drive input amplifier is used to provide the proper read or write current for the core transformer matrix. The amplifier requires two inputs to be turned on. The input to point A is usually obtained from an inverter which when turned on causes the drive input amplifier to be enabled. A read or write strobe is applied to point B thus applying a current drive at point C.



### 5A.4.7 DRIVE TRANSFORMER

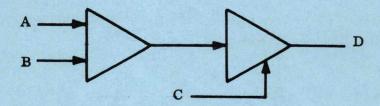
This device accommodates separate read and write current pulses through its two primaries to provide an output from its secondary; the two primary return lines are tied together except for sequential interlaced operation where separate load and unload address counters require separate decoders; drive transformers are arranged in separate X and Y selection matrices.



Point C is selected by a decoded address and enables both transformers. A read or write pulse applied to point A or B determines the operation of the circuit. Point D is the "X" or "Y" selection line to the core matrix.

#### 5A.4.8 SENSE AMPLIFIER

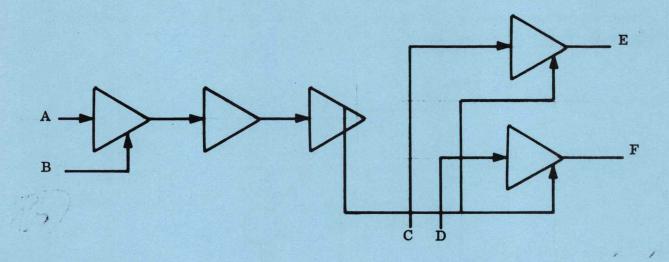
The functions of a sense amplifier are to sense the condition of a core when selected by the "X" and "Y" drive lines. The inputs to the amplifier are two from the core sense windings and one as an enable or sense strobe.



Point A and B are sense winding inputs and when point C goes negative point D produces a positive pulse. If A and B do not produce a voltage when the core is selected, point D remains at a negative potential although point C is enabled.

#### 5A.4.9 INHIBIT DRIVER

The inhibit driver is used to drive the inhibit lines of the core matrix when a zero is to be written into memory.

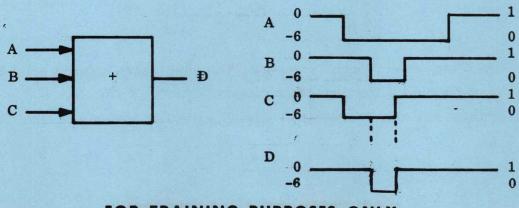


When no inhibiting function is being performed, point B is at ground potential. When inhibit is activated and a zero is to be written into memory, point B and point A are at -6 volts. Points C and D are enable terms to determine which group of cores are to be selected.

When enabled, C or D will be a negative 3 volts. Thus, an inhibit current of approximately 90 ma is present at point E or F to prevent a core from switching, and a zero is stored.

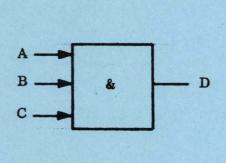
#### 5A.4.10 OR GATE

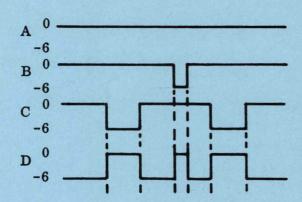
The Indiana General OR gate is a negative AND which produces a 0 volts out when one or more inputs are positive or at ground potential. When all inputs are at -6 volts simultaneously, point D goes to 76V



5A.4.11 AND GATE (not used in the Decom Memory)

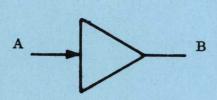
The AND gate is basically a negative OR which produces a -6 volts out when all inputs are at ground potential. When one or more inputs are at -6 volts point D goes to zero. The output at point D is fed through an inverter within the symbol.

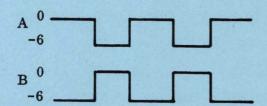




#### 5A.4.12 AMPLIFIER

An amplifier provides logic level inversion in that an input of A produces  $\overline{B}$  and for an input of  $\overline{A}$  the output is B.





#### SECTION 6

#### **OUTPUT RACK**

#### 6.1 MSB AND LSB PARALLEL REGISTERS

#### 6.1.1 GENERAL

The function of this logic group is to provide, as an output, all data words in both most significant bit (MSB) first and least significant bit (LSB) first formats at the same time. Any data word may be from 4 to 64 bits long. The different conditions under which the registers can accept data are:

- a. No parity or word sync code bits in the data word and either MSB or LSB first.
- b. Parity and word sync code bits present in the data word either at the beginning or the end of the word and either MSB or LSB first.

The program of the system being monitored dictates the above conditions.

The incoming data (Figure 6-1) is controlled by an up counter, a down counter, and the level of a signal which identifies the data as being either MSB first or LSB first data.

If the data is MSB first data, the up counter routes it to the MSB formatting register while the down counter routes it to the LSB formatting register. If the data is LSB first data, the up counter routes it to the LSB formatting register while the down counter routes it to the MSB formatting register. Hence the two counters are used to insure that the data is placed properly in its respective registers, regardless of the format in which it is received.

The memory buffer register forces the down counter to the number of bits in the incoming word. If the word has parity and word sync code bits present, the up counter is inhibited from counting until these control bits are past. The bits are stored in a four-stage format register until required at a later time.

After these control bits have passed, the two counters start counting, the up counter being incremented by one and the down counter being decremented by one with each clock pulse. The output of the counters are ANDed with the control level signal (MSB or LSB first), and the output of each again ANDed with the incoming data in the 'X-Y"

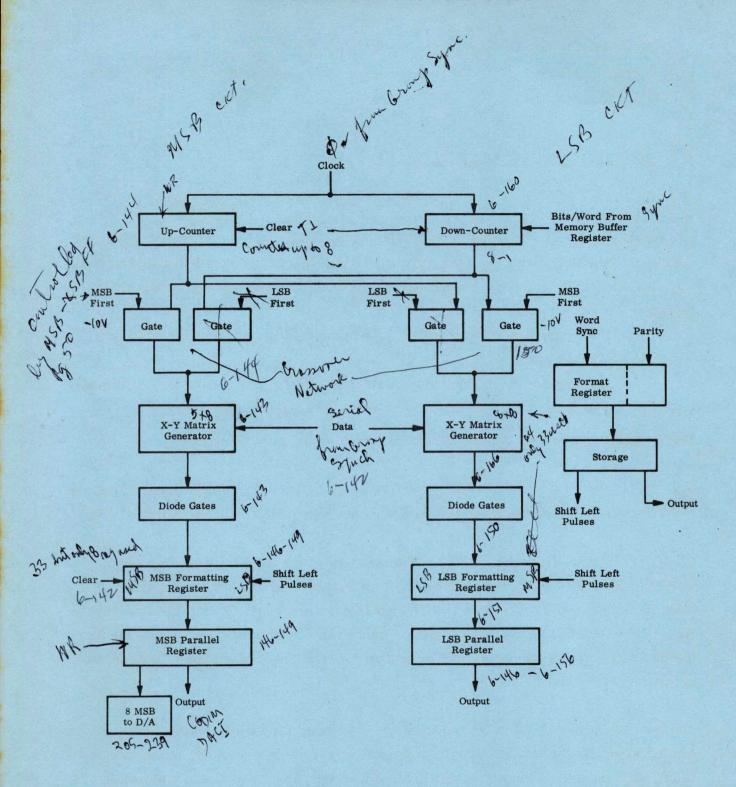


Figure 6-1. MSB and LSB Parallel Register, Simplified Block Diagram

matrix generator. The function of the "X-Y" matrix generator is to select one of a group of diode gates whose output is associated with a specific stage of the MSB and LSB formatting registers. Because the registers are preset to zero at the end of every word, it is necessary to gate only the binary 1's through the diode gates and apply them to the respective formatting register stages.

After the entire word has been entered into the two formatting registers, the register that was being controlled by the down counter is shifted to the left the number of places corresponding to the number of parity and word sync code pulses contained in the word. The reason for this is that the down counter was forced to the count of the number of bits in the word by memory. This count included the number of parity and word sync code bits.

At the end of the word, a word rate pulse is generated by the group synchronizer. This pulse is applied to the MSB and LSB formatting registers and shifts the data word into the respective parallel register in parallel. The eight MSB of the MSB parallel register are routed to the digital-to-analog converters, where they are converted to an equivalent analog voltage.

The contents of the two parallel registers are available as outputs at the end of every word time.

The MSB formatting and parallel registers are composed of 33 stages, while the LSB formatting and parallel registers are composed of 64 stages. The reason for this is that it is necessary to acquire only one more MSB bit than half the word length to determine the value of the measurand, while the entire word in LSB form must be gathered to determine which bits are the MSB of the word.

#### 6.1.2 MSB FIRST-WORD SYNC CODE AND PARITY BITS PRESENT

If word sync code bits and a parity bit are present in an incoming data word, the group synchronizer sends a -10 volt level that lasts for the duration of these control bits. It may not be present at all or it may be fron one to four bits long, depending on the program being executed. The parity bit level is applied to OR gate A6A (sheet A, figure 6-44). The word sync code bits level is applied to power inverter A10A and to OR gate A6A also. The two levels are ORed together and the zero volt output of the OR gate is routed through emitter follower A7A to CSR module A8A. The level is inverted by this module and applied to AND gate A9B, where it inhibits the gate. The parity bit is inverted and

ANDed with clock by AND gate A4B. The -10 volt pulse is applied to flip-flop A4C as the trigger input. The actual parity bit is applied from the data input inverter A6C.

The level that signifies that word sync code bits are present is also applied to power inverter A10A, where it is inverted and applied to AND gate A4A. The other two inputs to the AND gate are T1, which is a zero volt level whenever word sync code bits are present and clock. The -10 volt output of the AND gate is applied to trigger driver A3A. The positive transition of the trigger driver output triggers counter stage A2A. Counter stages A1A and A2A control a three-AND gate "X-Y" matrix. The output of these three AND gates are the trigger inputs to the word sync code bits formatting register (A1C, A2C, and A3C). The three bits that were applied to the data input power inverter during the time the word sync code level was present are gated into this three-stage formatting register. The word sync code bits and parity bit are shifted out of the four-stage formatting register and into a four-stage parallel register (A1D, A2D, A3D, and A4D). At the end of the word or prime frame, the word sync pulse or prime frame sync pulse is applied to trigger driver A5D. The corresponding zero volt transition from this module triggers the control bits parallel register and shifts the four control bits out in parallel.

With the absence of the parity and word sync code level, OR gate A6A returns to its normal unloaded state and produces the -10-volt output. This level is inverted by CSR A8A and trues AND gate A9B. The three inputs to this AND gate are inverted parity and word sync code level; bit rate clock pulses; and inverted data. Hence, during any decommutation process, this AND gate is the one through which all data is applied to the MSB and LSB "X-Y" matrices. The controlling input to the gate, as previously discussed, is the presence or absence of parity and word sync code bits. The output of the gate is applied to the LSB "X-Y" matrix and, through power inverter A10B, to the MSB "X-Y" matrix.

When the word sync pulse or the prime frame sync pulse is applied to OR gate C1A (sheet C, figure 6-44), the resulting 0 volt output is inverted and applied to flip-flop C4A. The set output is applied to AND gate U9C (sheet U) along with clock to true the AND gate. The resulting -10-volt pulse is applied to pins 2 and 7 of diode gates U1E through U6E. The count stored in the six-stage storage register U7D through U9D and U7E through U9E is gated through the diode gates and force counter U1D through U6D to the same count. This is the down counter. The count that was contained in the storage register was the number of bits in the incoming word as sent from the memory buffer register.

The inverted output of OR gate C1A (sheet C) is also applied to the six-stage storage register (sheet U) to reset it to zero.

The set output of flip-flop C4A (sheet C) is also applied to AND gates C3A and C7B, along with the control pulses indicating that parity and word sync code bits are present to true the gates. The -10-volt output from each gate is applied to the first stage of up counter C1B through C6B. This keeps the counter from counting during the time the control bits are present.

When the word sync pulse or prime frame sync pulse is removed from OR gate C1A, the clock (bit rate frequency) inputs to flip-flop C5A cause the module to be reset. The reset output, along with the inverted clock pulse from power inverter C10A are applied to AND gate U8C (sheet U) which trues the AND gate with every clock pulse. The resulting -10-volt outputs are applied to trigger driver U7C. With every positive transition of the trigger driver, the down counter is counted down by one. The set output of each stage of the counter is applied to pin 9 of diode gates U1C through U6C respectively.

With the removal of the -10 volt level control pulse from AND gate C9B (sheet C) and AND gate C3A, the up counter is free to count at bit rate starting with a one. The output of the AND gate is applied to trigger driver C8B, and, with every positive transition of the trigger driver, the up counter advances by one.

The set output of each up counter stage is applied to pin 2 of diode gates C1C through C6C respectively.

The control level identifying data as MSB first or LSB first data is applied to CSR module C10C from the group synchronizer. A -10-volt level signifies MSB first data; while a zero volt level signifies MSB first or LSB first data.

Assume the data is MSB first and the control level is -10 volts. This level, when applied to CSR C10C, is inverted and identified as the LSB first data signal and applied to the up counter and down counter diode gates. However, the level is zero volts; therefore, it has no effect upon the diode gates as the gates must have -10 volts applied to both inputs, as can be seen from the schematic diagram (in Appendix 2).

The original -10-volt level is again inverted CSR C8C and identified as the MSB first data signal. The signal is now at -10 volts. It is applied to pin 4 of diode gates C1C through C6C and pin 7 of diode gates U1C through U6C (sheet U).

Assume now that the first stage of the up counter and the last stage of the down counter contain a binary 1. The two -10-volt inputs on pins 2 and 4 of diode gate C1C cause a corresponding -10-volt output at pin 5. This output is applied to CSR module C1D, where it is inverted and made available as an output as well as an input to CSR module C1E, where it is inverted. Therefore, when counter stage C1B is set, an output pulse of -10 volts is available at C1E and zero volt is available at C1D. These two outputs are applied to the MSB formatting register 'X-Y' matrix.

At the same time the two -10-volt inputs to diode gate U6C (sheet U) causes a corresponding -10-volt output at pin 10. As a result a -10-volt output is available at CSR module U6A, and a zero volt output is available at U6B. These two outputs are applied to the LSB formatting register "X-Y" matrix. The outputs from the up counter diode gates C1C through C6C (sheet C) are applied to the MSB formatting register "X-Y" matrix, AND gates B1A through B8A and B1C through B6C (sheet B). The outputs from the down counter diode gates U1C through U6C (sheet U) are applied to the LSB formatting register "X-Y" matrix, AND gates N3A through N10A and N3C through N10C (sheet N).

Carrying the above process through and assigning the binary outputs to each CSR module at the output of the up counter and down counter diode gates, it can be seen that, for any given count in the two counters, only one four-input AND gate and one three-input AND gate of each "X-Y" matrix is true, or all zero volt level pulses present as inputs, at any one time. The fourth input to the four-input AND gates is data by the action of power inverters A10B (sheet A) and N2A (sheet N). Therefore, when a specific AND gate in the matrix is true, the corresponding -10-volt output from the four-input AND gate is the original data binary "1." Because the MSB and LSB formatting and parallel registers are reset to zero at the end of every word, it is necessary to enter only the binary "1's" of the data.

To complete the example presented of a binary "1" in the first stage of the up counter and the last stage of the down counter, the following action takes place.

AND gates B2A and B1C (sheet B) are true in the MSB formatting register "X-Y" matrix. The outputs from these two gates are applied to various diode gates (B1E through B10E and B4D through B10D) in the MSB decoding matrix; however only pins 2 and 4 of diode gate B1E have -10 volts applied to them at the same time. Therefore, only pin 1 of diode gate B1E has a -10-volt output during this bit time. The output of the diode gate is applied to the set side of stage E1A (sheet E) in the MSB formatting register (all the "A" shift register stages on sheets E, F, G, and H).

AND gates N3A and N7C (Sheet N) are true in the LSB formatting register "X-Y" matrix. The outputs from these two gates are applied to various diode gates (1B through 10B on sheets K, L, and M and 1B and 2B on sheet N) in the LSB decoding matrix; however, only pins 7 and 9 of diode gate K2B (sheet K) have -10 volts applied to them at the same time. The corresponding -10 volts output from pin 6 places a binary "1" in stage K2C of the LSB formatting register (all "A" and "C: stages on sheets K, L, M and stages 1C, 1E, 4E and 7E on sheet N). The entire word is loaded, bit by bit, into the two formatting registers.

The above discussion assumed an MSB first data word. Because the down counter was counting during the time parity and word sync code bits were on the line, the data word, now in LSB formatting register, is not stored properly and must be shifted left the number of places corresponding to the number of control bits in the word. The LSB first level (being zero volts) is ANDed with clock and the absence of the word sync or prime frame sync pulse through AND gate H10E (sheet H). The resulting -10 volt output is inverted twice by power inverters H9E and H5E and applied to all stages of the LSB formatting register. The register is shifted until the word sync or prime frame sync pulse inhibits the gate which corresponds to the original number of control bits. At the end of the word or of the prime frame, the word sync pulse or prime frame sync pulse is applied to OR gate C1A (sheet C). The resulting output pulse forces the down counter storage register (sheet U) to zero and after the pulse is inverted, causes flipflop C4A to change states. The set output of the flip-flop resets the up counter to zero; the reset output is applied to CSR A6D (sheet A). The inverted output of this stage is used to generate the MSB and LSB parallel registers load pulse through CSR stages 7D and 8D. The load MSB parallel register pulse is applied to all 33 stages of the MSB formatting register and causes all binary "1's" in the data word to be transferred to the MSB parallel register (all the "B" shift register stages on sheets E, F, G and H).

The eight MSB's of the word are routed to the digital-to-analog converters, where they are converted to an equivalent analog voltage. The entire word is available at the output jacks.

The load LSB parallel register pulse is applied to all 64 stages of the LSB formatting register and causes all binary "1's" in the data word to be transferred to the LSB parallel register (all of the "E" stages on sheets E, F, G and the "D" stages on sheets K, L, M and stages 2C, 2E, 5E, and 8E on sheet N). The entire word is available at the output jacks.

#### 6.1.3 LSB FIRST-NO WORD SYNC CODE OR PARITY BITS PRESENT

Data entering in LSB fashion may have parity and word sync code bits present the same as MSB first data. The identification and logic of handling them is the same as that described in the previous paragraph. However, in this example, assume that the control bits are not present.

The only difference between MSB first data and LSB first data is the level of the control signal and the fact that the up counter gates the data into the LSB formatting register while the down counter gates it into the MSB formatting register.

Assume the level applied to CSR module C10C (sheet C) is zero volt. The module inverts the signal and applies it to pin 7 of diode gates C1C through C6C and pin 4 of diode gates U1C through U6C (sheet U). The output of the up counter (sheet C) is applied to pin 2 of diode gates C1C through C6C; however, there is no output from pin 5 because pin 4 is at zero volts. The output of the down counter is applied to pin 9 of these gates; therefore, there is a -10-volt output on pin 10 because of two -10-volt levels applied at pins 7 and 9. The output of the up counter being applied to pin 2 of diode gates U1C through U6C (sheet U) results in an output from pin 5 of the diode gates because of -10 volts being applied to pins 2 and 4. As can be seen, the level of the control signal (MSB or LSB first) causes the two counters to be interchanged. All other functions described in the previous paragraph remain the same.

#### 6.1.4 DISPLAY ADDRESS REGISTER

This panel also contains a 12-bit display address register. This is shown in figure 6-44, sheet D, S and T. The register is completely independent of the logic discussed in the previous paragraphs. Various words of a given program are capable of being displayed on the decimal or binary display front panels. Every word capable of being displayed

is assigned a 12-bit code prior to the decommutation process. This code is entered into memory along with the basic program. As the program is executed, these 12-bit display addresses are routed from the memory auxiliary register to CSR stages D1A (4A2D) through D4A, D1B through D4B, and D1C through D4C (figure 6-44, sheet D). Each bit is applied to both the set and reset input of its respective CSR module. The address code bits are applied to CSR stages T1A through T10A and T1C, and T2C (sheet T) in a parallel transfer.

The set output of the 12 CSR's is routed to the decimal and binary displays, where the data word for that address can be displayed when desired. The reset outputs are routed through power inverters 1C through 10C, 9A and 10A (sheet S) in parallel. Each bit is inverted and applied to the output jacks.

## 6.2 MSB AND LSB TRUNCATION

#### 6.2.1 MSB AND LSB TRUNCATED CHARACTERS CONTROLS

The toggle switches for establishing the length of the MSB and LSB data word (character) sent to the computer are located inside panel 4A3, Figure 6-2. Table 6-1 contains a listing of the controls and their function.

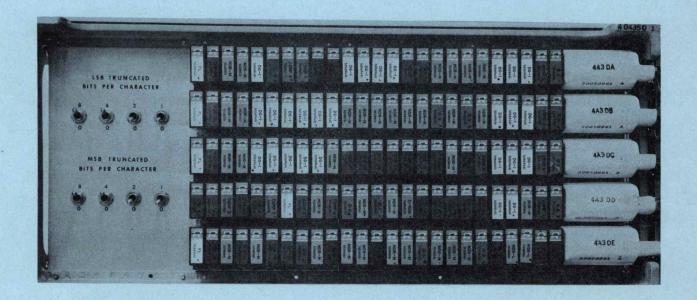


Figure 6-2. MSB and LSB Truncated Characters Controls

6-9

Table 6-1
MSB and LSB Controls

Control	Function	
LSB TRUNCATED	Establishes the number of	
BITS PER CHARACTER	bits to be in the LSB truncated	
toggle switches	character output.	
MSB TRUNCATED	Establishes the number of	
BITS PER CHARACTER bits to be in the MSB truncated		
toggle switches	character output.	

#### 6.2.2 MSB AND LSB TRUNCATED CHARACTERS

#### 6.2.2.1 General

The purpose of this group of logic is the truncation, or breaking up, of each word into smaller characters. These characters must be available in both MSB first and MSB first (LSB first) form for both MSB first and LSB first data. The data is routed into its respective registers by an up counter and a down counter, thereby forming the characters. The two counters are controlled by bits per character switches and a calculator.

Figure 6-3 is a block diagram of the character truncation process. These bits per character are established by setting up the count on the switch panel located inside of the 4A3 module panel. The switch settings are applied to a crossover network composed of four diode gates for each group of switches. These crossover diode gates are similar to those discussed in paragraph 6.1.

The reason for the crossover networks is that the data may come in either as MSB first data or LSB first data. The assignment as to whether the data is MSB first or LSB first is a function of the program being performed and is known before starting the decommutation process. A -10-volt level identifies MSB first data while a 0-volt level identifies LSB first data. If the data is MSB first, the MSB truncated character switch settings control the up counter while the LSB truncated character switch settings control the calculator and the down counter. If the data is LSB first data, the LSB truncated character switch settings control the up counter while the MSB truncated character switch settings control the calculator and down counter.

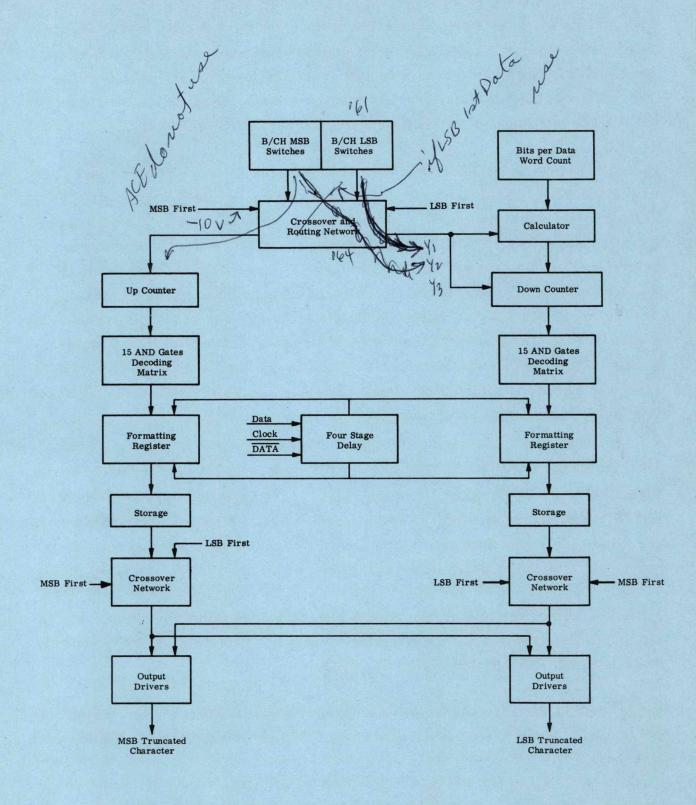


Figure 6-3. MSB and LSB Truncation Registers, Simplified Block Diagram

The logic decisions and steps necessary in forming the two truncated characters are listed in Table 6-2. The two columns of the table occur simultaneously, however, and are completely independent from each other. Because the calculator must perform a subtraction operation that may take up to four bit-times to complete, the data word is delayed four bit-times before being applied to the formatting registers.

Figure 6-4 shows an MSB first data word of 25 bits truncated into MSB first and LSB first characters. The MSB truncated character switches are set for seven bits per character; while the LSB truncated character switches are set for 11 bits per character. The output from the MSB truncated character register forms three complete seven-bit characters and one four-bit (last three bits are zeros) character from the 25-bit data word. The output from the LSB truncated character register forms the first character with the final remainder from subtracting 11 from 25 until the remainder is less than the character switch settings. In the example shown the first character contains three data bits and the rest of the character is filled with zeros. The remaining two characters are full 11-bit characters as a result of the subtraction. Figure 6-5 is a timing diagram of the above function.

## 6.2.2.2 Logic Analysis

Figure 6-45, sheets A through H and K through M, are the logic diagrams for the MSB and LSB truncated characters. The MSB and LSB truncated character switches (sheet A) are wired such that an open switch (up) places -10 volts on the associated pins of the diode gate; closing the switch (down) puts ground on the pin.

Setting the LSB truncated character switches to the desired number of bits per character applies the count to pin 4 of diode gates D1A through D1D (sheet D) and to pin 9 of diode gates D2A through D2D.

Setting the MSB truncated character switches to the desired number of bits per character applies the count to pin 4 of diode gates D2A through D2D and to pin 9 of diode gates D1A through D1D.

The output of diode gates D1A through D1D are applied to the up counter. The output of diode gates D2A through D2D are applied to the calculator to form the first character and then to the down counter to form the remaining characters.

 ${\bf Table~6\hbox{--}2}$  Logic Decisions and Steps in Forming Truncated Characters

LSB Truncated Character		MSB Truncated Character		
Α.	Determine whether data word is MSB first or LSB first. A -10-volt level means MSB first; a 0-volt level means LSB first.	A.	Determine whether data word is MSB first or LSB first. A -10-volt level means MSB first; a 0-volt level means LSB first.	
В.	Set truncated character switches to desired number of bits per character - 4 to 15 bits.	В.	Set truncated character switches to desired number of bits per character - 4 to 15 bits.	
C.	Count of bits per incoming data word sent from stored program processor.	C.	Start up counter at count of 1. Count up until count agrees with switch settings in B above.	
D.	Calculator subtracts B above from C. If C is still larger than B, C is shifted right one place and subtraction is performed again.	D.	Apply character formed by C above to output crossover network. Level of identifying signal determines whether character is crossed over.	
E.	Set down counter with final remainder when it is less than bits per truncated character count (Babove).	E.	Reset up counter to 1 and form second character as in C above.	
F.	Form first character from this count. Difference between this count and count established in B above is filled with zeros.	F.	Repeat D and E above until data word is completely truncated. Last bits of last character are zeros if data word does not completely fill character.	
G.	Apply character to output crossover network. Level of identifying signal determines whether character is crossed over.	G.	Next data word starts at C because A and B are constant for a given program.	
н.	Set down counter with count established in B above. Form next character from this count.	*		
I.	Repeat G and H above until data word is completely truncated.			
J.	Next data word normally starts at C because A and B are constant for a given program.			

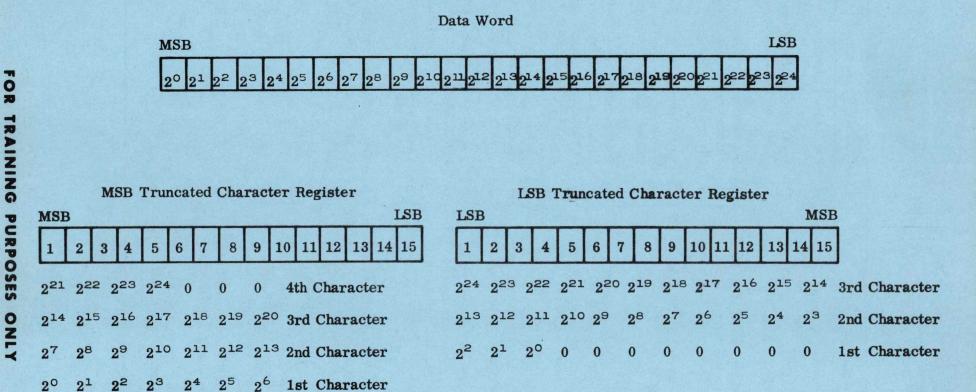


Figure 6-4. MSB and LSB Truncated Characters Formation Simplified Diagram

Figure 6-5. MSB and LSB Truncation Registers, Timing Diagram

These eight diode gates make up the switch crossover and routing logic. The identifying level signifying MSB first data is applied to pin 7 of all eight diode gates. When the data is LSB first data, the identifying signal is applied to pin 2 of all eight diode gates. Hence, depending upon the level of the identifying signal, the switch settings control either one counter or the other.

Assume the data being received is MSB first data. The identifying signal is the same signal used in the MSB and LSB formatting and parallel registers. A -10-volt level from the group sync means MSB first, and a 0-volt level means LSB first.

The level is applied to power inverter D5E (sheet D), where it is inverted and applied to the rest of the system as the LSB first level. The level is also applied to AND gate D3E, where it is again inverted and identified as the MSB first signal; it is applied to pin 7 of the eight diode gates.

The level out-of-power inverter D5E, in addition to being applied to the AND gate D3E, is applied to power inverter D4E inverted, and applied to AND gate D2E, where it is again inverted. The output of the AND gate is identified as the LSB first level. It is applied to pin 2 of the eight diode gates. Because of the fact that the diode gates must have -10 volts applied on adjacent pins (2 and 4 or 7 and 9) to obtain an output of -10 volts from either pin 5 or 10, respectively, it can be seen that the two groups of truncated character switches are crossed over, or control one or the other counter depending on the level of the identifying signal.

The LSB switches being set for 11, the 1, 2, and 8 switches are in the up position. This applies -10 volts to pin 9 of diode gates D2A, D2B, and D2D respectively, with -10 volts applied at pins 7 and 9; a -10-volt output is available at pin 10. These three outputs are applied to the down counter and to diode gates 3A, 3B, and 3C. If the character length is different from the word length, a subtraction must be performed by the calculator. If this is the case, as it is in the example presented, the output of the diode gates applied to the down counter are locked out until after the first character has been formed.

# 6.2.2.3 Calculator

The calculator logic is shown on sheet B. Diode gate B5A is the one designated as the units position (2°). The ten position (2°) consists of diode gates B5B through B9B. The

hundreds position (2<sup>2</sup>) is diode gates B5C through B9C. The thousands (2<sup>3</sup>) position is diode gate B10B.

The count of the bits per incoming data word is sent from the word length register of the stored program processor one word time in advance of when it will be used. This count is a total of six bits long and is stored in reverse order from the memory word in a six-stage storage register consisting of stages B2A, 2B, 2C, 2E, 4E, and 6E (figure 6-45, sheet B). Stage 2A contains the LSB of the count; stage 6E contains the MSB. At the end of the word being processed, the end-of-word pulse (WS) is applied to the storage register and transfers the bits per data word count out in parallel. The count is applied to AND gates 7A through 10A and 1B through 6B (sheet C). After the parity and word ID code bits in the incoming data word are blanked out, -10 volts is applied to power inverter C9C, where it is inverted and applied to the AND gates also. This trues the gates and forces the bits per word count into the set side of shift register stages C1C through C6C. The count is still in reverse order with the MSB in stage 6C and the LSB in stage 1C.

The four MSB positions (6C, 5C, 4C, and 3C) of this number are the ones used in the subtraction process; i.e., the count of the bits per character switches (maximum of four bits) which equal a count of 15 are subtracted from these four bits.

Shift register stage C3C is the LSB of these four bits (bits per word); therefore, it becomes the units bit. It is applied to the units diode gate B5A (sheet B). The set side of the stage is applied to pin 7 of the diode gate, while the reset side is applied to pin 2. The output from the LSB of the bits per character diode gate 3A (sheet D) is applied to inverter 3A (sheet B). The output is inverted and applied to inverter 4A and to pin 9 of diode gate 5A. The inverted output of 4A is applied to pin 4 of the diode gate. As mentioned previously, the diode gate must have a -10-volt input on two adjacent pins (2 and 4 or 7 and 9) to produce a -10-volt output from either pins 5 or 10 respectively.

Hence the units diode gate (5A) accepts both the set and reset output from the apparent LSB stage (C3C) of the bits-per-word count and the normal and inverted output from the units diode gate (D3A) from the bits per character count. These two binary digits are effectively compared in the diode gate (5A, sheet B) (i.e., if pins 2 and 4 have -10-volt input, -10 volts is available at pins 5 and 1). The voltage at pin 1 is designated the borrow pulse. It is applied to current driver 7A and CSR 6A. If it is -10 volts, it is

designated as borrow (B); if 0 volt, it is inverted by CSR 6A and designated borrow (B). If pins 7 and 9 have -10 volts applied, the -10-volt output is pin 10. Pin 1 is 0 volt.

The same general process is followed for the tens, hundreds, and thousands position. There are slight differences however. One of these differences is that the tens position consists of five diode gates (5B through 9B) in a matrix-type arrangement. The diode gates are used as 3-input AND gates in this particular application because the B or  $\overline{B}$  signal must be considered. The input to the five diode gate matrix is from the set and reset side of the apparent tens stage (C4C) of the bits per word count shift register and the normal and inverted output from the tens diode gate (D3B) from the bits-per-character count. Hence, these five diode gates act as a decoding and comparison matrix for the tens position of the two binary digits. When three inputs (pins 2, 4, 7) on any one diode gate have -10 volts applied simultaneously, a -10-volt output is available at both output pins 5 and 10. One of the output pins from each of the five diode gates is tied together as a common point so that, if any one of the diode gates has an output, the B and  $\overline{B}$  functioning is generated. The other output pins from the diode gates are tied together and applied to current driver B3D. The current driver applies the output to diode module C2A pin 9 (sheet C).

The hundreds matrix (sheet B) is functionally the same as the tens matrix in that five diode gates (5C through 9C) are used as 3-input AND gates. This is necessary, just as in the tens matrix, to detect the B or  $\overline{B}$  pulse.

The apparent hundreds stage of the bits per word count (shift register stage C5C), both set and reset sides, is applied to the five diode gate decoding and comparison matrix. In addition, the normal and inverted output from the hundreds bits per character switch setting (D3C) is applied to the matrix. Again, one output pin of each diode gate is connected as a common point to create the B or  $\overline{B}$  pulse. The output from the other pin is routed through current driver B6D and applied to diode gate C3A pin 9. Hence, the three binary bits, the hundreds position of the bits per word count, the hundreds position of the bits per character count, and the B or  $\overline{B}$  from the tens position are compared.

The last digit compared is the thousands position. The set and reset side of the bits-per-word shift register stage C6C is applied to diode gate B10B. The other two inputs are the B or  $\overline{B}$  function from the hundreds position. The borrow pulse is also ANDed (9D) with the reset side of stage C6C from the bits per word shift register. A binary one output is available only when both inputs are 0 volt. All other times the output of

the AND gate is 0 volt. The output is applied to AND gate C8C. The other input to the AND gate is from the set side of shift register stage C7C of the bits-per-word shift register. This stage contains a zero until a shift of the bits-per-word count places a one in it. The bits-per-word count must be 64 (maximum data word length) to place a one in the stage on the first shift. Hence, at least one shift is always made unless the B/CH and B/W switch settings are the same or B/W count is 4. The output of this AND gate determines whether a shift is to be performed or not. A -10-volt output designates that the bits-per-word count must be shifted right one place and another subtraction performed; while a zero output from the AND gate designates no shift and the remainder in the bits per word shift register in the number to be set into the down counter.

When the AND gate produces its normal saturated output of -10 volts, it is applied to CSR 5A, where it is inverted and applied to pin 7 of diode gates 1A through 4A. The inverted pulse is also applied to CSR 6A, where it is again inverted and applied to pin 2 of the four diode gates. This -10-volt signal applied to pin 2 makes a shift possible if a binary one is contained in the set side of the associated shift register stage, the output of which is applied to pin 4. These two -10-volt levels applied to adjacent pins produce a -10-volt output at pin 5. This output is applied to the next shift register stage and places a binary one in the set side. This effectively shifts the binary one to the next stage of the shift register.

The new count is compared again in the calculator unit just as in the previous discussion. The sequence continues until there is no carry from the hundreds position and the reset side of C6C is 0 volt. This causes AND gate B9D to produce its normal unloaded output of -10 volts. The output, when applied to AND gate C8C saturates the gate and causes it to produce its 0 volt output. This is inverted by CSR 5A and applied to pin 7 of the diode gates. This means there is no output from the diode gates and the number still in bits per word shift register stages 4C through 7C is the number set into the down counter. The only exception to the above description is when the count of the bits per word is four. Because the incoming data is delayed only four bit times, there is not time enough for the calculator to attempt a subtraction process. For this reason the count must be recognized immediately and set into the down counter with minimum delay in order to format the character. This is done by decoding the bits per word count from the stored program processor as soon as it is sent to the six-stage storage register (sheet B). The count is decoded by AND gates and all inputs are zero if the count is four bits per word. This causes the gates to produce their normal unloaded pulse of -10 volts. This pulse is applied to pin 5 and sets CSR module B7E.

The 0-volt output from the reset side is fed back to the steer set input at pin 4 and is also applied to power inverter B10E. The inverter applies the -10 volts inverted pulse to AND gates E7A, E8A, and E9C (sheet E). This inhibits the calculator from making an input to the down counter.

The WS pulse from the previous word shifts the bits per word count out of the storage register and into the bits per word shift register (sheet C). This count is immediately applied to the down counter so that formatting of this four-bit character can be performed immediately. During the time the character is being formed, the count of the bits in the next data word is sent from the stored program processor. If this count is not four, the output of the decoding AND gates is 0 volt. When the next  $T_1$  delayed pulse occurs, at the start of formatting the next data word, CSR module B7E is reset. The -10 volts applied at pin 4 insures that the module stays reset, regardless of the number of  $T_1$  delayed pulses applied, until it is set again by a -10-volt pulse at pin 5.

#### 6.2.2.4 Down Counter

The down counter is a four-stage counter. Each stage of the counter is made up of two CSR modules connected to act as a flip-flop. The reason for this is to provide additional discrete inputs to exercise the control needed over the down counter.

When the subtraction process is complete, and the remainder in bits per word shift register stages C4C, 5C, 6C, and 7C is applied to the down counter, the bits are applied to AND gates 2A, 4A, 6A, and 10C (sheet E). The other input to the AND gates is from diode gate D2D, which is the 2<sup>3</sup> bits per character switch setting. The calculator cannot distinguish whether a number is decimal 8 or greater or 7 or less. The truing input to the four AND gates, if it is zero, means that the number of bits per character is less than 8 and the number is shifted left one position. If the signal is -10 volts it is inverted and applied to AND gates 2A, 4A, 6A, and 7B. This allows the number to be entered in a straightforward manner and indicates that the number is 8 or greater. The manner in which this is implemented is as follows: The common input to AND gates E7A, E8A, E9C from AND gate 10E (sheet B) is a 0 volt level except when the bits per word count is 4. This means that pin 3 of AND gates E7A, 8A, and 9C have a 0-volt input whenever the count remaining in the bits-per-word shift register is applied to the down counter. The counter counts down to zero at bit rate. Each count of the counter is applied to a decoding matrix composed of 15 4-input AND gates on sheet F. The output from each AND gate is the trigger input to a corresponding stage of the formatting register (sheet G). The trigger input occurs during the last half of

the bit period and allows the data word to be gated into the stage during this portion of the bit period. The set side of each of the 15 stages of the formatting register (storage sheet) are applied to pin 7 of an associated diode gate (sheet L). The same output is applied to pin 2 of the diode gate associated with the output from the up counter, hence depending upon the level of the MSB first or LSB first signal (sheet M) the output from the storage register is crossed over again or presented as an output. This depends upon which counter was forming the LSB character. The LSB character is the one made available to the computer so it may be necessary to cross it over so that it is applied to the proper output jack settings.

The first character is usually established from the calculator as follows: The level applied from the 2<sup>3</sup> switch position is used to identify whether the remainder in the bits per word shift register is equal to decimal 8 or more or 7 or less. If the switch is open, the level is -10 volts, signifying the number is 8 or greater. This level is applied to AND gates E1A, 3A, 5A, and 8C. The level saturates the gate and causes it to produce its saturated 0 volt output. This is applied to the following AND gate stage as a 0 volt input. The level is also applied to power inverter E10A where it is inverted and applied to AND gates E7B, 6A, 4A, and 2A (sheet E). The remainder is from the set side of the bits per word shift register stages 4C, 5C, 6C, and 7C. If the bit is a zero it trues the AND gate and causes it to produce its normal unloaded output of -10 volts. This is applied to the following AND gate stage and saturates the gate.

The output of gates 7A, 8A, and 9A are ANDed with new word and the output of calculator zero detector AND gate B9E (sheet B) which is always 0 volt unless the bits per word and bits per character are the same. The count bit is applied to AND gate 1B (sheet E) and through inverter 9B to AND gate 1C. If the bit is a one, inverter 9B inverts it and applies it to AND gate 1C, the gate is trued and the resulting -10 volts output is the binary one bit. All four stages of the down counter are loaded with the remainder from the bits per word shift register in the same manner. The output of the down counter is applied to a decoding matrix (sheet F) that is composed of 15 4-input AND gates. The matrix is trued from right to left with each count. When AND gate 6C is trued, which corresponds to the last count in the counter, the recycle logic is energized and applies a 0 volt pulse to AND gates 2B, 2C, 4B, 4C, 6B, 6C, 8B, and 8C (sheet E) for one clock period. The character switch settings are applied to AND gates 2C, 4C, 6C, and 8C and through power inverters to AND gates 2B, 4B, 6B, and 8B. This allows the down counter to be set from the switch settings for the remainder of the characters in this particular data word. The calculator input is inhibited by a

summing AND gate B9E (sheet B) being true and giving the resulting unloaded -10 volts output. This output is applied to AND gates 1B, 1C, 3B, 3C, 5B, 5C, 7B, and 7C and acts as an inhibit level to the gates, thereby inhibiting the calculator from applying a count to the down counter and allowing the switch settings to do the setting.

The above described action continues, setting the down counter from the switch settings whenever the last AND gate in the 15 gate matrix is true until a new word starts and  $T_1$  is generated again, which happens at the first bit of every incoming data word.

The delayed data and data pulses are applied to formatting register stages (sheet G) 1A through 10A and 1C through 5C. The output from the AND gate matrix is the toggle input to the successive stages of the formatting register; hence during the first half of the bit period the data bit is applied and the last half of the period the toggle input places it into the stage.

The set output from the 15 stages of the formatting register are applied to diode gate associated with each stage. The set output is also applied to the diode gates associated with the up counter. The other signal applied to all 30 diode gates is the MSB or LSB signal. If the data is MSB first, the output from the down counter formatting register is gated through and made available as an output.

# 6.2.2.5 Up Counter

The output of diode gates 1A through 1D (sheet D) are applied to pin 4 of diode gates K1A, K3A, and K4A and pin 9 of diode gates K2A (sheet K). In order for an output to be available as a result of this, -10 volts must be applied to pin 2 of diode gates 1A, 3A, and 4A and to pin 7 of 2A. This is accomplished by the output of counter stages K3E and K10E being applied to the diode gates. The counter is an up counter with stage 3E as MSB and 10E as LSB. The counter, of course, counts randomly with the clock input until it reaches a count that coincides with the switch settings applied to diode gates K1A through K4A. This count is binary 1011 (or decimal 11), with the four diode gates producing their -10 volts output; the four AND gates 1B through 4B produce their normal saturated output of 0 volt. These are applied as inputs to AND gate K5B. The resulting -10-volt output is applied to AND gate K1C and to the set side of flip-flop 2C. The 0 volt output from AND gate 1C has no effect on the flip-flop. The coincidence of clock with the 0-volt output from the reset side of flip-flop cause it to true the AND and produce its normal unloaded output of -10 volts. This output is routed through emitter follower K5C, where it resets the counter to a count of 1000. The counter

always starts with a count of 1000 in it and counts at clock until the diode gates are trued with a negative input on adjacent pins at the same time. The reason for starting at 1000 is that, with a four-stage counter, it is possible to have a total count of 16 if the all-zero condition is considered. Because the maximum bits per character is 15, it is not necessary to decode the 0000 condition because it is not used. The resulting output pulse, which is one-half bit period wide, resets the counter to 1000 again.

The counter can also be reset to a count of 1000 by coincidence of  $\overline{\text{clock}}$  and  $\overline{\text{T}_1}$  delayed through AND gate K5A.

As the counter is counting at the rate of  $\overline{\text{clock}}$ , its count is also being applied, through power inverters 3D through 10D, to true the AND gate matrix. The matrix consists of 15 AND gates, each gate associated with a bit of the character for a maximum of 15 bits per character. The count of 1000 is decoded to apply a -10-volt pulse at the toggle input of the first stage of the 15-stage formatting register (sheet L). Each AND gate is associated with a stage of the 15-stage decoding matrix. With serial data being applied to the set side of the formatting register and data being applied to the reset side, the binary data word is gated into each stage with the toggle output from the AND gate decoding matrix. The data is now formed into the desired character length when it reaches the formatting register (sheet L); each stage of the formatting register is applied to a corresponding stage in the parallel register (sheet M), 1C through 10C and 1B through 5B. The contents of this 15-stage parallel register are applied to pin 7 of diode gates 1B through 10B and 1D through 5D (sheet L) in a parallel transfer as a result of the correct count being obtained at K5C10 (sheet K) or  $\overline{\text{clock}}$  and  $\overline{\text{T}_1}$ , delayed coincidence at K5A10.

With every binary one being applied to pin 7 of diode gates 1B through 10B and 1D through 5D (sheet L) and the MSB first identifying level applied to pin 9 of the same gates, the first bit of data is gated into the first stage of the formatting register and the following bit in succession.

Sheet H contains the logic that generates the character rate pulses and the pulse that identifies when a new character is starting. These two pulses are sent to the computer interface unit and allow the unit to identify the data character length.

The prime frame recycle, pulse which is generated at the end of every prime frame, is ANDed (H2A) with the word sync pulse which occurs during the last half of the last

bit of every word. The output of this gate is applied to the set side of CSR H3A. The toggle to the modules is the LSB truncated pulse, which is generated at the end of every truncated character. This effectively delays the output pulse from current driver H5B by two characters, thereby making certain that the last truncated character out of the machine is provided as an output.

The next word starts with the prime frame sync pulse. This pulse is applied to the set side of CSR 2D. The truncation process starts again on the data word. When the down counter reaches zero from its first character formation, the resulting pulse is applied to the reset side of CSR 3D. This pulse, in turn, is applied to the set side of 4D. This set output is applied to the computer interface logic and lets it know that the first truncated character of the next word is available.

AND gates H6D and H7D are associated with the up counter and MSB first signal and the down counter and the MSB first signal. These two gates, in effect, establish the "character rate" pulses from the MSB switch settings and the LSB switch settings. In this manner the computer knows how many bits are in the truncated characters.

## 6.3 DECIMAL DISPLAYS CONTROLS AND INDICATORS

Three identical decimal displays are provided; they are located in assembly locations 2A3, 2A4, and 2A5. A listing of the controls and indicators and their function is presented in Table 6-3. A front panel view of one decimal display is shown in Figure 6-6.

Table 6-3

Decimal Display Controls and Indicators

Control/Indicator	Function	
WORD NUMBER thumbwheels	Provides display selection capabilities for 4096 data words. Thumbwheels are coded in octal (0-7).	
Display window	Displays decimal value of word selected by WORD NUMBER thumbwheels. Dis- play capabilities up to decimal 999,999; however, only 999 is presently used.	

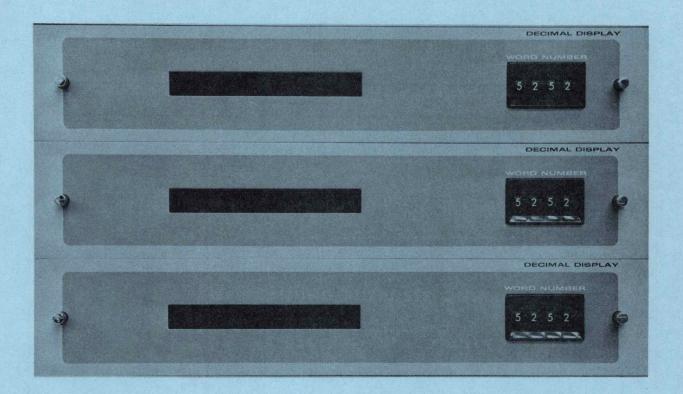


Figure 6-6. Decimal Display 2A3, 2A4, and 2A5 Front Panel

# 6.4 BINARY DISPLAY CONTROLS AND INDICATORS

The controls and indicators for binary display 2A6 are shown in Figure 6-7. A listing of the controls and indicators and their functions is contained in Table 6-4.

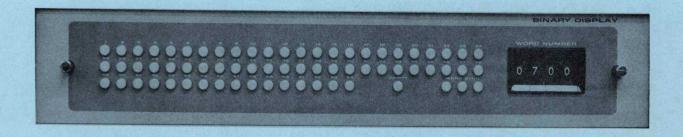


Figure 6-7. Binary Display 2A6 Front Panel

Table 6-4
Binary Display Controls and Indicators

Control/Indicator	Function	
WORD NUMBER thumbwheels	Provide display selection capabilities for 4096 data words. Thumbwheels are coded in octal (0-7).	
Display Indicators  1 through 64	Display the binary value of word selected by WORD NUMBER thumbwheels. Illu- minated when value of bit is a binary ONE.	
PARITY indicator	Displays the value of the parity bit for word selected. Illuminated when parity of word selected is even. Parity bit is stripped from data word displayed on indicators 1 through 64.	
WORD SYNC indicators	Display the binary value of word sync for word selected. Illuminated when value of bit is a binary ONE. Word sync bits are stripped from data word displayed on indicators 1 through 64.	

## 6.5 <u>DECIMAL AND BINARY DISPLAYS</u>

## 6.5.1 GENERAL

Three decimal displays and one binary display provide the capabilities for selecting and displaying the decimal and binary values of words from registers in the output cabinet. The three decimal displays are mounted assembly locations 2A3, 2A4, and 2A5; the binary display is mounted in assembly location 2A6. The thumbwheel switches, logic and display indicators comprising each display are contained within a single drawer assembly.

The three decimal displays operate independently, that is, all three can be used concurrently to select and display one word or three different words. Any word in the data train up to octal 7777 (decimal 4095) can be selected on any one display. The decimal displays are wired for word values up to 999,999; however, the displays only contain modules for word values up to 999.

The binary display provides the capabilities for selecting and displaying any of 4096 data words. A 64-bit word plus parity can be displayed. In addition, word sync is also displayed.

The decimal and binary displays function identically, except for the fact that the decimal displays must decode the BCD inputs. For that reason, only a decimal display is discussed and only one block diagram is presented. The decoding operation performed for decimal display can be ignored when evaluating the operation of the binary display. A block diagram discussion and basic timing follows.

#### 6.5.2 BLOCK DIAGRAM ANALYSIS

Functionally, a decimal display consists of four-word select thumbwheel switches, an address comparator, latching logic, indicator drivers used as a BCD-to-decimal decoder, and decimal display indicators as shown in Figure 6-8. When a specific word in the data train is to be observed, the octal value of the address associated with a word in the data train must be entered using the thumbwheel switches on the display front panel. Each switch is an octal-coded, 8-position, continuously rotating type. Each switch furnishes a 3-bit binary code as an input to the address comparator. Word addresses (bits 0-11) from the display address register of the output cabinet are compared with the 12-bit switch-programmed input. The word addresses appear in coincidence with the data word from the output cabinet. Therefore, immediately following a favorable comparison, the address comparator sends an unlatch pulse to the latch and unlatch control circuitry. This circuitry, in turn, unlatches the BCD-to-decimal decoder and indicator circuits and clears the indicators of any previously stored display. Subsequently, the address comparator furnishes a strobe pulse to the BCD-todecimal decoder and the BCD data word is converted to a decimal output that drives the decimal indicators. When the BCD data word is strobed, interaction between the indicators and the unlatch and latch circuitry causes this circuitry to return a latch level to the BCD-to-decimal decoder, and the active decoder and display indicator remain on.

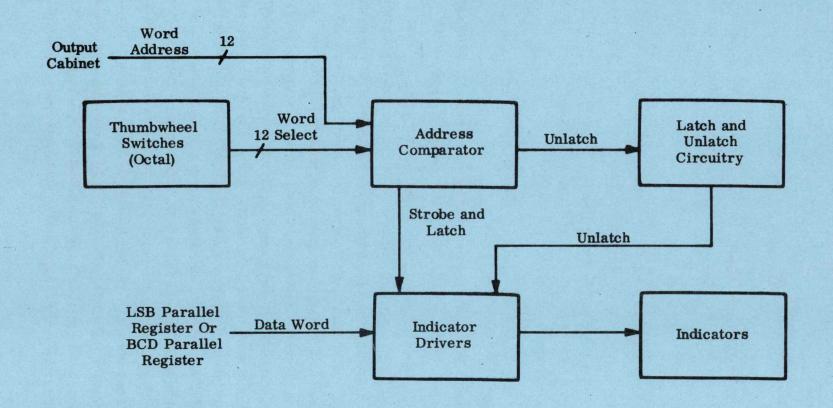


Figure 6-8. Decimal and Binary Displays Block Diagram

#### 6.5.3 DECIMAL DISPLAY LOGIC DISCUSSION

The logic for the decimal display is shown in figure 6-50, sheets A through D. As mentioned previously, the four thumbwheel switches on the display front panel provide the means for selecting a specific data word. Each switch provides 3 bits of word select address to the modules forming the address comparator (see sheet A). Thus, for the four switches, a total of 12 bits of address are supplied to the comparator. The address is supplied in its normal and complement form.

The address comparator consists of 12 four-input diode gates (DG-1) whose other two inputs are the normal and complement form of the word address from the address register. For the function implemented, the normal and complement form of the address is ANDed with the complement and normal forms of the switch programmed address, respectively. For all practical purposes, each diode gate functions as a negative AND gate and the comparator supplies a binary one output for unfavorable comparisons. When two addresses correlate, the comparator furnishes a binary zero output. A timing diagram illustrating the selection of word 77 is shown in Figure 6-9. The two-address match occurs at the beginning of word 77 and is depicted in the timing diagram as the comparators output. This is inverted by power inverters A6E and A9E and is applied to differentiator (Dif) module A7D.

The Dif module triggers on the binary one-to-binary zero transition on its input and produces an unlatch pulse routed to the latching (L-2) modules associated with each indicator driver (ID) module. This output, as the name implies, is used to unlatch or clear the indicator circuits of any previously stored data. The unlatch pulse occurs during the first two microseconds that output word 77 is available. It causes the latching modules to return their latch control output to a near ground level. As a result, the ID modules break their return circuit to the indicators. With the indicators cleared, the data word for word 77 can be sampled, decoded, and displayed. This function is accomplished by the strobe and latch pulse which occurs approximately two microseconds after the lagging edge of the unlatch pulse.

The strobe and latch pulse is produced by a monostable multivibrator (comprised of modules A5D and A6D) and Dif module A8D. The monostable multivibrator is triggered by the lagging edge of the unlatch pulse, and its output remains at a binary one level for approximately two microseconds. This provides sufficient delay for latching circuits to break the indicator return circuits and for circuit transients. With the lagging

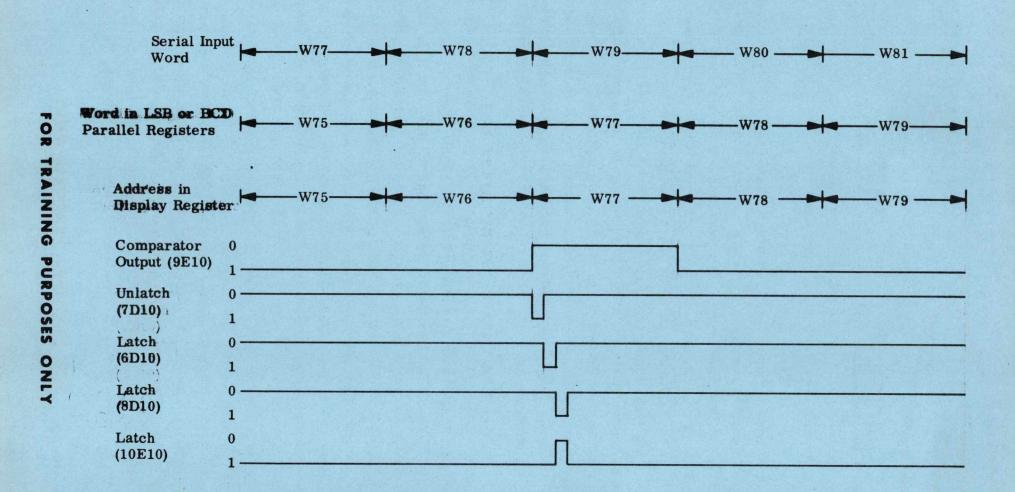


Figure 6-9. Decimal and Binary Display Timing Diagram

edge of the monostable multivibrators output, Dif module A8D is triggered and a 1-microsecond latch pulse is generated. This pulse is inverted by power inverter A10E and is routed to the indicator drivers by emitter followers.

There are six decimal-weighted groups of ID-6 modules used for the decimal display; one for units, tens, etc.; however, only three groups are presently used. Each group is comprised of 10 ID modules, one to decode each decimal digit (0-9) within the decimal-weighted groups. Each group decodes and stores (through the use of latching modules) the decimal equivalent of the BCD configuration on its four data input lines. An ID module is activated by all binary zeros on its input. With the arrival of the positive-going strobe and latch pulse, the BCD configuration of the data output word is sampled and one ID module in each decimal-weighted group is activated. The active ID module (through circuit interaction) causes its related latching module to produce a latch level which holds the decimal indicator on. As a result, the decimal display indicators display the output word until again cleared by the selection of another word.

#### 6.5.4 BINARY DISPLAY LOGIC DISCUSSION

The binary display functions are identical to the decimal displays, except that no BCD-to-decimal conversion is required. The logic diagrams for the binary display are presented in figure 6-51, sheets A through G.

#### 6.6 DIGITAL-TO-ANALOG CONVERTERS

#### 6.6.1 GENERAL

The digital-to-analog converters are provided to convert binary data words to analog equivalents for use by peripheral equipment. There are 60 digital-to-analog converters provided; 30 located in module panel assembly 4A5 and 30 in 4A6. The digital-to-analog converter address assignments and their location are listed in Table 6-5.

Any one of the 60 digital-to-analog converters can be selected to convert binary words from the MSB parallel register into an analog output. The digital-to-analog converters are selected by address inputs from memory. Each converter has the capabilities for converting the 8 most significant bits of a word in the MSB parallel register into a 0 to -5 volt output. In addition to the normal operating circuits, test circuits are provided that simulate an 8-bit word input, select each of the converters, and exercise them for conversions.

Table 6-5
Digital-to-Analog Converter Address Assignments and Locations

Converter No. Decimal	Location	Converter No. Decimal	Location
1	4A5A	31	4A6A
2	4A5B	32	4A6B
3	4A5C	33	4A6C
4	4A5A	34	4A6A
5	4A5B	. 35	4A6B
· 6 7 8	4A5C	36	4A6C
7	4A5E	37	4A6E
8	4A5F	38	4A6F
9	4A5G	39	4A6G
10	4A5E	40	4A6E
11	4A5H	41	4A6F
12	4A5G	42	4A6G
13	4A5K	43	4A6K
14	4A5L	44	4A6L
15	4A5M	45	4A6M
16	4A5K	46	4A6K
17	4A5L	47	4A6L
18	4A5M	48	4A6M
19	4A5R	49	4A6R
20	4A5S	50	4A6S
21	4A5T	51	4A6T
22	4A5K	52	4A6R
23	4A5S	53	4A6S
24	4A5T	54	4A6T
25	4A5W	55	4A6W
26	4A5X	56	4A6X
27	4A5Y	57	4A6Y
28	4A5W	58	4A6W
29	4A5X	59	4A6X
30	4A5Y	60	4A6Y

# 6.6.2 BLOCK DIAGRAM ANALYSIS

A block diagram of a digital-to-analog converter, the converter selection circuits, and test circuits is shown in Figure 6-10. The converter selection circuits consist of an input address register, address load gates, an address output register and a decoding matrix. Each digital-to-analog converter consists of an eight-stage register and eight digital-to-analog modules arranged in a digital-to-analog conversion ladder. A digital-to-analog conversion process is performed as follows.

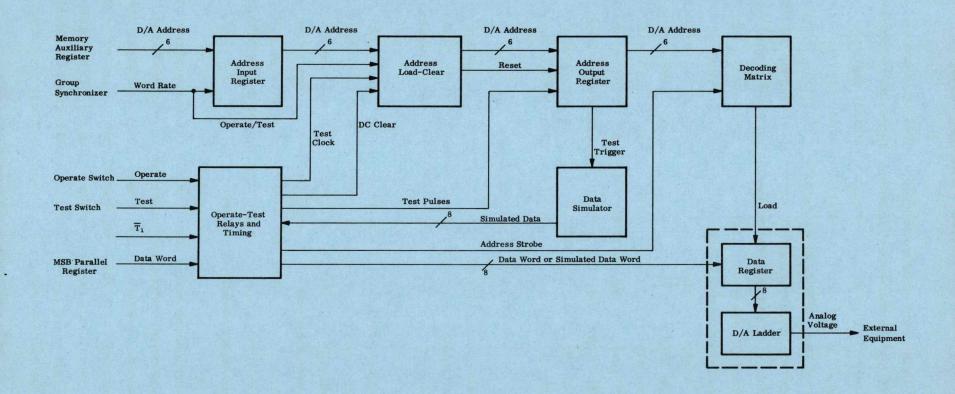


Figure 6-10. Digital-to-Analog Converters Block Diagram

Normal operation is initiated by depressing the OPERATE switch on module board assembly 4A5D. A six-bit address for selecting a digital-to-analog converter is entered into the input address register from the memory auxiliary register. These six bits correspond to bits 23 through 28 of a memory instruction word and are coded from decimal 1 through 60 (zero denotes no conversion is required). Loading of the six-bit address is accomplished by a word rate input and occurs during the last bit of a word time. Since the data word in the output cabinet is two words behind the memory instruction word, the digital-to-analog address must be delayed to load the correct data word into the specified converter. Since the address was stored at the end of a memory instruction word, a one-word time delay must be provided to have the address and data word coincide. The function is accomplished by leaving the address in the address input register for one word time, then transferring it into the address output register at the end of the word time. At the beginning of the next word time, the address is decoded and the eight-bit data word from MSB parallel register is loaded into the digitalto-analog converter specified by the address. In coincidence with this action, the output address register is cleared for receipt of another address at the end of the same word time.

The digital-to-analog conversion process is started with the loading of an eight-bit word into the data register of a converter. It entails the summation of analog voltages based upon the value of the binary word in the data register. The digital-to-analog conversion ladder consists of eight digital-to-analog modules connected to form a resistance ladder with the LSB stage of the ladder connected to the LSB stage of the data register. The LSB stage of the ladder furnishes a ground level output for a binary zero or 19.6 millivolts for a binary one in the LSB stage of the data register. Each succeeding stage adds multiples of 19.6 millivolts to the summation, based upon the binary ones in the data word. Thus, for a data word having a decimal value of 255, an analog voltage of -5 volts is furnished as an output. The analog voltage is available until a new word is loaded into the converter.

The test circuits included as part of the digital-to-analog conversion circuitry simulate digital-to-analog converter addresses and data words to exercise each of the 60 digital-to-analog converters for evaluation of their operation. As a safety precaution, the digital-to-analog test circuits cannot be activated when the system is operating on a program. A test operation is initiated by depressing the TEST switch on module board assembly 4A5D. This energizes five relays: one relay causes a disabling level (test) to be supplied to the address load gates and connects a test clock input to the address

output register; the other four relays permit a simulated data input to be used. The disabling level supplied to the address load gates prevents the loading of addresses from the address input register. For the test operation, the address output register is used as a six-stage counter. It is stepped through 64 states by the test clock input. Sixty of these 64 states are decoded by the decoding matrix and are used to select the digital-to-analog converters. An eight-stage counter is connected to the final stage of the address output register. This counter is used to simulate eight-bit words used as inputs to the digital-to-analog converters. It is stepped through 256 stages. It is advanced one state for each complete cycle of the address output register. As an end result each digital-to-analog converter is selected for one data word, and 256 different data words are supplied for test operation. Thus, each converter is exercised for each possible value of the eight-bit data word.

### 6.6.3 LOGIC ANALYSIS

The logic diagrams for 30 digital-to-analog converters and related control circuitry are presented in figure 6-52, sheets A, B, C, E, F, G, H, K, L, M, R, S, T, U, W, X, Y and Z. Thirty identical digital-to-analog converters are shown on the same sheets of figure 6-53. A timing diagram for normal operation is shown in Figure 6-11. Since the digital-to-analog selection circuits are conventional logic circuits, only a limited logic discussion of them is presented. Since each digital-to-analog converter operates identically, only one converter is discussed in detail.

The address input register consists of six bistable stages (six CSR modules) and six PI modules. The six stages are connected as a parallel storage register. The register is loaded by word rate input. The address input register is shown on sheet D. The address load and clear gates, the address output register and part of the decoding matrix are shown on 4A5H. The address load gates are standard three-input NOR gates that control the set inputs of the six-stage address output register. The part of the decoding shown on sheet H matrix consists of eight six-input diode gates (DG-1) (plus PI's per diode gate). It furnishes two outputs per stage to drive the decoding matrix on 4A5 and the decoding matrix for 4A6.

The timing and control logic, operate-test relay K1, and the balance of the decoding matrix are shown on sheet U. The eight-stage counter that generates the test words, the relays for selecting normal or test words, and the necessary drive logic are shown on sheet Z. The digital-to-analog data registers and the digital-to-analog conversion

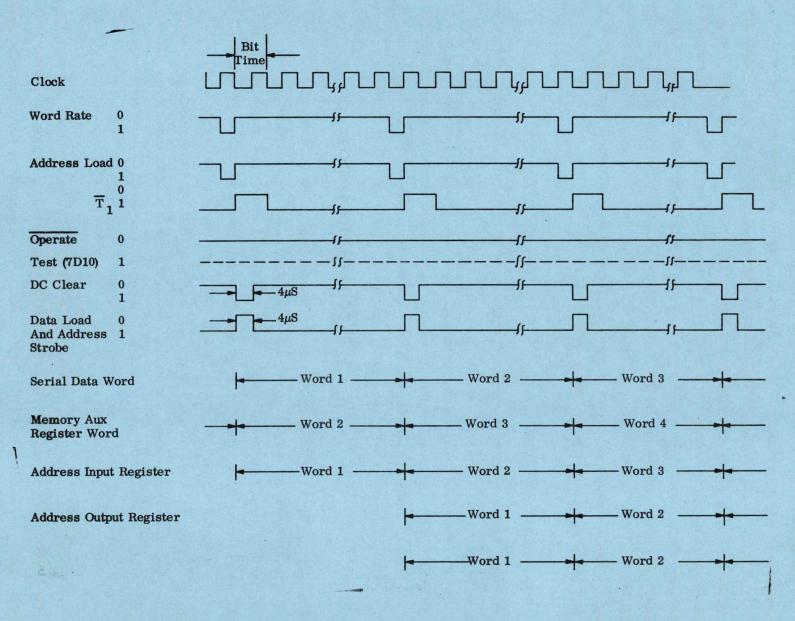


Figure 6-11. Digital-to-Analog Converters, Normal Operation Timing Diagram

ladders for 30 digital-to-analog converters are shown on sheets A, B, C, E, F, G, K, L, M, R, S, T, W, X and Y. Thirty identical digital-to-analog converters are shown on the same sheets of 4A6. A description of a digital-to-analog conversion for normal and test operations follows.

The control for normal or test operation is supplied by two momentary switches on module assembly board 4A5D. The switches control the energizing of five relays. One (5U9E) selects normal or test timing. The other four relays select a normal or test word input for application to the digital-to-analog converters. When the OPERATE switch (sheet D) is depressed, the holding circuit to relay 5U9E is opened and the normal operation timing logic (sheet U) is enabled. With the arrival of the next word rate input, a six-bit address from the memory auxiliary register is entered into the address input register (sheet D). In coincidence, the address loaded into the address input register by the previous word rate input is loaded into the address output register by the address load gates (sheet H). During the first bit time of the next word, a 4-microsecond pulse (normal and inverted form) is generated by the timing logic. The pulse is generated from the leading edge of  $\overline{T_1}$  input. The inverted form of the 4-microsecond pulse is used to strobe the decoding matrix (sheets H and U) connected to the address output register. As a result, the decoding matrix generates a load signal for the digital-to-analog converter specified by the address. (A no load signal is generated if the address code is all zeros.) The load signal causes an 8-bit data word from the MSB parallel register to be entered into the data register of the specified converter. In coincidence with this action, the address output register is cleared by the normal form of the 4-microsecond pulse applied to the dc reset of the address output register stages. This function is accomplished by a 2-input AND gate and buffer amplifier BA also on sheet H.

Assume that a valid address was decoded and that an 8-bit data word has been entered into the digital-to-analog converter data register composed of modules 5A1A through 5A10A, 5A1B, 5A2B, and 5A2C through 5A5C (sheet A). With the data entry, the digital-to-analog resistance ladder (modules 3B through 10B) begins the conversion summation process. Module 10B is connected to LSB stage (modules 4C and 5C) of the data register. If a binary zero is in the LSB stage, the digital-to-analog module supplies a ground level input to the next least significant stage (module 9B) of the resistance ladder. If a binary one is stored in the LSB stage of the data register, module 10B supplies approximately 9.6 millivolts to module 9B. Similarly, module 9B supplies a 0-volt level or approximately -39.2 millivolts to the summation if a

binary zero or a binary one, respectively, is stored in the second least significant stage of the data register. Each more significant stage of the digital-to-analog ladder supplies multiples of 19.6 millivolts if a binary one is in the corresponding stage of the data register. The total summation of outputs from all stages of the digital-to-analog resistance ladder results in an analog voltage output from 0 to -5 volts, based upon the binary configuration of the data word.

For the more explicit example, assume that the data word is binary 00010101 LSB (decimal 21). For this example the LSB stage furnishes 19.6 millivolts to the summation; the third least significant stage supplies 78.4 millivolts and the fifth least significant stage supplies 313.6 millivolts. All other stages supply a 0-volt level. The total summation results in analog voltage output of 401.6 millivolts for the decimal 21 input. This output is made available to external equipment.

As mentioned previously the test circuits simulate digital-to-analog converter addresses and test data words. For test operation, the normal address and data word inputs are inhibited. The generation of test addresses is accomplished by using the address output register (sheet H) as a six-stage, 64-state counter. Test data words are generated by an eight-stage, 256-state counter (sheet Z) connected to the final stage of the address output register. Timing for the test operation is supplied by the logic shown on sheet U. The balance of the digital-to-analog converter circuits operate the same as described above.

When the TEST switch on module board assembly 4A5D is depressed, relays K1 (5U9E), K1 (5Z2B), K2 (5Z2C), K3 (5Z2D), and K4 (5Z2E) are energized and remain energized by a holding circuit connected in series with the OPERATE switch. Relays K1 (5Z2B), K2, K3, and K4 open the input data lines from the MSB parallel register and select the outputs of the eight-stage counter used as a data simulator. Relay K1 (5U93) interrupts normal operation timing and selects test operation timing (shown in Figure 6-12) by furnishing a 0-level output. This output is inverted by PIU9A and disables the address inputs to the address output and inhibits clearing the register. It also enables the triggering of the first monostable multivibrator (modules 3E and 4E) by causing a one-to-zero transition on the output of module 10B. The first monostable multivibrator is connected to remain on for 4 microseconds. Its output is inverted by PI5E and is used to strobe the address-decoding matrix. The lagging edge of its output triggers a second 4-microsecond monostable multivibrator (modules 9D and 10D). This stage produces the test clock pulses used to step the address output register

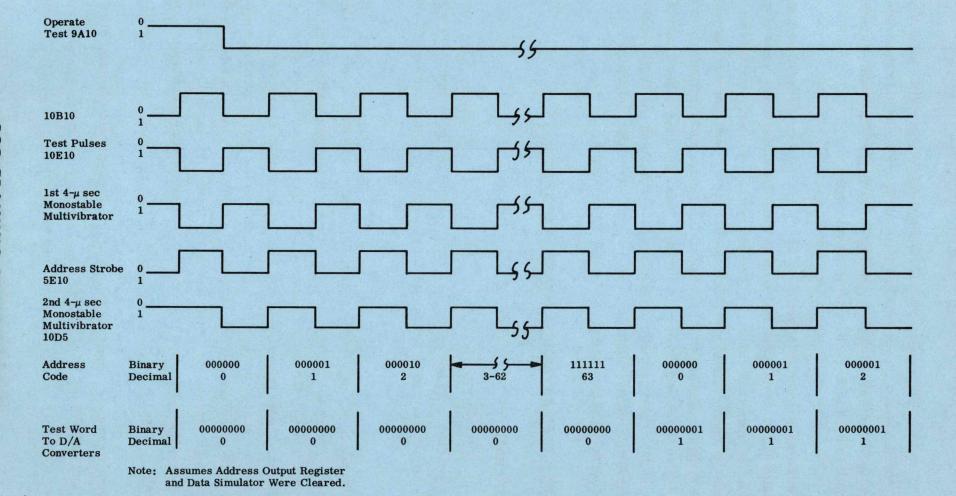


Figure 6-12. Digital-to-Analog Converters, Test Operation Timing Diagram

through its 64 states. The lagging edge of its output also triggers the first 4-monostable multivibrator again. Thus, the two monostable multivibrators generate an 8-microsecond square wave; the first half is used to strobe the decoding matrix and the second half is used to step the address output register.

The relative timing diagram in Figure 6-12 also illustrates the address code outputs of the data simulator. It assumes that both of these functional areas were cleared at the start of a test operation; however, this may not be the case. In any event, the address register (sheet H) is stepped through 64 states. Each time it is stepped through 64 states, it triggers the data simulator once. This causes the data simulator (sheet Z) to advance one state out of 256 possible states. Thus, when the address output register has completed 256 cycles or the data simulator has completed one cycle, each digital-to-analog converter has been tested for each of 256-word-input combinations. A test operation is terminated by depressing the OPERATE switch.

## 6.7 BINARY-TO-BINARY CODED DECIMAL CONVERTER

#### 6.7.1 GENERAL

The binary-to-BCD converter accepts MSB first serial PCM data from the signal conditioner (bit synchronizer) and produces a binary coded decimal output. This BCD output is routed to the displays in cabinet 2A to be displayed from a zero to 255 decimal value.

All data, regardless of a request for binary-to-BCD conversion, is input to the converter shown in Figure 6-13. The clock input to the timing and control logic generates shift pulses which are of the same frequency and phase as the bit rate generated by the bit synchronizer. These pulses allow the NRZ bit weights to be loaded into the first converter register and the decaded bit to be shifted to the next sequential stage. As the shifting takes place through the converter, conversion to BCD is made so that when a load strobe is generated, the converted data is loaded into the BCD parallel register. Therefore, the actual conversion is performed during the time the word is entering the decommutator.

From the parallel register, the data is loaded into the applicable decimal display and remains in the register for one word time.

The hash marked blocks in Figure 6-13 are not used in ACE-S/C.

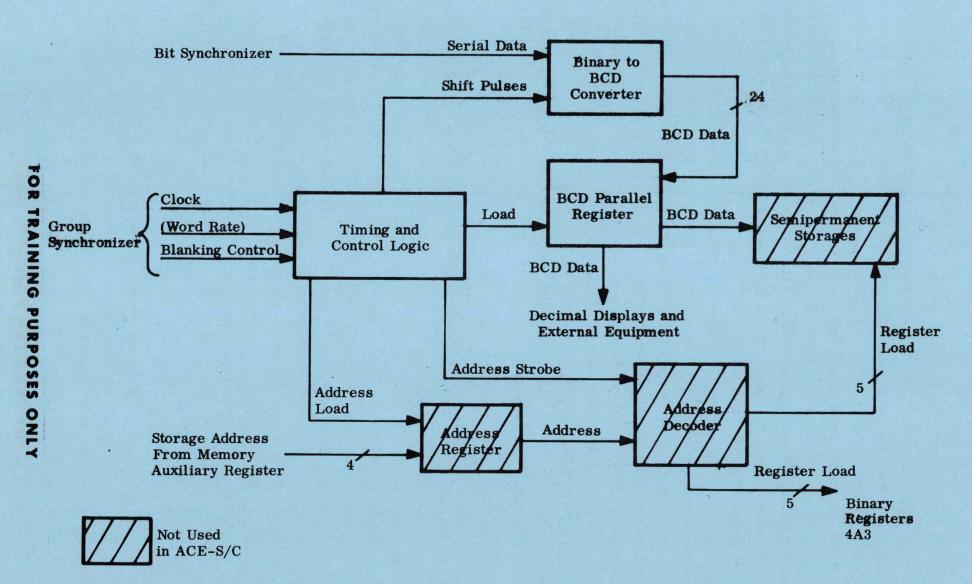


Figure 6-13. Binary-to-BCD Converter, Simplified Block Diagram

#### 6.7.2 FUNCTIONAL DESCRIPTION

The binary-to-BCD converters use the basic principle of a scheme called BIDEC. This conversion scheme makes use of the fact that the decimal value of any binary one digit in a binary number has the value of  $2^{n-1}$ , where n is equal to the location of the digit in question from the least significant digit end of the binary word. Also, the fact that if a digit is shifted one place toward the MSB end of a register, the decimal value doubles for the shifted digit. As an example, if a binary word of 10010 is shifted right one place the value changes from a decimal 9 to a decimal 18. When the LSB of one is shifted right its value now becomes 2.

To perform the conversion for the 8-bit word used in ACE-S/C, three decades are required as shown in Figure 6-14 and are increasing in the direction of shift. Additionally, each decade uses four stages for conversion. These stages increase in weight in the direction of shift, and the weights are 1, 2, 4, and 8, respectively. T1 represents the initial bit in to the converter and is the MSB of the 8-bit word. As the data is loaded and shifted right, its value is doubled. At T3 time the value is a decimal 5; however, on the next shift, a zero is shifted in and the decimal 5 becomes a decimal 10. Since the maximum value that can be contained in a BCD register is 9, a conversion must take place.

And as shown in Figure 6-14, a carry pulse is forwarded to the tens decade and places a one in the least significant stage of the tens decade. The action of the conversion forces the units decade to an all zero state and the total decimal value remaining is 10. The same holds true for time T7 where the decimal value is 84. In the next shift pulse, the 4 of the units decade is doubled and a one added to the LSD stage thus producing a decimal value of 9. The decimal 8 in the tens decade was doubled when shifted, thus producing a value of 16. Since the highest number per decade is 9, a one is carried forward to the LSD of the hundreds decade and the conversion logic produces a 6 in the tens decade. At this point, a word rate pulse occurs (a BCD load) and transfers the BCD value of 169 to the storage registers where storage is maintained for one word time. On the next bit in from the bit synchronizer another conversion begins for the next word time.

The timing for the binary-to-BCD converters is shown in Figure 6-15. If word sync or word parity is used a blanking pulse from the group synchronizer inhibits loading the first bit and prevents shifting until the first data bit is present. In ACE-S/C word sync and/or word parity are not used.

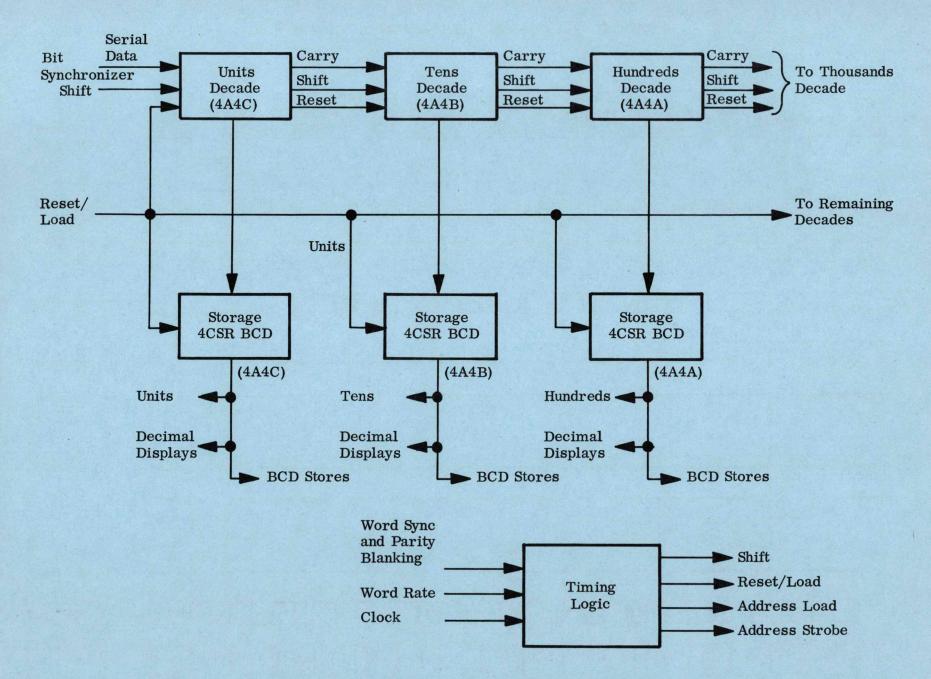


Figure 6-14. Binary-to-BCD Register and Converter

FOR TRAINING PURPOSES

ONLY

Bit

TRAINING PURPOSES ONLY

| WS | WS | 1 | 2 | 3 | 4 | 5 | 59 | 60 | 61 | 62 | 63 | 64 | P |

and two word sync bits at the beginning of word.

Timing is depicted for a data having a parity bit at the end of word

The logic for the binary-to-BCD converter is located on Figure 4-37 the logic document.

Table 6-6

LSB

	Binary Value			Un	Serial Data = 10010101 Units Tens						Hundreds			
			1	2	4	8	1	2	4	8	1	2	4	8
Load	T1	1	1	0	0	0	0	0	0	0	0	0	0	0
	<b>T2</b>	0	0	1	0	0	0	0	0	0	0	0	0	0
	Т3	1	1	0	1	0	0	0	0	0	0	0	0	0
	<b>T4</b>	0	0	0	0	0	1	0	0	0	0	0	0	0
	<b>T</b> 5	1	1	0	0	0	0	1	0	0	0	0	0	0
	Т6	0	0.	1	0	0	0	0	1	0	0	0	0	0
	Т7	0	0	0	1	0	0	0	0	1	0	0	0	0
	Т8	1	1	0	0	1	0	1	1	0	1	0	0	0

#### SECTION 7

#### COMPUTER INTERFACE UNIT

## 7.1 INTRODUCTION

The computer interface unit enables a free exchange of data and instruction between the Radiation Series 540 PCM Acquisition and Stored Program Decommutator System and a digital computer. Toward this end the unit decodes various instruction inputs from the computer and causes the decommutator to comply with them. It then provides a path through which program instructions can be transferred from the computer to the decommutator's memory. It also provides a transfer path for data words sent from the decommutator to the computer. As part of these functions, the unit converts the logic levels used by the computer to those used by the interface unit. Transfers from the decommutator to the decommutator are designated as input transfers. Transfers from the computer to the decommutator are designated as output transfers. These terms are used throughout the discussion and on the diagrams. All transfers are parallel bit-by-bit transfers.

Table 7-1 contains a listing of all operating controls and indicators. The table contains the name of the control or indicator and a brief statement of its function. Figure 7-1 is a front panel view of the computer interface unit. The associated logic prints consist of pages "A" through "F" of Figure 7-1 (logic print book).

#### 7.2 COMPUTER INSTRUCTION WORDS

The computer is capable of sending 17 different instruction words to the interface unit. Each word is 12 bits long. The instruction words, upon entering the interface unit, are broken into groups of three bits (designated octaves) to be decoded by a matrix. The outputs of the four matrices (one for each 3-bit octave) are applied to a final matrix which ANDs the output with a unique signal input from the computer. This final output causes the interface unit to decode and store the instruction requested.

RADIATION INCORPORATED MODEL 5401

3×62

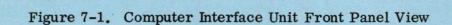
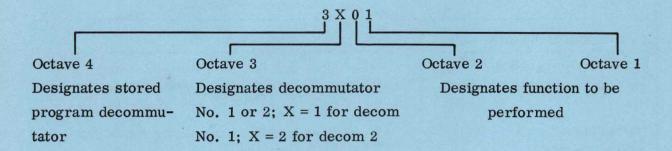


Table 7-1
Controls and Indicators

Control/Indicator	Function
LOADING PROGRAM Indicator (yellow)	Indicates that the computer is loading a new program, modifying an existing program, or checking the accuracy of an existing program.
RECEIVING DATA Indicator (green)	Indicates that the computer is receiving data from the decommutator.
NO EXCHANGE Indicator (white)	Indicates that there is no interchange of information between the computer and decommutator.
INTERRUPT 1 Indicator (red)  DECOM (Decommutator)	Indicates that one prime frame of data has been successfully transferred from the decommutator to the computer. Computer has to ask for PF by PF it would
UNIT 1 (white) 2 (white)	Indicates decommutator unit 1 is on line. Indicates decommutator unit 2 is on line.
INPUT DISCONNECT/ INTERRUPT 1 Toggle Switch	
INPUT DISCONNECT Position	Enables input disconnect output to computer and allows decommutator to send more than one prime frame of data to the computer without another external function code.
INTERRUPT 1	Enables Interrupt 1 output to computer and permits decommutator to send only one prime frame of data with each external function code.
POWER pushbutton switch indicator (white)	Applies ac input to -20-volt power supply.
UNIT 1/UNIT 2 selection switch	Located inside panel. Selects which unit is decommutator 1 and which is decommutator 2. (Observe front panel indicators.)

Table 7-2 lists the 17 instruction word inputs from the computer, their coding and their meaning. The codes are abbreviated throughout the text and in the diagrams. They are interpreted as follows:



### 7.3 DECOMMUTATOR WORDS

The interface unit sends three types of words to the computer; all types are sent upon request by the computer. The word types are: truncated data words or characters with a maximum of 12 bits per character, a 12-bit status word, and stored memory words. The truncated characters are received from the decommutator's LSB truncated character register in cabinet 4A. They are converted to logic levels compatible with that of the computer and are transferred to the computer in broadside form. The status word is partially generated within the interface unit and the decommutator. It informs the computer of the current status of the decommutator at the request of the computer. The status word and the meaning of each bit are shown in Figure 7-2. The stored memory words are the words in the program that the computer may want to check.

Octal
Equivalent
Notation

Table 7-2 Computer Instruction Words

17e 4 17e 3 17e 2 17e 1	Octave 4	Octa		Octave 2		Meaning
Octave Octave Octave Octave	2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup>	2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup>	22 21 20	22 21 20	2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup>	
3 X 0 1	011	0 0 1 or	010	000	001	Select Input
3 X 0 2	011	0 0 1 or	010	000	010	Select Output
3 X 1 1	011	0 0 1 or	010	001	001	Select Program 1
3 X 1 2	011	0 0 1 or	010	001	010	Select Program 2
3 X 1 3	011	0 0 1 or	010	0 0 1	011	Select Program 3
3 X 1 4	011	0 0 1 or	010	0 0 1	100	Select Program 4

Octal Equivalent Table 7-2
Computer Instruction Words (Cont.)

Notation

Octave 4 Octave 3 Octave 2 Octave 1	Octave 4 2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup>	Octav 2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup>		Octave 2 2 2 2 2 2 2 0		Meaning
3 X 1 5	011	0 0 1 or	010	001	101	Select Program 5
3 X 1 6	011	0 0 1 or	010	001	110	Select Program 6
3 X 1 7	011	0 0 1 or	010	001	111	Select Program 7
3 X 1 0	011	0 0 1 or	010	001	000	Select Program 8
3 X 2 0	011	0 0 1 or	010	010	000	Clear Decommutator
3 X 4 0	011	0 0 1 or	010	100	000	Status Request
3 X 5 0	011	0 0 1 or	010	101	000	Program Check
3 X 6 2	011	0 0 1 or	010	110	010	Enable DACI & Bank 2
3 X 6 4	011	0 0 1 or	010	110	100	Enable DACI & Bank 4
3 X 6 6	011	0 0 1 or	010	110.	110	Enable DACI & Bank 6
3 X 7 0	011	0 0 1 or	010	111	0 0 0	DACI Clear

## 7.4 BLOCK DIAGRAM ANALYSIS

A block diagram of the interface unit is shown in Figure 7-3. A relative timing diagram is presented in Figure 7-4. The interface unit receives 12-bit instruction words, 12-bit data words, and unique control signals from the digital computer. These inputs are converted from the logic levels used by the computer to those used by the interface unit by the input level converters. The word inputs are routed to the decoding matrix. The control inputs are routed to the instruction storage and control logic. This logic establishes the necessary gating and control functions, based upon the instruction word and unique signal inputs, for data transfers between the computer and the decommutator.

When the computer desires to transfer program data to the decommutator, it sends a clear decom instruction (3X20) and a function ready signal. These inputs are converted to logic levels compatible with those of the interface unit by the input level converters and are furnished to the decoding matrix and to the instruction storage control logic. The function ready input clears the bistable control logic of any previously stored instruction and enables the decoding of the clear decom instruction. The clear decom instruction is stored, then executed. The instruction clears the program storages, part of the status storages, and causes a clear decom output to be sent to the decommutator. This

Tored Prog

Bit 11

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	8
0 = Decom Able To Accept Data From Computer 1 = Decom Busy	0 = Data Sync Established 1 = Loss of Sync	Postition 1 = Local/Remote	0=Select Code Other than Status Request 1=Input Disconnect	0 = Interrupt 2 1 = Interrupt 1	0 = Decom not in Data Acqui- sition Mode 1 = Decom in Data Acquisition Mode	

Bit 6		Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	7
	Indica Form	e Below ates Which at Decom		Unused (Always 0)	Unused (Always 0)	0 = Some Function Other Than Status Request Selected By Computer 1 = Interrupt 1 or 2 Generator by Decom	AINING PU
22		21	20	1 stAc			R
				Parity Bit	20 A)CC		PURPOSE
Format 1	0	0	1	my Bet	Parix es		ES
Format 2	0	1	0		Jena		
Format 3	0	1	1				ONL
Format 4	1	0	0				7
Format 5	1	0	1	1 of Ac			
Format 6	1	1	0		ers - Naru	al CXP.	
Format 7	1	1	1	Frn	n Blk Con	A way	
Format 8	0	0	0	2d Acces	s - Nest.	al CARWY uter ddr, in Whener folies of Wed in	
					e 1	dar in Ulemer	100 1
				WZ	rel à a	1.1 Seg	A
	Figure	e 7-2. Twel	ve-Bit Status Respo	nse Word from Com	puter Interface Uni	faces of the	-co
						Dud in	X
							PACI
							~
							The second secon

output causes the decommutator to revert to the preacquisition mode. The instruction also causes an output resume to be returned to the computer.

The computer next sends a select output instruction (3X02) and another function ready. The function ready clears the bistable control logic that stored the clear decom instruction and enables the decoding of the select output instruction. If the interface is not operating in the Local mode, the select output instruction is stored and an output resume is returned to the computer. The instruction also terminates a NO EXCHANGE indication and lights the LOADING PROGRAM light on the front panel of the unit. It also conditions the control logic for gating a loading pulse to the decommutator's stored program processor (memory) upon the receipt of a 12-bit computer word and an information ready input. Each computer word is accompanied by an information ready input. Each word is converted to the logic levels used by the decommutator by the level converters and is made available to the formatting register of the decom memory, where four computer words are formed into one memory word. The words are entered into the register as a result of the information ready input. The first four computer words specify the program number and the address at which the program loading is to begin. When the memory has loaded a computer word, it supplies a resume loading input to the interface unit. This input causes an output resume to be returned to the computer. rate of word transfer is dependent upon the computer inputs and whether the stored program decommutator is decommutating. The execution of a select output instruction is terminated by the receipt of another instruction.

Essentially, the same sequence takes place in the program check operation (3X50). This operation provides the computer with a means of checking the program stored in the decommutator to determine its accuracy.

If the computer desires to receive status inputs from the decommutator, it sends a select status instruction (3X40) and a function ready input. As a result of the function ready input, any previously stored instruction is cleared and the select status instruction is decoded and stored. This stored instruction gates a 12-bit status word to the computer. When an input request is received, an input ready response is sent to the computer.

The 12-bit status word is formed from the existing conditions in the computer interface unit and from inputs furnished by the decommutator. The status word and its contents are shown in Figure 7-2. If the status indication is satisfactory, the computer can send

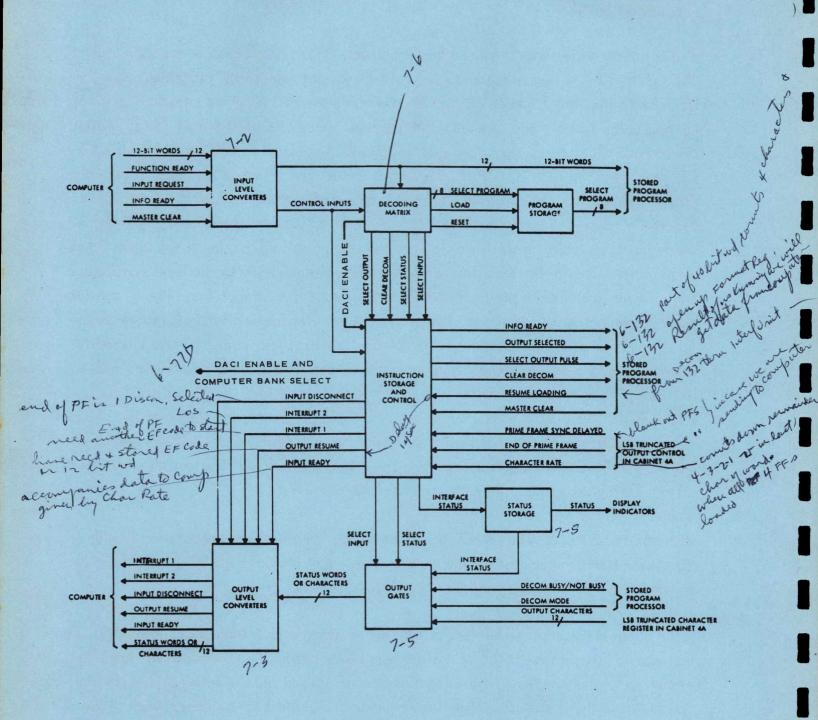


Figure 7-3. Computer Interface Unit Block Diagram

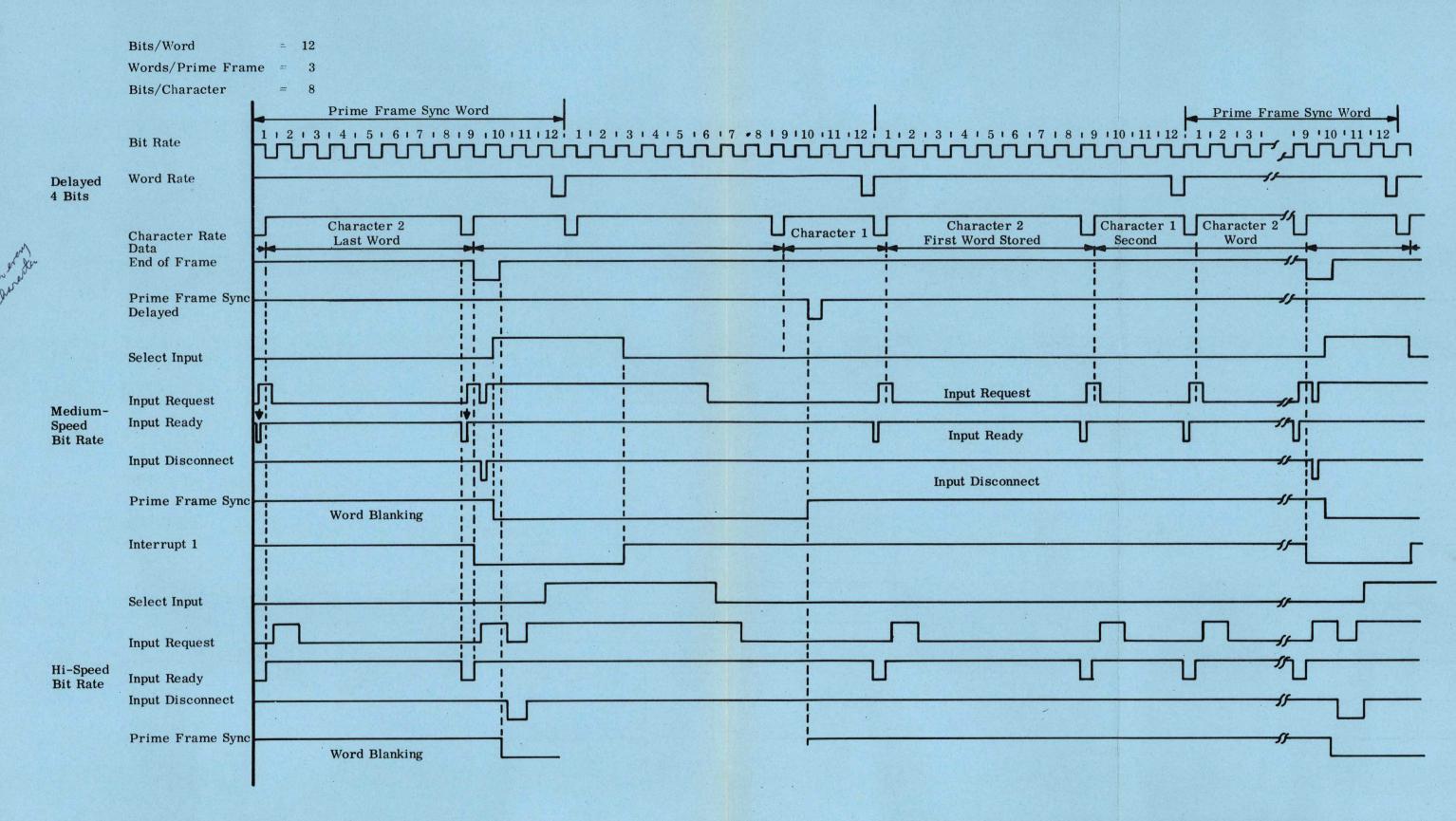


Figure 7-4. Computer Interface Unit Timing Diagram

a select program Y instruction (3X1Y, where Y is octal 0 through 7) code and a function ready. The select program Y instruction is decoded and an output resume is returned to the computer. As a result of the instruction, a program number is stored and is furnished to the decommutator's memory. This output specifies one of eight possible decommutating programs that may be stored in the memory. Next, the computer sends a select input instruction (3X01) and another function ready. This instruction is decoded and stored, and an output resume is returned to the computer. The instruction lights the RECEIVING DATA indicator and terminates any other indications.

The select input instruction results in data transfers from the LSB truncated character register in Cabinet 4A to the computer. The characters are converted to logic levels compatible with the computer by the output level converters. When the computer desires transfer of a group of characters, it sends an input request and the interface unit responds with an input ready. The characters are transferred at the character rate by a character rate input from the LSB truncated character control logic in cabinet 4A. An input request is required for each character. Prime frame sync words are not transferred to the computer. This function is implemented by a blanking pulse that is started by an end-of-prime frame input from the decommutator. It prevents the output gates from gating the prime frame sync word to the computer. The blanking pulse is terminated by a prime frame sync delayed input from the decommutator. If the front panel INPUT DISCONNECT/INTERRUPT 1 switch is in the INTERRUPT 1 position, the computer interface unit sends an interrupt 1 output and allows only one prime frame of data to be transferred to the computer without another instruction input. Similarly, if the INPUT DISCONNECT/INTERRUPT 1 switch is in the INPUT DISCONNECT position, the computer interface unit sends an input disconnect output and allows the transfer of only one prime frame of data until either input request is dropped or the 3 X 01 instruction is reselected.

# 7.5 LOGIC ANALYSIS

#### 7.5.1 GENERAL

Figure 7-1 (in the Logic Diagrams, not this manual), sheets A, B, C, D, E, and F, are the logic diagrams for the interface unit. An explanation of the routing of the signals used in the text and on the logic diagrams is as follows: when a signal enters or leaves the unit, the reference designation of its origin or destination is given. When a signal is applied to another sheet of the logic diagram, the sheet letter designation precedes the destination (example: D9B2, sheet D, module 9B, pin 2). When a signal

is applied to another module on the same sheet, there is no letter designation preceding the destination (example: 7D4, module 7D, pin 4). Further, the logic analysis assumes that the user understands coding of instruction words discussed in paragraph 7.2. Logic levels to and from the computer are assumed to be:

binary one = 0 to -0.5 volts binary zero = 1.95 to 2.36 volts

Internal to the interface unit and the decommutator the logic levels are:

binary one = -5 to -10 volts binary zero = 0 to 0.5 volts

The logic discussion is presented as follows: first, the four unique signals (function ready, input request, information ready and master clear) are discussed in detail. Second, a detailed discussion of the decoding process for one of the 13 computer instruction words is presented. Third, the formation and transfer of the status word is discussed. Finally, a summary of the data transfer, memory loading, and program check functions is presented.

### 7.5.2 FUNCTION READY SIGNAL

The computer sends the function ready signal to the interface unit with every instruction word. One basic purpose of the signal is to clear any previous instruction from the interface unit storage registers before a new instruction is sent. The function ready signal is also used to strobe into the interface unit the decoded instruction sent from the computer.

The function ready signal is applied to the interface unit through computer interface terminator (CIT) module A1D whose function is to convert the logic level from the computer to that used in the decommutator. The signal from A1D10 is a negative level until the interface unit answers with the output resume signal. The negative level is applied to dual-NOR (D-NOR) B1B1 and to counter shift register (CSR) E6B1. The CSR is used in the program check mode which is discussed in paragraph 7.6.3.

The negative function ready signal, when applied to D-NOR B1B1, causes this OR gate to produce a zero-volt output. This positive transition causes DIF B1C to produce a negative pulse the width of which is adjustable by use of an external capacitor. In this case the capacitor is 0.001 microfarad and effectively stretches the negative pulse width to approximately 2.4 microseconds. This negative pulse is applied to the other half of D-NOR B1B4 and is used to inhibit the gate for this time period and prevent the

generation of the store strobe signal. One reason for the time delay at this point is that store strobe is a controlling gating signal, however the incoming instruction word must be decoded before applying the gating pulse (store strobe) to the gates.

The negative output of the DIF is also applied to D-NOR OR gate B3A1 causing this OR gate to produce a positive output that is inverted through the other half of D-NOR B3A. This negative pulse from B3A5 is applied to the reset input of CSR's C1C through C4C and is used to clear the interface unit of any previously selected instructions. The same negative pulse is applied to the set side of CSR D7A to insure that the prime frame sync word is blanked from the data and to CSR E8A to inhibit the program check function.

The negative pulse from the DIF is also applied through inverter B2B to AND gate B3B1. The other input to B3B at pin 2 is a positive level signifying that one of the eight program selection signals has now been decoded. Since both inputs to AND gate B3B are now at a zero volt level, gate B3B10 produces its unloaded negative output that is inverted by OR gate B1A, re-inverted by B3C, and applied to the reset input of CSRs C3E through C10E to clear any program that may have been selected previously.

The purpose of the 2.4-microseconds time delay is: to allow time for any octal coded instruction to be decoded; to clear control CSRs C1C through C4C; to clear program selection CSRs C3E through C10E; and to produce a time interval between selected programs in the decommutator. This interval causes the decommutator to go into the acquisition mode when a new program is selected.

When the 2.4-microseconds pulse from DIF B1C10 returns to a zero level, the interface unit responds with an output resume signal and AND gate B1B is true and produces its negative unloaded output. This negative pulse is inverted at D-NOR B2B. The resulting zero volt pulse is identified as the inverted store strobe pulse and is used as a strobe, or truing, input in various places as described in the following paragraph.

#### 7.5.3 STORE STROBE

The store strobe signal is generated within the interface unit as a result of the function ready signal from the computer after the 2.4-microseconds delay from DIF B1C. This time delay allowed time for various control CSR's to be cleared and for any instruction to be decoded. The store strobe signal performs two important functions: (1) when one of the five instruction codes from the computer is present, the signal is needed to true

the final stage in the decoding process; (2) when one of the eight programs is selected, the signal is needed to true the selection gate.

The inverted store strobe pulse is applied to D-NOR AND gate C9A pin 2 and to D-NOR AND gates C3D through C10D. The output of D-NOR C9A, when trued, will be used to select one of five control instructions; while the output of D-NORs C3D through C10D will be used to select one of eight programs that control instructions. Which program is selected depends upon the selection made by the computer. For purposes of discussion, assume that the first command the computer sends is the status request (3X40). In this case the store strobe pulse that is applied to D-NORs C3D through C10D serves no purpose because a program is not being selected.

The store strobe pulse applied to D-NOR AND gate C9A is ANDed with octaves three and four of the 3X40 code. It should be noted that octave four is a binary three at all times and indicates that the decommutator is the piece of equipment being addressed. Octave four is decoded at AND gate C1A and causes the gate to produce its unloaded negative output. This negative pulse is inverted by D-NOR inverter C1B and applied as a zero volt pulse to D-NOR AND gate C2B, the other input of which is a continuous level indicating that decommutator one and decommutator two are on the line. This function is implemented by D-NOR C2A decoding octave three. If the decom unit switch setting corresponds to the decoded output for either decommutator one or decommutator two, a continuous zero volt level is applied to C2B. Thus, octave four is the controlling input to D-NOR AND gate C2B. AND gate C2B, now having both inputs at zero volts, produces its unloaded negative output; it is inverted by the other half of D-NOR C2B and applied as a zero volt input to D-NOR AND gate C9A pin 1 through buffer amplifier C3B. This is the pulse needed to true gate C9A because the inverted store strobe pulse was already applied as a zero volt input to C9A2. Thus D-NOR AND gates C9A output goes negative, is inverted through the other half of D-NOR C9A, and applied as a zero volt input to D-NOR's C5C and C6C. These two D-NOR's are part of the decoding matrix for the five control signals 3X01, 3X02, 3X20, 3X40, and 3X50. The original assumption was that the 3X40 signal was sent from the computer.

Previously, octave four was used to true D-NOR C9A without the actual decoding process being discussed. The remaining three octaves will be presented in the same manner at this time, with the decoding discussion left until later (paragraph 7.5.7).

Assume that input pins 3 and 4 of D-NOR C6C are at a zero volt level. With the application of the inverted store strobe pulse, the 3X40 side of D-NOR C6C is true, causing

the pin 5 output to go negative. This pulse is applied to the dc set input of CSR C4C. Thus, the status request signal has been decoded and stored within the computer interface unit.

It should now be apparent that the inverted store strobe signal performs the two previously stated functions: (1) When one of the five instruction codes from the computer is present, the signal is needed to true the final stage in the decoding process; (2) When one of the eight programs is selected, the signal is needed to true the selection gates.

The signal has one more function that is discussed in the program check paragraph.

### 7.5.4 INPUT REQUEST SIGNAL

The input request signal is sent by the computer when information is to be sent back to the computer during one of the following three operations:

<u>Operation</u>	Selection Code	<u>Information Sent</u>
Select Input	3X01	Decommutator Data
Status Request	3X40	Decommutator Status
Program Check	3X50	Decommutator Stored Programs

The input request signal is applied to CIT A2D pin 5 where the logic level from the computer is converted to that required by the interface unit and applied to D-NOR inverter D5B pin 4. The zero volt output from D5B is then used with the status request, select input, or program check operation, whichever the computer selects. Assume that the computer sends the status request (3X40) code along with function ready. When the 3X40 instruction has been decoded, CSR C4C is set. This causes a zero volt output from C4C pin 9 that is routed to D-NOR AND gate D5B, where it is ANDed with the inverted input request signal. The resulting negative pulse, status ready, is sent to the computer through CID B7E indicating that the status response word is present. The output of status bit CSR's D7B, D9B, D10B, D7C, D8C, and D9C, along with the remaining status bits from other points, is applied to D-NOR AND gates D2C, D1C, D2D, D3C, D4C, and D3D and then through CID modules B1D through B6D and B1E through B6E.

Secondly, the input request signal is used in conjunction with the select input (3X01) instruction to gate data to the computer. Its function in this respect is discussed in the following paragraphs.

The input request signal, after being inverted by D-NOR inverter D5B, is applied as a zero volt input to D-NOR AND gates D6A, D8B, and D10A. At AND gate D6A it is used with the inverted prime frame sync delayed pulse and the zero volt level, signifying that the select input instruction has been stored to true the gate and cause the prime frame sync word CSR D7A to change states. This indicates that all following words are data words.

The D5B pin 5 zero volt signal at D-NOR AND gate D8B pin 2 is used to gate and terminate the input disconnect signal that is sent at the end of a prime frame of data.

Input disconnect or Interrupt 1, depending on the position of S2, is sent to the computer after a prime frame of data has been sent. The trailing edge of an end-of-prime frame pulse causes a positive-going transition to be sent from D8A10 to D7A3. CSR D7A output pin 9 is then triggered to ground. When both D4B9 and D4B3 are at ground, there is a positive-going transition sent from D10C5 to D7B2 and D7C3. The ungrounded CSR is then triggered. If D9B5 is not grounded, D7B5 is triggered to send a zero-volt signal to D8B1. The zero-volt inverted input request signal at D8B2 will then cause a negative input disconnect signal to be sent from D8B10 to the output driver B9D pin 1. The trailing edge of input request causes a positive-going transition to be sent from D8B10 to D9B2, which triggers CSR D7B-D9B to terminate the input disconnect signal. Both input disconnect and interrupt 1 signals can be terminated by the selection pulse on D7B3. The interrupt 1 signal is not gated by input request.

### 7.5.5 INFORMATION READY SIGNAL

This unique signal, when coincident with the select output (3X02) instruction, allows the computer to load or modify a program in the memory of the decommutator. The information ready signal is applied to CIT module A3D pin 5. The signal is converted to a level that is compatible with the computer interface logic, and, if the information ready signal from A3D10 is not inhibited by the decoded program check, the instruction as described in paragraph 7.6.3 is applied to dual NOR module D2A pin 1 as a negative input. The dual NOR inverts the pulse and applies it as one input to dual NOR D1A pin 3. The pin 4 input to dual NOR D2A (functioning as an AND gate) is the inverted select output signal. This signal must be present at the same time as the information ready signal in order to true dual NOR D1A. The resulting negative output pulse from dual NOR D1A pin 5 is routed through buffer amplifier D2E to the memory in the decommutator. It causes the memory to set up the logic so that a program in memory can be loaded. The select output 0-volt signal is also routed to indicator driver A1C pin 1 to turn on the LOADING PROGRAM indicator. It is, therefore, apparent that the information ready

signal, when coincident with the select output instruction, allows the computer to enter a program into the memory of the decommutator.

### 7.5.6 MASTER CLEAR SIGNAL

This signal from the computer cancels any instruction that the computer interface unit is performing. The computer sends the master clear signal to the computer interface unit, where it is applied to computer interface terminator module A4D pin 5 (figure 7-1 logic diagrams). The input signal is converted to a logic level that is compatible with the interface unit and is applied to dual NOR B3A pin 2. This half of the dual NOR functions as an OR gate. The negative signal saturates the gate and allows the gate to produce a 0-volt output at B3A10. This output is applied to the other half of the dual NOR, where it is inverted and applied to the reset side of the four instruction storages (CSR C1C through C4C) to the set side of CSR D7A (sheet D), and to CSR E8A pin 5. This effectively cancels any instruction that the computer interface unit is executing. The master clear signal is also applied to gate D9A, where it is used to end either the input disconnect or interrupt 1 outputs generated by CSRs D7B, D9B, or D7C.

## 7.5.7 DECODING INSTRUCTION WORD 3X01 (SELECT INPUT)

The following discussion presents a typical example of the decoding process for the 13 different computer instruction words. These words were discussed in paragraph 7.2 and listed in Table 7-2. It should be understood that all 13 instruction words are decoded in the same manner presented. Also, it must be remembered that the instruction words from the computer and the data characters to the computer are always transferred in parrallel.

The select input (3X01) instruction is initiated by the computer whenever the computer requires decommutated data from the decommutator. The signal is typical, requiring that all four octaves be decoded, the instruction stored, and the decommutator and computer interface unit caused to respond.

The code is sent in binary form on 12 lines. These lines are hard-wired to input gates that effectively break the 12 bits into octaves of 3 bits each. Each three-bit octave is then passed through a decoding matrix, where that specific octave is decoded. This results in the matrix producing one discrete output that is ANDed with the outputs from the other three decoding matrices to result in one unique pulse which identifies that particular code.

The 12 bits are applied to computer interface terminators (CIT's) A5C, 5D, 6C, 6D, 7C, 7D, 8C, 8D, 9C, 9D, 10C, and 10D in parallel. These correspond to bits 0 through 11 shown on sheet A of figure 7-1 (logic diagrams). The purpose of the CIT's is to convert the logic level of the cable from the computer to that required by the interface unit and the decommutator. These logic levels are applied through non-inverting buffer amplifiers (BA) B4A, 4B, 5A, 5B, 6A, 6B, 7A, 7B, 8A, 8B, and 9B on sheet B to increase the drive of the signals. From the output of the BA's the bits are applied to the decommutator's memory as well as to the decoding matrices. The reason for all bits being applied to memory is so that a program can be entered or revised whenever the proper gating pulses are present (paragraph 7.6.2). Thus, all bits of every transmission from the computer are applied to the decommutator's memory and depend upon a unique signal from the computer as to whether or not they are gated into memory.

In addition to the bits being applied to memory, they are also applied to the decoding matrix in both their true and complement form.

Octaves three and four are decoded and are ANDed at D-NOR C9A (sheet C) with the store strobe pulse, inverted and applied as one truing input to D-NOR AND gate C5C. Octaves one and two are decoded by their respective matrices to produce negative outputs, which are inverted and applied as truing inputs to pins 1 and 2 of D-NOR AND gate C5C. D-NOR C5C produces its unloaded negative output pulse, which is applied to CSR C1C pin 5. This pulse forces the CSR to be set or to have a negative output at pin C1C10. Both the zero-volt and negative outputs of CSR C1C are used simultaneously to implement the select input instruction within the computer interface unit and the decommutator.

The negative output from C1C10 is applied to D-NOR OR gate D3A, causing the output at D3A pin 10 to go to zero volts. This is applied to D-NOR AND gate D2A pin 4 as a truing input. The pin 3 input to AND gate D2A is the inverted store strobe pulse. The resulting negative output pulse at D2A5 is identified as the output resume signal and is applied to computer interface driver (CID) B7D sheet B. The CID converts the logic level used by the decommutator to that required by the computer. This signal is the indication or reply to the computer that the instruction sent by the computer has been successfully decoded and stored. Note that the output from CSR C1C is in the opposite state, by the action of function ready, until instruction 3X01 is decoded. This is the case with all five of the unique instructions sent by the computer; a reply is not returned by the computer interface unit until the instruction has been decoded and stored.

The purpose of delaying the function ready signal by the action of DIF B1C before generating the store strobe pulse can now be clearly seen; it allows time for the instruction word, in this case 3X01, to be decoded. The delay is also used in the decom as an interval between selected program modes, so that changing a program puts the decom in the acquisition mode when a new program mode is selected by the computer.

Mentioned in the above paragraph was the fact that both the zero volt and negative outputs of CSR C1C (sheet C) are used to implement the select input instruction. The zero volt output at C1C9 is used much more extensively than the negative output and is discussed in the following paragraphs. It should be remembered that the above discussion concerning the negative output at C1C pin 10 and the following discussion concerning the zero volt output at C1C pin 9 occur simultaneously.

The zero volt output from CSR C1C pin 9 is applied through BA C10A to four different places. The first usage of the zero volt output is to AND it with the prime frame lock signal that signifies the decommutator is operating normally and decommutating data. The inverted prime frame lock signal, being a normally zero volt level, is inverted at D-NOR D4A. The negative level from D4A10 is applied as an inhibit level to D-NOR AND gate 1A pin 1 and causes the output at D1A10 to remain at zero volts. The pin 10 output of D-NOR D1A is identified as the interrupt 2 signal and, when negative, indicates to the computer that the decommutator is out of sync, which is the reason for applying the inhibit level to D-NOR D1A pin 1 and insuring that its pin 10 output remains at zero volts. If the decom is not in prime-frame lock during the select input operation, a negative signal from D1A10 is applied to pin 1 of CSR's D8C and D9C and is used to generate status bits 4 (logical 0) and 11 (logical 1) whenever the computer requests the status of the decommutator. In the select input operation the status bits are not used.

The next place to which the zero-volt output of BA C10A pin 10 is applied is to the dc set input of CSR D3B pin 3. This zero-volt signal allows D3B5 to be triggered to zero volts. When the select input instruction is not present, D3B3, and thus D3B5, are held at a negative level.

The function of bringing pin 1 of CSR D3B to a ground level is through the action of D-NOR 4B. This D-NOR is a rather unique gate in that pin 9 serves a double purpose. Whenever a negative input is applied at D4B pin 9, it inhibits the AND gate side and inverts the pulse through the other half of the gate. The input to pin 9 of D-NOR D4B is from CSR D7A pin 9. This CSR is used to blank the prime frame sync word from the

data so that it is not interpreted as data. The purpose is to keep D-NOR D10A from being true and sending the data input ready pulse to the computer until after the prime frame sync word has passed. The data (input) ready signal from D10A pins 5 and 10 is applied to C1D module B7E pin 1, to generate the input ready signal in response to the input request signal from the computer. With D3B1 at ground, the leading edge of character rate is D4A1, causing a positive-going transition at D3B2, which triggers this CSR to send a zero-volt output from D3B5 to D10A2. The trailing edge of input request causes a positive-going transition to be sent from D6B10 to D2B2, which triggers the D2B-D3B CSR to send a negative voltage from D3B5 to D10A2. At normal bit rates, this signal at D10A2 will go negative prior to the trailing edge of the inverted character rate pulse at D10A4. At high bit rates, the half-bit-wide character rate pulse can end before the end of input request. Thus, input ready begins with the leading edge of character rate, and ends with the trailing edge of character rate, or input request, whichever comes first.

After the prime frame sync word has passed, pin 9 of CSR D7A is a negative level. This level is inverted through D-NOR D4B and applied to pin 1 of CSR D3B. With pin 1 now at ground the next trigger pulse applied to pin 2 can be recognized.

The third place to which the select input level from BA C10A is applied is to D-NOR D5A pin 4. When this D-NOR is true, its negative output is inverted by D-NOR D6C and applied as a truing input to all data output D-NOR's. However, D-NOR 5A is not true until after the prime frame sync word has passed and CSR 7A is reset.

The last function of the select input is to force CSR 7A to change states and thereby allow data characters to be gated out. With the coincidence of inverted select input, input request, signal, and prime frame sync delayed pulse that occurs at the end of every prime frame sync word, D-NOR AND gate D6A pin 5 becomes a negative output which resets CSR 7A through pin 1. The zero volt output at D7A pin 10 is applied to D-NOR AND gate 5A pin 3 to true the gate and therefore gate out the data bits. The negative output at D7A pin 9 is inverted through D-NOR D4B to permit triggering CSR D2B-D3B. The zero volt output at D3B pin 5 is the level needed to true D-NOR D10A and cause it to send the data input ready signal to the computer, indicating that a data character is ready for transmission to the computer.

## 7.6 STATUS RESPONSE WORD

#### 7.6.1 GENERAL

The status response word is sent to the computer when the computer sends the status request instruction word (3X40, Table 7-2). The word is formed within the decommutation and the computer interface unit and tells the status of the decommutator at the time of receipt of the input request signal. The status response word format is shown in Figure 7-2.

The status request instruction is decoded and results in a negative output pulse from D-NOR AND gate C6C pin 5. This pulse resets instruction CSR C4C, causing the output at C4C pin 10 to be a negative level. This level is ORd through D-NOR D3A (sheet D) and then ANDed at D-NOR D2A with the store strobe signal generated as a result of the function ready signal from the computer to produce the output resume signal to the computer. This negative signal effectively tells the computer that its previously sent instruction has been received and successfully decoded. The negative level from the CSR C4C pin 10 is also applied to indicator driver A3C pin 4 to turn off the NO EXCHANGE indicator and through OR gate A6B to turn on the RECEIVING DATA indicator.

The zero-volt level from pin 9 of CSR C4C is used as a truing signal to gate out the status bits. Its first use is at D-NOR AND gate D5B pin 1 in conjunction with the inverted input request signal at D5B2. This produces the status (input) ready signal, which is sent to the computer and signifies that the status response word is being transmitted to the computer.

The second point to which the zero volt level from pin 9 of CSR C4C is applied is through D-NOR inverter D5A to D-NOR inverter 5C pin 9. The negative level at pin 9 of D-NOR D5C inhibits the gate and forces both outputs to be a zero-volt level. This zero-volt level is used as the true level gating input to the status bits output D-NOR AND gates D2C, 1C, 2D, 3C, 4C, and 3D. The other input to these gates is the inverted status bits themselves. Thus the status request signal itself is not used to generate the status bits, but only as a reply to the computer that the signal was received and successfully decoded and as a gating pulse allowing the status bits to be transmitted to the computer.

## 7.6.2 DATA TRANSFER

Data is transferred to the computer from the LSB truncated character register in cabinet 4A. The characters can be from 4 to 12 bits long and are applied to D-NOR

modules A8B through A10B and A8E through A10E in parallel. These D-NORs function as inverters and supply the complement of each character bit input to D-NORs D4D through D9D.

The clear selection pulse generated by function ready input causes CSR D7A to be set, and the negative output at D7A pin 10 prevents the transfer of characters until the prime frame sync word has passed. When the computer receives the output resume signal from the computer interface unit, it sends the input request signal (paragraph 7.5.4). This signal and the select input instruction are the two needed to gate the data bits to the computer.

The coincidence of the inverted input request signal, select input instruction, and the inverted prime frame sync delayed pulse, which occurs at the end of every prime frame sync word, at D-NOR AND gate D6A causes a negative output at D6A5 pulse that is applied to CSR D7A pin 1, causing the CSR to change states. The zero output from CSR D7A pin 10 is now ANDed with the inverted select input instruction at D-NOR D5A, causing the AND gate to produce its unloaded negative output at pin 5. This negative level is applied to pin 9 of D-NOR D6C and forces both D6C5 and D6C10 to be a zero-volt level. This level is used as the true level gating input to the data bits output D-NOR AND, gates D4D through D9D. The actual data bits are the other input to each of these AND gates and are applied from the LSB truncating register in the decommutator.

When the computer receives one character of data it sends the input request signal again, requesting another data character. A character rate pulse marks the end of every data character. Between the action of the input request signal and this character rate pulse, CSR D2B - D3B is caused to change states with every data character sent. The corresponding CSR output at pin 5 of D3B, when applied to D-NOR D10A, causes the D-NOR to produce the negative data (input) ready signal to mark the end of every data character transmitted, which, in turn, notifies the computer to drop the input request signal. Note that the truing input at D6C pin 9 of the data output D-NORs is a constant zero volt or truing level during the complete prime frame of data.

#### 7.6.3 MEMORY LOADING

To load the decommutator memory, the computer sends a function ready signal and a select output (3X02) instruction. The computer interface unit decodes the select output instruction and applies a zero-volt input to D-NOR AND gate D1A as well as responding with the output resume signal to the computer. The computer responds with

a 12-bit data word and an information ready signal (paragraph 7.5.5) that is applied to CIT A3D pin 5 where the logic level used by the computer is converted to the level used by the computer interface unit, inverted by D-NOR inverter D2A, and ANDed with the decoded select output instruction at D-NOR AND gate D1A. The resulting negative output is sent to the memory-gating circuitry of the decommutator and sets it up to accept a computer input. When the data has been stored, the decom sends a resume loading pulse to A7B pin 1. The computer interface unit then responds with the output resume signal that causes the computer to drop the information ready signal and place the next word to be loaded into memory on the 12 data lines. This word is applied to CIT modules A5C through A10C and A5D through A10D. The CIT modules convert the input logic levels to those used by the computer interface unit and apply the bits to buffer amplifiers B4A through 9A and B4B through B9B. The outputs of the buffer amplifiers are applied directly to the memory formatting register. The bits are loaded into the register by the information ready output of the computer interface unit.

The memory formatting register is a 40-bit register and does not dump its contents into memory until all 40 stages are loaded. The maximum word length of the computer is 12 bits; therefore, the computer must send four words with eight bits of the last computer word zeros to fill the memory formatting register. The first response of the output resume signal is generated within the computer interface unit and causes the computer to send the first 12-bit word. After this word is in the memory formatting register, the computer sends the information ready signal again. The memory unit now responds with the output resume signal (3A17B1), causing the computer to send the second 12-bit word.

The above process continues until the memory formatting register is loaded. If the decommutator is busy, the formatted word cannot be dumped immediately; this means that memory does not send the output resume signal upon receipt of the last 12-bit word. This effectively tells the computer not to send another word to be loaded into memory until it receives the output resume signal again.

#### 7.6.4 PROGRAM CHECK

The program check function provides a means for the computer to check or review the program stored in the decommutator. The program is read out, upon command, one 40-bit word at a time. Because there are only 12 data lines between the interface unit and the computer, each memory word must be broken into 12-bit characters.

The octal equivalent code for the program check command is 3X50. The 3X portion of the command is decoded by AND gate C1A, just as in all the other codes. The 50 portion is picked off the lines going to the decoding matrix on sheet C and applied to AND gate E6A and D-NOR E7A. Only the binary configuration of the bits in octave two is applied to AND gate E6A. The decoded zero from octave one is applied to E7A pin 9.

When the command is present and has been decoded, the output of AND gate E6A goes negative, is inverted by D-NOR E7A, and is ANDed with octave one and the fact that the system is in local/remote, thereby allowing computer control. These three conditions allow the other half of D-NOR E7A to produce, at pin 5, its unloaded negative output that is identified as the program check pulse. The positive going transition from D-NOR inverter E1D pin 10 causes DIF E2D to produce a negative pulse. The DIF has an external capacitor whose function is to make the negative pulse longer. The value of the external capacitor determines the length of the pulse, and, in this case, makes the pulse approximately 2 microseconds long.

The actual program check routine starts when the function ready signal is sent from the computer as shown in the timing diagram in Figure 7-5. As in all transmissions between the computer and computer interface unit, function ready is the first command from the computer. This level resets a two-stage counter that is used to count the number of characters per memory word. Since there is a maximum of four characters per memory word it is necessary that the counter count only from zero to three.

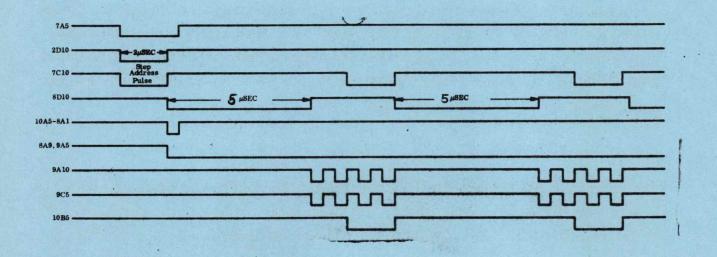


Figure 7-5. Program Check Function Timing Diagram

The zero-volt output at pin 10 of CSR E6B is the trigger to the next stage of the counter as well as being applied to D-NOR AND gates E8B and E9B. The output of CSR E6B, even though it is a positive transition, cannot trigger CSR E7B because it is being held in the reset state by the negative function ready signal at E7B1. With both stages of the counter in the reset state, pins 1 and 2 of D-NOR AND gate E8B are true, causing a negative output at pin 10. This pulse is inverted through D-NOR E9C and applied as a truing input to D-NOR AND gates F4D and F4E to gate out memory word one. D-NOR AND gates E8B and E9B are the decoding matrix for the two-stage counter. The outputs of these D-NOR AND gates are inverted by E9C, E10C, E6D, and E7D to become the truing inputs to the memory output gating circuitry on sheet F for characters one through four.

The computer starts every new transmission with the clear selection instruction, which is used to clear instructions CSR's C1C, C2C, C3C, and C4C and to set CSR E8A. Setting CSR E8A inhibits D-NOR AND gate E9A, which is the trigger input to the counter. Therefore, when the AND gate is inhibited, the counter cannot count. The only way to get the counter to count and, thus, to gate out data through gating inverters E9C, 10C, 6D, and 7D is to reset CSR E8A. The following discussion tells how this is accomplished.

The decoded 3X50 instruction causes a negative pulse to be applied to D-NOR inverter E1D. The pulse is inverted and applied to DIF E2D pin 4 as well as to D-NOR AND gate 10A pin 4. The positive going input at the DIF causes a negative output of approximately 2 microseconds. This negative pulse is applied to D-NOR OR gate E1D pin 3. The OR gate output goes to a zero-volt level and is applied to D-NOR inverter E6C pin 9. The D-NOR produces a negative pulse from each output; one is applied through BA E7C to the auxiliary counter in memory as a step pulse, causing memory to step to the next address while the other is applied to DIF E8D pin 4. However, the DIF does not respond because a positive transition is required.

When the output of DIF E2D returns to a zero-volt level, D-NOR OR gate E1D produces a negative output level. This causes D-NOR inverters E6C to go to ground. This positive transition causes DIF E8D to produce its negative output, which is a pulse approximately 5 microseconds long. The pulse is used to inhibit D-NOR AND gate E9A at pin 2, even though pin 9 is still at a negative level, and is routed to D-NOR inverter E10B pin 1. The inverted DIF output is ANDed at D-NOR E10A, causing it to produce at pin 5 its unloaded negative output. This pulse resets CSR E8A, causing the output at

E8A pin 10 to go to ground. When the 5 microseconds pulse from DIF E8D pin 10 returns to ground, gate E9A pins 2 and 9 are also grounded. Input request can then be sent to counter E6B-E7B, and also is sent back to the computer as input ready through D-NORs E10A, E9C, and CID B7E. When the computer drops input request, the input ready signal is terminated, and the positive transition at E6B pin 3 triggers the counter to the next binary state.

The negative output at pin 9 of CSR E8A is applied through power inverter 2E to turn on the LOADING PROGRAM indicator light. Note that this pulse has a sneak path to CSR C2C and forces the CSR to be reset by applying this zero-volt pulse to pin 9 which is the collector reset method of resetting a CSR stage. This appears to the interface unit as though a select output command has been received from the computer. To keep the CSR from having any effect, the negative level from pin 9 of CSR E8A, in addition to being applied to the LOADING PROGRAM indicator, is routed through inverter E1E to produce a zero-volt pulse that is applied to CIT A3D. This insures that the output of this CIT is a zero-volt level. This is applied through inverter D2A to inhibit D-NOR AND gate D1A at pin 3. Thus, even though CSR C2C is reset, its output is inhibited at D-NOR AND gate D1A.

Figures 7-6 and 7-7 outline memory loading from the computer and data transfer to the computer respectively.

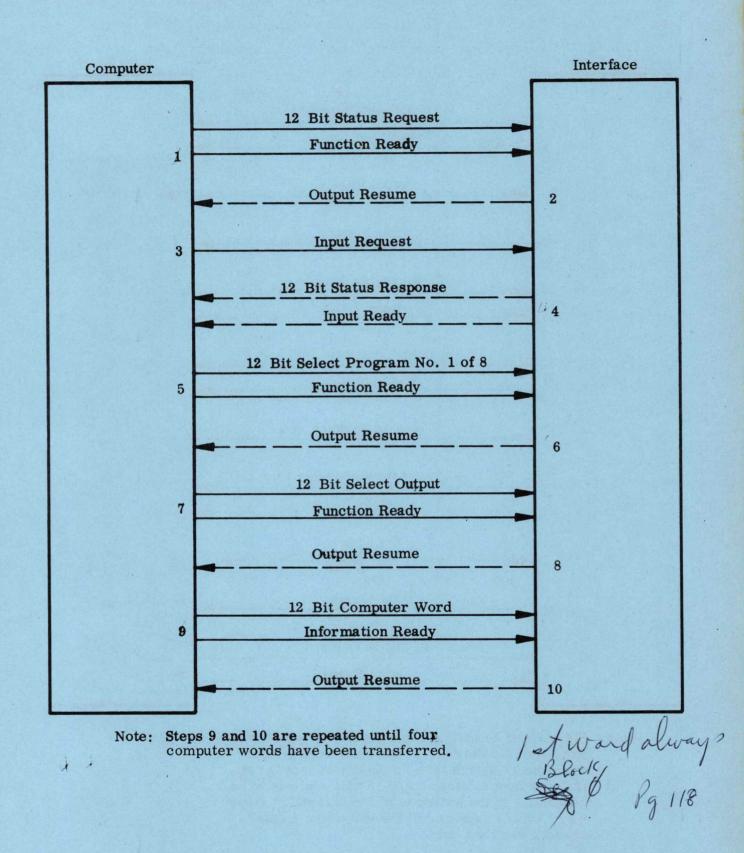
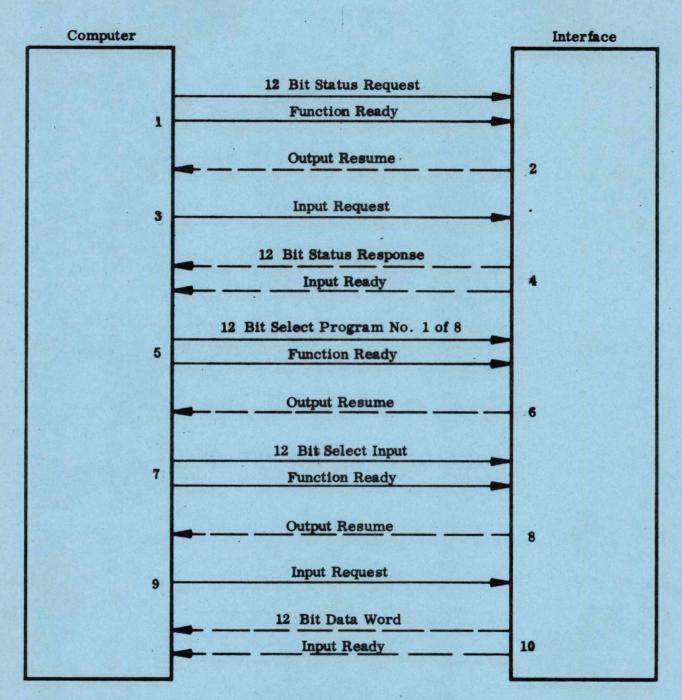


Figure 7-6. Sequential Loading of Decommutator Memory from Computer FOR TRAINING PURPOSES ONLY



Note: Steps 9 and 10 will be repeated until a total frame has been transferred. If the "Interrupt 1/input disconnect" switch is in "input disconnect" at the end of a frame, steps 9 and 10 will continue to be repeated. If the switch is in "interrupt11," steps 9 and 10 will repeat until the end of the frame is reached and then stop.

Figure 7-7. Sequential Transfer of Data Words to Computer

#### 7.6.5 DIRECT ACCESS COMPUTER INTERFACE INSTRUCTION

The DACI incorporates four basic instructions. Three of the 3 X 6 X type for enable and computer memory bank selection and one for clearing the 3 X 6 X selection.

The code of 3 X 6 when received is decoded by modules 3A1G 1E, and 2E and the result ANDed with the store strobe to set CSR 9D (Figure 7-1 of the logic prints). This enables Route Data To Computer and remains set during a total program. Modules 8E and 7E decode the least significant octave to define the bank selection and sets the appropriate CSR. 7D selects banks 4, 8D selects bank 2, and 6D selects bank 6.

When the 3 X 6 X instruction is decoded the DACI places a -10 volts on pin 9 of 3A1G10E. This disables an input request and a select input so that no communication can be made for data transfer via the computer I/O when the DACI is enabled.

The 3 X 70 (DACI clear) is decoded by modules 3E and 4E of 3A1G and ORed with decom clear and manual master clear in module 5E. The 3 X 70 clears only modules 6D, 7D, 8D, and 9D.

#### **SECTION 8**

#### PCM SIGNAL SIMULATOR

## 8.1 PCM SIGNAL SIMULATOR CONTROLS AND INDICATORS

The control and indicators for PCM signal simulator 1A6 are located on the front panel, Figure 8-1, and the rear panel shown in Figure 8-2. A listing of the controls and indicators and their function is presented in Table 8-1. The associated logic prints consist of Pages 6-241 through 6-250.

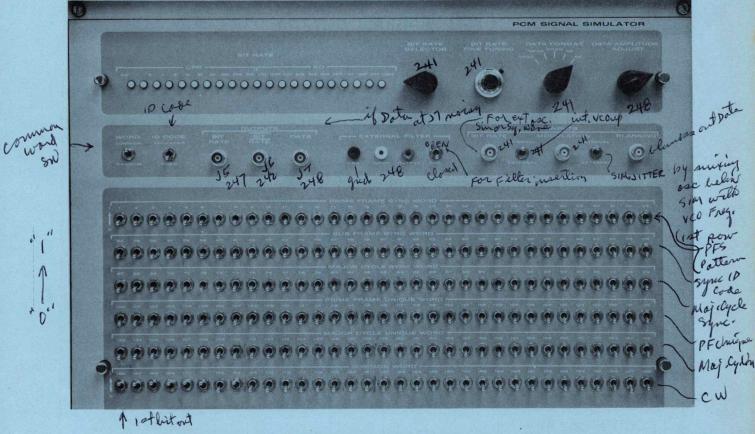


Figure 8-1. PCM Signal Simulator 1A6 Front Panel



Table 8-1
PCM Signal Simulator Controls and Indicators

Control/Indicator	Function
BIT RATE Indicators	Visual indication of selected bit rate. Indicators display from 0.5 cps to 1 mc.
BIT RATE SELECTOR Switch	21-position selector switch for selection of desired bit rate.
BIT RATE FINE TUNING Control	Provides fine adjustment of selected bit rate.
DATA FORMAT Selector Switch	Five-position selector switch for selecting NRZC, NRZS, NRZM, RZ, and SP format of data output.
DATA AMPLITUDE ADJUST Control	Variable control for adjustment of output level.
PRIME FRAME SYNC WORD Switch Bank	Bank of 33 switches for controlling binary pattern of this word. Up position inserts a binary 1; down position inserts a binary 0.
SUB-FRAME SYNC WORD Switch Bank	Same as above.
MAJOR CYCLE SYNC WORD Switch Bank	Same as above.
PRIME FRAME UNIQUE WORD Switch Bank	Same as above.
MAJOR CYCLE UNIQUE WORD Switch Bank	Same as above.
COMMON WORD Switch Bank	Same as above.
WORD Toggle Switch	
COMMON Position	Allows the output data to be controlled by the common word switch bank on front panel.
RANDOM Position	Removes control of data from common word switch bank and inserts a random distribution of ones and zeros in the output data.

Table 8-1
PCM Signal Simulator Controls and Indicators (Cont.)

Control/Indicator	Function		
ID CODE Toggle Switch			
ADVANCED Position	Allows the subframe ID code word to advance in count by one binary number every prime frame.		
FIXED Position	Provides a fixed subframe sync pattern.		
BIT RATE Output Jack	Output jack for bit rate.		
BIT RATE Output Jack	Output jack for bit rate not.		
DATA Output Jack	Output jack for data.		
EXTERNAL FILTER			
GRD (Ground) Jack	Input jack for ground lead of external filter.		
INPUT Jack	Input jack for input lead of external filter.		
OUTPUT Jack	Input jack for output lead of external filter.		
IN/OUT Toggle Switch			
IN Position	Allows insertion of external filter between output amplifier and output data jack.		
OUT Position	External filter jacks bypass.		
BIT RATE Input Jack	Provision for inserting bit rate from some external source.		
INTERNAL/EXTERNAL Toggle Switch			
INTERNAL Position	Allows internal VCO to generate bit rate.		
EXTERNAL Position	Select bit rate from external source.		
MODULATION Input	Provisions for inserting modulation of the bit rate frequency from some external source.		

Table 8-1
PCM Signal Simulator Controls and Indicators (Cont.)

Control/Indicator	Function
INTERNAL/EXTERNAL Toggle Switch	
INTERNAL Position	Allows internal audio oscillator to modulate bit rate.
EXTERNAL Position	Allows bit rate to be modulated from some external source.
BLANKING Input Jack	Input for Blanking output data with external source.
BITS PER PRIME FR SYNC WORD Switches	Sets the number of bits in the prime frame sync word.
BIT PER WORD Switches	Sets the number of bits per word.
WORDS PER PRIME FRAME	Sets the number of words in a prime frame.
PRIME FRAMES PER MAJ CY	Sets the number of prime frames for a major cycle.
PRM FR UNIQUE WORD CHAN LOC	Sets the channel position of the prime frame unique word or sync word.
SUBFRAME SYNC WORD CHAN LOC	Sets the channel position of the sub- frame sync or ID word.
SUBFRAME SYNC WORD FR LOC	Sets the location within the prime frame of the subframe sync word.
MAJ CY UNIQUE WORD CHAN LOC	Sets the channel position of the major cycle unique word.
MAJ CY UNIQUE WORD FR LOC	Sets the position of the major cycle unique word in relation to the number of prime frames.
DATA/DATA Toggle Switch	Allows data or inverted data to be gated out.

## 8.2 PCM SIGNAL SIMULATOR

#### 8.2.1 GENERAL

The PCM signal simulator provides a means of simulating the five standard PCM data inputs in a frequency range from 0.5 cps to 1 megacycle. It can be used to exercise the system for operation and troubleshooting checks.

A simplified block diagram of the PCM signal simulator is shown in Figure 8-3. An internal voltage controlled oscillator (VCO) provides bit rate for the PCM signal simulator. Jitter voltage may be applied to the VCO from either an audio oscillator, contained in the same equipment rack, or from some external modulation source. The VCO is applied to a 21-stage bit rate select counter. Selection of the bit rate is accomplished through a selector switch on the front panel, which is used to select one of the 21 stages. The bit rate selected is visually displayed on the front panel by the BIT RATE indicators. The format of the readout desired is selected by use of the FORMAT SELECT switch. NRZC, NRZM, or NRZS bit rate is routed directly through the switch, while RZ or SP bit rate is routed through an additional counter stage to the switch. From the wiper of the FORMAT SELECT switch, bit rate is passed through the BIT RATE selector switch (assuming it is in the INTERNAL position) and into a two-stage inverter, where the pulses are shaped as required. The EXTERNAL position of the switch allows an external signal generator or similar equipment to be applied, thus bypassing the previous circuitry. The shaper would then be used to shape a sine wave into a square wave. BIT RATE is applied to two AND gates and, depending upon the state of the controlling counter stage, the bits per prime frame sync word counter or the bits per word counter start accepting the signal.

As the initial signal, bit rate came out of the first logic level. The shaper, in addition to being applied to the two counter AND gates, was also sent through two inverters, the output of one being designated bit rate (BR) and the other bit rate not (BR). The BR signal is applied to the parallel-to-serial output register and is used to clock out the information in serial form when it enters the register.

The bits per prime frame sync word counter, bits per word counter, words per prime frame counter, prime frames per major cycle counter, and the relative location within the prime frame of the subframe sync word, major cycle unique word, and sync word, and prime frame unique word are controlled by switches on the rear panel. When the number of bits corresponding to the switch settings have entered the bits-per-prime

frame sync word counter, a reset pulse is sent to the controlling counter stage, causing it to clear. The reset pulse, in addition to allowing the bits-per-word counter AND gate to be trued, also resets the bits-per-prime-frame sync counter and is ORd with the output of the bits per word counter. The output of the OR gate is the word rate signal; it is applied to the words-per-prime-frame counter. This counter determines the words per prime frame. The word rate signal is also applied to a six-input inhibit gate after being delayed one-half bit time where, if not inhibited, the output senses the position of the switches associated with it. Each switch has an OR gate associated with it; a switch in the UP position causes a binary one to be generated by the OR gate and a switch in the DOWN position causes a binary zero to be generated. This particular signal is re-identified as data and is shifted into the parallel-to-serial output register in parallel. All other signals are designated control signals.

When the words-per-prime-frame counter reaches its preselected count, a reset pulse (designated frame rate) is generated. The frame rate signal resets the words-per-prime-frame counter, sets the counter stage controlling the bits-per-prime-frame sync counter and the bits-per-word counter, and the counter stage associated with the prime-frames-per-major-cycle counter. The output of this counter stage identifies the major cycle sync word. When the prime-frames-per-major-cycle counter reaches its preselected count, a reset pulse is generated, resetting the counter and its associated counter stage. The major cycle unique word, subframe sync word, and prime frame unique word are preselected by switches on the rear panel also. These switches use the prime frames per major cycle counter to establish their count and identify the words in their correct position within the major cycle and prime frame.

Provision is also made for three different subframe code formats: General, Apollo, and Gemini. The code formats are generated in bit positions three through 12 of the subframe sync word. The code may be either an advancing or a fixed code.

Any of the information pulses coming through is applied to diode logic that senses the position of the switches associated with it and generates the binary one or zero pattern required by the switch positions. Each control word enable signal is also applied to an inhibit gate. This functions to blank out the common word (data) when any control word is present. The two types of words are shifted into the parallel-to-serial output register in parallel, clocked out by the bit rate signal in serial fashion, and applied to the common-random word logic.

The logic is controlled by the position of the COMMON/RANDOM WORD switch, located on the front panel. If the switch is in the COMMON position, the output of the parallel-to-serial register bypasses all the logic and is applied directly to the output shift register 99A. The BR signal clocks the information through the shift register to the format converter. The position of the FORMAT SELECT switch determines the format (NRZC, NRZM, NRZS, RZ, or SP) of the output. From the wiper arm of the switch the signal is ANDed with a blanking signal to blank some of the signal if desired. The output of the AND gate passes through a noise generator, where a selectable signal-to-noise ratio is established, through an adjustable potentiometer, and applied to an amplifier. The output of the amplifier may be filtered externally if desired and then routed to the output jacks.

If the COMMON/RANDOM switch is in the RANDOM position, the information is gated through if any of the following signals are being applied as inputs to the controlling OR gate:

- Prime Frame Sync Word Enable
- Major Cycle Sync Word Enable
- Major Cycle Unique Word Enable
- Subframe Sync Word Enable
- Prime Frame Unique Word Enable

If any of these signals are present, the information is gated through the AND gate, the following OR gate, and then applied to the previously mentioned output circuitry. If any of these signals are not present, the output of the noise generator drives an AND gate and succeeding OR gate, producing a random distribution of ones and zeros at the output. This information in turn is shifted into a final shift register stage where it is processed as random data.

#### 8.2.2 FREQUENCY SELECTION

Figure 6-54 sheets 1 through 10 are the logic diagrams for the PCM signal simulator. The basic frequency of the PCM signal simulator is supplied by a voltage controlled oscillator (sheet 1). The VCO output is a basic frequency of 2 to 4 megacycles. The output is applied to a 21-stage binary counter. Each stage of the counter divides the frequency by two, which provides frequencies ranging from 2 cps to 1 mc in the NRZM, NRZC, and NRZS code formats. An additional counter stage is used for the RZ and SP types of codes; therefore, frequencies ranging from 0.5 cps to 500 kc are available for these code formats. The format is selectable through S2B and S2C. The reason

for the additional counter stage is to make the simulator compatible with the group synchronizer. Fine tuning of the VCO is provided through a helipot.

An audio oscillator is located immediately below the simulator within the equipment rack. When S7 is placed in the internal position, the output of the audio oscillator is applied as jitter voltage to the VCO. This is used to simulate a poor PCM signal. The audio oscillator is variable in frequency from 1 cps to 100 kc.

Each position of S1A corresponds to a different stage of the 21-stage counter. This allows selection of the desired frequency. The second deck of S1 is used to light the appropriate indicator on the front panel for the NRZS, NRZC, and NRZM code formats, while S1C is used to light the appropriate indicator for the RZ and SP formats. The frequency selected is designated bit rate (BR). The BR signal may be generated internally or applied to the simulator from some external source. Switch 6 must be placed in the position desired.

# 8.2.3 BITS-PER-PRIME-FRAME SYNC WORD AND PER-COMMON-WORD COUNTERS

Assume that the bits-per-prime-frame sync word counter is activated first. The set output of the controlling counter stage is applied to the prime-frames-per-major-cycle counter to start counting the number of prime frames and to an output OR gate used to inhibit the common-random word logic.

When the number of bits corresponding to the switch settings have entered the bits-per-prime-frame sync word counter, a reset pulse is sent to the controlling counter-stage, causing it to reset. The zero output from the set side then allows the bits-per-word counter to start counting. The reset output is used to inhibit the prime frames per major cycle one-shot multivibrator and the prime frame sync word front panel switches. The reset pulse is also ORd with the output of the bits-per-word counter to form the word rate (WR) pulse. This pulse is applied as the trigger input to the words-per-prime-frame counter. In addition, the reset pulse is used to reset the bits-per-prime-frame sync word counter.

These two counters are down counters, meaning that the desired number is manually set in with switches and the counter is allowed to count down to zero from the switch settings.

The selected BR frequency is applied through two power-inverter stages to AND gates 34D (sheet 2, figure 6-54) and, after two additional power inverter stages, to AND gates 34A and 34B. The other input to AND gate 34A and 34D is from counter stage 64A. Depending upon the stage of the counter stage, one or the other of the two AND gates is true and the counter controlled by that AND gate starts to count. Each counter is a six-stage counter and must be preset, by switches, to the desired number of bits to be in the prime frame sync word and the number of bits per common or data word, respectively. Assume that counter stage 64A is in the set condition, meaning that the zero output is at 0 volt. This output is applied as the second input to AND gate 34A. When both inputs are at 0 volt, the gate is cut off and the normal unloaded output of -10 volts is applied as a trigger input to the first of the six-stage bits-per-prime-frame sync word counter. The trigger pulse applied at BR causes the counter to count from its initial turn-on state toward zero.

#### NOTE

All counter stages trigger on the leading edge of negative going pulses.

As long as any -10-volt signal is applied to AND gates 42A and 43A, the gates produce their saturated output of 0 volt. This is applied as an input to AND gate 34C. The other input to this AND gate is from AND gate 34B, whose output is 0 volt immediately after turn-on. These two gates form a single-shot multivibrator. The two 0-volt inputs cause AND gate 34C to produce its normal unloaded output of -10 volts. This output is applied as the second input to AND gate 34B. The -10-volt input holds the output of AND gate 34B at 0 volt. The output of AND gate 34C is also applied to an emitter follower and power inverter and then to the switches for each counter stage. As long as the inverted -10-volt signal is applied, the counter stages count with each trigger pulse.

When the count of all zeros is reached, summing AND gates 42A and 43A are trued. This causes them to produce their normal unloaded output of -10 volts. This output, when applied to AND gate 34C, saturates the gate, causing it to produce a 0-volt output. This output is applied through the emitter follower and power inverter stages, where it is inverted to a -10-volt level that forces the switch selected number into the counters. The 0-volt output is also applied to AND gate 34B. When the next 0-volt level from BR is applied, it causes the gate to produce its normal unloaded output of -10 volts. This output is crossed back as an input to AND gate 34C as well as being

one input to OR gate 34H. The output pulse from OR gate 34H is routed through a power-inverter stage and identified as word rate (WR). This signal is generated whenever either of the two counters count down to zero. The pulse identifies the number of bits in the word. The output of the OR gate is also routed through a counter stage. The set output of this stage is applied to emitter follower 35G. This output is identified as word rate delayed (WRD). The last half bit-time of the BR pulse saturates AND gate 34B and causes it to produce its normal output of 0 volt. With the number being forced into the counter stages, AND gates 42A and 43A are saturated and produce their normal output of 0 volt. These two 0-volt levels cause AND gate 34C to produce its unloaded output of -10 volts, which is applied to AND gate 34B and holds its output to 0 volt. Hence, the reset pulse is present one-half bit time. The counter now counts toward zero from whatever number set into it. When it reaches zero, the same action described above takes place. When counter stage 64A is reset, AND gate 34D is trued and the bits-per-word counter starts counting. This counter functions in exactly the same manner as the bits-per-prime-frame sync word counter.

#### 8.2.4 WORDS-PER-PRIME-FRAME COUNTER

As discussed in the previous paragraph, the WR pulse is generated at the end of every word. These pulses are used as the trigger input to the words per prime frame counter (sheet 3, Figure 6-54). This counter is an up counter and is also controlled by setting switches on the rear switch panel. It is a nine-stage binary counter, thus capable of counting to a maximum of 512 words per prime frame. The counter has four sets of switches associated with it; one set, the words-per-prime-frame switches, controls the count of the counter; the remaining three sets, the major cycle unique word channel location, subframe sync word channel location, and prime frame unique word channel location switches, detect their respective counts as a result of the counter counting.

Assume that it is desired to have five words per prime frame. Figure 8-4 is the timing diagram for this count. Because the switches (sheet 3, Figure 6-54) are connected directly to the output of each counter stage, the complement of the desired number is recognized. When all inputs to summing AND gate 75D are zero, the gate produces its normal unloaded pulse of -10 volts, which is applied as an input to AND gate 75B. The output of this gate is RC coupled in parallel with a constant -10-volt signal. The -10-volt signal is the input to AND gate 75E and holds the gate in a saturated condition that insures an output of 0 volt. This output is doubled back as the other input to AND gate 75B. The two AND gates, 75B and 75E, function as a single-shot multivibrator.

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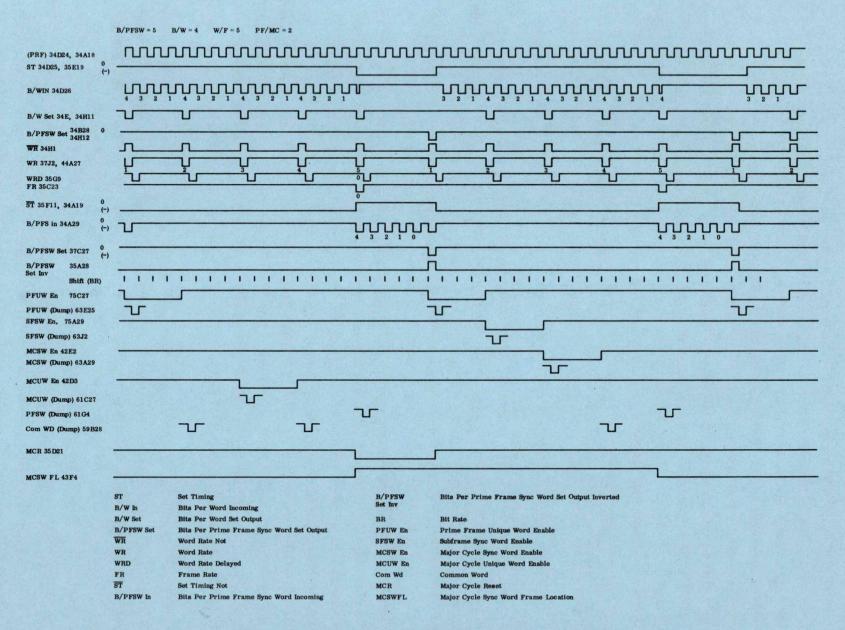


Figure 8-4. PCM Signal Simulator Timing Diagram

The -10-volt input from 75D saturates AND gate 75B, which causes its output to go to 0 volt. This allows the capacitor to discharge and then to charge in the opposite direction from the applied -10 volts. During the time it takes the capacitor to charge in the opposite direction, AND gate 75E has 0 volt as an input; thus, it produces its normal unloaded output of -10 volts. The width of this pulse is determined by the RC time constant. The -10-volt pulse from 75E is applied to AND gate 75B and through an emitter follower stage. The pulse is designated frame rate (FR) and is used to reset the counter to zero and to set counter stages 64A (sheet 2) and 64B (sheet 4).

#### 8.2.5 PRIME-FRAMES-PER-MAJOR-CYCLE COUNTER

The set output of CSR 64B identifies the start of a major frame of data; its output is applied to AND gate 43F (sheet 3) and is one of four inputs needed to identify the major cycle sync word location.

The set output of CSR 64A (sheet 2), after being applied through an emitter follower, is used as the trigger input to the prime-frames-per-major-cycle counter. Thus, the prime-frames-per-major-cycle counter is caused to count whenever the words-per-prime-frame counter reaches the count established by its controlling switches.

The prime-frames-per-major-cycle counter is also controlled by a bank of switches on the rear panel. This counter is the same as those discussed previously, that is, the counter is reset when its count reaches that established by the rear panel switches. One of the purposes of the prime-frames-per-major-cycle counter is to count the number of prime frames in every major cycle. The basic count in the counter is also used in establishing the subframe sync word frame location and the major cycle unique word frame location. These two groups of switches are also located on the rear panel and derive their count as a result of the prime-frames-per-major-cycle counter counting.

As previously mentioned, the counter functions in the same manner as those discussed in preceding paragraphs, incrementing the count by one with every FR input until coincident with the count established by the rear panel switches, at which time the counter is reset to zero.

In addition to the three functions just discussed, the prime-frames-per-major-cycle counter is used to frame-locate the subframe sync word. The simulator is capable of generating an advancing or fixed ID word in bit positions three through 12 of the

subframe sync word and, in the advancing mode, of having the ID reset to either zero or one. In order to permit flexibility in the orientation of the advancing code, ID format patch cards are provided. Specifically, there are three types of etched circuit cards for this purpose:

- a. General Patching Card
- b. Gemini Format Patching Card
- c. Apollo Format Patching Card

The general case printed circuit card characteristics are:

- a. Pins 1,2, and 3 are used to reset the ID counter (prime-frames-per-major-cycle counter) to either a one or zero at the end of each major cycle.
- b. Pins 8, 10, 12, 17, 19, 21, 23, 25, and 27 are inputs from each stage of the ID counter.
- c. Pins 7, 9, 11, 13, 18, 20, 22, 24, and 26 are outputs that determine the bits effected in the subframe sync word.

Therefore, any ID bit can be patched to any output bit to form any ID word orientation. Pin 29 is reserved as an input for front panel toggle switch 3 of the subframe sync word. In the Gemini format the toggle switch continues to serve this function and is routed out on pin 7. In Apollo it does not.

The Gemini printed circuit card characteristics are: the ID counter is reset to zero at the end of each major cycle. Bit 3 of the ID word is controlled by front panel subframe sync word toggle switch 3; while bits 4 through 8 are controlled by counter stages 2<sup>6</sup> through 2<sup>2</sup> in descending order respectively. In the Gemini format there are 96 prime frames per major cycle while the ID count is only 24 (one ID count every four prime frames). By disregarding the first two stages of the prime-frames-permajor-cycle counter and patching in stages 3 through 7 (2<sup>2</sup> through 2<sup>6</sup>), the ID code appears as a count from 0 to 23 as the prime-frames-per-major-cycle counter counts from 0 to 95. The MSB of the ID code appears in the fourth bit of the subframe sync word, with descending order appearing in each subsequent bit.

The Apollo printed circuit card characteristics are:

- a. The ID counter is reset to one at the end of every major cycle.
- b. Bits 3 through 8 are controlled by counter stages 2<sup>5</sup> through 2<sup>0</sup> in descending order respectively.

The Apollo format requires that the ID code be incremented in every prime frame;

thus the ID count and the prime-frames-per-major-cycle count are the same. The MSB of the ID code appears in the third bit of the subframe sync word, with descending order occurring in each subsequent bit.

#### 8.2.6 MAJOR CYCLE UNIQUE WORD CHANNEL LOCATION SWITCHES

This bank of switches obtains its count as a result of the count of the words-per-prime-frame counter. Because a power inverter stage is located between each counter stage output and the switch bank, the number desired must actually be present in the counter to enable the summing AND gate associated with each group of switches. Assume the word is to appear in channel four, when the counter reaches the desired count three inputs to AND gates 43B and 43F are 0 volt. The fourth input for AND gate 43B is the major cycle unique word frame location pulse which is derived as a result of the switch settings for that function. These particular switches are associated with the prime-frames-per-major-cycle counter.

When all inputs to AND gate 43B are true, the gate produces its normal unloaded pulse of -10 volts, which is applied as an input to AND gate 47A and OR gate 57A. The output of AND gate 47A, which was at -10 volts and held AND gate 47B in the saturated condition, is driven to 0 volt. The other input to AND gate 47B is WRD. These two pulses true the AND gate and cause it to produce its unloaded pulse of -10 volts, which is applied to power inverter 50J, where it is inverted and applied to four power-inverter stages. These four stages again invert the pulse and apply it to the shift register set logic. The remaining three sets of switches function in the same manner (that is, major cycle sync word, subframe sync word, and prime frame unique word switches).

#### 8.2.7 OUTPUT SHIFT REGISTER SET LOGIC

Each power inverter drives at least four shift register logic cards; each card has two outputs. Each output is connected to the reset side of one stage of the output shift register. Hence all 33 stages of the shift register are controlled by the 17 shift register set logic cards. As shown in Figure 8-5, diode AND gates are formed by CR1 and CR3, CR5 and CR7, CR9 and CR11, CR13 and CR15, CR17 and CR19, CR21 and CR23. These six AND gates are ORd together through CR25, CR26, CR27, CR28, CR29, and CR30. These AND-OR gates control Q1, whose outputs are tied directly to the reset side of 17 shift register stages. The same situation exists for the operation of Q2. Six diode AND gates are formed by CR2 and CR4, CR6 and CR8, CR10 and CR12, CR14 and CR16, CR18 and CR20, and CR22 and CR24. Again, these six AND gates are ORd together through CR31, CR32, CR33, CR34, CR35, and CR36. These

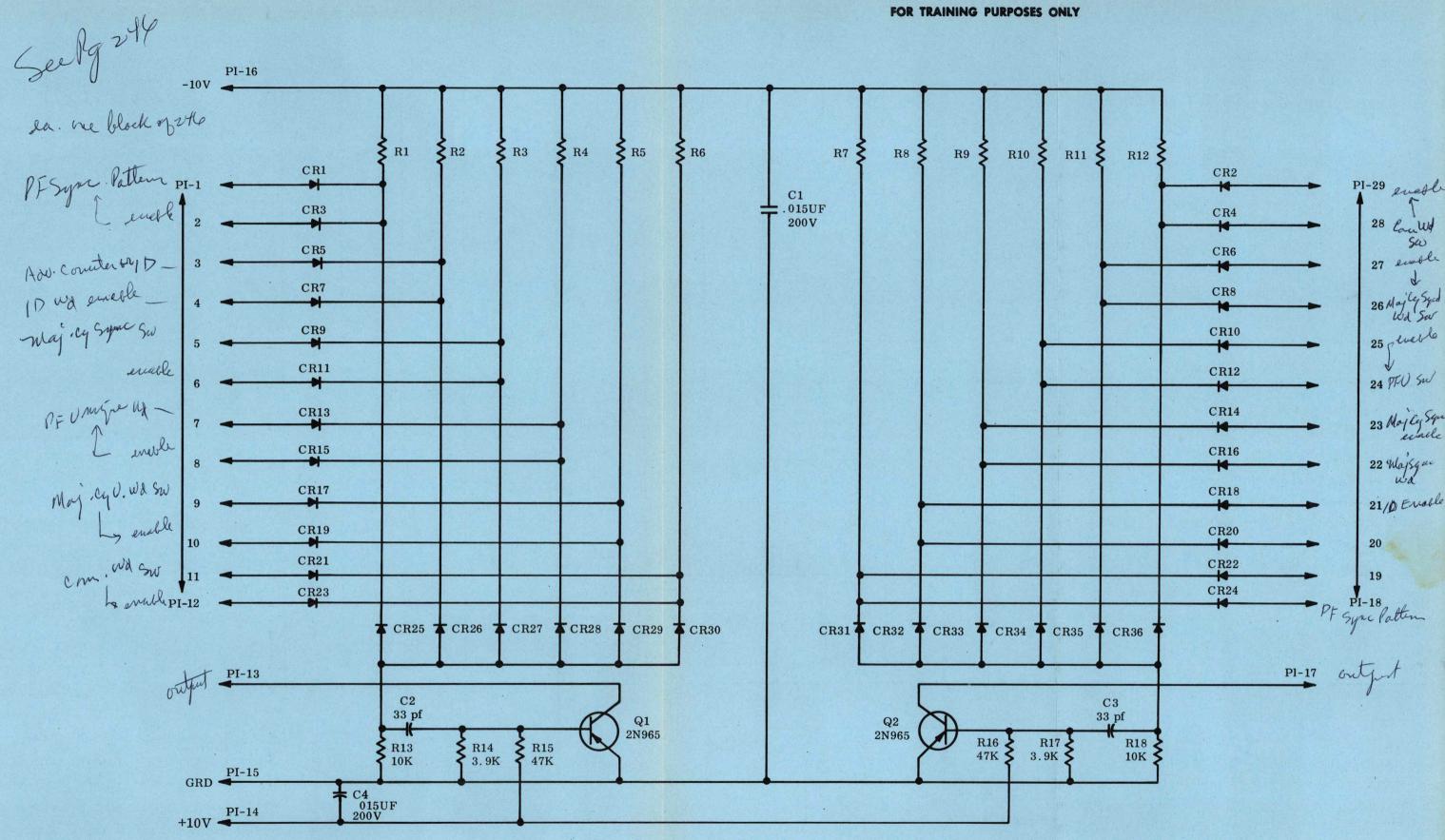


Figure 8-5. Shift Register Set

functional AND-OR gates control Q2, whose outputs are tied to the reset side of the remaining 16 shift register stages. One Q2 output is not used.

Assume the prime frame sync word has five bits in it and the binary pattern of the word is to be 10101. The count of five or binary 101 is set on the rear panel switches and the bits per-prime-frame sync word counterperforms the count at BR as described in the preceding paragraph. The binary pattern on 10101 is set on the switches on the front panel.

#### NOTE

The remaining 28 front panel switches must be set in the zero position, which ties them to ground.

When the prime frame sync word enable pulse is generated (which is a result of ANDing WRD from the set output of counter stage 36A and ST from the set output of counter stage 64A), the pulse is inverted and applied to four more power inverters in parallel, which again invert it. This -10-volt level pulse is applied to all 17 shift register set logic cards. The pulse is applied to pins 2 and 19 of P1 on all cards. This is one-half of a diode AND gate on the Q1 side and one-half of an AND gate on the Q2 side.

The first five switches are connected to five shift register set logic cards as follows: S8 to 96A pin 1; S9 to 95A pin 18; S10 to 95A pin 1; S11 to 94A pin 18; and S12 to 94A pin 1. These pins are the other one-half of the diode AND gates on those five cards.

The outputs of Q1 on cards 96A, 95A, and 94A are connected to the reset side of output shift register stages 97C, 97A, and 93B respectively. The output of Q2 on cards 95A and 94A are connected to the reset side of output shift register stages 97B and 93C respectively.

Hence the position of prime frame sync word switches S8, S9, S10, S11, and S12 determines the state of output shift register stages 97C, 97A, 93B, 97B, and 93C respectively. The shift register set logic card operates as follows:

- a. Transistors Q1 and Q2 on all cards are reverse biased by the 10 volts applied to the base of each.
- b. The outputs of the 17 Q1's are connected to the reset side of 17 shift register stages.
- c. Sixteen of the 17 Q2's are connected to the reset side of the remaining 16 stages. FOR TRAINING PURPOSES ONLY

Only the set side of all 33 stages of the shift register are used as output bits. The reset side is used to control each stage. All stages of the counter are held in the reset state until caused to be set by the shift register set logic cards, therefore, when the front panel switches are not in use or are all in the zero position, the outputs of the reset side of all counter stages are at -10 volts.

Placing S8 in the "1" position opens the line tied to pin 1 of card 96A. When the prime frame sync word enable pulse is applied to pin 2 of the card, it causes the applied -10 volts to develop a current through CR25. This causes C2 to discharge and start charging in the opposite direction. As a result of C2 being momentarily discharged, Q1 is turned on. Its output is connected directly to the reset side of register stage 97C. This forces the reset side of the stage to ground which, in turn, forces the set side to -10 volts. This is the required binary one. The shift register is shifted out in serial fashion at BR.

The switch set pattern, therefore, is entered into the shift register stages in parallel, because all front panel switches require the same enable pulse.

When S9 is placed in the "0" position, it ties pin 18 of card 95A to ground. The -10 volts applied to the card is therefore shunted to ground. Therefore, the prime frame sync word enable pulse on pin 19 has no effect on Q2, which remains in the cut-off condition. Hence, the set side of shift register stage 97B remains at 0 volt.

Placing S10 in the "1" position opens the line from pin 1 of card 95A. The prime frame sync word enable pulse is applied to pin 2 of this card. As previously stated, these two diodes form the AND gate.

When the line is open on pin 1 and the negative pulse applied to pin 2, it causes the applied -10 volts to develop a current through CR25. This causes C2 to discharge and charge in the opposite direction from the applied 10 volts. Because of the momentary lack of charge on C2 and the removal of -10 volts from its base, Q1 is turned on. This forces the reset side of 97A to ground which, in turn, forces the set side to -10 volts. This is the second binary one in the desired output pattern. It is also shifted out serially at BR.

The remaining two stages function the same as the three just discussed.

#### 8.2.8 SHIFT REGISTER OUTPUT LOGIC

Both the set and reset sides of the shift register are clocked out at BR to the contacts of a data-data switch mounted on the rear panel. The wiper arm output is applied to OR gate 98A. The other input to the OR gate is from CSR 36B. The inputs to gate 65F are from the set side of counter stage 64A and the subframe sync enable pulse, which is derived as a result of obtaining coincidence from ANDing the result of subframe sync word channel location and subframe sync word frame location switch settings. When either or both of these pulses are present, the OR gate produces its saturated output of 0 volt. When both inputs to the OR gate are at 0 volt, the gate functions as an AND gate and produces an unloaded output of -10 volts. In the example presented for the prime frame sync word, the shift register contains all zeros except for three stages which contain a binary one or -10-volt level. The output of the shift register and OR gate 65F being zero allows AND gate 98A to produce its unloaded output of -10 volts, which is applied to OR gate 98C. The output of OR gate 98A is -10 volts until the three binary one pulses are applied, at which time the output goes to 0 volt as a result of the gate being saturated.

#### 8.2.9 CODE FORMATTING

With S3 on the front panel in the COMMON position, the shift register output bypasses the OR logic and is applied directly to shift register stage 99A. This stage and associated logic establish the code format of the output (sheet 8, figure 6-54). The output is clocked out at BR. The set output of shift register stage 99A is the NRZC code format.

The output from the shift register is applied directly to the set side of shift register stage 99A. The same pulse is inverted and applied to the reset side also. The output of the set side is the NRZC code format; while the output of the reset side, after being ANDed with the inverted BR pulse, is provided as the RZ code format. The NRZC output, when ANDed with BR, and that output again ANDed with the RZ code format and this final output being inverted, is presented as the SP code format.

The NRZS code format is obtained by ANDing NRZC and BR. The output of this AND gate is applied to counter stage 99C. The set output of the counter stage is the NRZS code format.

NRZM code format is obtained by applying the RZ code format to counter stage 99B. The set output of the counter is the NRZM code format.

With S3 in the RANDOM position (this position allows a fixed noise level to be applied if desired) and this 0-volt level along with a 0-volt output from OR gate 98B applied, OR gate 98C produces its normal unloaded output of -10 volts. This is the binary one from the shift register. OR gate 98B is held in the saturated condition through the action of the CSR 36B any time any one of the control words is present. Noise can be applied to the data, or common words, through amplifier stage 49A.

The output code format is applied to AND gate 65H. This is ANDed with an external blanking pulse through J13 on the front panel. The resulting binary pattern is applied through an emitter follower to a summing resistive network. Noise may also be applied from an external source through J16. The output of the summing network is applied to a variable resistor, where the amplitude of the pulses can be adjusted. The pulses are tapped off the resistor, fed through an amplifier stage, and if S5 is closed or in the OUT position, applied to the front and rear output jacks.

#### SECTION 9

#### PROGRAMMING

### 9.1 INTRODUCTION

The development of a program for the series 540 PCM decommutator system is based primarily upon the characteristics of the incoming data and the pre-processing criteria of the data reduction and display programs. Although a detailed knowledge of PCM generation and multiplexing would aid the reader and provide latitude during the following discussion, it is not necessary, as a prerequisite, in developing a programming capability. Therefore, this section will present only that information required to provide the reader with a basic understanding of PCM general principles and its specific application in the ACE-S/C program.

PCM data can be compared to writing. The lowest order in writing is a letter, while in PCM, it is a bit. Table 9-1 can be used to make this comparison.

Table 9-1
Comparison of PCM Data with Writing

PCM Data	Writing
Bit	Letter
Words	Words
Prime Frame	Sentence
Major Cycle	Paragraph

The number of bits or letters in any given word depends upon the word itself. This is also true of the number of words in a prime frame or in a sentence, and the number of prime frames in a major cycle or number of sentences in a paragraph.

PCM words are of three types, based upon the rate that they are input. These are:

- a. Normal-commutated words.
- b. Super-commutated words.
- c. Sub-commutated words.

Normal-commutated words are sampled at least once a prime frame. Super-commutated words are sampled more than once a prime frame. Sub-commutated words are sampled less than once a prime frame.

In programming, normal- and super-commutated words are considered the same and are called prime frame data words. At this time it should be noted that the prime frame sync word and the ID sync word are considered to be prime frame data words because they do appear at least once a prime frame.

Figure 9-1 represents a serial PCM data train, with the PF sync word the first word received, the ID sync word the second, word A the third, and word J the last word in this prime frame. All the words in this particular example are prime frame data words and are commutated at a normal commutation rate. Super-commutated words are also prime frame data words (Figure 9-2), and word A is an example of a super-commutated word. All other words in Figure 9-2 are normal commutated. When super-commutated words are used, the number of unique data words possible in any one prime frame is decreased. In order to super-commutate you repeat the particular word symetrically in other word slots until the desired commutation rate is reached.

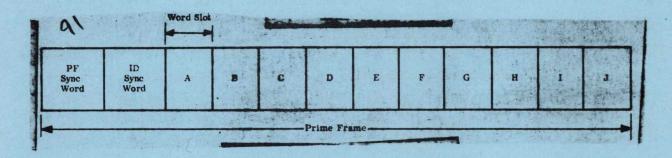


Figure 9-1. Serial PCM Data Train (Normal Commutation)

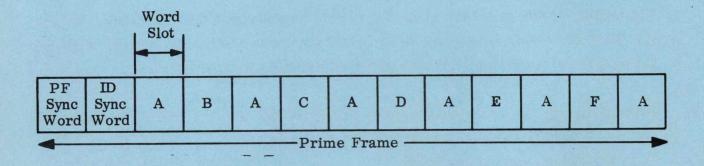


Figure 9-2. Serial PCM Data Train (Super Commutation)

If the serial PCM data contains only prime frame data words as shown in Figures 9-1 and 9-2, then one prime frame equals a major cycle. Figure 9-3 shows an example of a one prime frame/major cycle with normal- and super-commutated words in the prime frame/major cycle. In this situation, a frame and a major cycle are equal in length.

Prime Frame	PF Sync Word	ID Sync Word	A	В	A	С	A	D	A	E	A	F
Prime Frame	PF Sync Word	ID Sync Word	A	В	A	С	A	D	A	E	A	F
Prime Frame	PF Sync Word	ID Sync Word	A	В	A	C	A	D	A	E	A	F
Prime Frame	PF Sync Word	ID Sync Word	A	В	A	С	A	D	A	E	A	F
Prime Frame	PF Sync Word	ID Sync Word	A	В	A	С	A	D	A	E	A	F

Figure 9-3. Prime Frame/Major Cycle

When sub-commutated words are found in the serial PCM data, the number of prime frames in the major cycle is dependent upon the rate of the slowest sub-commutator. Therefore, the time for one major cycle is equal to the rate of the slowest sub-commutator. For example, for a sub-commutator of 1s/s the major cycle time would be one second. Anytime sub-commutation is used a frame is not equal to a major cycle.

In the ACE-S/C system, a major cycle does equal 1 second and contains 50 prime frames; therefore, all commutation rates subsequently discussed will use the 1-second time base. With a 1-second time base, normal commutations equal 50 samples per second, super-commutations equal something more than 50 samples per second, and sub-commutations equal something less. Since the slowest sub-commutation rate determines the number of prime frames in a major cycle, and ACE-S/C contains 50 prime frames, a sub-commutator of 1 sample per second is present.

Figure 9-4 contains a 1-sample-per-second sub-commutated word in time slot 9. Time slot 4 contains a 10-sample-per-second sub-commutated word (based on the ACE-S/C format). In the 1s/s word slot each word in each frame is derived from a different source, but the 10s/s word is repeated in frame time six.

In the programming of the decommutator, one has to know the type word in each of the time slots of a prime frame because of memory addressing. Decommutator memory addressing is accomplished by 13 stage counters (13 stage counters are needed to address 8192 locations) and there are six counters. These counters are:

- a. Auxiliary Counter.
- b. Block 0 Counter.
- c. Block 1 Counter.
- d. Block 2 Counter.
- e. Block 3 Counter.
- f. Block 4 Counter.

The auxiliary counter is used to load the decommutator memory with a program. It does not matter from what source the program is being loaded (computer, paper tape, or manually), the auxiliary counter will sequential-load the memory. The auxiliary counter is also used to unload the memory when a program is called out for program check. Nothing can be done by the program to control the action of the auxiliary counter.

Block 0 counter is used to decommutate prime frame data words as these words are input at the frame rate or higher. This block counter is controlled by the decommutator software program.

Block counters 1 through 4 are normally used for sub-commutated data words and each counter decommutates one sub-commutator. The block counters are controlled by the decommutator software program. The above stated facts is the conventional method of block counter usage; however, any counter can be used for any type of commutation rate except block zero, which must be used for normal rates to obtain ID synchronization.

In constructing a decommutator program, four types of words are used. The first of these are the sequences. The sequences are necessary to initiate the decommutation of incoming PCM data. Each is assigned a sequence number to identify the information in the word. There are 32 sequences available in the 540 decommutator and each utilizes one decom memory location. Bit 1 of each word is a parity bit, selected to produce even parity in the word. Bits 2 through 6 of each word are for coding of the sequence number. Sequence 00 must always be the first accessed from memory and sequence 31 must be the last—no other order is required.

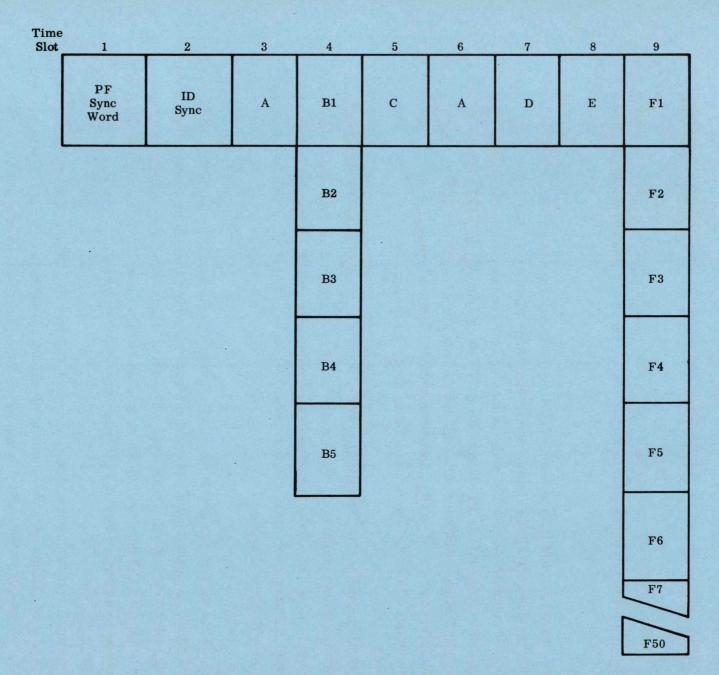


Figure 9-4. Samples per Second, Sub-Commutated Words, Time Slots 4 and 9

Some sequences may be omitted if they are not needed because all programs do not use the entire decom capability. Sequence numbers 11 and 16 should always be used, even if subframe synchronization is not used; this insures that the unused subframe synchronized circuits are turned off. The unused parts of the words may be filled with "zeros." Preacquisition words are loaded sequentially, starting at the Program Starting address, bits 28 to 40 of sequence 0.

The contents of each preacquisition word are explained in Table 9-2. For convenience, this information is condensed in Figure 9-5. Figure 9-6 is an example of a preacquisition block.

The second word is the control and routing (C&R) instruction word. Each data word has a unique control and routing word. The Block 0, Block 1, Block 2, Block 3, and Block 4 counters are used to address memory for reading out the various C&R words. Each block counter is used to address a particular type of data word based on their sampling rates. Block 0 counter is always used for prime frame data words; however, this is the only basic requirement for counter programming because any of the subcommutator counters can be used for prime frame words.

The third word is the ID instruction word. This word controls the decommutator, by speeding up the major cycle synchronization process by jamming the applicable block counters to an address correlating to the proper memory location with the incoming frame. The number of ID instruction words is always equal to the number of prime frames in a major cycle.

The fourth word is the Direct Access Computer Interface instruction word. This word, also under program control, is obtained from memory by the same block counters that accessed memory for the C&R word. The DACI word defines the processing information for a PCM data word if the word is to be processed. A DACI word is obtained from memory each time the PCM data word is to be processed.

An example of sub-commutation is shown in Figure 9-7. Words B, D, J, and L are parameters sampled at a sub-commutation rate, all other parameters in this example are at prime frame rate and will appear the same word slot in each frame.

Figure 9-8 depicts the three basic operating words of the decommutator.

Some functions are common and will be identified.

Table 9-2
Preacquisition Word Contents

Sequence Number	Bits	Explanation
0	7-24	These bits are unused. They should be all "zeros."
	25-27	Program number - Program 8 code is 000. Programs 1 through 7 use standard binary codes.
	28-40	Program starting address.
1	7-38	Prime frame synchronization (PFS) pattern - Bit 7 contains last PFS pattern bit.
2	39-40 7-38	Not used.  Prime frame synchronization pattern continuation - Pattern bit 33 in word bit 38. This sequence number is used only if PFS pattern is over 32 bits long.
	39-40	Not used.
3	7-38	PFS length - A"1" allows comparison of corresponding bit in sequence number 1 with incoming data. A"0" inhibits comparison.
	39-40	Not used.
4	7-38	PFS length continuation - For PFS patterns over 32 bits long. This sequence number must be used if the decommutator has 64-bit comparison circuits, even if PFS pattern is less than 32 bits long. It need not be used if the decommutator has only 32-bit comparison circuits.
	39-40	Not used.
5	7-10	PF bit errors - Search mode. Sets the greatest number of bit error that may occur and still allow the decommutator to recognize synchronization patterns in search modes.
	11-14	PF bit errors - Check and lock mode. Sets the greatest number of bit errors that may occur in a PFS word before an error, or miss signal, is generated.
	15-17	Number of prime frames checked in check mode - Sets the number of PFS patterns that are checked before the decommutator will advance from check mode to lock mode. All PFS patterns checked must have fewer bit errors than allowed in the search mode.

Table 9-2
Preacquisition Word Contents (Cont.)

Sequence Number	Bits	Explanation
5 (Cont.)	18-19	Number of misses allowed (check mode only) - Sets the number of PFS word misses that may occur before the decommutator must return to the search mode to acquire a better synchronization pattern.
	20	PF aperture - Sets the time during which a PF synchronized pulse must occur in order for the decommutator to remain in the lock mode. A "1" allows a 1-bit time aperture. A "0" allows a 3-bit time aperture.
	21-23	PFS pattern type - For true synchronization only, use the code 011. If synchronization or synchronization is acceptable, use 101. For alternating synchronization and synchronization, use 110.
	24	ID synchronization On-Off. A "1" is used if ID synchronization is used.
	25-26	ID reset - These bits determine which block counter recycle code is also used to recycle the ID block counter.  The codes used are:
		Reset ID Counter Code
		Block 1 10
		Block 2 01 Block 3 11
		Block 4 00
		The ID block counter may not be reset by the block 0 counter. Normally, the ID block counter is reset by the block counter with the highest sub-commutation ratio, that is, by the block counter which recycles only once per major cycle.
	27	Data MSB/LSB - A "1" is used for data MSB first. A "0" is used for data LSB first.
	28	ID countup or countdown - Informs the ID circuits of the direction of counting in the incoming ID data. A "1" is used for countdown. A "0" is used for countup.
	29	ID LSB or MSB first - This bit determines which direction to shift in the ID data register. A "1" is used for ID MSB first data. A "0" is used for ID LSB first data.
	30-35	ID position - This number is the number of shifts in the 9-bit long ID data register necessary to bring the data bits into the proper register positions plus one. ID LSB/MSB first and fixed ID bits affect the number of shifts necessary.

Table 9-2
Preacquisition Word Contents (Cont.)

Sequence Number	Bits	Explanation
5 (Cont.)		The number of shifts may be computed from the following equations:
		ID LSB: ID Position = 10 + Fixed bits Preceding ID Bits in ID Word
		ID MSB: ID Position = 1 + Fixed Bits + Number of ID Bits
	36-38	ID length - Sets the length of the data part of the ID word (fixed bits are not included in this number). The codes used are:
		<u>ID Data Bits</u> <u>Code</u>
		9 000 8 100
		7 010
		6 110 5 001
		$egin{array}{cccccccccccccccccccccccccccccccccccc$
	39	Not used.
	40	ID Off sub-commutator - If the ID word occurs once every prime frame, the ID is not off a sub-commutator. A "0" is used for this condition. If the ID occurs once every subframe, a "1" is used.
6	7-9	Word synchronization pattern - The first bit in the pattern is in word bit 9.
	10-12	Word synchronization length - A "1" allows comparison of the corresponding pattern bit with incoming PCM bits. A "0" inhibits comparison.
	13	Word synchronization bit error - Search. A "1" allows one error. A "0" allows no error.
	14	Word synchronization bit error - Lock. Same as search.
	15-17	Number of words checked - Same as for sequence number 5.
	18-19	Number of misses allowed - Same as for sequence number 5.
	20	Not used.
		FOR TRAINING BURBOSES ONLY

Table 9-2
Preacquisition Word Contents (Cont.)

Sequence Number	Bits	Explanation
6 (Cont.)	21	Parity position - A "1" indicates that the parity bit is the first bit of the word. A "0" indicates that it is the last bit.
	22-40	Not used.
7	7-38	Subframe 1 synchronization pattern - Same as for sequence number 1.
	39-40	Not used.
8	7-38	Subframe 1 synchronization pattern continuation - Same as for sequence number 2.
	39-40	Not used.
9	7-38	Subframe 1 synchronization length - Same as for sequence number 3.
	39-40	Not used.
10	7-38	Subframe 1 synchronization length continuation - Same as for sequence number 4.
	39-40	Not used.
11	7-10	Subframe 1 bit errors - Search.
	11-14	Subframe 1 bit errors - Lock.
	15-17	Subframe 1 synchronization type - Synchronization only, synchronization or synchronization, alternating.
	18	Subframe 1 On-Off - A "1" indicates subframe 1 is on.
	19-24	Not used.
	25-28	Read Pulse Inhibit Code as follows:  0000 - PF Lock
	29-40	Not used.
12	7-38	Subframe 2 synchronization pattern.
	39-40	Not used.
1 13	7-38	Subframe 2 synchronization pattern continuation.

Table 9-2
Preacquisition Word Contents (Cont.)

Sequence Number	Bits	Explanation	
13 (Cont.)	39-40	Not used.	
14	7-38	Subframe 2 synchronization length	
	39-40	Not used.	
15	7-38	Subframe 2 synchronization length continuation.	
	39-40	Not used.	
16	7	Subframe 2 On-Off - A "1" indicates subframe 2 is on.	
	8-11	Subframe 2 bit errors - Search.	
	12-15	Subframe 2 bit errors - Lock.	
	16-18	Subframe 2 synchronization type.	
	19	Subframe 3 On-Off.	
	20-23	Subframe 3 bit error - Search.	
	24-27	Subframe 3 bit error - Lock.	
	28-30	Subframe 3 synchronization type.	
	31-40	Not used.	
17	7-38	Subframe 3 synchronization pattern.	
	39-40	Not used.	
18	7-38	Subframe 3 synchronization pattern continuation.	
	39-40	Not used.	
19	7-38	Subframe 3 synchronization length.	
	39-40	Not used.	
20	7-38	Subframe 3 synchronization length continuation.	
	39-40	Not used.	
29	7-10	Not used.	
	11-14	Bit synchronizer program selector - Sets the frequency range of the bit synchronizer. Program 9 allows frequency adjustment by controls on the bit synchronizer panel. The	

Table 9-2
Preacquisition Word Contents (Cont.)

Sequence Number	Bits	Explanation		
29 (Cont.)		codes used to select the programs are:		
		<u>Program</u> <u>Code</u>		
		1 0001 2 0010 3 0011 4 0100 5 0101 6 0110 7 0111 8 0000 9 1000		
•	15-27	ID block starting address - These bits tell the ID ADDER where to start reading ID program words. This does not control the <u>loading</u> of the ID program words.*		
	28-40	Block 0 starting address - These bits tell where the zero block counter should start reading its program words.		
30	7	DACI Enable.		
	8-13	Floating Point Tolerance.		
	14	Not used.		
	15-27	Block 1 starting address.		
	28-40	Block 2 starting address.		
31	7-14	Not used.		
	15-27	Block 3 starting address.		
*If the ID co	28-40	Block 4 starting address.		

\*If the ID counts from 1 up or down to 1, start the ID block at one address less than the actual starting point.

The control and routing instruction word format can be divided into two major sections:

- a. Control or operational codes, which are concerned with the internal operation of the decommutator.
- b. The routing codes, which are concerned with the distribution of decommutated data to displays and outputs.

ITEM	CODING	FUNCTION
PFS,WORD SYNC, SF	1	BIT ALLOWED IN CORRELATION
Pro, CORD SINC, SP	0	BIT INHIBITED IN CORRELATION
	1	1-BIT APERTURE
PFS ARERTURE	0	3-BIT APERTURE
SYNC, COMP, ALT	011	SAMPLE SYNC ONLY
FOR PRIME FRAME	101	SAMPLE SYNC OR COMPLEMENT
AND SUBFRAME	110	SAMPLE ALTERNATE SYNC ECOM
	1	IDON
IDON	0	ID OFF
	00	BLOCK 4
	10	EXPLOSION TO A DESCRIPTION OF THE PERSON OF
ID RESET	01	2
	11	BLOCK 3
RESIDENCE OF STREET	1	COUNT DOWN
ID CU/CD	0	COUNT UP
CHARLES PARTY OF THE PARTY OF	1	MOST SIGNIFICANT BIT FIRST
ID LSB/MSB DATA LSB/MSB	0	LEAST SIGNIFICANT BIT FIRST
THE RESERVE AND THE PARTY.	000	USE 9 COUNTER STAGES
	100	
	010	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
ID LENGTH	110	6
	001	Marie Street Constitution Street
	101	4 house and the second second
Contraction of States	011	USE 3 COUNTER STAGES
ID OFF SUBCOM		YES
.5 011 30500101	0	NO
WS BIT ERRORS	100	IBIT ERROR ALLOWED
SEARCH	0	0
WS BIT ERRORS	1	Christian and District Assessment
LOCK	0	OBIT ERRORS ALLOWED
PARITY POSITION		FIRST BIT OF WORD
PARITY POSITION	0	LAST BIT OF WORD
SELSES deep out		SUBFRAME SYNC USED
SF 1,5F 2, ESF3 ON	0	SUBFRAME SYNC NOT USED
BIT SYNC	23-20	FORMATS I THRU 7
FORMAT SELECT		FORMATS 8

ITEM	CODING	FUNCTION
LIMIT	0	PEOGRAM CONTAINS NO LIMIT
	1	PROGRAM CONTAINS LIMIT CHECK INSTRUCTIONS
FULL SYNC	1	ENABLE ID VERIFIED
	_1	ENABLE SF * I SYNC COMPARISON
	1_	ENABLE SF#2 SYNC COMPARISON
		ENABLE SF #3 SYNC COMPARISON

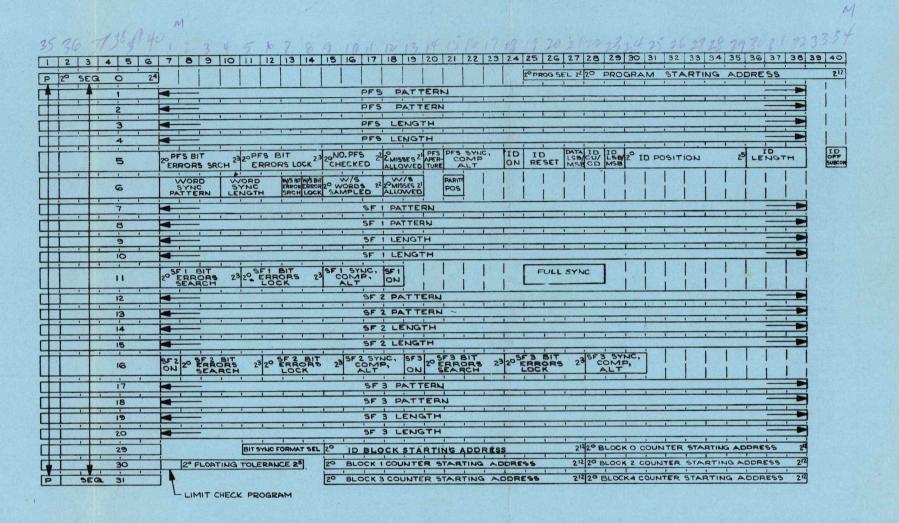


Figure 9-5. Preacquisition Word Formats

MEMORY BIT NUMBER

1		2	3	4	5	6	7	8	9	10	1	1	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
1		0	0	0	0	0			9			0				0				e.			1			0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0		1	0	0	0	0	0	1	0	0		1	1	0	0	1	1	0	1	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		
0	I	1	1	0	0	0	1	1	1	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		9
1	T	1	0	1	0	0	0	0	0	0	I	0	0	0	0	0	0	1	0	0	1	1	1	0	1	1	0	1	0	1	1	0	0	1	0	0	1	0	1		1
ī		1	1	1	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	1	1	0	1	0	1	0	0	0		
1		1	0	0	1	0	0	0	0	0		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
0		1	1	0	1	0	0	0	0	0		0	0	0	0	0	1	1	1			9	9	•				•							9						
ī		0	0	0	0	1	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
0		1	0	1	1	1					*	1	0	0	0	0	0	0	1	1	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	0
0	1	0	1	1	1	1				,		0	9	•		1	1	1	1	1	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	1	0	0	0	1	0
1		1	1	1	1	1		•	0			1		1		0	0	0	0	1	0	1	1	0	0	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	0

SEQUENCE NUMBER	OCTAL ADDRESS	EXPLANATION
0	17772	PROGRAM NO. 2. START LOADING PROGRAM IN LOCATION 04200g
	04200	PF SYNC PATTERN
3	04201	PF SYNC LENGTH = 24 BITS
5	04202	PF BIT ERRORS - SEARCH = 0 NUMBER OF PRIME FRAMES CHECKED = 4 PF BIT ERRORS - LOCK = 0 NUMBER OF MISSES ALLOWED = 0
		PF APERTURE = 1 BIT ID ON = YES ID CU/CD = CU DATA LSB/MSB = MSB PF SYNC TYPE = ALTERNATE ID RESET = BLOCK 4 ID LSB/MSB = MSB ID POSITION = 9 ID LENGTH = 3 ID OFF SUBCOM = YES
7	04203	SF SYNC PATTERN
ó	04204	SF SYNC LENGTH = 19 BITS
ıí	04205	SF BIT ERRORS - SEARCH = 0 SF SYNC TYPE = SYNC ONLY SYNC = ID SF BIT ERRORS - LOCK = 0 SF SYNC NO. 1 ON = YES
16	04206	USED ONLY TO TURN SUBFRAMES 2 & 3 OFF
29	04207	BIT SYNCHRONIZER PROGRAM = 9 (VARIABLE) ID BLOCK START = 04730 <sub>8</sub> BLOCK 0 START = 04220 <sub>a</sub>
20	04210	BLOCK 1 START - 042208 BLOCK 2 START - 04212 DACL - ON TOLEDANCE - 7
30 31	04211	BLOCK 1 START = 042378 BLOCK 2 START = 043128 DACI = ON TOLERANCE = 7 BLOCK 3 START = 043208 BLOCK 4 START = 045108

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Figure 9-6. Example of Preacquisition Block

	Subcommutated at 10 Samples Per Second													Subcommutated at 1 Sample Per Second			
Frame No. 1	PF Sync	ID Sync	A	В1	С	D1	E	F	G	Н	I	J1	К	L1			
Frame No. 2	PF Sync	ID Sync	A	B2	C	D2	E	F	G	Н	I	J2	K	L2			
Frame No. 3	PF Sync	ID Sync	A	В3	С	D3	E	F	G	Н	I	<b>J</b> 3	K	L3			
Frame No. 4	PF Sync	ID Sync	A	В4	С	D4	E	F	G	Н	I	J4	К	L4			
Frame No. 5	PF Sync	ID Sync	A	B5	С	D5	E	F	G	Н	I	<b>J</b> 5	К	L5			
Frame No. 6	PF Sync	ID Sync	A	В1	С	D1	E	F	G	Н	I	<b>J</b> 6	K	L6			
Frame No. 7	PF Sync	ID Sync	A	В2	С	D2	E	F	G	н	I	J7	K	L7			
Frame No. 8	PF Sync	ID Sync	A	В3	С	D3	E	F	G	н	I	<b>J</b> 8	К	L8			
Frame No. 9	PF Sync	ID Sync	A	В4	С	D4	E	F	G	н	I	<b>J</b> 9	K	L9			
Frame No. 49	PF Sync	ID Sync	A	B4	C	D4	E	F	G	Н	I	J49	К	L49			
Frame No. 50	PF Sync	ID Syn	A	В5	C	D5	E	F	G	Н	I	<b>J</b> 50	К	L50			

Figure 9-7. Example of PCM Data Train With Two Subcommutated Rates

Figure 9-8A. Normal Control and Routing Word

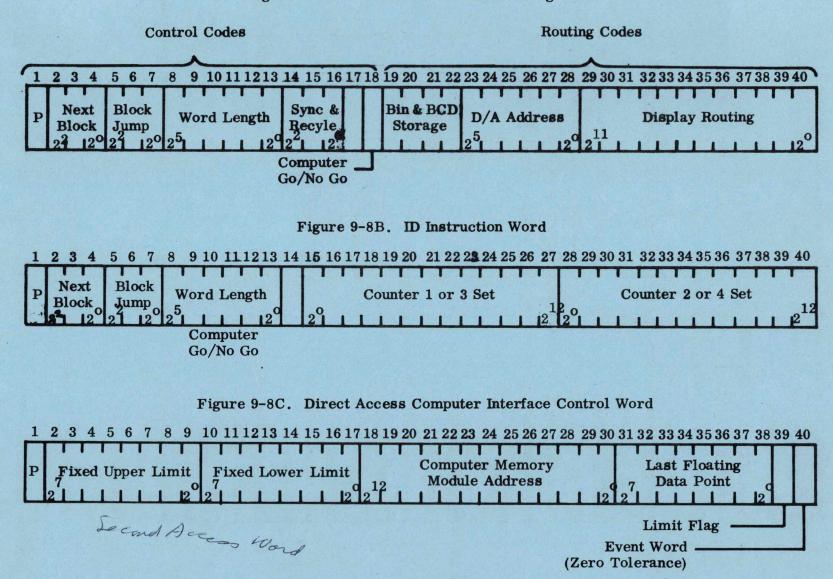


Figure 9-8. Instruction Word Formats

The functions of the operational codes are as follows:

- a. Next block—The next instruction to be executed is at the address contained in the specified block counter. This is common to the C&R and the ID instruction words.
- b. <u>Block jump</u>—When sub-sub-commutation is used, it is often necessary to transfer to a different block from that specified by a next block instruction. This is common to the C&R and the ID instruction, however, is not used in ACE-S/C.
- c. Word length—The word length refers to the number of bits in the data word.

  This is common to the C&R and the ID instruction words.
- d. Synchronization, ID, and recycle—The pattern of bits in this code indicates whether an ID pattern is contained in the data, what synchronization information is in the data, and whether or not to recycle the block counter. The ID code may be combined with the synchronization or recycle information if necessary. A summary of the operational codes is given in Table 9-8.

The functions of the routing codes are:

- a. <u>Channel strip</u>—This is a marker bit to allow external equipment to extract selected channels from the decommutator output (not used in ACE-S/C).
- b. <u>Computer Go/No Go</u>—This bit allows the individual selection of T/M data to be processed by the decommutator and sent to the downlink computer.
- c. <u>Binary and BCD storage</u>—These bits provide for the address of binary and BCD registers for the storage of selected data measurands (not used in ACE-S/C).
- d. <u>Digital-to-analog address</u>—These bits address a digital-to-analog converter for conversion of a selected measurand.
- e. <u>Display address</u>—These bits provide a preprogrammed code for external devices so that they may remotely select a particular data channel or channels for monitoring. Since the display address has no function inside the decommutator, its programming may be varied at will to meet the needs of the user.

Table 9-4 shows the routing instruction codes that are used.

In programming the decommutator, it may well be noted that the two parts of the control and routing word are for different telemetry samples. The C&R word is called from the decommutator memory during the previous word time of the word to be

decommutated; e.g., if the C&R is for word 4, it is called from memory during word 3 processing time. The next block and block jump instructions of the C&R word are for word 5. All other instructions are for word 4.

Table 9-3
Operational Codes

		Cod	le	
Name	Bit Numbers	Binary	Octal	Explanation
Next Block	2, 3, 4	000	0	Next Block is Block 0
		001	1	Next Block is Block 1
		010	2	Next Block is Block 2
		011	3	Next Block is Block 3
		100	4	Next Block is Block 4
Block Jump	5,6,7	000	0	No Block Jump
		001	1	Jump to Block 1
		010	2	Jump to Block 2
		011	3	Jump to Block 3
		100	4	Jump to Block 4
Word Length	8-13	000100	04	Word Length = 4 bits
		111111	77	Word Length = 63 bits
		000000	00	Word Length = 64 bits
Synchronization, ID, and Recycle	14, 15, 16	000	0	No Synchronization in this Word
		100	4	ID Synchronization Pattern in this Word
		010	2	Partial Synchroniza- tion Pattern in this
	Parties of the state of the sta	001	1	Word Synchronization Pat- tern is Completed in
		011	3	this Word Recycle this Block Counter

Table 9-4
Routing Codes

Name	Bit Numbers	Code	Explanation
Channel Strip	17	1 0	Strip this Channel Do Not Strip this Channel
Computer Go/No Go	18	1 0	Enable the DACI and Limit Check. Do not enable DACI.
On-Off Dump	18	Not Used 1 In ACE 0	Dump this On-Off Data Do Not Dump this Data
BIN/BCD Storage	19-22	0000 0001 0110 0111 1000 1011	Do Not Store Store this Data in BCD Store No. 1  Store this Data in BCD Store No. 6 Store this Data in Binary Store No. 1 Store this Data in Binary Store No. 2  Store this Data in Binary Store No. 5
D/A Address	23-28	000 000 000 001 111 111	No D/A Selected Route this Data to D/A No. 1  Route this Data to D/A No. 63
Display Address	29-40	000 000 000 000	This Data can be Selected by Address 000 000 000 000  This Data can be Selected by Address 111 111 111 111

Figure 9-8B depicts the ID instruction word. The function of the ID instruction word is to insure that the sub-commutators are synchronized with the prime frames. The ID instruction word is called from memory in place of a normal control and routing word. When synchronization has been established, the block counters are jammed to the memory location that coincides with the appropriate prime frame. As shown in Figure 9-8B, only two block counters can be updated at one time with an ID instruction word. If the ID count is even, block counters 1 and 2 will be updated. If the ID is odd, counters 3 and 4 will be updated. If only two sub-commutator block counters are used, synchornization of the counters will be made in one frame; however, if 3 or 4 sub-commutator block counters are used, two frames are needed to establish full sync.

The last word in Figure 9-8C is the direct access computer interface instruction word which obtains the preprogrammed information used in the checking and routing of telemetry data to the computer. This word always follows the control and routing word that specified route-to-computer and is programmed in the next sequential memory location. The fixed upper and lower limit remain constant for any given analog input word and is only used in the checking of parameter data. The computer memory module address defines the location in the 160G memory bank where the processed parameter data is to be stored. The last floating data point is loaded by decommutator DACI logic when the incoming telemetry data is out of tolerance by an amount specified by the preacquisition program. The limit flag is a programming aid and can vary depending upon whether the upper limit or lower limit is designated to control the flag to the computer. The event word bit defines that the incoming data is of event origin or that the analog word is to be checked for zero tolerance.

# 9.2 PROGRAMMING EXAMPLES

In ACE-S/C there are four different operational types of programs to be discussed—decommutation of the airborne format at 51.2 k/b per second, decommutation of the interleaved format at 204.8 k/b per second, decommutation if the 51.2 k/b the airborne format utilizing second access, and decommutation of the 204.8 k/b format utilizing second access. All four methods of programming will be discussed.

# 9.3 PROGRAMMING WITHOUT SECOND ACCESS

When programming without second access, the requirement of the decommutator is that prime frame data words are decommutated by block zero and all other sub-commutators are controlled by block counters 1-4. Each control and routing word for any sub-commutator group is programmed sequentially in the applicable memory block. When no second access is specified, all telemetry data is routed via the 171G I/O unit and in this situation bit 18 of the control and routing word remains a constant zero. Also, bit seven of sequence 30 will be programmed a constant zero.

With no second access and the requirement for telemetry transfer to the computer is at sample rate, the numbers of memory locations used by block zero will be equal to the number of prime frame data words per prime frame. Keep in mind that regardless of the operation of the decommutator, block zero must operate at prime frame rate to establish ID synchronization. Therefore, in accordance with the telemetry format in Figure 9-9 block zero's length will be equal to 10 clocations. The starting location in memory can be arbitrary and all control and routing words programmed sequentially.

Wd.	DATA	Wd.	DATA							
1	SYNC	33	12A1							
2	SYNC	34	12A2							
3 .	SYNC	35	12A3							
4	ĮD .	36	12A4							
5	51A2	37	12A5							
6	51A3	38	11D1 11D2 11D3 11D4 11D5							
7	51A4	39	51A18							
8	51A5	40	11A11 11A12 11A13 11A14 11A15							
9	51A6	41	12A6							
. 10	51A7	42	12A7							
_ 11	51A8	43	51A19							
12	51A9	44	51A20							
13	51A1O	45	11A16 11A17 11A18 11A19 11A20							
14	51A11	46	11A21 11A22 11A23 11A24 11A25							
15	51A12	47	11A26 11A27 11A28 11A29 11A30							
16	51A13 .	48	11A31 11A32 11A33 11A34 11A35							
17	51A14	49	11A36 11A37 11A38 11A39 11A40							
18	51A15	50	11A41 11A42 11A43 11A44 11A45							
19	51A16	.51	11A46 11A47 11A48 11A49 11A50							
20	51A17	52	1106 1107 1108 1109 11010							
21	22A1	53	22A1							
22	22A2	54	22A2							
23	22A3	55	22A3							
24	22A4	56	22A4							
25	22D1	57	22D1							
26	2202	58	22D2							
27	22D3	59	22D3							
28	1201	60	51A21							
29	1202	61	51A22							
30	12D3	62	51A23 ·							
31	1204	63	51A24							
32	1205	64	12A8							

Wd.			DATA			Wd.	DATA
65	10A10	1		1	0A150	97	12A1
66	10A51			<sub>L</sub>	OA100	98	12A2
67			51A2	5		99	12A3
68			51A2	6		100	12A4
69			51A2			101	1245
70			51A2			102	51A38
71			51A2	9		103	51A39
72	11A51	11A52	11A53	11A54	11A55	104	51A40
73	11A56	11A57	11A58	11A59	11A60	105	12A6
74	11A61	11A62	11A63	11A64	11A65	106	12A7
75	100200	10020	4		10D400	107	51A41
76			51A3	10		108	51A42
77			51A3	1		109	51A43
78		Salt	51A3	12		110	51A44
79			51A3	3		111	51A45
80			51A3	14		112	51A46
81			51A3	35		113	51A47
82			51A3	36		114	51A48
83			51A3	37		115	51A49
84	10D1-			10	D50	116	10D5110D100
85			22A1			117	22A1
86			22A2			118	22A2
87			22A3			119	22A3
88			22A4			120	22A4
89			22D1			121	22D1
90			2200			122	22D2
91			22D3			123	22D3
92			12D1			124	10A110A50
93			12D2			125	10D10110D150
94			1203			126	51A50 °
95			12D4			127	51A51
96			12D5			128	1248

Using this example, block zero's first word would pertain to the prime frame synchronization pattern and would be programmed for a word length of 24 bits, and the second word would pertain to the ID, etc. All remaining word lengths would remain at eight. The next block instruction remains 'next block = 0" until word time 37 when the control for word 38 is read from memory. This next block instruction would define a subcommutator counter. In accordance with this example this is the first sub-commutator encountered thus far; therefore, the starting address could be a few subsequent locations after the end of the block zero. The block counter used for 10 sample per second sub-commutated data would utilize 65 memory locations. The first time the block counter for 1 sample per second data would be specified would be during word time 64, and the counter controlling this sample rate would utilize 350 memory locations.

Thus, including all three block counters and the preacquisition information the following tabulation of memory locations would be for the example of airborne data in Figure 9-9.

 Preacquisition
 9

 Block Zero
 106

 Block One
 65

 Block Two
 350

 Total
 530

Using these locations lengths as reference, each block counter used would be recycled after stepping through its entire allocated memory locations. One additional function of counter recycle is that the ID frame counter should be recycled by the slowest sub-commutator which is, in this case, block two or the 1 sample per second block counter.

In programming the decommutator for the interleaved program, a number of circumstances must be taken into consideration:

- a. What is the configuration of the input PCM format?
- b. What is the change or changes in the prime frame sync word?
- c. Where does the ID sync word appear in the prime frame?
- d. What words in the prime frame are always blank or zero?

The interleaver, located in the spacecraft vicinity, outputs words designated A1, B1, C1, D1 through A128, B128, C128, D128 which adds up to 512 time slots per prime

frame, but due to the interleaver inserting a synthetic sync word during the A1 through D1 time slots, the resulting total words per prime frame equal 509—one 32-bit word and 508 eight-bit words. The interleaving of the spacecraft and support equipment data is performed in various configruations due to the requirements at each site. The airborne data is always placed in word slot A; however, the ground service and carryon data can be either OR'ed together in any word slot remaining or can be placed in B or C or D, separately. In any configuration encountered, one and possibly two inputs to the interleaver can be always zero as shown in the following examples:

Example No. 1

A = Airborne telemetry

B = Carry-on telemetry

C = Ground service telemetry

D = Blank

Example No. 2

A = Airborne telemetry

B = Carry-on/ground service telemetry

C = Blank

D = Blank

In example No. 1, all prime frame data words of A, B, and C plus all words of the D input will be controlled by block counter zero. All other sub-commutated data in A, B, and C will be controlled by the applicable sub-commutator counters. In example No. 2, all prime frame data words in A and B plus all words of C and D will be controlled by block counter zero. All other sub-commutated data in A and B will be controlled by the applicable sub-commutator counters.

The recycling of the counters is performed in the same manner as explained in previous paragraphs pertaining to the A/B format.

#### 9.4 PROGRAMMING WITH SECOND ACCESS

In programming for second access, all PCM words to be sent to the computer via the direct access computer interface require a second access instruction word. All other words require only the normal control and routing word. This means that for an interleaved program, the programmed locations in the decommutator can become quite large. Also, keep in mind that the basic operation of the decommutator remains the same in that block zero must control all prime frame data words and all sub-commutated data by the existing sub-commutator counters and that the recycle codes must be

inserted at the end of the memory locations used by those counters. Thus, the subsequent discussion for second access programming is based purely upon the requirements for second access and upon the downlink computer requirements when using "ADAP"—Adaptive Intercommunications Program.

In programming for second access, the DACI control word, Figure 9-8C, is always placed in the next sequential location to the control and routing word that specified second access. For example, if in block one, memory location 11462 a control and routing word specified second access, the block counter would automatically sequence to the next location 11463. The decoding of the next block instruction obtained in location 11462 would be inhibited until after the initiation of the next memory cycle at location 11463 which contains the second access instruction word. Therefore, if a given block counter controls 150 PCM words and one-half require routing to the computer, the numbers of programmed locations for that counter would be 225.

ADAP places the requirement on the 540 decommutator to write telemetry information into the computer at rates less than the normal commutated rate. This applies only to prime frame data words and is termed as write-over at one-half sample rate. To perform this, all 50 sample-per-second words to be written over at one-half sample rate must be treated as sub-commutated data and controlled by some counter other than block zero and would result in transferring to the computer data equal to a 25 sample-per-second sub-commutator. If block counter one is used to sub-commutate the 50 sample-per-second data, this counter would be recycled at the end of every other frame and the data would be written in the 169G memory in two separate locations.

Block zero can be used to decommutate supercommutated data even if one-half sample rate is required. Data at 100 samples-per-second appears twice in each prime frame; therefore, when second access is made for the first sample in the frame a given 169G memory address is specified. This allows one-half sample rate writing by deviation of the programmed addresses in the second access words and maintains the control and routing programming the same as without second access.

All the unused word locations in each prime frame are decommutated with block counter zero and will have no specified second access. By decommutating all unused and unwanted word slots with block zero, memory locations can be saved and less programming requirements are placed on the sub-commutator counters. However, keep in mind when no second access is specified, only transfer to the computer for that

word is inhibited, and a requirement for routing to displays may be valid. If this situation exists in a sub-commutated block, the word must be programmed normally, and bit 18 of the control and routing word is maintained zero.

# 9.5 ID PROGRAMMING

When using second access instructions, the ID word must be transferred to the 169G memory to allow the computer to obtain frame identification after an end-of-frame interrupt. To perform this, the control and routing word must specify second access when accessed from memory in the word time prior to the ID. Therefore, during DACI operations and as long as the computer requires the ID word, the ID area will be 100 locations long, this break-out being 50 ID C&R words and 50 second access instruction words.

Additionally, when programming the second access word for the ID word the upper limit should be 63, the lower limit should be 001, and the event word bit (No. 40) should be one. This will allow zero tolerance and indicate to the computer that the ID is incrementing and/or has been recycled. This programming function is subject to change and is based upon the downlink computer program requirements.

#### SECTION 10

#### DIRECT ACCESS COMPUTER INTERFACE

# 10.1 INTRODUCTION

The direct access computer interface (DACI) logic allows the decommutator to perform three additional functions to those performed in the normal mode. First, to decommutate the data and directly assign a unique location for data storage in the 169G memory module (CDC 160G computer system). This is performed by the direct access to the external memory from the decommutator. Second, the decommutator will relieve the downlink computing system of the task of limit checking and will advise the downlink program on the validity of the incoming telemetry data. Third, the decommutator will prevent any unwanted or dummy data words from being transferred to the external memory.

The DACI does not modify the decommutation principle of the decommutator and does not affect the control and routing of data words to the decommutator distribution unit and event storage and distribution unit. The data is output from the most significant bit parallel register of the output rack. During the DACI configuration, the decommutator/computer interface will be used for the transfer of instructions from the computer to the decommutator, load decommutator programs, and to check decommutator programs. No PCM data transfer will be effected over this path when the direct access computer interface is active. The PCM data is transferred via the direct access computer interface (DACI) which, shown in Figure 10-1, connects directly to an external memory module of the downlink computer system.

With the direct access computer interface, the ACE-S/C decommutator has the capability to perform parameter limit checks, floating point checks, and event transition checks. The limit checks are performed on the upper and lower parameter values for each PCM word determined by the loaded decommutation program. The values for the upper and lower limits are predetermined and are preprogrammed into the decommutator memory prior to testing. Thus, the values provide unique checking for each telemetry word input into the system.

The floating point check is performed on those parameters where the change is of significance rather than the exact upper or lower values. In this capacity the last known

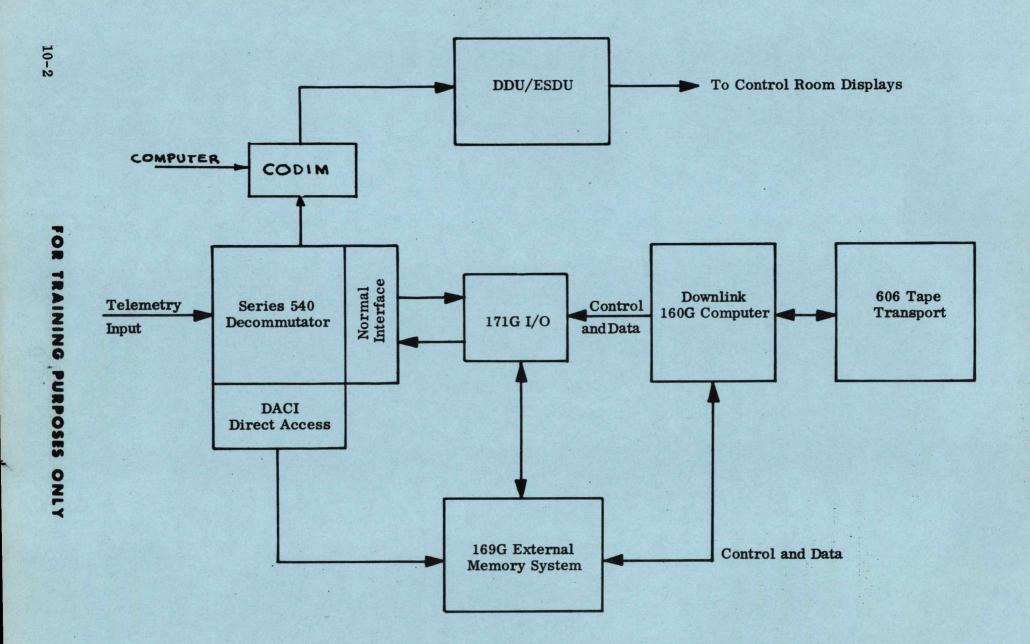


Figure 10-1. Interconnection Diagram

value of a parameter is used as the next point of reference, thus the floating point technique. The event transition checking is performed in the same manner as the floating point check in that the last unique event word input from the telemetry system is used as the next reference. This will define to the computer that an event change has occurred in a PCM word.

Although the decommutator performs check routines, the control over the gross routing of the decommutated data to the computer system is performed by defining the particular memory bank for any one block transfer.

# 10.2 FUNCTIONAL DESCRIPTION

#### 10.2.1 GENERAL

The direct access computer interface is virtually in parallel with the remainder of the decommutator as shown in Figure 10-2. The eight-bit data word out of the most significant bit parallel register is presented to the direct access computer interface, the decommutator distribution unit/event storage distribution unit, and the internal digital-to-analog converters simultaneously. Therefore, during the word time that the transfer is being made to the DDU/ESDU, the DACI must perform the checks on the word that is to be transferred to the computer. Thus, the transfer to the computer is made one word-time after the decommutation cycle has been completed.

If the incoming data is to be transferred to the computer, the normal control and routing word will enable the timing and control necessary to perform the checking and transfer of the data. A second access is made to memory to obtain the information necessary for checking and is located in the next memory location following the control and routing word. After the checks are made, the data and the status of the checking are made available to the computer external memory for storage in the location defined by the decom stored address. If the word in the process of being checked is an event word or a floating point word then the data from the MSB parallel register is transferred to the decommutator memory to be used as the updated reference when the word reappears in the PCM train. However, this transfer occurs only if a change is detected.

#### 10.2.2 INSTRUCTION WORD FORMATS

The decommutator control and routing word has been changed to identify the new modification in that bit 18 now designates the operation of the DACI (See Section 9). This bit

Figure 10-2. DACI/Decommutator Interface

position was previously used for an on/off dump signal. The coding of the DACI control bit is as follows:

**BIT 18** 

- Do nothing related to the computer; e.g., do not energize the DACI operation thereby inhibiting transfer to the computer external memory.
- 1 Enable the DACI and set the flag to the computer after the fixed and/or floating checks have been performed.

The second instruction word format, the DACI control word defines the preprogrammed parameters for performing the fixed and floating limit checks and the event transition checks. Bits 2 to 9 define the fixed upper limit of the parameter. If the programmed parameter upper value is summed to equal a binary 64 (01000000) and the data summed to equal 64 or less, the parameter is defined as within the upper limits. The same example holds true for the lower limit values bits 10 to 17; however, as an example, the sum of the fixed limit could equal a binary 10. Therefore, as long as the input parameter ranges from a binary 10 to a binary 64, the computer continually receives a flag indicating valid data, and no computer processing is initiated. Bits 31 to 38 define the last known out-of-tolerance data for a parameter floating limit check. This check is performed on all input data and incorporates a 6-bit tolerance preprogrammed into the preacquisition block. The tolerance is a function of data processing and will probably vary with different spacecraft testing operations. The floating limit check is performed to determine if the present parameter point has deviated from the previous like point by an amount more than defined by the allowable tolerance. If the floating point check is found to be within limits, the previous parameter information remains in memory bits 31 to 38; however, if the check is found to be out of the tolerance defined, the new parameter data will be stored in memory and used as the updated information when the like parameter recurs in the PCM train.

Bits 18 to 30 of the DACI control word contain the 13-bit address needed to define a unique location in a computer external 8192 memory bank. The particular memory bank being defined by the computer previously transferred to the decommutator. Bit 39 of the DACI control word defines which fixed limit checks are to be flagged. For example, if the bit defines upper limit check and if the parameter exceeds the upper limit an out-of-tolerance condition will be indicated and if the parameter exceeds the lower limit no flag is set. Bit 40 is used in event transition checking and causes the floating

tolerance to go to an all zero condition. This takes place each time an event word occurs in the PCM stream because the floating check logic is used to detect if there is a change from the last event word stored in memory.

#### 10.2.3 COMPUTER WORD FORMATS

Two 13-bit words are transferred to the computer external memory for each PCM data word decommutated and destined for transfer. One word is the 13-bit address from the DACI control word. A second word is made up from the telemetry data and the resultant of the checks made by the DACI logical functions (Figure 10-3). Bits 0 to 7 of the word contain the decommutated data, bits 8 and 9 are unassigned and remain a logical zero, bit 10 is the fixed limit high-low flag and is set to a logical one when the data word exceeds either the upper or lower limits defined by the DACI control word. This flag is controlled by bit 39 of the DACI control word which defines that the data should be limit checked for high or low limits. Bit 11 is the fixed limit check flag and is set to a logical one when the data word failed the fixed limit check. Bit 12 is the floating limit check flag and is set to a logical one when the data point.

# 10.2.4 FLOATING POINT TOLERANCE CHECK TECHNIQUE

The floating point tolerance check produces indirectly for the computer a deviation ratio from the parameter mean value, which in a sense establishes a trend for any given parameter of analog origin. The input PCM data can deviate in a binary configuration from 0 to 255 regardless of the parameter being sampled. As an example if a power supply of -28 volts dc is sampled by the telemetry system, the decimal equivalent of the binary word is 128 (maximum of 255) and to define a 150 psi pressure the decimal equivalent is also 128. Therefore, the tolerance value is a percentage of the parameter decimal equivalent and not of the parameter engineering units value. This explains the reason why the tolerance value can be set up during the preacquisition mode for any particular program. If, for example, the tolerance value programmed is 5 percent, then any PCM word deviating above or below the last known point an amount greater than 5 percent of the decimal equivalent of the parameter, the floating point check logic sets the out-of-tolerance flag. The deviation ratio previously mentioned for any given parameter is directly proportional to the sample rate of that parameter; e.g., if a parameter is sampled by the telemetry system at 100 samples per second, then the largest rate of change possible for the parameter is 100. Using, for example, the 150 psi pressure, the following limitations are given:

- a. Same rate of 100 per second.
- b. 150 psi pressure results in a PCM word decimal equivalent of 128.

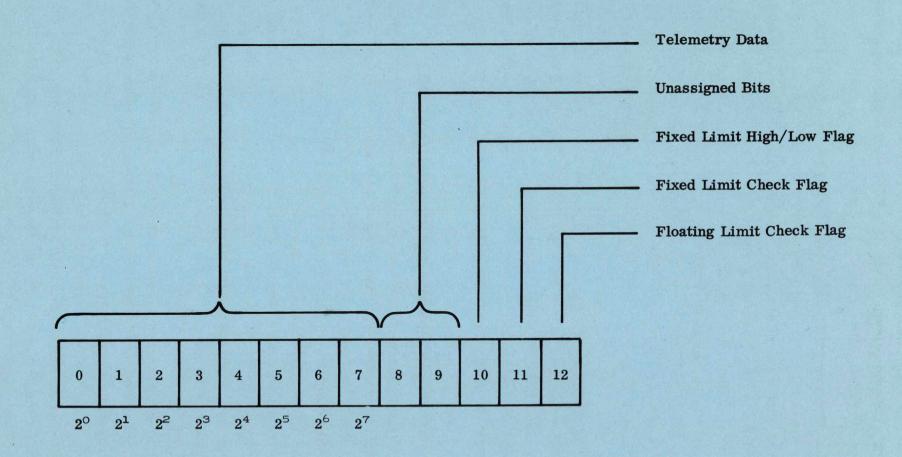


Figure 10-3. Computer Word Format

- c. 160 psi pressure results in a PCM word decimal equivalent of 255.
- d. 140 psi pressure results in a PCM word decimal equivalent of zero.

If the assumption is made that the first input sample is a decimal 128, then this value is used as the last floating point reference. If the next input is 5 percent greater than decimal 128, then the floating point check logic will indicate an out-of-tolerance condition and the new data is used as the next point of reference, thus 5 percent from the last known out-of-tolerance condition and not the mean. Based on the previous limitations and discussion, the graph in Figure 10-4 would occur if the deviation of 150 psi changed to 158 psi at a linear rate over a one second period. In the example taken, the first change of 5 percent from the mean would not be detected by the floating point logic because the value is only 6.4 decimal. Since the least two significant bits are not used in the example, no change would take place. This situation occurs quite often during the change of the pressure. Figuring the linearity in percentages, the memory bits 31 to 38 would be changed to a new value six times in one second and would reach the new value of decimal 228 during the next time period. Therefore, as shown by Figure 10-4, the floating point logic would indicate one out-of-tolerance condition approximately once every 16 samples of the parameter.

# 10.2.5 SEQUENCE OF OPERATION

The direct access computer interface operates essentially as a computer peripheral in that a computer instruction code of 3 X 6 X is used to enable the logic. The 160G downlink computer transfers the input instruction of 3 X 6 X via the 171G.3 I/O module to the existing decommutator/computer interface. The 3 X portion of the instruction enables the decommutator, the 6 enables the DACI and the least significant octave X defines the computer system memory bank. Therefore, the new codes can be 3 X 62, 3 X 64 or 3 X 66 and will be banks 2, 4, and 6, respectively. An additional instruction of 3 X 70 is used as a DACI master clear and has no effect on any other decommutator logic operations. The decom master clear of 3 X 20 also clears the DACI.

The instruction for program selection, the DACI instruction of 3 X 6 X, and the enable from preacquisition sequence 30 allow the 540 decommutator to perform the sequence of operations defined in subsequent paragraphs.

The normal decommutator control and routing word obtained from memory defines the instruction for the next block counter, the word length, the D/A address, the display

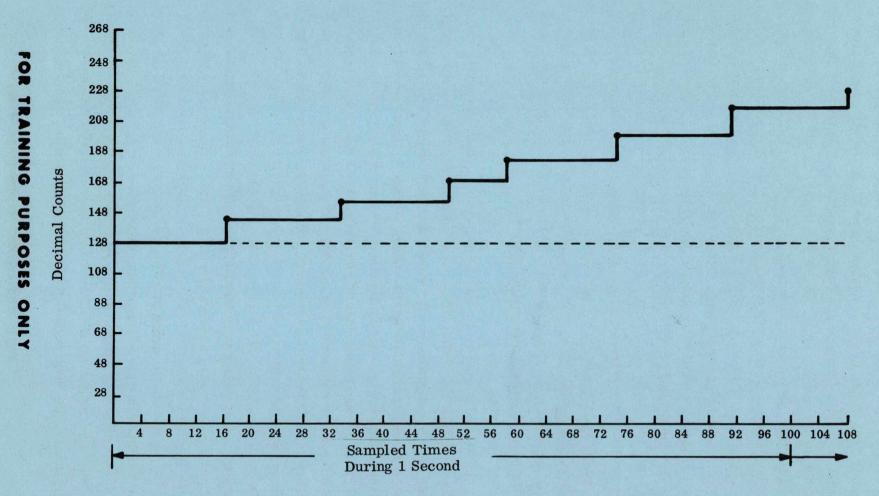


Figure 10-4. Deviation of psi Versus Time

routing, etc. This access to memory is made one word-time prior to the word to be decormutated and formatted. The information contained in bit time 18 of the normal C&R word defines if any processing should be performed prior to transfer of data to the computer. If the information contained in bit 18 defines no processing for the data transferred to the computer, the decommutator will operate in the normal manner and sequence to another memory location for the next control and routing word. However, if bit 18 defines processing, a second access must be made to memory to obtain the information necessary for the upper and lower limit checks and the floating point check. The decommutator memory will be stepped to the next sequential memory location of the block counter that accesses memory for the control and routing word. This access occurs at the next word rate pulse, e.g., the first word rate pulse after the one that generated the memory cycle to obtain the control and routing word. The second access or the direct access computer interface (DACI) instruction word is strobed into data register No. 1 (see Figure 10-5). The contents of the particular block counter that addressed memory will be strobed into address register No. 1 via the memory address register. This memory location is maintained until the floating point check is performed because if the check fails the memory must again be accessed so the new floating point data can be stored in memory.

After the second word rate pulse has passed, the DACI instruction word and the specific memory address are contained in the second access <u>data</u> register No. 1 and the second access <u>address</u> register No. 1. This transfer from memory occurred at the beginning bit time of the data word being formatted into the MSB parallel register. Since the DACI instruction word was obtained by the normal word rate pulse an extra or simulated memory read pulse must be generated to enable the next block counter and a memory cycle to obtain the next control and routing word. It may be noted here that the C&R word must be out of memory and loaded into all applicable registers before the first bit of the next word.

Therefore, in summary to this point, two memory cycles must be made for each data word processed and transferred to the computer and one memory cycle if no processing is to be performed.

During the time memory is being strobed for the next control and routing word by the simulated memory read pulse, the data is being formatted into the MSB parallel register. The next word rate pulse from the group synchronizer causes the formatted MSB parallel data to be transferred to the MSB parallel output register (Figure 10-5)

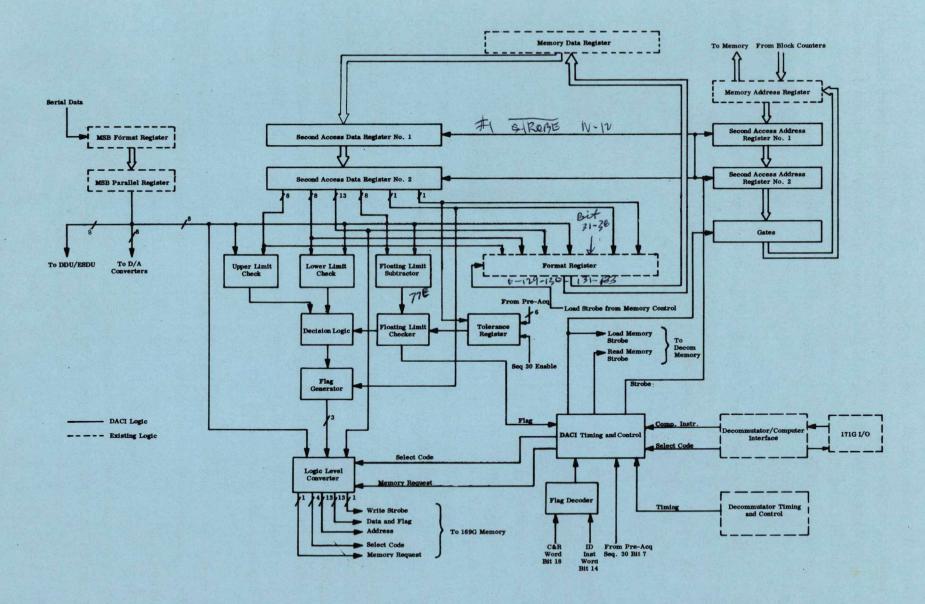


Figure 10-5. Direct Access Computer Interface

and the DACI instruction word to be transferred to data register No. 2. To maintain the sequence of operation, the memory address is transferred to address register No. 2. At this time the MSB parallel data is made available to upper limit check logic, the lower limit check logic, the floating point limit check logic, and the format register. It is also made available to the interface logic level converters; however, no transfer is made at this precise moment.

After the limit checks are performed, the decision logic will define if the incoming PCM data was out of tolerance defined by the DACI control word or if an event transition occurred, if the word was of discrete origin. The flag generator (Figure 10-5) will generate a 3-bit code to define for the downlink computer the status of the check made on the data.

If the data was floating point checked and found to be out of tolerance defined by the preacquisition information, the new data must be loaded into memory for the next floating point check. Thus, the DACI timing and control generates a load memory strobe which transfers the DACI contents from the second access data register No. 2 into the format register. On a continuation of the timing pulse, the contents of the second access address register is used to obtain the memory location where original access was made for the DACI instruction word. This loading of memory must be performed prior to the next word rate pulse generated by the group synchronizer.

The 160G downlink computer via the existing decommutator/computer interface transfers to the DACI the specific memory bank address where loading is to commence. This bank address only defines a 169G external memory. The specific address within the 8192 x 14 word memory is obtained from bits 18 through 30 of the DACI instruction word. This bank address remains a constant until changed by the downlink program and can be modified to select banks 2, 4, or 6.

The select code from the interface level converters defines the memory bank and the address defines the specific memory location. The data word contains the 3-bit code from the flag generator and the 8 bits of MSB parallel data. The write signal is generated by DACI timing and control to define to the 169G external memory the type of operation that is to be performed after memory has been selected. The memory request is the last signal generated by the DACI timing and control and is used by the 169G to initiate a memory cycle to store the 13-bit data word.

Figure 10-6 is a timing diagram showing the time relationships of decommutator memory cycles, PCM words, and transfers to the 169G memory. As obtained from Figure 10-6 the series 540 PCM decommutator is restricted from high bit rates/short word lengths due to the number of memory references that must be made during the worst case operation. This is when access must be made to memory to load new floating point data for future checks. Therefore, the system must have available three memory cycles for each word transferred to the 169G memory which constitutes a total of 18 microseconds. When a third access is made to memory to load new floating point data, the parity checker cannot be used because no provision has been made to change the state of the LSB of the memory word. For all other words placed in memory, the parity bit is operational.

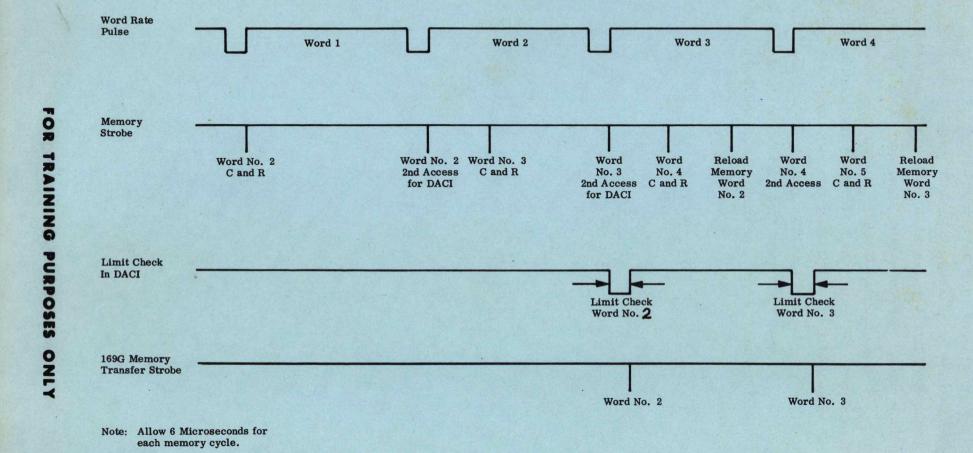


Figure 10-6. Direct Access Computer Interface Timing Diagram

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