

GENERAL  ELECTRIC

APOLLO
SUPPORT
DEPARTMENT

ACE—S/C
DESCRIPTION
MANUAL

ACCEPTANCE CHECKOUT EQUIPMENT—SPACECRAFT
SYSTEM NO. 1 INSTALLED AT NORTH AMERICAN AVIATION—DOWNEY, CALIF.

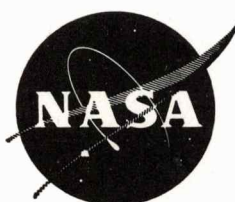
JOHN A. WISHARD

NASw-410-AM-13

DESCRIPTION MANUAL
for
ACCEPTANCE CHECKOUT
EQUIPMENT-SPACECRAFT

GROUND STATION No. 1
INSTALLED AT NORTH AMERICAN AVIATION
DOWNEY, CALIFORNIA

1 JUNE 1964



This document was prepared for the National Aeronautics and Space Administration/Apollo Spacecraft Program Office under Contract NASw-410 Task Order MSC/POD-1. Preparation of this Type II document is required by paragraph 10.3 of Exhibit D to the existing contractual requirements.

APOLLO SUPPORT DEPARTMENT
GENERAL ELECTRIC COMPANY
DAYTONA BEACH, FLORIDA

John A. W. W. W. W.

Insert Latest Changed Pages. Destroy Superseded Pages.

LIST OF EFFECTIVE PAGES

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 417 CONSISTING OF THE FOLLOWING:

Page No.	Issue
Title	Original
A	Original
i thru xii	Original
1-0 thru 1-0	Original
1-1 thru 1-32	Original
2-1 thru 2-92	Original
3-1 thru 3-190 ...	Original
4-1 thru 4-88	Original

*The asterisk indicates pages changed, added, or deleted by the current change

NASA

Manuals will be distributed as directed by the NASA-Apollo Program Office. All requests for manuals should be directed to the NASA Apollo Spacecraft Program Office at Houston, Texas.

TABLE OF CONTENTS

ParagraphPage

INTRODUCTION

SECTION I. GENERAL DESCRIPTION

PART 1	FUNCTIONAL DESCRIPTION	1-1
1-1	Acceptance Checkout Equipment - Spacecraft System Description . . .	1-1
1-5	Command Equipment	1-1
1-12	Data Recording and Display Equipment	1-5
1-18	Support Systems	1-6
1-22	Command Equipment Description	1-6
1-24	R START Module	1-6
1-26	C START Module	1-9
1-28	K START Module	1-9
1-30	Communications Unit Executor	1-9
1-33	Command Computer	1-10
1-37	Data Transmission and Verification Converter	1-10
1-42	Receiver-Decoder	1-11
1-51	Recording and Display Equipment Description	1-12
1-53	Spacecraft and Spacecraft Vicinity Equipment	1-12
1-60	Data Acquisition and Decommuration Equipment (DADE).	1-13
1-64	Alphanumeric Display System	1-14
1-74	Analog and Event Display System	1-15
1-83	Quick Reference Table of Major Unit Functions	1-17
PART 2	PHYSICAL DESCRIPTION	1-22
1-85	ACE-S/C Station Physical Configuration at Downey, California	1-22
1-90	Control Room Equipment	1-22
1-93	Computer Room Equipment	1-23
1-99	Terminal Facility Room Equipment	1-23

SECTION II. COMMAND EQUIPMENT

2-1	Data Entry Equipment	2-1
2-3	Interrupt Mode	2-1
2-12	Manual Mode	2-5
2-14	Maintenance Mode	2-5
2-16	R START Functions	2-5
2-18	R START Operation	2-5
2-20	C START Functions	2-6
2-22	C START Operation	2-6

TABLE OF CONTENTS (Cont'd)

<u>Paragraph</u>		<u>Page</u>
2-24	K START Functions	2-7
2-26	Tape Mode	2-7
2-29	Manual Mode	2-7
2-31	Keyboard	2-8
2-33	K START Operation	2-8
2-35	J-Box Functions	2-15
2-37	CUE Functions	2-15
2-39	Standby Mode	2-15
2-41	Interrupt Mode	2-15
2-54	Maintenance Mode	2-21
2-58	Manual Mode	2-21
2-62	CUE Description	2-22
2-64	Standby Mode	2-22
2-66	Interrupt Mode	2-22
2-79	Maintenance Mode	2-25
2-81	Manual Mode	2-25
2-83	Data Processing Equipment	2-26
2-86	Nonpriority Operation	2-26
2-90	Priority Operation	2-27
2-120	Computer Complex Functions	2-37
2-124	Computer Complex Description	2-37
2-125	Compute Module	2-37
2-149	Memory Module	2-45
2-160	Input/Output Module	2-47
2-183	Line Printer	2-55
2-193	Card Reader	2-58
2-206	Magnetic Tape Transport Units	2-64
2-236	Tape Control Unit	2-71
2-248	Card Punch Controller and Card Punch	2-74
2-256	X-Y Plotter	2-77
2-262	Typewriter	2-79
2-267	Data Transmission Equipment	2-80
2-269	Transmission	2-83
2-271	Reception	2-83
2-273	Status Response	2-83
2-276	Function Words	2-83
2-278	Receiver Interrupt	2-84
2-280	Interrupt on Error	2-84
2-282	Interrupt on Fake Ready	2-84
2-284	Data Transmission and Verification Converter Functions	2-84
2-286	Transmit Mode	2-84
2-288	Receive Mode	2-85
2-290	Transmit Cycle	2-85
2-296	Receive Cycle	2-89
2-302	Program Control	2-90

TABLE OF CONTENTS (Cont'd)

ParagraphPage

SECTION III. DISPLAY AND RECORDING EQUIPMENT

3-1	Introduction	3-1
PART 1	DATA ACQUISITION AND DECOMMUTATION EQUIPMENT.	3-1
3-3	Data Acquisition and Decommutation Equipment Functions	3-1
3-10	Interleaved PCM Test Data Description	3-2
3-15	Airborne PCM Test Data Description	3-5
3-18	Frequency Modulated Test Data Description	3-6
3-20	Video Distribution and Tape Transport Control Unit	3-6
3-21	Video Distribution and Tape Transport Control Functions	3-6
3-24	Video Distribution and Tape Transport Control Unit Description	3-10
3-27	Magnetic Tape Recorder Units.	3-12
3-28	Magnetic Tape Recorder Functions	3-12
3-41	Magnetic Tape Recorder Description	3-18
3-63	Tape Search Control Unit	3-29
3-64	Tape Search Control Functions	3-29
3-78	Tape Search Control Description	3-32
3-79	Signal Mixer Assembly	3-32
3-80	Signal Mixer Functions	3-32
3-85	Signal Mixer Description	3-34
3-92	Reference Oscillator/Mixer Assembly	3-36
3-93	Reference Oscillator/Mixer Functions	3-36
3-95	Reference Oscillator Description	3-38
3-102	Mixer Amplifier Description	3-40
3-103	Signal Separator Assembly	3-40
3-104	Signal Separator Functions	3-40
3-108	Signal Separator Description	3-40
3-115	FM Discriminator Unit	3-43
3-116	FM Discriminator Functions	3-43
3-120	FM Discriminator Description	3-44
3-150	FM Calibration Unit	3-53
3-151	FM Calibration Unit Functions	3-53
3-153	FM Telemetry Indicator Description	3-53
3-166	FM Telemetry Calibrator Description.	3-54
3-175	Frequency Counter Description.	3-57
3-176	Decommutator Unit.	3-58
3-177	Decommutator Unit Functions	3-58
3-189	Decommutator Unit Description	3-69
PART 2	ANALOG AND EVENT DISPLAY EQUIPMENT.	3-96
3-253	Control Room Test Data Display and Recording Equipment Functions	3-96
3-256	Decommutator Distribution Unit	3-96

TABLE OF CONTENTS (Cont'd)

<u>Paragraph</u>		<u>Page</u>
3-257	Decommutator Distribution Unit Functions.	3-96
3-263	Decom Distribution Unit Description	3-101
3-269	Event Storage and Distribution Unit	3-102
3-270	Event Storage and Distribution Unit Functions	3-102
3-282	Event Storage and Distribution Unit Description	3-108
3-298	Control Consoles	3-121
3-299	Control Console Functions	3-121
3-318	Control Console Circuit Descriptions	3-129
3-334	Eight-Channel Analog Recorder Description	3-137
3-338	32-Channel Event Recorder Description	3-137
3-342	100-Channel Event Recorder Description	3-137
3-345	Computer Room Test Data Display and Recording Equipment	3-140
3-348	Event Distribution Recording and Patching Unit	3-140
3-350	Event Processing Logic Description	3-142
3-352	Patchboard Description	3-142
3-354	100-Channel Event Recorder Description	3-142
3-356	Analog Recorder Unit.	3-142
3-357	8-Channel Analog Recorder Description	3-142
3-359	36-Channel Oscillographic Recorder Description	3-142
3-369	Computer Room Meter and Event Modules	3-145
3-370	Meter Module Description	3-145
3-372	Event Module Description	3-146
PART 3	ALPHANUMERIC DISPLAY EQUIPMENT.	3-146
3-374	Alphanumeric Display Equipment Functions	3-146
3-378	Data Processing Functions.	3-149
3-401	Data Transmission Functions	3-157
3-413	Symbol Generation and Display Functions	3-163
3-415	DTVC and DCCU Equipment Description	3-164
3-416	DTVC Description	3-164
3-418	DCCU Description	3-164
3-420	Control Unit Adapter Description	3-164
3-421	SGS and CRT Equipment Description	3-164
3-435	Display Control	3-168
3-437	Main Timing and Control	3-169
3-439	Resynchronization Circuits	3-169
3-447	Memory Lockout	3-170
3-449	Input Register	3-170
3-452	Input Gates	3-170
3-454	Input To Z Control	3-173
3-456	Write-Over Period	3-173
3-459	Memory Timing and Control	3-173
3-462	Control Circuits	3-173
3-464	Control Sequence	3-176

TABLE OF CONTENTS (Cont'd)

<u>Paragraph</u>		<u>Page</u>
3-467	Address Selection.	3-176
3-472	Memory Circuits	3-179
3-474	Beam Positioning.	3-179
3-480	Deflection	3-181
3-484	Character Generation	3-181
3-486	Primary Translation	3-181
3-491	Character Timing.	3-184
3-493	Translator Timing	3-186
3-495	Secondary Translation.	3-186
3-497	Character Positioning.	3-186
3-501	Unblanking.	3-186
3-504	CRT Module	3-187
3-507	Deflection Preamplifier	3-187
3-509	Deflection Amplifier	3-187
3-511	Focus and Astigmatism	3-187
3-515	Cathode Ray Tube.	3-189
3-517	Deflection	3-189

SECTION IV. SUPPORT EQUIPMENT

4-1	Introduction	4-1
4-3	Timing Equipment	4-1
4-8	Time Signal Distribution.	4-2
4-20	Time Code Generator.	4-17
4-23	Time Code Generator Functions	4-17
4-36	Time Code Generator Description	4-21
4-107	Countdown Time Code Generator.	4-35
4-109	Countdown Time Code Generator Functions	4-35
4-116	Countdown Time Code Generator Description	4-36
4-153	Tape Search/Time Code Translator/Computer I/O Synchronizer	4-49
4-155	Tape Search/Time Code Translator/Computer I/O Synchronizer Functions.	4-49
4-169	Tape Search/Time Code Translator/Computer I/O Synchronizer Description	4-55
4-269	Countdown Time Code Translator and Computer Input/Output Synchronizer	4-73
4-270	Countdown Time Code Translator and Computer Input/Output Synchronizer Functions.	4-73
4-272	Countdown Time Code Translator and Computer Input/Output Synchronizer Description	4-73
4-298	Time Code Distribution Unit.	4-78
4-302	Decommutator Distribution Unit	4-79

TABLE OF CONTENTS (Cont'd)

<u>Paragraph</u>		<u>Page</u>
4-304	Remote Time Display Units	4-79
4-306	Wall Clock Display Functions	4-79
4-310	Countdown Generator Remote Control Unit Functions	4-82
4-312	Remote Time Display Unit Description	4-82
4-317	Status Monitoring and Display Equipment	4-83
4-319	Control Console Status Control Panel Functions	4-87
4-324	Decommutator Distribution Unit Status Distribution Functions	4-87
4-327	Test Conductor Console Status Subassembly Functions	4-88

LIST OF ILLUSTRATIONS

FigurePage

SECTION I. GENERAL DESCRIPTION

1-1	ACE-S/C Equipment Simplified Block Diagram	1-3
1-2	ACE-S/C Equipment Block Diagram	1-7
1-3	First Floor Plan of NAA Building 290	1-25
1-4	Second Floor Plan of NAA Building 290	1-26
1-5	NAA Control Room Perspective View	1-27
1-6	NAA Computer Room Perspective View	1-29
1-7	NAA Terminal Facility Room Perspective View	1-31

SECTION II. COMMAND EQUIPMENT

2-1	Command Equipment Block Diagram	2-3
2-2	R START Module Block Diagram	2-9
2-3	C START Module Block Diagram	2-11
2-4	K START Module Block Diagram	2-13
2-5	J-Box Block Diagram	2-16
2-6	Communications Unit Executor Block Diagram	2-17
2-7	Command Equipment Functional Block Diagram	2-29
2-8	Computer Complex Block Diagram	2-39
2-9	Compute Module Simplified Block Diagram	2-41
2-10	Memory Module Simplified Block Diagram	2-49
2-11	Input/Output Module Block Diagram	2-51
2-12	Line Printer Simplified Block Diagram	2-59
2-13	Card Reader Logic Block Diagram	2-61
2-14	Tape Motion Simplified Diagram	2-65
2-15	Tape Transport Logic Block Diagram	2-67
2-16	Tape Control Unit Logic Block Diagram	2-72
2-17	Card Punch Controller Logic Block Diagram	2-75
2-18	X-Y Plotter Simplified Block Diagram	2-78
2-19	X-Y Plotter Motion Coordinates	2-79
2-20	Typewriter Logic Block Diagram	2-81
2-21	Data Transmission and Verification Converter Block Diagram	2-87
2-22	Data Transmission and Verification Converter Operational Flow Chart	2-92

LIST OF ILLUSTRATIONS (Cont'd)

FigurePage

SECTION III. DISPLAY AND RECORDING EQUIPMENT

3-1	Data Acquisition and Decommuration Equipment Functional Block Diagram	3-3
3-2	Typical Interleaved Prime Frame Composition and Word Location. . .	3-7
3-3	Typical Airborne Prime Frame Composition and Word Location. . . .	3-9
3-4	Video Distribution and Tape Transport Control Unit Functional Block Diagram	3-11
3-5	Patch Panel Layout and Signal Identification.	3-13
3-6	Magnetic Tape Recorder Input/Output Functional Block Diagram . . .	3-15
3-7	Search Control Functional Block Diagram.	3-19
3-8	Sequential Operation Functional Block Diagram	3-21
3-9	Status Indication Functional Block Diagram.	3-23
3-10	Wideband Analog Tape Transport	3-26
3-11	Direct Record Circuit Block Diagram	3-29
3-12	Direct Reproduce Circuit Block Diagram	3-30
3-13	Signal Mixer Functional Block Diagram.	3-33
3-14	Signal Mixer Simplified Block Diagram.	3-35
3-15	Reference Mixer/Oscillator Functional Block Diagram.	3-37
3-16	Reference Oscillator Simplified Block Diagram	3-39
3-17	Signal Separator Functional Block Diagram	3-41
3-18	FM Subcarrier Discriminator Block Diagram	3-45
3-19	FM Subcarrier Discriminator Idealized Waveforms	3-49
3-20	Idealized Waveforms, FM Subcarrier Discriminator Loss-of-Lock Circuit	3-52
3-21	FM Telemetry Indicator Simplified Block Diagram.	3-55
3-22	Telemetry Calibrator Block Diagram	3-59
3-23	Switching Module Block Diagram	3-61
3-24	Decommutator/Computer Connections	3-63
3-25	Digital Acquisition and Decommuration System Block Diagram	3-70
3-26	Signal Conditioner Block Diagram	3-72
3-27	Memory Organization and Coding	3-73
3-28	Stored Program Processor Simplified Block Diagram	3-75
3-29	Memory Word Program Control and Routing Instruction Format. . . .	3-77
3-30	BCD and Binary Display Simplified Block Diagram	3-80
3-31	Digital-to-Analog Conversion Simplified Block Diagram	3-81
3-32	Binary-to-BCD Converter Simplified Block Diagram.	3-83
3-33	MSB and LSB Parallel Registers Simplified Block Diagram.	3-84
3-34	MSB and LSB Truncated Character Formation Simplified Block Diagram	3-88
3-35	Binary Storage Registers Simplified Block Diagram	3-91
3-36	PCM Signal Simulator Simplified Block Diagram.	3-93
3-37	Decommutator/Computer Interface Simplified Block Diagram.	3-95

LIST OF ILLUSTRATIONS (Cont'd)

<u>Figure</u>		<u>Page</u>
3-38	Control Room Test Data Display and Recording Equipment Block Diagram	3-97
3-39	DDU Functional Block Diagram	3-100
3-40	Typical DDU Circuit	3-103
3-41	ESDU Block Diagram	3-105
3-42	Typical Address Distribution Amplifier	3-110
3-43	Typical Address Decoding Circuit	3-111
3-44	Typical Data and Read-Pulse Selection Circuit.	3-115
3-45	Typical Address and Read-Pulse Gate	3-117
3-46	Typical Set-Pulse and Trigger-Generator Circuit	3-118
3-47	Typical Storage Register Circuit.	3-119
3-48	Typical Control Console Block Diagram	3-123
3-49	Typical 2 to 1 Address Selection Circuit	3-130
3-50	Typical D/A Converter Circuit	3-132
3-51	Typical Lamp Driver and Indicator Circuit	3-133
3-52	Typical Meter Circuit	3-134
3-53	Typical Event Lamp Indicator Circuit	3-135
3-54	Typical Converter Circuit.	3-136
3-55	Eight-Channel Analog Recorder Functional Block Diagram	3-138
3-56	32-Channel Event Recorder Functional Block Diagram	3-139
3-57	100-Channel Event Recorder Functional Block Diagram	3-140
3-58	Computer Room Test Display and Recording Units Functional Block Diagram	3-141
3-59	36-Channel Oscillographic Recorder Block Diagram	3-143
3-60	Alphanumeric Display Units Functional Block Diagram.	3-147
3-61	PCM Data Read-In Functional Block Diagram	3-153
3-62	DTVC/DCCU Transmission Link Functional Block Diagram.	3-159
3-63	Symbol Generator Storage Unit Functional Block Diagram	3-165
3-64	Display System Timing Block Diagram	3-169
3-65	Input Data Control Functions Flow Chart	3-171
3-66	Input Gating and Input To Z Control Block Diagram	3-174
3-67	Memory Timing Diagram	3-175
3-68	Memory Section Simplified Logic Diagram.	3-177
3-69	Typical D/A Conversion Block Diagram	3-180
3-70	SGS Deflection System Block Diagram	3-182
3-71	Diagram of Character Generator Functions	3-183
3-72	Character Matrix and CRT Raster	3-184
3-73	Diagram of Typical Character Formation.	3-185
3-74	SGS Unblank System Block Diagram	3-187
3-75	Monitor Functional Block Diagram	3-188

LIST OF ILLUSTRATIONS (Cont'd)

FigurePage

SECTION IV. SUPPORT EQUIPMENT

4-1	IRIG B Real Time Distribution Block Diagram.	4-5
4-2	IRIG B Playback Time Distribution Block Diagram.	4-7
4-3	AMR B-1 Real Time Distribution Block Diagram	4-9
4-4	AMR B-1 Playback Time Distribution Block Diagram	4-11
4-5	Countdown Time Distribution Block Diagram	4-13
4-6	Playback Countdown Time Distribution Block Diagram	4-15
4-7	Time Code Generator Functional Block Diagram.	4-19
4-8	System Clock Circuits Functional Block Diagram	4-23
4-9	Major and Minor Counter Timing Diagram	4-27
4-10	IRIG B Time Code Format	4-31
4-11	Display Converter Coding.	4-37
4-12	Countdown Time Code Generator Simplified Block Diagram.	4-38
4-13	Minor and Major Counters Block Diagram	4-41
4-14	ACE-S/C Countdown Time Code Format	4-43
4-15	Word Generator and Local and Remote Display Circuit Block Diagram	4-45
4-16	Tape Search and Time Code Translator Simplified Block Diagram. . .	4-52
4-17	Time Code Translator Functional Block Diagram	4-53
4-18	Input Circuits Functional Block Diagram	4-56
4-19	Tape Search Control Functional Block Diagram	4-59
4-20	Tape Search Sequence	4-64
4-21	Input/Output Synchronizer Block Diagram.	4-65
4-22	Range Time Word Formats	4-67
4-23	Time Code Distribution Unit Functional Block Diagram.	4-80
4-24	Distribution of AMR B-1 Time Codes by the DDU	4-81
4-25	Remote Time Display Indicator Mask Formats	4-83
4-26	Display Converter Coding.	4-84
4-27	Status Control and Monitoring System Functional Block Diagram . . .	4-85

LIST OF TABLES

<u>Table</u>		<u>Page</u>
SECTION I. GENERAL DESCRIPTION		
1-1	Quick Reference Table of Major Unit Functions	1-17
SECTION II. COMMAND EQUIPMENT		
2-1	External Function Instructions.	2-19
2-2	Status Response Codes	2-19
SECTION III. DISPLAY AND RECORDING EQUIPMENT		
3-1	FM Channel Frequency Assignments	3-6
3-2	Decommutator to Computer Information Transfer Sequence.	3-64
3-3	Computer to Decommutator Information Transfer Sequence.	3-65
3-4	Decommutator Status Word Bit Weight and Assignment.	3-66
3-5	Computer Function Control Words to Decommutator Units	3-67
3-6	Steps in Forming Truncated Characters	3-89
3-7	Event Distribution	3-109
3-8	Control Console Component Complement	3-125
3-9	Display Computer Output Word Content.	3-156
3-10	External Function Codes Received by DCCU.	3-161
3-11	DCCU Status Reply Code	3-163

INTRODUCTION

This manual provides a complete functional and physical description of Acceptance Checkout Equipment - Spacecraft (ACE-S/C) Ground Station No. 1, installed at North American Aviation Company (NAA), Downey, California. The manual is divided into four sections:

Section I - General Description - This section contains a general functional description of the entire ground station, indicating equipment/station and station/facility relationships. In addition, a detailed physical description of the ACE-S/C installation at NAA is provided to show equipment location and site layout.

Section II - Command Equipment - This section contains a detailed functional description of the Command Equipment portion of the ground station.

Section III - Recording and Display Equipment - This section provides a detailed functional description of the Recording and Display Equipment portion of the ground station.

Section IV - Support Equipment - The Support Equipment category includes units that are not a direct part of the major system functions but are necessary for spacecraft test operations.

SECTION I

GENERAL DESCRIPTION

PART 1

FUNCTIONAL DESCRIPTION

1-1. ACCEPTANCE CHECKOUT EQUIPMENT - SPACECRAFT SYSTEM DESCRIPTION.

1-2. The Acceptance Checkout Equipment - Spacecraft (ACE-S/C) is an advanced, integrated checkout system that provides centralized, programmed control of spacecraft checkout operations. Both independent spacecraft systems testing and integrated system testing are possible. Large quantities of test data can be processed and displayed in real-time, as well as recorded for later analysis, with a relatively small staff of engineering personnel.

1-3. Specifically, the ACE-S/C station performs the following functions:

- a. Provides the operator controls and data processing facilities necessary to control spacecraft test stimuli equipment.
- b. Receives, processes, displays, and records spacecraft parameter data derived from the spacecraft ground and flight telemetry systems.
- c. Provides self-check and calibration capability for itself and related equipment.

1-4. The ground station may be divided into two functional data-chain groupings: the Command Equipment and the Data Recording and Display Equipment. (see figure 1-1.) The Command Equipment is comprised of those units that form the communication path over which all test commands and sequences (in digital word form) are generated and transmitted to the spacecraft. Verification of receipt of these commands is transmitted from the spacecraft test area, back through the command system, to the ACE-S/C station. Test result data from the spacecraft test area is received (again in digital word form) by the Data Recording and Display Equipment which presents these data for evaluation.

1-5. COMMAND EQUIPMENT.

1-6. Test commands are initiated at various system control consoles by setting switches on units called Selection-To-Activate-Random-Testing (START) modules. The setting of these

switches provides digital command inputs to the command computer. These commands vary from individual event functions (specific relay on-off actions) to the callup of computer sub-routines that control sequences of events and/or various analog operations in the spacecraft.

1-7. The testing of each functional spacecraft system is controlled from an associated system control console. The following functional systems are tested:

- a. Environmental Control System.
- b. Fuel Cell and Cryogenics.
- c. Power and Sequential System.
- d. Guidance and Navigation System.
- e. Stabilization and Control.
- f. Service Propulsion and Reaction Control System.
- g. Instrumentation.
- h. Communications.

1-8. Each system control console operates simultaneously with, and independently of, the other system consoles. Each has a wide variety of test command capability necessary for complete checkout of a particular spacecraft system. In order that the command computer may systematically process each of the many parallel inputs from these consoles, a unit called the Communications Unit Executor (CUE), operating essentially as a commutator, interrogates each START module on all of the system control consoles in sequence. These interrogations occur at a high rate. Therefore, to the individual console operators, there is no perceptible delay in their individual test procedures. When an interrogation determines that a command input exists at a particular START module, the scanning process ceases momentarily while the CUE transfers the digital command to the command computer.

1-9. The computer interprets and acts upon the command under program control. Some commands instruct the computer to modify memory while others require some action to occur in the spacecraft. In the latter case, the computer formulates a digital command message for transmission to the spacecraft. The digital command message, which is generated by the computer in a parallel format, is converted into a serial bit stream by a Data Transmission and Verification Converter (DTVC) and transmitted to the spacecraft over a hardline link.

1-10. At the spacecraft location, the message is received and stored in registers in a Receiver-Decoder unit. The message is then decoded and applied to analog and relay command modules where the proper stimulus is generated and transmitted to the spacecraft.

1-11. Verification of the command message is accomplished by redundant transmission from the DTVC to the Receiver-Decoder. A bit-by-bit comparison is made of the redundant words. In addition, checks are made of each message to determine whether it contains a legal address.

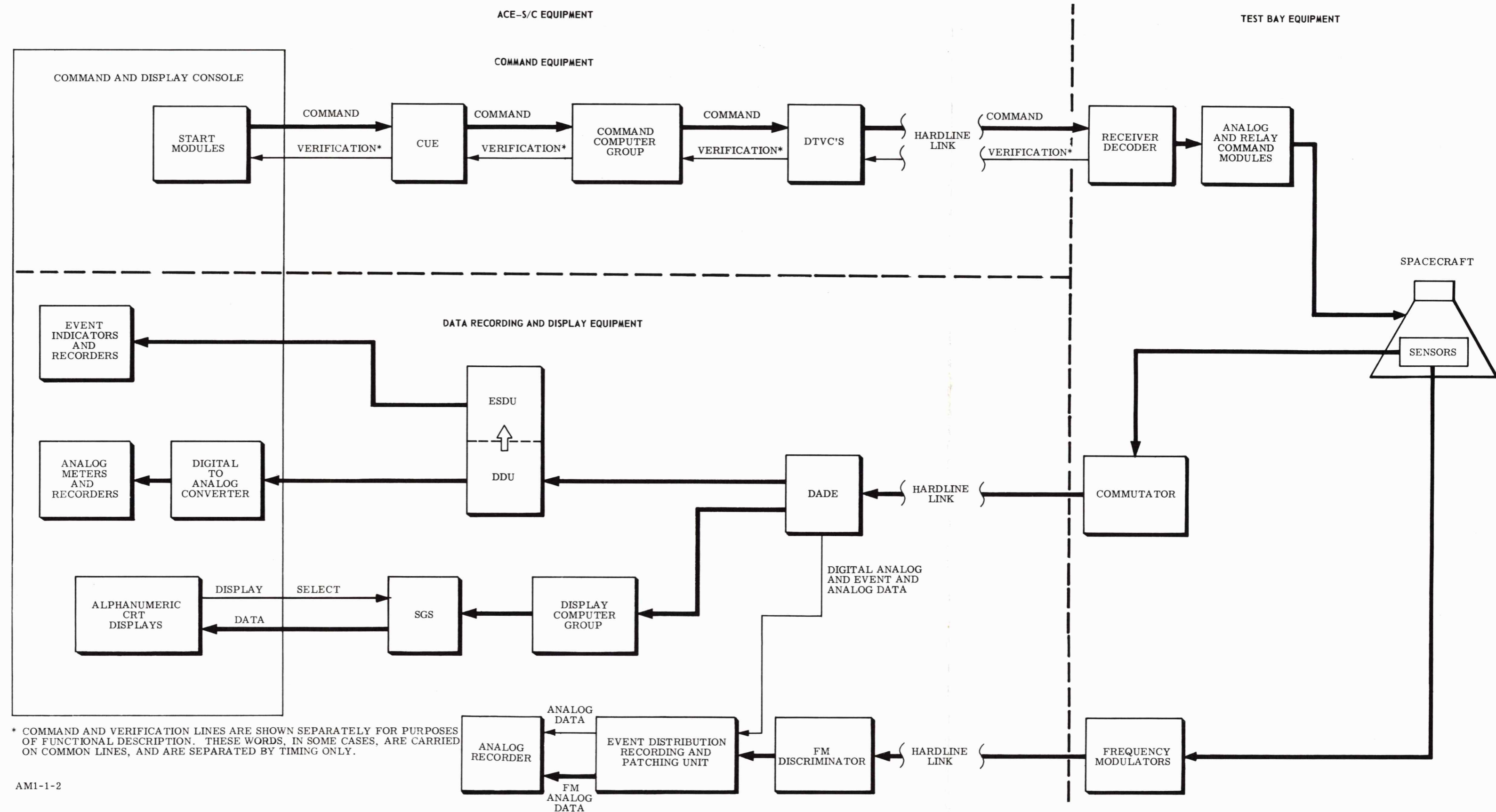


Figure 1-1. ACE-S/C Equipment Simplified Block Diagram

A verification reply message, containing the results of the foregoing checks, is transmitted from the Receiver-Decoder back to the DTVC. The delivery of a command message to the command computer and the verification of proper transmission from the computer to the spacecraft are indicated to the control console operator by appropriate lamps on the START modules.

1-12. DATA RECORDING AND DISPLAY EQUIPMENT.

1-13. Spacecraft performance and status data are monitored by sensors coupled to airborne checkout equipment, carry-on ground checkout equipment, and ground service equipment. Most of the measurements are commutated, converted to digital format, interleaved, and transmitted in serial pulse-code-modulated (PCM) form over a hardline link to the data acquisition equipment in the ACE-S/C station. A small portion of the data is frequency-modulated (FM) and transmitted over a separate hardline link.

1-14. At the ACE-S/C station, these data are received by the data acquisition equipment. The Digital Acquisition and Decommuration System (DADS) synchronizes on the incoming serial PCM bit stream, decommutates the data, provides an address for each event and analog data word, and presents these words for parallel transmission. The FM data are recorded directly on wideband magnetic tape and an oscillographic recorder. The analog and event words, derived from the PCM data, follow three paths when they leave the decommutator.

1-15. One path (addresses are not included) goes to the display computer where selected portions of the data are processed. This processing includes comparison of analog data with predetermined limits, and the conversion of these data into engineering units. A binary word representing the value of the data in engineering units is transferred into a memory in a Symbol Generator and Storage (SGS) unit. The SGS uses these words to generate alphanumeric character display signals (analog) for application to control console CRT displays. These alphanumeric characters appear in "page" form on the console displays. The particular page of data to be displayed at any console is selectable by the operator of that console. When a parameter has been determined by the computer to be out of limits, the intensity of the character representing that parameter will be caused to fluctuate at a low rate (i.e., the character will appear to blink).

1-16. The second data path transfers the digital data to the Decommuration Distribution/Event Storage and Distribution Unit (DD/ESDU). This unit accepts the data words, and, in the case of event data, stores each bit (representing an event) in an appropriate location in storage registers. The outputs of the storage registers, connected to indicator lamps and/or event recorders on the control consoles, cause the event lamps and recorders to indicate when an event has taken place. The analog data words are fed via the decommutator distribution

circuits of the DD/ESDU to all of the control consoles in parallel. When a console recognizes its particular address in these data words, it transfers the data portion of the word to a digital-to-analog (D/A) converter in the console. The output of the D/A converter drives meters or analog recorders located on the console.

1-17. The third data path transfers digital and analog data to the Event Distribution, Recording, and Patching Unit, and then to roll-chart recorders in the computer room. The digital data is processed in a manner similar to the DD/ESDU.

1-18. SUPPORT SYSTEMS.

1-19. There are several systems which form an integral portion of the ACE-S/C station, but cannot be categorized as portions of the Command, or Data Recording and Display, Equipment. These include the Timing System and the Status Display System.

1-20. TIMING SYSTEM. The timing group provides real-time signals for the use of the two computers and the various recorders. These time signals also drive wall time displays. In addition, the timing group supplies countdown-time signals to the computer wall clock displays.

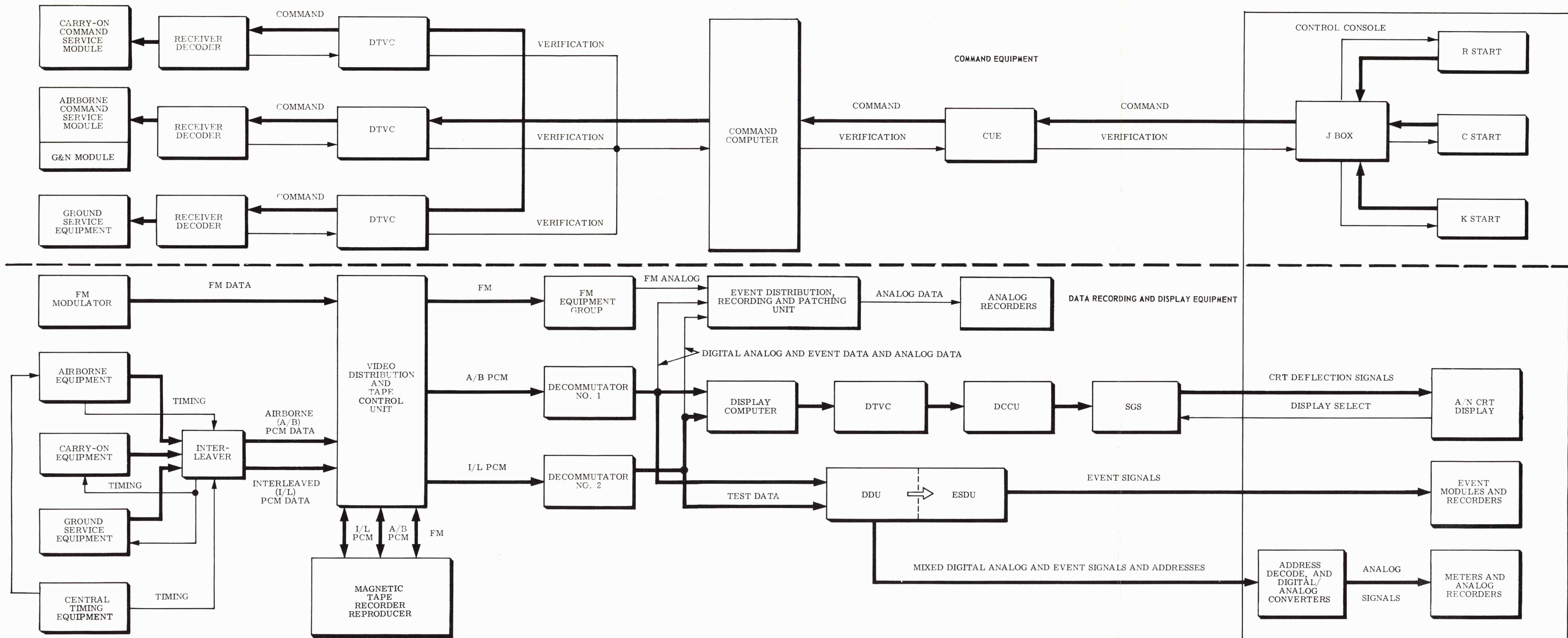
1-21. STATUS DISPLAY SYSTEM. The status display system consists of go-hold switches located on the command and display consoles for reporting the test operation status to the test conductor. The controls on the consoles are connected to a display panel on the test conductor console that displays indications of test countdown hold conditions.

1-22. COMMAND EQUIPMENT DESCRIPTION. (See figure 1-2.)

1-23. All commands are initiated by positioning switches on START modules. These modules are plug-in units, and are located in varying numbers on the system control consoles. There are three distinct types of START modules: R START modules providing for manual control of discrete events and selection of certain computer subroutines; C START modules providing for manual selection of computer subroutines and the parameters required by the subroutines; and a single K START module providing for manual and automatic means of inserting information into the spacecraft Automatic Guidance Computer (AGC).

1-24. R START MODULE.

1-25. The R START (relay selection START) module contains four pushbutton function switches, an execute (XEQ) pushbutton, and appropriate lights to indicate the status of the switches and of the module. The function switches provide the means to select the specific discrete events desired, and the XEQ switch initiates the sequence resulting in their occurrence. Each module controls the occurrence of four discrete events (e.g., individual relay action at the spacecraft) by providing a logical "one" or "zero" from each function switch.



AM2-1-2

Figure 1-2. ACE-S/C Equipment Block Diagram

The presence or absence of a "one" is established by the on or off condition of the function switch. The R START can also be used to call up certain computer subroutines.

1-26. C START MODULE.

1-27. The C START (computer communication START) module includes ten 12-position switches which provide the means to select a specific command function. Each individual switch position provides a four-bit digital word in binary-coded-decimal form for transmission to the computer. Thus, the command output of the C START is a 40-bit message which instructs the computer to perform specific operations (and also may provide parameters for these operations) and instructs the computer in the disposition of the results. The C START panel also includes status indication of the switches, an XEQ pushbutton to initiate the transmission, and appropriate lights to indicate the module status.

1-28. K START MODULE.

1-29. The K START (keyboard START) module may be operated either manually (using a keyboard) or automatically (using a perforated tape reader). The operator may select the operating mode. The keyboard provides 18 pushbutton switches. Depressing any one of these switches initiates the transmission of a five-bit word to the AGC. The module panel also includes tape reader control switches. These switches provide for automatic sequences of binary words from the tape or manual sequencing including both forward and reverse steps. A visual tape character readout display is provided. Appropriate display lights on the panel indicate the status of the module and of various events within the AGC.

1-30. COMMUNICATIONS UNIT EXECUTOR.

1-31. The primary function of CUE is to control the two-way communication path between the test operators and the command computer. To accomplish this control function, CUE sequentially interrogates all START modules in a repetitive fashion. The depression of an XEQ pushbutton (R START or C START) or a K START keyboard pushbutton results in interruption of CUE when it reaches that point in its cycle. CUE, under control of the computer, transfers the command data out of the START module, assigns an address which relates the data to its specific module, and transmits the data and its address to the computer. (The address assigned at this point is used for identification purposes between the START modules and the computer only.) The transmission to the computer is accomplished in two ways. If the data is from an R START, the data and its address will be transferred as a single 12-bit word in parallel format. If the data is from a C START or K START, the data and its address will be transferred as four consecutive, 12-bit words in parallel format.

1-32. When instructed by the computer, the CUE transmits verification replies to appropriate lights on the START modules. In the event of a failure, and when instructed by the computer, the CUE will display malfunction codes on a maintenance panel enabling the CUE operator to isolate the cause of failure.

1-33. COMMAND COMPUTER.

1-34. The command computer receives the addressed data words from the CUE and performs the required processing under program control. Data from an R START or K START are encoded into a 24-bit message which includes the required address for processing at the spacecraft location. Usually, C START data instruct the computer to perform preprogrammed subroutines, the results of which may or may not be transferred out of the computer.

1-35. The output of the computer is one or more 24-bit messages presented to a DTVC. Each 24-bit message is transmitted by the computer as two successive 12-bit words in parallel format. The computer selects one of three DTVC's depending on whether the message is intended for airborne, carry-on, or service equipment.

1-36. The command computer receives verification replies from the DTVC. If verification of proper message delivery is received, the CUE is instructed to indicate verification on the appropriate START module panel. Should the verification reply indicate malfunction, the computer will retransmit the message a predetermined number of times - each time waiting for verification of proper message delivery. Should the final reply still indicate failure, the computer will branch into a malfunction isolation subroutine. This routine will functionally isolate the failure, and the computer will instruct CUE as to the appropriate malfunction code to indicate on the maintenance panel.

1-37. DATA TRANSMISSION AND VERIFICATION CONVERTER.

1-38. The DTVC is a two-way communicator and a parallel-to-serial and serial-to-parallel converter. All computer input/output communications are in parallel format but all transmissions to and from the Receiver-Decoder at the spacecraft test area are in serial format.

1-39. The output of the uplink computer to the DTVC is a 24-bit message presented as two successive 12-bit words in parallel format. The DTVC converts each 12-bit word to serial format and transmits a 24-bit serial word, the second half of which is identical to the first half. Thus, the output of the DTVC is 48 bits which provide complete redundancy of the 24-bit message from the computer.

1-40. The DTVC also receives a 24-bit serial verification reply from the Receiver-Decoder at the spacecraft location. The second half of this 24-bit reply is a repetition of the first half.

The DTVC reads the first 12 bits into a register and then performs a bit-by-bit comparison with the second 12 bits to confirm redundancy.

1-41. If the redundancy check fails, the DTVC transmits the first 12-bit word to the computer along with the information that the check failed. If the redundancy check is successful, the DTVC proceeds according to a computer-selected mode of operation. It may decode the verification reply or present the word to the computer. If the reply is decoded by the DTVC, and the reply indicates a legal transmission, this fact is reported to the computer. If the transmission is determined to be illegal, the verification reply word is transmitted to the computer for evaluation.

1-42. RECEIVER-DECODER. (This is not a part of the ACE-S/C station.)

1-43. The Receiver-Decoder receives the first 24-bit word from the DTVC and assembles the first 12 bits into a 24-position register. It then compares the remaining portion bit-by-bit to check redundancy. The second 24-bit word of the command message is received, and the first 12 bits are assembled into the remaining spaces in the register. A bit-by-bit redundancy check is then performed. If either redundancy check fails, the register is cleared, the Receiver-Decoder is set to receive, and a verification message, coded to indicate transmission error, is transmitted back over the uplink line to the DTVC.

1-44. If a successful redundancy check is completed, decoding of the message address is begun. Decoding is accomplished at several levels. At each level, a number of discrete bits are examined to determine which of several alternate routes the remaining message bits are to follow. Decoding begins with the more significant address bits. In each case, the decoded bits are dropped, and only the remaining bits of the word are transmitted to the next lower level.

1-45. The Receiver-Decoder performs the first step of address decoding and accordingly selects one of several groups of modular assemblies known as baseplates, or the Guidance and Navigation (G and N) module. If the G and N module is selected, the remaining message bits are sent to this module which transfers the proper data into the spacecraft onboard automatic guidance computer. If one of the baseplate groups is selected, the remaining message bits are sent to all baseplates in this group for further decoding.

1-46. A given baseplate group may contain as many as eight baseplates. However, only one of these can accept the message as addressed. The selected baseplate will decode the message further and select one of the modules installed on the baseplate. The selected module will accept the remaining bits for further decoding.

1-47. There are two types of modules mounted on the baseplates - a D/A converter module and a relay module. Any baseplate can contain up to four modules with any combination of the two types, or all four of a single type.

1-48. If a D/A converter module is selected, it will decode the remaining bits and provide the indicated positive or negative voltage level as a spacecraft stimulus.

1-49. If a relay module is selected, it will decode the message further to select one of four subgroups of relays controlled by the module. Four data bits will be transferred to a buffer memory of the subgroup which exercises control over four relays. A second transmission from the uplink computer provides four duplicate data bits which are compared with those from the first transmission. If the comparison is exact, the first four data bits are shifted from the buffer memory to an execute memory which causes the four relays to react to the data bits, with a "one" causing latch and a "zero" causing unlatch. If the comparison is not exact, the data bits are not shifted to the execute memory, a coded verification reply is sent to indicate the comparison failure, and the Receiver-Decoder is set to receive.

1-50. At each level of decoding, from the Receiver-Decoder to the subgroup, the legality of the address is determined. In every case, there are fewer legal addresses than the total which the number of bits would permit. If the decoded portion of the address is found illegal, decoding ceases, the Receiver-Decoder is set to receive, and a coded verification reply is sent to the DTVC to indicate the level of decoding at which the error was detected.

1-51. RECORDING AND DISPLAY EQUIPMENT DESCRIPTION. (See figure 1-2.)

1-52. The recording and display equipment provides for receiving, recording, and displaying the spacecraft performance parameters and other data necessary for complete checkout of the spacecraft. This system is made up of the spacecraft and spacecraft vicinity equipment (not a part of ACE-S/C), Data Acquisition and Decommuration Equipment, Alphanumeric Display Equipment, and Analog and Event Recording and Display Equipment.

1-53. SPACECRAFT AND SPACECRAFT VICINITY EQUIPMENT.

1-54. Test data are obtained from sensors in the spacecraft (permanently installed), in the carry-on equipment (which is removed prior to flight), and in the Ground Service Equipment. Data obtained from the permanently installed spacecraft sensors are identical to that which are transmitted by the flight telemetry system and are called airborne (A/B) data.

1-55. The majority of data are converted to serial PCM format and transmitted to the ground station over hardlines. Certain data (e.g., the outputs of vibration sensors), which are required in raw form, are frequency modulated and transmitted to the ground station over a separate hardline.

1-56. The flight telemetry system contains the signal conditioning, commutation, encoding, and digital multiplexing equipment necessary to convert the A/B sensor outputs into a serial PCM output at 51.2 kilobits per second. This output is called A/B PCM. The carry-on equipment performs these same functions for the carry-on sensors.

1-57. The outputs of the ground service equipment sensors are fed to a unit known as the service equipment adapter, which performs the commutation, encoding, and digital multiplexing required to convert them into a third serial PCM output, called service equipment PCM. The carry-on and ground service equipment PCM data are combined to form a single 51.2-kilobit-per-second signal.

1-58. These three PCM outputs (A/B, and combined carry-on and service equipment) are fed to an interleaver which combines the PCM inputs into a single, interleaved (I/L), serial PCM output and transmits this to the ground station over a hardline at a rate of 204.8 kilobits per second. The A/B PCM, in addition to being interleaved with other data, is also transmitted intact (at its original rate of 51.2 kilobits per second) to the ground station over a separate hardline.

1-59. All PCM data, analog and event, are presented as eight-bit words. For the analog data, each eight-bit word represents a single analog sample. For the event data, each eight-bit word represents eight discrete events. Interleaving is performed on a word basis.

1-60. DATA ACQUISITION AND DECOMMUTATION EQUIPMENT (DADE).

1-61. The Data Acquisition and Decommutation Equipment group provides for acquiring, recording, synchronizing, decommutating, and distributing the data transmitted from the spacecraft vicinity. The three data lines (A/B, I/L, and FM) are routed to this equipment group through a terminal patch facility. This equipment group is made up of the Video Distribution and Tape Transport Control Unit and DADS.

1-62. VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT. The three incoming data lines are initially terminated at the Video Distribution and Tape Transport Control Unit which provides patching and switching to route the data to the desired decommutator (PCM), discriminator (FM), and magnetic tape recorder-reproducer (PCM and FM). The data are routed as follows:

- a. All data are routed to wideband magnetic tape recorders.
- b. The FM data may be routed to discriminators and then to an analog recorder.
- c. The A/B PCM data are routed to one of two DADS units.
- d. The interleaved stream of A/B, carry-on, and service equipment data is routed to the other DADS unit.

1-63. **DIGITAL ACQUISITION AND DECOMMUTATION SYSTEM.** The DADS unit provides the processing necessary to convert the incoming eight-bit serial data words into parallel format and assign addresses to them for distribution within the ground station. At the input to the DADS unit, bit synchronization is achieved, and each pulse is reshaped to assure good bit definition prior to further processing. The serial data bits are read into a shift register and as the data are shifted through the register, frame synchronization is established. Following frame synchronization, subframe synchronization is established. At this point, the location and identity of each data word are known and read out of the register in parallel format and presented at the decommutator output. Simultaneously, in accordance with decommutator programming, the appropriate address for each data word and a read pulse are presented at the decommutator output. The decommutator output (without addresses) is routed to the Alphanumeric Display System via the Decommutator/Computer Interface Unit and Display Computer, and (with addresses) to the Event and Analog Data Display System.

1-64. **ALPHANUMERIC DISPLAY SYSTEM.**

1-65. The Alphanumeric Display System furnishes the primary displays for monitoring analog measurements and certain event occurrences. It provides at a single location the capability of simultaneously viewing 24 lines of data presented in decimal numbers and engineering units on the screen of a CRT. Switching capability on the display module permits the callup of 40 separate data tabulations each of which has a 12-line capacity. Suitable function and page identification are also displayed. This display capability requires data processing, storage, symbols generation, and CRT display.

1-66. **DATA PROCESSING.** Data from the decommutators are routed to the downlink computer through the input/output module. These data are stored in two locations in the memory. While a block of data is being stored in one location, the computer processes data in the other location. The primary operations which the computer must perform in processing the downlink data include the following:

- a. Assemble the data into proper word length and format.
- b. Compare any given word or words to determine whether the data fall within predetermined limits, and flag out-of-limit conditions.
- c. Compute the average of a block of words and retain this average for output display.
- d. Convert data into engineering units, both linear and quadratic functions, using curve techniques.
- e. Convert data and place in proper format for alphanumeric CRT display.

1-67. Operating under program control, the computer provides a series of 12-bit coded words which include parameter value and address and associated instructions. These 12-bit words are transmitted in parallel format to the DTVC.

1-68. DATA TRANSMISSION. The DTVC converts each 12-bit word to serial format and transmits it redundantly as a 24-bit serial message to a Digital Communication and Control Unit (DCCU). The DCCU assembles the first 12 bits into a register and then compares the second 12 bits with the first 12 bits to check redundancy. If the redundancy check is successful, the DCCU transmits the 12-bit word in parallel format to an SGS unit. The DCCU has the capability of preventing transmission to the SGS if the redundancy check fails.

1-69. SYMBOL GENERATION AND STORAGE. The SGS unit receives the coded words from the DCCU. The 12-bit words are decoded, and the data are stripped out and stored in memory locations according to received instructions and addresses. The entire content of this memory is updated once per second, and it is scanned at a rate sufficient to update all alphanumeric displays at least 30 times per second.

1-70. The character repertoire of the SGS allows display of all alphanumeric characters together with a set of special symbols. Also incorporated is the capability to cause characters to blink on the CRT screen when so instructed by the computer. This blinking indicates an out-of-tolerance condition.

1-71. Memory allocations in the SGS are sufficient to provide for display of 20 pages of data, a page consisting of 24 lines of 40 characters each plus two 32-character lines, one at the top and one at the bottom of the page. Upon demand, the SGS will provide the proper signals to cause the contents of any top half-page and any bottom half-page to appear on the screen of the requesting CRT. Any given half-page can be selected by as many as 20 cathode ray tubes simultaneously.

1-72. CRT MODULES. The CRT's utilized for the Alphanumeric Display System are 10-inch, electrostatically deflected devices. The modules include controls for selecting any top half-page and any bottom half-page of the 20 pages of data stored in the SGS for simultaneous display. In addition, the CRT module includes controls for focusing, brightness, horizontal and vertical gain and centering, and an on/off switch.

1-73. Any given half-page display contains 12 lines of identified data in decimal numbers and engineering units. In addition, a single top (or bottom) line provides page identification.

1-74. ANALOG AND EVENT DISPLAY SYSTEM.

1-75. All data words from the decommutator are applied to the decommutator distribution section of the DD/ESDU. This portion of the unit acts as a distribution amplifier, providing one 21-line output to the event storage and distribution section (for events) and one 21-line output to each console (for analog words).

1-76. **EVENT DATA DISPLAY.** Event data words are selected from intermixed analog and event data words received from the decommutator distribution circuits in the event storage and distribution section of the DD/ESDU. This selection (by address recognition) and the storage location of each event bit is predetermined by the selection and arrangement of plug-in logic modules within the event storage and distribution circuits.

1-77. The ESDU will select and store 150 event words, each of which consists of eight discrete event functions (a total of 1200 events). The event words are gated into registers within the ESDU. The output of each bit position in a register represents the status of a specific event (whether it has or has not occurred).

1-78. The outputs of the storage registers are routed to a patch facility in the DD/ESDU. The patching at this point determines the distribution of each event function to the various consoles and permits routing any specific event function to multiple locations. The outputs of the ESDU are fed to event recorders and/or lamp drivers (in the consoles) which cause event lamps to light.

1-79. Event modules are located on the various system control consoles. The front panel of an event module contains 24 lights arranged in three vertical rows of eight lights each. Each light is equipped with a colored lens marked to identify the event function. These lenses are replaceable, should it be desired to change the display. A lamp test switch on the module tests the function of all lamps simultaneously.

1-80. Event recorders are utilized to provide permanent records of events where the time and/or duration of events are desired. Two types of event recorders are used: a 32-channel recorder providing a continuous-write, deflection-type presentation; and a 100-channel recorder providing a write/no-write indication of event status. Both recorders have paper-speed controls and each includes time-recording channels.

1-81. **ANALOG DATA DISPLAY SYSTEM.** The intermixed analog and event data words from the decommutator distribution circuits of the DD/ESDU are routed to all system control consoles. Each control console has address selection circuits that select the analog data words to be displayed at that particular console. The division between decommutator output and the selection of addresses that will be accepted are predetermined by the selection and arrangement of plug-in modules in each control console.

1-82. These address logic circuits decode the address portion of analog data words to gate the data portion of the word into a storage register. The storage register is connected to a D/A converter that operates a meter and/or a pen on an analog recorder. In some consoles, the data to be displayed on a particular indicator can be selected from as many as four

different addresses. This address selection is controllable by means of a switch on the console front panel.

1-83. QUICK REFERENCE TABLE OF MAJOR UNIT FUNCTIONS.

1-84. Table 1-1 provides a brief description of the functions of each major unit in the ACE-S/C ground station and the relationship of each unit to units immediately preceding and following. This table is not intended to supplant the functional description of the ground station, but should be used as a reference after the functional description has been read.

Table 1-1. Quick Reference Table of Major Unit Functions

UNIT NO.	NAME	FUNCTION
		NOTE
		Items <u>a.</u> and <u>b.</u> apply to all consoles except as noted.
1	Environmental Control Console - High Cabinet ⁽⁶⁾	a. Display and/or record: Analog signals, received in digital form from Decommutator Distribution Unit/Event Storage and Distribution Unit 21.
2	Fuel Cell and Cryogenics Console - High Cabinet ⁽¹⁾⁽⁶⁾	Discrete event signals received from Decommutator Distribution Unit/Event Storage and Distribution Unit 21.
3	Power and Sequential System Console - High Cabinet	Alphanumeric data received in analog form from Symbol Generator and Storage Unit 201.
4	Guidance and Navigation System Console - High Cabinet	b. Send command words via Communications Unit Executor 202 to Command Computer Unit 120 from:
5	Stabilization and Control Console - High Cabinet	R START modules - controlling discrete events (relay closures) in the spacecraft vicinity.
6	Service Propulsion and Reaction Control System Console	C START modules - providing specific operation instructions to the Command Computer (may supply operational parameters) and instructs computer in disposition of results.
7	Power and Sequential Recorder Console - High Cabinet ⁽¹⁾⁽³⁾⁽⁴⁾⁽⁵⁾	K START module - initiates transmission of five-bit command words to spacecraft Automatic Guidance Computer. ⁽²⁾
8	Fuel Cell and Cryogenic and Environment Control Shared Console - High Cabinet ⁽¹⁾⁽³⁾⁽⁴⁾	
10	Test Conductor Console ⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾	

Table 1-1. Quick Reference Table of Major Unit Functions (Cont'd)

UNIT NO.	NAME	FUNCTION
11	Environmental Control Console - Low Cabinet (3)(5)(6)	
12	Fuel Cell and Cryogenics Console - Low Cabinet (3)(4)(5)(6)	
13	Power and Sequential Console - Low Cabinet (5)(6)	
14	Guidance and Navigation Console - Low Cabinet (5)(6)	
15	Stabilization and Control Console - Low Cabinet (3)(5)(6)	
16	Service Propulsion and Reaction Control System Console - Low Cabinet (5)(6)	
18	Instrumentation Console - Low Cabinet (5)(6)	
19	Communications Console - Low Cabinet (4)(5)(6)	
NOTES:	(1) Does not contain alphanumeric display. (2) In Guidance and Navigation Console High Cabinet only. (3) Does not contain analog meter displays. (4) Does not contain event display panels. (5) Does not contain analog recorder. (6) Does not contain event recorder.	
21	Decommutator Distribution/Event Storage and Distribution Unit	DDU circuits amplify and fan out decommutator digital words to ESDU circuits and to consoles. ESDU circuits decode event words and distribute discrete event signals to consoles. Real or playback time is also distributed to console recorders by this unit.
100, 102	PCM Decommutator	Achieves synchronization with incoming data from spacecraft. Converts serial data to eight-bit parallel words, assigns addresses, and supplies them to the Display Computer, Decommutator Distribution Unit, and Event Distribution, Recording, and Patching Unit. Additional analog outputs are supplied to Analog Recorder Unit 110.

Table 1-1. Quick Reference Table of Major Unit Functions (Cont'd)

UNIT NO.	NAME	FUNCTION
101	PCM Simulator	Provides simulated PCM signals for maintenance of PCM Decommutator Units 100, 102.
104	Video Distribution and Tape Transport Control Unit	Distributes incoming signals, from spacecraft test area, between decommutation equipment and raw data tape recorders. Allows patching between raw data recorders and decommutators. Provides controls for tape search and positioning on recorders.
105, 106, 107	Magnetic Tape Recorder and Reproducer	Record and play back PCM and FM raw data from the spacecraft test area, reconstructed PCM data (data on which synchronization has been obtained), voice and other miscellaneous signals.
110	Analog Recorder	Records analog signals received from decommutation equipment units 100, 102, 165.
113	Event Distribution, Recording, and Patching Unit	Decodes event words and distributes discrete event recorder in this unit. Provides patching facilities for Analog Recorder Unit 110.
116	Tape Recorder/Computer Time Decoder and Search Control Unit	Decodes and displays current (present) time from Timing Group 203; generates signals used to position tapes on raw tape recorders 105, 106, and 107; provides interface for transfer of current time to computers.
117	Countdown Generator/Interface and Translator Unit	Decodes countdown time from Timing Group 203 for display on wall clocks, and provides interface for transfer of countdown time to computers.
119, 139	Computer Console	Contains operating controls for computers.
120	Command Compute Module	Receives test command inputs from START modules via CUE. Formulates command messages, under program control for transmission to spacecraft via DTVC's.
121, 141	Typewriter	Provides computer data entry, and readout display. Primarily for maintenance.

Table 1-1. Quick Reference Table of Major Unit Functions (Cont'd)

UNIT NO.	NAME	FUNCTION
122, 142	Card Reader	Provides means of entering data from punched cards into computer.
124	Magnetic Tape Controller	Controls movement of tapes on magnetic tape transport units 125, 126, 195, and 146 under computer control.
125, 126, 145, and 146	Magnetic Tape Transport	Reads program tapes into computer memory.
127	Digital Transmission and Verification Converter	Contains four DTVC units, three units convert parallel digital test command words from the command computer to serial format and transmit them to the spacecraft test area. They then receive a verification reply and transfer this to the computer. The fourth DTVC forms part of a chain that transmits display words from the display computer to Symbol Generator and Storage Unit 201.
130	Input/Output Unit	Provides additional data channels for the computers. Operates under control of the computers.
131	Memory Unit	Shared by command and display computers. Increases memory storage capacity of both computers.
140	Display Compute Module	Receives digital format analog display data from Decommutator Units 100, 102. Performs limit comparisons and mathematical computations on these data, and sends resultant display words to the SGS Unit 201 via display DTVC Unit 127 and DCCU Unit 200.
145, 146	Magnetic Tape Transport	Provides program data for transfer into computer memory from tapes placed on the transport.
147, 148	X-Y Plotter	Provides computer with curve tracing capability mainly for long-term data trends.
150	Line Printer	Provides for printout of data from computer.
151	Punch Control	Allows computer readout to punch 80-column cards on card punch.

Table 1-1. Quick Reference Table of Major Unit Functions (Cont'd)

UNIT NO.	NAME	FUNCTION
152	Card Punch	Punches 80-column cards either from keyboard (manually) or from punch control (computer).
153	Computer Complex Console	Provides system monitoring facilities, de-commutator status display, and raw data tape recorder controls.
165	FM Discriminator Unit	Demodulates incoming FM data for recording.
166	FM Calibration Unit	Provides calibration signals for FM Discriminator.
200	Digital Communications and Control Unit	Part of the data link between the display computer and Symbol Generator and Storage unit. Converts serial display data words from the display DTVC to parallel formats and performs a verification check on these words. Also provides the control signals necessary to enter the data words into the SGS.
201, 211	Symbol Generator and Storage Unit	Receives the digital display data words from the DCCU, and converts these words to analog voltages to create an alphanumeric display on console CRT display units.
202	Communications Unit Executor	Controls the two-way communication path between the test operators and the command computer. Scans all START modules sequentially and stops at START having entered data. Transmits this data and its address to the computer.
203	Timing Group	Generates present (real) and countdown time for display, recording, and the use of the computers.
220	Terminal Facility Patchboard	Provides patching facility between units, and between ground stations, for various test configurations.
240	CCTV Control Racks	Provides controls for closed circuit TV cameras.

PART 2

PHYSICAL DESCRIPTION

1-85. ACE-S/C STATION PHYSICAL CONFIGURATION AT DOWNEY, CALIFORNIA.

1-86. The purpose of this part is to present the physical arrangement of the equipment within the ACE-S/C station and the orientation of the ACE-S/C station within the NAA Apollo Systems Integration and Checkout Facility.

1-87. The ACE-S/C station is made up of three separate equipment areas: the Control Room, the Computer Room, and the Terminal Facility Room. This provides for logical equipment grouping and separation of personnel concerned with different aspects of system operation. Certain subsystems, of necessity, cut across these physical boundaries. Portions of these subsystems, will, therefore, be found in more than one of the three rooms.

1-88. Two ACE-S/C stations support spacecraft test operations at the NAA Downey facility. Actually, two Control Rooms, two Computer Rooms, and only one Terminal Facility Room are employed. In this installation, the Terminal Facility Room is capable of supporting two ACE-S/C stations simultaneously.

1-89. The two ACE-S/C stations at NAA Downey are housed in the Apollo Systems Integration and Checkout Facility. This facility, identified as Building 290, is an extension of Building 6. The stations occupy areas on the first and second floors in the west wing, or Building 290, as shown in figures 1-3 and 1-4.

1-90. CONTROL ROOM EQUIPMENT.

1-91. The Control Room contains the primary controls and displays of the ACE-S/C station. These are arranged in a series of consoles, grouped according to functional spacecraft systems, providing a central location for stimulating and monitoring the performance of each functional system.

1-92. The Control Room equipment layout is shown in figure 1-5. The system consoles are arranged in the following functional groups:

- a. Test Conductor Console.
- b. Instrumentation Console (Inst).
- c. Communications Console (Comm.)

- d. Environmental Control System Console (ECS).
- e. Fuel Cell and Cryogenics Console (FC and C).
- f. Power and Sequential Console (Pwr and Seq).
- g. Guidance and Navigation Console (G and N).
- h. Stabilization and Control (Stab and Cont).
- i. Propulsion and Reaction Control Console (Prop and RCS).

1-93. COMPUTER ROOM EQUIPMENT.

1-94. The Computer Room (figure 1-6) contains the digital acquisition and decommutation equipment, a computer complex, the DTVC's, and the ACE-S/C station checkout equipment.

1-95. The data acquisition and decommutation equipment is comprised of the DADS, the magnetic tape recorder-reproducers, the video distribution and tape transport control unit, and the FM equipment group.

1-96. The computer complex includes a computer complex console, two computer modules (the command and display computers), a shared memory module, a shared input/output module, and associated peripheral equipment.

1-97. The ACE-S/C checkout equipment includes a PCM simulator, an event recorder, and several analog recorders. The computer complex console contains START modules, displays, and controls employed in ACE-S/C station checkout as well as for monitoring system performance. An Event Distribution, Recording, and Patching Unit is provided to drive the Computer Room event displays.

1-98. Wall clocks, displaying real- and countdown-time, are also provided in the Computer Room.

1-99. TERMINAL FACILITY ROOM EQUIPMENT.

1-100. The Terminal Facility Room (figure 1-7) provides a flexible interface between the remote spacecraft test areas and the two ACE-S/C stations. It also provides certain support and interfacing functions within the stations.

1-101. The Terminal Facility Room contains the Terminal Patch Facility, the timing group, certain alphanumeric display system units, and the CUE unit.

1-102. The Terminal Patch Facility serves as the external interface for all ACE-S/C station input and output data lines. It also serves as the primary patch facility for intrastation and interstation data lines.

1-103. The Timing Group is comprised of a time code generator which drives various real-time displays in the two stations and two countdown generators (one for each station) which drive countdown displays.

1-104. The units of the alphanumeric CRT display system located in the Terminal Facility Room are the DCCU and the SGS. These units interface between the Control Room and the Computer Room. Two of each are provided to serve the two ACE-S/C stations.

1-105. Normally, the two ACE-S/C stations will operate independently of each other; however, by means of cross-patching within the Terminal Facility Room, either Computer Room can operate with either Control Room.

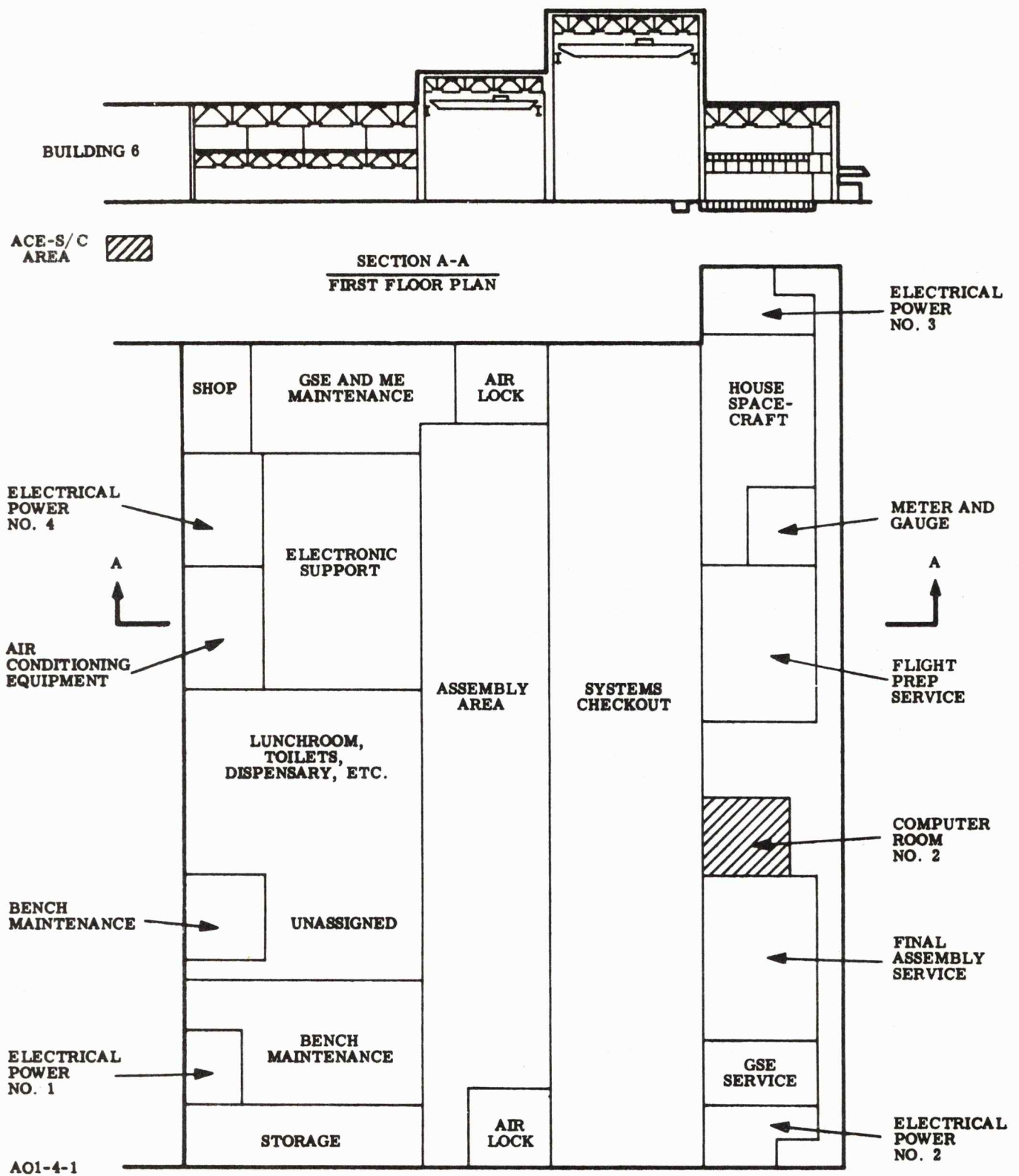
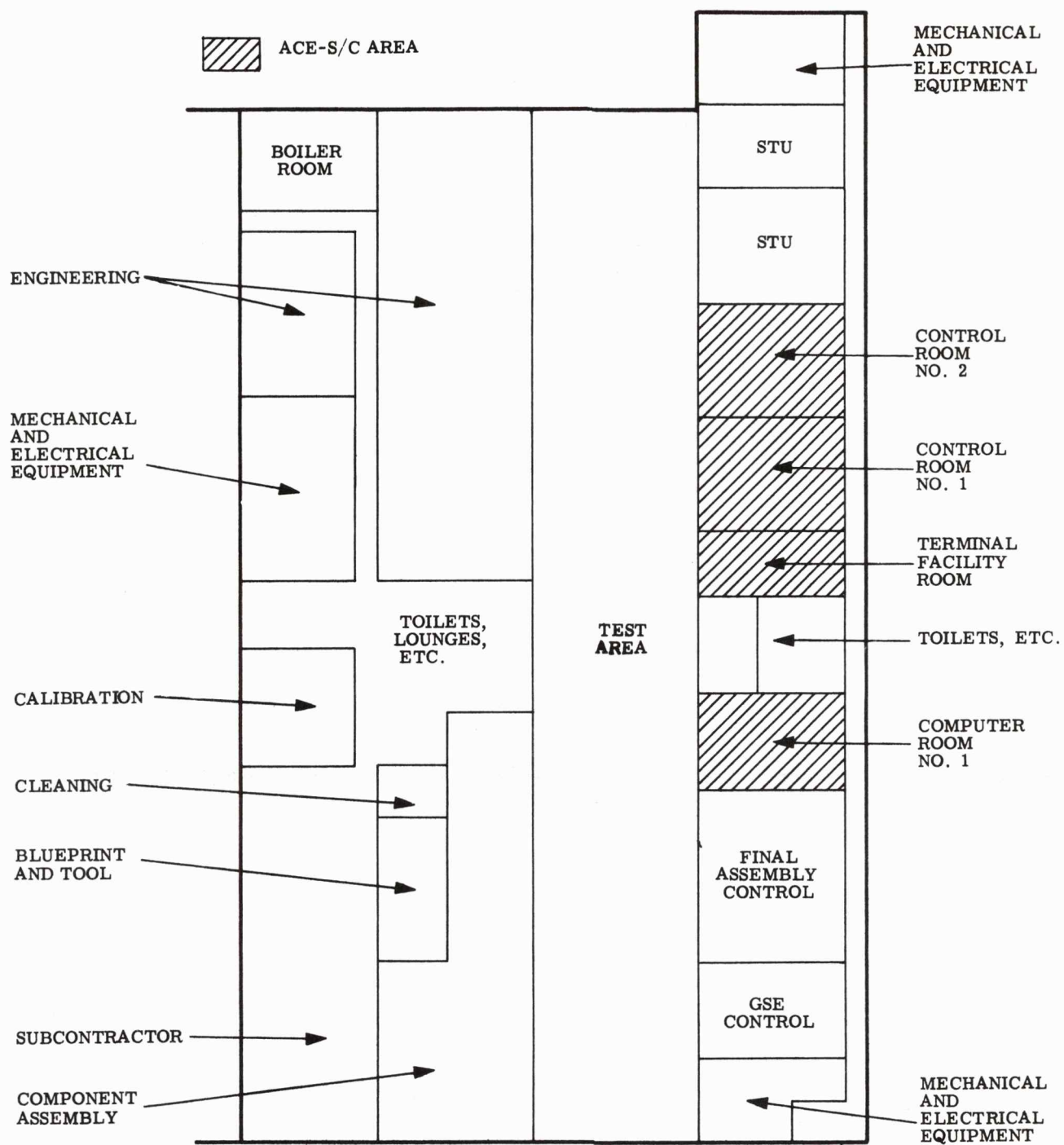
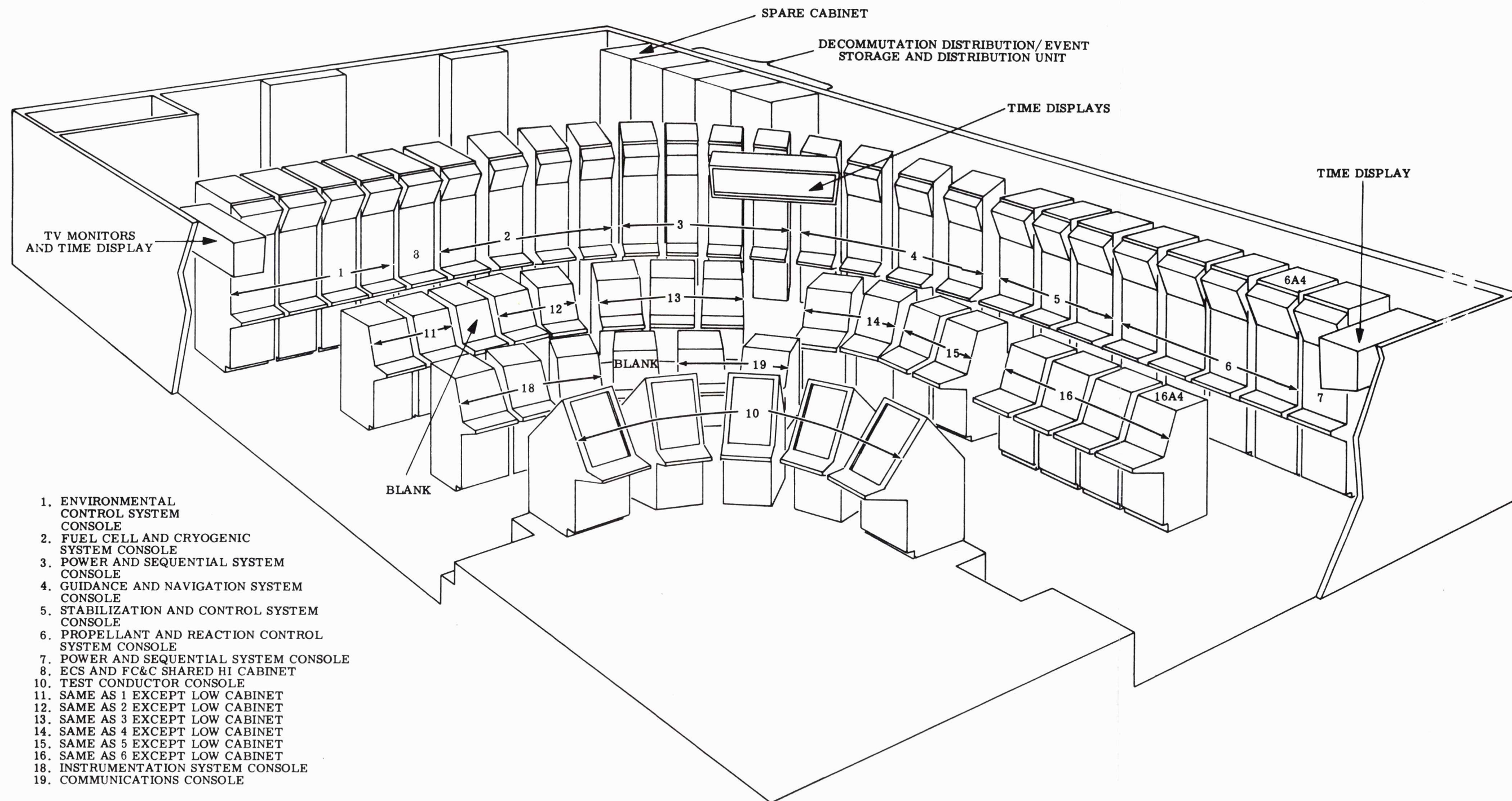


Figure 1-3. First Floor Plan of NAA Building 290



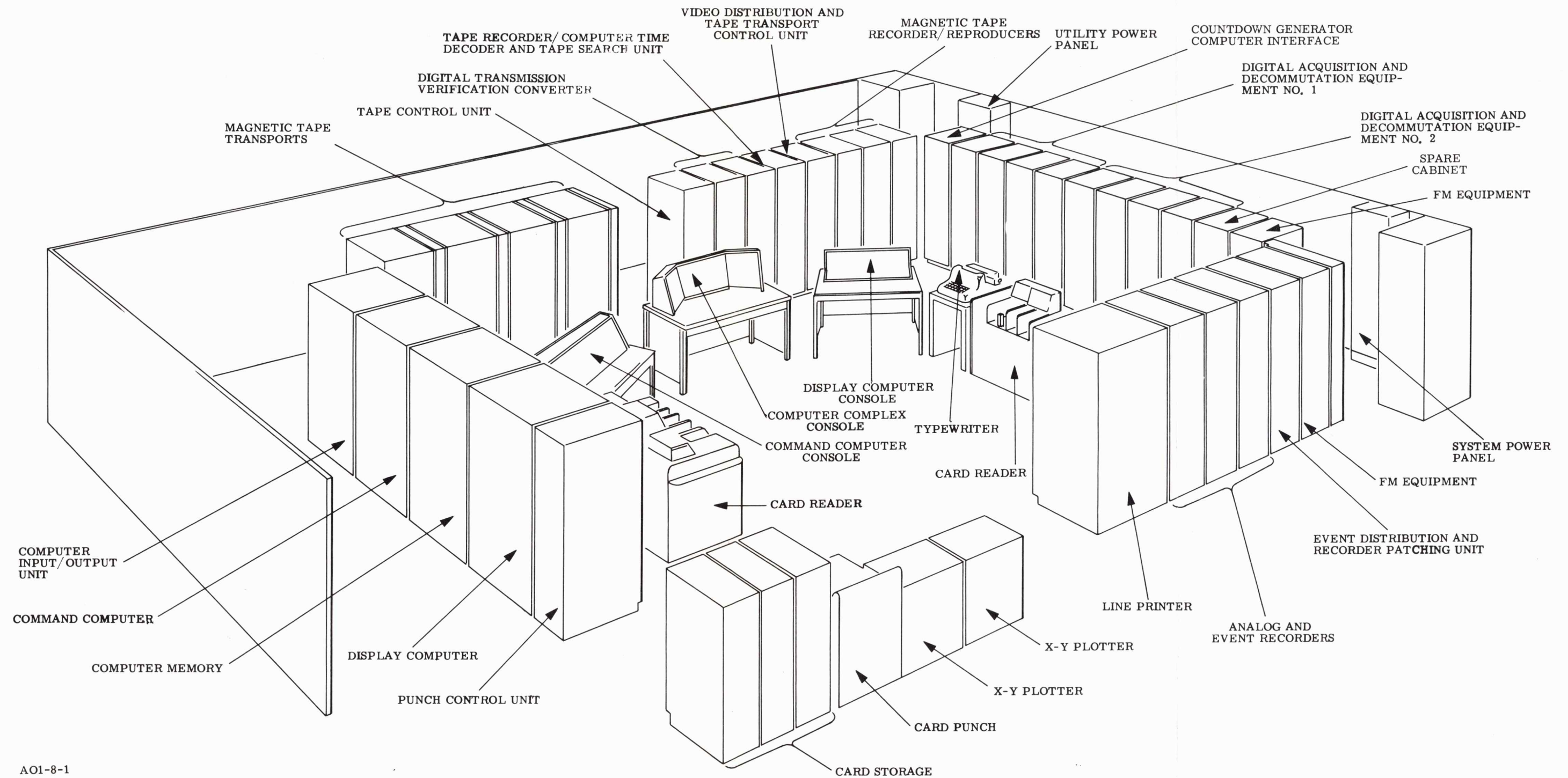
AO1-5-1

Figure 1-4. Second Floor Plan of NAA Building 290



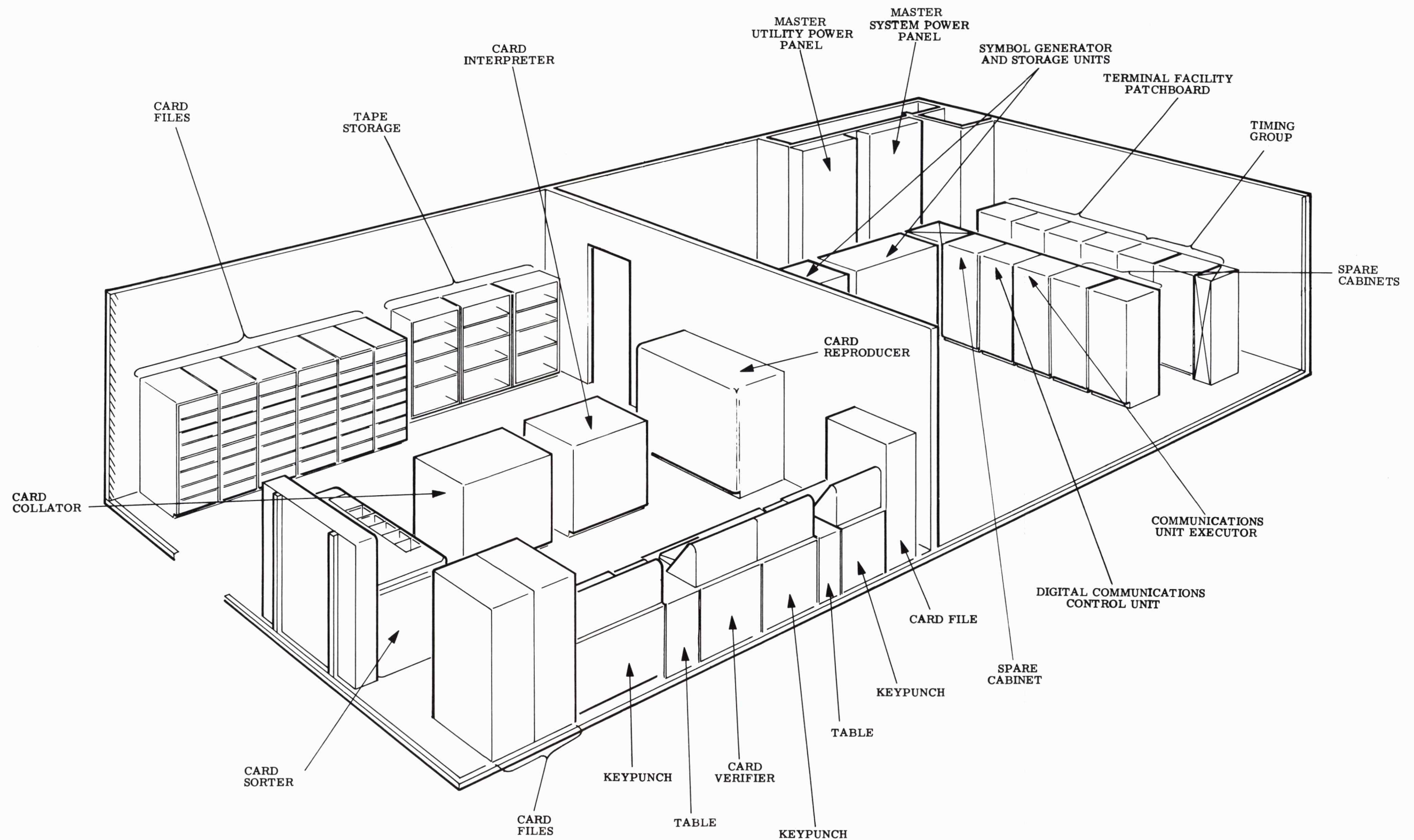
AO1-6-1

Figure 1-5. NAA Control Room Perspective View



AO1-8-1

Figure 1-6. NAA Computer Room
Perspective View



AO1-10-1

Figure 1-7. NAA Terminal Facility Room
Perspective View

SECTION II

COMMAND EQUIPMENT

2-1. DATA ENTRY EQUIPMENT. (See figure 2-1.)

2-2. The data entry equipment consists of the START modules, J-Boxes, and CUE. This equipment is described below as functional parts of the data entry portion of the Command Equipment. The data entry equipment operates in three modes: Interrupt Mode, Manual Mode, and Maintenance Mode.

2-3. INTERRUPT MODE.

2-4. The computer initiates data entry equipment operation by a program-controlled Master Clear. This command places the data entry equipment in the Standby Mode of operation. When the computer is ready to send data to the data entry equipment, it sends an Interrupt Mode instruction to the CUE. On receipt of this code, the CUE changes the equipment from the Standby Mode to the Interrupt (normal working) Mode of operation. The equipment is then capable of transmitting data or test commands to the computer.

2-5. When power is turned on and all controls are in initial operation positions, the data or instructions are set on the switches of the START modules by the individual operators. The switch indicators light to confirm operator selection. The operator activates the module by depressing the execute switch. The START module gates the execute signal and the data through the J-Box to the CUE. The CUE generates an interrupt to the computer when it receives this signal and stops the scanning operation at the address of the START unit.

2-6. When the computer recognizes the interrupt, it halts its normal routine and jumps to a subroutine. The subroutine normally sends a Status Request instruction followed by an INA instruction to the CUE. The interrupt signal is dropped following a select signal. The INA instruction generates an Input Request signal to the CUE. Following this signal a response code is gated from the CUE to the computer. The INA instruction gates the status response code into the computer's exchange register. After the computer requests and has received the status of the equipment, it must then select the data entry equipment for the input of data.

2-7. An input instruction selects the data entry equipment to transmit data to the computer. The INA instruction generates an Input Request signal to the CUE. The CUE generates an

Input Ready signal and transmits it, and the data (consisting of four data bits and eight address bits), to the computer. The input of data to the computer proceeds one word at a time, until the last word has been transmitted. The computer gates the data or issues a compare instruction to a DTVC. The compare instruction is followed by an OTA instruction. This instruction gates an Information Ready signal, four data bits, and the eight-bit address back to the CUE for a second comparison. If the addresses compare, an Output Resume signal is gated to the computer. If the addresses do not compare, the computer halts and waits for a reply from the control program or from the operator.

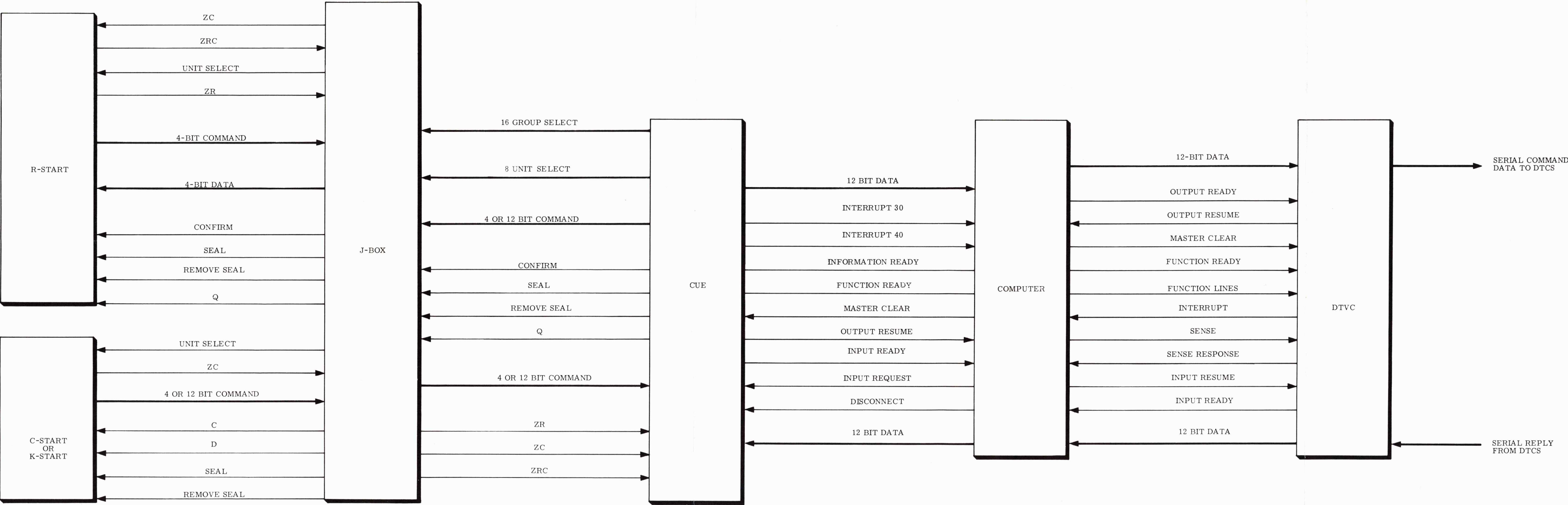
2-8. When the computer receives the Output Resume signal, it gates the next data to the DTVC. The DTVC processes the data and gates a response back to the computer. The computer gates the eight-bit address and the four response bits to the data entry equipment by using one of the output instructions. The Select External Allocated Lockout (SEAL) and remove SEAL instructions are used to initiate an input to the START modules. The control program must contain either one of the two instructions.

2-9. The SEAL command is used to temporarily inhibit processing of a command from a START module until the computer has completed processing a subroutine resulting from a previous command from that module. The remove SEAL command serves two purposes:

- a. If the START module was previously SEALed, this command will enable the processing of a data entry that was set into the START during the SEAL condition. If no new entry was made, the command simply extinguishes the SEAL lamp.
- b. When the equipment is turned on, the unSEAL command is separately applied to all START modules to set them to initial conditions prior to operation.

2-10. If the SEAL instruction is called for, it is followed by an OTA instruction. The OTA instruction gates the eight-bit address and the four response bits to the CUE. The control logic of the CUE translates the four data bits and sends a confirm signal and a SEAL command to the START module.

2-11. The remove SEAL instruction is followed by an OTA instruction. The OTA instruction gates the eight-bit address and four response bits to the CUE. The control logic in the CUE generates group and unit select signals and a remove SEAL signal to the particular insertion unit. The CUE also generates an Output Resume signal to the computer indicating that it has processed the information. If the status of the system is known, another Status Request is not required. The computer selects the equipment directly by using the input or remove SEAL instruction. The two instructions do not gate a status response code to the computer. Their operation is the same as discussed previously.



AM2-1-5

Figure 2-1. Command Equipment Block Diagram

2-12. MANUAL MODE.

2-13. This mode of operation provides the data entry equipment with a checkout system for maintenance purposes. The operator at the control panel of the CUE controls the operation of the system in this mode. The primary use of this mode is to determine which particular START module is malfunctioning. The use of this checkout feature does not interfere with the DTVC. Initially, the operator sets the START ADDRESS switches on the control panel of the CUE to select the desired START unit. The equipment is activated by depressing the execute switch on the CUE control panel. The CUE sends execute and select signals to the START unit. When the START receives these signals, it gates its data content to the CUE. The computer must be programmed to supply an INA instruction. This instruction enables the data to be transmitted to the computer. An OTA instruction is used to gate the data back to the CUE for display.

2-14. MAINTENANCE MODE.

2-15. The computer, under program control, selects this mode by a Maintenance Mode instruction. This instruction is followed by an OTA instruction. The eight-bit address of the START module and the four data bits must follow the OTA instruction. The OTA instruction generates an Information Ready signal. The computer transmits the Information Ready signal, the data, and the address to the CUE. The CUE selects the START module that corresponds to the address and returns an Output Resume signal to the computer. The CUE then transmits the data to the START module unit where it is displayed on the F switch indicators. This data is also displayed in the START ADDRESS and FUNCTION SWITCH STATUS indicators on the control panel of the CUE. A second word, containing 12 bits of data that represent a faulty reply from the DTVC, is displayed in the TRANSMISSION STATUS RESPONSE indicators. After displaying the data and address, the computer halts and waits for a reply from the control program or from the operator.

2-16. R START FUNCTIONS.

2-17. R START operation is initiated by setting any combination of function switches on the front panel to a "1." Each switch that is set to a "1" sends a current to the lamp in the lower half of the pushbutton causing it to light (figure 2-2). Each switch that has the lower half of the pushbutton lighted also sends a signal to the data gate for transmission to the CUE. After the R START operation is initiated, actual logic functions may occur one of several ways as explained below.

2-18. R START OPERATION.

2-19. When the operator is ready to enter data from the function switches into the CUE, the operator depresses the XEQ switch. This sends a signal to the execute logic and a current

to light the execute lamp in the lower half of the XEQ switch pushbutton. The execute signal to the execute logic causes a level to be sent to the Z_{RC} gate. If a Z_C is also applied to the gate, a Z_{RC} signal will be sent to the CUE to prevent the CUE from interrogating any of the C START's before all the R START's have been checked. After the execute switch has been operated, the execute logic will send a Z_R pulse to the CUE and to the data gate when a unit select signal is received from the CUE. This pulse will cause the data gate to also send the contents of the function switches (function data) to the CUE. If the computer accepts the function data from the CUE, a confirm signal will be sent to the R START control logic along with a function code. The confirm will cause the control logic to send a set signal to the latch register and a reset signal to the execute logic. This allows the function code to set the latch register and light the appropriate lamps in the upper half of the function switch pushbuttons as well as reset the execute logic. If the function data has caused the computer to call up a special subroutine, a SEAL signal will be applied to the control logic. This will light the SEAL lamp and send an inhibit signal to the execute logic. The signal prevents the execution of additional commands until the computer completes the present one. However, new data may be set into the function switches and the execute switch depressed. The command will be stored by the execute logic until a remove SEAL signal is received by the control logic. The control logic will then execute the new command as described above. The signal is supplied to the R START by the CUE for test purposes. The Q signal performs the same function as the execute signal generated by the execute switch.

2-20. C START FUNCTIONS.

2-21. The C START module operation is initiated by setting any combination of numbers into the function switches on the front panel of the module. Each switch sends signals to a translator which converts these signals into four-bit binary coded signals (figure 2-3). The translators in turn apply the four-bit binary signals to output gates and decimal display indicators. After the C START operation has been initiated, actual logic function will occur one of several ways explained below.

2-22. C START OPERATION.

2-23. When the operator is ready to enter data from the function switches into the CUE, he depresses the XEQ switch. This sends a signal to the execute logic which in turn lights the execute lamp in the lower half of the XEQ switch pushbutton. When a unit select signal is applied to the execute logic by the CUE it sends an execute signal to the control logic. This causes the control logic to apply a signal to the gate circuits and gate the four-bit binary coded signal from S1 out to the CUE. The CUE adds an eight-bit address to the signal and sends it to the computer as a command. If the computer accepts the command it returns

signals to the CUE that are processed by the CUE and sent to the C START as C and D signals. These signals are applied to the C START control logic and used to generate gate signals. Each time the computer is ready for another 12-bit word a gate signal is applied to one of the gate circuits and three binary coded switch positions (12-bit word) are gated out to the CUE. After the computer has received four 12-bit words from the C START via the CUE, it calls up a subroutine. If the subroutine is completed immediately, the computer sends a confirm signal to the C START. The confirm signal causes the execute logic to be reset and allows another execute signal to be processed. If the subroutine cannot be run immediately, or requires an extra length of time to run, the computer sends a SEAL signal to the C START. This prevents the control logic from accepting additional execute signals from the execute switch until the computer has completed the subroutine. As long as the SEAL signal is present, the control logic lights the SEAL lamp in the upper half of the execute switch pushbutton.

2-24. K START FUNCTIONS. (See figure 2-4.)

2-25. The K START module provides the means of generating digital data for the guidance computer. The data is in the form of five-bit words which represent one character each. The characters may be generated manually with a keyboard or automatically with a perforated tape reader. The Automatic or Manual Mode is selectable by the operator.

2-26. TAPE MODE.

2-27. In the Tape Mode of operation, the five-bit character words are read from an eight-level perforated tape reader. The reader delivers one 8-bit word to the K START and halts until it is commanded to read the next word. The K START delivers this word to the AGC, via the CUE, computer, and the DTCS. The computer receives two verify signals, one from the DTCS reply, and one from the Digital Test Monitor System (DTMS) reply. The computer compares the word received by the DTMS and the word transmitted from the K START, and generates a verify or non-verify signal. This signal is then delivered to the K START which displays the result of the comparison on the verify or the non-verify lamps.

2-28. A verify reply causes the tape reader to advance one character and deliver the next eight-bit word to the K START. In the event of a non-verify reply, the non-verify switch lamp is lighted, and further character entry is inhibited. However, the tape reader retains the capability of being indexed in either direction. Operation of the non-verify switch turns off the non-verify switch lamp and allows another character entry.

2-29. MANUAL MODE.

2-30. In the Manual Mode of operation, the five-bit character words are entered from a manually operated keyboard. The K START delivers a word to the AGC via the CUE, computer,

and the DTCS. The computer receives two verify signals. One of the signals is from the DTCS reply which drops the XEQ request and turns off the upper half of the XEQ display. The other signal is from the DTMS which releases the SEAL and turns off the lower half of the XEQ display. The computer then performs comparisons of the word transmitted from the AGC and the word transmitted from the K START. After the comparison the computer delivers a verify or non-verify signal to the K START which displays the results of the comparison on the verify or non-verify display. Operation of the non-verify switch turns off the non-verify switch lamp and allows character entry.

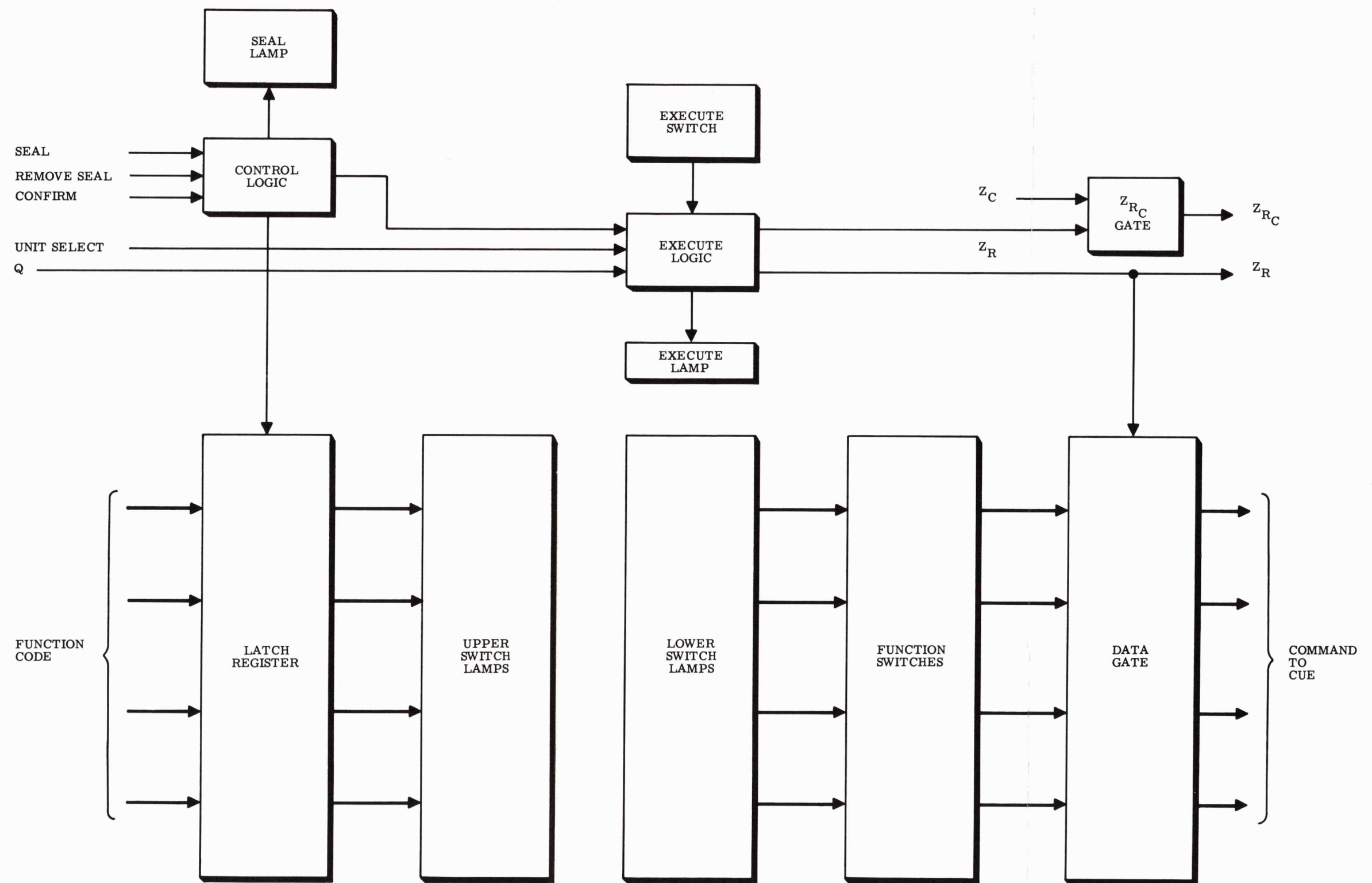
2-31. KEYBOARD.

2-32. Operation of a given key on the keyboard results in one of the following five-bit codes being sent to the CUE:

0 - 10000	VERB	- 10001
1 - 00001	NOUN	- 11111
2 - 00010	+	- 11010
3 - 00011	-	- 11011
4 - 00100	ENTER	- 11100
5 - 00101	CLEAR	- 11110
6 - 00110	RELEASE	- 11001
7 - 00111	ERROR RESET	- 10010
8 - 01000		
9 - 01001		

2-33. K START OPERATION.

2-34. The K START may be operated by either of the two previously described methods as a function of the operator selected mode. However, in either mode, the entry of a new character into the K START causes the K START to send an execute (Z_C) signal to the CUE and turn on the XEQ lamp. The K START data and the address are then transferred to the computer. Upon receipt of a valid verification reply from the computer, the upper half of the XEQ display turns off and the K START is SEALed, at which time the SEAL display lamp is turned on. Receipt of a verify from the computer releases the SEAL and causes the lower half of the SEAL display lamp to turn off. This action causes the verify lamp to turn on. If the second verify is not valid, the SEAL display lamp is turned off. This indicates a SEAL release. The non-verify reply switch lamp is turned on, and in the Automatic Mode the tape is not advanced. The non-verify lamp is turned off upon operation of the non-verify switch, thereby allowing character entry.



AM2-2-5

Figure 2-2. R START Module Block Diagram

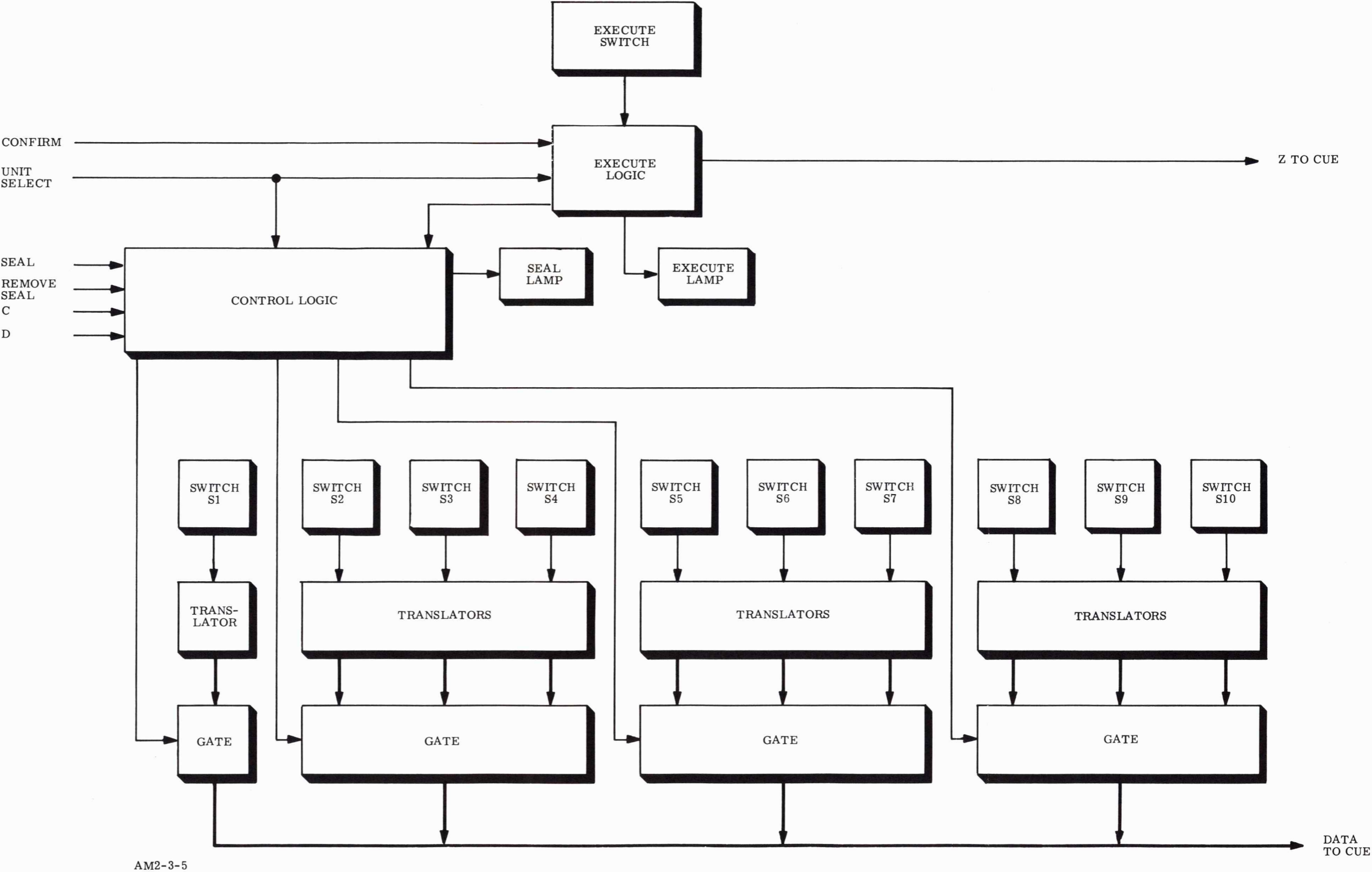


Figure 2-3. C START Module Block Diagram

(To be supplied)

Figure 2-4. K START Module Block Diagram

2-35. J-BOX FUNCTIONS.

2-36. All J-Boxes are connected in parallel to the CUE output and input signals. This causes the same signals to be present at each J-Box and develops the requirement of interpreting the signals at each J-Box. The unit select signals from the CUE are applied continuously to two select gates in each J-Box (figure 2-5). Group select signals also from the CUE are supplied to each J-Box. There are as many group select signals as there are select gates in all the J-Boxes. Therefore, one group select signal is applied to each select gate. When one of the group select signals is present, the select gate connected to that signal is enabled and the unit select signals are gated out to the START modules. Each of the unit select signals are sent to an individual START module. These signals cause the START modules to return data and control signals to the CUE via the J-Box that initiated the unit select. This is dependent upon the function code and control signals sent to the START module by the CUE via the same J-Box.

2-37. CUE FUNCTIONS.

2-38. The CUE may operate in one of four different modes. Three of the modes (Standby, Interrupt, and Maintenance) are selected automatically by the computer. The fourth mode of operation (Manual) is selected by the operator at the CUE control panel. Mode selection by the computer is accomplished by sending an external function code (EF) over the CUE input bus. The CUE interprets the code and applies signals to the control logic that switch the CUE to the appropriate mode. A general functional description of the CUE operation in each mode is described below.

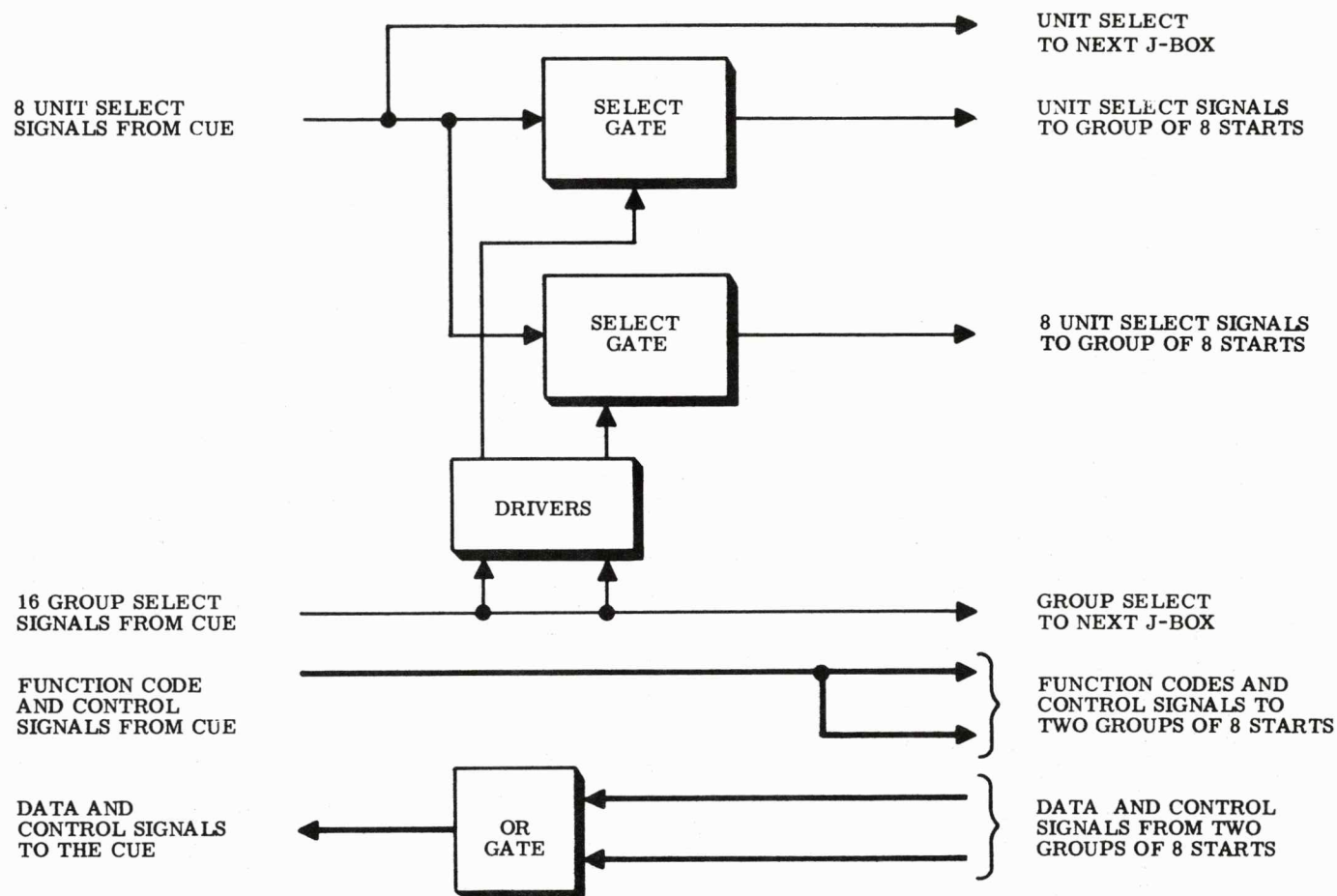
2-39. STANDBY MODE.

2-40. The Standby Mode of operation is selected and de-selected by the computer under program control. The Standby Mode can be selected by either a Master Clear signal or an external function code from the computer. When the CUE is in this mode, it will not transmit commands or receive data from the computer. When the computer is ready for normal operation, it sends the appropriate EF to the CUE to switch operation to the Interrupt Mode.

2-41. INTERRUPT MODE.

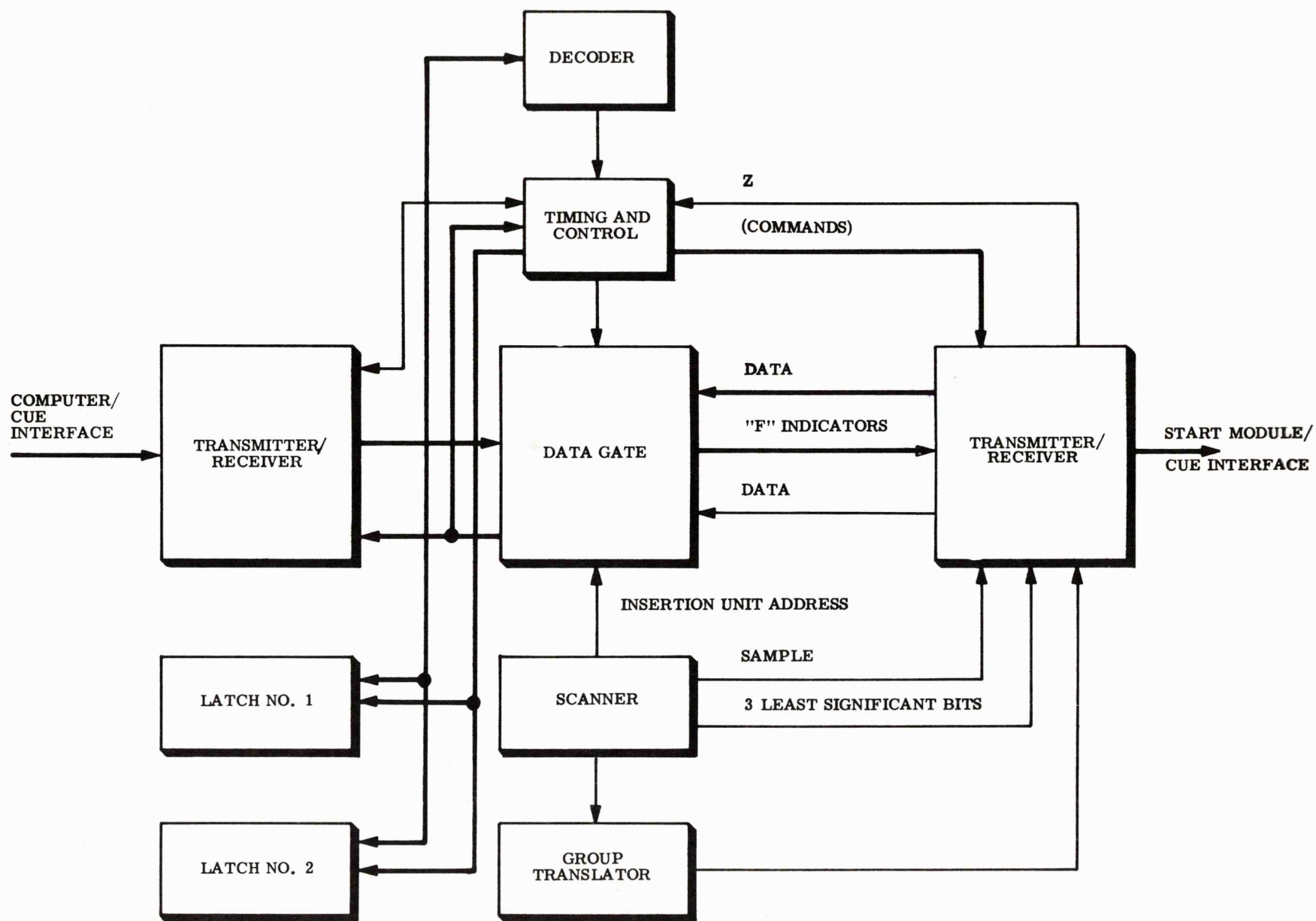
2-42. The Interrupt Mode is the normal working mode for the CUE. This mode allows the CUE to transfer commands from the START's to the computer.

2-43. INTERRUPT SIGNALS. The CUE requests access to the computer by generating interrupt signals. The interrupts are generated when execute signals and data are received from a START module. The CUE examines the Z signal and generates either a high priority (Interrupt 30) or a low priority (Interrupt 40) signal (figure 2-6). If the Z signal was received



AM2-4-5

Figure 2-5. J-Box Block Diagram



AM2-5-5

Figure 2-6. Communications Unit Executor Block Diagram

from an R START module, the CUE generates an Interrupt 30, or an Interrupt 40 if the Z signal was received from a C START or K START. Every time the CUE generates an interrupt it displays the address and function switch status of the START module that generated the Z signal on the CUE control panel.

2-44. DATA TRANSMISSION. Input commands to the CUE may be either one four-bit or four 12-bit words and a Z signal. If the input is from an R START module, it will be one 4-bit word and a Z signal. If the input is from a C START or K START, it will be four 12-bit words and a Z signal. The Z signal causes the CUE to generate an interrupt that is sent to the computer. The computer recognizes the interrupt and calls up the appropriate subroutine. This subroutine sends EF and Input Request signals to the CUE.

2-45. The Input Request signal initiates the timing and control logic. This logic generates an Input Ready signal and transmits it and the data to the computer. The first 12-bit word of data contains four data bits and the eight-bit address transferred from the address scanner. The next three words each contain 12 bits of data. The input of data to the computer proceeds one word at a time until the last word has been transmitted.

2-46. ADDRESSING. Each insertion unit in the data entry equipment has a unique eight-bit address. This eight-bit address allows a maximum of 256_{10} insert units to be addressed or selected by one CUE. The CUE services low groups of eight data function terminals connected in parallel. These two groups are assigned patch 0 and 1 for addressing purposes.

a. Address Scanner. The address scanner sequentially scans the unique address of every insertion unit for a signal requesting access (Z signal). The DSU stops the address scanner at the insertion unit's address at the same time it sends an interrupt to the computer. The address scanner provides the computer with the eight-bit address. This address is also gated to the group and unit select logic. Initially, the address scanner logic is enabled by the selection of the Interrupt Mode. The scanner is also enabled after an interrupt has been recognized and processed.

b. Group and Unit Select. The group select logic determines which of the possible 16 data junction terminals to reference when a particular insertion unit is to be addressed or selected. The unit select logic selects one of the 16 possible insertion units connected to each data junction terminal.

2-47. COMPUTER RESPONSES. The computer communicates with the data scanner unit and the data entry equipment using 12-bit external function instructions. These instructions (EF codes) are located in the computer's control program. The decoder interprets these EF codes and generates one of eight commands to the control logic. The control logic enables the other sections of the CUE to perform the correct operations. Table 2-1 contains the external function instructions for the data entry equipment.

2-48. A Status Request instruction, as its name implies, requests the status of the equipment. The CUE gates the status response to the computer. Table 2-2 contains the status response codes for the data entry equipment.

Table 2-1. External Function Instructions

EF CODES	DESCRIPTION
<p>NOTE</p> <p>X can be only 1 or 2 depending on the number of data scanner units in the system.</p>	
37X0	Status Request
37X1	SEAL
37X2	Standby Mode
37X3	Interrupt Mode
37X4	Remove SEAL
37X5	Compare
37X6	Input
37X7	Maintenance Mode

Table 2-2. Status Response Codes

STATUS RESPONSE CODES	DESCRIPTION
0000	Standby Mode
0001	Interrupt Mode
0002	Maintenance Mode
5001	Scanner stopped; indicates a high-priority interrupt
6001	Scanner stopped; indicates a low-priority interrupt

2-49. Inputs. The computer selects the data entry equipment for input by using the input instruction. It is followed by one or four INA instructions depending on the type of insertion unit transmitting data. The INA instruction is used in the Input Mode only to gate the data into the computer's exchange register for further action. Each INA instruction allows one 12-bit word to be transmitted to the computer.

2-50. Outputs. The input instruction gates the data into the computer from the insertion units. The computer transmits this data to the remote device. The data is processed by the remote device and a response is returned to the computer. The computer transfers this response using the output instructions, and various other commands to the data entry equipment. This confirms responses to the original test commands.

2-51. The computer selects the data entry equipment by using either the SEAL (37X1) or the remove SEAL (37X4) instruction. The SEAL instruction is used to gate the insertion unit address and the four response bits to the insertion unit as a confirmation of the initial test completed in the remote device. An OTA instruction follows the SEAL instruction. The OTA instruction is used (in the Output Mode only) to transmit data out of the exchange register of the computer. This instruction gates the data to the CUE.

2-52. The CUE translates the four response bits and sends a confirm signal and a SEAL command to the insertion unit. A confirm signal causes the execute lamp on the control panel of the insertion unit to extinguish. The insertion unit is again able to transmit data when the lamp is extinguished. A response is not returned to the computer if the remote device takes too much time in processing the data. The computer issues the SEAL instruction followed by the OTA instruction to the CUE. The CUE translates the four bits of response as a SEAL command from the computer. The SEAL command is gated to the insertion unit by the CUE. This command isolates or SEALs that particular insertion unit from the system. The SEAL lamp on the control panel of the insertion unit lights when the unit is placed in the SEAL condition. The insertion unit is unable to communicate with the computer or any other portion of the data entry equipment until the computer issues a remove SEAL instruction. The remove SEAL instruction is used in two ways. It is used to gate a confirming response to the insertion unit the same as for the SEAL instruction or to remove the SEAL condition in a particular insertion unit. To remove the SEAL condition, the computer, at any time, issues the remove SEAL instruction, even while the CUE is sequentially scanning the insertion unit addresses. An OTA instruction follows this instruction. The eight-bit address of the insertion unit follows the OTA instruction. The computer under program control must provide the address of the insertion unit because the CUE does not retain the address of the SEALED insertion unit. The CUE translates the instruction and data (address and response) and generates a remove SEAL signal to the insertion unit. The SEAL lamp on the control panel of

the insertion unit extinguishes when the unit receives this signal, indicating that the insertion unit is again able to transmit data.

2-53. Error Detection. The logic of the CUE contains compare circuitry by which the data is checked for errors occurring during transmission. The compare instruction is an optional instruction. It is used only if the original test data is of a critical nature. The compare instruction, generated by the computer, enables this circuitry to check the address portion of the data for errors. The data (eight-bit address and four data bits) are transmitted to the computer by the input and INA instructions. If the compare instruction follows these instructions, the computer gates the address back to the CUE. The compare logic compares the eight-bit address, located in the address scanner, with the eight-bit address gated from the computer. If the addresses do not compare, the computer halts with an error indication.

2-54. MAINTENANCE MODE.

2-55. The Maintenance Mode of operation is used in an on-line capacity to check the data transmitted from the computer to the data insertion units for errors occurring during transmission. The eight-bit address and four data bits are also displayed on the control panel of the CUE. The computer initiates this mode using a Maintenance Mode (37X7) instruction.

2-56. ADDRESSING. The control program of the computer must provide the eight-bit address and the four data bits in this mode of operation. The computer generates an Information Ready signal and transmits it and the eight-bit address and the four data bits to the CUE. The data and address are displayed on the START ADDRESS and FUNCTION SWITCH STATUS indicators and transferred to the group and unit select logic. The Information Ready signal initiates the timing logic. This logic enables the group and unit select to reference the correct data insertion unit.

2-57. DATA TRANSMISSION. The transmission of data is a one-way transmission from the computer through the CUE to the addressed data insertion unit. The data is displayed on the control panel of the START module for operator evaluation.

2-58. MANUAL MODE.

2-59. The Manual Mode provides the data entry equipment with a checkout system for maintenance purposes. It is manually initiated at the control panel of the CUE.

2-60. ADDRESSING. The operator at the control panel of the CUE controls the selection of the insertion units. Initially, the operator selects the START ADDRESS switches to correspond to the desired insertion unit's address. Depressing the XEQ pushbutton activates the unit. The group and unit select logic interprets the eight-bit address (from the switches) and

references the correct insertion unit if there is a preprogrammed Input Request signal from the computer.

2-61. DATA TRANSMISSION. The execute signal enables the data content of the addressed insertion unit to be transmitted to the CUE. The timing logic generates and transmits an Input Ready signal to the computer. The control logic enables the four bits of data and the eight-bit address (from the switches) to be transmitted to the computer. The computer, in turn, generates an Information Ready signal which is transmitted with the four data bits and the eight-bit address back to the CUE. The data and address are displayed on the START ADDRESS and FUNCTION SWITCH STATUS indicators.

2-62. CUE DESCRIPTION.

2-63. The CUE consists of data gates, scanner, group translators, control logic, decoder logic and transmit/receive circuits (see figure 2-6). The CUE has four modes of operation: Interrupt, Maintenance, Standby, and Manual. The Interrupt Mode is the normal mode of operation. The Interrupt, Standby, or Maintenance Modes may be selected automatically by the computer. The Manual Mode must be selected with a switch on the CUE control panel. A detailed block diagram description of the CUE operation in each of the four modes is given below.

2-64. STANDBY MODE.

2-65. This mode of operation is selected by the computer under program control. When a $37X2_g$ instruction is applied to the CUE by the computer, it is sent to the decoder logic. This logic interprets the instruction as a request to select the Standby Mode of operation, and sends the appropriate signal to the control logic. These signals cause the control logic to generate the necessary signals required to disable the data transfer operation of the CUE. In this mode, execute (Z) signals will not cause the CUE to generate interrupt signals, nor will data be transferred to or from any of the equipment. The $37X2_g$ instruction is generated by the computer as the result of a Master Clear signal. When the computer again requires inputs from the CUE, a new instruction, which is generated by the computer program, will be sent to the CUE. This instruction will be decoded similarly to the standby instruction, and the CUE will be switched into the desired mode of operation.

2-66. INTERRUPT MODE.

2-67. The Interrupt Mode is selected by a $37X3_g$ instruction from the computer. This instruction causes the control logic to send out the appropriate signals to switch the CUE circuits into the configuration described below.

2-68. In the Interrupt Mode, 100-kc pulses are applied to a two-stage gray code counter by the clock. The output of one stage of the gray code counter is applied to an eight-stage binary counter. The output of the other stage is sent to the unit select logic as a sample signal. The eight-stage binary counter counts sequentially from 0 to 255. On the 256th count, the counter is reset to 0, and the count is repeated. A signal from each stage is sent to the select logic as an eight-bit parallel binary signal. The three least significant bits ($2^0 - 2^2$) are applied to the unit select logic. The five most significant bits ($2^3 - 2^7$) are applied to the group select logic.

2-69. The group select logic decodes the five input bits into 16 group select signals. These signals are sent to two groups of eight J-Boxes (patch 0 and patch 1). The group select signals are repeated twice (once for each 128 START module locations) during each complete scan of the 256 START module locations. After the first 128 START module locations have been scanned, the group select logic sends a patch select signal to the unit select logic. After the next 128 START module locations have been scanned, the patch select signal is removed, and the cycle is repeated.

2-70. The unit select logic decodes the three least significant bits of the eight-bit count into eight, unit select signals. The unit select signals are gated out of the unit select logic onto one of two 8-channel control buses by the sample pulse from the gray code counter. If a patch select signal is not received from the group select logic, the unit select signals will be gated onto the patch 0 control bus. If a patch select signal is present, the signals will be gated out on the patch 1 bus.

2-71. The group select signals are applied to both groups of eight J-Boxes simultaneously. However, the unit select signals are applied to only one group at a time. When the group select and unit select signals are combined by a J-Box, they interrogate a START module. If the module requests data entry, the sequence of events described below occur.

2-72. If the START module was an R START, a Z_R signal will be applied to the receiver. If other R START modules have pending requests for data entry, a continuous Z_{RC} signal will also be applied to the receiver. These two signals are sent to the interrupt logic. The Z_R signal will cause the interrupt logic to send an Interrupt 30 signal to the computer when a timing signal is received from the control logic. The Z_C signals, sent to the CUE when a C START is selected, cause the interrupt logic to react by sending an Interrupt 40 signal to the computer. This is accomplished by using the interrupt timing signal from the control logic just as the Z_R did. The Z_{RC} signal prevents the interrupt logic from responding to Z_C signals until all R START modules have been serviced.

2-73. Every time a Z signal is received by the CUE, a four-bit data word is also received. The four-bit word could be the entire data from an R START module or the first word from a C START or K START. In either case, the sequence of events described below occur.

2-74. The Z signal causes the eight-stage binary counter to stop counting and sends the eight-bit count to the data logic to be added to the four-bit data word. The Z signal also causes the interrupt logic to send an Interrupt 30 or 40 to the computer. The computer recognizes the interrupt and sends a function code to the CUE receiver along with a Function Ready signal. This enables the CUE to receive further instructions from the computer. The CUE indicates reception of the instruction by generating an Output Resume signal from the Function Ready signal with the timing logic. The computer verifies that the CUE has properly interpreted the select instruction by reception of the Output Resume signal. It then drops the Function Ready signal which causes the CUE to drop the Output Resume signal since it is generated by the Function Ready signal.

2-75. The computer then sends an Input Request signal to the CUE. The CUE responds by applying the eight-bit scan address and four-bit data to the computer through the CUE transmitter. The CUE then generates an Input Ready signal from the computer Input Request signal with the timing logic and sends it to the computer. This causes the computer to accept the data. If the data was from a C START or K START, the computer sends another Input Request signal. This signal performs the functions covered above and one additional function. The Input Request signals cause the timing logic to send signals to the control logic which generates C and D signals. These signals are sent to the C or K START module that generated the Z signal. The C or K START module uses these signals to sequentially gate a 12-bit word to the CUE data logic every time an Input Request signal is received by the CUE. This continues until three Input Requests have been received. When the last word has been sent to the computer, the data transfer sequence has been completed, and the CUE functionally disconnects from the computer.

2-76. After the computer has received all of the input data, it performs the required program controlled operations. After these operations are completed, it sends an Information Ready signal to the CUE along with the CUE select function code (37XX). This causes the CUE timing logic to generate an Output Resume signal from the Input Ready signal and send it to the computer. The computer responds by dropping the Input Ready signal. This causes the CUE to drop the Output Resume signal since it is generated by the Input Ready signal. The computer will now send data or function codes to the CUE depending upon the results of the computer operation.

2-77. If the computer completes processing of the command immediately it sends a confirm function code to the CUE. This code is interpreted by the decoder which causes the control

logic to generate and transmit a confirm signal to the START modules. This signal allows the R START modules to accept a four-bit data word stored in Latch No. 2 by the data logic. It also resets the START that generated the command causing the Z signal and input data from the START to drop.

2-78. If the computer cannot complete processing the command immediately, it will send a SEAL function code to the CUE. A SEAL function code is interpreted the same as the confirm. However, it causes the control logic to generate a SEAL signal that is sent to the START that generated the command and causes the same results at the CUE as the confirm signal did. If the computer is unable to process the command according to program it will send a Maintenance Mode function code to the CUE. The decoder interprets this command and sends signals to the control logic that automatically switch the CUE to the Maintenance Mode.

2-79. MAINTENANCE MODE.

2-80. The Maintenance Mode is selected by a $37X7_8$ instruction from the computer. This instruction is decoded and sent to the control logic. The control logic inhibits the scan and lights the indicators on the CUE display panel with input and output data. The input data consists of four data bits from the data logic, plus the scan address from the binary counter. The CUE output to the computer (which consisted of only four data bits) sets Latch No. 1 with these four bits and eight bits from the binary counter. The contents of Latch No. 1 is displayed on the CUE control panel ADDRESS and FUNCTION SWITCH STATUS indicators. The 12-bit data found to be invalid or incorrectly processed by the computer is sent to Latch No. 1 and displayed on the CUE display panel TRANSMISSION and STATUS RESPONSE indicators.

2-81. MANUAL MODE.

2-82. The Manual Mode is selected manually by the operator through a manual/automatic switch on the CUE control panel. This switch disables the CUE scanner circuits. The operator may now choose a START module for operation by setting a code into START ADDRESS switches on the CUE control panel. These switches send an eight-bit signal to the data logic and the unit and group select logic. The unit and group select logic process the eight-bit manual input in a similar manner to the binary counter input. An XEQ switch on the CUE control panel sends a signal to the unit select logic that performs the same function as the sample signal from the gray code counter. When the execute switch is depressed, the CUE operates in much the same manner as described in the Interrupt Mode except for two main differences. The module scan does not advance, and the computer returns the word transmitted by the CUE. The CUE sets this word into Latch No. 2 for display on the TRANSMISSION and STATUS RESPONSE indicators and displays the word sent out to the computer on the ADDRESS and FUNCTION SWITCH STATUS indicators.

2-83. DATA PROCESSING EQUIPMENT.

2-84. The data processing equipment consists of a stored-program, high-speed, single-address, parallel operation, modular computer. The computer (part of the Computer Complex) accepts digital information, processes the information according to preprogrammed logical sequences and presents the resultant data to output terminals for transmission to the on-board equipment.

2-85. The command computer time is occupied by two separate types of operations that may be described as nonpriority and priority operations. The nonpriority operation is controlled by the executive program which maintains a logic flow of low-priority (non-time critical) processing tasks. These tasks serve the dual purpose of performing important maintenance and housekeeping functions while efficiently using the computer's spare time between priority operations. The priority operation may be best described as the handling of test operation request interrupts from the CUE. The priority operation is controlled by interrupt handling routines. The various interrupts are the key to the priority operation. The priority operation consists of processing these interrupts to determine what action is necessary to satisfy a test operation request.

2-86. NONPRIORITY OPERATION.

2-87. The nonpriority computer operation consists of two main operations that are best termed initialization and housekeeping. During the initialization operation, normal Command Equipment operation is prevented while the computer receives parameters that are arranged into tables. The tables are then assembled, and the computer selects the operating status for external equipment. After this is accomplished, normal operation of the Command Equipment group is enabled, and the computer breaks into the housekeeping operation. During this operation, the computer systematically performs low-priority information transfers and real-time maintenance checks. The housekeeping operation may be temporarily halted at any time by interrupts from the DTVC or CUE. When this occurs, the computer breaks into a priority operation.

2-88. INITIALIZATION OPERATION. The initialization operation begins when punched cards containing table parameters are read into the computer. The computer assembles these parameters into three unique tables (according to program control) and stores them in allocated memory locations. These tables are termed clock table, R START table, and C START table. The clock table is associated with timed interrupts to the computer from the Tape Recorder/Computer Time Decoder and Search Control. The clock table is used to interpret these interrupts, call up the subroutine requiring attention, and set the clock for the next controlled interrupt. The R START table is associated with the Interrupt 30 from the CUE.

This table is used to associate each R START module with a group, baseplate, and module of the Receiver-Decoder. The R START table is also used to control SEAL requests or reference an appropriate preroutine address. Additional information in respect to function switch status of the current R START module is added to the data determined by the R START table. The C START table performs much the same function as the R START table in the respect that it associates each C START module with a group, baseplate, and module of the Receiver-Decoder. The C START table also controls SEAL request or references appropriate preroutine memory address for special analog functions. After the tables have been assembled, the computer initializes all equipments that are used during normal operation. This is accomplished by verifying that all peripheral equipments are ready and selecting the proper operating mode for each. If this cannot be accomplished, the computer types out an appropriate message and halts. After equipment initialization is completed, the computer sets all programmed flags to their normal state, releases the lockout interrupt, and begins the housekeeping operation.

2-89. HOUSEKEEPING OPERATION. The housekeeping operation is actually a wait operation which efficiently uses the computer time to perform nonpriority tasks while the computer is waiting for priority operation requests. During this operation, the computer may perform a number of various operations that are designated by the program. Examples of these operations are the transfer of information between computers through shared memory or the performance of routine maintenance checks. The housekeeping operation can be interrupted at any time to perform priority operations. After the priority operation is completed, the housekeeping operation begins again at the point where the interruption occurred.

2-90. PRIORITY OPERATION.

2-91. A priority operation is the functioning of the computer as a translator interface between the CUE and the DTCS. This operation begins as the result of an interrupt received from the DTVC or CUE (figure 2-7). After an interrupt occurs, the computer receives an input from the START module that generated the interrupt. The computer reads the START module input and generates one or more commands to be sent to DTVC, or beings to perform a subroutine. After the DTVC transmits the command and performs a validity check, it returns a Check Status Reply (CSR) to the computer. The computer then uses the CSR to determine the success or failure of the transmission. If the transmission was successful, the START module that originated the command is notified by a confirm or a SEAL from the computer. The confirm allows the START to enter new commands to the computer. The SEAL prevents further action from being initiated by that particular START until the preset command has been executed. If three transmissions of the command are unsuccessful, the computer will notify the CUE and diagnose the malfunction.

2-92. INTERRUPTS. The computer is switched from housekeeping operation by interrupt signals from the external command equipment. During normal operation, these interrupts consist of high priority (Interrupt 30) and low priority (Interrupt 40) signals. The Interrupt 30 signal is applied to the computer by either an R START module or a DTVC. The Interrupt 40 signal is applied to the computer by a C START, K START, DTVC, or the real-time clock. Both interrupts cause the computer to respond in much the same manner. However, the computer will always respond to all Interrupt 30 signals before it will answer an Interrupt 40.

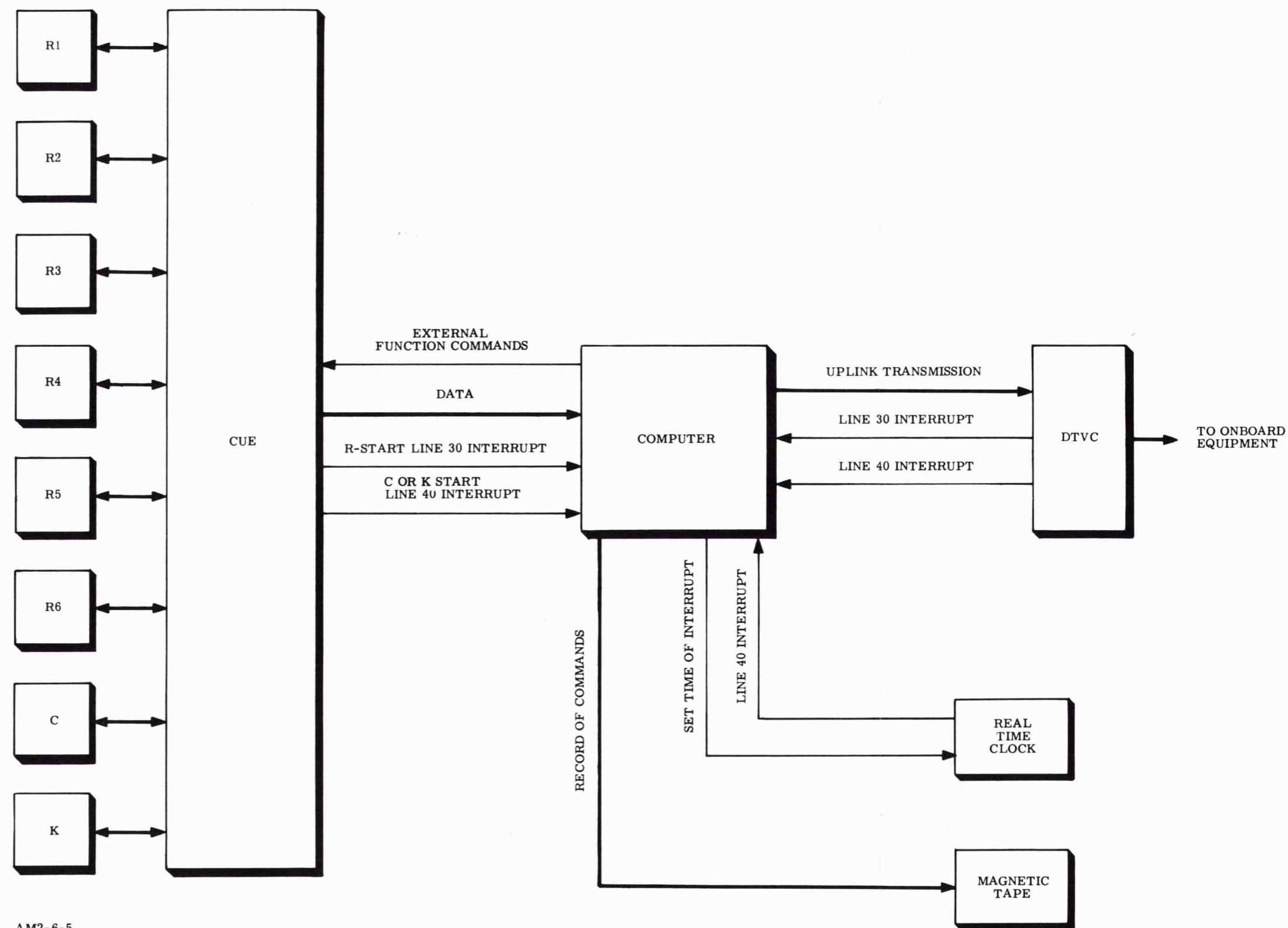
2-93. When an Interrupt 30 is sent to the computer, the first action performed is to save the accumulator contents so it may be used when housekeeping operations are resumed by the computer. Then the I flag is cleared so that the housekeeping operation may resume at the point of interrupt. Finally, the computer checks a series of routing flags to determine if the DTVC generated the interrupt. If none of the routing flags are set, the computer checks the status of the CUE. If the CUE did not generate the interrupt, the computer assumes the interest was generated by the DTVC and starts a priority operation by initiating a DTVC routine.

2-94. When an Interrupt 40 is sent to the computer, it reacts in much the same way as when the Interrupt 30 was received. The only difference is a few additional steps performed to determine if the interrupt came from the Tape Recorder/Computer Time Decoder and Search Control. After the computer has determined which external unit has generated an interrupt, it will start a priority operation which may be one of several routines. The routine will be determined by the equipment that generated the interrupt.

2-95. R START ROUTINE. The R START routine causes the computer to accept a coded R START command word from the CUE, interpret the command word, and transmit commands to the DTCS via the DTVC. This is accomplished through the sequence of computer operations described in the subsequent paragraphs.

2-96. After the computer has determined that the Interrupt 30 was received from the CUE, the computer control is transferred to the R START routine. This causes the computer to select the CUE for an input. When one 13-bit word is received by the computer, the CUE is de-selected. The upper eight bits of the 13-bit word contain the R START module address. The eight-bit address is applied to the R START table, and will be used to interpret them as described below:

- a. Bit 13 denotes an analog trigger. When this bit is present, the remaining bits will reference a table of parameters. This table will translate these bits as a command to initiate or terminate the output of a specific analog output. Depending upon the bit configuration of the remaining 12 bits, the table may or may not generate a relay command.



AM2-6-5

Figure 2-7. Command Equipment Functional Block Diagram

b. Bit 12 denotes that the R START is being used to call up a subroutine. In this case bit 13 will always be "0" and the remaining bits will contain the number of the subroutine.

c. Bit 11 denotes the DTVC to be used for transmitting the message. If bit 10 is a "1" the command will be transmitted by DTVC No. 2. If bit 10 is a "0" the command will be transmitted by DTVC No. 1.

d. Bits 8, 9, and 10 are interpreted as an octal code. Octal numbers 1 through 5 select groups 1 through 4 and the airborne computer respectively.

e. Bits 5, 6, and 7 are interpreted as an octal code. Octal numbers 0 through 7 select baseplates 1 through 8 respectively.

f. Bits 3 and 4 are interpreted as an octal code. Octal numbers 0 through 3 select modules 1 through 4 respectively.

g. Bits 1 and 2 are interpreted as an octal code. Octal numbers 0 through 3 select relay subgroups A through D respectively.

2-97. Bits 1 through 10 are used to generate the command signal to the DTCS. After the command is generated the computer performs one or two different operations, depending on whether the command required relay action only or is for a special function.

2-98. If a command generated by the R START module requires relay action only, the computer checks the DTVC for availability. If the DTVC is available for transmission, the command words are set into the output buffer and control is transferred to the DTVC output routine. If the DTVC is not available, the computer begins nonpriority operation until the DTVC is available. In either case, the appropriate routing flags are set to the proper state.

2-99. If a command generated by the R START module is for a special function, the required special subroutine is called up from memory and recorded on magnetic tape. The computer then returns the CUE to Interrupt Mode and clears the interrupt lockout logic. It then replaces the housekeeping operation with the special subroutine. The computer then runs the special subroutine and answers interrupts just as though it were performing the housekeeping operation. When the special subroutine has been completed, the computer returns control to the R START routine which returns the computer to normal housekeeping operations.

2-100. C START ROUTINE. The C START routine causes the computer to accept four coded command words from the CUE, interpret the command words, and transmit commands to the DTCS via the DTVC. The C START command words will contain up to ten decimal digits of parametric information to add to the uplift commands. The parametric information is added to one of three general subroutines that are called up by the first C START input word. The subroutine can generate commands to apply stimuli and control relay closure sequence in the DTCS. This is accomplished through the sequence of computer operation described below.

2-101. After the computer has determined that the Interrupt 40 was received from the CUE, the computer control is transferred to the C START routine. This routine causes the computer to store the contents of the A and Q register and input four 13-bit words from the CUE. The upper 9 bits of the first word contain the C START module address and K START flag. First the computer applies bits 3 through 13 of word one to the C START table which interprets them as described below:

- a. Bit 13 is a flag that denotes the origin of the input message. If bit 13 is a "1," the origin was a K START module and computer control is shifted to the K START routine. If bit 13 is a "0," the origin was a C START module and computer operation continues as described below.
- b. Bit 12 denotes that the C START command is to be used to call up a subroutine. The subroutine may be used to control relay sequence or generate an uplink control program.
- c. Bit 11 denotes the DTVC to be used to transmit the command to the DTCS. If bit 11 is a "1," the command will be transmitted via DTVC No. 2. If bit 11 is a "0," the command will be transmitted via DTVC No. 1.
- d. Bits 8, 9, and 10 are interpreted as octal codes. Octal numbers 1 through 5 select groups 1 through 4 and the airborne computer respectively.
- e. Bits 5, 6, and 7 are interpreted as octal code. Octal numbers 0 through 7 select baseplates 1 through 8 respectively.
- f. Bits 3 and 4 are interpreted as octal code. Octal numbers 0 through 3 select modules 1 through 4 respectively.

2-102. If the C START input is for a normal function, the computer generates commands using the on-board addresses and other data contained in the input words. The computer then checks DTVC for availability. If the DTVC is not available for transmission, the computer returns to housekeeping operations until the DTVC is available. If the DTVC is ready to transmit, the command words are placed in the output buffer and computer control is transferred to the DTVC routine. In either case, appropriate routing flags are set to the proper state.

2-103. If the C START input is for a special function, the computer derives the test area equipment address and appropriate preroutine from the C START table. The computer then heads the test area address into the A register, and makes a return jump to the preroutine. After the preroutine has run, the A register contains the address of the routine that will perform the special function. This address is placed in the clock table. Then the initial interrupt time is calculated, and also placed in the clock table opposite the address. If this is the first entry in the clock table, the computer requests the first interrupt from the clock. Thereafter, this condition is handled by the clock servicing routine. The command is recorded on magnetic tape, and the CUE Write Mode is selected. This releases the scanner

and returns the CUE to Interrupt Mode. After this, the computer returns to normal house-keeping operations.

2-104. K START ROUTINE. The computer switches to this routine from a C START routine. This routine causes the computer to interpret K START inputs, and generates command signals to be sent to the airborne computer. The computer receives four 13-bit words from the K START module. Word one contains the unique address of the K START module and a flag bit that indicates whether the input originated at the K START keyboard or paper tape reader. Words three and four are dummy words to make the K START input format compatible with the C START input.

2-105. The computer uses only two bits of the first word. Bit 12 denotes that the input words are from the K START module. Therefore bit 12 has been examined and found to be a "1" before the computer calls up the K START routine. The remaining bit used is bit 11 which indicates the DTVC to be used to transmit the command. If bit 11 is a "1," DTVC No. 2 is selected. If bit 11 is a "0," DTVC No. 1 is selected. Bit 1 of word one is a parity bit for paper tape inputs. The computer performs a parity check on the input paper tape data, and notifies the K START via the CUE if an error is detected. If no error is detected, the input data bits are gated into the command word. The command is then loaded into the A and Q registers to be stored by the output control routine.

2-106. DTVC ROUTINE. The purpose of this routine is to transmit commands to the DTCS via a DTVC. This routine causes the computer to send Load Buffer Memory (LBM) words and Execute Buffer Memory (EBM) words to the DTVC for transmission. CSR words are received from the DTCS by the DTVC. The CSR words cause the DTVC to send an Interrupt 30 to the computer if the transmission was successful, and an Interrupt 40 if the transmission was unsuccessful. The DTVC will not transmit a command until the CSR of a previous command has been received.

2-107. The computer determines which DTVC is to be used to transmit from the START input, then stores the command in a rotating table. This table is large enough to control the largest backlog of commands anticipated. The computer also stores the first word from the CUE and the previous function switch settings in the table. These are required in the event the transmission fails. In this case, the CUE word and the fail CSR word will be sent to the CUE maintenance panel, and the previous function switch settings will be sent to the requesting START module. After the command has been stored, the computer checks the DTVC status. If the DTVC is not busy the computer moves data from the rotating table to the output block for transmission to the DTCS. After transmission, the computer converts the command from a Load DTCS Buffer Memory to an Execute DTCS Buffer Memory. When the

Input/Output (I/O) Module buffer interrupt indicates the LBM has been transmitted, the computer will allow the EBM to be transmitted. When the I/O Module indicates the EBM has been transmitted, the computer will select the DTVC to recognize the CSR word and generate a high- or low-priority interrupt to indicate success or failure of the transmission. The computer performs interrupt operations between the steps explained above to make efficient use of time required for the actual transmission. Success or failure of the transmission is determined by the DTVC. After reception of the CSR, the DTVC will generate an Interrupt 30 or 40 depending on the success or failure of the transmission. If the transmission has been a failure, an Interrupt 40 will be generated and the CSR will be inputted to the computer. The computer will check to determine if this is the third failure for this command. If it is, the computer will call up a maintenance routine. If not, transmission will be tried again. If an Interrupt 30 is generated by the DTVC indicating success of transmission, the computer will release the CUE to scan. The computer will also send a function code to the START module that originated the command to light the upper half of the function switch pushbuttons. The computer then checks the rotating table for a backlog of commands. If a backlog exists, the DTVC routine will be called up. If a backlog does not exist, the DTVC will be set to "not busy."

2-108. CLOCK SERVICING ROUTINE. The purpose of this routine is to maintain a check on the special function routines. This is accomplished with clock interrupts which assure transfer of these routines at the appropriate time.

2-109. When the computer transfers control to the clock servicing routine, time is inputted from the real-time decoder. The computer applies this time to the clock table to find the routine that requires attention. If this function has output its last iteration, the computer clears this routine from the clock table and returns to normal housekeeping operation. If the routine is still available to be called, the computer updates the clock table and sets the clock for the next interrupt. Then it makes a return jump to the special subroutine that requires attention. After running the special subroutine, the computer checks to determine if the last iteration has been outputted for this function. If this was the last iteration, the routine is made unavailable for the next "call." The computer then checks the DTVC for availability. If the DTVC is not available for transmission, the computer returns to normal housekeeping operations. If the DTVC is available, the contents of the special routine storage locations are transferred into the output buffer, and control is transferred to the DTVC output routine. In either case, the computer sets the appropriate routing flags to their proper positions.

2-110. EXIT ROUTINE. The purpose of this routine is to return the computer operation to the point in the housekeeping routine where the interrupt occurred.

2-111. After the last required transmission is complete the computer clears the E (error flag). If an interrupt has occurred during transmission of a command, the computer transfers control to the appropriate routine. (The clock servicing routine has first priority in this return.) If there are no routines that require processing, the I (interrupt) flag is checked. Then the computer sets the accumulator with the housekeeping data that was present when the interrupt occurred. Finally, the computer clears the interrupt lockout and makes a return jump to the housekeeping routine.

2-112. SPECIAL SUBROUTINES. The following is a general description of special subroutines and functions that may be called up by the computer as the result of commands from the CUE requesting special functions.

2-113. Analog Routines. The purpose of the analog routine is to control housekeeping operations for the analog generators. This routine causes the computer to save and restore the banks, format the analog stimuli for the DTCS, and perform any of the bias and amplitude corrections required. Any one of four analog routines can be set to call up any one of its slave analog generator routines. Before the computer exits from this routine, the requested command words are stored in the output area.

2-114. The sine-wave generator routine is an example of an analog routine. This routine causes the computer to generate a digital sine wave output with a maximum absolute value of 255 counts. This routine can be used to generate other periodic functions which are symmetrical about the zero-crossing (disregarding linear bias). Each type of function requires a table that must contain the number of points needed to describe one quarter of the desired wave for the lowest frequency desired. In the case of a sine wave, one quarter of a 0.1 cps cycle (with an iteration rate of 250 IPS) is 625 points. The computer will scan up and down the table according to the desired frequency for the sine wave. The number of points between each pickup is equal to the frequency in tenths of cycles per second since the table is based on a frequency of 0.1 cps. Each time that the scan is reversed around the lower extreme the sign of the output is inverted since this is the zero crossing end of the table.

2-115. Preroutine. The purpose of the preroutine is to allow the computer to evaluate the formatted CUE words and initialize the actual special purpose subroutines. This allows the computer the flexibility of making minor format or calling procedure changes when needed while maintaining fixed subroutines. Each preroutine varies with the function for which it is intended, but all are in a common form. When a preroutine takes control of the computer, the A register is set to the test area equipment address to which the output will be transmitted. The CUE input words are evaluated as required, and parameters are set into the special purpose routine. The computer then loads the address of the referenced special routine into the A register. The following sine preroutine is a typical case.

2-116. The sine preroutine will set any analog routine to call up a sine-wave generator sub-routine. Inputs to this routine are as follows:

- a. The A register contains the on-board equipment address.
- b. C-INPUT +1 through C-INPUT +3 contains the BCD C START information.

2-117. The output of the routine is the address of the assigned analog routine in the A register. Format of the three BCD words is as follows:

- a. Word 1 contains the frequency format XX.X cps. The frequency range is 00.1 to 250 cps.
- b. Word 2 contains the zero-to-peak amplitude format X.XX volts. The voltage range is 0.00 to 5.00 volts.
- c. Word 3 contains the number of cycles desired format XXX. The cycle range is 000 to 999 cycles.

2-118. Error Routine. This routine informs the CUE maintenance panel and the recording media of a DTVC-error transmission. The computer relinquishes control to this routine after three unsuccessful attempts are made to transmit data. This routine causes the computer to attempt another transmission and wait for the CSR return. The computer sends a function code to the CUE to select the Maintenance Mode. When the CSR is received, the computer sends it to the CUE along with the problem word for display on the maintenance panel. The computer then sets the E (error) flag to control lighting of the START function switch pushbuttons and selects one of the following as the appropriate word message:

- a. Transmission error.
- b. Group decode error.
- c. Baseplate decode error.
- d. Buffer busy decode error.
- e. Module decode error.
- f. Subgroup decode error.
- g. LBM/EXC buffer decode error.
- h. Load buffer decode error.
- i. DTVC noise excessive.
- j. Illegal BCD SET or C START.
- k. Interrupt failure.

2-119. The computer then places the message in the output storage to be written on magnetic tape by the DTVC routine. After this has been accomplished, the computer transfers control back to the DTVC routine. If the errors are of the type that require operator intervention, the appropriate message is typed out on the on-line typewriter and computer operation is halted.

2-120. COMPUTER COMPLEX FUNCTIONS.

2-121. The Computer Complex (figure 2-8) consists of a Central Computer Group and associated peripheral equipment. The Command Computer and the Display Computer, although normally functionally independent of each other, are both physically located within the single Computer Complex. The Central Computer Group consists of the two separate computers which jointly share a common I/O Module.

2-122. Each Computer Module functions as a complete computer by means of self-contained input/output and memory circuits. The I/O circuits consist of buffered and non-buffered, bidirectional data channels. The memory circuit provides 8192 words of magnetic core storage. The arithmetic circuits, and control logic circuits, in conjunction with the self-contained I/O and memory circuits, provide the Compute Module with all of the functional capabilities of a basic computer. The addition of the I/O Module and Memory Module provides expansion of the functional capabilities for ACE-S/C system operation.

2-123. Each of the Computer Complex peripheral equipments is connected, via bidirectional data channels (I/O), to the Compute Modules of either the Command or Display Computer, or to the jointly shared Input/Output Module.

2-124. COMPUTER COMPLEX DESCRIPTION.

2-125. COMPUTE MODULE.

2-126. The Compute Module contains circuits for accomplishing each of the four basic functions of a computer; control, arithmetic, memory and I/O. Figure 2-9 is a simplified functional block diagram of the Compute Module. The blocks are background codes to the four functions of the equipment. Those blocks that are not background-coded are common to several computer functions.

2-127. COMPUTE MODULE REGISTERS. The registers contained within the Compute Module serve as temporary storage for operands, instructions, and control words. The contents of the registers can be displayed on the Computer Console. Registers which are available to the programmer by means of computer instructions are called addressable registers; those that are not available are called non-addressable registers.

2-128. CONTROL FUNCTION. A program consists of a number of routines, each of which contains a series of instructions that are stored in sequential memory locations. The instruction being executed is called the current instruction. Upon completion of a routine, control is normally transferred to the next routine.

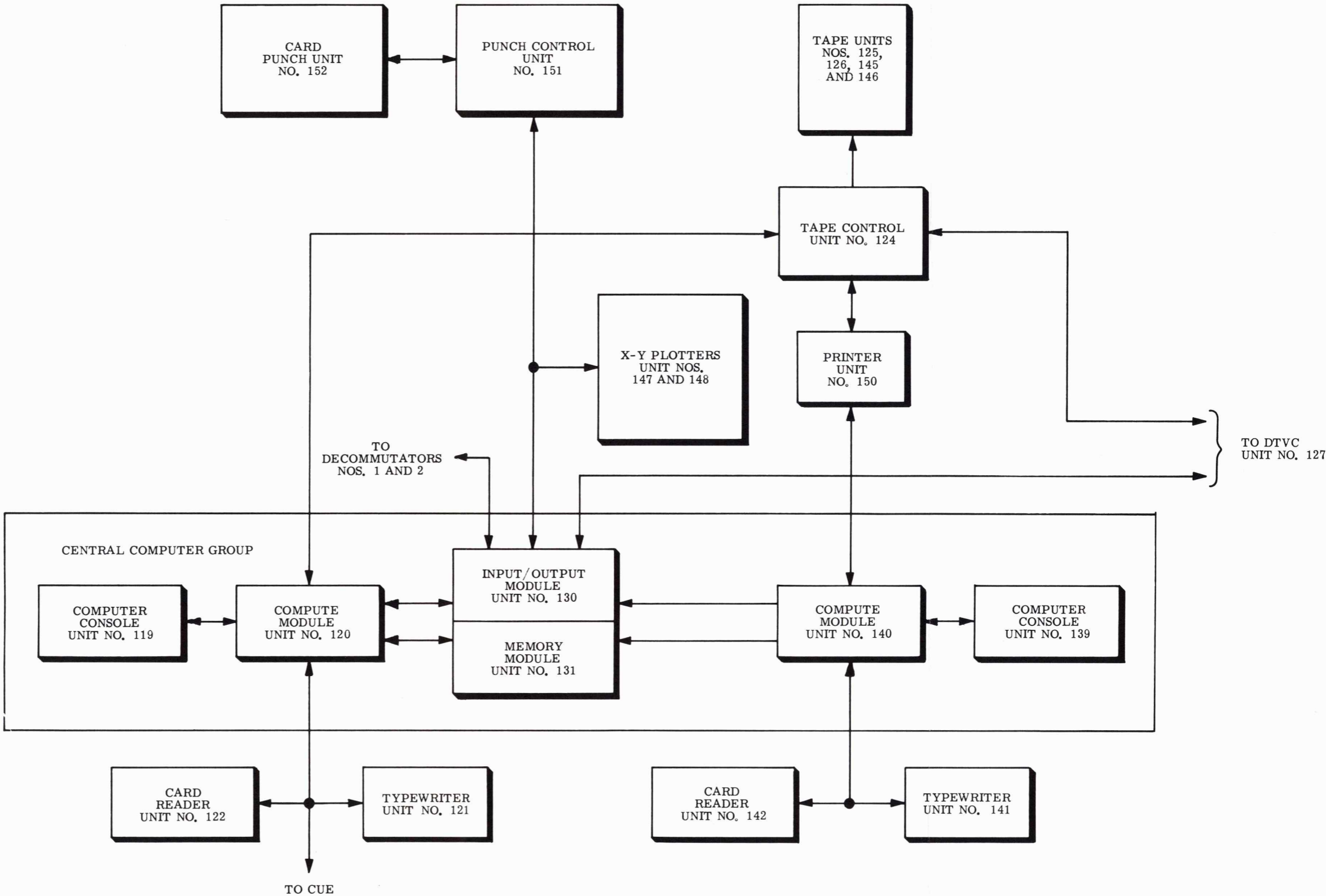
2-129. The control circuits direct the operations required to execute instructions and establish the timing relationships needed to perform these operations in a prescribed sequence.

The control circuits also generate the preliminary instructions which initiate the events required to store or obtain data from the Memory Module or to buffer data through the Input/Output Module.

2-130. The control circuits acquire an instruction from memory, interpret it, perform a sequence of events, and send necessary instructions to other functional circuits. The following paragraph briefly describes the operation of the circuits which contribute to the control function of the Compute Module.

2-131. The P register serves to hold the memory address of the current instruction. The P register receives such data from the S register. When the P register contains the first address in a routine as a result of a manual or programmed entry, the Compute Module is ready to begin the routine. The address in the P register is transferred to the S register, which functions to hold the memory address currently being referenced for an instruction, operand, or addressing operation. The instruction specified by the contents of S (current instruction) is read from its location in memory. This instruction is transferred via the Z register to the X and F registers. After the instruction has been transferred to the X and F registers, the Z register restores the instruction to the original location in memory, thus permitting nondestructive memory reference. Once within the F register, the instruction conditions the control logic to execute this instruction. Some time before the execution of the instruction has been completed, the contents of P are transferred to the adder, a circuit which operates upon two operands to find their sum. The command is then generated which increments the current address to the address of the next instruction. This new address appears in the A' register, which serves as the output of the adder. The new address is then transferred to the S register and from there to the P register. This new address in the P register represents the current instruction address. The preceding procedure is repeated until all of the steps in the routine have been completed, unless the Compute Module is interrupted. At the completion of each routine, control is transferred to the next routine until a manual or programmed stop occurs.

2-132. ARITHMETIC FUNCTION. The arithmetic circuits consist essentially of four registers (A, A', Q, and Q') and the adder. The A and Q registers hold operands during the performance of arithmetic or logic operations. The A' and Q' registers serve as exchange registers in the transmission of data between registers. The A' register also functions as an output register for the adder in the performance of the control functions, as explained in a previous paragraph. The adder (or borrow pyramid) performs arithmetic operations by the one's complement, subtractive arithmetic method. When an arithmetic instruction is executed, the control logic conditions the adder and the A, A', Q, and Q' registers to perform the necessary arithmetic operation. The adder provides the necessary signals, to form



AD2-1-9

Figure 2-8. Computer Complex Block Diagram

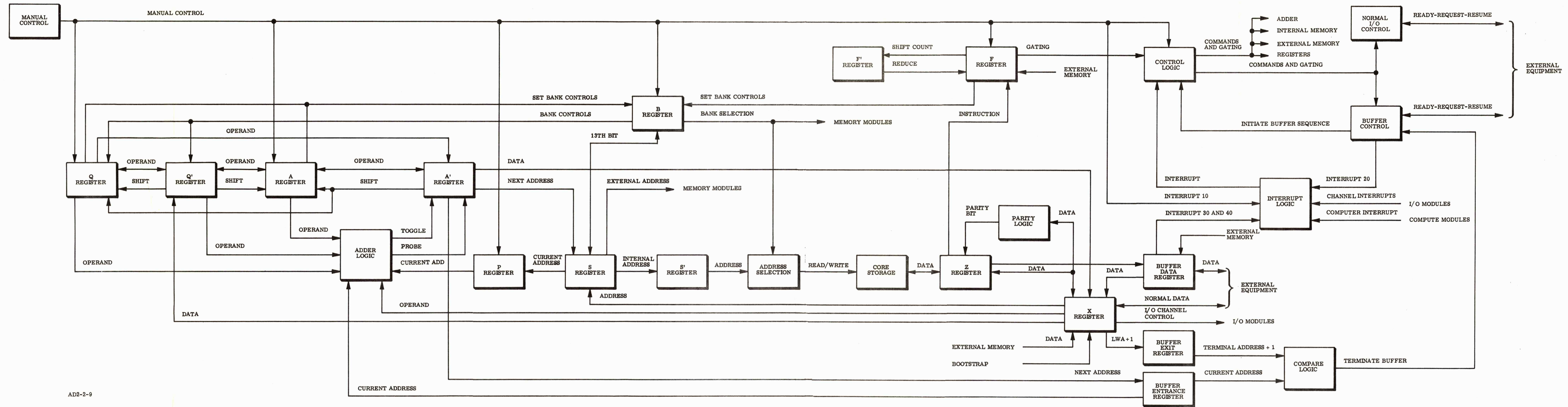


Figure 2-9. Compute Module Simplified Block Diagram

in the A' register by one's complement addition, the sum of an operand from the X register and an operand from either the A or Q registers. Whether the resultant in the A' register represents the sum or difference of two numbers is determined by the nature of the operand from the X register. If the operand from the X register represents the contents of the X register, the A' register resultant equals the sum of the two numbers. If the operand from the X register represents the complement of the X register contents, the A' register resultant equals the difference of the two numbers.

2-133. The A, A', Q, and Q' registers also have capabilities for shifting. The A' register contents can be shifted right or left into the A register, and a similar shift can be accomplished between the Q' and Q registers. Similarly, A'Q' can be shifted right or left into AQ. Multiplication is accomplished by repeated additions and right shifts while division is achieved by repeated subtractions and left shifts. The shifts are performed to maintain relative magnitude of the partial resultant.

2-134. MEMORY FUNCTION. The memory function is performed by two registers (Z and S'), magnetic core storage, memory control logic, and parity circuitry. In the A Mode of computer operation, the magnetic core storage is divided into two banks, each of which provides retention for 4096 14-bit words. In the G Mode of computer operation, the magnetic core storage is considered as a single bank which contains 8192 14-bit words. Only the Compute Module has access to the memory locations in the Compute Module memory banks.

2-135. The contents of the S register and the correct bank control in the B register (control function circuitry) enables a memory location to be referenced for an instruction, operand, or addressing operation. If the memory location is in the external Memory Module, the current memory address stored in the S register is placed on the external address lines where it is forwarded to the S' register of the Memory Module. If the memory bank (as determined by the B register contents) is within the Compute Module, the current memory address stored in the S register is transferred to the Computer Module S' register which, in turn, provides outputs which condition the address selection logic to reference the correct address in memory.

2-136. Data is read out of a memory location through the Z register to the X register where the data is available for manipulation. After the transfer is completed, the Z register restores the data in the original memory location.

2-137. Data is entered into core storage by a write operation. The data to be entered in storage is transferred from the X register to the Z register. The selected storage location is then cleared, and the contents of the Z register is written into this location.

2-138. The parity logic performs a parity check on the contents of the Z register during each read operation. Should parity be wrong, a parity error signal is generated which indicates

that the data is faulty. During the write operation, the parity logic generates a parity bit (as required) to accompany each word that is written into core storage.

2-139. INPUT/OUTPUT FUNCTION. The I/O circuits permit the Compute Module to communicate with external equipment. This circuitry consists of one normal data channel, one buffered data channel, external function logic, and control logic. The transfer of data over the normal channel completely monopolizes the operation of the Compute Module. However, during a data transfer via the buffered channel, the Compute Module is available most of the time to perform other operations.

2-140. A normal input occurs only when it is programmed as a part of a routine. An external function code must be generated by the Compute Module before the normal input can occur. This code activates the appropriate external input device. The control logic in the Compute Module also enables the normal I/O control logic for an exchange of status signal with the external input device. At the appropriate time during the exchange, the input data is transferred into the X register and then stored in memory (via the Z register) at the address specified by the contents of the S register.

2-141. A transfer of data from the Compute Module via the normal data channel (normal output) is a similar operation to that described above for a normal input data transfer. In this instance however, the contents of the address placed in the S register is read from core storage and transferred through the Z and X registers to the selected external device.

2-142. Data entering the Compute Module through the buffered data channel results in a series of operations. Input instructions specify both a first word address (FWA) and a last word address plus one (LWA+1) of a storage area. The FWA portion of the instructions is placed in the buffer entrance register. The LWA+1 portion of the instructions is placed in the buffer exist register. The B-register, buffer bank control is set to the proper storage bank. The buffer input is then initiated.

2-143. The buffer control logic causes the Compute Module to interrupt the current routine to perform a buffer sequence. This sequence generates the commands which perform the following:

- a. Gate the data word into the buffer data register.
- b. Transfer the FWA to the S register.
- c. Store the input word at the address specified by the contents of the S register (FWA).
- d. Transfer the contents of the buffer entrance register (the current address) to the adder.
- e. Current address is increased by one in the adder to form the next address.
- f. Transfer the next address thus generated, via the A' register to the buffer entrance register where this address becomes the new current address.

g. Clear the I/O control logic (terminate buffer signal) if the contents of the buffer entrance register and the buffer exist register are equal.

2-144. The preceding steps are repeated by each input word until the current address equals the LWA+1, thus resulting in the generation of the terminate buffer signal. The resulting Interrupt 20 signal enables the interrupt logic which, in turn, causes the control logic to terminate the buffer and to continue with the interrupted routine.

2-145. The operation of the Compute Module for an output buffer is similar to the operation for an input buffer. The preliminary operations are the same. The Compute Module then executes an instruction which causes the performance of the buffer sequence. This sequence reads from core storage the contents of the location specified by the FWA and transfers this data through the Z and X registers to the buffer data register. When the output data is ready, an Output Ready signal is sent to the external output device.

2-146. INTERRUPTS. Certain internal and external conditions arise which make it necessary for the main program to be notified of their presence. An interrupt is the program signal which transfers control to some fixed location in memory without losing the information needed to return to the main program.

2-147. A signal on any of the interrupt lines into the interrupt logic results in a signal to the control logic which interrupts the routine presently being performed, except under conditions where the interrupt function has been locked out. Upon interruption of the present routine, program control is transferred to the routine which services the active interrupt. Regardless of the type of interrupt, the same general procedure is followed. The Compute Module stores the address of the next instruction to be executed in the routine which has been interrupted, and reads the instruction contained in the special storage location associated with the active interrupt. At the completion of the interrupt routine, the next instruction in the interrupted routine is read from memory and program control is returned to the interrupted routine.

2-148. CONSOLE. Each Compute Module (Command and Display) has an associated control console. The console, consisting of a display panel and a switch panel, contains the controls and indicators necessary for maintenance and operation of the computer. The display panel contains three status indicator displays and four 13-bit register displays. The switch panel is a row of pushbuttons which are used to exercise manual control over the computer.

2-149. MEMORY MODULE.

2-150. The Memory Module consists of two banks of magnetic core storage, priority circuitry, parity circuitry, and memory control logic. The Memory Module has six access

channels, each of which contains the necessary control and data lines to service one Compute Module or the I/O Module. Figure 2-10 provides a block diagram of the Memory Module.

2-151. The physical arrangement of the core storage and method of readout, write-in, and address selection within the Memory Module is practically identical to the memory within the Compute Modules. The major differences lie in the access channels contained in the Memory Module.

2-152. The Compute Module memory section cannot be used except by the Compute Module, whereas the Memory Module storage may be used by either the Compute Module or the I/O Module. To facilitate this additional flexibility, the Memory Module requires such additional circuits as a scanning circuit, a line receiver, a transmitter circuit, and associated control circuits.

2-153. CORE MEMORY. The Memory Module has a storage capacity of 8192 14-bit words, contained in two banks of 4096 words each. The storage function of the Memory Module is controlled by a delay line, for timing, and a Z and S register (similar to those in the Compute Module) to directly effect a memory reference at a specific location.

2-154. PRIORITY CIRCUITRY. A scanner in the Memory Module sequentially examines the access lines for a request from either of the Compute Modules or the I/O Module. When a request occurs, the scanner stops, a memory cycle is initiated, and resume signals are returned to the module which originated the request. The timing of the memory cycle is controlled by the delay line and associated circuitry during the last quarter of the memory cycle. The scanner is restarted from the point at which it was stopped. If requests for a memory reference are on the access lines from other modules, the Memory Module processes each of the references in turn before returning to the first module for any subsequent references. This feature prevents one Compute Module, or the I/O Module, from monopolizing the Memory Module.

2-155. MEMORY CONTROL LOGIC. A signal from the priority circuitry initiates a memory cycle. Each cycle consists of a read operation followed by a write operation and the generation of timing and control signals necessary to the performance of these operations. The results of the memory cycle operations differ depending upon whether the memory reference requested is a read or write.

2-156. For a memory reference which requires that a word be read from memory, the memory cycle read operation will read the contents of the selected memory location. The subsequent write operation, accompanied by appropriate inhibit signals, restores the data to the same memory location after this data has been duplicated for use by the requesting module.

2-157. For a reference which requires that a word be written into memory, the initial read operation clears any old data from the selected location. The subsequent write operation, again accompanied by appropriate inhibit signals, writes the word into the selected location.

2-158. PARITY LOGIC. The 13th bit of the word in each location is used to provide a comparison bit for parity check. A 1 bit is inserted into the 13th bit of each word, as required, to make the total of 1 bits in the word an odd number. Where the word already contains an odd number of 1 bits, a 0 bit is inserted in the 13th bit position.

2-159. The parity circuitry generates the parity bit for all data to be written into core storage and checks the parity of all data read from storage. If during a parity comparison check an error is detected, the computer stops and a parity error signal is sent to the module requesting access.

2-160. INPUT/OUTPUT MODULE.

2-161. GENERAL. The I/O Module contains two buffered bidirectional data channels and associated control logic. The channels are designated Y and Y', where Y equals an even number from 2 through 6 (2, 4, 6) and Y' equals Y+1 (3, 5, 7).

2-162. Figure 2-11 is a simplified, functional block diagram of the I/O Module, presenting only the Y channel and the logic common to both Y and Y'. The discussion that follows considers the functional operation of the I/O Module with Respect to the various types of operations which involve the module.

2-163. EXTERNAL FUNCTION. When either Compute Module (Command or Display) executes an External Function (EF) instruction, an EF code is read from the Compute Module memory and placed in the Compute Module X register, from there it is sent over a Compute Module I/O channel, or an I/O Module channel, to the equipment for which the code is intended. The I/O channel to be used is determined by the instruction in the Compute Module F register (control function). EF codes are generally used to sense the status of a particular equipment or to activate the equipment for a specific type of operation.

2-164. When an EF code is meant for an equipment that interfaces with either the Command or Display Computer through the I/O Module, the code and associated control signals are transmitted from the appropriate Compute Module to the I/O Module. If the I/O Module has been previously cleared by an internal or external control signal, the correct channel select signal enables the priority circuitry for an EF operation. When the EF code is available on the data lines from a Compute Module, the Compute Module transmits a Function Ready signal to the I/O Module. This signal conditions the compute interface control logic to generate a signal which gates the EF code into the buffer data register. This register temporarily stores all buffer data which enters or leaves the I/O Module. A signal from the compute

interface control logic also enables the I/O control logic to generate a signal which gates the EF code out of the buffer data register onto the data lines to the external equipment.

2-165. Upon sensing the EF code, the external equipment returns an Output Resume signal to the I/O Module. This Output Resume signal is forwarded to the Compute Module which then removes the Function Ready and data signals from the lines.

2-166. INPUT-TO-A OPERATION. Equipment external to the Central Computer Group will generate a status response code when queried by an EF Status Request signal from a Compute Module. An input-to-A operation is required to transmit the status response code from the external equipment to the A register in the Compute Module, via the Y channel logic of the I/O Module. To facilitate the transmission of the status response code, the Y channel of the I/O Module must be selected by the select channel code from the Compute Module.

2-167. The sequence of events is initiated by an input-to-A signal from the Compute Module. This signal causes the compute interface control logic to enable the I/O control logic. The I/O control logic, in turn, sends an Input Request signal to the external equipment, which then places the status word on the data lines and generates an Input Ready signal. The Input Ready signal from the external equipment is received by the I/O control logic, causing the Input Request signal to be removed, and the data from the external equipment to be gated onto the data lines to the Compute Module. The input-to-A signal is applied to the compute interface control logic during the entire operation, and is removed only after the status word from the external equipment has been received at the Compute Module. The removal of the input-to-A signal results in the clearing of the channel Y buffer data register and the I/O control logic.

2-168. INPUT BUFFER. In the performance of an input buffer, the I/O Module buffers data from an external device into a selected block of memory locations in a memory bank. A select channel code from the Compute Module determines which channel will be affected (Y or Y') by subsequent control signals from the Compute Module. Prior to the initiation of the input buffer, however, the Compute Module sets the current address, which is initially FWA, into the buffer entrance register, the LWA+1 into the buffer exit register, and the bank designation into the buffer bank control for channel Y. The data for the registers and associated control signals are transmitted, one word at a time, through the data receivers and placed in the proper register or control circuit. These words control the address selection for each data word and the repetition of the buffer operation.

2-169. Upon the arrival of an initiate buffer input signal from the Compute Module, the channel select, priority logic, and I/O control logic are conditioned for an input buffer operation. The I/O control logic sends an Input Request signal to the external equipment. The external equipment, in turn, sends an Input Ready signal back to the I/O control logic when the

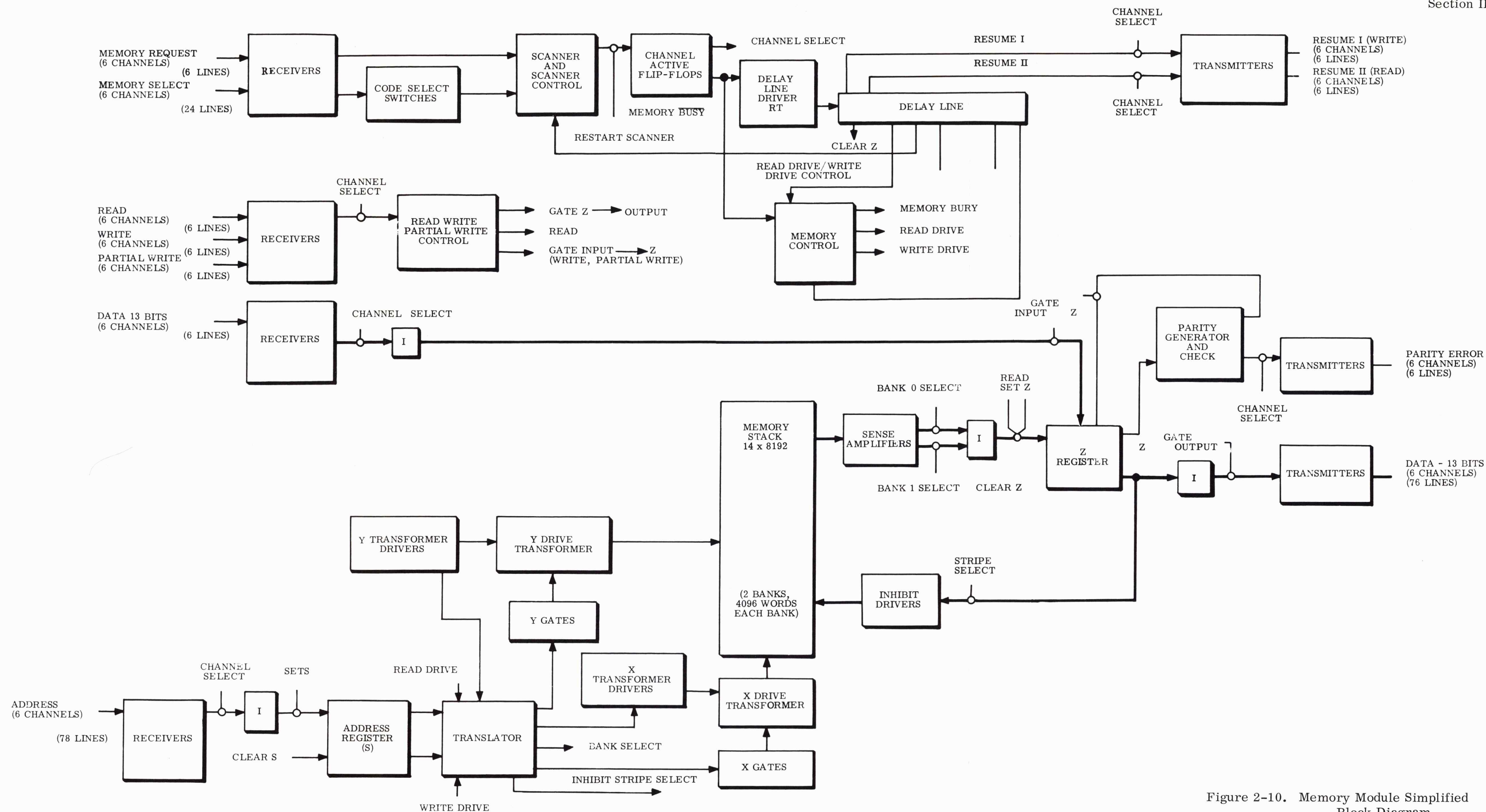


Figure 2-10. Memory Module Simplified Block Diagram

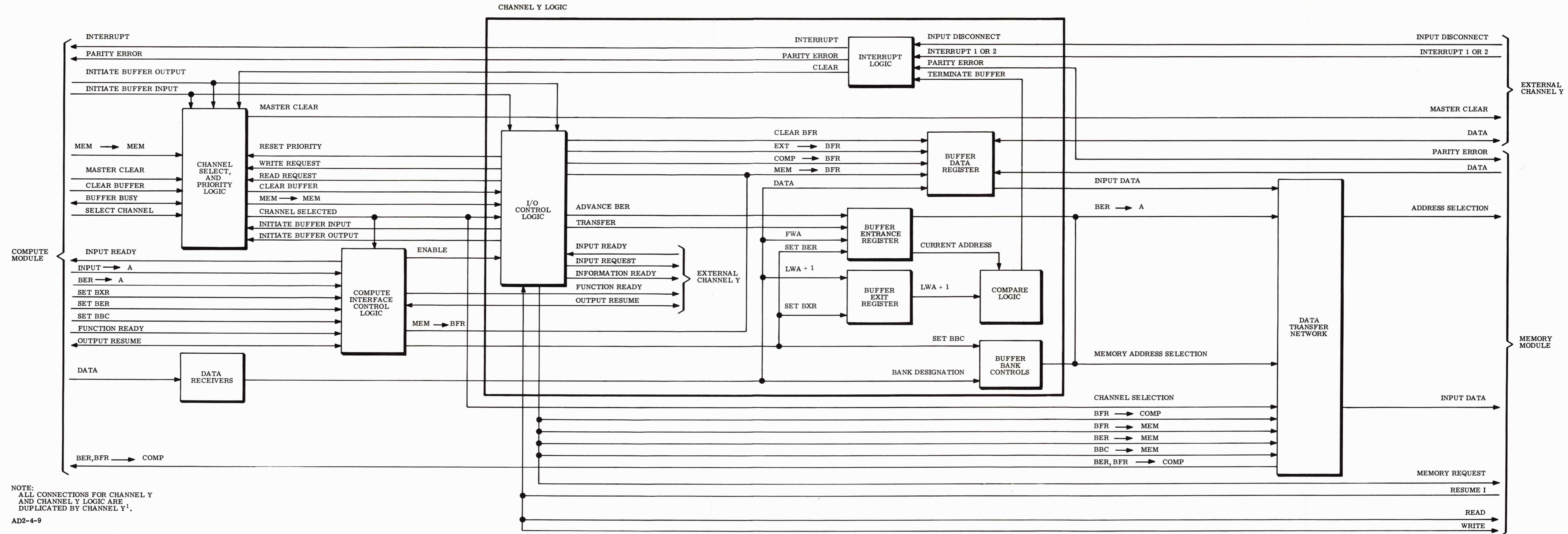


Figure 2-11. Input/Output Module Block Diagram

input word has been placed on the data lines to the buffer data register. The Input Ready signal causes the I/O control logic to:

- a. Remove the Input Request signal to the input equipment.
- b. Gate the input into the buffer data register.
- c. Send a write signal to the Memory Module.
- d. Place the contents of the buffer entrance register (FWA), buffer bank control, and buffer data register, on the lines to the Memory Module.
- e. Send a Memory Request signal to the Memory Module.

2-170. The Memory Request signal causes the Memory Module to store the input data word at the address specified by the contents of the buffer entrance register in the bank designated by the contents of the buffer bank control.

2-171. After the data has been stored, the Memory Module returns a resume 1 signal to the I/O control logic which then generates the signals necessary to increase the contents of the buffer entrance register by one (FWA), clear the buffer data register, and generate another Input Request signal to the external device. Upon receipt of the next Input Ready signal from the input device, the steps performed by the I/O control logic (previously described) are repeated for the next input word.

2-172. This process is repeated for each input word until the contents of the buffer entrance register equals the contents of the buffer exit register (LWA+1). When this occurs, the compare logic sends a terminate buffer signal to the interrupt logic, thus generating an interrupt signal which clears the channel Y control logic.

2-173. OUTPUT BUFFER. The I/O Module logic circuitry is also involved in the transfer of data from a selected block of memory locations in the Memory Module to an output equipment. Channel Y, to which the output device is attached (chosen for the purpose of this discussion), is selected by a select channel code from the Compute Module. Prior to the initiation of the output buffer, the Compute Module sets the LWA+1 in the buffer exit register, the FWA in the buffer entrance register, and the bank designation in the buffer bank control.

2-174. When the initiate buffer output signal arrives from the Compute Module, it conditions the channel select, and priority logic and the I/O control logic. The I/O control logic then gates the contents of the buffer entrance register (FWA) and buffer bank control (bank designation) onto the address selection lines to the Memory Module and generates a read signal. The I/O control logic then sends a Memory Request signal to the Memory Module. This signal initiates a memory cycle which reads the contents of the location as specified by the address selection. When the data is available at the Memory Module, a resume 1 signal is forwarded

to the I/O control logic in the I/O Module, which causes the following:

- a. Removes the address selection and Memory Request signals from the lines to the Memory Module.
- b. Gates the output data word from the Memory Module into the buffer data register.
- c. Gates this data from the buffer data register onto the data lines to the output equipment.
- d. Sends an Information Ready signal to the output equipment.

2-175. The output equipment, having processed the data word, sends an Output Resume signal to the I/O Module, which causes the I/O control logic to remove the output data and Information Ready signals from the lines and to enter a resume cycle which clears the buffer data register and increases the content of the buffer entrance register by one. The next address is then gated onto the address selection lines, and the buffer cycle is repeated for the next output word. This repetition continues until the contents of the buffer entrance register equal the contents of the buffer exit register (LWA+1), at which time a terminate buffer signal is sent from the compare logic to the interrupt logic. The interrupt logic generates the correct interrupt signal and clears the channel Y logic.

2-176. MEMORY-TO-MEMORY TRANSFER. Both the Y and Y' channels of the I/O Module participate in the transfer of a block of data from one memory area to another. Channel Y performs an output buffer function while the Y' channel provides an input buffer function to the new memory area. Only a single buffer data register for both operations is required, however, since the data is transferred (within the Central Computer Group) to another memory area rather than to an external equipment.

2-177. A channel Y select channel code from the Compute Module is used to enable the channel Y priority logic. Prior to the initiation of the memory-to-memory transfer, the Compute Module sets into the buffer entrance register, buffer exit register, and buffer bank control, the FWA, LWA+1, and bank designation, respectively, for the memory area from which the data is to be transferred. After the initial transfer address data has been entered, the Compute Module issues a memory-to-memory signal that sets a control in the priority logic. This control conditions the I/O control logic of both Y and Y' channels to perform the required operations. The memory-to-memory transfer is activated by a Compute Module instruction to initiate a Y-channel buffer output. The I/O control logic gates the contents of the Y channel, buffer entrance register, and buffer bank control onto the address lines and sends a read signal to the Memory Module. The I/O control logic then generates a Memory Request that starts the reading of the first data word at the location specified by the address selection.

2-178. When the data is available, the Memory Module returns a resume 1 signal to the I/O Module to remove the read, Memory Request, and address selection signals and to gate the

data into the channel Y' buffer data register. The channel Y' I/O control logic then performs a resume cycle that increases the content of the channel Y buffer entrance register by one.

2-179. The channel Y' I/O control logic then gates a write signal and the contents of the channel Y' buffer entrance register, buffer bank control, and buffer data register onto the signal lines to the Memory Module. A Memory Request signal is then sent to the Memory Module to initiate the storage of the data word at the location specified by the channel Y' address selection. The data having been stored, a resume 1 signal is returned to the I/O Module which causes the channel Y' I/O control logic to remove all channel Y' data and control signals and to perform a resume cycle which increases the contents of the channel Y' buffer entrance register by one. The channel Y' buffer data register is cleared at the same time.

2-180. Upon completion of the channel Y resume cycle, the channel Y logic begins a repetition of the memory-to-memory transfer by selecting the address of the next word. The operations involving channels Y and Y' are repeated for each word to be transferred until the contents of the channel Y buffer entrance register equals the contents of the channel Y buffer exit register, at which time the memory-to-memory transfer is terminated.

2-181. INTERRUPT. The interrupt logic circuitry in the I/O Module functions as a repeater network. When an interrupt signal is generated by an external equipment, the interrupt logic receives this signal and transmits it to the Compute Module.

2-182. The I/O Module contains separate interrupt logic for channels Y and Y'. There are two external interrupt lines and an input disconnect line associated with each channel. Any of these lines may be activated by any equipment serviced by the channel. Each channel also contains provisions for a buffer termination interrupt. Whenever any interrupt is active, the correct interrupt signal is sent to the Compute Module. This signal causes the Compute Module to perform the routine necessary to satisfy the interrupt. Input disconnect and buffer termination signals also result in a clear signal to the channel selection and priority logic which frees channel Y for the next I/O operation.

2-183. LINE PRINTER.

2-184. The Line Printer is a high-speed printer with integral provisions for storage, decoding, and supervision that enable the equipment to accept and print out data furnished in binary encoded form. The printer serves as a peripheral unit for the Central Computer Group. The equipment accepts information from the Compute Module (Display Computer) and prints this computer data output on fan-fold forms at a nominal maximum rate of 1000 lines per minute with each line containing up to 120 characters. A choice of 64 marks, characters, and symbols, including a full set of numbers and capital letters, can be printed.

2-185. LINE PRINTER FUNCTIONS. Figure 2-12 shows the Line Printer in block diagram form. As indicated, the printer has three main functional subdivisions: the logic or buffer that communicates with the computer to exchange control signals and store data for printing and provides driving power for printing; the high-speed line printer (printer), which produces the printed document and provides the timing signals needed to synchronize operation of the printer and the logic; and the power supply and distribution system, which controls the application of power to the buffer and printer circuits.

2-186. The logic circuits are further subdivided into eight major subdivisions:

- a. Interface logic, which provides communication between the printer and Compute Module.
- b. Master timing generator, which synchronizes and sequences data storage and printing operations.
- c. Core driver "A," which translates the data storage code from the master timing generator to address vertical wires in the memory plane during the data storage operation. During the printing operation, core driver "A" provides read pulses to sense the stored data.
- d. Core driver "B," which translates the data storage code from the computer in order to address horizontal wires in the memory plane.
- e. Memory plane, or magnetic core storage array, which provides internal storage of data for printing.
- f. Sense amplifiers, which operate during the printing operation to sense, shape, and amplify the data bits stored in the memory plane.
- g. Hammer drivers, which provide the necessary driving power for the solenoids in the printing mechanism. Each hammer driver contains a one-shot multivibrator (OSMV), which triggers on coincidence of a sense amplifier output and an enabling pulse from the master timing generator.
- h. Vertical format control, which provides internal storage of printed-line spacing (format) instructions and control of format operations.

2-187. PHASES OF OPERATION. Operation of the system can be described as taking place in four steps or phases: interface communication (between buffer and computer); data storage; printing; and line spacing.

2-188. INTERFACE COMMUNICATION. During the interface communication phase, the buffer is selected by the computer and conditioned to accept data through an exchange of control signals between the computer and the interface section.

2-189. DATA STORAGE. When informed that the buffer is ready to accept data, the computer transmits a word of data to core driver B. The six data bits comprising the word are sampled by a write-sample pulse from the master timing generator. This write-sample

pulse originated in the interface (as a write-in drive pulse) in response to a signal from the computer that the data bits were ready for translation. The write-sample pulse causes the core drivers to translate the character address (identified by the data bits) within the memory plane. Each six-bit character code received by the Line Printer relates not only to one of the 64 possible characters but also specifies the character's position within the proposed line of print. Transmission of words from the computer continues until the entire block of words corresponding to the line of characters to be printed has been transmitted.

2-190. PRINTING. During the time information is being buffered from the computer to the line printer buffer and placed in the magnetic core storage array, the print cylinder is continuously rotating. Following the termination of the buffer data storage phase, an index pulse from the printer is sensed by the master timing generator. The index pulse occurs once every print cylinder revolution and provides a reference point which indicates the beginning of the printing cycle.

2-191. The print cylinder consists of 64 rows of characters, with one character repeated 120 times over each row. The A row, for example, contains 120 A characters, the B row 120 B characters, etc. Each row of characters is accompanied by its own character mark. As the print cylinder rotates, each row of characters is brought into position over the row of 120 hammers. Sensing of the character mark by the master timing generator enables the firing of the print hammers. As a row of characters move past the row of hammers, the appropriate hammers fire, as determined by the contents of the memory plane. Paper and inked ribbons are passed between the print cylinder and the hammers. Although the print wheel is in continuous motion, hammer actuation is so rapid that a clear, sharp impression of each character is produced. Each time a row of characters passes the row of hammers, the process is repeated. The paper is held stationary for each line of print, then advanced automatically in preparation for the next line of print. If any of the last 15 characters on the print wheel (non-FORTRAN set) are used in a line of print, the print cylinder must make an additional revolution to sense the index mark. Printing speed will be consequently reduced to one-half of the initially selected value.

2-192. LINE SPACING. Control of printed-line spacing is accomplished through the vertical format control logic. An end-of-print pulse, produced by the master timing generator at the conclusion of the printing operation, triggers an automatic paper feed pulse. Two sources of control are provided to limit paper advance: (1) function bits from the computer, decoded by a sampling pulse from the interface, and (2) operator's controls, mounted on the printer.

2-193. CARD READER.

2-194. The Card Reader provides a fast and efficient source of information input to the Central Computer Group. The data input provided by the Card Reader is recorded on cards by means of holes punched by an operator using a card punch.

2-195. The transfer of data and the exchange of control information with either the Central Computer Group or other peripheral equipment is routed through a control unit. The control unit provides the timing signals required to control the flow of information into and out of the Card Reader. The Card Reader can accommodate up to 4000 punched cards of either the 80-column or 51-column type.

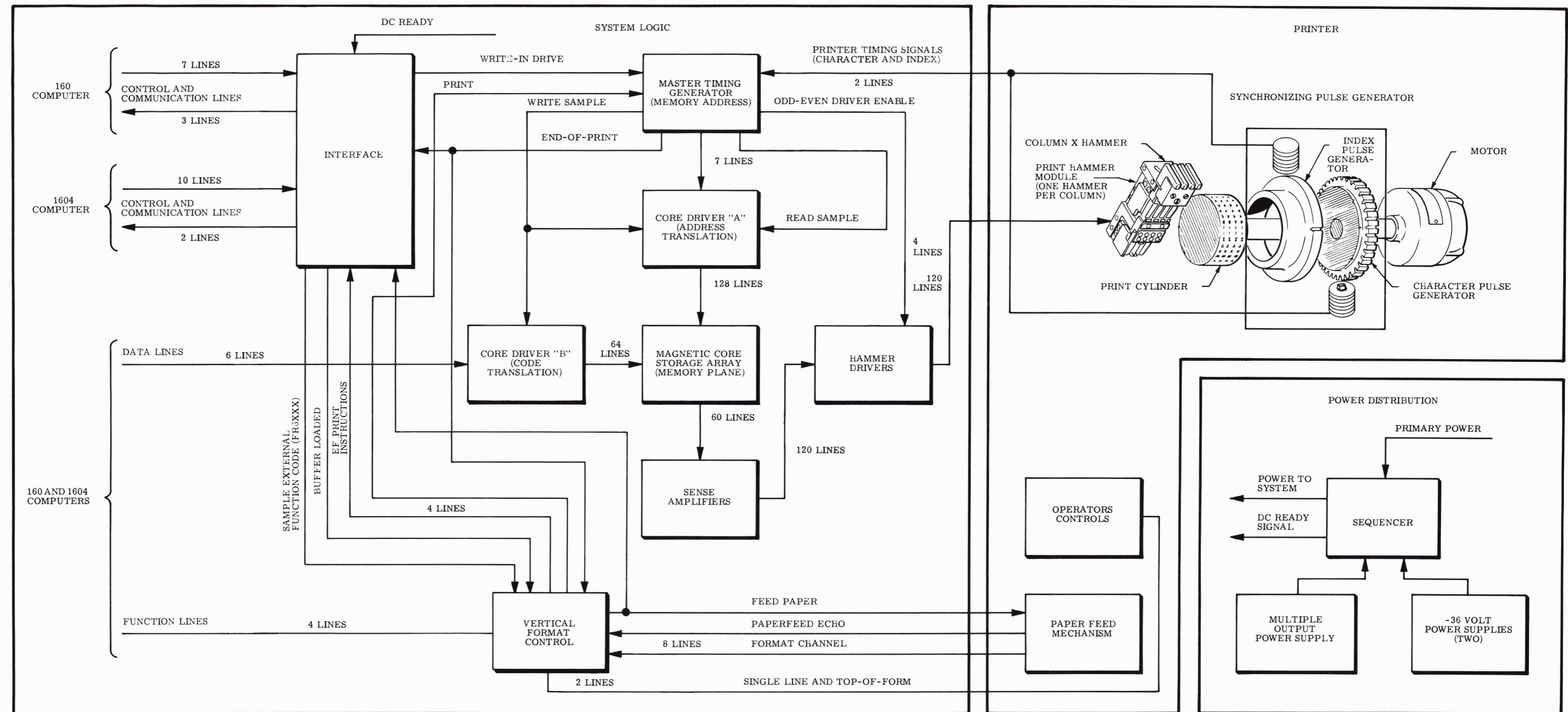
2-196. The data contained on each card, in the form of punched holes, is read photo-electrically. Each card is read by two separate rows of photodiodes, the outputs of which are compared to detect possible errors.

2-197. **CARD READER FUNCTIONS.** Figure 2-13 is a block diagram of the Card Reader. For the purpose of the following discussion, the circuits can be divided into four logic sections: read, compare, timing, and local control.

2-198. **READ LOGIC.** The read logic circuits detect the data punched into cards and routes this information to the control unit in binary code form. The read logic is divided into primary and secondary read circuits. Each of the read circuits sense the card information by means of 12 photodiodes set in a row so as to read each card column by column. The photodiodes are energized by the light that has passed through the holes in the card from an exciter lamp. The signals from the 12 primary read-circuit photodiodes are amplified, converted to standard logic voltage levels, and gated into a read register. The read register provides temporary storage for the information bits while they are transferred to the control unit. The 12 information bits obtained by the primary read circuit are also supplied to the compare logic circuit for checking.

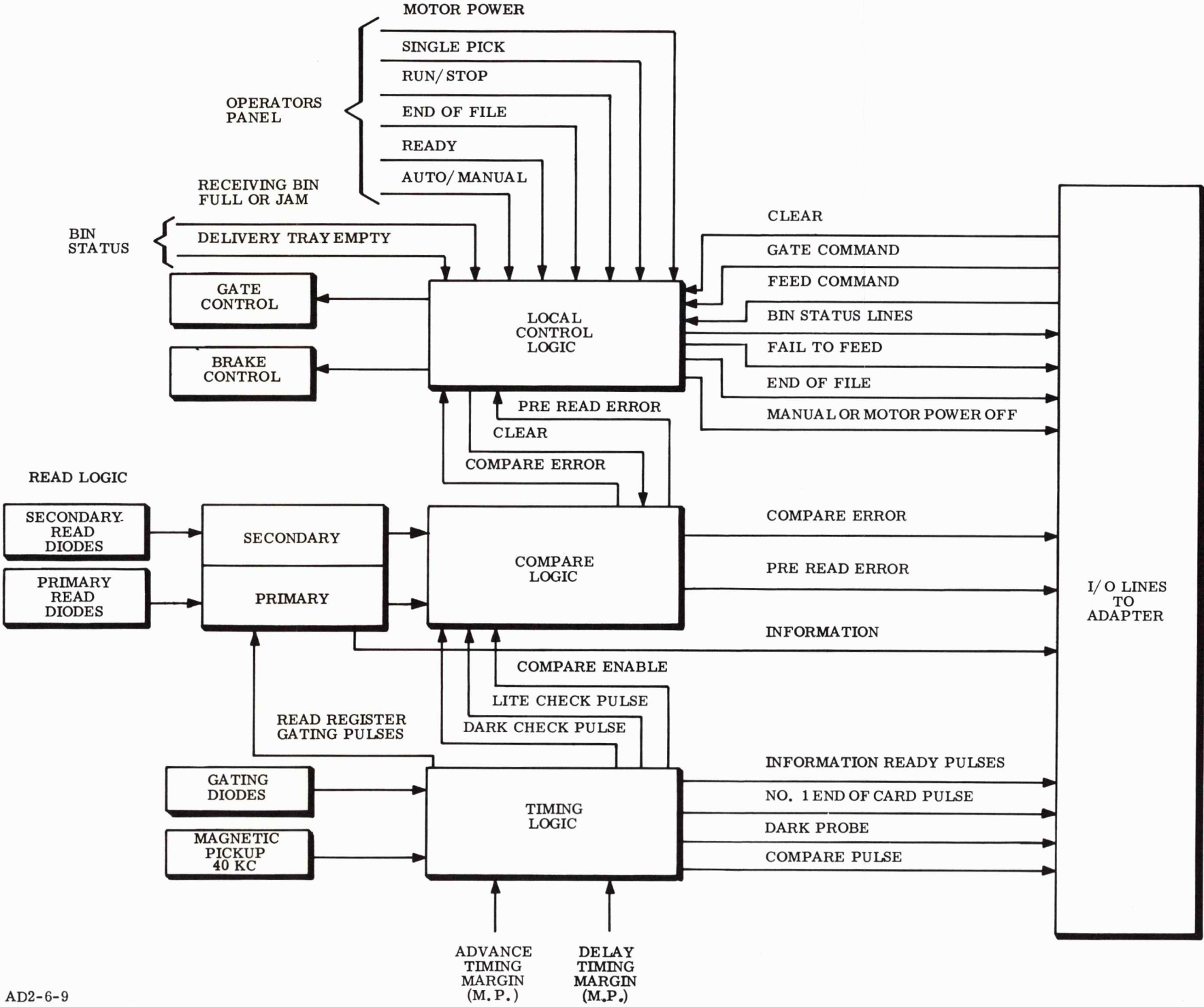
2-199. The secondary read circuit contains a second row of 12 photodiodes that read each column of a punched card approximately 400 milliseconds after the column has been read by the primary read circuit. This second set of 12 information bits is amplified, converted to standard logic voltage levels, and routed directly to the compare logic circuit. This data is neither stored nor sent to the control unit.

2-200. **TIMING LOGIC.** The timing logic circuits provide enabling signals to the Card Reader logic circuits and timing pulses to the control unit. A clock counter counts 40-kc pulses and provides the basic source of timing for the Card Reader. Counter output pulses are arranged so that associated circuits are enabled when the counter reaches a specified



AD2-5-9

Figure 2-12. Line Printer Simplified Block Diagram



AD2-6-9

Figure 2-13. Card Reader Logic Block Diagram

count. The various pulses generated by the timing logic circuits synchronize the reading, storing, and comparing of each column of data read from a card.

2-201. COMPARE LOGIC. The compare logic circuits provide two basic functions: (1) a preread-error test of the light and dark detecting capability of both the primary and secondary read stations, prior to reading each card, and (2) a compare-error test in which outputs from the secondary read circuit are compared with data stored in the read register. A compare error institutes four actions:

- a. Lights the compare error indicator on the Card Reader maintenance panel.
- b. Turns off the read indicator on the Card Reader operator's panel.
- c. Sends a 0 pulse to the control unit.
- d. Sends enable gate signals to various logic circuits within the Card Reader.

2-202. A compare error is cleared by either a Master Clear signal or by the light probe signal.

2-203. LOCAL CONTROL LOGIC. The local control logic circuits perform four discrete functions:

- a. Ready and Master Clear Circuit. Informs the operator when a fault has been detected and clears the fault detecting circuit by a signal received from either the operator's panel or the control unit.

- b. Motion Control Circuits.

- (1) Feed Control Circuit. Receives manual or automatic feed commands and supplies them to the card brake, which stops or starts card feed and informs the operator of a fail-to-feed condition.
- (2) Gate Control Circuit. Receives manual or automatic gate commands and determines whether a card will be directed to a primary or secondary receiving tray.

- c. Tray Status Circuits.

- (1) Jam or Receiving Tray Full Circuit. Detects a full condition in either of the receiving trays, or a jammed card in the primary receiving tray.
- (2) Input Tray Empty Circuit. In the Automatic Mode, this circuit informs the control unit when the last card has been taken from the input tray; in the Manual Mode, it disables all manual feed commands.

2-204. CONTROL UNIT. The Card Reader controller (control unit) provides additional logic circuitry for functions that are not performed by the basic Card Reader, but are necessary for a satisfactory interface with the Central Computer Group. Approximately 80 logic cards are contained within the control unit to provide the following functions:

- a. EF Translations. Recognizes the selection of the Card Reader by the Central Computer Group and determines the function it is to perform.

b. Status Request. Responds to Status Request signal from Central Computer Group by sending Card Reader status information and Input Ready signal to the computer.

c. Hollerith to Binary-Coded-Decimal Translation. Provides automatic translation from Hollerith to binary-coded-decimal code when the card being read does not have a 7 and 9 punch in the first column.

d. Input Disconnect. The input disconnect is forwarded to the computer in response to an Input Request when the Card Reader is unable to transfer valid data for any of several reasons.

2-205. When the card being read contains straight binary data (first column of card has 7 and 9 punch), the 12-bit parallel data output from the Card Reader is applied directly to the Central Computer Group without any further processing. When a card contains data in Hollerith code, however, the Hollerith-to-BCD translator operates upon each column of data. The odd column translation is stored temporarily in the hold register until the next even column has been translated, at which time both columns of data (12 parallel bits) are simultaneously applied to the output register. The odd column data form the upper six bits whereas the even column data represents the lower six bits.

2-206. MAGNETIC TAPE TRANSPORT UNITS.

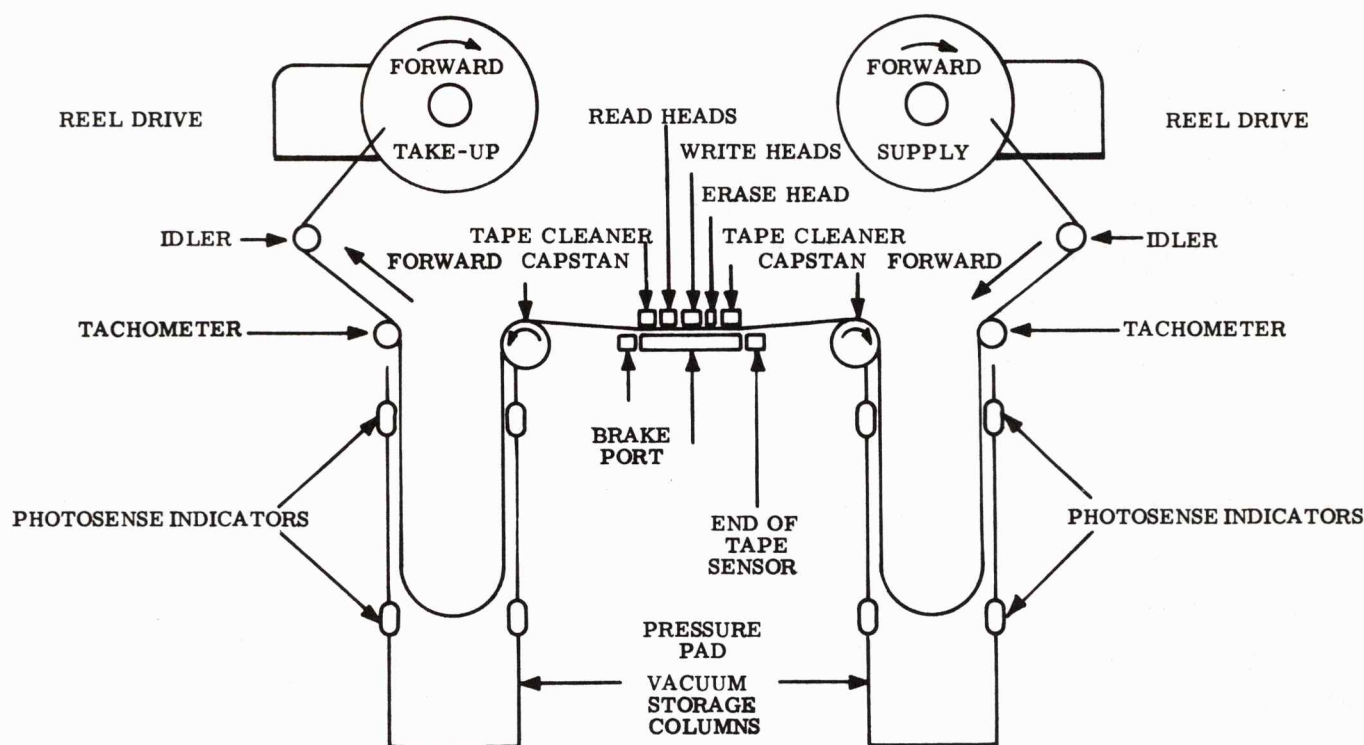
2-207. The Magnetic Tape Transport provides a high-speed medium for recording and retaining information. Information is read (detected) or written (stored) by passing the tape over read/write heads. Reflective spots, consisting of adhesive plastic strips coated with vaporized aluminum, are placed on the tape to determine the beginning and end of the usable portion of the magnetic tape.

2-208. Information may be written on any of seven independent tracks on the tape by means of seven recording heads placed vertically across the tape. Information may be simultaneously recorded on each of the seven tracks. The seven recording heads simultaneously record a line (or frame) of data consisting of a six-bit character and a parity bit. Tracks zero through five specify the character, while track six holds the parity bit.

2-209. A non-return-to-zero (change-on-ones) recording method is used. For this method, magnetic particles on the tape are aligned in either the positive or negative direction. A binary 1 is recorded by reversing the alignment (polarity); no polarity reversal results in a binary 0. Each track of the tape is fully magnetized prior to recording, and the polarity is reversed as each 1 bit is recorded.

2-210. TAPE MOTION. During a read or write operation, tape is moved from the supply reel, past the read/write heads, to the takeup reel (figure 2-14). Tape motion is provided by two fluted capstans that rotate continuously in opposite directions. Tape is drawn against the drive capstan by vacuum and floated over the nondriving capstan by air pressure. If the

tape is moving from the supply reel to the takeup reel (forward motion), the left capstan drives the tape. If tape motion is in the opposite (reverse) direction, the right capstan provides the drive.



AD2-7-9

Figure 2-14. Tape Motion Simplified Diagram

2-211. Tape motion is quickly and smoothly stopped by means of a pneumatic brake port. Tape is drawn to and firmly held against the brake port by means of vacuum. Because pressure is applied to both capstans during this period, neither capstan contacts (drives) the tape.

2-212. READ/WRITE HEADS. The head assembly consists of individual read and write heads, an erase head, tape cleaners, and a pneumatic pad. Each of the seven read/write heads used in the tape transport has two magnetic gaps. One gap is used for writing, the other for reading. The gaps are arranged so that during a write operation, the tape first passes under the write gap to record the data and then under the read gap to check the writing. This allows each line of information to be examined and verified immediately after it is written on the tape. Thus, if any discrepancy occurs during the write operation, it is immediately detected at the read head.

2-213. The tape cleaners and erase head clean and prepare the tape for a read or write operation. The broadband erase head removes any information recorded on the tape before

new information is recorded by the write heads. The two tape cleaners, located on either side of the heads, pneumatically remove foreign particles on the tape surface during a read or write operation.

2-214. A pneumatic pressure pad maintains precise contact pressure between the tape and the head gaps. This contact pressure is provided by means of air pressure which minimizes head and tape wear by blowing the tape against the heads.

2-215. VACUUM BUFFER COLUMNS. The tape transport can accelerate tape to high speed within 3 milliseconds. Conversely, tape motion is completely stopped within 2 milliseconds. The tape transport uses vacuum loops to reduce to a minimum the tape mass that must be accelerated during the 3-millisecond period. These loops separate the heavy tape reels from the portion of tape under the heads.

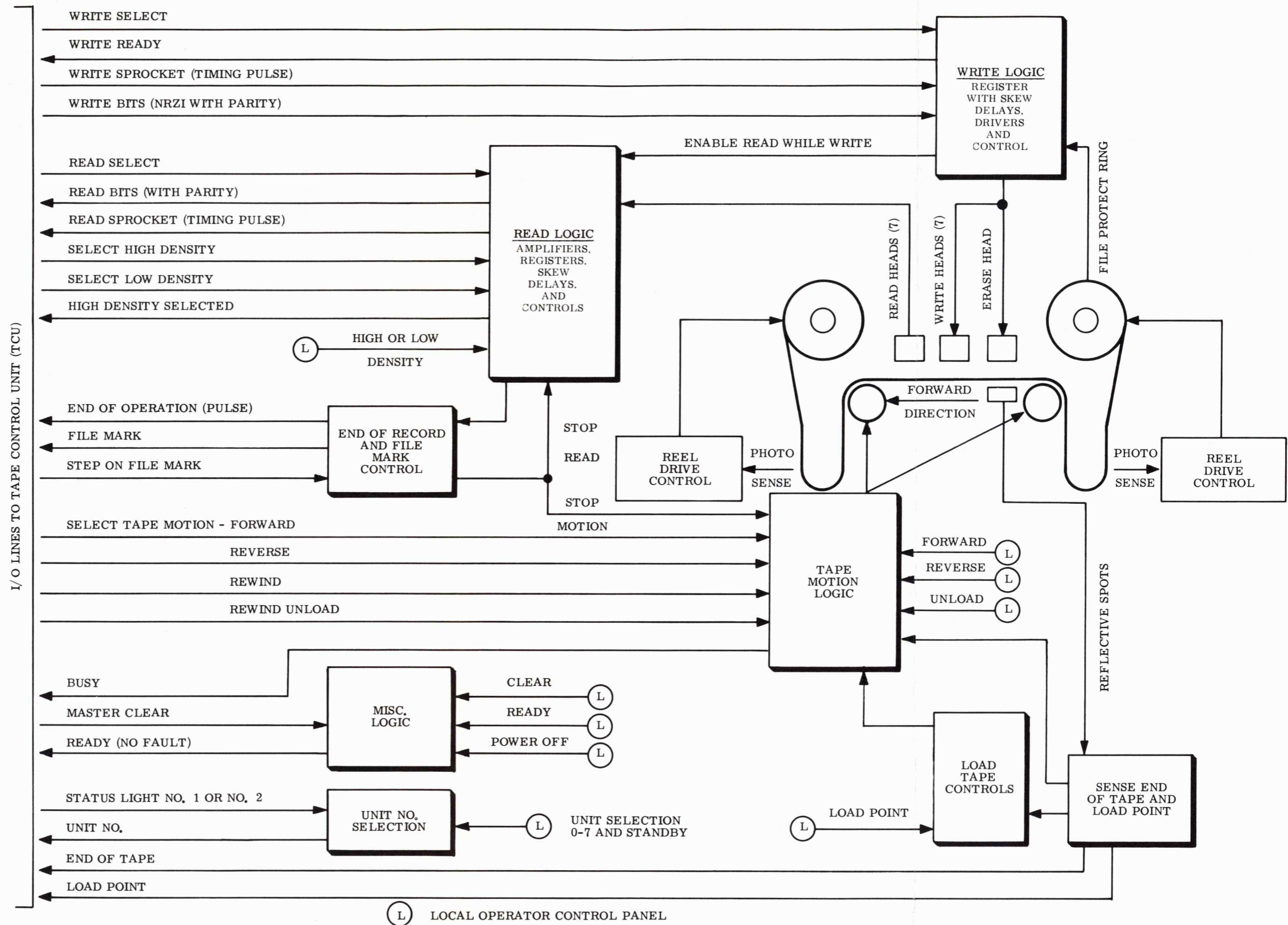
2-216. The two tape loops form tape reservoirs for the capstan drive system. During the first few milliseconds of acceleration, the actuated capstan pulls tape from one loop and places it in the second loop. As tape is drawn from one column, it is replaced from the reel above it. As tape is fed into the opposite column, the associated reel takes up the slack. The heavy tape reels therefore are given more time to accelerate and act to increase or reduce the amount of tape in the vacuum columns. In other words, tape loops buffer the heavy reels out of the high acceleration capstan drive system. This minimizes the inertia in the high acceleration system, since the capstans need only accelerate the mass of a few feet of tape.

2-217. The vacuum columns also maintain proper overall tape tension. Each loop fits snugly into a chamber and divides the chamber into two parts. The bottom portion of the column is under reduced pressure. The upper part is at atmospheric pressure and pushes the loop down, providing a small amount of tension on the loop.

2-218. REEL DRIVE AND SERVO CONTROL. The reel drive controls the position of the tape loops in the vacuum columns. A servo system between each loop and tape drive positions the tape reels by responding to signals from the vacuum column photosense indicators. If the tape loop in a column is too long, the photosense indicators signal the reel drive to take up tape. If the loop is too short, the indicators signal the reel drive to deliver tape.

2-219. FUNCTIONAL LOGIC DISCUSSION. The Magnetic Tape Transport Unit can be divided into five functional logic groups: read, write, motion, servo drive, and local. Figure 2-15 is a block diagram illustrating the relationships between the five Magnetic Tape Transport functional logic groups, and between these groups and the tape control unit.

2-220. READ LOGIC. The read logic circuits control the transfer of information from the Magnetic Tape Transport and the tape control unit (TCU). The TCU determines which of the



AD2-8-9

Figure 2-15. Tape Transport Logic Block Diagram

four available Magnetic Tape Transports will be selected to make information available from its tape storage (read) by sending a read select signal to the appropriate unit. A select-read circuit within the Magnetic Tape Transport read logic allows a read operation to be performed upon receipt of the read select signal.

2-221. After the proper data has been read from the tape, the seven-bit words (six character bits plus one parity bit) are applied to a read data circuit in the read logic, which provides temporary storage for the information bits while they are placed on the output lines to the TCU.

2-222. A select-density circuit within the read logic specifies the rate at which information is to be transferred to the TCU. Either high- or low-density data transfer can be selected by means of corresponding signals from the TCU or by means of locally controlled push-buttons on the Magnetic Tape Transport operator's panel.

2-223. Control of the information read from the tape as it passes through the read-logic circuits is provided by a read gate. The read gate allows the transmission of information to the TCU in response to signals from the select-density circuit.

2-224. The read logic also contains provisions for notifying the TCU when designated points on the tape have been reached. The file mark stop and end-of-operation circuit sends appropriate signals to the TCU when a file mark or load-point marker has been detected. The circuit also stops the tape when a selected file mark is detected.

2-225. WRITE LOGIC. The write logic portion of the Magnetic Tape Transport Unit consists of write-data circuits and an associated write-enable circuit. The write-data circuits accept information from the TCU in the form of seven-bit characters and route the data to the write heads for recording. A write sprocket signal accompanies all input information from the TCU. This signal serves to indicate that a seven-bit character is on the input line and may be sampled and routed to the write register. Each incoming bit is delayed proportionately so as to vertically align all seven bits on the tape.

2-226. A write enable circuit allows the information to be transferred from the TCU to the write heads by activating several switches and relays and returning a write ready signal to the TCU.

2-227. MOTION LOGIC. The motion-logic circuits consist of the motion-select circuit and the capstan drive and brake-control circuit. The motion-select circuit controls the direction of tape motion. Motion of the tape in either the forward or reverse direction can be selected by signals from the TCU or from pushbuttons on the operator and maintenance panels of the Magnetic Tape Transport Unit.

2-228. After the direction of tape motion has been selected, the actual motion of the tape is controlled by the capstan-drive and brake-control circuits, which apply pressure or vacuum to the capstan and pneumatic brake port.

2-229. In the drive condition, vacuum is applied to the forward or reverse capstan while vacuum is removed from the brake port. The tape is held against the rotating capstan and moved across the read/write heads. In the clear or nondrive condition, vacuum is applied to the brake port while pressure is applied to both capstans. The tape, in this case, is held against the brake port but separated from both rotating capstans.

2-230. SERVO-DRIVE LOGIC. The servo-drive logic circuits monitor and control the length of the tape loop in each of the vacuum columns. The servo-drive logic function is provided by two circuits, a photosense circuit and a tachometer circuit.

2-231. Each vacuum column contains an upper and lower photocell network. The photocells, when illuminated, indicate that the tape loop is above the respective photocell since the light source which illuminates the photocell has not been blocked by the tape. When both the upper and lower photocells are illuminated, an indication that the tape loop is too short, more tape is supplied to the column. When the tape is positioned so only the lower photocell is illuminated, this indicates that the takeup reel must be braked to maintain the tape loop in this position. When the tape is positioned within the vacuum column to block light to both the upper and lower photocells, this indicates that tape must be removed from the column by the takeup reel.

2-232. The outputs from the photocells are amplified and applied through inverters to the brake, clockwise (CW), and counter-clockwise (CCW) relay pullers, which cause the takeup reel to be either braked or driven in the CW or CCW direction.

2-233. The tachometer circuit prevents the application of drive pulses to the reel motor circuit when tape speed into or out of the vacuum storage columns exceed capstan speed by approximately 10 feet per second. The maximum speed of the reel motor is thus limited in order to reduce the time required to stop the reel.

2-234. LOCAL CONTROL LOGIC. The local control logic circuits consist of sense circuits as well as those control circuits that are activated by manual switches on the Magnetic Tape Transport Unit or signals from the TCU. Sense circuits within the local control logic perform the following functions:

- a. Ready. This sense circuit, when set, indicates that the tape is under external control (ready). A not-ready condition indicates that the tape unit is under manual control and cannot communicate with the TCU.

b. Sense End of Tape (EOT). This circuit detects the end of tape reflective marker and (1) turns on the EOT indicator on the maintenance panel, (2) returns an end-of-tape signal to the TCU, (3) stops the tape motion if Magnetic Tape Transport Unit is under manual control.

c. Fault. The fault circuit stops operation when any one of the following fault conditions is detected:

- (1) The pneumatic switches are open, indicating that the tape has been removed from the vacuum column.
- (2) Fault switch on maintenance panel has been depressed.
- (3) Capstan and pump motors are off.
- (4) Presence of an external or local Master Clear.

d. Sense Load Point. This circuit detects the load point reflective marker and stops tape motion when the marker is positioned over the photocell.

2-235. In addition to the sense circuits described in the previous paragraphs, the local control logic also includes several additional circuits which:

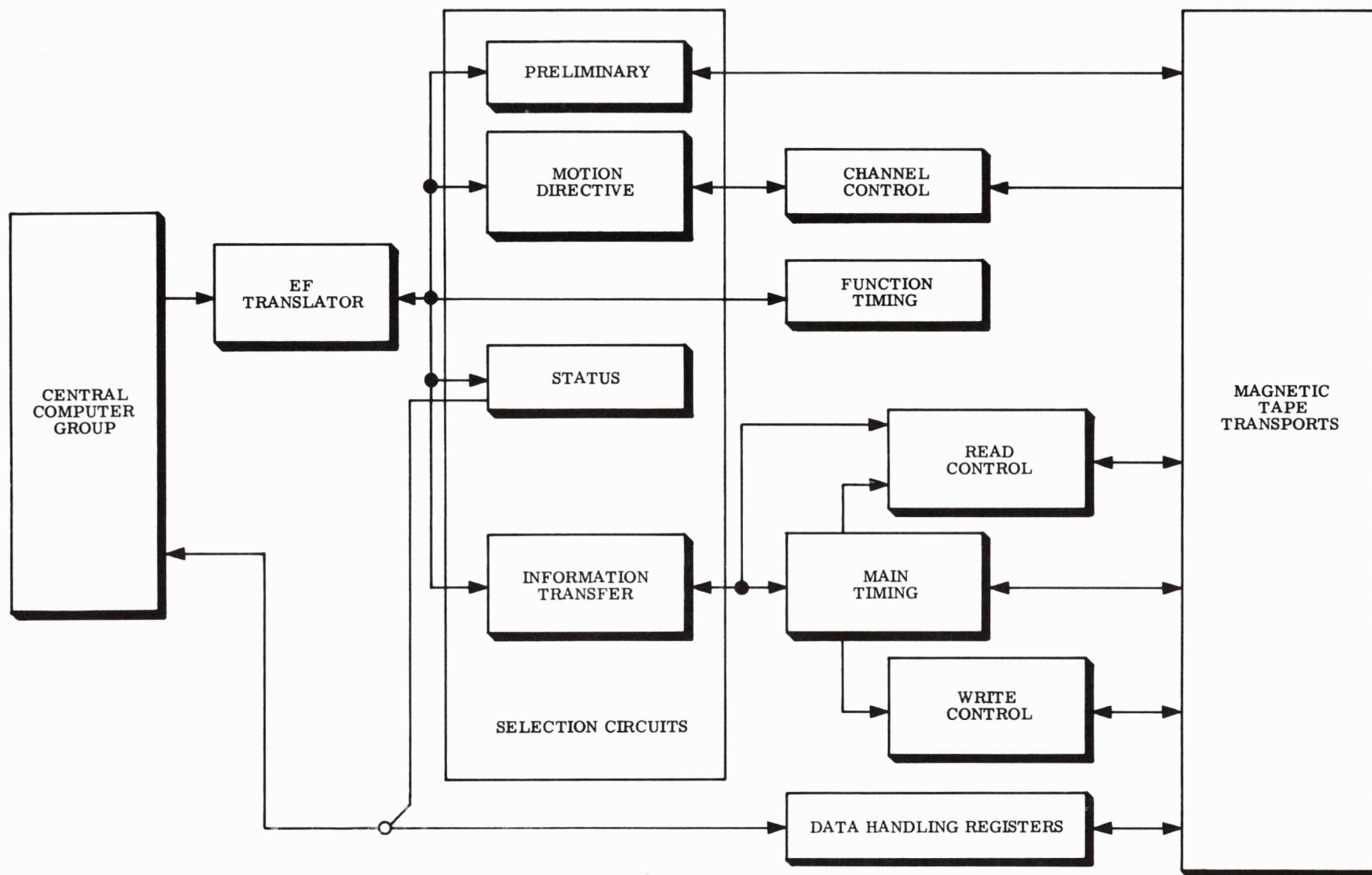
- a. Extend the pressure pad prior to low-speed operation (pad extend circuit).
- b. Allows tape to be moved from an unloaded status (all tape on the supply reel) to the tape-loaded status (tape at load point).
- c. Allows tape to be rewound from the takeup reel to the supply reel at a rate of over 350 inches per second, until a load point mark is sensed (rewind).
- d. Permits reversals of tape at high speed from takeup reel to supply reel until all tape is rewound on supply reel (rewind unload).

2-236. TAPE CONTROL UNIT.

2-237. The magnetic tape synchronizer (tape control unit) provides communication between the ACE-S/C system, Central Computer Group, and the four Magnetic Tape Transports. The tape control unit also makes possible communications between the Magnetic Tape Transports and the Line Printer. Figure 2-16 is a simplified block diagram depicting the major functions of the tape control unit. The tape control unit, activated by EF codes from the Central Computer Group, performs the following functions:

- a. Controls the four Magnetic Tape Transports.
- b. Transfers information back and forth between the Central Computer Group and the selected Magnetic Tape Transport.
- c. Converts the data representation to a usable format.

2-238. The status selection circuits permit the Central Computer Group to determine the condition of both the tape control unit and the selected Magnetic Tape Transport. The status selection circuits generate a pseudo input-word to the Central Computer Group which reflects



AD2-12-9

Figure 2-16. Tape Control Unit Logic Block Diagram

the existing conditions. This status word is forwarded to the computer on an input-to-A instruction.

2-239. Selection of a particular Magnetic Tape Transport is made by the initial EF code from the computer. A specific Magnetic Tape Transport is chosen for an operation by means of a comparison between the last digit in the EF code and the setting of the selection switch, located near the top of each Magnetic Tape Transport. The responsibility for determining the appropriate Magnetic Tape Transport rests with the channel control circuit.

2-240. The preliminary selection circuits permit selection of:

- a. High or low density.
- b. Odd or even parity.
- c. 12-bit or 6-bit word format.

2-241. The motion directive selection circuits recognize the appropriate computer select code and initiate any of the following motion directives to a selected Magnetic Tape Transport:

- a. Search forward to file mark.
- b. Search backward to file mark.
- c. Backward one record.
- d. Rewind load.
- e. Rewind unload.

2-242. The information transfer selection circuits, in conjunction with the main timing circuits, sequence the information and register transfers necessary for an operation. The main timing chain is triggered for the following functions:

- a. Each character written on the tape.
- b. Each character read from the tape.
- c. Each of the four spaces in a check character gap.
- d. Each status response.
- e. For assembling an odd number of words in a read operation.

2-243. The function timing circuit sequences selection and transmission of the control signals to a Magnetic Tape Transport. The control signal outputs of the circuit are a series of gates. The start of these gates is determined by circuit delay elements.

2-244. Upon receipt of suitable select codes from the Central Computer Group, the function timing circuit control signals activate circuits that initiate write and forward signals to the Magnetic Tape Transport. The write control circuit generates the signals to the Magnetic Tape Transport which initiates forward motion of the tape and the write operation.

2-245. The function timing circuit also enables the read control circuit when activated by an appropriate select signal. The read control circuit, in turn, sends suitable signals to the Magnetic Tape Transport which enable tape motion and the activation of the read heads.

2-246. The data handling registers process the read and write data as it passes through the tape control unit. The registers are able to handle both the 12-bit word (Assembly Mode) and the six-bit word (Character Mode) data. The data handling registers are also flexible in regard to selection of parity bits. In binary format, the parity bit is chosen so that the total number of 1 bits in any line is odd. In the BCD format, the total number of 1 bits in any line is even.

2-247. In addition to on-line operation, the Magnetic Tape Transports can be utilized for off-line operations. During off-line operation, the tape control unit facilitates communication between the Magnetic Tape Transports and the Line Printer.

2-248. CARD PUNCH CONTROLLER AND CARD PUNCH.

2-249. The Card Punch Controller serves as a signal adapter between the Central Computer Group and the Card Punch.

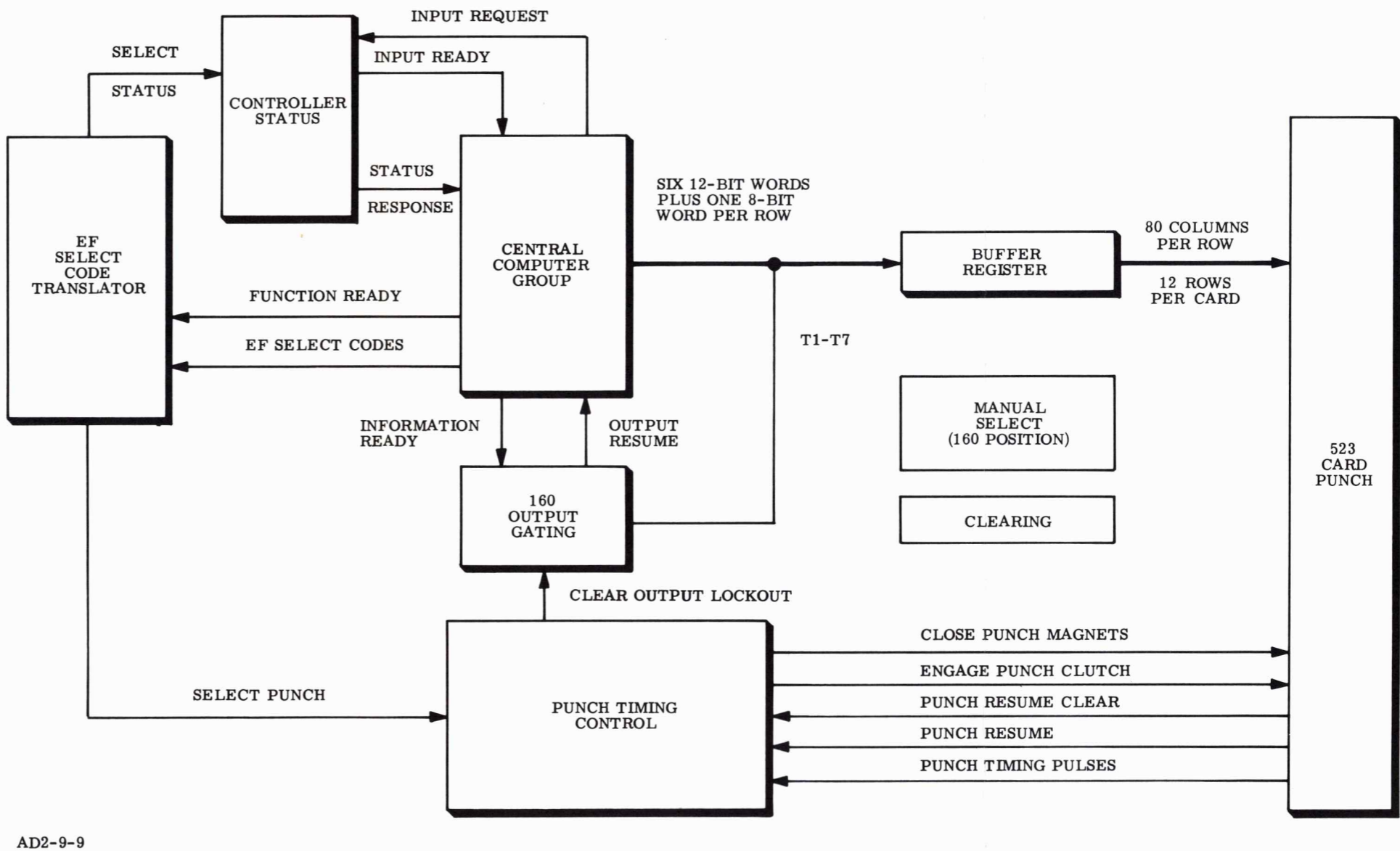
2-250. The Card Punch Controller provides four basic interface functions:

- a. Recognizes and translates EF codes from Central Computer Group.
- b. Generates and forwards Card Punch status response and Input Ready signals.
- c. Provides temporary storage of computer data to be punched on cards.
- d. Controls transfer of data from computer to Card Punch.

2-251. The Card Punch Controller (figure 2-17) contains those circuits required to achieve compatibility between the Card Punch and the Central Computer Group. The EF select-code translator monitors the computer EF select codes, recognizing those intended for the Card Punch. Translations of EF select codes fall into two general categories: those which request status signals, and those which require a card-punching operation.

2-252. When a status response signal to the Central Computer Group is required, the EF select code translator activates the controller status circuit which in turn generates the status response signal. The status circuit also provides the Central Computer Group with Input Ready signals.

2-253. When a translated EF select code requires a punch operation, the punch timing control circuit is activated by a select-punch signal from the EF select code translator. The punch timing control circuit coordinates the transfer of input data to the Card Punch at a rate which is acceptable to the Card Punch. The computer output gating circuit, in response to



AD2-9-9

Figure 2-17. Card Punch Controller Logic Block Diagram

clear output lockout signals from the punch timing control, controls the transfer of data from the Central Computer Group to temporary storage in the buffer register.

2-254. The buffer register provides storage facilities for one Card Punch cycle. The Card Punch operates on each of the 12 rows on a card, one row at a time. Since each cycle punches one row of the card, which contains 80 columns per row, the buffer register has a capability for storing 80 data bits in parallel. The Central Computer Group input to the buffer register consists of seven 12-bit words, the last word consisting of only eight active bits (total of 80 bits).

2-255. The Card Punch operates on each card row by row; therefore requiring that the Card Punch controller cycle 12 times to complete the punching operation for each card.

2-256. X-Y PLOTTER.

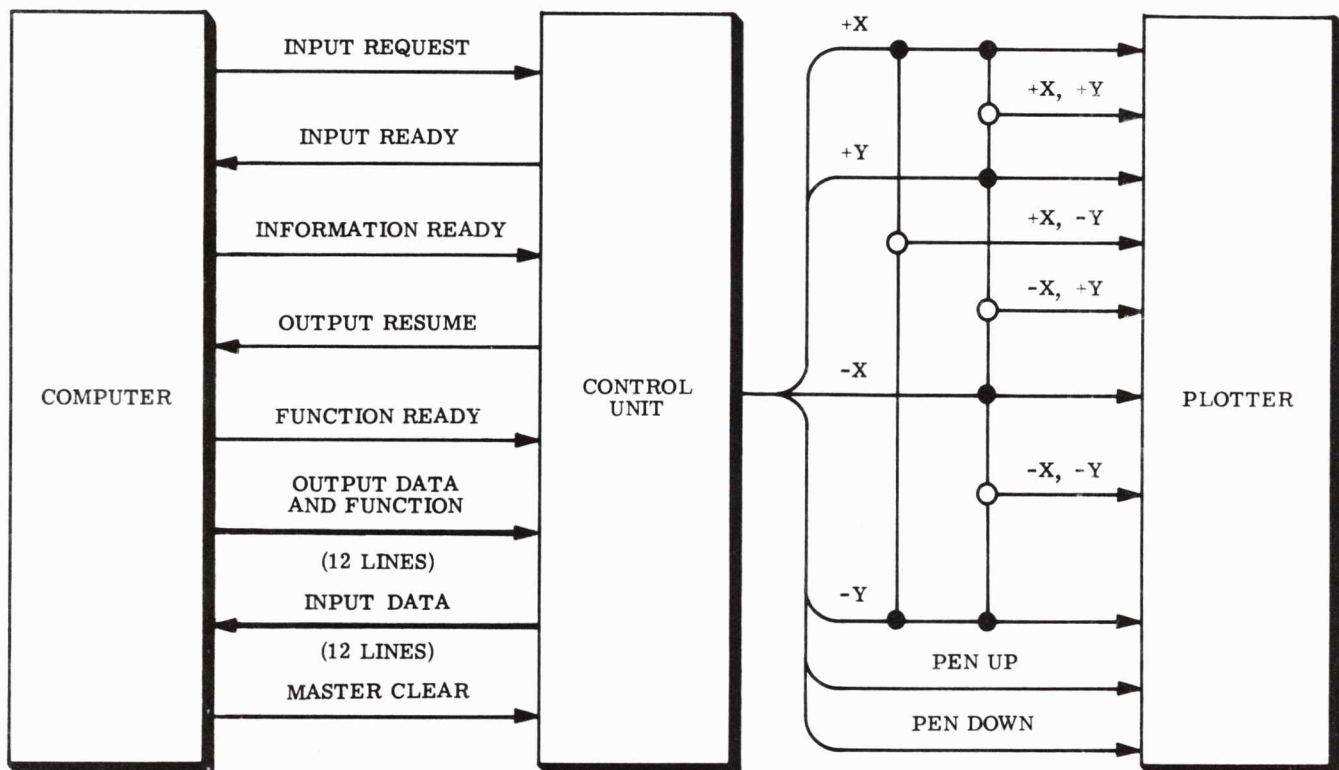
2-257. The X-Y Plotter is a high-speed, two-axis recorder that can trace a visible plot of one variable against another. The plot is accomplished by means of a carriage-mounted ballpoint pen, writing on paper placed on a bidirectional recording drum. A paper feed and takeup mechanism handles paper rolls 12 inches wide by 100 feet long. Recording drum sprocket teeth engage sprocket holes in the paper in order to drive the paper past the pen. The plotter control unit provides the interface between the computer and the actual plotter mechanism (figure 2-18).

2-258. The control unit interchanges signals by means of 12 data input lines, 12 data output lines, and several additional lines for the transfer of control signals. The 12 output lines from the computer to the plotter control unit carry either a 12-bit EF function code or 12 data bits that are required to initiate a segment of the plot. Each plot segment moves the ballpoint pen (in relation to the paper) 1/100 inch.

2-259. Each 12-bit output data word from the computer causes a line segment to be scribed in one of eight directions (figure 2-19), or to raise or lower the pen. Movement in the horizontal direction, either left (-X) or right (+X) is accomplished by moving the pen carriage. Movement in the vertical direction, either up (+Y) or down (-Y), is accomplished by rotating the drum. Movement in directions having both X and Y components is accomplished by simultaneously moving both the pen carriage and the drum.

2-260. A total of 12 different 12-bit parallel words may be sent from the computer to the plotter control unit over the output data and function lines:

- a. EF - write operation.
- b. EF - read operation.
- c. through j. - eight directions of pen movement.

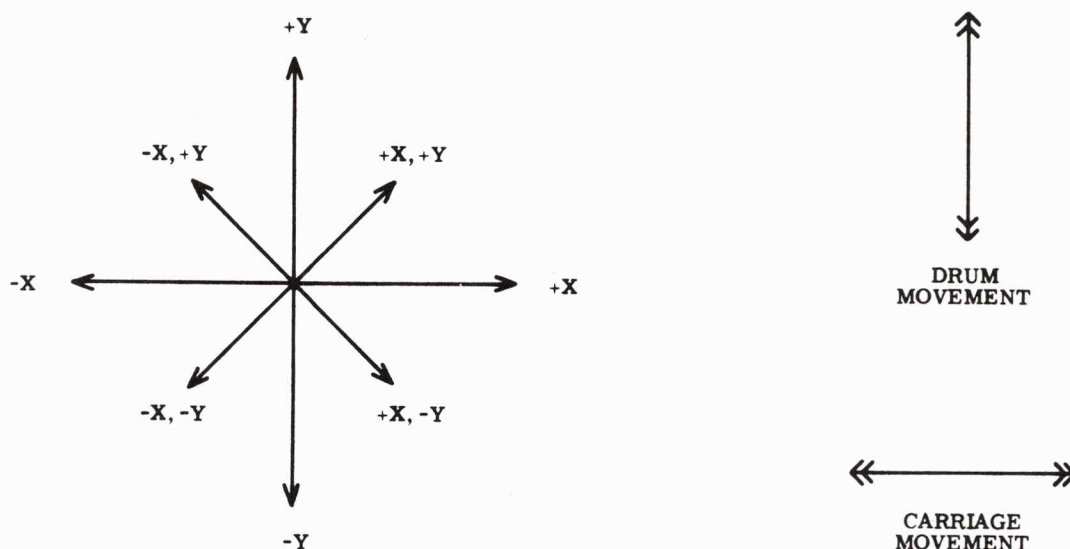


AD2-10-9

Figure 2-18. X-Y Plotter Simplified Block Diagram

- k. Pen up.
- m. Pen down.

2-261. The Read Mode of operation sends a 12-bit word to the computer reflecting the setting of manual switches located on the control unit. The manual switches are set and read into the computer for special applications.



AD2-11-9

Figure 2-19. X-Y Plotter Motion Coordinates

2-262. TYPEWRITER.

2-263. The Control Data 161 Typewriter serves as an input/output device for the ACE-S/C system Central Computer Group. The Typewriter unit consists of an electric typewriter and a logic control chassis. A d-c power supply is also contained within the Typewriter unit.

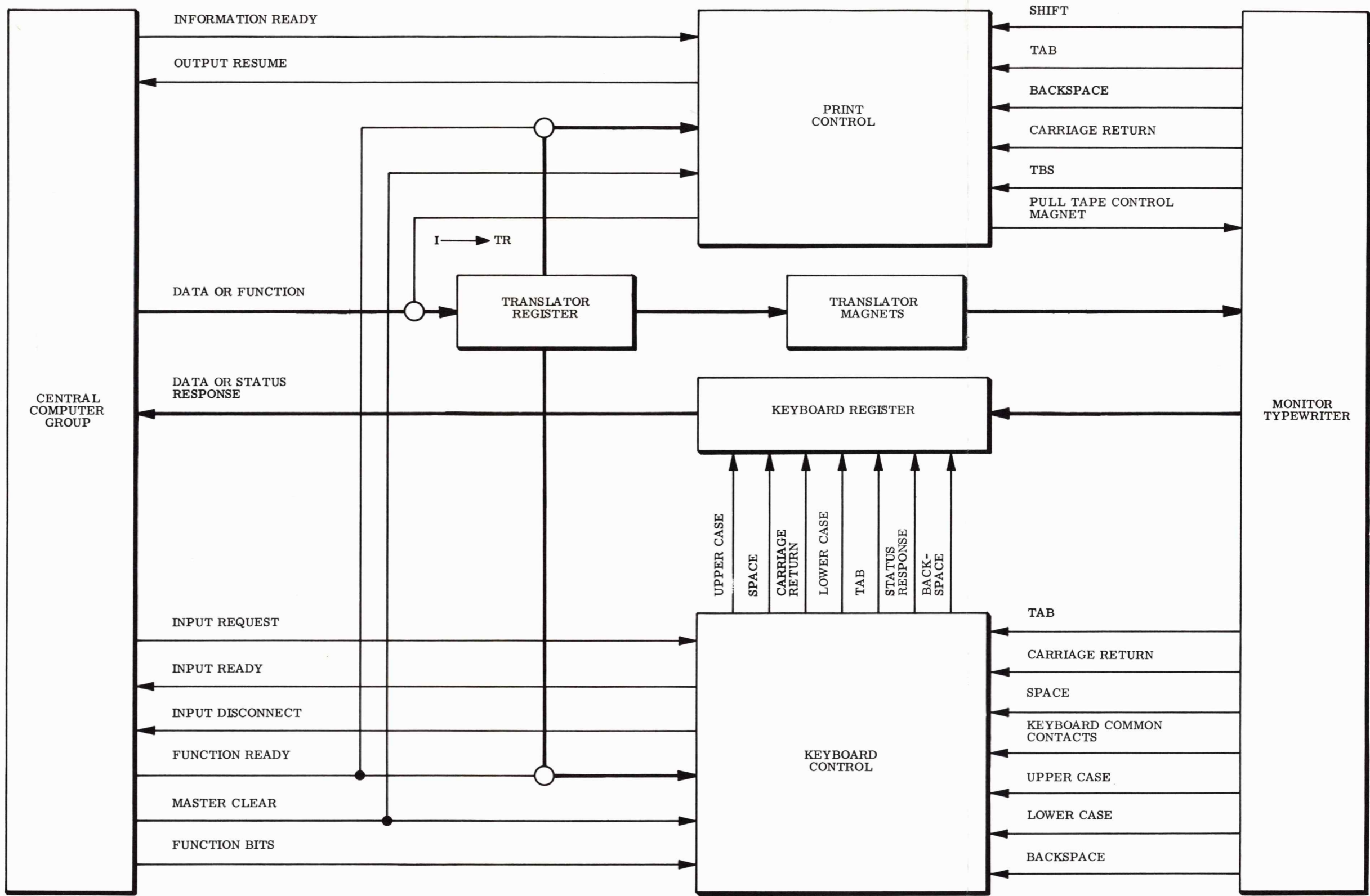
2-264. The Typewriter operates at a rate of approximately 10 to 12 output characters per second and may be used as either a keyboard input device or as an output device for producing printed copy. The Typewriter unit provides the Central Computer Group with a flexible input/output device. Through this medium, data may be entered manually into the computer, or, in the Output Mode, monitoring information may be received from the computer and read out in printed form by the Typewriter.

2-265. Figure 2-20 illustrates the major functions of the Typewriter unit. All typewriter characters and functions are represented by unique combinations of six bits. When the Typewriter unit is used as an input device, striking a character key causes keyboard contact settings to be encoded and forwarded to the keyboard register as a six-bit character code. Keyboard functions, such as tab, carriage return, space, etc., are also represented as contact settings and are routed to the keyboard control circuit. During an input to the computer operation, the keyboard control circuit enables the sampling of the keyboard common contacts and allows the circulation of data in the keyboard register. The keyboard control circuit prevents the return of an Input Ready signal to the computer during a character action, except when a request for keyboard input or status response has been made. The keyboard control circuit also provides status response signals to the keyboard register for transmission to the computer.

2-266. To type a character, the computer forwards an Information Ready signal to the print control circuit. The character code from the computer is then gated into the translator register by an I → TR signal from the print control circuit. The translator register converts the six-bit character code to a unique arrangement of energizing signals to six Typewriter translator magnets. An additional Typewriter tape control magnet (TCM) also is energized to start the print cycle and to activate a TBS contact closure which clears the input for another Information Ready signal.

2-267. DATA TRANSMISSION EQUIPMENT.

2-268. The data transmission equipment consists of Data Transmission and Verification Converters (DTVC) that serve as an interconnecting or communications link between the command computer and various remote units. There are three DTVC units in the uplink or command loop. The DTVC's relay the various commands from the computer to the stimuli generators located in the test bays. The commands are verified for correctness, and verification signals then are routed back from the test bays to the computer via the DTVC. The DTVC accepts 12-bit parallel commands from the computer, and transmits the commands in serial form over the hardlines. The DTVC receives 24-bit serially coded words from the remote units, assembles and stores the first 12 bits, then performs a bit-by-bit check of the second word with the first word. The DTVC then presents a 12-bit parallel coded word to the computer whether correct or in error. When an error is detected, interrupt, disconnect, and status signals are made available to the computer. Various modes of operation and equipment configuration are discussed in the following paragraphs.



AD2-13-9

Figure 2-20. Typewriter Logic Block Diagram

2-269. TRANSMISSION.

2-270. The DTVC operates in a Transmit Mode where data is received in a 12-bit parallel mode and is transmitted in a 24-bit redundant serial mode. Twelve-bit words are received from the computer under ready/resume control. Each is placed in a register and the contents of consecutive stages of that register are transmitted over the serial communication link. When all 12 bits have been transmitted, the contents of the register are retransmitted to provide 100 percent redundancy with no delay between transmissions. Transmission begins with the least significant bit.

2-271. RECEPTION.

2-272. The DTVC receives serial 24-bit words, assembles and verifies 12-bit words, and presents them to the computer in parallel. All 12-bit words are sent to the computer whether correct or in error. If insufficient bits are received to form a 12-bit word, the DTVC completes the word by adding zeros and sends the word to the computer. The first 12 bits of each 24-bit word are assembled in a register. Each of the second 12 bits, as it is received, is compared with the corresponding bit of the assembled word to verify the accuracy of the transmission. Upon detection of an error, interrupt, disconnect, and status signals are made available to the computer. The interrupt and disconnect signals are optional under manual control.

2-273. STATUS RESPONSE.

2-274. The DTVC sends status response signals to the computer that indicate one of the following conditions:

- a. Error was/was not detected during verification.
- b. Fake Ready signal was/was not generated.
- c. Interrupt signal was/was not produced.

2-275. These signals are available for interrogation by the computer until a function other than select status is received by the DTVC.

2-276. FUNCTION WORDS.

2-277. The DTVC receives 12-bit function words from the computer. These words are interpreted by the DTVC as follows:

- a. Bits 0 through 2 indicate the DTVC function requested by the computer.
- b. Bits 3 through 5 designate the desired serial channel.
- c. Bits 6 through 11 designate the equipment.

2-278. RECEIVE INTERRUPT.

2-279. In the Receive-Interrupt Mode of operation, the DTVC examines the first word of each block of data appearing on the transmission link. The upper six bits of the word are compared with manual preset switches. When the selected bit configuration is found, an interrupt signal is sent to the computer. The least significant of the lower six bits is used to provide the option of choosing one of two interrupt lines. This first word and all following words in the block are made available for parallel transmission to the computer. The interrupt status indication is generated when this interrupt occurs.

2-280. INTERRUPT ON ERROR.

2-281. An error interrupt switch is provided to allow an interrupt on error. When this switch is in the error interrupt position, an interrupt signal is sent to the computer when an error is detected during verification. An error status indication provides in either case for sensing by the computer, and the interrupt status indications are not generated.

2-282. INTERRUPT ON FAKE READY.

2-283. If a request for data has been issued to the DTVC and data is not received within the selected period of time, a Fake Ready signal is sent to the computer, and a Fake Ready status indication is provided for sensing by the computer. When the Fake Ready interrupt switch is set, an interrupt signal is sent to the computer when a Fake Ready signal is generated.

2-284. DATA TRANSMISSION AND VERIFICATION CONVERTER FUNCTIONS.

2-285. The DTVC operates under program control of a digital computer and communicates in a parallel mode with that computer over a standard input/output communications channel. The DTVC will be able to communicate with another DTVC or similar device in a serial mode over a long-distance communications link. Serial data will be transmitted with 100 percent redundancy for verification by the receiving unit. The DTVC has two basic modes of operation: Transmit and Receive. The unit remains in the Monitor or Receive Mode until the computer is ready for a transmission.

2-286. TRANSMIT MODE.

2-287. In the Transmit Mode, data is received as a 12-bit parallel word and is transmitted as a 24-bit redundant serial word. Each word is placed in a register and the contents of consecutive stages of that register are transmitted over a preselected serial communications channel. When all 12 bits of the word have been transmitted, the contents of the register will be retransmitted to provide 100 percent redundancy with no applicable delay between the transmissions.

2-288. RECEIVE MODE.

2-289. The DTVC in the Receive Mode receives a serial 24-bit word. The first 12 bits of each 24-bit word are loaded into a register. Each of the second 12 bits, as they are received, will be compared with the corresponding bit of the assembled word to verify the accuracy of the transmission. Upon detection of an error, an interrupt signal will be made available to the computer. All 12-bit words will be presented to the computer whether correct or in error. If insufficient bits are received to form a 12-bit word, the word will be completed by the addition of zeros and presented to the computer.

2-290. TRANSMIT CYCLE.

2-291. Figure 2-21 shows the DTVC operating in conjunction with the computer acting as a communication link between the computer and the uplink to the spacecraft. For the computer to facilitate the data flow to the DTVC, preliminary conditions (channel selection, etc.) must be established between the two pieces of equipment, and the DTVC must be in the Transmit Mode. This condition is attained through the use of control signals which is essentially the raising or lowering of lines. Prior to entering a presentation on data flow and time sequenced events, it is necessary that the following control signals be established:

- a. Function Ready. This signal is generated by the computer and transferred to the DTVC, indicating that a function code is available for translation.
- b. Information Ready. This signal is generated by the computer and transferred to the DTVC, indicating that a data word is available for transmission.
- c. Output Resume. This signal is generated by the DTVC and is a response to receiving the Function Ready or Information Ready and indicates to the computer that the word has been accepted and is ready for another.
- d. Input Ready. This signal is generated by the DTVC and transferred to the computer, indicating that the DTVC has CSR for the computer.
- e. Input Request. This signal is generated by the computer and transferred to the DTVC, specifying that the computer is ready for an input word.
- f. Interrupt. This signal is generated by the DTVC and transferred to the computer, indicating the status of the transmission. It causes the computer to interrupt the main program and to take action on the incoming data word.
- g. Master Clear. This signal is generated by the computer and is transferred to the DTVC to establish initial operating conditions.

2-292. If the computer has information to be transmitted over the serial communications channel, the computer must select the proper DTVC and determine which one of several serial channels is to be utilized. To facilitate this, the computer generates a 12-bit function

code. The most significant six bits select the proper DTVC, and the least significant six bits select the proper channel within the DTVC and the operation required. The following sequential steps indicate how the computer and DTVC communicate to effect the proper conditions for a data word transmission. For explanation purposes, it is assumed that the DTVC is in the Monitor Mode.

- a. The computer transmits a 12-bit EF code to the DTVC over the normal data lines.
- b. A Function Ready signal is transmitted to enable the DTVC to recognize the input function code.
- c. The translation of the EF code puts the DTVC into the Select Receiver Mode and selects the serial data channel to be utilized.
- d. An Output Resume is then transmitted to the computer to indicate that the DTVC is ready to receive the data word. The Output Resume causes the Function Ready to drop. In turn the Output Resume drops.
- e. The computer generates an Information Ready, indicating to the DTVC that a 12-bit data word is available for transmission.

2-293. The DTVC is now in the condition to accept the 12-bit data word from the computer for transmission over the serial data channel selected.

2-294. The computer after transmission of the EF code places a 12-bit parallel data word on the output lines (refer to figure 2-21). DTVC control logic (Information Ready) enables 12 parallel gates in the transmit loop to facilitate the data transfer to the assembly (A) register. The contents of the A register is gated immediately to the exchange (X) register in parallel format. Upon completion of this transfer, the 12-bit word is now ready to be transmitted. The transmit or timing enable is sent from control to the timing unit to gate the clock pulses out to the counter. The counter, a chain of flip-flops, sequentially gates the contents out of the X register; i.e., the contents of register No. 1 at time 1, register No. 2 at time 2, etc. By gating sequentially the contents of the 12-bit register, the parallel word is shifted to serial form. To perform the 100 percent redundancy required, the counter gates out the contents of the X register a second time. The serialized data is transferred to the transmit pyramid. The function of the transmit pyramid is to convert the 24-bit digital input to a split-phase modulated signal containing the intelligence transferred out of the X register. The output split-phase data is transferred to a line for transmission over the serial communications channel.

2-295. If the DTVC is utilized for transmission of data to the uplink receiver/decoder, two 12-bit data words must be transferred out of the computer for transmission. In the previous discussion, a 12-bit word was transferred to the DTVC and transmitted by the DTVC as a 24-bit redundant word. As the last bit is being gated out of the X register, the A and X

registers are cleared; i.e., the output sides are set to zero. The DTVC at this time generates an Output Resume to the computer. This signal indicates to the computer that the first 12-bit word has been serialized, redundancy performed, the word transmitted uplink, and that the DTVC is ready for another 12-bit word. The computer generates an Information Ready signal indicating to the DTVC that another data word is on line for transmission. For the second word transmission the above steps will be repeated.

2-296. RECEIVE CYCLE.

2-297. After each transmit cycle, the DTVC will, after an interword null, return to the Monitor Mode ready to receive data over the last channel selected. Prior to entering the receive cycle, the following conditions are established:

- a. Computer has transmitted a 12-bit function code to the DTVC containing the channel selection and places the DTVC in the Select Receive Mode. As previously stated, the DTVC is in the Monitor Mode; however, no data will be outputted to the computer until the select receive circuit has been enabled.

- b. After translation of the function code, an Output Resume is generated. This causes the computer to drop the Function Ready signal which in turn drops the Output Resume. The DTVC is now set to receive the incoming data over the serial channel selected.

2-298. The split-phase data containing the information from the remote equipment is received by the bit and timing detector, which changes the incoming serial waveform to digital information and provides timing for word assembly and error detection. The output serial data is fed to the receive pyramid. Timing, a resultant of the first detected bit, is fed to the counter to start the gating cycle and to transfer the serial data from the receive pyramid sequentially into stages 1 through 12 of the A register. Each incoming bit causes the counter to change one step, therefore bit No. 1 is gated into stage No. 1 and bit No. 2 is gated into stage No. 2, etc., until all 12 stages have been set. This action converts the serial data to parallel data. The data is immediately gated into the X register as 12 parallel bits. Bits 13 through 26, that is, bits 1 through 12 of the redundant portion of the 24-bit word, are gated into the error comparator to be compared with the 12 bits now contained in the X register. To expedite the data transfer, the contents of the X register are gated into the error comparator as the 24th bit of the redundant word is gated in the comparator. After comparison is made and no error is detected, the DTVC will generate an Interrupt 30, indicating to the computer that the redundancy checked. If redundancy failed, the DTVC will generate an Interrupt 40 indicating to the computer that an error was detected.

2-299. As bit No. 13 is gated into the A register, the DTVC generates an Input Ready signal to the computer, indicating that data is on line. If the computer is ready to receive data, an

Input Request will be generated by the computer to the DTVC. During the exchange of control signals between the computer and the DTVC, the transfer from the A to X register is effected. The contents of the X register will now be gated out to the computer by the receive enable from the DTVC control.

2-300. Again, if the DTVC is acting in the capacity of the uplink communications transmitter, the select receive remains intact and the second 24-bit redundant word is accepted and the above process repeated.

2-301. A complete transmit and receive cycle has now been completed. Should the computer desire to transmit another word and/or words, an exchange of control signals will be effected.

2-302. PROGRAM CONTROL.

2-303. FUNCTION SELECTIONS. For the DTVC to operate as a communications channel between the computer and remote equipment, it must operate under program control. The following function select signals allow the DTVC to be controlled by computer program.

a. Select Transmit. Prepares the equipment to receive 12-bit parallel words from the computer and transmit 24 serial bits for each word received on one of the available channels. The equipment remains in the mode until an interword null is detected. After the detection of an interword null the DTVC goes to the Monitor Mode.

b. Select Receive. Prepares equipment to receive 24-bit words in serial mode on one channel, assemble and verify 12-bit words, and present the words in parallel to the computer. The Monitor Mode differs from the Select Receive Mode in that the received data will not be transferred to the computer until the select receive is enabled.

c. Select Interrupt. Prepares the equipment to monitor data on one channel and compares the upper six bits of the first word with the positions of a predetermined selection of six switches. If the two match and no error is detected, an interrupt signal is activated (see interrupt code word below).

2-304. SWITCH SELECTIONS. Under program control, the computer may select various types of DTVC internal modes. However, to satisfy the type of operation determined by the program, selection switches must be preset to either a condition or a not-condition. The following selection switches are located on the operator's panel of the DTVC and are selected in accordance with the applicable programming method.

a. Interrupt Code Word (ICW). The position of these six switches determine the interrupt code word. The up position inserts a 1 and the down position inserts a 0. The normal configuration of these switches will be 110101 (see Select Interrupt above).

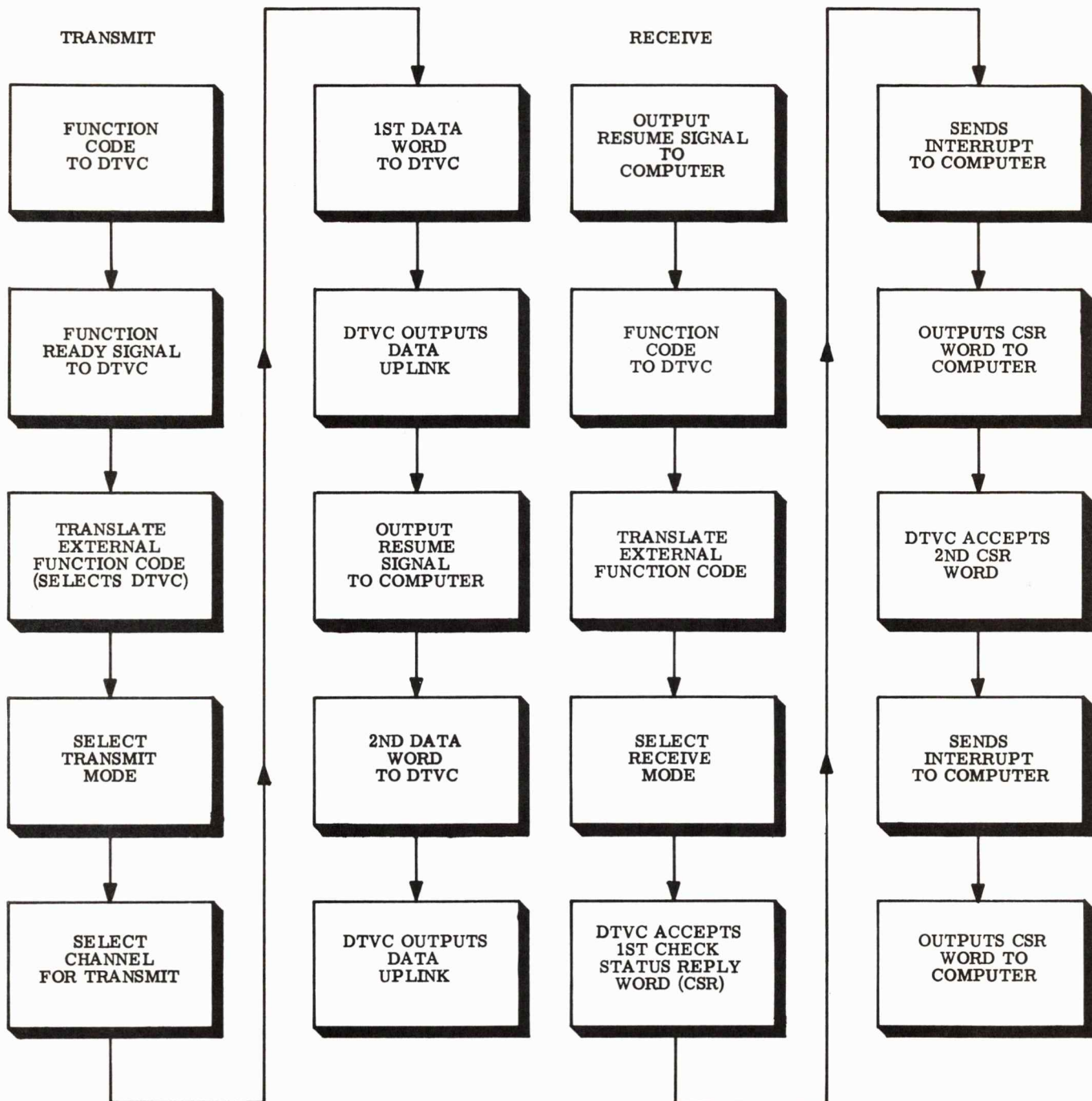
b. Interrupt On Error. The position of this switch when in the IOE position will generate an Interrupt 40 if the incoming data word and the interrupt code word match.

c. Simulator. These switches consist of a simulator switch controlling the action of the simulator, a transmit switch controlling the length of the transmission, a group of 12 switches for data word configuration, and a Master Clear switch to reset all registers affected by the simulator action.

d. Word Space Control. This controls the spacing between each transmitted word and is variable. This switch has ten positions with the following microsecond delays:

- (1) 5.
- (2) 10.
- (3) 25.
- (4) 50.
- (5) 100.
- (6) 600.

e. Computer/DTVC Uplink Routine. The DTVC operation under the 160G Computer program control operates as an uplink communications unit in accordance with the following sequential routine as shown in figure 2-22.



AM2-8-5

Figure 2-22. Data Transmission and Verification Converter
Operational Flow Chart

SECTION III

DISPLAY AND RECORDING EQUIPMENT

3-1. INTRODUCTION.

3-2. The Display and Recording Equipment is comprised of those units of the ACE-S/C system that receive, process, and display the spacecraft responses to test stimuli. For purposes of presentation, the Display and Recording Equipment is divided into three functional parts: (1) data acquisition and decommutation, (2) analog and event display, and (3) alphanumeric display.

PART 1

DATA ACQUISITION AND DECOMMUTATION EQUIPMENT

3-3. DATA ACQUISITION AND DECOMMUTATION EQUIPMENT FUNCTIONS.

3-4. The Data Acquisition and Decommutation Equipment acquires, synchronizes, records, and distributes the test data received from the spacecraft test area. The units of the ACE-S/C system that perform these functions are illustrated in figure 3-1.

3-5. The Video Distribution and Tape Transport Control Unit is the receiver and distributor of all incoming test data from the spacecraft test area. Three types of test data are received over separate transmission hardlines: (1) interleaved serial PCM digital words, (2) airborne PCM digital words, and (3) FM signals. The distribution of the received test data is accomplished by means of Video Distribution and Tape Transport Control Unit patch-panel assemblies and the appropriate patch-panel coax jumper connections. The distribution of the received data is as follows:

- a. Airborne PCM test data to both decommutators simultaneously and to a recording channel on one of three wideband magnetic tape recorders.
- b. Interleaved PCM test data to both decommutators simultaneously and to a recording channel on one of the tape recorders.

c. FM test data to the FM Discriminator Unit and to a recording channel on one of the recorders.

3-6. The decommutator units synchronize with the PCM data they receive, decommutate it, and convert it to several output forms that are then sent to the analog and event display units and to the alphanumeric display units.

3-7. The FM Discriminator separates the test data contained in the FM signals it receives and converts the data to analog voltages that are sent to the analog and event display units.

3-8. The magnetic tape recorder units provide a permanent record of all test data received by the ACE-S/C system. The data recorded on magnetic tape can be played back as required. The playback PCM data is routed to the Video Distribution and Tape Transport Control Unit patch panels and is continuously distributed to the decommutator units. The playback FM data also is routed to the patch panels but requires special patching connections to be sent on to the FM Discriminator Unit.

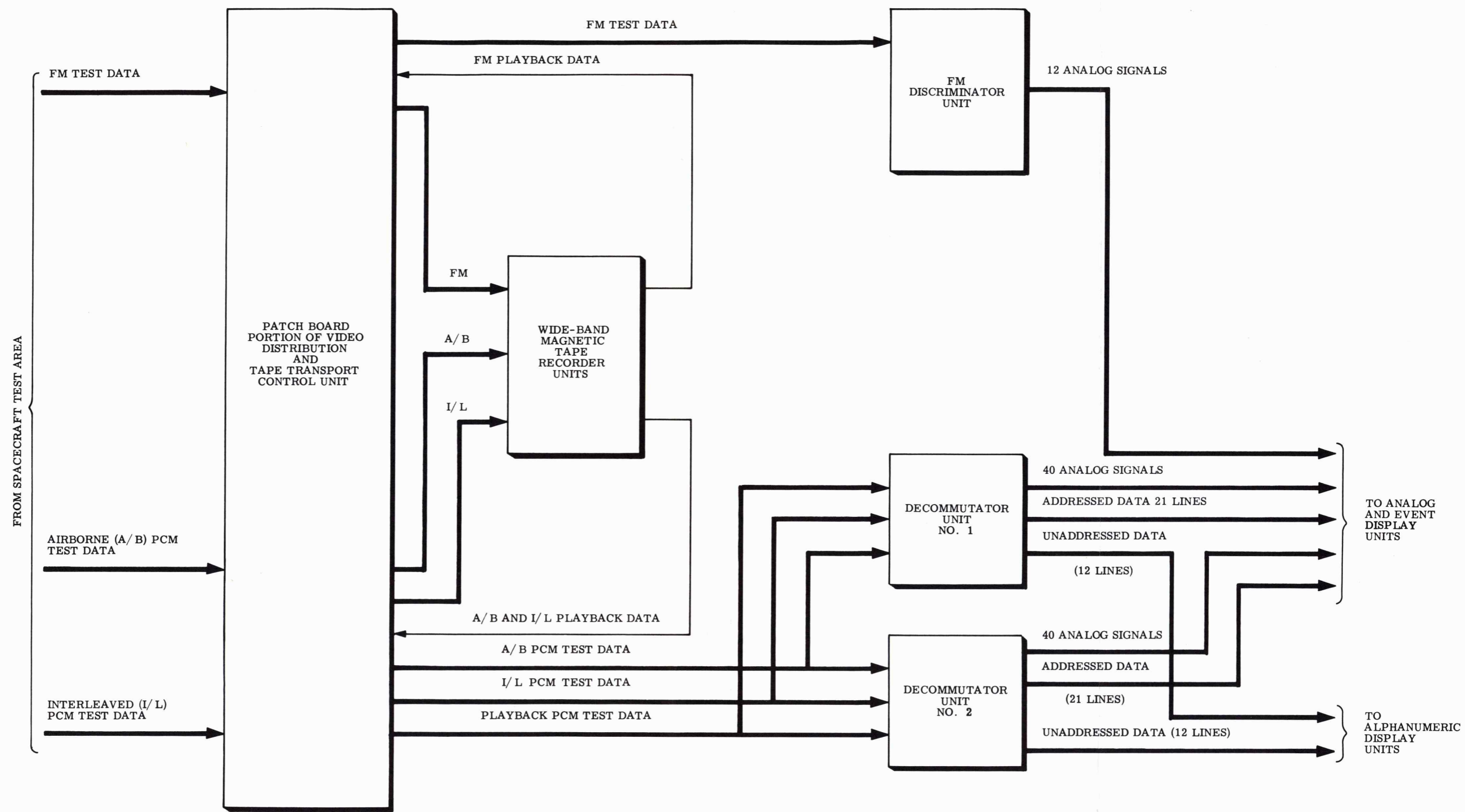
3-9. The PCM test data received from the spacecraft test area via the Terminal Patch Facility contains information obtained from sensors that are permanently installed in the spacecraft, from carry-on equipment that is removed prior to launch, and from ground service equipment. A composite signal containing all sensor information is developed by units in the spacecraft vicinity and is received at the input to the data acquisition and decommutation units as I/L PCM test data. The test data obtained from the permanently installed spacecraft sensors also is received as a separate second PCM input and is called A/B PCM test data. Certain test data (e.g., outputs of vibration sensors), which is required in a raw form, is received in the form of FM signals. The following paragraphs describe each of the received test data formats in detail.

3-10. INTERLEAVED PCM TEST DATA DESCRIPTION.

3-11. Interleaved test data is comprised of data from three primary input sources:

- a. Command Module flight telemetry equipment (permanently installed spacecraft equipment). Data from this source is called airborne PCM test data.
- b. Command Module carry-on equipment (removed prior to launch).
- c. Ground service equipment.

3-12. The data from these sources is in the form of split-phase PCM telemetry signals and is received as a continuous serial bit stream. The rate of the incoming data bits is 204.8 kilobits per second. The data is organized into subframes that are received at the rate of one a second. Each subframe comprises 50 prime frames. Each prime frame is composed of 512 eight-bit data word time slots.



AM2-21-3

Figure 3-1. Data Acquisition and Decommultiplexing Equipment Functional Block Diagram

3-13. Two of the input data sources, Command Module carry-on equipment and/or ground service equipment, supply 128 of the 512 prime frame words. The Command Module supplies another 128 words of airborne PCM data. The remaining 256 word slots, necessary to complete a 512 word prime frame, are not used and are filled in with binary zeros unless otherwise noted. (At certain ACE-S/C installations, the spare 256 word slots will be used to receive test data from the Lunar Excursion Module carry-on and permanent sensor equipment.) The most significant bit of each eight-bit word is received first. An eight-bit word can represent either analog or event information. For analog information, an eight-bit word represents a single analog parameter sample. In the case of event information, each bit of the eight-bit word represents a discrete event.

3-14. The composition and word location of a typical interleaved data prime frame are illustrated in figure 3-2. The inputs from up to four (maximum) prime sources are identified as A, B, C, and D. The sources are scanned sequentially: the first word of each source (A_1 , B_1 , C_1 , D_1), then the second word (A_2 , B_2 , C_2 , D_2) and so on to the last word (A_{128} , B_{128} , C_{128} , D_{128}). The first four words of each prime frame (A_1 , B_1 , C_1 , and D_1) form a single 32-bit sync word. (The remaining sync words, A_2 , B_2 , A_3 , and B_3 are present but are not used during the decommutation of interleaved PCM test data.) The 13th eight-bit word, A_4 , is the prime frame identification (ID) word. Only the least significant six bits of the ID word are used to identify a prime frame. (The most significant two bits are the same for each prime frame.) Fifty prime frames are received each second. The incoming eight-bit data word rate is 25,600 words per second (50 prime frames x 512 eight-bit words each). Of the 512 word time slots in a prime frame, 502 word time slots are reserved for data words (analog and/or event).

3-15. AIRBORNE PCM TEST DATA DESCRIPTION.

3-16. Airborne test data is that data received from the Command Module flight telemetry equipment. (The same airborne test data is also received as part of interleaved test data.) Airborne test data is received as split-phase PCM telemetry signals in the form of a continuous serial bit stream. The incoming bit rate is 51.2 kilobits per second. The data is organized into subframes that are received at the rate of one per second. Each subframe comprises 50 prime frames. Each prime frame is composed of 128 eight-bit data word time slots. The most significant bit of each eight-bit data word is received first. An eight-bit word can represent either analog or event information. For analog information, an eight-bit binary data word represents a single analog parameter sample. In the case of event information, each binary bit of the eight-bit data word represents a discrete on/off event.

3-17. The composition and word location of a typical airborne data subframe is shown in figure 3-3. The first three words (A_1 , A_2 , and A_3) form a single 24-bit prime frame sync word that is used for decommutation purposes. The fourth word (A_4) is the prime frame ID word. Only the least significant six binary bits of the ID are used to identify a prime frame. (The most significant two bits are zeros and are the same for every prime frame.) Of the 128-word time slots in a prime frame, 124-word time slots are reserved for data words (analog and/or event).

3-18. FREQUENCY MODULATED TEST DATA DESCRIPTION.

3-19. FM signals from up to seven different data sources in the spacecraft area are combined into a single composite FM signal. The composite FM signal is received by the data acquisition units of the ACE-S/C system via a single transmission hardline. Each of the seven spacecraft data sources is assigned a specific subcarrier frequency channel. Four of the data sources are assigned standard IRIG FM channel frequencies and three are assigned nonstandard FM channel frequencies. The channel frequency assignments are listed in table 3-1.

Table 3-1. FM Channel Frequency Assignments

IRIG CHANNEL NUMBER	CHANNEL CENTER FREQ (KILOCYCLES)	DEVIATION LIMITS (PERCENT)
STANDARD IRIG FM CHANNELS		
14	22.0	± 7.5
15	30.0	± 7.5
16	40.0	± 7.5
17	52.5	± 7.5
NONSTANDARD FM CHANNELS		
	95.0	± 7.5
	125.0	± 7.5
	165.0	± 7.5

3-20. VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT.

3-21. VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL FUNCTIONS.

3-22. The Video Distribution and Tape Transport Control Unit provides:

- a. The means to distribute selectively all incoming raw test data from the spacecraft test area, refined test data generated within the ACE-S/C system, and the

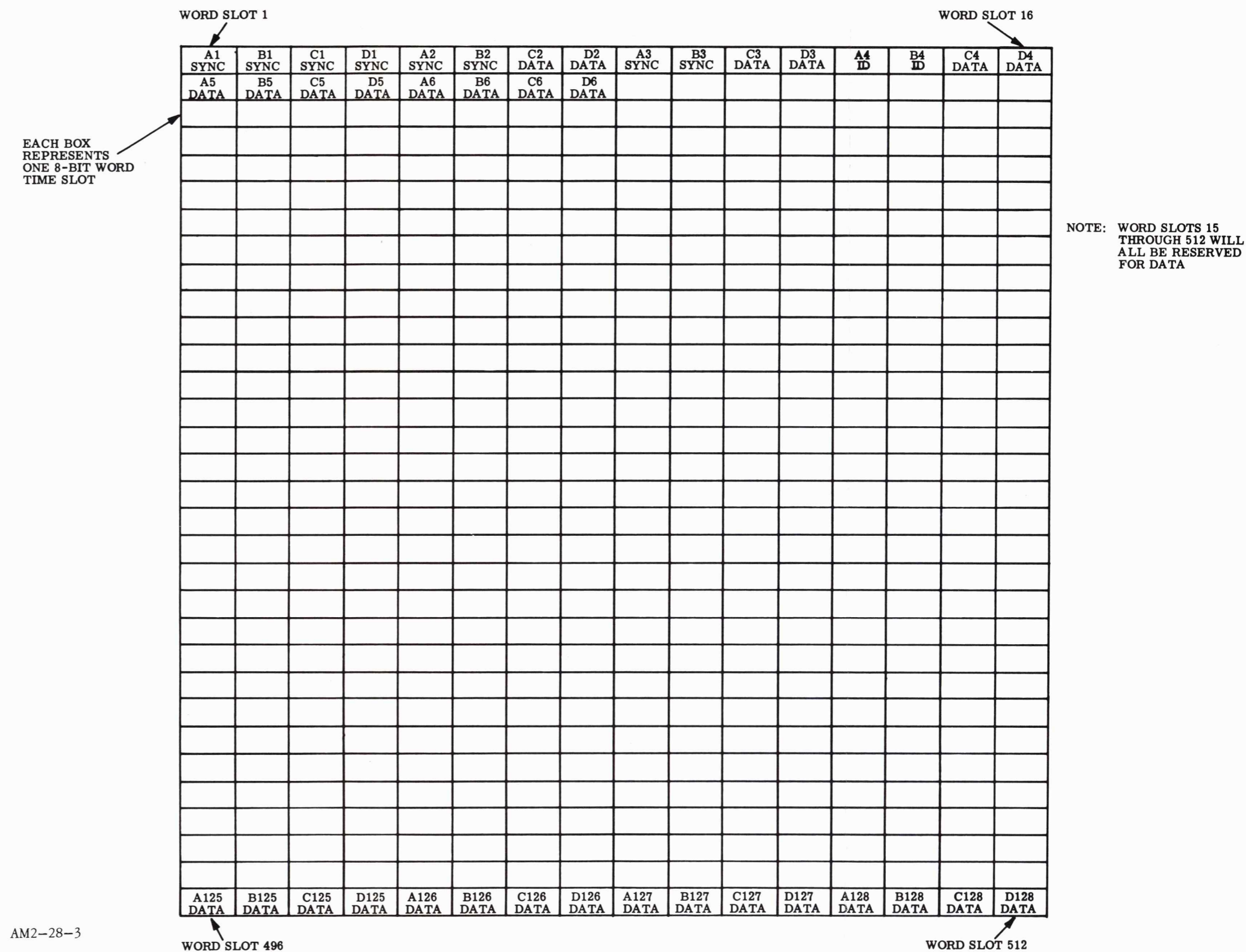


Figure 3-2. Typical Interleaved Prime Frame Composition and Word Location

WORD 1				WORD 8			
A1 SYNC	A2 SYNC	A3 SYNC	A4 ID	A5 DATA	A6 DATA	A7 DATA	A8 DATA
A121 DATA	A122 DATA	A123 DATA	A124 DATA	A125 DATA	A126 DATA	A127 DATA	A128 DATA
WORD 121				WORD 128			

NOTES: WORD TIME SLOTS SHOWN
CONTAIN 8 BINARY BITS
EACH.

WORD TIME SLOTS A5
THROUGH A128 ARE
RESERVED FOR DATA.

THE PRIME FRAMES ARE
RECEIVED AT A RATE OF
50 PER SECOND. THE DATA
BITS ARE RECEIVED AT A
RATE OF 51.2 KILO BITS
PER SECOND.

AM2-29-3

Figure 3-3. Typical Airborne Prime Frame Composition and Word Location

support signals (time codes, voice, tape speed lock, etc.) generated by the support equipment.

b. The means to condition certain selected signals prior to their being recorded on magnetic tape.

c. A magnetic tape recorder remote control switching capability.

3-23. The subassemblies that make up the Video Distribution and Tape Transport Control Unit and their functional relationship are illustrated in figure 3-4. The selective routing of test data signals is facilitated by patch panels. The signal mixer and reference mixer/oscillator subassemblies contained in the Video Distribution and Tape Transport Control Unit are used to modify certain selected signals prior to recording them on magnetic tape. The outputs of these subassemblies are routed to the magnetic tape recorders via the patch panels. The signal separator is used to process certain magnetic tape recorder playback signals prior to their distribution by the patch panels. The magnetic tape recorder relay control unit provides a means by which the magnetic tape recorder transport control unit may be remotely controlled from the Computer Complex Console or from the tape search unit. This unit also is used to route the current status indications of the magnetic tape recorders to the Computer Complex Console and to the tape search unit.

3-24. VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT DESCRIPTION.

3-25. The Video Distribution and Tape Transport Control Unit is comprised of five, physically identical patch panels. A typical patch panel layout is illustrated in figure 3-5. Two rows of 24 connectors are mounted on the front of each patch panel. The routing of the signals available at the patch panel is accomplished by means of coax jumper cables. Some signals are available on more than one patch panel connector; e.g., interleaved PCM test data. This availability is accomplished by means of T-connectors on the rear of the patch panel. The exact patch-panel jumper connections to be used are dependent upon specific test program needs and are not given here. With respect to maintenance, the patch panels provide a convenient and centrally located means to monitor many of the signals passed through the units of the ACE-S/C Computer Room.

3-26. The signal mixer, signal separator, reference oscillator/mixer, and magnetic tape recorder relay control units are functionally part of the magnetic tape recording equipment. These units are described in paragraphs 3-79 through 3-114, following the description of the recording equipment.

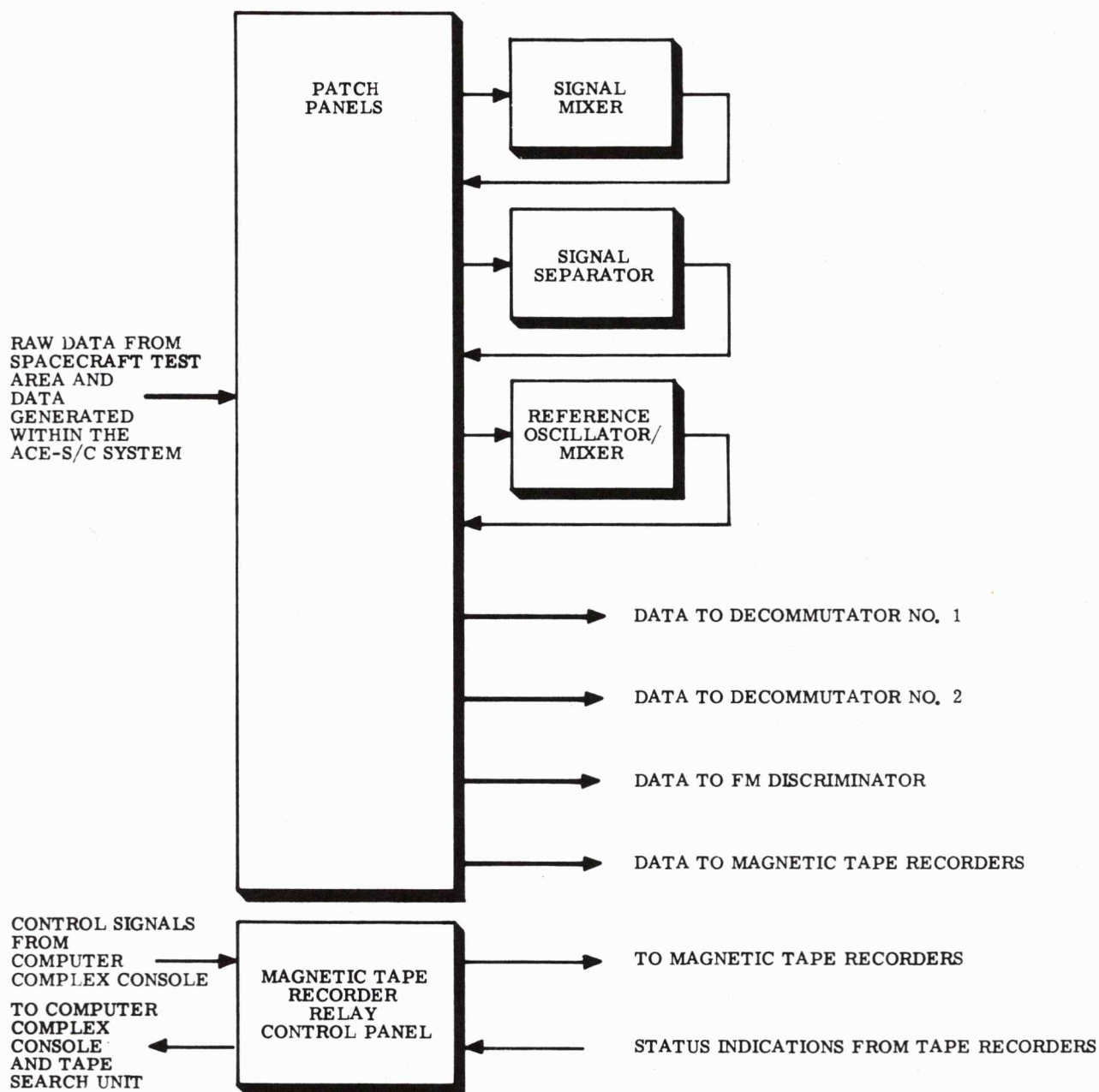


Figure 3-4. Video Distribution and Tape Transport Control Unit
Functional Block Diagram

3-27. MAGNETIC TAPE RECORDER UNITS.

3-28. MAGNETIC TAPE RECORDER FUNCTIONS.

3-29. There are three identical magnetic tape recorder units located in the computer room of an ACE-S/C system. They are used to record selected test data resulting from a spacecraft testing sequence. The recorded data is a permanent record of incoming PCM test data, FM test data, reconstructed decommutator PCM data, time code signals, and voice signals. The data stored on the magnetic tapes may be reproduced (played back) at any time to facilitate data reduction, ACE-S/C system pre-operation checkout, and maintenance test procedures.

3-30. Each magnetic tape recorder is capable of recording and reproducing up to seven discrete channels of data: six direct record/reproduce channels and one FM multiplex record/reproduce channel. The magnetic tape recorders are of modular construction and are designed for field modification to 14 channels at a later date.

3-31. MAGNETIC TAPE RECORDER INPUTS. (See figure 3-6.) All data signals to be recorded on magnetic tape are routed through the patch panels of the Video Distribution and Tape Transport Control Unit to the magnetic tape recorder units. Certain data, such as airborne PCM test data, is routed through the patch panels directly to a magnetic tape recorder. Other data, such as timing codes and voice, are first patched to a signal mixer unit (located in the Video Distribution and Tape Transport Control Unit), processed, and then patched to a magnetic tape recorder unit. The total number of data inputs that a magnetic tape recorder can record at a time is seven: up to six directly patched inputs and one processed input.

3-32. Each recorder also receives control signals from remote control units. The Computer Complex Console contains three remote control units, one for each magnetic tape recorder unit. A tape search control unit (located in the Tape Recorder/Computer Time Decoder and Search Control Unit) also supplies remote control signals to the magnetic tape recorders. All remote control signals are fed to the magnetic tape recorders via a magnetic tape recorder switching control unit located in the Video Distribution and Tape Transport Control Unit. The switching function of the magnetic tape recorder switching control unit is controlled by the operator of the Computer Complex Console.

3-33. MAGNETIC TAPE RECORDER OUTPUTS. (See figure 3-6.) All data signals reproduced (played back) by the magnetic tape recorder units are routed to the appropriate units of the ACE-S/C system by the patch boards of the Video Distribution and Tape Transport Control Unit. Certain test data (e.g., PCM test data) is routed through the patch panels directly to the appropriate ACE-S/C units. Some data (e.g., timing codes, voice, etc.) are first patched to a signal separator (located in the Video Distribution and Tape Transport Control Unit) processed, and then patched to an appropriate ACE-S/C unit.

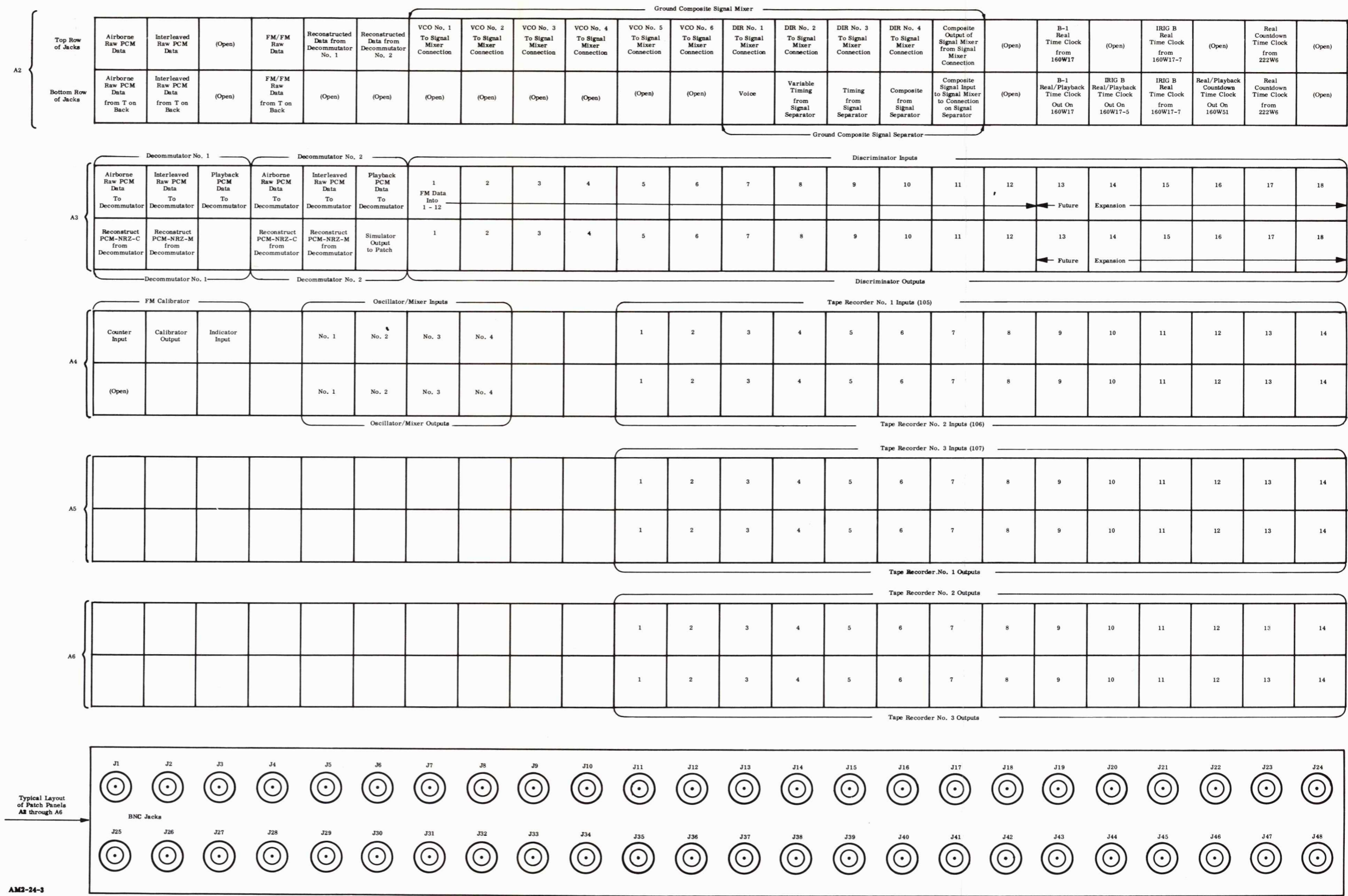


Figure 3-5. Patch Panel Layout and Signal Identification

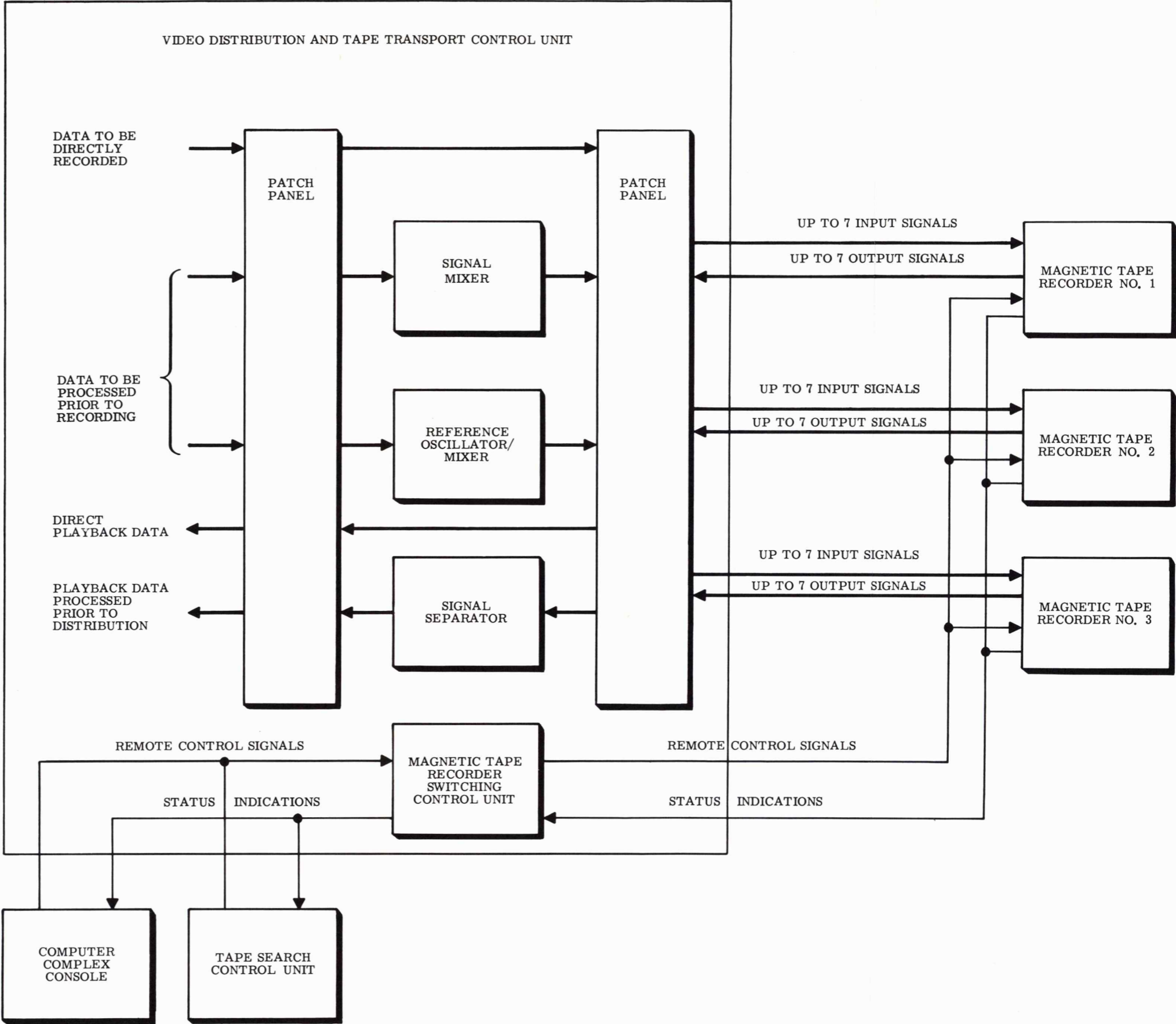


Figure 3-6. Magnetic Tape Recorder Input/Output Functional Block Diagram

3-34. Each magnetic tape recorder also sends status indicating signals to the remote control units. These status signals are routed to the appropriate remote control units via the magnetic tape recorder relay control panel located in the Video Distribution and Tape Transport Control Unit.

3-35. **MAGNETIC TAPE RECORDER CONTROL.** Each magnetic tape recorder may be controlled at its associated local control panel or by remote control units. The remote control units, one for each magnetic tape recorder, are located in the Computer Complex Console. Remote control of a single magnetic tape recorder, selected by the Computer Complex Console, is provided by a tape search control unit. All remote control signals are routed through the Video Distribution and Tape Transport Control Unit to the magnetic tape recorders. The status output of each magnetic tape recorder is also routed through the Video Distribution and Tape Transport Control Unit to the appropriate remote control unit status displays. This routing is done by the magnetic tape recorder relay control panel. For the purpose of describing the remote operation of the magnetic tape recorders, the control function is divided into three parts: (1) search control selection, (2) sequential operation selection, and (3) status indication.

3-36. Search Control Selection. (See figure 3-7.) Each magnetic tape recorder is fed remote control signals from an associated remote control unit located on the Computer Complex Console. The tape search control unit (physically part of Tape Recorder/Computer Time Decoder and Search Control Unit 116) can also be selected to control a single magnetic tape recorder. Search control selector switches, located on the Computer Complex Console, determine which one of the three recorders will be under the control of the tape search control unit. The search control selector switches operate magnetic tape recorder selection relays located in the Video Distribution and Tape Transport Control Unit relay control panel. The closure of a search control selector switch will energize the control relay associated with that particular switch. The energized relay then will route the search commands, generated by the tape search control unit, to the magnetic tape recorder associated with that relay. The search commands from the tape search control unit dictate the sequence of operation of the magnetic tape recorder to which they are applied. The remote control unit, associated with the magnetic tape recorder that has been selected to receive search commands, can still issue, at any time, remote commands that will override the search command signals. Only one magnetic tape recorder will be in the search mode at any one time.

3-37. A more complete description of the tape search control unit is given in paragraphs 3-63 through 3-78.

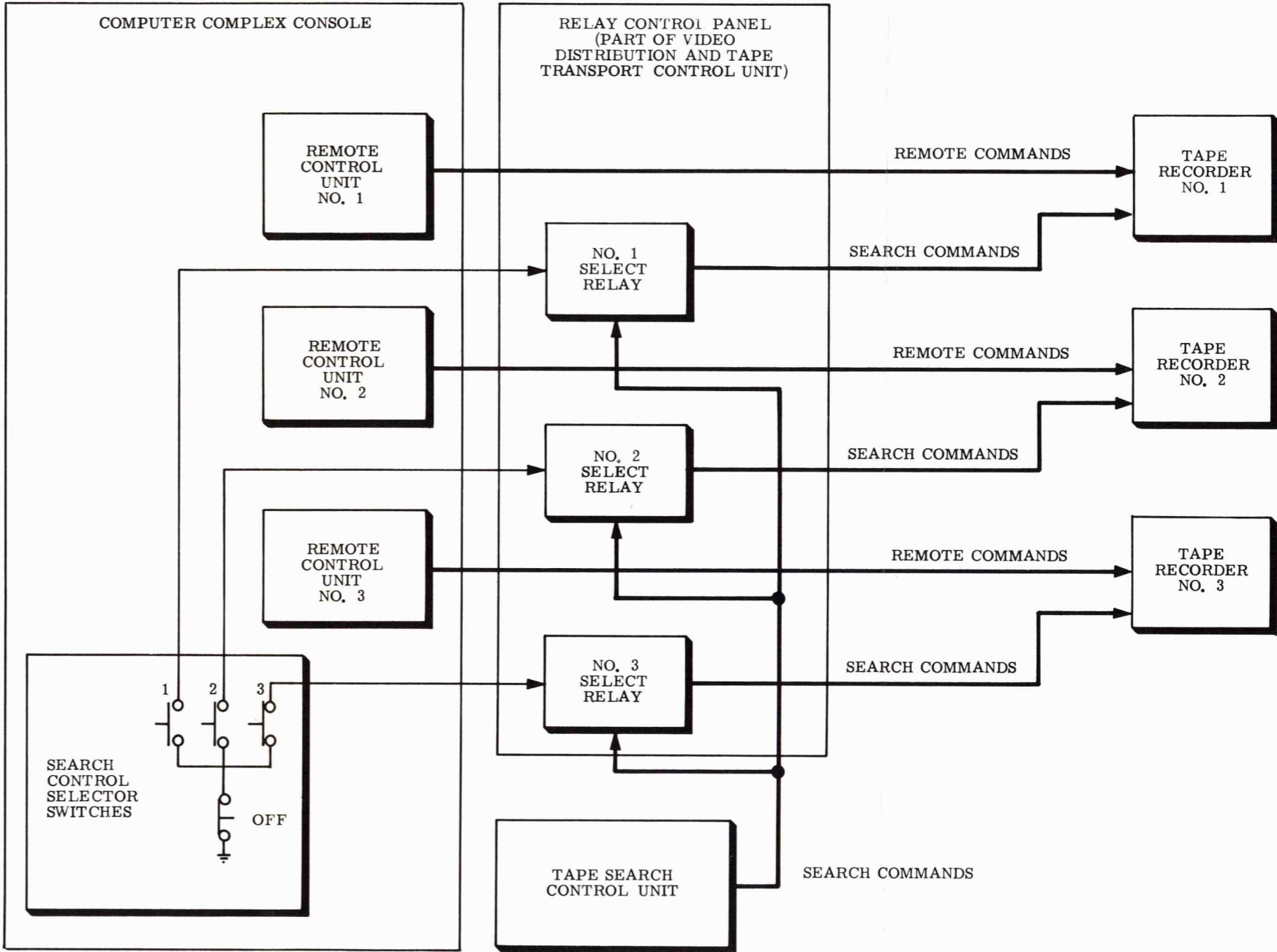
3-38. Sequential Operation Selection. (See figure 3-8.) In normal operation, two of the magnetic tape recorders may operate in conjunction with each other to facilitate the uninterrupted recording of data. To accomplish uninterrupted recording, when one recorder is about to reach the end of its tape supply, it will signal a second recorder to start running. When the second recorder is up to recording speed, it will signal the first tape recorder to stop recording. At this point, the second magnetic recorder will begin to record incoming data on its fresh tape supply. When the second recorder is approaching the end of the tape supply, the sequence just described will be reversed.

3-39. Sequential operation selector switches, located on the Computer Complex Console recorder control panel, determine which two of the three magnetic tape recorders available are to operate in conjunction with each other. A separate selection switch is available for each possible recorder combination: 1 and 2, 1 and 3, and 2 and 3. Associated with each sequential operation selector switch are control switching relays located in the relay control panel of the Video Distribution and Tape Transport Control Unit. When a sequential operation selector switch is depressed, the control relays associated with that particular switch are energized. The energized relays complete a control signal link between two of the magnetic tape recorders. The start-stop sequence signals are passed between the two selected magnetic tape recorders via the relay link.

3-40. Status Indication. (See figure 3-9.) The current operational status of each magnetic tape recorder is displayed on the control panel of each recorder. The same status indications are simultaneously displayed at each of the associated Computer Complex Console remote control units. The status indicating signals are routed through the Video Distribution and Tape Transport Control Unit. Some of the status indications coming from each of the magnetic tape recorders are sent to switching relays in the Video Distribution and Tape Transport Control Unit relay control panel. The closure of these relays is controlled by the search control selector switches on the Computer Complex Console recorder control panel. When a magnetic tape recorder is selected to receive search commands from the tape search control unit, the control relays associated with that particular magnetic tape recorder will be energized. The status indicating signals associated with the selected magnetic tape recorder will be routed to the tape search control unit status display indicators. Since the tape search control unit has only one set of status indicators, the status displayed will always be that of the magnetic tape recorder that the tape search control unit is currently governing.

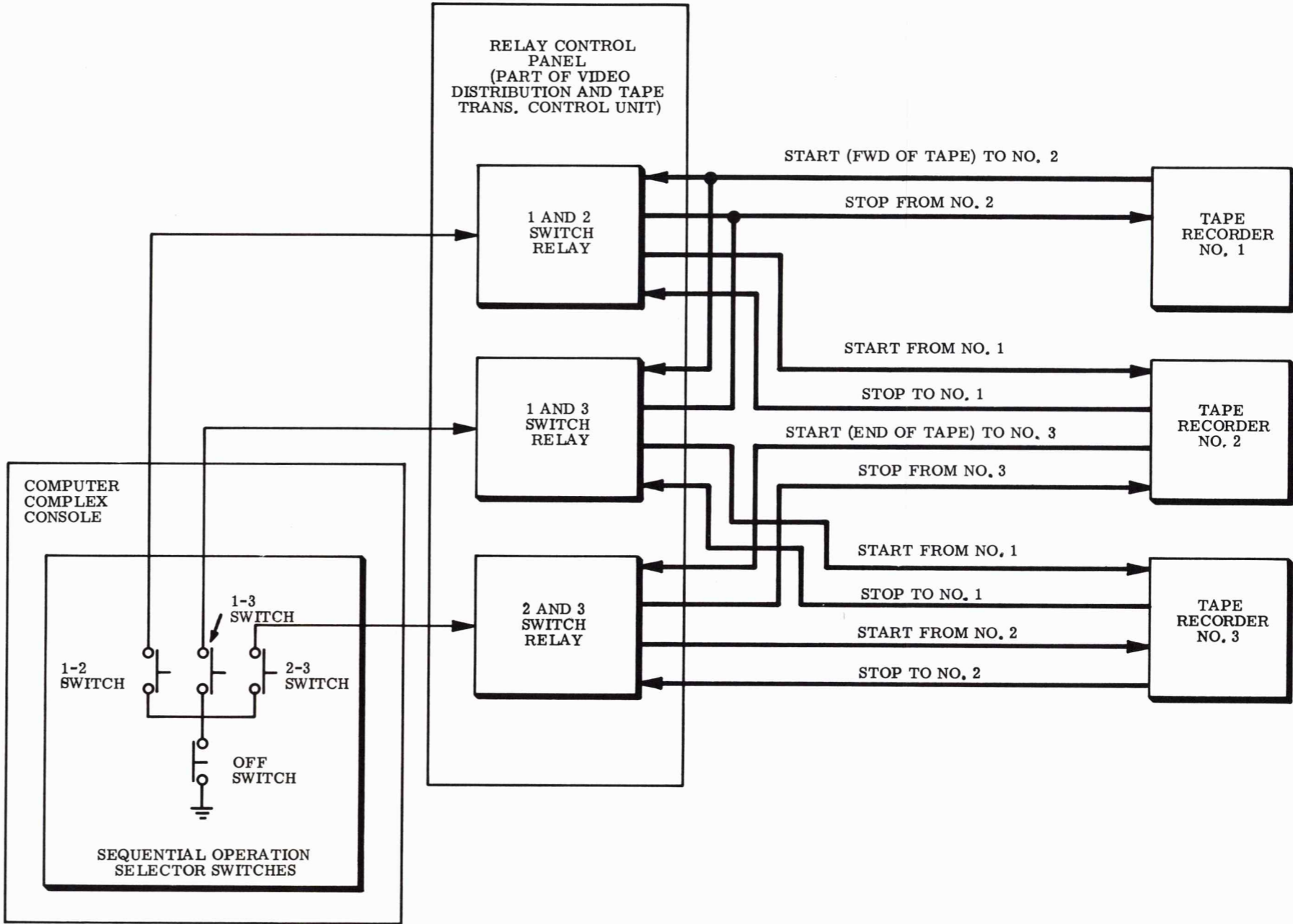
3-41. MAGNETIC TAPE RECORDER DESCRIPTION.

3-42. Each magnetic tape recorder provides seven channels for recording and reproducing wideband signal data. The tape used with the magnetic tape recorders is 0.5-inch wide,



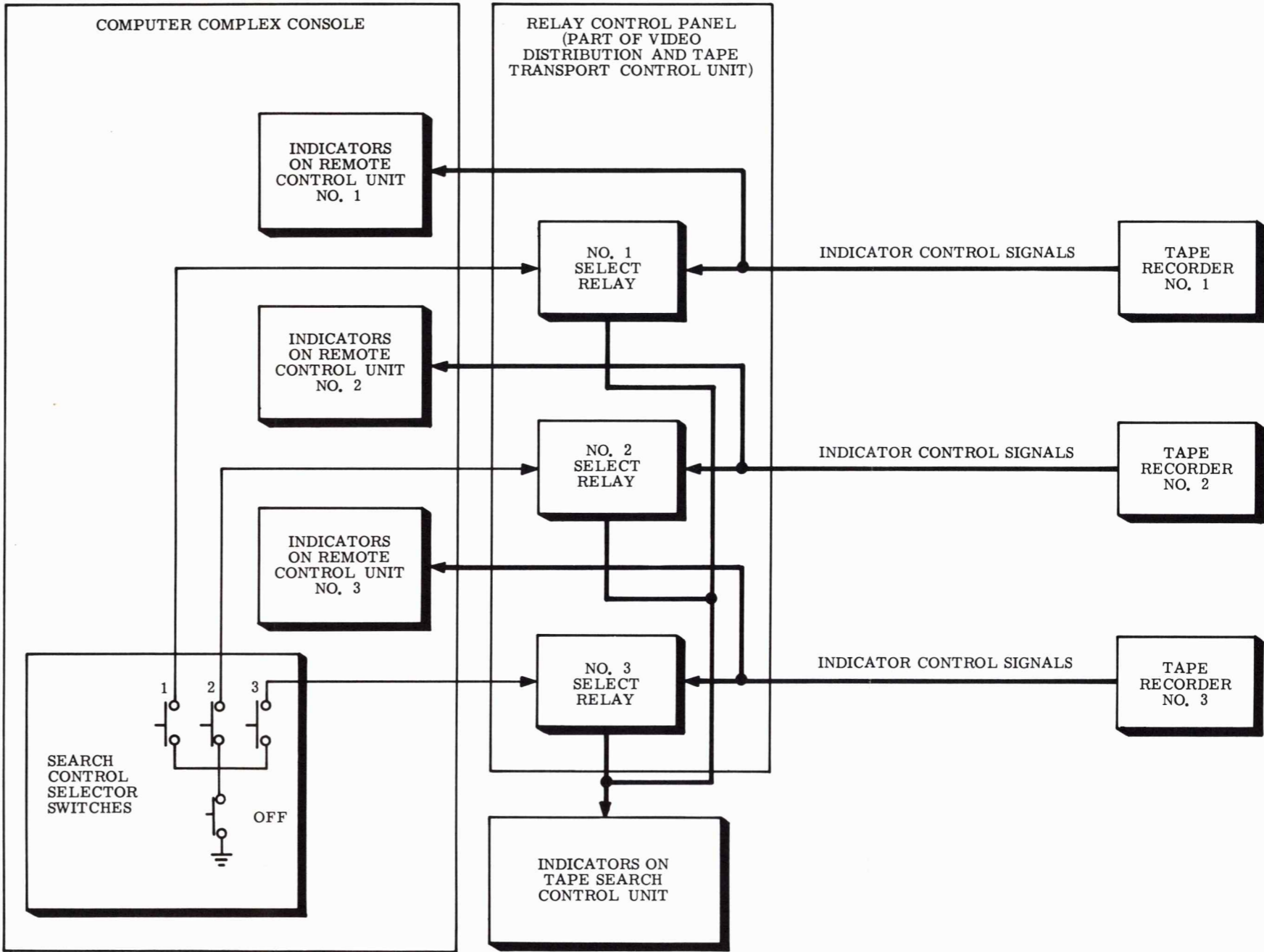
AM2-30-3

Figure 3-7. Search Control Functional Block Diagram



AM2-32-3

Figure 3-8. Sequential Operation Functional Block Diagram



AM2-33-3

Figure 3-9. Status Indication Functional Block Diagram

1.0-mil-thick mylar-base magnetic tape on 10.5-inch reels. (For 14-channel operation, 1-inch tape is used.) The recorders have four record/reproduce speeds: 15, 30, 60, and 120 inches per second. Recorder frequency response is from 400 cps to 1.5 megacycles. The basic components of the tape recorder are a precision four-speed tape transport, a control section to control the tape transport, and the record and reproduce signal circuits.

3-43. TAPE TRANSPORT REEL ASSEMBLIES. The supply and takeup reel assemblies each consist of a motor, a brake assembly, a turntable, and a hold-down knob. The supply reel assembly drives the reel rotation counter by means of a toothed pulley.

3-44. Each brake consists of a rotating disk on the rear of the drive motor shaft, between a stationary shoe on the motor case and a second stationary disk. The brake is activated by a solenoid coil. The brakes are used only to prevent tape creep after the tape motion has stopped.

3-45. Tape tension is controlled by varying the voltage input to the drive motors. This drive motor voltage is controlled by a tape tension servo, or in the Forward and Rewind Mode, by speed control circuits.

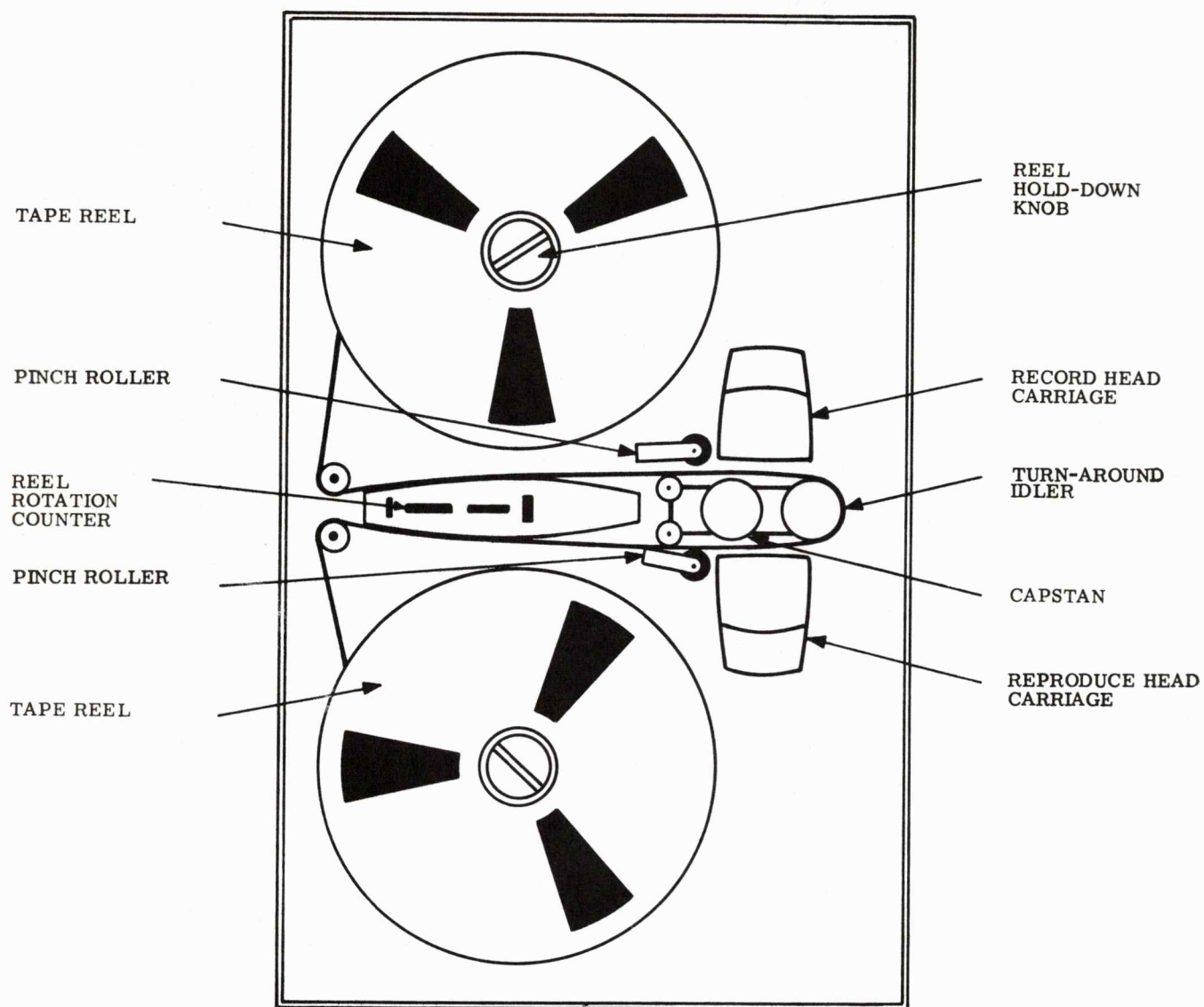
3-46. TAPE TRANSPORT TAPE DRIVE. (See figure 3-10.) In the Record and Reproduce Modes, the tape is driven past the heads in a closed loop with positive drive at each end. The tape is held against a rotating capstan, by pinch rollers, as it enters and leaves the loop. Tape speed in the Record and Reproduce Modes is a function of capstan surface velocity. The capstan is driven continuously by a four-speed synchronous motor and flywheel.

3-47. TAPE HEADS. The tape heads are mounted on a carriage in the closed-loop drive area. The record heads are positioned above the tape loop between the capstan and the turn-around idler. The reproduce heads are mounted below the tape loop between the turn-around idler and the capstan. The heads are placed against the tape by actuating cylinders in all modes, except Forward and Rewind, when they are withdrawn.

3-48. TAPE CONTROL CIRCUIT FUNCTIONS. The tape transport may be operated in any of seven modes: Stop, Forward, Rewind, Forward Search, Rewind Search, Reproduce, and Record.

3-49. When the POWER switch is OFF, no power is applied to any part of the unit. With the POWER switch ON and the TRANSPORT switch OFF, the system is placed in the Electronics Standby Mode. In this mode, power is applied to all system electronic circuits except the reproduce amplifiers. No power is applied to the tape transport or to the preamplifier power supply.

3-50. When both the POWER and TRANSPORT switches are ON, the unit is in the Stop (Ready) Mode, provided that all special operating controls in the control unit are in their



AD3-17-2

Figure 3-10. Wideband Analog Tape Transport

normal positions and that the tape is properly threaded on the transport. In this mode, the supply reel brake is engaged (de-energized) to prevent tape creep. The takeup reel brake is always disengaged (energized), except when the transport power or main power is turned off. The tape is kept under proper tension in the Stop Mode by the takeup reel motor, which receives normal tensioning voltage from the takeup tension servo.

3-51. When the Forward Mode is selected by actuation of the corresponding switch, the supply reel brake disengages, releasing tension on the tape. The takeup motor then pulls the tape in the forward direction, rotating the turn-around idler. The turn-around idler contains a tachometer composed of a light source, interrupted by slots in the idler, and a photocell. The photocell output is rectified, filtered, and compared with a preset voltage from the FAST SPEED ADJ control; any resultant error is used to control the voltage applied to the supply reel motor. As the tape approaches the proper speed, the supply motor voltage is increased, applying a torque that opposes the takeup motor. The takeup tension servo senses the increased tension and reduces the takeup motor voltage until the proper stable speed is reached, with the tape under correct tension.

3-52. Selection of the Rewind Mode results in the same conditions as the Forward Mode, except that motor control is reversed, with the supply motor (now taking up tape) under tension control, and the takeup motor (now supplying tape) under speed control from the turn-around idler tachometer.

3-53. Operation in the Forward Search and Rewind Search Modes is identical to the Forward and Rewind Modes, except that the turn-around idler tachometer output is compared with a preset voltage from the SEARCH SPEED ADJ control, and the head carriages are actuated to bring the heads in contact with the tape. Search Modes are selected by setting the REWIND-FORWARD SPEED switch on the control unit to the SEARCH position.

3-54. When the Reproduce Mode is selected, the starting conditions are identical to those for the Forward Mode. In this case, however, the signal from the turn-around idler tachometer is compared with a signal from the capstan tachometer. (The capstan tachometer signal is generated in the same way as the turn-around idler tachometer signal.) As the tape velocity (measured by the turn-around tachometer) and the surface velocity of the capstan (measured by the capstan tachometer) approach the same value, the supply motor voltage is increased. This holds the tape at a uniform velocity equal to the capstan surface velocity. When the velocities are equal, pinch rollers close, clamping the tape against the capstan. The capstan then takes over tape drive and drives the tape through the closed loop at a constant speed. As the pinch rollers close, control of the supply motor is removed from the turn-around tachometer and transferred to the supply-tension servo. Both reel motors are

now under normal tensioning control. At the time that the pinch rollers close, the heads are moved into contact with the tape.

3-55. The Record Mode is identical to the Reproduce Mode, except that all record relays in the unit are energized. Since record and reproduce elements of the unit function independently, signals may be recorded and reproduced simultaneously.

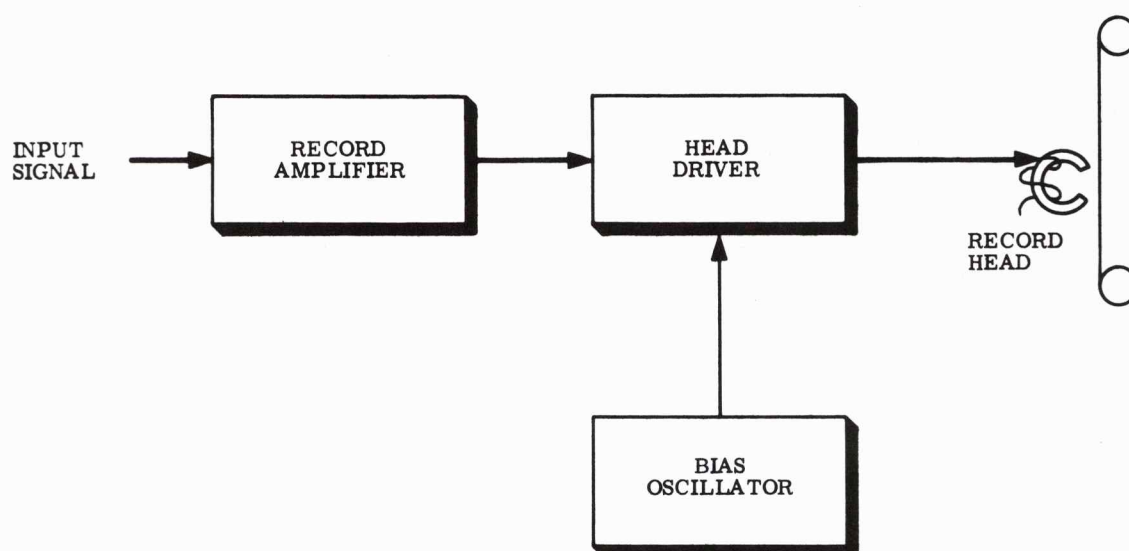
3-56. When the Stop Mode is selected from any forward operating mode, the tape is brought to a stop by reversing control of the reel motors from forward conditions to rewind conditions. That is, the supply motor is placed under normal tension control and the takeup motor is placed under speed control. Speed control voltage on the takeup motor then is suppressed by the stop circuit, and the supply tension servo, sensing a low-tension condition, applied a large retarding torque that brings the tape to a stop. When the tape stops, the supply reel brake is engaged to prevent tape creep. If the system is in the Record or Reproduce Mode when the Stop Mode is selected, the stop circuits release the pinch rollers and transfer tape drive from the closed-loop (capstan) drive to the reel motors before decelerating the tape. Stopping the tape from a rewind operating mode is accomplished in a similar manner. However, since motor control is normally reversed for rewind conditions, control reverts to forward conditions to stop the tape.

3-57. If the Record or Reproduce Mode is selected from any other mode, the tape first is brought to a standstill by automatic stop circuits. After the tape stops, the transport automatically assumes the conditions of the selected mode in the same manner as a normal start from the Stop Mode. If the Stop Mode is selected immediately after the Record or Reproduce Mode, the automatic stop circuits take precedence over the normal stop circuits. The transport will enter and stay in the Record or Reproduce Mode until the STOP switch is pressed a second time.

3-58. RECORD SIGNAL CIRCUIT FUNCTIONS. The record signal circuit consists of three units: (figure 3-11) direct record amplifiers (one for each track), head driver amplifiers (one for each track), and a single bias oscillator (for all tracks).

3-59. The direct record amplifier consists of a feedback amplifier and a monitor amplifier. The direct record amplifier increases the gain of the incoming signal sufficiently to drive the head driver amplifier. The monitor amplifier provides a signal output for input gain adjustments.

3-60. The head driver amplifier provides the necessary power amplification and impedance matching to drive the record heads. The bias oscillator output is mixed with the record signal in this stage.



AD3-18-2

Figure 3-11. Direct Record Circuit Block Diagram

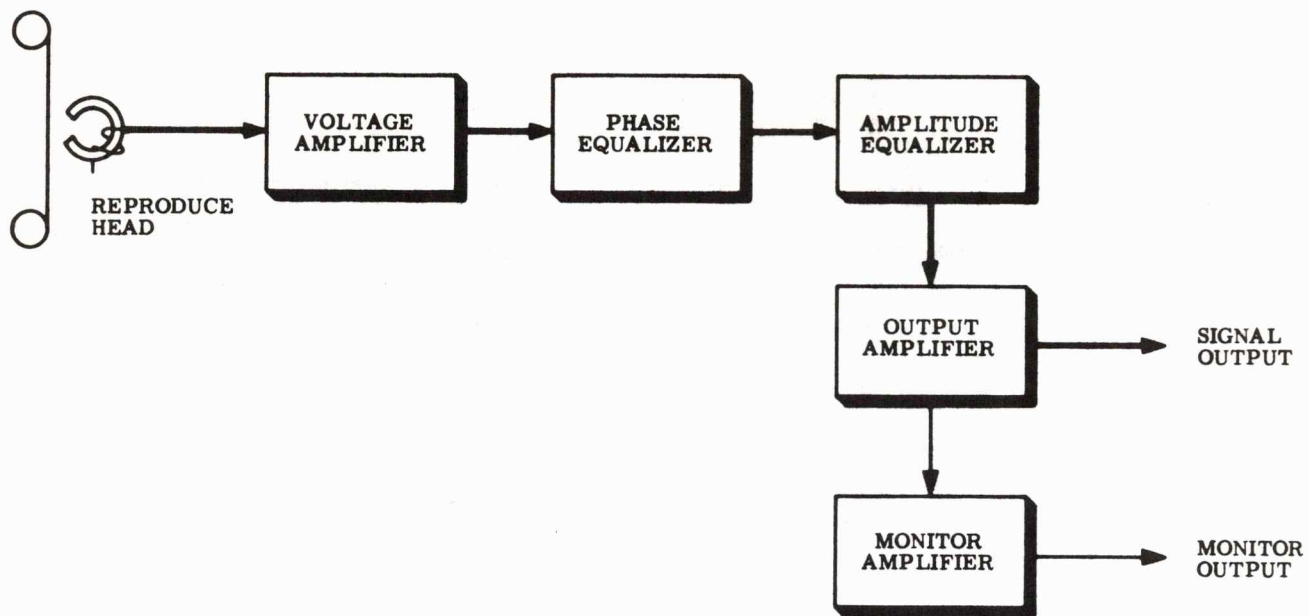
3-61. REPRODUCE SIGNAL CIRCUIT FUNCTIONS. The reproduce signal circuit includes: (figure 3-12) a voltage amplifier, phase and amplitude equalizers, and output and monitor amplifiers.

3-62. The voltage amplifier provides an impedance match to the reproduce head and sufficient gain to operate the equalizer circuits. The equalizer circuits provide the necessary corrections for variations caused by varying tape speeds. The output amplifier raises the output to an adequate level for line input, and the monitor amplifier provides an output signal for maintenance purposes.

3-63. TAPE SEARCH CONTROL UNIT.

3-64. TAPE SEARCH CONTROL FUNCTIONS.

3-65. The tape search control unit is located in the computer room and is physically a part of the Tape Recorder/Computer Time Decoder and Search Control Unit. The tape search control is capable of either fully automatic or manual positioning of a magnetic tape transport unit.



AD3-19-2

Figure 3-12. Direct Reproduce Circuit Block Diagram

3-66. The tape search control unit accepts serial IRIG B time-code information from the time decoder, which is also a part of the Tape Recorder/Computer Time Decoder and Search Control Unit. The tape search control compares the time value recorded on the tape with a preset value of time and issues appropriate control signals to a magnetic tape transport. The control signals issued are used to start, stop, rewind, and control the playback drive of a tape transport. Thumbwheel switches are available on the tape search control to preset the desired playback start/stop time values. The search time resolution provided by the thumbwheel switches is days, hours, minutes, seconds, and milliseconds. The tape search control compares the BCD time code preset into the thumbwheel switches with the time-code recorded on a magnetic tape and instructs the tape transport to search in a forward or reverse direction for the location of the start time. When the start time is located, the tape search control instructs the tape transport to playback in the forward direction until the stop time is reached.

3-67. MANUAL SEARCH MODES. A tape search control mode selector switch is provided to select any one of four operating modes: Recycle Mode, Single-Cycle Mode, Search-to-Start Mode, and Playback Mode.

3-68. Recycle Mode. In the Recycle Mode, the tape search control will cause a tape transport to search in the conventional manner to the preset start time and then automatically reproduce (playback) to the preset stop time. This process will repeat until a new control instruction is set into the tape search control unit.

3-69. Single-Cycle Mode. In the Single-Cycle Mode, the tape search control functions the same as in the Recycle Mode except that it stops the tape when the preset stop time is reached.

3-70. Search-to-Start Mode. The Search-to-Start Mode is similar to the Single-Cycle Mode except the tape is halted when the preset start time is reached. To cause the tape transport to commence playback operation toward the preset stop time, the tape search control must be set manually to the Playback Mode.

3-71. Playback Mode. The Playback Mode causes a tape transport to playback indefinitely from a preset start time.

3-72. The tape search system serves as a conventional computer peripheral input/output device. As such, the tape search system shares a (current driver) computer input/output channel along with a variety of other peripheral devices. In all respects, the tape search system appears to the computer system as a regular input/output device exhibiting all the characteristics required for proper integration with the computer input/output functions. The tape search system also simultaneously serves both the Command Computer and the Display Computer.

3-73. AUTOMATIC SEARCH MODES. The two general purpose digital computers employ the peripheral tape search system in the following modes.

3-74. Interrogate Mode. When operated in the Interrogate Mode, the tape search system accepts requests for real time from the computers and responds with a serial-parallel presentation to the requesting computer with the actual on-time real-time information. The time transfer is in modified straight binary notation with ten bits representing milliseconds, six bits representing seconds, six bits representing minutes, and five bits representing hours. An input real-time request from the computer results in the tape search system automatically presenting a series of four words (milliseconds, seconds, minutes, hours) to the requesting computer.

3-75. Interrupt Mode. When operated in the Interrupt Mode, the tape search system accepts an interrupt time from either of the digital computers on a single-word transfer arrangement, or alternately from the preset start/stop switches located on the front panel. When the real-time code coincides with this preset interrupt time, an interrupt signal is transmitted to the appropriate computer. Coincidence of real time and interrupt time does not destroy preset

time. This permits a continual updating of time on a single word basis. Provisions are made within the tape search system to permit the computer to distinguish between interrupts generated as a result of manual preset interrupt time. Capability exists for each computer to enable or disable its designated manual and/or computer-programmed interrupts. When one computer sends an interrupt time to the tape search system, the other computer is capable of destroying this time by sending its own interrupt time, provided it has not been locked out.

3-76. COMPUTER LOCKOUT. Capability exists for one computer to lock out the other computer. Lockout is defined as follows: When lockout is imposed on a computer, this computer is advised by status that it should not set up interrupt time. A locked-out computer is capable of receiving time on request.

3-77. COMPUTER STATUS RESPONSE. The tape search system is capable of advising either computer of its present operating condition through a response to status request from the computer. A status word supplies the following information:

- a. Computer which last set interrupt time is designated.
- b. Computer lockout status (each computer).
- c. Manual preset interrupt status is available to each computer.
- d. Programmed preset interrupt status is available to each computer.

3-78. TAPE SEARCH CONTROL DESCRIPTION.

NOTE

As stated previously, the tape search control is physically part of Tape Recorder/Computer Time Decoder and Search Control Unit 116. Unit 116, in turn, forms part of the Tape Search/Time Code Translator/Computer I/O Synchronizer, which is described in Section IV. Refer to Section IV for a detailed description of the tape search control.

3-79. SIGNAL MIXER ASSEMBLY.

3-80. SIGNAL MIXER FUNCTIONS. (See figure 3-13.)

3-81. The signal mixer serves a two-fold purpose. First, it allows a multitude of low priority or nonactual data signals to be combined into a single composite signal that will utilize only one of the seven magnetic tape recorder input channels, rather than monopolize several input channels. Second, it allows certain very low frequency data (i.e., below 400 cps) to be

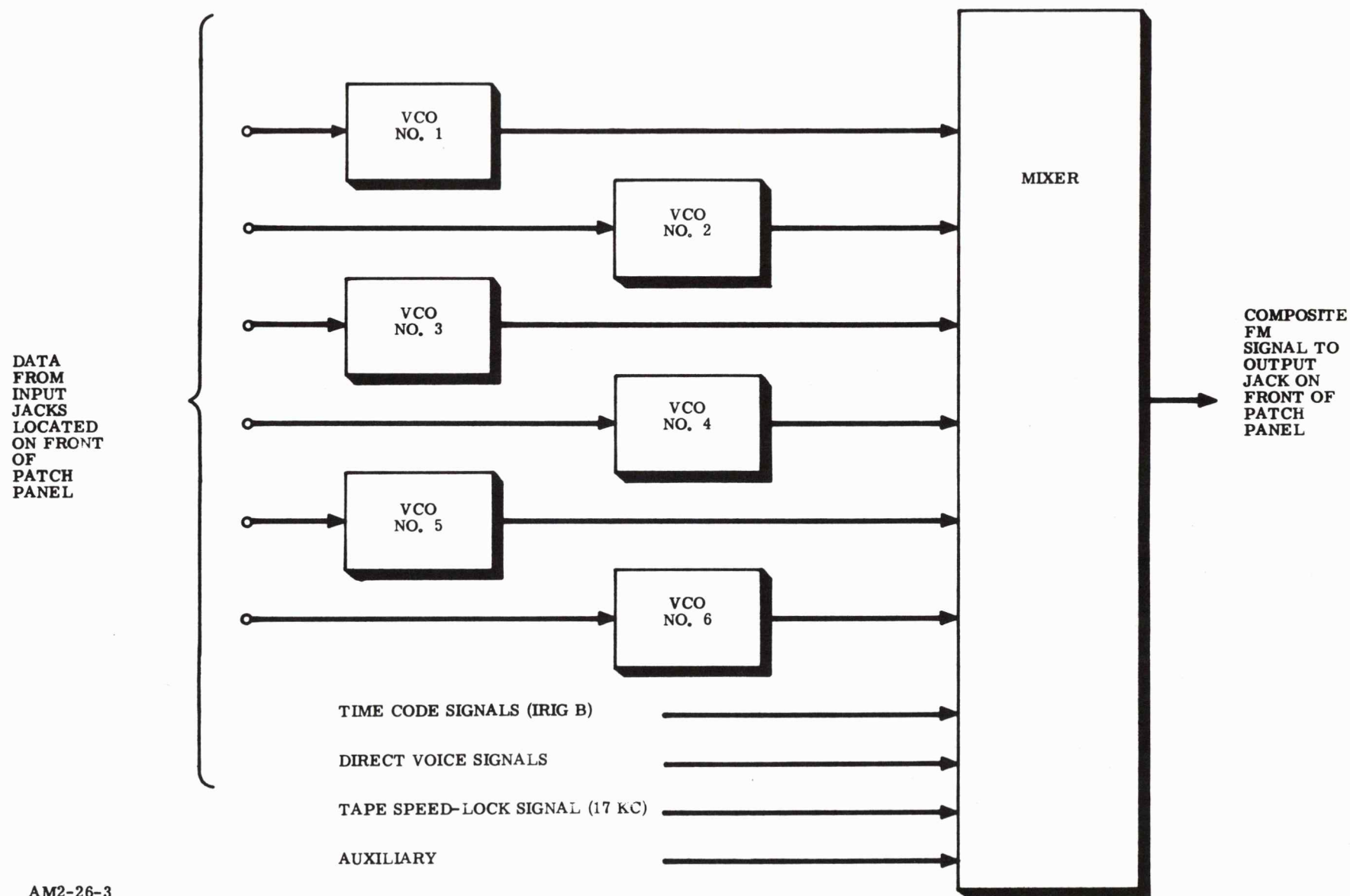


Figure 3-13. Signal Mixer Functional Block Diagram

recorded on magnetic tape that could not otherwise be recorded because of the low frequency response cutoff of the magnetic tape recorders.

3-82. The signal mixer is comprised of six voltage-controlled oscillators (VCO's) and a mixer. The signal mixer can accept up to 10 input signals simultaneously from the Video Distribution and Tape Transport Control Unit patch panels. Four of the inputs are fed directly to the mixer, and six are fed through associated VCO's to the mixer. Low frequency signals (e.g., voice, countdown time code, etc.) that cannot be directly recorded by the magnetic tape recorders are patched to the VCO's. The output of each VCO is a relatively high-frequency (in the order of 10 kc to 20 kc) FM signal modulated by the low-frequency signal input. The FM output of each VCO is then fed to the mixer.

3-83. Each VCO is assigned a specific and different subcarrier center frequency. The mixer combines all input signals into a single composite multiplexed signal. One of the direct mixer inputs is reserved for voice annotation but is generally not used. If a voice input is present on this line, all other inputs (direct and FM) are disconnected automatically from the mixer. The multiplexed output of the mixer is routed to an input channel of a magnetic tape recorder via the appropriate patch panel connections on the Video Distribution and Tape Transport Control Unit.

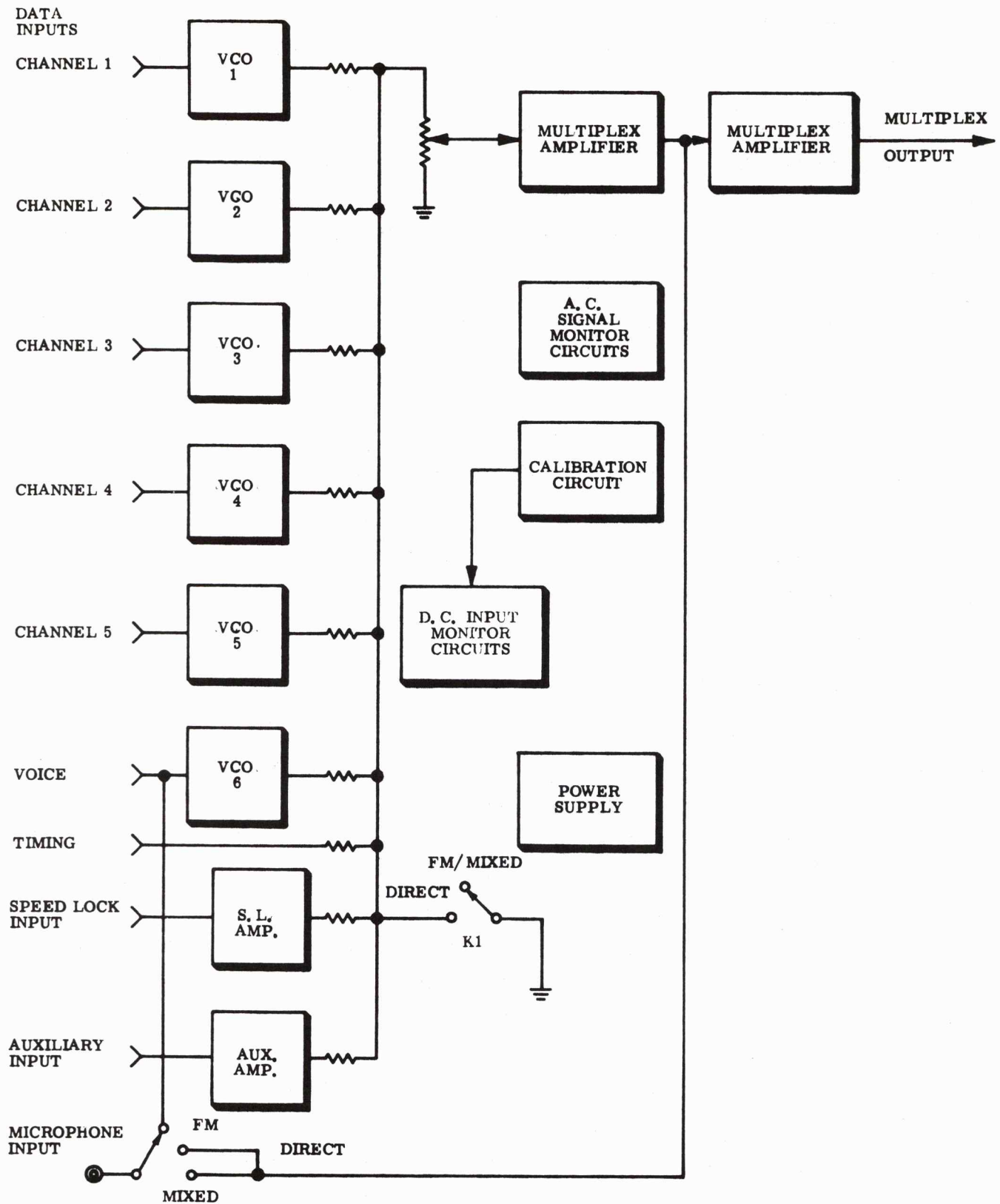
3-84. The measurement and adjustment of all input and output signals, including the multiplexed output, can be accomplished by using two panel-mounted meters and their associated selector switches and potentiometer controls located on the front of the signal mixer unit. The frequency and deviation of each VCO can be adjusted by means of front-panel-mounted oscillator controls. A front-panel BNC connector and selector switch make possible the monitoring of all signal frequencies.

3-85. SIGNAL MIXER DESCRIPTION.

3-86. The signal mixer is an EMR 808D Auxiliary Signal Mixer. The equipment can multiplex as many as six FM subcarrier channels as well as voice, timing, speed-lock, and auxiliary signals. Figure 3-14 is a simplified block diagram of the signal mixer.

3-87. The six FM subcarrier channels are each produced by a VCO. Five of the VCO's are modulated by various input signals (e.g., IRIG B time code); the sixth VCO is modulated by an FM voice signal. Input and output level controls for each VCO are located on the front panel. The center frequency of each VCO is as follows:

<u>VCO</u>	<u>CENTER FREQUENCY (kc)</u>	<u>VCO</u>	<u>CENTER FREQUENCY (kc)</u>
1	5.4	4	14.5
2	7.35	5	22.0
3	10.5	6	30.0



AD3-3-9

Figure 3-14. Signal Mixer Simplified Block Diagram

3-88. One direct channel is provided for local voice annotation by means of a carbon microphone. There are three modes for local voice insertion: FM, Direct, and Mixed. In the FM Mode of operation, the local voice is placed on the subcarrier multiplex by means of the No. 6 VCO. In the Mixed Mode of operation, the local voice signal is applied to the input of the second multiplex amplifier where it is mixed with the FM multiplex signal. In the Direct Mode of operation, a relay (K1) is energized, which causes all inputs other than the local voice signal to be grounded. The local voice signal is then applied along through the multiplex amplifiers. In this last mode, the signal mixer effectively operates as an audio amplifier.

3-89. The multiplex amplifiers provide the signal gain and impedance match required at the output of the signal mixer. The output stage (a cathode follower) provides a low impedance signal in a band from 0.5 to 40 kc into a 50-ohm line.

3-90. The signal mixer contains circuits that facilitate the application of calibration voltages to each of the VCO's. Both a-c and d-c voltage levels throughout the unit may be monitored and calibrated by means of front panel meters and controls.

3-91. A self-contained, regulated power supply provides the +150 volts dc and filament voltages required by the signal mixer.

3-92. REFERENCE OSCILLATOR/MIXER ASSEMBLY.

3-93. REFERENCE OSCILLATOR/MIXER FUNCTIONS. (See figure 3-15.)

3-94. The reference oscillator/mixer is used in conjunction with the magnetic tape recording equipment (units 105, 106, and 107) to provide a reference signal for tape speed compensation during the Playback Mode. It also serves to amplify low-level signals prior to being recorded. The reference oscillator/mixer is comprised of two separate reference oscillators and four mixer amplifiers. One oscillator operates at 100 kc and the other at 200 kc. The output of the selected oscillator is fed in parallel to the four mixer amplifiers through an oscillator selector switch. Each mixer amplifier also receives a selectable data signal input from the Video Distribution and Tape Transport Control Unit patch panels. The exact signals chosen to be fed to the mixer amplifiers are determined by the current needs of the testing program. Within the mixer amplifiers, the data signal is mixed with the selected reference oscillator signal. The resulting signals are then amplified by the mixer amplifiers and sent to the Video Distribution and Tape Transport Control Unit patch panels where they may be patched as necessary to other units of the ACE-S/C system (usually to the magnetic tape recorders).

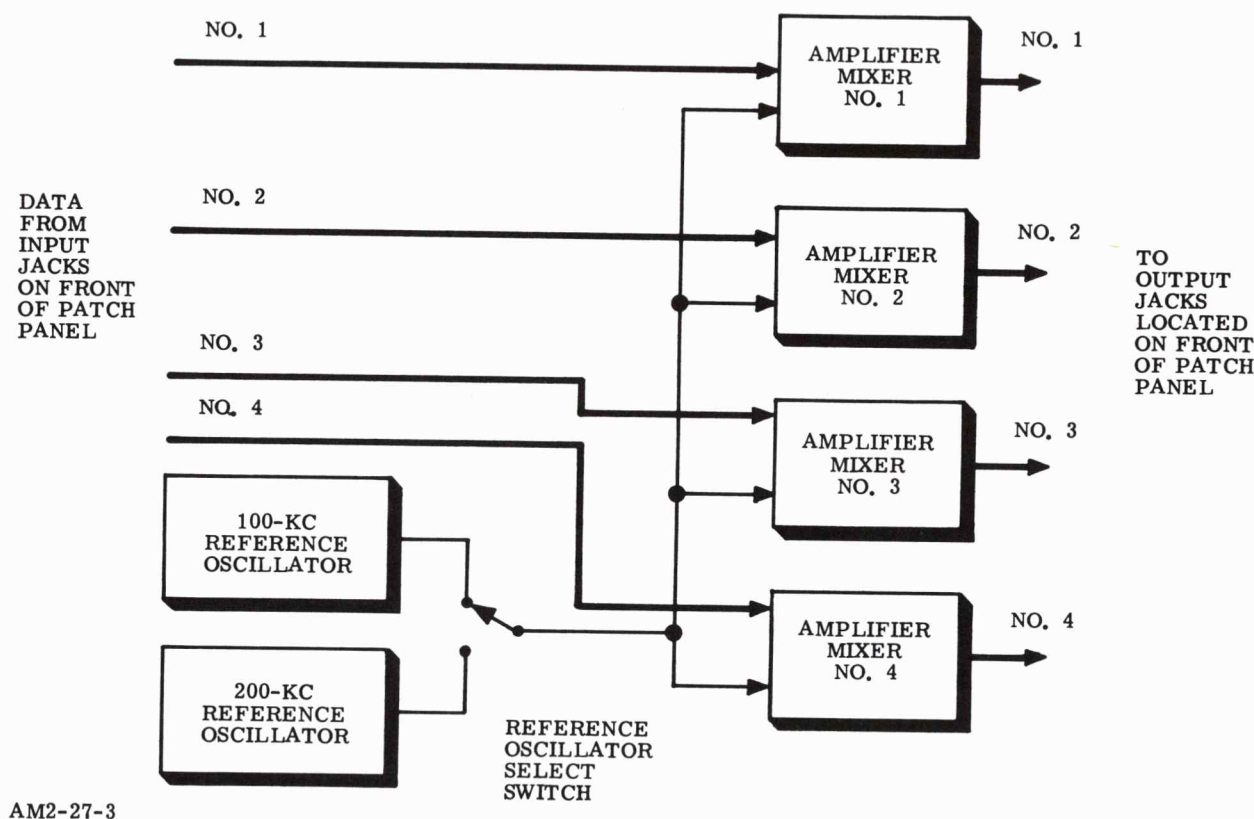


Figure 3-15. Reference Mixer/Oscillator Functional Block Diagram

3-95. REFERENCE OSCILLATOR DESCRIPTION.

3-96. Figure 3-16 is a block diagram of the reference oscillator. The reference oscillator consists of a crystal-controlled oscillator, a squaring amplifier, a divide-by-thirty-two binary counter, and a low-pass filter.

3-97. The crystal-controlled oscillator contains two transistor stages, and operates at a discrete, crystal-determined (100 kc or 200 kc) frequency. The oscillator provides a nominal output signal of 6 volts peak-to-peak.

NOTE

In present system applications, only the sinusoidal output of the crystal oscillator is used. This signal is fed directly to the mixer amplifier. The remaining circuits of the reference oscillator are not presently used but will be described to indicate complete capability of the unit.

3-98. The squaring amplifier is a single transistor overdriven amplifier stage, which amplifies and reshapes the crystal-controlled oscillator output signal. The squaring amplifier generates a 16-volt, peak-to-peak, square-wave signal that is applied to the input of the divide-by-thirty-two binary counter.

3-99. The divide-by-thirty-two binary counter consists of five flip-flop stages, each comprised of two transistors and associate diode gates. The flip-flop stages are connected in cascade, providing five divisors (2, 4, 8, 16, and 32). An output from the divide-by-thirty-two binary counter is applied as a 16-volt, peak-to-peak signal to the low-pass filter. The input signal to the low-pass filter may be obtained from six different points in the equipment so as to provide different reference frequency signals as required.

3-100. The following list indicates the six possible sources from which the low-pass filter may derive an input signal and the reference frequency thus generated by the equipment:

<u>SOURCE</u>	<u>OUTPUT FREQ. (KC)</u>
Squaring amplifier output	100 to 500
First binary flip-flop output	50 to 100
Second binary flip-flop output	25 to 50
Third binary flip-flop output	12.5 to 25
Fourth binary flip-flop output	6.25 to 12.5
Fifth binary flip-flop output	3.125 to 6.25

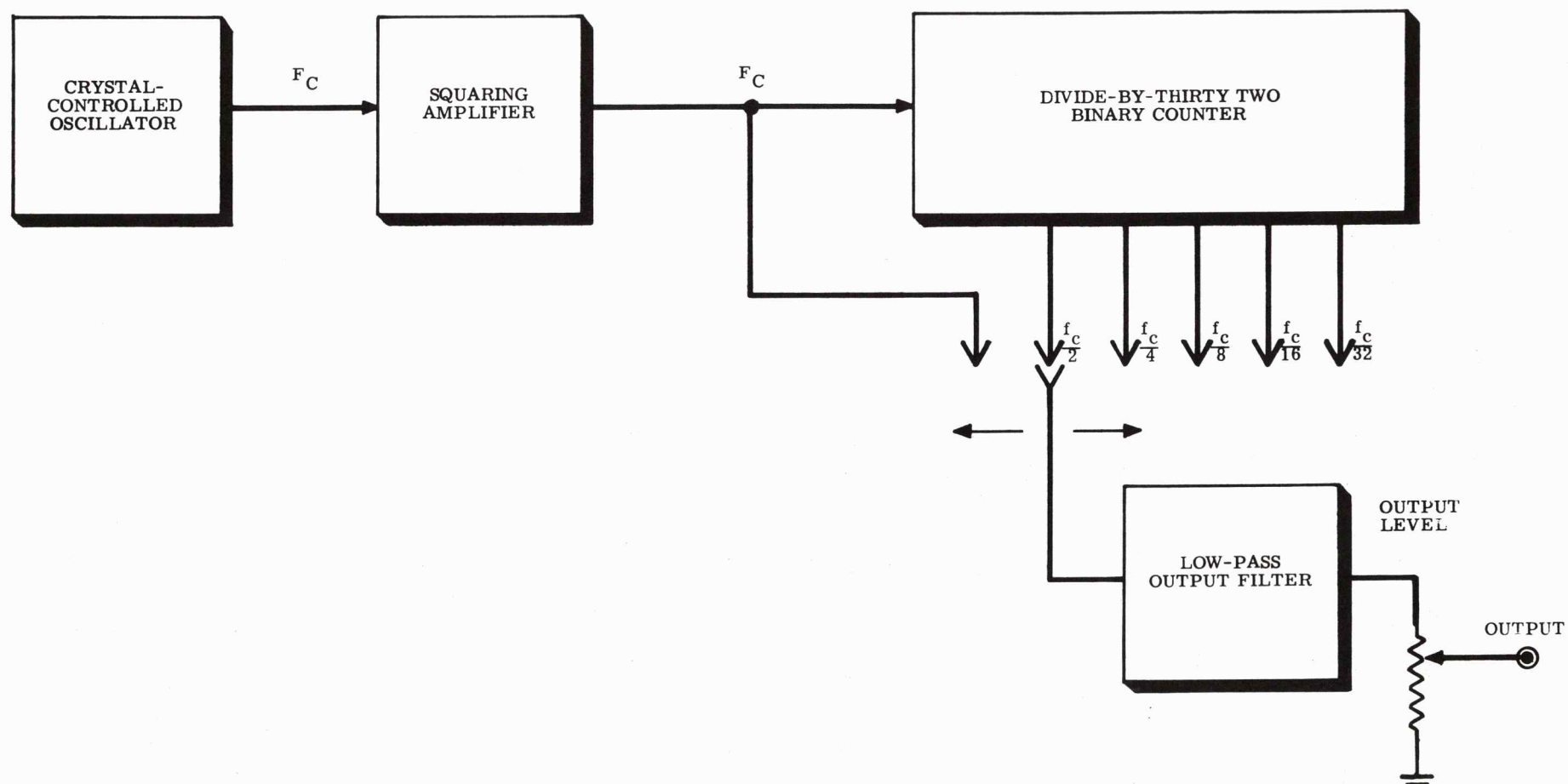


Figure 3-16. Reference Oscillator Simplified Block Diagram

3-101. The low-pass filter is a passive network, with sharp cutoff characteristics at the output frequency. The filter characteristics enable square-wave input signals to be converted to the sine-wave reference signal. A transistor driver stage at the input to the filter provides a high- to low-impedance matching function. The sine-wave reference frequency signal output is applied to an output jack through an output-level control that permits adjustment of the signal from 0 to 2 volts.

3-102. MIXER AMPLIFIER DESCRIPTION.

(To be supplied.)

3-103. SIGNAL SEPARATOR ASSEMBLY.

3-104. SIGNAL SEPARATOR FUNCTIONS.

3-105 The signal separator assembly is used in conjunction with the signal mixer assembly described in paragraphs 3-79 through 3-91. The signal separator assembly and its functional relationship to the signal mixer assembly are illustrated in figure 3-17.

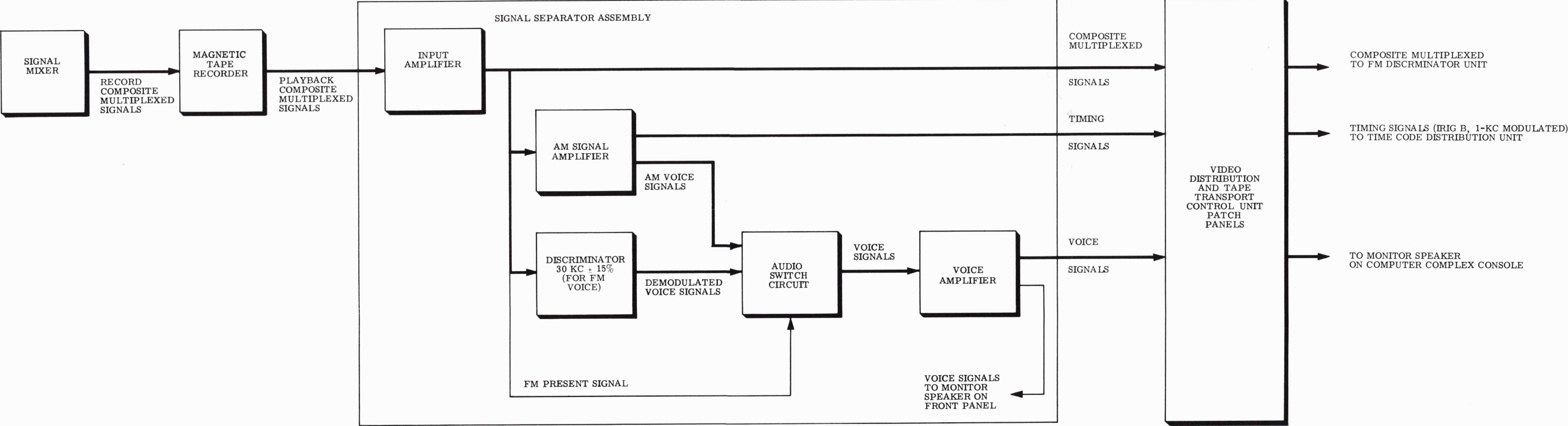
3-106. During the Record Mode of operation, the magnetic recorders record the composite multiplexed signal output of the signal mixer assembly on a single track. During the Playback Mode of operation, the magnetic tape recorders reproduce the composite multiplexed signal previously recorded. This reproduced composite multiplexed signal is routed through the Video Distribution and Tape Transport Control Unit patch panel to the signal separator assembly input.

3-107. The composite multiplexed signal received by the signal separator assembly is made up of an FM component along with an AM component. The FM component is comprised of up to six different subcarrier frequencies that contain voice, AMR B-1 time code, countdown time code, and other information. The AM component is a composite of IRIG B time code, tape transport speed lock, and other auxiliary signals, or may contain voice only. When voice is present, all the other components of the composite multiplexed signal (both FM and AM) will be absent.

3-108. SIGNAL SEPARATOR DESCRIPTION.

3-109. The signal separator assembly input amplifier receives the playback composite multiplexed signal, increases its drive capability, and distributes it as follows:

- a. Directly to the signal separator output, and thence to the Video Distribution and Tape Transport Control Unit patch panel.
- b. To an AM signal amplifier.
- c. To an FM discriminator.



AM2-46-3

Figure 3-17. Signal Separator Functional Block Diagram

3-310. A low-pass filter at the input to the AM amplifier circuit allows only the IRIG B time code signals, or AM voice signals, to be passed and amplified. The IRIG B time code signals output is sent directly to the signal separator assembly output and then to the Video Distribution and Tape Transport Control Unit Patch Panel. When AM voice signals are present, the AM signal amplifier will accept these signals and send them to a voice switch circuit.

3-111. A bandpass filter at the input to the FM discriminator circuit allows only the FM subcarrier containing voice information to be passed and demodulated by the FM discriminator. The demodulated voice signal output of the FM discriminator is sent to a voice switch circuit. The FM voice component of the composite signal is used to operate an audio switch.

3-112. When the FM voice signal is present, the audio switch applies the voice signal output of the FM discriminator to the voice amplifier circuit. When the FM component is not present, the audio switch changes state, and passes the voice signals of the AM signal amplifier to the voice amplifier circuit.

3-113. The output of the voice amplifier is sent to the Video Distribution and Tape Transport Control Unit patch panel. The output of the voice amplifier also drives a monitor speaker located on the front panel of the signal separator assembly.

3-114. The Video Distribution and Tape Transport Unit patch panel distributes the signal separator assembly output signals as follows:

- a. The composite multiplexed signal is routed to the appropriate discriminator located in the FM Discriminator Unit.
- b. The IRIG B timing signals are sent to the Time Code Distribution Unit.
- c. The voice signals are sent to a monitor speaker located on the Computer Complex Console.

3-115. FM DISCRIMINATOR UNIT.

3-116. FM DISCRIMINATOR FUNCTIONS.

3-117. The FM Discriminator Unit separates the incoming FM test data received from the Video Distribution and Tape Transport Control Unit and converts it to analog voltages that are sent to the analog and event display units. The unit contains 12 subcarrier discriminators. The inputs of seven of the discriminators are tied in parallel and receive a composite FM signal containing seven subcarrier frequencies from the spacecraft test area. The inputs of the remaining five discriminators also are tied in parallel and receive a composite FM signal containing five subcarrier frequencies from the signal separator assembly located in the Video Distribution and Tape Transport Control Unit. These signals received from the ACE-S/C system are MULT B1, IRIG B, and countdown time; voice; and a recorder reference signal.

3-118. One subcarrier channel is assigned to each of the 12 discriminators within the FM Discriminator Unit. Each discriminator provides three processing functions:

- a. Selection of the assigned subcarrier channel from the composite FM input signal.
- b. Detection and conversion of the select FM signal to a voltage analogous to the data contained in the FM signal. Phase-locked-loop FM detection is employed.
- c. Filtering and amplification of the detected signal to provide a data output suitable for recording on analog recorders.

3-119. The output of the FM Discriminator Unit is 12 separate analog signals, one from each discriminator. The analog outputs are all sent to the Video Distribution and Tape Transport Control Unit patch panels and to the analog and event display and recording units. The analog data is recorded for data reduction purposes at the conclusion of a spacecraft test sequence.

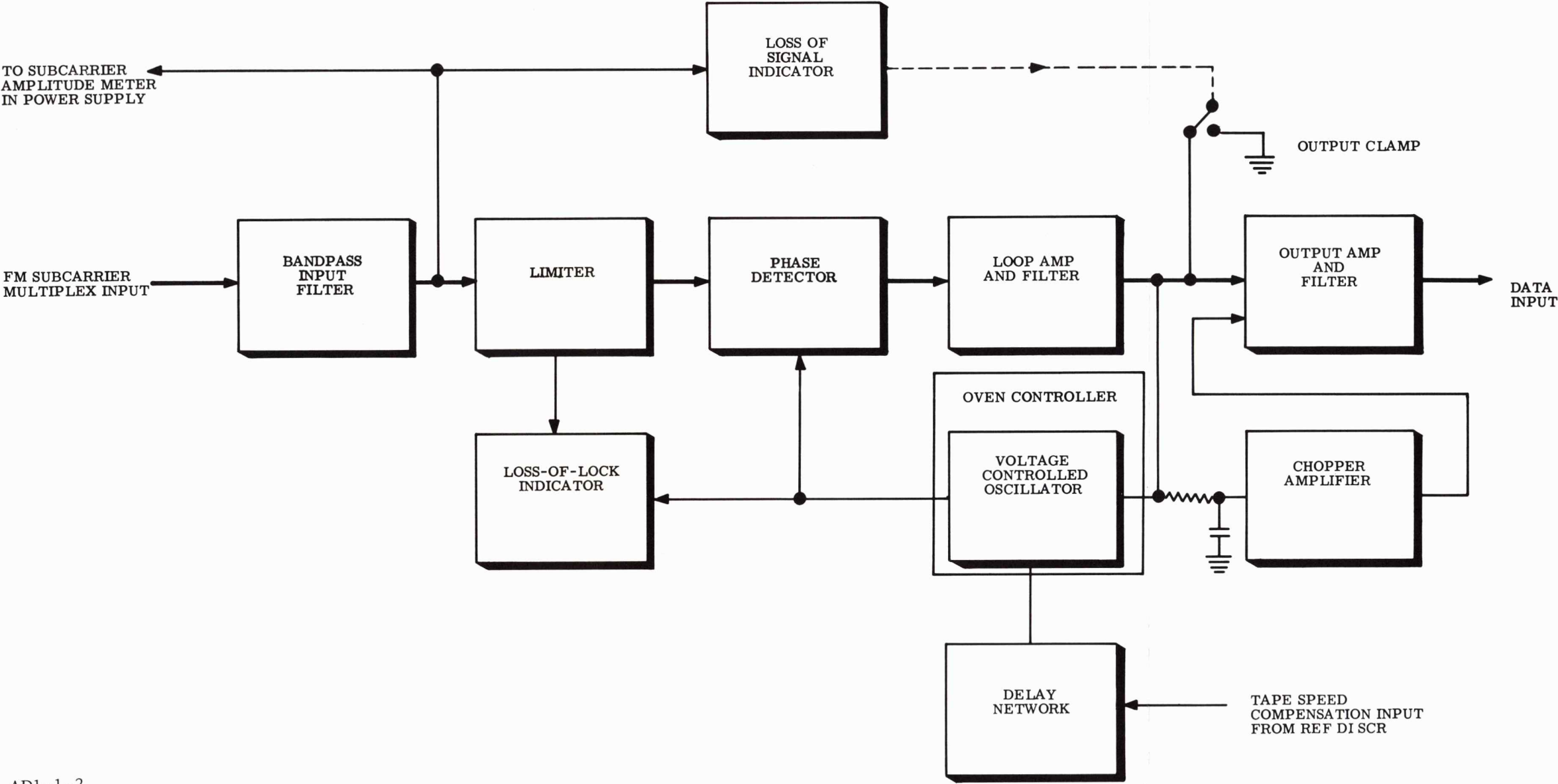
3-120. FM DISCRIMINATOR DESCRIPTION.

3-121. Figure 3-18 is a block diagram of the FM Subcarrier Discriminator. The assigned subcarrier is selected from the FM subcarrier multiplex input by a bandpass input filter and applied to a limiter. The limiter has sufficient gain to provide a substantially constant amplitude square-wave output to the FM detector throughout the 60-db signal range.

3-122. A phase-locked-loop FM detector is employed for detection of the selected FM subcarrier. The phase-locked-loop FM detector provides improved signal-to-noise performance compared to other means of FM detection. The phase-locked-loop detector consists of the phase detector, VCO, and loop amplifier and filter connected as essentially a second-order feedback system. The d-c component of the output of the phase detector is proportional to the phase error between the limiter and VCO signals, 90 degrees phase shift is considered as the zero phase error reference. The phase detector output is amplified and filtered by the loop amplifier and filter, and applied to the VCO in a manner to drive the oscillator to the same frequency as the limiter output signal and to reduce the phase error to zero. The static frequency therefore is always zero and the d-c component of the loop amplifier and filter output or VCO input signal is the detected signal.

3-123. The detected signal is filtered and amplified by the output amplifier and filtered to provide a data output signal suitable for driving recorders.

3-124. Temperature-sensitive components of the VCO are operated in an oven at a constant temperature regulated by the oven controller. Zero drifts in the output amplifier and filter are virtually eliminated by means of the chopper amplifier. The loss-of-lock circuitry provides an indication of loss-of-lock operation and poor input signal quality. The loss-of-signal circuitry provides an indication of low input signal level and clamps the discriminator



AD1-1-2

Figure 3-18. FM Subcarrier Discriminator Block Diagram

data output to ground for input signal of amplitude less than a preset level. A delay network is provided for completion of the tape speed compensation process. The power supply regulators provide highly regulated voltages to all critical circuitry of the discriminator.

3-125. BANDPASS INPUT FILTER. All components of the BPIF are contained in the channel selector. The purpose of the BPIF is to separate a selected subcarrier from the multiplex and reduce the effect of interfering signals. The filter circuitry itself, however, could be the cause of interference. If there was a nonlinearity in the BPIF circuitry, a beat frequency in the passband of the filter could be generated by signals far removed from the passband of the filter.

3-126. The BPIF is a precision network utilizing all passive elements operated well below their saturation levels. Active elements are not used in or ahead of the BPIF circuitry to carry the multiplex signal; thus, additional noise is not introduced into the data channels at low signal levels, and extremely large peak signal level capability is provided to virtually eliminate cross-talk caused by nonlinear amplification.

3-127. The input filter is of a special design so that input impedance increases at frequencies out of the passband. The input impedance at band center is greater than 100 ohms for data frequencies to and including 10.5 kc, and exceeds 10K ohms for frequencies beyond 10.5 kc up to 100 kc. When 18 discriminators are connected in parallel in an 18-channel IRIG subcarrier discriminator system, the system input impedance is greater than 3000 ohms at any frequency from 200 cps to 110 kc.

3-128. The design of the BPIF is such that the time delay through the filter is constant for all subcarrier frequencies in the passband while maintaining sufficient attenuation to prevent adjacent-channel interference. Bandwidths of ± 7.5 percent and ± 1.5 percent of center frequency normally are provided; other bandwidths from ± 2.5 percent to ± 40 percent are supplied to order. The overall BPIF insertion loss is 6 db.

3-129. LIMITER. Three limiting stages are employed to provide two 60 db dynamic input signal range capabilities of the discriminator. The first stage is a nonlinear voltage divider. The second and third limiter stages each contain a common-emitter amplifier and an output emitter follower. The linear gain of the limiter is approximately 2000, and the 3-db frequencies are 50 cps and 500 kc. For minimum input-signal level, only the third stage limits; for maximum input-signal level, all three stages limit.

3-130. PHASE DETECTOR-LOOP AMPLIFIER AND FILTER. These circuits provide combined phase detection, amplification, and filtering with complementary elements for temperature stabilization. Additional input-signal limiting is provided because the limiter output signals are a-c coupled to the phase detector coincidence gates with set switching levels.

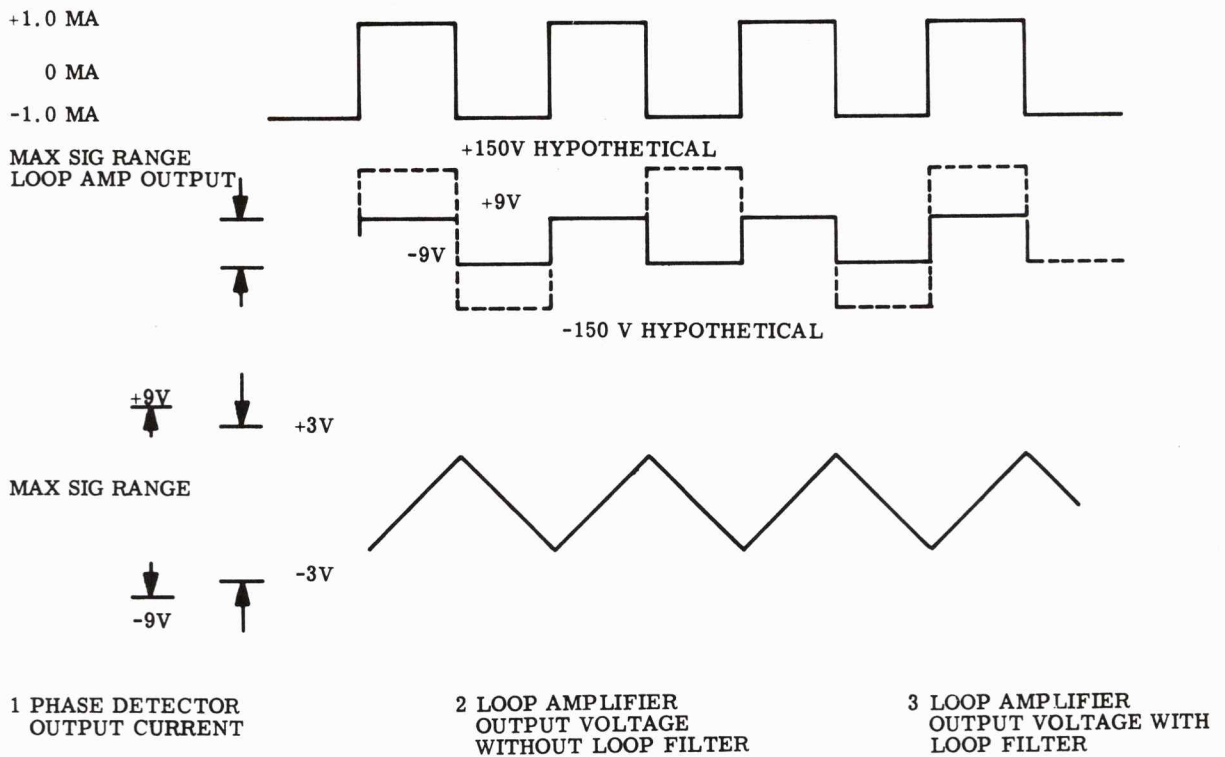
3-131. The static phase-locked-loop phase error, that is the phase error at band edge, is 90 degrees divided by the d-c loop gain, or less than 2 degrees. This low static phase error does not significantly deteriorate the signal-to-noise efficiency of the phase-locked-loop detector. During normal operation of the phase-locked-loop detector, modulation of the FM subcarrier results in a dynamic phase error in the linear range of ± 90 degrees. The duty cycle of the rectangular wave shown in waveform 1 of figure 3-19 is dynamically modulated, and the average signal represents the detected data signal. The output of the loop amplifier is then the data signal with the ripple (twice the subcarrier frequency) shown in waveform 3 superimposed. The second harmonic ripple is removed from the discriminator data output by the output filter.

3-132. VOLTAGE-CONTROLLED OSCILLATOR (VCO). The VCO consists of a modified astable (free-running) multivibrator and a bistable (flip-flop) multivibrator used for output-isolation and wave-shaping.

3-133. The VCO design provides high linearity for the signal input and stability against power supply variations. Diode and transistor function polarities are reverse-connected and operating currents are adjusted to provide a very low temperature coefficient. All transistors and diodes that can affect the VCO operating frequency are stable planar types; resistors are encapsulated low-temperature-coefficient metal-film types. The above considerations, the high stability of the power supplied, and the operation of the VCO in a controlled oven provides the highly stable performance of the VCO.

3-134. VCO OVEN CONTROLLER. All VCO components whose temperature would affect operating frequency are contained in a temperature-controlled oven. The VCO oven temperature is controlled at a constant 65°C by means of a contactless, continuous-control servo loop. Both the VCO and oven-controller components are contained in the oven: This system provides long-term stable operation without the reliability, cycling, and resetting problems associated with mechanical-contact type thermostats.

3-135. The continuous-control servo operates by sensing the temperature electrically, comparing the voltage to a standard, and controlling the oven heater with the amplifier error signal. The error signal is obtained from a resistive bridge. One leg of the bridge is a temperature-sensitive resistor (thermistor); the bridge is only in balance at the temperature determined by the thermistor resistance/temperature characteristic and bridge adjustment. The bridge error signal is amplified, and the output signal is applied to the oven heater in such a manner as to keep the bridge in balance and the internal oven temperature constant regardless of the operating temperature of the discriminator in its range.



AD1-2-2

Figure 3-19. FM Subcarrier Discriminator Idealized Waveforms

3-136. **OUTPUT FILTER AND POWER AMPLIFIER.** The output filter consists of a high-gain power amplifier and chopper amplifier for d-c stabilization connected in the configuration of an analog low-pass filter which contributes 18 db per octave to the total rolloff. The input signal to the output amplifier is the output of the loop amplifier having a signal range of ± 3.0 volts corresponding to full bandwidth. The output signal at the feedback reference point (pin 10 of connector 1J3) is ± 1 volt, filtered, at band edges; the gain to this point is minus one third. The amplifier full-scale output voltage is ± 1 volt to ± 10 volts, depending upon the setting of the BANDEDGE VOLTS control. Frequency-determining components for the analog low-pass filter are contained in the output filter; values are switched in the output filter to provide either the constant-delay or constant-amplitude response. A seven-pole passive filter is contained in the output filters to provide 42 db per octave rolloff.

3-137. Dual frequency inputs to the gain stages of the output amplifier are provided by a crossover network with a crossover frequency of 50 cps. High frequencies are coupled directly into the output amplifier while low frequencies and direct current are coupled from the output of the chopper amplifier. The low-frequency open-loop gain of the output amplifier is 10,000.

3-138. The excellent d-c stability (versus operating time, supply variations, and temperature changes) of the output amplifier is accomplished by the addition of an open-loop gain of 1000 in the chopper amplifier ahead of the output amplifier.

3-139. CHOPPER AMPLIFIER. The input to the chopper amplifier is the d-c error signal obtained from the feedback network of the analog, low-pass output filter. A-c components of this signal are filtered out. The d-c gain of 1000 of the chopper amplifier, connected ahead of the output amplifier, has the effect of dividing the equivalent drift at the input of the output amplifier by 1000. Since the input stage of the output amplifier is a special low-drift silicon transistor, extremely stable d-c operation is provided.

3-140. The d-c gain of the chopper amplifier is accomplished by modulating the d-c error signal by means of a shunt-type chopper. This type of chopper has the advantages of very low d-c drift, low-term stability, infinite life, and high-frequency operation. The output of the chopper is a 6-kc square wave, whose amplitude is proportional to the d-c error signal of the output amplifier, and whose phase is either zero or 180 degrees, depending on the polarity of the error signal. The high chopping frequency in conjunction with an RC network provides very low intermodulation distortion of discriminator output signals harmonically related to the chopper frequency.

3-141. The a-c error signal is amplified and converted back to a d-c signal by a complementary synchronous detector. The 6-kc signals driving both the chopper and synchronous detector are the outputs of an astable (free-running) multivibrator. Adjustment of the output amplifier d-c offset is accomplished by feedback of a properly phased signal to the input of the ac-coupled chopper amplifier.

3-142. PERCENT BANDEDGE METER. The percent bandedge meter and its series multiplier resistor are connected at the input of the voltage-controlled oscillator. The meter has a center balance movement and, with the multiplier resistor, a sensitivity of ± 3.0 volts for full-scale deflection. The meter scale is calibrated to ± 100 percent from center. Since ± 3.0 volts at the VCO input corresponds to bandedge frequency deviation, the meter indicates percent of bandedge frequency deviation regardless of the position of the BANDEDGE VOLTS control.

3-143. SIGNAL LOSS CIRCUIT. When the subcarrier amplitude falls below a predetermined threshold level for a significant period of time, the signal loss circuit energizes the SIGNAL LOSS light and clamps the discriminator output to ground. The output of the second limiter stage (first gain stage) is coupled to a feedback amplifier. The amplifier output is converted to a d-c signal whose amplitude is proportional to signal amplitude by a full-wave voltage-doubling rectifier.

3-144. LOSS-OF-LOCK CIRCUIT. The phase relationships between the limiter and VCO signals during normal operation of the phase-locked-loop detector are shown in figure 3-20. Limiter output signal A (waveform 1) is coupled to the loss-of-lock circuit via an isolator transistor stage. VCO output signal B (waveform 4) is coupled to the loss-of-lock circuit by an isolator-shaper transistor stage, which inverts the signal, phasing it with VCO output signal A (waveform 2). The VCO signal is differentiated and added to the limiter signal by a resistive matrix whose output serves as a coincidence gate (refer to waveform 3).

3-145. The operation of the phase-locked-loop is normal when phase error between the limiter and VCO signals is less than ± 90 degrees. When the phase error exceeds ± 90 degrees, however, the phase-locked-loop goes into loss-of-lock operation (figure 3-20, waveform 4).

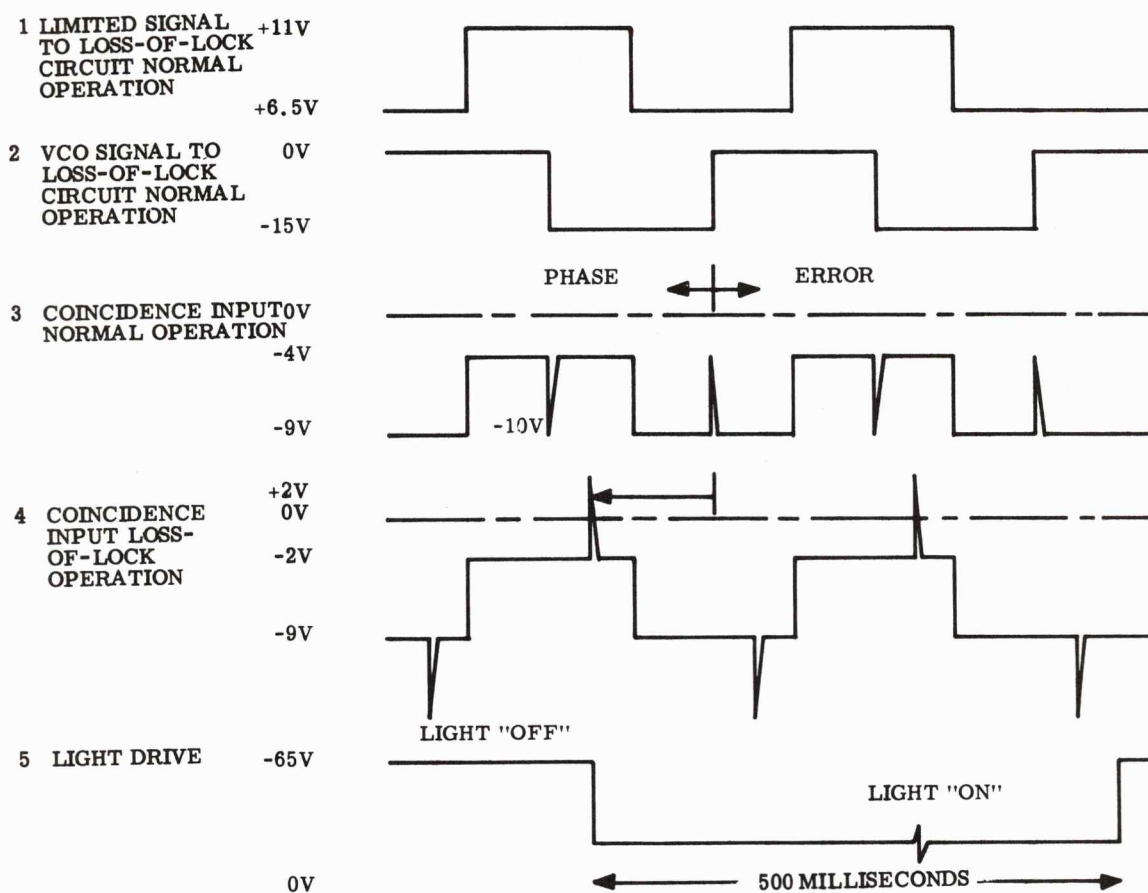
3-146. DELAY NETWORK. The delay network is necessary to delay the tape-speed error signal applied to the VCO, an amount equal to the time delay of the bandpass input filter. D-c tape-speed error signals are coupled to the tape-speed-compensation input of the VCO. Because the d-c error signal is not transmitted to the VCO by active elements, the delay network does not contribute drift instability to the discriminator circuitry. The a-c tape error signal is coupled to the tape-speed-compensation input of the VCO.

3-147. REFERENCE CHANNEL SELECTOR. The channel selector is identical to the band-pass input filter with the following exceptions:

- a. Output filter frequency-determining components are not independently variable but are fixed for a given reference frequency.
- b. All delay network components are deleted.
- c. The front-panel switch is used as the tape-speed-compensation ON-OFF switch by disconnecting the input of the discriminator output amplifier from the phase-locked-loop detector and connecting it to ground.
- d. Delay (D) and gain (G) adjustments of the reference discriminator are accomplished by means of potentiometers which, being connected in the feedback network of the output filter, vary its phase shift and gain.

3-148. SUBCARRIER AMPLITUDE METER. The subcarrier amplitude meter and its associated DISCRIMINATOR and METER RANGE switches are mounted on the front panel of the power supply. The meter indicates the rms magnitude of the subcarrier signal at the output of the BPIF of each discriminator in the rack adapter, but is calibrated with reference to the center-frequency amplitude of the subcarrier signal of the discriminator input.

3-149. POWER SUPPLY REGULATORS. All circuitry of the discriminator, other than the power output stages of the output amplifier, the VCO and heater, and the SIGNAL LOSS and LOCK LOSS neon lights, are supplied by plus and minus 15-volt highly regulated power.



AD1-3-2

Figure 3-20. Idealized Waveforms, FM Subcarrier Discriminator Loss-of-Lock Circuit

This power is furnished by two power-supply regulators, one for each supply polarity, which receive their power from the plus and minus 17.5 volt preregulated output of the power supply. The output current of the supply regulator is limited to 150 percent or less of its normal load current, thus providing short-circuit protection to itself and continuous operation of other discriminators in a rack adapter connected to the same power supply.

3-150. FM CALIBRATION UNIT.

3-151. FM CALIBRATION UNIT FUNCTIONS.

3-152. The FM Calibration Unit provides a means of testing various subassemblies of the FM recording equipment. The unit contains an FM telemetry indicator, a telemetry calibrator, and an electronic counter. Each of these assemblies is described in the following paragraphs.

3-153. FM TELEMETRY INDICATOR DESCRIPTION.

3-154. The FM telemetry indicator is part of the FM Calibration Unit 166. The indicator provides a means of checking FM equipment operation, subcarrier channel center frequencies, and channel limits. It can be used to monitor the entire telemetry band to confirm the presence of subcarriers and to check their operating levels. The equipment also is able to display the channel location and level (relative to subcarrier amplitude) of noise, intermodulation distortion, and other spurious signals.

3-155. Two modules of operation can be selected:

- a. A logarithmic sweep can be selected to display the entire spectrum from 350 cycles to 200 kc. A complete scan occurs once per second.
- b. A linear sweep can be selected to display any subcarrier center frequency between 350 cycles and 200 kc and sweep widths from 100 cycles to 22 kc. A scan of the selected portion of the spectrum occurs once per second.

3-156. Input signals to the indicator are applied to a phase splitter via a calibrated input attenuator and cathode follower. (See figure 3-21.) The attenuator provides a maximum of 80-db attenuation of the input signal.

3-157. Four marker frequencies can be injected into the cathode circuit of the phase splitter. Markers of 350 cycles, 5 kc, 100 kc, and 200 kc are provided for calibration purposes. The 350-cycle and 5-kc markers are provided by an audio oscillator. The 100-kc and 200-kc markers are provided by two crystal oscillators. Marker amplitudes are not affected by the input attenuator because they are combined and injected following signal attenuation.

3-158. The phase splitter output and the swept oscillator output are mixed to derive the sum and difference products at the output of the balanced mixer.

3-159. When the SWEEP RANGE SELECTOR switch is in the LIN position, the swept oscillator frequency is controlled by a linear sawtooth waveform. The linear sum and difference frequencies are then present at the output of the balanced mixer. When the SWEEP RANGE SELECTOR switch is in the LOG position, an exponential waveform is generated and controls the swept oscillator. The swept oscillator frequency then varies logarithmically, and the logarithmic sum and difference frequencies appear at the output of the balanced mixer.

3-160. The input of the IF section is a 226-kc tuned circuit that selects the difference products for amplification. The IF section consists of three stages of amplification and two 226-kc crystal filters.

3-161. The frequency resolution of the indicator or ability to separate individual frequencies is a function of the instantaneous rate of frequency scan and the selectivity of the IF stages. Optimum resolution is obtained when a definite relationship exists between the two.

3-162. In the LOG position of the SWEEP RANGE SELECTOR switch, the instantaneous rate of frequency scan (swept oscillator frequency) is varying continuously, following a logarithmic function. Consequently, the IF selectivity (bandwidth) must vary accordingly to maintain optimum resolution, as explained in the preceding paragraph. The IF bandwidth is automatically varied by changing the impedance of the crystal-filter load coils. This is accomplished by varying the impedance of two selectivity control tubes that forms part of the crystal-filter loads. In this way, IF selectivity is automatically varied in step with the frequency scan to maintain optimum resolution.

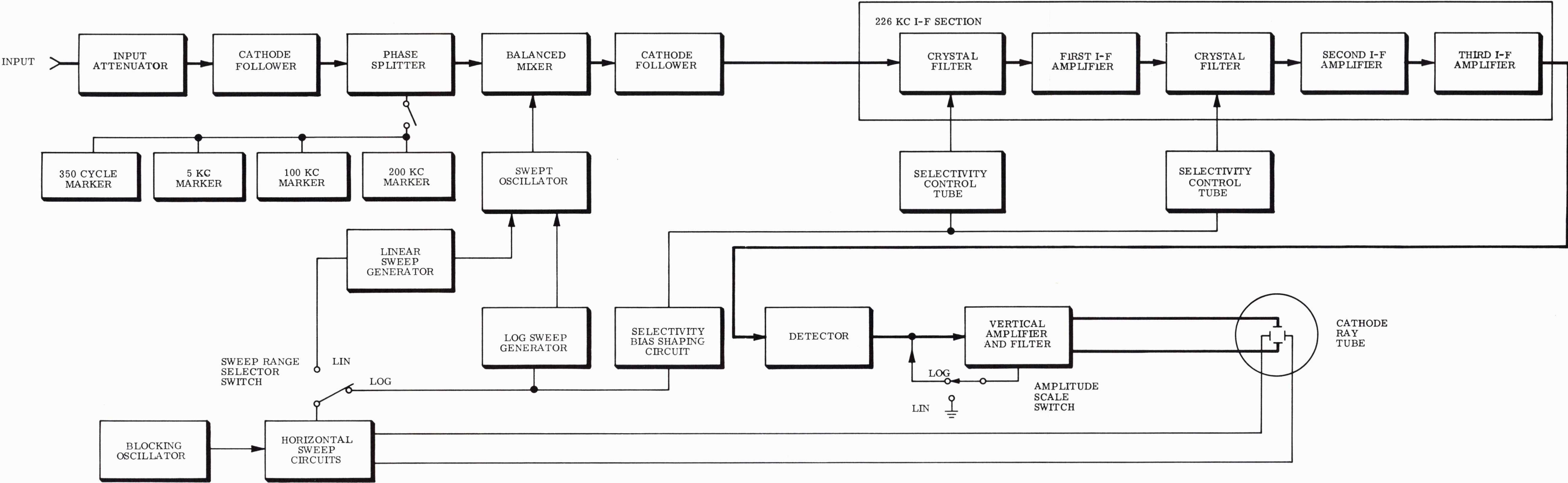
3-163. Following the IF section are the detector, and vertical amplifier and filter. Part of the vertical-amplifier output can be fed back by setting the amplitude-scale switch to LOG. Without this negative feedback, amplitude ratios of 10 to 1 can be observed in the cathode ray tube. Ratios as high as 100 to 1 can be observed when feedback is introduced.

3-164. The vertical output is connected to the cathode ray tube vertical plates in push-pull. A video filter is included in the vertical amplifier stages to reduce spurious beats that result when two signals are close in frequency.

3-165. The sawtooth generator and horizontal sweep circuits are conventional and require no explanation.

3-166. FM TELEMETRY CALIBRATOR DESCRIPTION.

3-167. The FM telemetry calibrator is part of FM Calibration Unit 166 and is used to test and align the FM subcarrier discriminators. The calibrator is comprised of a group of crystal-controlled frequency generators capable of generating 11 equally spaced deviation



AD3-3-0

Figure 3-21. FM Telemetry Indicator
Simplified Block
Diagram

frequencies sequentially within each of 21 FM subcarrier channels. The center frequencies of the subcarrier channels range from 400 to 165,000 cps.

3-168. Within each of the subcarrier channels, the following 11 calibrated deviation frequencies (expressed in percentage of deviation from subcarrier center frequency) are provided: -7.5, -6, -4.5, -3, -1.5, 0, +1.5, +3, +4.5, +6, and +7.5 percent.

3-169. Within subcarrier channels 14 through 18 (22 to 70 kc), a choice is provided between the above 11 deviation frequencies and the following deviation frequencies: -15, -12, -9, -6, -3, 0, +3, +6, +9, +12, and +15 percent.

3-170. Figure 3-22 illustrates the basic operation of the FM calibrator. Model A1, for example, contains 11 separate crystal oscillator stages. Oscillator Y6 is used to derive the center frequencies of four subcarrier channels (30, 40, 52.5, and 70 kc), and the remaining oscillators are used to derive the deviation frequencies.

3-171. At any given time, only one of the 11 oscillator stages is feeding into the pulse amplifier and counter chain. At periodic intervals, a control network on module A9 automatically switches out one oscillator and switches in the next successive oscillator. In this manner, stepping is accomplished through the 11 deviation points.

3-172. Control and switching module A9 (figure 3-23) consists of a relaxation oscillator, monostable multivibrator, a counter, and gating network. The output of the counter is used to sequentially gate the 11 oscillators on and off. The time that each oscillator is on (dwell time) is adjustable and is determined by the frequency of the relaxation oscillator, which feeds the multivibrator and counter.

3-173. The outputs of the various oscillator/divider modules are fed through filter assemblies and are applied to a summing network. This network isolates the various frequencies on the one hand and provides a composite output on the other. Each isolated frequency is applied to a channel selector switch that grounds all but the selected output frequency. The composite output and the selected output then are fed through level controls and are amplified.

3-174. The composite amplifier consists of three differential amplifiers that provide the stringent linearity control required for multifrequency handling. Each differential amplifier is phase corrected and employs negative feedback to provide flat response over all frequencies.

3-175. FREQUENCY COUNTER DESCRIPTION.

(To be supplied.)

3-176. DECOMMUTATOR UNIT.

3-177. DECOMMUTATOR UNIT FUNCTIONS.

3-178. The decommutator unit provides the processing necessary to convert the incoming eight-bit serial PCM test data words into parallel format and address them for distribution within the remainder of the ACE-S/C display and recording equipment. Bit synchronization is achieved at the decommutator input and each pulse is reshaped to assure good bit definition prior to further processing. The serial data bits are read into a shift register. As the data is shifted through the register, prime frame synchronization is established. Following prime-frame synchronization, subframe synchronization is established. At this point, the location and identity of each eight-bit data word is known. The data is read out of the shift register in parallel format and is presented to the decommutator output. The various outputs of the decommutator units are formulated in accordance with the current decommutator program instructions. The output of each decommutator unit is routed to the alphanumeric display units (via the display computer) and to the analog and event display and recording units.

3-179. DECOMMUTATOR INPUTS. Each decommutator unit receives the following prime inputs:

- a. Interleaved PCM test data.
- b. Airborne PCM test data.
- c. Playback PCM test data (either interleaved or airborne PCM test data, depending upon the current patch-panel wiring configuration of the Video Distribution and Tape Transport Control Unit).

3-180. All incoming data is received as a continuous serial bit stream formatted in eight-bit data words. Each of the eight-bit data words received is representative of analog or event information and may be received in an intermixed form. An input selector switch (located on the front panel of each decommutator unit) selects one of the three inputs to enter a decommutator unit for processing. In normal operation, the positions of the input selector switches will be such that one decommutator unit will process airborne PCM test data while the other decommutator unit will process interleaved PCM test data. A fourth input is synthetic PCM data that is generated by a built-in PCM signal simulator. During maintenance activities, the simulated PCM signals may be substituted for the signals received in normal operation.

3-181. DECOMMUTATOR OUTPUTS. The PCM data selected for decommutator processing is presented to the decommutator output circuits in the following forms:

- a. Analog: Up to 40 data words (selected by the decommutator program) are transformed to analog voltages by 40 built-in digital-to-analog (D/A) converter units. The 40 analog

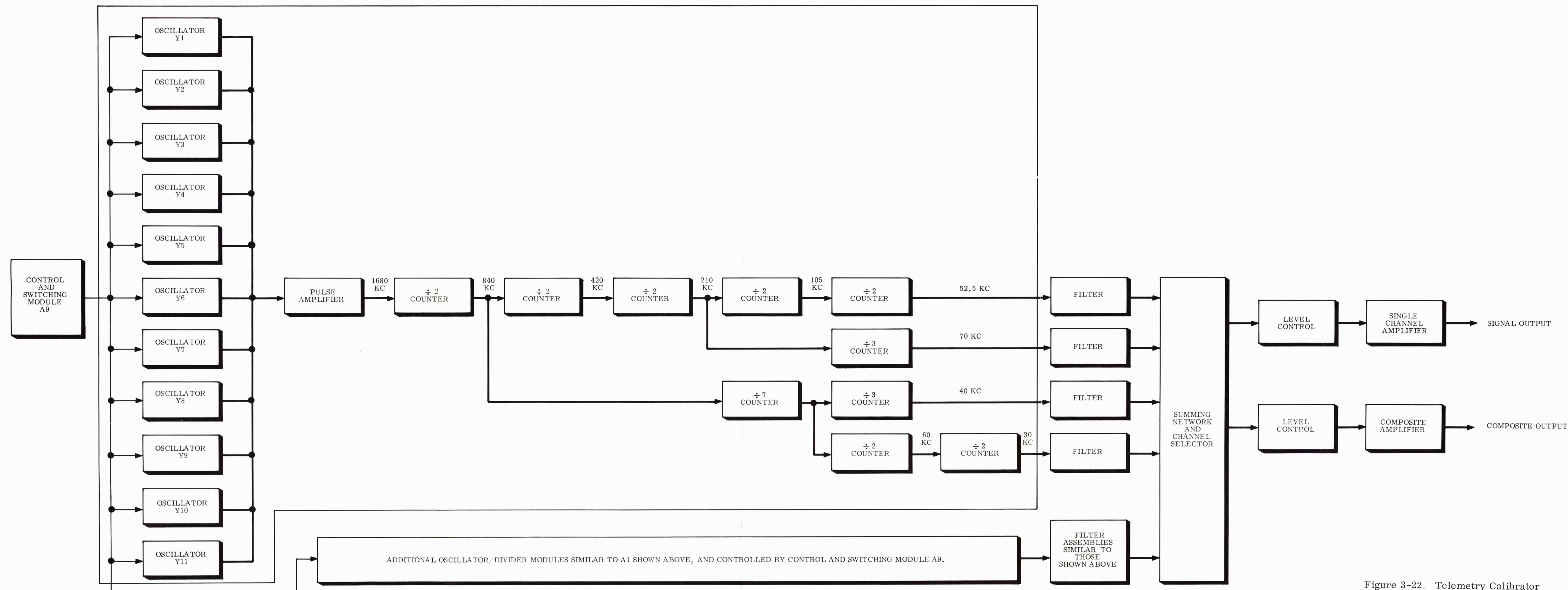
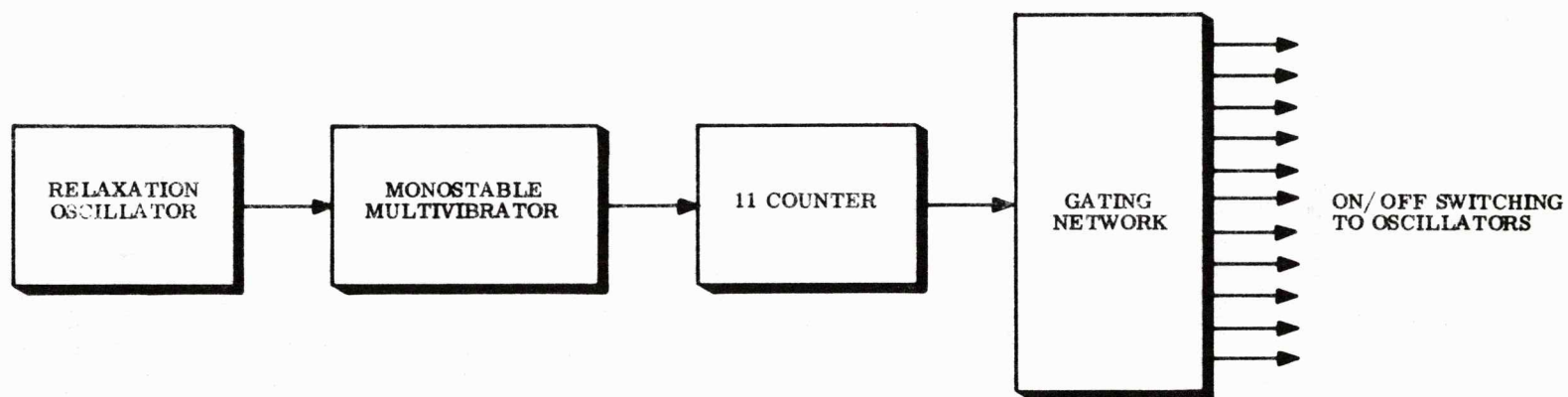


Figure 3-22. Telemetry Calibrator Block Diagram



AD3-2-0

Figure 3-23. Switching Module Block Diagram

outputs of each decommutator unit are sent to the computer room analog and event display and recording units.

b. Addressed PCM data words: The eight-bit data words processed by a decommutator are loaded into a parallel output register along with a 12-bit address that is assigned by the decommutator program. The 20-bit addressed data words are strobed out in a broadside manner along with a timing read pulse. These PCM test data words may represent either analog or event data, and appear at a decommutator output in an intermixed form. The addressed PCM test data words are transmitted via 21 hardlines (8 data, 12 address, and 1 read pulse) from each of the decommutator units to the analog and event display and recording units.

c. Unaddressed PCM test data words: The unaddressed PCM test data words are eight bits in length and are the same eight-bit data words as those that were addressed and sent to the analog and event display and recording units. The unaddressed parallel eight-bit data words are sent (via a decommutator/computer interface unit) to the display computer where they are processed for presentation on the alphanumeric display units.

d. Reconstructed data: The decommutated data, in addition to being fed to the decommutator output in parallel formats, is also available in the forms of NRZ-C and NRZ-M coded serial digital test data. This output is fed to the Video Distribution and Tape Transport Control Unit patch panels and thence to a magnetic tape recorder.

3-182. The computer interface unit provides for the bi-directional transmission of data and instructions between a decommutator and the display computer. The transmission of data and instructions between a decommutator and the display computer is over two 24-hardline cables: an output cable and an input cable. (See figure 3-24.) Twelve lines of a decommutator output cable are reserved to convey test data and status information to the display computer. The remaining 12 lines of a decommutator output cable are used for sending control functions to the display computer. Twelve lines of a decommutator input cable are used to program the decommutator memory or to transmit special coded command inputs to a decommutator from the display computer. The remaining 12 lines of a decommutator input cable convey special control functions from the display computer.

3-183. Control function words are used to logically connect a decommutator to the display computer and vice versa. Because the decommutator units operate asynchronously with respect to the display computer, a sequence of control function words is used to initiate the presentation and acceptance of information. Only the display computer is allowed to initiate an information transfer. Once the display computer has requested and initiated a data transfer from a decommutator unit, that particular decommutator unit will continue to transfer eight-bit parallel data words to the display computer until the end of a prime frame. If the

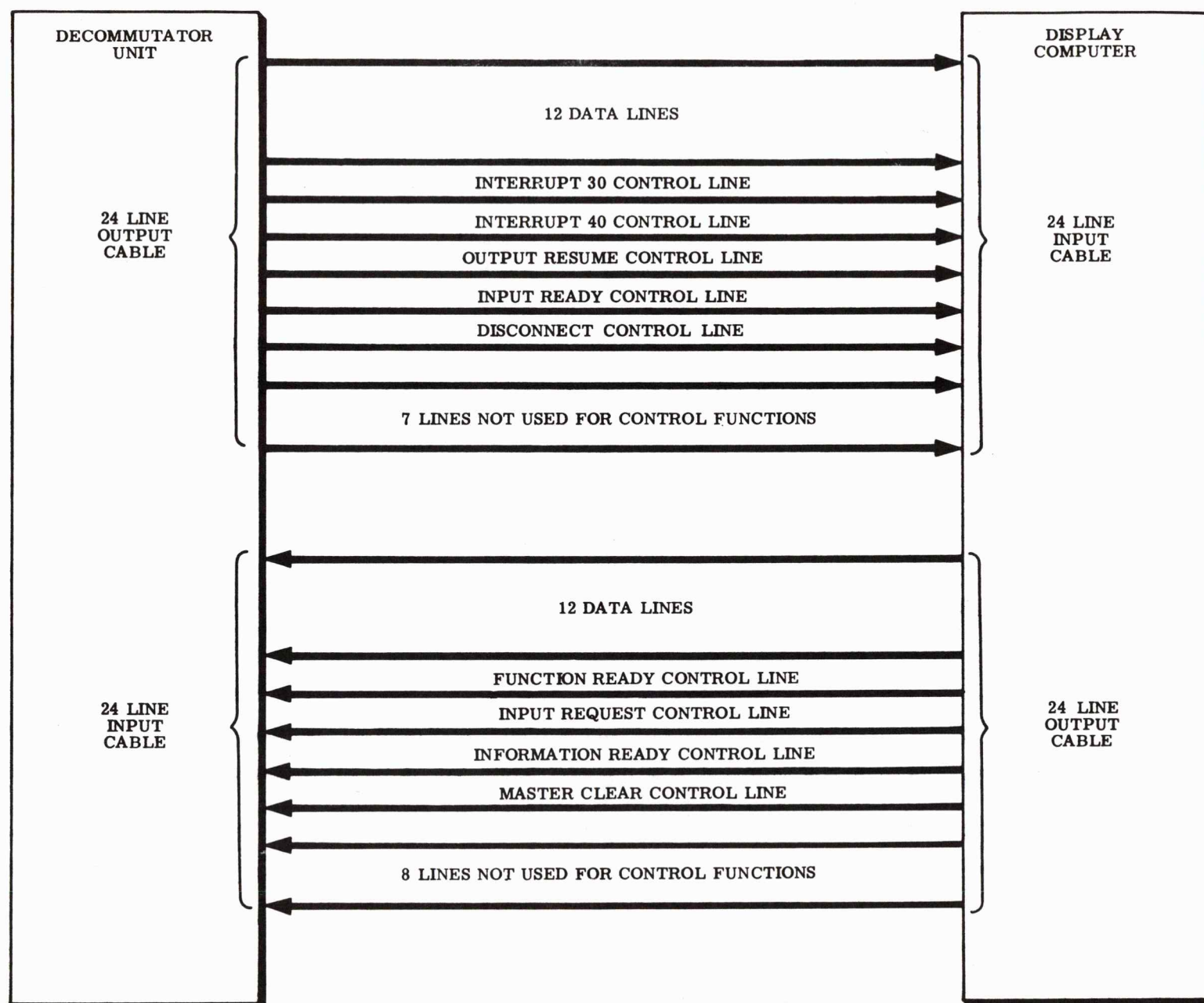


Figure 3-24. Decommutator/Computer Connections

AM2-22-3

display computer program requires the next prime frame of data, there is time for the display computer to again establish communication with the decommutator after the last word in the previous prime and before the first word in the next prime frame. A typical decommutator to display computer information transfer sequence is given in table 3-2.

Table 3-2. Decommulator to Computer Information Transfer Sequence

STEP	ACTION
1	The display computer places a 12-bit function control word on its 12 data output lines and raises the Function Ready control line. The 12-bit function control word prepares the decommutator that is addressed to send its information to the computer.
2	The decommutator responds to the function control word by raising the Output Resume control line.
3	The computer recognizes the Output Resume signal and reacts by lowering the Function Ready control line.
4	The decommutator reacts to the lowering of the Function Ready control line by lowering the Output Resume control line.
5	The computer responds to the lowering of the Output Resume control line by raising the Input Request control line.
6	The decommutator responds by raising the Input Ready control line and places a 12-bit data word on the decommutator output data lines. The first word sent is the first word after frame sync. Only 8 bits and 12 data words are used for the actual data, the remaining 4 bits are filled with zeros.
7	The computer recognizes the Input Ready signal, accepts the data words, and signals the decommutator by lowering the Input Request control line.
8	The decommutator reacts to the lowering of the Input Request control line by lowering the Input Ready control line.
9	Under the control of the computer program, the computer again raises the Input Request control line and steps 5 through 8 are repeated for each data word to be transferred to the computer until the end of a prime frame of data when the decommutator sends an Input Disconnect or an Interrupt 1 to the computer (the signal sent to the computer depends upon the computer programming requirements and is determined by a switch on the interface unit). If the computer requires another frame of data it must repeat steps 1 through 9. (There is time for the computer to do this after the last word in the prime frame and before the first word of the next frame.)

3-184. The computer will initiate an information transfer to a decommutator unit whenever the computer program calls for such a transfer, and this can occur anywhere in the computer program. To accomplish an information transfer to a decommutator, the computer first establishes communication with a decommutator, and then asks for the status of the decommutator unit to determine if that decommutator can or cannot receive data. When the status response of a decommutator indicates that it can receive data, the computer prepares the decommutator unit to receive data. The computer then commences to transfer a block of data to the decommutator unit and continues to do so until a change in the computer routine is called for by the computer program. A typical computer to decommutator information transfer sequence is given in table 3-3. The bit assignment and bit weight meaning of a decommutator status response in reply to a request for status by the computer are given in table 3-4. The function instruction words and their bit content as issued by the computer and received by a decommutator unit are given in table 3-5.

Table 3-3. Computer to Deccommutator Information Transfer Sequence

STEP	ACTION
1	The display computer places a 12-bit function control word on its 12 data output lines and raises the Function Ready control line. The function control word in this case will be a request for the status of a particular decommutator unit.
2	The appropriate decommutator unit responds by raising the Output Resume control line and loads its status code in an output register.
3	The computer recognizes the Output Resume signal and reacts by lowering the Function Ready control line.
4	The decommutator reacts to the lowering of the Function Ready control line by lowering the Output Resume control line.
5	The computer responds to the lowering of the Output Resume control line by raising the Input Request control line.
6	The decommutator responds by raising the Input Ready control line and places the 12-bit status word on the decommutator data output lines. (The bit weight of a status response is shown in table 3-4.)
7	The computer recognizes the Input Ready signal, accepts the status word, and signals the decommutator by lowering the Input Request control line.
8	The decommutator reacts to the lowering of the Input Request line by lowering the Input Ready control line.

Table 3-3. Computer to Decommutator Information Transfer Sequence (Cont' d)

STEP	ACTION
9	After analyzing the received status word, the computer places another 12-bit function control word (select output 3X02) on its data output lines and raises the Function Ready control line. In this case, the function control word will cause the decommutator to prepare to receive programming data from the display computer for loading into the decommutator memory.
10	The decommutator reacts by preparing to receive data from the computer and raising the Output Resume control line.
11	The computer recognizes the Output Resume signal and reacts by lowering the Function Ready control line.
12	The decommutator reacts to the lowering of the Function Ready control line by lowering the Output Resume control line.
13	The computer then places a 12-bit data word on its data output lines and raises the Information Ready control line.
14	The decommutator recognizes the Information Ready signal, accepts the data word, and signals the computer by raising the Output Resume control line.
15	The computer reacts to the raising of the Output Resume control line by lowering the Information Ready control line.
16	The decommutator reacts to the lowering of the Information Ready control line by lowering the Output Resume control line.
17	Under the control of the computer program, the computer again raises the Information Ready control line and steps 13 through 16 are repeated for each data word to be transferred to the decommutator, or until the computer program calls for a change in routine.

Table 3-4. Decommutator Status Word Bit Weight and Assignment

BIT NO.	BIT FUNCTION ASSIGNMENT
1	Logic 0 = Decommutator able to accept data from computer. Logic 1 = Decommutator "Busy"; not able to accept data from computer.
2	Logic 0 = Decommutator has established sync with the incoming PCM data. Logic 1 = Loss of sync.
3	Logic 0 = LOCAL switch position. Logic 1 = LOCAL/REMOTE switch position.

Table 3-4. Decommutator Status Word Bit Weight and Assignment (Cont'd)

BIT NO.	BIT FUNCTION ASSIGNMENT
4	Logic 0 = Function control word other than Status Request required from computer. Logic 1 = Disconnect from computer.
5	Logic 0 = Interrupt 40 sent by this decommutator. Logic 1 = Interrupt 30 sent by this decommutator.
6	Logic 0 = This decommutator not in data acquisition mode. Logic 1 = This decommutator is in data acquisition mode.
7, 8, and 9	The bit combination of these three bits indicates which mode (program, format, etc.) this decommutator is currently using. The bit combinations are listed below: Mode 1 = 0 0 1 Mode 2 = 0 1 0 Mode 3 = 0 1 1 Mode 4 = 1 0 0 Mode 5 = 1 0 1 Mode 6 = 1 1 0 Mode 7 = 1 1 1 Mode 8 = 0 0 0
10 and 11	Unused; will always be zeros.
12	Logic 0 = Function word code other than Status Request was last received by this decommutator from the computer. Logic 1 = An Interrupt 30 or 40 was generated by this decommutator.

Table 3-5. Computer Function Control Words to Decommutator Units

FUNCTION NAME	FIRST OCTAL DIGIT	SECOND OCTAL DIGIT (SELECTS DECOM NO. 1 OR DECOM NO. 2)	THIRD OCTAL DIGIT	FOURTH OCTAL DIGIT
Select Input	3	1 or 2	0	1
Select Output	3	1 or 2	0	2
Select Mode 1	3	1 or 2	1	1

Table 3-5. Computer Function Control Words to Decommutator Units (Cont'd)

FUNCTION NAME	FIRST OCTAL DIGIT	SECOND OCTAL DIGIT (SELECTS DECOM NO. 1 OR DECOM NO. 2)	THIRD OCTAL DIGIT	FOURTH OCTAL DIGIT
Select Mode 2	3	1 or 2	1	2
Select Mode 3	3	1 or 2	1	3
Select Mode 4	3	1 or 2	1	4
Select Mode 5	3	1 or 2	1	5
Select Mode 6	3	1 or 2	1	6
Select Mode 7	3	1 or 2	1	7
Select Mode 8	3	1 or 2	1	0
Clear Decom	3	1 or 2	2	0
Status Request	3	1 or 2	4	0

3-185. MAINTENANCE FEATURES. Certain maintenance aids are built into the decommutator units. One such maintenance aid is the means by which any word of the incoming data may be displayed either in decimal form or binary form. The data word is displayed on decimal or binary indicators located on the decommutator front panel. Up to four words may be displayed at the same time: three in decimal form and one in binary form. Thumb-wheel switches associated with each word display permit the selection of the test data word to be monitored. By the use of the test data word displays a maintenance technician can isolate trouble to either the spacecraft test area or the ACE-S/C display and recording equipment without causing an interruption in normal operation. The data word display feature also can be used to isolate troubles within the decommutator units themselves.

3-186. Another built-in maintenance aid is a PCM signal simulator. The PCM signal simulator is capable of providing a wide range of PCM data and synchronization signals. The sync and PCM data words to be simulated are manually programmed into the PCM signal simulator by means of panel selection switches. The data rate, content, and frame location are at the discretion of a maintenance technician.

3-187. During tests requiring the use of the PCM signal simulator, the signals generated by the simulator replace the normal operating inputs to the decommutator unit. As a result,

when the PCM signal simulator is in use, normal system operations are interrupted. The selection of PCM simulator signals as the input to a decommutator is accomplished by means of the decommutator input selection switch. The PCM signal simulator can be used for the checkout, calibration, pre-operational evaluation, and troubleshooting of the decommutator units themselves and/or some of the units that receive a data input from the decommutator units.

3-188. Various front panel mounted meters, indicators, and monitoring test jacks are also available on each decommutator unit. By the use of these built-in monitoring devices, a maintenance technician can determine the current operational status of a decommutator unit. The monitoring devices are also useful in isolating troubles within the decommutator units.

3-189. DECOMMUTATOR UNIT DESCRIPTION.

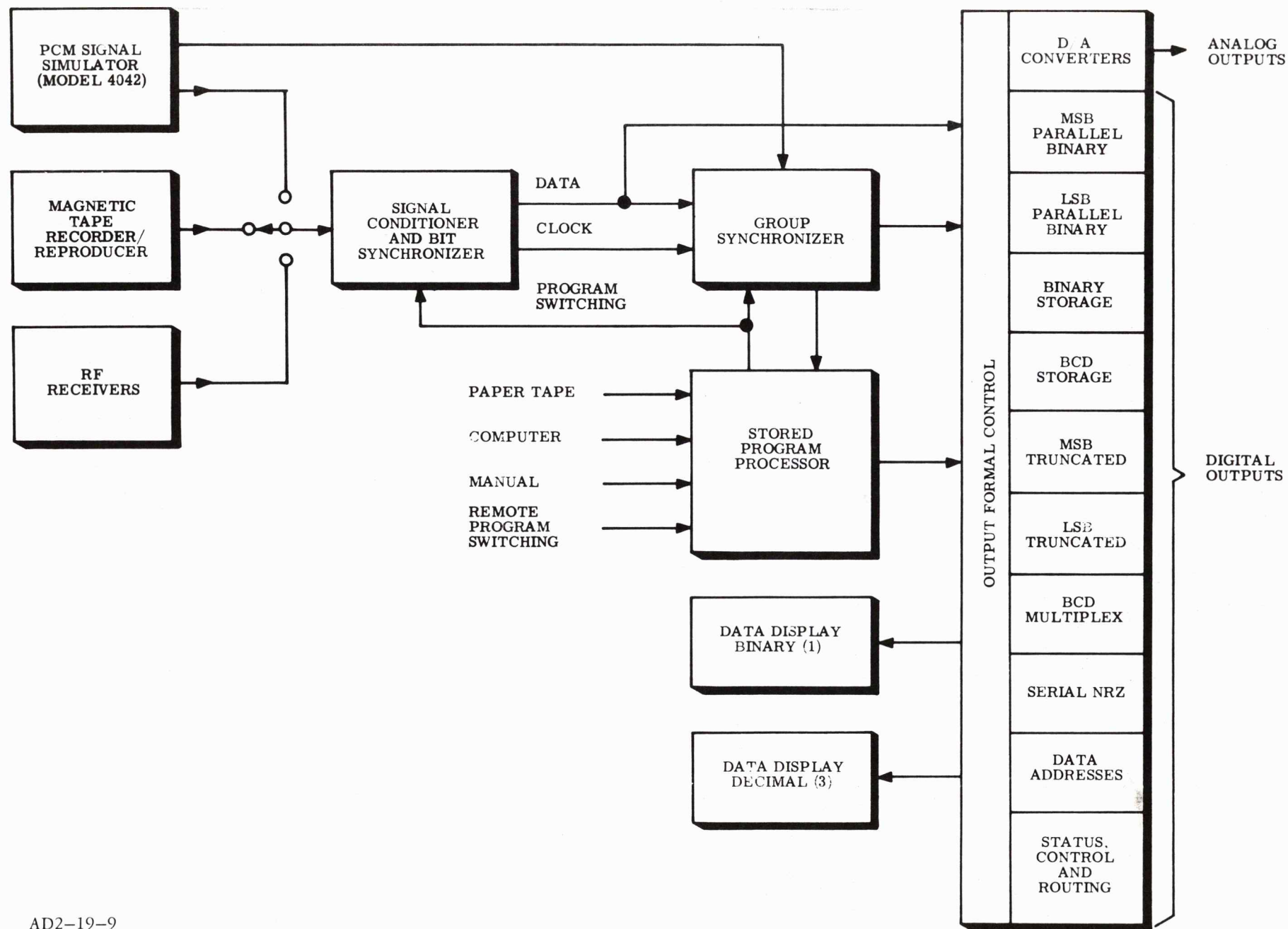
3-190. Figure 3-25 is a simplified block diagram of a decommutator. The equipment may accept serial inputs from either RF receivers, magnetic tape recorders, or a PCM signal simulator. Incoming data may be presented most significant bit (MSB) or least significant bit (LSB) first.

3-191. The signal conditioner restores and reconstructs the input signal when required. The signal conditioner also contains circuits that generate clock and timing signals that are synchronized with the input data rate.

3-192. The group synchronizer accepts the serial data and clock data from the signal conditioner and provides synchronization throughout the decommutator. Prime frame, subframe, and word synchronization as well as parity check capability, data flagging signals, and timing functions also are provided.

3-193. The stored program processor contains a random access core memory capable of storing 8192 words of 40 bits each. The memory provides storage for two selectable decommutation instruction formats (A and B). Either the A or B format can be any one of eight preprogrammed formats, or a format determined by front-panel control settings. Half of the memory capacity (4096 words) accommodates the A format while the other half stores the B program. Each program (both A and B) is divided into seven blocks, consisting of 512 words each. Each word contains 39 information bits plus a parity bit. The stored program processor accepts inputs from either a paper tape reader, the Central Computer Group, or through manual entry by means of front panel settings.

3-194. The output format control unit receives serial reconstructed data from the signal conditioner, timing signals from the group synchronizer, and program control instructions from the stored program processor. The output format control unit provides analog and digital outputs, as well as status, control, and routing information to the external ancillary



AD2-19-9

Figure 3-25. Digital Acquisition and Decommulation System Block Diagram

devices. Parallel binary and binary coded decimal (BCD) data are also provided to data displays on the decommutator control panel.

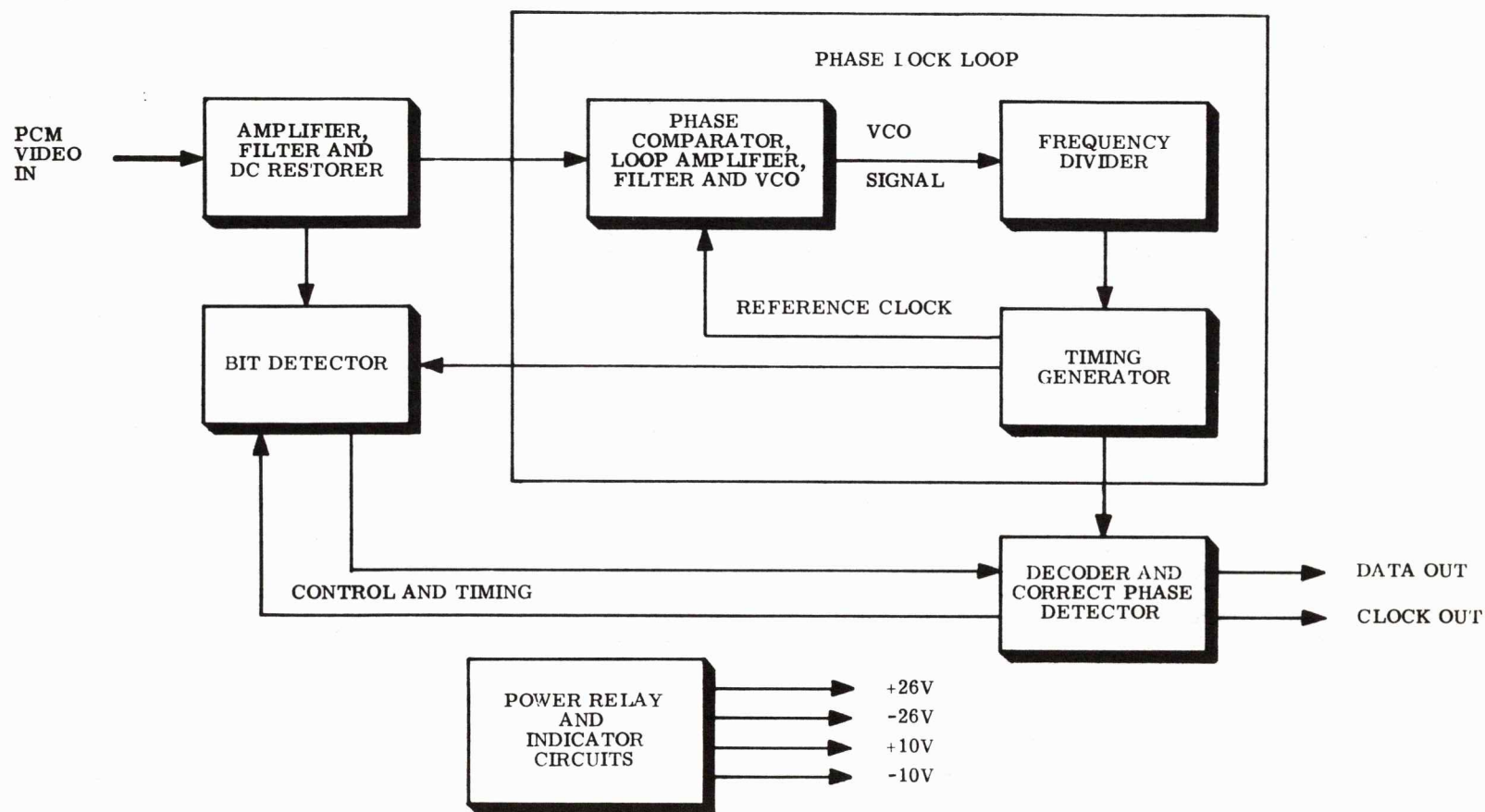
3-195. The PCM signal simulator is capable of providing a wide range of PCM data and synchronization signals that are used for checkout, calibration, and evaluation of the decommutator. The simulator also is capable of simulating a weak or bad incoming signal, at the discretion of the operator, by inserting jitter voltage and noise into the signal.

3-196. SIGNAL CONDITIONER. The signal conditioner (figure 3-26) consists of three principal circuits: (1) a d-c restorer, (2) a bit synchronizer (phase lock loop), and (3) a bit detector. The bit synchronizer outputs are: (1) a clock signal at the bit rate of the input data, and (2) various timing signals and gates used throughout the decommutator.

3-197. The d-c restorer receives the PCM video signals via a front panel input attenuator which is adjusted to provide proper decommutation operation over the input voltage range. The PCM video is applied through an input amplifier and filter, which provides a stabilized signal amplitude, to a buffer amplifier which permits multiple distribution of the signal. The d-c restorer circuit adds a mixed positive and negative peak detection signal to the input attenuator, forming a feedback loop that causes a shift in the video signal level. The filtered video signal is level shifted to provide a symmetrical signal about ground (zero volts) potential.

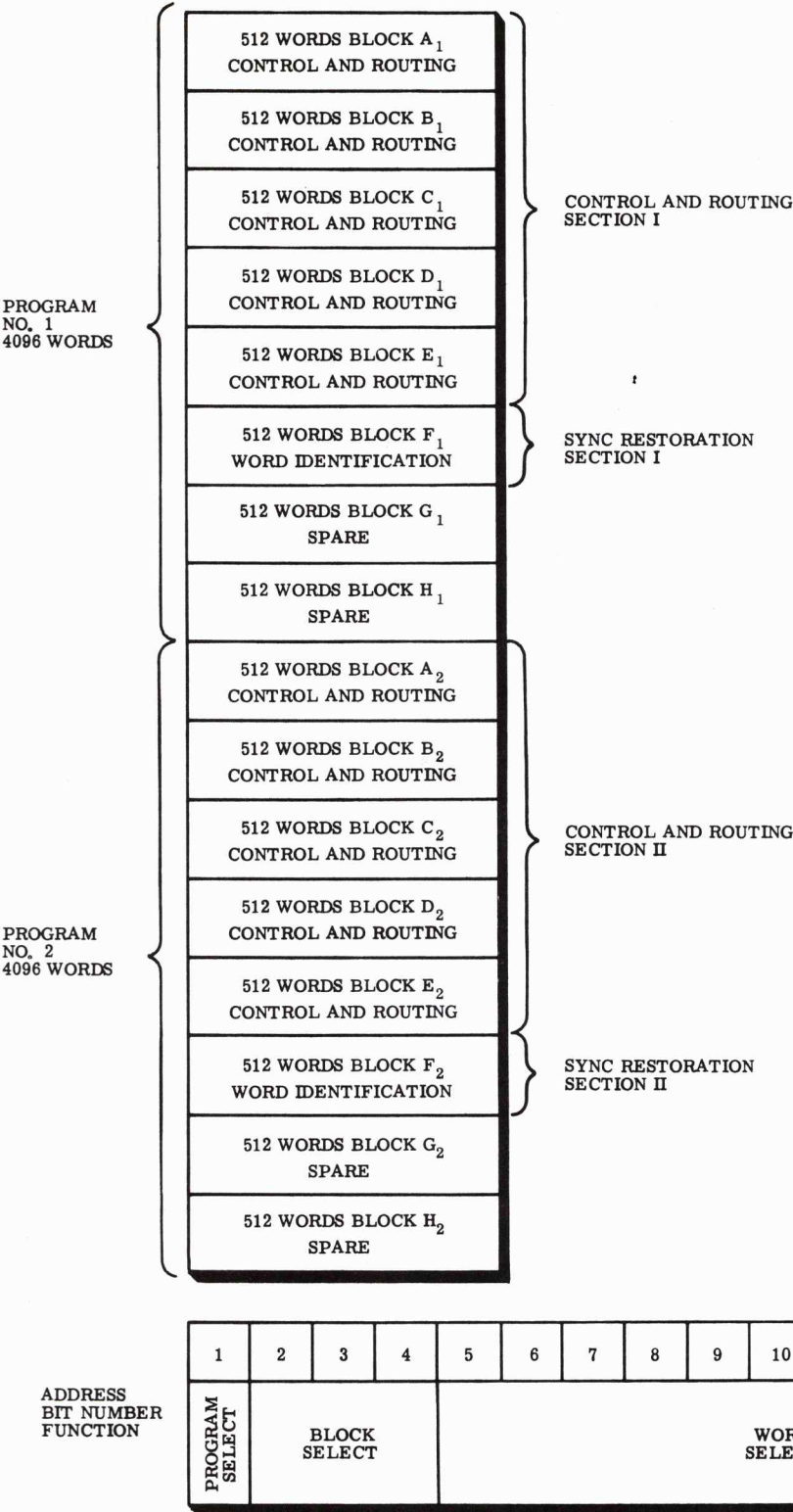
3-198. The bit synchronizer accepts the filtered and level restored signal from the buffer amplifier and applies it to a transition. The transition pulses, and internally generated reference clock pulses, are both applied to phase comparators that produce an output voltage which is proportional to the phase difference between the two signals. The phase error signal thus derived is applied as a control signal through a loop filter and loop amplifier to the VCO, which serves as the basic clock frequency source. The VCO output, in turn, is applied through a frequency divider to a function generator and gating circuit, which provide the reference clock signal to the phase comparator and control and timing signals to the bit detector. The bit detector receives the filtered and level restored video from the buffer amplifier and the clock and gating pulses from the bit synchronizer. Integrator circuits sense the polarity of the PCM video; a decision amplifier makes a polarity decision each bit interval and provides a reconstructed NRZC modulation data output.

3-199. STORED PROGRAM PROCESSOR. The stored program processor consists of the random access core memory and the associated circuits required to read data from and write data into the memory. The 8192-word memory is divided in half (4096 words each) so as to store two programs (A and B). Figure 3-27 illustrates how the memory storage capacity has been allocated to both programs. Each program is divided into blocks capable of storing 512 words of 40 bits each. The first five blocks of each program contain control and



AD2-15-9

Figure 3-26. Signal Conditioner Block Diagram



AD2-16-9

Figure 3-27. Memory Organization and Coding

routing instructions, the sixth block in each program contains sync code information which enables the group synchronizer to restore sync in the event it is momentarily lost. Figure 3-27 also illustrates the memory address word bits. The first bit selects either the A or B program, the next three bits select the appropriate block within a program, and the remaining nine bits select a particular 40-bit word within the block.

3-200. A program may be entered into memory from either the computer or a tape reader. A program also can be manually entered from the decommutator program control panel. Figure 3-28 is a simplified block diagram of the stored program processor. When a program is entered into memory from the computer, the bits are loaded, 12 at a time, into the formatting gates. The load control, and the format counter and decoder circuits enable the memory word to be routed from the formatting gates through the load data register and the master load gates to the memory register. This is accomplished each time 39 bits have been stored in the formatting gates. During the interval the word is in the memory register a parity check is accomplished, and a parity bit (40th bit) is inserted as necessary.

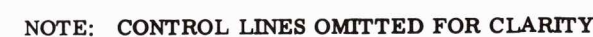
3-201. The memory register loads the core memory sequentially. When a new program is to be entered or the memory is being loaded for the first time, the memory register starts to load in the first word location of the first block. The memory register continues to load the first block until 512 words have been stored, at which time the words are sequentially stored in the second block. The process is continued until the complete program has been stored in memory.

3-202. When a tape reader is used as the loading device, the sequence is similar to that described above, except that the tape reader forwards data to the formatting gates six bits at a time. Every seventh word on the tape is a three-bit word, thus enabling the formatting gates to build up the 39-bit memory word.

3-203. When instruction words are entered manually from the decommutator program control panel, the data is entered directly to the formatting gates, bypassing the input circuits.

3-204. Decommutation of input data (PCM video) may be started after at least one complete program has been entered into memory. The second program may be entered into memory while the decommutator is operating from the first program.

3-205. Figure 3-29 illustrates a 40-bit instruction word. The various groupings of bits are called syllables: each performing a specific function. Each instruction word read out of memory is parity checked by the parity generator and checker circuit. The parity bit slot of the instruction word may contain either a binary 1 or 0. The determination as to what the parity bit slot should correctly display is dependent upon whether an odd or even number of



3-75/3-76

SYLLABLE NUMBER		10			9			8						7	6		5	4
BIT NUMBER	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22
FUNCTION	PARITY	NEXT BLOCK 3 BITS			BLOCK JUMP 3 BITS			WORD LENGTH 6 BITS						ID	SYNC AND RECYCLE 2 BITS		CHANNEL STRIP	ON-OFF DUMP

3				2						1											
21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIN/BCD STORAGE 4 BITS				SPARE 6 BITS						DISPLAY ADDRESS 12 BITS											

AD2-18-9

Figure 3-29. Memory Word Program Control and Routing Instruction Format

binary 1's are contained within the body of the instruction word. When a parity error is detected, red indicators light on the decommutator display panel.

3-206. The memory must remain one word ahead of the incoming PCM video data in order to exercise control over the decommutation process. Syllables nine and ten of the instruction word enable the stored program processor to read instruction words from memory in a timely fashion, thus permitting the decommutator to process and route the incoming PCM video to which the instruction word applies.

3-207. Syllable ten contains the address of the next block in memory to be accessed. The three binary bits in this syllable correspond to a particular memory block. This code is routed from the memory register through the auxiliary register, and the block decoder to the unload control and decoder circuit. When sync is acquired by the group synchronizer and sync pulses are applied to the unload control and decoder circuit, a pulse is sent to the counter for the particular block corresponding to the syllable ten code. The appropriate counter (A, B, C, D, or E) accesses the memory address corresponding to the count in the counter, and the counter is stepped to the next higher number. The instruction word in that memory location is read out into the memory register and the sequence is repeated throughout the decommutation process.

3-208. Syllable nine consists of three bits, the most significant of which indicates whether a block jump is to be executed; the remaining two bits indicate which memory block to go to. The syllable bits are decoded by the block jump entry gates and the block jump address decoder and are stored in the block jump store circuit. Whenever a subsequent instruction word calls out this stored address in the next block address (syllable ten), the location is not accessed because of the previously stored block jump instruction. The second time that location is specified by an instruction word, however, it will be accessed and the word read out again since the block jump store circuit has been previously cleared.

3-209. Syllable eight provides the group synchronizer with information concerning the number of bits in the incoming PCM video data word. This syllable is gated through the memory register, an AND gate, and the word length register to the group synchronizer where it is used to derive the word rate signal. The word rate signal is one of the signals required to address the next instruction word from memory (applied as an input to the unload control and decoder). Thus, it can only be generated by the group synchronizer after the length of the incoming PCM video data word is known. The memory must always furnish the length of the word (syllable eight) to the group synchronizer before the actual PCM video word is received, thereby requiring that the memory remain one instruction word ahead of the incoming data.

3-210. Syllable seven of the instruction word designates whether the incoming data word contains a subframe ID sync code word. Syllable six assists the group synchronizer to reacquire the sync code in the event it is lost during transmission, and also to recycle information for the stored program processor. Syllable six is gated through the auxiliary register and applied to the sync and recycle decoder, where it may be used, as required, by the group synchronizer to reacquire sync. This syllable is also applied to the identification set gates where it is retained for reidentification of the instruction word.

3-211. Syllable five of the instruction word indicates whether the associated incoming data word is to be decommutated or discarded. Syllable four designates that four bits of the associated incoming data word be dumped to the digital store of on-off bits.

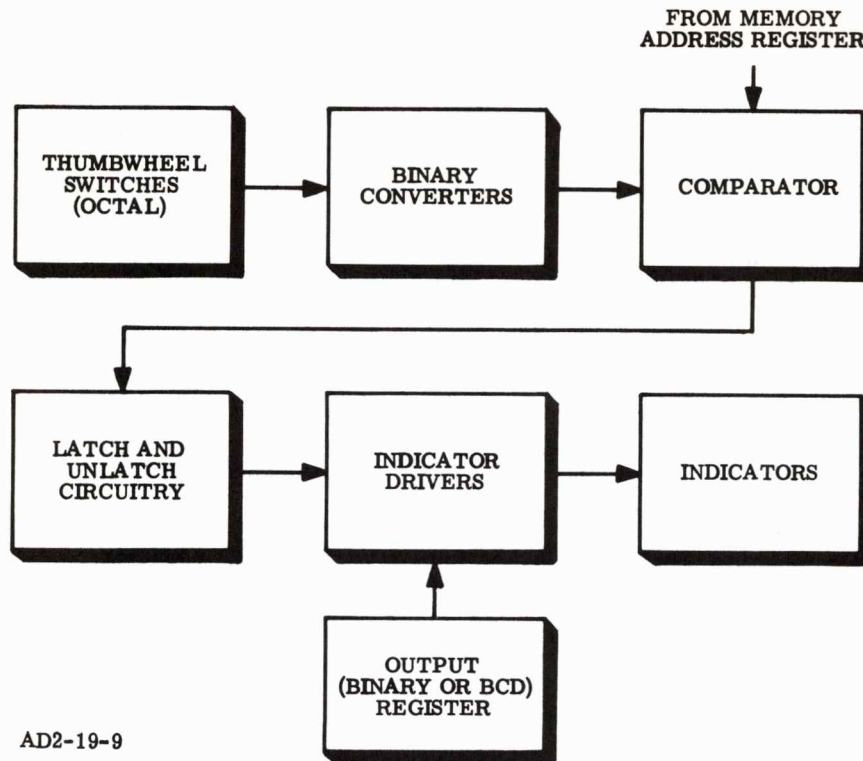
3-212. Syllable three indicates the address of the binary or BCD storage register that is to accept the input data. Syllable two contains six spare bits that may be used as required for future memory control. Syllable one identifies the output device that is to receive the processed input data.

3-213. GROUP SYNCHRONIZER. The group synchronizer maintains three modes of operation: Search Mode, Check Mode, and Lock Mode. During Search Mode, the group synchronizer samples data in an effort to acquire the sync code. The Check Mode permits the group synchronizer to check the acquired sync code several times to insure that it is really correct. The Lock Mode is in effect the normal operating mode, in which the sync code and its time slot (word position within the prime frame) have been definitely established.

3-214. The group synchronizer achieves prime-frame synchronization. Serial data and the bit-rate signal are applied to a serial-to-parallel converter. As the data enters each stage of the serial-to-parallel converter, each bit of the incoming data is compared with the programmed prime-frame sync code until a favorable comparison results. After 15 bits of the data agree, a prime-frame sync pulse is generated. After prime-frame sync has been initially established, the group synchronizer then tests the sync only at intervals instead of all the time.

3-215. When word sync bits are required by the program, they are processed in a manner closely related to that used for prime-frame sync. Word sync bits must be blanked from the rest of the data word, however, so that they are not processed with data.

3-216. DECIMAL AND BINARY DISPLAYS. Both the decimal and binary displays permit visual observation of a given word of incoming data. There are three decimal and one binary, front-panel-mounted, displays. Although each category of display processes and displays different information, both the binary and the decimal displays function similarly. Figure 3-30 is a simplified block diagram of the binary and decimal display circuits.



AD2-19-9

Figure 3-30. BCD and Binary Display Simplified Block Diagram

3-217. In order to observe a special word, the octal equivalent of the word's decimal location within the program is entered on front panel thumbwheel switches. The octal location code is converted to binary and applied to a comparator circuit. The comparator also receives a next word address input from the address register in the stored program processor. During the time interval of the input data word immediately preceding the word that has been chosen for display, the two comparator inputs are in coincidence, and the comparator circuit gates the latch and unlatch circuit. The latch and unlatch circuit clears the indicator drivers of any previous display and enables the input data word that follows to be displayed.

3-218. DIGITAL-TO-ANALOG CONVERTERS. The digital-to-analog (D/A) converters provide signals to any output device requiring, for its input, an analog voltage. Figure 3-31 is a simplified block diagram of the D/A converter circuits. The decommutator contains 60 D/A converters. The stored program (A or B) provides instructions concerning when a D/A converter is to be selected. The memory supplies the six-bit address of a specific converter to the load gates. These six bits are the code which designate which of the 60 D/A converters will be activated for the input data word and are shifted from the load gates to the D/A address storage. The six-bit code activates a unique combination of one "X" gate

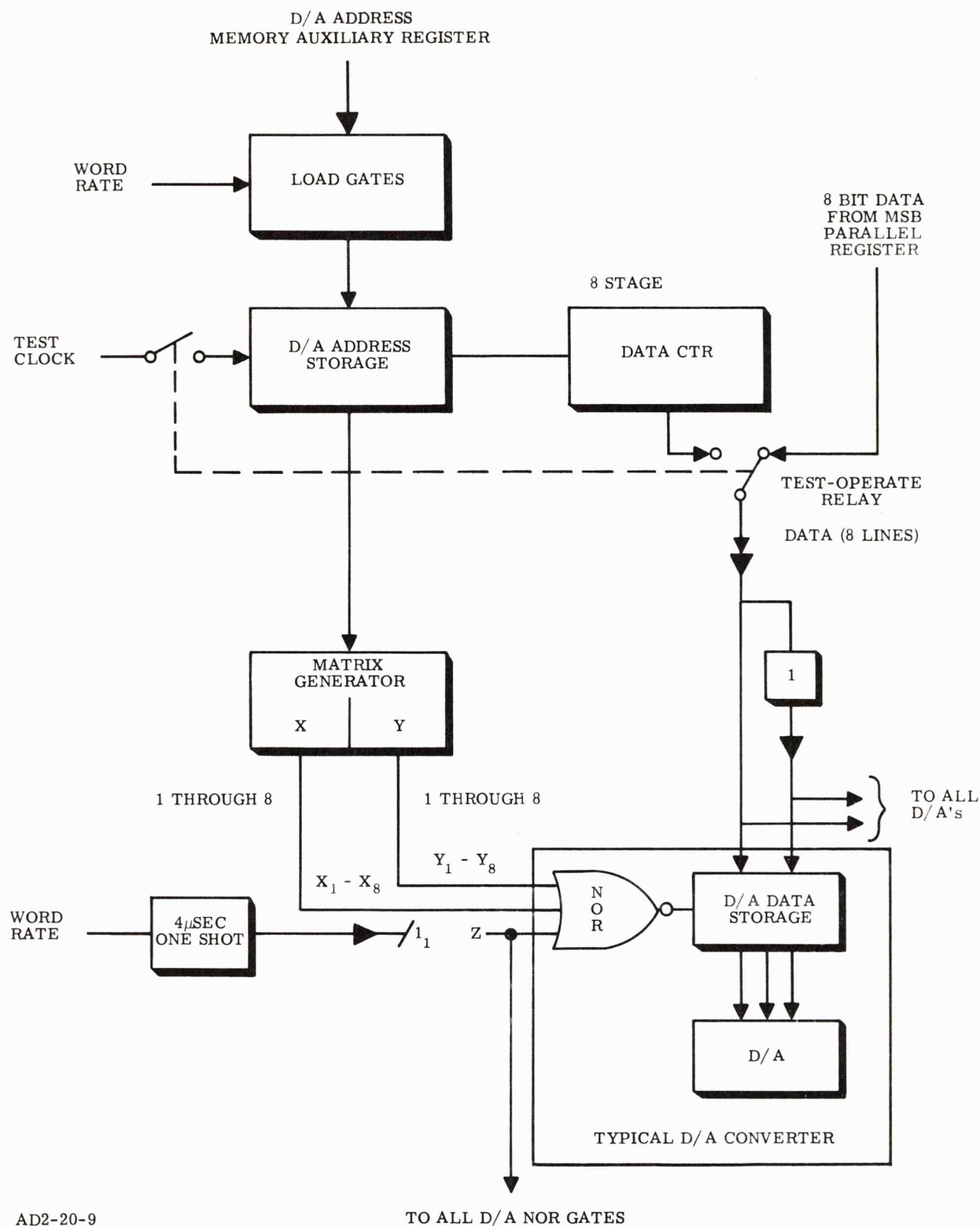


Figure 3-31. Digital-to-Analog Conversion Simplified Block Diagram

and one "Y" gate within the matrix generator. Because there are eight "X" gates and eight "Y" gates, it is possible to have 64 different output combinations. Sixty of these output combinations are associated with a particular D/A converter. A word sync pulse extracted from the end of every data word is applied to a one-shot multivibrator whose output is a 4-micro-second pulse. This pulse is applied to a power inverter and then two complementary drivers. The resulting pulse is designated as "Z." The "Z" pulse is applied to each D/A select NOR gate. With the three control signals generated, the incoming digital data may be gated into the selected D/A storage register.

3-219. Each D/A converter processes only the eight MSB's of the incoming data word. The eight MSB bits of every data word are shifted, in parallel, out of the MSB parallel register. The bits are applied to eight steer set drivers which in turn apply the data to the selected D/A converter. The output of each D/A is sent to the output jack.

3-220. A test circuit is included as part of the D/A converter circuitry. This is energized by placing the OPERATE/TEST switch to the TEST position which switches the MSB parallel register inputs to a data counter that causes the D/A address register to act as a counter. This causes the "X-Y" matrix to generate each of the 64 output combinations. Each time the D/A address counter cycles to every D/A converter, the data counter is advanced one step. This allows all 60 of the D/A converters to be cycled to every analog level represented by the digital data word.

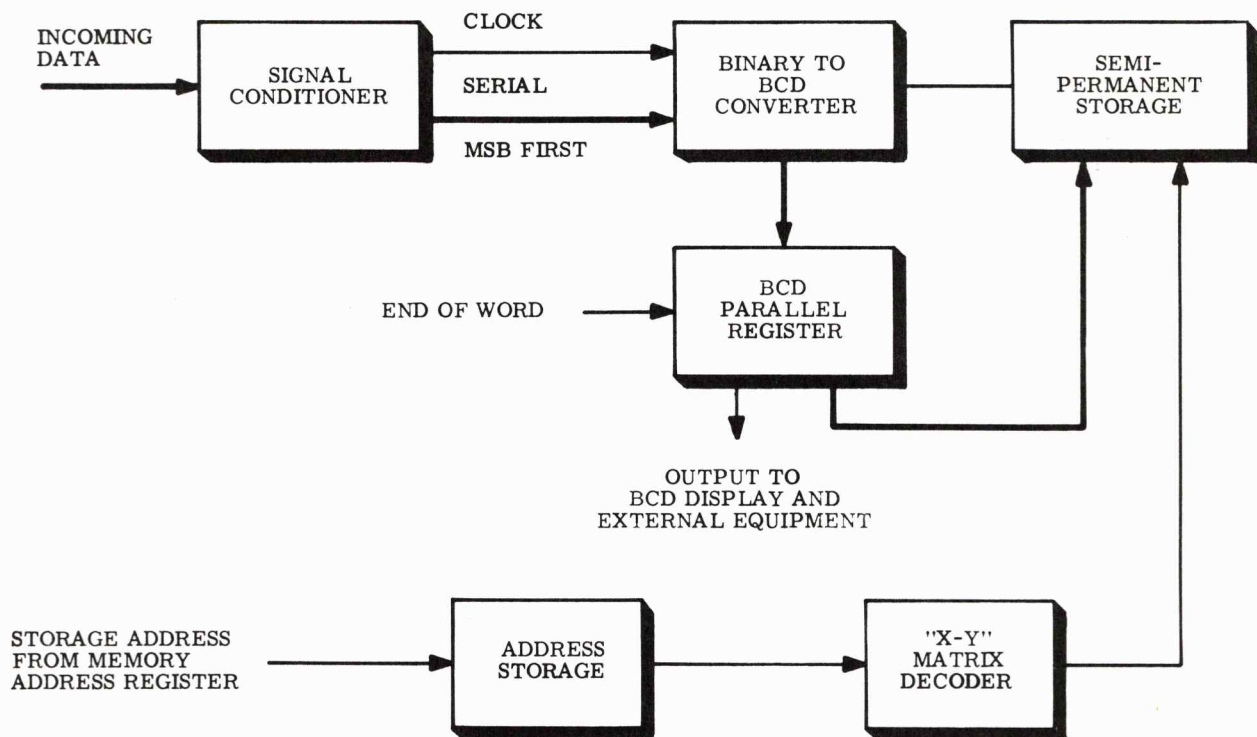
3-221. BINARY-TO-BINARY CODED-DECIMAL CONVERTERS. The binary-to-binary coded-decimal (BCD) converters accept serial binary data words MSB first and convert them to their equivalent BCD numbers. The converted data is used for display purposes as well as outputs to ancillary equipment. Figure 3-32 is a functional block diagram of the binary-to-BCD converter.

3-222. The incoming binary data is routed directly from the signal conditioner to the binary-to-BCD converter. The data must be presented MSB first and in serial form. The binary-to-BCD converter is, in effect, a series of translator decades - the output of each translator decade driving the next. Each translator decade is weighted by a multiplication factor - this factor is of the form of powers of ten. The decimal equivalent number is available at the input of the BCD parallel registers at the end of the same word time.

3-223. At the end of each word, a load pulse is sent to the storage register, causing it to accept the decimal digit while at the same time a reset pulse is applied to the converters resetting them to zero.

3-224. Each binary-to-BCD converter has a storage register associated with it which stores the decimal equivalent and provides the driving power needed to route the number to three

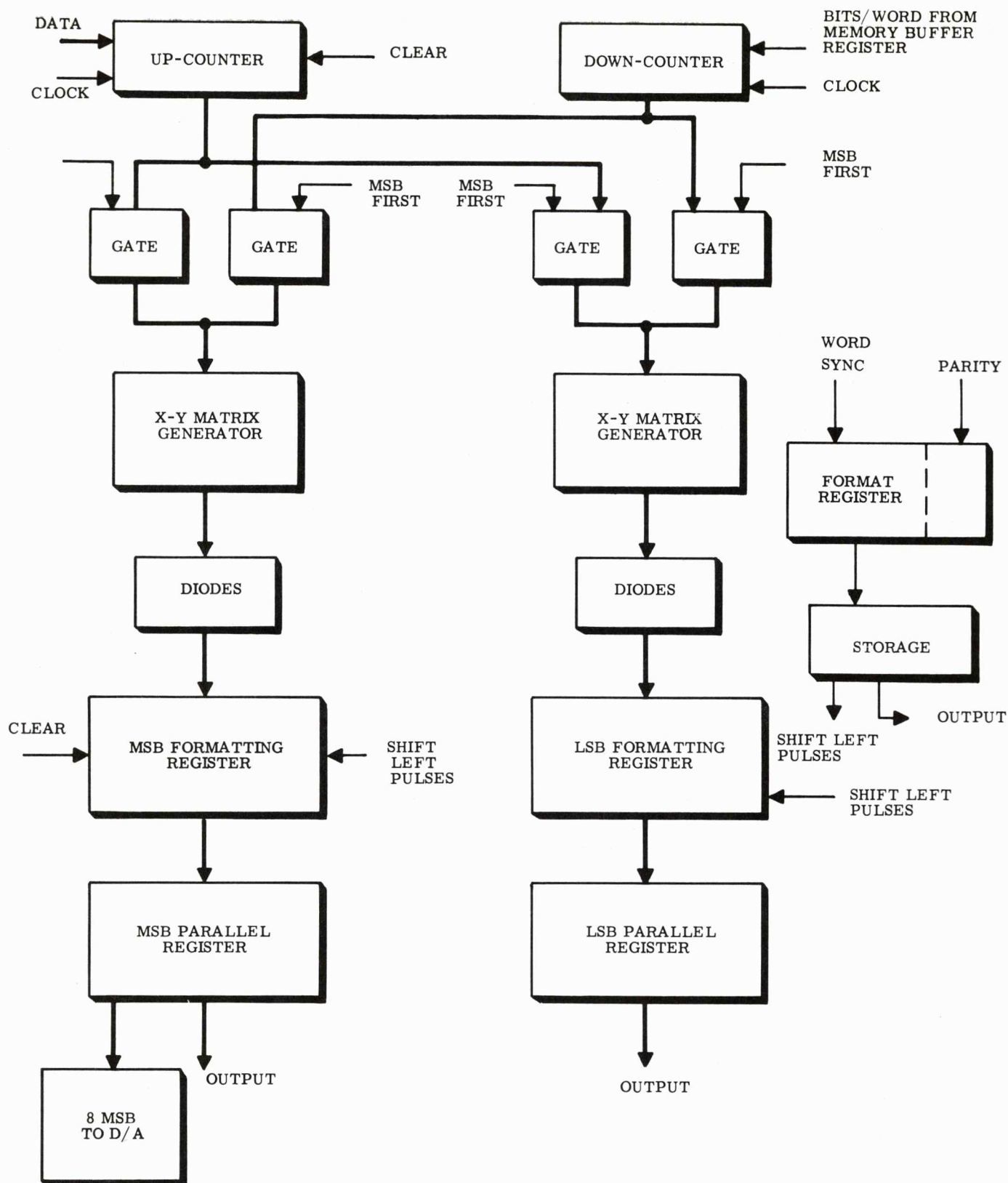
different destinations simultaneously. The three destinations are: the BCD parallel output register, the decimal display panel, and the BCD storage register. These storage registers hold the number until instructed by memory to route it to a certain location. The address of the storage register that is to be used to hold the number is contained in the memory buffer register. This address is applied to the address storage register which routes it to an "X-Y" decoding matrix. The corresponding "X-Y" pulses are generated to gate the BCD information from the BCD parallel register into the selected storage register.



AD2-21-9

Figure 3-32. Binary-to-BCD Converter Simplified Block Diagram

3-225. MSB AND LSB PARALLEL REGISTERS. The function of this logic group is to provide a given word output to any external equipment, either MSB or LSB first. The data word may be from 4 to 64 bits long. The different conditions under which the registers can accept data are: (1) no parity or word synchronization bits in the data word, and either MSB or LSB first and (2) parity and word synchronization bits present in the data word either at the beginning or at the end of the word, and either MSB or LSB first. Figure 3-33 illustrates the associated circuitry in block diagram form.



AD2-22-9

Figure 3-33. MSB and LSB Parallel Registers Simplified Block Diagram

3-226. No Parity or Word Synchronization Bits - MSB First. When the first bit comes in, a pulse indicating that the word is starting is received. This pulse is applied to an up-counter where a constant count of the bits in the word is maintained. The output of this counter is applied to crossover gates and ANDed with the incoming data. In this condition, the only time that data is gated is when that particular bit is a binary 1. Because the MSB formatting register has previously had all its stages preset to binary 0, there is no need to gate the data zeros through. The data is applied to the binary-to-unitary converter, which consists of an "X-Y" matrix and 17 diodes. The "X-Y" position of each bit of the data is decoded and applied to the set side of a corresponding stage in the MSB formatting register. As the up-counter continues to count, the data is set sequentially into the MSB formatting register, loading only the data that is a binary 1. At the end of the word, a pulse from the word synchronizer causes the data to be shifted into the MSB parallel register in parallel fashion. A control pulse also clears the counter to zero and clears all stages of the MSB formatting register to zero. The MSB parallel register provides the data as outputs to any external device plus supplying the eight MSB of the data through eight power inverters to the D/A converters where they may be converted to an equivalent analog voltage.

3-227. Converting Word to LSB First. In this case, because the word length is known, the memory buffer register must send a code corresponding to the number of bits in the word. Assume there are 30 bits in a particular data word. Memory sends the binary number equivalent to the number 30, which is used to force the down-counter to the count of 30. With each successive clock pulse, the counter counts down sequentially until arriving at zero. The data still enters MSB first; however, the counter, being set at 30, places the first bit (MSB) into position 30 of the LSB formatting register. Each clock pulse counts the counter down by one, and if the data is a "ONE" it is gated through. The "X-Y" matrix, decoding the count, places the bit in the LSB formatting register in the position corresponding to that count on the down-counter. The internal circuitry is the same for the LSB formatting register as is used for the MSB formatting register, except that the MSB counts up while the LSB counts down.

3-228. At the end of the word, the word synchronizer sends a pulse which causes the data to be shifted into the LSB parallel register where it is provided as an output to any of the external devices and to the binary displays. A control pulse then clears the LSB formatting register and the down-counter to zero.

3-229. No Parity and Word Synchronization Bits - LSB First. If a word is received initially as LSB first data, then a crossover situation must take place. The incoming data as it comes through the up-counter must be gated to the LSB formatting register. Since the up-counter is ready to count at the first bit time, the first bit (LSB) is gated into position one in the LSB

formatting register. As the up-counter continues to count, the "X-Y" matrix insures that the bits are placed in their relative position.

3-230. If it is desired to make the word available at MSB data, then the down-counter must be set to the number of bits in the word and the counter output applied, through the crossover gates to the MSB formatting register in this case. With the exception of the crossover requirement, all other circuitry functions exactly the same as previously discussed.

3-231. Parity and Word Synchronization Bits Present - MSB First. When there are parity and/or word sync bits (control bits) present as a portion of the data word, the number of control bits must be counted, and they must be identified so that they can be routed to display panels or external equipment when required. When a prity bit and/or word sync bits are present, the word synchronizer sends two levels to the output unit that lasts for as long as there are control bit times. These control bits must not be confused as being data. The levels are ORed together in the output unit and applied to a counter. The output of the OR gate also is used to blank the up-counter so that it will not count during the time the control pulses are present. This insures that the control pulses and data do not get into the formatting register that the up-counter is controlling.

3-232. As the word comes in, in MSB first form, with the parity and sync bits in the first positions, the blanking pulse from the word synchronizer is applied to the counter, preventing it from counting. When the bits are past, the counter still is at position one, ready to gate the first data bit into position one of the MSB parallel register. From here on the circuitry functions in the same manner as previously discussed. Of course, if the sync and parity bits are at the end of the word, the same blanking pulse will not allow them to be gated through. If parity appears at the first of the word and word sync at the end, the same situation will hold true.

3-233. Parity and Word Synchronization Bits Present - LSB First. The same operation takes place if the initial data enters as LSB first data. The up-counter is blanked for the period that the control bits are present. The only difference is the crossover operation where the data is gated into the LSB formatting register as previously discussed.

3-234. If it is desired to make the MSB first word available as LSB first data, the count and position of the parity and word sync controls bits must be accounted for. The down-counter must be set to the number of bits in the word from the memory buffer register; however, this count now includes the data as well as the control bits. Assume the first example presented if a count of 30 bits has a parity bit and three word sync bits in it. Now the memory buffer register must send a binary number equivalent of 34, which is used to force the down-counter to the count of 34. The same operation takes place as in the initial data word discussed: the

first bit of the word being gated into position 34 of the LSB formatting register. With each clock pulse, the counter counts down and the bits are gated into their relative location. When the counter reaches zero, the data and control bits are now in the LSB formatting register with the control bits in the first four LSB positions of the register. These bits must be separated from the data word.

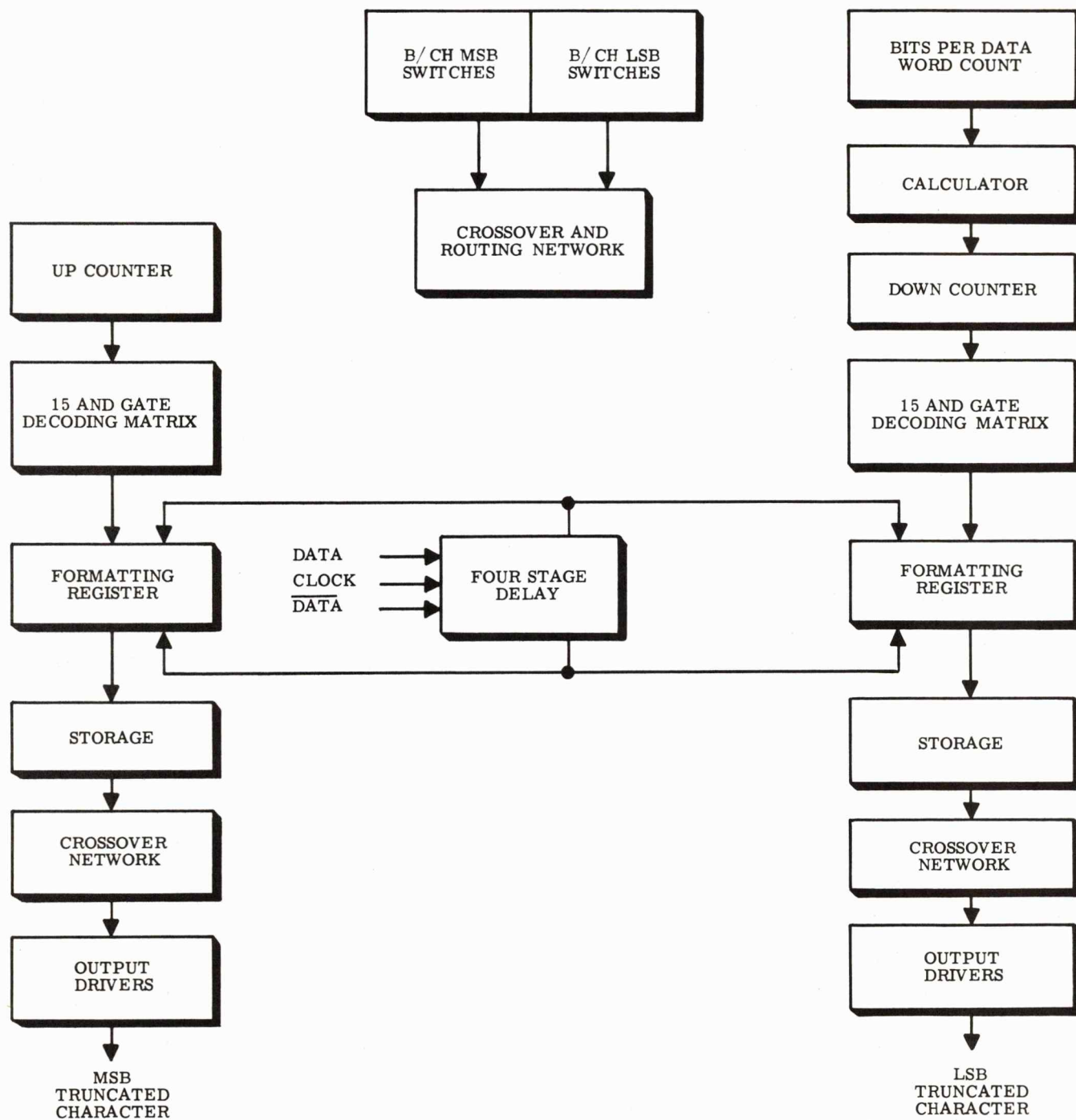
3-235. The storage register, where the count of the number of control bits was retained, now is used to generate shifting pulses. In this particular example, four pulses are applied to the LSB formatting register, causing the entire word to shift left four bit times. Hence the control bits are shifted out and the LSB of the data word is in position one in the LSB formatting register.

3-236. MSB AND LSB TRUNCATED CHARACTERS. The purpose of this group of logic is to truncate or break up each data word into smaller characters. These characters must be available in both MSB first and MSB first (LSB first) form for both MSB first and LSB first data. Figure 3-34 is a block diagram of the character truncation circuitry.

3-237. The bits per character are established by setting up the count on the switch panel located inside the 4A3 module panel. The switch settings are applied to a crossover network composed of four diode gates for each group of switches. The determination as to whether the data is MSB first or LSB first is a function of the program and is known before starting the decommutation process. A -10-volt level identifies MSB first data while a 0-volt level identifies LSB first data. If the data is MSB first, the MSB truncated character switch settings control the up-counter while the LSB truncated character switch settings control the calculator and the down-counter. If the data is LSB first data, the LSB truncated character switch settings control the up-counter while the MSB truncated character switch settings control the calculator and down-counter.

3-238. The logic decisions and steps necessary to form the two truncated characters are listed in table 3-6. The two columns of the table occur simultaneously; however, they are completely independent of each other. Because the calculator must perform a subtraction operation which may take up to four bit times to complete, the data word is delayed four bit times before being applied to the formatting registers.

3-239. Figure 3-34 shows an MSB first data word of 25 bits truncated into MSB first and LSB first characters. The MSB truncated character switches are set for seven bits per character while the LSB truncated character switches are set for 11 bits per character. The output from the MSB truncated character register forms three complete seven-bit characters and one four-bit (last three bits are zeros) character from the 25-bit data word. The output from the LSB truncated character register forms the first character, which is the final



AD2-23-9

Figure 3-34. MSB and LSB Truncated Character Formation
Simplified Block Diagram

remainder obtained by subtracting 11 from 25 until the remainder is less than the character switch settings. In the example shown, the first character contains three data bits and the rest of the character is completed with zeros. The remaining two characters are full 11-bit characters.

Table 3-6. Steps in Forming Truncated Characters

STEP	LSB TRUNCATED CHARACTER	MSB TRUNCATED CHARACTER
A	Determine whether data word is MSB first or LSB first. A -10-volt level means MSB first; a 0-volt level means LSB first.	Determine whether data word is MSB first or LSB first. A -10-volt level means MSB first; a 0-volt level means LSB first.
B	Set truncated character switches to desired number of bits per character - four to fifteen bits.	Set truncated character switches to desired number of bits per character - four to fifteen bits.
C	Count of bits per incoming data word sent from stored program processor.	Start up-counter at count of 1. Count up until count agrees with switch settings in B.
D	Calculator subtracts B from C. If C is still larger than B, C is shifted right one place and subtraction performed again.	Apply character formed by C to output crossover network. Level of identifying signal determines whether character is crossed over.
E	Set down-counter with final remainder when it is less than bits per truncated character count (B above).	Reset up-counter to 1, form second character as in C.
F	Form first character from this count. Difference between this count and count established in B is filled with zeros.	Repeat D and E until data word is completely truncated. Last bits of last character are zeros if data word does not completely fill character.
G	Apply character to output crossover network. Level of identifying signal determines whether character is crossed over.	Next data word starts at C because A and B are constant for a given program.
H	Set down-counter with count established in B above. Form next character from this count.	
I	Repeat G and H until data word is completely truncated.	
J	Next data word normally starts at C because A and B are constant for a given program.	

3-240. BINARY STORAGE REGISTERS. The binary stores provide semipermanent storage for five 33-bit data words. The program determines which data words are placed in the binary storage register. The purpose of the registers is to allow quick access to these selected words. Figure 3-35 is a block diagram of the binary storage registers.

3-241. The memory auxiliary register sends the address of the register that is to store the next incoming data word to the address decoder, which decodes addresses for both the binary storage registers and the BCD stores. The binary codes used to address the five binary storage registers are listed below and are shown on the block diagram.

<u>BINARY CODE</u>	<u>DESIGNATION</u>
0000	No storage necessary
0111	Binary Storage Register No. 1
1000	Binary Storage Register No. 2
1001	Binary Storage Register No. 3
1010	Binary Storage Register No. 4
1011	Binary Storage Register No. 5

3-242. When an address corresponding to a binary storage register is decoded, a toggle pulse is applied to all 33 stages of that register simultaneously. The LSB parallel register applies the data word to all five registers in parallel. However, only the register addressed accepts the data word.

3-243. PCM SIGNAL SIMULATOR. The PCM signal simulator is capable of generating a wide range of simulated PCM data and synchronization signals. A single PCM signal simulator, located in Decommutator Unit 102, provides simulated signals for both decommutators and other equipment within the ACE-S/C system. Figure 3-36 is a simplified block diagram of the PCM signal simulator.

3-244. A VCO provides a simulated bit-rate signal. Jitter voltage may be introduced at the discretion of the operator by means of either a self-contained audio oscillator or an external modulation source. The output of the VCO is applied to a 21-stage bit-rate select counter, where the bit-rate signal may be varied by means of a front panel switch, which selects one of the 21 stages.

3-245. A FORMAT SELECT switch enables the selection of various bit-rate formats (NRZC, NRZM, NRZS, RZ, or SP) for visual display on the front panel. An additional counter stage is provided through which RZ and SP bit rates are routed. The bit-rate signal is applied through a BIT RATE switch to several inverter stages where the signal is shaped. The BIT RATE switch, when placed in the EXTERNAL position, permits the application of an external clock signal, thereby bypassing the previous circuitry.

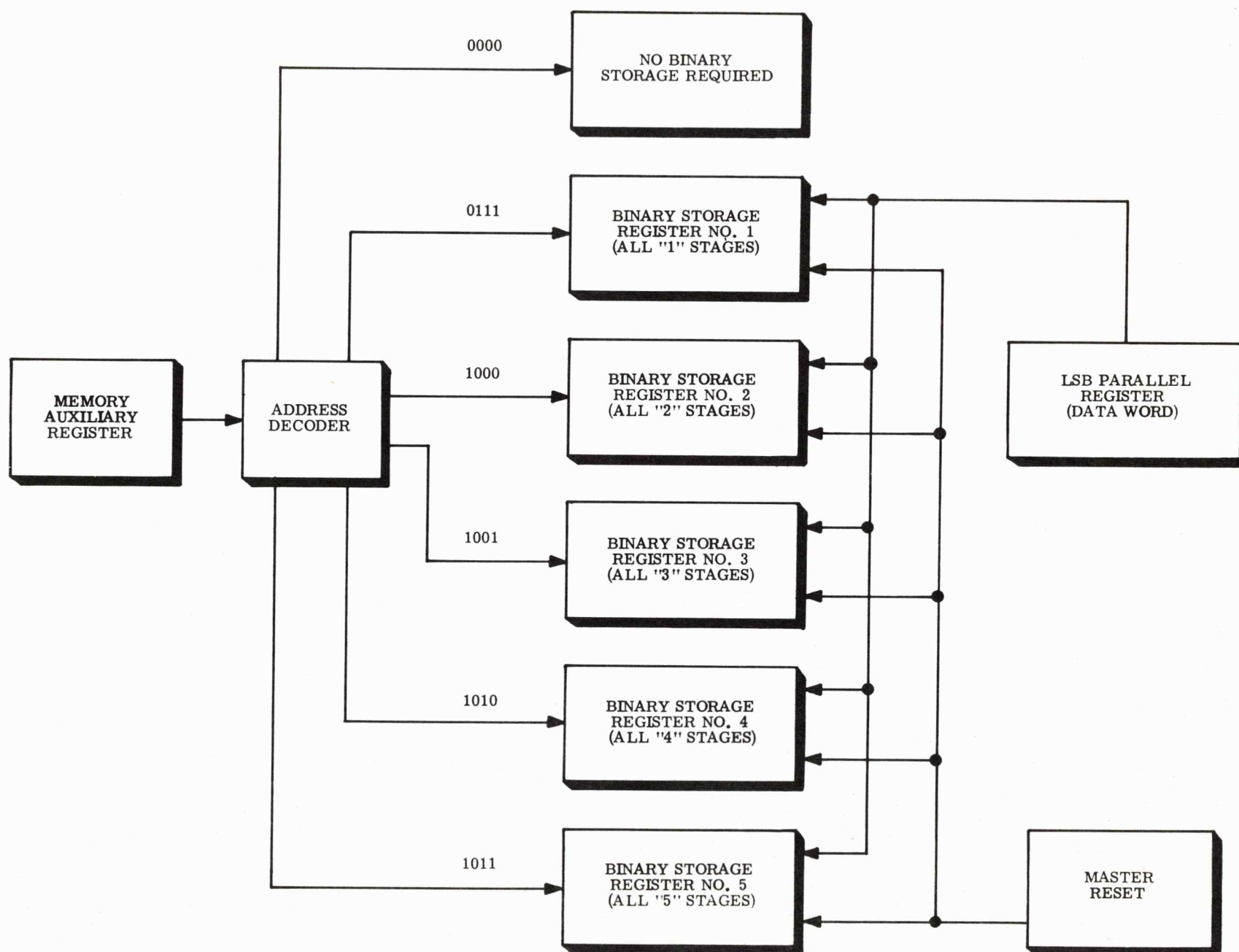


Figure 3-35. Binary Storage Registers Simplified Block Diagram

3-246. The bit-rate signal is available at both the bits per prime frame sync counter and at the bits per word counter AND gate inputs. Only one of the counters may accept the bit-rate signal, depending upon which of the input AND gates have been enabled by a controlling flip-flop. When the bits per prime frame sync counter has accepted a specific number of bits, predetermined by SELECT SWITCH settings, a reset gate clears the controlling flip-flop. The reset gate pulse also resets the bits per prime frame sync counter, and is ORed with the output of the bits per word counter. This OR gate output represents the word rate signal and is applied as an input to the words per prime frame counter. The word rate signal also enables a switch bank-controlled word to be generated and applied to a parallel-to-serial output register. A bit rate (BR) obtained from the output of the bit rate select counter through the inverters is used to clock out the data in serial form when it enters the register.

3-247. Upon reaching a preselected count in the words per prime frame counter, an associated reset gate generates a frame rate signal, which resets the counter, clears the gate controlling flip-flop and their associated counters, and is also applied to a flip-flop which controls the prime frames per major cycle counter. When the prime frames per major cycle counter reaches a preselected count, a reset gate pulse resets the counter and the associated flip-flop. The prime frames per major cycle counter, during the counting operation, senses preselected switch positions and identifies the following words within the major cycle and prime frame:

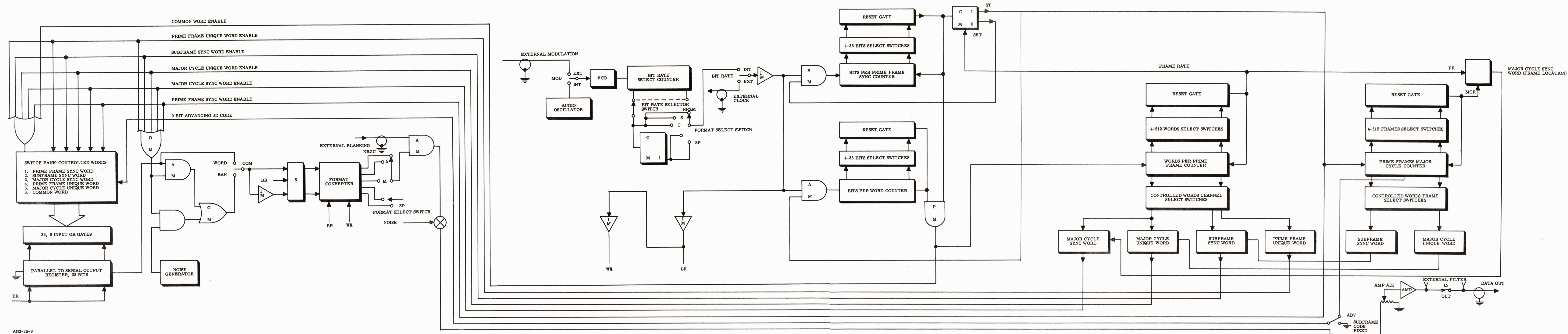
- a. Prime frame unique word.
- b. Major cycle unique word.
- c. Subframe sync word.

3-248. COMPUTER INTERFACE UNIT. The Computer Interface Unit shown in figure 3-37 is a simplified block diagram.

3-249. Inputs to the Computer Interface Unit are received from the computer and converted to standard logic levels by the input level converters. These converted signals then are fed to the code recognizer and to the input gates.

3-250. In a typical application, information is transferred to the decommutator when the computer sends Information Ready codes and signals and places the data on the input lines. Upon receipt of a "not busy" signal from the decommutator, the code recognizer and control transfers the data into the decommutator and sends an Output Resume signal to the computer.

3-251. Similarly, information is transferred from the decommutator to the computer when it sends coded request signals to the interface unit. Upon receipt of the "not busy" signal from the decommutator, the interface unit transfers the requested information to the computer. The interface unit continues to send data as long as the request signal is present.



AD2-25-9

Figure 3-36. PCM Signal Simulator
Simplified Block
Diagram

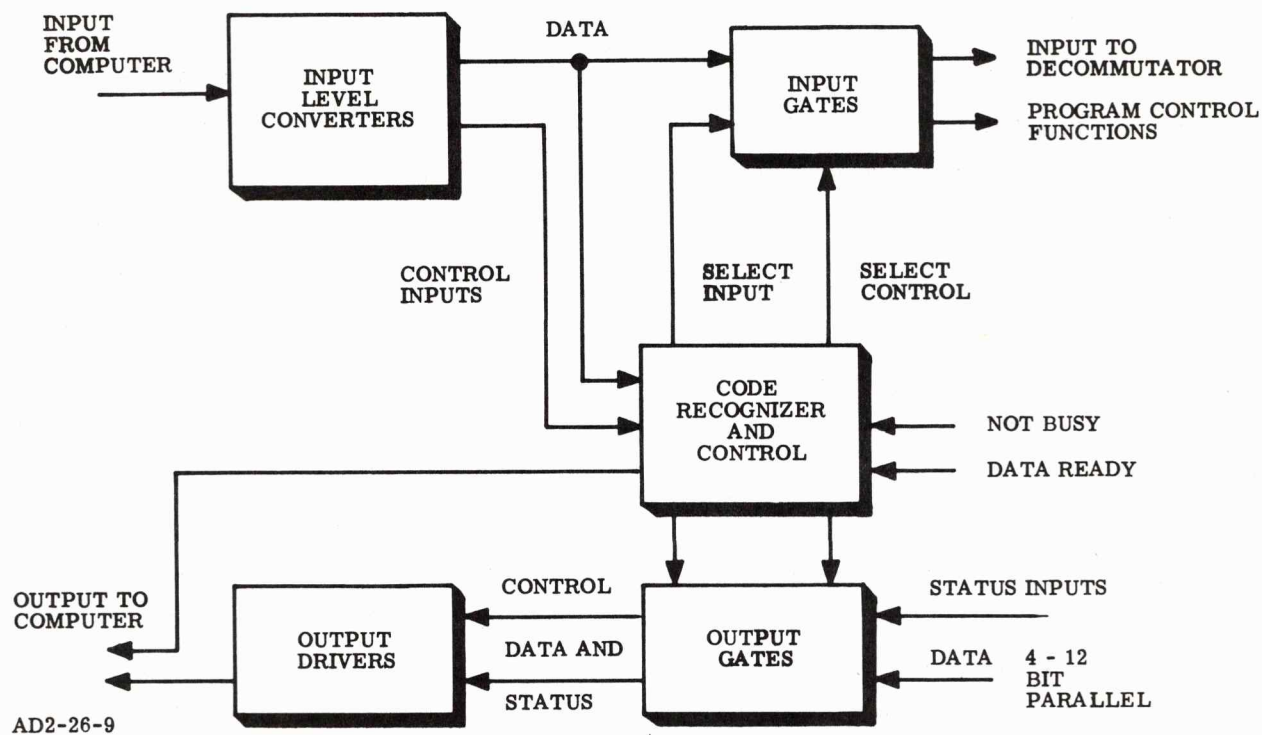


Figure 3-37. Decommulator/Computer Interface Simplified Block Diagram

3-252. The data input to the computer can begin immediately or at certain points in the PCM format.

PART 2

ANALOG AND EVENT DISPLAY EQUIPMENT

3-253. CONTROL ROOM TEST DATA DISPLAY AND RECORDING EQUIPMENT FUNCTIONS.

3-254. Units of the ACE-S/C system control room utilized to process, display, and record the addressed digital test data outputs of the decommutator units are shown in figure 3-38. The Decommulator Distribution Unit (DDU) receives addressed digital test data from both decommutators via transmission hardline connections (one line per bit). Fan-out amplifiers within the DDU distribute the received test data word to the ESDU and control consoles.

3-255. Within the ESDU, the test data event words are identified (by address recognition) and are routed to storage registers by the selection and arrangement of plug-in-logic modules. The outputs of the storage registers, representing on/off event functions, are distributed through a patch facility within the ESDU to predesignated control consoles. The control consoles route the incoming event signals, via a patch panel, to appropriate recording and/or display units (event indicators) mounted in the control consoles. Analog data words from the DDU are identified in a manner similar to that used for event data words and are stored by digital logic circuits contained within the control consoles. In this case the storage register outputs are fed to D/A converters. The resultant analog signals are routed, via a patch-board, to appropriate recording and/or display units (meter modules) mounted in the control consoles.

3-256. DECOMMUTATOR DISTRIBUTION UNIT.

3-257. DECOMMUTATOR DISTRIBUTION UNIT FUNCTIONS.

3-258. The DDU simultaneously receives addressed digital test data words from the two PCM decommutators, located in the computer room. The circuits of the DDU are identical for both decommutator inputs and provide the following functions: (1) sample the incoming data rate, (2) switch decommutator inputs in the event of a read pulse failure, and (3) distribute the test data word received to the ESDU and various control consoles.

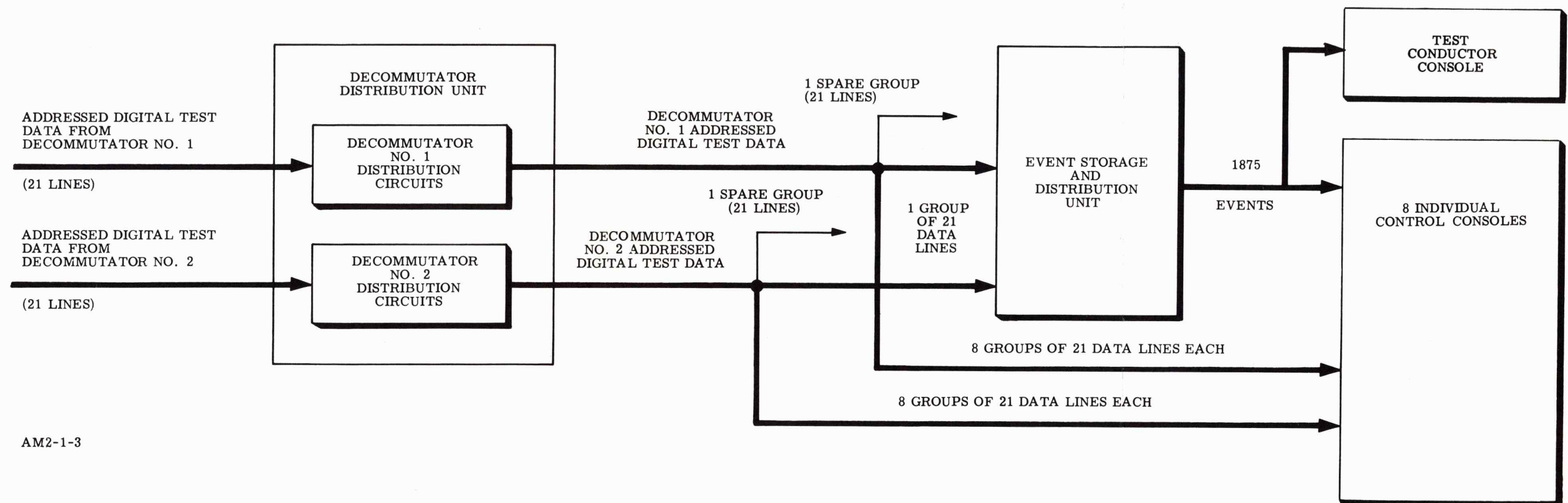


Figure 3-38. Control Room Test Data Display and Recording Equipment Block Diagram

3-259. Each test data word received from the decommutators is in parallel format. Each word is comprised of: 12 binary bits representing the address, 8 binary bits representing data, and an associated read pulse. To receive a test data word, 21 lines are required: one for each bit of the word. Either analog or event information may be represented by the incoming test data words and they arrive at the DDU input in an intermixed form.

3-260. The test data words are routed from the decommutators through the Terminal Patch Facility to the DDU via 42 hardlines. (See figure 3-39.) Twenty-one of these lines carry Decommutator No. 1 data and 21 carry Decommutator No. 2 data. Each line is terminated at the DDU input and is applied to a set of switch gates. All switching gate circuits are identical. Each of the 42 switching gates receives a Decommutator No. 1 input line and a Decommutator No. 2 input line. Each read pulse line (one from each decommutator) is also fed to a read pulse detection circuit. The outputs of each read pulse detection circuit are switching signals used to control the status of their associated switching gates.

3-261. Half of the switching gates will normally pass Decommutator No. 1 test data words while the remaining half will normally pass Decommutator No. 2 test data words. This will be the case as long as both decommutators are supplying a read pulse to the DDU. If, for any reason, a decommutator ceases to supply a read pulse, the output of the read pulse detection circuit associated with that particular decommutator will change state. This change of state in the read pulse detection circuit output will cause the status of the associated switching gates to change. As a result, the switching gates associated with the nonoperative decommutator will pass the test data still being supplied by the decommutator that is operative. For example, assume Decommutator No. 1 is not supplying an input but Decommutator No. 2 is. The Decommutator No. 1 read pulse detection circuit will cause the Decommutator No. 1 switching gates to accept and pass Decommutator No. 2 test data words. The Decommutator No. 2 switching gates will not change status and will continue to pass Decommutator No. 2 test data words. The switching function has three modes of operation that allow fully automatic, manual, or inhibited (that is, prevented from switching at any time) switching. Switches on the DDU allow the operator to select the desired mode of operation.

3-262. The test data word passed by a switching gate is fed to a set of associated distribution fan-out amplifiers that generate 10 identical isolated outputs. The net result is that, for each test data word input, 10 identical test data words are presented to the DDU output for distribution. One test data word output is sent to the ESDU; eight of the outputs are sent to those control consoles that contain digital logic, and one output is spared.

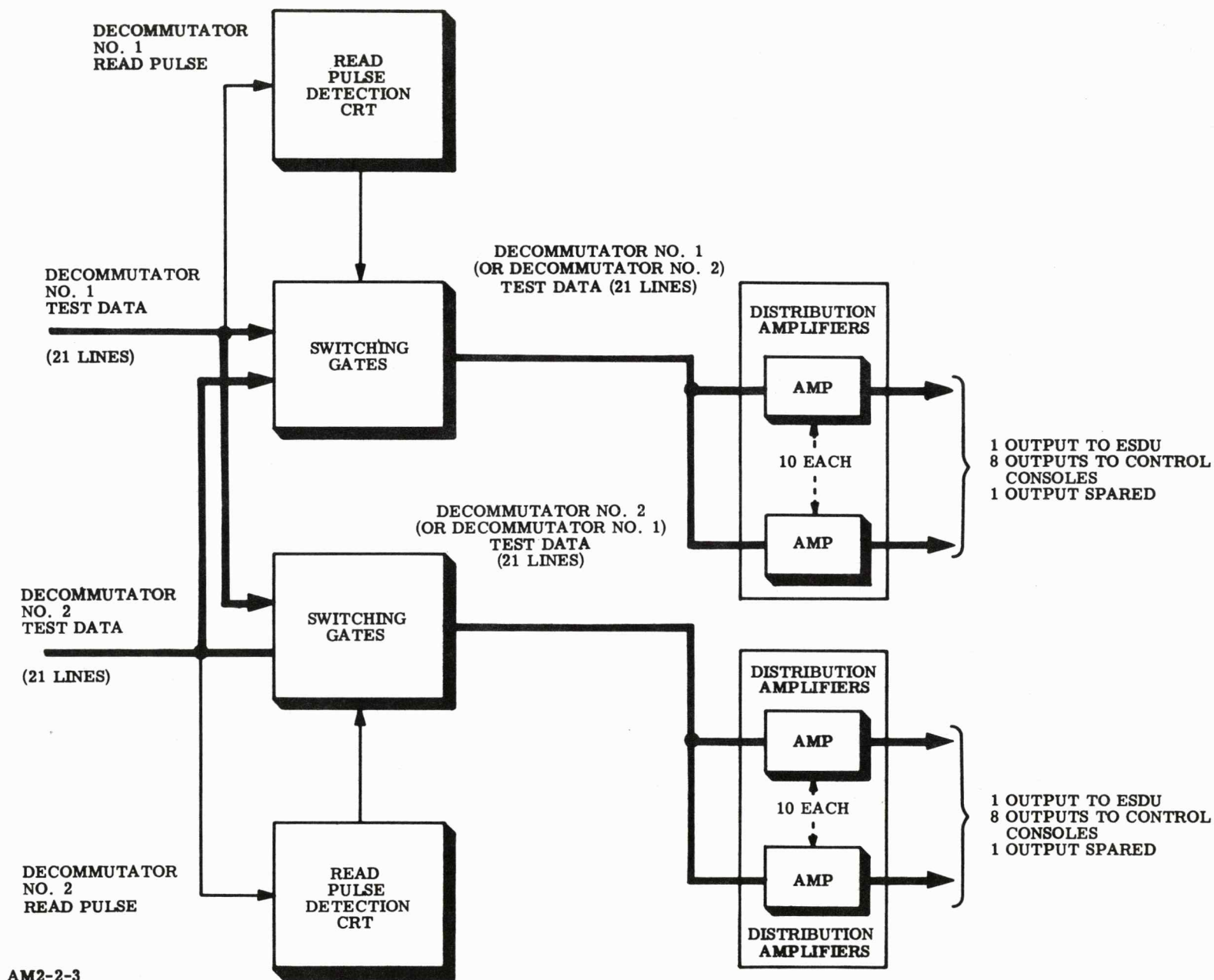


Figure 3-39. DDU Functional Block Diagram

3-263. DECOM DISTRIBUTION UNIT DESCRIPTION.

3-264. READ PULSE DETECTION CIRCUIT. (See figure 3-40.) The incoming read pulse is fed through a logic inverting NOR gate (1) to an integrator. The integrator produces an output with an effective d-c level that is proportional to the input pulse rate. The integrator output is fed to a Schmitt trigger. As long as the integrator is receiving a read pulse input at least once every millisecond, the integrator output is sufficient to keep the Schmitt trigger cut off. If for any reason the integrator does not receive an input for a period greater than one millisecond, the Schmitt trigger will "turn on." With the Schmitt trigger cut off, its output will be a steady -10 volts dc indicating that a read pulse is being supplied. The Schmitt trigger output will be 0 volt dc when it is "turned on." The Schmitt trigger output level is sent to a complementary driver (CD) through three NOR gates (2, 3, and 4). The CD (1) output (X) is sent to all 21 switching gates associated with the decommutator supplying the read pulse. The output of the CD (1) will be 0 volt dc when the read pulse is present and -10 volts dc when the read pulse is absent. The CD (1) output is also sent to a logic inverting NOR gate and thence to a second CD (2). The output (\bar{X}) of the CD (2) is -10 volts dc when the read pulse is present, and 0 volt dc when the read pulse is absent (the exact opposite of CD1).

3-265. The sequence just described is the automatic mode of operation for the read-pulse detector and will be the case whenever MODE SELECT switch S1 is set to the AUTO position. Setting S1 to the INHIBIT position will cause NOR (2) to constantly see a read-pulse-present condition. As a result, the X signal will be a constant 0 volt dc and the \bar{X} signal will be a constant -10 volts dc. The signals will remain at these levels regardless of the presence or loss of the read pulse. Setting S1 to the SWITCH (manual) position will cause NOR (3) to constantly see a read-pulse-not-present condition. The result will be that the X signal will be a constant -10 volts dc and the \bar{X} signal will be a constant 0 volt dc. Again the signals will remain at these levels regardless of the read-pulse input status.

3-266. SWITCHING GATE CIRCUIT. Since all of the switching gate circuits are identical, only one will be described here. For the purpose of this presentation, a Decommulator No. 1 switching circuit will be described. The description of a Decommulator No. 2 switching gate would be the same except that the decommutator inputs would be reversed.

3-267. A switching gate comprises three NOR gates (6, 7, and 8). One NOR gate (6) receives a Decommulator No. 1 input line and the X signal. NOR gate (7) receives a Decommulator No. 2 input line and the \bar{X} signal. NOR gate (8) receives the outputs of NOR gates (6) and (7), simultaneously. When the read pulse is present, the X signal will be 0 volt dc and will enable NOR gate (6), allowing the input signal to be passed to NOR gate (8). At the same time NOR gate (7) will be inhibited by a -10-volt d-c \bar{X} signal and will block the Decommulator No. 2

input from being passed by this gate. NOR gate (8) will accept and pass the Decommutator No. 1 signal from NOR gate (6). If, on the other hand, the read pulse is absent, the X and \bar{X} signal levels will be reversed. In this case the X signal will inhibit NOR gate (6) and prevent the Decommutator No. 1 input from being passed. By the same token, the \bar{X} signal will enable NOR gate (7) and allow it to pass the Decommutator No. 2 input on to NOR gate (8). The output of NOR gate (8), whether it be a Decommutator No. 1 or Decommutator No. 2 signal, is fed directly to associated distribution amplifiers, with one exception. The output of a read pulse NOR gate (8) is fed through another NOR gate, inverted, and then sent directly to associated distribution amplifiers. The result is that the logic level of the read pulse signal will be opposite to that of the address and data signals at the output of the DDU.

3-268. DISTRIBUTION AMPLIFIER CIRCUITS. All distribution amplifier circuits are identical and there is one circuit for each of the 42 decommutator input lines to the DDU. A distribution amplifier circuit consists of one power inverter (PI) and 10 emitter followers (EF). The input to a PI is amplified and inverted by the PI and is fed in parallel to 10 associated EF's. The output of one EF is fed to the ESDU. Eight EF's feed their output to an associated control console; the output of the remaining EF is spared.

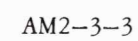
3-269. EVENT STORAGE AND DISTRIBUTION UNIT.

3-270. EVENT STORAGE AND DISTRIBUTION UNIT FUNCTIONS.

3-271. The input to the ESDU is addressed digital test data words in a parallel format. These test data words are received from the two decommutator units via the Terminal Facility Patchboard and DDU. A test data word may represent either analog or event information and is identified as one or the other by its associated address. The test data words arriving at the ESDU input are intermixed analog and event. The ESDU selects only the event words (by address recognition) and stores up to 150 such words, each consisting of eight discrete event functions for a total of 1200 events. (See figure 3-41.)

3-272. Addressed digital test data is received from the DDU by the ESDU via 42 parallel data lines. One half (21) of these lines carry Decommutator No. 1 data while the remaining half carries Decommutator No. 2 data. Each digital test data word received is composed of 20 parallel binary bits (12 address and 8 data) and a delayed timing read pulse. The test data words received are sent to distribution subassemblies where the address bits of the test data words are fed to two-stage logic inverting distribution amplifiers. The data bit and read pulse portions of the test data words are fed to one-stage logic inverting distribution amplifiers. The logic inverting distribution amplifiers are identical for both decommutators.

3-273. ADDRESS DECODING FUNCTIONS. Upon receipt of a test data word, the 12 address bits of the word and their complements are fanned out to 150 address decoding circuits by the



3-103/3-104

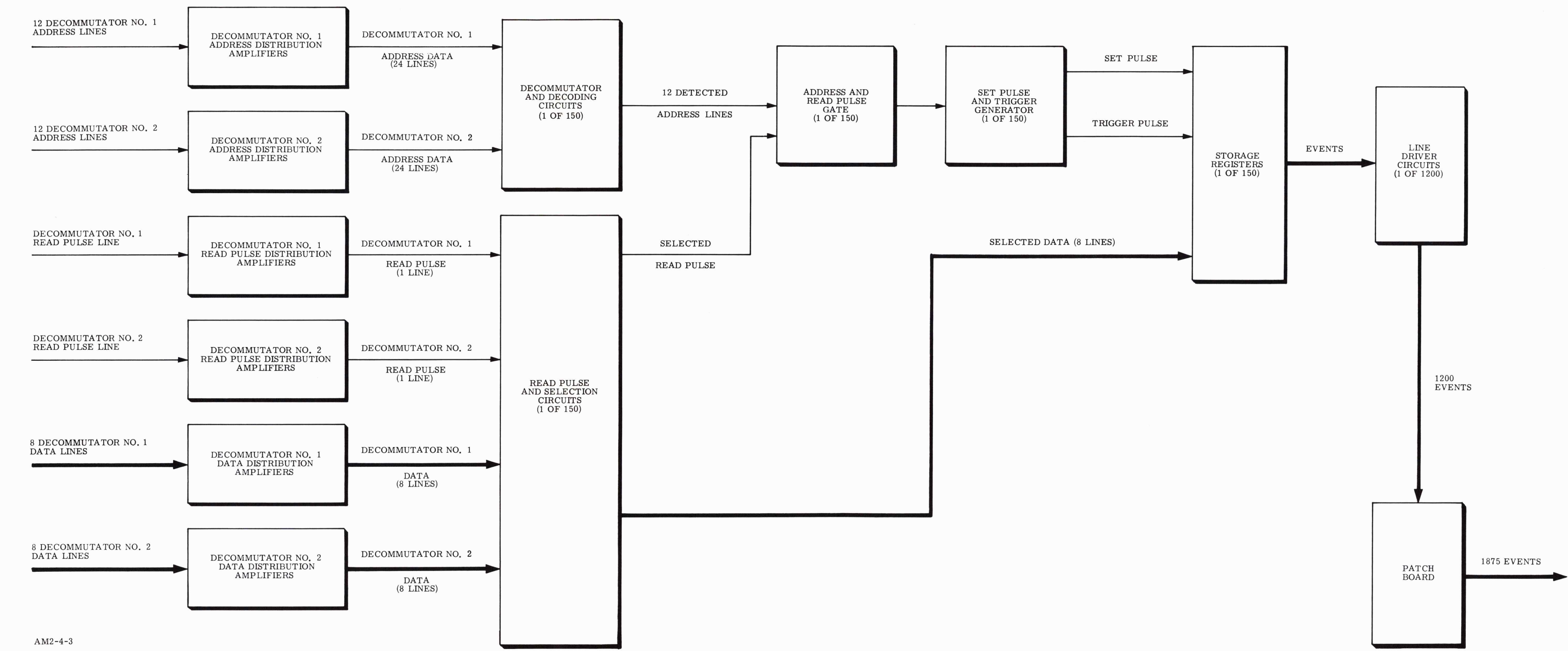


Figure 3-41. ESDU Block Diagram

two-stage distribution amplifiers. Each address decoding circuit comprises four selectable plug-in logic modules. The selection and arrangement of these modules determines the following: (1) the Decommulator No. 1 or Decommulator No. 2 address lines that will be monitored, and (2) the 12-bit address code that will be recognized in the form of four binary-coded octal digits.

3-274. When the bit content of an address matches one of the preselected address codes set into the decoding circuit, the 12 output lines of that particular decoding circuit all will be a logic 0 simultaneously. The 12 output lines of each address decoding circuit are fed to an associated address and read-pulse gate.

3-275. DATA AND READ-PULSE SELECTION FUNCTIONS. The eight data bits and read-pulse portions of the digital test data words received are distributed to 150 data and read-pulse selection circuits. One selection circuit is associated with each address decoding circuit. The data and read-pulse selection circuits consist of two jumper modules. The arrangement of these modules selects either the Decommulator No. 1 or Decommulator No. 2 data bits and read pulse to be passed. The decommutator input selected to pass is always the same as that which the associated address decoding circuit is currently accepting.

3-276. ADDRESS AND READ-PULSE GATE FUNCTIONS. Each address and read-pulse gate receives 13 input lines: 12 representing a preselected octal address from an associated read-pulse and data-selection circuit. The circuit functions as a 13-input AND gate and generates a "display" pulse whenever its associated address and read-pulse input lines are simultaneously at logic 0. The display pulse is fed to an associated set pulse and trigger generator circuit.

3-277. SET PULSE AND TRIGGER GENERATOR FUNCTIONS. Upon receiving a display pulse, the set and trigger generator develops a set pulse. The set pulse is sent simultaneously to an associated storage register and to a trigger-pulse generating circuit. The trigger pulses that are generated are slightly delayed from the set pulse and are sent to the associated storage register.

3-278. STORAGE REGISTER FUNCTIONS. The ESDU contains 150 storage registers, one for each addressed data word that can be recognized and processed by the ESDU. Each storage register is composed of eight flip-flops (bistable multivibrators), one for each data bit of a selected word. Each flip-flop receives a set pulse, trigger pulse, and one of eight selected data lines. Upon receipt of a set pulse, all flip-flops of the storage register are cleared of past data. After being cleared, the trigger pulse and any selected data present are ANDed at the input to each flip-flop and are loaded into the storage register. The output of each flip-flop

represents one discrete on/off event. A logic 0 indicates the event has occurred while a logic 1 indicates the event has not occurred or has ceased.

3-279. LINE DRIVER FUNCTIONS. The "false" output of each storage register flip-flop is applied to the input of a logic inverting line driver and then to the distribution patchboard. The purpose of the line drivers is to provide (1) the capability to drive relatively long cables, and (2) signal isolation prior to distribution by the patchboard. Since there are 150 storage registers supplying eight event outputs each, there are 1200 line drivers. It should be noted that because of inversion by the line drivers, the signals received by the patchboard will be the complement of the storage register output signals.

3-280. PATCHBOARD FUNCTIONS. The patchboard contained in the ESDU provides a flexible means to selectively distribute the event signals to appropriate control consoles. The patchboard is of the removable program type. The input to the patchboard is 1200 separate events. Each event is coupled to the output of the patchboard by means of plug-in jumper connections. To change the distribution of an event, the patchboard is removed from the ESDU and the appropriate jumper connections are made. After completing the necessary jumper changes, the patchboard is returned to the ESDU.

3-281. By means of "commoning blocks" or "squids," a single event input may be coupled to the several patchboard output connections. Each patchboard output pin is connected via hard-line to predesignated control consoles. The total output of the ESDU patchboard is 1875 event lines. To determine the exact number of event lines each individual control console receives, refer to table 3-7.

3-282. EVENT STORAGE AND DISTRIBUTION UNIT DESCRIPTION.

3-283. ADDRESS DISTRIBUTION AMPLIFIER CIRCUIT. (See figure 3-42.) There are three sets of address distribution amplifiers in the ESDU. Each set comprises 24 address distribution amplifier circuits: 12 for Decommutator No. 1 address bits and 12 for Decommutator No. 2 address bits. Each of the three sets of address distribution amplifiers is capable of driving 50 address decoding circuits. The total number of addressed test data words that can be processed is therefore 150. All address distribution amplifier circuits are identical.

3-284. An address distribution amplifier circuit comprises two power inverter (PI) modules and two complementary driver (CD) modules. (The following circuit description will be for one bit of an incoming address.) The incoming address data bit is fed directly to a PI module input. (It should be noted that the DDU sends the complement of the address to the ESDU.) The PI module amplifies and inverts the signal received. The output of the PI has two paths: (1) to a second PI, and (2) to associated CD. The second PI functions as the first PI, but only feeds an associated CD. The net result is that one CD is receiving a "true" level signal

input while the other CD is receiving a "false" level input. Each CD increases the drive capability of the signal it receives. The output of each CD is fed in parallel to 50 address decoding circuits.

Table 3-7. Event Distribution

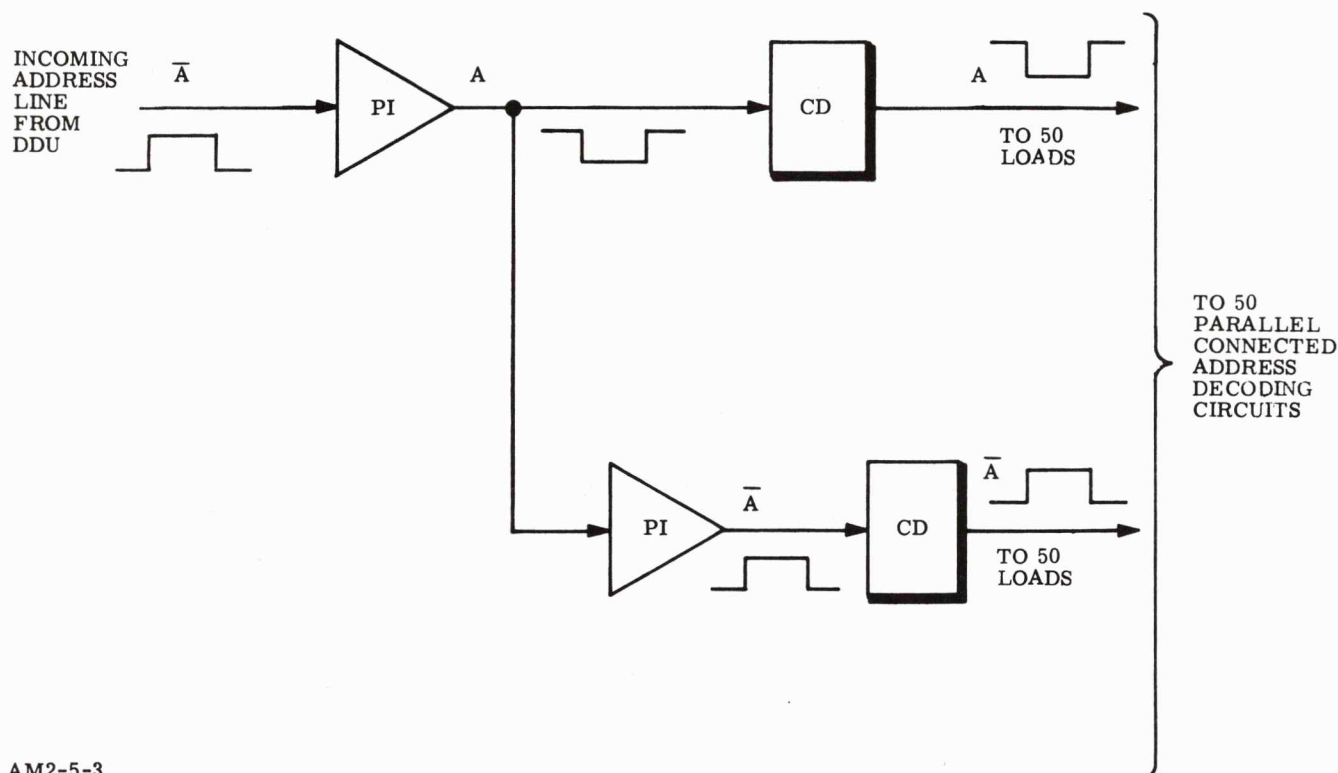
CONSOLE	NUMBER OF EVENTS RECEIVED
Environmental Control System Console	288
Fuel Cell and Cryogenics Console	240
Power and Sequential System Console	432
Guidance and Navigation System Console	192
Stabilization and Control Console	168
Service Propulsion and Reaction Control Console	432
Test Conductor Console	50
Instrumentation Console	48
Communication Console	<u>25</u>
TOTAL	1875

3-285. DATA AND READ PULSE DISTRIBUTION AMPLIFIER CIRCUITS. There are three sets of data and read-pulse distribution amplifiers in the ESDU. Each set is comprised of 18 data and read-pulse distribution amplifier circuits: nine for Decommutator No. 1 data bits and read pulse and nine for Decommutator No. 2 data bits and read pulse. Each of the three sets of data and read-pulse distribution amplifiers is capable of driving 50 data and read-pulse selection circuits. The total number of test data words that can be processed is therefore 150. All data and read-pulse distribution amplifier circuits are identical.

3-286. Each amplifier circuit is comprised of a PI module and an associated CD module. The incoming signals are fed to an associated PI module input. The PI module amplifies, inverts, and sends the input signal to its associated CD module. The CD module increases the drive capability of the signal it receives. The CD module output is fed in parallel to 50 data and read-pulse selection circuits.

3-287. ADDRESS DECODING CIRCUITS. (See figure 3-43.) All address decoding circuits are identical. There are 150 of these circuits employed in the ESDU, one for each test data

word to be processed. Each decoding circuit consists of an address-select module receptacle (sometimes referred to as a contact plate) and four plug-in address-select modules. The address-select module receptacle is divided into two halves: one half receives Decommutator No. 1 address data while the other half receives Decommutator No. 2 address data. The input to each receptacle half is 24 lines: 12 "true" level address lines and 12 "false" level address lines (e.g., an address and its complement). Each half of the module receptacle will accept four address-select modules and only one half of the receptacle is used at a time. Data from either of the decommutators can be monitored by plugging the address-select modules into the appropriate receptacle half. For example, if Decommutator No. 1 address data is to be monitored, four address-select modules will be plugged into the receptacle half receiving Decommutator No. 1 address data.



AM2-5-3

Figure 3-42. Typical Address Distribution Amplifier

3-288. Each plug-in module represents and recognizes one binary-coded octal digit of the incoming four octal digit address. The recognition of an octal digit by an address-select module is accomplished by means of internal jumper connections. Each module will receive three of the 12 address bits and their complement for a total of six inputs. Three of these

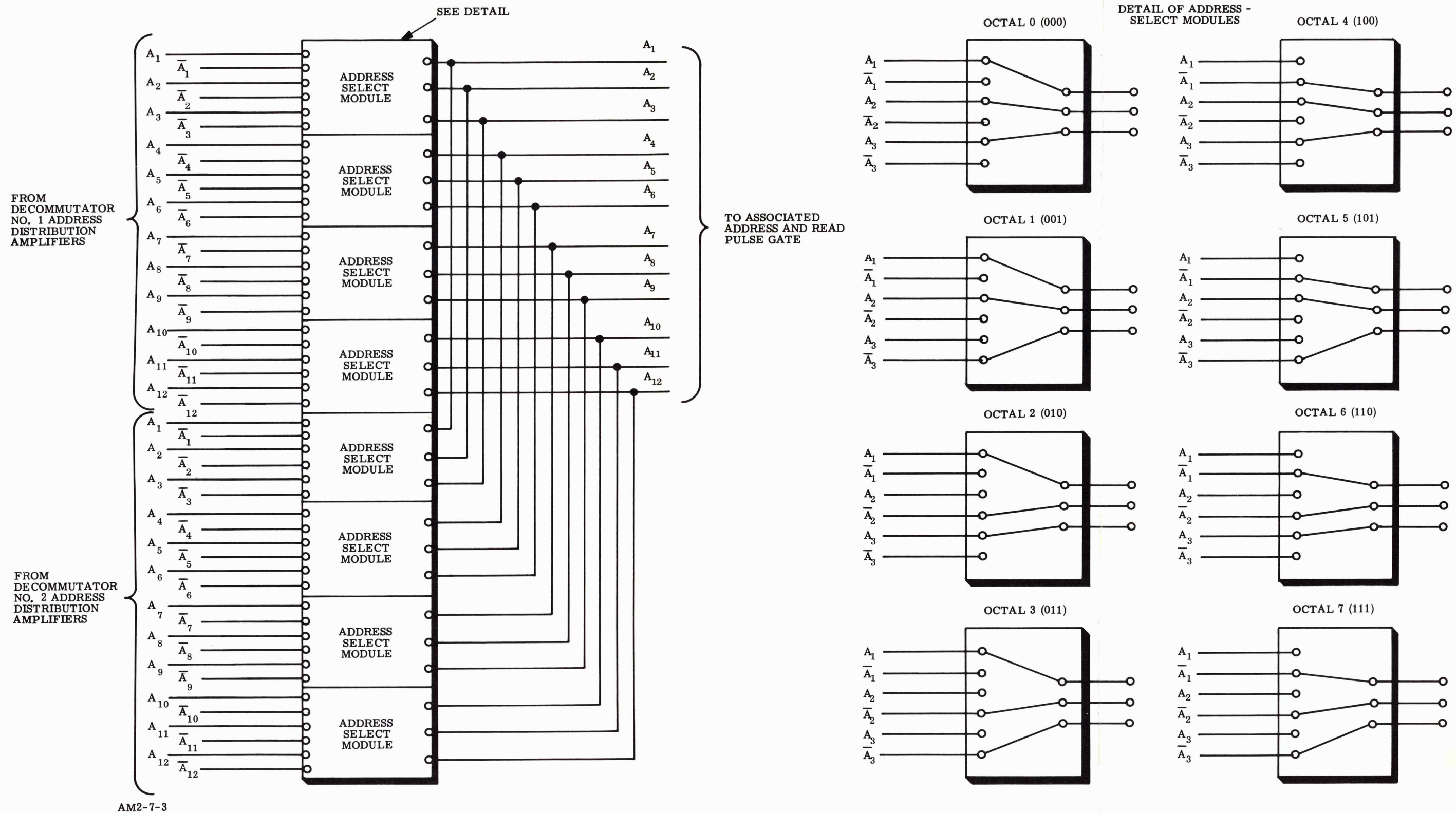


Figure 3-43. Typical Address Decoding Circuit

six inputs are jumpered to three output connections. The internal jumper connections are such that all three outputs of an address-select module will be logic 0 whenever the address bit combination is correct. (Typical address-select modules are shown as part of figure 3-43.) Each module receptacle has 12 output lines (three from each of the four address-select modules). When the correct address bit combination is present, all 12 lines will be at logic 0. The total 12-line output of each address-select module receptacle is sent to an associated address and read-pulse gate circuit.

3-289. DATA AND READ-PULSE SELECTION CIRCUITS. (See figure 3-44.) All data and read-pulse selection circuits are identical. There are 150 of these circuits employed in the ESDU: one associated with each of the 150 address decoding circuits. Each data and read-pulse selection circuit is comprised of an information-select module receptacle (sometimes referred to as a contact plate) and two plug-in information-select modules. The information-select module receptacle is divided into two halves: one half receives Decommutator No. 1 data and read-pulse signals while the other half receives Decommutator No. 2 data and read-pulse signals. The input to each half is nine lines: eight for data and one for the read pulse. Each half of the module receptacle will accept two information-select modules; however, only one half of the module receptacle is used at a time.

3-290. Either Decommutator No. 1 or Decommutator No. 2 signals can be passed on for processing, depending upon the side of the receptacle into which the information-select modules are plugged. The information-select modules are always plugged into the same side of the receptacle as their associated address select modules. For example, if the address select modules of the associated address decoding circuit were accepting Decommutator No. 2 address data, the information-select modules would be arranged to pass the Decommutator No. 2 data and read-pulse signals. The passing of an input signal by an information-select module is accomplished by means of internal jumper connections. The internal-jumper connections are such that each module input is coupled directly to the module output on a one-to-one basis. The read pulse selected is sent directly to an associated address and read-pulse gate circuit. The data selected is sent directly to an associated storage register.

3-291. ADDRESS AND READ-PULSE GATE CIRCUIT. (See figure 3-45.) All address and read-pulse gate circuits are identical. There are 150 of these circuits employed in the ESDU: one for each test data word that can be processed by the ESDU. An address and read-pulse gate is composed of four separate NOR gate modules. Collectively, the four NOR gates operate as a single AND gate with 13 inputs: 12 from an associated address decoding circuit and 1 (read pulse) from an associated address and read-pulse selection circuit. The output of the address and read-pulse gate will be a logic 1 when all 13 inputs are at a logic 0 simultaneously. When an address bit combination is recognized by an address decoding circuit, all

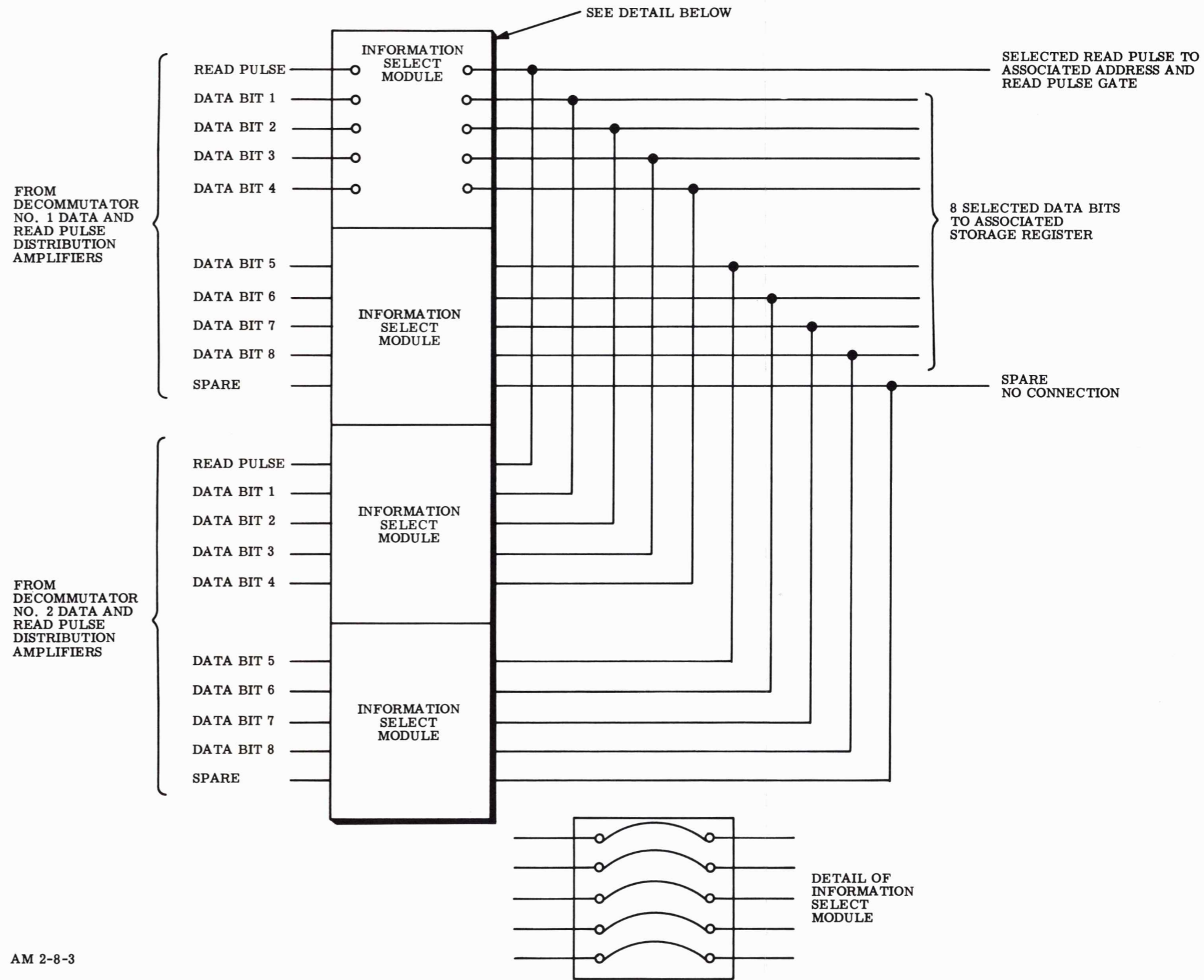
12 of its output lines will be at a logic 0 for an 8-microsecond period (equal to the period that address data is present on the incoming address lines). The read pulse follows the address data signals by 3 microseconds and has a duration of approximately 3.5 microseconds. As a result, the address and read-pulse gate output will be approximately 3.5 microseconds in duration and will lag the address data input by 3 microseconds. The address and read-pulse output is fed directly to an associated set-pulse and trigger-generator circuit.

3-292. SET-PULSE AND TRIGGER-GENERATOR CIRCUIT. (See figure 3-46.) All set-pulse and trigger-generator circuits are identical. There are 150 of the circuits employed in the ESDU: one for each data word that can be processed by the ESDU. A set-pulse and trigger-generator circuit is comprised of a complementary driver (CD) module and three power inverter (PI) modules. The input to the CD module is a 3.5-microsecond logic 1 from an associated address and read-pulse gate (provided the address and read-pulse input signal conditions have been met). The CD module amplifies the signal received and increases its drive capability. The output of the CD module is a set pulse that is sent to a PI module and to all eight flip-flops of an associated storage register.

3-293. Trigger pulses are generated from the set pulse in the following manner. A PI module receives the set pulse, inverts it, and feeds it in parallel to two other PI modules. Each of these PI modules amplify and invert the signal. The output of these PI modules is called a trigger pulse. Each trigger pulse is fed in parallel to four storage register flip-flops. Because the trigger pulses are developed from the set pulse, they will be of the same duration as the set pulse (3.5 microseconds).

3-294. STORAGE REGISTER CIRCUITS. (See figure 3-47.) There are 150 identical storage registers employed in the ESDU, one for each data word that can be processed by the ESDU. Each storage register is composed of eight flip-flops (one for each incoming data bit). Each flip-flop receives three inputs: a set pulse, a trigger pulse, and one of the eight incoming data bits. The 0 (or "false") side of each flip-flop is taken as the output. Therefore, the output data of a storage register is the complement of the input data. The following paragraphs describe the loading of new data into a storage register: first for a logic 1 data bit, and then for a logic 0 data bit.

3-295. Logic 1 Input. With a logic 1 input, a -10-volt d-c signal will be present on the data input line. Capacitor C1 will charge to -10 volts dc through R2, and diode CR1 will be back-biased. Transistor Q1 will be cut off by the +10-volt d-c bias voltage. Three microseconds later, a -10-volt d-c, 3.5-microsecond set pulse will be applied at the input to R1. Through the voltage divider action of R1 and R3, transistor Q1 will be forward biased and will cause the flip-flop to be set to a logic 1. Coincident with the set pulse, a -10-volt d-c, 3.5-microsecond trigger pulse is applied to one side of capacitor C1. The trigger pulse is differentiated



AM 2-8-3

Figure 3-44. Typical Data and Read-Pulse Selection Circuit

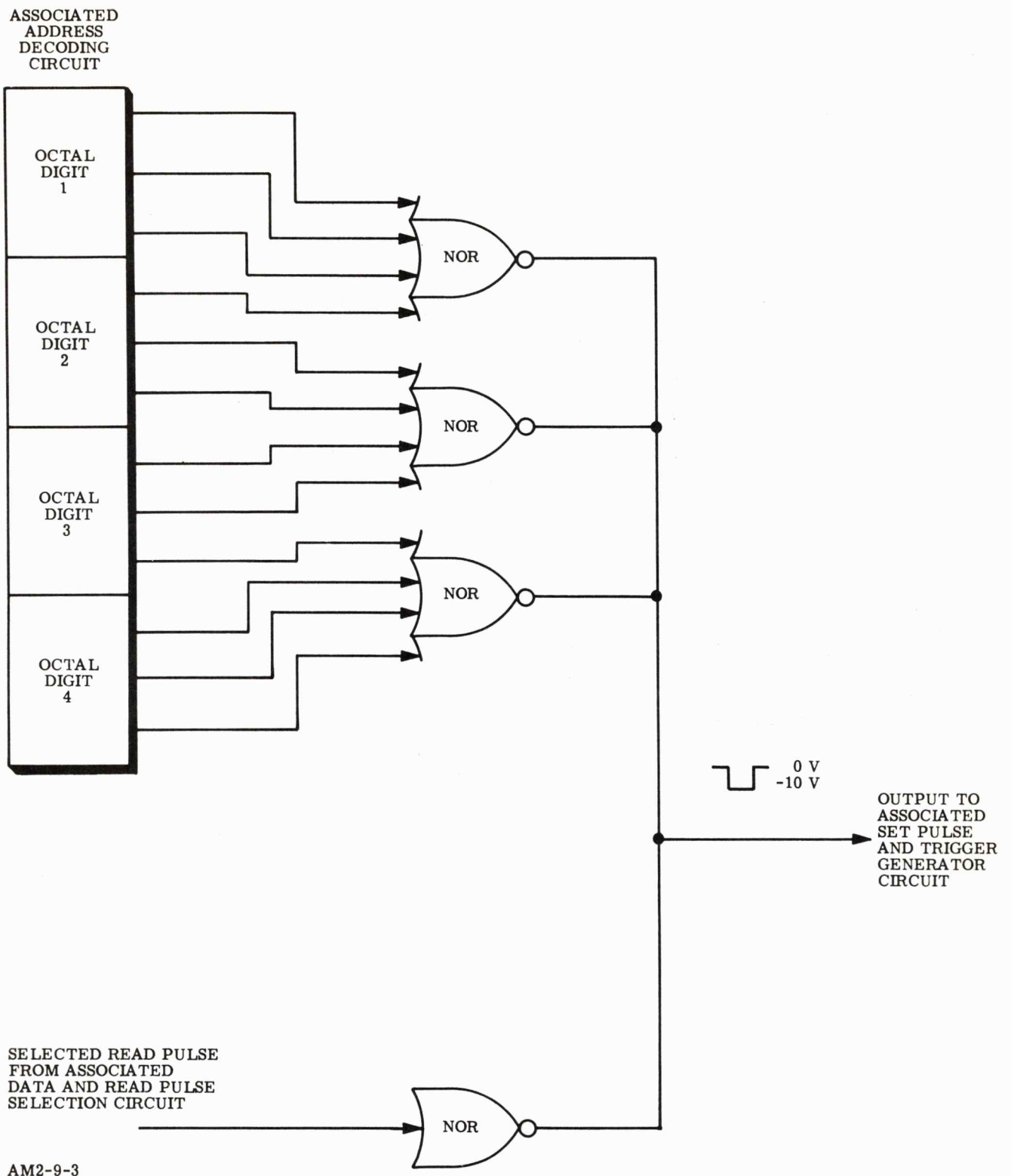
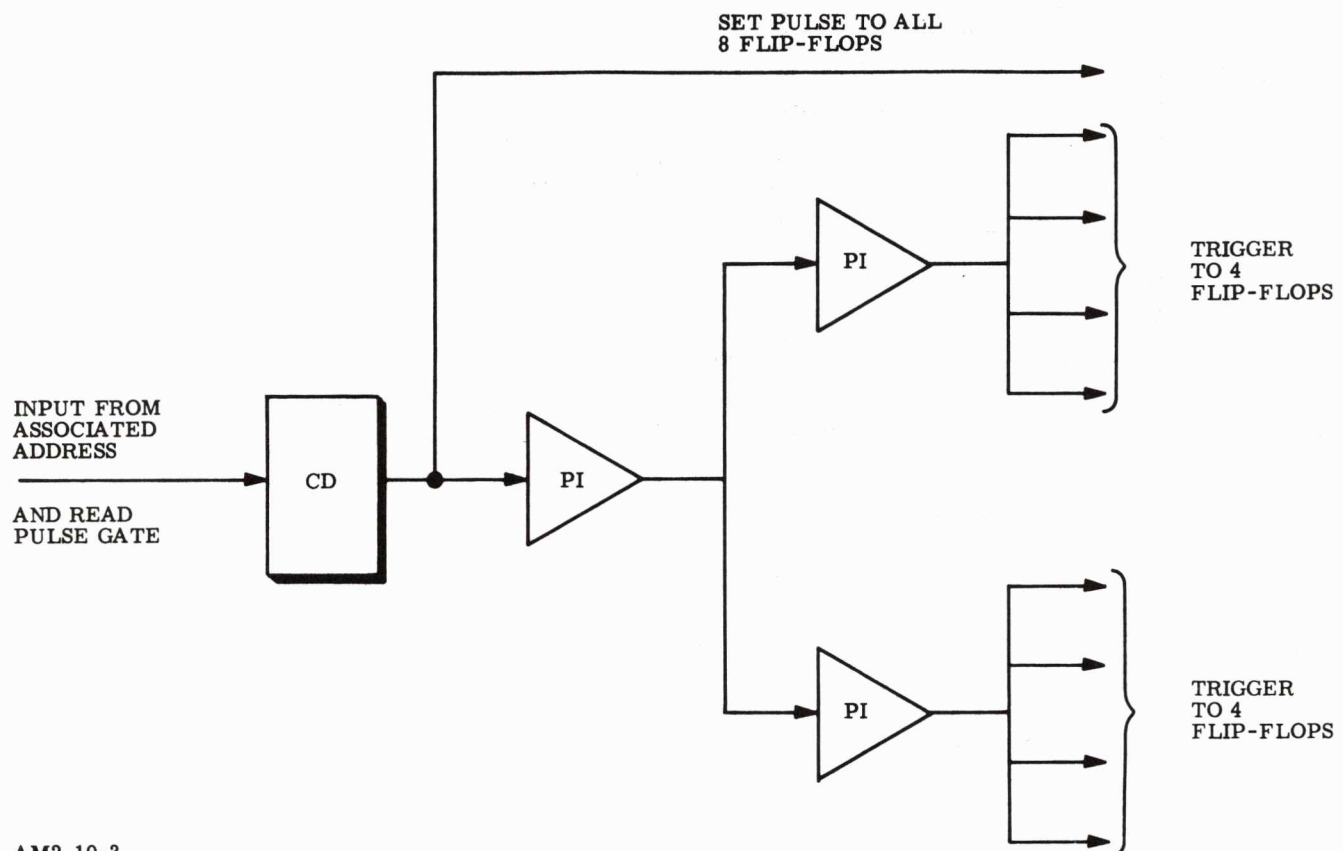
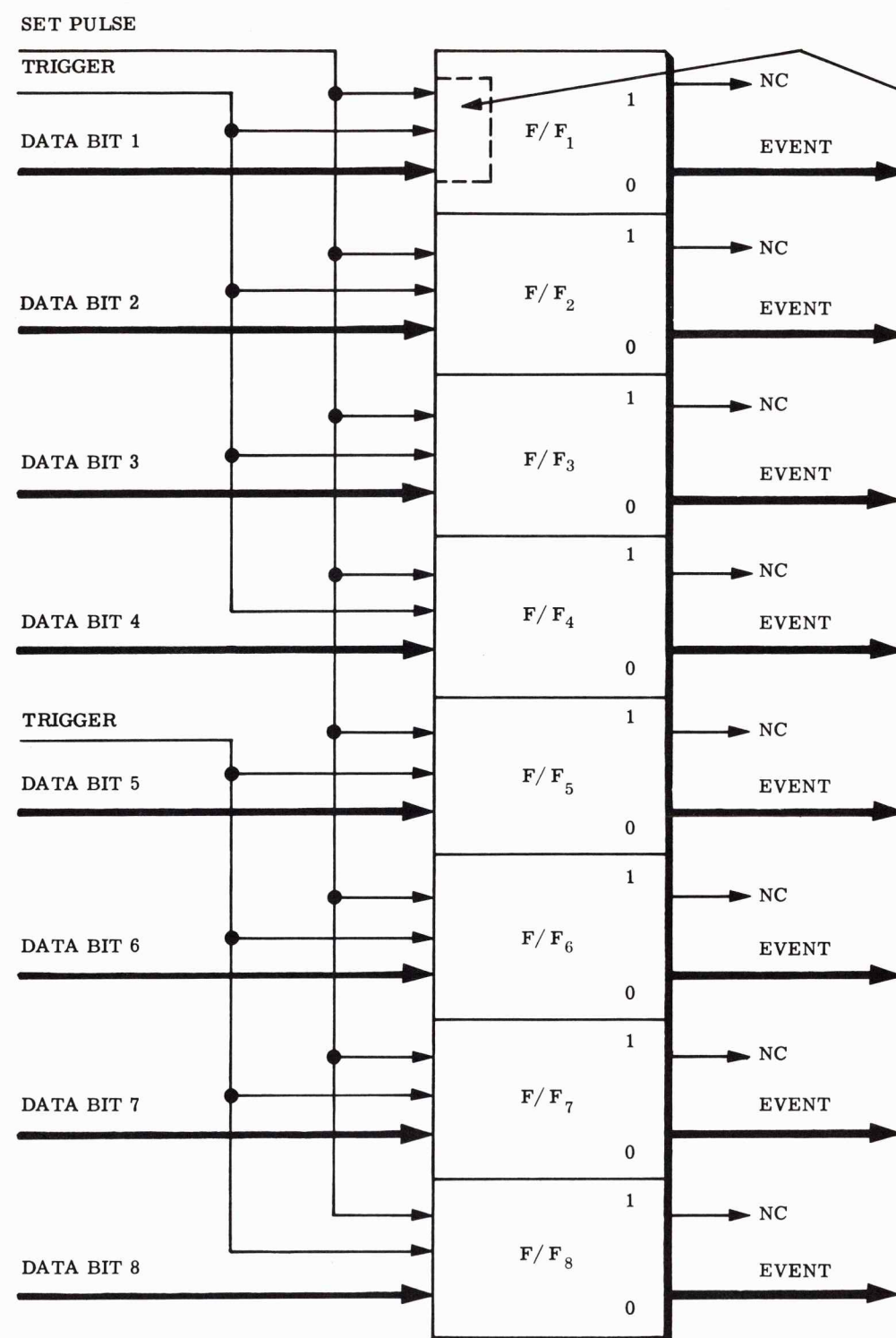


Figure 3-45. Typical Address and Read-Pulse Gate



AM2-10-3

Figure 3-46. Typical Set-Pulse and Trigger-Generator Circuit



AM2-11-3

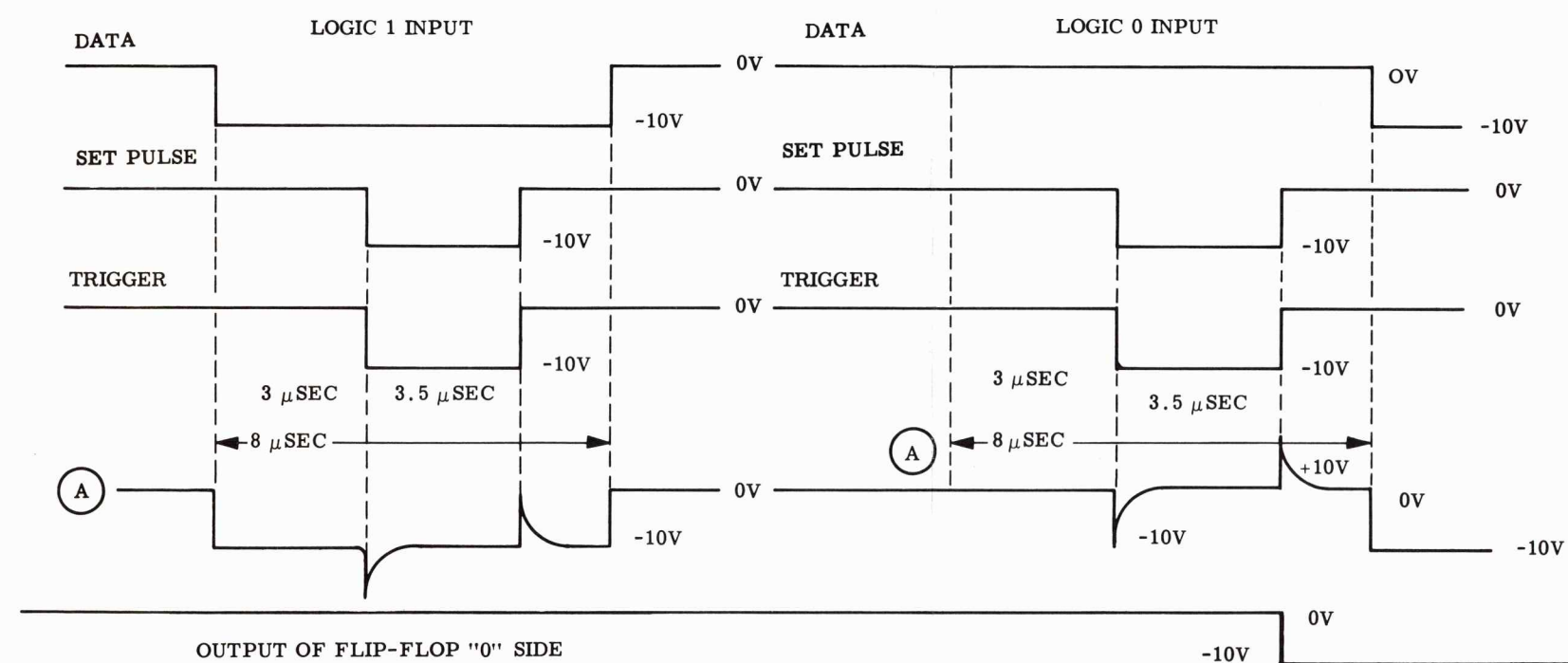
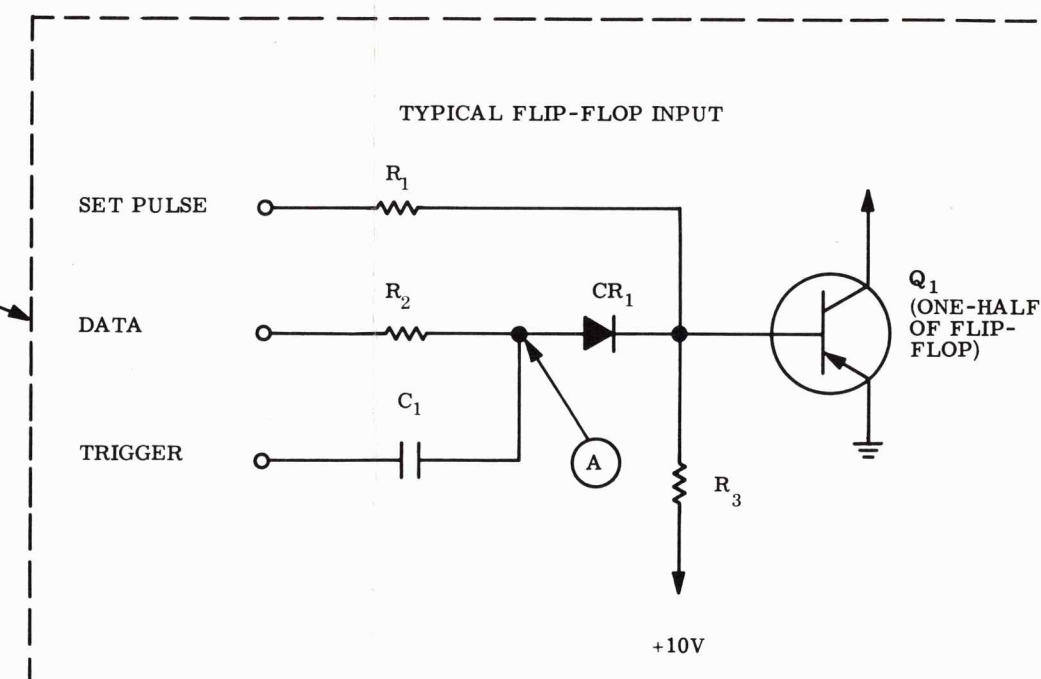


Figure 3-47. Typical Storage Register Circuit

by the combination of C1 and R2. As a result, the anode side of the diode will see a negative 10-volt spike followed by a positive 10-volt spike riding on a -10-volt d-c level. The negative spike will have no effect. The positive spike will cause CR1 to conduct. However, the bias on Q1 will not be greatly effected and Q1 will remain forward biased. The net result is that the logic 1 set into the flip-flop by the set pulse will remain unchanged. When this is the case, the zero side of the flip-flop will be 0 volt dc (or the complement of the input).

3-296. Logic-0 Input. With a logic-0 input, a logic 1 again will be set into the flip-flop by the set pulse. In this case, however, the differentiated trigger pulse will be riding on a 0-volt d-c level. As before, the negative going spike has no effect. The positive going spike, however, will be coupled through CR1 and will cause Q1 to be back-biased. The net result is that a logic 0 is now set into the flip-flop. When this is the case, the zero side of the flip-flop will be a -10-volt d-c signal (or the complement of the input). The zero side output of each flip-flop represents one discrete on/off event.

3-297. The total number of events that can be stored by the ESDU is 1200 (150 storage registers by 8 outputs each). Each flip-flop output is fed directly to an associated power inverter (PI) module. Each of the 1200 PI modules amplifies and inverts the signal it receives. The output of each PI module is connected directly to an associated input pin on the ESDU patchboard.

3-298. CONTROL CONSOLES.

3-299. CONTROL CONSOLE FUNCTIONS.

3-300. The inputs to the control room consoles are: (1) events via separate hardlines from the ESDU and (2) addressed digital test data via 42 hardlines from the DDU. Each incoming event line is fed to a console patchboard. The patchboard routes each event signal to an associated lamp driver and/or event recorder channel for display. Each lamp-driver output is connected directly to an event-module indicator lamp. The analog data words, intermixed with event data words, that are contained in the addressed digital test data input are recognized and stored. The recognition and storage process of analog data words is the same as that used for event data words in the ESDU (see paragraphs 3-273 through 3-278). The exact number of analog data words that can be accepted varies from console to console. The output of each storage register is applied to an associated D/A converter. All D/A converter output signals are fed to a console patch panel which selects and routes the analog signals to the appropriate meter module and/or analog recorder.

3-301. The display and recording requirements for each ACE-S/C control console is different. As a result, the type of subassemblies and the number of each type used by each control console is variable. To avoid unnecessary and awkward redundancy in the following paragraphs, one of each of the different subassembly types available is used to form a "typical"

control console configuration (figure 3-48). To determine the exact number of each display and recording subassembly used in a specific control console refer to table 3-8.

3-302. Event data flow event signals are received by control room consoles from the ESDU patchboard over separate hardlines. The signals received are a logic 1 when an event has occurred. The number of event lines received by each control console is dependent upon the display requirements of that particular console and is different for each console. Each incoming event line is connected directly to an input pin on the console patchboard. At this point the event signal may be routed to either a lamp driver or an event recorder channel or to both simultaneously.

3-303. LAMP DRIVER FUNCTIONS. A lamp driver is a solid-state switch that is connected in series with one side of an indicator lamp in an associated event module. The lamp driver will cause the indicator lamp to light when its associated event input is a logic 1; i.e., the event has occurred.

3-304. EVENT MODULE FUNCTIONS. The event modules provide the means to display event data to the control console operators. Up to 24 events may be displayed on each event module by means of indicator lamps. Physically, an event module is an enclosed chassis that is plugged into the console. The front panel of each module consists of three vertical rows of eight indicators each. Each indicator is composed of two lamps connected in parallel. The lamps are lighted when the associated event has occurred. A press-to-test push-button on each event module will light all indicator lamps at once for pretest confidence check. In certain applications, the event modules are interchangeable with meter modules.

3-305. EVENT RECORDER FUNCTIONS. The event recorder provides a means of permanently recording the time and duration of an event. Two types of event recorders are used in various control consoles: (1) a 32-channel multi-stylus recorder that provides a continuous-write deflection type presentation, and (2) a 100-channel multi-stylus recorder that provides a write/no-write type presentation. All recorders use roll-chart paper and have paper-speed controls. Two recorder channels are reserved for time (AMR B1) code data.

3-306. ANALOG DATA FLOW. Addressed digital test data is received by those control consoles that contain digital processing logic. This data is received from the DDU via 42 parallel data lines and is the same as that sent to the ESDU. Only that test data pertinent to analog information will be accepted and processed by a control console. One half (21) of the input lines carry Decommutator No. 2 data test data words. Each test data word received is composed of 20 parallel binary bits: 12 address and 8 data. The twenty-first input is a delayed timing read pulse. The address bits of the test data words are fed to two-stage logic inverting distribution amplifiers. The data bits and read pulse are fed to one-stage logic inverting

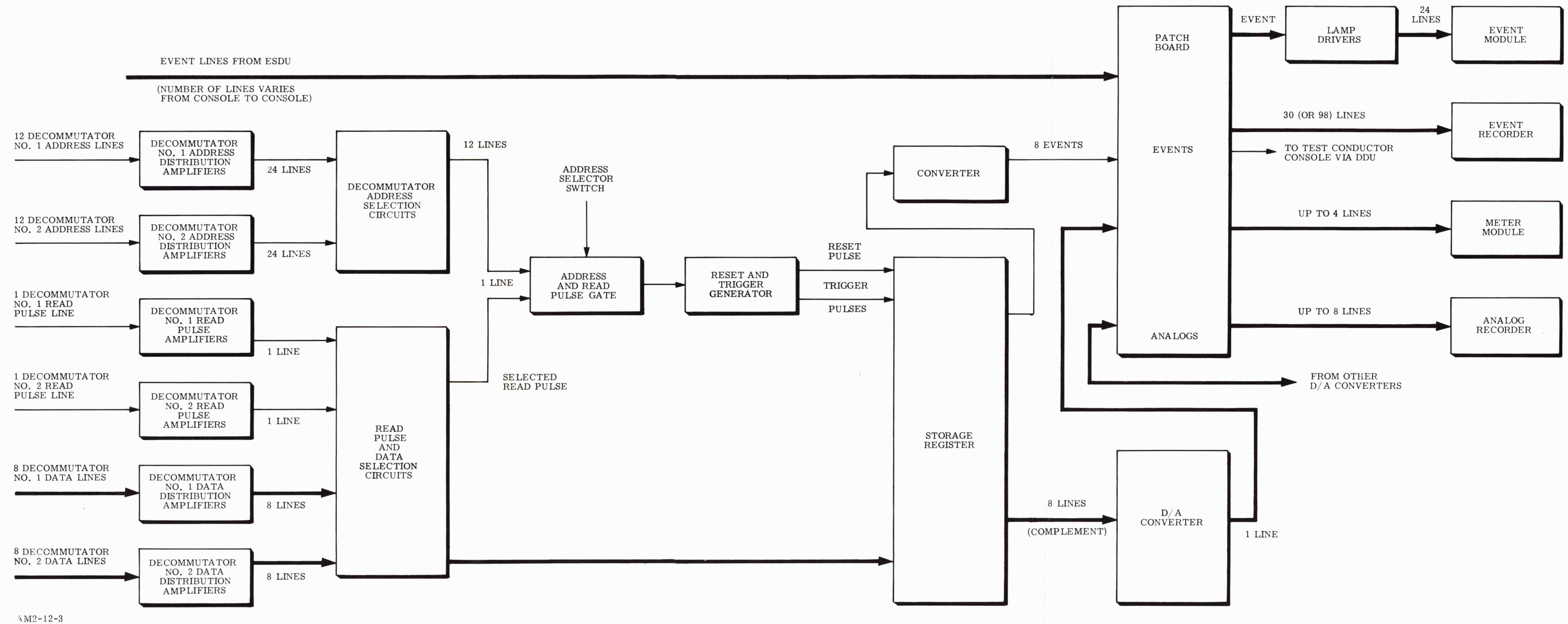


Figure 3-48. Typical Control Console Block Diagram

Table 3-8. Control Console Component Complement

COMPONENT NAME	ENVIRONMENTAL CONTROL SYSTEM CONSOLE			FUEL CELL AND CRYOGENICS CONSOLE			POWER AND SEQUENTIAL SYSTEM CONSOLE			GUIDANCE AND NAVIGATION SYSTEM CONSOLE			STABILIZATION AND CONTROL CONSOLE		SERVICE PROPULSION AND REACTION CONTROL CONSOLE		TEST CONDUCTOR CONSOLE	INSTRUMENTATION CONSOLE	COMMUNICATIONS CONSOLE
	HIGH CABINET UNIT NUMBER 1	LOW CABINET UNIT NUMBER 11	SHARED HIGH CABINET UNIT NUMBER 8	HIGH CABINET UNIT NUMBER 2	LOW CABINET UNIT NUMBER 12	HIGH CABINET UNIT NUMBER 3	LOW CABINET UNIT NUMBER 13	HIGH CABINET UNIT NUMBER 7	HIGH CABINET UNIT NUMBER 4	LOW CABINET UNIT NUMBER 14	HIGH CABINET UNIT NUMBER 5	LOW CABINET UNIT NUMBER 15	HIGH CABINET UNIT NUMBER 6	LOW CABINET UNIT NUMBER 16	LOW CABINET UNIT NUMBER 10	LOW CABINET UNIT NUMBER 18	LOW CABINET UNIT NUMBER 19		
Address Decoding Circuits	80			76		44			72		56		80			8	32		
Data and Read Pulse Selection Circuits	80			76		44			72		56		80			8	32		
Address and Read Pulse Gate	80			76		44			72		56		80			8	32		
Set Pulse and Trigger Generator Circuit	80			76		44			56		40		56			8	8		
Storage Register	80			76		44			56		40		56			8	8		
D/A Converter	80			76		44			56		40		56			8	8		
Patch Board	1		1	1		2			1		1		1		1	1	1		
Lamp Driver	216			144		408			96		144		336		110	24	8		
Event Module	5	4		6		14	3		2	2	2	4	12	2		1			
Meter Module	10			11		5			6	2	4		6	4		2	2		
8-Channel Analog Recorder	4		1	3		3			3		3		2						
32-Channel Event Recorder			1			3			1										
100-Channel Event Recorder								2			1		1						
2 to 1 Analog Switch Panel											2								
3 to 1 Analog Switch Panel									1				2						
4 to 1 Analog Switch Panel																		1	

distribution amplifiers. The logic inverting distribution amplifiers are identical for both Decommutator No. 1 and Decommutator No. 2 inputs.

3-307. ADDRESS DECODING FUNCTIONS. Upon receipt of a test data word, the 12 address bits of the word and their complements are distributed to address decoding circuits by the two-stage distribution amplifier. The total number of address decoding circuits contained in a console is determined by the needs of that console. Each address decoding circuit is comprised of four selectable plug-in logic modules. The selection and arrangement of the address decoding logic modules determines the following: (1) the decommutator address lines that will be accepted and (2) the four octal digit address code that will be recognized. When the bit content of an address received matches one of the address codes set into an address decoding circuit, the 12 output lines of that particular address decoding circuit will all be a logic 0 simultaneously. The 12 output lines of an address decoding circuit are fed to an associated address and read-pulse gate.

3-308. DATA AND READ-PULSE SELECTION FUNCTIONS. The eight data bits and read-pulse portions of the received digital test data words are fanned out to data and read-pulse selection circuits by the one-stage distribution amplifiers. There is one data and read-pulse selection circuit for each storage register contained in a given console. The data and read-pulse circuits contain two jumper modules. The arrangement of these modules selects either the Decommutator No. 1 or Decommutator No. 2 data bits and read pulse to be passed on for processing. The decommutator input selected to pass is always the same as that which the associated address decoding circuit is currently monitoring.

3-309. ADDRESS AND READ-PULSE GATE FUNCTIONS. Each address and read-pulse gate received 13 input lines: 12 representing a preselected octal coded address from an associated address decoding circuit and one selected read pulse from an associated data and read-pulse selection circuit. The gate functions as a 13-input AND circuit, generating a "display" pulse when all inputs are at the same logic level. The "display" pulse is fed to an associated set-pulse and trigger-generator circuit.

3-310. SET-PULSE AND TRIGGER-GENERATOR FUNCTIONS. The set-pulse and trigger-generator develops a set pulse for each "display" pulse input. The set pulse is simultaneously sent to an associated storage register and trigger-generating circuit. The trigger pulses generated from the set pulse are also fed to the associated storage register.

3-311. STORAGE REGISTER FUNCTIONS. The control consoles contain a storage register for each analog display and/or recorder mounted on the front panel of the control console. Each storage register contains eight flip-flops (bistable multivibrators), one for each selected data bit. Each flip-flop receives a set pulse, trigger pulse, and one data line. Upon receipt

of a set pulse, all flip-flops are cleared of past data. Following the set pulse, the trigger pulse and any selected data present are ANDed at the input to each flip-flop and new data is loaded into the storage register. All eight outputs of the storage register are sent collectively to an associated digital-to-analog converter. The data output of a storage register is the complement of the data input.

3-312. D/A CONVERTER FUNCTIONS. For each storage register there is an associated D/A converter. A D/A converter transforms the eight-bit binary data it receives from a storage register into a representative d-c voltage. This output voltage is divided into 256 increments, one for each binary combination using eight binary digits. The output analog signal is the complement of the digital input signal. For example:

<u>Input</u>		<u>Output</u>
11111111	=	0.0 volt dc
00000000	=	-5.0 volts dc

3-313. Each D/A converter output is fed directly to an input pin on the control console patch-board. The incoming analog signals are patched to a meter module or to an analog recorder, or to both simultaneously.

3-314. METER MODULE FUNCTIONS. Meter modules provide the means to display current analog data to control console operators. Up to four different analog signals may be displayed on each meter module at one time by means of four edgewise panel meters. Physically, a meter module is an enclosed chassis that is plugged into the front panel of a control console. Four edgewise 0-1-milliampere meter movements are mounted on the front panel of each meter module. Meter identification inserts are readily removed and replaced without removing a meter from the module case. Certain meter modules are interchangeable with event modules.

3-315. ANALOG RECORDER FUNCTIONS. The eight-channel analog recorders will accept and record up to eight channels of analog data simultaneously. Two additional channels are provided for recording real- and playback-time codes. The analog recorders are moving-paper-roll-chart, continuous-write-deflection-type recorders. The recorders provide a permanent, time-correlated, graphical presentation on rectangular coordinate paper. Eight inches of the recorded data are visible on the recorder front panel. The recorders include controls for selecting paper speed and channel sensitivity.

3-316. ANALOG SELECTION SWITCH FUNCTIONS. On certain consoles, an analog address selection switch panel is made available to the console operator. (See table 3-8.) Three different types of switch panels are available: 2 to 1, 3 to 1, and 4 to 1. Eight selection switches are mounted on each panel. Each switch has control over one analog signal input to

the patchboard. By the use of a selection switch, the console operator can select one of 2, 3, or 4 (as the case may be) analog parameters to be displayed by the meter connected to that patchboard input. The same is true for the inputs to an associated analog recorder.

3-317. CONVERTER FUNCTIONS. The Power and Sequential System Console and the Communications Console contain special converter circuits. Each converter monitors the three most-significant-bit input lines of an associated D/A converter. The output of a converter is a logic 1 whenever the associated analog function is equal to or above 12 percent of full scale. There are eight converter circuits in each of the two consoles mentioned above. The outputs of the converters are treated as event signals. Each signal is sent to the patchboard in its respective console and is routed to an event module in that console or to the Test Conductor Console via the DDU.

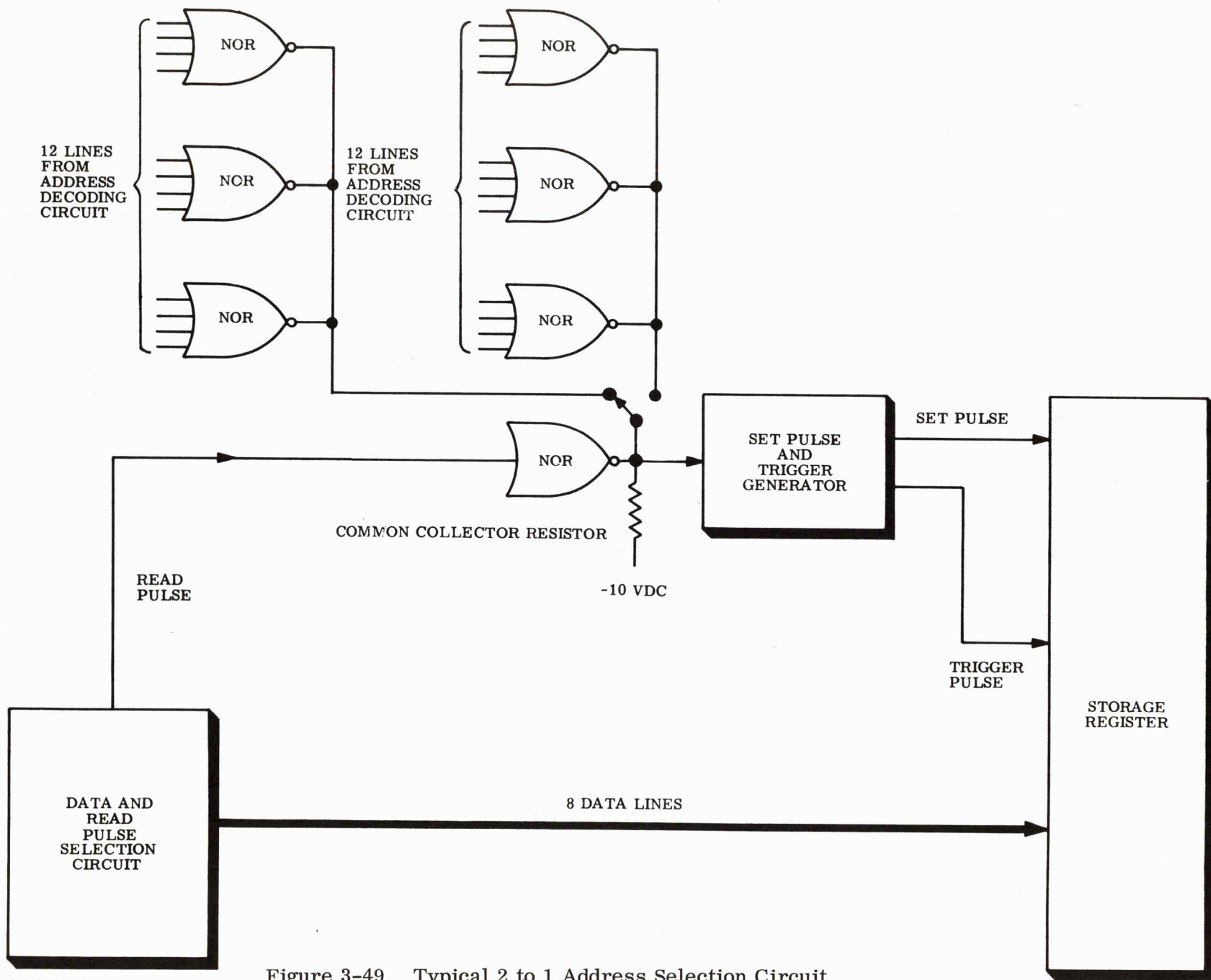
3-318. CONTROL CONSOLE CIRCUIT DESCRIPTIONS.

3-319. ADDRESS DISTRIBUTION AMPLIFIER CIRCUITS. For a circuit description of the address distribution amplifiers, refer to paragraph 3-283. The address distribution amplifiers contained in the control consoles are identical to the address distribution amplifiers used in the ESDU.

3-320. DATA AND READ PULSE DISTRIBUTION AMPLIFIER CIRCUITS. For a circuit description of the data and read-pulse distribution amplifiers, refer to paragraph 3-285. The data and read-pulse distribution amplifiers contained in the control consoles are identical to the data and read-pulse distribution amplifiers used in the ESDU.

3-321. ADDRESS DECODING CIRCUITS. For a description of an address decoding circuit, refer to the ESDU address decoding circuit description given in paragraph 3-287. The address decoding circuits used in the control consoles are identical to those in the ESDU with one exception. The number of address decoding circuits employed in a control console varies from console to console, instead of being exactly 150 as in the ESDU.

3-322. ADDRESS AND READ-PULSE GATE CIRCUITS. The operation of a control console address and read-pulse gate is identical to an ESDU address and read-pulse gate (see paragraph 3-291) with one exception. Certain control consoles have the capability to select one address from a number of addresses. Three selection combinations are available: 2 to 1, 3 to 1, and 4 to 1. Figure 3-49 illustrates a typical 2 to 1 selection combination. The 2 to 1 combination shown will allow the data associated with one of two addresses to be loaded into a single storage register. The selection of the desired address is accomplished by means of ANALOG SELECT switches located on the front panel of the control console. As shown in figure 3-49, an ANALOG SELECT switch will enable only the NOR gates receiving inputs from the address decoding circuit associated with the selected address. The only NOR gates that



AM2-13-3

Figure 3-49. Typical 2 to 1 Address Selection Circuit

will be operative are those connected to the common collector resistor through the contacts of the ANALOG SELECT switch. The three selected (enabled) address NOR gates operate in conjunction with a common read-pulse NOR gate. The resulting four NOR-gate combinations function as a single address and read-pulse gate as used in the ESDU. For a detailed description of an address and read-pulse gate circuit refer to paragraph 3-291. It should be noted that the switching process shown in figure 3-49 is the same as that used for the 3 to 1 and 4 to 1 selection combinations.

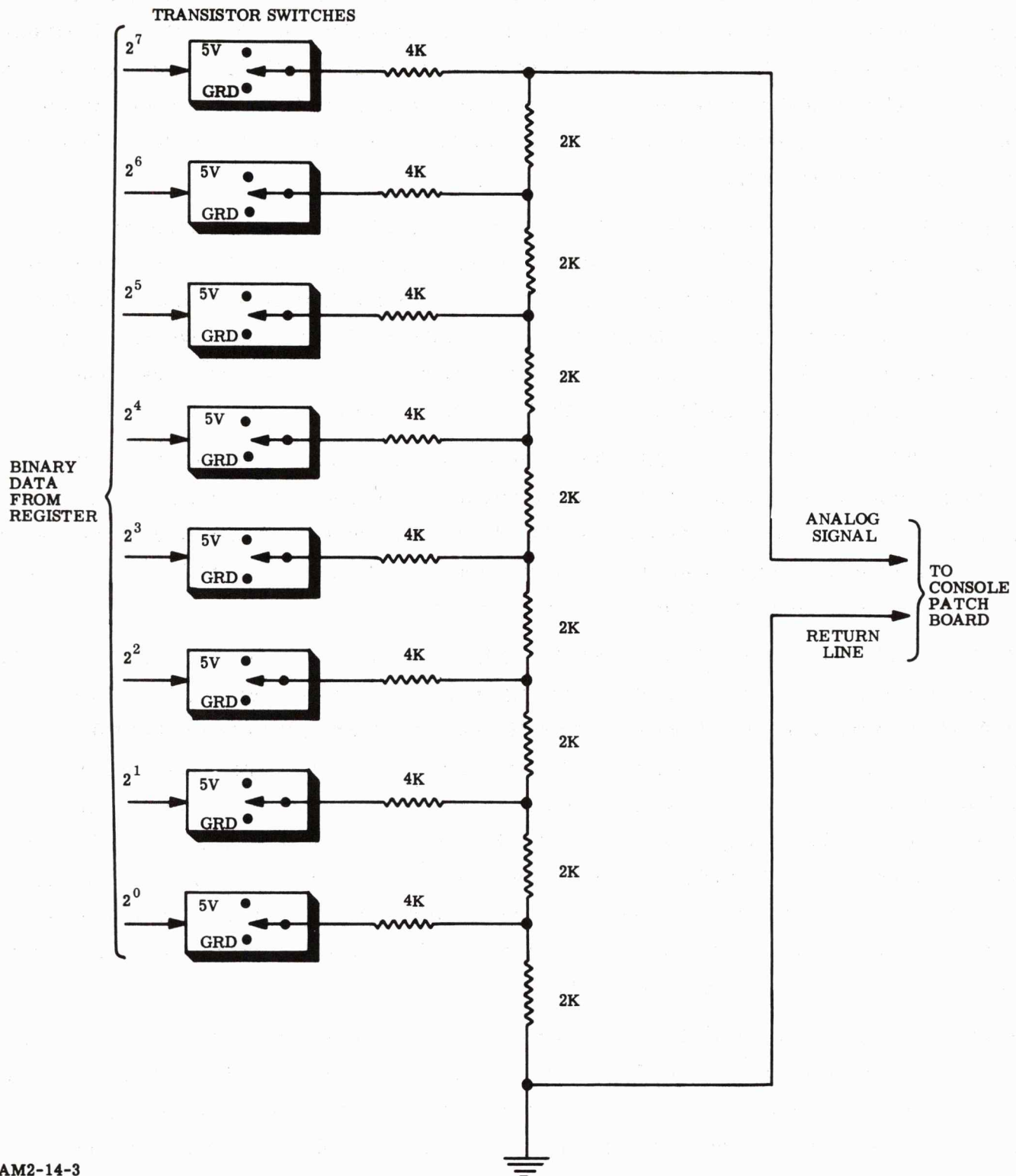
3-323. SET-PULSE AND TRIGGER-GENERATOR CIRCUIT. For a description of a set-pulse and trigger-generator circuit, refer to the ESDU set-pulse and trigger-generator circuit description given in paragraph 3-292. The set-pulse and trigger-generator circuits used in the control consoles are identical to those used in the ESDU, with one exception. The number of set-pulse and trigger-generator circuits employed in the control consoles varies from console to console, instead of being exactly 150 as in the ESDU.

3-324. STORAGE REGISTER CIRCUITS. For a detailed circuit description of a storage register, refer to paragraph 3-294. The operation of a control console storage register is identical to an ESDU with two exceptions: (1) the exact number of storage registers employed in a control console varies from console to console, and (2) all eight output lines of a storage register are fed collectively to an associated D/A converter.

3-325. DIGITAL-TO-ANALOG CONVERTER CIRCUITS. Each D/A converter receives eight binary data bits from an associated data storage register. A D/A converter is composed of eight identical voltage divider networks (one for each incoming data bit) so connected as to form a resistive ladder. (See figure 3-50.) Switching transistors control the input to each voltage divider network. The switching action is such that a logic 0 will cause -5 volts dc to be applied to a voltage divider network input. A logic 1 will ground the input to a voltage divider network. The output of a D/A converter is taken across the entire resistive ladder. The voltage developed across the resistive ladder will depend directly upon the bit combination received from the associated storage register. The output of each D/A converter is fed directly to an input pin on the console patchboard.

3-326. PATCHBOARD CIRCUITS. The console patchboards provide a flexible means of selectively distributing incoming analog and event signals to appropriate display and/or recording devices. The patchboards used are of the removable program type. Several different types of patchboards are available because not all control console requirements are identical.

3-327. Assume, for presentation purposes, that a particular patchboard is to distribute both analog and event input data. The patchboard then would be divided into four sections: (1) an event output hub, (2) an event input hub, (3) an analog output hub, and (4) an analog input

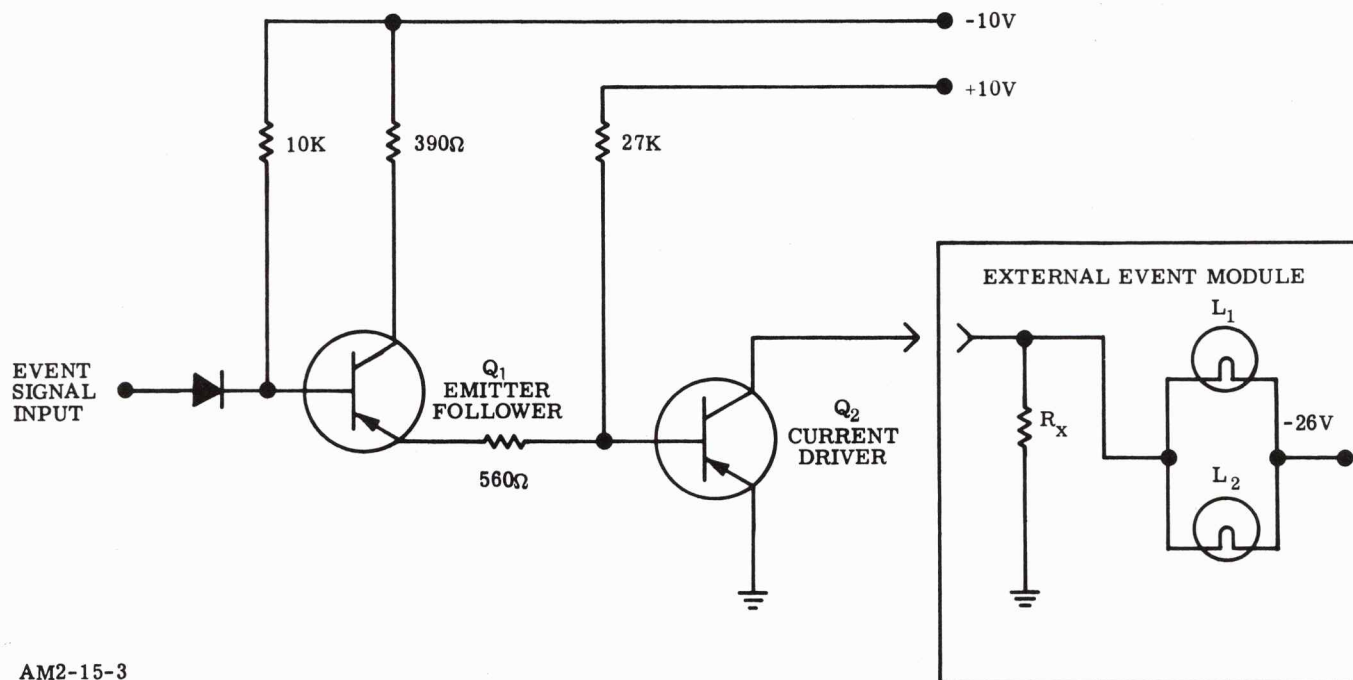


AM2-14-3

Figure 3-50. Typical D/A Converter Circuit

hub. (An output hub receives incoming data while an input hub couples the data to the appropriate display and/or recording devices.) Single-pin, molded-plug jumper cables are used to route event signals. Two-pin, molded-plug jumper cables are used to route analog signals. A change in signal routing is accomplished by removing the patchboard from the control console, making the necessary new jumper connections, and then reinstalling the patchboard in the control console.

3-328. LAMP DRIVER CIRCUITS. Associated with each event module indicator there is a lamp driver circuit. Each lamp driver circuit acts as a current switch. A typical lamp driver and its associated indicator lamps are shown in figure 3-51. With a logic 0 (0 volt dc) applied to the input diode, both Q_1 and Q_2 are turned off. As a result, lamps L_1 and L_2 will be turned off thereby indicating that the event has not occurred or has ceased. With a logic 1 (-10 volts dc) applied to the input, both Q_1 and Q_2 conduct heavily and provide L_1 and L_2 with a low impedance ground path. The lamps will now be lighted indicating that the event has occurred. Resistor R_x shunts Q_2 and allows a "keep-alive" current to flow through L_1 and L_2 during the time Q_1 and Q_2 are turned off. This will keep the filaments of L_1 and L_2 warm and thereby keep the initial turn-on current through Q_2 at a safe level.



AM2-15-3

Figure 3-51. Typical Lamp Driver and Indicator Circuit

3-329. METER MODULE CIRCUITS. All meter module circuits are identical. Each meter module contains four identical meter circuits. A typical meter circuit is shown in figure 3-52. The analog input signal is routed to the negative side of the meter via the console patchboard. The analog signal return (ground) line is connected to the positive side of the meter through resistor R_1 and potentiometer R_2 . The d-c meter movements used are edge-mounted panel meters with a current range of 0 to 1 milliampere with an internal impedance of 50 ohms or less. The meters have an accuracy of at least 2 percent. Potentiometer R_2 is used to calibrate the meter for full scale deflection when the output of its associated D/A converter is maximum. The calibration potentiometers are accessible at the rear of the meter module enclosure. It should be noted that each analog signal fed to a meter module by a twisted-pair, shielded cable.

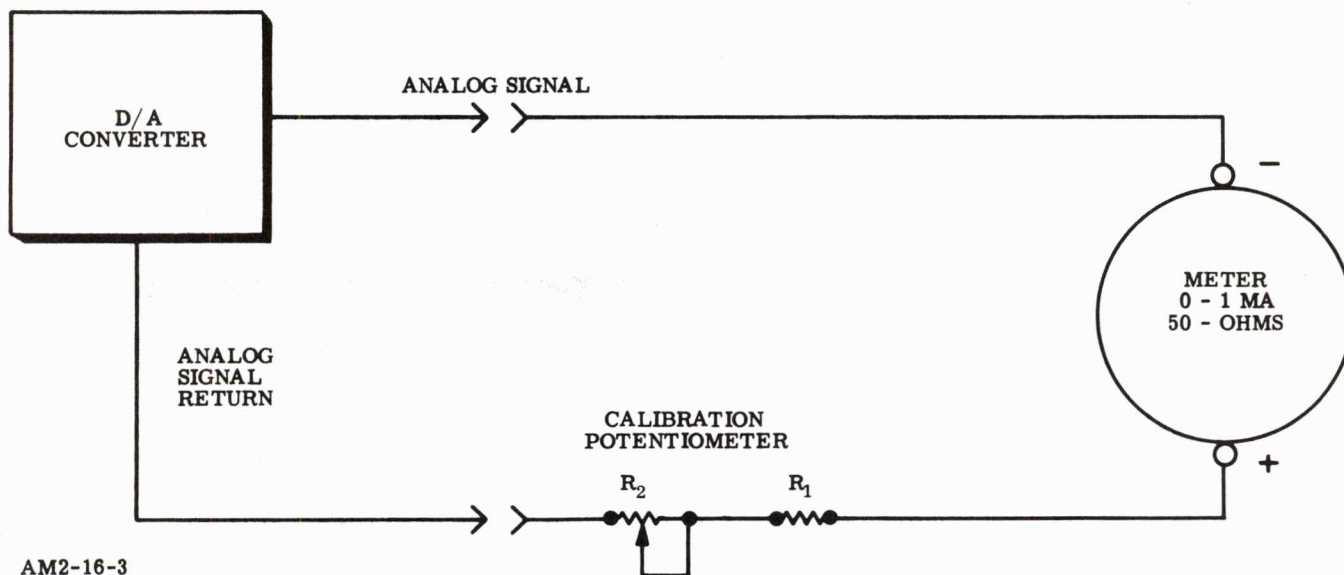


Figure 3-52. Typical Meter Circuit

3-330. EVENT-MODULE CIRCUITS. All event-module circuits are identical. Each event module contains 24 identical indicator lamp circuits. A typical indicator lamp circuit is shown in figure 3-53. Indicator lamps L_1 and L_2 are controlled by the inputs to diodes CR_1

and CR_2 . A small keep-alive current is always flowing through resistor R_x , diode CR_1 , and indicator lamps L_1 and L_2 . The filaments of L_1 and L_2 will be hot but will not glow. Transistor Q_x , part of an associated lamp driver circuit, shunts resistor R_x . When an event occurs, Q_x will conduct and provide a low-impedance ground path. This will cause diode CR_1 to conduct heavily and the filaments of L_1 and L_2 to glow brightly. The increased resistance of L_1 and L_2 , because of the preheat current through R_x , limits the turn-on surge current through Q_x to a safe value. When press-to-test switch S is closed, diode CR_2 conducts heavily causing indicator lamps L_1 and L_2 to light.

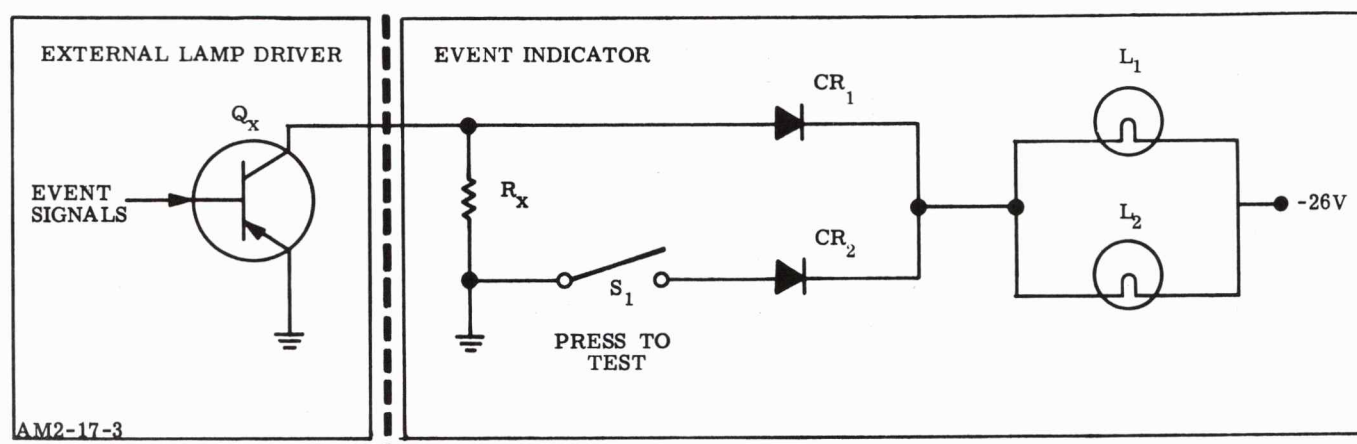


Figure 3-53. Typical Event Lamp Indicator Circuit

3-331. CONVERTER CIRCUITS. The converter assemblies are special purpose and only exist in two of the control consoles: Power and Sequential Console Unit 3 and the Communications Console Unit 19. Each converter assembly contains eight identical converter circuits. Each converter circuit is comprised of a NOR gate and a PI module. A typical converter circuit is illustrated in figure 3-54.

3-332. As is shown in figure 3-54, the converter NOR gate monitors the "1" side of the three most-significant-bit flip-flops of an associated storage register. Whenever the input to the storage register is greater than 32 (000 11111), at least one of the inputs to the NOR gate will be a logic 1. In this case, the NOR gate output will be a logic 0 that will be sent to the associated PI module. The PI module output then will be a logic 1, indicating that the parameter binary monitored is above 12 percent of full scale (32 divided by 256). When the parameter being monitored is below 12 percent, the NOR gate output will be a logic 1 and the PI module output will be a logic 0.

3-333. The output of each converter circuit is treated as an event signal and is fed directly to the control console patchboard. At this point, the converter event signal is sent to an event module on that particular control console and/or to an event display device on the test conductor console via the DDU.

STORAGE REGISTER

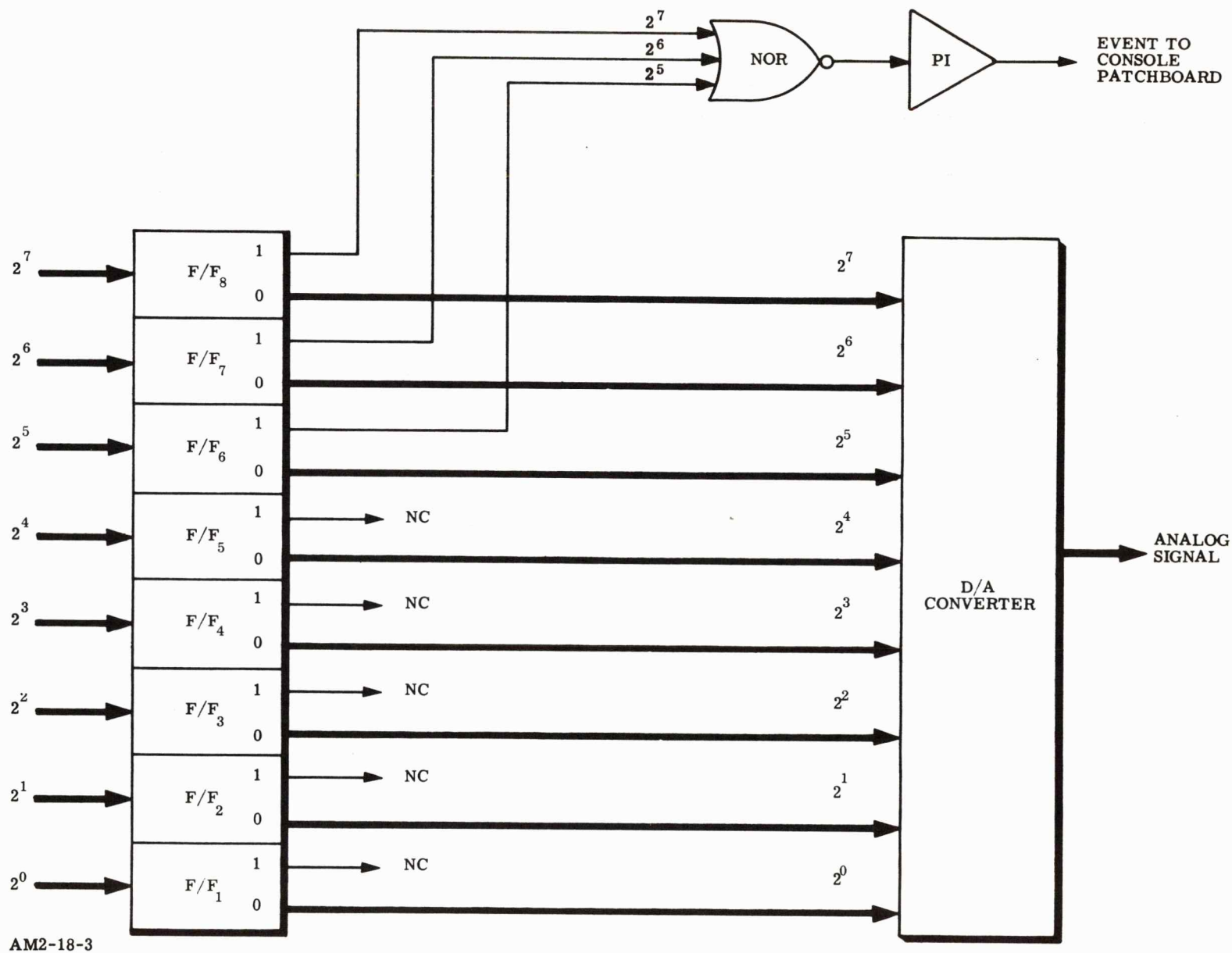


Figure 3-54. Typical Converter Circuit

3-334. EIGHT-CHANNEL ANALOG RECORDER DESCRIPTION. (See figure 3-55.)

3-335. The eight-channel analog recorder is a direct-writing, true-rectilinear, roll-chart recorder. Eight deflection-type analog trace channels, and two on-off event channels are provided. Twelve chart speeds are provided. Writing fluid is force-fed, to pens, from pressurized cartridges. The recorder is capable of frequency response to 200 cycles (flat to 75 cycles).

3-336. Incoming analog signals are applied via an attenuator panel to two channel pen-drive amplifiers. (There are four of these amplifiers to operate eight pens.) The pen-drive amplifiers also receive velocity and position feedback signals from the pen motors to improve linearity and stability. The outputs of the pen-drive amplifiers are applied to the pen motors via a polarity reversal circuit.

3-337. Event (time) signals are amplified by event marker amplifiers and applied to the event marker pen motors.

3-338. 32-CHANNEL EVENT RECORDER DESCRIPTION. (See figure 3-56.)

3-339. The 32-channel event recorder is a deflection-type direct writing recorder, providing on-off indications for inputs from 5 to 60 volts. Two of the channels are reserved for time indication. The recorder will respond to indications occurring at rates up to 100 cycles per second. Writing fluid is supplied to the pens under pressure provided by a built-in pump.

3-340. Incoming signals are applied to pen-drive amplifiers (arranged in four groups of eight each) via transfer relays. These relays provide switching between the input signals and a calibration voltage source. The outputs of the pen-drive amplifiers are applied to the 32 pen-drive motors.

3-341. The calibrator circuits provide either 4 volts dc or 5 volts dc, depending upon whether the HIGH TEST or LOW TEST pushbuttons are depressed. When the HIGH TEST button (applying 5 volts dc) is pressed, the pens should deflect. When the LOW TEST and HIGH TEST buttons are depressed simultaneously (applying 4 volts dc) the pens should not deflect.

3-342. 100-CHANNEL EVENT RECORDER DESCRIPTION. (See figure 3-57.)

3-343. The 100-channel event recorder is a write-nonwrite recorder, providing on-off indicators for 100 event inputs (two of these are reserved for timing signals). Maximum recorder response time is 1.25 milliseconds at maximum chart speed. Recording is done electrically on specially sensitized paper.

3-344. Incoming signals are applied to transistor switch circuits. These circuits control application of high-voltage pulses, from the pulse supply, to the writing styli. The PRF of the high-voltage pulses varies with chart speed.

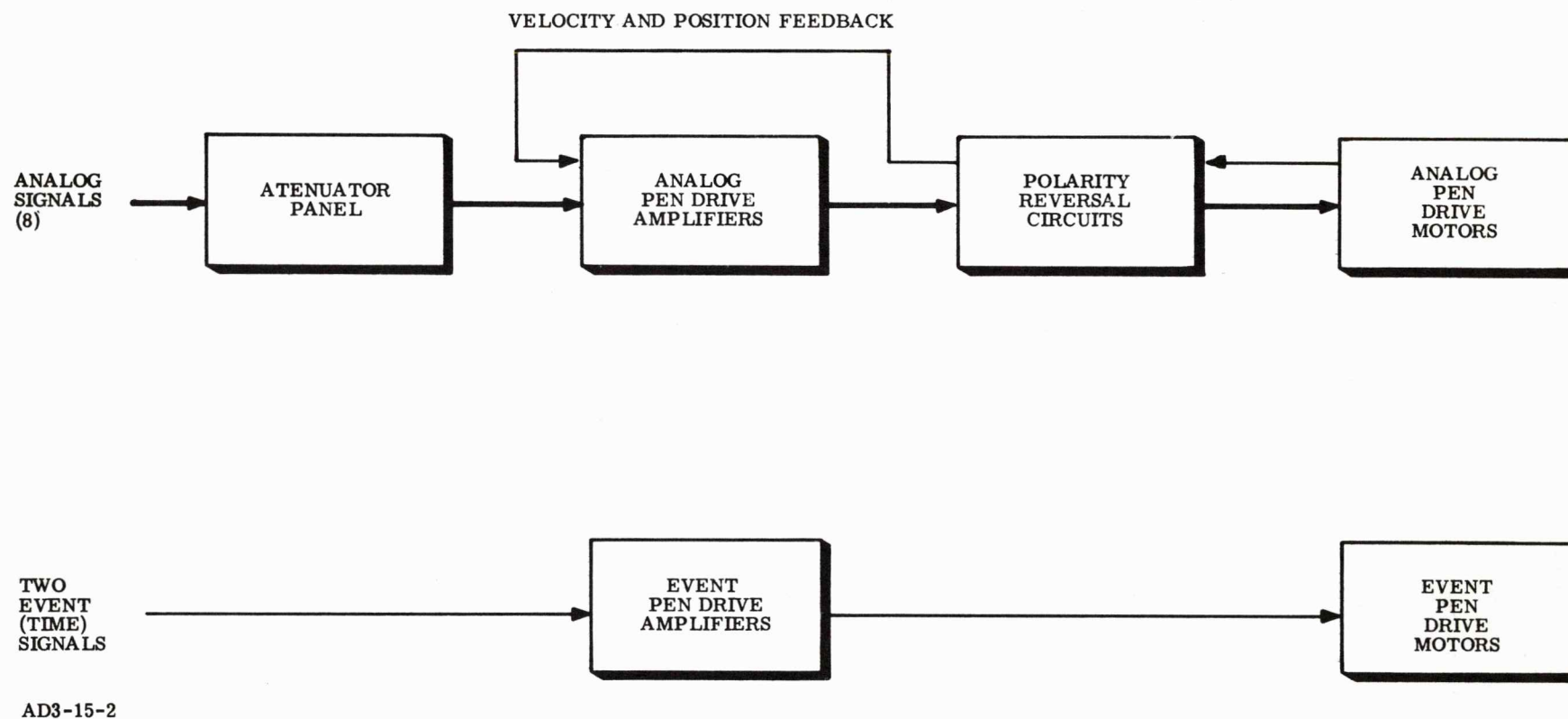
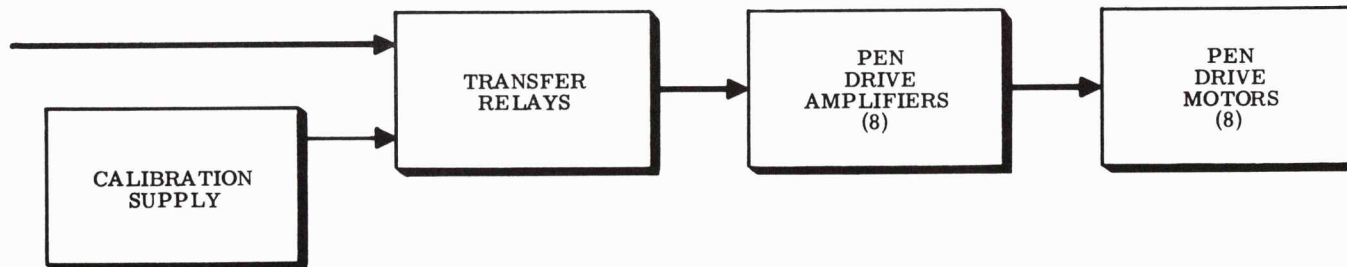
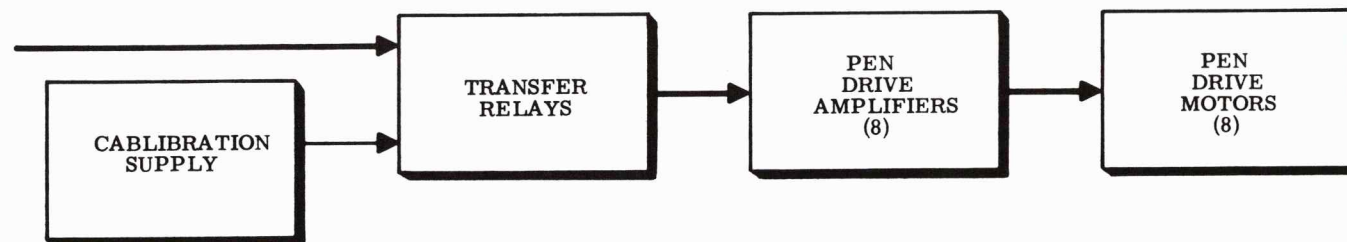


Figure 3-55. Eight-Channel Analog Recorder Functional Block Diagram

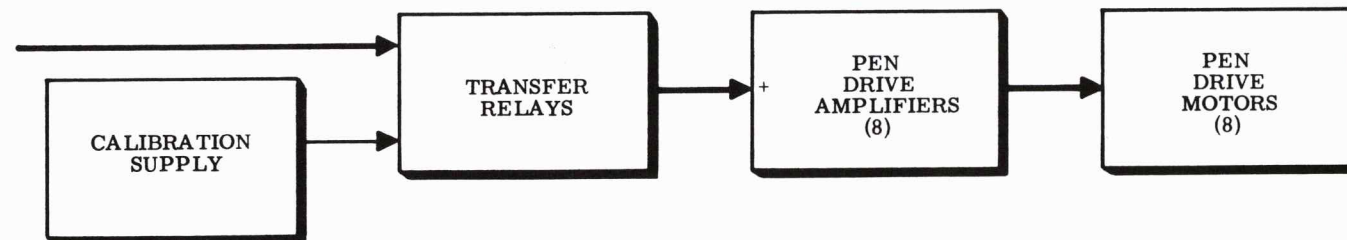
EVENT
INPUTS
CHANNELS
1-8



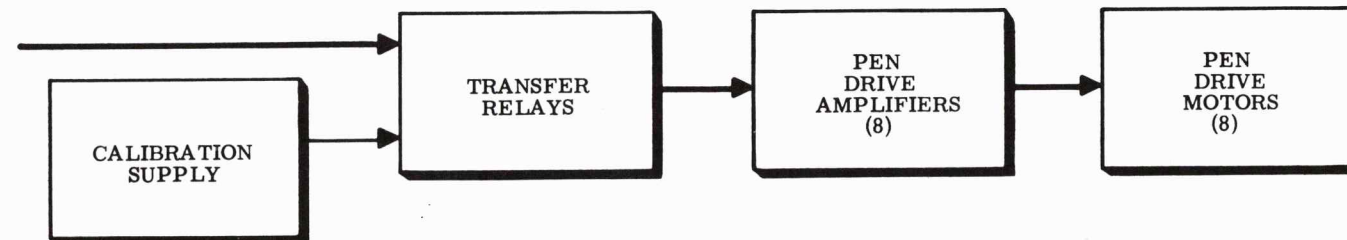
CHANNELS
9-16



CHANNELS
17-24



CHANNELS
25-32

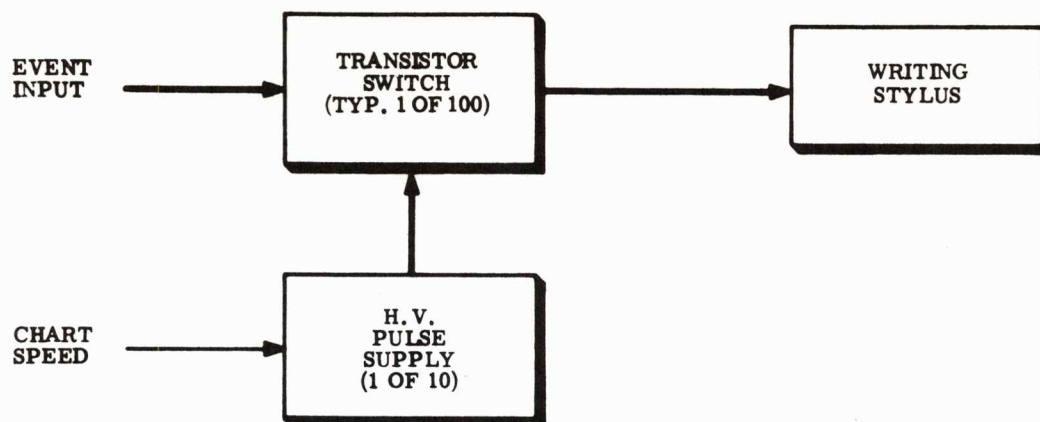


Description

Section III

AD3-16-2

Figure 3-56. 32-Channel Event Recorder Functional Block Diagram



AD3-14-2

Figure 3-57. 100-Channel Event Recorder Functional Block Diagram

3-345. COMPUTER ROOM TEST DATA DISPLAY AND RECORDING EQUIPMENT.

3-346. The units of the ACE-S/C system computer room utilized to process, display, and record analog and addressed digital test data are shown in figure 3-58.

3-347. The Event Distribution Recording and Patching Unit receives addressed test data words from both Decommutator No. 1 and No. 2 via transmission hardlines. The transmission hardlines are similar to those routed from the decommutator units to the DDU in the control room and carry the same information. Logic circuits within the Event Distribution Recording and Patching Unit identify (by address recognition) and store event information contained in the selected addressed test data words received (in a manner similar to that employed in the control room ESDU). These event signals then are fed to a patchboard and are routed to a 100-channel event recorder located in Event Distribution Recording and Patching Unit and/or to an event display module located on the Computer Complex Console. The Event Distribution Recording and Patching Unit also receives analog data signals: 12 from the FM Discriminator Unit, 40 from Decommutator No. 1, and 40 from Decommutator No. 2. All 92 analog signals are received by the Event Distribution Recording and Patching Unit patchboard. At this point, the 12 analog signals from the FM Discriminator Unit are routed to the 36-channel oscillograph contained in the Analog Recorder Unit. Certain of the decommutator analog signals are selected for distribution to the two 8-channel analog recorders in the Analog Recorder Unit and/or to a meter module located on the Computer Complex Console.

3-348. EVENT DISTRIBUTION RECORDING AND PATCHING UNIT.

3-349. The Event Distribution Recording and Patching Unit provides the means to distribute analog and event information within the computer room, select specific event information, and record the selected event information. To accomplish these functions the Event Distribution Recording and Patching Unit contains event processing logic, a patchboard, and a 100-channel event recorder.

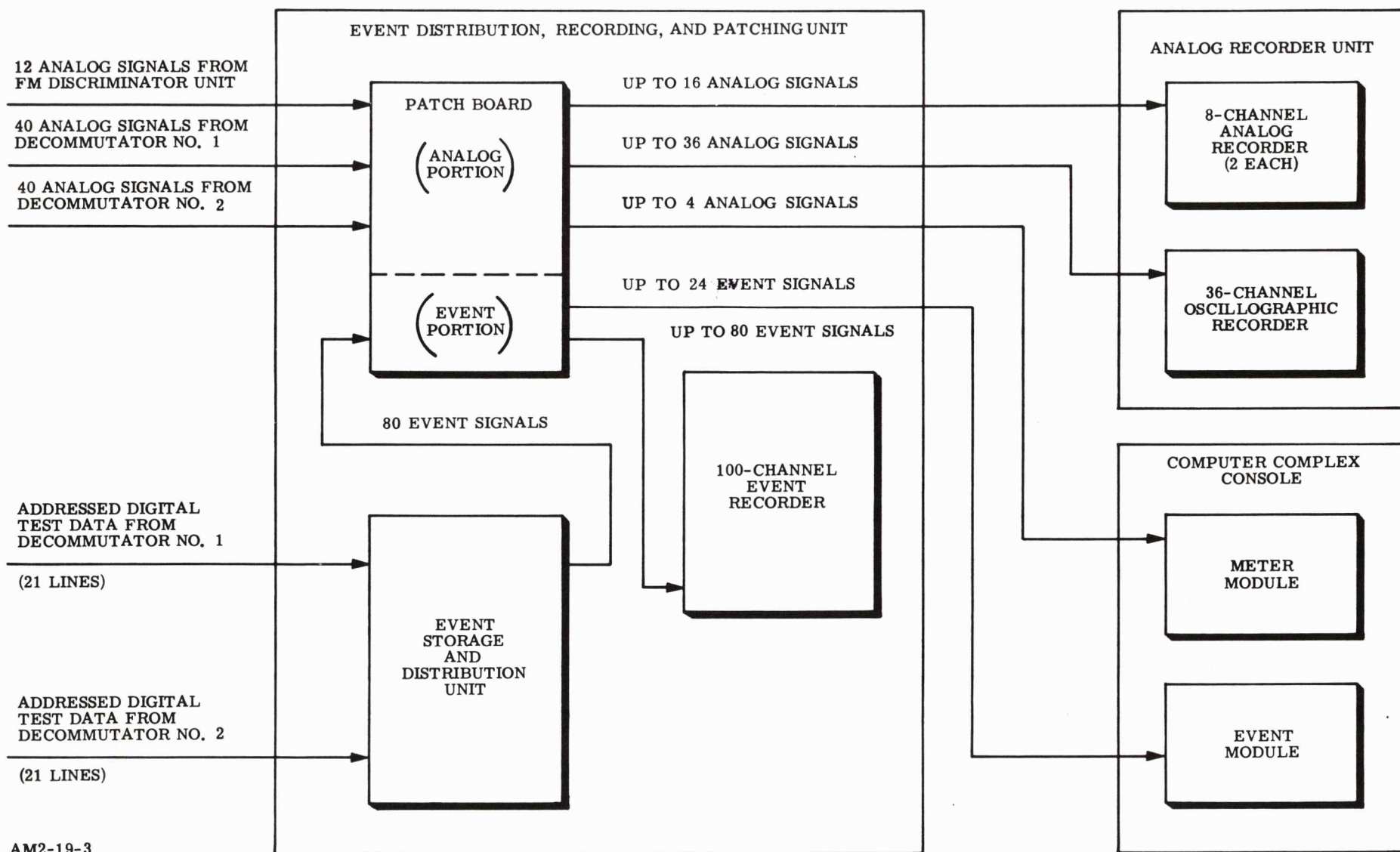


Figure 3-58. Computer Room Test Data Display and Recording Units Functional Block Diagram

3-350. EVENT PROCESSING LOGIC DESCRIPTION.

3-351. The Event Distribution Recording and Patching Unit event processing logic is identical to that employed in the control room ESDU with one exception. The Event Distribution Recording and Patching Unit can only identify and store 10 test data words as opposed to 150 test data words for the control room ESDU. Since each test data word accepted represents eight discrete on/off events, the total number of events stored and distributed by the Event Distribution Recording and Patching Unit is 80. The Event Distribution Recording and Patching Unit event logic circuits are very nearly identical to those employed in the control room ESDU. The first difference is that there are only 10 of each circuit type instead of 150 as with the ESDU. The second difference is that the data bits of each test data word are fed directly to the storage registers, since there are no data-bit fan-out distribution amplifiers used. For a detailed description of the event processing logic circuits refer to paragraphs 3-283 through 3-297, keeping in mind that only 10 test data words are to be processed (not 150) and that there are no data-bit fan-out distribution amplifiers.

3-352. PATCHBOARD DESCRIPTION.

3-353. The patchboard assembly of the Event Distribution Recording and Patching Unit is identical to those used in the control room console. For a more complete description of the patchboard assembly refer to paragraph 3-326.

3-354. 100-CHANNEL EVENT RECORDER DESCRIPTION.

3-355. The 100-channel event recorder is identical to those used in the control room consoles. For a more complete description of the 100-channel event recorder refer to paragraph 3-342.

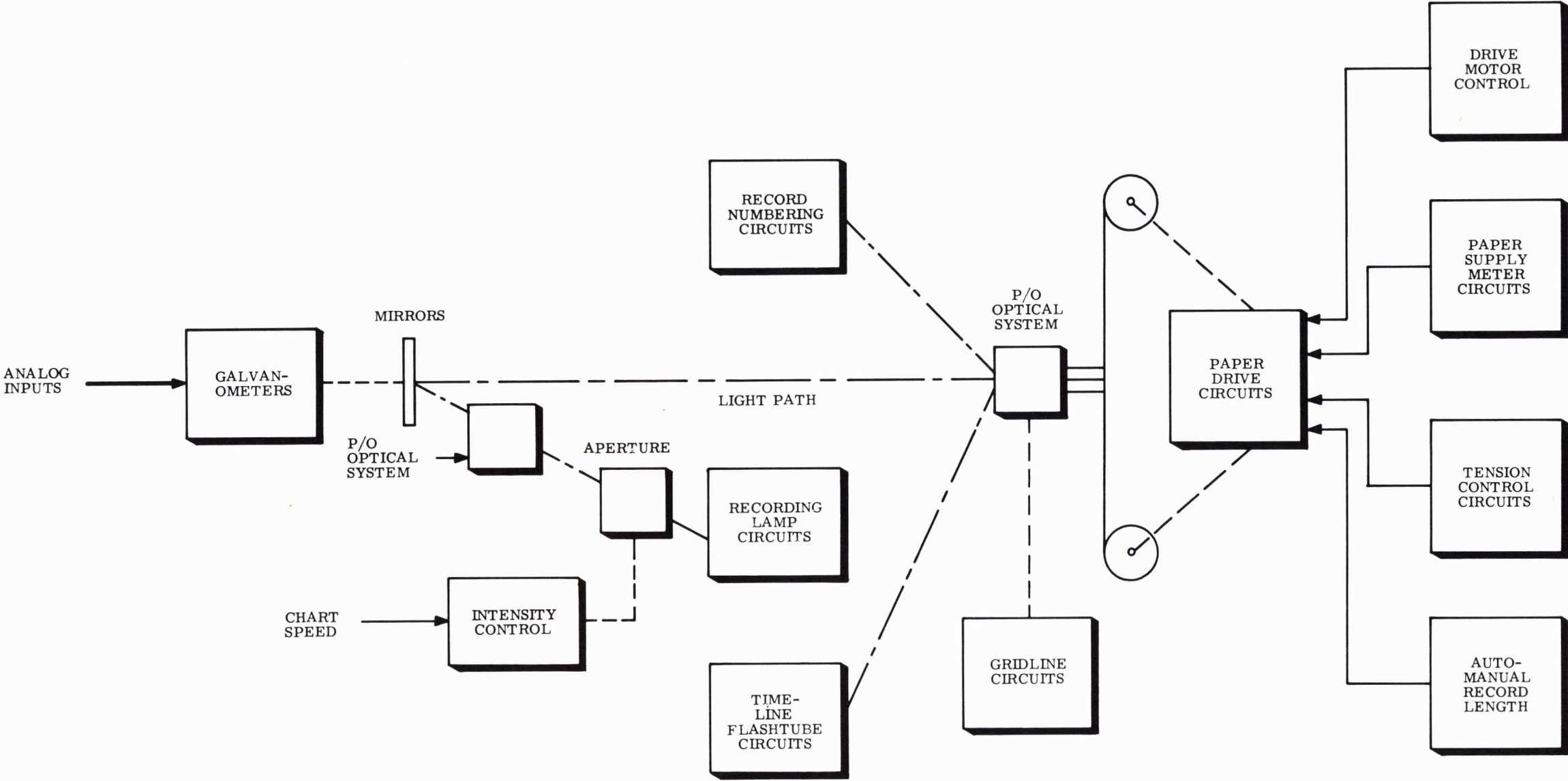
3-356. ANALOG RECORDER UNIT.

3-357. 8-CHANNEL ANALOG RECORDER DESCRIPTION.

3-358. The two 8-channel analog recorders contained in the Analog Recorder Unit are identical to those used in the control room consoles. For a complete description refer to paragraph 3-334.

3-359. 36-CHANNEL OSCILLOGRAPHIC RECORDER DESCRIPTION.

3-360. The 36-channel oscillographic recorder is a high-speed, continuous-write, deflection-type, roll-chart recorder. Analog recordings are made by means of galvanometer mirror-deflected ultra-violet light, from a single high-intensity source on photo-sensitive paper. The paper record resulting requires no chemical developing. The 36-channel recorder contains two categories of equipment: that used to drive and control the recording paper, and the units that generate and control the light used to write on the paper (see figure 3-59).



AD3-20-2

Figure 3-59. 36-Channel Oscillographic Recorder Block Diagram

3-361. PAPER DRIVE FUNCTIONS. The electromechanical drive system drives the paper either in the forward or reverse direction, stops after a preset length of record has been run, and gives a continuous indication of the amount of paper remaining on the supply spool.

3-362. One of the 15 paper speeds may be selected by means of front-panel controls. These controls operate electromechanical clutches in the drive transmission in order to select the proper drive ratios for the desired speed.

3-363. Length of the record desired may be set by means of a front panel control. When the desired record length is reached, the recorder is stopped by means of a microswitch, operated by a mechanical device that monitors paper motion. If continuous recording is desired, the record length circuit is not energized.

3-364. WRITING UNIT FUNCTIONS. A single writing light source provides the necessary high-intensity light to enter a trace on the recording paper. This light is distributed to the various channels by means of mirrors and lenses. The incoming signals drive sensitive galvanometers, that in turn deflect mirrors, to record the incoming waveshapes on the chart paper. Light intensity is varied, by a motor-driven variable aperture, to provide constant trace exposure with variable chart speeds.

3-365. The common light source also supplies light to gridline units that provide a grid exposure on the chart paper for reference purposes.

3-366. Record (trace) numbers are sequentially recorded by firing a flash tube behind a counter and simultaneously interrupting the gridline of the appropriate channel for a moment.

3-367. Time lines at intervals of 0.001, 0.01, 0.1, 1.0, and 10 seconds are recorded across the width of the chart paper by a flash tube and line mask. The interval of the flash tube is controlled either by an interval timer or an external source. Every tenth line is made heavier than the other nine.

3-368. A record numbering circuit is provided. This circuit fires a flash tube each time the RECORD switch is pressed, indicating the start of a record operation. By means of this circuit, a sequential record number, an event marker, and the recorder serial number are recorded on the chart paper.

3-369. COMPUTER ROOM METER AND EVENT MODULES.

3-370. METER MODULE DESCRIPTION.

3-371. The meter module employed in the computer room is located on the Computer Complex Console and is identical to the meter modules employed in the control room consoles. For a detailed description of the meter module refer to paragraph 3-329.

3-372. EVENT MODULE DESCRIPTION.

3-373. The event module employed in the computer room is located on the Computer Complex Console and is identical to the event modules employed in the control room consoles. For a detailed description of the event module refer to paragraph 3-330.

PART 3

ALPHANUMERIC DISPLAY EQUIPMENT

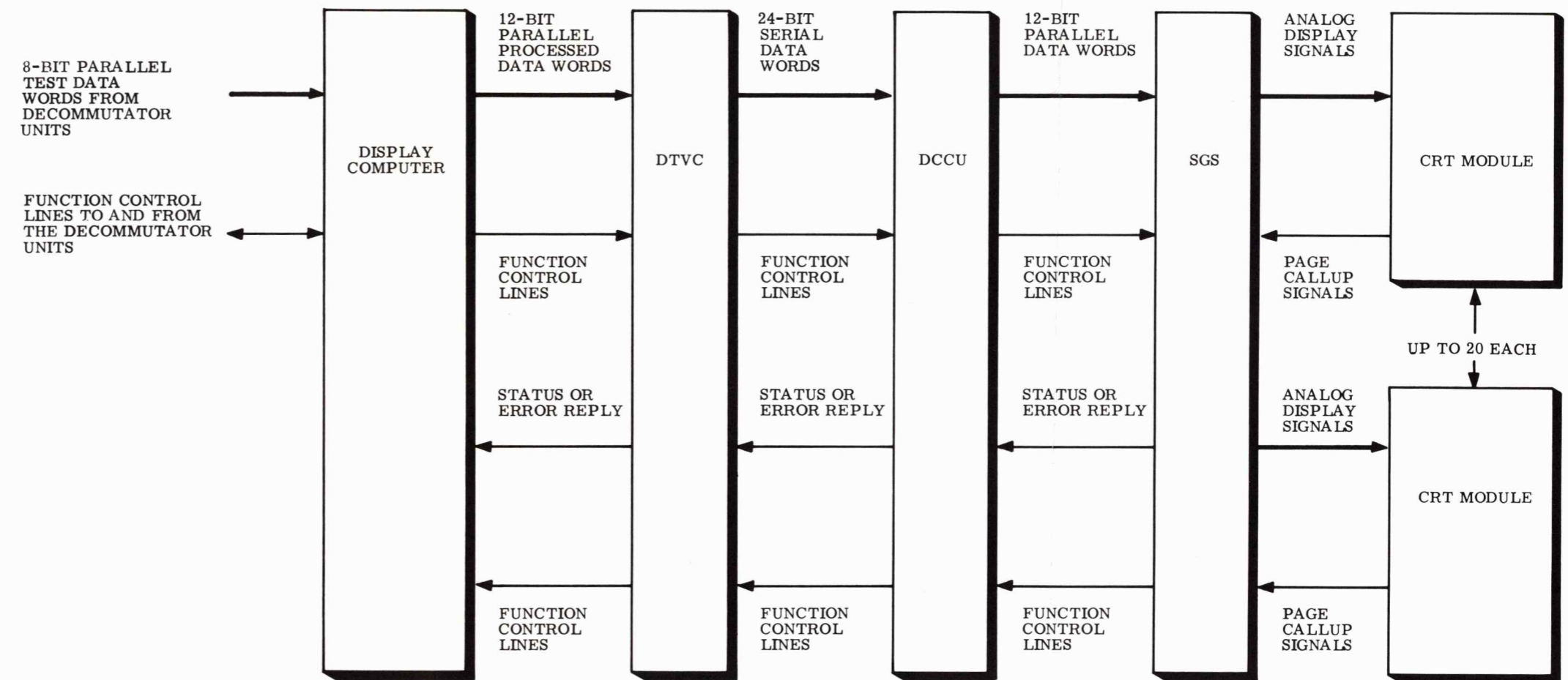
3-374. ALPHANUMERIC DISPLAY EQUIPMENT FUNCTIONS.

3-375. The units comprising the alphanumeric display equipment accept PCM digital test data from the decommutator units, process it, and display the test measurements in real time. At each display location the data is viewed as 26 lines of decimal numbers and engineering units on the screen of a cathode-ray-tube (CRT). A selection capability provided at each display location permits the callup of 40 separate data tabulations, each of which has a 13-line capacity.

3-376. The units of the ACE-S/C system comprising the alphanumeric display units and their functional relation are illustrated in figure 3-60. The functions provided by alphanumeric display units can be divided into three categories: (1) data processing, (2) data transmission, and (3) symbol generation and display. The data processing function is provided by the display computer. Data from the decommutator units is routed to the display computer via the computer I/O Module. The primary programmed operations of the display computer are:

- a. Acquisition and formatting of data for processing.
- b. Comparing any word (or words) with programmed values to determine whether the data is within predetermined limits.
- c. Conversion to engineering units, both linear and polynomial functions, using curve fitting techniques.
- d. Compare event status with previous status received.
- e. Prepare and format processed data for display.

3-377. The computer processed data output (instructions, parameter value, and associated address) is fed to a DTVC in parallel format. The DTVC operates in conjunction with a Digital Communications Control Unit (DCCU) to provide a data transmission to the display producing unit. The processed data received by the DCCU is fed to the Symbol Generator and Storage



AM2-34-3

Figure 3-60. Alphanumeric Display Units
Functional Block Diagram

(SGS) Unit. The SGS operates in conjunction with CRT Modules located in certain control consoles to provide the symbol generation and display function. The SGS stores the incoming data and converts the data into alphanumeric characters for display on the requesting CRT Modules.

3-378. DATA PROCESSING FUNCTIONS.

3-379. The data processing function is supplied by the display computer located in the ACE-S/C computer room. The display computer is a stored-program, high-speed, single-address, parallel-operation, modular, electronic data processor. The primary functions of the computer include data reduction, analysis, and preparation for display of the test data derived from spacecraft testing programs.

3-380. Incoming PCM test data is read into computer memory via an I/O Module and is then processed in preparation for display on an alphanumeric CRT display unit. Processing of the incoming PCM data includes:

- a. Selection of specific data from the incoming data.
- b. Comparison to determine whether the measurement represented by a digital word is within preprogrammed limits.
- c. Conversion to engineering units.
- d. Conversion and formatting test data for display.
- e. Storage of selected parameters for trend analysis, etc.

3-381. In addition to driving the alphanumeric CRT displays, the display computer also supplies a number of peripheral units with processed data. The peripheral units include a high-speed printer, an X-Y Plotter, tape unit, Card Punch, and a Typewriter. These units may be used for the setup and checkout of the computer complex in preparation for a spacecraft testing sequence, as well as provide a display and recording capability during the actual test operations.

3-382. The general functions and operations of the display computer are best described in terms of the computer program. The space available here does not permit a complete description of all the programs that will be available. Instead, the program categories are given and briefly described in the following paragraphs. It is intended that these brief descriptions will clarify the role of the display computer in the display and recording equipment of the ACE-S/C system. For a description of computer machine operation and basic theory refer to Section II of this manual.

3-383. SUPERVISORY EXECUTIVE PROGRAM. The supervisory executive program (SEP) organizes the display computer (as well as command computer) program in preparation for processing test data. The SEP is recorded on a test file tape, along with certain common

programs (such as ACE-S/C self-test programs), all display executive programs that are part of a test series, spacecraft test subroutines, and test parameters.

3-384. This test file tape may be placed on a command computer tape unit. The command computer then interrupts the display computer by means of a SEP bridge punched card placed in the display computer card reader. The SEP portion of the test file tape then selects a display computer executive program and its appropriate subroutines and parameters in the proper order and stores them in the display computer memory bank zero. Communication between command and display computers then ends until another spacecraft test (requiring a new display computer executive program, etc.) is to be instituted, or until one of the common programs is to be instituted. The display computer is now effectively under control of the display computer executive program in its memory. To change to a new spacecraft test simply requires that the operator call SEP to load the new display computer program, subroutines, and parameters into the display computer memory. Prior to or during loading, any display computer parameter on the test file tape may be changed by using change cards. Changes called for by the change cards are not limited to load time but may be made at any point during the test sequence.

3-385. An ACE-S/C self-check program, included as part of the SEP, is readily accessible to the display computer. This self-check program provides the assurance that the required ACE-S/C subsystems are in the Ready Mode prior to the actual test run and that they have the proper operational status while a test is in progress. Indications of a no-go nature are provided by this program, along with sufficient additional information to enable program call-up of selected diagnostics for prompt decision as to corrective actions.

3-386. EXECUTIVE ROUTINE. It is the purpose of this routine to control the sequence of data processing by the display computer. This routine may be divided into three major sections:

- a. Primary initialization.
- b. Subroutine linkage.
- c. Summary filing.

3-387. Primary initialization insures that all registers, counters, and other indexes used by the display computer executive routine are cleared and reset to the start conditions. This prepares the display computer for an interrupt from the decommutator units to commence the loading of PCM test data for subsequent processing. The subroutine linkage portions of the executive routine consist of fixed sets of instructions that control the exit from one subroutine and the entry to the next subroutine. By using the subroutine linkage instructions, the processing order is flexible and is easily changed, since only the linkage routines need to be

rearranged to create a new and different subroutine processing order. Before the entry to a subroutine, the subroutine linkage instructions supply the new subroutine with the address of the first parameter for the data word to be processed by that particular subroutine. Upon exit from the subroutine, the linkage routine determines if there are any more data words to be processed by the subroutine and will cause the subroutine to repeat if necessary. Processed data, derived from display computer subroutine operations, is stored and transmitted to the appropriate peripheral units under the control of the summary filing portions of the executive routine.

3-388. In the following paragraphs, thumbnail-sketches of some typical display computer subroutines are given. It is not the intent to list and describe every subroutine available in detail, but rather to demonstrate the purpose of the display computer in the alphanumeric display equipment and its function as related to the overall ACE-S/C system.

3-389. PCM TELEMETRY DATA READ-IN SUBROUTINE. It is the purpose of this subroutine to allow the entry of PCM digital test data from the decommutator units into the display computer memory for further processing. The data input sequence is initiated by an interrupt signal from the PCM decommutator equipment. The incoming PCM data is in the form of eight-bit parallel words and are buffered into two separate areas of auxiliary memory. One prime frame of PCM data (512 eight-bit words) is read in at a time. There are 50 such prime frames to be read in each second. Figure 3-61 illustrates the read-in process. The following steps are required for a typical read-in process:

- a. Read first prime frame of 512 words into memory bank 02 in address locations 17000 through 17777.
- b. Begin read-in of second (even numbered) prime frame of 512 words into memory bank 04 in address locations 17000 through 17777, and start processing data in memory bank 02.
- c. Begin read-in of odd-numbered prime frame of data into memory bank 02, and start processing data in memory bank 04.
- d. Return to step b.

3-390. This switching type of buffer allows time to transfer selected data to be processed, from one input area to a relocatable data table, while filling the other input area. Identification of data to be transferred is based primarily on the PCM data prime frame count. This program subroutine tests for synchronization in the last input area to receive test data. If an in-sync condition exists, all data to be processed is transferred to a relocatable data table. If a lost-sync condition exists, the relocation of data is bypassed and a flag is set. A real-time clock reading is stored in the computer so that a specific time can be related to each data prime frame received.

3-391. ENGINEERING UNITS SUBROUTINE. It is the purpose of this subroutine to convert the received PCM test data to the proper engineering units, determine analog percentages, and make limit checks. The data is processed in one of three ways:

- a. Type A - the average of every N^{th} point.
- b. Type B - process every N^{th} point.
- c. Type C - compare a data point with a constant to check difference.

3-392. Prior to the read in of any PCM test data, all the necessary information required to convert the incoming PCM test data associated with a specific measurement will be read from magnetic tape and stored by the display computer. This information consists of a polynomial (of appropriate degree), the coefficient constants of the polynomial, the location of the binary points of the coefficients, the binary point of the upper and lower limits, and the specific upper- and lower-limit values. The polynomial and its associated coefficients are the mathematical expression for a curve to which the PCM data is fitted. The general polynomial form is given as:

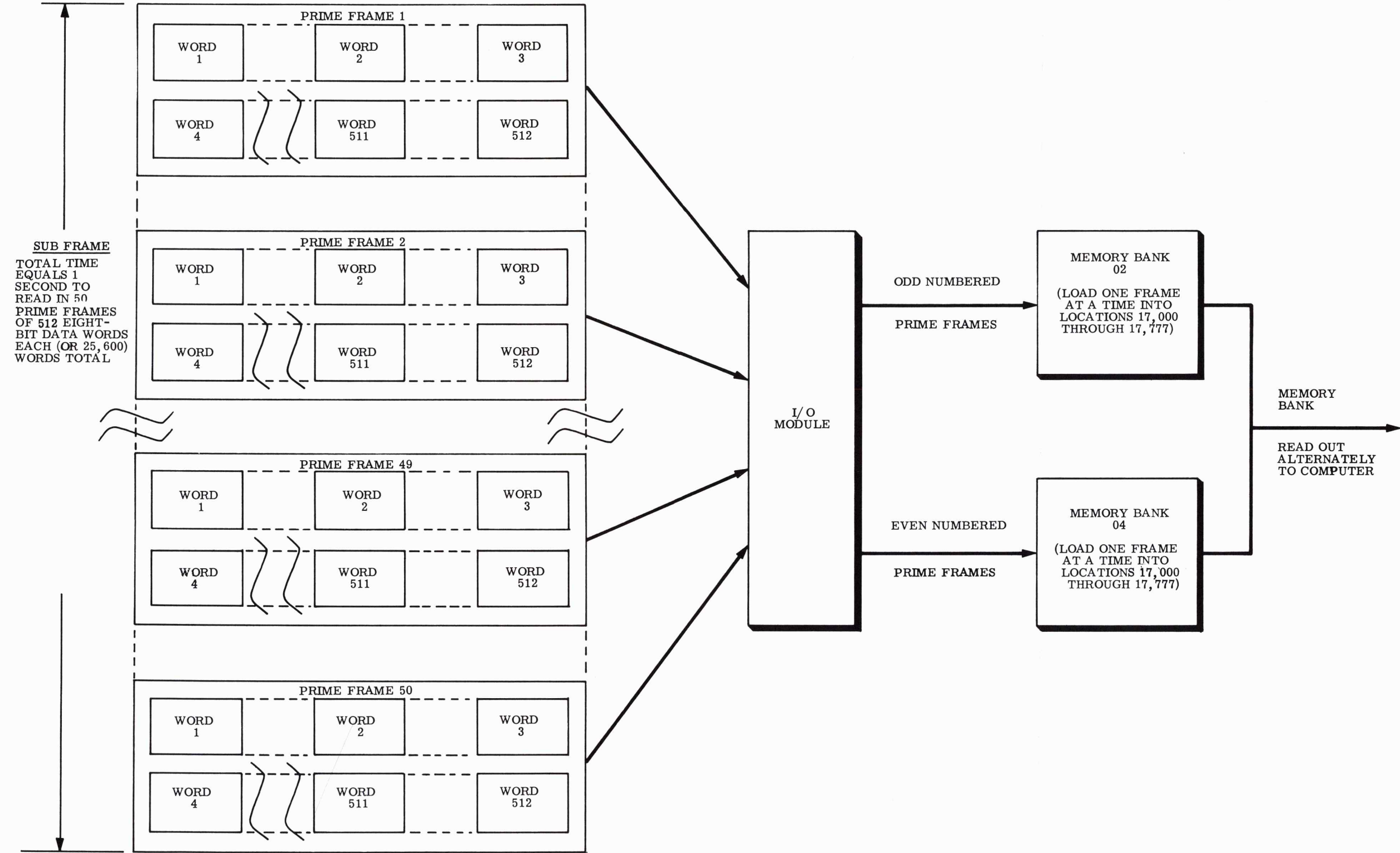
$$A_0 + M(A_1 + M[A_2 + M(A_3 + M[A_4 + A_5M])])$$

where A_0 through A_5 are the coefficients and M is the eight-bit PCM data word associated with the measurements.

3-393. The display computer solves the polynomial expression and generates one 12-bit word. This 12-bit word is a solution to the polynomial expression and is in engineering units. The engineering units are appropriate for the measurement that was represented by PCM test data input. The engineering unit value for the measurement is stored and can be transmitted to the SGS for display on a CRT.

3-394. Following the conversion to the appropriate engineering unit value, the display computer may check this value against preprogrammed limit tolerances. As was previously stated, the specific upper- and lower-limit values of each measurement to be processed are read into the display computer prior to acceptance of any PCM test data. First the measurement value is compared with the upper-limit value and then the lower-limit value. If the measurement value is within the tolerance limits, no further computations are made. If an out-of-tolerance condition is indicated, the display computer will flag the measurement value and cause this value to blink when displayed on a CRT.

3-395. Certain PCM data words are converted to engineering units and then only checked for an in- or out-of-limits indication. These measurement values are compared with the maximum and minimum values of operational limits in percent of full scale. The measurement values are compared, each time they are received, with the previous value to determine if



AM2-35-3

Figure 3-61. PCM Data Read-In Functional Block Diagram

they are going out of limits or coming into limits. Each time a measurement value changes status (goes out of limits or comes into limits) it is stored for transmission to the SGS and then to a CRT display.

3-396. EVENT STATUS CHECK SUBROUTINE. It is the purpose of this subroutine to extract specific event information from certain incoming PCM test data words and to determine its state and disposition. Based on the bit position of the event, the display computer extracts the bit from the PCM data word. The computer then compares the state of this bit with the previous subframe state. If a transition has occurred, the present state (on/off condition), the time of transition, and a flag indicating that a transition has occurred are stored for output to magnetic tape recording and printout. The programmer also can cause the present on/off condition to be sent to the SGS and then to a CRT display. If a transition has not occurred, the present state of the event will not be updated on the CRT display since the previous state is still valid.

3-397. OUTPUT DATA FOR CRT DISPLAY SUBROUTINE. It is the purpose of this subroutine to output (via an external buffer) the information required to update the SGS memory and thus the CRT displays. This subroutine is used whenever an information updating is required for one of the following types of CRT displays:

- a. A display of the engineering units of a measurement.
- b. A display of a measurement requiring only an in- or out-of-limits indication.
- c. A display of an event requiring only an on/off or open/closed type of indication.
- d. The display of an event and the time a transition of state occurred.
- e. The display of decommutator loss of sync or its removal.
- f. Any other display of parameters deemed necessary by the programmer to fulfill the current test requirements.

3-398. The data that the display computer has identified and processed is stored in the common output area of memory for scope updating as required. By means of a parameter table look up, the stored parameters are identified fully and the CRT character code and positioning codes are prepared. The display will output the stored parameter values, CRT positioning codes, and any other instructions necessary for proper CRT display as blocks of data. The blocks of data are groups of sequentially outputted 12-bit parallel words. The type of information contained in these sequential words is given in table 3-9.

3-399. STORE INFORMATION FOR PERIODIC OUTPUT SUBROUTINE. It is the purpose of this subroutine to store the processed data and its associated time codes, in/out limit indications, CRT display X and Y coordinates, status, and engineering unit values. This data is converted to a form appropriate for printing or plotting and is stored in a common output

area. The data is also stored in the common output memory area in an unprocessed form for output to magnetic tape recorders. This data is transmitted to the appropriate peripheral units at the end of each prime frame (i.e., at the completion of processing 50 subframes) which occurs once every second.

Table 3-9. Display Computer Output Word Content

WORD TYPE	CONTENT
Engineering Units	<ul style="list-style-type: none"> a. CRT X and Y display coordinates. b. Blink or no blink depending upon current limits and status. c. A minus symbol for negative values (- X), or a blank space for positive values (X). d. The engineering units character code with a decimal point override. (Number of characters varies depending upon the updating requirements.)
In- or Out-of-Limits Indications	<ul style="list-style-type: none"> a. CRT X and Y display coordinates. b. Either a blink or no-blink flag depending upon current limits. c. The measurement event and time of transition.
Event	<ul style="list-style-type: none"> a. CRT X and Y display coordinates. b. Blink or no-blink flag depending upon status. c. The event name and status; i.e., OFF or ON, CLOSED or OPEN.
Event and Transition Time	<ul style="list-style-type: none"> a. CRT X and Y display coordinates. b. Blink or no-blink flag depending upon status. c. Event name and status; i.e., OFF or ON, CLOSED or OPEN. d. Time of transition to current state.
Event and Duration Time	<ul style="list-style-type: none"> a. CRT X and Y coordinates. b. Event name and status; i.e., OFF or ON, CLOSED or OPEN. c. Length of time the event has maintained its current status and the time when the event entered the current status.
Lost Sync	<ul style="list-style-type: none"> a. CRT X and Y coordinate. (The X coordinate remains the same for all pages of data. The Y coordinate changes by a fixed amount for each page of data.) b. Character code to display the words LOST SYNC at all the appropriate CRT line locations.

3-400. CALL-UP ALTERNATE CRT DISPLAY DATA SUBROUTINE. After each subframe is processed, a check is made by the display computer to see if a call-up of alternate display data has been requested. When a call-up has been requested and is recognized by the display computer, the time of call-up is determined and is used to search for the alternate displays requested. At the completion of the read-in of the alternate displays and the associated parameters and data, the new CRT character display codes are stored and transmitted to the SGS in the same manner as normal processed data.

3-401. DATA TRANSMISSION FUNCTIONS.

3-402. The transmission of data between the display computer and the SGS is facilitated by the DTVC and the DCCU. The functional relationships of the units comprising the data transmission link are illustrated in figure 3-62. The DTVC is an inter-computer communication device that provides long-distance serial data transfer at high speeds under computer program control. The DCCU is identical to the DTVC, except that it contains an additional control unit adapter. The added control unit adapter allows the DCCU to act as a computer interface with the SGS. This eliminates the need for a remote computer at the SGS input and allows the display computer to communicate directly with the SGS via the DTVC/DCCU serial data link over extended distances.

3-403. The display computer, operating under program control, establishes communication with the DTVC and DCCU combination by means of control function lines and 12-bit EF codes. The control function lines constitute the Function Ready, Output Resume, Information Ready, and Input Ready control signals. The EF codes are transmitted to the DTVC/DCCU via the normal computer data output lines and provide the function of unit selection, mode selection, and data channel selection.

3-404. During all idle periods, the DTVC is in a Monitor Mode of operation awaiting instruction from the display computer. In like manner, the DCCU is in a Select-to-Receive and Interrupt Mode awaiting the receipt of instructions from the display computer via the DTVC. The DTVC and DCCU operate essentially in a back-to-back manner in that the DTVC transmission output loop is always fed to the DCCU receive loop and vice versa.

3-405. The DTVC receives EF codes and data words from the display computer in the form parallel of 12-bit words. To transfer data via the DTVC/DCCU to the SGS, the display computer first establishes communication with the DTVC, then with the DCCU, and finally with the SGS. In effecting a data transfer, the first parallel 12-bit word sent out from the display computer is an EF code that addresses the DTVC and selects the proper DTVC operation for succeeding transmissions. The following sequential steps are required for the initial transfer

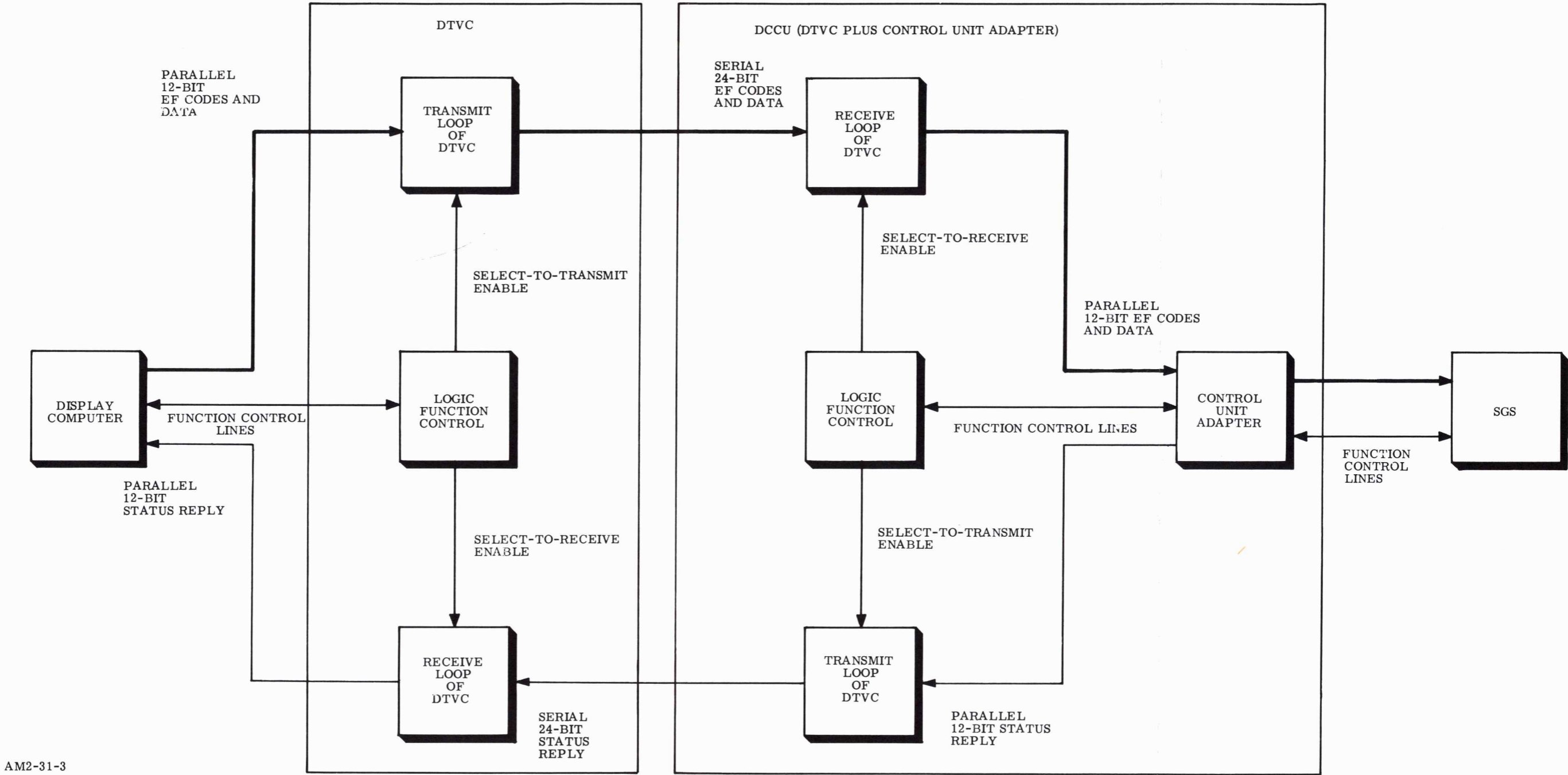
between the display computer and the DTVC:

- a. The display computer transmits a parallel 12-bit EF code over normal output data lines to the DTVC.
- b. The display computer raises the Function Ready control line, allowing the DTVC to recognize and accept the EF code.
- c. The DTVC translates the EF code received and prepares to transmit the display computer outputs to follow to the DCCU.
- d. The DTVC notifies the display computer that it is ready to receive data by raising the Output Resume control line.
- e. The display computer recognizes the Output Resume by lowering the Function Ready control line. The DTVC responds by lowering the Output Resume control line.

3-406. At this point, the DTVC is in the proper mode to allow the display computer to communicate with the DCCU via the DTVC. The second parallel 12-bit word transmitted by the display computer is another EF code to the DCCU via the DTVC. The DTVC treats this EF code as a data word. The EF code is converted from parallel format to serial format by the DTVC and is transmitted to the DCCU as a redundant serial 24-bit, split-phase data word. (The received 12-bit word is transmitted serially twice.) As previously mentioned, the DCCU is in a Select-to-Receive and Interrupt Mode upon initial receipt of signals from the DTVC. The DCCU accepts the second EF code word from the display computer and from it determines the type of operation the control unit adapter is to perform.

3-407. The most significant six bits of the received serial 12-bit EF code designate the interrupt word for the DCCU. The least significant six bits of the code designate the type of operation the control unit adapter portion of the DCCU is requested to perform. The function codes and bit weight of the most significant six bits received and the least significant six bits received are given in table 3-10. Once the DCCU has accepted and translated the second EF code that the display computer has issued, the DCCU is prepared and ready to transmit any subsequent data issued by the display computer to the SGS.

3-408. The third parallel 12-bit EF code is transmitted by the display computer to the DTVC, is converted to a redundant 24-bit serial word by the DTVC, and is retransmitted to the DCCU. The DCCU treats the EF code word as a function control word for the SGS. The DCCU converts the received serial EF code to a parallel 12-bit EF code word. The control unit adapter transmits the parallel 12-bit word to the SGS along with the raising of a Function Ready control line. The Function Ready signal enables the SGS to accept the EF code word. Upon accepting and translating the EF code word, the SGS replies by raising the Output Resume control line. The control unit adapter responds by lowering the Function Ready control line which in turn causes the SGS to lower the Output Resume control line.



AM2-31-3

Figure 3-62. DTVC/DCCU Transmission Link Functional Block Diagram

Table 3-10. External Function Codes Received by DCCU

BIT CODE	INTERPRETATION
<p>MOST SIGNIFICANT SIX BITS</p> <p>6</p> <p>7</p> <p>8</p> <p>9</p> <p>10</p> <p>11</p>	<p>If bit No. 6 is a 0 - DCCU address 40 interrupt, output operation.</p> <p>If bit No. 6 is a 1 - DCCU address 30 interrupt, input operation.</p> <p>If bit No. 7 is a 0 - no function word follows interrupt word.</p> <p>If bit No. 7 is a 1 - it indicates that a function word follows the interrupt word.</p> <p>If this bit is present (i.e., if it equals a 1), the status of the DCCU will be transmitted to the computer after the output operation is completed.</p> <p>If bit Nos. 6, 7, and 9 are 1's, the input operation is limited to one word. It may be noted here that bit No. 9 will always be 0, when used in this capacity.</p> <p>Not used in ACE-S/C, always 0.</p> <p>If a 1, a master clear will be generated for the DCCU (dependent on switch selected options).</p>
<p>LEAST SIGNIFICANT SIX BITS</p> <p>(LSB is on Right-Hand Side)</p> <p>000 000</p> <p>000 010</p> <p>000 100</p> <p>000 110</p>	<p>Output - transfer each word in the block of serial data following the command to the SGS. Return to the Monitor Mode after interblock null is detected.</p> <p>Function Output - transfer the function word, which follows the command on the serial channel, to the SGS. Then transfer the blocks of data following the function word to the SGS. Return to Monitor Mode at end of block.</p> <p>Output Reply - transfer data as in 000 000, then transmit DCCU status (one word) over serial channel to display computer.</p> <p>Function Output Reply - transfer a function word and blocks of data, then transmit DCCU status (one word) over serial channel to display computer.</p>

Table 3-10. External Function Codes Received by DCCU (Cont' d)

BIT CODE	INTERPRETATION
1XX XXX	Master Clear - Master Clear the DCCU.
001 011	Function Input one word - return to Monitor Mode after one-word input. Used for status input.

3-409. The transfer of data between the DCCU and the SGS is identical to that between the display computer and the DTVC. The fourth word and all subsequent data words of a block of data to be transmitted by the display computer are first transmitted to the DTVC in parallel form, converted to serial form, and transmitted by the DTVC to the DCCU. The DCCU converts the data to parallel form and transmits it to the SGS. The SGS loads the block of data received into memory locations under the instructions received via the data link from the display computer. The data transfers will continue as described above until an interblock null is detected or until an error is detected.

3-410. Upon detecting an interblock null (i.e., a wait period between blocks of data), the DCCU returns to the Monitor Mode of operation and awaits another EF code from the display computer. When another block of data is to be transferred to the SGS from the display computer via the DTVC/DCCU transmission link, the entire transmission sequence previously described will be repeated.

3-411. To detect the possibility of transmission errors, the DCCU makes a bit-by-bit comparison of the first 12 serial bits received, with the redundant second 12 serial bits received. If, during the transmission of data or EF code words, an error is detected, the DCCU will enter a hold state and prevent any of the erroneous data from being transferred to the SGS. As soon as the first interblock null is detected, the control unit adapter places the DTVC portion of the DCCU into a Select-to-Transmit Mode. The DCCU then will transmit a 12-bit code word to the display computer, via the DTVC, that conveys the status and error detected by the DCCU. The display computer accepts the 12-bit code word, translates it, and determines the status and/or error indications. The display computer will then retransmit the original block of data a preprogrammed number of times. If for each time the display computer retransmits the block of data the DCCU returns the same status and/or error indicating code, the display computer enters into a programmed maintenance routine in an attempt to determine the exact nature of the problem. The bit weight and assignment for the DCCU status reply is given in table 3-11.

Table 3-11. DCCU Status Reply Code

BIT NO.	INTERPRETATION WHEN BIT IS A LOGIC 1
0	DCCU detected a transmission error
1	(Not used)
2	(Not used)
3	(Not used)
4	(Not used)
5	No data has been received
6	SGS does not respond to commands
7	Hold set
8	(Not used)
9	(Not used)
10	SGS does not generate an Output Resume signal
11	DCCU interrupt

3-412. As an aid to maintenance, the DTVC and the DTVC portion of the DCCU both contain test simulators. Each test simulator provides the means to select and generate selectable word patterns that may be transmitted over the serial-bit communications link without instruction from the display computer. This leaves the display computer free to operate while maintenance is being performed on either the DTVC or DCCU. By using the simulator, the error detector, and an oscilloscope, the receive logic loop or the transmit logic loop can be checked under conditions that approach actual operation. The simulator also can be used to set all communication channel parameters and margins prior to actual operation. A DTVC can be placed into the Maintenance Mode of operation by means of front panel controls located on each DTVC. When a DTVC is in the Test Mode, its associated test simulator is operative. By means of 12-bit select switches located on the simulator front panel, the operator may set in any 12-bit word necessary for test or maintenance purposes.

3-413. SYMBOL GENERATION AND DISPLAY FUNCTIONS.

3-414. The generation and display of symbols representing display computer processed data is provided by the SGS unit (located in the Terminal Patch Facility room) and by the remote

CRT display modules (located in certain of the control consoles in the control room). The SGS unit accepts and stores 12-bit instruction words and data words from the display computer via the DTVC/DCCU data transmission link. The SGS converts the data words to analog signals and transmits this information to the CRT modules where the data may be monitored by certain of the control console operators. The information displayed on the CRT's is dependent upon character codes and memory instructions received from the display computer. The character codes determine the character (alphabetical letter or number) that is to be displayed. The memory instructions received determine the SGS memory locations into which the display computer character codes will be stored. The SGS memory location determines the position on the screen of the CRT that the character is to appear. All displays on the screens of the CRT modules are the result of analog output functions of the SGS. The circuits generating and controlling the displays are located in both the SGS and the CRT modules. The SGS can supply up to 20 CRT modules with display information.

3-415. DTVC AND DCCU EQUIPMENT DESCRIPTION.

3-416. DTVC DESCRIPTION.

3-417. The DTVC used in conjunction with the display computer is identical to the DTVC's used in conjunction with the command computer. For a detailed description of DTVC machine operation and basic theory, refer to Section II of this manual.

3-418. DCCU DESCRIPTION.

3-419. The DCCU is identical to the DTVC except that it incorporates an additional assembly called the control unit adapter. For a detailed description of the DTVC portion of the DCCU with respect to machine operation and basic theory, refer to DTVC description given in Section II of this manual. The control unit adapter machine operation and basic theory is given in the following paragraphs.

3-420. CONTROL UNIT ADAPTER DESCRIPTION.

(To be supplied.)

3-421. SGS AND CRT EQUIPMENT DESCRIPTION.

3-422. Displays presented on the dd 74G Display Equipment are dependent upon character codes and memory instructions issued by the computer. The character code determines the character to be displayed and the memory address determines the position on the face of the CRT where the character will appear. All displays appearing on the CRT module screens are the direct result of combined digital and analog functions. The circuits generating the displays are located in both the SGS cabinet and up to 20 CRT modules (monitors). Figure 3-63 is a functional block diagram of the dd 74G.

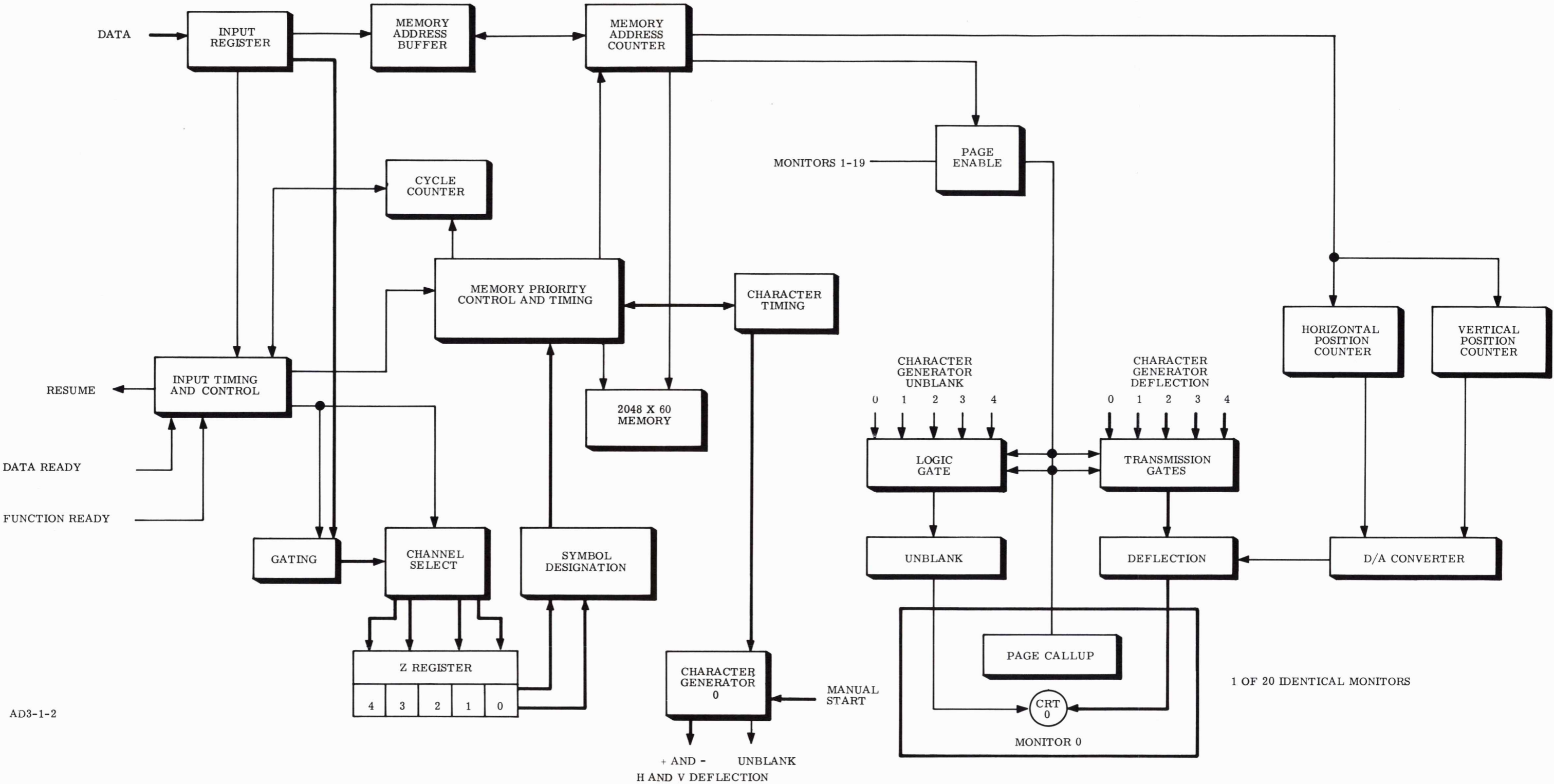


Figure 3-63. Symbol Generator Storage Unit Functional Block Diagram

3-423. Each CRT module contains thumbwheel switches for selecting any one of 20 top-half pages and any one of 20 bottom-half pages giving a total of 400 combinations. Each display is a page format consisting of 1024 characters displaying in two lines of 32 characters and 24 lines of 40 characters. Internal wiring determines the page format.

3-424. Input signals to the SGS are in the form of 12-bit digital words. The input signals are of four categories: external function-select word, SGS control word, address word, and data word.

3-425. An external function-select word selects the display system. It will not respond to any information sent by the computer unless such information is preceded by the external function-select word. The octal code of the external function for the dd 74G is 0100.

3-426. The second category is the SGS control word, which dictates the format of the data words and the location of memory for the address word. The most significant six bits (octal 75) indicate that the word is an SGS control word. The seventh most significant bit (MSB) is a spare. The eighth MSB indicates whether the data word is to be octally coded (the bit is equal to 0) or binary coded decimal (the bit is equal to 1). The ninth MSB dictates whether the data word will write over a period decimal point in memory or not. In some instances it is undesirable to destroy a period that has been stored in a certain memory address; if the ninth MSB bit is a 0, the data word will skip any memory locations that contain a period and will write in the next address. If, however, the ninth MSB is a 1, the data word will replace (write over) the period in the memory location. The last three bits of the SGS control word indicate the channel, and consequently the section of memory, where the data word will be stored. The channels are numbered zero through four.

3-427. The address word, which must follow the SGS control word, specifies the address in the selected channel where the computer will begin loading. The memory section assigned to the selected channel then is loaded sequentially with data words until recognition of the next control word.

3-428. A sequence of data words follow an address word and, depending on the coding specified by the SGS control word, each data word will either contain three BCD coded characters or two octally coded characters. The data words sent to the SGS from the computer are converted to octal form and stored in memory as dictated by the SGS control word and the address word.

3-429. The SGS generates a resume, after resynchronizing each input word, which allows the computer to enter a computer word with no visible effect on the CRT presentation. The storage section is a 2048 by 60-bit magnetic core memory. Memory read out is 60 bits per read/write cycle. The logic transfers the 60 bits to the five character generators which

operate in parallel. Each character generator receives 12 bits from the 60-bit word and generates two characters (each character requires six bits) in sequence. Therefore, during readout of the entire 2048 word memory, each character generator forms 4096 characters that will fill four full pages (eight half pages).

3-430. Each character generator generates a synchronized X and Y character deflection signal and an unblank signal, each dependent on the six-bit code transmitted to that generator. The outputs of any one of the generators may be transmitted to any, or to all, of the CRT modules as selected by the half-page callup thumbwheels on each module. The character generators can produce 58 characters.

3-431. The X and Y deflection for each character must be summed with the X and Y position corresponding to the location of the character on the page. A position generator in the SGS cabinet develops the position deflection signals. The position generator forms the page format for positioning the characters on the face of the CRT module. Page format deflection signals are summed with the character deflection signals, from each character generator, prior to transmission to the CRT module. The page format presents first a top line of 32 characters, then 24 lines of 40 characters, and finally a bottom line of 32 characters.

3-432. Central switching logic receives the half-page command signals from each of 20 CRT modules. Upon receipt of these signals, the switching logic selects the correct character generator output and the correct half-page from memory for transmission to the requesting CRT module. The central switching logic enables the selection of any of the 20 top-half pages and any of the 20 bottom-half pages by any of the 20 CRT modules. There are no restrictions on simultaneous selection of pages by any of the monitors.

3-433. The SGS cabinet also contains logic to cause characters to blink on command. Input of the character code start blink sets a blink control flip-flop. This causes the blinking of all subsequent characters at a preset rate, which normally is 2 to 5 cycles per second. A control on the SGS maintenance panel provides a means of adjusting the blink rate. A stop blink code causes the clearing of the blink control flip-flop and thus subsequent characters are displayed normally.

3-434. The following paragraphs describe how the display equipment operates functionally. Information flow is from the receipt of data to its display on the CRT in the monitor.

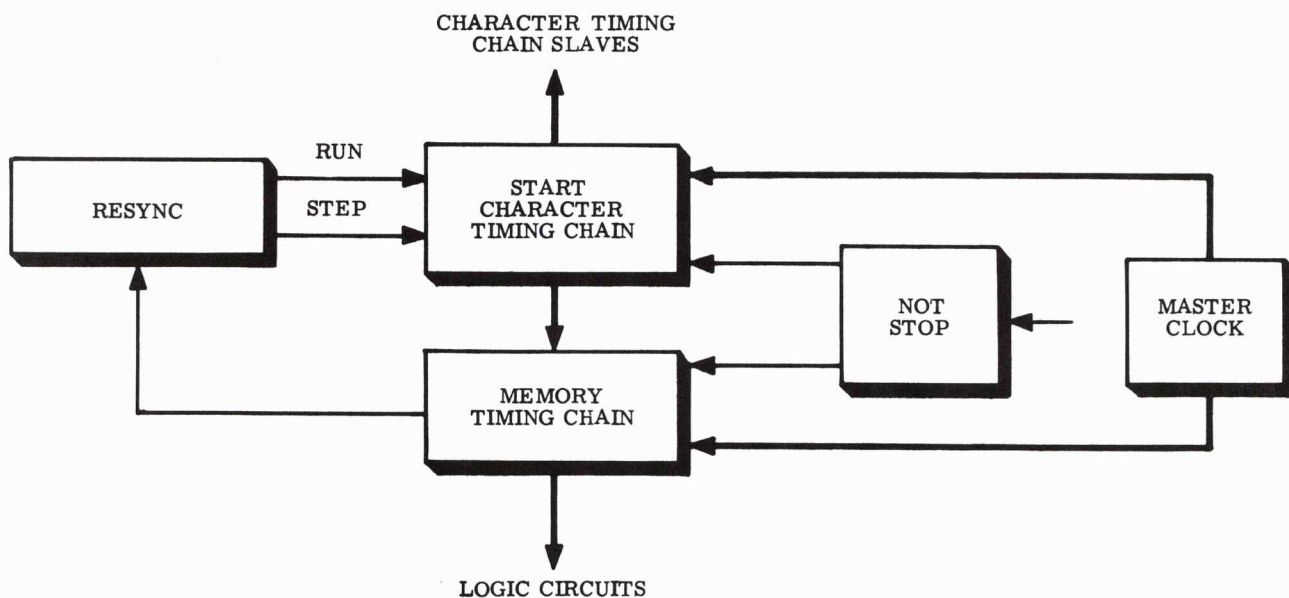
3-435. DISPLAY CONTROL.

3-436. Initially the display equipment is in an inactive, power-off condition. First the circuit breaker is placed ON. Depressing the POWER ON button on the maintenance panel then activates the main contactor. The blowers start and power is then applied to the +20-volt and

-20-volt power supplies. The logic now has power applied to it and is ready to operate. Placing the RUN-STOP-M CLR switch in the M CLR position sets up the display equipment for operation. Next the RUN-STOP-M CLR is placed in the RUN position. This sets a run FF. It, in turn, sends a pulse that starts the character timing chain. The character timing chain initiates the memory timing chain, placing the display equipment in a timing loop during which data is read from memory, translated, and displays generated. When the equipment is running, the display computer can enter data into the memory section. The following paragraphs explain the timing and control functions in detail.

3-437. MAIN TIMING AND CONTROL.

3-438. The main timing and control circuits govern the function sequences within the display equipment. Commands from the display computer, or operation of the maintenance panel controls, initiate command and data functions. Timing and control consists of the system timing pulses and resynchronization circuits. Figure 3-64 shows the overall timing relationship for the display equipment.



AD3-2-2

Figure 3-64. Display System Timing Block Diagram

3-439. RESYNCHRONIZATION CIRCUITS.

3-440. As previously explained, the first word to the display equipment must be on external function code (0100₈). Figure 3-65 graphically portrays the sequences of operation. The computer raises the Function Ready (figure 3-65, a) after the data lines have had time to settle. Raising the Function Ready line lights the DATA READY indicator, initiates the Data Ready resync circuit, which clears the resync FF's, sets the select FF, and sets the resume FF.

3-441. The computer now drops the Function Ready line, places the SGS control word on the data lines (figure 3-65, b), and raises the Data Ready line. Note that dropping the ready line clears the resume FF and resets the resync circuit. For example, placing a 7511 on the data line specifies an octal coded Character Mode writeover period, Channel 1.

3-442. Control logic translates the 7511. The Data Ready resync circuit resyncs the Data Ready signal and enables the gating of the input data to control FF's. An enable is generated to allow gating of the next input word into the memory address register.

3-443. The next data word, an address word (figure 3-65, c), is gated in the same way as the SGS control word. It will be an address word which specifies the memory address where data will be stored. The same resync function occurs as with the SGS control word.

3-444. The computer will now enter all data words for storage into memory (figure 3-65, d).

3-445. The display equipment stores all data appearing on the data lines until the computer raises the Function Ready line with a NOT 0100 word on the data lines or raises the Master Clear line.

3-446. The data word input enables the gating of a pulse to the memory timing chain through AND gates. Each cycle of the memory timing chain will enable the setting of the resume FF at the last count of the timing chain.

3-447. MEMORY LOCKOUT.

3-448. A double pulse occurring in the memory timing chain will result in the setting of a memory lockout FF. A failure of input power will also enable the setting of a lockout enable FF and then the lockout FF. Each lockout function prevents the storing of fault data in memory.

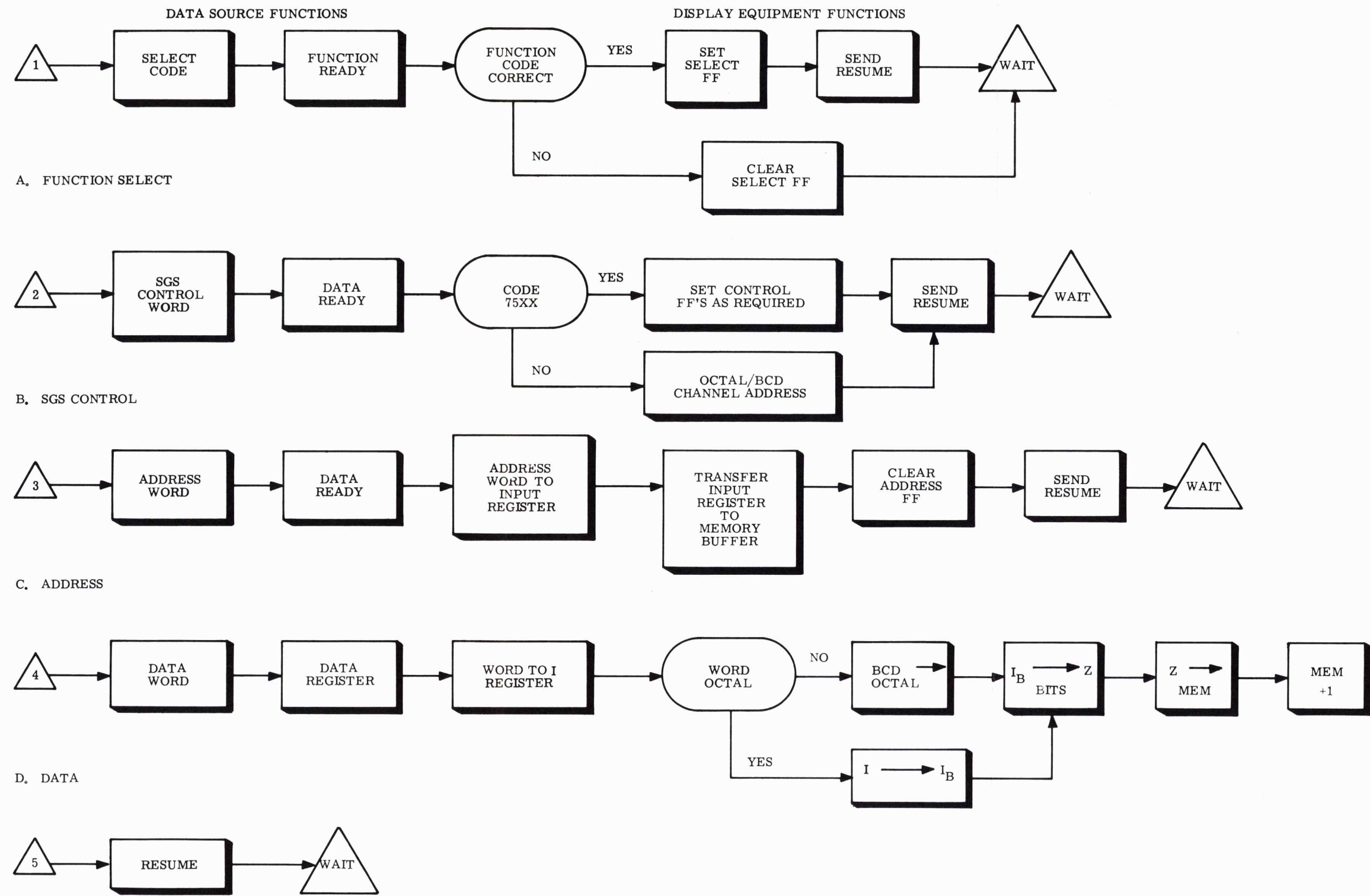
3-449. INPUT REGISTER.

3-450. A 12-bit register receives all data coming from the data source. Data entering the display equipment first goes through line receivers. The receivers feed data to the input register through AND's gated with the input timing control and to the resync logic.

3-451. Each input register FF feeds the memory address register, input gates, and neon indicator drivers. The drivers operate the INPUT indicators on the maintenance panel. A timing pulse clears the input register, then the data is gated from the receivers into the input register. Data also may be entered by using the input switches on the maintenance panel.

3-452. INPUT GATES.

3-453. The input gates convert both octal and BCD data contained in the input register into octal digits during an input to Z transfer. An octal/BCD FF gates the data directly as octal information, or enables the BCD to octal conversion.



AD3-3-2

Figure 3-65. Input Data Control Functions Flow Chart

3-454. INPUT TO Z CONTROL.

3-455. Figure 3-66 shows in block form how data is gated from the input register into the Z register. It also shows the effect the gating has on memory addressing. The input to Z circuit gates the contents of the input gates to the Z register.

3-456. WRITE-OVER PERIOD.

3-457. The basic function of the Not Write-Over-Period Mode is to provide a means of preserving all periods stored in memory yet still store all incoming information. This is accomplished by the input to Z control and the OCTAL, BCD counter. Figure 3-66 also shows the routing of the input words. The first input word is WOP (write-over period). Data transfer is direct and code 2 replaces the period code. Word 2 is in the Not WOP Mode ($\overline{\text{WOP}}$). Code 3 goes direct to 1 of word A_{n+1} while code 4 goes to 1 of word A_{n+2} . Code 4 cannot replace the period code in 2 of word A_{n+3} . Memory addressing will now be +1 for each new input word as long as a period is not read up.

3-458. The memory address register is an 11-bit counter. It may be force-set to an address or it may be counted up, starting at zero or a force-set address. The most significant bits (8, 9, and 10) control the page and channel selection. This is further described in the character generation paragraphs. Each memory stack is associated with a channel. A DISABLE ADVANCE ADDRESS switch provides a means for inhibiting a memory address advance. The memory timing chain controls all memory referencing sequences.

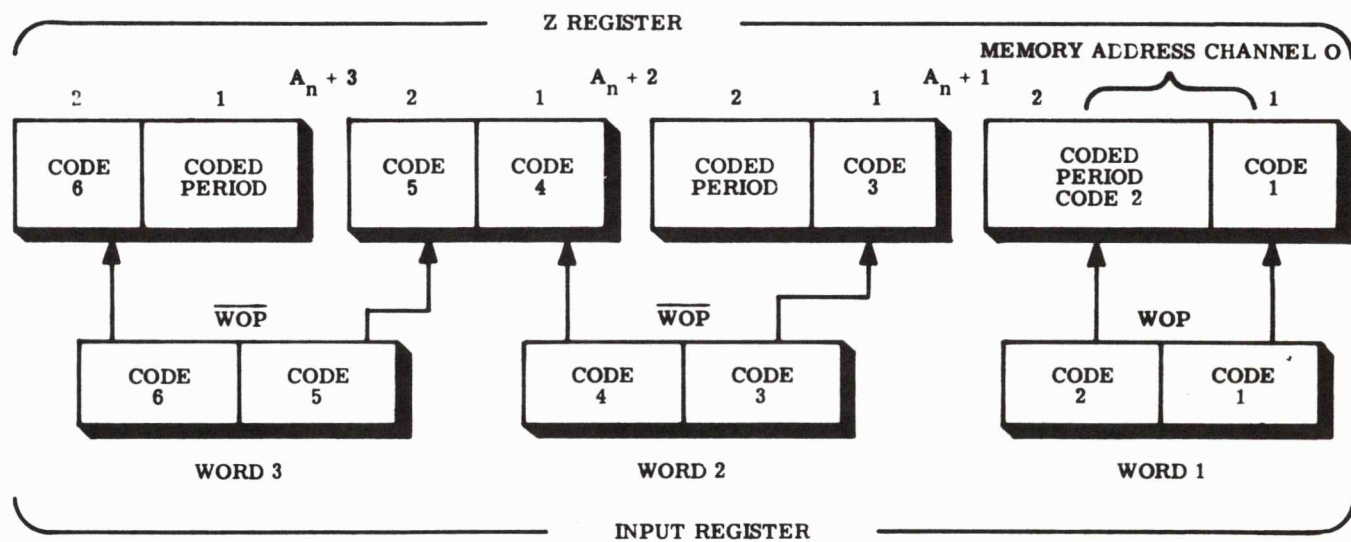
3-459. MEMORY TIMING AND CONTROL.

3-460. An initiate from the resync control or an initiate from the character generator starts the 32-pulse timing chain. The total time required for a memory reference is 64 microseconds. There are eight control delays in the timing chain which are cycled through four times.

3-461. The timing chain clears the Z register, transfers data from the input register or memory to the Z register, and initiates the character timing chain. Figure 3-67 presents the memory timing functions and the memory times at which they occur.

3-462. CONTROL CIRCUITS.

3-463. The memory cycle consists of four phases: divert, write, ready, and inhibit. Setting or clearing memory control flip-flops initiates or terminates, respectively, each of the phases which overlap one another during the 32-pulse cycle. The divert phase enables the selection of the drive lines in each stack, thus addressing the desired memory word. Each divert phase encompasses both the read and the write phases, since the drive lines must remain selected for ready or writing.



AD3-4-2

Figure 3-66. Input Gating and Input to Z Control Block Diagram

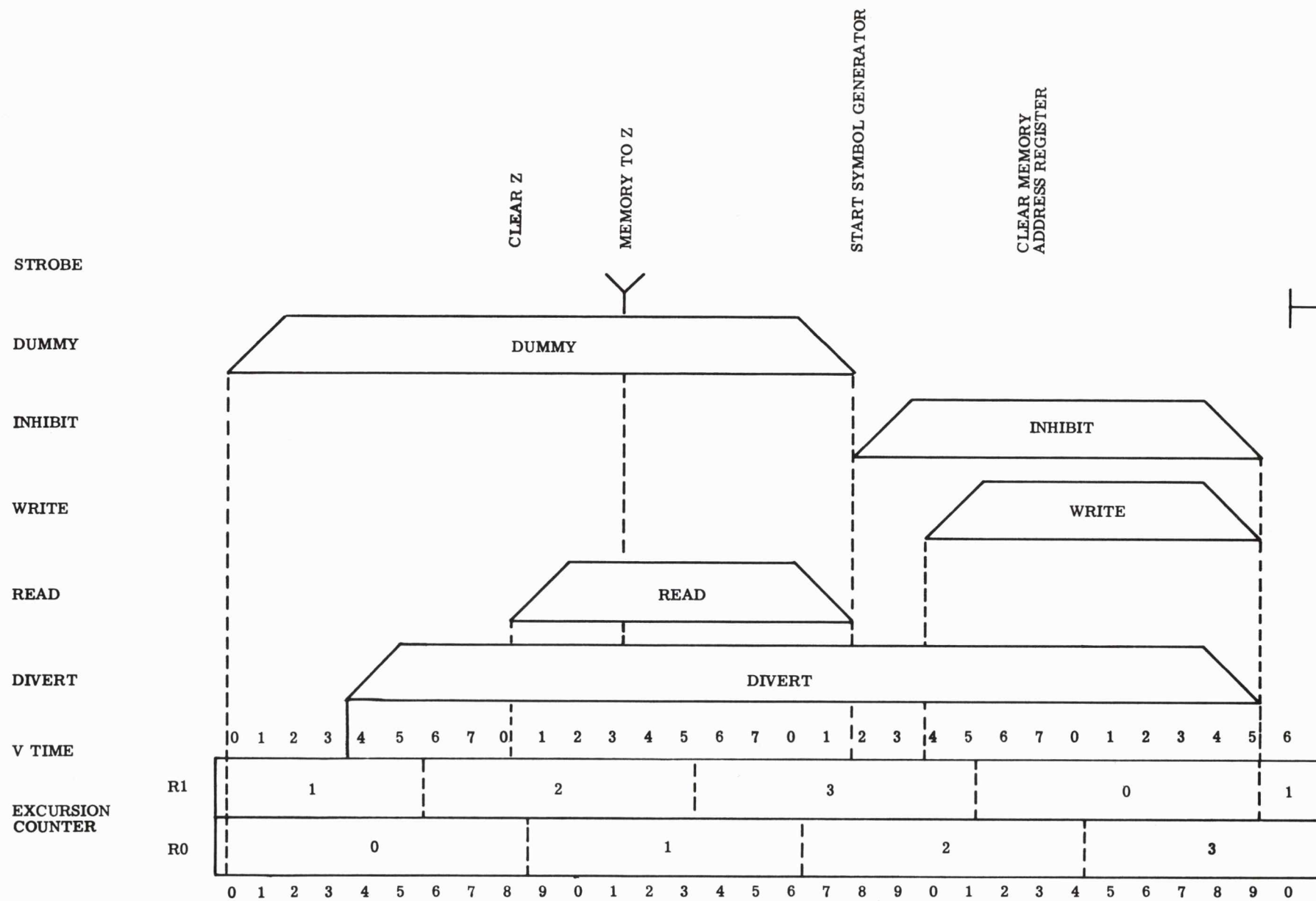


Figure 3-67. Memory Timing Diagram

3-464. CONTROL SEQUENCE.

3-465. The actual memory read phase begins 1.8 microseconds after initiation of the memory cycle. This delay provides time for formation of the memory reference address. A read phase takes 1.8 microseconds, during which a 200-nanosecond read strobe gates the information contained in the selected storage address to the storage (Z) register. The read phase reads out and destroys all information in a memory address. However, the 1.8 microsecond write phase, which starts 4.2 microseconds after initiation of the memory cycle, restores information destroyed during the read phase or stores new information.

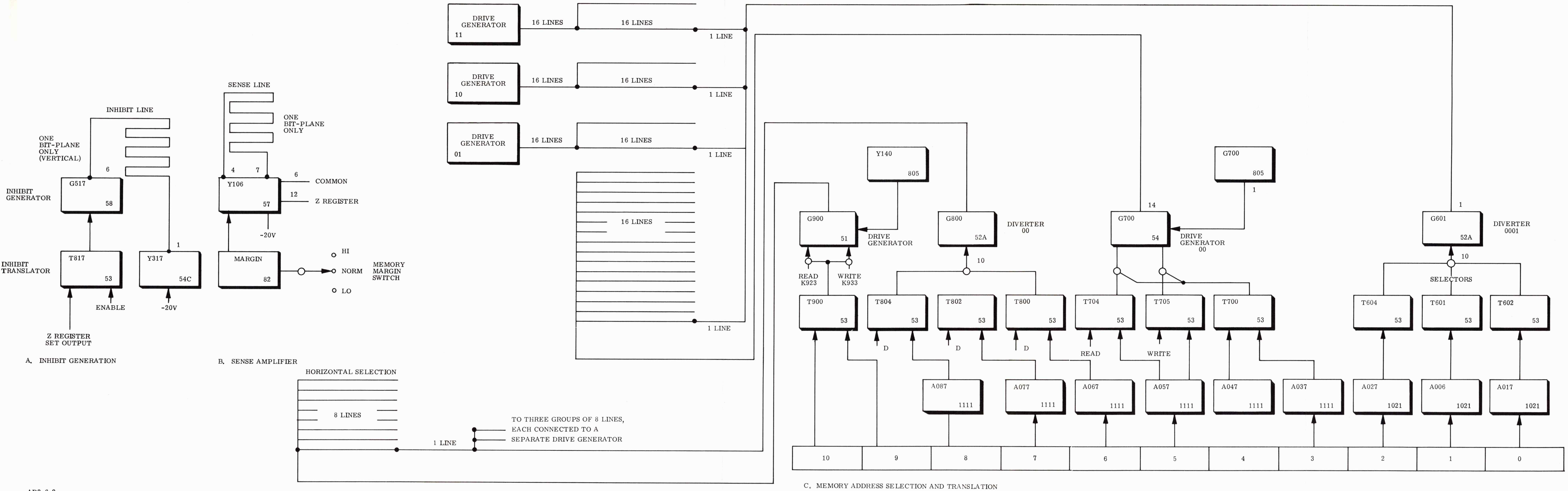
3-466. During the write phase, the drive lines attempt to set each of the 60 selected cores to a 1, and do so, except when prevented by the inhibit line for that plane. Therefore, the inhibit phase must occur at the same time as the write phase. There are dummy loads associated with the inhibit circuits to maintain a constant load on the power supply. During periods of no storage references, the dummy load is disabled for a period of 2.4 microseconds by the dummy drive signal.

3-467. ADDRESS SELECTION.

3-468. Each core may be addressed by a discrete combination of one of the 64 horizontal and one of the 32 vertical drive lines. The 64 horizontal drive lines are connected in groups of 16, to four horizontal drivers; the 32 vertical drive lines are connected, in groups of eight, to four vertical drivers. Current from the drivers may be directed or diverted to one of the selected drive lines by means of 8 vertical and 16 horizontal diverter cards. Thus, the combination of four drivers and eight diverters allows for a selection of any one of 32 vertical drive lines, and a combination of 4 drivers and 16 diverters allows for a selection of one of 32 horizontal drive lines.

3-469. Address selection is simultaneous for each bit-plane. Thus horizontal and vertical addresses 00 are the same in each of the planes (figure 3-68). Each horizontal diverter selects four lines of which one goes to each of the four drivers. Only one horizontal diverter and one horizontal driver is selected at any one time. Thus, for horizontal address 00000₂, the driver 00₂ and the diverter 000₂ are selected. The vertical drivers and diverters are connected in a similar manner except only eight diverters are connected to each of the four drivers.

3-470. Figure 3-68, d shows a simplified diagram of the inverters, selectors, diverters, and drivers involved in selecting memory address 1 in memory stack 0. Refer to figure 3-68 during the following discussion. Bit 0 being in the set state (memory address = 0001₈) enables the selecting of address 1 in the following manner. Vertical address 1 = 1 while horizontal address = 0.



AD3-6-2

Figure 3-68. Memory Section Simplified Block Diagram

3-471. The sense amplifiers detect the switching of any core in a bit-plane. Since each plane contains all of the bits associated with a single bit of a memory word for each address, only one core switches at any one time. There is a total of 60 bit-planes, each having a sense amplifier connected to both ends of the sense wire which threads each core. When the core switches, indicating a 1 in the core, the pulse activates a sense amplifier driving its output from -3 volts to -0.5 volt. The output goes to an inverter for inversion and strobes an AND of a Z register FF. A strobe pulse from the memory timing chain enables the AND, thus setting the Z register FF. A zero core does not switch, thus the sense amplifier output remains a -3 volts. In turn, the inverter is equal to 0 volts, which inhibits the Z register FF AND gate.

3-472. MEMORY CIRCUITS.

3-473. The memory storage section performs non-logical functions such as amplification, pulse generation, and switching.

3-474. BEAM POSITIONING.

3-475. Positioning of the beam on the face of the CRT depends on the contents of the horizontal (H) and vertical (V) position register. This register is an overall 11-stage counter divided into two parts, H and V. Altogether there is a total of 1024 positions comprising a page format on the CRT, although 2048 can be obtained by wiring changes.

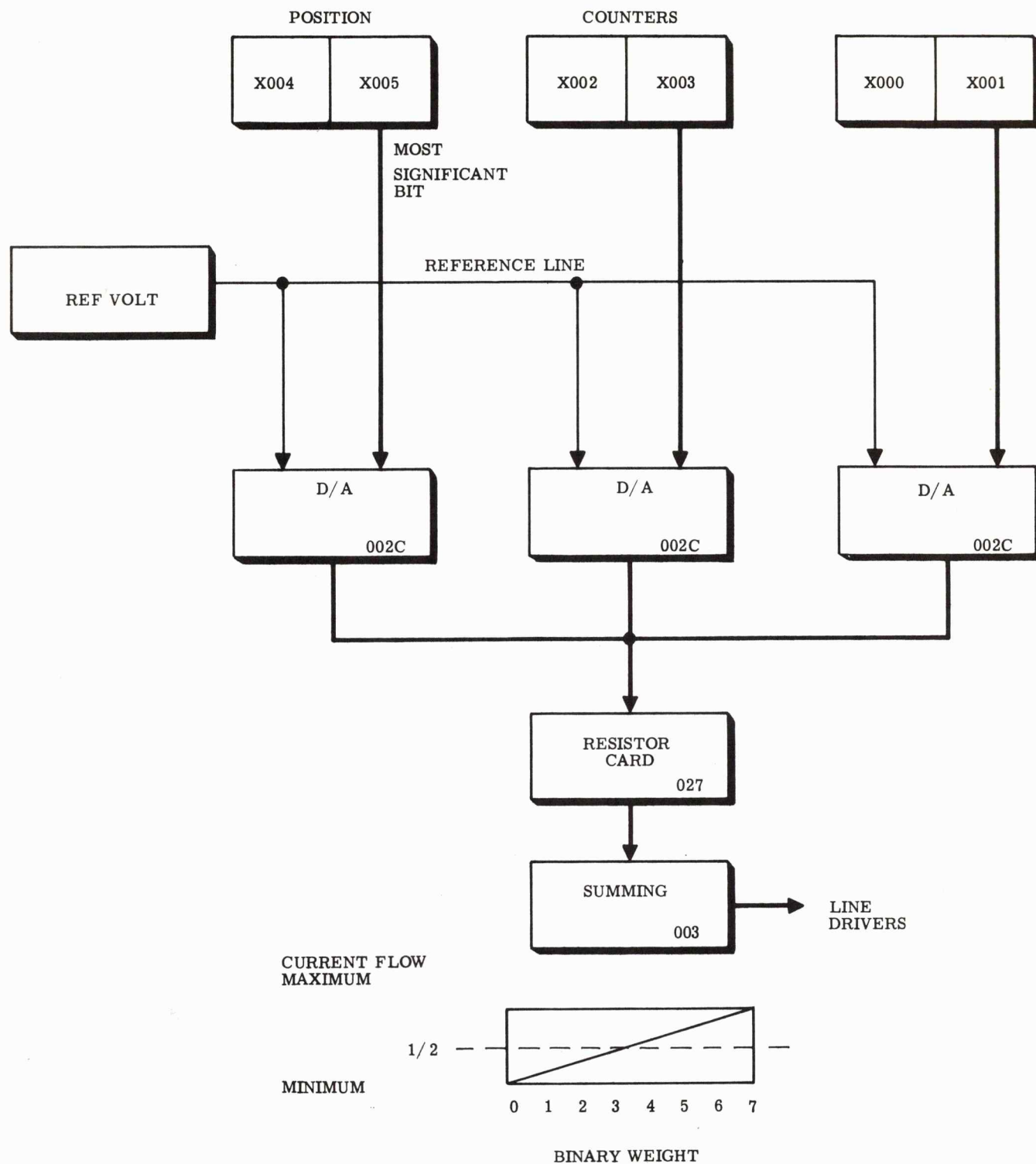
3-476. The upper left-hand corner of the CRT matrix is addressed 0 and the lower right-hand corner is matrix position X counter equal to 37_8 and Y counter equal to 31_8 .

3-477. As mentioned previously, a page of information consists of one line of 32 characters, 24 lines of 40 characters each, and one line of 32 characters. The position counter incorporates a carriage return function which makes a display appear similar to a typewritten message. After the painting of the last character in a horizontal line, the logic clears the X (horizontal) counter and increments the Y (vertical) counter by 1. To achieve the 32 and 40 character lines, the logic must detect the correct Y counts to govern the maximum X count.

3-478. The position counter drives the D/A converters (see figure 3-69). Each D/A converter converts the digital enable to an analog current. The currents are fed to resistor cards, which weight each current proportionally to its binary value.

3-479. Each D/A string operates from a 5-volt reference. The reference for the positioning D/A's is a constant 4.5 ± 0.5 volts. Each D/A converter output, in a string, goes to a single resistor card. The resistors are of different values, depending upon the weight of the bit; i.e., the most significant bit carries the greatest weight and the least significant bit carries the smallest weight. The resistor card output, which is the algebraic sum of the inputs, goes

REGISTER CONTENTS			
MINIMUM DEFLECTION	0	0	0
1/2 DEFLECTION	0	1	1
MAXIMUM DEFLECTION	1	1	1



AD3-7-2

Figure 3-69. Typical D/A Conversion Block Diagram

to the +H, -H, +V, or -V summing amplifiers, depending upon the inputs. The summing amplifier output is fed to the line drivers for each monitor. Cards are provided for adjusting the overall deflection level fed to all monitors.

3-480. DEFLECTION.

3-481. Figure 3-70 graphically shows the deflection system of the display equipment. As previously mentioned, the deflection counter drives the D/A conversion network.

3-482. All four deflection lines from the D/A conversion network enter the deflection circuitry through a differential amplifier used for shifting the 5-volt output of a card to -15 volts.

3-483. Signals +H, -H, +V, and -V then go to the character forming network which distributes the four signals through a line driver to the deflection preamplifiers of the CRT's. Each deflection line goes to an impedance matching card and preamplifiers located in the monitor.

3-484. CHARACTER GENERATION.

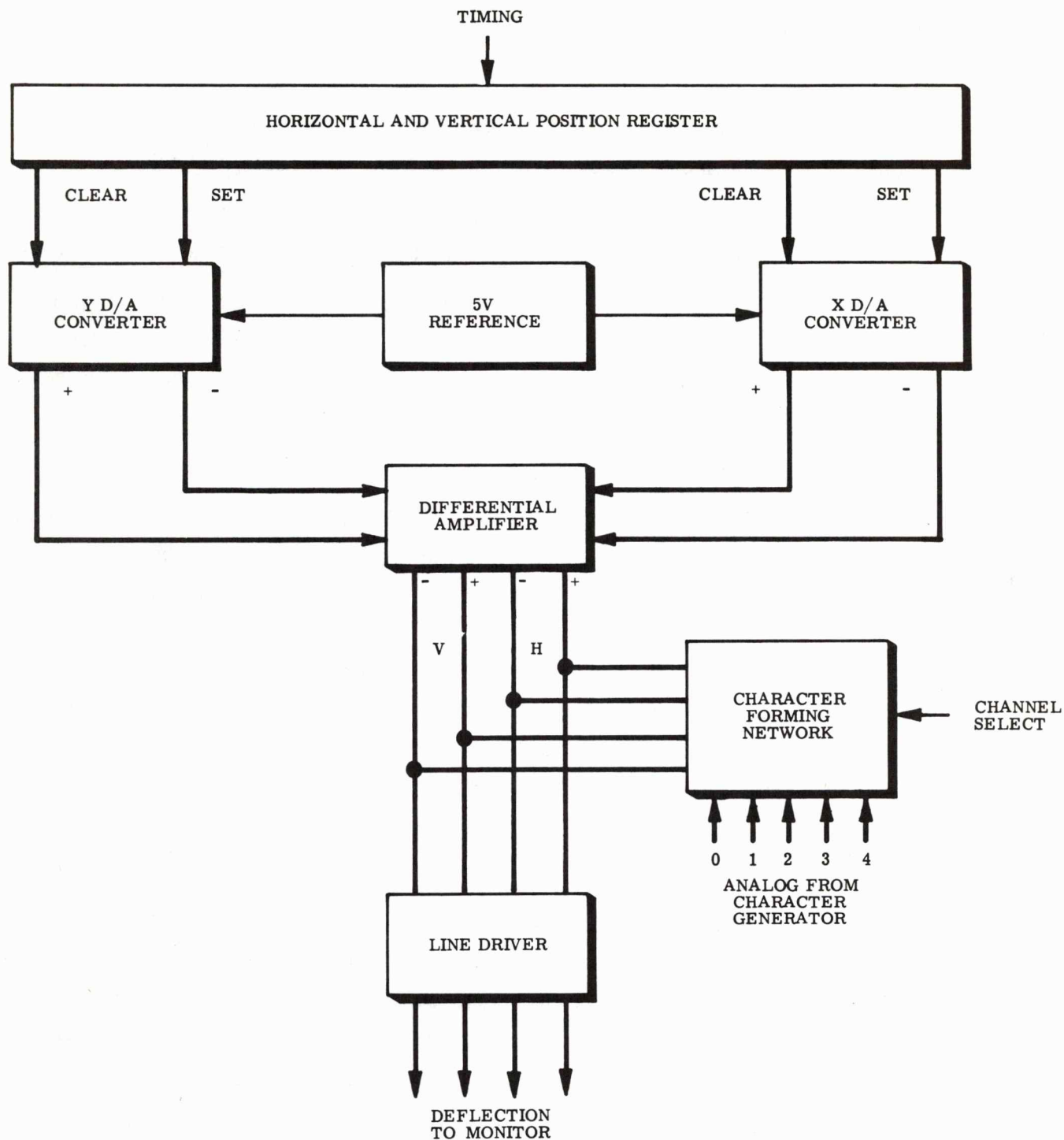
3-485. There are five character generators in the dd 74G. Each generator requires a coded binary word to activate it. The word comes from 12 bits of the Z register, thus there are 60 bits reserved for character generation. Six bits of each word defines two characters. Figure 3-71 shows a block diagram of the character generator functions. Character formation occurs within a 7 x 7 matrix centered on one of the CRT raster points. The generator moves the beam progressively from the center of one increment to the center of another, thus forming a pattern on the CRT face. Figure 3-72 shows a typical character, the beam movements involved in its formation and its relationship to the CRT raster.

3-486. PRIMARY TRANSLATION.

3-487. The first six-bit character code, then the second six-bit character code is gated into the translation circuit. As previously mentioned, each memory channel word contains two six-bit character codes. The state of the translator FF's, in turn, enable the AND-gates of inverters. The outputs of the inverters go to second primary translation inverters. The outputs of the second primary translators activate the drive lines on the D88 diode matrix cards.

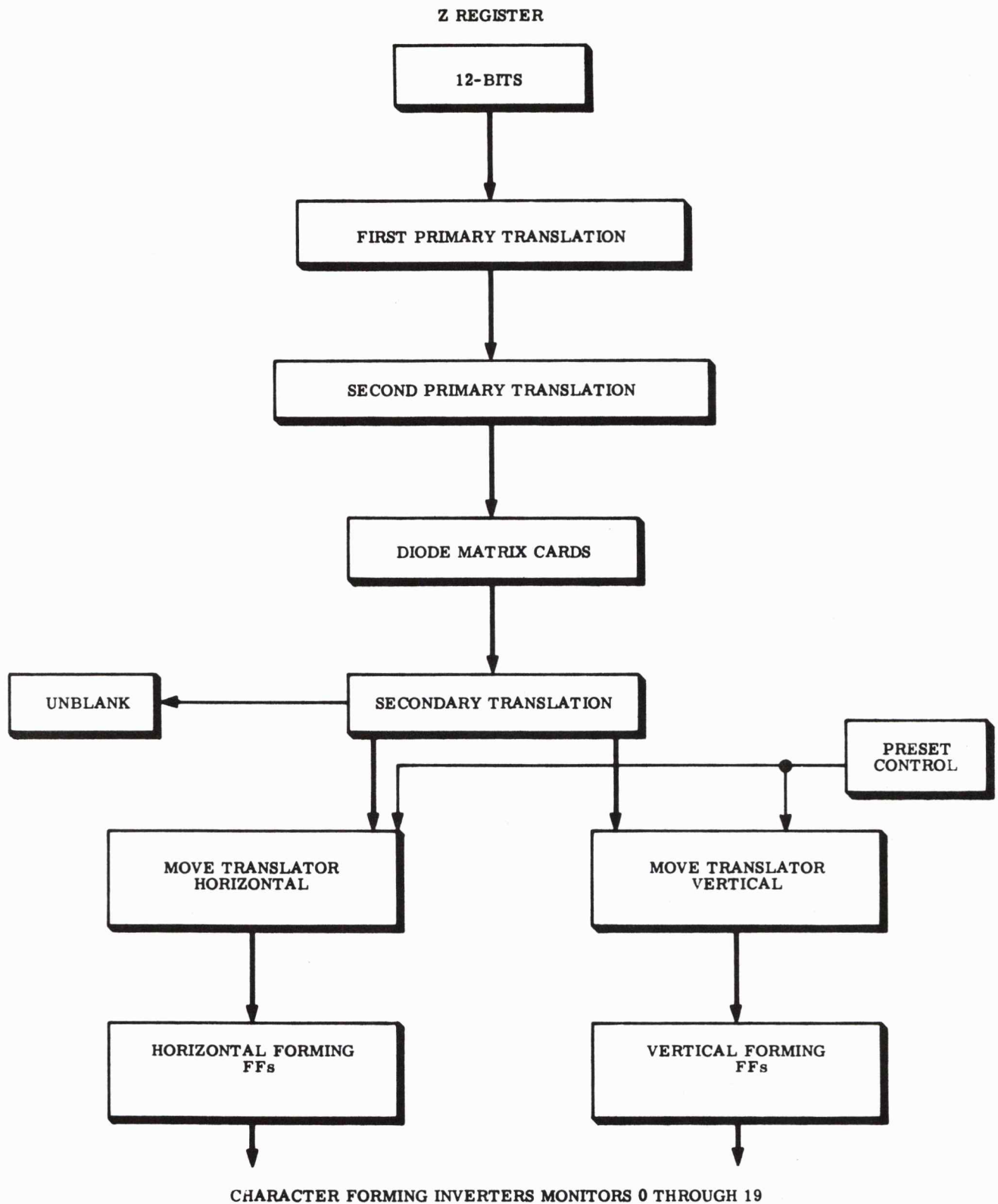
3-488. D88 cards form the secondary character translation within the display equipment. Figure 3-73 shows a drawing of a typical D88 card, its construction, connections, and how its outputs go to the stepping network.

3-489. Each D88 card is connected to eight drive lines corresponding to character groups. The horizontal lines in the figure represent the eight drive lines. The other 25 pins on each card go to five groups of five-line wires (enables) represented by the vertical lines. The five



AD3-8-2

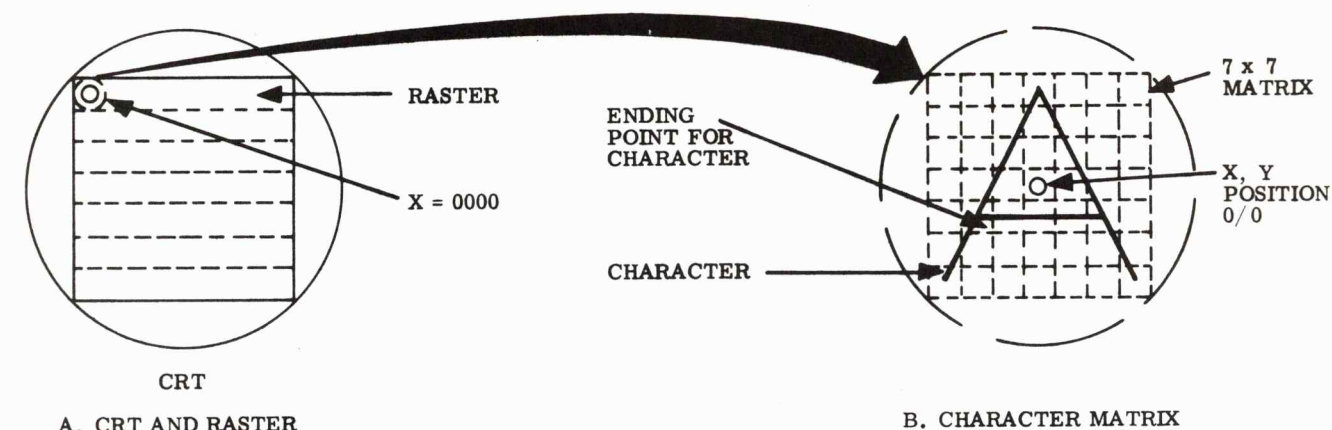
Figure 3-70. SGS Deflection System Block Diagram



AD3-9-2

Figure 3-71. Diagram of Character Generator Functions

lines of each group correspond to one time period of the character timing chain. They may go to any one of several diode isolated drive lines for enabling beam movements, one and two increments horizontally, one and two increments vertically, or for unblanking.



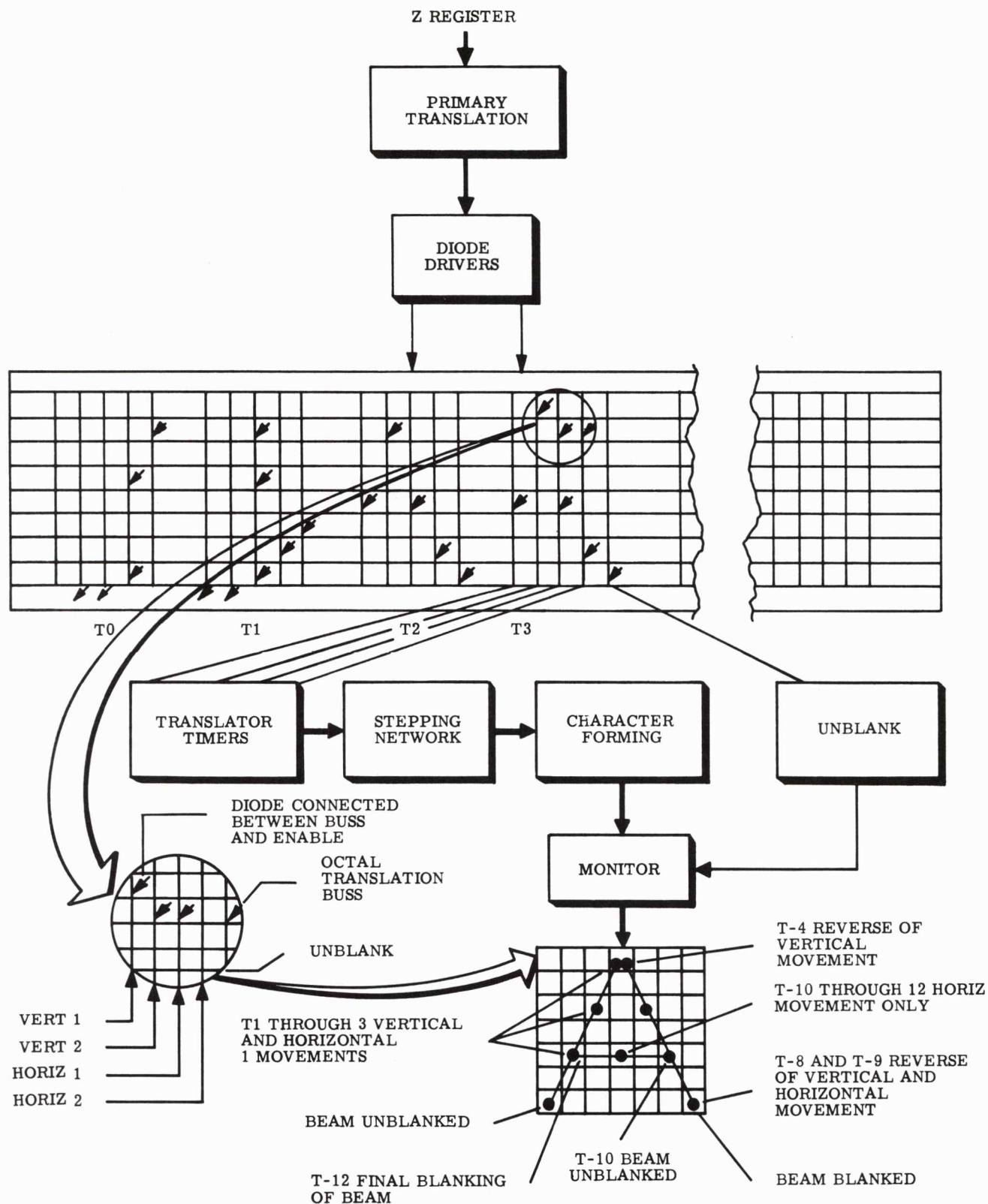
AD3-10-2

Figure 3-72. Character Matrix and CRT Raster

3-490. Three D88 cards are connected in series for each character group. This gives a total stepping capacity of 15 times. A diode connected between a character drive line and the third horizontal advance 1 line enable beam movement one horizontal position at time 2. The drive line accomplishes this by placing a -0.5-volt level on the horizontal advance 1 line continuously until translation of a different character code. The horizontal advance 1 line feeds an inverter which, in turn, outputs a -3-volt level to the character stepping circuitry. Likewise, connecting diodes to any of the other enable lines will activate inverters which provide enables to the character formation section. The diodes prevent feedback from the enable lines to the other drive lines, otherwise a direct connection would be possible. Enabling both a horizontal 1 and a horizontal 2 line at the same time constitutes an axis reverse signal.

3-491. CHARACTER TIMING

3-492. A 24-step timing chain times the character generation. A pulse from the memory timing chain at time 17 initiates the timing chain. This timing chain consists of 24 control delays and an excursion counter. H terms of the counter delays drive slave inverters. The slaves form character timing pulses 1 through 18. The timing pulses go to the translator timers where they probe the same input AND's that the translation inverters do. Thus coincidence between a time and translation inverter initiates the translator timer. Three of the times, 15, 17, and 18, are not gated with outputs of the diode matrix.



AD3-11-2

Figure 3-73. Diagram of Typical Character Formation

3-493. TRANSLATOR TIMING.

3-494. The horizontal and vertical translator timers issue the advance-up and -down and advance-left and -right signals to the stepping networks.

3-495. SECONDARY TRANSLATION.

3-496. Secondary character translation (SCT) provides outputs in five categories: horizontal movements 1 and 2, vertical movements 1 and 2, and unblank.

3-497. CHARACTER POSITIONING.

3-498. The character positioning networks form the analog values necessary for character generation. Outputs from both the secondary translation network and the character timing chain enable character stepping through the translator timers. Vertical and horizontal stepping both operate in the same manner.

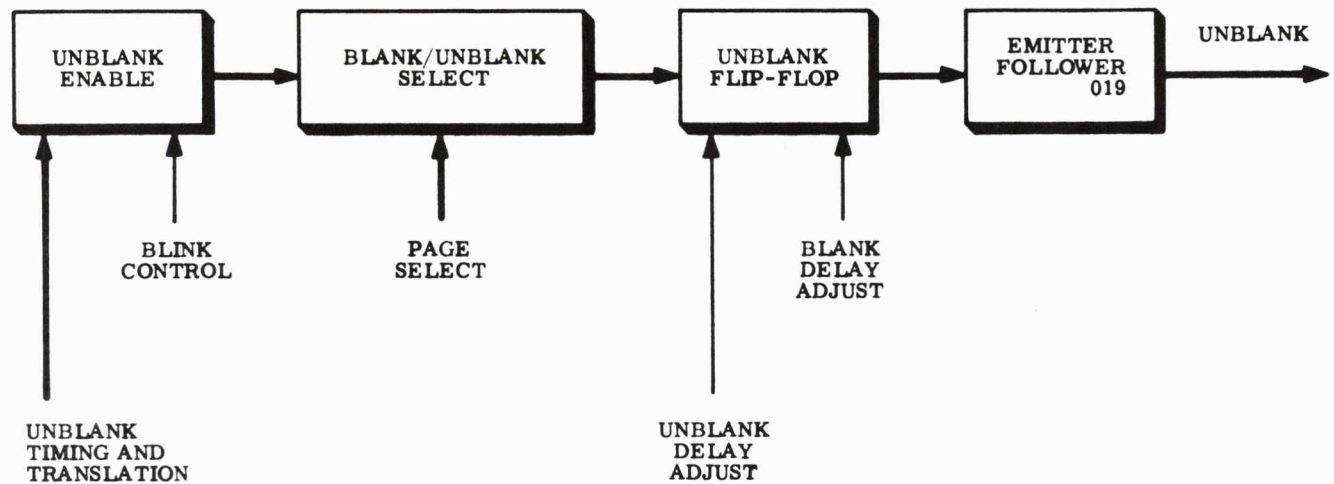
3-499. The character translation timing networks, previously discussed, furnish advance 1 or 2 pulses that control the stepping function. The six FF sets function as an additive or subtractive counter, depending upon the state of a reverse FF. Setting all of the FF's places the beam at the top of the matrix, while clearing all of them places it at the bottom of the matrix.

3-500. The base deflection signals and the character generation signals are mixed in this circuit. Figure 3-70 shows a block diagram of the deflection system. Character signals from each of the five character generators are ANDed with enables from the half-page call-up circuit. The character forming circuit feeds a current summing amplifier. The resistive outputs of the current summing amplifier are connected directly to the deflection lines going to the monitor. Trimmers are connected to the current summing amplifier to provide a means of smoothing the character forming outputs. The combined character and deflection signals go to line drivers, which drive the preamplifier in the CRT module.

3-501. UNBLANKING.

3-502. Unblanking involves the turning on for the CRT beam. Later paragraphs will explain the CRT module and its circuitry. This portion explains only the logic functions necessary to provide unblank signals to the CRT module. Figure 3-74 is a graphic illustration of the unblank system. The output goes to the monitors.

3-503. Unblanking of the CRT beam depends upon enables furnished by the character unblanking circuit. Each character generator has its own unblank control circuit that operates similarly to the deflection translation timing circuit. When the unblank control circuit is set, it enables the unblanking of the beam through the half-page callup logic, which drives the unblank preamplifier in the monitor.



AD3-12-2

Figure 3-74. SGS Unblank System Block Diagram

3-504. CRT MODULE.

3-505. The monitor (CRT module) is that portion of the display equipment that contains the CRT, high-voltage power supplies, deflection amplifiers, and CRT reference voltage controls. Figure 3-75 is a functional block diagram of the monitor.

3-506. There are two categories of signals that go from the SGS cabinet to the CRT module: deflection and unblank. Both types of signals go through the line driver subassembly, which distributes the signals to the CRT modules.

3-507. DEFLECTION PREAMPLIFIER.

3-508. Deflection signals from the SGS logic are of push-pull, vertical, and horizontal form. They go to the deflection preamplifier, which is a two-stage differential voltage amplifier.

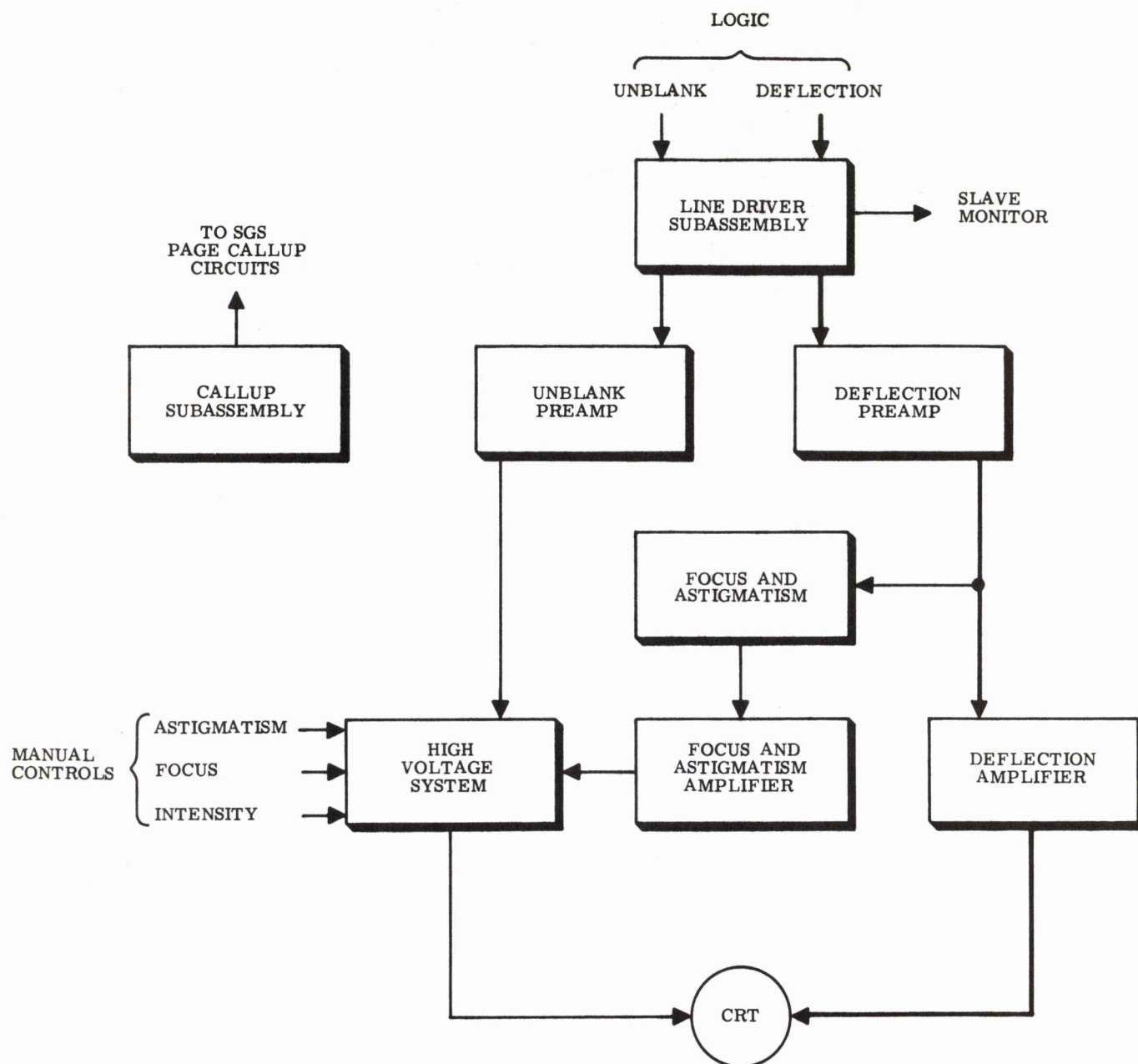
3-509. DEFLECTION AMPLIFIER.

3-510. The signals from the preamplifier go to the two-stage noninverting push-pull deflection amplifier and to the focus and astigmatism preamplifiers.

3-511. FOCUS AND ASTIGMATISM.

3-512. The focus and astigmatism circuit consists of two preamplifiers and two vacuum tube amplifiers.

3-513. The output of the focus/astigmatism circuit increases or decreases as the horizontal and vertical deflection levels vary. This compensates for the defocusing effect on the CRT as the beam approaches the sides of the raster, thus keeping the beam in focus.



AD3-13-2

Figure 3-75. Monitor Functional Block Diagram

3-514. Unblank signals enter the monitor through the driver assembly. They then go to a type 205 unblank preamplifier. From the preamplifier, the signals go to an unblank amplifier which is coupled to the CRT control grid circuit.

3-515. CATHODE RAY TUBE.

3-516. The CRT is electrostatically deflected. The CRT also contains electrodes for focus and astigmatism correction, a control grid for turning the beam on and off, and varying its intensity.

3-517. DEFLECTION.

3-518. The CRT deflection plates, which are directly coupled to the output of the deflection amplifier, must be at approximately the same potential as the CRT acceleration electrode to obtain the optimum spot size. A ground reference potentiometer, located on the high-voltage divider, matches the acceleration potential to that of the deflection amplifier.

3-519. Adjusting this potentiometer moves the zero reference point of the voltage divider in either a positive or negative direction. This, in effect, raises or lowers the accelerator to ground potential, which provides a means of obtaining the correct relationship between the deflection plates and the high-voltage circuits.

SECTION IV

SUPPORT EQUIPMENT

4-1. INTRODUCTION.

4-2. The Support Equipment includes units that, while they do not enter the major test data flow, provide functions necessary to overall test operation of the ACE-S/C ground station. For purposes of description, these are grouped into two secondary equipment categories: timing equipment and status monitoring and display equipment.

4-3. TIMING EQUIPMENT.

4-4. The time code signals generated by the ACE-S/C timing equipment may be divided into two general types: (1) real-time code signals and (2) countdown time code signals. These time codes are used in the ACE-S/C system as:

- a. Real-time signals for recording on magnetic tape recorders, for tape search, and for playback to time indicators and the computer.
- b. Real-time signals to drive visual time indicators located in the computer and control rooms.
- c. Real-time signals for recording on analog and event strip chart recorders.
- d. Countdown time signals to drive visual time indicators located in the computer and control rooms.
- e. Countdown time signals for recording on magnetic tape recorders, for playback to time indicators and the computer.
- f. Countdown and real-time signals for computer usage.

4-5. For the purpose of this manual, real time is defined as the time of day at which an event is actually occurring. As data is recorded on magnetic tape during checkout testing, the real-time signals are simultaneously recorded on another data track of the same tape. During playback of this data on any subsequent date, the recorded time signals are utilized for time correlation of events. Recorded time signals, reproduced with the playback of previously recorded data, are defined as playback time.

4-6. Countdown time is defined as the amount of time prior to, or subsequent to, an actual or simulated liftoff time. Countdown time counts up to zero, and then forward from zero, in one-second steps from a preset start time. This start time may be set at any time between

-999 hours and +999 hours. The countdown time is recorded in the same manner as the real time previously described and may also be used in the Playback Mode for data reduction purposes. Countdown time when used in the Playback Mode is referred to as playback countdown time.

4-7. Real time may be further divided into two different types of time code formats: (1) IRIG B and (2) AMR B-1. In the following paragraphs, the distribution of each of the time codes used by the ACE-S/C system (IRIG B, AMR B-1, and countdown) will be described: first in the Normal or present actual time Mode and then in the reproduce or Playback Mode.

4-8. TIME SIGNAL DISTRIBUTION.

4-9. IRIG B REAL-TIME DISTRIBUTION. The distribution of the IRIG B time code, on a real-time basis, is illustrated in figure 4-1. The IRIG B time code signals are generated by the Time Code Generator. The Time Code Generator is physically a part of the Timing Group located in the Terminal Patch Facility room of the ACE-S/C system. The IRIG B time code output of the generator is provided in both serial and parallel format. The parallel IRIG B time code format is sent to wall clock display units: three located in the control room and two located in the computer room. The serial IRIG B time code format is routed directly to the Time Code Distribution Unit and distributed as follows:

- a. To the oscillographic recorder (located in the Analog Recorder Unit) via a patch panel in the Event Distribution Recording and Patching Unit.
- b. To a Video Distribution and Tape Transport Control Unit patch board and thence to a Magnetic Tape Recorder via the signal mixer.
- c. To the Tape Recorder/Computer Time decoder and Search Control Unit.

4-10. The Tape Recorder/Computer Time Decoder Search Control Unit converts the serial IRIG B time code signals to a parallel format for the use of the computers, as required by the computer programs. The serial IRIG B time code signals received by the Tape Recorder/Computer Time Decoder Search Control Unit are also converted to a parallel code format suitable for display on a Computer Complex Console clock and a Test Conductor Console clock.

4-11. IRIG B PLAYBACK TIME DISTRIBUTION. The distribution of played back IRIG B time code signals is illustrated in figure 4-2. When it is necessary to use reproduced (playback) information stored on magnetic tape, the output of the tape channel containing previously recorded IRIG B time code signals is fed to a patch panel of the Video Distribution and Tape Transport Control Unit via the signal separator. The played back IRIG B time code signals (in serial form) are patched to the Time Code Distribution Unit. The Time Code Distribution Unit amplifies the played back IRIG B time code signals and distributes them:

- a. To the oscillographic recorder (located in the Analog Recorder Unit) via a patch connection on the Video Distribution and Tape Transport Control Unit.

- b. To the Tape Recorder/Computer Time Decoder Search Control Unit.

4-12. The Tape Recorder/Computer Time Decoder Search Control Unit processes and distributes the played-back IRIG B time code signals exactly as it did with IRIG B real-time code signals.

4-13. AMR B-1 REAL-TIME DISTRIBUTION. The distribution of the AMR B-1 time code signals on a real-time basis is illustrated in figure 4-3. The AMR B-1 time code signals are generated by the Time Code Generator. The AMR B-1 time code signal output of the Time Code Generator is in a serial format. The AMR B-1 time code signals are simultaneously sent to the Decommutator Distribution and Event Storage and Distribution Unit (DD/ESDU) located in the control room and to the Time Code Distribution Unit (part of the Event Distribution Patching and Recording Unit) located in the computer room. The DD/ESDU routes the AMR B-1 time code signals to the console mounted strip-chart analog and event recorders. The AMR B-1 time code signals received by the Time Code Distribution Unit are routed as follows:

- a. To a 100-channel strip-chart event recorder located in the Event Distribution Patching and Recording Unit.
- b. To the analog recorders contained in the Analog Recording Unit.
- c. To the Video Distribution and Tape Transport Control Unit.

4-14. The AMR B-1 time code signals received by the Video Distribution and Tape Transport Control Unit are fed to a voltage-controlled oscillator (VCO) in the signal mixer, combined with other miscellaneous data, and fed to a magnetic tape recorder channel.

4-15. AMR B-1 PLAYBACK TIME DISTRIBUTION. The distribution of played-back AMR B-1 time code signals is illustrated in figure 4-4. When it is necessary to use reproduced (playback) information stored on tape by the magnetic tape recorders, the output of the tape channel containing previously recorded AMR B-1 time code signals is fed to a Video Distribution and Tape Transport Control Unit patch panel. (It should be remembered that the AMR B-1 time codes signals previously recorded were mixed with other miscellaneous data signals prior to being recorded on the magnetic tape recorders.) The playback signal, containing the AMR B-1 time code information, is patched to the signal separator subassembly in the Video Distribution and Tape Transport Control Unit. The outputs of the signal separator are selected data signals and a multiplexed signal that contains the AMR B-1 time code information and other miscellaneous information. This multiplexed signal is then patched to the appropriate FM discriminators located in the FM Discriminator Unit. The output of one of the FM discriminators is the demodulated AMR B-1 time code signal. The AMR B-1 time code

signals are then fed to the Video Distribution and Tape Transport Control Unit and, from there to the Time Code Distribution Unit. At this point, the AMR B-1 time code signals are distributed as follows:

- a. To the event and analog recorder equipment located in the computer room via the Event Distribution Recording and Patching Unit.
- b. To the DD/ESDU via the Terminal Patch Facility room and thence to event and analog recorder equipment located on various control room consoles.

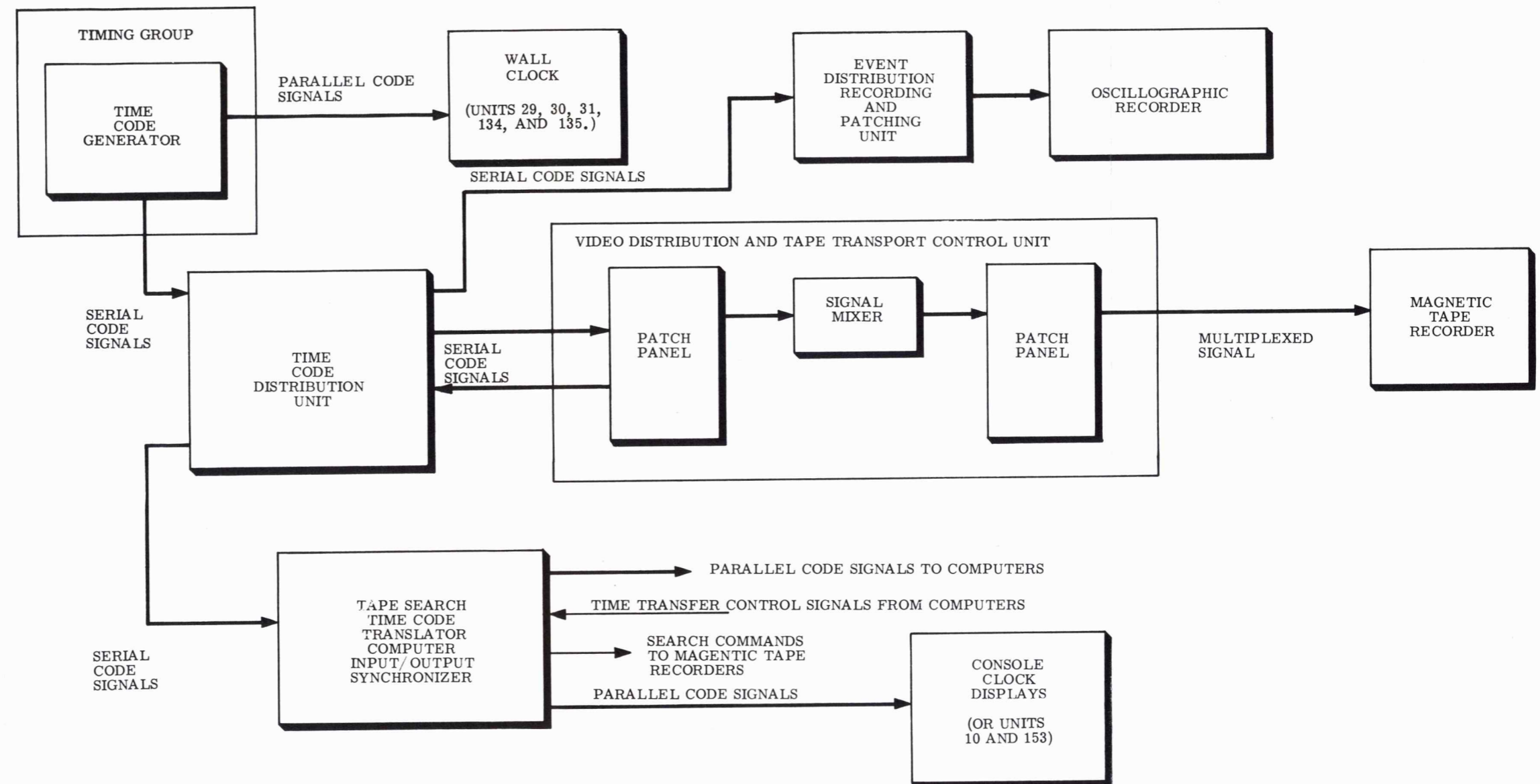
4-16. COUNTDOWN TIME DISTRIBUTION. The distribution of countdown time code signals is illustrated in figure 4-5. The countdown time code signals are produced by the Countdown Generator, that is physically a part of the Time Group Unit located in the ACE-S/C Terminal Patch Facility room. The countdown time code output of the Countdown Generator is produced in both serial and parallel format. The parallel countdown time code is routed via the Terminal Patch Facility to three wall clock display units in the control room and two wall clock display units in the computer room. The serial countdown time code signals are routed via the Terminal Patch Facility to a Video Distribution and Tape Transport Control Unit patch panel. The Video Distribution and Tape Transport Control Unit distributes the serial countdown time code signals:

- a. To a VCO contained in the signal mixer subassembly of the Video Distribution and Tape Transport Control Unit where it is combined with other miscellaneous data signals to form a multiplexed composite signal. This composite signal containing the countdown time code information is then sent to a magnetic tape recorder channel.
- b. To the Countdown/Computer Interface/Translator Unit.

4-17. In the Countdown/Computer Interface/Translator Unit, the serial countdown time code signals are converted to a parallel format for the use of the computers (both display and command) as required by the computer programs. The serial countdown time code signals received by the Countdown/Computer Interface/Translator Unit are also converted to a parallel format suitable for display on a Computer Complex Console clock and a Test Conductor Console clock.

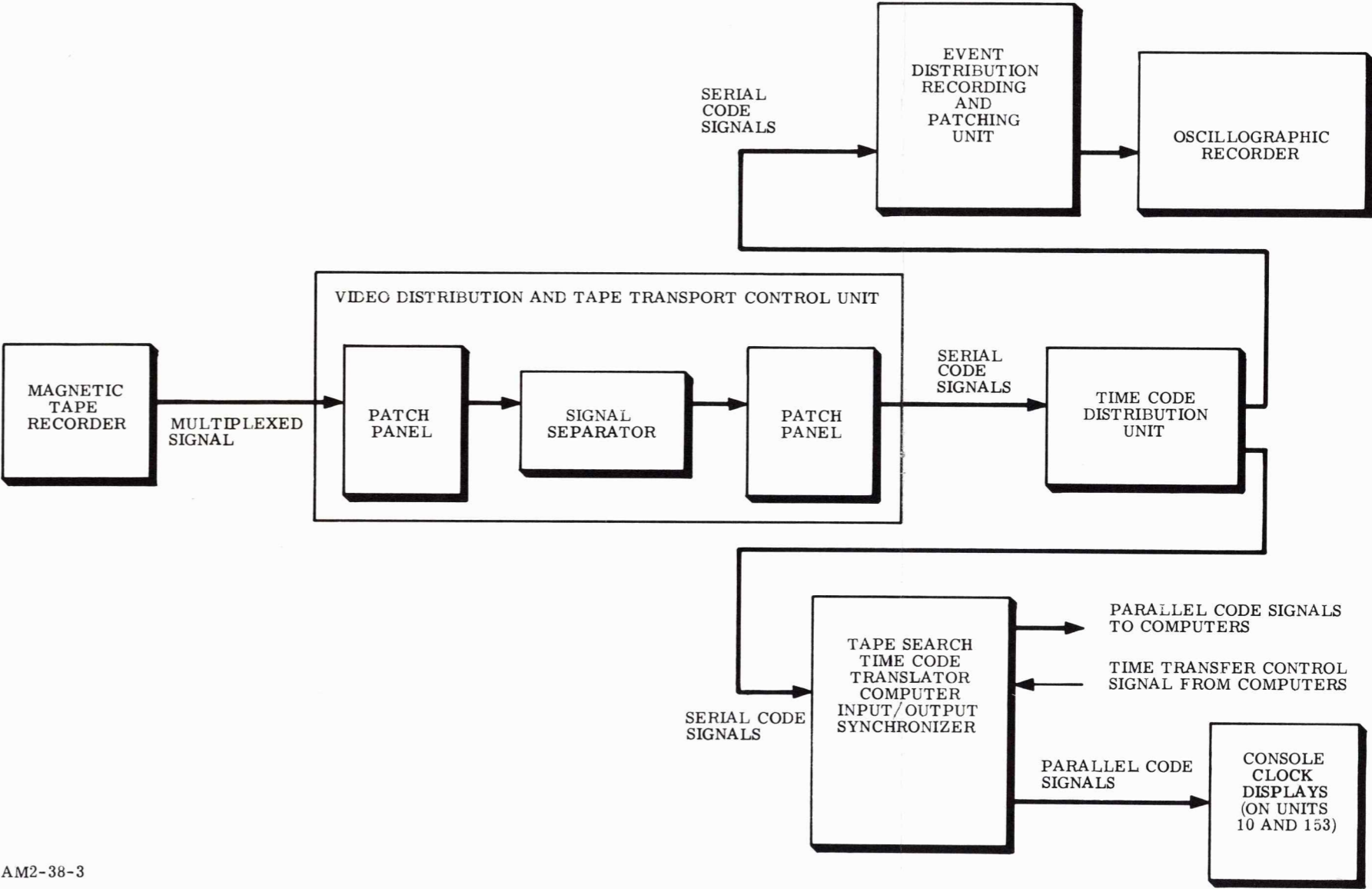
4-18. The setting of desired start count time may be accomplished at the Countdown Generator unit local control panel or by a remote control unit located on the Test Conductor Console. A visual display of current countdown time is available at both the local and remote control points.

4-19. PLAYBACK COUNTDOWN TIME DISTRIBUTION. The distribution of the played back countdown time code signal is illustrated in figure 4-6. When it is necessary to use playback (reproduced) information stored on tape by the magnetic tape recorders, the tape channel output



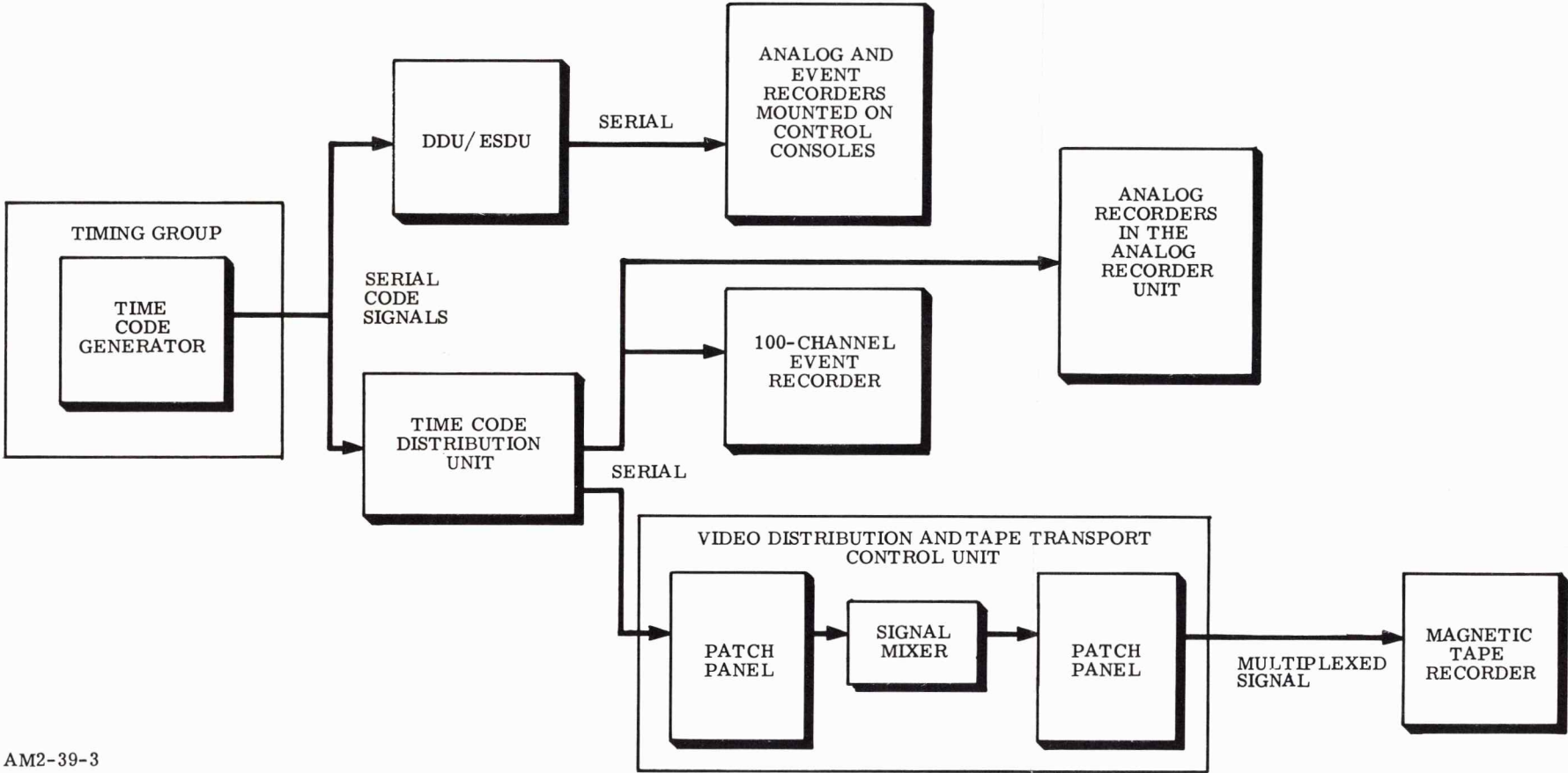
AM2-37-3

Figure 4-1. IRIG B Real Time Distribution Block Diagram



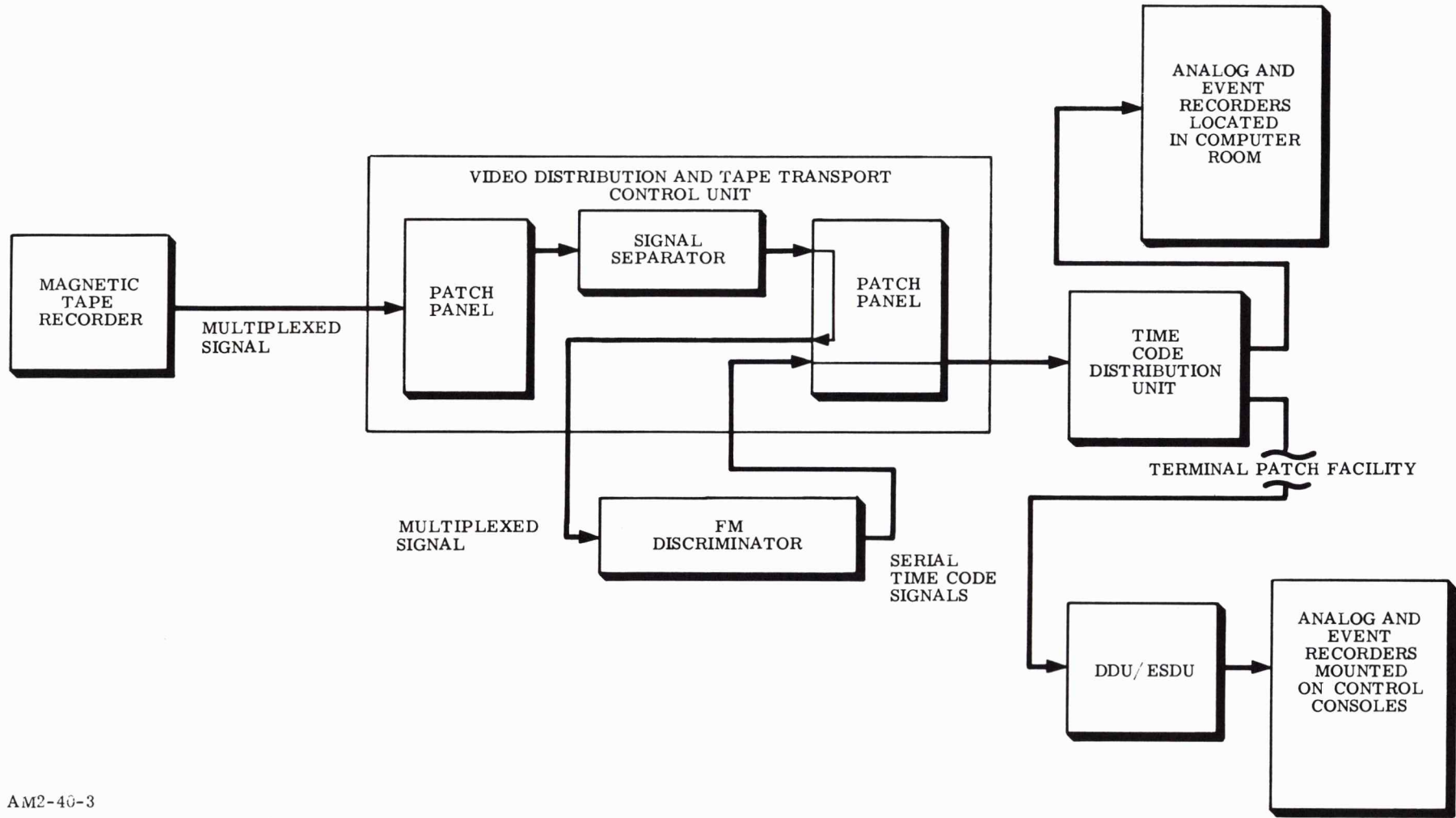
AM2-38-3

Figure 4-2. IRIG B Playback Time Distribution Block Diagram



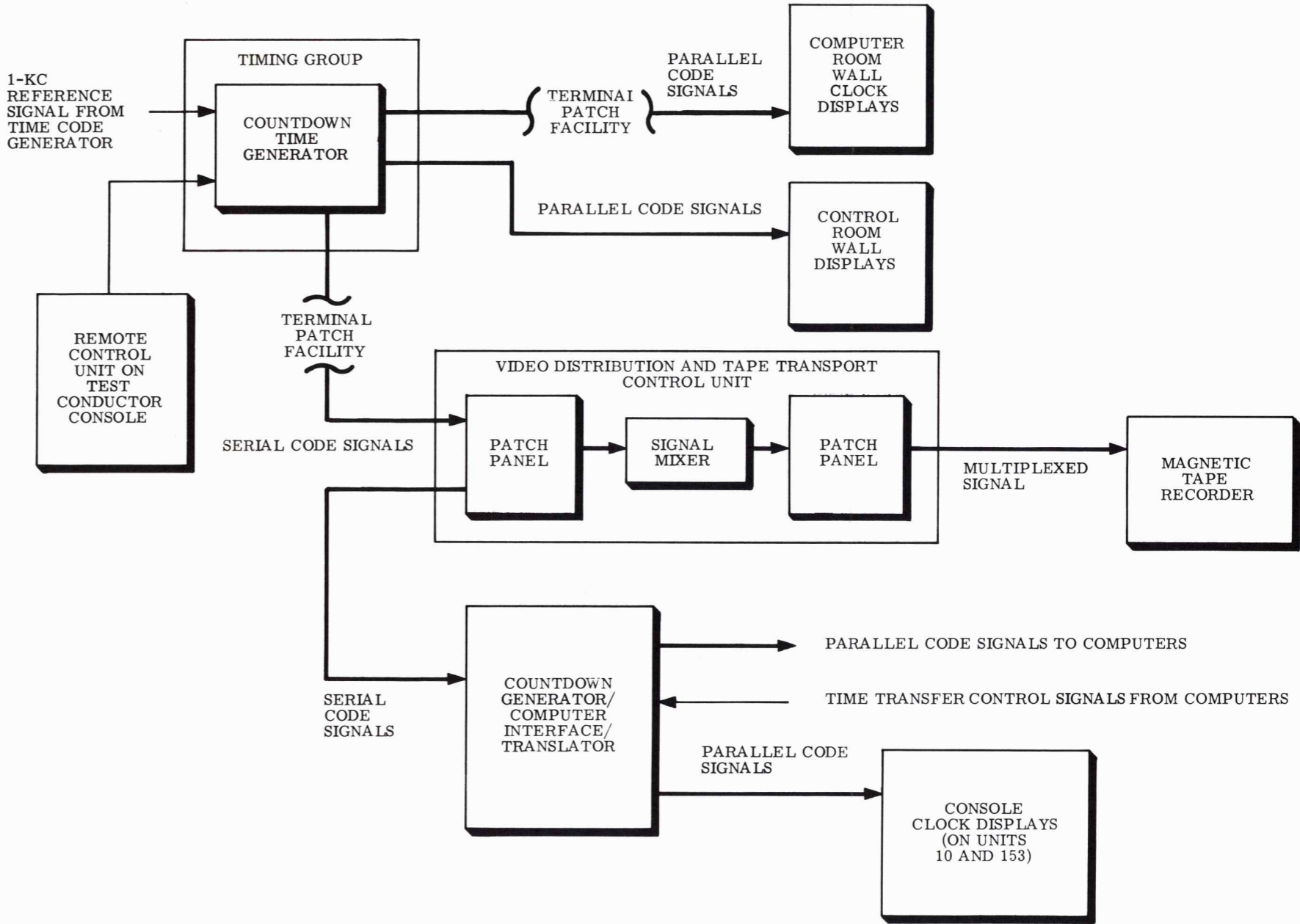
AM2-39-3

Figure 4-3. AMR B-1 Real Time Distribution Block Diagram



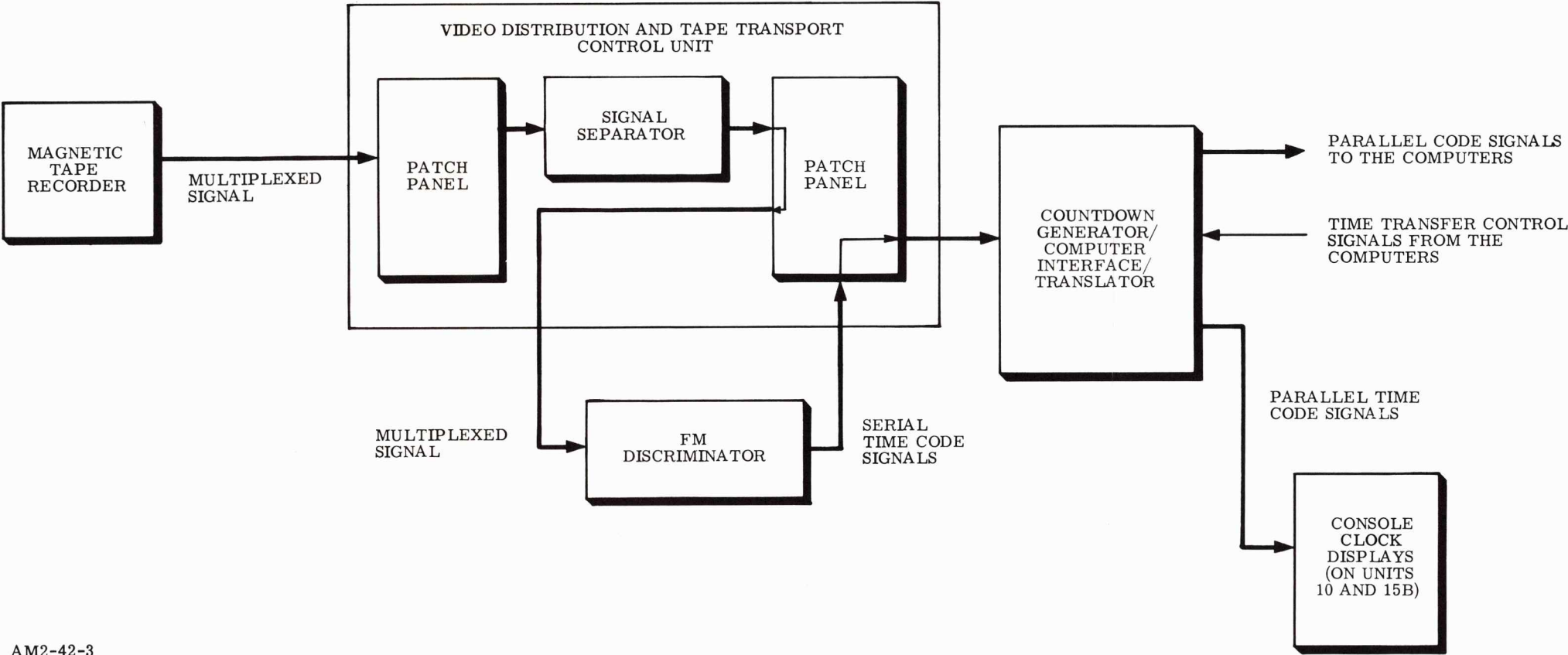
AM2-40-3

Figure 4-4. AMR B-1 Playback Time Distribution Block Diagram



AM2-41-3

Figure 4-5. Countdown Time Distribution Block Diagram



AM2-42-3

Figure 4-6. Playback Countdown Time Distribution Block Diagram

containing previously recorded countdown time code signals is fed to a Video Distribution and Tape Transport Control Unit patch panel. The countdown time code signals previously recorded were multiplexed with other miscellaneous data signals prior to being recorded by the magnetic tape recorders. The multiplexed playback signal is patched to the signal separator subassembly in the Video Distribution and Tape Transport Control Unit. The outputs of the signal separator are several selected data signals, and a multiplexed signal that contains the countdown time code signals as well as other miscellaneous information. This multiplexed signal is then routed by the Video Distribution and Tape Transport Control Unit to the appropriate FM discriminators located in the FM Discriminator Unit. The output of one of the FM discriminators is the demodulated serial countdown time code signal. The countdown time code signals are then routed to the Video Distribution and Tape Transport Control Unit, and thence to the Countdown/Computer Interface/Translator Unit. The Countdown/Computer Interface/Translator Unit converts the incoming serial countdown time code signals to parallel format and sends the parallel time code to the computers (both command and display) as required by the individual computer programs. The serial countdown time code signals are also converted to a parallel format suitable for display on a Computer Complex Console clock and a Test Conductor Console clock.

4-20. TIME CODE GENERATOR.

4-21. The Time Code Generator provides the IRIG B and AMR B-1 time codes for the use of the computers, recorders, and various time displays. All codes are generated in dc level-shift form. Amplitude modulation of a 1-kc sine wave by any of the IRIG B codes is provided. Timing pulse rates are also available. These consist of rectangular waveforms at specified frequencies.

4-22. Controls are provided with which a binary coded decimal "word" may be placed in the output time code. This word identifies the particular station generating each code.

4-23. TIME CODE GENERATOR FUNCTIONS.

4-24. The generator is made up of a system clock, a clock control, minor and major counters, days counter, and code format generators. (See figure 4-7.)

4-25. SYSTEM CLOCK. The system clock provides 100-kc pulses that will be counted to form output clock pulses. The clock circuits comprise:

- a. Internal/External Time Base. The Internal/External Time Base contains an internal, one-megacycle oscillator and the facilities whereby either a one-megacycle or a 100-kilocycle source may be provided externally.

- b. Signal Shapers and DCU. The one-megacycle time base (internal or external) is fed into a sine-to-square-wave shaper. The square-wave output of this device is then used to

clock a divide-by-ten decimal counting unit (DCU). The 100-kc output of this DCU is then shaped into a sine wave by a square-to-sine-wave shaper. The resultant 100-kc sine wave (or the external 100-kc sine wave) is then routed to the resolver and phase-shift circuit.

c. Resolver and Phase-Shift Circuit. The resolver and phase-shift circuit provides a means whereby the phase of the 100-kc sine wave signal may be continuously shifted. This allows precise synchronization of the Time Code Generator to an external reference, such as WWV.

d. 100-KC Sine-to-Square-Wave Shaper. The phase-controlled signal from the resolver circuit is routed through a sine-to-square-wave shaper and amplifier. This circuit provides six-volt, sharp-rise-time pulses capable of clocking flip-flop circuits. The 100-kilocycle shaper provides 100-kilocycle phase one and phase two signals directly to the clock control circuits.

4-26. CLOCK CONTROL CIRCUITS. The clock control circuits provide gated 100-kc pulses, formed from the 100-kc signals received from the system clock. The clock control consists of:

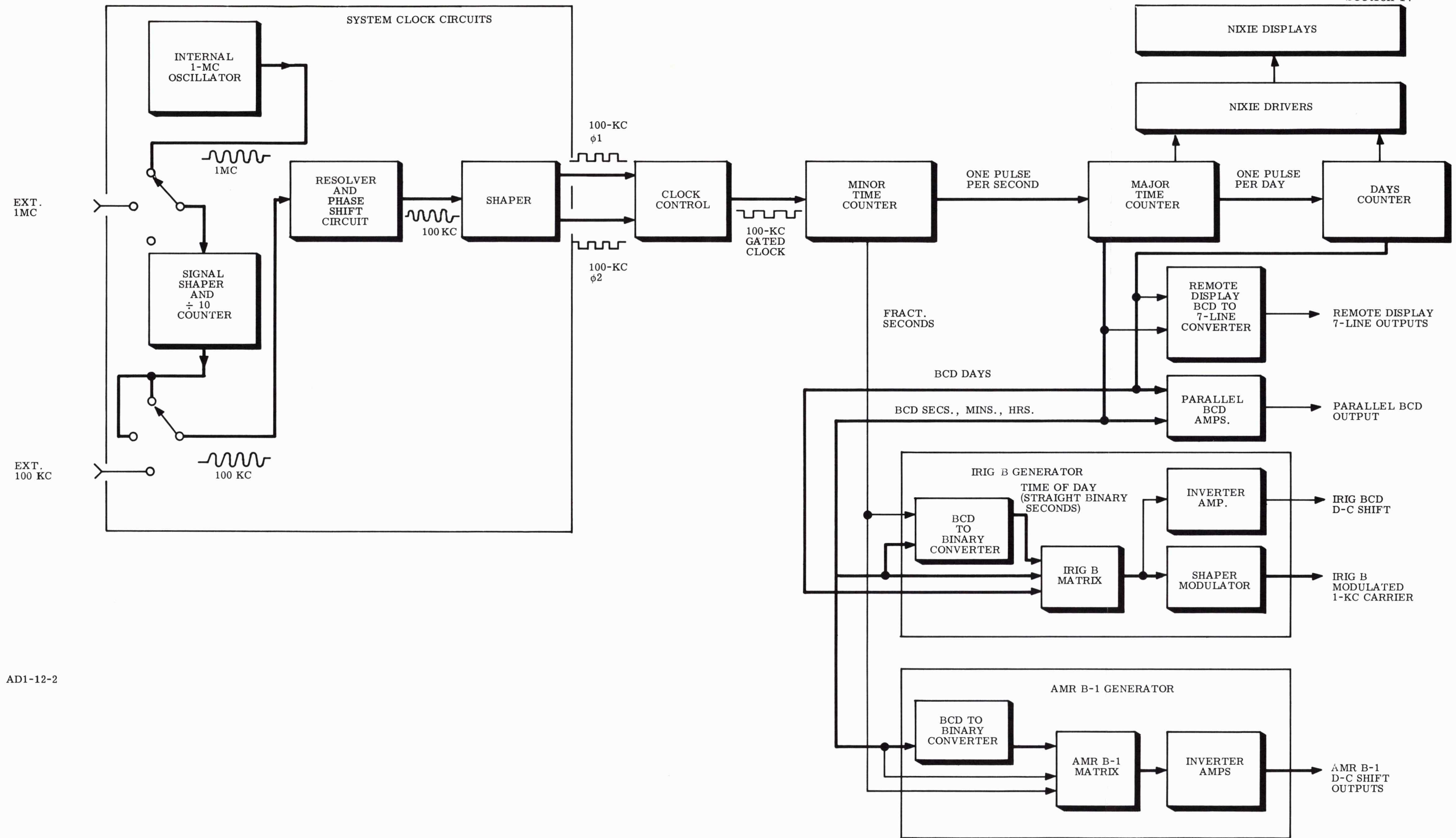
a. Advance/Retard Circuit. This circuit produces and controls 100-kilocycle gated clock pulses. The 100-kilocycle gated clock is formed from the 100-kilocycle phase one signals. The counter is advanced (speeded up) by adding 180-degree out-of-phase (phase two) pulses into the gated clock signal when the ADVANCE button is pressed. Selected phase one pulses are dropped out of the gated clock signal when the RETARD button is pressed. Thus, the clock may be speeded up, or slowed down, to allow coarse adjustments to be made during the synchronization of the generator with an external reference.

b. External Start-Arm, Start, Stop. Pressing the EXTERNAL START-ARM button sets a flip-flop that allows the 100-kilocycle gated clock signal to enter the minor counter when the flip-flop is triggered by an external start signal. The START button allows the 100-kilocycle gated clock signal to enter the minor counter whenever it is pressed. The STOP button, when pressed, disables the 100-kilocycle gated clock signal.

4-27. THE MINOR COUNTER. The minor counter flip-flops and decoders divide the 100-kilocycle clock down to a precision one-per-second pulse. This pulse is delivered to the major counter (clock dividers). Decimal decoded outputs of the minor counter are used in the tenth-second and one-second time frame code format matrices. Here they position pulses in the correct places in the codes.

4-28. The decoded zero time from each of the minor counters is routed through driver amplifiers to connectors on the rear panel. These are called pulse rate outputs. Driver amplifiers invert the negative-true decoded zero pulses.

Description



AD1-12-2

Figure 4-7. Time Code Generator Functional Block Diagram

- 4-29. THE MAJOR COUNTER AND DECODER. The major counter and decoders consist of permuted counters that count up to 23 hours, 59 minutes, 59 seconds and then reset to zero on the next one-per-second input pulse. This produces a one-per-day pulse that is counted by the days counter and decoders.
- 4-30. A RESET DISPLAY pushbutton allows the major counter (and the days counter) to be manually cleared to zero at any time. The decimal decoded outputs of the major counter are scanned by the one-minute and one-hour time frame codes to provide elapsed-time information to the code format matrices. This establishes correct bit placement in the time codes.
- 4-31. The decimal decoded outputs of the major counter are also applied to the nixie driver circuits, which supply ground connections to the days, hours, minutes, and seconds visual display nixie tubes.
- 4-32. DAYS COUNTER. The days counter will count to 399 days before resetting to zero. Therefore, a RESET DAYS pushbutton is supplied to allow the days counter and displays to be cleared to zero independently of the major and minor counters. This allows the days counter to be set to the correct time of the year at any time without disturbing the synchronism of the equipment.
- 4-33. CODE FORMAT GENERATORS. The code format generators accept elapsed time information from the counters to position the pulse information in each individual code format.
- 4-34. Pulse widths (such as binary ones, binary zeros, reference markers, index markers, etc.) are derived from the counters and converters by diode coincidence logic. The time of day and year is then placed in 1-2-4-8 BCD form by the elapsed-time diode coincident gates. These gates serially scan the counters to determine the state of each flip-flop.
- 4-35. IDENTIFICATION DATA TOGGLE SWITCH. Identification data toggle switches mounted on the front panel allow each generator to place a station identification code word (also in 1-2-4-8 BCD form) into the output time code. This code word can also be used as a control function, if required.
- 4-36. TIME CODE GENERATOR DESCRIPTION.
- 4-37. SYSTEM CLOCK CIRCUITS. The system clock circuits include the external/internal time base, phase shift network and resolver, control start-stop, advance-retard and display circuits.
- 4-38. Internal/External Time Base (See Figure 4-8). The internal/external time base produces and controls precision 100-kc clock pulses. It receives its input from an internal 1-megacycle oscillator, an external 100-kc sine wave signal, or an external 1-megacycle sine wave signal.

4-39. An internally mounted three-position switch selects either the internal 1-megacycle oscillator, the external 1-megacycle sine wave signal, or the external 100-kc sine wave signal.

4-40. The external 100-kc time base, when used, is sent through a buffer circuit, and then to the 100-kc phase shift network and continuous resolver.

4-41. The selected (internal or external) 1-megacycle sine wave signal is routed to the sine-to-square wave shaper. The amplified square wave output then goes through a 1-Mc divide-by-ten DCU. The nearly symmetrical square wave output of the counter is used to drive a filter-ringing network to generate a 100-kc sine wave output. This sine wave output is then directed to the 100-kc phase shift network and continuous resolver.

4-42. Phase-Shift Network and Continuous Resolver. The phase-shift network delivers a 90-degree out-of-phase signal to one leg of the resolver stator windings. The original 100-kilocycle signal is introduced at the other leg.

4-43. The rotor winding (operated by the 10 μ SEC/REV Control) is located in the fields produced by the two stator windings. Thus, the phase of the resultant output signal is a function of the position of the rotor winding.

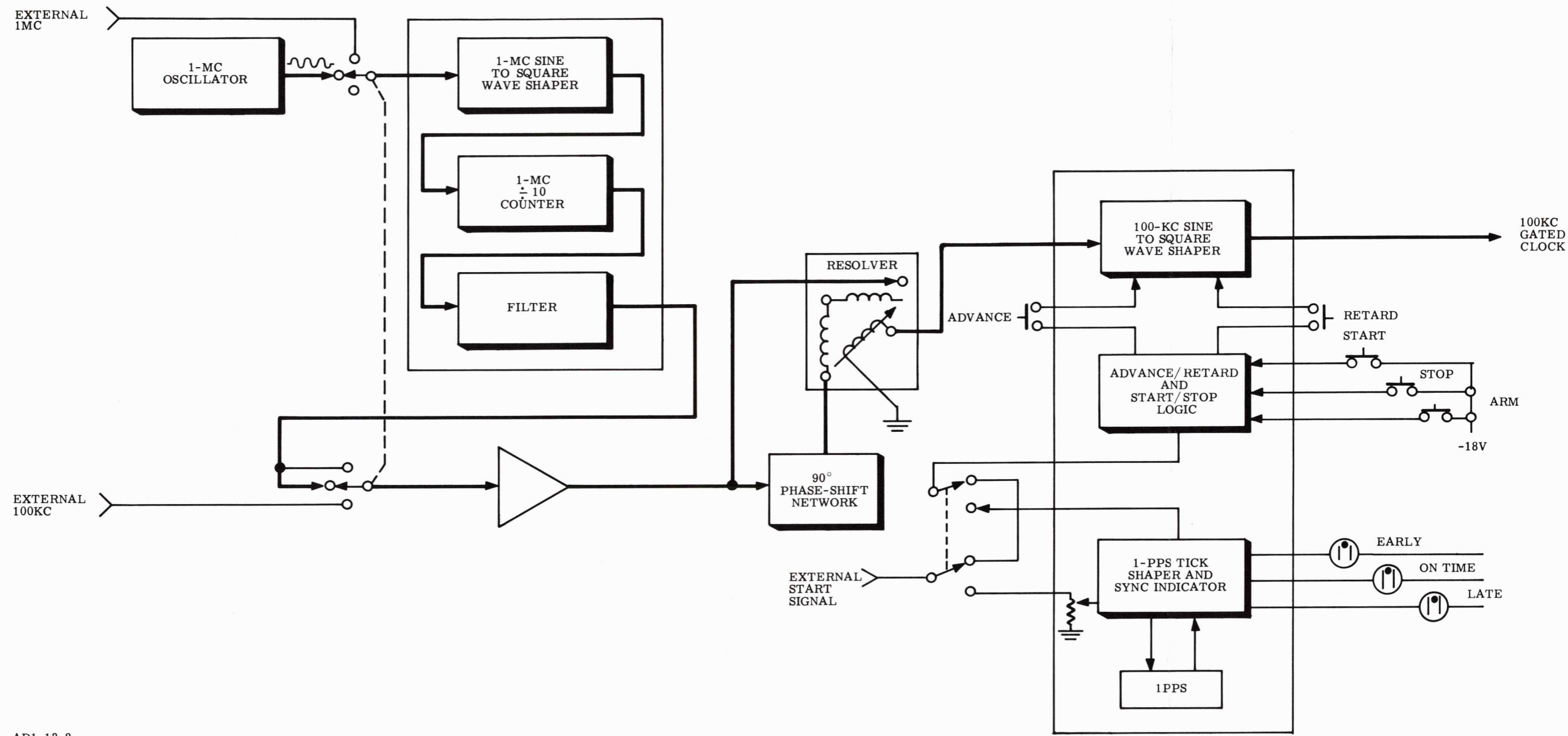
4-44. By rotating the 10 μ SEC/REV control through 360 degrees, the 100-kilocycle output signal may be made to lead or lag the input signal by 180 degrees. Thus, a fine adjustment of the Time Code Generator is provided, allowing it to be synchronized precisely to an external time standard such as WWV.

4-45. The output shaper transforms the 100-kilocycle sine wave from the resolver to a symmetrical square wave of the same frequency. This signal is differentiated and gated with the advance/retard circuitry to form the phase-two signal. This is supplied to the advance/retard circuitry.

4-46. Counter Control Start-Stop, External Start Arm. The 100-kc phase-one signal is ANDed with two control terms (START and RETARD). The output of this AND gate is then ORed with a control term (ADVANCE) to produce the 100-kilocycle gated clock signal.

4-47. The START control term operates a START flip-flop. This flip-flop is controlled by the STOP, START, and EXTERNAL START-ARM pushbuttons. When this flip-flop is reset, the START term is "true." This term allows the 100-kilocycle phase one signals to pass through the AND gate mentioned above.

4-48. The START pushbutton directly resets the START flip-flop. The STOP pushbutton directly sets this flip-flop, preventing the 100-kilocycle, phase one signal from passing through the AND gate.



AD1-13-2

Figure 4-8. System Clock Circuits Functional Block Diagram

4-49. The EXTERNAL START-ARM pushbutton sets an ARM flip-flop. This, in turn, allows the START flip-flop to be reset by the next positive-going external start signal.

4-50. The external START signal may be either a d-c shift signal, or a 1-kc time "tick" from a radio receiver tuned to a suitable source of timing signals. If the d-c shift signal is used, the signal is selected by the DC SHIFT/REC switch and applied to the START flip-flop.

4-51. If the 1-kc time "tick" is used, the signal is first conditioned and then coupled to the START flip-flop. With the DC SHIFT/REC switch in the REC position, the "tick" is routed to the REC LEVEL control. The output signal from the REC LEVEL control is filtered by a tick filter and coupled to a pulse shaper. The pulse shaper transforms the "tick" into a sharp, positive-going pulse of sufficient amplitude to reset the START flip-flop. A second output from the pulse shaper is routed to the synchronization indicator circuits. This output is monitored by the TICK indicator light.

4-52. Synchronization Advance-Retard. Synchronization advance-retard is accomplished by a sync flip-flop that generates pulses that are 10 microseconds wide. Each of these 10-microsecond periods contains one of the 100-kilocycle, phase one pulses and one of the 100-kilocycle, phase two pulses. The number of sync pulses generated each second is determined by the position of the MS/S rate switch.

4-53. The sync pulse controls AND gates which generate synchronization advance/retard pulses. These are then delivered to their corresponding pushbuttons. The advance pulses are made up of 100-kilocycle, phase two pulses which occur in between the 100-kilocycle, phase one pulses. The number of advance pulses that occur each second is determined by the setting of the MS/S rate switch. When the ADVANCE button is pressed, these out-of-phase pulses are ORed with the normal 100-kilocycle, phase one pulses to speed up the clock.

4-54. The retard pulses are false for selected pulses of the 100-kilocycle, phase one signal. The number of times each second that the retard pulses occur is also determined by the MS/S switch. When the RETARD button is pressed, these false pulses are ANDed with the basic 100-kilocycle, phase one pulses to produce pulse drop-outs at a rate determined by the MS/S rate switch. Thus the clock is slowed down.

4-55. Synchronization Indicators. Synchronization between the Time Code Generator and the external timing source is indicated by the SYNCHRONIZATION lights: EARLY, ON TIME, and LATE. The external timing source is used as a reference. If the Time Code Generator is running ahead of the external timing source, the EARLY light flashes. If the Time Code Generator is running in synchronism with the external timing source, the ON TIME light flashes. Similarly, if the Time Code Generator is running behind the external timing source, the LATE light flashes.

4-56. **MINOR AND MAJOR COUNTERS AND DISPLAY.** The major and minor counters consist of a series of decimal counting units (DCU's) that count the 100-kc gated clock. Two types of outputs are available from the DCU:

- a. Binary-coded-decimal (BCD) information.
- b. Decoded-decimal information.

4-57. **Minor Counter.** The minor counter consists of five divide-by-ten DCU's (decimal counting units), which are cascaded to divide the 100-kc input clock pulses down to a precision 1-pps. The last three DCU's are decimally decoded to provide scan-time information to the code format generators.

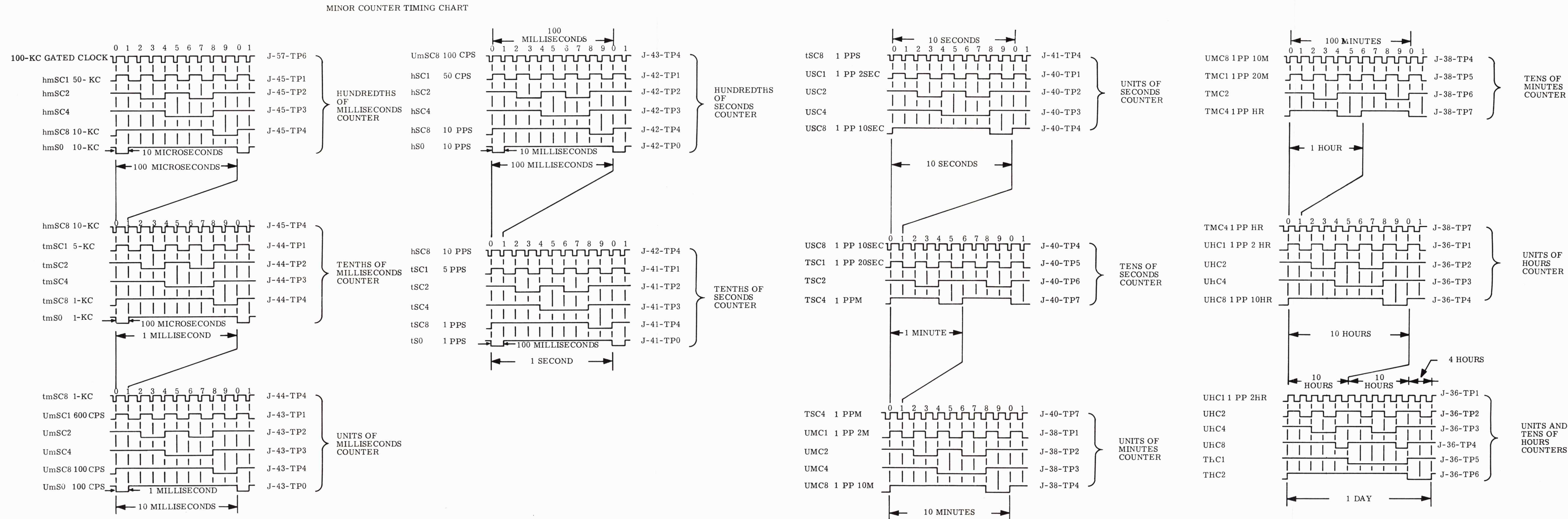
4-58. **Major Counter.** The major counter consists of six decimal counting units. These counting units divide and count in binary-coded decimal seconds, minutes and hours, the precision one-pulse-per-second from the minor counter. Three of the counters are divide-by-ten units: the units-of-seconds counter (USC), the units-of-minutes counter (UMC) and the units-of-hours counter (UHC). Two of the decimal counting units are permuted to recycle every sixth count: the tens-of-seconds counter (TSC) and the tens-of-minutes counter (TMC). The final counter is permuted to recycle every third count. This is the tens-of-hours counter (THC). Thus, USC and TSC recycle every 60 seconds, UMC and TMC recycle every 60 minutes, and UHC and THC are further permuted to recycle every 24 hours.

4-59. The outputs of the major counters are used to drive decoded nixie driver circuits. These, in turn, drive the nixies in the visual display. Some of the decimally decoded outputs of the major counter are also used to provide scan-time information to the one-minute and one-hour time frame codes.

4-60. **Timing.** The interrelationship of the individual counters (DCU's) in the major and minor counters may be seen by referring to figure 4-9. The waveforms of each flip-flop in each DCU are shown, along with the clock input to each DCU (each new clock input being the output of the previous DCU). Where applicable, the decimally decoded outputs are also shown. These outputs divide the count of the DCU into ten equal parts, wherein the leading edges of all of the decoded zero terms are on time.

4-61. **Manual Advance.** Six front-panel-mounted pushbuttons are provided. Each button, when pressed, individually clocks the major counter DCU under which it is mounted. The Time Code Generator can be stopped by pressing STOP, then reset to zero by pressing RESET DISPLAY. It may then be preset to any time via the MANUAL ADVANCE buttons.

4-62. **Reset Display.** When the front-panel-mounted master RESET DISPLAY pushbutton is pressed, the display and the major counters are reset to all zeros.



AD1-14-2

Figure 4-9. Major and Minor Counter Timing Diagram

4-63. DAYS COUNTER AND DISPLAY. The days counter counts the precise one-per-day major counter pulses to produce BCD days information. This can then be placed in the generated time codes. The 1-2-4-8 BCD counters are also decimally decoded to drive nixie drivers which, in turn, drive the units, tens and hundreds-days visual display.

4-64. A units-of-days counter counts the one-pulse-per-day output and divides it by ten to produce one-pulse-per-10-days pulses. The tens-of-days counter divides these pulses by ten to produce one pulse per 100 days.

4-65. A hundreds-of-days counter consists of two binary counters. The true output of each counter is ANDed with outputs from the units-of-days and tens-of-days counters, to generate a reset signal at the count of 364, 365, or 366 days. This reset can be changed by means of a metal pin that is manually inserted through two test points.

4-66. A separate RESET DAYS pushbutton is provided to allow the days counter to be reset at any time without disturbing synchronization of the rest of the Time Code Generator. Separate MANUAL ADVANCE pushbuttons are provided for each of the three decades of the days counter to allow manual setting of the counters to any desired indication. The master RESET DISPLAY pushbutton, which resets the major counter, also resets the days counter.

4-67. IRIG B GENERATOR. The IRIG B code is made up of the following (see Figure 4-10):

- a. A reference marker, eight milliseconds wide. The leading edge of the reference marker defines the beginning of each second and of the time frame.
- b. Ten position identifiers, eight milliseconds wide. A position identifier occurs during the last tenth of each section of the time frame. Note that only two eight-millisecond-wide pulses, PO and the reference marker, occur consecutively. This facilitates locating the beginning of a time frame when visually scanning the time code format, such as on a strip chart.
- c. Two-millisecond-wide index markers, which occur at a basic rate of 100 pps at the beginning of every hundredth-second division of the time frame not occupied by the above-mentioned pulses, or "one" bit weights. Thus, the index markers also indicate a "zero" bit-weight in the code.
- d. Nine code "words" in 1-2-4-8 binary-coded-decimal form. This word allows station identification in accordance with the setting of the four front-panel toggle switches, marked IDENTIFICATION DATA.
- e. One code "word" in straight 17-bit binary form which indicates the time of the day in straight binary seconds form.

4-68. The generator that forms this code consists of a BCD-to-binary converter, an IRIG B matrix, an inverter amplifier, and a shaper modulator.

4-69. BCD-to-Binary Converter. This converter must, for the IRIG B format, change the binary-coded decimal readout of the time of the day in hours, minutes, and seconds to straight binary notation of the time of the day in seconds. The binary-coded decimal-to-binary converter, designed for this purpose, operates as described in the following paragraphs and illustrations.

4-70. The system clock reads out time in 1-2-4-8 code individually for hours, minutes, and seconds. To translate this time to straight binary notation, the arbitrarily assigned weights of eight, four, and two must be decoded to straight binary and must be converted, from hours and minutes, to seconds.

4-71. Upon command of a fill clock pulse, the flip-flops of the fill register are loaded with the contents of the clock and assume the same configuration.

4-72. The next command pulse is shift. At the arrival of this pulse, the entire contents of the fill register are divided by two. This is accomplished by shifting to the left the state of each binary decade counting unit.

4-73. Note, however, that the value of the smallest digit of any decade counting unit is not divided by two when it shifts to the next smaller decade counting unit. It will, rather, assume a larger value in terms of the decade counting unit that it enters. For instance, when a decimal one in the flip-flop representing the tens-of-hours counter shifts to the left into the units-of-hours counter, rather than being divided by two, it changes from a value of ten hours to a value of eight hours and three must be subtracted from it to reduce it to a value of five (half of ten).

4-74. When a decimal one in the tens-of-minutes counter shifts to the units-of-minutes counter, it, too, shifts from ten to eight minutes rather than being divided by two; it changes from a value of ten hours to a value of eight hours and three must be subtracted from it to reduce it to a value of five (half of ten).

4-75. When a decimal one in the tens-of-minutes counter shifts to the units-of-minutes counter, it, too, shifts from ten to eight minutes rather than to five minutes. Three must be subtracted from the decade value if it is to be divided by two.

4-76. When a decimal one in the units-of-minutes counter shifts to the tens-of-seconds counter, it changes from a value of 60 seconds to a value of 40 seconds, and ten seconds must be subtracted from it.

4-77. When a decimal one in the tens-of-seconds counter shifts to the units-of-seconds counter, it assumes a value of eight seconds and three must be subtracted from it.

Figure 4-10. IRIG B Time Code Format

4-78. All of the necessary weight-adjustments described in the preceding paragraphs are accomplished by the conversion logic. This is commanded by a convert pulse that appears one-half millisecond after the shift pulse. Twenty times the three processes are repeated to complete one cycle for each second. When the cycle is complete, the binary accounting of time in seconds is jammed into the output register, aligning it with the binary-coded decimal system clock.

4-79. Converter Output Register. A register (or memory) is required to permit each one of the 20 steps to be stored until the process is finished. The output register contains 17 bits. Therefore, 17 flip-flops are required.

4-80. Considering the shift-to-divide procedure, the contents of the fill register shift from right to left and, in order of increasing significance, leave the fill register. As the least significant digit moves to the left one flip-flop, the flip-flop it leaves is idle.

4-81. A method is used whereby, as the least significant digit is shifted out of the fill register, it re-enters the most significant bit of the same fill register. Thus the fill register is also used as a storage register.

4-82. Four milliseconds after the last convert clock pulse, the transfer clock pulse causes the contents of the fill register to be loaded into the output register, thus aligning it with the readout of the binary-coded decimal system clock time.

4-83. No further action takes place in the conversion circuit until the next fill pulse appears at the beginning of the next one-second period.

4-84. Clock Pulser for Binary Converter. The clock-pulser provides the fast rise pulse necessary to trigger flip-flops and other circuits that require a trigger input. It produces a positive-going pulse of about 5 volts amplitude and 2 microseconds duration, triggered by the trailing edge of -5-volt input pulse.

4-85. Decoder Timing Logic. This module supplies the timing logic needed for the binary-coded-decimal-to-binary converter.

4-86. IRIG B Code Format Matrix. The IRIG B code is produced in a -6-volt to 0-volt dc level-shift form. The code is formed using negative true logic, then inverted to produce positive-true pulses which can be accepted by a shaper modulator circuit. This circuit produces, in turn, an amplitude-modulated, 1-kc, sine-wave carrier.

4-87. The IRIG B code is contained in a one-second time frame and is produced at a rate of 100 pulses per second. The code can be broken down into ten sections (each one-tenth-second long). These sections correspond to the decimally decoded fractional-second outputs of the minor counter. Each section can be further divided into ten one-hundredth-second

divisions. These also correspond to the decimally decoded fractional second outputs of the minor counter. Coincidence gates (AND gates) are used to position the pulses in the correct sections and divisions of the time frame.

4-88. Formation of BCD Time. BCD seconds, minutes, hours, and days are formed by AND gates that scan the outputs of the major and days counters. Outputs of the minor counter are used to properly position the time data.

4-89. Formation of the Control Functions. The control functions (CF) logic operates similarly to the BCD time logic. Four AND gates scan the IDENTIFICATION DATA switches mounted on the front panel. The station identification data is placed in the first four divisions of the sixth section of the time frame.

4-90. Formation of the Straight Binary Seconds Time of Day. The BCD-to-binary near the beginning of each second, converts the BCD seconds, minutes, and hours information into straight binary seconds. It stores this information in a register until the next second.

4-91. Seventeen AND gates scan the BI-DEC register and position each binary bit in its correct division. The outputs of these AND gates are grouped according to sections in which they appear on the time code format.

4-92. Modulated Output Circuit. The Time Code Generator presents 1-kc carrier-modulated outputs of the time codes that it creates. The modulated outputs are created by a square-wave generator, a sine wave shaper and modulator cards.

4-93. The square-wave generator receives its timing signals from the minor counter and uses these to generate a 1-kc symmetrical square wave.

4-94. The square-wave generator is set and reset by a 10-kc trigger. The triggering of the flip-flop is controlled by inhibit signals. The resultant symmetrical 1-kc output is applied to the sine-wave shaper.

4-95. The shaper modulator circuit converts the square-wave generator output into sine waves and amplitude-modulates it with the time code. The sine-wave shaper circuit consists of three twin-T filters, two low-pass filters, two high-pass filters, and the output amplifier. The twin-T filters reject the third, fifth, and seventh harmonics; the low-pass filter further rejects these harmonics as well as the harmonics of a higher order.

4-96. The output of the sine-wave shaper and the dc shift code outputs of the code matrices are applied to the modulator. The modulator itself consists of a voltage divider operated by a transistor switch. The switch operates in such a manner as to amplify, in a three-to-one ratio, those segments of the sine-wave signal that would fall within the square-wave envelopes of the incoming time code pulses.

4-97. AMR B-1 GENERATOR. The AMR B-1 time code is made up of:

a. A 20-second reference marker which consists of one 0.800-second-wide bit. On time occurs at the leading edge of this marker. The reference marker defines the beginning of each time frame.

b. Three words in binary format give the time of day in seconds, minutes, and hours.

c. "Zero" is a 0.200-second-wide pulse. "One" is a 0.600-second-wide pulse. The leading edge of the code pulses are synchronized to the positive-going zero axis crossings of the code carrier.

4-98. The generator that forms this time code comprises a BCD-to-binary converter, an AMR B-1 matrix, and inverter output amplifiers.

4-99. AMR B-1 BCD Binary Conversion. The BCD-to-binary converter converts BCD units-seconds and BCD tens-seconds into six bits of straight binary seconds. These have bit weights of 1, 2, 4, 8, 16, and 32 seconds, respectively. BCD minutes are converted in the same manner as seconds, resulting in weights of 1, 2, 4, 8, 16, and 32 minutes, respectively. Hours are similarly converted, except that hours have only five bits, weights of 1, 2, 4, 8, and 16 hours.

4-100. The conversion is accomplished by using diode matrice gates except in the case of zero seconds, minutes, and hours.

4-101. AMR B-1 Code Format Matrix. The AMR B-1 code is produced in a -6-volt to 0-volt dc level-shift form. The code is formed using negative true logic. It is then inverted by output drivers.

4-102. This code is contained in a 20-second time frame and is produced at the rate of one pulse per second. The code is a 17-bit binary seconds, minutes, and hours time code. Since the code only occurs three times a minutes at 00, 20, and 40 seconds, it can be seen that the one- and two-second bit positions are not used. Diode coincidence gates are used to position the pulses in the correct sections and divisions of the time frame.

4-103. The reference marker is formed by a three-way AND gate. This is an eight-tenths-second-wide reference marker generated at 00, 20, and 40 seconds, the leading edge being on time.

4-104. Index markers are generated during the first 2/10 of each second. Since these markers are the same width as binary zeros, it is not necessary to generate binary zeros.

4-105. BCD-TO-SEVEN-LINE CONVERTER LOGIC. The BCD-to-seven-line converter logic converts the BCD outputs of the major counter to seven-line-type parallel outputs.

These are used for driving the seven-line displays. Figure 4-11 shows the outputs of the BCD-to-seven-line converter.

4-106. **PARALLEL BCD OUTPUTS.** This unit presents the true outputs of the major counter (seconds, minutes, hours, and days) as zero and -6-volt levels at rear-connector panel J64. The true outputs of the counters are applied to noninverter amplifiers (on 12007 circuit cards). The outputs appear as 0 volts for a binary zero and -6 volts for a binary one.

4-107. COUNTDOWN TIME CODE GENERATOR.

4-108. The Countdown Time Code Generator, located in the timing group, provides a special ACE-S/C countdown time code for the use of the computers, recorders, and time displays. The code is generated in dc level-shift form. Local and remote control are provided for manually controlling the count start time.

4-109. **COUNTDOWN TIME CODE GENERATOR FUNCTIONS.**

4-110. The Countdown Time Code Generator (figure 4-12) consists of five major functional sections: the minor counter, the major counter, the local (nixie) display, the countdown time code word generator, and the remote display converter. The following paragraphs describe the functions of each of these major functional sections.

4-111. An external 1-kc clock signal, from the Time Code Generator, enters the countdown generator and is coupled through an input signal reshaper to the counting circuits. The minor counter utilizes three decimal counting units (DCU) to divide the 1-kc clock signal to a precise one-pulse-per-second signal. This signal is routed to the major counter. The outputs of the flip-flops of the hundredths and tenths DCU's are decoded by eight-to-ten-line converters. These flip-flop outputs and decoded terms are the minor clock pulses from which the time code is generated.

4-112. The major counter counts and stores as elapsed time the precise 1-pps output from the minor counter. The major counter is composed of five decimal counting units and two divide-by-six counters. These seven counters can count either up or down as determined by sign-control logic. The sign-control logic condition is a function of operator control settings and the counter content. The desired start count, including the sign, is entered by the operator on thumbwheel digital switches. The count is transferred from the thumbwheel switches to the counter by depressing the PRESET switch, and the counter begins counting when the COUNT switch is depressed. The sign displayed and the direction of count is a function of the operator's choice of start count, until the time count reaches zero. At this time the major counter will automatically start counting up and display the + sign.

4-113. Both local and remote controls are provided for manually controlling the start count and operation of the major counter.

4-114. The BCD coded outputs of the major counter are the driving signals for the local (nixie) display, the remote display converter, and the countdown time code word generator. The BCD outputs from the major counter are converted into nixie display control signals by a BCD-to-decimal converter. The nixie display is located on the front panel of the Countdown Time Code Generator. The remote display converter uses the BCD outputs from the major counter to produce the seven-line code signals which are used to drive the remote time-display devices.


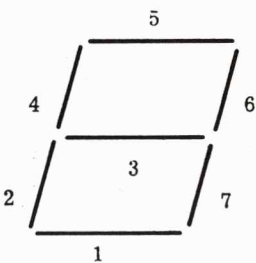

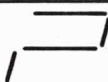





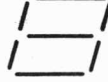

4-115. The countdown time word generator produces a special ACE-S/C countdown time code in d-c shift serial form. The d-c shift serial time code is formed by using scan matrices. These matrices scan the flip-flops in the minor and major counters and logically generate the code information bits (mark pulses). The matrix output pulses are then serialized to form the time code envelope. The time code envelope is then routed to a shaper/modulator circuit to amplitude-width modulate a 1-kc sine-wave carrier. This modulated carrier is routed to the Video Distribution and Tape Transport Control Unit for distribution.

4-116. COUNTDOWN TIME CODE GENERATOR DESCRIPTION.

4-117. MINOR COUNTER. The input signal reshaper (two inverter-amplifiers) provides the proper line termination for, and reshapes, the input signal (figure 4-13). The input signal is a 1000-pps square wave that rises from a -6-volt baseline to ground. The frequency of the external input signal may be speeded up or slowed down for test purposes. The maximum allowable input frequency is 10,000 pps.

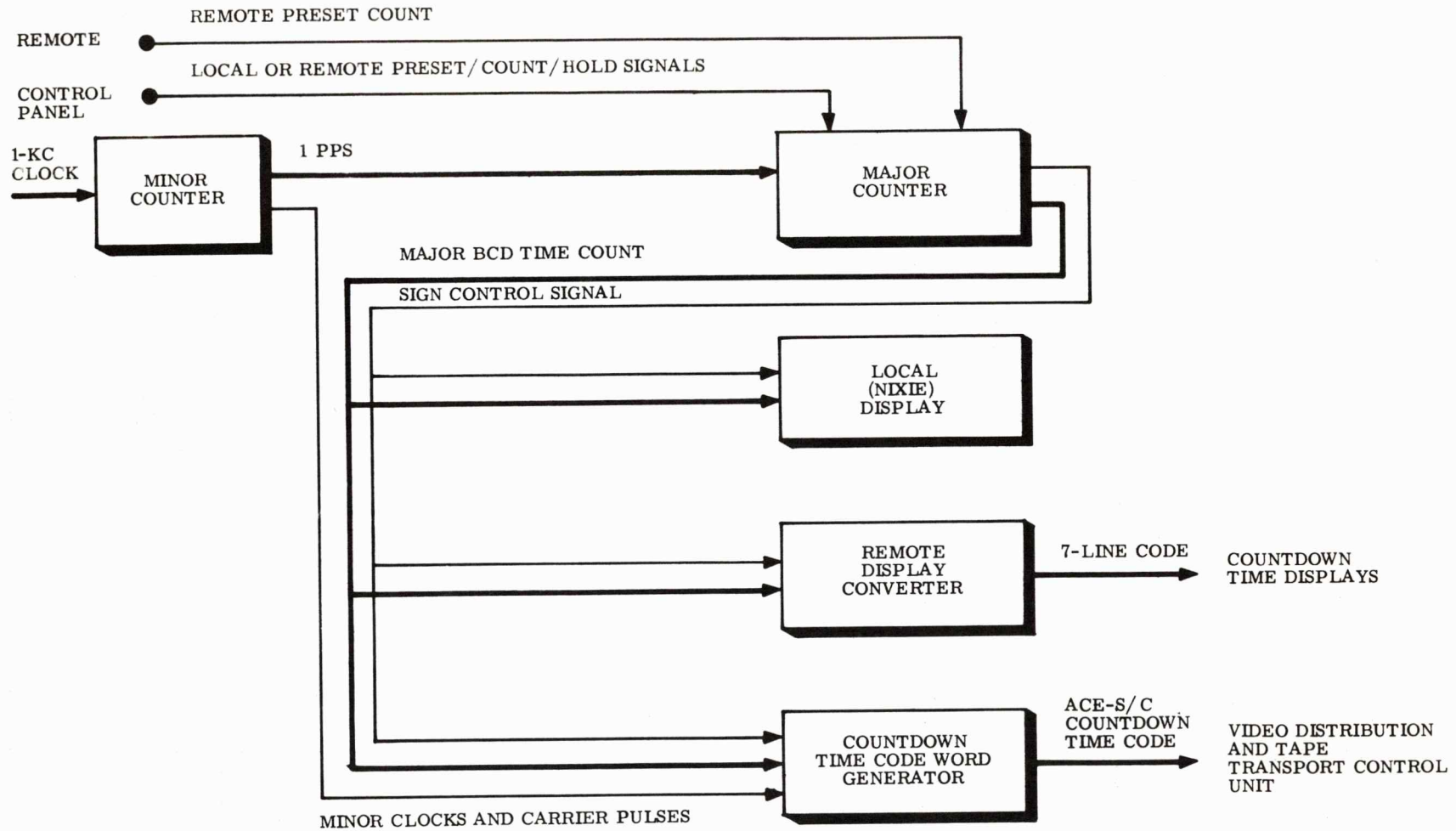
4-118. Three 1-2-4-8 BCD counters permuted to divide-by-ten are connected in cascade and divide the 1000-pps inputs by 1000. The 1-pps output of these counters clock the units-of-second counter of the major counter. The 1-2-4-8 terms of the minor counter are decoded from BCD to decimal or ten-line code. Flip-flop output pulses and decoded terms from the minor counter are the minor clock pulses used to produce the time code word. All three of these counters are reset to zero when either the local PRESET or the remote PRESET push-button is pressed. The 1000-pps square wave output from the input signal reshaper is routed to the countdown time code word generator, where it is reshaped to provide the output carrier.

4-119. MAJOR COUNTER. The major counter consists of a group of up/down counters and the controls and circuits necessary to establish a start count and control the advance, direction of count, and output of these counters.

DECIMAL	BINARY CODE				7 LINE CODE							CHARACTER DISPLAY	CHARACTER
	1	2	4	8	1	2	3	4	5	6	7		
0	0	0	0	0	1	1	0	1	1	1	1		
1	1	0	0	0	0	0	0	0	0	1	1		
2	0	1	0	0	1	1	1	0	1	1	0		
3	1	1	0	0	1	0	1	0	1	1	1		
4	0	0	1	0	0	0	1	1	0	1	1		
5	1	0	1	0	1	0	1	1	1	0	1		
6	0	1	1	0	1	1	1	1	1	0	1		
7	1	1	1	0	0	0	0	0	1	1	1		
8	0	0	0	1	1	1	1	1	1	1	1		
9	1	0	0	1	1	0	1	1	1	1	1		

AD1-11-1

Figure 4-11. Display Converter Coding



AD4-1-1

Figure 4-12. Countdown Time Code Generator Simplified Block Diagram

4-120. Up/Down Counters. The up/down counter circuits consist of flip-flops and diode gates arranged in a configuration that counts input pulses in an up or down direction, depending upon the voltage of a control signal. The control signal is generated by a flip-flop in the signal control logic.

4-121. The up/down counters can be side-loaded to a specific count by pullover signals from the START TIME digital switches and advanced by count or carry pulses. In the case of the units-of-seconds stage, the advance is controlled by the 1-pps update pulse from the minor counter. The tens-of-seconds through hundreds-of-hours stages are advanced by carry pulses from the preceding stages.

4-122. Sign Control Logic. The sign control logic contains the flip-flop which produces the up/down count control signal.

4-123. When the flip-flop is in the true state, the counters are set into the Up Mode. The flip-flop is reset (into the false state) or set (into the true state) by the \pm output of the thumb-wheel switch. The flip-flop is also set true when the count has progressed in a down direction to 000 hours, 00 minutes, 00 seconds. This count is detected by a zero detector that is on each counter card. When the count of 000 00 00 has been reached, the sign control flip-flop is set true, the counters shift into the Up mode, and the count progresses in the up direction.

4-124. Start Time Switches. The start time digital switches use an integral circuit to select the binary-coded-decimal term that corresponds to the number displayed by the switch control. The \pm switch produces two terms that may be coded as plus or minus. The output of the \pm switch directly controls the state of the sign control logic as described in the preceding paragraphs.

4-125. The outputs of these digit-selecting switches are connected to the side-load inputs of the up/down counter flip-flops. When the PRESET switch is pressed, -18 volts are connected to the common input terminal of the START TIME switches. This voltage, routed to the counters, side-loads the BCD equivalent of the decimal numbers displayed on the faces of the switches into the counter flip-flops.

4-126. Count-Hold Circuits. In the Hold Mode, only the major counter is stopped. The minor counter continues to count and generate the time code word. Only the low-order flip-flop is stopped in order to prevent the major counter from advancing.

4-127. In order to prevent a spurious pulse, when going from the Hold to the Count Mode, the low-order flip-flop is disabled by grounding either the true or false output, instead of gating the input line.

4-128. The COUNT and HOLD controls that are active are determined by the REMOTE/LOCAL switch on the remote control assembly. The signals from the local COUNT and HOLD switches pass to the remote control panel and through the REMOTE/LOCAL switch. The signals of either the local or the remote COUNT and HOLD switches return to the count-down generator from the remote control, to the count hold logic.

4-129. The timing of the count/hold control logic is arranged so that if the HOLD pushbutton is pressed during the first 980 milliseconds of a one-second period, the CDG will stop counting immediately. If the HOLD pushbutton is pressed during the last 20 milliseconds of a one-second period, the CDG will not hold until the end of that one-second period. This will prevent a remote translator from being out of step with the time in the ACE-S/C countdown time code.

4-130. COUNTDOWN TIME CODE WORD GENERATOR. Timing signals from the minor counter and time count, hold, and sign signals from the major counter are used to generate the ACE-S/C countdown time code.

4-131. The ACE-S/C countdown time code is a modification of the standard IRIG B Time Code. (See figure 4-14.) Countdown time in seconds, minutes, and hours is represented in BCD 8-4-2-1 form. One bit is also included for plus or minus and one bit for count or hold. Two formats are actually used. During the Countup (+) Mode, the time is scanned, least-significant bit first, for each subword. In the Countdown (-) Mode, the format is scanned, most-significant bit first, for each subword.

4-132. Time Code Scanners. To generate the time code, the major counter output terms are converted from parallel to serial form by the scanner code matrices. (See figure 4-15.) The serial, dc-shift time-code generated by the envelope generator modulates a sine wave carrier signal.

4-133. The several scanner matrices that convert the major counter terms to serial form operate similarly. To illustrate the conversion, the matrix that serializes the BCD seconds information will be described.

4-134. The units-of-seconds counter and the tens-of-seconds counter terms are scanned with minor clock pulses. Units-of-seconds counter and tens-of-seconds counter terms are each applied as inputs to AND gates. The second input to each of these AND gates is a minor clock pulse (decoded hundredths-of-seconds term). If the major counter term is a binary one (or true), the AND gate output is true and the scanner will emit minor clock pulses during the scan period.

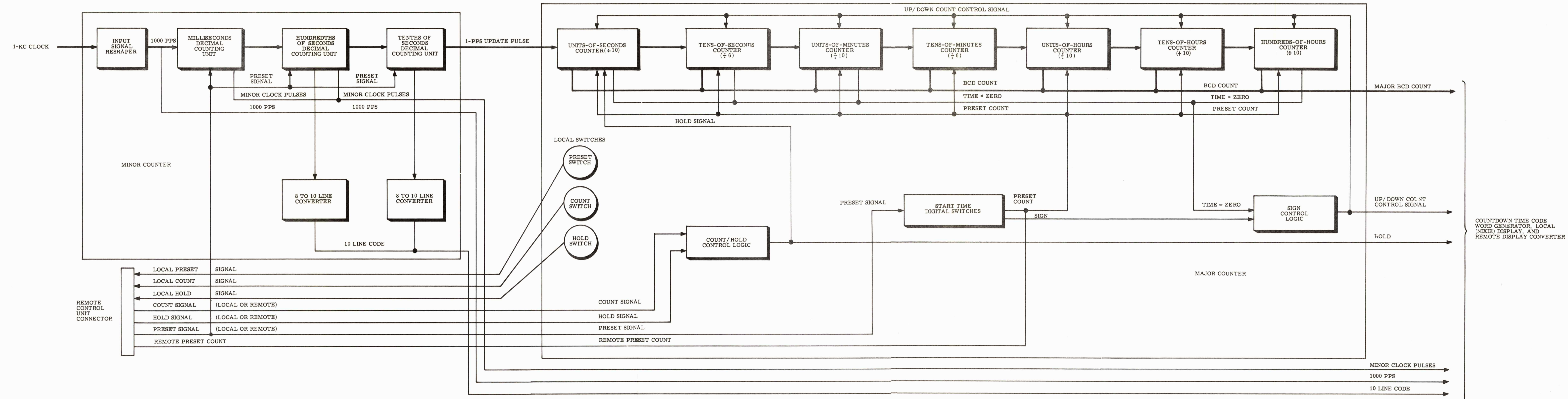
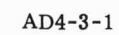


Figure 4-13. Minor and Major Counters Block Diagram



4-43/4-44

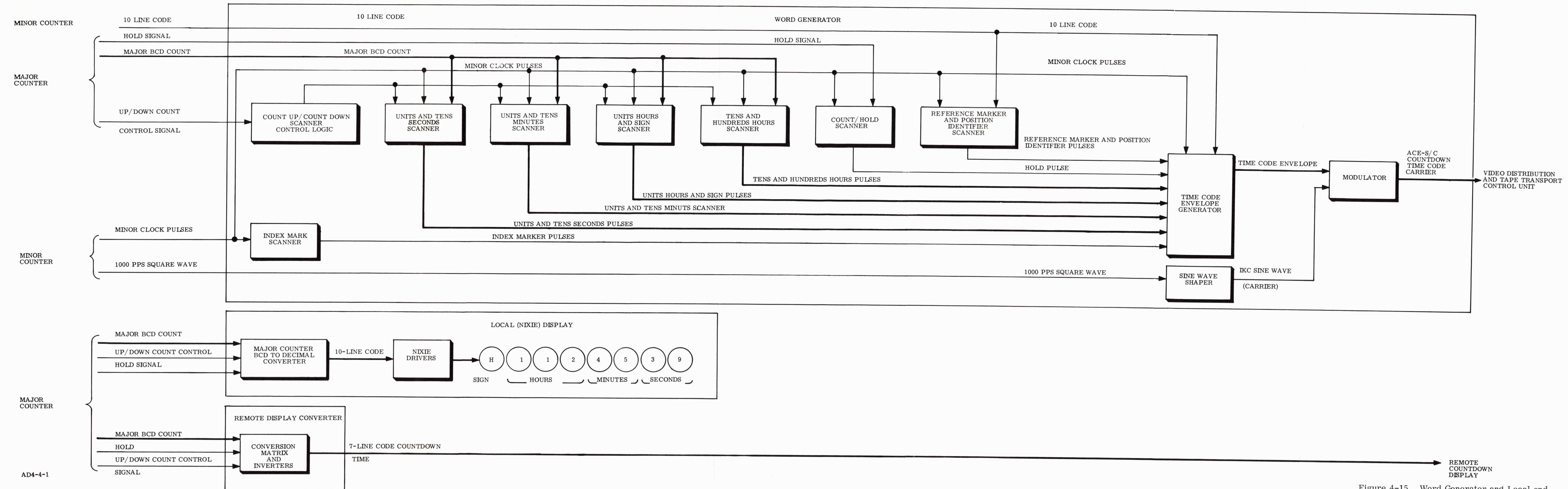


Figure 4-15. Word Generator and Local and Remote Display Circuit Block Diagram

4-135. Countup/Countdown Scanner Control Logic. To control the format of the time code, the countup/countdown scanner control logic uses the countup/countdown control signal from the sign control logic to reverse the scan sequence. There are two sets of AND gates for each decade in the scanners: one for countup and one for countdown. These AND gates are ORed together. The outputs of the AND gates are controlled by a reset driver that supplies pull down voltage to the appropriate gates during countup or countdown. These reset drivers change the time code word output format when counting up or down.

4-136. Time Code Envelope Generation. The combined outputs of the units-of-seconds matrix AND gates are inverted to form one input to a second AND gate. The other input term to this gate (a minor clock pulse) defines the first tenth-second of a time-code frame. The BCD seconds information is encoded during this time. If the major counter being scanned contains a zero, the matrix will emit minor clock pulses to the envelope generator.

4-137. The envelope generator is clocked (again by minor clocks) to generate a square-wave pulse 5 milliseconds wide unless it receives clock pulses from a scanner. The 5-millisecond pulses represent the BCD 1 in the time code format (figure 4-14).

4-138. The clock pulse output from a scanner matrix resulting from detecting a major counter BCD 0 will cause the envelope generator to produce a square-wave pulse only 2 milliseconds wide. This corresponds to the BCD 0 in the time code format. The envelope generator will emit BCD 1 or 0 pulses for the first half of the time-code frame as a result of the scanner inputs. If the time count is 0000000 the time code envelope will consist of a series of 2-millisecond (BCD 0) pulses.

4-139. Index Mark Scanner. The envelope generator must be provided with input signals in order to produce any output pulses. Since no count is scanned during the last half of the time-code frame, input signals are provided to the envelope generator to cause generation of index markers. This is the function of the index mark scanner. The index mark scanner consists of a reset driver and an input matrix to which minor clock pulses are applied. During the last half of the frame, these clock pulses cause the index mark scanner to drive the envelope generator with a waveform identical to that which would be generated by detection of a matrix scanner 0. Thus the envelope generator produces index marks during the last half of the time code frame.

4-140. Reference Marker and Position Identifier Scanner. The time code format contains a position identifier pulse 8 milliseconds wide during index count nine, and every ten index counts thereafter. This pulse identifies the end of a time frame. A position identifier pulse is contained in the time-code frame during the last 8 milliseconds of each tenth second. Thus the start of a time frame may be identified by the two adjacent 8-millisecond pulses. The

reference marker and position identifier scanner generates the necessary drive pulses for the envelope generator by combining ten-line code pulses and minor clock pulses.

4-141. Count/Hold Scanner. The count/hold scanner combines the hold signal from the count/hold control logic with minor clock pulses to generate drive pulses for the envelope generator. The output of the count/hold scanner causes generation of the count pulse. The count pulse is a 1 pulse (5 milliseconds wide), located at index mark eight of the last tenth second of the time code frame. If the major counter is holding, output from the count/hold scanner logic will cause the envelope generator to produce a 0 pulse at this time in the frame.

4-142. Sign Pulse Generation. During the third tenth second of the time code frame, the units hours and sign scanner is active. In addition to scanning the major counter BCD count, this scanner treats the countup/countdown control signal as it would a major counter register. During the fifth index mark of the third tenth second of the time code frame, a 1 pulse is produced by the envelope generator if the major counter is counting up.

4-143. Sine Wave Shaper. The sine wave shaper circuit shapes a 1000-pps square wave into a sine wave for modulation by the dc-shift time code envelope.

4-144. The shaper circuit consists of three twin-T filters, two low-pass filters, a high-pass filter, and output emitter-follower.

4-145. The twin-T filters attenuate the third, fifth, and seventh harmonics of the fundamental frequency of the square wave input. The second of these low-pass filters includes a phase-correcting potentiometer. This potentiometer is used to adjust the phase of the shaper-output sine-wave so that the leading edge of the modulator-signal occurs simultaneously with the sine-wave zero-axis crossing.

4-146. The high-pass filter is included in the circuit to further attenuate harmonics of the input signal.

4-147. Modulator. The 1-kc sine wave from the shaper circuit and the square wave time code envelope from the envelope generator are used by the modulator to produce the pulse width modulated time code carrier.

4-148. The modulator circuit consists of a carrier amplifier and a clamping circuit. The clamping circuit receives the time code envelope and uses it to attenuate the carrier during the zero (space) periods of the time code format. A potentiometer in the clamp circuit allows adjustment of the mark-space ratio. Another potentiometer in the amplifier portion of the modulator allows adjustment of the signal output.

4-149. LOCAL (NIXIE) DISPLAY. The content of the major counter and the count/hold status are displayed on the control panel of the countdown generator. The display devices used

for this purpose are nixie tubes which display the characters 0 through 9 and the special +, -, and H characters to indicate count, sign, and count/hold status.

4-150. The BCD count contained in the major counter, the condition of the sign control logic output, and the condition of the count/hold logic output are converted to ten-line code signals for controlling the nixie drivers. The conversion is accomplished by AND and OR gate matrices in the major counter BCD-to-decimal converter.

4-151. The nixie driver consists of switching transistors for each of the nixie tube elements. Decoded BCD output signals from the BCD-to-decimal converter cause these switching transistors to complete the high-voltage circuit for the selected nixie element.

4-152. REMOTE DISPLAY CONVERTER. Countdown time is displayed at remote locations by indicators which require a seven-line code. The remote display converter uses AND and OR matrices to convert the major counter BCD count to this seven-line code. The remote countdown display uses filament bulb character display devices rather than nixie tubes. Each character displayed is produced as the result of a specific combination of seven-line signals. The characters are displayed by lighting lamps behind character segment slots in a mask. The two masks required to display the numbers 0 through 9 and the special +, -, and H characters are covered in the paragraph describing Remote Time Display Units.

4-153. TAPE SEARCH/TIME CODE TRANSLATOR/COMPUTER I/O SYNCHRONIZER.

4-154. The Tape Search and Time Code Translator (TSTCT) Unit performs three primary functions:

- a. Translation of serial range-time code format into parallel binary-coded decimal digits. The BCD outputs represent the time of the year and the time of the day. An inline display presents the time being translated.

- b. Generation of signals that automatically control a magnetic tape transport for high-speed search in both the forward and reverse directions. The start and stop times are selected using switches on the control panel.

- c. Provides time data for operation-interval timing for the ACE-S/C System Command and Display Computers.

4-155. TAPE SEARCH/TIME CODE TRANSLATOR/COMPUTER I/O SYNCHRONIZER
FUNCTIONS.

4-156. Figure 4-16 is a simplified block diagram of the TSTCT. IRIG B time code modulated carrier signals may be applied to the input from one of two sources. During test operation, IRIG B time code from the Time Code Generator is patched to the input; during tape search operations time signals from the tape transport are patched to the input. The input

and decoding circuits strip the time code envelope from the time code carrier and the resultant binary coded data is stored in the output register. The time code translator output register is the common source for time data used for time displays, computer elapsed-time reference, and tape search functions.

4-157. Time data contained in the output register is translated into display control signals by the display converter circuits. The resultant seven-line code control signals are routed to the various console time display devices of the ACE-S/C system.

4-158. The Command and Display Computers of the ACE-S/C system make use of the time data in performing certain test operations. For example, an operator's command entry might call up a subroutine, which calls for computer generation of two distinct command messages separated by a discrete time interval. To accomplish this task the computer must make a note of the time of the first command message, generate the message, and return to other operations until the proper amount of time has elapsed. At the end of the allotted time period, the computer must issue the remaining command. The computer makes use of a clock service routine to perform such an operation and the sequence of data transfer is as follows: Upon callup of an operation such as described previously, the computer asks the TSTCT for the present time. This time data is then transferred to the computer and the time allotted between operations is added to this present time. The result is the time at which the second operation is to be performed. This time is then transferred to the TSTCT synchronization circuits for storage and comparison with the current time data. When sufficient time passes, so that the current time in the output register of the TSTCT is equal to the time stored in the sync circuits, the computer is notified that it is time for the second operation. This notification is accomplished by the TSTCT sync circuits which generate a computer interrupt signal. A significant point concerning the time data handling operation is the fact that the computer treats the time data as a command. Time data messages transferred to the computer as the result of an interrupt are converted to computer instructions, through use of a clock table stored as a part of the computer program. Thus the computer can have a number of time-sequence operations in progress at the same time, yet know exactly which command is to be generated as a result of each interrupt from the synchronizer.

4-159. To index the magnetic tape on which incoming raw data is recorded, the IRIG B time code is recorded on the tape along with the test data. To locate a specific portion of recorded data, the tape search logic compares the time on the tape with the time the operator has selected to begin playback. To accomplish this function, switches on the control panel are used by the operator to enter the tape-times at which he wants the playback to start and stop. The time signals from time track on the tape recorder/reproducer are patched into the

TSTCT input and the tape search mode is selected by the operator. The TSTCT issues signals which cause the tape transport to move the tape so that the time track may be read, and sample data entered, for comparison with the search start time. If the time from the tape is greater than the search start time, the TSTCT issues control signals which cause the tape transport to reverse and run at high speed until the tape time is less than the tape search start time. At this point the TSTCT recognizes the fact that the tape time is less than search start time, and issues transport control signals which cause the tape to be played back at normal speed. The TSTCT has a recycle feature which allows the sequence described above to repeat continuously. This feature makes use of the tape search stop controls which the operator may use to enter the stopping point of the playback cycle. Thus the TSTCT may be used to search out data recorded during a specific time period and replay it continuously.

4-160. Figure 4-17 is a block diagram of the time code translation circuits. IRIG B time code carrier signals are patched to the input circuits from the Time Code Generator during test operations or from the tape transport being searched during search and playback operations. The incoming modulated carrier is applied to the input circuits for stripping of the carrier envelope and generation of clock pulses.

4-161. The demodulation or code stripping of modulated carrier time codes requires two distinct operations. The first is a determination of reference time and the second is the determination of modulation characteristics. The reference time is that portion of the carrier wave that represents a known value of time. This may be the zero-axis crossing, the peak of the carrier, or any point in between. The zero-axis crossing is used in practical applications for two reasons: (1) the use of a wide bank comparator circuit eliminates frequency response problems and (2) the zero-axis crossing is usually synchronized with the leading and trailing edges of the pulse modulation to prevent excessive transient response problems. Modulation characteristics are determined by detecting the presence of code pulses.

4-162. The carrier decoder converts the output of the mark detector and the zero axis detector to a d-c level shift representing the envelope of the carrier. This d-c level shift is delayed by two cycles of the carrier. For example, if the carrier frequency is 1000 cps, the envelope is delayed by two cycles or two milliseconds. The carrier decoder also generates a reset term, pulse rate reset (PRR). The frequency of this term is equal to the time code pulse rate. In addition, the carrier decoder samples the envelope at specified times to determine whether it represents a binary one, zero, or a reference marker.

4-163. Following this determination, a count is made to determine the start of frame, at which time a frame rate reset (FRR) signal is generated. This signal synchronizes the unit.

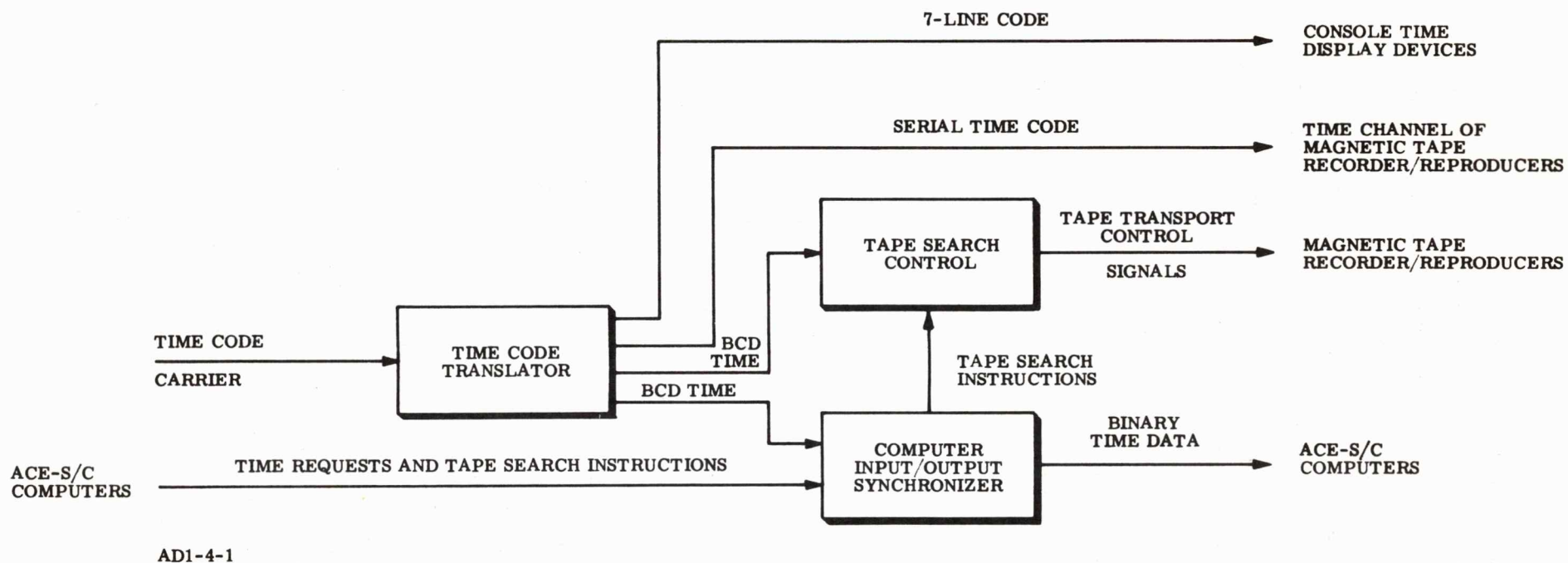
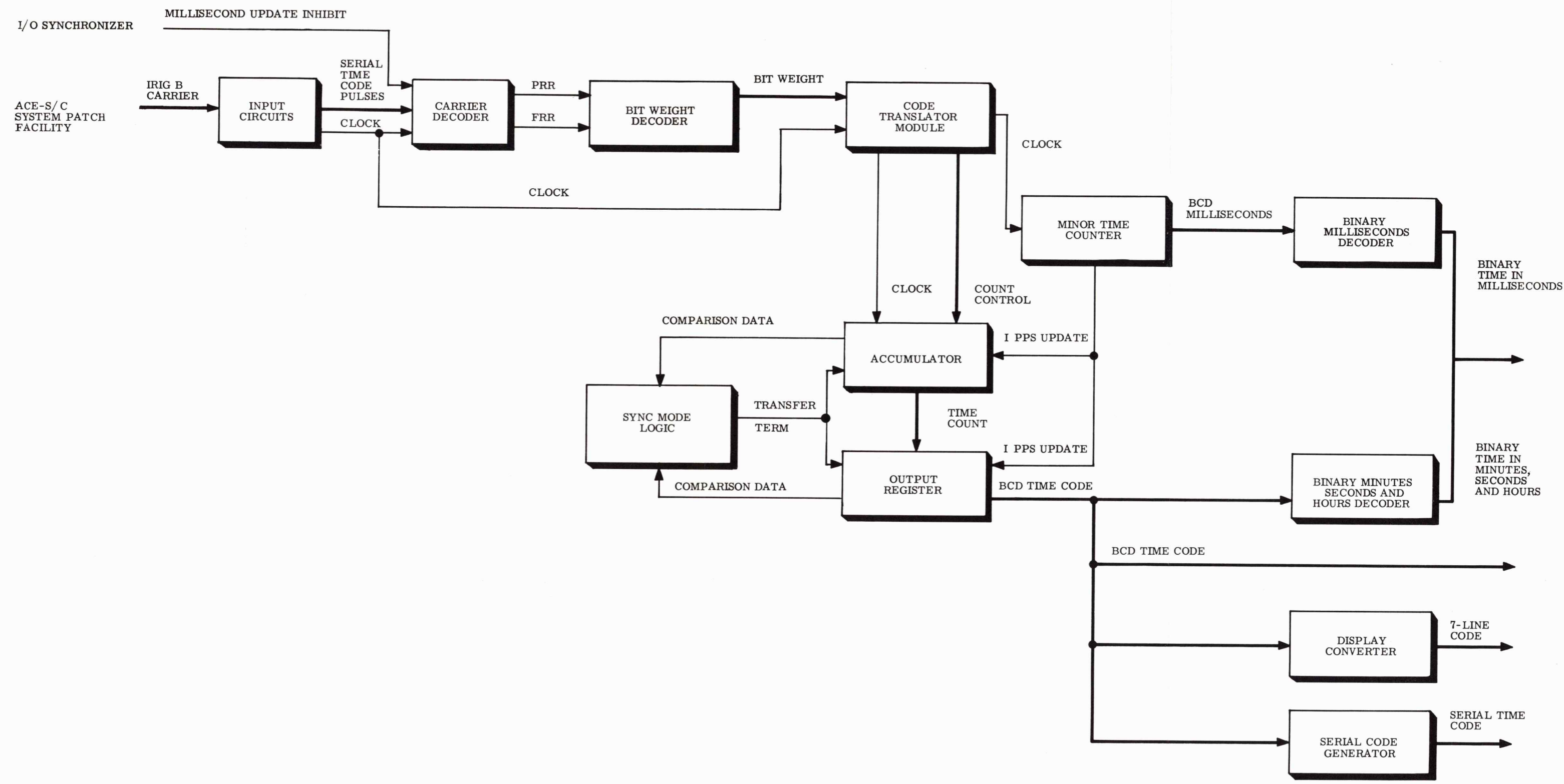


Figure 4-16. Tape Search and Time Code Translator Simplified Block Diagram



AD1-5-1

Figure 4-17. Time Code Translator Functional Block Diagram

4-164. The gating necessary to decode the bit weight after the FRR is generated is contained in the code translator module. FRR resets the accumulator, the minor time counter, and the bit weight decoder. After the start of the frame, the bit weight decode logic counts the number of incoming code pulses and this number becomes the address number.

4-165. The address number is used to determine the actual value or weight that the individual pulse carries. This weight is sent to the accumulator, where the decoding operation takes place. The accumulator stores the output in terms of seconds, minutes, hours, and days and transfers the number to the output register at the appropriate time. The number in the output register is fed to the parallel output connector, tape search logic, and the display conversion logic.

4-166. The tape search system functions that are affected by noise or dropouts are carrier decoding and zero-axis detection. These functions have a high inherent degree of noise immunity. For example, carrier decoding is entirely insensitive to one-cycle dropouts and random noise pulses. The zero-axis detector makes use of the controlled hysteresis of a Schmitt trigger to provide noise immunity. High amplitude noise may obscure the amplitude modulation on the carrier, causing carrier decoding errors to appear in the accumulator. However, the effect of this type of noise on the carrier is negligible. The zero-axis detector will continue to generate the reliable clock needed to update the output register.

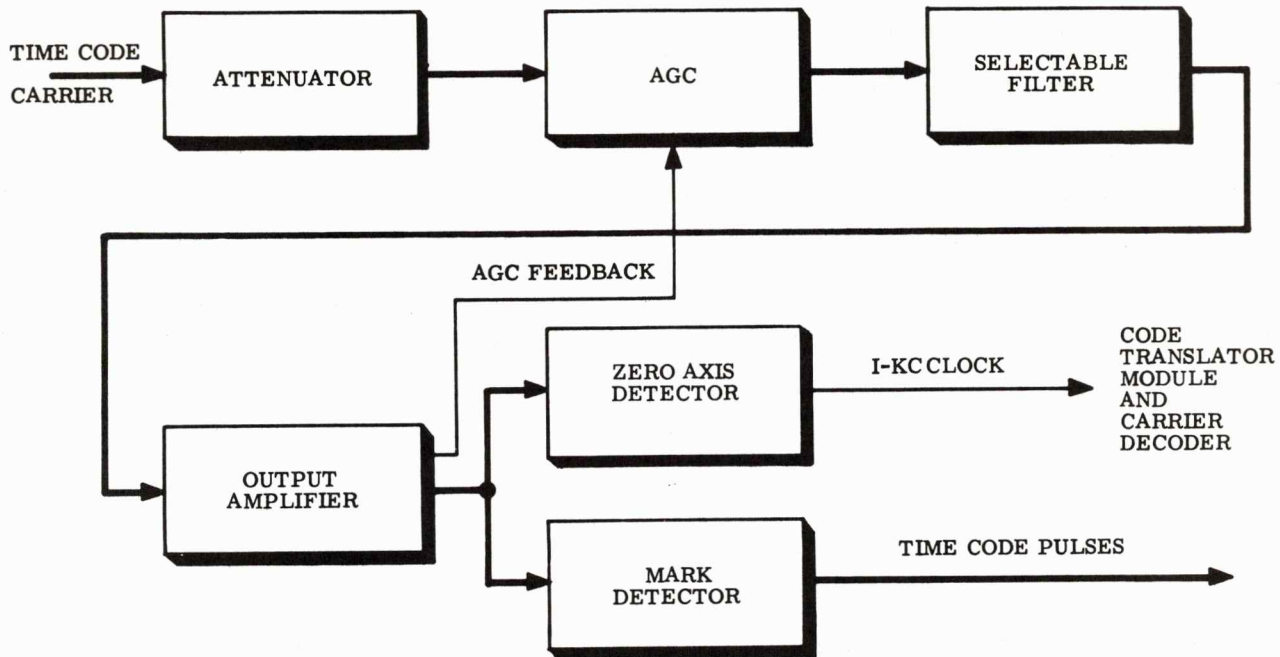
4-167. A noise suppression switch is provided to eliminate errors due to noise. However, if noise errors are still introduced into the accumulator, the synchronization mode logic allows the translator to ignore the erroneous data. Thus, the TSTCT is immune to noise errors that may be generated in an individual frame.

4-168. Complete loss of carrier will obviously result in a continuous incorrect count in the output register. If this occurs, the erroneous data in the output register will be corrected by the sync mode logic.

4-169. TAPE SEARCH/TIME CODE TRANSLATOR/COMPUTER I/O SYNCHRONIZER DESCRIPTION.

4-170. INPUT CIRCUITS. Figure 4-18 is a block diagram of the input circuits. The circuits consist of an attenuator, an AGC amplifier, a selectable filter, an output amplifier, the zero-axis detector, and the mark trigger. The attenuator (10 to 1 or 20 db) provides input signal ranges from 100 millivolts to 20 volts rms. The precision AGC amplifier operates over a 40 db range of input signal with less than 1 db variation in output. The amplifier bandwidth accepts carriers from 100 cps to 100,000 cps in frequency. A maximum resolution capability of ± 5 microseconds at 1 kc is provided in the zero-axis detector. This resolution

corresponds to a hysteresis range of 3 percent of the average carrier at 1 kc. The hysteresis is held constant from 100 cycles to approximately 2 kc. Above 2 kc, the resolution is held constant at 5 microseconds up to approximately 30 kc. Beyond 30 kc, the hysteresis increases proportionately as the carrier frequency increases up to 10 percent or 1.5 microseconds resolution, whichever is less.



AD1-6-1

Figure 4-18. Input Circuits Functional Block Diagram

4-171. The zero-axis detector is a phase detection device that gives an output each time the input signal crosses the zero axis. This output is a clock pulse that is termed $\overline{Z}A$ when it is coincident with the positive-going crossing. When the clock pulse is coincident with the negative-going crossing, it is designated ZA . These pulses are used in the synchronization of the decode logic and are counted in the minor time counter.

4-172. The mark detector determines instantaneous signal amplitude. The operating range of this trigger circuit is set for a signal level 20 percent greater than the average carrier amplitude. This trigger level allows detection of codes with an average duty cycle varying from 10 to 50 percent and a modulation ratio varying from 2:1 to 4:1.

4-173. The mark detector produces a pulse on either the negative-going or positive-going excursion, depending on the position of the INPUT switch. This switch allows the TSTCT to

accept modulated carriers that have the start of the code pulse on either the positive- or negative-going zero-axis crossing. No timing errors are introduced.

4-174. CARRIER DECODER. The carrier decoder converts the outputs of the zero-axis detector and the mark detector into a d-c level shift representing the envelope of the carrier. It also generates a pulse rate reset term (PRR) with a frequency equal to the pulse rate of the time code. In addition, the carrier decoder samples the envelope at specified times to determine whether it represents a binary one, binary zero, or a reference marker.

4-175. BIT-WEIGHT DECODER. The bit-weight decoder consists of three clock pulsers, the pulse-width generator, two DCU's, and a flip-flop.

4-176. The two DCU's are connected in cascade to form a pulse counter. This counter is clocked by the pulse-width generator and is reset to zero by the frame rate reset (FRR). The outputs of the counter are decimally decoded, making available terms that identify the decimal units of the time frame (i.e., units of seconds, tens of seconds, units of minutes, tens of minutes, etc.). These terms are used by the code translator module to control the loading of the accumulator.

4-177. MINOR TIME COUNTER. The minor time counter can accept carrier frequencies of 1 kc or 100 pps directly. If it is desired to accept a 10-kc carrier, an additional DCU is added in the code translator module. The minor time counter consists of three DCU's (the milliseconds counter, the hundredths-of-seconds counter, and the tenths-of-seconds counter) that can be arranged to count the number of cycles of the desired carrier for decoding the IRIG B time code. These DCU's are decoded by four-to-ten-line converters. These converters provide terms used for the loading and output matrices.

4-178. The PRR sets the first DCU to a count of two to achieve synchronization with the delayed envelope. The FRR resets the minor counter at the appropriate time as determined by the code format.

4-179. ACCUMULATOR. The accumulator consists of ten counters (the units-of-seconds counter through the hundreds-of-days counter) that accumulate the total decimal value of the binary ones of the time code in a given time frame. The code translator module supplies gating inputs to the counters. These inputs allow the appropriate counters to count a number of clock pulses equal to the decimal value of the binary one pulses.

4-180. The code translator module contains AND gates that recognize and evaluate the binary ones on the code. The gates are enabled by a binary one on the code. The AND gates also contain a pulse position term or address and a pulse-width term. The pulse-width term allows the appropriate counter to count the number of clocks equal to the value of the particular

pulse being scanned. The outputs of each AND gate are ORed together in the OR gate that corresponds to the counter to be enabled.

4-181. When the radix of a counter is reached, a carry pulse is fed to the following counter. The use of out-of-phase clocks allows counting of binary ones and carry pulses during the same pulse-width term interval.

4-182. The tens-of-seconds counter and the tens-of-minutes counter each have a carry flip-flop. These flip-flops are included to avoid simultaneous carries.

4-183. At a selected time after the accumulation is complete, the contents of the accumulator are transferred in parallel into the output register. The output register now contains the decoded time value of the time frame under consideration. The accumulator is reset to zero by the next FRR and the decoding process is repeated for the next frame.

4-184. OUTPUT REGISTER. The output register is a decade counter that is permuted to count seconds through 59, minutes through 59, hours through 23, and days through 399. The output register is updated by 1-pps output of the minor time counter. The output register, in conjunction with the minor time counter, operates essentially in a Time Code Generator Mode.

4-185. The contents of the accumulator are loaded into the output register just prior to frame-rate reset time.

4-186. Each output register flip-flop has an associated parallel loading amplifier. The input to each of these amplifiers consists of the transfer term and a logical input. The transfer term is developed by a reset driver and brought in on a line common to all the amplifiers. The logical term is obtained from the false side of the corresponding flip-flop in the accumulator.

4-187. At transfer time, each flip-flop is set or reset according to the bit weight of the input logic. If the input is a zero, the flip-flop is set. If the input is a one the flip-flop is reset.

4-188. SYNCHRONIZATION MODE LOGIC. The synchronization mode logic compares the data in the accumulator with the data in the output register. If there is a disagreement, this logic generates a transfer term which allows the data in the output register to be corrected. The synchronization mode logic provides an additional degree of noise immunity for the TSTCT.

4-189. The basic assumption is that the data in the output register is correct. This data is compared to the data in the accumulator for one, two, or three time frames, depending upon the setting of the SYNC MODE selector switch. If a disagreement exists for the selected number of consecutive time frames, it is then assumed that the data in the accumulator is correct. The transfer command will be generated on the next time frame. This allows the contents of the accumulator to be transferred into the output register.

4-190. DISPLAY CONVERTER FUNCTION. The display converter converts the BCD output from the output register to the seven-line code necessary for driving the console time displays. Figure 4-11 shows the decimal number versus BCD and seven-line code.

4-191. BINARY MINUTES, SECONDS, AND HOURS DECODER. The BCD time output from the output register must be converted to straight binary format for use by the input/output synchronizer. This conversion is the function of the binary minutes, seconds, and hours decoder. The conversion results in six bits of seconds information, six bits of minutes information, and five bits of hours information. The conversion is accomplished by diode matrix gates, except in the case of units of seconds, minutes, and hours terms which are taken directly from the output register.

4-192. TAPE SEARCH CONTROL. In addition to the translation operations, the TSTCT provides output signals (figure 4-19) that automatically control a magnetic tape transport. The transport, under control of the tape search system, searches for the desired data at high speed in both the forward and reverse directions. The start and stop times are selected using the START TIME and STOP TIME switches on the control panel.

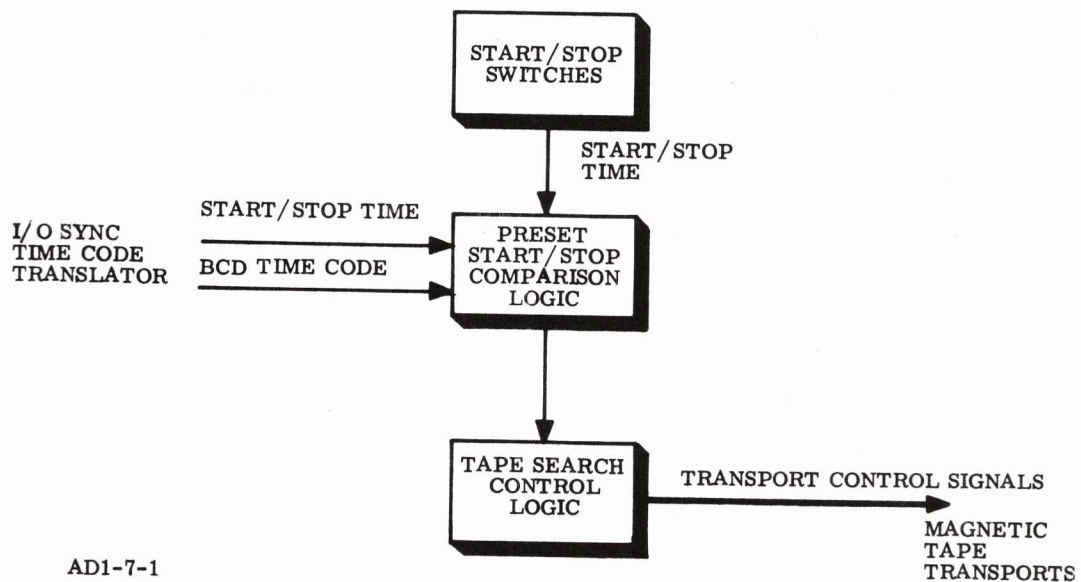


Figure 4-19. Tape Search Control Functional Block Diagram

4-193. There are four possible modes of operation: Recycle, Single-Cycle, Search/Start, and Playback. If the Playback Mode is selected by the operator, he then activates the PLAY-BACK switch to start the tape transport. In all other modes, the START SEARCH switch is used to start the transport.

4-194. In the Single-Cycle and Recycle Modes, the transport searches at high speed for the preselected start time. When the start time is found, the transport is slowed to playback speed, and the desired portion of the tape is played back. In the Single-Cycle Mode, the transport stops upon reaching the stop time. In the Recycle Mode, the transport returns to the preset start time and replays the tape. This cycle will be repeated as long as the TSTCT is in the Recycle Mode or until the STOP switch is pressed. In the Search-to-Start Mode, the transport searches for a time that is three time frames earlier than the preset start time. When this time is found, the transport stops. In the Playback Mode the search logic is bypassed and the system functions as a translator in the forward direction. The tape search system also provides controls for manually controlling a tape transport.

4-195. In discussing the tape search function, the actual time on the tape is represented by A (see figure 4-20). The time set on the START TIME and STOP TIME switches is represented by S1 and S2, respectively.

4-196. The operator sets the desired start and stop times on the control panel switches and then presses the START SEARCH switch. The tape search control logic places the tape transport in the Fast Forward Mode. A delay allows the tape transport to reach search speed before the comparison count is started. When a comparison shows A to be greater than S1 ($A > S1$), a counter is energized. Three consecutive time frames of $A > S1$ comparisons must be obtained before the search control logic will signal the transport control logic to reverse the transport.

4-197. When the three time frames of $A > S1$ comparisons have been received, the tape transport is stopped and put into fast reverse. After a delay to allow the transport to reach search speed, comparisons are made to determine when A is less than S1 ($A < S1$).

4-198. When three consecutive time frames of $A < S1$ comparisons are counted, the tape transport is stopped and put into the Forward Playback Mode. Playback speed is maintained and, when A is equal to S1, a start pulse and a d-c level voltage are applied to external equipment.

4-199. The transport continues at playback speed until the stop time, a stop pulse is generated, the d-c level voltage is removed, and the transport stops.

4-200. The preset start/stop comparison logic will also accept start/stop time from the input/output synchronizer circuits to control the search functions, thus giving the ACE-S/C command and display computers tape search capability.

4-201. COMPUTER INPUT/OUTPUT SYNCHRONIZER. Figure 4-21 is a block diagram of the input/output synchronizer. The synchronizer is the communications link between the time code translator circuits and the command and display computers. Throughout the discussion, the computers are referred to as computer A and computer B.

4-202. The input/output synchronizer alternately examines the output data lines from each of the digital computers. This monitoring interval is set at 10 microseconds. Therefore, for a 10-microsecond interval, the tape search system monitors the output data lines from computer A. If no external function is addressed to the TSTCT during this 10-microsecond interval, the input/output synchronizer then examines the output data lines of computer B for 10 microseconds. If no valid external function appears during this 10-microsecond period, the synchronizer returns to computer A, etc. When a tape search system external function code from one computer is detected (04XX_g), the tape search system temporarily ignores the other computer and responds to that external function. When the particular external function sequence has been executed, the synchronizer immediately examines the output lines of the other computer and the alternating, biphase, control-monitoring procedure is re-established. This technique guarantees that neither computer can monopolize the tape search system. The external function codes recognized by the TSTCT are discussed in the following paragraphs.

4-203. Input Range Time (0401_g). The "75" instruction that generates this external function is followed by a four-word input sequence. When this external function code is detected, the function decode logic loads the function register with the function code (01_g). (Refer to the Input/Output Synchronizer Block Diagram, figure 4-21.)

4-204. The tape search system then responds to the requesting computer with an Output Resume signal. The computer, in turn, responds by removing the Function Ready signal. The tape search system then removes the Output Resume signal. In connection with subsequent input instructions (INA), the computer issues an Input Request signal. Meanwhile, the input/output synchronizer has issued a temporary inhibit update signal. The inhibit update signal prevents the output register from updating for a period of 400 milliseconds.

4-205. The contents of the binary milliseconds accumulator are then placed on the output lines to the requesting computer. When the Input Request signal appears, the tape search system responds with an Input Ready signal. After the computer accepts the range time data, the Input Request Signal is removed. At this time, the Input Ready signal from the tape search system is terminated. The transfer of milliseconds is now complete. The tape

search system then proceeds, automatically, to another input cycle which commences when the computer issues a second Input Request signal.

4-206. Four input transfer cycles occur as a result of executing this external function: input milliseconds, input seconds, input minutes, and input hours. The range time word formats are shown in figure 4-22.

4-207. When the Input Ready signal corresponding to the transfer of hours is terminated, the exchange of data related to this external function is complete. The time code translator inhibit update is then released. If a time code translator update pulse occurs while output register is frozen (during the input range time operations), the update pulse is stored until the inhibit update is removed. When the range-time output register is properly updated, the input/output synchronizer immediately directs its attention to the alternate computer for the next 10-microsecond interval.

4-208. Load Milliseconds (0402_g). This computer output function permits preset interrupt range times to be transferred from the computer core to the appropriate interrupt time register within the tape search system. Upon detecting this external function code, the tape search system responds to the initiating computer with an Output Resume. The computer then withdraws the Function Ready signal and the tape search system responds by dropping the Output Resume.

4-209. The tape search system is then prepared to accept preset milliseconds information from the computer core. The computer next executes an output instruction that delivers the milliseconds word to the data lines. Data is accompanied from an Information Ready signal. The tape search system, upon recognizing the Information Ready signal, loads the milliseconds information into the computer program preset milliseconds register.

4-210. After a delay of a few microseconds, the tape search system returns an Output Resume signal to the computer. The computer responds by turning off the Information Ready signal. At this time, the tape search system drops the Output Resume signal. The one-word information exchange is then complete and the tape search system directs its attention to the other computer for 20 microseconds. It is not necessary to clear this register before it may be reloaded; however, this register may be cleared by loading with all zeros or by execution of Master Clear (0400_g).

4-211. Load Seconds (0404_g). This external function sequence is identical to the typical output sequence described for the Load Milliseconds external function. This register can be reset with the Master Clear signal (0400_g).

4-212. Load Minutes (0410_g). This external function permits an output instruction to load the tape search system computer-programmed preset interrupt time minutes register. This register can be reset by the Master Clear signal (0400_g).

4-213. Load Hours (0411_g). This external function permits an output instruction to load the tape search system computer-programmed, preset interrupt time hours register. This register may be reset by a Master Clear signal (0400_g).

4-214. Lockout Other Computer (0412_g). If originating computer has not been locked-out, execution of this external function will set a 1 in the appropriate status register position (2^{10} or 2^{11} , depending upon originating computer). If the originating computer is already locked-out, this signal is ignored.

4-215. Lockout this Computer (0413_g). This external function sets the lockout flip-flop that corresponds to the originating computer. This external function is used only during orientation operations.

4-216. Clear Computer A Lockout (0414_g). This external function resets status register position 2^{11} to the 0 state.

4-217. Clear Computer B Lockout (0416_g). This external function resets status register bit position 2^{10} to the 0 state.

4-218. Enable Interrupt 30 Computer A (0431_g). This external function sets status register position 2^7 to the 1 state. When the tape search system detects the preset start time (during playback), an Interrupt 30 is directed to computer A.

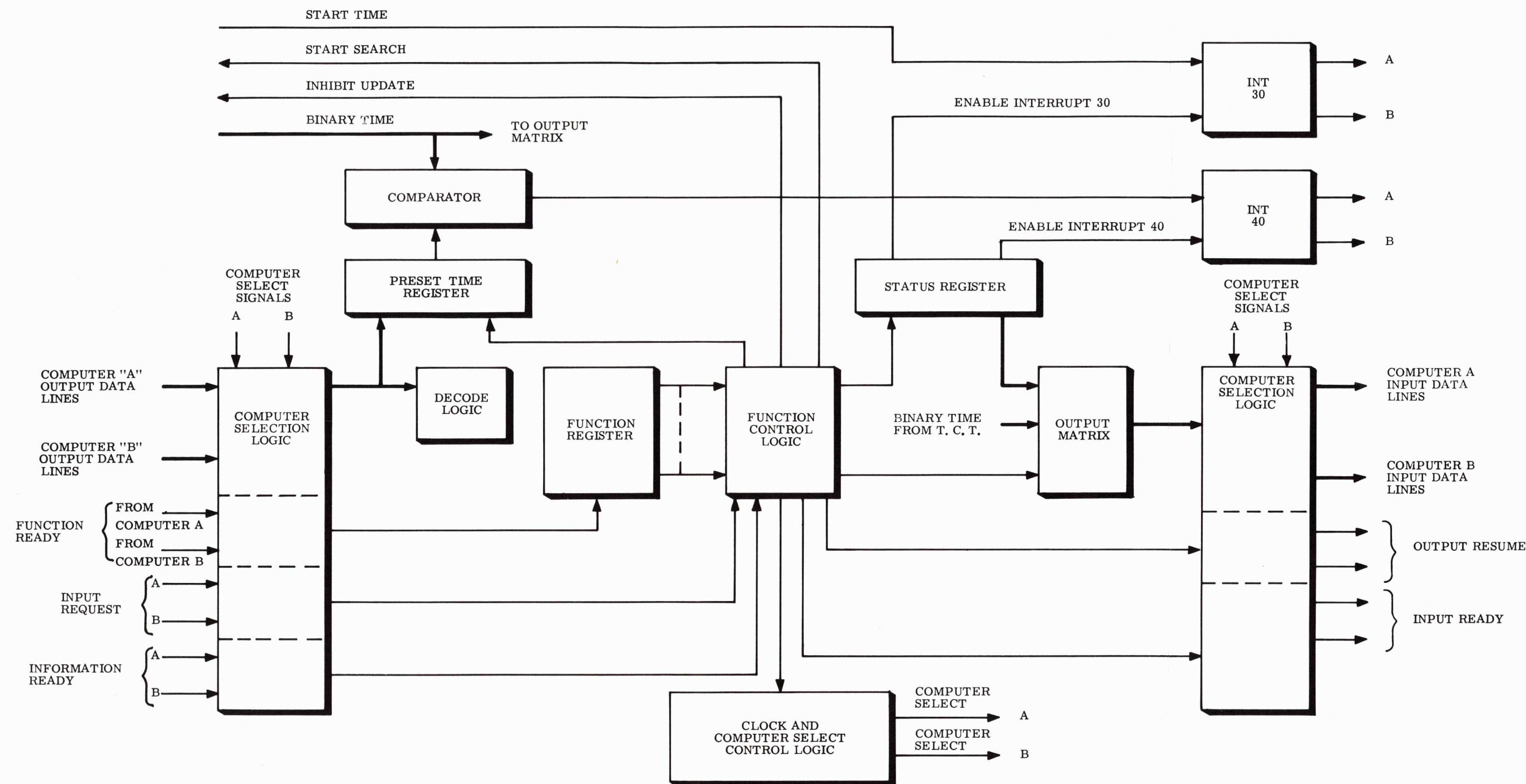
4-219. Enable Interrupt 30 Computer B (0432_g). This external function sets status register bit position 2^6 to the 1 state. When the tape search system detects the preset start time, an Interrupt 30 is transmitted to computer B.

4-220. Enable Interrupt 40 Computer A (0441_g). This external function sets status register position 2^5 to the 1 state. The tape search system then monitors the comparison between the computer program preset interrupt time registers and the range time binary accumulators. Upon sensing coincidence, the tape search system sets Interrupt 40 No. 1 flip-flop (status register bit position 2^1). This interrupt flip-flop, in turn, transmits an Interrupt 40 to digital computer A.

4-221. Enable Interrupt 40 Computer B (0442_g). This external function sets status register bit position 2^4 to the 1 state. Upon sensing coincidence between the computer program preset interrupt time registers and the range time binary accumulators, the tape search system sets the Interrupt 40 No. 2 flip-flop. This interrupt flip-flop then transmits an Interrupt 40 to digital computer B.

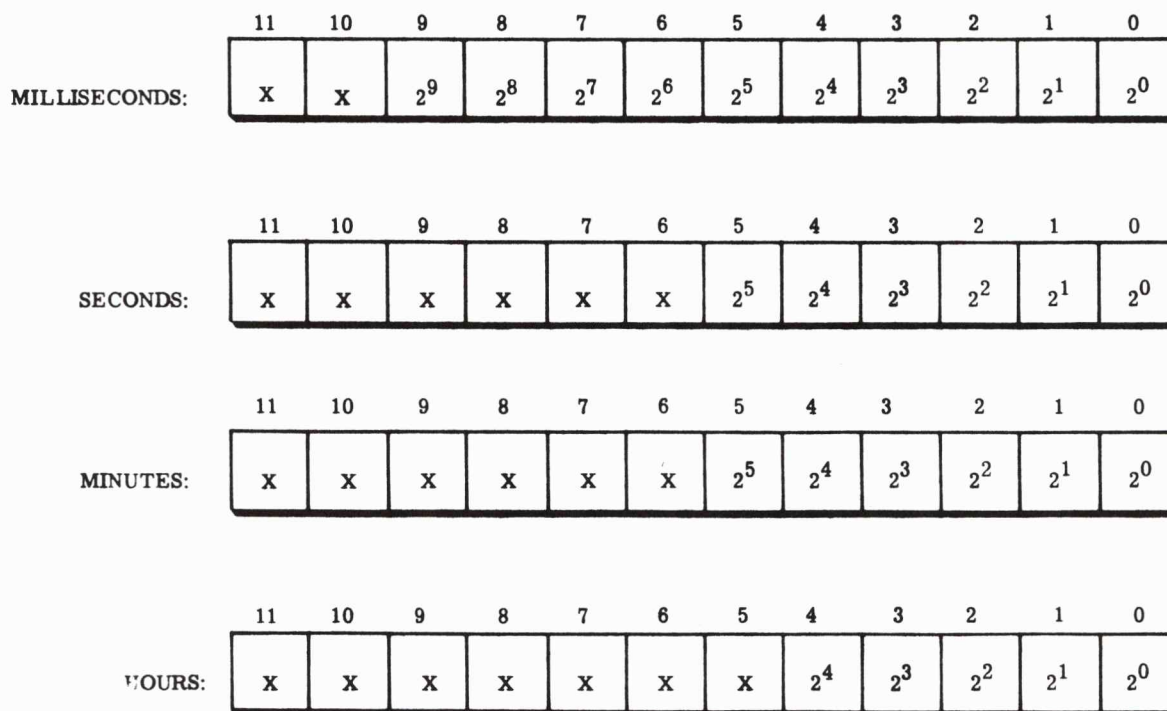
AD1-8-1

Figure 4-20. Tape Search Sequence



AD1-9-1

Figure 4-21. Input/Output Synchronizer Block Diagram



NOTE: DATA BITS SHOWN AS 'X' ARE ALWAYS LOGICAL '0'

AD1-10-1

Figure 4-22. Range Time Word Formats

4-222. Commence High-Speed Search (0450_g). Execution of this external function causes the tape search system to commence high-speed search for the tape segment selected on the START/STOP time switches. This external function is essentially in parallel with the START SEARCH switch located on the control panel.

4-223. Master Clear (0400_g). Execution of this external function resets all interrupt flip-flops, enable flip-flops, and lockout flip-flops. This instruction is useful only in special situations where it is guaranteed that its execution will not disturb programs in progress.

4-224. Clear Interrupt 30 (0473_g). This external function clears the Interrupt 30 flip-flop corresponding to the computer originating the 0473_g. In addition, this external function clears the enable Interrupt 30 flip-flop corresponding to the originating computer.

4-225. Clear Interrupt 40 (0474_g). Execution of this external function clears the Interrupt 40 flip-flop corresponding to the computer originating the 0474_g. In addition, this external function clears the enable Interrupt 40 flip-flop corresponding to the computer originating the 0474_g external function.

4-226. Status Reporting (0440_g). Upon inquiry from either computer, the tape search system responds with a 12-bit status response. The 12-bit status register is an assembly of control flip-flops within the tape search system. The assignment of the various status register bit positions and their significance are described in the following paragraphs.

4-227. Lockout Computer No. 1 (2¹¹). A 1 appearing in the status register bit position indicates that computer B has previously executed external function 0412_g Lockout Other Computer. This bit position is an advisory message only and is provided as a means for computer B to transmit the lockout message to computer A. There is no hardware to restrict the activity of the lock out computer. That is, in an emergency situation a locked out computer could clear the lockout and proceed.

4-228. Lockout Computer No. 2 (2¹⁰). The presence of a 1 in this bit position indicates that computer A has executed external function 0412_g Lockout Other Computer. The significance of this status bit is similar to the significance of bit position 2¹¹.

4-229. Last Load (2⁹). This bit position maintains a continuous presentation indicating the computer which most recently executed a load external function. A 1 in this position indicates that the most recent load instruction (0402_g, 0404_g, 0410_g, or 0411_g) originated from computer A. A 0 in this position indicates that the most recent load instruction originated from computer B.

- 4-230. Tape Search in Progress (2^8). A 1 appearing in this bit position indicates that a high-speed tape search is in progress and the contents of the range time registers may not be meaningful.
- 4-231. Enable 30 - No. 1 (2^7). The presence of a 1 in this position indicates that manual preset Interrupt 30 has been enabled for computer A.
- 4-232. Enable 30 - No. 2 (2^6). The presence of a 1 in this position indicates that manual preset Interrupt 30 has been enabled for computer B.
- 4-233. Enable 40 - No. 1 (2^5). The presence of a 1 in this position indicates that stored program preset Interrupt 40 has been enabled for computer A.
- 4-234. Enable 40 - No. 2 (2^4). The presence of a 1 in this position indicates that stored program preset Interrupt 40 has been enabled for computer B.
- 4-235. Interrupt 30 - No. 1 (2^3). A 1 appearing in this position indicates that the manual preset interrupt for computer A has triggered and an Interrupt 30 has been transmitted to computer A.
- 4-236. Interrupt 30 - No. 2 (2^2). A 1 appearing in this position indicates that the manual preset interrupt has triggered and an Interrupt 30 signal has been transmitted to computer B.
- 4-237. Interrupt 40 - No. 1 (2^1). A 1 appearing in this bit position indicates that the stored program preset interrupt has triggered and an Interrupt 40 has been transmitted to computer A.
- 4-238. Interrupt 40 - No. 2 (2^0). A 1 appearing in this position indicates that the stored program preset interrupt has triggered and an Interrupt 40 has been transmitted to computer B.
- 4-239. DATA INPUT LOGIC. The data input logic comprises cable terminators that transpose the current mode computer outputs to voltage mode system logic levels, computer A, computer B or test select gates, the function register, and the unit designator decode logic.
- 4-240. The computer data output lines are presented to the inputs of cable terminators. The outputs of the cable terminators are true (-6 v) for an input more positive than -1.5 v. The outputs of the cable terminators are routed to the computer select gates. The selection of the gates is dependent upon which computer is being scanned or, if in the Test Mode, the outputs of the test switches. The outputs of the computer select gates are buffered by noninverting amplifiers.
- 4-241. INPUT/OUTPUT FUNCTION CONTROL LOGIC. The input/output control logic accepts the Function Ready, Information Ready, and Input Request signals from the computer and transmits the Output Resume and Input Ready signals to the computer. The input control lines are routed through cable terminators to the inputs of the computer/test select gates.

4-242. Function Ready. Whenever a Function Ready signal is received, an Output Resume signal is transmitted to the computer. Approximately 2 microseconds after the computer receives the Output Resume signal, it drops the Function Ready signal. When the Function Ready line goes false, the Output Resume signal is removed.

4-243. The computer select flip-flop is reset on the next 100-kc clock if the function designator indicates that further action is not required by the same computer (Status Request, Input Range Time, or Load Time). If any of these functions are recognized, the computer select flip-flop remains true until the appropriate action is taken and is then reset. Therefore the computer which generated the Function Ready stays selected until the function has been completed.

4-244. Input Request. An Input Request command from the computer is always preceded by a Function Ready command. The Function Ready command sets up the required function designator (either Status Request or Input Range Time) so that an Input Request is recognized only if the Function Ready command has been received.

4-245. When the Input Request is recognized, an Input Ready command is transmitted to the computer. When the computer removes the Input Request signal, the Input Ready command is removed.

4-246. Data is gated to the computer so that data is on the line for 10 microseconds before the Input Ready command is transmitted. This allows time for the lines to settle. When range time has been requested as an input, four sequential Input Requests are required to input the four time data words to the computer.

4-247. Information Ready. An Information Ready command from the computer is always preceded by a Function Ready command. This command sets up the required Function Designator (load milliseconds, load seconds, load minutes, or load hours) so that an Information Ready is recognized only if Function Ready has been received. When an Information Ready command is recognized, an Output Resume command is transmitted to the computer.

4-248. The computer removes the Information Ready signal upon receiving Output Resume. The removal of Information Ready causes the Output Resume command to go false and gate the input data to the preset time register addressed by the preceding Function Ready command. When the Output Resume command goes false, the computer select flip-flop changes state and scans the other computer input lines.

4-249. CLOCK AND SYSTEM CONTROL LOGIC. The clock logic consists of a precision crystal-controlled 400-kc oscillator and three flip-flops. The flip-flops are arranged to form a divide-by-eight counter. The output of the divide-by-four stage is the input to the 100-kc clock. The output of the divide-by-eight state is connected to the input of the 50-kc clock.

4-250. Computer Select Flip-Flop. The computer select flip-flop scans the input lines of computers A and B. When the flip-flop is true, the inputs from computer A are enabled; when it is false the inputs from computer B are enabled. The computer select flip-flop toggles on every 50-kc clock pulse unless a Function Ready has been recognized from the computer being scanned at that time. The computer select flip-flop is then inhibited from changing state or from scanning the other computer until the instructions given by the scanned computer have been complied with.

4-251. Master Clear Flip-Flop. The master clear flip-flop is set upon recognition of the Master Clear Function designator (00_g). This flip-flop is reset 10 microseconds later by the next 100-kc clock pulse. When the master clear flip-flop goes true, the status register, preset time register, interrupt flip-flops, and the inhibit update flip-flop are all reset. The master clear flip-flop can be set in the Test Mode by pressing the RESET switch on the test panel.

4-252. Start Search Flip-Flop. The start search flip-flop is set when the start search function designator (50_g) is recognized. This flip-flop is reset 10 microseconds later by the next 100-kc clock pulse. When FU02 is true, a start search command is transmitted to the tape search control circuits, specifically the preset start/stop comparison logic.

4-253. Inhibit Update Flip-Flop. The inhibit update flip-flop is set upon recognition of the input range time function designator (01_g). The flip-flop is reset after the fourth range time word has been transmitted to the computer. When FU03 is true, the time code translator carrier decoder is prevented from updating the output register while time is being transmitted to the computer.

4-254. Data Word Counter. The data word counter counts the number of data words transmitted to the computer during an input range time operation. The counter is reset to zero when a Function Ready command is received. Every Input Ready signal transmitted to the computer is then counted. The data word counter is reset by the fourth Input Ready command.

4-255. STATUS REGISTER AND OUTPUT DATA MATRIX. The status register is a 12-bit register that stores the computer and system status. The bit content and resultant effect on synchronizer functions were covered in the paragraph entitled Status Reporting.

4-256. The output data matrix gates the five data words that are to be transmitted to the computers. The gating is accomplished by allowing the enabling term for a group of 1-way gates to go to -18 volts to enable the gates and to 0 volts to inhibit that particular group of gates.

4-257. The outputs of the status register are activated when a Status Request has been received. The status decode term is true for the Status Request function designator (40_g).

4-258. The milliseconds outputs of the range time register are enabled when an input range time has been requested and the data word counter is at zero. The input range time decode term is true for the input range time function designator (01_g).

4-259. The seconds outputs of the range time register are enabled when the data word counter is at a count of one. The minutes output of the range time register are enabled when the data word counter is at a count of two. The hours outputs of the range time register are enabled when the data word counter has reached a count of three. The enabled gates are then buffered by 12 noninverting amplifiers.

4-260. DATA OUTPUT LOGIC. The data output logic consists of 24 gated output drivers (12 for computer A and 12 for computer B) and four interrupt flip-flops and drivers.

4-261. The gated data terms which are generated in the output data matrix are the inputs to the gated output drivers. Each set of outputs drivers is then gated by respective computer gate terms from the computer select flip-flop.

4-262. Four interrupt flip-flops are used to generate either Interrupt 30 or Interrupt 40 signals to each computer. Each flip-flop is set when a corresponding flip-flop is set in the status register. Each interrupt flip-flop is reset when its respective computer responds with a Status Request command.

4-263. PRESET TIME STORAGE REGISTER COMPARISON LOGIC. The preset time storage register stores the preset time loaded from either computer for comparison with the range time from the time code translator output register. Information is loaded into the register upon receipt of an Information Ready command which has been preceded by the appropriate function designator. The Function Designator addresses the particular part of the register to be loaded. The function designators are as follows:

- a. Load milliseconds (02_g).
- b. Load seconds (04_g).
- c. Load minutes (10_g).
- d. Load hours (11_g).

4-264. The register may be reset either by loading all zeros or by a Master Clear function code from either computer.

4-265. The time stored in the preset time register is compared with system range time and when equality is recognized, an Interrupt 40 command is sent to either computer if the interrupt has been enabled.

4-266. TEST MODE LOGIC. The test mode logic consists of flip-flops and associated drivers, and switches located on the test panel. The following switches are located on the test panel:

- a. Six Function Designator (2^0 through 2^5) toggle switches.
- b. COMP/TEST toggle switch.
- c. Computer A/B toggle switch.
- d. Function Ready pushbutton switch.
- e. Inform Ready pushbutton switch.
- f. Input Request pushbutton switch.
- g. RESET switch.

4-267. When the system is under computer control, the COMP/TEST switch must be in the COMP position. When in this mode, all other test panel switches are disabled.

4-268. When the COMP/TEST switch is in the TEST position, the test panel switches are enabled and the computer interface circuits are disabled. In the Test Mode, the test panel pushbutton switches are used to simulate their respective computer commands.

4-269. COUNTDOWN TIME CODE TRANSLATOR AND COMPUTER INPUT/OUTPUT SYNCHRONIZER.

4-270. COUNTDOWN TIME CODE TRANSLATOR AND COMPUTER INPUT/OUTPUT SYNCHRONIZER FUNCTIONS.

4-271. The command and display computers make use of the countdown time just as they do the real (or IRIG B) time. Like the real time, the countdown time is generated in serial pulse-width-modulated form. The format of the countdown time code differs from the real time format and is covered in the discussion of the Countdown Time Code Generator. The translation of the countdown time code is done much in the same manner that is used for real time. The circuits contained in the countdown time code translator are generally the same as those in the real time translator.

4-272. COUNTDOWN TIME CODE TRANSLATOR AND COMPUTER INPUT/OUTPUT SYNCHRONIZER DESCRIPTION.

4-273. TIME CODE TRANSLATOR. There are some differences between the real and countdown translators due to the difference in the formats of the time codes they process. Countdown time can be counted up or down and can be stopped. There are special pulses in the code format to indicate the sign and the hold status. The countdown translator logic differs from the real time translator logic in that it can detect these extra pieces of information and change its internal operation accordingly. For example, the format of the countdown

time code changes when the time count direction changes. When the time is being counted down toward zero, the incoming code must be read most-significant-bit first. When time zero is reached, the time sign changes and the count direction starts up, the code must be read least-significant-bit first. The countdown translator contains a display converter which performs the same function as the display converter in the real time translator, in that it provides the seven-line code signals to drive the time displays.

4-274. INPUT/OUTPUT SYNCHRONIZER. The countdown synchronizer circuits are almost identical to those in the real-time I/O synchronizer. The prime differences are that the countdown synchronizer control panel has digital thumbwheel-switches which allow the manual entry of computer interrupt time for test purposes.

4-275. The other prime differences between the real-time synchronizer and the countdown synchronizer are in the information interchange between the computer and the synchronizer. These differences are in the function codes used by the computer when communicating with the countdown synchronizer and in the time data formats. The countdown synchronizer function codes and time data formats are discussed in the following paragraphs.

4-276. Input Countdown Time (4601_g). The 75 instruction that generates this external function is followed by a two-word input sequence. Upon detecting the presence of this external function, the function decode logic loads the function code (01_g) into the synchronizer function register.

4-277. The synchronizer then responds to the requesting computer with an Output Resume signal. The computer, in turn, replies by removing the Function Ready signal. The synchronizer then withdraws the Output Resume signal. The synchronizer, meanwhile, has directed a temporary inhibit update signal to the binary storage register within the countdown translator portion of the unit. Thereafter, the contents of the binary seconds and minutes storage register are placed on the input lines of the requesting computer.

4-278. When the Input Request appears, the unit responds with an Input Ready signal. After the computer has accepted the countdown time data, the Input Request signal is turned off. At this time, the Input Ready signal is turned off. Also, the Input Ready signal from the synchronizer is terminated. The exchanges related to the transfer of seconds and minutes is now complete. The synchronizer then proceeds, automatically, to another input cycle which begins when the computer issues a second Input Request signal.

4-279. There are two input transfer cycles as a result of executing this external function:

- a. Input seconds and minutes.
- b. Input hours and sign.

4-280. The various countdown time word formats are shown as follows:

	11	10	9	8	7	6	5	4	3	2	1	0
Seconds and Minutes:	2^5	2^4	2^3	2^2	2^1	2^0	2^5	2^4	2^3	2^2	2^1	2^0
	11	10	9	8	7	6	5	4	3	2	1	0
Hours:	X	sign	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

4-281. When the Input Ready signal related to the transfer of hours is terminated, the exchange of data related to this external function is complete and the countdown inhibit update signal is released. If a 1000-pps updating pulse occurred while the binary storage register was frozen, the binary storage register is updated at this time. The synchronizer then directs its attention to the alternate computer for the next 10-microsecond interval.

4-282. Load Seconds and Minutes (4602_g). This external function is a typical computer output function that permits preset interrupt countdown times to be transferred from the computer core to the appropriate interrupt time register within the synchronizer. Upon detecting this external function code, the unit responds to the initiating computer with an Output Resume signal. The computer then withdraws the Function Ready signal and the synchronizer responds by dropping the Output Resume signal.

4-283. The synchronizer is now prepared to accept the preset seconds and minutes information from the computer core. The computer next executes an output instruction that delivers the seconds-and-minutes word to the data lines. The data is accompanied by an Information Ready signal. The synchronizer, upon recognizing the Information Ready signal, loads the seconds-and-minutes information into the computer program preset interrupt time seconds-minutes register.

4-284. Following a delay of a few microseconds, the synchronizer returns an Output Resume signal to the computer. The computer responds by turning off the Information Ready signal. At this time, the unit drops the Output Resume line. At this point, the one-word information exchange is complete and the synchronizer now directs its attention to the other computer for at least 10 microseconds.

4-285. It is now necessary to clear this register before it may be reloaded; the register may be cleared either by loading with all zeros or by execution of Master Clear signal, 4600_g.

4-286. Load Hours (4604_g). This external function permits an output instruction to load the synchronizer computer program preset interrupt time hours-and-sign register. This register may be reset with the Master Clear signal, 4600_g.

4-287. Lockout Other Computer (4612_g). If the originating computer has not been locked out, execution of this external function will set a one in the appropriate status register position (2^{10} or 2^{11} , depending upon originating computer). If the originating computer is already locked out, this external function is ignored.

4-288. Clear Computer A Lockout (4614_g). This external function resets status register position 2^{11} to the zero state.

4-289. Lockout this Computer (4613_g). This special external function sets the lockout flip-flop corresponding to the originating computer. This external function is used only during orientation operations.

4-290. Clear Computer B Lockout (4616_g). This external function resets status register bit position 2^{10} to the zero state.

4-291. Enable Interrupt 30 Computer A (4631_g). This external function sets status register position 2^7 to the one state. Later, when the synchronizer detects the manually preset countdown time, an Interrupt 30 signal will be directed to computer A.

4-292. Enable Interrupt 30 Computer B (4632_g). This external function sets status register bit-position 2^6 to the one state. When the synchronizer detects the manually preset countdown time, an Interrupt 30 signal is transmitted to computer B.

4-293. Enable Interrupt 40 Computer A (4641_g). This external function sets status register position 2^5 to the one state. The synchronizer will monitor the comparison between the computer program preset interrupt time registers and the binary storage register. Upon sensing coincidence between the computer program preset interrupt time registers and the binary storage registers, the synchronizer sets the interrupt 40-B flip-flop. This interrupt flip-flop then transmits an Interrupt 40 signal to computer B.

4-294. Master Clear (4600_g). Execution of this external function resets all interrupt flip-flops, enable flip-flops, and lockout flip-flops. This instruction is useful only in special situations where it is guaranteed that its execution will not disturb programs in progress.

NOTE

In general, this external function should be used with caution.

4-295. Clear Interrupt 30 (4673_g). This external function clears the Interrupt 30 flip-flop corresponding to the computer originating the 4673_g. In addition, this external function clears the enable Interrupt 30 flip-flop corresponding to the originating computer.

4-296. Clear Interrupt 40 (4674_B). Execution of this external function clears the Interrupt 40 flip-flop corresponding to the computer originating the 4674_B. In addition, this external function clears the enable Interrupt 40 flip-flop corresponding to the computer originating the 4674_B external function.

4-297. Status Request (4640_B). Upon inquiry from either computer, the synchronizer will respond with a 12-bit status response. The 12-bit status register is an assembly of critical control flip-flops within the synchronizer. The assignment of the various status register bit positions and their significance are:

a. Lockout Computer A (2^{11}). A 1 appearing in the status register bit position indicates that computer B has previously executed external function 12_B lockout other computer.

NOTE

This bit position is an advisory message only and is provided as a means for computer B to transmit the lockout message to computer A. There is no hardware lockout to restrict the activity of the locked-out computer; that is, in an emergency situation, a locked-out computer could clear the lockout and proceed.

b. Lockout Computer B (2^{10}). The presence of a 1 in this bit position indicates that computer A has executed external function 12_B, lockout other computer. The significance of this status bit is similar to the significance of bit position 2^{11} .

c. Last Load (2^9). This bit position maintains a continuous presentation indicating the computer which most recently executed a load external function. A 1 in this position indicates that the most recent load instruction (4602_B or 4604_B) originated from computer A. A 0 in this position indicates that the most recent load instruction originated from computer B.

d. Countdown Hold in Progress (2^8). A 1 appearing in this bit position indicates that the input countdown time is in a hold condition and the countdown time registers are not being updated.

e. Enable 30 Computer A (2^7). The presence of a 1 in this position indicates that manual preset Interrupt 30 has been enabled for computer A.

f. Enable 30 Computer B (2^6). The presence of a 1 in this position indicates that manual preset Interrupt 30 has been enabled for computer B.

g. Enable 40 Computer A (2^5). The presence of a 1 in this position indicates that stored program preset Interrupt 40 has been enabled for computer A.

- h. Enable 40 Computer B (2^4). The presence of a 1 in this position indicates the stored program preset Interrupt 40 has been enabled for computer B.
- i. Interrupt 30 Computer A (2^3). A 1 appearing in this position indicates that the manual preset interrupt for computer A has triggered and an Interrupt 30 signal is being transmitted to computer A.
- j. Interrupt 30 Computer B (2^2). A 1 appearing in this position indicates that the manual preset interrupt has triggered and an Interrupt 30 signal is being transmitted to computer B.
- k. Interrupt 40 Computer A (2^1). A 1 appearing in this bit position indicates that the stored program has triggered and an Interrupt 40 signal is being transmitted to computer A.
- m. Interrupt 40 Computer B (2^0). A 1 appearing in this position indicates that the stored program preset interrupt has triggered and an Interrupt 40 signal is being transmitted to computer B.

4-298. TIME CODE DISTRIBUTION UNIT. (See figure 4-23.)

4-299. The time code distribution unit is physically a portion of the Event Distribution, Recording, and Patching Unit located in the ACE-S/C computer room. IRIG B and AMR B-1 timing codes are received directly from the time code generator located in the ACE-S/C Terminal Patch Facility room. The IRIG B time code signals are routed directly to a Video Distribution and Tape Control Unit patch panel via a connection on the time code distribution unit. The AMR B-1 time code signals are first amplified by a power inverter (PI) logic module, and then distributed:

- a. To the 100-channel event recorder contained in the Event Distribution Recording and Patching Unit, and to the analog recorders contained in the Analog Recorder Unit by means of connections within the Event Distribution Recording and Patching Unit.
- b. To a Video Distribution and Tape Transport Control Unit patch panel via a connection on the time code distribution unit.

4-300. IRIG B and AMR B-1 timing codes are also routed back to the time code distribution unit from the Video Distribution and Tape Transport Control Unit. By appropriate patch connections at the Video Distribution and Tape Transport Control Unit, the IRIG B time codes received may be real or playback (reproduced from magnetic tape) time. In either case, the IRIG B time code signals are first fed to a PI module and then distributed:

- a. To the oscillographic recorder via connections within the remaining portions of the Event Distribution Recording and Patching Unit.
- b. To the Tape Search Time Code Translator Computer Interface Input/Output Synchronizer via direct connections on the time code distribution unit.

4-301. The AMR B-1 time code signals received from the Video Distribution and Tape Transport Control Unit are always playback time information. The AMR B-1 time code signals are first fed to a PI module and then distributed:

- a. To the 100-channel event recorder contained in the Event Distribution Recording and Patching Unit and to the analog recorders in the Analog Recording Unit.
- b. To the console-mounted analog and event recorders in the control room via the Decommutator Distribution Unit (DDU).

4-302. DECOMMUTATOR DISTRIBUTION UNIT. (See figure 4-24.)

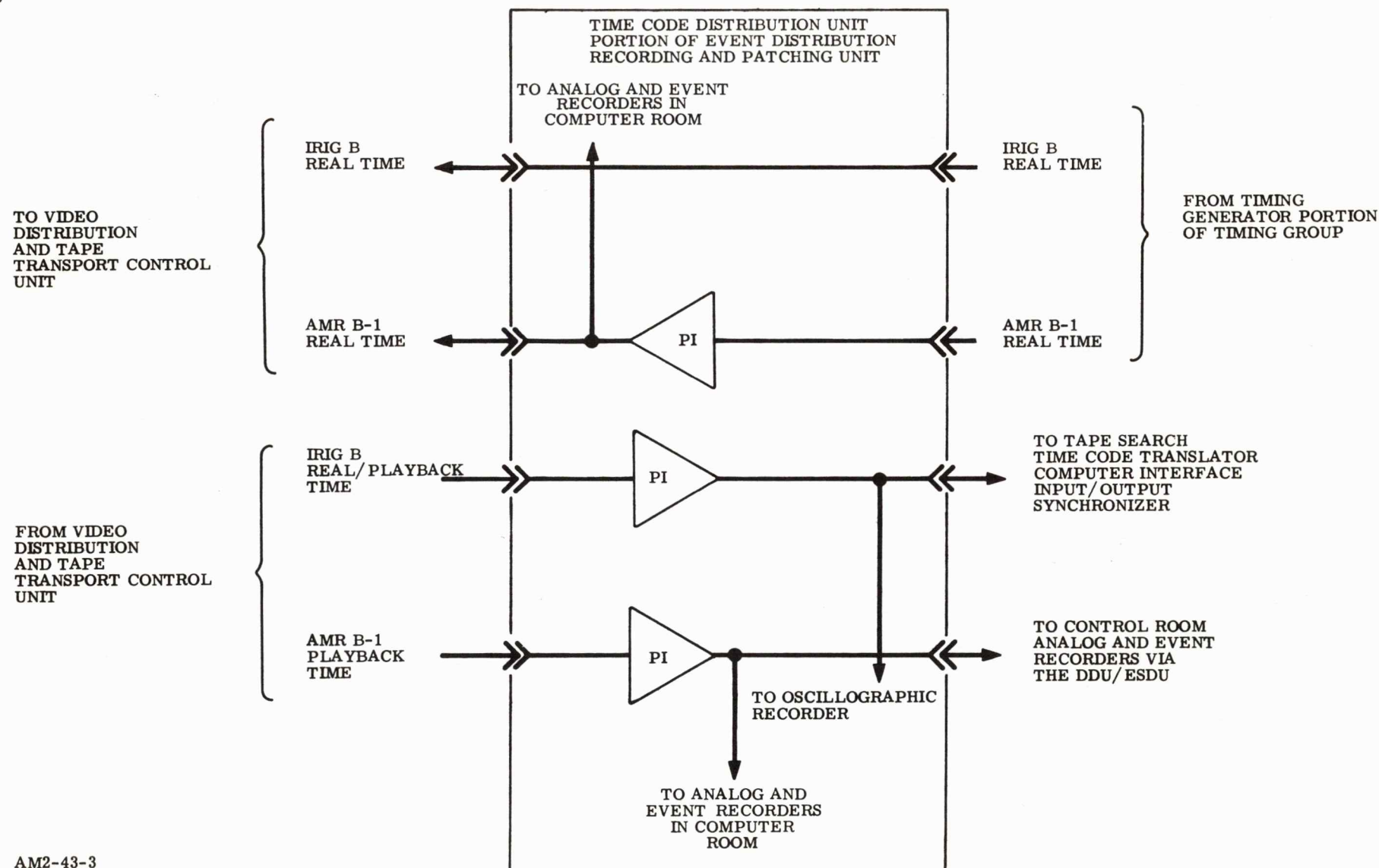
4-303. The Decommutator Distribution Unit (DDU) portion of the DD/ESDU receives both real and playback AMR B-1 time code signals over two separate lines. The real-time AMR B-1 timing signal is received directly from the time code generator, while the playback AMR B-1 timing signal is received from the time code distribution unit via the Terminal Patch Facility. The DDU time distribution circuits are identical for both real and playback timing signals. Each received timing signal is first fed to a logic inverting power amplifier (PI) module and thence to a complimentary driver (CD) module. The output of the CD module is fed in parallel to ten emitter followers (EF's). Eight of the EF modules feed their respective output to an associated control console. Two EF module outputs are spared.

4-304. REMOTE TIME DISPLAY UNITS.

4-305. The ACE-S/C system employs five wall clock display units, three in the control room and two in the computer room, and two console clocks. Each wall clock contains two sets of in-line decimal display indicators: one set for the display of real time (actual or range time), and one set for the display of countdown time. The console clocks may display either real or countdown time.

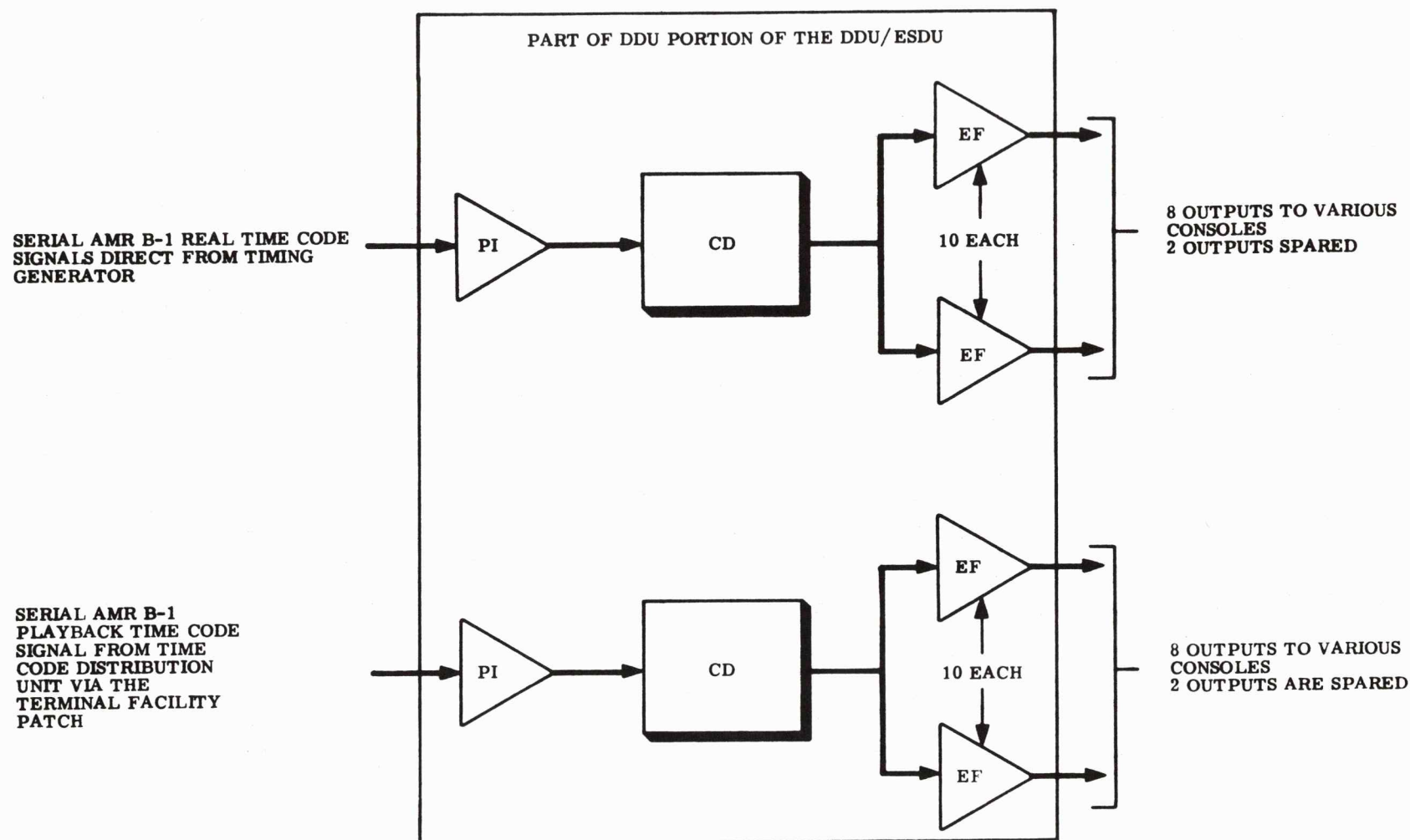
4-306. WALL CLOCK DISPLAY FUNCTIONS.

4-307. The real-time wall clock displays always show the current time of day or range time, never playback real time. The real time wall clock display units consist of nine decimal in-line indicators: three for day, two for hours, two for minutes, and two for seconds. Each indicator is made up of seven separate back-lighted segments that are turned on in various combinations to form the desired decimal character. To provide the necessary back-light control, each indicator receives seven input lines and a common ground return or a total of eight lines per indicator. Each of the real-time wall clock display units receive 63 driven time code lines (seven for each of the nine segmented indicators) and nine ground return lines (one for each of the nine segmented indicators) from the Time Code Generator.



AM2-43-3

Figure 4-23. Time Code Distribution Unit Functional Block Diagram



AM2-44-3

Figure 4-24. Distribution of AMR B-1 Time Codes by the DDU

4-308. The countdown time wall clock displays always show current countdown time, never playback countdown time. The countdown wall clock display units consist of eight in-line decimal indicators: two for seconds; two for minutes; three for hours; and one to indicate plus, minus, or hold. Each decimal indicator is the same as those described in the preceding paragraph for real-time wall clock display. Each countdown wall clock receives 56 driven time code lines (seven for each of the eight segmented indicators) and eight ground return lines (one for each of the eight segmented indicators) from the Countdown Generator.

4-309. Both the Computer Complex Console and the Test Conductor Console contain front panel mounted real and countdown clock display subassemblies. The console real-time clock display units are capable of showing either current range time or the playback range time depending upon the present ACE-S/C Operational Mode. In like manner, the console countdown time clock display units are capable of showing either the current countdown time or playback countdown time. The same number and type of indicating devices are used in the console clocks as are used in the wall clock displays.

4-310. COUNTDOWN GENERATOR REMOTE CONTROL UNIT FUNCTIONS.

4-311. The Test Conductor Console contains a countdown generator remote control unit that is equipped with the same type of control switches that are located on the Countdown Generator unit. By the use of thumbwheel switches available on the remote control unit, the Test Conductor Console operator can set in any desired start count time and stop count time. The remote control unit also contains start, count, stop count, and hold count controls. The remote control unit will only have control over the Countdown Generator when the LOCAL/REMOTE switch on the front of the Countdown Generator is set to REMOTE.

4-312. REMOTE TIME DISPLAY UNIT DESCRIPTION.

4-313. The real-time and countdown time displays utilize filament-lamp indicators to display appropriate numerals and symbols. There are two types of indicators: those that display the numerals 0 through 9 and those that display special symbols such as +, -, or the letter H (used only on the remote countdown display).

4-314. Each indicator displays either a numeral or symbol by discrete combinations of seven illuminated line segments (see figure 4-25). Each of the seven line segments are illuminated by two filament-type lamps, visible from the front of the indicator through an internal mask that determines the line segment configuration. The symbol and numeral indicators contain different masks to achieve the line segment configurations. The symbol and numeral indicators contain different masks used to achieve the line segment configurations shown in figure 4-25.

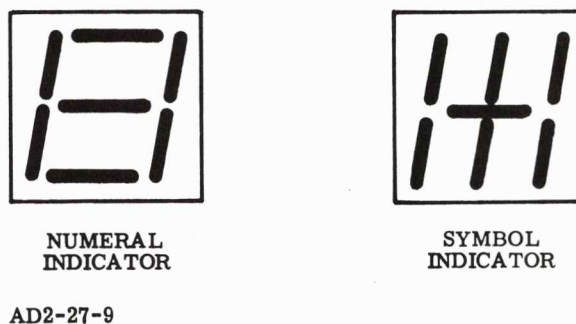


Figure 4-25. Remote Time Display Indicator Mask Formats

4-315. An indicator is activated by a lamp driver assembly containing seven amplifiers, one for each line segment. Each amplifier is driven by a separate input line. A discrete seven-bit parallel code is utilized to generate each number (see figure 4-26).

4-316. The seven-line code required to display any character may be determined by the line segments necessary to form that character. For example, the numeral eight is displayed when all slots in the numeral mask are lighted.

4-317. STATUS MONITORING AND DISPLAY EQUIPMENT.

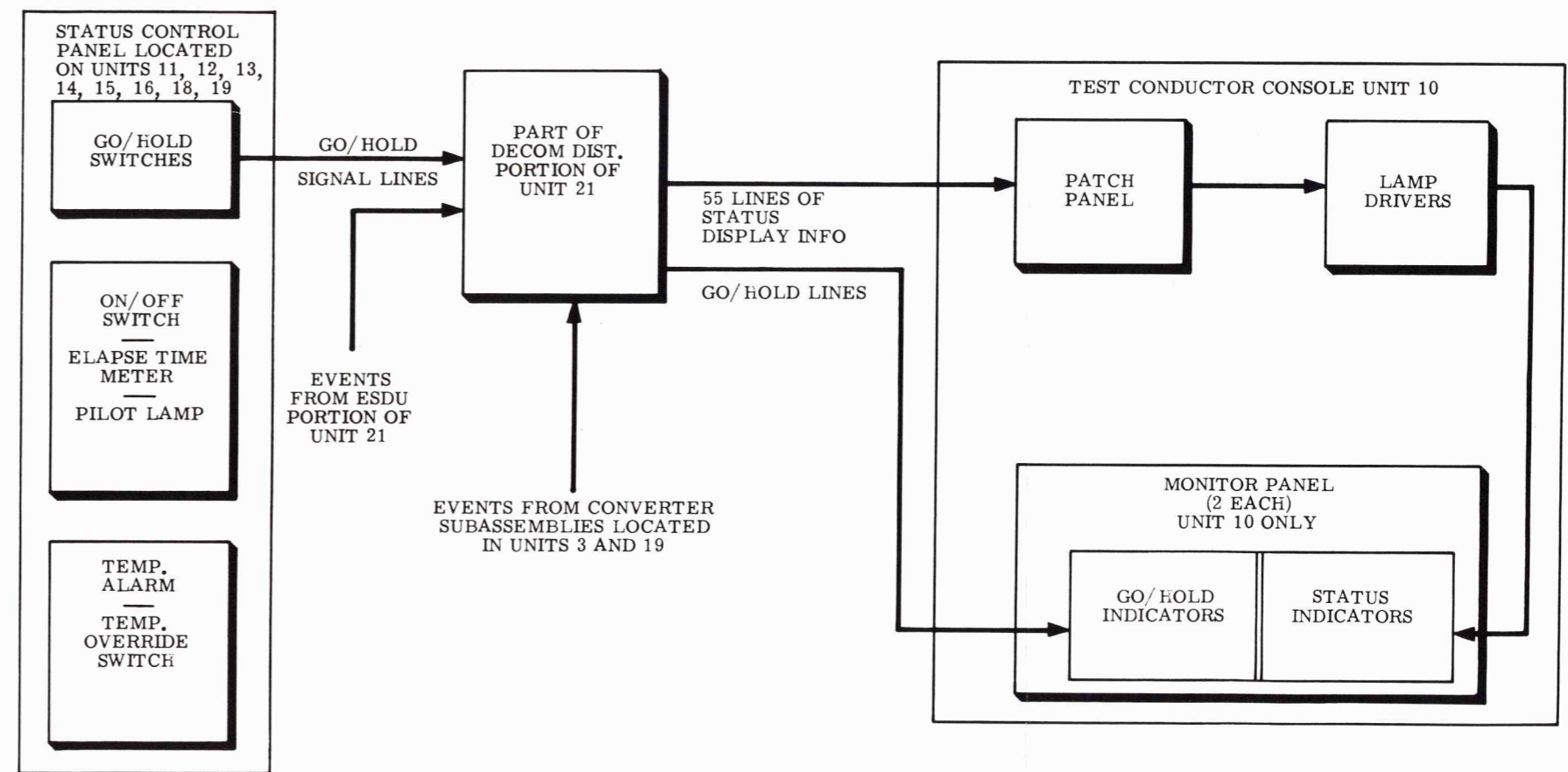
4-318. The subassemblies of the ACE-S/C system units comprising the status monitoring and display system are illustrated in figure 4-27. Status control panels located on various control consoles provide the means to (1) turn the power on or off to that particular console, (2) warn the console operator of a console cabinet overheat condition, and (3) allow the console operator to report his operational status to the Test Conductor by the use of GO/HOLD signals. The GO/HOLD signals from each of the control console status control panels, certain event signals from the Event Storage and Distribution Unit, and special event signals from control consoles containing converter subassemblies are all routed through the DDU to the Test Conductor Console. The GO/HOLD signals received by the Test Conductor Console

7 LINE CODE							CHARACTERS DISPLAYED	
LINE 1	LINE 2	LINE 3	LINE 4	LINE 5	LINE 6	LINE 7	NUMERAL	SPECIAL
1	1	0	1	1	1	1	0	
0	0	0	0	0	1	1	1	
1	1	1	0	1	1	0	2	
1	0	1	0	1	1	1	3	
0	0	1	1	0	0	1	4	
1	0	1	1	1	0	1	5	
1	1	1	1	1	0	1	6	
0	0	0	0	1	1	1	7	
1	1	1	1	1	1	1	8	
1	0	1	1	1	1	1	9	
1	0	1	0	1	0	0	+ - H	}
0	0	1	0	0	0	0		
0	1	1	1	0	1	1		

USED ON
REMOTE
COUNTDOWN
DISPLAY
ONLY

AD3-1-9

Figure 4-26. Display Converter Coding



AM2-45-3

Figure 4-27. Status Control and Monitoring System Functional Block Diagram

are fed directly to appropriate GO/HOLD indicator on a status monitor panel. The event signals received by the Test Conductor Console are first fed to a patchboard, then to lamp driver circuits, and finally to appropriate status indicators also located on the Test Conductor Console status monitor panel.

4-319. CONTROL CONSOLE STATUS CONTROL PANEL FUNCTIONS.

4-320. Each control console status control panel contains three functional groups of switches and associated indicators: (1) GO/HOLD, (2) power control, and (3) temperature alarm.

4-321. GO/HOLD SWITCHES AND INDICATORS. The current operational status of a particular control console may be transmitted to the Test Conductor Console through the use of GO/HOLD switches. The operator of a particular console evaluates the spacecraft test data being received and makes a decision based on his observations, as to whether to continue in the test or to stop and re-evaluate his position or isolate an observed malfunction. To inform the Test Conductor of his decision he may actuate either of two rectangular, back-lighted pushbuttons labeled GO and HOLD. The pushbutton switches are interlocked to prevent simultaneous activation. Upon depressing a switch, it will become back-lighted (green for GO and red for HOLD) and remain back-lighted until the other switch is depressed or by depressing the same switch a second time.

4-322. POWER CONTROL SWITCH AND INDICATOR. A power control switch is provided on each status control panel to control the input power to that particular unit and to each of its associated cabinets. Associated with each power control switch is a power-on pilot lamp and a power-on elapsed time meter.

4-323. TEMPERATURE ALARM. The temperature alarm consists of a red indicator lamp, cabinet temperature sensing units, and a manual override switch. The indicator lamp flashes whenever the cooling air temperature (under operating conditions) in any associated system console rack exceeds a maximum value. An additional lamp is provided in each console rack to identify the location of the fault. Upon activation of the temperature alarm, the unit will automatically shut down after a time delay of 30 seconds. The manual override switch will prevent shutdown should a critical test be in progress.

4-324. DECOMMUTATOR DISTRIBUTION UNIT STATUS DISTRIBUTION FUNCTIONS.

4-325. Only a very small portion of the DDU is allocated for the handling of status information. This portion receives the following:

- a. GO/HOLD status lines from each of the control consoles containing status control panels.
- b. Up to 50 on/off event status lines from the ESDU.

c. Special event lines from control consoles containing converter subassemblies, i.e., the Power and Sequential Control Console Unit and the Communications Control Console Unit.

4-326. This portion of the DDU functions as a junction box and serves only to collectively send all inputs to the Test Conductor Console.

4-327. TEST CONDUCTOR CONSOLE STATUS SUBASSEMBLY FUNCTIONS.

4-328. There are three subassemblies of the Test Conductor Console to facilitate the display of GO/HOLD and event signals received from the DDU: (1) a status monitor panel, (2) a patchboard, and (3) a set of lamp drivers.

4-329. STATUS MONITOR PANEL. The test conductor status monitor panel receives GO/HOLD information lines and up to 55 event status lines. The monitor panel contains two types of rectangular back-lighted indicators. One type displays the status of RF systems, power systems, arming, mission milestones, and other parameters as required. The other type of indicators display the status of each major spacecraft system and are divided into two segments: GO (green) on the lower half and HOLD (red) on the upper half. It should be noted that the reason for a HOLD indication is not presented to the Test Conductor Console operator.

4-330. PATCHBOARD. The Test Conductor Console patchboard is similar to those used in the other control console and provides a means to selectively distribute the incoming event status signal to the appropriate lamp drivers, and thence to the appropriate display indicators on the status monitor panel.

4-331. LAMP DRIVERS. The Test Conductor Console lamp drivers are identical to those used in other control consoles. A detailed description of a lamp driver and its operation is given in paragraphs 3-303 and 3-328. There is one lamp driver element for each incoming event line or 55 total (one lamp driver per event line X 55 lines = 55).