

**APOLLO  
BLOCK II and LEM  
COMPUTER DESIGN REVIEW**

**9 May 1966**

**REVISED**





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## 0. PRELIMINARY MIT/IL COMMENTS

### 0.1 RESPONSIBILITIES

The design review and examination of the Apollo Guidance System Block II Computer reported herein was intended to reflect only on the technical status of the design and associated supporting operations and documentation. Nowhere in the body of this report should the responsibility for elements of the design under criticism or praise be apparent. The responsibilities are actually shared and they overlap among the principal participants somewhat as follows . . .

Manned Spacecraft Center of NASA -- Responsible for defining the basic requirements for the design, providing contractual support to accomplish the effort, and passing upon the acceptability of the design.

Instrumentation Laboratory of MIT -- Responsible for the basic design of circuits, hardware, and packaging and the integration of the computer and its functions into the rest of the G & N equipment, the spacecraft, and the ground test facilities.

AC Electronics Division of General Motors -- Responsible for the administration of the production of the computer and the exercise of the qualification testing, acceptance testing, and integrated guidance system testing.

Raytheon -- Responsible for the manufacture of the computer and for the detailed design and design analysis of portions of the equipment.

Space and Information Division of North American Aviation -- Responsible for the integration of the guidance system (with the computer) into the command module, the generation of CM interface documents, and the identification of the interfacing spacecraft circuits, installations constraints, and spacecraft environment.

Grumman Aircraft Engineering Corporation -- Responsible for the integration of the guidance equipment (with the computer) into the lunar excursion module, the generation of LEM interface documents, and the identification of the interfacing spacecraft circuits, installation constraints, and spacecraft environment.

### 0.2 CONSTRAINTS ON DESIGN

As items of the review are discussed in the body of the report, it will be apparent that no effort was made to provide the justifications or qualifications which led to design features which on some other less confined basis were not "best possible". The design of equipment such as this naturally is the result of tradeoffs among a multitude of conflicting constraints. Some of the more important considerations are outlined here so as to provide a background of the design environment and circumstances.

Schedule -- In October 1963, the basic configuration of the Block II G & N system was substantially identified following negotiations with MSC. However, in June 1964, some basic decisions were made by MSC which lead to considerable changes in the configuration and functions. In particular, the redundant computer was eliminated, the computer was given the task of vehicle stabilization (the digital autopilot) and the computer was required to provide the several new wide bandwidth interfaces with the spacecraft. During this period a sequence of "implementation meetings" among MSC, the spacecraft contractors, and MIT was held to try and define the Block II CM and LEM requirements. A basic outline of the computer configuration definition became available late in 1964. Negotiations on the electrical and mechanical characteristics with the spacecraft contractors offered enough difficulty so that the last computer electrical interface control document was not signed until February 1965, and the last computer mechanical ICD was not signed until July 1965. Meanwhile, in order to meet the needs of the program, a substantially complete release of the computer design was made in the Spring of 1965. Since that time much of the activity has been in making those necessary design changes which became identified as mandatory as a result of problems with the design or as a result of newly identified requirements. The latest requirement changes of note occurred on 13 January 1966, at a LEM "Critical Design Review". This review identified a new interface and new function for the computer ... a three-axis minimum impulse attitude control based upon commands from discrete switches on the rotational hand controllers. In summary, many more optimum designs and many desirable features were deliberately bypassed in order to meet the stringent schedule constraints.

Volume -- Early in the series of implementation meetings in the Summer of 1964, a space for installation of the computer in the command module was negotiated with North American. Although during the implementation meeting series a much more powerful computer was identified and furthermore, that a requirement for moisture proofing resulting in the hermetic sealing of the case was identified, no added volume in the installation was provided. Many compromise decisions were made in the design as a result of the most limited volume allowance.

Miscellaneous -- Other constraints which influenced decisions which might be cited are:

1. The extreme effort to hold and reduce the weight of the computer, particularly in the LEM.
2. The extreme effort to hold down electrical power consumption.
3. The requirement to make physically identical both the computers in the LEM and CM and also to make physically identical the DSKY in LEM with both DSKY locations in the CM. Unfortunately, the physical environment in these two spacecraft is significantly different.

4. The practical desire to save funds and the consequent shortcuts in development testing, comparison designs, etc. This meant that prototype and early production computers could not be made available as desired to provide the early experimental identification of problems and verification of design changes.

### 0.3 CRITIQUE OF COMMITTEE REPORTS RESULTS

The team of computer specialists assembled to make this Block II computer review was made up of members from AC and Raytheon. The substance of their findings is given in Section I through Section VIII and in the appendices. MIT has taken exception with many of these findings and reports its position and justification in Section IX.



## I INTRODUCTION AND SUMMARY

### 1.1 BACKGROUND

This review of the Apollo guidance computer design was performed at the request of the NASA Manned Spacecraft Center. The following is a quote from contract change authorization to AC Electronics.

"Description of Change: It is requested that the contractor immediately initiate a complete design review of the electrical and mechanical design margins to insure adequate performance during the lunar landing mission. MIT has been notified that AC Electronics will be conducting this design review and have been requested to provide all available information regarding design criteria, analysis, and testing to date.

Justification for Change: Recently the Block II and LEM computers have had numerous design problems. The blue nose logic situation, the refusal of computer 601 to operate on the cold plate and the apparently inadequate timing margins (based on tests on computers PC-2 and 201) have given rise to doubts regarding the adequacy of the electrical and mechanical margins throughout the computer."

In addition, this authorization suggested that the computer review should be accomplished by June 1, 1966.

In response to this NASA request, a team of computer specialists was convened. Team members from the AC Electronics Digital Computer Laboratory in El Segundo, from the AC Electronics engineering departments in Milwaukee, and from the Raytheon Co. Space and Information Systems Division engineering departments began the requested design review. This report covers the initial findings of this team and spans approximately the first two months of the design review. The review has not been completed, but the number of problem areas discovered to date warrants a fairly complete discussion of the review and the problems at this time.

### 1.2 SCOPE OF THE INVESTIGATION

This report describes topics ranging considerably beyond the Apollo guidance computer hardware and its electrical and mechanical margins. The review committee realized that "to insure adequate performance during the lunar mission", it would be necessary to investigate more than the design of the computer, per se. Therefore, the committee has also looked into the designs of those equipments which are immediately peripheral to the computer, and into the manufacturing techniques, the testing methods, and the documentation required to realize these designs as functioning elements of a navigation system.



It may at first seem strange that our review did not include the subject of computer reliability. A typical reliability model for an irredundant computer is constructed by counting the piece parts and ascribing failure rates to each part. Little can be done to affect the reliability calculated from such a model once the basic logic structure and electronic parts have been selected. The review has been much concerned with the overall computer dependability, but not in the sense of the conventional reliability model. The review has concentrated on areas of possible design difficulty which would lead to degraded operation rather than to spontaneous failure of the computer components.

### 1.3 METHOD OF INVESTIGATION

At the outset of the investigation a set of ground rules were developed to guide the committee in performing the design review. These ground rules were as follows.

1. This review is an effort to assess the design integrity of the Apollo computer. Cost and schedule impact will not normally be considered as design criteria.
2. The review team will not attempt to assign responsibility for any deficiencies which may be illuminated.
3. The review team will not perform the designs, but will suggest approaches and techniques, if they are apparent.
4. The review team will not assign the design tasks which it recommends.
5. MIT will be kept apprised of the significant team findings by the AC Electronics Program Director, or his designee.

The committee has attempted to judge the technical excellence of the various subject matters investigated irrespective of the organization responsible for the particular topic. The design review was conducted as though the computer were critical to the Apollo missions and essential to the safety of the astronauts. That these assumptions may not be true can completely negate the findings with regard to the design adequacy or inadequacy, and certainly will affect the ultimate decision as to the design changes which are put into the computer.

Ordinarily, an investigation of this type would begin with a review of the computer specification and any other documents describing the functional requirements which the system reflects on the computer. The computer design would then be scrutinized and compared with the requirements of the defining documents. Unfortunately, in this case the procurement specifications for the computer and the computer modules do not exist. The functional requirements were apparently determined during the



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series of implementation meetings, and the review committee has not read the minutes of these meetings. As a result the review has been limited to those properties of the computer, such as the logic design, circuit design, and mechanical design, which can be judged against good practice applying sound judgment. It was necessary for the review team to accept, without question, many of the basic parameters of the computer, such as the instruction set, the memory capacities, operating speeds, and input-output functions. This means that even if the entire mechanical and electrical designs are corrected as recommended by the committee, the ability of the computer to perform the lunar landing mission may not have been completely guaranteed.

The NASA request was for a review of the Block II and LEM computer designs. The production version of these computers begins with one designated C-1 which is different from all previous prototype and production computers in several significant areas. These changes include some new logic design, the use of the expander gate, new multi-layer circuit boards, new memory drivers, new erasable memory mechanical design, new power supply circuits, new electroluminescent panels, new materials and finishes for the computer proper. This first production computer is scheduled for delivery to AC 14 days after NASA had hoped to receive the final review report. The second production computer, C-2, is scheduled to fly. These tight production and flight schedules, combined with many new designs and with further changes as a result of this design review, present a very difficult situation.

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Since the design of the first production Block II computer is not complete and since the design criteria documents for this series of computers are largely nonexistent, it was necessary to adopt an oblique approach to the design review. We have, of course, reviewed those documents and those designs which are available for the Block II system. We have also reviewed those designs, documents, and tests of the Block I and Block 100 computers which appear to be pertinent to the Block II design. As a result of this we have inadvertently uncovered some possible difficulties with the flyable computers. Since some of these computers will fly in manned as well as unmanned spacecraft, the review committee feels an obligation to bring these design deficiencies to light. This will be done by publishing a special report on the specific subject of the Block I-100 findings. That report will follow this one as quickly as we can arrange it. It should be emphasized, however, that a thorough investigation of the Block I-100 computers has not been done by this committee. Possibly the most significant recommendation in this regard would be the establishment of a special flight readiness review committee for these earlier systems.

In order to accomplish this review, the committee en masse interviewed members of the AC Electronics computer integration group in Milwaukee and then moved to Boston for four weeks. During the first two weeks, interviews were held with the responsible Raytheon engineers from the checkout, testing, and design groups. Of the next two weeks, approximately one week was spent interviewing the original designers from MIT. The remaining period of time covered by this report has been





spent by the committee members individually reviewing the work presented by the engineers interviewed, preparing this report, and performing detailed individual reviews of specific areas of the computer design.

#### 1.4 CATEGORIES OF FINDINGS

Findings of the review team are categorized later in this report into four major groups as follows:

Group A: Adequate

This category applies to those designs which have been reviewed by the committee and which have been found to have adequate design margins.

Group B: Marginal

This category applies to those designs which are considered to be inadequate but whose performance is not vital to the success of the mission, or whose inadequacies will manifest themselves only under some worst, worst combination of environments considered to be unrealistic.

Group C: Inadequate

This category includes those designs and situations which have been reviewed and have been found to be unsatisfactory. These designs or situations must be corrected at any cost.

Group D: Indeterminate

This classification includes those subjects which have not been successfully placed into one of the three categories above. In some cases the indeterminacy was caused by the committee's inability to conduct a thorough review in the elapsed time, and in some cases it has been caused by the lack of design information. Each item in this category must be studied further until it can be placed in one of the above categories.

In subsequent sections of this report the category applying to each numbered paragraph will be indicated in parentheses behind the paragraph title. In some cases the committee has felt that it was impossible or inappropriate to apply one of the above four categories to a specific paragraph, and therefore no such indication is given.

There is, of course, another category which contains all of those designs, documents, and situations which have not been reviewed by the committee at all. The committee has tried to be exhaustive in its review of the Apollo guidance computer but it has not been able to work at every aspect of that computer, its manufacture, testing, and documentation. Unless a particular subject matter is discussed in this report, it is not safe to assume that it is adequate, but should be placed in Category D.





## 1.5 SUMMARY OF FINDINGS

This section is intended to provide a brief summary of the more important findings of the design review as it has been accomplished so far. The recommended actions are discussed in Paragraph 1.6. There were 17 working members of the Tiger Team, and each would undoubtedly have provided a different summary of the work which has been reviewed, even though there has been general unanimity in the assignment of the categories A, B, C, and D to the specific topics which are discussed in the remaining sections of this report. There has been some difference of opinion as to the relative urgency of correcting those designs which are inadequate and of pursuing those which are indeterminate. This section is organized in such a way as to convey the urgency as it is viewed by the chairman of the review committee. The more important topics are discussed first, topics of lesser importance are discussed next, etc.

Perhaps the most significant fault uncovered to date in the Apollo guidance computer project is the lack of adequate documentation supporting the Block II computer and its design. The review committee has not been able to find a satisfactory functional description of the task which the computer is expected to perform in the command module, although such a description does exist in a functional interface document for the Lunar Excursion Module. Many documents exist which describe the computer design as it presently is, but these documents are informal and uncontrolled. The formal documents contain significant blanks and significant inconsistencies in the data.

A second feature of the Apollo guidance computer project which is regarded as dangerous and in need of correction is the testing philosophy. There is still vacillation with regard to the probable content of the computer qualification test document and there is some danger that document will not be approved in its final form by the time the first qualification test article is delivered by Raytheon. It is the committee's understanding that this test document will, in essence, provide a qualification test of the computer subsystem to the lunar excursion module mission profile and will qualify the entire guidance and navigation system to the command module profile. This is an unsatisfactory philosophy, since the computer must function in either module, and since adequate self-test programs cannot be performed by the computer while it is also providing control and tests of the guidance and navigation system.

Qualification testing at the module level is not recommended. The present environmental test levels are significantly below the levels which the modules will see in the actual computer during its qualification test, and during the acceptance test, and probably in flight. The available test equipment does not exercise the modules thoroughly enough to prove that they will operate with satisfactory margins in the

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computer. Rather than invest in the more complex support equipment required to provide adequate exercising of the modules, it is recommended that a better qualification test of the entire computer be provided. With the proper program in the computer memory, the individual modules can be thoroughly exercised. It should be stressed, however, that this program must be very carefully designed to provide a proper exercise.

It is the committee's understanding that the computer qualification test will not include a test for electromagnetic compatibility. This could have serious ramifications during system integration. The present interface control documents do not provide satisfactory guarantees that the various subsystems will not mutually interfere with one another. If a test of the subsystem electromagnetic compatibility is not provided, then this test must be provided at the system level. There is danger, of course, that the test at the system level will not uncover problems early enough that they can be corrected in subsequent redesigns of the subsystem. Therefore, EMI testing at the computer level is recommended.

Qualification of the piece parts is lagging and this matter is considered most urgent. Failure of the parts to pass the qualification test should require one of three actions: a) the parts can be designed out of the system, b) the parts can be subjected to a special screen at receiving inspection to uncover the specific weaknesses which are turned up during the part qualification test, or c) the parts can be procured from a different vendor.

The present acceptance testing procedures are deemed to be inadequate because they do not subject the modules to a satisfactory workmanship test. If the present acceptance tests are carried out, the final flight program ropes will not see vibration until the Apollo system leaves the launching pad. Furthermore, the present acceptance test does not provide for measuring the electrical operating margins of the ropes and therefore provides no assurance that the marriage between a specific set of flight ropes and the electronics in the computer (already installed in the spacecraft) will be successful.

With regard to acceptance testing of the rest of the computer modules, the philosophy presently advocated is adequate only if the currently planned black box level maintenance philosophy is strictly adhered to. Up to the present time, the committee has been unable to find any documentation which sets forth the maintenance philosophy. If, as the committee has recommended, the computer is sealed at the time of the final acceptance test, and if no one is permitted to break that seal and replace a module except in the factory, the present acceptance philosophy for the individual computer modules (except for the ropes as noted above) will provide adequate testing. However, this philosophy has the distinct disadvantage of making it impossible for the manufacturer of these modules to sell them off until they are installed in a computer. The maintenance and sparing philosophy for the computers needs to be examined carefully, to be set forth clearly, and to be enforced completely.



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The logic and electrical design of the computer has not been done using a worst-case design philosophy. The committee recognizes that short of providing a completely new design, the problem of fixing up the present design is a very difficult one. It is unlikely that any set of recommended changes will absolutely guarantee a design which will work under all possible circumstances. It is the committee's opinion that the logic overloads must be fixed. Appendix C treats that topic in considerable detail and constitutes the committee's noise analysis. That analysis raises the question whether even fixing the logic overloads is sufficient. Certainly, the noise immunity is improved, but if the noise levels which the committee has seen in its laboratory experiments are actually realized in the operating computer, even a fan-out of five will not provide satisfactory margins. Basically, the answer is we simply do not know what noise margin exists between the tolerance of the circuits and the noise generated in the system.

There is some concern that the present design does not have adequate timing margins, and that it may not work over the temperature range. The review committee has seen no proof that the computer timing design is predictable or that bad timing situations cannot exist in production computers.

The erasable memory design has been questioned in two areas. Much concern has been expressed about the present mechanical design of the module. It is contrary to industry experience that such a module cannot be satisfactorily encapsulated. There is fear that if the present mechanical design is allowed to remain unchanged, wire breakage will result from fatigue of the wires due to the fact that the mass of encapsulation is not mechanically supported.

Electrical design data of the erasable memory is lacking. Paragraph 2.5 presents a discussion of the kinds of tests which are required in order to develop the necessary data for both RCA and EMI modules.

The design margins in the DSKY are certainly unsatisfactory. Mechanically and thermally the design is probably as good as could have been provided by anyone given the constraints which are present in the system. However, the basic decision to use the electroluminescent panels should be re-examined. It is these panels which require the relays which, in turn, have proven to be unreliable piece parts and have also been designed into an unsatisfactory circuit. The electroluminescent panels themselves have serious deficiencies, and have yet to pass their qualification tests. Suitable filamentary segmented displays have existed for some time and some have been qualified for use in military systems. Use of these devices would allow the troublesome relays and electroluminescent panels to be designed out of the system. Use of the incandescent segmented displays would probably require the DSKY to dissipate somewhat more power than it presently does. However, power consumption appears not to be as important today as it was a few years ago. The additional power



consumption will, of course, aggravate an already difficult thermal situation. If the incandescent lamps are used, it would be recommended that the DSKY be provided with a small amount of cooling fluid for the electrical modules.

With regard to the mechanical and thermal design of the computer, the situation appears to be tolerable, but considerable effort has been expended in trying to design a one-foot by two-foot cover which could contain the computer pressurization. There is apparently no firm requirement that the computer have internal pressurization, and there are several critical parts, such as the flight ropes and electrical connectors, which must necessarily be located outside the pressurization.

The use of the Malco pin within the computer structure can be tolerated only so long as field replacement of modules (other than ropes) is absolutely prohibited. The present, needless dissassembly and reassembly of the computer should be stopped, and it is recommended that the quality control man put a seal on the computer at the time of final assembly to prevent unnecessary exposure of the Malco pins to damage.

The voltage alarm philosophy has been criticized because the alarms fail to activate an overvoltage protection circuit. This circuit should be within the computer, but must at least be within the ground support equipment. Appendix A suggests that since the power supply itself has internal short-circuit protection, protection of the computer could be supplied by short-circuiting the output of the power supply. A typical circuit is suggested in that appendix.

The flight processing specifications for the piece parts have been given considerable attention by the review committee. That committee is not universally in agreement on all aspects of the problem, but there is general agreement that the flight processing does not seem to be accomplishing what it was intended to accomplish, since it is generally impossible to get the piece parts through these tests without waivers. Obviously, some changes should be made in the system. This is an area of considerable specialization and even those specialists called in by NASA and AC to help with these problems have been unable to agree on a recommended change to the system. The committee, lacking expertise in this particular art, is forced to defer to the review committee expert and accept the recommendations expressed in Paragraph 4.1

The multilayer boards have already been found to exhibit the usual unreliability associated with the conventional multilayer process. One can expect that perfectly excellent boards will be manufactured one day and subsequent production will be unusable. It is quite possible to provide better incoming inspection than is now given to these boards, and such an inspection process is discussed in Section 4.



The programmers place considerable reliance on the all-digital simulation to uncover problem areas in the computer program. The committee recognizes that this all-digital simulation is absolutely essential for program checkout, but such a simulation does not provide the necessary insight which can be gotten by an adequate analytical approach to some specific problems. The committee feels a general, vague apprehension about the ability of the computer to perform the necessary computations in real time under all conditions of loading on the program, and recommends that the counter increments and external interrupts be analyzed to insure that a worst-case buildup of these inputs will not degrade the system performance.

Many of the specification control documents against which the piece parts are purchased, are not satisfactory. In particular, the SCD covering the micrologic, both the dual and the expander gates, contains certain ambiguities, and does not contain satisfactory noise threshold requirements.

The logic design of the counter fail alarm is considered to be unsatisfactory, since it permits the interface to drop bits without detecting this loss of information. The counter increment analysis referred to previously may show that such a condition is impossible, in which case that aspect of the design would have to be reclassified as acceptable.

The computer power supply module specification allows an unnecessarily large amount of radio frequency noise on the output of the power supply. This noise will detract from the available noise margin of the logic. Adequate filtering and better placement of the parts within the power supply module could effectively reduce the high frequency noise by one or two orders of magnitude.

The standby flip-flop, according to the present logic design, can turn on the standby condition when the computer is first turned on. If the computer operation were momentarily interrupted by a power supply transient, and the computer came back on in the standby condition, some number of seconds must elapse before the astronaut can recognize what has happened and place the computer back in the operating mode. This appears to be a dangerous situation. In addition, the standby indicator is presently driven by logic operated directly from the flip-flop. As a result the light is not an indicator of the true status of the computer.

There are several aspects of the computer which are considered to be adequate, and those are indicated in the following sections of the report. One item not discussed there is the overall logic design of the computer. The fact that the computer can run the several programs which it has run successfully, indicates that, by and large, the logic does what the programmers expect it to do. However, logic design changes are being made fairly continuously and that indicates the need for a detailed logic verification.





## 1.6 RECOMMENDED ACTIONS

This paragraph presents a brief description of the actions which are recommended as a result of the design review findings summarized in the previous paragraph.

### 1.6.1 Continued Design Review

This report is not considered a final design review document. The design review should certainly continue until each of the Category D items has been resolved into a more definite category. In addition, the design review to date has not been exhaustive. Certain aspects of the computer and its associated equipments have not been reviewed at all, and are not even mentioned in the body of this report. The complete computer should be reviewed. A detailed breakdown of the Category D items is contained in Section 2 of Appendix H of this report.

### 1.6.2 Engineering Tests

Certain data need to be developed in order to provide a basis for the design of the computer, and for the design of the final acceptance tests for the computer and the computer modules. This paragraph discusses those engineering tests which fall into that category.

The timing analysis is one of the major tasks to be accomplished. This analysis will require the use of an operating, fully potted, production computer; a computer test set; and a program analyzer console. The timing analysis must develop detailed knowledge of the timing margins at the temperature extremes as well as at room temperature.

The same computer which is used for the timing analysis can also be used to determine the margins which exist between the noise thresholds of the circuits and the noise generated within the wiring of the computer.

The results of the detailed timing and noise studies are required before the program can be written which the computer will run during its final acceptance test.

Another significant task is the electrical testing of the erasable memory module to determine the basic operating characteristics of the core assembly. These tests also must be done over the temperature range using modules produced by both vendors. Special equipment is required for these tests, but it should be possible to rent time on satisfactory equipment at one of the vendor's facilities.

The erasable memory mechanical design has been troublesome. A thorough, operating environmental test of the module should be performed to prove out the new mechanical design.



The new core rope mechanical design must be subjected to a thorough engineering evaluation. Vibration, mechanical shock and temperature shock should be performed immediately. These tests should be operating tests, since the operating margins of the fixed memory can be influenced by mechanical stresses applied to the cores, especially in the temperature and vibration environments.

An engineering evaluation of the signal layer means of interconnecting the logic flat-packs should be conducted. This test should demonstrate conclusively whether or not the signal layer is a satisfactory substitute for the multilayer board. This test would presumably be performed by selecting a logic module whose performance is critically dependent on the circuit board wiring capacities and building that module with the improved signal layer process. A comparison can then be made of the performance of that module with the performance of the same module built using the multilayer boards.

The mechanical and thermal design of the computer is still questionable with regard to three problem areas. There is significant danger of corrosion of the magnesium material, especially at the interfaces with the aluminum inserts. The present series of tests to find some means of overcoming this difficulty should be continued. Tests should continue in an effort to determine the capability of the computer to maintain its pressurization during vibration and thermal environments, and the thermal model computer C-0X should be instrumented and a thorough study should be made of the temperatures developed within the computer modules over the full range of temperatures and heat inputs.

### 1.6.3 Documentation

The design review committee recommends that a serious attempt be made to bring the documentation controlling the computer design, manufacture, and testing up to an acceptable working level. It is strongly recommended that a single organization be given the responsibility of straightening out the documentation, particularly the interface control documents and procurement specifications.

The maintenance and logistics plan for the computer, insofar as the committee has been able to determine, has not been documented. This plan should be developed in detail and documented, and this document should be made a contractual requirement for all of the parties who will be providing maintenance of the Apollo guidance computer.

The specification control drawings against which the piece parts and certain modules are purchased should be revised. Those SCD's which are particularly significant are for the integrated logic circuits, for the multilayer boards, for the erasable memory module, for the fixed memory cores, and for the DSKY relays.



It is strongly recommended that a programmer's manual be compiled to record the restrictions which the computer design places on the programmers.

#### 1.6.4 Test Plans

##### 1.6.4.1 Screen and Burn-in

The present flight processing of semiconductor components is deemed to be generally questionable because of the extreme difficulty of obtaining parts which can pass these tests. While it is agreed that something should be done to make the screen and burn-in tests more reasonable from the vendor's standpoint, there is considerable uncertainty with regard to the detailed recommendations. The committee recommends, therefore, that a study be undertaken to determine if there are testing procedures which can be meaningful in terms of guaranteeing the overall quality of the parts so screened and yet make it possible for the vendors to produce parts which will pass the screen. Certain parts which are not now included in the screen and burn-in process should be; in particular, the relays and the multilayer boards come to mind.

##### 1.6.4.2 Qualification Testing

The committee has recommended that qualification testing at the module level be discontinued but that a satisfactory qualification test plan be developed for the entire computer. This test plan could be a revision of ND 1002037 which would include the worst portions of the mission profiles for both the command module and the lunar excursion module, when the relative severity can be determined. The test should include both profiles if the relative severity cannot be determined.

##### 1.6.4.3 Acceptance Testing

It is necessary to develop a new set of acceptance test plans for the computer and for its modules. This is a significantly difficult task, as is pointed out in some detail in the remainder of this report. It is not feasible to guarantee analytically that the computer has adequate design margins. The acceptance tests must, therefore, guarantee empirically that each computer, as built, has adequate operating margins over the extremes of the environment. The quality of the computer will be as good as the final acceptance test and it is imperative that this final test be exhaustive. The acceptance test procedure must be predicated on data which is developed during the engineering evaluation tests. In particular, the computer acceptance tests must demonstrate adequate margins with regard to computer timing, logic noise margins, erasable and fixed memory sense amplifier thresholds, and erasable and fixed memory drive current tolerances.

The digital computer program which exercises the hardware during these acceptance tests is extremely critical and must be designed specifically to stress those conditions





of the computer which are being tested. In the case of the memory test, the program is almost trivial, it being merely required to generate the two worst-case noise patterns. In the case of the timing margin and the logic noise margin, the program is apt to be considerably complicated and it will be very difficult to determine precisely what the program should consist of.

The rope module acceptance tests must be revised to provide these critical modules with a complete test. It is strongly recommended that the ropes be given a twofold test. The first should be a workmanship test which would prove that there are no bad solder joints or damaged wires in the assembly. This workmanship test should consist of a simultaneous vibration and thermal cycle while the windings of the rope modules are monitored for continuity. Assuming that the module passes the workmanship test, it should then be subjected to a realistic operating test over the temperature range with tests designed to guarantee adequate electrical operating margins. Adequate marginal testing will provide some assurance that each set of ropes will work in any computer.

#### 1.6.5 Design Tasks

The present computer contains several specific designs which have been rated as C - Inadequate. A list of those specific problem areas is contained in Section 3 of Appendix H. This paragraph discusses some of the more important design tasks.

The voltage failure alarms should be redesigned to cause an overvoltage condition to disconnect power from the computer when it is connected to the ground support equipment. The use of the voltage fail alarms to cause a program restart has been seriously questioned and should be examined from an operational standpoint. The alarms should be redesigned so that the undervoltage and overvoltage conditions at which the alarm is indicated are those conditions which are either dangerous to the reliability of the circuits or which will cause the circuits to operate improperly.

The committee recommends that the overloaded conditions in the computer logic be corrected. The committee also recommends that the wire-wrap program be revised to include electrical considerations of the wiring noise in addition to the present mechanical considerations. Introduction of these new constraints into the program should help to avoid conditions of bad noise generation or undue noise pickup.

The oscillator circuit presently uses parts which cannot be qualified to the flight environment. The oscillator could be redesigned to remove the troublesome parts without seriously affecting the performance of the oscillator.

The DSKY utilizes electroluminescent panels which presently exhibit serious quality problems and which require the use of relays, which also have serious quality problems. An investigation should be made of the possibility of substituting incandescent displays for the present electroluminescent panels.



If the electroluminescent panels are retained in the DSKY, the indicator driver modules which contain the latching relays should be redesigned to provide sufficient power to the relays under all conditions of temperature and input voltage level.

It is recommended that a relief valve or a bellows be provided to limit the over-pressure to a value tolerable to a simple cover, thereby simplifying the mechanical design.

Counter failures should be detected and signalled to the computer program. The present logic design is also known to have a minor flaw (see Paragraph 2.1.1.8) and should be corrected.

The logic of the standby flip-flop should be redesigned to prevent its coming on in an arbitrary state. In addition, the indicator light should be operated from the relay which disconnects the power from the remainder of the computer.

#### 1.7 ORGANIZATION OF THIS REPORT

This report is organized along the general lines which the investigation took. There were some aspects of the computer design which significantly influenced several other areas and, therefore, are mentioned in more than one section of the report. This is primarily due to the specific organization or format chosen for the report, and is not intended to imply that those items mentioned more than once are more important than the other items. It is not possible, for example, to treat the Malco pin as just a piece part problem, since it affects the choice of interwiring techniques, the choice of construction processes, and the maintenance and logistics plan for the computer.

Section II contains the bulk of the material and discusses the computer; its mechanical; thermal, logic, and circuit problems.

Section III discusses the display and keyboard which provides the interface between the computer and the astronauts.

Section IV discusses the piece part problems and the flight processing techniques.

Section V discusses the qualification and acceptance tests.

Section VI treats the documents which should provide design definition and system integration information, as well as the documents which are used or are generated in manufacturing the computer.

Section VII discusses those computer programs which are pertinent to the testing of the computer as well as aspects of the mission programs which are intimately affected by the constraints imposed by the computer hardware design.



Section VIII discusses several miscellaneous topics which bear only indirectly on the adequacy of the computer itself. This section includes brief discussions of the GSE insofar as it affects the thoroughness of the testing of the computer and the safety of the computer during these tests. It also discusses the CDU blue nose problem and computer manufacturing techniques. Section IX contains MIT/IL comments on the content of the original report. Following Section IX there are several appendices. These, in general, contain the details of the specific design reviews which have been performed.

6-8-66



## II BLOCK II APOLLO GUIDANCE COMPUTER (AGC)

### 2.1 FUNCTIONAL ASPECTS

The operational criteria which the computer must fulfill for the lunar landing mission have not been documented to the extent that the acceptability of the computer design can be judged by a straightforward procedure. There is apparently no sample problem nor its functional equivalent which is explicitly specified and being imposed upon the designers of the computer by the customer. As a result, many of the characteristics of the computer have not been questioned. Even so, there are some functional aspects which have raised doubts in the minds of the review committee and these are discussed in the immediately following paragraphs.

#### 2.1.1 Alarms and Restart (B)

The alarm situation has been questioned beginning with the choice of the alarm parameters and extending all the way through the techniques used to guarantee a satisfactory restart of the computer program. Even if it is granted that the entire set of alarms is desirable, the disposition of each is inconsistent. In the first place, the identity of the alarm is not generally retained. This should be changed, since continuing use of the computer might depend on the failure mode. Furthermore, the storage of each failure should be unique, i.e., failures which imply impending shutdown can still allow memory access to store the failure data, while others implying loss of memory would require flip-flop storage. The program exit point at the time of the alarm should be saved if at all possible. The recovery routine following a restart can then review the failure type, as well as the locations involved. In the case of parity failure, it may be possible to reserve blocks of memory for scratch pad and blocks for mission data, and the recovery could be handled accordingly.

##### 2.1.1.1 Parity Alarm (B)

A parity failure is treated identically whether it occurs in fixed or erasable storage. This seems incorrect. First, a parity failure in the rope memory due to a transient may not be disastrous. Repeated trials (two or three) should be allowed to read the correct data. Second, parity failures in the erasable memory are allowed to regenerate good parity with bad data, which may act properly after a restart. This could lead to a dangerous condition. A better solution would be to identify the word in which the failure occurred and that the type of failure was parity. Obviously, this is of no use when the failure affects more than one word, such as a sense amplifier would. But in that case, the computer will not run anyway.



#### 2.1.1.2 Transfer of Control (B)

This alarm guarantees that the program does not either run wild or lock up in a one word loop. If an instruction transfers control to itself continuously, the alarm will be indicated after some period of time. If there is as much as one other instruction in the loop the alarm will not be tripped. It is not absolutely known whether this alarm guards against a particularly likely mode of failure, or not. It presumably does not. Therefore, it will detect a small percentage of the possible failures of this kind, and can hardly be considered worth while. The alarm logic also checks to see that a transfer of control instruction is executed within some longer time period. This alarm needs additional study, but it does not seem to provide any high confidence that things are going well.

#### 2.1.1.3 Rupt Lock (B)

This alarm checks to see that the program services at least one new interrupt request within an interval of from 160 to 320 ms, and that no single interrupt servicing routine lasts longer than that same period of time. This alarm is considered marginal because it will detect only a gross malfunction of the computer hardware. There are many critical functions being carried out in the various interrupt sub-routines during several phases of the mission, and these functions cannot be ignored as long as this alarm permits without serious degradation of system performance. By the same token, there are several phases of the mission during which the checking performed by this alarm is quite appropriate. The general question of interrupts is discussed in more detail in Paragraph 2.1.2.

#### 2.1.1.4 Night Watchman (A)

This logic checks to see that the executive program addresses memory cell "New Job" (0067)<sub>8</sub> at least once in .64 to 1.92 seconds. This is a sound alarm technique, but the sensitivity of this implementation is low due to the long sampling time.

#### 2.1.1.5 Oscillator Fail (D)

The computer oscillator provides the basic time and frequency reference to the entire spacecraft, yet its failure is not handled any differently from any other alarm condition. As far as the computer is concerned, when the clock stops the computer stops, and when the clock restarts the computer will restart with no knowledge that anything untoward had happened. If the clock stops intermittently at critical times, say during thrusting, the consequences could be quite severe. Yet this condition is not detected at all by the alarm circuit. It should at least trip a latching indicator and be telemetered on Down Link, assuming that is possible when the oscillator stops.



The oscillator failure alarm does provide a quarter of a second delay when the computer power is first applied. This is a useful function in that it allows the computer power supplies to stabilize and the logic to be initialized before the computer actually begins to run. The committee's investigation of this alarm has not been complete, and since several questions remain to be answered, this particular alarm must be placed in the indeterminate category.

#### 2.1.1.6 Voltage Failure (C)

All voltage failures (+28V input, +14V, +4V) are treated the same. When the +4 or +14 outputs of the power supply rise above their normal values, the alarm turns on the "Restart" light but no attempt is made to turn off the power to the computer, thereby preventing serious damage. It is argued that in flight it is more desirable to allow the computer to burn up than to include more equipment which can itself fail. Since the alarm circuits themselves already constitute a significant number of components, the few additional components for a safe shutdown circuit are easily justified. The additional arguments obtain that most of the computer's life is in ground operation and, even in flight, recovery might be effected from a temporary power excursion, if the computer does not burn up.

There is some question about the undervoltage alarm conditions as well as the over-voltage condition. At the present time the 28 volt alarm threshold is set at 21.6 volts. This appears to be a satisfactory compromise between the 23 volts guaranteed lower limit of the spacecraft power supply and the 18 volts at which the 4 and 14 volt power supplies begin to lose regulation. On the other hand, as indicated in Section III, there is a significant circuit problem associated with the relays in the DSKY. At high temperatures the relay will fail to operate at a voltage level which is higher than the 28 volt alarm threshold. Therefore, this alarm cannot be expected to indicate satisfactory DSKY operation. This is not considered to be an inadequacy of the alarm circuit, however, but an inadequacy of the DSKY circuit. If the DSKY relay circuit cannot be corrected, the alarm threshold should be raised to the value dictated by the circuit.

#### 2.1.1.7 Restart (D)

Each of the above alarms causes the main computer program to restart and the restart light to be lit. The hardware provides no clues to the nature of the difficulty which created the restart and, therefore, the restart program has no knowledge of the particular difficulty from which it is trying to recover. Certainly, the restart procedures should be different if the restart were due to a parity failure in erasable memory or in rope memory. There is not sufficient information available with regard to the detailed nature of the restart program to allow us to judge whether this is a serious problem or not. It would appear to be a questionable approach for the



lunar landing, during which time the computer is providing direct control of the LEM. In addition, continuous restarts, with no clue as to reason, make checkout of the computer and its integration into the system much more time-consuming than it would be otherwise.

The restart also provides an input to the warning filter, and repeated restarts are necessary before the AGC Warning light will be turned on as a result of the output of the filter exceeding the circuit threshold. The rationale for this appears to be that the computer and its program are designed to tolerate restarts, since restarts happen even in the laboratory environment. As a result, restarts are treated quite casually, and diagnosis of an individual restart cause is not normally attempted.

The current restart program devotes a significant amount of erasable and fixed memory to establishing recovery points to protect against scratch pad contamination. Not only is the protection doubtful, but without consideration of the failure type, it is dangerous. For example, an oscillator failure of several seconds duration could be obscured from the astronaut's recognition and could allow a restart that would look like an unimportant transient. The same amount of storage devoted to identification and analysis of the failure effects might prove more valuable.

A hard-wired restart seems desirable so the astronaut can command a restart rather than depending on the alarms. Such a switch would be useful in the event the computer gets locked up in some sort of a program loop and cannot respond to the normal verb/noun inputs through the keyboard.

A considerable fraction of the computer circuitry is used to generate the alarms and the restart signal. There is some danger that a failure in these circuits will prevent operation of an otherwise healthy computer. This could be prevented by providing the astronaut with a manual override of the restart.

#### 2.1.1.8 Counter Failure Alarm (C)

This alarm occurs if a counter increment fails to happen following an increment request, or if counter increments happen too frequently. This logic has recently been found to be faulty and a logic design change is required. Appendix B treats this redesign in detail. In addition, the counter fail alarm philosophy appears unsatisfactory. This alarm does not cause a restart but does provide an input to the AGC warning filter. This means that a single counter failure will not be detected and that a certain frequency of failures is required before the warning signal will be energized. Up-link and PIPA pulses are handled through the counter increment logic. While no definitive system specification exists, it seems highly unlikely that the system can tolerate undetected failures of the ground-to-spacecraft communication, or of the accelerometer counters.





In addition, there is some fear that counter activity is not guaranteed to be satisfactorily processed at the time of peak loading. cursory analysis seems to indicate that if a counter update pulse were lost, a likely candidate would be an optics pulse from the Optics CDU. CDU pulses can arrive at the rate of 6.4 kc so that during a burst, the optics pulses arrive every 156 microseconds or 13 memory cycle times (MCT). Therefore, the computer must service the optics update request some time during the 13 MCT interval or lose the information when the next optics pulse arrives on top of the previous one.

X, Y, Z, Trunion, and Shaft CDU's send pulses to the AGC at the same time so that once counter incrementing is initiated, the five CDU E-Memory counters will be incremented in the above order with the optics CDU's (Trunion and Shaft) being processed last. Counter increments are enabled only between instructions, keeping in mind the exception that counter increments are inhibited before the Extend, Relint and Inhint instructions.

An optics update pulse could be lost then, if one of the sequence of events occurred as illustrated in Table 2-1 or Table 2-2.

DCS	3 MCT
Relint	1 MCT
Extend	1 MCT
Time 2	1 MCT
Time 1	1 MCT
Time 3	1 MCT
Time 6	1 MCT
CDUX	1 MCT
CDUY	1 MCT
CDUZ	1 MCT
CDUT	1 MCT
CDUS	<u>1 MCT</u>
	14 MCT

Table 2-1

Divide	6 MCT
Inhint	1 MCT
Extend	1 MCT
Time 6	1 MCT
CDUX	1 MCT
CDUY	1 MCT
CDUZ	1 MCT
CDUT	1 MCT
CDUS	<u>1 MCT</u>
	14 MCT

Table 2-2

The above sequences indicate that if the five CDU's send pulses to the AGC during the divide instruction, counter increments are inhibited for the six MCT's of that instruction. Increments are also inhibited by the Relint and Extend instructions so that all counter activity is inhibited for a total of eight MCT's. After Extend, counter increments are enabled and all counters are processed according to their priority as shown in the examples.





The probability of the above sequences occurring when the CDU's are being updated is unknown to the review team. Perhaps the above combinations can never occur. On the other hand, over a long period of flight time when the CDU's are updated many times over, the probability of the above sequences occurring certainly increases.

The LORS needs at least the minimum specifications which are presently applied to the rendezvous radar system, and if an optics pulse is dropped, those specifications will not be met. It also seems likely that the AGC will not be aware that it is performing calculations on bad data since a single missing update pulse is not detected by the alarm circuits.

In summary, it is felt that a thorough simulation of peak counter activity must be performed to assure that sufficient counter increment margins exist in the AGC, and that no counter increments will be lost. Otherwise, the alarm circuits must be redesigned to be sensitive to the loss of a single increment.

#### 2.1.1.9 PIPA Failure (A)

This alarm occurs if no pulses arrive from a PIPA during a 312 microsecond period. It also occurs if both plus and minus pulses occur simultaneously, or if a period of time between 1.28 and 3.84 seconds passes without at least one plus and at least one minus pulse arriving. This alarm does not cause a restart but appears as an input bit which can be sampled by the program.

#### 2.1.1.10 Scalar Alarms (B)

There are two scalar alarm circuits. One triggers if the 1.28 second stage of the scalar (stage 17) fails to produce pulses. This signal is sent to the test connector and also turns on AGC Warning directly. The second scalar alarm is activated if the scalar stage which normally operates at 100 pps is operating at a higher frequency. This signal is not sent to the test connector but does provide an input to the warning filter. This circuit will detect regular miscounts of the early scalar stages but is rated as marginal in view of the small amount of logic which it checks. Repeated failures of the 100 pps scalar are required before a warning is produced. Intermittent or transient failures of the scalar will not be detected.

#### 2.1.1.11 AGC Warning (B)

The AGC Warning light is turned on directly by the scalar fail alarm or by failure of the primary 28 volt supply to the computer, and is turned on as a result of an output from the warning filter. Inputs to the warning filter are Restart, Counter Fail, Voltage Failure in the standby mode, and Scalar Double Frequency Failure. The AGC warning circuit detects gross failure of the computer but does not protect against many possible intermittent or transient failures. The circuit itself is



fail-safe in the sense that the warning signal will be generated if the alarm conditions exist or if the 4 volt power supply is lost.

### 2.1.2 Interrupts and Counter Increments (D)

Interrupt requests to the computer may come at times which are mutually asynchronous and interaction of these interrupts is unavoidable. Logic within the computer treats these interrupts on a "first come-first serve" basis as long as they occur singly. If two or more interrupt requests arise simultaneously the one with highest priority is serviced first. The one with lower priority is remembered and is serviced later. A request with higher priority is not allowed to interrupt a subroutine which is presently in progress but will be remembered (stacked), and those interrupts which are stacked will be serviced in order of their priority after the present subroutine is finished. There appears to be no logical or program guarantee that one interrupt program or a cascade of several interrupt programs will not cause the loss of a low priority request. The programming rules are presently not written down, and the programming conventions which prevail appeared so variable (depending on the programmer interrogated) that fear has arisen that a serious build-up of interrupt and counter increment activities may result in the loss of some information at the computer interface.

There is one request, called T6RUPT, which provides the basic timing by means of which the computer program controls the LEM engines and attitude jets. Since the computer performs the digital autopilot function, the accuracy with which these times are measured can be important. The documents which define the acceptable granularity of the control signals has not been reviewed. The programmers have said that the granularity will be as long as 15 milliseconds, unless each interrupt program specifically watches for the occurrence of the T6 counter overflow and provides a program branch when it recognizes that condition. This places a considerable burden on the interrupt programmers, since the comment was made that the T6RUPT should be serviced no less often than every three milliseconds. A hardware high priority interrupt could be created by the T6RUPT signal such that this highest priority request will be able to interrupt the subroutines which are responding to lower priority requests.

The design program load on the computer is said to be 80 percent. When all programs are combined the 20 percent margin would appear to be adequate, except that it does not guarantee proper handling of short duration peak loads. Some comfort has been taken in the past from the program load histograms developed on the digital simulator at MIT. This simulator cannot possibly produce a worst-case loading since many of the interrupts which can pile up are totally independent and asynchronous. Furthermore, the simulator does not flag interrupts which have been delayed so long that a second request is received before the first is acknowledged. It is



understood that such a feature is presently being written into the simulator and will be available in the future. In view of the abundance of other alarm circuitry, it is surprising that the simple logic to detect an unanswered interrupt was not incorporated in the AGC.

The same general comment applies to the counter increments. These are relatively low frequency binary inputs which are either summed into a core memory location or are assembled into a word in a core memory location. These operations are performed during memory cycles which are stolen from the program. These increments are also asynchronous with the running of the program and are not individually taken into account by the simulator in analysis of the overall program timing. Since increments cannot occur within an instruction (because the main arithmetic adder is used to provide the incrementation), low priority increments might be lost if a long instruction, as is divide, holds up servicing of the increments and if all of the increment requests occur simultaneously (see Paragraph 2.1.1.8). A program timing analysis which takes into account counter increments as well as interrupts should be undertaken immediately.

### 2.1.3 Maintenance and Logistics (C)

In reviewing the design, testing, and checkout of the computer and its modules, the subject of the Malco pins kept recurring. There are several thousand of these pins in the computer, and the computer structure requires that these pins be blind mated at the time any module is plugged into the tray. There was not sufficient volume allowed within the computer for protective skirts around these connectors or for pins to guide the insertion of the modules. There is some danger that the pins will be slightly bent or broken when the module is inserted into the tray. This makes field disassembly of the computer extremely risky.

The committee has been told that a black box maintenance philosophy has been adopted for the G and N system, and that a failed computer will be returned to the factory for analysis and repair. This philosophy has already been violated for those computers which are currently in the field. Since they are not flyable computers, we need not be overly concerned with these violations. However, current practice requires that when a computer has passed the final acceptance test at Raytheon, it is disassembled and given a visual inspection before it is reassembled, with the attendant danger to the Malco pins, and shipped to AC. When the computer is received at AC it is again disassembled and given a visual inspection, after which it is reassembled with additional danger to the Malco pins. It is strongly recommended that the computer be sealed at the time of final assembly before the acceptance test begins, and that this seal be broken only by a qualified person in the computer factory, in order to prevent trouble during the assembly process. In order to aid the assembly process in the factory, jigs should be provided to align the modules and the Malco pins during the module insertion.



If the black box maintenance philosophy is not rigidly enforced in the field, and if the committee's recommendations for acceptance testing computer modules (discussed fully in Paragraph 5.2.2) are not heeded, then it is quite likely that "green" modules will find their way into the flight computers. These are modules which will have been sold off without vibration or adequate thermal testing and which will have been installed in the computer in the field. With the present acceptance test philosophy, there is a high probability that flight program ropes will see vibration for the first time during lift-off. This seems like an extremely risky policy. It is highly recommended that a firm field maintenance policy be established; however, in view of the probability that this policy will be violated, it is also recommended that the acceptance tests for the modules be made complete.

## 2.2 MECHANICAL DESIGN

There are several documents which typically purport to specify the environment which the computer will see, and, therefore, which tend to dictate the mechanical design of the system. Perhaps the most important single document in this category is the qualification test plan, since that is a firm test procedure to which the designer of the computer must commit the product of his design. As will be pointed out in Section VI, this document does not exist for the Block II computers. The designers of the equipment have marked up a previous edition of the qualification test specification and have designed the computer to withstand the test as they believe it will be specified when this document, ND 1002037, is finally approved in the new Revision C. The review committee was faced with the task of judging the probable mechanical design margins of this computer against this incomplete qualification test specification. Other documents were also reviewed, in particular, the mechanical interface control documents, to see that the limitations imposed by these would be properly applied to the computer design.

### 2.2.1 Structure (C)

The production version of the Block II and LEM computers will be built of magnesium. All previous computers were aluminum. Engineering evaluation tests on simulated computers indicated that their structural integrity was probably satisfactory with the exception noted below. The transmissibility of the structure from the mounting points to the modules within the trays was found to have a maximum of 15. This is an acceptable number for such a structure. The production computers made of magnesium are expected to have smaller transmissibilities, and Raytheon is planning to install a foam damping material (made by Union Carbide) which should tend to reduce the resonances even further. The structural integrity of the present computer design should be verified on a representative magnesium structure with the proposed damping materials included.



The principal structural problem is attributable to the decision to pressurize the computer. It is apparently very difficult to design a cover 12" x 24" which will stand the anticipated 20 psi overpressure which would occur in a condition of high heat input and loss of cabin pressure. According to the present dimensions of the various parts of the computer structure, if the cover bows at all under pressure the computer will exceed the maximum vertical dimension allowed on the mechanical interface control document.

A test structure designated C-0X is being prepared at this time. It will consist of magnesium trays, covers, and mid-tray spacer, and an aluminum rope header. The trays will be wire-wrapped and foamed, and dummy weighted modules will be plugged into the trays. Five dummy rope modules and one live Zantow rope will be installed. Testing of this mechanical model will include vibration, shock and salt spray. Unfortunately, the magnesium covers cannot be obtained with gaskets. Therefore, pressure testing will be done with aluminum covers. As a result this test will not conclusively prove or disprove the structural design adequacy. This proof will have to wait on the qualification tests planned for later this year. Meanwhile, of course, computers are being built.

There seems to be no general requirement for the AGC or the DSKY to be pressurized. Moisture sealing appears to be adequate. There are many vulnerable parts, principally connectors and rope modules, which are located outside the pressure seals and which are protected from the corrosive effects of the atmosphere and moisture by conventional seals. Although the number of connector points within the computer is far greater than the number which are outside the pressure seals, it seems inconsistent to protect part of the connector points and not all. It is recommended that the pressurization be limited, if it is required at all, by a relief valve set to blow off at a few psi above ambient. Or, as an alternative, and since the volume of entrapped air is not very large, a bellows could be arranged which would allow a positive pressure of a few psi to be maintained within the computer, even in the LEM where the air pressure will vary radically. This arrangement would be considerably more bulky than the valve but would also probably be more reliable.

The rope header, which is an aluminum structure mounted externally to the Tray B, has recently been redesigned to overcome a major difficulty. While there is some hope that the redesign has eliminated the problem, additional analysis will be required before it can be given a clean bill of health. This rope header assembly contains the connectors into which the rope modules themselves plug. The computer is normally shipped without ropes installed and without these connectors covered. In view of the fragile nature of the connectors, discussed in Paragraph 2.2.4, these connectors should be covered at all times when ropes are not actually installed.





### 2.2.2 Materials and Finishes (D)

The extensive use of magnesium in the structural members of the Block II computer has introduced the possibility of serious corrosion problems. This problem is aggravated by the fact that electrical currents will be flowing through the structure and a dissimilar metal (aluminum) is pressed into the magnesium. A committee made up of representatives from MIT, Raytheon, and AC is presently working on this corrosion problem with the objective of finding a water barrier to keep the aluminum-magnesium interfaces dry. It is assumed that they will be successful in this for the areas around the fasteners which mount the covers to the trays and the computer to the cold plate. There is still the interface between the aluminum rope header and the magnesium mid-tray spacer to be concerned about. If corrosion occurs in any of these areas it can possibly lead to degradation of the structural members, although that is not of major concern, and it may also introduce contamination into the sub-assemblies and into the spacecraft.

Ground pins are presently planned to be installed directly in the magnesium trays. The connector pins themselves are a brass material and they will be installed in an aluminum insert which will be pressed directly into the magnesium tray. These interfaces are also candidates for corrosion. There are many ground pins inside the sealed computer. There are also several in the connectors which are outside the main computer seals. Ordinarily, they will be protected from the atmosphere by the gaskets which seal the connector housings to the computer case, except in the case of the test connector which may be uncovered, or covered only with a simple mechanical protection, and the rope module connectors before the modules are installed.

All these areas of difficulty are presumably recognized by the committee which is presently working on the problem, and straightforward solutions can probably be found, but these solutions should be reviewed.

There has been some considerable discussion of the finish system to be used on the exterior surfaces of the computer. These discussions have indicated that it is a rather complex problem which is further complicated by the differing requirements of the LEM and the command module with reference to such things as toxicity, emissivity, thermal conductivity, etc. It is presently understood that NASA will specify the finish system according to a recent decision. Therefore, no statement can be made with regard to the adequacy or inadequacy of the computer finish.

### 2.2.3 Thermal (D)

A dummy model of the early Block II computer was constructed of aluminum and instrumented with thermocouples. This model was subjected to the worst-case internal and external heat loads and a thermal map made from the resulting measurements. That map has been analytically extended to account for the use of magnesium.



Figure 2-1 is the thermal analog of the computer in a 5 psi gaseous atmosphere with a surrounding structure at 160°F. This provides the worst-case high temperature within the computer. ND1002037 requires testing the computer in a different environment, namely, in a vacuum with the surrounding structure at 160°F. This situation is depicted in Figure 2-2, and results in lower temperatures. Since the various elements of the computer are designed to operate at +70°C, that requirement alone embodies some safety margin, since the thermal maps do not indicate temperatures that high within the computer.

An equivalent map for the lowest operating temperature was not made. It should be. The requirement for the computer to operate at 0°C (or -10°C as some references state) seems to be quite reasonable, again probably providing some margin over the expected lowest operating temperature.

The temperature gradients across the computer are as important as the absolute temperature. Gradients across Tray A will detract from the d-c noise margin of the micrologic. Temperature differences of about 10°C have been noted across the tray, with another 3.5°C difference in the self-heating of the elements, resulting in a 13.5°C difference in the junction temperatures. The consequences of this are discussed fully in Appendix C.

Temperature gradients across Tray B will have a deleterious effect on the operation of the erasable memory, since the memory cores and the memory drivers are in different modules and the temperature sensing elements are in the driver modules, not in the module with the cores. As a result, the drive currents will not be compensated according to the requirements of the cores. This difference in temperature will subtract from the normal drive current tolerances. Whether this is a serious matter or not cannot be stated at this time, since the thermal characteristics of the erasable memory module have not been determined. It would be possible to compensate for any steady-state difference in temperature between the ferrite cores and the drivers, during the selection of the nominal resistor values for the memory driver module. Any change in the temperature difference due to variations in the ambient would still subtract from the driver current tolerances, however. At the moment this is not considered vital since the cores and the temperature compensating diodes are at nearly the same temperatures.

#### 2.2.4 Module Interconnections

The electronic modules of the computer are interconnected by means of Malco pins which are set into the module housings and the tray structure. The Malco pins extend into the tray and interconnection of these pins is accomplished by an automatic wire-wrap machine.

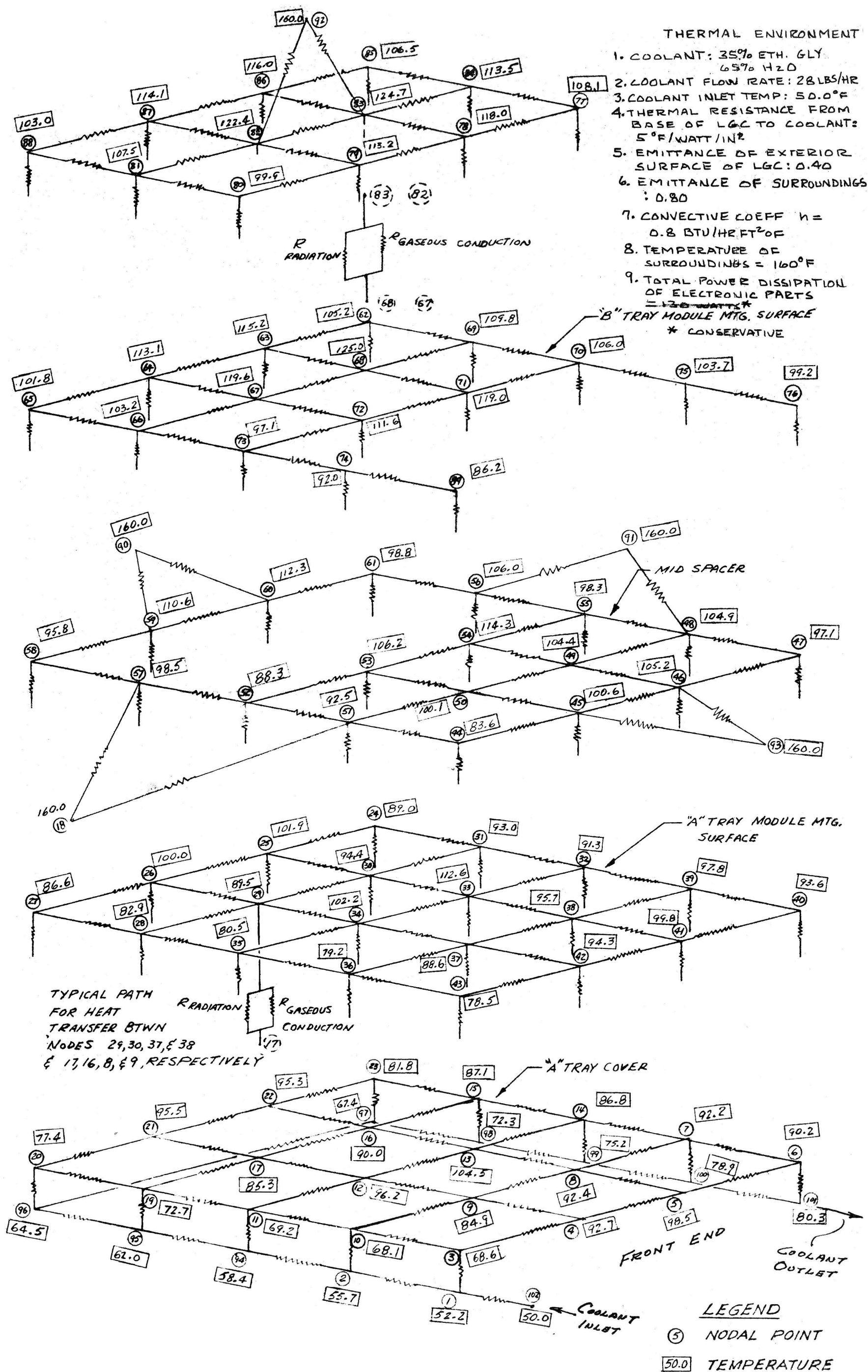


Figure 2-1. Computer Thermal Analog







#### 2.2.4.1 Malco Pins (B)

There has been a long history of successful use of the Malco "Wasp" pins as electrical connectors for the Polaris guidance system. These were relatively large pins spaced on .200" centers. The equivalent connector in the Apollo system is the Malco "Miniwasp" which mounts on .125" centers.

All experts on the subject express concern over the immediate or potential problems associated with the new Malco pins. The original design of these pins was determined to be particularly fragile, and the pin has been redesigned to prevent the fracture which had been occurring. The new pin should be given a new part number to prevent use of the old design. Many objections remain, however. The pin is pressed into place without the benefit of the structure as a supporting guide, and installation damage is extremely difficult to detect. Insertion of the module into the tray connector is blind, leaving doubt as to whether these pins have been bent or broken in the process. All connectors suffer from difficulties of this kind, more or less, however, the Malco pins seems to be especially vulnerable. Small weight and volume were extremely important in the design of the computer and no space was allotted within the structure for pins to guide the insertion of the module or for skirts to protect the male Malco pins when the module is not inserted in the tray.

The committee feels that it would be impossible to suggest the use of another type of connector at this point in the program. We also feel that field assembly and disassembly of the computer is extremely risky and the maintenance philosophy described in Paragraph 2.1.3 should be made an official Apollo procedure, well documented and completely enforced. In addition, it would be reasonable to expect that an insertion fixture could be provided in the factory to aid insertion of the modules and to minimize the probability of damage to the Malco pins.

If all these recommendations are implemented, the Malco pins can be considered marginal, but not dangerous. If the procedures are not changed to account for their fragility, the pins would deserve a rating of inadequate (C).

#### 2.2.4.2 Tray Wiring (D)

The Block 100 computers had shorts in the tray wiring due to what has been termed cold flow of the wire insulation. This presumably occurs when a teflon-insulated wire is subjected to small but constant pressure against a sharp corner, such as the Malco pins have. This continuous pressure does not result in immediate cutting of the insulation but rather in gradual regression of the insulation. A new wire insulation and a new potting method have been adopted for the production series of computers to improve this situation. If the shorts were, in fact, due to cold flow these methods are probably adequate. However, there have been some recent indications that other



computer companies experience shorts in the wire wrapping process which are not due to cold flow but are due to misadjustments of the Gardner-Denver machine. Presumably, we must still depend on the DITMCO test to pick up these shorts after the trays have been potted.

The length of the wires in the tray is of some concern since the wires are capacity loading on the micrologic elements and may also be a source of coupled noise where wires run parallel for a number of inches. In a computer which measures 12" x 24" there are a few wires as long as six feet and several wires as long as three feet. This problem would not be especially serious in the production computers if it were possible to guarantee that the capacities from the wires to the chassis and the capacitive and inductive coupling among the wires would remain constant. Noise and timing results seen on one computer would, therefore, be extendable to all other computers. However, the nature of the wire-wrapping process is such that it cannot place all of the wires in the same relative location from one tray to the next. As a result, there are likely to be considerable variations in these troublesome parameters. A rigid interconnection technique, such as a multilayer board or a welded wire matrix, would be preferable since the capacities and inductances would be nearly constant. However, such a radical change in the method of constructing the computer cannot be recommended at this time. The alternatives are discussed in Paragraph 2.4 insofar as they impact the loading and the noise margin.

The lengths of the wires in the tray are presently determined by a computer program which specifies the exact routing of each wire. The only restrictions placed on the program were those inherent in the wiring patterns available with the Gardner-Denver machine. It is strongly recommended that an electronic engineer be assigned the task of implementing certain optimizing features within the wire-wrap routing program to reduce the probable difficulties mentioned above.

Many of the wires in the tray are much longer than required, and minimization of the total wire length should be one important criterion. In order to minimize noise coupling between wires, it would be desirable to restrict the number of inches any two wires can run in the same channel parallel to one another. With such restrictions placed on the program the variations mentioned above may not be as significant as they are in the present system.



## 2.3 POWER SUPPLY

The general design of the computer power supply has been reviewed and is discussed in detail in Appendix A. That discussion is summarized in the following paragraphs.

### 2.3.1 Power Distribution and Grounding (C)

MIT is presently operating on the informal information that power dropouts of between 20 and 100 milliseconds can be expected. This is in direct conflict with the primary electrical interface control document MH01-01327-216, which states:

"Power Interruption: There shall be no interruption of dc power to loads from prelaunch through earth landing flight phases for normal or emergency operations modes."

This ICD provides a transient test which superimposes noise pulses of less than 20 microseconds duration on the main power bus into the equipment being tested. These pulses can be positive or negative, but clearly do not constitute a power dropout. The LEM electrical interface control document provides essentially the same statements, although they are different in detail. If these documents are wrong they should be corrected and satisfactory transient protection should be provided in the computer power supply.

These interface control documents do not specify the amount of noise which the computer is allowed to put onto the power bus, and the standard electromagnetic compatibility test has been eliminated. If all of the equipments in the spacecraft are permitted to dump unlimited amounts of noise on the power bus, there is serious doubt that the pulse noise test described above is likely to be adequate. There is even grave doubt that the system will function. The source impedance of the power bus as seen by the computer is not specified. The average power loads of the computer are specified in the ICD MH01-01327-216, but there is no limit to the peak currents which can be drawn at the computer power supply input terminals.

The grounding system used originally inside the Block 100 units has proven inadequate. That technique consisted of tying a common logic ground through an inductor back to single-point ground, and keeping that ground separate from the case. The computer was found to be susceptible to EMI. After this experience all grounds were connected to computer chassis.

The power supply low, as well as all other computer signal lows, are presently separated from 28V dc low by a 25-microhenry coil. Since the computer zero volts dc is internally connected to the chassis of the computer, the coil is paralleled by the circuit through the spacecraft structure. Since the true single-point ground is located a considerable distance from the computer, there could be large circulating ac currents which would pass through the coil, generating large voltage transients.

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In addition, the effect of these chassis currents on the noise margins within the computer is yet to be determined. It is not now possible to give the internal grounding method a clean bill of health, but it is recommended that a noise interference fragility test be performed on a completed G and N system with and without the inductor in the circuit. There is little hope that any analytical work would be fruitful when discussing the possible noise paths of equipment within the spacecraft.

Figure 2-3 is a power and ground diagram for the computer. Regarding Figure 2-3, note that +4, +14, and 0V dc are brought to this connector, presumably as test points. If so, they should be buffered inside the computer for protection.

### 2.3.2 Power Supply Circuits

A detailed analysis of the power supply is presented in Appendix A. It is summarized here.

#### 2.3.2.1 Standby Transient (B)

There is a considerable transient on the output of the power supply when the computer goes into the standby mode. The 4-volt power supply can have an output of 8.5 volts at this time. This transient is not considered detrimental to the operation of the computer.

#### 2.3.2.2 Noise Output (C)

The power supply specification permits noise of 0.4 volts peak-to-peak of unlimited bandwidth on the power supply output. Noise of approximately this amount at a frequency of about 30 megacycles has been observed. This noise could be detrimental to the proper operation of the logic circuits and will certainly reduce the calculated noise margins. This noise is apparently caused by the switching regulator, and careful placement of the components within the power supply module appears to be the only technique which has worked to reduce the noise. Additional filtering and shielding of components within the module would probably improve the situation. Use of a toroidal core in the switching regulator choke, rather than the present laminated core, might reduce the radiation from the choke. Additional filter capacitors in the trays would also be helpful. In view of the probable small noise margins (see Paragraph 2.4.2), it is important that this noise output be eliminated.

#### 2.3.2.3 Overvoltage Protection (C)

The computer power supply has a current protection feature which prevents an accidental short circuit, external to the power supply, from damaging it. The power supply is a switching regulator between the +28 volt power bus and the computer circuits. Several failure modes exist which will cause the power supply output to approach 28 volts. It is true that if the power supply, or the logic circuits driving it,

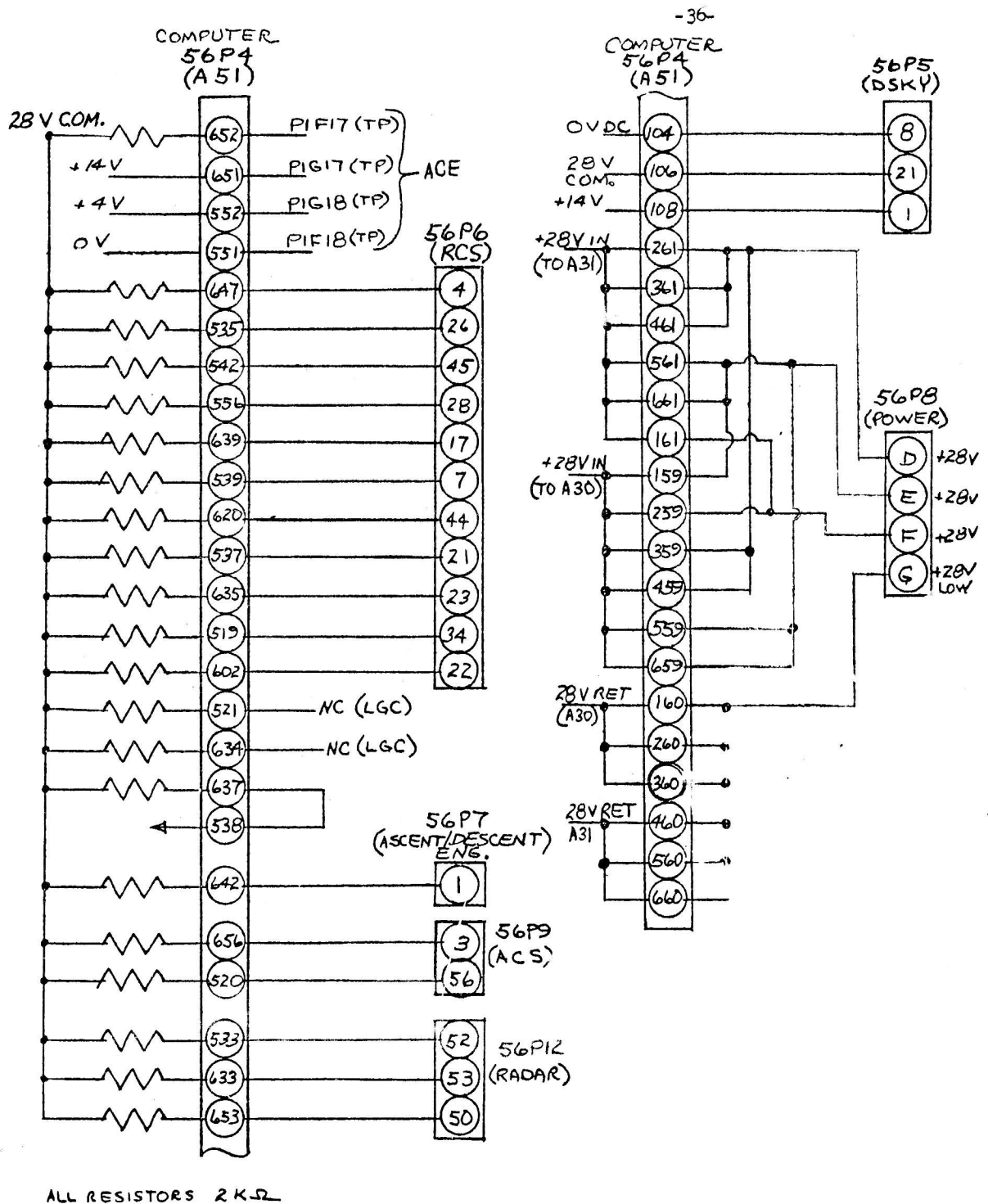


Figure 2-3. Power and Grounding Diagram



fail in flight there is little to be gained by providing an overvoltage protection. On the other hand, the first 18 months of the computer's lifetime will be spent on the ground. During this time, the computer is exposed to complete destruction if the power supplies lose control. One way of protecting the computer would be to provide a silicon-controlled rectifier across the output of the power supplies. Appendix A suggests the form of such a circuit. This rectifier can be fired when the output voltage exceeds a certain value. A sufficiently long pulse can be required to fire this circuit so that noise spikes will not trigger it. If the SCR is triggered when the computer power supply is operating normally, the current protection feature will shut the power supply down without damage to it or the computer. If the overvoltage protection feature is not desired in flight, the SCR circuit could be disabled by a switch.

#### 2.3.2.4 The Drivers (D)

There are three transistors in the switching regulators, Q9, Q10, Q11, which are connected in parallel. There is no way to test the power supply module to determine if these three transistors are working. As a result, one of these transistors may fail during the assembly process and the remaining two transistors be overloaded for the entire lifetime of the computer. The procurement specification for the driver transistors does not provide satisfactory guarantees that one of these three transistors will not run away and destroy itself, and perhaps destroy the power supply and/or the computer as well. The simplest solution to this problem would be to replace the three separate transistors with a single unit. A 2N3467, or equivalent, would be a satisfactory choice. If the addition of another part type is intolerable, then the addition of a base resistor for each of the present transistors would help to equalize the load somewhat. As things now stand, considerably more data on the basic characteristics of the transistors is required before the circuit can be judged safe or not as regards the probability of thermal run away.

#### 2.3.2.5 Factory Tests (B)

The factory tests do not check to see if the power supply control circuits draw abnormally large power. Such a test could easily be provided. It would merely require measuring the input power with a minimum load on the output. Also, the short circuit test is done at a low duty cycle. There is no reason it should not be made a continuous test.

#### 2.3.2.6 Differential Amplifier (B)

Three items have been discovered in the design of the differential amplifier which are not in accordance with good practice. They are not expected to give rise to any difficulty, however. They are 1) operation of the Zener diode at the wrong current, 2) a ratio of 10:1 to the collector currents of the two halves of the amplifier, and 3) a ratio of 3:1 in the input resistors of the amplifier.



## 2.4 LOGIC

The design review committee has not yet been able to judge the adequacy of the overall logic design of the computer. There is a general consensus that the self-test programs which have been written to date demonstrate the ability of the logic to perform the instruction set outlined in Memo AGC No. 9. A considerable amount of work remains before this feeling can be verified beyond any question, however, since logic design errors are still being found in the prototype computers. That alone would indicate that a fairly complete design review of the logic is desirable. The following paragraphs treat those particular topics of the logic where problems have been encountered or where problems are suspected.

### 2.4.1 Noise Margin (C)

One of the inherent advantages of the resistor-transistor logic (RTL) circuits used in the Apollo guidance computer is their superior speed/power ratio as compared to other forms of logic. This is achieved by minimizing the magnitude of the signal swings. As a result, one of the disadvantages of this kind of circuit is its sensitivity to external and self-induced noises. The measure of this sensitivity, or lack thereof, is called the circuit noise margin. This noise margin is a function of a number of things besides the integrated circuit parameters. It is a function of the noise on the power supply, the temperature gradients within the computer structure, the method of wiring the computer, etc. Appendix C presents a detailed discussion of this problem. The computations in that appendix are summarized in Table 2-3. These are the "1" level thresholds. The "0" noise threshold has a similar trend, but cannot be calculated readily due to operation at the knee of the circuit saturation characteristic.

FAN-OUT	NOISE THRESHOLD		
	0°C	25°C	75°C
4	93 mv	172 mv	90 mv
5	48 mv	105 mv	44 mv
5 (interface)	45 mv	92 mv	62 mv
6	14 mv	68 mv	6 mv

Table 2-3. Calculated Noise Thresholds of Apollo RTL Circuits





In these noise calculations the supply voltage was assumed to be at its nominal value of 4.0 volts, and the junction temperatures were assumed to be all identical. In the real computer temperature gradients do exist across the tray, and when these are taken into account the noise thresholds may be reduced by about 24 millivolts. This results in negative noise margins for the signals overloaded by 20 percent (Fan-out = 6). That means they will not merely be susceptible to noise, they cannot be expected to work at all. It must be emphasized at this point that the numbers which are required for these calculations are not contained in, nor are they implicit in, the micrologic procurement specification. There is only one known method of guaranteeing a satisfactory noise margin at the temperature extremes and that is to make such a guarantee an explicit part of the procurement specification.

Preliminary tabulations show that of the eighty overloaded micrologic signals in the computer A tray, nineteen are overloaded by 16 percent or more, ten are overloaded by 20 percent, and seven of the nineteen drive blue noses. In addition, most of the overloaded signals occur in the highly active modules, A7 through A11, which contain the central processor and its associated service gates. Appendix D tabulates these overloaded signals.

The next question to be determined is: what is the expected noise, and how does it compare with the predicted margin? Appendix C also treats that matter. There are long wires in the tray. Some of these long wires are driven with what amounts to micrologic buffers and feed loads which are concentrated some distance from the driving source. This situation was simulated in the laboratory. Photographs taken of noise induced in adjacent wires indicate that in a one-foot parallel run of wires spaced as much as 1/8 inch apart, the noise generated can be 400 to 500 millivolts. Due to the lower sensitivity of the logic elements to high frequency pulses, this signal is equivalent to about 160 millivolts dc noise. Such noise level, coupled with the thresholds indicated in Table 2-3, would result in an intolerable situation.

The fact that the computers have been working can be explained. The noise thresholds were calculated for combinations of worst-case micrologic elements, located at unfortunate temperature extremes within the computer. It is improbable (but not impossible) that such a worst-case will occur. The noise generated within the real wiring of the computer is indeterminate, but the probability of worst noise generators running parallel for some distances to most sensitive circuits is also improbable. Within the logic modules the rigid interconnecting wiring provides good assurance that the situation will not vary significantly from one production computer to the next. Unfortunately, the same is not true of the wrapped wiring in the trays. There the variability is unknown, but will be considerable, and there is where the long wires exist.

Appendix C also indicates the recommended solution to this problem. In fact, there is no direct solution which will guarantee that all production computers are free of



problems. The recommended procedure is to add a marginal test which will essentially measure the noise threshold of each computer as part of the acceptance tests. Those computers which fail the test can be used for hangar queens, simulation computers, or other non-flying jobs. Only those computers which pass the test with adequate margins should be allowed to fly.

#### 2.4.2 Timing Margin (D)

The design review team has been unable in the allotted time to perform a detailed timing analysis of the Apollo guidance computer. The Apollo computer is not a clocked system in the conventional sense and the logic has been designed empirically using a breadboard computer to set up the logic chains and adjust the logic circuit delays to make the computer work. This amounts to tuning up the computer once it has been built. An illustrative example is described more fully in Appendix E. It is urgent that a detailed analysis of the timing margins be performed in such a way that these analyses will be pertinent to the production computers. There are two possible approaches.

The MIT approach is to go through an operating computer, signal by signal, and observe that there are adequate timing margins. This is a difficult task. MIT estimates that this analysis will take three months once they have been given a representative computer. We have no way of judging the accuracy of that estimate. It is imperative, however, that this analysis be done on a production computer. Therefore, some computer, such as C-1, should be made available to for this purpose. The computer trays must be potted and the modules must use circuit boards which are identical to the final production computer configuration, since the capacities on the signal wires in the circuit boards and in the tray play a prominent role in determining the propagation delays through the logic. The trays must be potted since the dielectric constant of the potting compound is estimated to be 3. Once the detailed analysis has been accomplished at room temperature, it will be necessary to extend this analysis to the two temperature extremes, 0°C and 70°C. This can perhaps be done by identifying those signals which appear to be marginal or which are known by the computer designers to be critical, and by monitoring them during thermal testing. The timing margins of the computer must also be checked by running the clock frequency up and down from two megacycles while the critical signals are monitored. The program which the computer runs during this test is very critical and must be intentionally designed to stress the logic circuits. An obvious block of logic to be concerned with is the adder, and sets of worst-case numbers should be cycled through it while the test is being performed. There are undoubtedly other equally critical gate chains, however, and tests must be defined which stress them all.



Once this test has been performed on a computer, it is possible that changes must be made in order to rectify certain problems. Once these changes are made, the changed computer must then undergo this same testing procedure, although perhaps only the areas of change need be investigated thoroughly. There are some other pitfalls along this road; one being that the computer must be fully operating while the test is performed. If the memory fails to operate over the temperature range, then it will be impossible to test the logic of the computer and little or nothing will be learned of the logic timing margins until the other problems are fixed. A second pitfall is that, even if the first test is completed satisfactorily, it is a test of only one computer. There are known variations in the circuit parameters which affect the timing margins, and these variations are large enough to make it probable that the timing chains of each individual production computer will differ significantly from one another. It would, therefore, be necessary to subject each and every flyable computer to this timing margin test over the temperature range.

There is an alternative approach. It also will require a good deal of time, and an estimate of the amount of time is not available today. The approach would require a logic designer and a bookkeeper (preferably a computer program) to go through the logic diagrams, line by line, signal by signal, and define the timing situation at the input to each and every NOR gate. In order to do this there are three different sets of data required. The inherent micrologic propagation delays must be known as a function of fan-in and fan-out, and the variation in these delays must be known. The nominal value of the collector load resistors and the variations must be known. The nominal multilayer circuit board capacitances must be measured for every signal conductor and the expected variation in that capacitance must be generated. Finally, the tray wiring capacitance must be known and the expected variations in that capacity must be determined.

The wire-wrap card deck printout contains a listing of the signal conductors in each tray and the length of the wire. It may be possible to provide a satisfactory estimate of this wire capacity as a function of its length and the level on which it is wrapped. This estimate should, of course, be confirmed on a fully potted tray.

The bookkeeping program which the logic designer will use will then keep track of the accumulated expected delays and the statistics of these delays as a function of all these measurements. The logic designer can then identify groups of NOR gates which function as flip-flops, AND gates, and OR gates. If the analysis of the logic is carried forward from the two megacycle clock generator, the logic designer should be able to observe the nominal delays and the variations of the delays at each of these functional circuits and make some statement of his confidence that the circuit timing is adequate. He must observe that the flip-flops are presented with a pulse of some minimum duration, that the signals at the inputs to the AND gates will overlap for some minimum time.



The advantage of this approach is that it will pertain to all production computers. If it can be demonstrated that a satisfactory timing margin exists when the delays are at their, say,  $2\sigma$  limits, then some inference can be made of the probability that one of the 44 production computers will not have satisfactory timing margins. If the probability is sufficiently low, detailed testing of the production computers is not vital. If the probability is sufficiently high, then the same testing procedures will be required as for the other approach.

The disadvantage of this approach is that a special digital computer program must be written and a logic designer must go through the logic in very careful detail. An additional disadvantage is that an enormous amount of circuit capacitance data must be collected. The feeling is that the second approach is likely to take at least just as many man hours and just as many calendar days as the MIT approach, but the result could be a significantly greater insight into the actual expected performance of the computer.

#### 2.4.3 Blue Nose (A)

The use of the expander gates in the computer appears to be an adequate solution to the previous blue nose problem. The expander gates are somewhat more susceptible to the overload condition than the conventional micrologic. This matter is also treated in Appendix C. Specific consideration is given to the expander gate procurement specification in Paragraph 4.2.

#### 2.4.4 Ring Counter (A)

The early Block II computers have experienced failures due to ring counters hanging up in an undesired state at turn-on. A logic modification has been made for inclusion in all Block II computers which adequately corrects the situation.

#### 2.4.5 Module A18 Standby Flip-Flop (C)

The logic associated with the standby flip-flop permits it to come on in an arbitrary state determined by the parasitic loading of the circuits and the gains of the NOR gates in that circuit. The logic design should be altered to initialize this flip-flop properly to prevent the computer entering the standby mode accidentally.

#### 2.4.6 Standby Indicator (C)

The standby light in the DSKY is driven from the standby logic. It is possible that the circuitry which follows the logic and which actuates the standby relay could malfunction. If this were to happen the light would not indicate the true mode of operation of the computer. This circuit should be redesigned to drive the light from the relay.



## 2.5 ERASABLE MEMORY

There are three principal aspects of the erasable memory which have received considerable attention; these are, mechanical design of the stack, the magnetic properties of the stack, and the designs of the driving and sensing circuits.

### 2.5.1 Mechanical Design (C)

There has been a long history of mechanical difficulties in the erasable memory modules. Both the Block I and Block II engineering evaluation and module qualification tests have disclosed a variety of problems. The wide temperature range ferrite cores are magnetostrictive and must be protected from any stress due to thermal gradients or vibration environments. Although these cores are fully encapsulated in a resilient silastic material which is commonly used for potting aerospace memories, this particular memory has shown trouble when the potted assembly was subjected to thermal shock tests. In fact, cores, wires, and connector pins have been fractured. This suggests that the silastic material is not of the right composition or is being processed improperly, otherwise it would remain resilient far below the temperatures to which this memory is tested.

Previous designs have shown difficulty with the hard epoxy mold breaking free from the module header, which leaves the bulk of the plastic potting material mechanically unsupported. The most recent design leaves the side supports off the module altogether to provide for expansion during thermal cycling. This leaves the mass of the potting material supported principally by the wires. It is feared that with the present arrangement, wire fatigue will take place during vibration. This design is incomplete at the present time and evaluations are still being performed. The memory modules which are presently being made are certainly satisfactory for ground use, but their use for flyable computers would not be recommended at this time. The module should be redesigned to support the magnetic assembly firmly.

### 2.5.2 Magnetic Design (D)

The erasable memory drive circuits are not worst case designed. Nominal values of drive current measured on breadboard circuits provided the basis for the core and core stack specifications. Raytheon engineers are presently attempting to establish manufacturing limits for the memory drivers and sense amplifiers. It is impossible to determine whether or not the limits thus established will guarantee satisfactory operation of the memory without detailed shmoo plots which establish the operating limits of the core stack. Since such shmoo plots have never been produced for either the RCA or the EMI core stack, typical shmoo plots made at ACLA for an avionics computer memory are shown and described below to illustrate their use and to indicate the degree of variability found between core mats employing nominally identical cores.





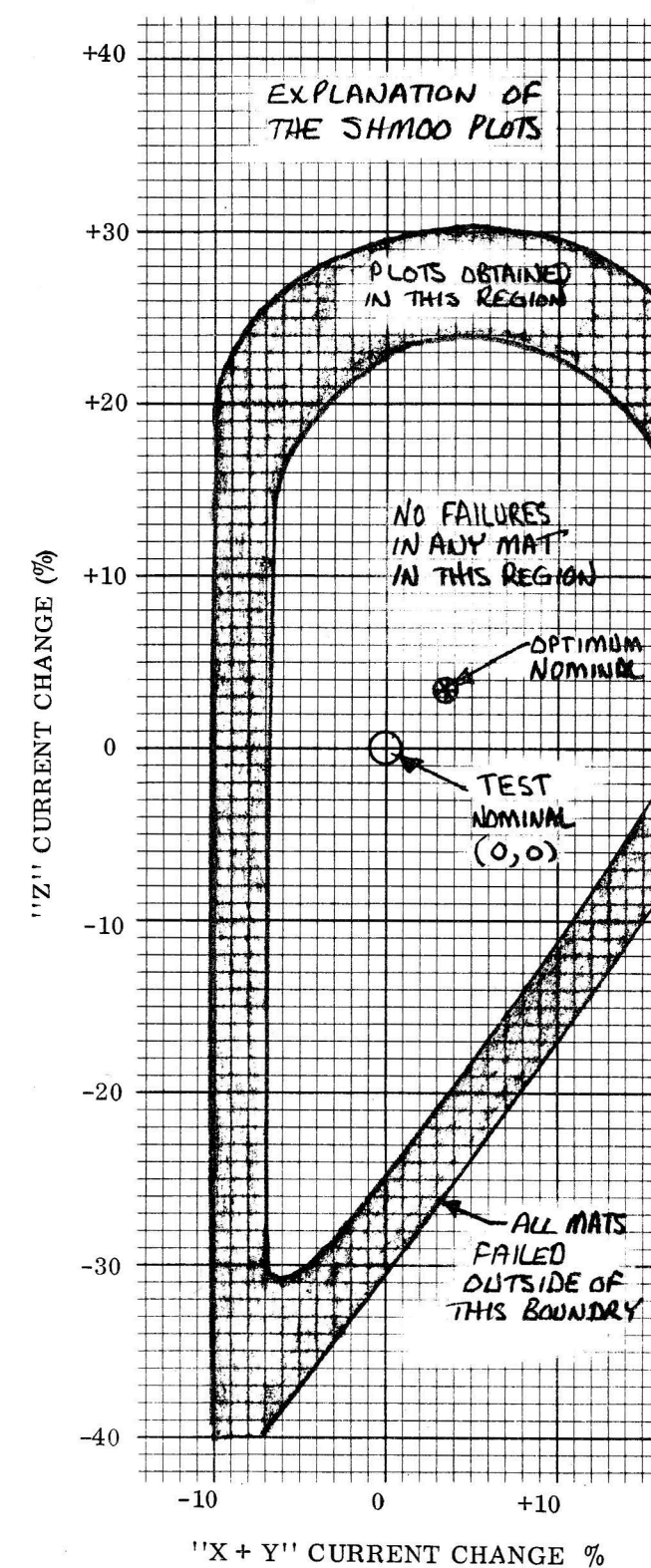
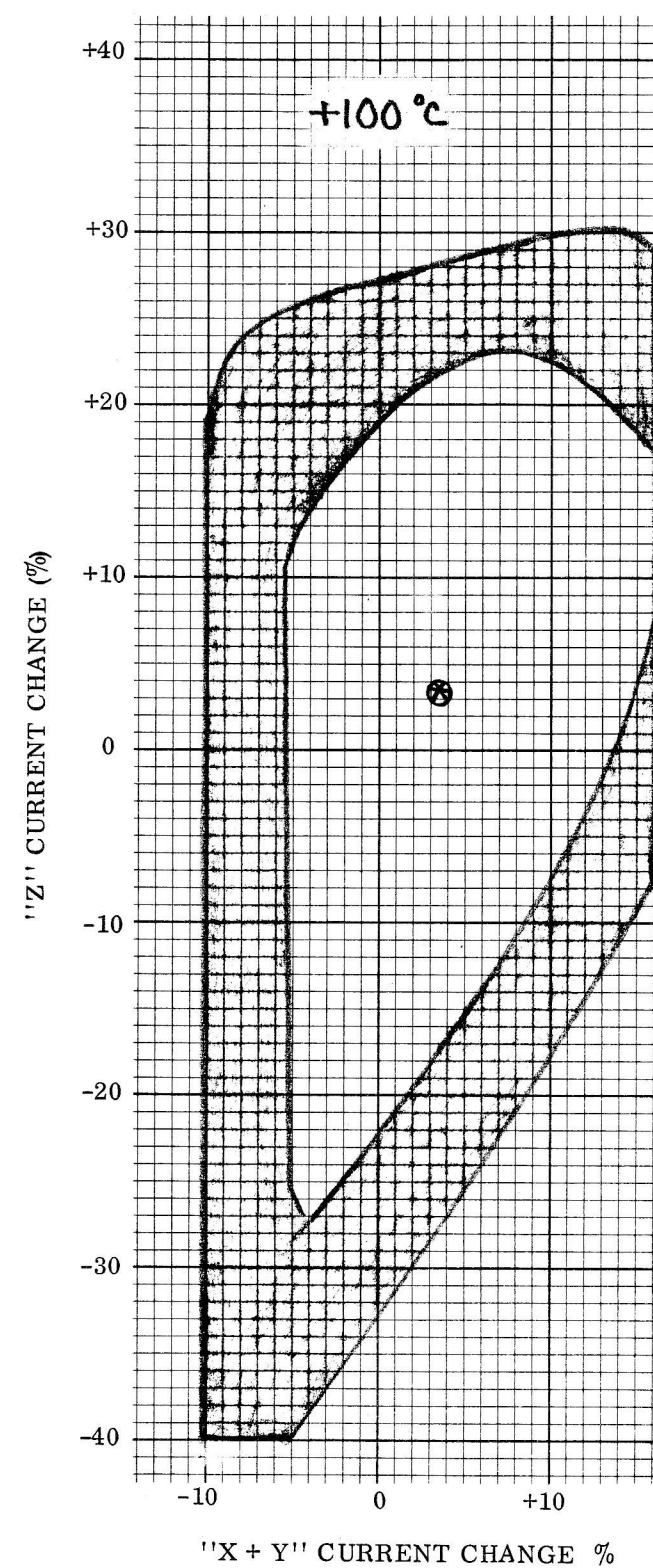
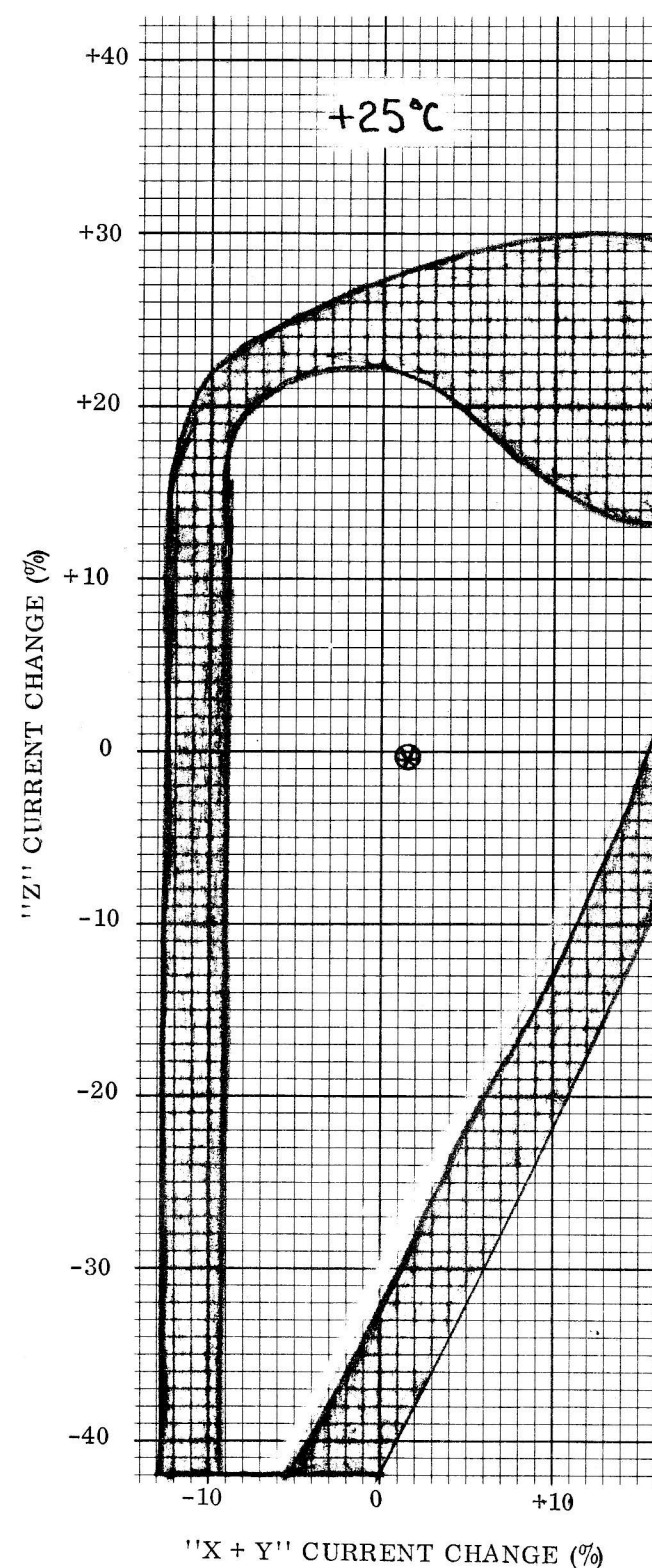
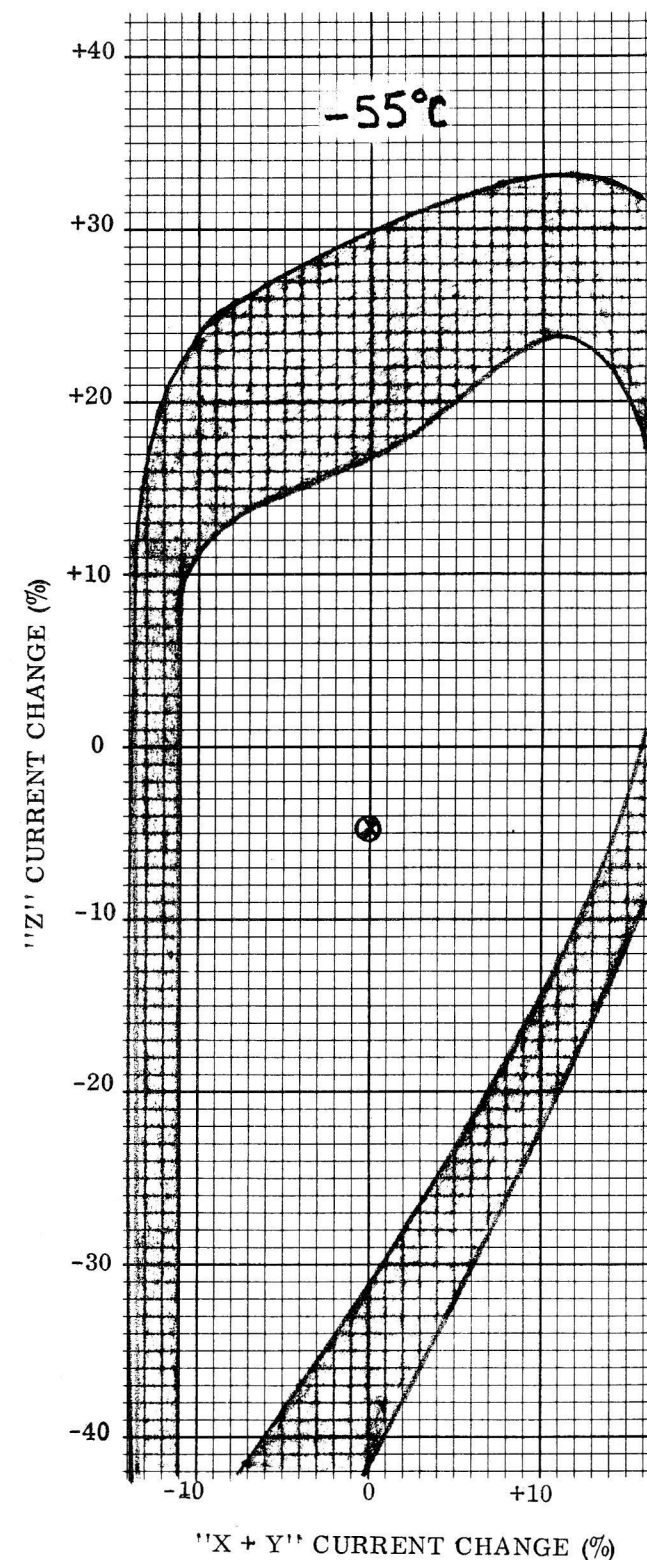
Referring to Figure 2-4, shmoo plots for 32 core mats at each of three temperatures;  $-55^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$  and  $+100^{\circ}\text{C}$ ; are shown together with an explanatory plot at the extreme right. As noted in the latter, the broad dark region defines the area within which the 32 plots at a particular temperature lie. The variability shown by the breadth of the dark region is due entirely to differences between mats, since the same sense amplifiers and drive selection system was used in each case. The variations are attributed to differences between cores and their distribution, differences in coupling between drive and sense lines due to imperfect balance of the sense line, etc. Obviously, memory performance cannot be predicted directly from the core characteristics, nor can it be predicted accurately from a shmoo plot of a single mat.

Shmoo plots are normally plotted using absolute current values. This is convenient when operation at a fixed temperature is intended, but when temperature compensation is employed to enable operation over a wide temperature range it is easier to evaluate the performance if the currents are normalized to the nominal value at each temperature. The several plots can then be overlayed to obtain a composite plot applicable to operation over the full temperature range. Considerable preliminary testing is required to establish a preliminary nominal drive current. If the mat used to establish the preliminary nominal currents is not typical of the stack as a whole, the optimum values will be offset from the "0,0" position, as shown by the  $\otimes$  marks. If the offsets are small, the plots can be overlaid with the  $\otimes$  marks aligned and the current axes shifted accordingly without significant error. If the offsets are large the scales should be adjusted accordingly, or the plots should be rerun with the revised nominals.

In Figure 2-5 the innermost boundaries of the plots shown in Figure 2-4 are shown superimposed with the adjusted nominals aligned with the 0,0 coordinates. This alignment implies perfect temperature compensation. The temperature compensation required to obtain the optimum drive currents is  $-0.24\%/^{\circ}\text{C}$  for the X + Y drive and  $-0.21\%/^{\circ}\text{C}$  for the Z drive between  $-55^{\circ}\text{C}$  and  $+25^{\circ}\text{C}$ ; and is  $-0.22\%/^{\circ}\text{C}$  and  $-0.19\%/^{\circ}\text{C}$ , respectively, between  $+25^{\circ}\text{C}$  and  $+100^{\circ}\text{C}$ . Any variation from these values can be accounted for by offsetting the corresponding plots. The square area enclosed by the composite plots defines all possible operating points that can result from independent variation of drive currents over a  $\pm 8\%$  range, assuming symmetrical drive (equal read and write currents) is guaranteed.

Since separate read and write drivers are provided in the Apollo memory, a further complication must be added to the shmoo plot to account for this independence. Since the read and write drivers use identical circuits and thus have equal tolerance limits, it is suggested that the most convenient way of obtaining the required shmoo plot is to employ equal values of read and write current at the nominal value of "X + Y" and vary them in the opposite senses for values of "X+Y" other than nominal. The largest square that can be placed in the resulting composite plot will enclose all possible operating points for simultaneous independent variation of all drivers. The square must be centered on the selected nominal operating point. If it is offset, a new composite plot with a revised nominal point must be made.





NORMAL CONDITIONS			
TEMP	-55°C □	+25°C ○	+100°C △
X+Y	810	670	548
Z	390	320	265

DISTURB RATIO = 0.50  
 PATTERN = WCP  
 STROBE TIME = 375 nsec @ 100°C  
                   350 " " 25°C  
                   325 " " -55°C

STROBE WIDTH = 80 nsec  
 "ONE" THRESHOLD = 25 mV  
 "ZERO" THRESHOLD = 12.5 mV

MANUFACTURE = Milw  
 SERIAL NO. = 001-008  
 DATE: 18 Mar. 1966

Figure 2-4. Shmoo Plots



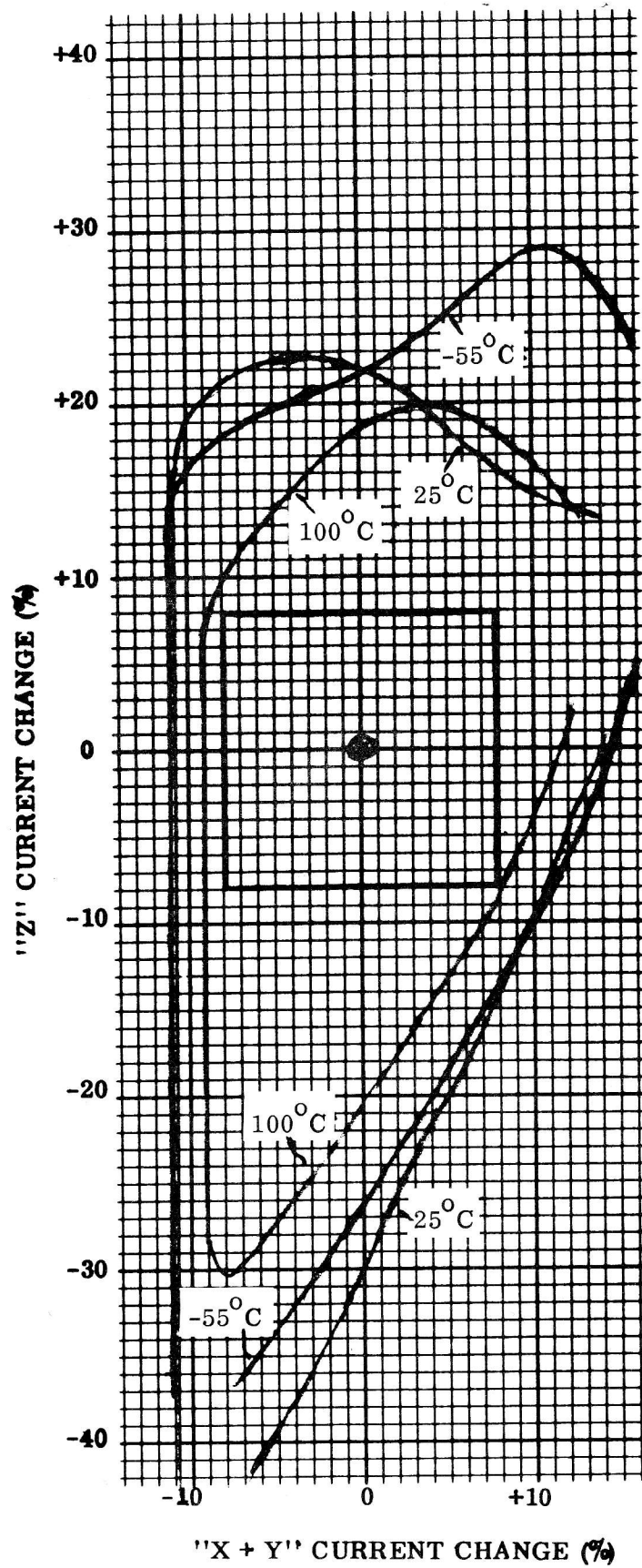


Figure 2-5. Composite Shmoo Plot for -55 to +100°C





Since the Apollo core stacks are obtained from two vendors, each supplying cores of their own manufacture, it is essential that composite shmoo plots of each such memory be overlaid with the specified nominal operating points in alignment. The maximum size square that can be enclosed by the innermost boundaries of the combined plots determines the tolerance limits of the driver circuits. The tolerance limits for the sense amplifier are generally determined first, since the shmoo area is directly related to the sense threshold limits. The illustrative shmoo plots of Figures 2-4 and 2-5 were obtained with a maximum ZERO threshold of 12 mv ( $V_Z > 12$  mv) and a minimum ONE threshold of 25 mv ( $V_1 > 25$  mv). The difference is greater than the initial sense amplifier threshold values,  $V_Z < 15$  mv and  $V_1 > 22$  mv, to provide for aging effects.

The initial sense amplifier thresholds for the Apollo sense amplifiers are presently specified as,  $V_Z < 18$  mv and  $V_1 > 34$  mv, per Raytheon internal memo BD:66:164. To allow for aging of the voltage sources that supply temperature compensated reference voltages to the sense amplifiers, a greater spread between the ONE and ZERO thresholds should be used when the shmoo plots are made. If  $\pm 3$  mv is allowed for drift, the limits become  $V_Z < 15$  mv and  $V_1 > 37$  mv. In making the shmoo plots these values may be used, or they may both be shifted up or down like amounts, as  $V_Z < 12$  mv and  $V_1 > 34$  mv.

The operating limits of the core stack, determined as described above, must exceed the tolerance limits of the drivers, including allowances for aging of components. Raytheon engineers are proposing tolerance limits for the driver module based on empirical measurements on production samples. The measurements made thus far on a single module indicate that the tightest tolerances that can be guaranteed are  $\pm 2.7\%$  @  $25^\circ\text{C}$ ,  $\pm 3.9\%$  @  $-10^\circ\text{C}$ , and  $\pm 4.5\%$  @  $+70^\circ\text{C}$ . These are initial values which allow for selection of a nominal resistor at  $25^\circ\text{C}$  plus a tolerance of  $\pm 5$  to  $10\%$  on the overall temperature coefficient, which is affected by variations in diode characteristics and cannot be compensated for. The diode characteristics can actually vary by more like  $\pm 25$  to  $30$  percent. The only way to guard against that much variation is to measure the temperature coefficient during the screen and burn-in process. Variations in duty cycle, from single step operation to continuous operation, result in a change in  $V_{BE}$  of the driver output transistor which results in an additional  $\pm 1$  percent tolerance on drive currents. The total initial tolerance is then  $\pm 3.7$  percent @  $25^\circ\text{C}$ ,  $\pm 4.9$  percent @  $-10^\circ\text{C}$ , and  $\pm 5.5$  percent @  $+70^\circ\text{C}$ .

There are many aging factors involved in determining the end-of-life tolerance limits for the current drivers. These are listed below.



1. Change in regulator diode drop due to $\pm 3.5\%$ change in current from prior stage . . . . .	$\pm 0.2\%$
2. Ageing of regulator diodes . . . . .	$\pm 0.5$
3. Ageing of output transistor $V_{BE}$ . . . . .	$\pm 0.5$
4. $\pm 20\%$ change in output transistor $H_{FE}$ . . . . .	$\pm 0.7$
5. Ageing of emitter variable resistor . . . . .	$\pm 0.5$
Total	$\pm 2.4\%$

It is highly improbable that all of the components contributing to the drift of the driver will drift the maximum amount in the same direction, however, there is no means of assuring what margin, if any, remains after the computer is assembled and has been subjected to environmental stress during checkout, acceptance test, and operational use. A marginal testing system which allows the X + Y and Z current driver outputs to be changed by fixed amounts, say  $\pm 2\%$ , while a memory test program is being run at the temperature extremes would provide a check on drifts from initial values. Marginal testing of the sense amplifier thresholds and strobe timing is also required for the same reasons.

On the basis of the evidence presently available it appears to be very unlikely that the erasable memory will meet the design objective of interchangeable modules which are tested at the module level only. It is also unlikely that the temperature compensation of the current drivers is optimum for both RCA and EMI core stacks. It is doubtful that satisfactory performance can be guaranteed without redesign of the current driver to obtain optimum temperature compensation. Considerable degradation of drive current tolerances occurs when writing and reading from memory are done at different temperatures, unless very close tracking of drive currents and core characteristics is provided.

It is customary to impose a common mode noise test on the vendor of magnetic core assemblies since the symmetry of the windings and the workmanship in general tend to influence the amount of common mode noise seen in the memory system. During testing of the magnetics assemblies at one of the vendors, the unused drive windings are presently grounded. This provides a great reduction in the common mode signal which is coupled to the sense winding, and largely tends to nullify the test results. The current waveforms permitted during the stack tests are not representative of those seen in the actual computer, and the test equipments used by the two vendors are quite different. These differences in the waveforms and the equipment make correlation of the test results very difficult. The procurement specification for the memory module should be rewritten to cover these objections.



### 2.5.3 Memory Circuits

#### 2.5.3.1 Driver Circuits (D)

The committee has not been shown a satisfactory analysis of the design of the X, Y, and Z driver circuits. Module test procedures assure a drive current uncertainty of no more than +4.5 percent. If the memory stack tests described above give favorable results, this tolerance may provide an adequate margin of safety.

The only undesirable characteristic of Erasable Driver Module, NASA Dwg. No. 2005004 (disregarding temperature compensation and drive current tolerance), is parallel operation of transistors Q6 and Q7 in the gate (CKT's No. 40017 and 40022). The combined current is about 600 ma, and these transistors are held out of saturation by a  $V_{CE(SAT)}$  drop ( $\cong .2$  volt). If one transistor hogged all of the current, the average dissipation would be  $.6 \times 1.2 \times .25 = .18$  watts. At  $60^{\circ}\text{C}/\text{watt}$ , the junction would be  $11^{\circ}\text{C}$  above the header temperature, which is a reasonable operating condition.

#### 2.5.3.2 Sensing System (B)

The sensing system consists of the input transformer, the sense amplifier, the reference power supply, and the strobe circuit. The common mode rejection capability of the input transformer and the sense amplifier have not been specified, and there is no common mode test as part of the sense amplifier module factory test plan. Common mode noise typically accounts for much of the difficulty experienced with larger coincident current memory systems. The fact that the Apollo memory is only 2048 words and uses staggered drives means that the common mode signals will be smaller than experienced in larger systems. However, common mode requirements should be reflected in the purchase specifications for both the input transformer and the sense amplifier, and a common mode test should be specified for the sense amplifier module in the factory test plan.

It is generally felt that the module tests do provide satisfactory assurance of the frequency response and gain of the sense amplifiers and the accuracy of the reference power supply, as well as the performance of the strobe circuit over the operating temperature range.

#### 2.5.3.3 Address Selection (A)

The design of the address selection circuits appears to be adequate. The 11 Maxwell core can sustain the required volt-microseconds during the read and write cycles. The transistors are provided with adequate base drive. No voltage ratings are exceeded.



## 2.6 FIXED MEMORY

The rope memory for the Block II computers has been completely redesigned from the Block I configuration. It is different mechanically and electrically. The entire computer structure has been redesigned to allow the ropes to be easily replaced from outside the computer. The electrical designs have been altered in order to improve the signal-to-noise ratio and other electrical properties of the fixed memory system.

### 2.6.1 Mechanical Design (D)

It is believed that to date no mechanical shock, vibration, or temperature shock tests have been run on the new rope module design. This appears to be a significant oversight, and these tests should be initiated immediately. It is recommended that a serious attempt be made to design a fully operating test for the rope modules. The cores themselves are subject to mechanical and thermal disturbance, and the test to qualify this new mechanical design should insure that the cores are not stressed.

Since the rope modules are intended to be replaced in the field, they are located outside the pressurized portion of the computer. The connectors into which these modules plug should be protected from the environment, both before and after the rope modules are installed. Before the modules are installed, a water-tight cover should be installed over these vacant connectors. This cover should include a gasket of the same type used to seal the rope module to the computer structure. In the case of the rope modules themselves, this gasket is not presently captive to either the computer structure or to the rope module. It is definitely feasible and highly desirable to captivate this gasket. Since these gaskets are subject to damage and wear, the captivation should be done in such a way that the gasket is easily removed from the rope for replacement.

### 2.6.2 Fixed Memory Circuits (D)

The same general comments made about the erasable memory driver also apply to the core rope drivers, since the same general circuit configuration is utilized. Furthermore, the drive current amplitudes are considerably less critical in the case of the rope and the temperature compensation is practically not required.

The rope memory is a notoriously noisy system. The timing of the Block II memory was changed significantly from the system used in Block I in order to avoid some of the noise problems. The memory is read at "reset" time rather than at inhibit time, and a parity inhibit winding has been added which guarantees better saturation of the unselected cores. The timing of the strobe signal has recently been delayed. This appears to sample the rope sense signals when there is less noise present, and improves the overall performance of the system. Since the output of the rope is a much larger voltage than the output of the erasable memory cores, the sense amplifier



thresholds for the ropes could be increased. This proposal has been made by Raytheon and accepted by MIT, but has not yet been accepted by NASA. This appears to be a worthwhile change and will improve the operation of the system.

If the proposed change to the sense amplifier is approved the nominal threshold,  $V_T$  will be 35 mv. Applying the tolerances arrived at for the erasable memory sense amplifiers, the initial limits will be  $V_Z < 28$  mv and  $V_1 > 44$  mv. To allow for component drift the spread should be increased  $\pm 3$  mv, i.e.,  $V_Z < 25$  mv and  $V_1 > 47$  mv. The test limits for the rope module are  $V_Z < 25$  mv and  $V_1 > 45$  mv. The limits are therefore not quite adequate to guarantee safe operation. Furthermore, the module is tested at  $-10^\circ\text{C}$  and  $+70^\circ\text{C}$ , but the drive currents are not varied; hence these limits are meaningless since they result from different drive currents than those which will actually be generated at the temperature extremes by the AGC current drivers. Appropriate tolerances for the drive currents are discussed in Paragraph 2.5.2.

Assuming that the adequacy of the ONE and ZERO outputs of a rope module can be determined by electrical tests performed on the completed module, the tests made on the cores prior to wiring are insufficient to guarantee that the ZERO output will be below the specified limit. In the absence of such testing, there is some danger that a completed module will be unacceptable due to high ZERO outputs. The module will then have to be discarded and a replacement made, with no assurance that the replacement will be any better. The ZERO level is determined by the degree of balance of the shuttle voltages of the + and - groups of cores threaded by a sense winding. In the worst case there are 64 cores in each group, thus a few millivolts difference in shuttle voltage of each pair of cores can result in a significant ZERO output. The specification on the core limits the maximum shuttle voltage to 15 mv with a drive current rise time of 1 amp/ $\mu\text{sec}$ . It is assumed that with a risetime of 0.4 amp/ $\mu\text{sec}$ , as the core sees in use in the computer memory, the maximum shuttle voltage would be 6 mv. It is suggested that a minimum value of 5 mv should be specified to limit the net shuttle of 64 pairs of cores to 60 mv, which is about 20 percent of the ONE output. If necessary, the cores can be graded to control the shuttle voltage difference within groups of 128 cores used in a particular rope module. The effect of strand select currents on the shuttle voltage can also be incorporated in the core test at the same time.

The arguments presented in Paragraph 5.2.1 with regard to marginal testing of the erasable memory when in the assembled computer are equally applicable to the rope. In the assembled computer common mode signals are coupled into the sense lines of all modules, whether selected or not, and can influence the sense amplifier inputs by feeding through the capacity of the reverse-biased strand and module select diodes. This potential noise source is absent when modules are tested individually. The ONE and ZERO signal levels are also functions of the drive current amplitudes and rise times, which vary from one driver module to the next. Strobe timing is a function of logic circuit delays which vary from one computer to the next. Thus, tests made at



the module level provide no assurance that adequate margins exist in the assembled computer. A rope module may be installed in a flight computer and flown without any tests to assure adequacy of that specific combination of driver circuits, sense amplifiers, and rope components. Marginal testing of drive currents, strobe timing, and sense thresholds could reveal an unsafe combination and prevent its use in a flight computer.

The Strand Select Module, NASA Dwg. No. 2005009-A, shows three current drivers, including transistors Q11, Q13, and Q15, which supply 128 ma at 25°C to the selected strands. This current is temperature-compensated by virtue of the three series diodes in the base circuit, in the same manner as memory drive currents are compensated. The purpose in temperature-compensating this current is apparently to balance out the change in ac resistance of the selection diodes in the rope modules with temperature. If not compensated for, this change in ac resistance will vary the attenuation of the sense signals and lower the S/N ratio of the sensing system. The adequacy of the temperature compensation cannot be determined without further information on the selection diode characteristics and information regarding the maximum difference in temperature between the selection diodes in the rope module and the regulating diodes in the Strand Select Module. It should be noted that the rope module test (per FTP No. 186305) is performed with a constant strand select current. The observed signal amplitudes consequently do not accurately represent those seen by the sense amplifier in an operating computer at other than 25°C.

## 2.7 OSCILLATOR (B)

The oscillator is critical to the operation of the computer and provides a necessary time reference to the other spacecraft subsystems. There is no formal oscillator performance specification approved by NASA. The circuit designer has interpreted the overall accuracy requirements according to his own judgment, and has allocated tolerances due to ageing, temperature, supply voltage stability, and cabin pressure. Whether these allocations are reasonable or not cannot be judged at this time, except it appears to be possible to manufacture oscillators which meet these budgeted accuracies. This does not eliminate the need for a formal document, especially since the stability requirements arise from areas outside of the computer.

The basic design of the oscillator circuit is very good. It is possible, however, that the oscillator is overdesigned. There are several unqualified and single source parts in the oscillator which could perhaps be removed if the accuracy and drift requirements were relaxed slightly. The oscillator piece parts which have failed qualification testing are discussed in Section IV.





## 2.8 ALARM CIRCUITS (A)

The alarm module contains seven separate circuits; six of which indicate out-of-tolerance or failure conditions in the computer and one which provides +5 VDC as a reference voltage to several of the other circuits.

The circuits used for tolerance or failure sensing are:

1. Voltage Alarm - senses high or low out-of-tolerance condition on 4 and 14 volt, and low out-of-tolerance condition on 28 volt common.
2. Oscillator Alarm - senses the loss of the 1.024 mc oscillator signal.
3. Scalar Alarm - senses the loss of the output of stage 17 (1.28 sec period) of the scalar.
4. MYCLMP - generates memory logic clamping signal when 4 VDC is 2 VDC or lower, and 14V is still on.
5. Warning Integrator - repeated restart signals (six consecutive) are integrated to set an alarm.
6. Double Frequency Scalar Alarm - senses the doubling of the 100 pps output of the scalar.

In the following discussions, reference is made to schematic drawing number 2005029. The circuits will perform as required with no overstressing of components. The matching of the differential amplifiers over the temperature range is more than sufficient. The power for the reference supply and for circuit operation will hold up long enough to give the failure signal, using as a reference the photographs of the turn off transients that were obtained from actual tests on an operating computer.

### 2.8.1 Voltage Alarm

The voltage alarm circuit contains five differential amplifier circuits which detect out-of-tolerance supply voltages measured with respect to internally generated references, derived from 28 V common. The trigger points for the 4 V alarms are approximately 3.6 and 4.5 volts, for the 14V alarms approximately 12.5 and 16 volts, and for the 28 V alarm approximately 21.5 volts.

### 2.8.2 Oscillator Alarm

The oscillator alarm circuit detects the presence or absence of the 1.024 mc oscillator frequency and, in addition, the presence of the 14 V SW through a long time constant. This time constant provides the turn-on delay to allow for stabilization of the oscillator.



Transistor Q11, when the clock is in operation, is continually pulsed to discharge the capacitor-resistor combination on the base of Q12. If this discharging disappears, Q12 starts to conduct, discharging C7 and cutting off Q14 and Q15 which set the alarm. Q13 operates with Q14 and Q15 to provide a sharper cut-off knee.

This circuit does not attempt to determine an out-of-tolerance condition on the oscillator, but merely the gross presence or absence of oscillator pulses. For this intended usage, the circuit design is adequate; there are no overstressed nor under-specified components. However, as Q14 approaches turn-on, the circuit is evidently sensitive to noise; therefore, a circuit change is in process to change the output to a bistable circuit with hysteresis. This new circuit has not been evaluated.

### 2.8.3 Scalar Alarm

The scalar alarm senses the presence or absence of the 1.28 pps signal from stage 17 of the scalar. In normal operation, Q19 and Q20, in combination, keep C19 and C13 discharged below the approximately 6 volt threshold of Q22. The circuit appears to be adequate for the purpose with no components overstressed.

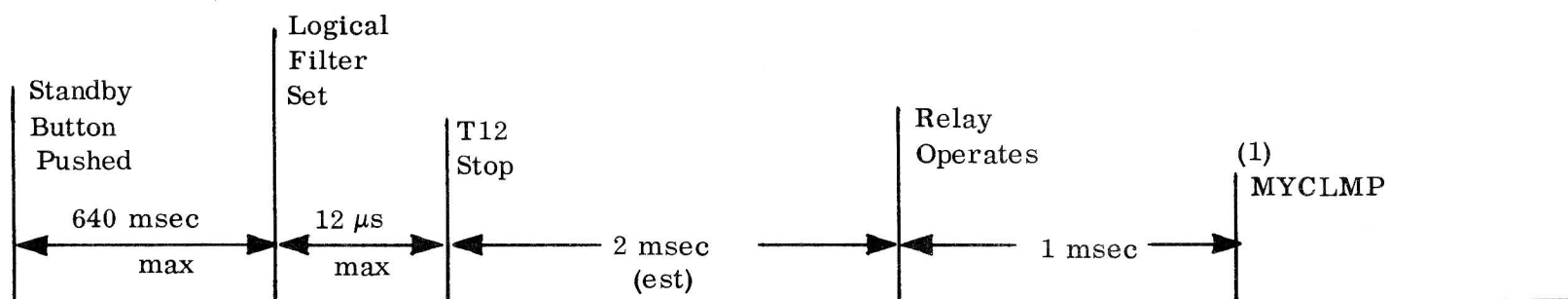
### 2.8.4 MYCLMP Circuit

The MYCLMP alarm circuit is intended to protect the erasable memory in the event that the +4 volts fails while the 14 volts is still on. This protection is desirable in that the erasable memory can be disturbed if the micrologic controlling it behaves erratically. The MYCLMP circuit is a very simple differential amplifier comparing 4 V SW to a 2 volt reference derived from the 5V power supply in the alarm module. The circuit per se is adequate for its intended use; however, the selected voltage threshold is questionable. This circuit drives two NOR gates which are the last gating point in the generation of the SETEK and INHIBIT signals. A latest change that is in process inserts the MYCLMP signal in the STRT 2 point in the logic circuits. This removes the clamping action further from the memory and would seem to be a marginal change.

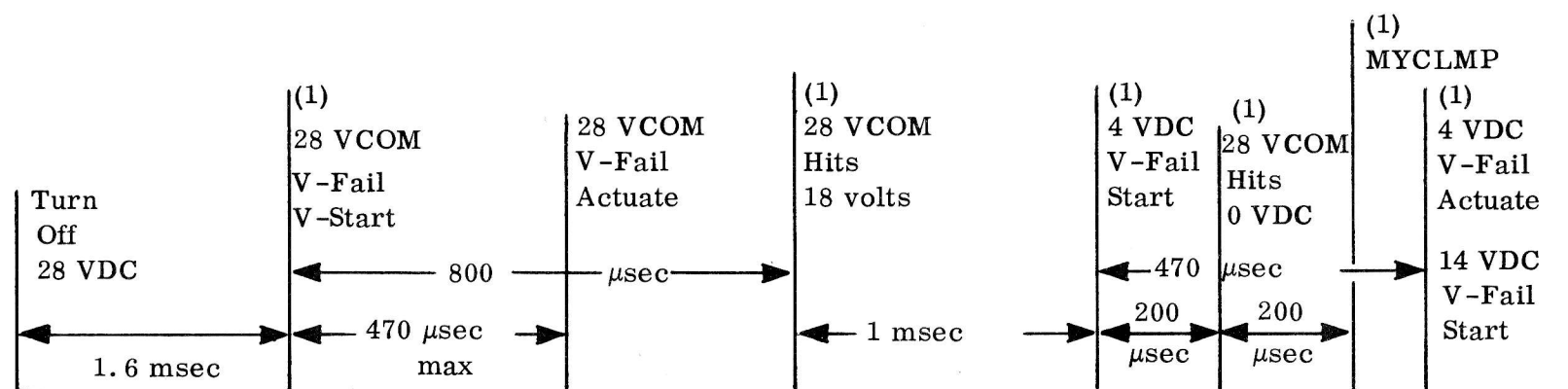
The alarm sequence and operation during standby and turn-off has been estimated, by examining the logic drawings and photos of waveforms of an operating power supply, to be as shown in Figure 2-6.

The standby condition is generated by pressing the STBY button. The button must be depressed for a period of 640 msec to actuate the circuitry. At the end of that period a T12 stop is initiated, taking a maximum of 12  $\mu$ sec, and the standby relay is actuated. Assuming the action time of the relay is 2 msec, which is reasonable for this size of relay, the T12 stop will have occurred long before the relay opens the 4 and 14V switched leads. Approximately 1000  $\mu$ sec later MYCLMP would be initiated.





STANDBY SEQUENCE



TURN OFF SEQUENCE

Note (1): From P.S. Photos

Figure 2-6. Standby and Turnoff Sequences



Since the T12 stop completely paralyzes the computer, there does not seem to be any real problem unless "out of control" logic generates false read or write signals. MYCLMP appears to be rather ineffectual in preventing this due to its 2V actuation level and its latest mechanization where its signal goes to STRT 2.

The turnoff sequence is on the lower line of Figure 2-6. When the 28 volt source is turned off, the 28V common starts to decrease hitting the V-fail condition in approximately 1.6 msec. 470  $\mu$ sec later, maximum, the V-fail is generated, which in turn generates a T12 stop. Approximately 300  $\mu$ sec beyond this point 28V common reaches 18V and the power supply goes out of regulation. At this point the 4 and 14 volt power starts to decrease, the 4V reaching its fail condition approximately 1 msec later. MYCLMP occurs before the 4 or 14V V-fail signal is generated, since there is no R-C or logical delay in the MYCLMP circuit. The MYCLMP would fulfill its intended role if its actuation threshold were raised to 3.0 volts, a level at which the micrologic is guaranteed still to have logical control of the memory.

#### 2.8.5 Warning Integrator

The warning integrator receives the several restart signals which are generated by other alarms. These signals are 1.125 msec long and have a minimum interval of 160 msec. Six successive pulses are sufficient to trigger the circuit, other combinations of pulses and no pulses over a longer interval will also do so, since the circuit is a simple integrator. Q29 acts as a current source which is gated into C12 for charge storage. The voltage on C12 is compared in a differential amplifier with a reference derived from 5 VDC. When the threshold is exceeded and the alarm is generated, Q23 forms a feedback path for hysteresis holding the alarm on.

Before a recent change was initiated the base of Q29 was essentially open, when Q28 was off. The  $BI_{CO}$  on Q29 was sufficient at high temperatures to partially charge C12 and create either false alarms or at least marginal operation. The addition of a 10k resistor across diodes CR9 and CR10 has corrected this situation. Other than this, the circuit design is adequate.

#### 2.8.6 Double Frequency Scalar Alarm

This circuit is designed to detect a doubling of the 100 pps signal from the scalar. The circuit is a single shot with a time constant of 3.7 msec. The output is compared externally in a NOR gate with the input. The changing of the state of the 100 pps before the change of state of the single shot constitutes a failure. The frequency at which a failure occurs is approximately 135 cps.

The design and tolerance of the circuit are adequate with no overstressing of components.



### 2.8.7 5VDC Source

This circuit provides 5VDC for use as a reference and also to power some circuits. Two nominal resistors are used to compensate for the tolerances of the Zener and the diode which control the shunt regulator. No problems should be experienced in this circuit.

## 2.9 COMPUTER INTERFACE

The computer interfaces with the remainder of the guidance and navigation system and the other spacecraft systems are accomplished through a set of standard circuits. A detailed analysis of each of these circuits is contained in Appendix F. The results of that analysis are summarized here.

The nature of the signals and the interface cabling are presumably specified in the interface control documents. These documents are, in many cases, contradictory or wrong. The method of updating the documents is difficult to control and makes it almost impossible to tell whether one is in possession of an up-to-date document or not. Certain schematics which are included in these control documents are either not complete enough to define the circuit adequately or are "for reference only". The circuit designs which have been reviewed are those which are included in the computer and the design adequacy has generally been judged on the basis of good practice.

### 2.9.1 Signal Distribution and Grounding (D)

During the course of the design review, attempts were made to document the grounding system used for the computer in the command module and LEM installations and to discover the philosophy which supported it. This has not been entirely possible because the interrelation to the spacecraft wiring did not seem to be known outside of the G and N system. Certainly, consideration was given to the computer grounding, as evidenced by the treatment of the chassis and shield returns, but it seems to have been on a piece meal basis. It would be desirable to review a complete grounding and shielding diagram for the two spacecraft looking outward from the computer, and to feed back the results of any spacecraft level noise tests into the computer testing to guarantee that noise margins are adequate.

The committee was told that the LEM radar signal cable is 40 feet in length, has a characteristic impedance of 60 ohms, sees a source impedance of 510 ohms, and a load impedance of 200 ohms. Regarded as a transmission line, it is badly mismatched. Further study is needed before it can be determined if this will cause any trouble.



### 2.9.2 The "A" Circuit (C)

The "A" circuit provides for conversion of the rotational hand-controller signals into digital form. This circuit converts the 800-cycle amplitude-modulated analog signal into a pulse-width modulated signal which can be subsequently digitized by counting its time duration. The design goals for this circuit are not met at the temperature extremes. The threshold voltage and the circuit scale factor are both functions of temperature. Since these circuits are used in a manual control system, an investigation should be made to see if both the offset and the linearity specifications could be relaxed rather than add further complication to the circuit.

The synchronizing input (pin A of schematic) overloads the NOR gate driving it to the point where one of the three circuits tied to this point may not function reliably.

### 2.9.3 The "C" Circuit (A)

The procurement specification for the transistor used in this circuit has recently been revised and this circuit is now deemed to be adequate.

### 2.9.4 The "XT" Circuit (B)

This circuit provides ground isolated outputs from the computer and is used to supply a variety of loads. Although the signal amplitude and rise time vary with temperature, these variations are not expected to be troublesome. The interface control documents seem to be inadequate where they refer to this circuit. The circuit is tested with a 500 ohm load and its output is specified with that load. The actual load varies from 500 to 51 ohms, and is paralleled by an unknown cable capacitance, and therefore the actual output will be different from the value as tested. It is therefore recommended that the interface control documents be revised to show the true circuit conditions, and that the transformer and the XT circuit be tested in those conditions.



### III DISPLAY AND KEYBOARD (DSKY)

The DSKY contains the electroluminescent panels, their power supply, some incandescent lamps, electronic circuits to run both the electroluminescent indicators and the incandescent indicators, and a keyboard. There are two DSKYs in the command module and one in the LEM, and their principal function is to provide communication between the G&N system (via the AGC) and the astronauts.

#### 3.1 MECHANICAL DESIGN (A)

The DSKY is a dry-nitrogen-filled unit of two piece box-type structure in which all wiring interconnections from front to rear are contained. In order to provide accessibility to this wiring, connections from front to rear are made through an innerconnector. Six interchangeable Indicator Driver Modules and a power supply contain the majority of electrical components and are plugged into connectors mounted on the rear portion of the structure. A rear cover is then placed over those modules to keep them enclosed in the nitrogen atmosphere. The rear structure also contains the AGC connector and a pressurizing fill valve.

Pluggable indicator and alarm lights are mounted to the front, or display, portion of the unit which also contains 19 push-button switches with pluggable panelescent lamps. The electrical components for this keyboard are housed in a module and mounted inside the unit. Finally, a front cover of egg-crate construction, to prevent unintentional activation of the switches, is placed over the units which are mounted to the front structure.

A brief description of the basic components, some of the considerations taken during design, and existing problem areas follow.

##### 3.1.1 Indicator Driver Module (IDM), Power Supply Module (PSM), and Keyboard Module

Material:	Magnesium. Lightweight; and located in the humidity-free, dry-nitrogen atmosphere.
Finish:	Dow 17, dark anodize.
Connector:	Protected male Malco pins aligned and keyed by use of guide pins.
Location:	<u>IDM and PSM</u> pluggable to rear portion of unit after removal at rear cover. <u>Keyboard Module</u> pluggable and located inside wiring area because of its related functions.



Problem Areas: Malco pin alignment in all modules. No known solution other than extreme care in pin installation and unit handling. Failure of relays in IDM under vibration. Vendors have been informed and problem is under investigation. See Section IV.

### 3.1.2 Digital Indicator Light (Electroluminescent)

The basic lamp is of glass-to-metal hermetic seal construction mounted in an encapsulated pluggable housing. Earlier prototype models were sealed using plastic materials but failed during humidity testing. Glass-to-metal sealed lamps have been received and evaluation testing has begun.

### 3.1.3 Indicator Alarm Light (Incandescent)

The new incandescent lights are molded into acrylic plastic and mounted to an encapsulated, pressure-tight, pluggable header. Units for evaluation are expected 3 May 1966.

### 3.1.4 Push-button Switches

The switches are illuminated by panelescent lights and mounted pressure tight against front structure. The basic switch is encapsulated and mounted outside the pressurized area with wiring to the inside accomplished through glass-to-metal sealed discs. The panelescent light is encapsulated using a Maraglass compound. Maraglass cracking and panel delamination problems have occurred in this area and design and assembly procedure investigations are under way.

### 3.1.5 Structure

The main structure is made of aluminum. The rear cover design incorporates structural ribbing inside the pressure area, and this design allows for a larger volume of nitrogen to be inserted into the unit. The rear structure, or wire wrap plate, receives a portion of its structural stiffness from the innerconnector. This method has also been followed in the design of the front housing.

Pressure sealing has been obtained by using Parker seal between the main structural components of the unit. Components external to the unit are mounted using Butyl "O" rings. Leak rates, better than required by specification, have been held on various units. However, some leakage problems have developed due to dirt in the seal grooves. Steps have been taken to prevent this in the future. Another area of leakage has recently developed. A washer-type seal, located under the screw used to purge the unit, has shown signs of wear during excessive purging. This problem has been submitted to the design and product support sections and an investigation is being conducted.





### 3.1.6 Environmental Testing

A mechanical model of the Block II DSKY was used to perform structural tests using levels as specified in Figures 3-1, 3-2, and 3-3. This model is equipped with 18 of the 19 required Indicating Push-button Switches. Five of these push-button switches were instrumented so the current and microswitch continuity could be monitored during the tests. This model performed successfully when vibrated to the latest qualification LEM and Command Module design limit schedules. During the qualification overstress vibration tests in the command module X-axis (direction of actuation of the indicating push buttons), the number 8 normally-closed contact opened for a period greater than 75 microseconds during the 13th minute of the 21-minute duration LEM lunar ascent and descent vibration schedule. The push button remained in the normally-closed condition for the remaining 8 minutes. This test was repeated in the same axis and no open contact occurred for the entire 21-minute vibration schedule. The vibration qualification overstress tests were successfully performed to the LEM and Command Module schedules in all the other axes.

The mechanical model was vibrated for a total schedule period of 5 hours 21 minutes and approximately 2 hours setup time. It is concluded that the Block II-DSKY is dynamically sound.

A harmonic vibration survey indicates that the IDM modules have an amplification of approximately 13, and the switch housing plate has an amplification of approximately 6. These are acceptable levels.

Flight shock, lunar landing shock and acceleration tests as specified in ND1002037, Rev. B, were also successfully performed utilizing the same engineering model. The earth landing shock was also successfully performed with the minor exception that one translucent "ENTER" cap fell off. This failure was investigated and determined to be a workmanship problem rather than a design deficiency.

Aerostatically, the DSKY model was tested successfully at 23 psig (proof pressure). Gas leakage tests were also performed successfully.

An engineering model (200B) is undergoing tests similar to those for qualification. Thus far the Design Limit vibration tests appear satisfactory (except failures noted in IDM relays). In addition, acceleration and shock tests appear satisfactory.

In conclusion, it is believed that the structure of the Block II DSKY will successfully meet the qualification structural requirements.

### 3.2 THERMAL (A)

The total power dissipation for the Block II-DSKY is 13.4 watts and is based upon a nominal input voltage of 25 volts. The component power dissipations are listed in Table 3-1.

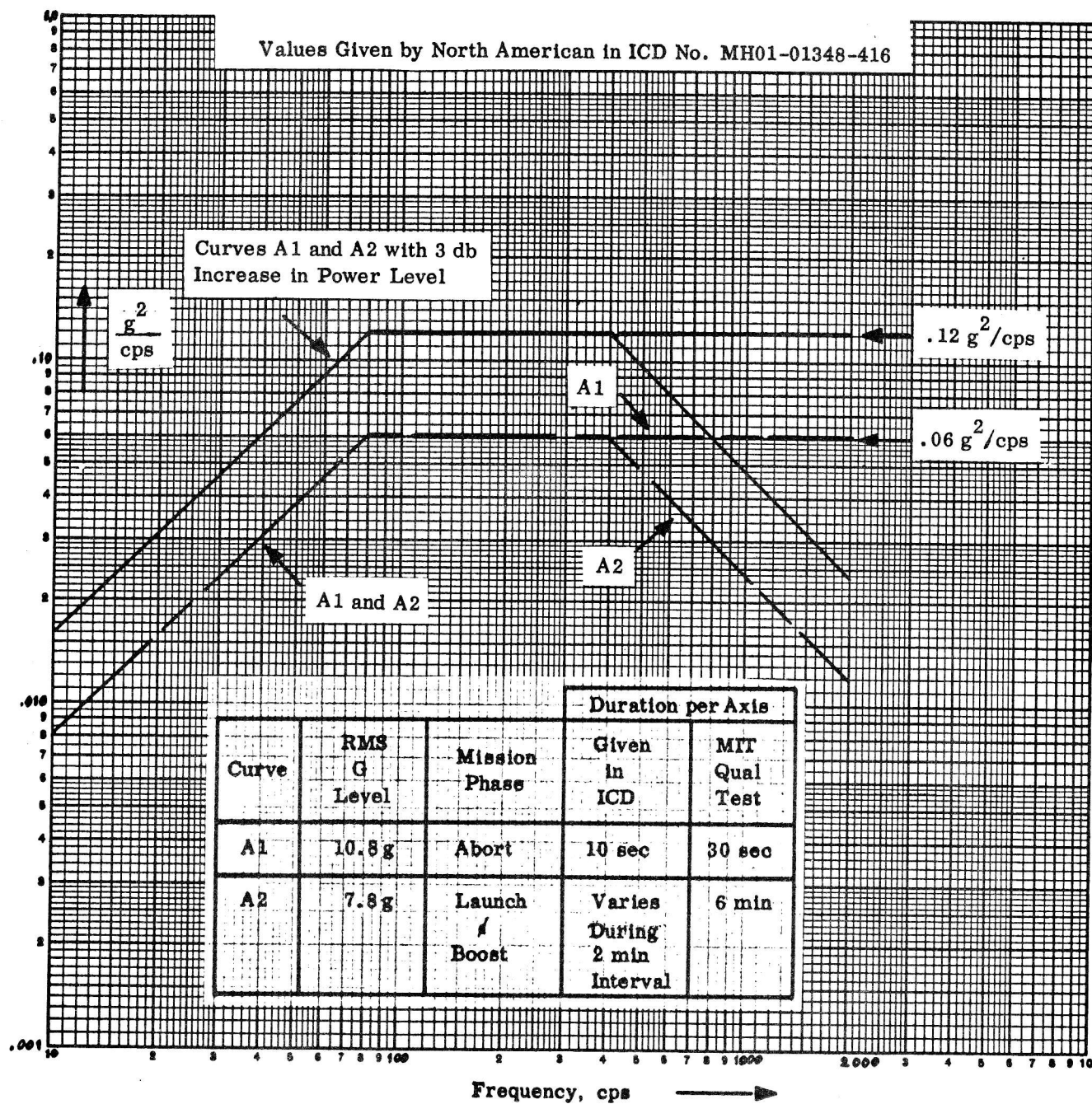


Figure 3-1. Command Module Vibration Specs

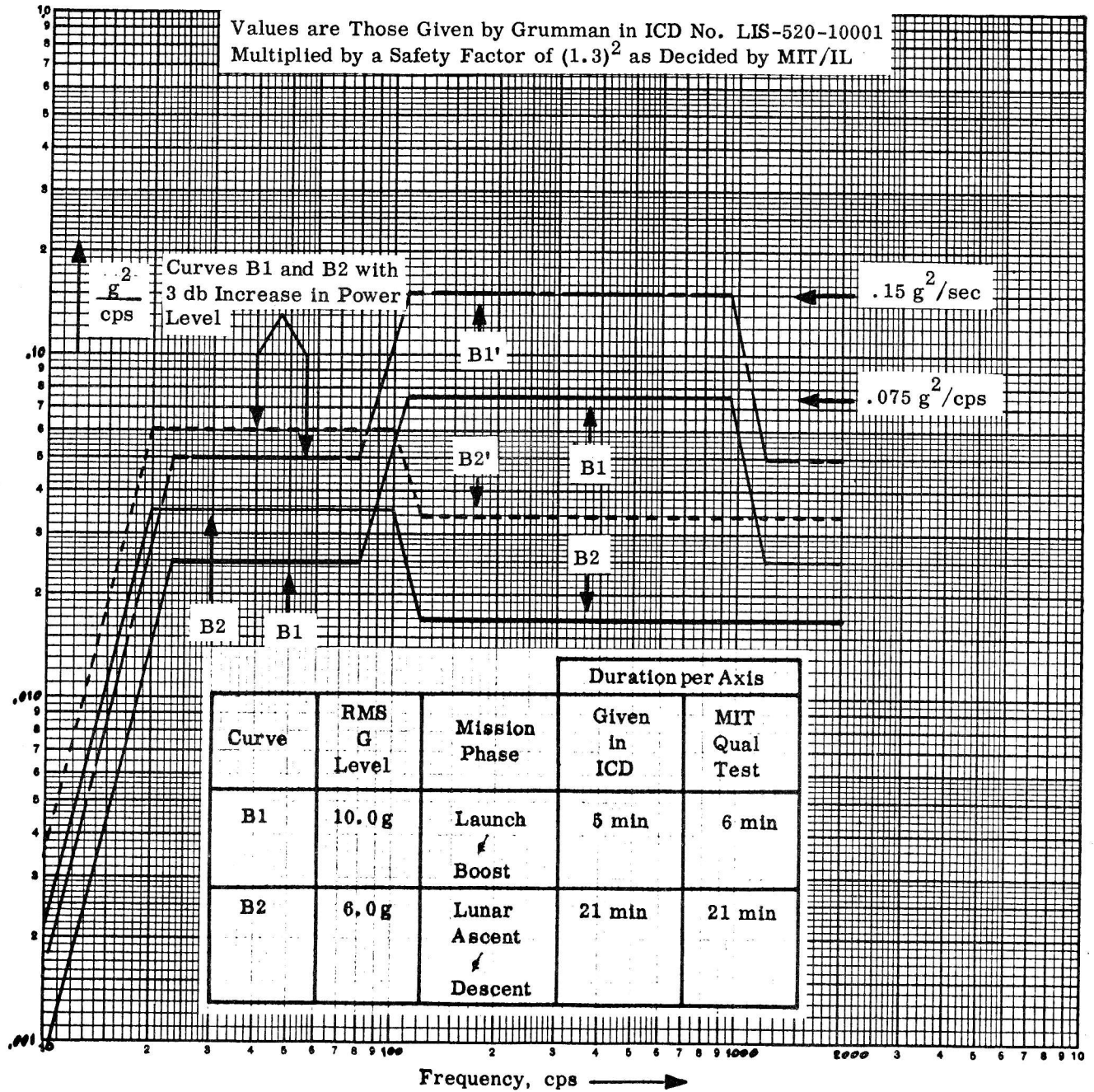


Figure 3-2. Lunar Excursion Module Vibration Specs



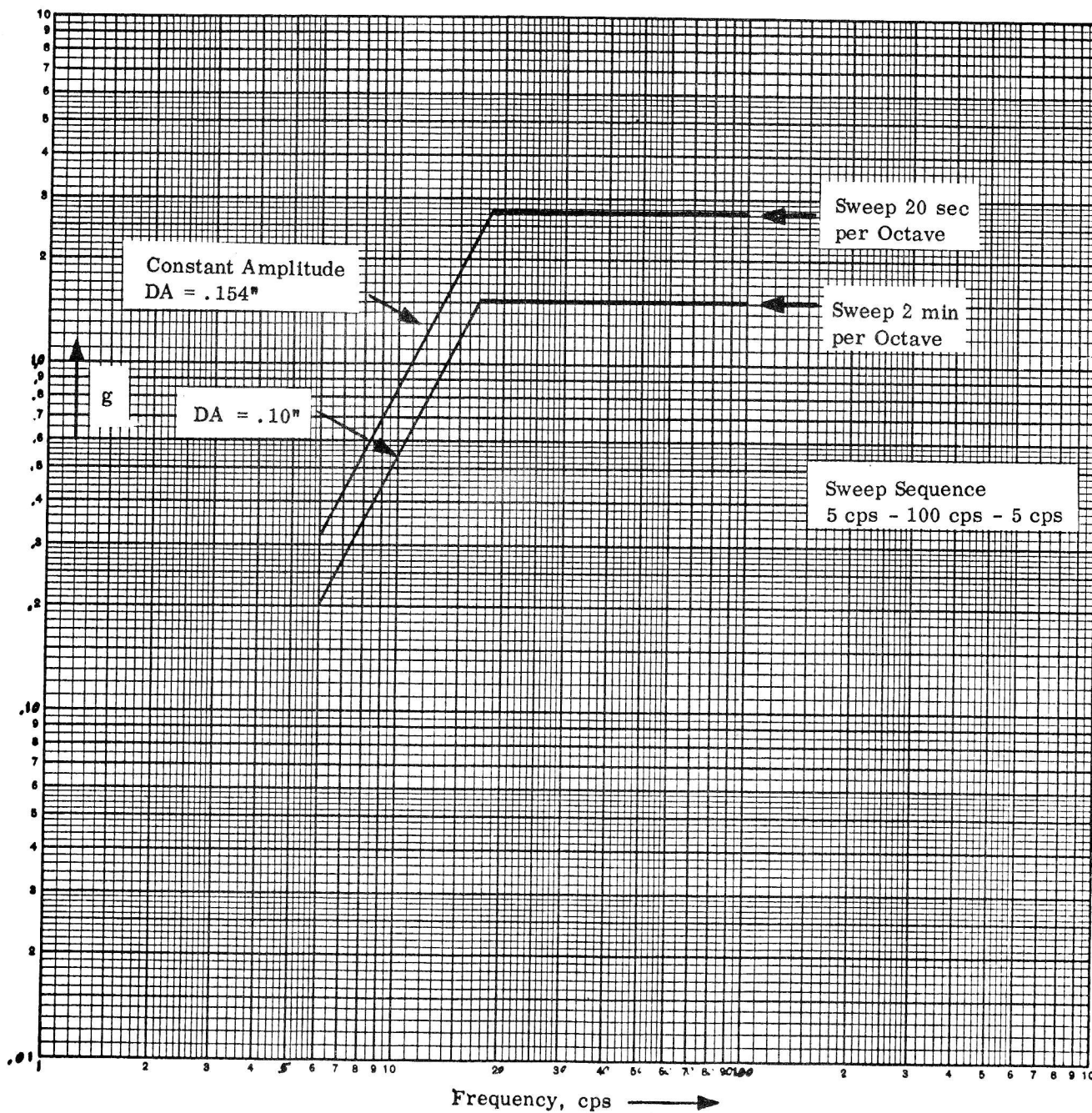


Figure 3-3. LEM and Command Module Sinusoidal Sweep



COMPONENT	POWER DISSIPATION (watts)
Indicator Driver Modules (6)*	6.50
Power Supply Module	1.35
Keyboard Module	1.00
Digital Indicator	1.50
Alarm Indicator**	3.04
Push-button Indicators	negligible

\* Maximum power dissipated by any two IDM's is 6.23 watts.

\*\* Based upon a worst condition of 1.5 yellow and 1.5 white lights operating at one time.

Table 3-1. DSKY Power Dissipation

The DSKY is required to operate for 24 hours when attached to and viewed by a shroud at 160°F (infrared emittance of shroud = 0.80) and a pressure of  $1 \times 10^{-6}$  torr to  $1 \times 10^{-7}$  torr (Apollo G&N Qualification Specification ND1002037). For this thermodynamic environment, the above component power dissipations, and electronic part power dissipations, the maximum temperature of each type of electronic part in each electronic component is summarized in Table 3-2. It is noted that the semiconductor devices operate at junction temperatures less than 221°F, a thermal design criterion established by MIT/IL Reliability. No comment can be made at this time pertaining to the thermal reliability of the remaining electronic parts pending the receipt of reliability stress sheets for these parts.

The foregoing thermal design verification was obtained at the subsystem level utilizing a thermal model with simulated component power dissipations. The results of the test are contained in Raytheon Report FR-65-482 entitled, "Apollo Guidance Computer, Display Keyboard, Block II Thermal Model Test."

Further thermal design verification will be obtained with Engineering Model No. 200B which contains an Indicator Driver Module instrumented with thermocouples. The tests to be performed are contained in Raytheon Test Plan 200-1.

### 3.3 INDICATOR DRIVER MODULES (C)

The indicator driver modules contain the magnetic latching relays, the nonlatching relays, and the circuits used to operate these relays. The circuit which contains the latching relay has been analyzed and is inadequate. At the expected operating



MODULE	CRITICAL COMPONENT	POWER DISSIPATION (watts)	CASE TEMPERATURE (°F)	JUNCTION TEMPERATURE (°F)
Power Supply	CR4 1006751	0.050	180.0	207.0
	L2 1006325	0.700	179.7	
	Q2, Q3 1010269-2	1.300 ea	192.7	197.9
	R3, R4 1006760	0.200 ea	196.0	
	T1 1010291	0.0042	180.5	
Keyboard	CR1-CR43 1006751	0.005 ea	165.3	168.0
	R1-R6 1006750	0.010 ea	165.2	
Indicator Driver	C(TYP)	0+	167.8	
	CR1-CR40 1006751	0.0024 ea	195.4	196.5
	K22 1010784-9	0.895	213.9	
	L1, L2 1010406-7	0.0320 ea	168.6	
	Q5 2004004-001	0.029	168.8	171.4
	R3 1006750-56	0.060	175.0	

Table 3-2. Block II-AGC (DSKY) Component Temperatures





temperature of  $90^{\circ}\text{C}$  and with the minimum specified computer input voltage of 23.5 volts, the latching relays cannot be guaranteed to work. Appendix G provides a detailed analysis of the relay circuit. It appears that the only satisfactory fix for this circuit is to replace the present relay with one whose design is optimized to work in the circuit. There is little else that can be done to improve the operation of the present circuit, unless it would be possible to guarantee a power bus minimum input voltage greater than 25 volts. That is considered to be unreasonable.

The circuits which drive the nonlatching relays have not been analyzed and, therefore, their design rating is indeterminate. An immediate review of the nonlatching relay circuit is planned, since they play a critical function in the operation of the Block II system.

All evidence points to the fact that the specification control drawings for the semiconductors utilized in the indicator driver modules were generated before the supply voltage was determined. Good reliability practice dictates that these devices should have approximately twice the voltage rating of any voltage they will encounter in the operation of the circuit. Since the DSKY has a maximum supply voltage of 25.5 volts, the diodes and transistors should be rated to at least 50 volts. At the present time the transistor is rated at 35 volts and the diodes at 30 volts. Analysis of the indicator driver circuitry indicates that the transistor carries currents in excess of 200 milliamperes and has a junction temperature near  $100^{\circ}\text{C}$ . This combination of high internal temperature and low voltage rating adds up to an unreliable application of these semiconductors.

The manufacturer of the relays in the indicator driver modules will guarantee reliable operation only up to 2,000,000 relay closures. System requirements documents state that the DSKY shall have a 2,000-hour useful life. There is a possibility that 2,000,000 operations of certain of the relays can occur before the 2,000-hour point. It is recommended, therefore, that a definite program be instigated for replacement of the indicator driver modules.

### 3.4 POWER SUPPLY MODULE (B)

The electroluminescent panels of the DSKY require a 250-volt, 800-cycle power supply. This power supply is basically a power amplifier which takes the 800 cycles from the computer scalar, filters it, and provides it to the electroluminescent panels. The output of this power supply is not referenced to ground but is allowed to float. Good practice and consideration of personnel safety generally require that power supply outputs be referenced to ground. Some minor problems were discovered in the older DSKYs which prevented one side of the 800-cycle power supply being grounded. However, there is no reason to believe that the center point of the output cannot be grounded.



During the review of the power supply, it was pointed out that the output voltage varied as a function of temperature. A recent design modification has overcome this difficulty and that portion of the circuit is considered to be adequate.

### 3.5 ELECTROLUMINESCENT PANELS (D)

The entire Apollo spacecraft makes use of electroluminescent panels for display purposes because of their inherently low power consumption. However, there are some basic problems associated with the use of these devices. They have a known wear-out mechanism. The light decreases in intensity at a given excitation level, and it has been estimated that it will decrease to approximately 40 percent of its initial brightness in about 1,000 hours. Although this is not a catastrophic failure mechanism, the brightness may fall below a comfortable level even though a brightness control is provided for the DSKY. The particular electroluminescent panels used in the DSKY are new and therefore long-term information is not available on them. Someone (MIT, Raytheon, or the vendor) should start a life test program for these panels immediately. Until complete confidence in our knowledge of the life factors for this panel is established, it is recommended that all electroluminescent panels be replaced every 1,000 hours.

These panels are difficult to procure and have not yet passed their qualification tests; in particular, the water immersion portion of the test. Previous panels used a silicone plastic to seal the panel, and this has proved to be unsatisfactory. A newer design contemplated for use in the flyable computers closes the panel with a glass-to-metal solder seal. Qualifications tests should be rushed on these units to verify the adequacy of this new design. As an interesting sidelight, there are many electroluminescent panels in the spacecraft, but it is rumored that only the DSKY panels must pass the water immersion test.

If the DSKY had used the incandescent lights which were available three years ago, it would consume a few watts more power than it presently consumes. However, new segmented incandescent lamps are available, some with redundant filaments, which would not require much more power overall than the present lamps. These filamentary lamps could be used on dc with the present relays, or could be given storage elements and different driver circuits at some additional increase in power. These units have been qualified for military use and a parallel effort is recommended to see whether the present DSKY design could not be changed to use these lights in place of the electroluminescents. If such an effort were completely successful, the latching relays could be eliminated altogether, thereby reducing the problems which they always cause.



#### IV PIECE PARTS

##### 4.1 FLIGHT SPECIFICATIONS (C)

A review of Raytheon test records and waivers indicates that there has been great difficulty in obtaining semiconductor materials which can pass the flight specification (ND's 1002238, 1002248, 1002264, 1002266, 1002267). These specifications call out the method by which semiconductor materials are processed through certain environmental and operating screens. Any parts which fail during this processing are analyzed electrically and physically to determine the failure mode and mechanism. An evaluation is made of these failures and they are to be classified as to seriousness of the defect and the ability of the screening program to weed out such failures. For example, a defect which is easily weedable is classified in a category where a reasonably large percentage of failures of this type are allowed in a lot. However, if a failure is detected that is not easily screenable, the number of allowable failures per lot of this type is much smaller, generally by an order of magnitude. A typical specification (ND 1002248) will allow 0.3 percent defectives for easily weedable mechanisms at electrical test following certain environmental and operating screens, and only 0.04 percent on defects which are considered to be difficult to screen from the general population.

These percentages are considered by industry to be exceptionally tight. Experience has proved this to be so. To date, the only semiconductor material which can meet the flight processing specifications is the integrated gate SCD 1006321. This was accomplished by very close coordination between Raytheon and the supplier of this part. The attitude of this vendor played a large part in the successful qualification of the dual gate to the flight specification. In cases where the Raytheon purchases against these specifications comprise a small percentage of the vendor's total manufacturing capability, there is considerable difficulty motivating the vendor to provide the exceptional care and quality control. For example, the two principle suppliers of transistors for this program are engaged in high volume commercial and industrial transistor production. In many cases the representatives of these suppliers have indicated they would rather not do business with Raytheon than accept liability to the flight specifications.

Raytheon has often been forced into the position of buying transistors and diodes from commercial product lines and then processing the material to flight qualification specifications. Seldom does any given lot of material meet all of the requirements of the specification, and in order to meet schedule commitments, Raytheon must submit waivers against the flight qualification specification. In some cases additional screening is required.

A careful evaluation of these flight specifications is needed. Do the failure rates, as specified in these documents, really indicate the system requirements, or are they



goals intended to advance the technology of suppliers? Can this program continue to use parts which have not passed the flight qualifications? It appears that parts capable of meeting these requirements are not available at present and may not be available for some time. The confusion that exists today over adequate part quality should be resolved rapidly. If these questions remain unanswered, the Block II schedule may slip many months.

It is recommended that the following modification of flight processing specifications be evaluated:

1. A careful review should be made of all screens required by these specifications. In many cases the screening level appears to be inadequate, in that it is not severe enough to screen out all devices which have latent defects. For example, the all-aluminum bonding system in certain transistors almost completely nullifies the advantage of the high-g centrifuge test. The gold-aluminum bonding system used in most transistors is adequately stressed by this 20,000 g centrifuge test. However, the much lighter aluminum wires of 0.001 inch diameter and smaller do not generate enough pull on the bond area to reveal bad bonds. A second example is in the back bias test as performed on diodes. At present, this test is run at room temperature. Recent information indicates that a good test for surface stability on diodes requires that they be run at 100°C or more.
2. The lot acceptance criteria should be re-evaluated. These documents are a combination of screening and lot-by-lot qualification. The screens are not adequate to weed out all defective units, and the lot-by-lot qualification requirement, based on part failure rates, appears to be unrealistic in terms of material presently available.
3. Many items which can play a major part in system reliability are not included in the flight processing specifications. It is proposed that these items be included. In particular, the DSKY relays and electroluminescent panels are known to have problems which could perhaps be screened out before the components are used in the flight systems.

#### 4.2 INTEGRATED NOR GATE (1006321, 1006394) (C)

The specification control drawing for the dual NOR gate does not assure adequate noise threshold over the expected temperature range, 0°C to 70°C. (See Appendix C.) It is recommended that a sample of each shipment lot be tested at 0°C and 70°C at the

6-3-66



vendor's plant. A noise threshold of at least 50 millivolts should be specified at both temperature extremes.

The present specification control drawing for the micrologic is ambiguous. It requires "Operating Temperature Range,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ." No definition is provided for "Operating." The definition should be specific in terms of fan-in, fan-out, and noise margin (or voltage levels) at the temperature extremes. The data sheet for Philco's Milliwatt III circuits specifies greater than 30 millivolts "noise immunity" at  $-55$  and  $+125^{\circ}\text{C}$ . These circuits have been derived directly from the Apollo-NOR gate, and are available commercially. It is unreasonable that the circuits used in the Apollo-computer should be purchased to a looser specification.

The present specification was designed to serve a variety of micrologic vendors. As a result, the package materials, lead materials, and lead dimensions are virtually meaningless. If flat packs were delivered by one vendor to the limits of the specification dimensions it would be impossible for Raytheon to use them because the existing weld schedules would not be satisfactory. A separate specification should be drawn up for each vendor in order to provide definite controls over the part which he delivers. This should be no great hardship in this case since Philco is presently the only supplier of acceptable micrologic.

#### 4.3 MULTILAYER BOARDS (1006395) (C)

The flight processing specification (ND 1002293) used for the multilayer board is inadequate to screen out defective boards. The board itself is electrically tested only before and after a thermal cycle. It is possible that opens may occur in the board during thermal cycling. This test is performed on an automatic machine which is not capable of making sufficiently sensitive resistance measurements on the circuits.

Boards can have breaks in patterns and plated-through holes, which will open at some specific temperature and close again, and yet will test good at room temperature because of the mechanical pressure. It is possible to detect these failures by monitoring resistance during the thermal cycle, or by making sensitive resistance measurements before and after the cycle. A test which has been used successfully at AC Electronics consisted of a careful measurement of the resistance of every circuit. Measurements must be made to an accuracy of 0.001 ohm, or better. The circuit board is then subjected to five thermal shocks from  $-62^{\circ}\text{C}$  to  $+71^{\circ}\text{C}$  to  $-62^{\circ}\text{C}$ , with sufficient time at both temperatures for the board to reach thermal equilibrium. Following the thermal cycles the circuit resistances are measured. Any circuit which shows a resistance change of more than a few percent has probably been fractured, and that circuit board should be discarded. However, these measurements must be made by hand and the process is quite tedious and time-consuming.

A second method, used by IBM, provides excessive current through all interconnect patterns. It has been suggested that five times rated current could be used. If there



are defective joints, or potentially defective ones, it is hoped they will burn out under this condition. A further refinement of the overcurrent test would be to place the board on infrared film during this stressing. The developed film would reveal hot spots that would perhaps not burn out.

The multilayer circuit boards produced by Melpar have a coupon attached. This coupon is intended to be separated from the useful circuit board and analyzed in detail. The sequence of drilling the holes in the circuit board and in the coupon should be called out on the procurement specification so the holes in the coupon are truly representative of the holes in the circuit board proper. The coupon is monitored for intermittent opens during thermal cycling by a detector circuit. It is questionable whether the sensitivity of the detector is adequate. It is not specified in the ND. Further, the coupon may not be representative of the board quality unless the drilling operation is properly sequenced. The coupon should not be drilled after the main board. The holes should be drilled on the coupon as the drilling on the main board progresses. The same drill should be used on both the coupon and board. Certainly, the sharpness of the drill has a lot to do with the hole quality. The ND requires a vertical section be made of the plated-through hole. While this is a good test, it ignores the possibility of a horizontal section which in many cases makes it easier to detect epoxy smear and improper registration.

An Apollo Engineering Report E-1699, dated December 1964, in its appendix discussed the two common failure modes of conventional multilayer circuit boards, and presented solutions to them. The problem of circumferential cracks through the plated-through cylinders has been reported recently. This problem is normally prevented by electroplating nickel inside the hole after the first or second copper plate to give the cylinder additional strength. Melpar is not using the nickel plating.

There appears to be an alternative to the multilayer circuit board. The original design used the "signal layers" for mounting and interconnection of the flat packs. Some capacitance problems were found in that design. The multilayer boards were then substituted for the signal layers, even though it was subsequently demonstrated that a modification to the original signal layer design would allow the production of satisfactory interconnects. It would be a simple matter for logic modules to be made using both interconnection methods. If the signal layer is demonstrated to be acceptable for use in the computer (it is still used in the CDU) it could be used, since it seems to be an inherently more reliable interconnection technique than the multilayer board.





#### 4.4 MALCO PINS (1006781, 1006782) (B)

The general problem of Malco pin breakage has been discussed elsewhere (Paragraph 2.2.4.1). The male pin is fabricated from half-hard nickel. This material bends quite easily. The nickel pin has been so specified in order to facilitate the welding process. The welding advantage should be sacrificed so that a stronger material, such as stainless steel, could be used.

#### 4.5 THERMISTOR (1006291) (C)

The positive temperature coefficient thermistor (1006291) used in the temperature compensation network for the oscillator appears to be mechanically unreliable. Attempts to qualify this part have met with failure. It is quite fragile and cracks easily. During the qualification program, the part was subjected to the military specification thermal cycle tests for thermistors. It failed. Before the second set of tests, the parts were potted in a silastic material similar to the end use application. It was hoped that the thermal mass surrounding the device would have sufficient thermal delay to provide adequate protection during this test. Again the parts failed. Despite these failures during qualification tests, it has been reported there have not been failures of this part in the end use application. The part is used in such a way that the thermal gradient surrounding it is small and rate of change of temperature is quite slow. Apparently, high mechanical stresses never do reach the part during module or system testing.

Raytheon Reliability Engineering has recommended that these parts be designed out of the system. If the thermistor did fail, it would result in an erroneous voltage being applied to the temperature compensating diode, and if the thermistor were intermittent the frequency would be unstable, especially during periods of changing temperature or vibration. Circuit designers have insisted that proper operation and compensation of the crystal oscillator require this device. This is probably not true. This thermistor is required to provide the correct temperature compensating voltage at the higher temperature extremes, since the rest of the compensation network produces a voltage which is too high at the higher temperatures. A diode could be provided which would simply limit the voltage available from the temperature compensation network. This diode could be the same one used in the rest of the computer. The temperature compensation resulting from this change would be inferior to the present design, but adequate.

#### 4.6 VARIABLE INDUCTOR (1006324) (B)

In order to allow frequency adjustment of the oscillator during manufacturing, a variable choke has been used in the circuit. The variable choke which was used in Block 100 cannot be used in Block II because it is too large to fit into the new design. The new tuning coil is quite small and fragile. Extended performance testing of this



part shows that it has a failure mode which could be dangerous if field technicians were allowed to tune the oscillator. The ferrite material mounted on the tuning screw will break if it is run against the end stop. The part fails well below the three inch-pound specification for end-stop maximum torque. It is recommended that the adjustment hole on the side of the AGC case be eliminated. This will prevent field personnel from moving the slug.

The adjustments are only convenient, not necessary, during checkout of the module. If breakage occurs at this time, it may or may not be detected on the oscillator test station. It would be a very minor modification to the oscillator circuit to eliminate the need ever to adjust the coil. It is recommended that this be done.

#### 4.7 RELAYS (1006282, 1006304, 1010784) (C)

The one-half crystal can size relays used in the Block II DSKY suffer from a wide variety of quality problems. These problems indicate that the relay is presently unacceptable for space applications.

A complete review of the vendor's in process assembly and inspection methods is required immediately.

It is also recommended that the latching relay be added to the list of parts which are screened and burned-in at Raytheon. A flight processing specification should be generated. The possibility of an electrical check of the firmness of the magnetic latch under vibration should be included. A "half-current switch" test has been suggested.

The following paragraphs list specific problems noted to date.

##### 4.7.1 Contamination

- a. Gross - large metal flakes of plating which cause shorts inside the can.
- b. Minute particles - many of these are nonconducting slivers from the nylon coil form or mylar tape which will prevent proper contact closure under zero "g" environment.
- c. Diffuse contamination - the organic material used in the relay out gasses and coats the entire inside surface of the relay. This increases contact resistance. A getter is used to control this problem, but the getter tends to contribute to the minute particle problem mentioned above. Under random vibration, small pieces of getter material are shaken loose.

##### 4.7.2 Open Coils

- a. Opens at header pin to intermediate wire weld junctions.
- b. Breaks in the coil wire. The use of wire as small as No. 48 is questionable.



- c. Breaks in coil wire adjacent to the intermediate-to-coil wire solder joint.

#### 4.7.3 Shorts

Shorts between coils caused by faults in insulation and assembly techniques.

#### 4.8 ELECTROLUMINESCENT PANELS (1006315) (D)

During Blocks I and 100 a program was started to develop a source of truly hermetically sealed electroluminescent panels for digital displays and certain computer program function indicators. This effort has been long and tedious with many starts and many failures along the way. As a result, today it is still not known whether we have flightworthy electroluminescent panels or not.

There is no life test data on the sealed units available. It is projected that electroluminescent panels have a known wearout mechanism. This device apparently decreases in intensity with time. It has been estimated that it will decrease to approximately 40 percent of its initial brightness. Although this is not a catastrophic failure mechanism, it may fall below system requirements. Inasmuch as this device is a new development, good long-term light information is not available. It is suggested that Raytheon or MIT start a long-term life test program on these devices immediately. Until complete confidence in the life factors for this part are established, it is recommended that all electroluminescent panels be replaced every 1,000 hours.

#### 4.9 SWITCH (1010901-2) (D)

A review of SCD 1010901-2, the microswitch used in the DSKY keyboard reveals that there is no bounce specification called out. It is recommended that this be rectified immediately. Further, the push-button switch assembly (2003974) as fabricated by Raytheon should be subjected to complete functional and environmental testing as rapidly as possible. Difficulties experienced during Block I/100 with push-button switches indicate this is a critical design area and all testing of this part should have high priority.

#### 4.10 "WIRE-WRAP" WIRE (1006376) (A)

Interconnections in AGC trays and the DSKY's are made by the wire-wrap technique. This technique requires that conductors be routed around the Malco pin. The insulation on the wire-wrap wire prevents electrical contact between pins and the conductor. The programming of the wire-wrap machine provides slack when the wire is laid down so that the wire is not pulled taut around these Malco pins. However, after many successive wires are laid down in a particular area, there is a possibility that the wire will be pressed firmly against a sharp corner of a Malco pin. During the potting



operation, there is further shifting and moving of the wires. If the insulation material of the wire is not tough, the pressure will eventually cause a cut in the insulation. This is sometimes referred to as a "cold flow." The simple solution to this problem would be to obtain a wire with a greater "cold flow" resistance. However, these tougher wires present problems to the wire-wrap machine. They do not strip easily and have a mechanical memory which makes them spring up from the wire wrapping surface. It is, therefore, necessary to make a compromise between the toughness of the insulation and the ability of the wire-wrap machine to perform the wire-wrap operation successfully.

After more than a year of search for an acceptable wire, Raytheon has finally located a vendor who can produce a wire which is both tough and "wrappable."

#### 4.11 TAPE WOUND CORE (1006320) (B)

The tests made on the fixed-memory cores prior to wiring are insufficient to guarantee that the ZERO output will be below the acceptable limit. In the absence of such testing, there is some danger that a completed module will be unacceptable due to high ZERO outputs. The module will then have to be discarded and a replacement made, with no assurance that the replacement will be any better. The ZERO level is determined by the degree of balance of the shuttle voltages of the + and - groups of cores threaded by a sense winding. In the worst case there are 64 cores in each group, thus a few millivolts difference in shuttle voltage of each pair of cores can result in a significant ZERO output. The specification on the core limits the maximum shuttle voltage to 15 mv with a drive current rise time of 1 amp/ $\mu$ sec. It is assumed that with a rise time of 0.4 amp/ $\mu$ sec, as the core sees in use in the computer memory, the maximum shuttle voltage would be 6 mv. The specification should call out a minimum value of 5 mv in order to limit the net shuttle of 64 pairs of cores to 60 mv, which is about 20 percent of the ONE output. If necessary, the cores can be graded to control the shuttle voltage difference within groups of 128 cores used in a particular rope module. The effect of strand select currents on the shuttle voltage should also be incorporated in the core test at the same time.

#### 4.12 CRYSTAL (1006847) (A)

Although the qualification of this part is not completed as of this date, it appears that the part is suitable for the application. An extensive evaluation program was performed by the circuit designer to prove the flight worthiness of this device under environmental extremes. It is recommended that an acoustic test be added to the part qualification test as the LGC system specification has a significant acoustic requirements.



#### 4.13 TRANSISTORS AND DIODES (1006323, 1006310, and 1006751) (B)

It appears that the specification control drawings for the transistors and diodes utilized in the DSKY were generated before the supply voltage was determined. Good reliability practice dictates that these devices should have at least twice the voltage rating of any voltage to be encountered in the application. The DSKY maximum supply is 25.5 volts. The diodes and transistors should be rated to at least 50 volts. Presently, the 1006323 transistor is rated at 35 volts and the diode 1006751 is rated at 30 volts. Analysis of the Indicator Driver Module for the DSKY indicates that the transistors do carry considerable current (200 ma peak) and that the ambients surrounding these devices are also high (100°C). This combination of internal heating, high ambient, and low voltage rating on the devices add up to an unreliable situation.

#### 4.14 AUDIO TRANSFORMER (1010291) (B)

The audio interstage coupling transformer used in two places in the DSKY Power Supply and in the "A" interface circuit is a reliability hazard. Devices of this generic type have been used in other programs and have proven to be unreliable. The difficulty rests mainly in the size of the magnet wire (No. 41 or smaller), and the method of termination of the magnet wire to the external leads. There appears to be no good reason why a larger and more reliable transformer should not be substituted in this application.

#### 4.15 RESISTORS (1006750, 1006760, 1006714, 1006712, 1006788, 1006802) (A)

#### 4.16 CAPACITORS (1006755, 1006777, 1006793) (A)

#### 4.17 INDUCTORS (1006327, 1006325, 1010406) (A)

#### 4.18 POWER INDUCTOR (1006328) (C)

The specification control drawing for this inductor specifies the inductance only at a current of 7 amperes. As pointed out in Appendix A, proper operation of the power supply circuit requires that the inductance vary from 25  $\mu$ hy at 7 amps to 370  $\mu$ hy at 0.2 amps. The specification should be corrected in this regard.

#### 4.19 TRANSFORMERS (PULSED) (1006319, 1006293) (C)

Neither of these pulse transformers has a common-mode rejection requirement in the specification. This appears to be required for proper system operation.





## V TESTING

For the purposes of this discussion on testing, no differentiation will be made between the computer and the DSKY or between the computer modules and the DSKY modules.

### 5.1 QUALIFICATION TESTING

#### 5.1.1 Computer (C)

The present schedule for the computer qualification test shows testing to begin early in July and to be completed by November. In view of the fact that the Block I-100 qualification test began in August 1965 and has not yet been completed, the Block II plan appears quite optimistic.

The qualification test specification ND 1002037-C for the Block II computer has not yet been issued. If it is issued in its present form, it will provide for qualification of the computer subsystem to the LEM mission environment. Qualification of the computer to the command module environment will be provided during qualification of the entire G and N system. This is considered a very difficult predicament. At the computer qualification test it is possible to be thorough in testing the computer but the environment is very special to the LEM and is not considered to give the computer a satisfactory test. The command module environment is, in some cases, more severe, but the computer is required to support the entire G and N system during that test and, therefore, the testing of the computer itself cannot be as thorough. Since the qualification tests are intended to prove out the design and producibility of the computer, and since only one design is used for both the LEM and the command module, it is felt that a single test could be devised which would guarantee that the computer is fully qualified for either use. This combined qualification test would presumably make use of the more severe environments from the LEM and the command module missions when the relative severity is apparent. In some cases it may be necessary to perform parts of both tests when the relative severity cannot be accurately determined.

The proposed qualification test plan does not presently include acoustic noise testing, even though the LEM design environment calls out an acoustic noise level of 150 db overall. This level is considered significant, and the acoustic test should be put into the qualification test plan. EMI testing has also been eliminated. In view of the previous difficulty with computer noise susceptibility and considering the redesign of the computer structure to utilize magnesium, this decision should be reconsidered. The committee recommends that EMI testing be done, if for no other reason, at least to gather data on the generated noise levels and the probable susceptibility levels. This information can be vital to the spacecraft systems integrator.



The program which the digital computer runs during the qualification test is very important. At the present time the FTM programs described in Paragraph 7.1 are used to check the computer. These programs take several minutes to accomplish, which means that certain areas of the computer are not exercised at every environmental condition. It should be possible to construct a short program loop which provides a more rapidly repetitive exercise of the computer and thereby improve the probability of discovering a malfunction which is induced by a single environmental condition, and not by other conditions.

#### 5.1.2 Modules (D)

The module qualification program requires some careful thought, and the review committee is still somewhat divided in its opinions on this matter. The vibration levels called out for module qualification testing are presently well below those levels which are expected to be encountered in the computer and the DSKY during qualification and acceptance tests. For example, it is anticipated that vibration levels as high as 50 g's can be experienced by modules mounted in the computer, yet the module qualification test requires only 10 g's. In some cases the module is not exercised electrically during the test environment but is tested functionally before and after. Marginal circuit problems and interconnection problems which show up during environment may, therefore, be overlooked because they are not apparent when the environment is removed. In order to exercise the modules rigorously during the environmental test, a considerable investment in automated test equipment would be required, unless the testing is done in an operating computer. That amounts to an entire computer qualification test, not a module level test. An attractive alternative would therefore seem to be to dispense with formal module qualification testing for most of the computer modules.

Those modules which represent difficult design problems, however, should undergo a thorough engineering evaluation test program. Modules which should be so tested, and for which satisfactory tests can be arranged, include the oscillator module, the power supply module, the erasable memory module, and the fixed memory modules. Other modules should be qualified as part of the computer assembly during its qualification test, since they can be fully exercised when installed in the computer but not when tested alone. That is the recommendation at this time, but a rating of indeterminate should be given to the module qualification test plan pending further investigation.

#### 5.1.3 Parts Qualification (C)

In most qualification programs electronic parts are qualified before the modules and the system. Scheduling difficulties on the Apollo project have caused the parts qualification program to occur in parallel with module and system qualification tests. For example, the Block I-100 part qualification program has not been completed. Of the 45 parts to be qualified, 27 tests have been completed. Eighteen remain to be



completed, including such parts as the negative temperature coefficient thermistor, a new diode for the oscillator, and the pulse transformer used in the interface circuits. If severe part problems are discovered there is little opportunity to stop and make appropriate design corrections or part substitutions, and there is a natural tendency by all parties to minimize the seriousness of any failures because of firm schedule commitments. As discussed in Section IV, there are several unqualified parts which appear to represent potential difficulties in the Block II systems.

To date, failure of a part in the qualification program seems to have had little bearing on whether or not that part was used in the system. This would be understandable if the part qualification tests had been completed after the module design had been frozen, but this has not always been the case. It is recommended that the part qualification program be accelerated in order to guarantee that sound parts are available for the computer system. It is recommended, in addition, that when a part fails the qualification test, that part should be designed out of the system.

## 5.2 ACCEPTANCE TESTING

### 5.2.1 Computer (C)

The procurement specification for the production computers has not been completed. As a result, there is no official acceptance test for the computers. However, it is the committee's understanding that the acceptance test will include a 3 g sinusoidal shake and the "new" thermal cycle. This acceptance test is run with the computer Final Test Method (FTM) program in operation, and the same comments apply to the use of this program here as in the previous section; namely, it takes too long. Especially with the sinusoidal vibration, it is very likely that the critical parts of the computer will not be exercised at the time the structure sees its maximum amplitude vibration. The program which the computer runs during the acceptance test should be especially designed to provide the maximum stress for the logic and memory, and to run in a loop which takes no more than 50 to 100 milliseconds to run through.

Paragraph 2.4 describes the problems associated with the timing margins and noise margins of the computer. As indicated there, the lack of a worst-case design philosophy and the dependence of the computer timing and noise margins on the specific construction of the computer require that great reliance be placed on a thorough acceptance test to guarantee adequate margins. Without adequate acceptance tests utilizing a specially designed program and making use of marginal checking techniques, adequate margins cannot be guaranteed. Marginal testing facilities should be provided in the computer test set in order to guarantee that the computer has some design margins in excess of those needed to operate in the simulated environment. In order to test the noise threshold of the computer, the +4 volts should be varied as discussed in Appendix C. The program which the computer is running at



that time should be especially designed to provide a bad noise situation, since that is what is being tested. The master clock should also be varied in frequency as the computer soaks at the temperature extremes in order to guarantee that there are timing margins at the temperature extremes. At this time it is difficult to predict what limits should be placed on the +4 volts and on the oscillator frequency. These numbers can best be determined after the detailed timing analysis and noise analysis have been performed.

The test equipment should also be designed to juggle the memory drive currents and the sense amplifier thresholds. It would be desirable, but it may not be possible, to vary the strobe time in the sense amplifiers as well. Again, the computer must be running a program which is especially designed to provide bad situations for these marginal tests.

The Final Test Method for the Block 100 computer apparently allows the individual tests to be run in any arbitrary order. If this same procedure is to be applied to the Block II computer it is neither reasonable nor desirable. A fixed sequence should be prescribed with allowable variations specified whenever they exist. There is also a statement in the Block 100 Final Test Method that a single restart is not indicative of a failure but must be repeated to cause the test to fail. Any unprogrammed or unplanned restart constitutes a computer failure.

The thermal testing should be modified. It presently allows the computer to be operated at the temperature extremes, but not during the excursion of the computer temperature from one extreme to the other. Many of the possible failure modes of the computer are excited more by temperature gradients than by absolute temperatures. The test should be redesigned to provide several cycles of temperature variation, and the computer must be operating during the thermal transients.

During acceptance testing on other computer projects, it has been found that thermal cycling and vibration testing simultaneously are very likely to detect more workmanship errors than these same tests conducted separately. Furthermore, experts are almost universally in agreement that a random shake is of greater benefit than a sinusoidal shake. The committee has been told that the Raytheon factory in which the acceptance tests are performed does not have a random shaking capability and that this is the reason sinusoidal acceptance tests are performed. This appears to be a marginal situation. It is recommended that the computer be given a combined thermal and vibration test by simply mounting the computer on a heat exchanger on the shaker, and modulating the temperature of the fluid through the heat exchanger while the vibration is taking place. It is further recommended that a random shake be employed.

The tests of the input/output equipment are not thorough. The programs do not check at all certain portions of the input/output functions. Because the supporting equipment



is not sufficiently automatic, the detailed signal tests are usually provided by the operator and are usually performed only before and after the environments.

It is reported that a recertification plan exists for those computers which have been repaired and are about to be rated to flight status. There are conflicting opinions as to what this recertification plan will be. It is strongly urged that a firm procedure be adopted.

#### 5.2.2 Modules (C)

There is presently no vibration in the acceptance procedure for the individual computer modules. Except for the rope modules, this procedure is probably adequate as long as the entire computer receives a full acceptance test following the replacement of any failed modules at the factory, and assuming that modules are never replaced in the field. There is a disadvantage to this approach in that the manufacturer of these modules cannot sell them off as spares until they are installed in a computer.

An important exception to this concept is the set of flight ropes. While it is possible that a test computer could be reserved for acceptance testing of the rope modules, it is felt that this would be a wasteful procedure and would not be the best test for detecting workmanship defects in the rope. The ropes should be given an acceptance test at the module level. This acceptance test should include vibration and temperature cycling while monitoring series connections of the rope windings. The circuit used to monitor these windings should have a sensitivity and a speed adequate to detect momentary changes in resistance of several percent with a duration of a microsecond or less.

Previous programs have demonstrated the value of a combined temperature vibration acceptance test at the module level. Workmanship difficulties which produce intermittent malfunctions are usually detected more readily in the module level, especially with the aid of a carefully prepared operational test fixture which can exercise the module inputs and monitor the outputs. At the present time the acceptance test for the Block 100 modules consists of testing them at three temperatures: 0°C, 25°C, 70°C. The procurement specifications state that testing at the temperature extremes is not intended to verify adequate performance but only to detect intermittent welds or other workmanship problems. This is considered to be an inadequate procedure. There are many dissimilar materials used in the construction of the computer, and a bad weld often exhibits a thermostatic action which causes it to open or shut only at a particular temperature. Thermal shock combined with vibration is recommended for detecting problems of this kind. The test should be designed to create the maximum possible thermal gradient across the module, and the module must be rapidly exercised during this transient period.





Tests on the erasable memory module, if the present plans are not changed, will be nonoperational. There are several kinds of problems which can be expected in such a module and the acceptance tests should be designed to weed out at least the commonly encountered difficulties. For example, workmanship problems occur frequently in terminating the wires, and at first blush one would suggest a series connection of all the wires in the module to detect any bad solder joints or broken wires. Unfortunately, the selection diodes in the windings prevent this series connection; therefore, an operational test will be required. This same operational test, if properly implemented, can detect not only broken wires but also broken or chipped cores and bad diodes. This operational test must be designed to exercise the memory as quickly as possible, and therefore should probably be accomplished with a special memory tester rather than with the computer itself.

Numerous problems have also been uncovered in the indicator driver modules of the DSKY, especially in the relays. These modules should also receive the combined vibration and temperature test.

In the course of reviewing the designs of the individual modules, it has also been necessary to review the corresponding Factory Test Plans (FTP's). All of the factory test plan documents which have been reviewed were marked, "PRELIMINARY", even though modules are being built and delivered and presumably tested according to these plans. Not all FTP's have been reviewed. These Factory Test Plans are documents which are intended to be used at the in-process and acceptance testing levels. They are created by Raytheon and bear no evidence of having been approved by MIT or NASA. The MIT engineers made it clear that, although they are interested in the detailed testing which is accomplished on each of the modules, they feel the responsibility for the thoroughness of the tests rests with Raytheon. The committee's opinion is that this should not be so. The original designer of the circuit should be required to certify the adequacy of the tests.

#### 5.2.2.1 Logic Modules

The following FTP's were reviewed: 187914 through 187934, 186332, 186420 through 186422, 186447 through 186454, 186465 through 186467, 186988, 186995, 187000, 187001, 187010, 187011.

The individual FTP's for each module do not contain enough information for the review committee to determine the adequacies of the tests. These tests are performed at an automatic testing station utilizing a PB-250 computer to provide the input stimuli for the logic modules and to observe the outputs of the modules. The factory test plan makes reference to truth tables and a "test tape with same FTP number and revision". The content of these test tapes has not been reviewed by the committee. These factory tests are intended to demonstrate the general functioning of the individual modules and are not intended to be marginal tests.





The modules are tested at  $-10^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+70^{\circ}\text{C}$ . The modules are soaked at these temperatures before the tests are performed. Input test voltages are not appropriate in many cases to the circuits being tested. For example, the input logic ONE is defined to be a level "of not less than 850 millivolts". As shown in Table C-1 of Appendix C, this is inappropriate for the low temperature condition, since a  $V_{\text{IN}}$  of 910 millivolts is required to guarantee proper operation of the integrated NOR gate. Another FTP referring to the same logic module (there appear to be two FTP's for each logic module) establishes an input logic signal of  $850 \pm 50$  millivolts. This is inappropriate even at room temperature, and certainly inappropriate at the lower temperatures. Since the objective of the testing is not to determine marginality but to demonstrate functionality, the input signals should be in the neighborhood of one volt or greater.

The test plan also contains an elaborate set of rules for determining the load resistors to be applied externally to the modules. The value of the load resistor is taken from a matrix whose dimensions are the number of internal drivers connected together and the number of internal bases connected to that driving source. This table could be considerably simplified without destroying the usefulness of the functional test if the output logic one and zero signals were allowed greater ranges of values.

The FTP also allows the same tolerances to be placed on the input and output signals when the tests are repeated with 4.8 volts and 3.4 volts as a power supply input. Again, the numbers cited for the one and zero levels are inappropriate and should be determined in accordance with the table in Appendix C. These tests are static and will give no indication of timing problems. This is certainly adequate if only workmanship problems are to be sought out.

#### 5.2.2.2 Interface Modules

These modules are covered by FTP's 187196 and 187197. These test plans appear to be consistent with the circuit designs and the intended usage of these circuits with the exceptions noted below.

The XT circuit is tested with a single value of load resistor and no shunt capacity. It is recommended that to guarantee proper operation of the circuit, the simulated loads during this test should have the values of resistance and cable capacitance which the circuit will see in the spacecraft. The circuit should also be tested at the duty cycle which it will experience in actual use.

The test for the "C" circuit is adequate, except that the output impedance is not tested at 40 volts. This is a condition specified in the electrical interface control documents and should be applied as a test.



#### 5.2.2.3 Power Supply

Factory Test Plan 186413 covers this module. The critique of the FTP is implicit in the power supply review contained in Appendix A. To summarize that briefly, the FTP does not provide a measure of the input current to the power supply under low load conditions, and therefore will not discover possible faults in the control circuitry.

It is recommended that the short-circuit test of the power supply be made a continuous short circuit rather than a pulsed short circuit. The interface control documents do not limit the amount of noise which the power supply can conduct onto the main power bus. It would be advisable for the FTP at least to make a measurement of this noise.

#### 5.2.2.4 Rope Memory Module

FTP 186305 presently specifies tests at  $-10^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+60^{\circ}\text{C}$ . The committee has been informed that the  $+60^{\circ}\text{C}$  will be changed to  $+70^{\circ}\text{C}$  for all production modules. This FTP provides that the information wound into the core rope module will be compared with data from a punched paper tape. Gross resistance measurements are made of the individual rope windings. The resistance range of 4 to 12 ohms allowed for the parity, inhibit, set, reset, and clear windings appears to be excessive. The wire length and wire size is known for all of these windings and a more precise resistance measurement should be required.

In the dynamic testing of the module the drive current magnitudes are set at  $25^{\circ}\text{C}$  and, since the driver is not subjected to the temperature extremes, are maintained at the original value. This is deemed to be inadequate since in the computer, driver outputs will vary with temperature but the core parameters are essentially independent of temperature over the test range. The drive current used to test the rope module should correspond to the extremes of the current driver tolerance. This amounts to a marginal test of the rope module. This recommendation is especially critical for the reset current, since that current is the one which actually produces the read signal.

The voltage levels which have been specified for acceptable one and zero levels appear to have no margin to allow for degradation of the system after testing. The acceptable levels at the module test should also provide a practical dead band about sense amplifier threshold level. The acceptable one level is specified over an interval of .6 microseconds long, and the zero level over a 1.5 microsecond interval, but the inferred instrumentation does not provide for such a measurement. This is a practical method for assuring an adequate signal-to-noise ratio and the instrumentation should be provided.



#### 5.2.2.5 Strand Select Module

FTP 186138 provides for testing the strand select module at  $-10^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+70^{\circ}\text{C}$  with a voltage margin test at  $-10^{\circ}\text{C}$  and  $+70^{\circ}\text{C}$ . It is during this test that the emitter resistor of the current regulator is selected and installed. The accuracy with which the current is determined during this test is about  $\pm 4$  percent. A discussion of the accuracies of these various currents is contained in Section II. These currents are not compensated for temperature during the test, but should be. Generally, the simulated load exceeds the system requirement, but this is considered acceptable.

#### 5.2.2.6 Rope Driver Module

FTP 186247 is vague with regard to the low level of the input voltage described under the dynamic tests. The purpose of the "A" float level measurement under Paragraph 4.3.5 is not understood. The FTP allows current deviations from the nominal, due to a combination of voltage and temperature, which are too large. While the system can tolerate considerable variation in the inhibit and clear currents, the specified variations are not consistent with the expected circuit performance. The expected variations in the reset current clearly indicate that the rope module requires a marginal test.

#### 5.2.2.7 Erasable Memory Module

FTP 186187 requires testing of the erasable memory module at  $25^{\circ}\text{C}$  only. This is considered to be an inadequate test. Satisfactory testing methods are discussed in Paragraph 2.5. The erasable memory should be provided with an adequate marginal test over the temperature range. In addition, the signal levels should be specified to provide a dead band around the sense amplifier threshold and should provide for degradation in the sense amplifiers.

#### 5.2.2.8 Current Switch Module

FTP 186049 provides for testing current switch modules at  $25^{\circ}\text{C}$  and exercises each core under simulated system drive timing and load conditions. If these tests were provided at the temperature extremes as well, this FTP would be acceptable.

#### 5.2.2.9 Erasable Driver Module

FTP 186062 provides for testing the driver module at the three temperatures. The test allows too great a variation in the driver current under the voltage margin test.



## VI DOCUMENTATION (C)

At the present time the whole Apollo documentation system must be given a rating of inadequate. Documentation appears to exist in almost staggering quantities, yet in many instances it is repetitive, inaccurate, out of date, or incomplete. Examples are numerous where in the very places one would expect absolute interface control, circuits are described as "For Reference Only" or "For Information Only." As noted previously with regard to the qualification test plan, the computer and module procurement specifications and other documents are normally approved late with respect to the production of the computer, and therefore have little bearing on the design of it. A genuine system integration function is needed. This function would provide a file of interface control documents and attempt to work out the discrepancies in these documents. One group of people should be charged with bringing the entire documentation of the guidance and navigation system, internal as well as external, up to a satisfactory working level. This system integration group should also be provided with sufficient muscle to insist that the specifications and other control documents are obeyed.

### 6.1 INTERFACE CONTROL DOCUMENTS

There is reason to believe that the interface control documents are not a contractual requirement. These documents tend to be inaccurate and incomplete. Those parties who are required to sign the interface control documents often feel that they need not abide by a literal interpretation of the document because it would mean a redesign of some of their interface circuits. Mechanical designers of the computer structure allege that they have not seen an interface control document which clearly defines the envelope available to the computer under all conditions of flight (particularly vibration). The thermal interface control document between MIT and Grumman is of a different nature than the thermal interface negotiated between MIT and North American.

Some specific criticisms of the drawings which are supposed to control the physical interface are the following:

- a. Aluminum material is called out for the computer cover that is in contact with the cold plate. That computer cover is being manufactured of magnesium.
- b. The envelope dimensions called out for the computer are not specified as maximum. The dimension called out is 6.00 inch. The nominal computer dimension is 5.996 inch, and if there is any internal pressurization at all it will exceed the 6-inch value.



- c. The command module installation drawings do not call out the need for access to the computer for installation of rope modules in the spacecraft.

The electrical interface control documents specify a variety of loads for the commonly used interface circuits and, in some cases, the value of the load impedance is simply unknown. While it is conceivable to design the circuits with sufficient margins to handle all anticipated loads, there is no document which can be relied upon to provide assurance that all real loads have been properly anticipated. It is unreasonable to design a test for these interface circuits in the factory which will include all of the possible loads, and it is not apparent that the circuits are presently tested with the worst-case load. Furthermore, there is no specification of the interface between the computer and its test set.

There is one formal interface control document which is generally deemed to be satisfactory: that is the LEM PGNCs functional interface requirements approved by Grumman, MIT, and NASA. Other than keeping this ICD up to date, it is felt there is no further work required insofar as that document is concerned. There is no such functional interface requirement document for the command module. Such a document should be created.

## 6.2 FAILURE REPORTING

As a general comment, the complete process of failure reporting is much too slow. Apollo failure reports are generated as soon as the computer acceptance tests have begun. The level of detail in these first reports is generally sketchy and often does not include any notation of the environmental situation in which the failure took place. As a result, many of these failures are simply listed as ghosts which are not repeated. The failure analysis reports are supposed to provide exhaustive explanation of the nature of the failure and recommend any corrective action. The corrective action reports then report what action has been taken. In the documentation review by the committee, the failure analysis reports were observed to lag behind the original failure report by no less than 3 months and, in many cases, by as much as 9 months. Few corrective action reports were found to exist. As a result this whole failure reporting process is completely ineffective insofar as it is intended to accomplish its primary aim, that is, to allow the engineers to make design changes to correct the failure mechanisms which are found during the acceptance testing.

There is another aspect to this which is bothersome. Failures which are detected by Raytheon during manufacturing and factory testing, but prior to acceptance testing of



the computer modules, are not part of the formal failure reporting system. This appears to be a dangerous situation. Failures which occur infrequently during final sell-off of the computers (or their modules) would not be considered dangerous and might not be given urgent redesign attention. On the other hand, if these occasional failures are merely a continuation of failure modes observed frequently during the build-up and testing of the modules during the manufacturing process, the situation would be viewed quite differently. It is recommended, therefore, that failure reporting begin as soon as the module is assembled. There is danger that such a reporting system would include types of failure (workmanship, missed welds, erroneous test results) which would tend to obscure the real failure modes which are likely to be important at the computer system level. An attempt should be made to design the preacceptance test failure reporting system so as to guarantee to include failures which are important to the reliability of the product and not to include those failures which will not affect that reliability.

### 6.3 LOGIC DRAWINGS AND WIRE LISTS

At the beginning of the design review, a set of latest up-to-date logic drawings was gotten from MIT, as well as a latest wire list. The logic drawings were relatively easy to get, but the wire lists are very scarce. In fact, the checkout engineers at the Raytheon factory are required to use marked-up obsolete wire lists. When the wire list was cross-checked with the logic diagrams, numerous discrepancies were discovered, and not one of these discrepancies has been corrected yet.

### 6.4 SYSTEM SPECIFICATIONS

A detailed review of the system Master End Item and the Performance and Interface Specifications was made by four members of the review team. These included

#### North American Document (Command Module)

SID 65-299 "Block II GN&C Performance & Interface Document" dated 2 October 1965 approved by MIT and NASA 30 November 1965.

#### MIT Document (Command Module)

ME1 No. 201500 Spec. No. PS2015000 "Master End Item Specification Block II G&N. "

#### Grumman Document (LEM)

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MIT Document (LEM)

ME1 No. 6015000 Spec. No. PS6015000 "Master End Item Specification  
LEM GN&C" dated 15 October 1965.

It is understandable that separate "top specifications" are required for the command module and the LEM due to differences in functional requirements for the guidance and navigation system and, therefore, the computer. However, except for the fact that one system has two DSKY's and the other (LEM) only one, the computer subsystems are identical. It is, therefore, not clear why such major discrepancies exist in the system and subsystem weights as those listed below.

LEM P&I

G&N Total Weight	240 lbs
Computer Weight	58 lbs

CM P&I

G&N Total Weight	400 lbs
Computer Weight	80 lbs

Since the actual computer weight will be in the neighborhood of 65 pounds, Grumman structural people may have a serious problem.

Generally, except for the inaccuracies, the above documents can be considered to contain adequate information. Based on those documents, it is strongly recommended that a second level document should be written entitled, "Computer Subsystem Design Criteria." This document should contain all of the information necessary to design, fabricate, and test the computer subsystem to fulfill both the command module and the LEM requirements, and should include, by reference, all of the appropriate interface and testing documents. With such a document in force it would then be possible for the manufacturer of the computer to generate a realistic end-item specification. This document would specify those criteria and tests which the computer hardware would be required to meet in the acceptance test.

Much of the information that would be required in these documents is available in the Digital Design Memos, Digital Development Memos, and Apollo Guidance Memos generated at MIT. Many of these memoranda provide excellent descriptions of the hardware and how it is intended to function. They are, unfortunately, not official documents and therefore have no official status in the program, even though one document, DD185, is constantly referred to by all parties as though it were the official signal interface document of the digital computer. The more important of these documents should at least be summarized and made an official part of the Apollo system documentation.



## 6.5 PROGRAMMING MANUAL

There is no official programmers' manual for the Apollo guidance computer. An informal memo, AGC No. 9, is taken to be the gospel and is used by the programmers as a description of the computer instructions and how they behave. This document certainly provides an adequate description of the hardware. On the other hand, there are many programming restrictions outside the hardware which are not included in this document. Those restrictions are discussed in the next section.

6-3-66



## VI DOCUMENTATION (C)

At the present time the whole Apollo documentation system must be given a rating of inadequate. Documentation appears to exist in almost staggering quantities, yet in many instances it is repetitive, inaccurate, out of date, or incomplete. Examples are numerous where in the very places one would expect absolute interface control, circuits are described as "For Reference Only" or "For Information Only." As noted previously with regard to the qualification test plan, the computer and module procurement specifications and other documents are normally approved late with respect to the production of the computer, and therefore have little bearing on the design of it. A genuine system integration function is needed. This function would provide a file of interface control documents and attempt to work out the discrepancies in these documents. One group of people should be charged with bringing the entire documentation of the guidance and navigation system, internal as well as external, up to a satisfactory working level. This system integration group should also be provided with sufficient muscle to insist that the specifications and other control documents are obeyed. At this time there is evidence that lack of approved, signed control specifications has contributed greatly to the individualized design approaches for the different subsystems within the G and N system.

### 6.1 INTERFACE CONTROL DOCUMENTS

There is reason to believe that the interface control documents are not a contractual requirement. These documents tend to be inaccurate and incomplete. Those parties who are required to sign the interface control documents often feel that they need not abide by a literal interpretation of the document because it would mean a redesign of some of their interface circuits. MIT has on occasion been instructed by NASA to sign these documents even though MIT did not agree with the content and had no intention of abiding by the content. Mechanical designers of the computer structure allege that they have not seen an interface control document which clearly defines the minimum envelope available to the computer under all conditions of flight (particularly vibration). The thermal interface control document between MIT and Grumman is of a different nature than the thermal interface negotiated between MIT and North American.

Some specific criticisms of the drawings which are supposed to control the physical interface are the following:

- a. Aluminum material is called out for the computer cover that is in contact with the cold plate. That computer cover is being manufactured of magnesium.
- b. The envelope dimensions called out for the computer are not specified as maximum. The dimension called out is 6.00 inch. The nominal computer dimension is 5.996 inch, and if there is any internal pressurization at all it will exceed the 6-inch value.



- c. The command module installation drawings do not call out the need for access to the computer for installation of rope modules in the spacecraft.

The electrical interface control documents specify a variety of loads for the commonly used interface circuits and, in some cases, the value of the load impedance is simply unknown. While it is conceivable to design the circuits with sufficient margins to handle all anticipated loads, there is no document which can be relied upon to provide assurance that all real loads have been properly anticipated. It is unreasonable to design a test for these interface circuits in the factory which will include all of the possible loads, and it is not apparent that the circuits are presently tested with the worst-case load. Furthermore, there is no specification of the interface between the computer and its test set.

There is one formal interface control document which is generally deemed to be satisfactory: that is the LEM PGNCs functional interface requirements approved by Grumman, MIT, and NASA. Other than keeping this ICD up to date, it is felt there is no further work required insofar as that document is concerned. There is no such functional interface requirement document for the command module. Such a document should be created.

## 6.2 FAILURE REPORTING

As a general comment, the complete process of failure reporting is much too slow. Apollo failure reports are generated as soon as the computer acceptance tests have begun. The level of detail in these first reports is generally sketchy and often does not include any notation of the environmental situation in which the failure took place. As a result, many of these failures are simply listed as ghosts which are not repeated. The failure analysis reports are supposed to provide exhaustive explanation of the nature of the failure and recommend any corrective action. The corrective action reports then report what action has been taken. In the documentation review by the committee, the failure analysis reports were observed to lag behind the original failure report by no less than 3 months and, in many cases, by as much as 9 months. Few corrective action reports were found to exist. In many cases the failure analysis reports were impertinent, stating that although the particular observation was properly categorized as a failure at the time, the specifications had subsequently been changed and the same action under the present specification would no longer be classed a failure. As a result this whole failure reporting process is completely ineffective insofar as it is intended to accomplish its primary aim, that is, to allow the engineers to make design changes to correct the failure mechanisms which are found during the acceptance testing.

There is another aspect to this which is bothersome. Failures which are detected by Raytheon during manufacturing and factory testing, but prior to acceptance testing of



the computer modules, are not part of the formal failure reporting system. This appears to be a dangerous situation. Failures which occur infrequently during final sell-off of the computers (or their modules) would not be considered dangerous and might not be given urgent redesign attention. On the other hand, if these occasional failures are merely a continuation of failure modes observed frequently during the build-up and testing of the modules during the manufacturing process, the situation would be viewed quite differently. It is recommended, therefore, that failure reporting begin as soon as the module is assembled. There is danger that such a reporting system would include types of failure (workmanship, missed welds, erroneous test results) which would tend to obscure the real failure modes which are likely to be important at the computer system level. An attempt should be made to design the preacceptance test failure reporting system so as to guarantee to include failures which are important to the reliability of the product and not to include those failures which will not affect that reliability.

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At the beginning of the design review, a set of latest up-to-date logic drawings was gotten from MIT, as well as a latest wire list. The logic drawings were relatively easy to get, but the wire lists are very scarce. In fact, the checkout engineers at the Raytheon factory are required to use marked-up obsolete wire lists. When the wire list was cross-checked with the logic diagrams, numerous discrepancies were discovered. Many of these discrepancies, it was learned later, had been reported in a memo written by Mr. Richard Volpi (of Raytheon) several weeks before. Mr. Volpi's discrepancies had not and, as far as the committee can tell, still have not been corrected in the present documentation. Mr. Volpi's responsibility is to keep the logic diagrams and wire lists compatible, and yet he does not sit on the change review board and is apparently not given direct access to the design information at the time the change is made. As a result, he is really not able to do his function properly. It should be emphasized that it is a necessary function and he should be placed more directly in the change loop. Furthermore, his recommendations should be given some attention.

### 6.4 SYSTEM SPECIFICATIONS

A detailed review of the system Master End Item and the Performance and Interface Specifications was made by four members of the review team. These included

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## 6.5 PROGRAMMING MANUAL

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## VII PROGRAMS

This general subject of programs and programming documentation was reviewed only from the standpoint of how the hardware might influence the writing of the programs. Functional requirements of the computer are not stated in any official document and, therefore, it was impossible to review the general topic of adequacy of the computer or the programs to fulfill these functional requirements. However, the mission programs are influenced by computer design, and were discussed briefly. Some of the factory programs were pursued, since they affect the thoroughness with which the computer is tested.

### 7.1 MISSION PROGRAMS (D)

The bulk of the mission program is written in an interpretive language. The interpreter program which is contained in the airborne computer consists of a set of basic subroutines which perform very elaborate operations such as matrix multiply, double precision add, etc. These subroutines are invoked by instructions stored in the computer memory in a highly compact form. These instructions are retrieved from the memory, decoded by the main interpretive program, and are used to call up the appropriate subroutines. The principal advantage of such a system is twofold. First, it allows the programmer to write his rather complex mathematical operations in a language which is familiar to him. Therefore, it makes the generation of the program easy. Secondly, it reduces the amount of memory capacity required to store the program instructions, since the Polish string notation is used. This means that much of the addressing is accomplished with push-down lists, and every instruction need not have an explicit set of addresses associated with it.

The question of computer speed versus memory size is always broached. In the discussions with the programmers the committee was told that they fully expect to use all of the available program memory space; namely, 36,000 words. In the discussions with the hardware people, on the other hand, we were informed that if speed should become a problem, the interpreter, which is quite slow in operation, would be the first thing to be sacrificed; "after all, it principally just saves memory space". These comments, to say the least, are unsettling. It would be to the advantage of all concerned for a sizing and timing estimate to be made on at least a representative set of guidance and control equations to guarantee the computer has the capability to do the job.

#### 7.1.1 Programming Restrictions

Many of the restrictions on the programmer are known only through "convention". Each major mission program is assigned a "rope mother" who bears the ultimate responsibility for coordinating the work of the individual programmers and seeing to it that any restrictions are observed. Considerable reliance is placed on the low



turnover and the high competence of the programming individuals. The idea of a rope mother is certainly useful. However, enough of the fixed rules seem to be in doubt to warrant the generation of a programmer's manual which will document the restrictions imposed by the computer hardware, as well as the system's requirements.

#### 7.1.2 Interrupt Programs

The general philosophy of the interrupt programs was discussed in Paragraph 2.1. The time expended in interrupt routines is important in establishing the capability of the computer to do all of its allotted tasks without omission. The committee was told that interrupt programs were restricted to time durations which are less than 5 to as much as 15 milliseconds. The committee has no way of judging at this time whether such a variation in the maximum interrupt program time is likely to be catastrophic or not. During some mission modes, where the computational rate is low, the longer interrupt programs can undoubtedly be tolerated. The fear is that with no program specification the agreed upon rules may be violated, or the rules may not be appropriate.

Each interrupt program must search for the overflow of the T6 counter and must be prepared to respond to such an overflow. While this is perhaps not a burden to the programmer, it is certainly a necessity with the present logic design. Yet without a formal program control document it is the sort of thing which might be forgotten. There may be other important program restrictions which have not been uncovered by the committee which may not be obeyed by the programmer, such as the recent difficulty with gimbal lock.

#### 7.1.3 Self-Test

The review team was told that the objective of the airborne self-test program is primarily a go/no-go exercise to be used prior to critical mission phases and during idle periods. It is not a diagnostic program, nor is it intended to be, since in-flight repair of the computer is no longer contemplated. The basic philosophy of this program is to test all control pulses and to seek out number sensitivity problems with an exhaustive brute force approach. As a result, this program takes approximately four minutes to run to completion. This is felt inappropriate for an airborne program. Furthermore, the operational use of the program is open to some criticism as well. The self-check program will normally be run as the lowest priority job, or when it is required by the astronaut. It can also be elevated to a higher priority by the astronaut. This is certainly a questionable philosophy. The committee recommends that the self-test program be made smarter. It should take advantage of the foreknowledge of critical information in the arithmetic unit and exercise those worst-case number situations directly rather than depending on the



exhaustive use of all possible numbers. This would permit the self-test program to run to completion in approximately 50 to 100 milliseconds and yet provide the same high level of confidence in the go/no-go indication as the present program provides. This short self-test program should be interspersed throughout the mission program and run automatically. There would be no need for the astronaut to call upon the self-check program. If the computer appears to be behaving erratically and the astronaut has no indication of failure from the self-check program, he should perhaps have available a second program of the exhaustive nature, or perhaps one which will indicate to him more information of a diagnostic nature. This same basic self-test program would probably be a satisfactory one to use during the acceptance tests of the computer.

#### 7.1.4 Restart

The Apollo guidance computer has been designed to recover from transient failures by means of a restart program. The specific restart techniques were not discussed in detail during the design review. The general approach, however, was discussed. Since the restart program has no hardware clues as to the nature of the malfunction which created the restart, the programmer has tried to give himself some clues. About the only thing he has been able to do is to infer whether the problem is in the erasable memory or not. The restart program has a set of 12 memory locations in which six predetermined numbers are stored redundantly. The programmer examines these numbers in the restart sequence and from these numbers infers that the erasable memory is healthy or sick. The number of locations chosen and the relative position of these locations in the memory provides very small confidence that the memory is working satisfactorily. Without considerably greater effort in the investigation of the program, the committee is unable to determine whether the techniques and the specific restart program are adequate or inadequate.

#### 7.2 SIMULATOR (A)

The term simulation generally refers to the operation of a second system in such a way as to simulate the descriptive model of another system. Thus, in the case of the MIT all-digital simulator, the MH1800 is used to simulate the guidance, navigation and control system including the guidance computer.

Simulation is generally used either 1) when the descriptive model of a system is intractable to analysis, or 2) it is desirable to use the simulator as a training or test and checkout device prior to the existence of, or in preference to, the actual system. Its use for analysis has its pitfalls, however, since it provides only a particular solution rather than the general solution which is sometimes desired.

Simulators are used to simulate two basic types of systems: sequential and simultaneous. The digital computer is naturally suited to the simulation of sequential systems (such as the AGC) since it is itself a sequential machine.



An analog computer, which is inherently a simultaneous machine, has the advantage over the general-purpose digital computer in simulating many problems of the physical world (which is by nature simultaneous). Although digital computers have been programmed to simulate such systems, from physical systems to analog computers, this generally has been found to be a formidable task except for the simplest of systems. In addition to the simultaneous/sequential difficulty, in most systems there is the problem of how to simulate what are basically continuous-time functions with a digital computer which is inherently a discrete-time device.

In spite of the difficulties of simulating simultaneous systems and continuous functions, the general-purpose digital computer has a number of significant features which make its use mandatory for most applications: controllable inputs, data and commands; modeling flexibility; high accuracy; repeatability; trouble-shooting aids such as traces and dumps; and hard-copy output. Its use is also mandatory in the simulation of systems which in themselves contain a digital computer.

The hybrid simulation system, in this case the marriage of a digital computer and an analog computer, becomes the obvious next step in the process, making it possible to combine the advantages of each type of computer into an overall simulation system. The hybrid approach has been successfully demonstrated in a number of large scale systems in industry. The MIT/IL hybrid computer approach is discussed briefly in the next section.

#### 7.2.1 Apollo Program Verification

The initial tests on the MIT/IL programs are conducted with an all-digital simulation on the Honeywell 1800 computer. This simulation tool consists of an instruction-by-instruction simulation of the AGC, mathematical simulations of all factors which influence the computations of the AGC; e.g., real time clock, interrupts and counter increments. Environmental factors such as vehicle dynamics, astronaut inputs, accelerometer and gyroscope performance are also simulated in the total model.

The programmer can select those portions of the simulated system which he needs for a particular simulation run; e.g., he may wish to use the AGC and DSKY models only. The framework of the simulator contains features which may be used to evaluate AGC performance and isolate programming faults. Data may be recorded during any part of the simulation for post-processing by other MH1800 programs which the AGC programmer may prepare in MAC compiler language. Since any such simulation may be repeated by supplying identical inputs, anomalous behavior may be studied until a problem is eliminated. Such complete repeatability is not possible with other types of testing. The chief disadvantage of the all-digital simulation is its consumption of computer time. Typically, running time is ten times real time. Also, the fidelity of the environmental simulation is a problem; however, this situation exists to some extent on any test short of the actual flight.



The fact that the Apollo guidance, navigation and control system, with the guidance computer, is in actuality a hybrid system suggests a hybrid computer simulation. Recognizing the limitations of the all-digital simulation of such a complex system, MIT/IL has developed a hybrid computer simulation capability.

Once preliminary checkout of the AGC program has been completed on the all-digital simulation, hybrid simulation may commence. The components of the hybrid simulator are:

1. AGC,
2. Core rope simulator,
3. Beckman analog computer,
4. Three CDU's,
5. Special electrical interface equipment,
6. SDS-930 digital computer (on order),
7. AGC down-link recorder.

The current hybrid simulation configuration uses actual guidance and navigation hardware (Block I) and an analog simulation of the environment operating in real time. With its speed advantage, extensive testing may be performed using a large variety of initial conditions. However, the output of such a simulation is more limited than that of the all-digital one and is usually in the form of strip-chart recordings of selected variables from the analog computer.

Another mode of testing is afforded by the full guidance and navigation system in the laboratory. Using a flight model guidance and navigation system to exercise programs loaded into a core rope simulator is an important mode of testing. In particular, any program which can be meaningfully operated in a one g gravitational field can be tested in this configuration. Such programs include prelaunch operations, manual and display features, free-fall navigation, in-flight IMU alignment, etc. The disadvantages of this mode of testing are the lack of reproducibility, the limited hard-copy output, and, of course, the one g field and rotating earth.

#### 7.2.2 Conclusions

MIT/IL places reliance on the simulation where analytical work is probably called for. For example, the peak interrupts and counter increments should be analyzed to determine the peak loading factors, rather than to rely upon the simulations which, as discussed earlier, provide only the solution to a particular problem rather than the general problem.





### 7.3 FACTORY TEST PROGRAMS (D)

The Block II factory test programs are just now being written and most of the conclusions drawn in this report will have to be based on the Block I-100 programs. This is probably an appropriate procedure since the committee has been informed that the Block II programs will be a minor revision of the Block I-100 programs. In view of the expanded instruction set and the revised logic design of the Block II computers, this certainly appears to be a dangerous approach, but if carried out carefully the dangers can be minimized. It has already been determined, for example, that the adder test carried forward as a worst-case from Block I-100 into the Block II does not provide an appropriate test for the Block II adder. There is some fear that other differences between the two computer designs may be treated similarly.

The principal criticisms of the factory test programs are that, first, they take too long a period of time to run; namely, several minutes. If the committee recommendations for acceptance testing are followed, all of the parts of the computer will not be stressed at each environmental condition (vibration frequency, and temperature). The second criticism is that the programs are not complete without the intervention of the test man to push buttons on the test set and to make measurements of the output signal waveforms. Program-controlled testing of the I/O circuits of a computer such as this is always difficult. Although the general computer testing procedure may be marginal, it is unlikely that the situation can be improved without the expenditure of considerably greater amounts of money on the design and construction of very sophisticated test equipment.

The Final Test Methods document does not make it clear what portions of the program are run during the various tests and does not describe what computer functions are being tested. A new, more definitive document should be created which specifies the testing procedure and describes in detail what functions are being tested at each step of that procedure.

The Block II factory test programs will probably include as one subprogram the flight self-check program. If the self-check program is rewritten to make it a much faster running program, then the inclusion is reasonable. On the other hand, the factory test programs should be more diagnostic in nature than the self-check program. Factory test programs should not only indicate that the computer has malfunctioned, but should provide as much information as possible of a diagnostic nature. This is another instance where hardware clues as to the nature of the malfunction could be used to make the test diagnosticians' task considerably simpler.



## VIII MISCELLANEOUS

### 8.1 COUPLING DATA UNIT (CDU)

The CDU is a piece of flight equipment which is closely associated with the AGC. It contains a 4 volt power supply, some logic modules, and some analog modules. This design review has been limited to those potential problems in the CDU which are similar to problems already discovered in the AGC. Unless a design area is specifically mentioned, the reader should assume that it has not been reviewed.

#### 8.1.1 Logic Circuits (A)

The CDU does not presently use the new expander gate, but accomplishes the additional fan-in by the same "blue nose" circuit which was so troublesome to the computer. The Block II CDU uses these fan-in gates of only two types, as shown in Figure 8-1. Considered as a hogging gate, the blue nose gate is worse than a normal gate due to the additional current drawn by a sneak path diode in series with the paralleled collector resistors to the output.

The worst hogging case is for collector resistors of 2700 ohms with one output grounded, as shown for Case II. With the normal  $V_{IN}$  of 870 mv applied to the blue nose gate the transistor base could draw up to 152  $\mu$ a and the sneak path could draw up to 200  $\mu$ a in addition (assuming a diode drop of 0.6 volts). The total hogging current could then equal 11.5 load units instead of the normal 5 load units. The total load is then  $10 \times 5 + 1 \times 4 + 1 \times 11.5 = 65.5$  units. The source is capable of driving  $25 \times 3 = 75$  load units, hence it is underloaded by about 12.5 percent. The analysis in Appendix C indicates that the noise threshold will be above 65 mv at the temperature extremes in this case.

Another problem caused by use of a regular gate for increasing fan-in is the lack of correlation between collector and base resistors, which results in a higher  $V_{ON}$  voltage and, consequently, a degraded noise threshold. The worst starving case is for a collector resistor of 4150 ohms, which results in a maximum value base resistor of 1900 ohms. This leads to a calculated  $V_{BE}$  of 713 mv. Using this value of  $V_{BE}$ , the  $V_{ON}$  when used as a fan-in gate pulling down a minimum value collector resistor of 2700 ohms is found to be 814 mv. The noise threshold is therefore degraded by  $814 - 770 = 44$  mv, as compared to use of a gate expander for the fan-in gate. However, the underloaded condition of the logic results in correspondingly higher values of  $V_{IN}$ , which is a compensating factor. The value of  $V_{IN}$  was calculated to be 913 mv for Case II, yielding a noise threshold of 99 mv at 25°C. From the analysis in Appendix C, it appears this noise threshold would be degraded to about 40 mv at 0°C and 75°C. By using the gate expander the noise threshold would be increased to 90 mv (F.O. = 4) at these temperatures.





### 8.1.2 Mechanical Design (B)

Although the CDU and the AGC are superficially quite similar, there are some significant differences in their designs. Pressurization of the CDU is accomplished in the tray and the covers are primarily for protection during handling. The covers do not have to contain the pressure and, therefore, are quite simple in their design. In fact, they are flimsy. Since the tray itself contains the pressurization, it is necessary to provide air-tight seals around the Malco pins. This is accomplished by using a silicone rubber potting material for the entire tray. Because the potting material is incompatible with the insulation on the turbo-wrap wire which will be used in the AGC, it is impossible to introduce the new wire into the CDU. Although the density of the wire in the CDU tray is relatively low, the committee doubts that this fact can be relied upon to guarantee there will never be cold flow problems, since these tend to develop long after the initial fabrication. This situation is clearly indeterminate at this time, but it is an area of potential difficulty.

Due, apparently, to the simpler nature of the logic within the CDU, more space was available on those modules than was available on the computer modules. As a result, the CDU modules have guide pins to align the Malco connectors prior to insertion of the modules. This is considered a very desirable feature.

Since the CDU is also magnesium, it has the same materials compatibility problem as the computer. This problem will be solved jointly by the AC, MIT, and Raytheon mechanical designers who are presently working on it.

### 8.1.3 Power Supply (A)

A cursory examination of the +4 volt power supply indicates that it was well designed. Its basic design is such that a malfunction is unlikely to create an overvoltage condition for the micrologic elements. A more detailed analysis of that power supply is not anticipated.

### 8.1.4 Grounding (C)

The CDU case is connected to the spacecraft structure, and the CDU micrologic signal grounds are connected to the 28-volt low side. There can be noise voltages between the logic grounds and the CDU case. These noise voltages were large enough in the AGC to create serious problems and to make it necessary to ground the AGC signal and power lows to the computer structure. Adequate spark tests have apparently not been performed on the CDU to guarantee that the present arrangement is satisfactory. These tests should be made. The nature of the CDU power supply makes it feasible to have the micrologic signal low connected to the CDU case and the 28-volt low isolated from the computer case.



## 8.2 GROUND SUPPORT EQUIPMENT (GSE)

The investigation into the GSE has been pretty superficial. The committee has been primarily concerned with those features of the GSE which might somehow endanger the airborne computer or which have been associated with problems within the computer. Generally, the GSE design seems to be adequate for its intended use with the exceptions noted below.

### 8.2.1 Overvoltage Protection (C)

The GSE (computer test set) presently monitors the input current to the 28 volt supply of the computer and shuts that power supply down if the current level is exceeded. Means are not provided to protect the computer against an overvoltage on the 28 volt input or against the overvoltage conditions mentioned previously in the 4 and 14 volt power supplies. If the computer is provided with the overvoltage protection, then the computer test set need not have this protection. On the other hand, if the computer is not provided with this protection internally, the computer test set must provide it.

At the present time the computer test set has the ability to vary the 4 and 14 volt power supplies within the computer. The range on the 4 volt control is 0.6 to 6.8 volts, which is considered excessive but not dangerous. The range on the 14 volts is 2.2 to 23.6 volts, which is excessive and dangerous. The committee has been informed that the circuit is being redesigned in order to limit the excursion of the power supply voltages. This is certainly highly recommended.

### 8.2.2 Buffer Box (C)

The computer cannot drive the long cables required between itself and the computer test set. As a result a buffer box was introduced between the test set and the computer to amplify the signals. The interface between the buffer box and the computer has recently been redesigned, since the computer circuits were not capable of driving the short cable to the buffer box. The new design has resulted in an overstress condition on the micrologic driving the short cable to the buffer box. The overloaded condition of the micrologic makes that micrologic as susceptible to noise pulses as any other overloaded micrologic. It would be possible to correct this situation by a minor redesign of the buffer circuit. The cable shield could be driven from the emitter of the input stage of the buffer box circuit, thereby largely eliminating the capacitive load on the micrologic element. This would permit decreasing the amount of current which the micrologic has to supply to the interface cable. It would probably then be necessary to provide a second system ground shield over the whole cable bundle in order to prevent noise pickup. If this situation is not corrected the computer interface circuits may not behave properly when the computer is tested at the temperature extremes.



### 8.2.3 Temperature Monitors (B)

Thermal monitors presently exist in the oscillator and in the memory driver modules. These temperature sensitive elements are connected to the test connector but are not utilized in the test set. They should at least be used in the GSE for monitoring the actual internal temperature of the computer. This would provide a means to guarantee that the internal parts of the computer see the worst possible temperature gradients during the acceptance tests.

### 8.2.4 Marginal Testing (C)

The means should be added to the computer test set to provide marginal testing of the computer. Memory drive currents, sense amplifier thresholds, and strobe timing should be adjustable. The means already exist in the voltage control circuits to vary the +4 volts to provide the noise margin measurements. Means should be added to vary the basic clock frequency in order to guarantee adequate timing margins.

## 8.3 MANUFACTURING

During a tour of the manufacturing plant, the general manufacturing and testing facilities were reviewed. In general, this area appears to be highly satisfactory. The screen and burn-in area used for receiving inspection is certainly very elaborate and well equipped. The question of its effectiveness has already been discussed in Section IV.

### 8.3.1 Selection of Nominals (A)

In the build-up of several of the computer modules certain "nominal" values are selected in order to make the circuit work. This technique requires that a group of parts be supplied to the person building up the unit. Questions that arise in this area are concerned with the criteria being used for the selection of the nominals and the control of the piece parts which are not used. The circuits are most often tested at room temperature, presumably using criteria which will guarantee that the design is adequate at the temperature extremes. The review has not been complete enough in several of these areas to indicate whether this is a satisfactory procedure or not. In the case of one resistor value in the A circuit of the interface module, it has been determined that the range of nominals is inadequate to account for the range of parameters of associated components of the circuit which are presumably not selected.





### 8.3.2 Hand Tools (B)

Two problems were noted with regard to the use of tools in the factory. Sharp tweezers and long-nosed pliers were being used to handle piece parts and to bend wires. Numerous examples of nicked insulation were found when the modules were examined. During a subsequent discussion, the tool control procedure was described. This procedure is adequate as it was described, but apparently has not been fully implemented. It should be, and the use of the sharp tweezers and pliers should be stopped.

It was also noted that a Bendix "poke home" tool was being used to insert wires into the GSE connectors. This is a tool which has been outlawed for some time at AC. The tool is designed in such a way that it can split the pin and push the separated parts close to adjacent pins. A new tool has been designed by AC. That design should be made available to Raytheon.

### 8.3.3 Welding to Multilayer Boards (D)

Manufacturing personnel are having problems with parallel-gap welding the micro-logic leads to the multilayer board pads. The multilayer pads are made of a three-part material known as "alnifer". This is a laminate of aluminum, nickel, and iron. There are two problems with the alnifer. The first is that the heat of welding causes the softer aluminum to splatter and form little balls. There is some fear that these balls might short to other pads on the circuit board. This problem has gotten considerable attention recently, and the manufacturing people hope that gold plating the surface of the circuit boards will solve the problem. Another solution to the problem would be to allow Raytheon to use the signal layer interconnection technique which is natural to them. Since the signal layers are made of nickel material there could be no problem with the aluminum balls.

The second alnifer problem has to do with the lack of control of the relative quantities of the three metals in the laminate. It has been very difficult for the process engineers to set up weld schedules which will work for the variety of alnifers delivered to date. This will probably continue to be a serious problem. Receiving inspection tests are required on each lot of circuit boards to test their weldability. The problem is recognized at Raytheon and the solution can be easily implemented.

## IX COMMENT BY MIT ON COMMITTEE FINDINGS

This section was written by MIT who were permitted to examine the final results before publication and were allowed this section for their comments. It summarizes some of the more important exceptions which MIT makes with respect to the judgments and conclusions of the Design Review Committee.

At the outset it is to be noted that MIT agrees fully with much the committee has reported. And on the other hand, much of the disagreement stems from an honest difference of professional opinion, and much stems from practical limitations in information which the committee obtained and was able to evaluate. It is recognized that the computer under examination is a tremendously complex instrument and by no means subject to completely accurate review in a short span of time. The committee did a Herculean effort in its examination and likewise we feel it was vigorously supported by Raytheon and MIT during the information gathering visits. Although faulty and incomplete communication was unavoidable, MIT has been impressed by the thoroughness in which the examination was pursued in some areas.

As a note of optimism we report that computer 200M was tested for combined temperature, voltage and frequency margins with good results. Computer 200M passed self-check with, for instance,  $\pm 10\%$  frequency change while simultaneously varying the 4-volt supply from 3 to 6 volts and the 14-volt supply from 9 to 16 volts. All of this at  $0^{\circ}\text{C}$  and  $60^{\circ}\text{C}$ , which corresponds to or exceeds the specified upper limit of  $35^{\circ}\text{C}$  for the cold plate and  $65^{\circ}\text{C}$  for the ambient.

## 9.1 DOCUMENTATION

### 9.1.1 General

It is quite true that the required documentation was quite meager during the design. For practical reasons the decisions, the designs, and the documentation proceeded in parallel. As a result, the requirements became documented in several places: Minutes of Implementation Meetings, DD Memos, Raytheon memos, NASA drawings, and ICDs.

Unfortunately, the formal documents that describe the computer were not released at the time of the committee's review. For example, the module and computer Purchase Specifications, the qualification testing and maintenance and repair manuals were not available. Most of these have since been released.

### 9.1.2 Interface Control Documents (ICD's)

In the ICDs it is admitted that errors, misprints, and incomplete areas have been found. These have been rectified as they are realized or when the information is available. When a serious incompatibility has been realized, it has been corrected.

There are areas where possible problems could exist. For example, as pointed out (Section 2.9.1), there is a mismatch between the LEM landing radar interface and the computer. Analysis and simulations have been carried out at MIT and Grumman and there is no reason to justify a design change. This situation is being watched and NASA is aware of it.

It is a fact that MIT signed ICDs with only the circuits on the computer side of the interface shown. The spacecraft circuits were just not available. However, we felt that we were covered by the written specifications, and the ICD as it existed allowed us to release drawings for manufacturing. Wherever any important gap was noticed it was called out in a letter accompanying the ICD.

The discrepancy noted in section 6.4 between the computer weight on the LEM and that on the command module is known by all concerned. MIT has not signed the LEM weight ICD because of this; NASA signed for MIT.

Additional remarks on the ICDs are contained in 9.3.7, the Interface Section, and 9.3.9, the Overall Mechanical Section.

## 9.2 TESTING AND QUALIFICATION

### 9.2.1 Parts

Several opinions and recommendations put forth in Section 4 of the report are not in keeping with the goal of the Apollo mission. For example, the comment that "The lot acceptance criteria should be revised to allow higher failure rates," does not reflect the mean time before failure required by the parts in the computer. It has been shown that the percent failures and failure modes generated during screen and burn-in are directly related to field failure rates. It has been further determined that all integrated circuit field failures in computers came from lots which did not meet the lot acceptance criteria.

The comment by the committee that the "percentages [of the flight spec] are considered by industry to be exceptionally tight", appears to be in contradiction to their admission that the integrated circuit SCD 1006321 can meet the flight processing specification. It should be noted that integrated circuits are more complicated than transistors and diodes and the flight processing specification applied to them are naturally tighter than those applied to transistors and diodes.

The goal of the Apollo mission has required that the very best parts be used in the computer. It is therefore reasonable that some firms in industry consider the specification tight.

In the summary, the committee states that, "the flight processing does not seem to be accomplishing what it was intended to accomplish". Their reason for this statement is the fact that waivers must be signed. Many of the reasons for parts not passing the flight spec were only due to documentation requirements of the flight spec; the parts themselves met the criteria. The poor quality of the parts which did not meet the criteria has been generally agreed upon by Raytheon, AC, and MIT.

The committee, which recommends the changes to the flight specs in Section IV, could not agree among themselves on what change would be desirable and states that "those specialists called in by NASA and AC to help Raytheon with these problems have been unable to agree on a recommended change to the system".

The intent of the recommended changes is to increase stress levels because "screening levels appear to be inadequate in that they are not severe enough to screen out all devices which have latent defects". First, no screening exists which will screen out all failures, for all failure modes, for all manufacturers, for all time. Secondly, there is a great danger in increasing stress levels in that failures and weaknesses may be introduced rather than screened.

The committee has recommended that the Nor Gate specification be extended to guarantee 50 mV of noise margin at 0°C and 70°C. MIT agrees. In actual test on the integrated circuits, a guarantee of 80 mV is possible at 0°C and 70°C with virtually no fall out with the existing gates. Since most of the vendors now have a mechanized capability to test at temperature extremes, the added cost by the vendor should be negligible.

The committee also recommended an additional high temperature specification be added to the 1006323 Transistor. MIT also concurs in this change. Added confidence is realized at temperature extremes.

Item 4.3 of the report states that the ND 1002293 is inadequate to screen out defective boards. MIT is concerned about the multilayer boards and originally wrote a tighter flight processing specification but modified the ND in deference to schedule and cost. MIT agrees that a tighter processing specification is desirable and could be phased in to the computer schedule.

Failure reporting should be improved.



### 9.2.2 Modules (Pages 1-7 and 5-5)

The committee is in error on module vibration. The purchase specification of several modules, including the rope memory module, does include vibration and thermal cycling requirements. Preliminary copies of these specifications were provided to the committee by MIT.

We note that no spare module should be installed in a flight or qualification computer except at the factory prior to acceptance testing.

For information on vibration testing of erasable memory, see section 9.3.3.

The committee's recommendations on marginal checking of rope modules (5.2.2.4) are well taken, and should be implemented.

Numerous other specific comments by the committee regarding module testing are out of date with respect to the latest purchase specifications.

### 9.2.3 Computers

In paragraph 5.2.1 the committee states that "the lack of a worst-case design philosophy and the dependence of the computer timing and noise margins on the specific construction of the computer require that great reliance be placed on a thorough acceptance test to guarantee adequate margins". A literal interpretation of this statement leads to the suggestion that some computers designed worst-case do not require a thorough acceptance test, which is a difficult position to defend. Rather, a thorough acceptance test is a requirement regardless of the design philosophy.

(Page 1-6). MIT agrees that there were problems with the computer test program. Since the review, MIT has reviewed the critical SCDs and module and computer purchase specification to ensure that the design levels are maintained and demonstrated as part of sell off. For example, combined temperature, voltage, and frequency margin testing has been written into the computer purchase specification to augment the previous, less demanding, margin tests.

MIT agrees that EMI testing is desirable during computer subsystem testing and has consistently proposed it. In addition, some EMI tests should be added to the computer purchase specification.

Section 7.3 discusses the factory test programs and indicates a disagreement with the procedure utilized to develop an approach for testing the Block II computer; that is, to utilize the same approach as was used in the Block I-100 programs. It was felt the Block II computer is sufficiently similar to the Block I to warrant the same approach of testing the computer. The Block I and Block II computers are basically the same except for instructions, expanded memory, interface changes, and some logic changes. None of these changes justified using a different approach to testing the Block II computer.

Concerning the interest shown in a short time period for factory test programs, we feel the important criterion here should be to check the computer and not how fast it is done. However, the programmed part of the factory test programs that can be run automatically is shorter in Block II because a success indication is made only at the end of the program without pause instead of during parts of the program as it was in Block I. It now takes approximately four minutes to run to completion.

The automatic programmed part of the factory test programs is made up of 60 separate subroutines controlled by placing or omitting 60 separate bits in four erasable registers. Placing a "1" in a bit position allows a particular subroutine to be run as part of the automatic program, while placing a "0" in a bit position eliminates that particular subroutine from the automatic part of the program. Thus any combination of the 60 subroutines may be chosen to run automatically. This adaptability of the automatic programmed part of the factory test method may be utilized when deciding what subroutines should be used during environmental testing (e.g., frequency, and temperature) of the computer.

The point made that human intervention is required by the test procedures is a valid one. However, more sophisticated and expensive test equipment would be required to make the test procedures more automatic.

The Block II Test Methods document will be more descriptive than Block I. Everyone associated with the factory test was in agreement on this point before the Block II factory test procedures were written. There is also a specification section in the Block II Test Methods document.

It is obviously reasonable that the present self-check program should be part of the factory test program. The criterion should be to fully check the computer rather than speed. The cost of inclusion is low.

The point that factory test programs could be more diagnostic is true, though the main purpose of a factory test is to make sure the computer performs all the functions it is built to perform. Factory test programs do have some diagnostic capability, but knowledge of the programs is required as well as quite a bit of manual intervention. We do not feel that a complete step-by-step diagnostic should be built into the factory test program. If a complete diagnostic program is desired, it should be separate from the factory test program.

It is stated in paragraph 7.1.3 that the basic philosophy of self-check is to test all control pulses and to seek out number sensitivity problems with an exhaustive brute force approach. This is true; however, this program also checks the special and central registers, the erasable memory, and the fixed memory, as well as the addressing and sensing logic for these three memories. These three groups of registers are also checked by the brute force approach.

This brute force approach is expensive when time is considered but cheap in regard to number of instructions required to get the job done. At the present time it takes approximately 105 seconds of BLOCK II computer time to completely run through self-check once; if the multiply and divide subroutines are eliminated in flight ropes, as has been recommended, it will take approximately 65 seconds. Following is a list of the computer time required to run through the different parts of self-check as well as the number of instructions in each part.

<u>PART OF SELF-CHECK</u>	<u>APPROXIMATE INSTRUCTIONS</u>	<u>APPROXIMATE TIME</u>
constants, error subroutines and control subroutines	70	
Control pulses	480	30 to 40 MS
special and central registers	60	19.5 seconds
erasable memory	100	7 seconds
fixed memory	140	1 second/bank
arithmetic multiply	55	19
arithmetic divide	105	21.5
	<hr/>	<hr/>
	1010	103 seconds

The decision to use the brute force approach for all of self-check except the "pulses" part was made because of the type of airborne application the computer will be used in. It was felt that 105 or 65 seconds is not an excessively long time because the computer will have much longer periods of light activity while it is airborne. Even during periods of heavy activity, the self-check program continues on from where it was interrupted after a Resume and from where it was left for a new job of a higher priority after that job is completed; thus it does not require 105 or 65 seconds of continuous computer time to run to completion. However, a more important consideration was that a more sophisticated approach would require many more instructions, and space is critical in a flight rope. There would also be a slightly lower level of confidence in the go/no-go ability of self-check if the brute force approach was not used because all 16 possible bit combinations would not have been exercised and every memory register would not have been addressed. The brute force approach also allows the computer to display the sum of each bank on the DSKY at very little cost in number of extra instructions required.

The options of SELF-CHECK, (described in Apollo Report E-1877 for the Block I computer and Digital Development Memo #9 for the Block II computer) depend on the contents of an erasable register called SMODE. One of these options allows the computer to run only the pulses part of the self-check, which takes 30 to 40 milliseconds to run to completion once. It is thus possible to select various options of self-check to run during different phases of the mission, if this is desired. There is no need for the astronaut to call the self-check program unless he feels a necessity to do so.

A second exhaustive diagnostic program would not seem feasible because of the large number of instructions required. At the present time, MIT is considering eliminating the multiply and divide sub-routines of the existing self-check because of lack of space in the flight rope.

The recommended suggestions for a flight self-check in paragraph 7.1.3 do not seem feasible at the present time, mainly because of the large number of instructions that would be required.



### 9.3 DESIGN

#### 9.3.1 "Worst Case" Design Philosophy (Pages 1-7, bottom paragraph, and elsewhere)

The committee finds fault with the design in that it is not "worst case"; i. e., it is possible to have a computer made of parts which fit specifications, but which, due to an unlucky build-up of tolerances or variations from nominals, fails to work. Note that failure to work at "worst-case" refers to the problem of worst distribution of components, not to the problem of a computer made with nominal components which fails to work at its worst specified environment. The latter is clearly a bad design. A "worst case" design is one for which no possible set of parts which meet their individual specifications can fail to work. A good design is one in which the probability of failure due to component tolerance buildup is extremely low, but which saves substantial weight, power or size over the most conservative possible design.

The "worst-case" approach is valuable in mass production because it allows a minimum of rejection in final inspection. To achieve a "worst-case" design, however, it is usually necessary to reduce performance, increase weight, circuit complexity or power consumption, or some combination thereof. In the case of the AGC the value of "worst-case" design, carried to the extremes suggested by the committee, would result in either a larger or slower computer, or one which is late, and not worth the price in MIT's opinion. There are many instances where the worst case is so unlikely that it is simpler to prove in final sell-off that each computer is not an unlucky one than it is to pay a weight penalty or schedule slippage due to a redesign. The burden of proof then rests upon an adequate final test, including operation under extreme condition. The sell-off test which tries each AGC at temperature extremes while simultaneously varying the power supplies and the clock frequency (to

test timing margins) is felt to be an adequate such test. It is inconceivable that such a test should not be used if the computer were designed under "worst-case" rules. The worst that can happen now is that an occasional AGC fail the final test; if the design is basically sound, as is the case, failure will be a very rare occurrence, if it occurs at all.

Finally, the statistical argument against the extreme form of "worst-case" design is as follows:

If one has a circuit with  $N$  parameters, normally distributed and with equal variance  $\sigma$ , one finds that the variance of the ensemble is  $\sqrt{N}\sigma$ . A worst-case design would consider a variance of  $N\sigma$ , that is, a worst on worst set of conditions. Now if this circuit is a computer, a guidance system, or a spacecraft it is not long before one can appreciate the impact of the square root. In addition a worst-case study tends to oversimplify the analysis by generating unrealistic modes and limits and thus imposing additional design margins which even further accentuate the  $N\sigma$ .

#### 9.3.2 Logic (P. 1-7 and 8, 2-21 to 23)

The logic "overloads" in the computer are there as a result of a design decision by MIT for which the loading rules and the 100-millivolt noise margin were regarded as guidelines rather than rigid constraints. In one computer, the seventy-odd "overloaded" signals were measured and found to have DC noise margins from 110 to 240 millivolts. At present, the likelihood of computer malfunction due to the "overloads" appears slight.

Induced noise of the sort predicted in Appendix C can indeed exist. It has been observed in Block I and Block II computers, though its severity

is apparently below the stated levels. There are no known instances of logic malfunction in Block I or Block II owing to this effect, and in Block I the current levels, gate bandwidths and wire lengths are all greater than in Block II. All three of these parameters tend to aggravate the effect.

The timing margin concern (par. 2.4.2) seems overstated in our opinion. In any event, the margin test is a powerful tool for exposing these. The interface circuits are not thoroughly checked under frequency variation, but the interface area is most probably not subject to failure occasioned by small timing changes. However, we concur with the committee's opinion that a C-1 series computer be analyzed for its timing and noise margins. Our experience thus far with multilayer boards has been favorable as far as timing is concerned.

The committee predicts (par. 2.2.4.2) "considerable variation" in the electrical parameters of logic interconnection. Our experience and calculations indicate that the expected variation is a small fraction of the net parameter value.

The committee has possibly underrated the capabilities of the MIT wire-wrap program. The wrap program is sufficiently "smart" to minimize wiring density, avoid obstructions, minimize wire length, limit the number of wraps per post, arrange the wiring to hold down long wires with short ones, and arrange the wiring to minimize the wiring time on the Gardner-Denver wirewrap machine.

### 9.3.3 Erasable Memory

The committee seems misinformed with regards to the problems of AGC erasable memories. For example, "The wide temperature range ferrite

cores are magnetostrictive and must be protected from any stress due to thermal gradients or vibration environments." (par. 2.5.1). The Lithium ferrite cores used in this memory exhibit no change in switching characteristics as a function of temperature between potted and unpotted modules. On the other hand, wide temperature range cores made by magnetically annealing magnesium nickel ferrites are extremely magnetostrictive and are very sensitive to the type of Silicone rubber used in potting. These may be the cores the committee has in mind, but this is not our particular problem.

The "long history of mechanical difficulties" attributed to AGC erasable modules happened in the "constrained" mechanical structures which the committee favors, not in the "unsupported" modules used successfully in both Block I and II and which the committee is so uneasy about. Further discussion, including the latest vibration information, is presented in Section 9.5.

The magnetic and electrical design of erasable memory is faulted because it is not a probable "worst-case" design. Added testing to insure that each stack is guaranteed to work with any possible set of drivers is a good idea. The successful performance of many erasable memories in Block I, over temperature margins, is the best proof of the quality of the basic design.

The erasable memory purchase specification is presently being altered to provide a guarantee of operation over a region of current variability. It is expected that vendor agreement can be obtained for a worst-case difference from nominal of the currents of the order of 6%. This specification will be written with temperature as one of the parameters. The drivers are currently controlled to within 3%, inclusive of temperature. Assuming deltas assigned to the various components for aging

are accurate, the total driver current change due to initial acceptance limits and end-of-life tolerancing will be 5.4%, and the memory will still function.

Degradation of the memory outputs occurs when the memory is written into at high temperature and read out at low temperature: our information (unverified as yet) is that the memory outputs deteriorate by about 20%. The SA threshold is 17 mv, considerably below the worst output which will be approximately 25 mv. The SA will be strobed well after noise outputs have deteriorated to below 10 mv.

Stack testing at Raytheon on the module level: stacks are exercised with drive, selection and sense equipment used in the final system. Stacks are tested using worst initial acceptance level current tolerances. This procedure will be modified to call out worst-case end-of-life currents when the Erasable Memory Procurement Specification is modified.

Some comment has been made about the lack of a common mode noise rejection test on the sense amplifier module. Common mode noise was a serious concern in the initial phases of the design. The current sense amplifier geometry was chosen because of its excellent common mode noise rejection capability. The use of the coupling transformer enhances this quality (by a factor of 30 per Raytheon measurements). The Sense Amplifier geometry is very well controlled by the Sense Amp Specification and Test Procedure. While common mode noise rejection is not routinely measured during the acceptance test, an amplifier which meets all the other tests could not be built different from what the circuit schematic dictates. The addition of more tests to an already complex test would only increase product cost without affecting product quality.

Module test procedures assure a drive current uncertainty of  $\pm 2.7\%$  rather than  $\pm 4.5\%$  stated in 2.5.3.1.

#### 9.3.4 Fixed Memory

With some exceptions, discussed below, MIT agrees with the committee's comments on ropes.

The reason mechanical or temperature shock tests have not been made on ropes (par. 2.6.1) is that no ropes had been available for that purpose, rather than because of oversight. Since the committee's visit, one rope and five dummy ropes have been vibrated on a computer by Raytheon, with inconclusive results. The need for additional such tests is clear and plans are being made to implement them. The Z-axis test (surface normal to the flat plane of the module) has been completed and the rope operated successfully after the test. This test will be repeated with more ropes, to evaluate both ropes and rope-header assemblies. As of this time, no design changes are indicated.

The committee's analysis of the worst-case shuttle noise (par. 2.6.2, Page 2-34) is not completely clear. It seems to err in that peak noise is assumed to occur during strobe time, whereas it occurs about 1  $\mu$ sec earlier. By the time the signal is strobed, the noise amplitude is down to less than 10% of its peak value. Thus changing the core specification to a lower noise value, while generally desirable, does not seem to be necessary.

The committee's point about lack of certainty that a new set of flight ropes will work with a particular computer (para. 2.6.2, page 2-35) is well taken. Rope purchasing specifications will be modified to include current variations from nominal, to cover possible variations in AGC driver electronics.



#### 9.3.5 Power Supply (par. 2.3.1)

The power transient test is not intended to test power dropout. The power interruption item in the ICD's is not "wrong" if adhered to. The separation of the 28-volt return from chassis by an inductor is being studied in an attempt to determine whether it increases or decreases the transient susceptibility in a spacecraft installation. The test points referred to as unbuffered are buffered.

The power supply's switching noise (par. 2.3.2.2 and Pages 1-11) has not interfered with logic circuit operation and is not expected to. In Block I the amplitude is higher with no known malfunction. Thus it does not seem urgent to reduce this noise; nor do we think it as easy to reduce as alleged.

Overvoltage (par. 2.3.2.3) has been caused in Block I in numerous instances by catastrophic failure of the switching transistor induced by short circuit or overload. In Block II, two ring counter malfunctions have brought on overvoltage, but there have been no catastrophic failures of the switching transistor, owing perhaps to the short circuit protection. The likelihood of further ring counter malfunction is low, and the likelihood of overvoltage problems is likewise low.

With respect to the parallel transistors (par. 2.3.2.4), the committee is right; it is not desirable to have these transistors paralleled and not testable. Our recommendation is to add pins to make them testable in order to avoid a new part procurement and qualification program.

#### 9.3.6 Alarms and Logical Design Items

We disagree with the committee's approach to alarm design (par. 2.1.1). Preserving the identity of alarms and attempting to deduce proper action

as a consequence of the kind of alarm is often a chimera. The MIT design started in that direction and evolved towards a more fundamental approach in which action (restart) is standard. The "detection" approach gets very involved in terms of programming and hardware without appreciable benefit.

The committee failed to consider the alarms from the point of view of their effectiveness in terms of the mission. Criticism as to the slow response of certain alarms, for instance, failed to take into account the relatively slow nature of the guidance system as a whole, and the added cost, in terms of equipment, of faster and more sophisticated alarms.

If parity failures in erasable (par. 2.1.1.1) are not allowed to regenerate good parity with bad data it will be very difficult or impossible to restart after such a failure. The point of the restart procedure is that very little data need be preserved, and most of it capable of internal or external checks. If the odds are low on a key erasable word being regenerated incorrectly at a key time, we feel that it is better to attempt a restart than to turn the computer off. The position that such a word, when written back incorrectly, might act properly in the restart cycle and "lead to a dangerous condition," fails to consider the dangerous condition of not restarting at all.

TC Trap (par. 2.1.1.2). This alarm covers the important case of a transfer of control to the accumulator at a time when it contains zero (as might be the case due to a transient).

The present ruptlock alarm (par. 2.1.1.3) is useful and powerful. We are not convinced of the usefulness of one which records unfulfilled requests.

Oscillator Fail (par. 2.1.1.5). If the clock stops intermittently it will, in all likelihood, trigger one of the many alarms because of faulty timing (e.g., memory will malfunction). If a condition can exist when the clock is intermittent but programs are executed correctly (and the only way we can conceive of this is if the clock paused every 24 cycles exactly), the damage will be proportional to the slip in real time: a most unlikely situation. Dowlink will show such a condition within 1 sec. The purpose of the oscillator fail alarm is protection of the memory in power turn on. The alarm sets an inhibit flip-flop.

There is a spacecraft circuit breaker (specified on the power ICD's) operated either by current overload or manually. (par. 2.1.1.6)

The power fail detectors were not designed to detect satisfactory DSKY operation. Their purpose is to protect the erasable memory from power line transients. If the power remains outside of ICD limits, a number of subsystem malfunctions can be expected.

It might be appropriate to extend the 4- and 14-volt alarm limits so as not to cause premature shutdown.

Restart (par. 2.1.1.7). We doubt that knowledge as to the nature of the difficulty can be of help in restarting. The whole restart approach is predicated on:

- 1) that restarts are caused by intermittent failures, power interruptions, etc.
- 2) that all vital programs are dependent on a small amount of information, which is usually stored in duplicate and protected, e.g., position and velocity, and that restarting

will cause some small degradation in performance due to time slippage. Programs are written so that they can fall back to an "arbitrary point rerun" with performance degradation which depends on both the program and the time.

The false counter fail (par. 2.1.1.8) which can occur during restart is an extremely trivial fault, and no change is required. Nor would it be appropriate to execute a restart upon occurrence of a valid counter fail.

The AGC Warning (par. 2.1.11) is specifically designed not to protect against intermittent or transient failures. Its function is to signal a hard failure.

A more elaborate interrupt system would indeed be desirable (par. 2.1.2). The system demands on the AGC have grown considerably since the Block II AGC's inception, without the benefit of a redesign or increased equipment. The T6RUPT condition mentioned in the second paragraph would be more comfortable if there were another level of priority interrupt. The programmers involved, however, claim that the extra scanning burden imposed upon other interrupting routines is minimal.

The standby flip-flop (par. 2.4.5) is connected to a capacitor to steer it to the off state at power turn on, and prevent unwanted transients.

The best standby indicator (par. 2.4.6) would be two lights: one for standby logic indication and one for 4-volt power. (14-volt power affects the DSKY electroluminescent power supply). Short of this, we prefer the present arrangement, for standby mode causes a stop which is only detectable by this indicator if the relays are not actuated.

### 9.3.7 Interfaces

#### 9.3.7.1 Interface Specification and Testing

It has always been a ground rule for the MIT computer group to strive for a commonality of circuits to lead to a minimum number of specifications and components. It is felt that this results in less paper work, simpler testing, fewer misinterpretations, and increased reliability.

We feel it is not practical to test under all the conditions experienced at the interfaces; the test conditions we do have verify that the circuit is built as designed and thus it is known from correlation tests that the ICD conditions are met. There is no reason why the factory tests should change because an ICD load is changed. The review committee appears to agree with this view when they say, "It is unreasonable to design a test for these interface circuits in the factory which will include all possible loads" (Page 6-1) yet they disagree when they say that the circuits should be tested with the actual loads (Page 2-41), "with values of resistance and cable capacitance which the circuit will see in the spacecraft" (Page 5-7) with the actual duty cycles (Page 5-7) and the actual voltages (Page 5-7).

The MIT approach is considered realistic and flexible, recognizing that there are situations when simulated loads are required (such as the hand controller source impedance).

#### 9.3.7.2 Electromagnetic Compatibility

With respect to the second paragraph of Section 5.2.2.3, the computer, as part of the G&N, is required to meet EMI 10A and MIL-I-26600 (Ref. MEI #2015000 Set 3.5.9) to the degree negotiated with the procuring authority.

On the basis of experimental evidence, NASA has approved the computer case to be connected to internal zero volts. The LEM power ICD also limits the G&N in the amount of noise it can insert into the power bus.

With regard to EMI testing (Pages 1-6, 2-18, and 2-40) a preliminary noise susceptibility test was successfully run at GAEC on the LGC (ref. ETR #005 May 4, 1966) and the G&N (ETR #007 May 4, 1966). Tests will also be made for interference when systems are available.

The fact that the effective source impedance of the power bus as seen from the computer is not specified (Page 2-17) should be understandable when one stops to consider all the systems that are connected to it. MIT naturally would desire such information also.

With reference to the possible lack of grounding information (Section 2.9.1), grounding is specified on the computer electrical ICD's for spacecraft wiring.

The same grounding philosophy was used for spacecraft and G&N system cabling for all computer signals. This grounding philosophy is compatible with MIL-I-26600 for high frequency signals.

#### 9.3.7.3 "A" Circuit

This circuit is discussed on Pages 2-41 and in Appendix F. On Page 2-41 the committee says that the design goals are not met at the temperature extremes. The ICD requirements are met over the anticipated temperature extremes ( $10^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ ). The synchronizing input does function reliably.

The analyses contained in Appendix F (which has five items) are oversimplified.



Figure F-3 summarizes (Item 1) the analysis and indicates that at 75°C, 1.17 volts will not turn on the A circuit. In laboratory tests it is possible to turn on the circuit at room temperature with +0.8 volts. At 75°C it should be easier. This leads one to believe that the worst-case values assumed may be unrealistic.

The analysis is oversimplified on two counts: the model for the diode is unrealistic in that it does not allow conduction below .63 volts, while a real diode will conduct for any voltage greater than zero. Secondly, all the circuits under consideration have feedback paths that will hold them on once conduction is started. It takes very little current to turn on this circuit. In addition, the worst-case values for the transistors are high. At room temperature a  $V_{BE}$  of 0.5 to 0.55 volts is enough to supply 10 - 100  $\mu$ a of collector current which is approximately the level used.

The factory test plan (187198) referred to in Item 2 was preliminary and is being replaced by PS 2003067 which was released 5/11/66. The latter allows the pulse width to vary more than 10%, which is the ICD specification. The A circuit will meet the ICD over the expected operational temperature range (10°C - 50°C).

In Item 4, the analysis is oversimplified and suffers from the type of diode model assumed. The average value of R3 on the nine modules (P001-P009) is 900 ohms. If one solves for  $V_{Threshold}$  in the equation in this section, one finds that the threshold is 415 mv. This conflicts with the selection procedure that requires a threshold value of 100 mv. PS 2003067 requires the threshold to be greater than 45 mv at 70°C which is more than adequate to meet the ICD.

There are two conclusions in Item 5 of Appendix F concerning the X circuit.

- 1) The  $1.024 \times 10^6$  cps clock circuit application at nominal values allows more current to flow than the transformer specification allows for.
- 2) A low beta transistor will result in an out-of-specification condition and the waveform shown on sheet F7.

Both conclusions are incorrect. Measurements made at the junction of the 200-ohm resistor and the transformer were 7.0 volts during the on time and 12.5 volts during the off time with a 14-volt B+. These numbers indicate that 35 ma flows through the 200-ohm resistor and of this, 17.5 ma through the load during the on condition. During the off state, the load current will be 10 ma. The output voltage would be 5.5 volts which is close to the 6 volts actually measured across the 100-ohm load. This indicates that one has 35 ma flowing through the transformer in the normal condition, 17.5 ma of which is due to the magnetizing current.

In the SCD for the transformer 1006319, requirement 2.B(9)d, the transformer is tested with a 10  $\mu$ sec period and a 5  $\mu$ sec wide pulse, 13 volts on the collector and a 510-ohm load resistor in order to assure that the transformer will not saturate. The transformer is checked to see that it doesn't saturate with 34 ma flowing through it, at least 22 ma of which is magnetization current. Thus the transformer is tested with a magnetizing current compatible with the circuit application, and no change should be required of the SCD.

The analysis of the effect of a low beta unit is incorrect in that the transistor will not turn off and generate a shortened waveform, but will increase its saturation voltage and reduce its output.

When the collector current is reduced to 28 ma, it can be shown that the waveform shown on sheet F7 cannot exist, and the signal will be within specification.

#### 9.3.8 Displays and Keyboard (DSKY) (par. 3.1 and further)

##### EL's (3.1)

The recommendation of the committee to use filamentary type indicators (Pages 1.9 and 4.7) does not appear to be justified for the following reasons:

Available filamentary type bulbs for segmented displays require at least 250 mw (depending upon the intensity) per segment. If one multiplies this by the number of segments presently on the DSKY, one could dissipate up to 40 watts (as opposed to .6 watts for the present design), which means approximately 8 Amperes out of the 5-volt variable supply. MIT has been required to remove 3 incandescent status lights from the DSKY because the 5-volt power supply in the LEM does not have sufficient capacity and could not handle the lamp test currents (0.6 amps).

The main problem with the present EL's is the moisture seal. The EL's should last for at least a year with in-spec legibility, based on past experience, provided moisture and sunlight exposure is controlled. The seriousness of the EL problem is not clear at this time.

Relay (par. 4.7) There is a quality problem - one vendor has been removed and a new one is being evaluated.

Switch (10010901-2). Difficulties experienced in Block I/100 will not be repeated in Block II because the switch inputs to the computer are filtered and the computer will not see contact bounce.

Indicator Driver Module (par. 3.1.1). This problem is under analysis. Evaluations to date are not felt to be accurate. The temperature of 160°F for the DSKY mounting is incorrect. Values have been requested from NAA and GAEC for the thermal ICDs.

#### 9.3.9 Overall Computer Design (Mechanical)

Interface Control Documents in the mechanical area have historically been treated by NAA, GAEC, and MIT engineers as describing the normal interface dimensions agreed to be present at installation of the equipment. Package-to-package clearances under all environmental conditions as well as shifts in these nominals resulting from manufacturing tolerance stack ups can only be analyzed and allowed for by vehicle contractors. If NASA desires refinement in these ICD's to cover these environmental changes, the already established IRN procedure will be used to make the necessary changes. Such IRN's are already updating the direction material changes in a computer case.

The Thermal Design (par. 2.2.3) of the computer is adequate based on MIT's experiments and analysis.

The Structural Design (par. 2.2.1) has been analytically determined to be adequate and all testing to date has supported this analysis. The computer design for Block II has been consistently proposed as a sealed pressure vessel. It is the judgment of MIT that this is the best moisture-proofing mechanism for a unit with this number of connectors. Although previously explored early in the design, a re-study of a pressure relief valve vs. weight and reliability could be accomplished. Such a device could be placed in the now unused oscillator tuning boss already on the computer. It is not felt to be a necessary change but one that could be easily implemented.

Vibration tests are continuing at this time. The rope header assembly (par. 1.6) needs further test confirmation. No changes in this area are deemed necessary at this time. However, it is felt that since this is a new approach to rope replacement, more testing is desirable to evaluate the design.

Pluggable module design. All external pluggable modules, ropes, rope-header assemblies, and input/output connectors are gasket sealed for moisture security. Pin guards, and keying are provided. As internal (inside pressure wall) replacement of modules is only a factory-level activity by experienced competent personnel, no mechanical guides or pin protectors are provided, to save weight and volume.

#### 9.3.10 CDU

The report states (par. 8.1.4) that the nature of the CDU power supply makes it feasible to connect logic 4-volt low to the chassis and have the 28-volt low isolated from the chassis. This is true of the power supply, but the remainder of the CDU circuitry requires that 4-volt low be connected to the 28-volt low. The micrologic drives analog switches which use the 28-volt supply.

#### 9.4 PROGRAMMING

Paragraph 6.5, relating to the lack of an official programming memo cannot be faulted. There are several documents not mentioned in the above paragraph which make an ineffective substitute for a programmers' manual. The generation of such a document is currently underway. We intend to begin a series of lectures on programming, and to generate a programmers' manual for Block I and Block II.

With regard to section 7.1, design of programs often does involve a judgment of speed vs. storage optimization. It has been quite clear for several years now that the interpreter is essential if we are to produce a total AGC program which can meet MSC requirements. It is true that the interpreter is "sacrificed" in programs requiring extremely fast computation, if that word means that it is not used in these circumstances. The interpreter could never be "sacrificed" if the word implies deletion from the systems program section of a flight rope. It is hard to believe that this was even suggested by anyone intimate with the total design of the guidance computer. Sizing the timing estimates are continuously made and updated by the responsible engineer in each section of AGC programming. For example, in the digital autopilots these parameters dominate the design.

In terms of total mission programs, it has been difficult to make total size estimates of memory requirements for the lunar mission because many of the requirements were not defined.

Planning in terms of mission requirements is lately coming into focus. It is clear that available program memory is likely to be a serious constraint, along with flight schedules, on the total mission capability of the computer.



The caution restrictions and conventions described in section 7.1.2 will be documented in the programming manuals.

The programming manuals referenced in section 7.1.4, currently under preparation, will contain more detailed information regarding restart. At the time they are available, the committee may, if they desire, make a judgment concerning the worthiness of these techniques.

Concerning the digital simulator (sec. 7.2.2), the process of determining the best mix of tools in the design of AGC programs is best left to the designer. It is MIT's opinion that the all-digital simulator as developed at MIT is useful and important for this purpose to give some confidence to analytical results.

## 9.5 ERASABLE MEMORY MECHANICAL DESIGN

### 9.5.1 Summary

The erasable memory mechanical design for the Block II computer has been evolved out of a necessity to contain the ferrite cores in a medium that will not apply excessive pressure to the cores (because the cores might break) during thermal cycling, and not apply stress to the wiring during curing and vibration. The only medium found suitable for this is silastic potting compound, which has a volumetric expansion coefficient approximately one order of magnitude higher than the supporting hardware. It was found to be impossible to restrain the silastic, and therefore, the memory was designed to allow the silastic to move, but to let the pins and wiring move with it.

Memories and stacks have successfully withstood vibration at up to 21g rms swept sine, and vibration at 5.2 dB above the LEM launch and boost specification for 60 min, and 5.2 dB for 40 min plus 18 min at 8.2 dB above specification. Thermal cycling between  $-55^{\circ}\text{C}$  and  $+105^{\circ}\text{C}$  has not caused failure. While it is not possible to say categorically that the memory will not fail from wire fatigue, since no fatigue time/energy spectrum has been evolved, it is felt that a considerable safety factor has been demonstrated.

While a non-rigidly supported stack is an innovation, it is the result of lengthy design evaluation testing and has so far been demonstrated to be an acceptable engineering solution to the design problems inherent in this unit. All attempts to design a rigidly restrained stack have to date resulted in environmental test failures.

### 9.5.2 Detailed Discussion

#### BLOCK I

The Block I cross-section configuration is shown in Figure I. It consists of a 16,384 core stack with 16 sense lines, 16 inhibit lines,

and 64 drive lines. All lines are terminated at Malco pins, with the exception of one end of the drive lines, which are terminated at feed through pins (5), these are connected to a diode decoding assembly (6), this in turn is connected to other Malco pins. Original design modules were tested by temperature cycling at  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  5 cycles, 50g 11 msec shock, 2 shocks each way each axis and 7g rms shock sine vibration. Open lines were found after completion of vibration in the Y axis. (See Fig. 2 for axis locations.) Examination shows that no stress relief has been provided for the wires and the breaks had occurred at Malco pins at the interface between the wire and the solder. (Fig. 3) To give maximum relief from this condition, three changes were made:

- 1) A minimum of  $1\frac{1}{2}$  turns of wire around the pins were left as stress relief
- 2) The solder joint was made approximately  $\frac{1}{2}$ " from the header to reduce the differential movement between the pins and silastic.
- 3) Approximately  $\frac{1}{8}$ " height of epoxy applied to the base of the Malco pins, to dampen the pin vibration.

With these modifications, Block I memory went into production. A total 40 memories were built to this design. All core stack assemblies less diodes and epoxy encapsulation were temperature shocked and vibrated at incoming inspection. A total of two failures occurred, both traceable to faulty workmanship. The first was a memory built by a second source supplier and had no wire stress relief; the second was vibrated before the silastic was properly cured. The only trouble occurring in production was parting of the epoxy encapsulation from the header during thermal cycling. No further wire or core problems occurred.

## BLOCK II

The erasable memory for Block II had double the memory capacity of Block I (32,768 cores, 16 inhibits, and 96 drive lines). The stack layout and general termination scheme were retained from Block I. In order to obtain the volume required for the increased number of cores, the height of the stack was increased and the header was changed to a "dish" cross section, Fig. 4. The pins in the feed through plate Fig. 4 Item 7 were modified to take the stack terminations outside the board. It was decided to "box in" the core stack silastic array to support the silastic stack mechanically. Epoxy glass side plates were added (Fig. 4 Items 2 & 3) fitting into grooves in the header and feed through plate. Wires were fed through these plates and soldered to pins (Item 7), these pins were then encapsulated in epoxy. Although silastic has an order of magnitude higher coefficient of expansion than the rest of the components in the system, it is also compressible, and it was felt that the silastic would be contained.

The first core stack assembly built was tested without diode assembly or cover. (Items 8 & 9) During thermal cycling, cracking occurred at line AA, and Malco pins were sheared along the crack line due to silastic expansion. The memory was operable after cycling, and subsequently passed 50g, 11 msec shock and 10g swept sine vibration in 3 axis.

A two-pronged fix was investigated: a) alternate materials to silastic were unsuccessfully sought and b) an "expansion chamber" built in (see Fig. 5). Again the core stack was successfully thermal cycled and vibrated at 7g rms swept sine. Two memories were completed, and both successfully passed thermal cycling, shock and vibration (swept sine). One memory was then recycled through swept sine, and again passed successfully. The two memories were then subjected to random vibration, the spectrum being:

10-80 cps 3 dB/octave  
80-950 cps  $.15g^2/cps$   
950-1200 cps 12 dB/octave  
1200-2000 cps  $.05g^2/cps$

Total RMS acceleration 14.1 g RMS

Both memories passed 20 minutes vibration in the X and Y axis, but one memory failed after 5 minutes in the Z axis, and the second after 10 minutes in the Z axis. Examination showed that Z termination wires in each had sheared at the side-board/silastic interface, obviously due to the expansion chamber allowing the silastic to move relative to the side plates.

Meanwhile, tests made with alternate materials uncovered only one material that would allow the ferrites to function between  $-20^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$ , and yet have a better thermal expansion coefficient, and a greater rigidity than silastic. This was solid urethane encapsulant. However, at this time the material was new, and large batch-to-batch variations were found, and it was felt that the material was not sufficiently in control to be used.

#### PRESENT DESIGN

At this point all the design data and decisions were reviewed. Silastic was still the only medium found satisfactory for encapsulating the ferrite cores, but its expansion-compression characteristics had proven to be such that it could not be confined. Therefore, the design had to be such that the silastic be allowed to "move" during thermal cycling, yet the silastic not move relative to the pins throughout environmental test. Since the silastic could not be restrained, the pins must move with the silastic. This, of course, brings us full circle back to Block I design, or a modification of it. Block I had not been proven weak under vibration, but had been assumed so on paper. Accordingly, two Block I memories were subjected to random vibration (spectrum, as before) and passed 20 minutes in each axis.

It was therefore decided to change the design of the Block II memory to incorporate all stack wiring and solder joints inside the silastic. Analysis of the memories already built showed that the height provided for the stack could be reduced by .100 inches, providing that the feed through plate assembly pins were outside the core stack area. Accordingly the Mod. II design, the present design, was originated. (See Fig. 6).

To expedite testing, a simulated memory was made consisting of the designed hardware, but wires which were soldered to the pins were not part of a core stack. Reject core mats were encapsulated with the wires to give an inertia similar to a true memory. For test results, see Fig. 7.

To date, three real memories have been tested. The first was tested as a core stack - no diode assembly or epoxy encapsulation. It was tested to PS2003109, for -55 to +105°C temperature cycling, 50g 11 msec shock, 7g rms swept sine vibration. No failures.

The second memory was also tested as a core stack and was subjected to swept sine vibration. (.12 inches max. excursion, swept at 2 min/octave, 5-2000 cps, approximately 10 min. per run). Initial testing was a 7g rms in each axis, then 11.5, 14, 17.5 and 21g rms in the X axis. Finally it was run at 14 and 21g rms in the Y and Z axis. No failures occurred.

After thermal cycling and mechanical shock testing per PA2003111, the third memory was assembled as a complete module and was subjected to random vibration. (For results, see Fig. 7)



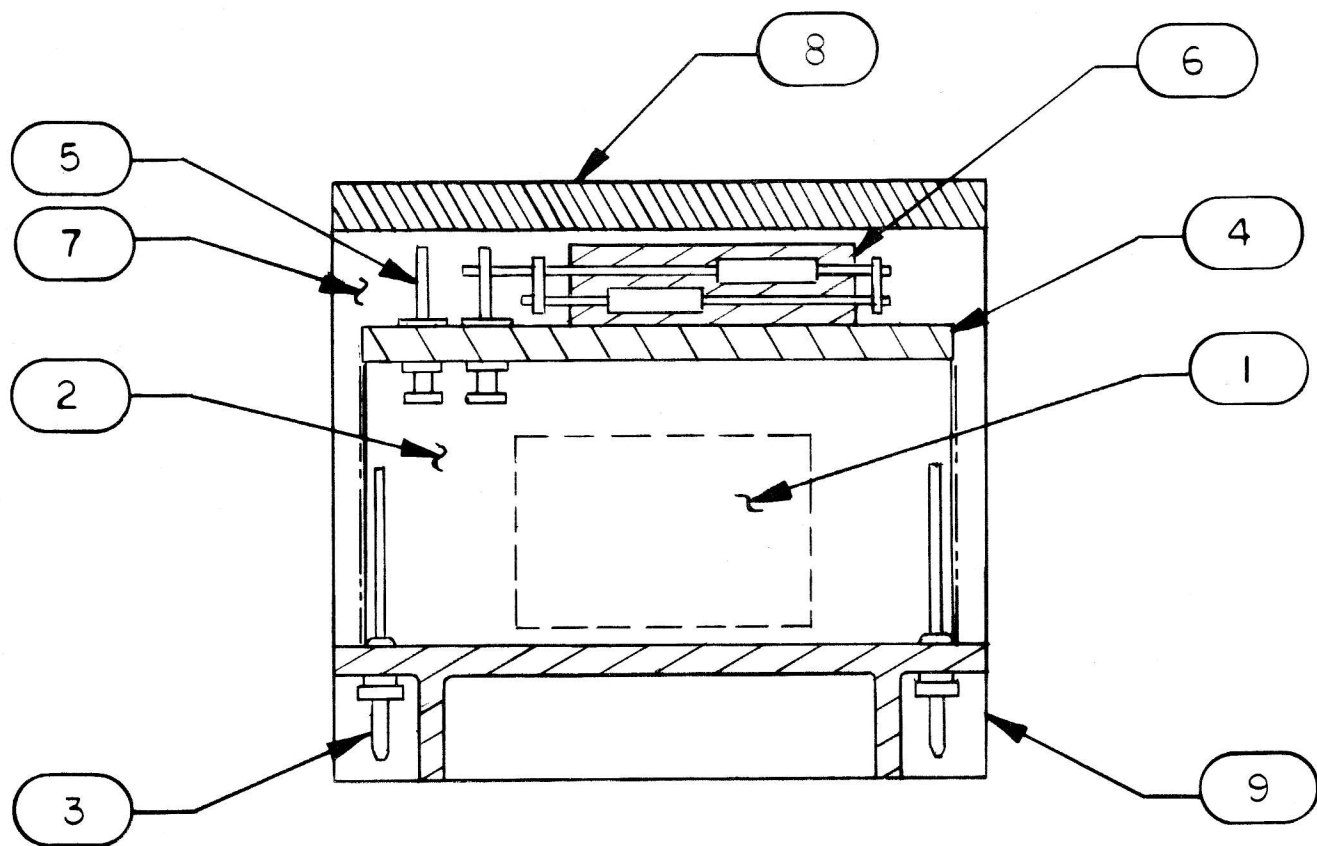


FIG: 1

1. CORE STACK
2. SILASTIC ENCAPSULATION
3. MALCO PINS
4. GLASS EPOXY BOARD
5. FEED THRU PINS
6. DIODE DECODING ASSEMBLY
7. FILLED EPOXY ENCAPSULATION
8. METAL TOP COVER
9. HEADER

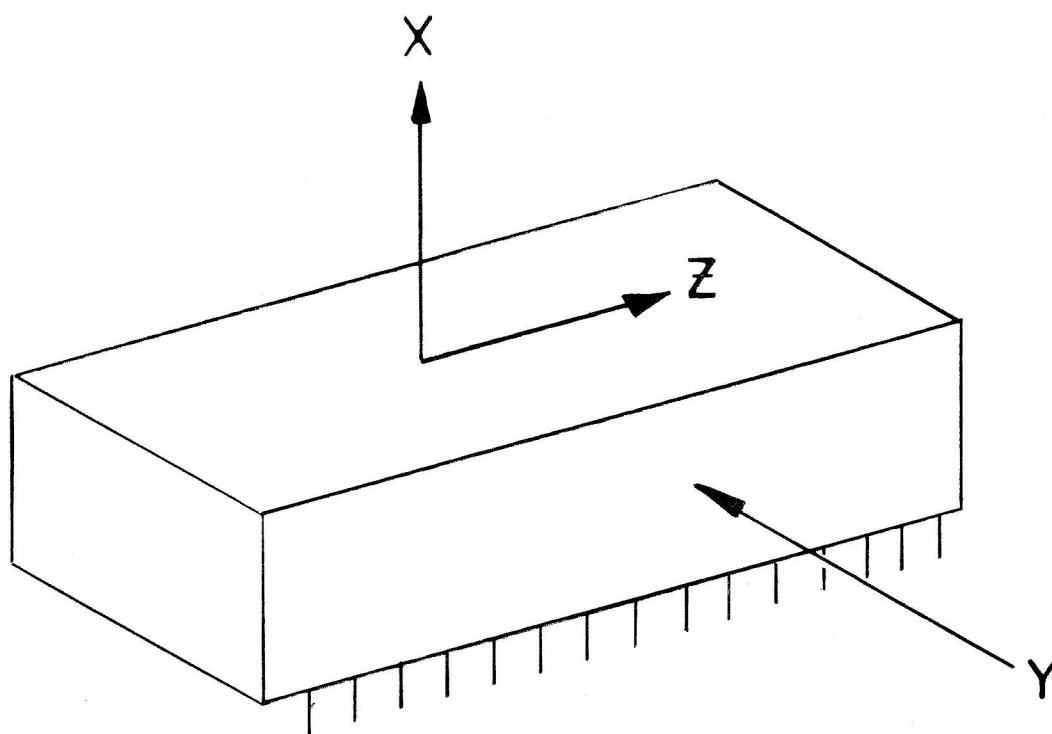
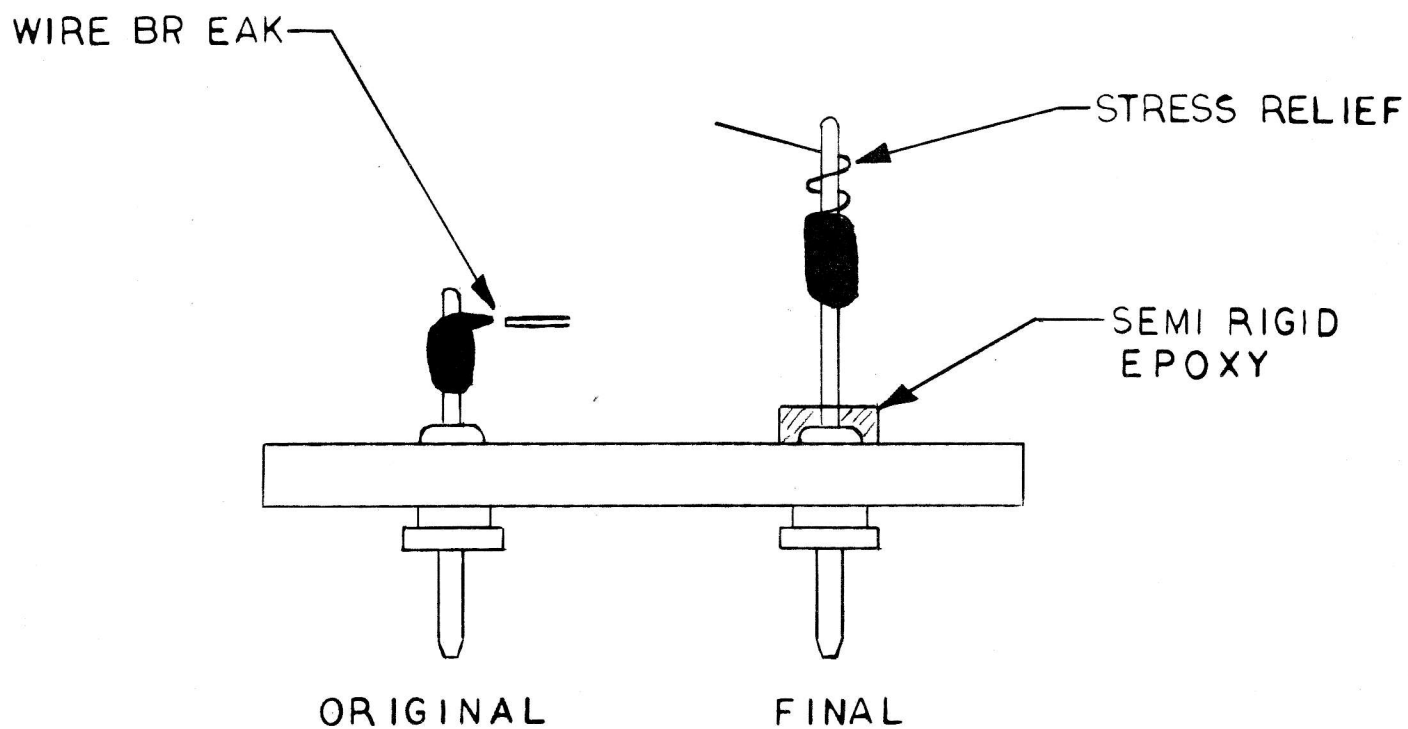
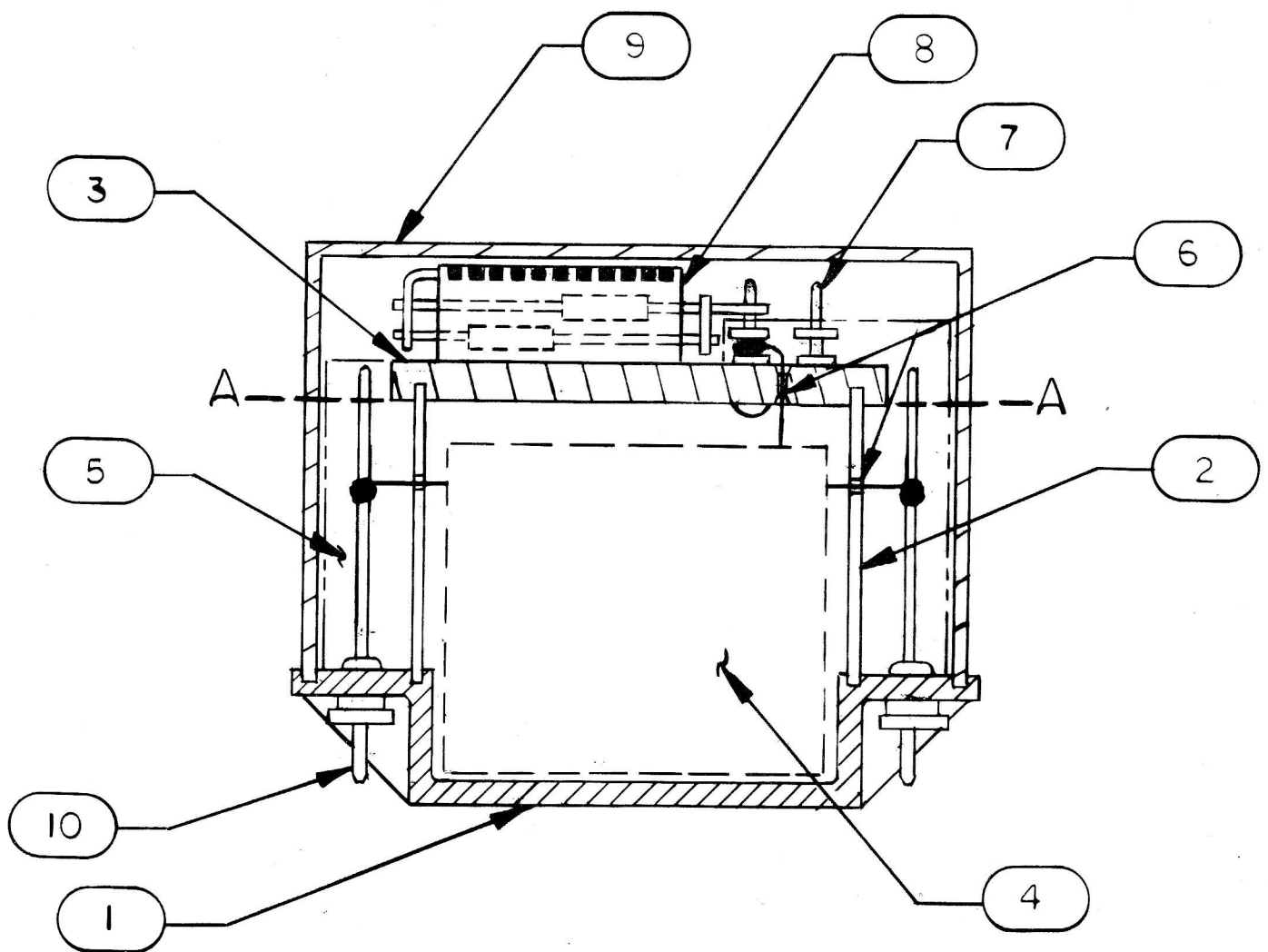


FIG: 2  
VIBRATION AXES



PIN TERMINATION METHOD  
FIG: 3



**FIG: 4**  
**BLOCK II DESIGN; ORIGINAL**

1. HEADER
2. EPOXY GLASS SIDE PLATES
3. EPOXY GLASS FEED THRU PLATE
4. CORE STACK, SILASTIC ENCAPSULATED
5. EPOXY ENCAPSULATION (DASH LINE INDICATES  
 POTTING AT CORE STACK ASSEMBLY STAGE)
6. CORE STACK TERMINATIONS FEED THRU .010 DIA HOLES
7. FEED THRU PLATE PINS
8. DIODE ASSEMBLY
9. COVER
10. MALCO PINS

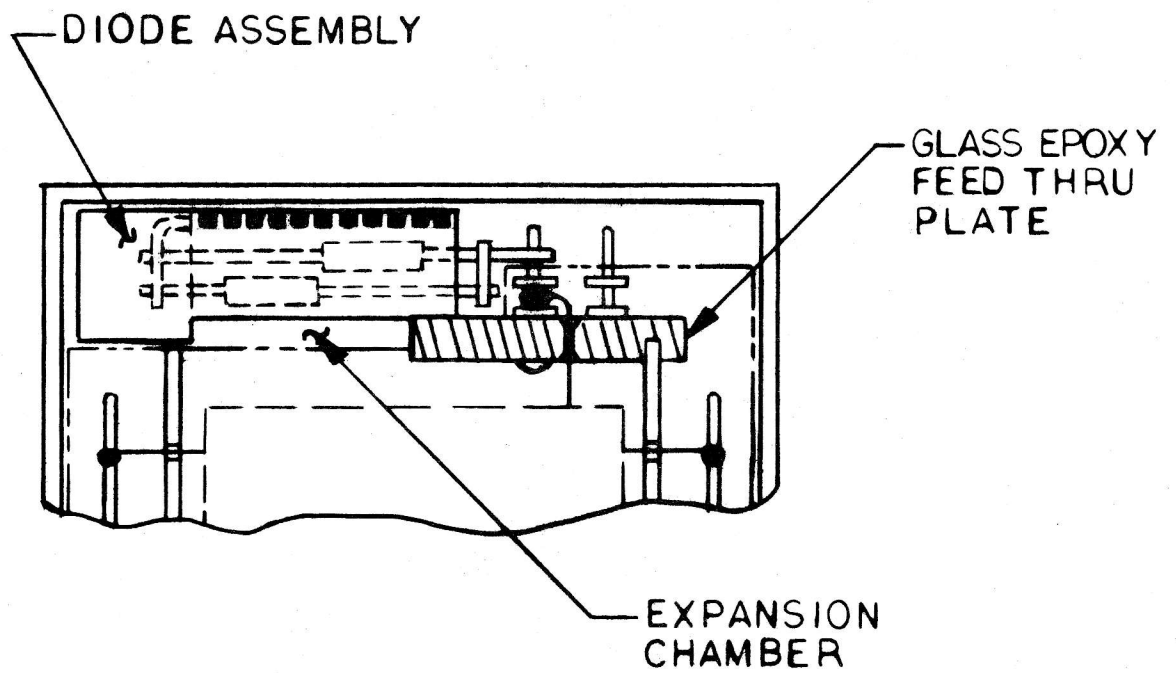
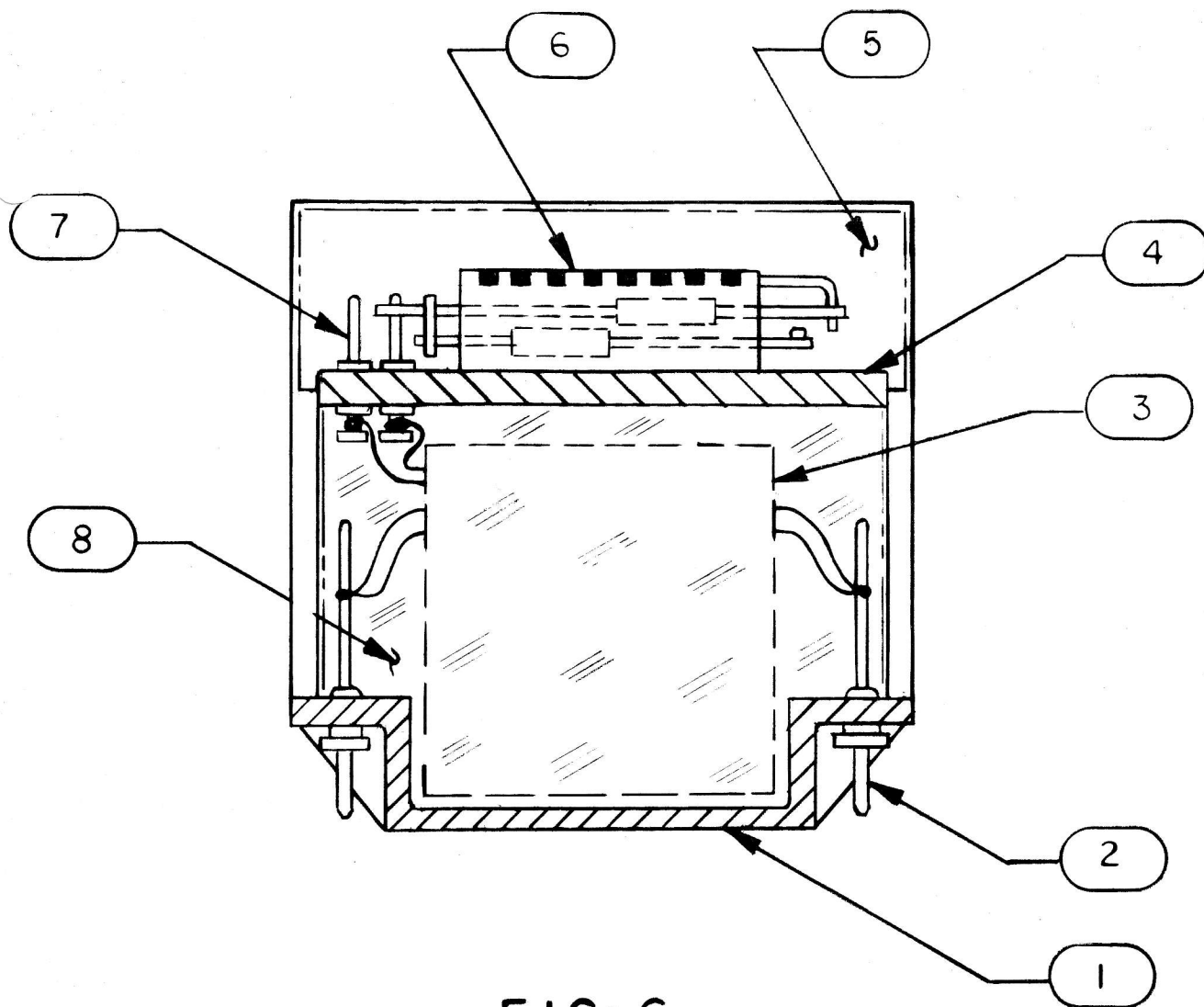


FIG: 5  
BLOCK II DESIGN; MOD I



**FIG: 6**  
**BLOCK II, PRESENT DESIGN**

- 1. HEADER
- 2. MALCO PINS
- 3. CORE STACK
- 4. FEED THRU PLATE
- 5. EPOXY ENCAPSULATION
- 6. DIODE ASSEMBLY
- 7. FEED THRU PINS
- 8. SILASTIC ENCAPSULATION

FOR MORE DETAILED PRESENTATION REFER  
 TO DRAWINGS 2003109 AND 2003111



FIGURE 7

## VIBRATION SPECTRUM

UNIT  
TESTEDSIMULATED  
MEMORYERASABLE  
MEMORY  
MODULE  
PER 2003111R. M. S.  
g.  
Equ't

1. 10-20 c/s at + 12db/octave 20-50 c/s at + 6db/octave 100-950 c/s at .15g <sup>2</sup> /cps 950-1200 c/s at -12db/octave 1200-2000 c/s at .05g <sup>2</sup> /cps (See Note 1)	14.1	x axis 20 mins y axis 20 mins z axis 20 mins OK	x axis 6 mins y axis 6 mins z axis 6 mins OK
2. 10-80c/s at +3db/octave 80-2000 c/s at 0.15g <sup>2</sup> /cps	17.1	x, y, z axis 6 mins OK	
3. 10-80c/s at + 3db/octave 80-2000 c/s at 0.24 g <sup>2</sup> /cps	21.8	z, y, z axis 6 mins OK	
4. 1000-2000 c/s at 2.0g <sup>2</sup> /cps	45.5	x axis 6 mins OK z axis 6 mins OK y axis 5 mins*	
5. 400-1000 cps at 0.55g <sup>2</sup> /cps	18.6	SEE NOTE 3 y axis 3 mins**	
6. Profile 1. Increased by 3db (See Note 2)	17.1		x, y, z axis 6 mins OK
7. Profile 1.			y axis, 25 mins OK

\* A Momentary open, 1.E longer than 1 microsecond, occurred after approximately 5 mins.

\*\* 2 lines opened after 3 mins

Note 1 This is the LEM Launch and boost vibration specification per Grumman ICD  
# LIS-520-10001 with the power raised by 5.2db.

Note 2 This is the ICD #LIS-520-10001 with power raised by 8.2db.

Note 3 The level of input and spectral density is so severe that this may be considered  
destructive testing to demonstrate safety factors.

## 9.6 MIT PROPOSED ACTION

The following is a summarized listing of the various actions proposed by MIT.

### 9.6.1 Logic Circuits and Design

#### a) NOR Gate SCD

To test at 0°C and 70°C and a test to detect base-to-base shorts.

#### b) Computer P.S.

Measure one level of overloaded signals as part of P.S.

#### c) Module P.S.

More complete test at module level to detect high impedance shorts.

#### d) Multilayer Boards

1. Tighter processing spec to include DITMCO tests at high and low temperature.
2. Second source.
3. Continued investigation of quality and weldability.

### 9.6.2 Power Supply

#### a) Provide test for parallel transistors.

#### b) Over voltage protection in GSE.

### 9.6.3 Interfaces

Transistor SCD

Add high temperature  $I_{CEX}$ .

### 9.6.4 Erasable Memory

#### a) Core Stack P.S.

Change to vary currents of drivers.

- b) Memory Module P.S.

Test using end-of-life currents.

#### 9.6.5 Rope Memory

- a) Rope P.S.
  - 1. Implement vibration testing
  - 2. Introduce current margins at module testing.
- b) Core SCD
- c) Correct this SCD

#### 9.6.6 Oscillator

- a) Change variable choke to a nominal selection.

#### 9.6.7 Alarms

Study function of voltage alarms.

#### 9.6.8 Mechanical

- a) Implement "Black Box" maintenance.
- b) Weight trade-off study on pressure relief valve versus increased weight for structure.
- c) Engineering vibration complete with rope header and ropes well instrumented.
- d) Add dummy rope module for protection of pins. (Rope jumper module may be sufficient.)
- e) Return to Aluminum computer case.

#### 9.6.9 Computer P.S.

MIT is assuming that the tests we have requested are in the P.S.

- a) Study more automated testing.
- b) Continue to review the P.S.
- c) EMI testing.

#### 9.6.10 Qualification Testing

The procedures and plans are being changed and are subject to the changing constraints. An example is the situation on system qualification and the fact that module qualifications are no longer planned. An EMI test should be added.





APPENDIX A

AGC POWER SUPPLY

L. Keranen





Figure A-1 gives a simplified diagram of the main elements of the switching regulator. Consider its operation when L1 is conducting current continuously. When Q12 is on,

$$\begin{aligned} V_{A(ON)} &= V_{IN} - V_{CR10} - I_{IN} (R_{L3} + R_{L2}) - V_{CE(ON)} \\ &\cong V_{IN} - V_{CR10} - V_{CE(ON)} \end{aligned}$$

When Q12 is off

$$V_{A(OFF)} = -V_{CR6}$$

So long as L1 conducts continuously,

$$\begin{aligned} V_{OUT} &= V_A \text{ (average)} - I_{OUT} (R_{L1} + 0.12) \\ &\cong V_A \text{ (average)} = V_{A(ON)} \zeta + V_{A(OFF)} (1 - \zeta) \end{aligned}$$

where  $\zeta$  is the fraction of the time Q12 is on.

Thus,

$$V_{OUT} \cong (V_{IN} - V_{CR10} - V_{CE(ON)}) \zeta - V_{CR6} (1 - \zeta)$$

$$\zeta \cong \frac{V_{OUT} + V_{CR6}}{V_{IN} - V_{CR10} + V_{CR6} - V_{CE(ON)}}$$

When

$$V_{OUT} = 14.0 \text{ volts}$$

$$V_{CE(ON)} = 1.0 \text{ volt}$$

$$V_{IN} = 28.0 \text{ volts}$$

$$V_{CR6} = V_{CR10} = 0.6 \text{ volt}$$

$$\zeta \cong \frac{14.0 + 0.6}{28.0 - 0.6 + 0.6 - 1.0} = .541$$

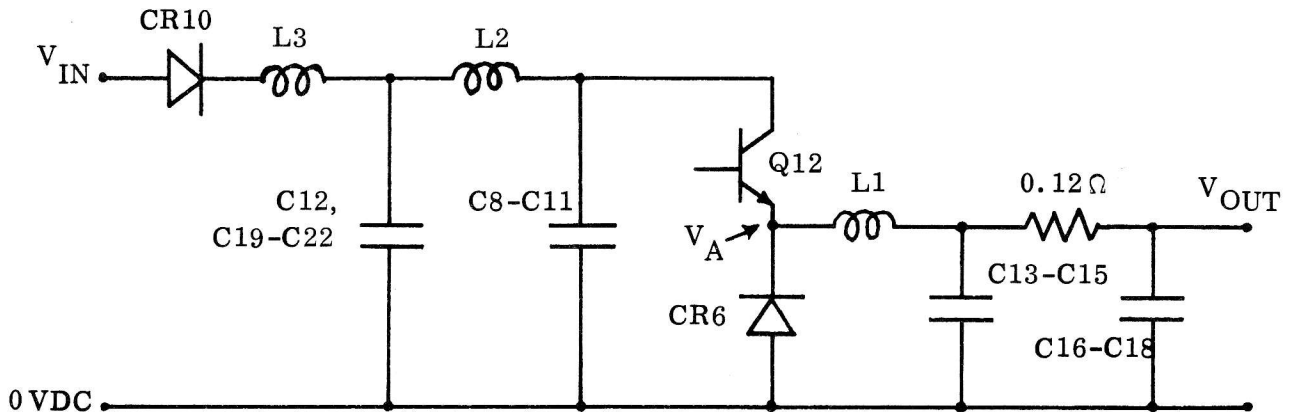


Figure A-1

For a switching frequency of 100 kc, Q12 is on for 5.41  $\mu$ sec each cycle. Assuming that the inductance of L1 is constant over the current range considered, the increase in current in L1 is

$$\Delta I_{L1} = \frac{e_L \Delta t}{L1} = \frac{(V_{IN} - V_{CR10} - V_{CE(ON)} - V_{OUT}) \Delta t}{L1}$$

The minimum inductance required is given by

$$L1 > \frac{(V_{IN} - V_{CR10} - V_{CE(ON)} - V_{OUT}) \Delta t}{\Delta I_{L1}}$$

For the conditions of minimum load of 0.2 amps given in the test spec for the +14 volt supply,

$$L1 > \frac{(28 - .6 - 1.0 - 14.0) 5.41 \times 10^{-6}}{0.4}$$

$$L1 > 168 \mu h.$$

For the free-running mode, with the period of 22  $\mu$ sec given in Table 1 of the factory test plan, L1 must be greater than 370  $\mu$ h. These calculations are based on typical conditions, so the worst-case conditions will require an even larger inductor.

The specification control drawing No. 1006328 for L1 gives no indication of its inductance at any current except 7 amperes. The inductance should be specified over the full range of operating currents from minimum load current to the maximum short-circuit current. If L1 does not conduct continuously over the entire cycle, two problems arise. First, the output voltage is no longer even approximately



proportional to the duty cycle of Q12, but becomes a function of the load current. Thus a step in the load current will cause a transient in the output voltage until the differential amplifier can respond and change the duty cycle. Secondly, when L1 and CR6 cease conducting, L1 will tend to ring severely, causing RFI problems.

A suggestion for decreasing any RFI problem is minimizing the lead lengths in the path from the positive terminal of C8 - C11 to the collector of Q12, from the emitter of Q12 to the cathode of CR6, and from the anode of CR6 to the negative terminal of C8 - C11. Also, these components should be isolated from any sensitive circuits.

With regard to the driver composed of Q9, Q10, and Q11, it is recommended that these three transistors be replaced by a single 2N3467 or similar transistor. Otherwise, isolation resistors should at least be included in the bases of each transistor.

The power supply does not contain current-limiting when used to supply +14 volts. This is confirmed by the absence of current-limiting test for the +14 volt supply. The emitter of Q13 is tied to the +14 volts, and its collector is coupled through CR3 to the oscillator. The anode of CR3 is at a potential of less than 9 volts, so the only time Q13 can provide protection is when the output voltage is considerably less than 9 volts. Also, it is not clear how this circuit can provide short-circuit limiting at 9 amps on the +4 volts and at 10 amps on the +14 volts. The +4 volt supply has a 0.06 ohm sensing resistor and the +14 volt supply has a 0.12 ohm resistor, implying that the limiting currents should likewise be different by a factor of two.

There is no test made to see if the control circuits of power supply are using an unreasonable amount of power. A measurement should be made of the input power with a minimum load to determine the power consumed by these circuits.

The short-circuit test is performed at a low duty cycle. The supply should be tested with a continuous short-circuit to verify that no damage will result.

Three items have been discovered in the differential amplifier that are not in accordance with good design practice. First, the temperature-compensated Zener reference, CR1, is not operated at the specified current of 7.5 ma, as required to achieve the best temperature coefficient, but at 4.5 ma. This is based on the statement in Paragraph 4.3 of the factory test plan that the supply voltage for the differential amplifier is +9 volts.

Second, there is approximately a 10:1 difference in the collector currents of the two halves of the differential amplifier, and no apparent reason for it.

Third, the input resistance to one half of the differential amplifier is about three times as great as for the other half. This is aggravated by the fact that the side with the high input resistance also has the larger collector current. Figure A-2



shows the equivalent circuit for each half of the differential amplifier when used in the +14 volt supply, and  $R_{NOM} = 200 \Omega$ .

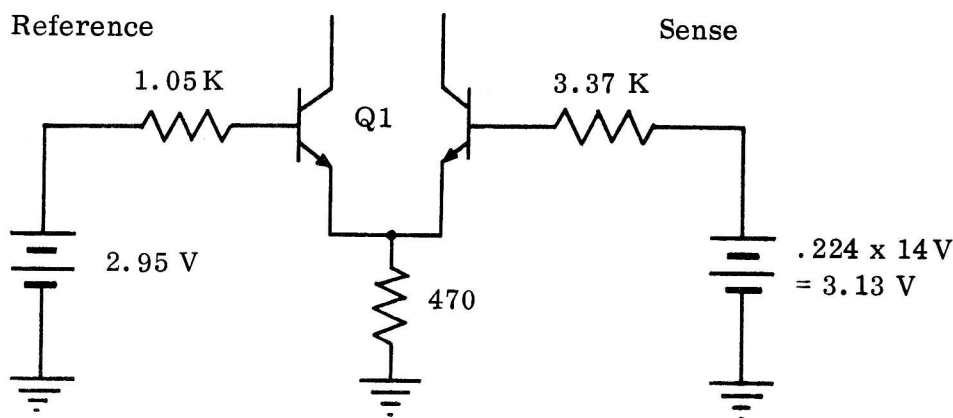


Figure A-2

Since a typical transistor will show about 70 mv difference in  $V_{BE}$  for a 10:1 difference in  $I_B$ , the drop across the 3.37 K $\Omega$  resistor is about 110 mv greater than the drop across the 1.05 K $\Omega$  resistor. Since  $h_{FE}$  will vary about 2:1 over the temperature range, the 3.13 volts can be expected to vary 0.11 volt and the +14 volts to vary about 0.5 volt over the temperature range.

The limits over which the supply voltages can be varied by use of the circuits in Figure 2 of the factory test plan were calculated. The factory test plan does not specify a tolerance on the 1 K $\Omega$  pot required. Although its tolerance will have an effect on the limits, the following table is based on calculations using no tolerance.

TABLE	TEST	VOLTAGE	CIRCUIT	RANGE
V	No. 1	+4 v	Fig. 2B	2.80-5.93
V	No. 2	+14 v	Fig. 2A	11.0-18.0
VI	No. 1	+4 v	Fig. 2C	0.6-6.8
VI	No. 2	+14 v	Fig. 2C	2.2-23.6

Table A-1

These ranges seem to be much greater than what is necessary. The figures for the ranges for the tests in Table VI are only approximate, because the operating point of the differential amplifier is affected by the test. However, it is recommended that the circuit be redesigned to limit the range of the voltages.



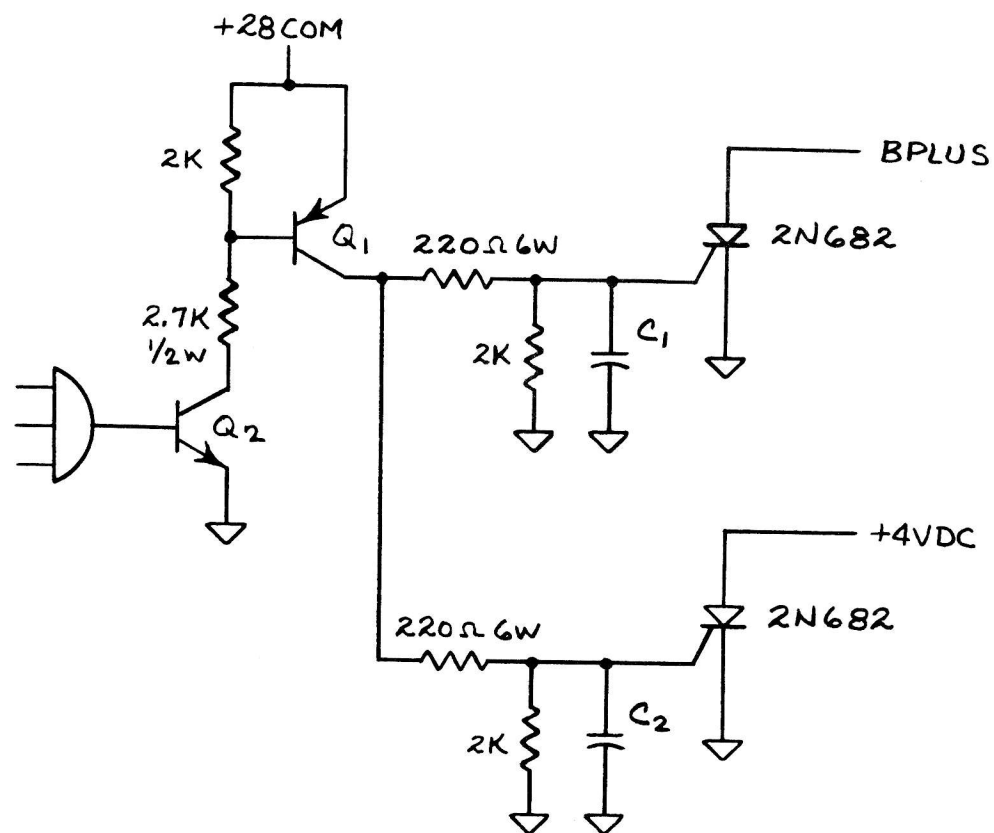
This design review was based on the following documents:

Schematic		2005916-
Transistor	Q12	1006317A
"	Q1	1010376J
"	Q14, Q18	1006363-
"	Q4, Q7, Q9, -Q11	1006310C
"	Q2, Q3, Q5, Q6, Q8, Q13, Q15, -Q17	1006323B
Rectifier	CR6, CR10	1006329A
Zener Diode	CR1	1006838D
Inductor	L1	1006328-
"	L2, L3, L4	1006327-
Factory Test Plan		186413 (Prel 2)

Table A-2

Figure A-3 shows a circuit configuration which could possibly be used to protect the computer in the event of a power supply failure. When the voltage alarm circuit detects excessive voltage from either supply, it will send a logic-level signal to the overvoltage protection circuit. The driver composed of Q1 and Q2 will fire the two SCR's, short-circuiting the power supply outputs until the computer is turned off. Since the supplies have short-circuit current limiting, they will not be damaged unless the failure is such as to prohibit operation in the current-limited mode.

If the voltage transient that occurs when the computer enters the standby mode exceeds the detection threshold of the voltage alarm circuit, it will be necessary to inhibit firing the SCR's for the period of the transient. The capacitors C1 and C2 can possibly provide that delay, and will also prevent noise from firing the SCR's.



$Q_1 - 1006310C$

$Q_2 - 1006323B$

Figure A-3. Overvoltage Protection Circuit

66-157

APPENDIX B

COUNTERFAIL REDESIGN

D. HOLTSHOUSE



66-157  
Counter increments and decrements, serial-parallel conversion steps, and GSE interface transactions are lumped together under the name of counter interrupts because they perform limited tasks by snatching one or two memory cycles and then let the computer continue. Counter interrupts can occur before any instruction except RELINT, INHINT, or EXTEND.

The counter alarm circuit detects for:

- (a) Excessive counter activity,
- (b) A counter update request not followed by a counter interrupt.

That section of the alarm circuit not functioning properly is the section for counter update request not followed by a counter interrupt. All counter update pulses activate two areas of logic composed of the alarm circuit (A13) and the counter priority and servicing circuits (A20). Normal counter interrupt procedures may be best illustrated by an example.

Suppose the computer is performing the last MCT of an instruction and that the next instruction is not EXTEND, INHINT or RELINT, since this will simplify the illustration and not affect the final outcome for demonstration of the malfunction. Suppose also that a counter update pulse, such as CDUXP, occurred during T01 of the last MCT of the current instruction (Figure B-3) and sets flipflops A of Figure B-1 and C of Figure B-2. Actually CDUXP can occur anytime prior to T10 of MCT to generate a counter interrupt. NISQL is generated at T02 or T08 and indicates the completion of the current instruction and a flag to bring forward the next one.

Since NISQL has been generated and the next instruction is not INHINT, RELINT or EXTEND, NOTEST is a logical low and flipflop B is set at T09. CTROR is generated at T10 which indicates that a counter update pulse has been received by at least one of the counters on Figure B-2. Provided the GOJAM condition does not exist, all other conditions enable flipflop D (Figure C-1) to be set at T12 which results in the generation of the counter interrupt command INKL. The computer now services all counter requests and then returns to the program to execute the next instruction. Notice that an alarm would have been generated at the following T03 if INKL generated at T12 had not reset flipflop B (Figure B-1). This is where the problem exists today.

As stated earlier and described in Figure B-3, INKL is inhibited by GOJAM. Therefore, if conditions for GOJAM are generated during the last MCT of the current instruction, the GOJAM signal is generated at T12 and also inhibits INKL from being generated at T12. Consequently, the alarm flipflop "B" is not reset and the following T03 generates a false counter alarm. The alarm is false, obviously, because counter interrupts are not to be generated if GOJAM exists.

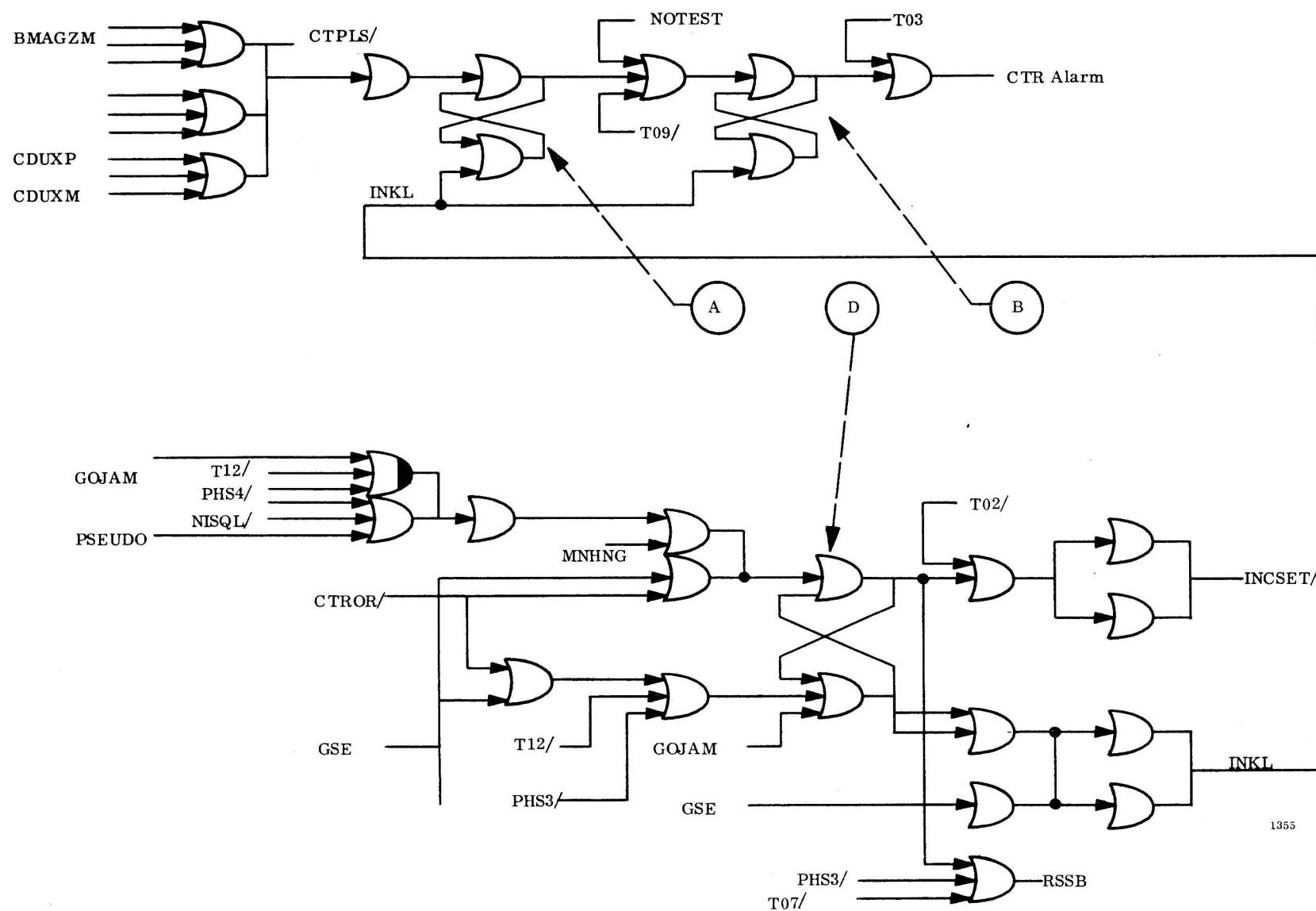


Figure B-1. CTR ALARM and Increment Service



B-3

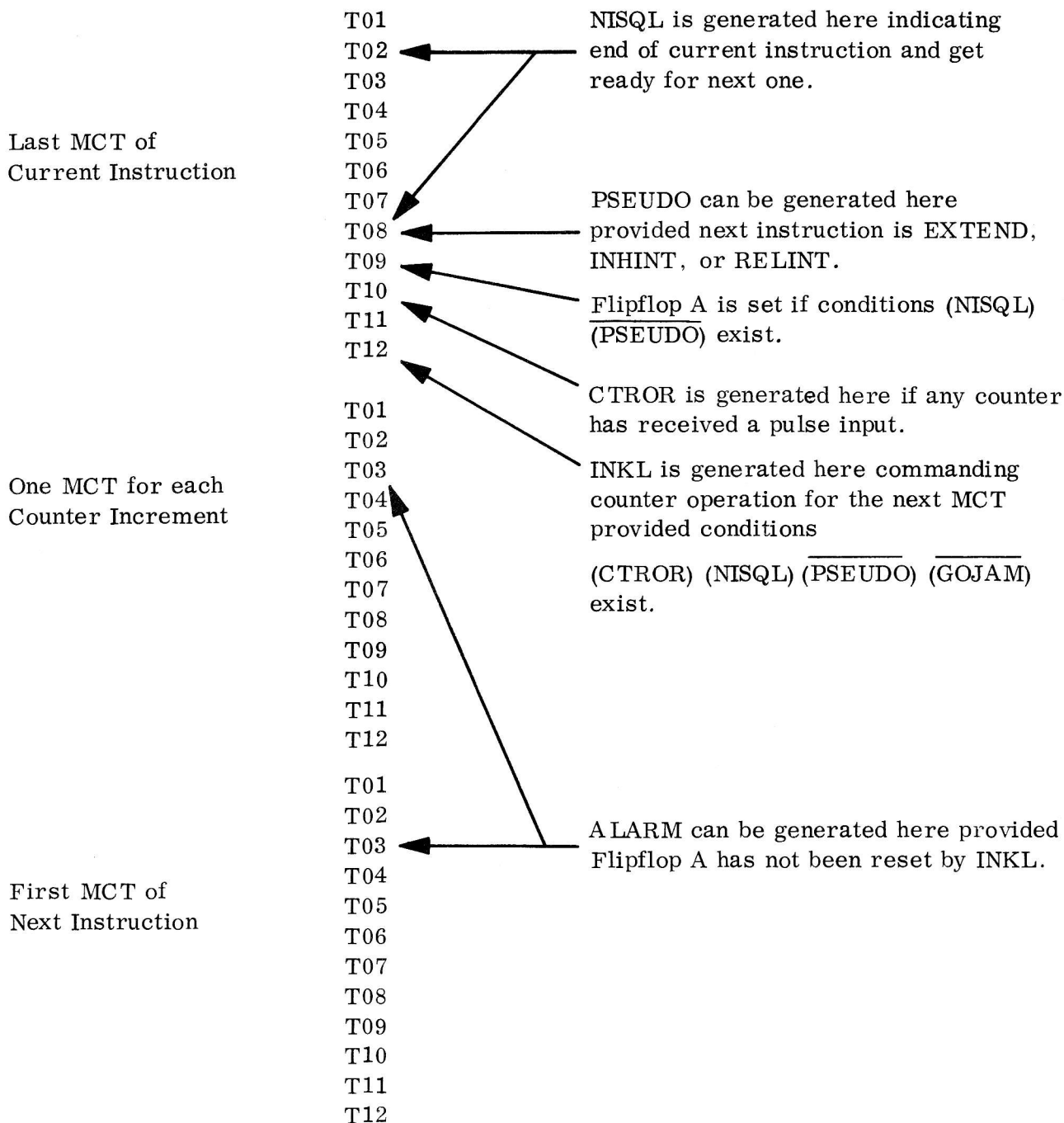


Figure B-3. Counter Servicing

66-157  
The probability of GOJAM occurring simultaneously with counter interrupt requests may not be significant during normal system operation since, hopefully, the probability of GOJAM occurring often is low. But the probability is high during computer checkout when the GOJAM signal is being induced as a result of forcing the computer into TC Trap and Rupt Lock during checkout of the other alarm circuits.

A cursory examination of the alarm circuit seems to indicate that flipflop B (Figure B-1) should be reset by INKL or GOJAM. It would not be appropriate to reset both flipflop (A and B); however, since the counter priority flipflops are not reset by GOJAM and the alarm circuit would not be aware of any counter update request still remaining in the priority chain.



APPENDIX C

NOISE MARGIN ANALYSIS

A. H. Faulkner



The logic loading rules for the Apollo NOR gate allow 25 load units to be connected to a gate output. Each gate input is presumed to draw 5 load units with a clamped collector, or 4 units with an unclamped collector. Each expander gate output node is presumed to draw 1/2 load unit from the gate it is paralleled with. In practice the loading rules have been violated in many instances by exceeding the permissible load by 20 percent; i. e., 30 load units drawn from a 25-unit source. The device specification is intended to guarantee a noise threshold of 100 mv at 25°C for a fully loaded gate under worst case conditions. In view of the logic overloads and the extended temperature range (0° to 70°C) the actual noise threshold is open to question.

At the request of the Apollo Design Review Committee, Philco generated a specification applicable to the Apollo gates and expanders when operated at 0°C and 75°C with normal loading. This specification, shown in Table C-1, is intended to be sufficiently conservative to guarantee 0°C and 75°C operation with 100 percent final testing at 25°C only. Acceptance would require only sampling at the temperature extremes. Philco emphasized that this information is to be regarded as engineering data. Study of a larger distribution would be needed before a firm commitment could be negotiated.

The parameter values for 25°C correspond to those specified in MSC Drawing 1006321 and are shown for reference only.

PARAMETER	UNITS	0°C	25°C	75°C
$V_{CC}$	V	4	4	4
$V_{IN}$	MV	910	870	790
$V_{ON}$	MV	870	770	750
$V_{OUT}$	MV	350	300 (Gate) 400 (E)	325
$V_{OFF}$	MV	500	500	500
$V_{CE}$	MV	280	220	300
$I_{IN}$	$\mu a$	155	152	150
$I_A$	$\mu a$	744	760	720
$I_{CEX}$	$\mu a$	15	15	20

Table C-1. 0°C and 75°C Spec for Apollo Gates and Expanders

It should be noted that  $I_A = 5.0 I_{IN}$  at 25°C, and  $I_A = 4.8 I_{IN}$  at 0°C and 75°C. The latter value has been used by vendors in specifying parameters more recently to take into account the fact that a typical starved gate draws about 80 percent as much current as a typical hogging gate. It corresponds to the logic loading rule which assigns





four load units to a starved gate and five load units to a hogging gate.

The limiting noise threshold at the temperature extremes is established by a worst-case configuration of logic elements which results in the starved gate receiving appreciably less than 80 percent of the specified  $I_{IN}$ , hence the actual node voltage is higher than the specified  $V_{IN}$ . Consequently, the worst-case noise threshold is actually slightly higher than the 40 mv difference between  $V_{IN}$  and  $V_{ON}$ , which is commonly referred to as the guaranteed noise threshold. This fallacy has been taken into account in the following analysis and the resulting higher noise thresholds are the values tabulated in the body of the report.

In order to calculate the actual noise threshold the minimum value of  $h_{FE}$  and the range of  $R_B$  and  $R_C$  must be known. Drawing 1006321 specifies the ranges of  $h_{FE}$  and  $R_C$ , and the range of  $R_B$  can be inferred from the known relation,  $R_C = 2.28 R_B$ . Using these parameters, the actual noise threshold at 25°C is calculated in Case 1 for a gate with a maximum value collector resistor driving a starved gate expander and three (Case 1C) to five (Case 1B) hogging gates.

#### CASE 1A

$$T = 25^{\circ}\text{C} \quad \text{F.O.} = 5$$

##### a. Hogging Gate Parameters

$$V_{IN} = 870 \text{ mv}$$

$$R_B = 1200 \Omega$$

$$I_{IN} = 152 \mu\text{a}$$

$$V_{BE} = 870 - (1.200 \times 152) = 688 \text{ mv}$$

##### b. Starved Gate Parameters

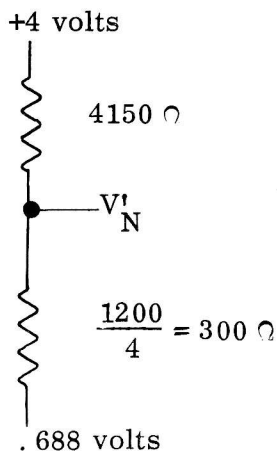
$$V_{ON} = 770 \text{ mv}$$

$$R_B = 1200 \Omega$$

$$I_B = 44.5 \mu\text{a}$$

$$V_{BE} = 770 - (1.200 \times 44.5) = 717 \text{ mv}$$

##### c. First determine $V'_N$ with a starved gate open.

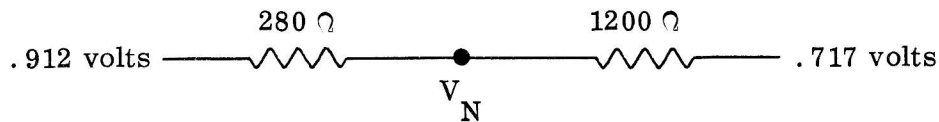


$$V'_N = (4.000 - 0.688) \times \frac{300}{4450} + .688 = .912 \text{ volts}$$

$$\text{Source resistance} = \frac{300 \times 4150}{4450} = 280 \Omega$$



- d. Next determine the loading effect of the starved gate on  $V'_N$ .



$$V_N = .912 - (.912 - .717) \times \frac{280}{1480} = .875 \text{ volts}$$

- e. Noise threshold =  $V_N - V_{ON} = .875 - .770 = 105 \text{ mv}$

The actual noise threshold (105 mv) is thus determined to be 5 mv higher than the "guaranteed noise threshold" (100 mv) indicated by the difference between  $V_{IN}$  and  $V_{ON}$  in the device specification.

The effect of the 20 percent logic overload, corresponding to F.O. = 6, in the Apollo computer is considered next.

#### CASE 1B

$$T = 25^\circ\text{C}$$

$$\text{F.O.} = 6$$

- a. Hogging Gate Parameters

$$V_{IN} = 870 \text{ mv}$$

$$R_B = 1645 \Omega$$

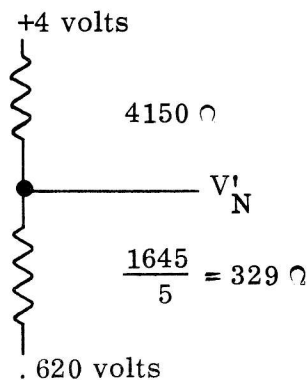
$$I_{IN} = 152 \mu\text{a}$$

$$V_{BE} = 870 - (1.645 \times 152) = 620 \text{ mv}$$

- b. Starved Gate Parameters

Same as Case 1A

- c. Determine  $V'_N$  with starved gate open.

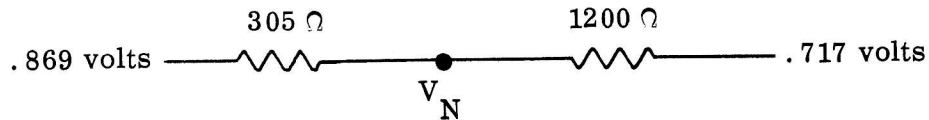


$$V'_N = (4.00 - .620) \times \frac{329}{4479} + .620 = .869 \text{ volts}$$

$$\text{Source resistance} = \frac{329 \times 4150}{4479} = 305 \Omega$$



- d. Determine the loading effect of the starved gate on  $V'_N$ .



$$V_N = .869 - (.869 - .717) \times \frac{305}{1505} = .838 \text{ volts}$$

- e. Noise threshold =  $V_N - V_{ON} = .838 - .770 = 68 \text{ mv}$

Finally, the effect of underloading the logic by 20 percent, i. e., F.O. = 4, is considered.

### CASE 1C

$$T = 25^\circ\text{C} \quad \text{F.O.} = 4$$

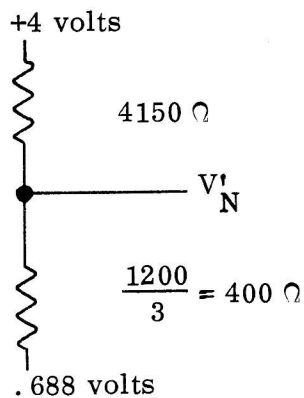
- a. Hogging Gate Parameters

Same as Case 1A

- b. Starved Gate Parameters

Same as Case 1A

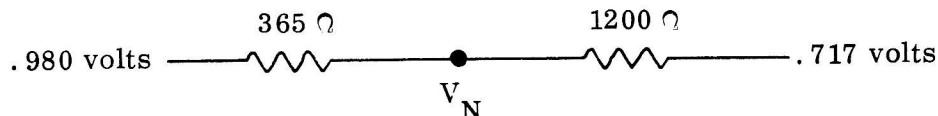
- c. Determine  $V'_N$  with starved gate open.



$$V'_N = (4.000 - .688) \times \frac{400}{4550} + .688 = .980 \text{ volts}$$

$$\text{Source resistance} = \frac{400 \times 4150}{4550} = 365 \Omega$$

- d. Determine the loading effect of the starved gate on  $V'_N$ .



- e. Noise threshold =  $V_N - V_{ON} = .942 - .770 = 172 \text{ mv}$



The next case to be considered involves the same configurations as Case 1 but operating at  $0^{\circ}\text{C}$ . The difference between  $V_{\text{IN}}$  and  $V_{\text{ON}}$  is much less (40 mv) at  $0^{\circ}\text{C}$  than it is at  $25^{\circ}\text{C}$  (100 mv). The principle factor controlling this difference, for a given fanout, is the difference between the  $V_{\text{BE}}$ 's of the starved and hogging gates. Due to the considerable spread in temperature coefficient of the base diode for different diffusion lots, the spread between the  $V_{\text{BE}}$ 's of the hogging and starved gates can increase considerably with temperature changes. Since the exact range of this temperature coefficient is not known, the change in  $V_{\text{BE}}$  characteristics must be obtained indirectly from the known values of  $V_{\text{IN}}$  and  $V_{\text{ON}}$  by considering the effect changes in  $R_{\text{B}}$  and  $h_{\text{FE}}$  with temperature have on these black box parameters.

The temperature characteristics of diffused silicon resistors is shown in Figure C-1 for a small sample of Philco dual NOR gates. Philco engineers stated that they have observed a spread from +12 percent to +16 percent at  $125^{\circ}\text{C}$ , which agrees well with the data obtained by ACLA. The expected range is seen between 0.965 and 0.98 at  $0^{\circ}\text{C}$ , and between 1.055 and 1.075 at  $75^{\circ}\text{C}$ , referred to the  $25^{\circ}\text{C}$  value.

The change in  $h_{\text{FE}}$  with temperature for typical Philco dual NOR gate devices is shown in Figure C-2. It appears from this data that  $h_{\text{FE}}$  can be expected to degrade from a minimum of 30 at  $25^{\circ}\text{C}$  to a minimum of 22.5 at  $0^{\circ}\text{C}$ .

Using these parameters, the actual noise threshold at  $0^{\circ}\text{C}$  is calculated in Case 2 for a gate with a maximum value collector resistor driving a starved gate expander and three (Case 2C) to five (Case 2B) hogging gates.

#### CASE 2A

$$T = 0^{\circ}\text{C}$$

$$\text{F.O.} = 5$$

##### a. Hogging Gate Parameters

$$V_{\text{IN}} = 910 \text{ mv}$$

$$R_{\text{B}} = 1200 \times .98 = 1175 \Omega$$

$$I_{\text{IN}} = 155 \mu\text{a}$$

$$V_{\text{BE}} = 910 - (1.175 \times 155) = 728 \text{ mv}$$

##### b. Starved Gate Parameters

$$V_{\text{ON}} = 870 \text{ mv}$$

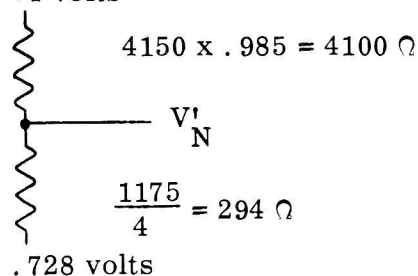
$$R_{\text{B}} = 1200 \times .965 = 1160 \Omega$$

$$I_{\text{B}} = 62 \mu\text{a}$$

$$V_{\text{BE}} = 870 - (1.160 \times 62) = 797 \text{ mv}$$

##### c. Determine $V'_{\text{N}}$ with starved gate open.

+4 volts



$$V'_{\text{N}} = (4.000 - .728) \times \frac{294}{4393} + .728 = .946 \text{ volts}$$

$$\text{Source resistance} = \frac{294 \times 4100}{4393} = 274 \Omega$$

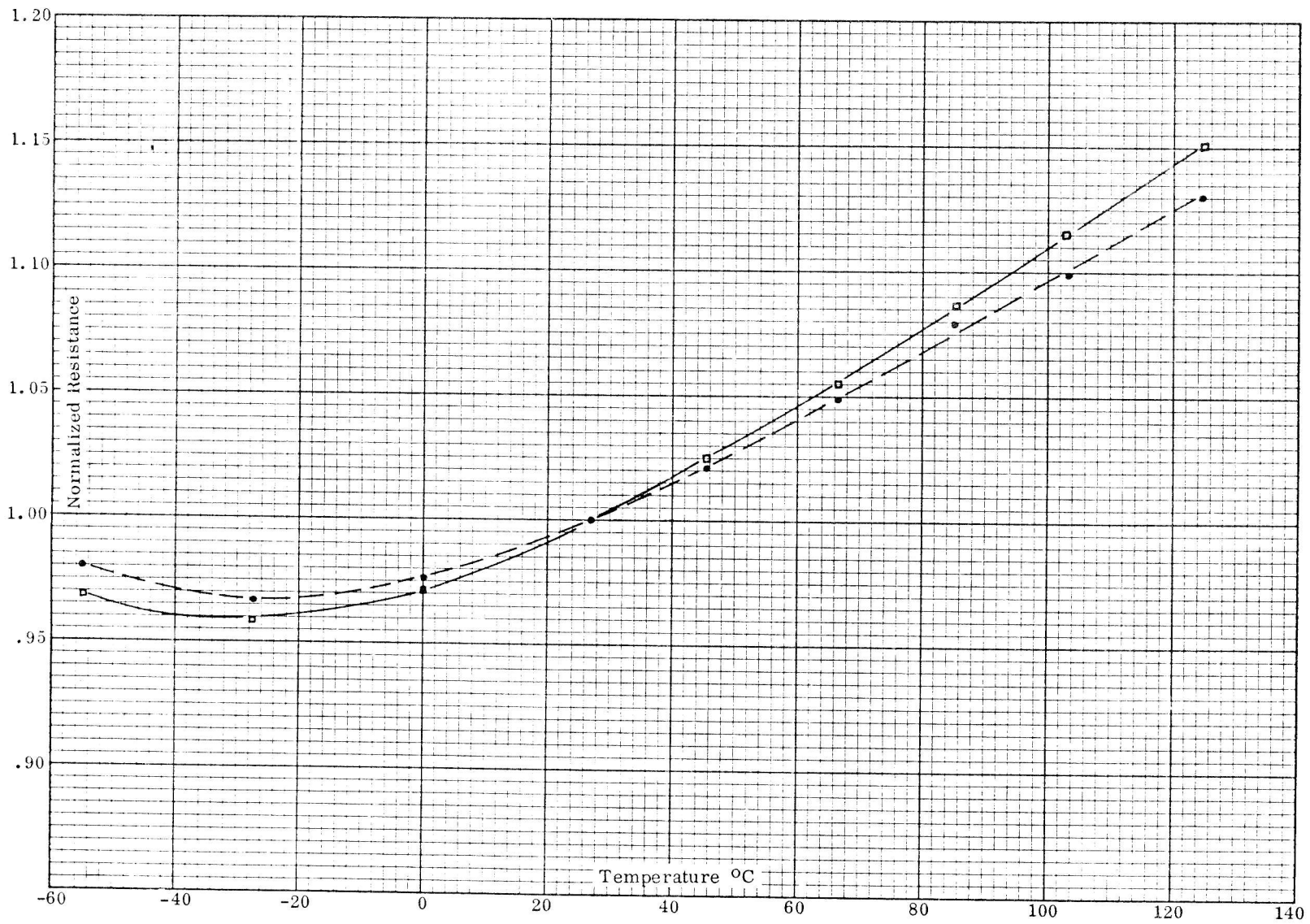


Figure C-1. Resistance vs. Temperature for Apollo NOR Gates

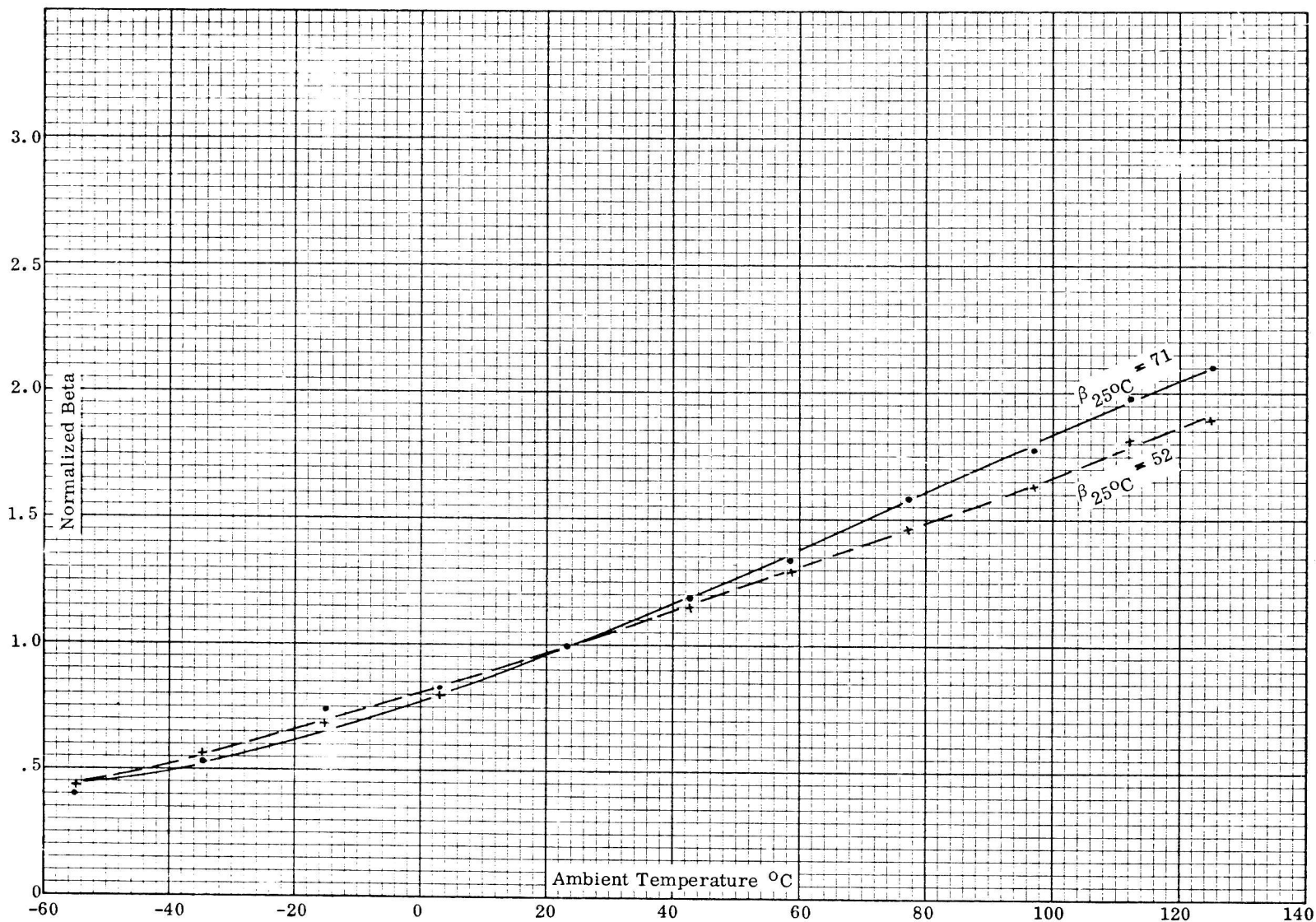
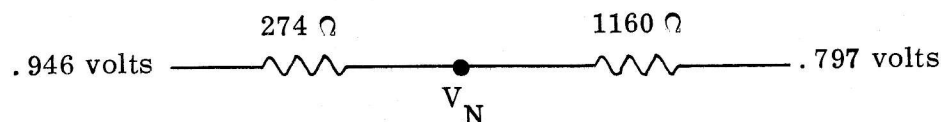


Figure C-2. Beta vs. Temperature for Apollo NOR Gates



- d. Determine the loading effect of starved gate on  $V'_N$ .



$$V_N = .946 - (.946 - .797) \times \frac{274}{1434} = .918 \text{ volts}$$

- e. Noise threshold =  $V_N - V_{ON} = .918 - .870 = 48 \text{ mv}$

### CASE 2B

$$T = 0^\circ\text{C}$$

$$\text{F.O.} = 6$$

- a. Hogging Gate Parameters

- b. Starved Gate Parameters

$$V_{IN} = 910 \text{ mv}$$

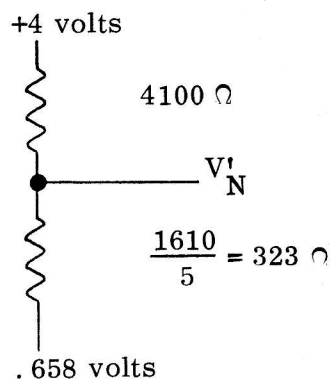
Same as Case 2A

$$R_B = 1645 \times .98 = 1610 \Omega$$

$$I_{IN} = 155 \mu\text{a}$$

$$V_{BE} = 910 - (1.620 \times 155) = 658 \text{ mv}$$

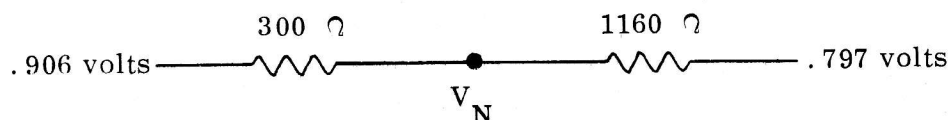
- c. Determine  $V'_N$  with starved gate open.



$$V'_N = (4.000 - .658) \times \frac{323}{4423} + .658 = .906 \text{ volts}$$

$$\text{Source resistance} = \frac{323 \times 4100}{4423} = 300 \Omega$$

- d. Determine the loading effect of starved gate on  $V'_N$ .



$$V_N = .906 - (.906 - .797) \times \frac{300}{1460} = .884 \text{ volts}$$

- e. Noise threshold =  $V_N - V_{ON} = .884 - .870 = 14 \text{ mv}$





## CASE 2C

$$T = 0^{\circ}\text{C}$$

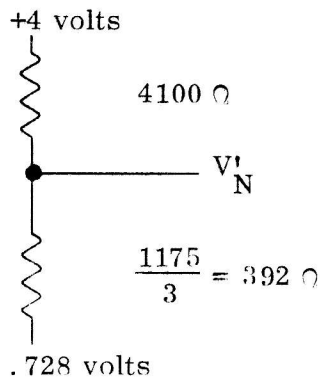
$$\text{F.O.} = 4$$

a. Hogging Gate Parameters

Same as Case 2A

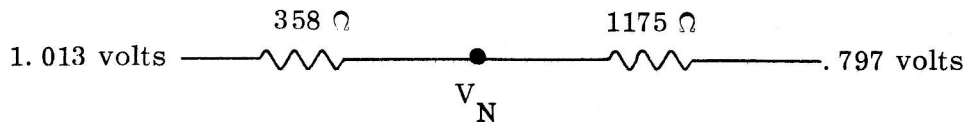
b. Starved Gate Parameters

Same as Case 2A

c. Determine  $V'_N$  with starved gate open.

$$V'_N = (4.000 - .728) \times \frac{392}{4492} + .728 = 1.013 \text{ volts}$$

$$\text{Source resistance} = \frac{392 \times 4100}{4492} = 358 \Omega$$

d. Determine loading effect of starved gate on  $V'_N$ .

$$V_N = 1.013 - (1.013 - .797) \times \frac{358}{1533} = .963 \text{ volts}$$

$$\text{e. Noise threshold} = V_N - V_{\text{ON}} = .963 - .870 = 93 \text{ mv}$$

The third case to be considered is operation at  $75^{\circ}\text{C}$ . From Figure C-1 it is seen that the spread in resistor values is from +6 percent to +8 percent. Figure C-2 indicates that  $h_{\text{FE}}$  increases at  $75^{\circ}\text{C}$ , however, this is the  $h_{\text{FE}}$  measured at  $V_C = 0.5$  volts. The  $h_{\text{FE}}$  at  $V_C = 0.325$  is the parameter desired. In view of the fact that the  $V_{\text{OUT}}$  of the gate expander must be lowered from 400 mv at  $25^{\circ}\text{C}$  to 325 mv at  $75^{\circ}\text{C}$ , it is assumed that  $h_{\text{FE}}$  will drop from a minimum of 30 at  $25^{\circ}\text{C}$  to 20 at  $75^{\circ}\text{C}$ . This assumption is justified by the more reasonable range of values obtained for the temperature coefficient of the  $V_{\text{BE}}$  diode than would be obtained if a higher value was used for  $h_{\text{FE}}$ .

Using these parameters, the actual noise threshold at  $75^{\circ}\text{C}$  is calculated in Case 3 for a gate with a maximum value collector-resistor driving a starved gate expander and three (Case 3C) to five (Case 3B) hogging gates.



## CASE 3A

$$T = 75^{\circ}\text{C}$$

$$F.O. = 5$$

## a. Hogging Gate Parameters

$$V_{IN} = 790 \text{ mv}$$

$$R_B = 1200 \times 1.055 = 1265 \Omega$$

$$I_{IN} = 150 \mu\text{a}$$

$$V_{BE} = 790 - (1.265 \times 150) = 599 \text{ mv}$$

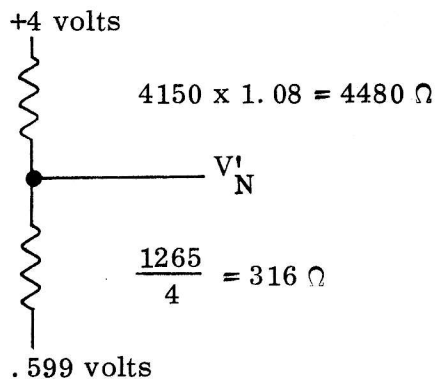
## b. Starved Gate Parameters

$$V_{ON} = 750 \text{ mv}$$

$$R_B = 1200 \times 1.055 = 1265 \Omega$$

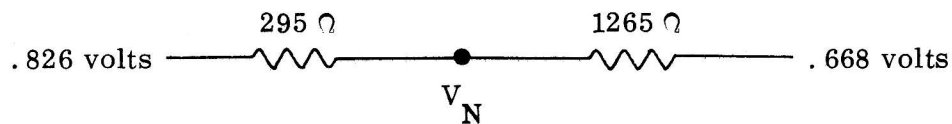
$$I_B = 64 \mu\text{a}$$

$$V_{BE} = 750 - (1.265 \times 64) = 668 \text{ mv}$$

c. Determine  $V'_N$  with starved gate open.

$$V'_N = (4.000 - .599) \times \frac{316}{4796} + .599 = .826 \text{ volts}$$

$$\text{Source resistance} = \frac{316 \times 4480}{4796} = 295 \Omega$$

d. Determine loading effect of starved gate on  $V'_N$ .

$$V_N = .826 - (.826 - .668) \times \frac{295}{1560} = .794 \text{ volts}$$

e. Noise threshold =  $V_N - V_{ON} = .794 - .750 = 44 \text{ mv}$



## CASE 3B

$$T = 75^{\circ}\text{C}$$

$$\text{F.O.} = 6$$

a. Hogging Gate Parameters

$$V_{\text{IN}} = 790 \text{ mv}$$

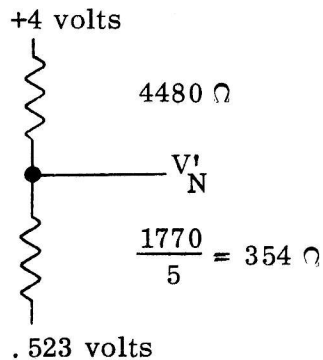
$$R_{\text{B}} = 1645 \times 1.075 = 1770 \Omega$$

$$I_{\text{B}} = 150 \mu\text{a}$$

$$V_{\text{BE}} = 790 - (1.770 \times 150) = 523 \text{ mv}$$

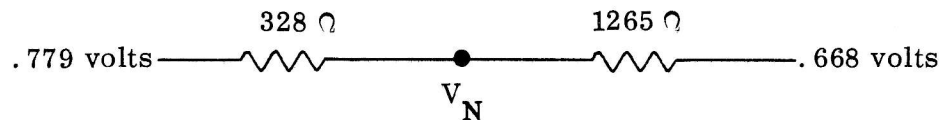
b. Starved Gate Parameters

Same as Case 3A

c. Determine  $V'_{\text{N}}$  with starved gate open.

$$V'_{\text{N}} = (4.000 - .523) \times \frac{354}{4834} + .523 = .779 \text{ volts}$$

$$\text{Source resistance} = \frac{354 \times 4480}{4834} = 328 \Omega$$

d. Determine loading effect of starved gate on  $V'_{\text{N}}$ .

$$V_{\text{N}} = .779 - (.779 - .668) \times \frac{328}{1593} = .756 \text{ volts}$$

e. Noise threshold  $= V_{\text{N}} - V_{\text{ON}} = .756 - .750 = 6 \text{ mv}$ 

## CASE 3C

$$T = 75^{\circ}\text{C}$$

$$\text{F.O.} = 4$$

a. Hogging Gate Parameters

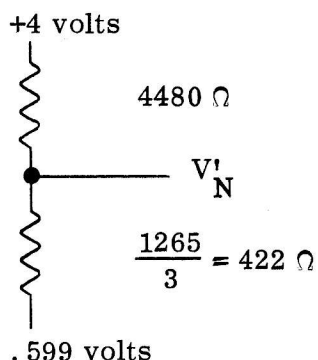
Same as Case 3A

b. Starved Gate Parameters

Same as Case 3A



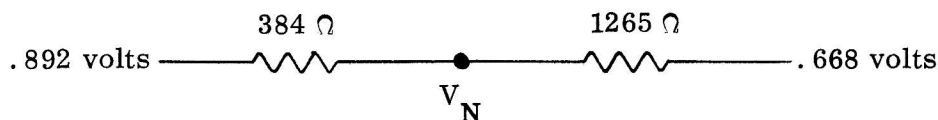
- c. Determine  $V'_N$  with starved gate open.



$$V'_N = (4.000 - .599) \times \frac{422}{4902} + .599 = .892 \text{ volts}$$

$$\text{Source resistance} = \frac{422 \times 4480}{4902} = 384 \Omega$$

- d. Determine loading effect of starved gate on  $V'_N$ .



$$V_N = .892 - (.892 - .669) \times \frac{384}{1649} = .840 \text{ volts}$$

- e. Noise threshold  $= V_N - V_{ON} = .840 - .750 = 90 \text{ mv}$

In addition to normal interconnections with other NOR gates, the gate expander is also used to drive interface circuits. This situation is considered in Case 4 for an expander gate pulling down a  $3.0 \text{ K } \Omega$  load from +10 volts and having two inputs driven in parallel with three hogging gates by a gate having a maximum value collector resistor.

#### CASE 4A

$$T = 25^\circ \text{C}$$

- a. Hogging Gate Parameters

Same as Case 1A

- b. Starved Gate Parameters

Same as Case 1A, except for changes due to increase in  $I_C$  to 1.6 ma.

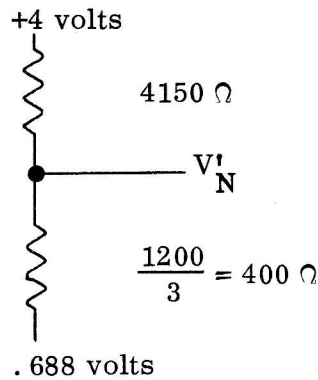
$$I_B = 44.5 \times \frac{1.6}{1.33} = 53.5 \mu\text{a}$$

$$*V_{ON} = 717 + 30 (1.6 - 1.33) + (1.200 \times 53.5) = 787 \text{ mv}$$

\*Allowing  $30 \Omega$  for  $R_E$



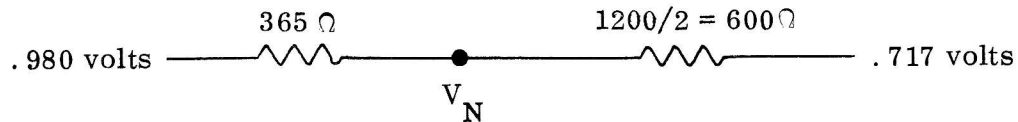
- c. Determine  $V'_N$  with starved gate expanders open.



$$V'_N = (4.000 - .688) \times \frac{400}{4550} + .688 = .980 \text{ volts}$$

$$\text{Source resistance} = \frac{400 \times 4150}{4550} = 365 \Omega$$

- d. Determine loading effect of starved gates on  $V'_N$ .



$$V_N = .980 - (.980 - .717) \times \frac{365}{965} = .881 \text{ volts}$$

- e. Noise threshold  $= V_N - V_{ON} = .881 - .789 = 92 \text{ mv}$

#### CASE 4B

$$T = 0^\circ\text{C}$$

- a. Hogging Gate Parameters

Same as Case 2A

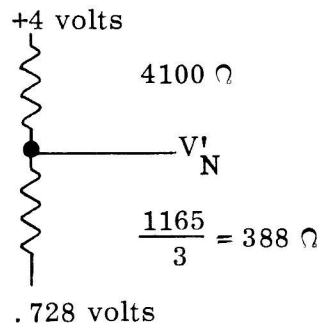
- b. Starved Gate Parameters

Same as Case 2A, except for changes due to increase in  $I_C$  to 1.6 ma.

$$I_B = 62 \times \frac{1.6}{1.39} = 71 \mu\text{a}$$

$$V_{ON} = 797 + 30(1.6 - 1.39) + (1.165 \times 71) = 886 \text{ mv}$$

- c. Determine  $V'_N$  with starved gate open.

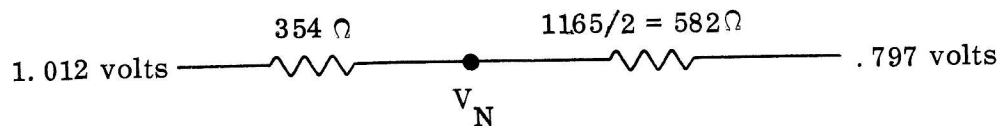


$$V'_N = (4.000 - .728) \times \frac{388}{4488} + .728 = 1.012 \text{ volts}$$

$$\text{Source resistance} = \frac{388 \times 4100}{4488} = 354 \Omega$$



- d. Determine the loading effect of starved gate on  $V'_N$ .



$$V'_N = 1.012 - (-.12 - .797) \times \frac{354}{936} = .931 \text{ volts}$$

- e. Noise threshold =  $V'_N - V_{ON} = .931 - .886 = 45 \text{ mv}$

CASE 4C

$T = 75^\circ\text{C}$

- a. Hogging Gate Parameters

Same as Case 3C

- b. Starved Gate Parameters

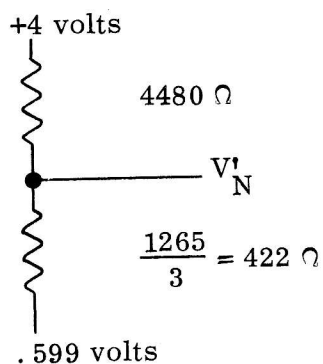
$$V_{BE} = 668 \text{ mv (see Case 3A)}$$

$$R_B = 1265 \Omega$$

$$I_B = \frac{1.6}{30} = 53.5 \mu\text{a}$$

$$V_{ON} = 668 + 30(1.6 - 1.28) + (1.265 \times 53.5) = 746 \text{ mv}$$

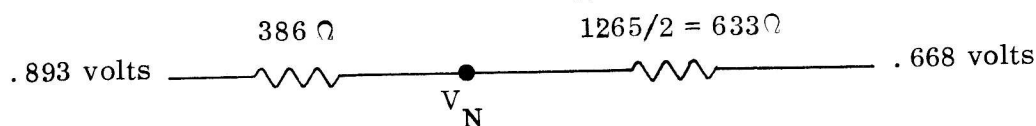
- c. Determine  $V'_N$  with starved gate open.



$$V'_N = (4.000 - .599) \times \frac{422}{4902} + .599 = .893 \text{ volts}$$

$$\text{Source resistance} = \frac{422 \times 4480}{4902} = 386 \Omega$$

- d. Determine loading effect of starved gate on  $V'_N$ .



$$V'_N = .893 - (.893 - .668) \times \frac{386}{1019} = .808 \text{ volts}$$

- e. Noise threshold =  $V'_N - V_{ON} = .808 - .746 = 62 \text{ mv}$



The results of the preceding calculations are summarized in Table C-2. These are the "1" level noise thresholds. The "0" level noise threshold has a similar trend, but cannot be calculated readily due to operation at the knee of the saturation characteristics.

FANOUT	NOISE THRESHOLD		
	0°C	25°C	75°C
4	93 mv	172 mv	90 mv
5	48 mv	105 mv	44 mv
5 (Interface)	45 mv	92 mv	62 mv
6	14 mv	68 mv	6

Table C-2. Calculated Noise Thresholds of Apollo NOR Gates

In the preceding noise calculations the supply voltage was assumed to be at its nominal value of 4.0 volts. The effect of supply voltage variations on noise threshold is significant since it provides a measure of the effectiveness of marginal testing in guaranteeing a specified noise margin. The linear behavior of the NOR gate input characteristic in the normal operating region (see Figure C-3) permits use of superposition to predict the effect of supply voltage variations. Thus, in Case 1B, a 10 percent drop in the supply voltage causes a  $0.4 \times 10^3 \times 258/4408 = 23$  mv reduction in  $V_N$ . Due to the lower collector current  $V_{ON}$  will also be reduced from 770 mv to 766 mv (allowing for a 10 percent reduction in  $I_B$ ). The noise threshold is consequently reduced by a net amount of 19 mv. If the calculated noise threshold of 68 mv at 25°C is correct, the logic should operate until the supply voltage reaches 2.5 volts, provided the noise threshold is not degraded by temperature gradients and the noise level is relatively low. The interface circuits are more sensitive to marginal testing due to the independence of the input (4v) and output (10v) currents.

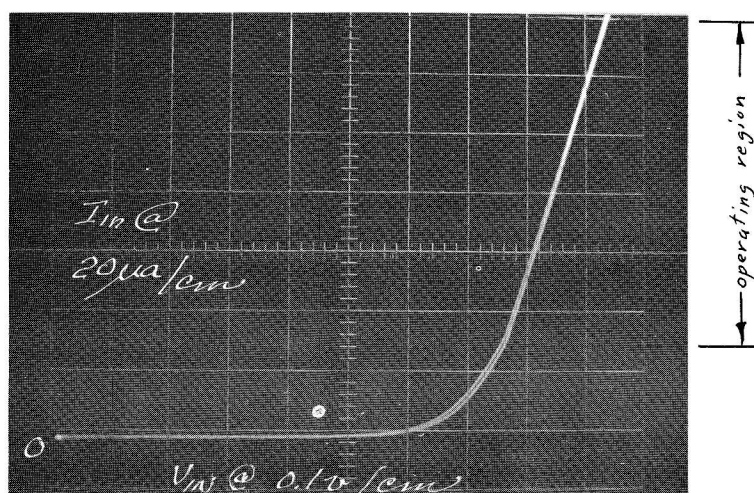


Figure C-3.  $V_{IN}$  vs.  $I_{IN}$  Characteristics





No allowance was made for temperature gradients between logic elements in the preceding noise threshold calculations. The maximum difference in case temperatures plus the junction to case variations due to logic state and usage must be considered. The gate expanders have a minimum dissipation of zero due to the absence of collector resistors. A dual gate with all six inputs true can dissipate as much as 17 mw. At  $200^{\circ}\text{C}/\text{watt}$  the junction to case temperature can be a maximum of  $200 \times 0.017 = 3.4^{\circ}\text{C}$ . Thermal analysis of the Block II magnesium structure made by Raytheon engineers indicates that the maximum difference in case temperature, between elements in different modules, is about  $10^{\circ}\text{C}$ . Hence the difference in junction temperatures can be  $13$  to  $14^{\circ}\text{C}$ , thereby reducing the previously calculated noise thresholds by approximately 24 mv if the worst-case gate configuration is adversely located in the computer. The net noise threshold for F. O. = 6 is then 44 mv at  $25^{\circ}\text{C}$ , -10 mv at  $0^{\circ}\text{C}$ , and -18 mv at  $75^{\circ}\text{C}$ . The negative noise threshold indicates the logic circuits cannot be guaranteed to operate, even in a noise-free environment, if worst-case elements are used in the overloaded groups of gates and these gates are unfavorably positioned with regard to temperature differentials. With normal loading, F. O. = 5, the inclusion of a  $13.5^{\circ}\text{C}$  temperature differential lowers the noise threshold to 24 mv at  $0^{\circ}\text{C}$ , 81 mv at  $25^{\circ}\text{C}$ , and 20 mv at  $75^{\circ}\text{C}$ .

The noise margin provided by these thresholds depends on the noise level to which the critical circuits are exposed. In the absence of a detailed noise analysis, the effective noise margin can be estimated by calculating the noise generated by selected noise sources. One source of noise is the difference in IR drops in the Malco pins that connect individual modules to the tray. Assuming a maximum resistance of  $0.01\Omega/\text{pin}$ , the maximum drop across four paralleled pins at a current of 120 ma is 0.3 mv, hence the noise due to variations in these drops is insignificant. DC drops in the tray and in the ground plane of the multilayer boards are also expected to be insignificant; however, pulse noise in the order of 10 mv is likely to be found between remote ground points. Inductively coupled noise can be significant when large currents with fast rise or fall times are routed through small size conductors which parallel micrologic signal leads for considerable distances. This source of noise is considered in some detail in the following paragraphs.

When printed wiring is employed for interconnections it is common practice to use wide lines to reduce the  $L di/dt$  drop for large amplitude signals having fast rise or fall times. A ground plane located in close proximity to the signal layers is also commonly used to effect a further reduction in lead inductance. In the Apollo computer, No. 28 AWG wires are used for all signal leads and they may be spaced a considerable distance from the ground plane (tray), hence crosstalk due to mutual inductance between signal conductors must be considered a potential source of significant noise.

The free air inductance of a No. 28 ga wire is calculated to be  $0.445 \mu\text{h}/\text{ft}$ . For  $di/dt = 1\text{A}/\mu\text{s}$ , or 10 ma/10 ns, the inductive drop along such a wire is 37 mv/in. The coefficient of coupling to an adjacent No. 28 ga wire, spaced one wire diameter, is



estimated to be 0.4. Hence an induced signal of 15 mv/in is conceivable. The CT/ signal is used as an example in the following analysis, which is an attempt to estimate the effectiveness of such a signal conductor as a noise generator.

The wire wrap routing of CT/, together with the loads within each module, is shown in Figure C-4. To simplify the analysis the connections to A13 and A24 are ignored, the load in A3 is lumped with that in A2, and the distributed load in A7 is assumed to be lumped at midpoint of the 11.5 inches of jumper wires interconnecting pins on A7. The resulting equivalent circuit is shown in Figure C-5.

For the steady-state condition indicated, the current (i) is 4.9 ma and the voltage across the load is 0.954 volts. At  $t = 0$ , the switch is closed and the current decays exponentially towards -9.6 ma with a time constant of 9.1 ns, as shown in Figure C-5. The current reaches zero at  $t = 3.0$  ns. During the decay of current the voltage across the lead inductance decays from an initial value of 0.754 volts to a final value of 0.5 volts. The voltage gradient is shown in Figure C-5 to a scale of mv/in of conductor. Assuming a coupling coefficient of 0.4, it is evident that a peak noise signal of 25 mv/in of exposure can be induced in neighboring conductors. Typical resistor values, not worst case, were used in the equivalent circuit; thus the voltage gradient could be 20 percent higher than calculated. This voltage gradient is not regarded as unusual, rather it should be regarded as a fairly typical value. The characteristic of the CT/ signal that makes it a serious noise hazard is the energy in the noise pulse. The high value of  $I^2L/2$  which gives rise to this characteristic results from driving a concentrated load through a long conductor. Good design practice would require that buffers be located close to their loads, thereby minimizing the possible exposure of other signal leads and limiting the energy in the noise pulse.

The effect of the noise pulse in CT/ on neighboring conductors is not easily predicted due to the many possible variations in conductor length, loading, and load distribution. To obtain some indication of the potential noise signal thus created, the equivalent circuit of Figure C-5 was approximately simulated, using 12 inches of No. 24 ga wire spaced 3/8-inch above a ground plane. A second 12-inch length of wire, paralleling and closely spaced to the first, was used to measure the interference. The results are shown in Figure C-6. The step function driving the CT/ conductor was generated by a transistor. The fall time was adjusted to approximately 5 ns, which it is reasonable to expect from the Apollo gates in this circuit. The secondary conductor was connected to the ground plane at one end and the voltage between the other end and the ground plane was displayed on the oscilloscope. Figure C-6 shows the waveform for the open circuit condition. In Figure C-6(a) and C-6(c) the secondary conductor was terminated in 1.5 K $\Omega$  and 300 $\Omega$ , respectively, in lieu of the open circuit.

The amplitude of the noise induced in the secondary lead is seen to be about 480 mv peak. Increasing the spacing to 1/8 inch reduced the amplitude of the induced signal 30 to 35 percent. Due to the lower sensitivity of the logic elements to narrow pulses,

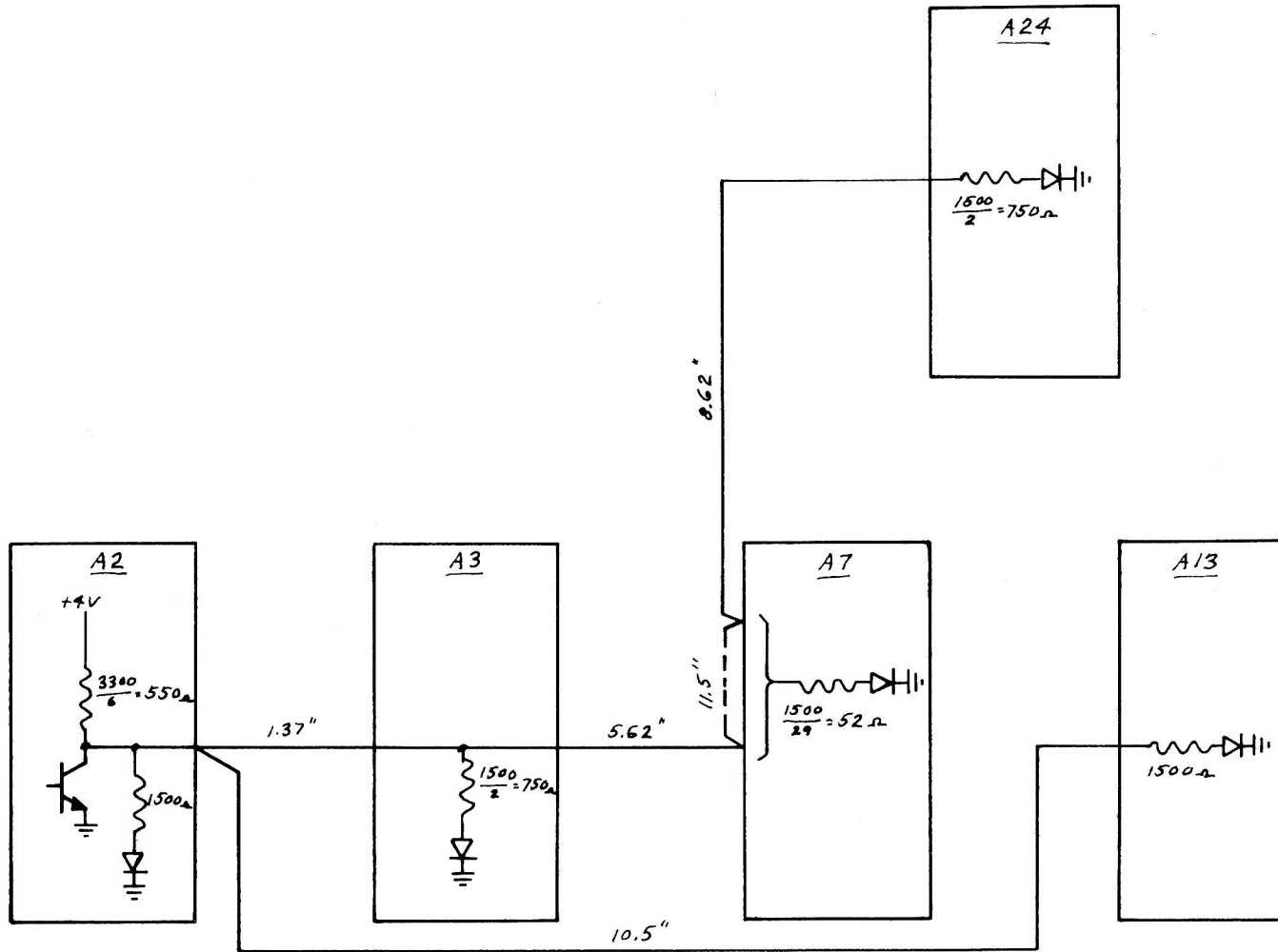
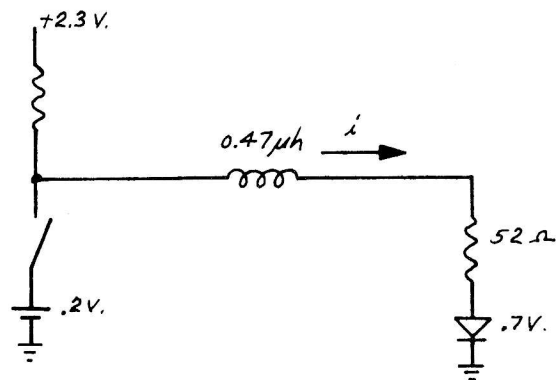
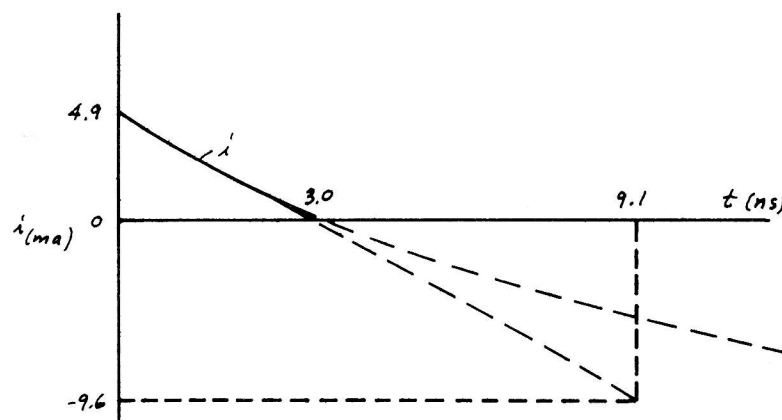


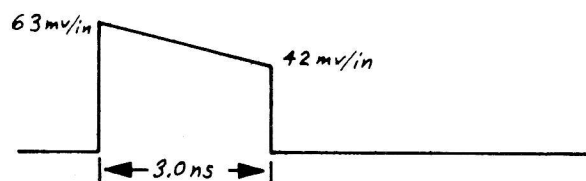
Figure C-4. Wire Wrap Routing of CT/



(a). Equivalent Circuit

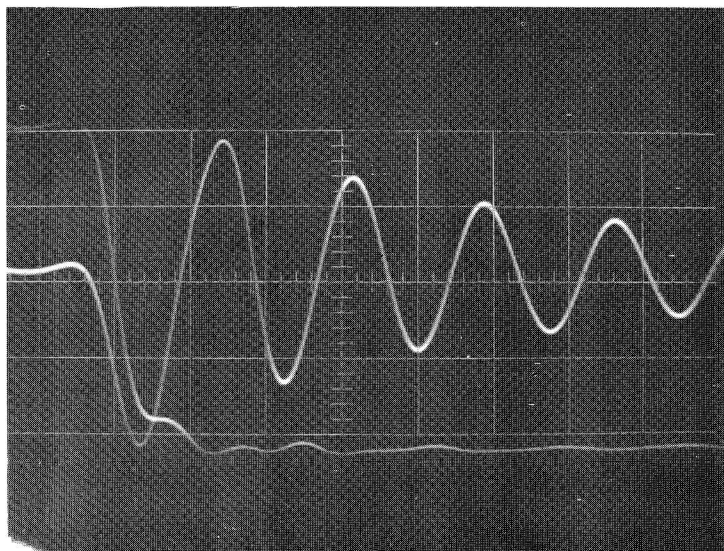


(b). Current in Signal Conductor

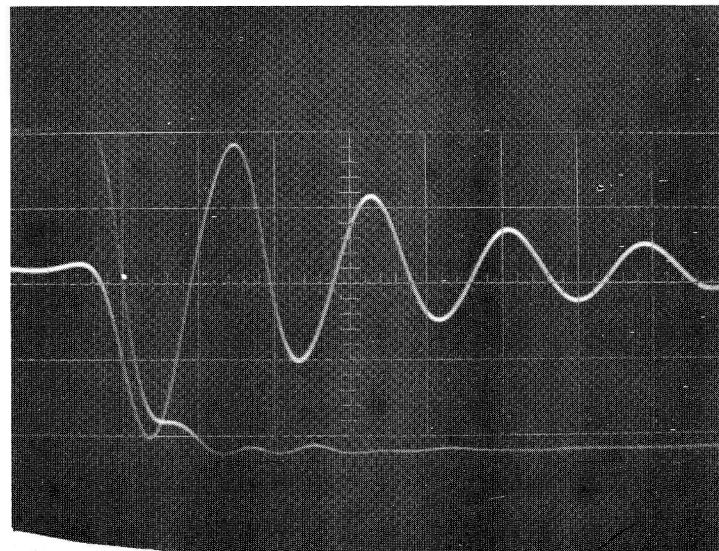


(c). Voltage Gradient in Signal Conductor

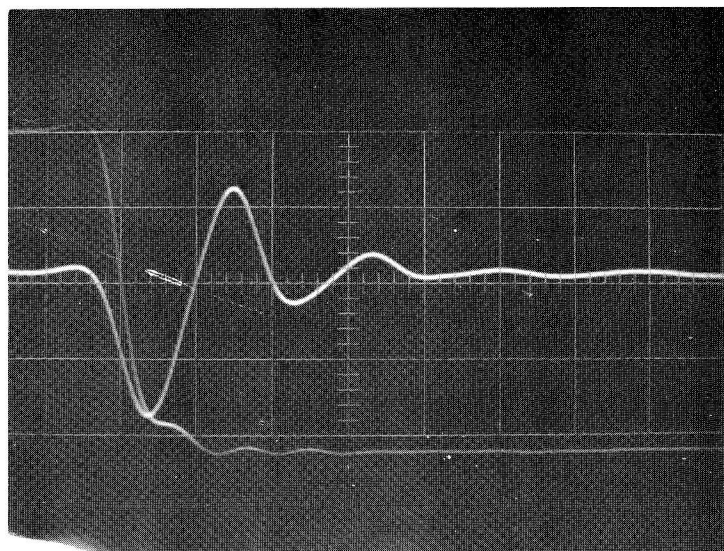
Figure C-5. Noise Generated by CT/



(a) Step Voltage on CT/ and Resulting Oscillating Transient in Neighboring Conductor --Unterminated. Scale is 200 mv/cm and 10 ns/cm.



(b) Same as (a) with 1.5 K $\Omega$  Termination



(c) Same as (a) with 300 $\Omega$  Termination.

Figure C-6. Noise Induced in Neighboring Conductor by Pulse on CT/  
Conductor Length = 12 inches



this signal is equivalent to 56 mv of dc noise. The method of establishing the dc equivalent noise is illustrated in Figure C-7. The dc threshold control, which applies a positive bias to the ground pin of gate No. 30, is used to increase the bias until the flip-flop triggers in the absence of noise. The operation is then repeated with the noise present. The difference in the dc biases at the triggering points is the equivalent dc noise.

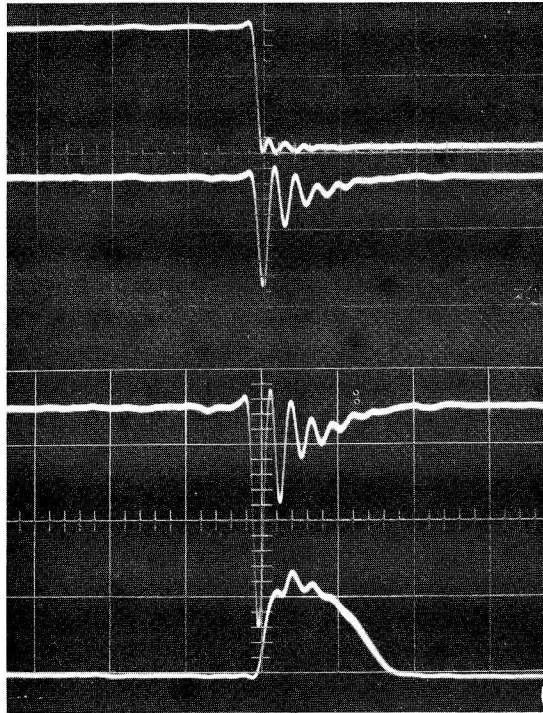
The previous experimental setup was modified slightly to measure capacitive crosstalk in a similar manner. The load was changed to a 2K resistor in series with the diode to simulate a single input to a NOR gate, and the source was changed to a 2.7K resistor to +4 volts to simulate the driving NOR gate. The equivalent dc noise was found to be 163 mv.

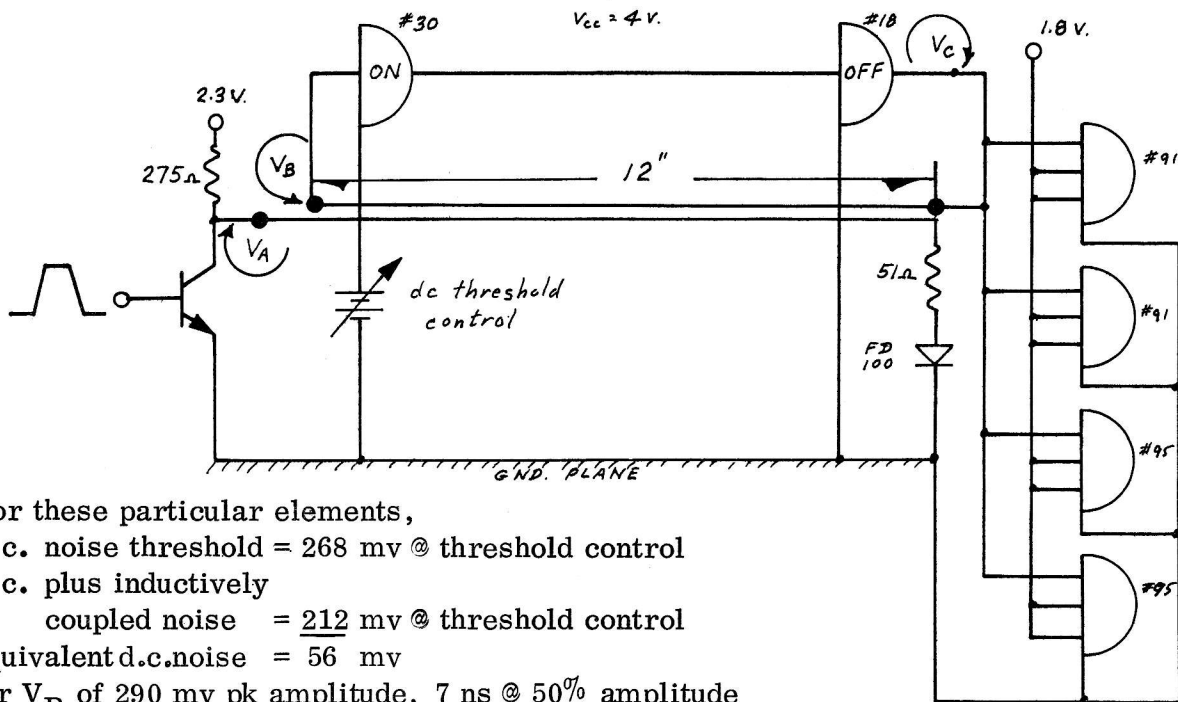
There are many leads much longer than 12 inches in the wire-wrap tray (GOJAM is 72 inches long), but the existence of long parallel wire runs has not been investigated. In the absence of any guarantee regarding the maximum value of noise due to crosstalk, it is impossible to determine the minimum required noise threshold for the logic elements.

In the absence of evidence regarding potential noise sources and the exact influence of these noise sources on the micrologic signals, the extent to which the +4 volt supply can be reduced without causing a logic failure provides a measure of the actual noise margin, for the specific operating conditions, and a measure of the noise threshold in general. The reliability of this method of measuring the noise margin is open to question since it does not necessarily provide for worst-case number sensitivity, worst-case temperature gradients, or activity of worst-case noise sources. Furthermore, varying the +4 volts supply also affects the noise level. For example, if the +4 volts supply is lowered by 10 percent, the noise induced in the secondary conductor (Figure C-8) drops about 7 percent. Thus, the use of voltage margining to measure noise margin requires a detailed knowledge of the characteristics of the noise sources and their behavior with varying supply voltage.

If the noise level is kept low with respect to the noise threshold, by careful design and layout, and if a sufficiently elaborate test is devised to insure that all of the overloaded logic circuits are stressed to worst-case conditions during environmental stress with the logic operating on 2.8 volts or less, then the noise threshold can reasonably be believed to be greater than 50 mv. It cannot be guaranteed that all computers will pass such a test, hence this approach is a gamble based on the statistical distribution of elements minimizing the possibility of a worst-case combination occurring. The problem of measuring the noise margin remains even if all violations to the logic rules are removed. This change will only guarantee a noise threshold of 90 mv at 25°C, or about 45 mv at the temperature extremes; and still requires an analysis to establish the noise margin.



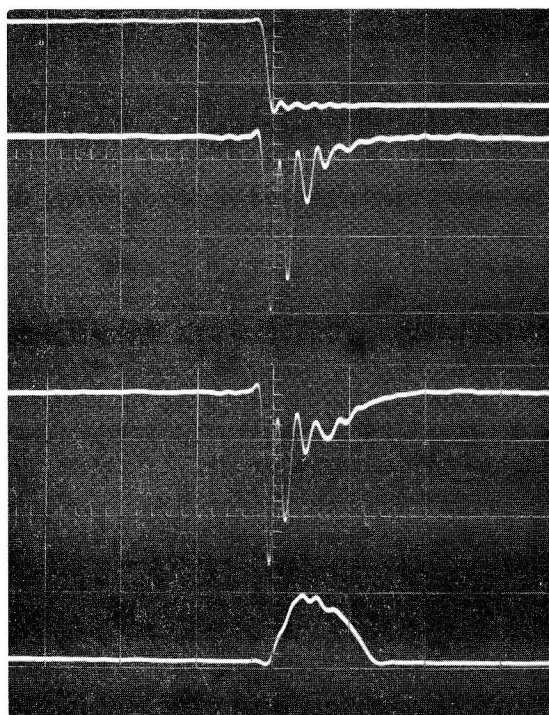

 $V_A @ 0.5 \text{ v/cm}$ 
 $V_B @ 0.2 \text{ v/cm}$ 
 $V_B @ 0.1 \text{ v/cm}$ 
 $V_C @ 0.5 \text{ v/cm}$ 

 "ON" Unit  $\rightarrow$  "OFF"
Philco  $\mu 7093$ 

For these particular elements,  
 d.c. noise threshold = 268 mv @ threshold control  
 d.c. plus inductively  
     coupled noise = 212 mv @ threshold control  
 equivalent d.c. noise = 56 mv  
 for  $V_B$  of 290 mv pk amplitude, 7 ns @ 50% amplitude

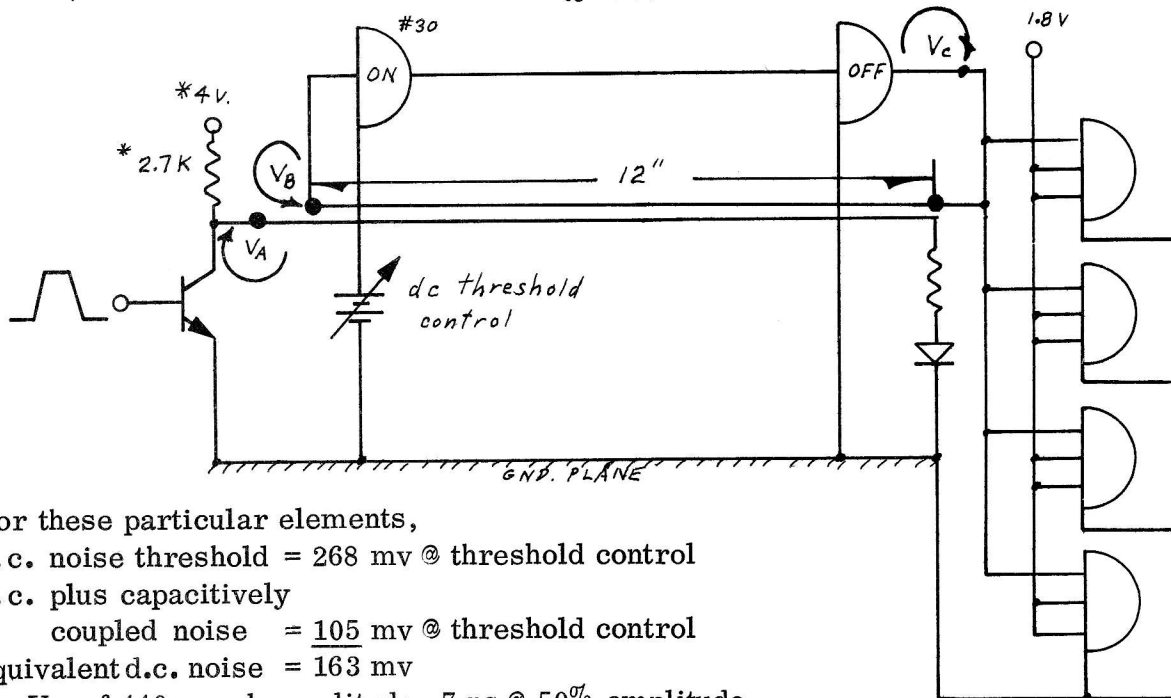
Figure C-7. Experimental Setup for Inductive Crosstalk Measurements




 $V_A @ 2 \text{ v/cm}$ 
 $V_B @ 0.2 \text{ v/cm}$ 
 $V_B @ 0.2 \text{ v/cm}$ 
 $V_C @ 0.5 \text{ v/cm}$ 

"ON" Unit → "OFF"

50 ns/cm

 Philco  $\mu 7093$ 


For these particular elements,  
 d.c. noise threshold = 268 mv @ threshold control  
 d.c. plus capacitively  
     coupled noise = 105 mv @ threshold control  
 equivalent d.c. noise = 163 mv  
 for  $V_B$  of 440 mv pk amplitude, 7 ns @ 50% amplitude

\*Circuit modifications to inductively-coupled noise circuit.

Figure C-8. Experimental Setup for Capacitive Crosstalk Measurements

APPENDIX D

LOGIC OVERLOADS

D. HOLTSHOUSE

66-159

Listed on the following pages are intermodule, overloaded micrologic signals as documented in the AGC Block 2 Computer Wirelist (revised March 23, 1966), and intramodule overloads not subjected to wirelist tabulation.

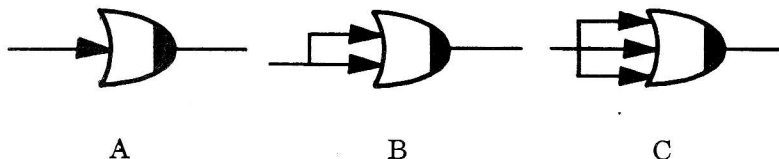
Various nomenclature has been used to facilitate overload documentation and is defined as the following:

Overload Ratio:

The ratio is the number of load units over the number of driving units as defined in NASA drawing 2005011. The wirelist defines the number of driving units to be zero if the driving signal is generated by a nonmicrologic source.

Blue Nose:

Overloaded signals driving one or more blue noses are denoted as XA, XB, or XC where X is the number of blue nose loads and A, B and C are defined as:



Non-micrologic  
Signal From:

Driving signals not generated by micrologic are indicated here.

A1-A29:

The modular location of each overloaded signal is indicated by entries under the appropriate A module heading with each entry representing the number of modular pins connected to the overloaded signal. Asterisks indicate driving signals.

Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
A2XG/	80/75									1*	4	4	4	4														
CAG	80/75									1*	2	2	2	2														
CBG	80/75									1*	2	2	2	2														
CCHG/	55/50																		3	1		1			1	2	1*	
CCH34	80/75																							2	1*			
CCH35	80/75																							1	1*			
CGG	85/75									1*	4	4	4	4	1													
CLXC	85/75								1*		4	4	4	4														
COG	80/75									1*	2	2	2	2														
CT/	175/150				1*	1				10						1											1	
CUG	165/150									2*	4	4	4	4														
CZG	80/75									1*	2	2	2	2														
DBLTST	5/0		Interface																									
DE033	25/0		Interface																									
DE034	25/0		Interface																									
DOSCAL	5/0		Interface																									
DV1	27/25						1*	2																				
EVNSET/	105/100				8*																							

1365

Table 1 (Sheet 1 of 8). Logic Overloads

Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
EXSTO/ F10A	55/50					2*	1														1	1						
F18AX	30/25			1*																						2	1	
GOJAM	370/350	2A		1*		3*	1	1	1	1				1	1	2	4	2	3	2	2	2		1	1	1	1*	
GO1	29/25	1A									1*				1													
GO2	29/25	1A									1*				1													
GO3	29/25	2A									1*				1													
GO4/	27/24	1C									3*																	
GO5/	27/24	1C										2*			1													
GO6/	27/24	1C										2*			1													
GO7/	27/24	1C										1*			2													
GO8/	27/24	1C										2*																
G10/	27/24	1C									1	1*																
G11/	27/24	1C									1	1*																
G12/	27/24	1C											2															
G13/	27/24	1C											1	1*														
G14/	27/24	1C											1	1*														
G16/	27/24	1C												2*														
G01/	28/25	1C									2*			1														

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Table 1 (Sheet 2 of 8). Logic Overloads

Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
G09/ INOUT	27/24 29/25	1C 2A					1*	1				1	1*					1										
KYRLS L01/ L2GDG/	25/24.5 29/25 80/75								1		2*								1									1
MDT01	5/0		GSE																									
MDT02	5/0		GSE																									
MDT03	5/0		GSE																									
MDT04	5/0		GSE																									
MDT05	5/0		GSE																									
MDT06	5/0		GSE																									
MDT07	5/0		GSE																									
MDT08	5/0		GSE																									
MDT09	5/0		GSE																									
MDT10	5/0		GSE																									
MDT11	5/0		GSE																									
MDT12	5/0		GSE																									
MDT13	5/0		GSE																									
MDT14	5/0		GSE																									

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Table 1 (Sheet 3 of 8). Logic Overloads

Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
MDT15	5/0	3A	GSE																									
MDT16	5/0		GSE																									
MLDCH	10/0		GSE																									
MLOAD	10/0		GSE																									
MNHNC	5/0		GSE																									
MNHRPT	5/0		GSE																									
MNHSBF	5/0		GSE																									
MONPAR	5/0		GSE																									
MONWBK	5/0		GSE																									
MP1	29/25						1*	1		1								2										
MP3	28/25						1*		2																		1	
MRDCH	10/0			GSE																								
MREAD	10/0			GSE																								
MSTP	9/0			GSE																								
MSTRT	4/0			GSE																								
MTCSAI	15/0			GSE																								
NHALGA	5/0			GSE																								
ODDSET/	85/75					3*	1																					1

Table 1 (Sheet 4 of 8). Logic Overloads



Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
PC15/	27/25	1C													1*													
PO4	30/25				3*				1																1	1		
RCG/	80/75									1*	2	2	2	2														
RCHG/	85/75									2*											1					2	1	
RQG/	80/75									1*	2	2	2	2														
RZG/	80/75									1*	2	2	2	2														
SAP	5/0		Sen. Amp																									
SA01	5/0		Sen. Amp																									
SA02	5/0		Sen. Amp																									
SA03	5/0		Sen. Amp																									
SA04	5/0		Sen. Amp																									
SA05	5/0		Sen. Amp																									
SA06	5/0		Sen. Amp																									
SA07	5/0		Sen. Amp																									
SA08	5/0		Sen. Amp																									
SA09	5/0		Sen. Amp																									
SA10	5/0		Sen. Amp																									
SA11	5/0		Sen. Amp																									

Table 1 (Sheet 5 of 8). Logic Overloads

Signal	Over- load- Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
SA12	5/0	1A	Sen. Amp																									
SA13	5/0		Sen. Amp																									
SA14	5/0		Sen. Amp																									
SA16	10/0		Sen. Amp																									
SB1/	55/50				1*																						1	
SIGNX	10/0		Interface																			1						1
SIGNY	10/0		Interface																			1						1
SIGNZ	10/0		Interface																			1						1
STRTFC	30/25						1*	1																				
SUMA16/	30/25							1							2*		1		1									
T01	52/50					1*		1	1	1								1									1	
T01/	83/75					1*	1	1	2	1								1										
T03/	113/100					1*		2	2	1						2	1	1										
T04	26/25					1*				1						1												
T05	53/50					1*				1						1		2				1						
T10/	128/125					1*		1	2	1	1					1*	1	3						1				
T11	28/25					1*				1								1				1						
VNFLSH	25/24.5																			1							1	

Table 1 (Sheet 6 of 8). Logic Overloads

Signal	Over-load Ratio	Blue Nose	Non-Micro-Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25-A29
WAG/	80/75									1*	2	2	2	2														
WCH34/	80/75																								2	1*		
WCH35/	80/75																							1	1*			
WLG/	80/75									1*	2	2	2	2														
WL10/	80/75	2A				1	1					1	4		1			1										
WL12/	80/75	2A			1	1							3	2	1			1										
WQG/	103/100	1B								1*	2	2	2	2														
WSG/	83/75	1B								2*					2													
WZG/	103/100	1B								1*	2	2	2	2														
WBG/	103/100	1B								1*	2	2	2	2														
XBO	28/25																2*							1				
XB4/	82/75									2							1*	2							1	2	1	
XT1/	112/100	1C					1									1*	1*	1	1	1	2			1				

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Table 1 (Sheet 7 of 8). Logic Overloads

## INTRAMODULE LOGIC

Signal	Over- load Ratio	Blue Nose	Non-Micro- Logic Signal From	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25- A29
BR1	25/24.5	2A					X																					
CH1308/	30/25																					X						
MAINRS	30/25	1A																			X							
NAVRST	30/25	1A																			X							
WL · WT	30/25									X																		
WSCG · XB1	30/25									X																		
XB6 · WSCG	28/25									X																		
XT0 · XB1	30/25									X																		
ZIP	29/25							X																				

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Table 1 (Sheet 8 of 8). Logic Overloads

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## APPENDIX E

### TIMING SYSTEM

D. HOLTSHOUSE

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The computer is not a "clocked computer" in the conventional sense, since propagation delays are counted on to provide the proper shifts in the gating and clocking sequence. Due to the variability of the delays which are primarily a function of gate delay and board and wire capacitance, it would seem that each computer would lend itself to "tuning" under a complete set of tune regulations that check all critical signals in their worst case combination. Surely one of the first steps required to check a "tuned computer" is to verify that all critical signals having marginal timing requirements do indeed have sufficient marginality under worst case conditions (data flow, temperature extremes, etc.) No set of critical signal combinations has been, to our knowledge, generated, nor has the Review Team had sufficient time to perform such a task. A complete timing analysis is definitely required to define all timing margins. A brief review of the timing techniques may give more insight to the type of timing margins being considered.

The basic clock frequency of 2.048 mc is divided down by two Westinghouse flip flops (one of which drives the other, see Figure E-1). Read Time  $\overline{RT}$ , Write Time  $\overline{WT}$ , Clear Time  $\overline{CT}$ , Phase Four  $\overline{PHS4}$ , and Phase Two  $\overline{PHS2}$  are generated by the first Westinghouse flip flop while the second generates Ring Counter Phase A ( $\overline{RING A}$ ), Ring Counter Phase B ( $\overline{RING B}$ ),  $\overline{ODDSET}$ , and  $\overline{EVNSET}$ .  $\overline{RING A}$  and  $\overline{RING B}$  drive a ten state ring counter used to generate timing for the scalar and  $\overline{ODDSET}$  and  $\overline{EVNSET}$  drive a twelve state counter providing the "12 Action Pulses" T01 through T12. The timing relationships desired from the Westinghouses are shown in Figure E-2. Roughly, the waveforms shown represent the majority of the timing signals — but, in reality some may be longer or shorter by some fifty nanoseconds. A cursory inspection of the timing scheme developed by the Westinghouse flip flops tends to place the action pulse at the beginning of the first quadrant, rather than the second quadrant, as shown in Figure E-2 by the dotted waveform. Analysis of Figure E-3 indicates that first stage switching action is dependent upon the falling clock edge as shown by the heavy lines, and that four gate delays are used to generate the falling edge of B. Additional delays by  $\overline{B}$ ,  $\overline{B'}$ ,  $\overline{RING A}$ , and  $\overline{ODDSET}$  accumulate to a total of thirteen gate delays (from the falling edge of the clock signal to the rising edge of an Action Pulse). Thirteen gate delays at twenty-four nanoseconds per gate easily provide the two hundred and fifty nanosecond slip that places the front edge of an Action Pulse in quadrant two instead of one.

We do not have a clocked computer in the conventional sense. The phase of a basic clocking signal (Action Pulse) is a function of propagation delays and the accuracy of the phase adjustment depends upon how well the actual propagation delays compare with the anticipated ones.

Figure E-3 contains a reasonably accurate sketch of the basic timing waveforms derived directly from the logic and with delays based on the slowest switching times of twenty-four nanoseconds per gate. For the slower switching speeds, the phases are arranged

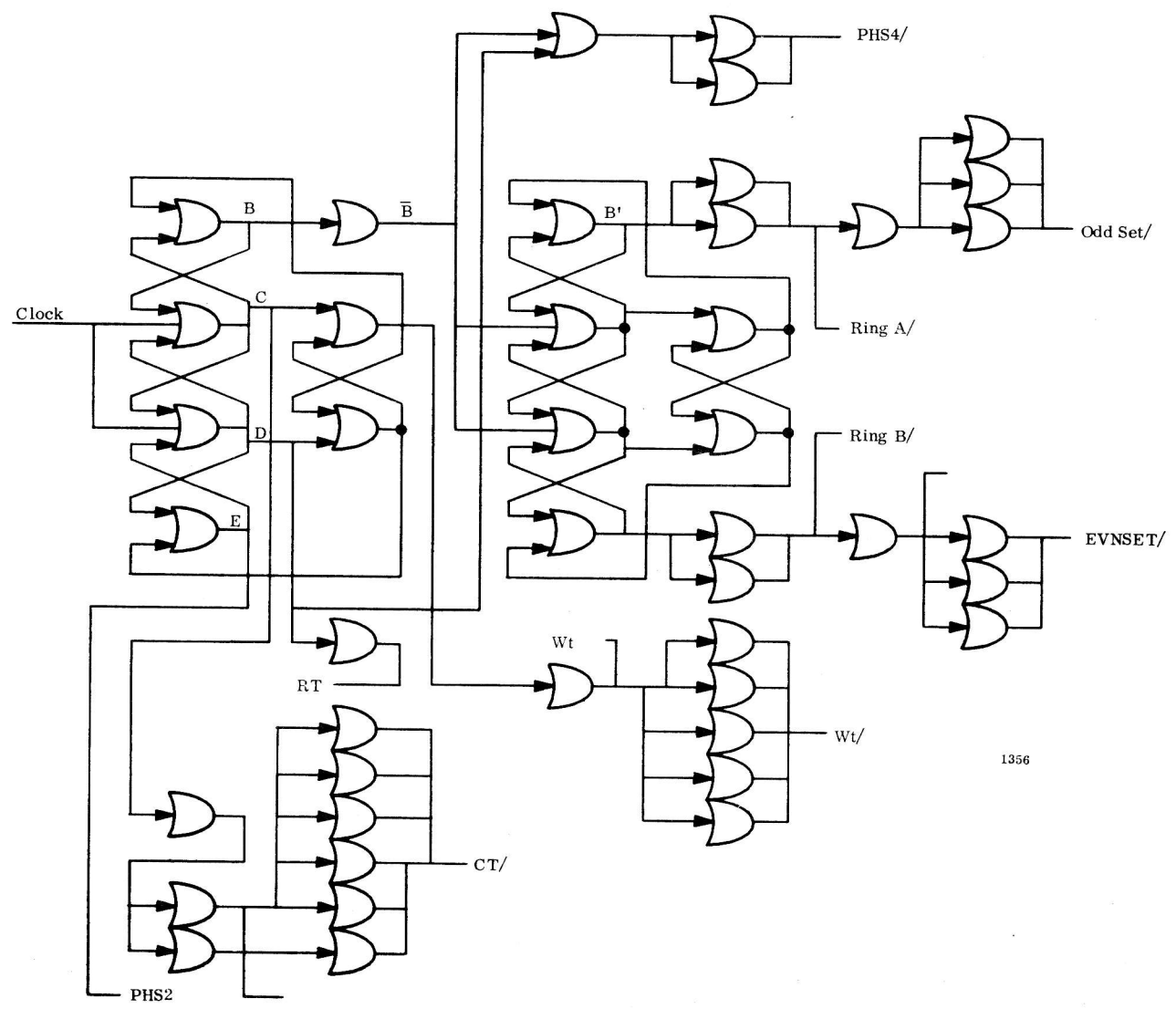
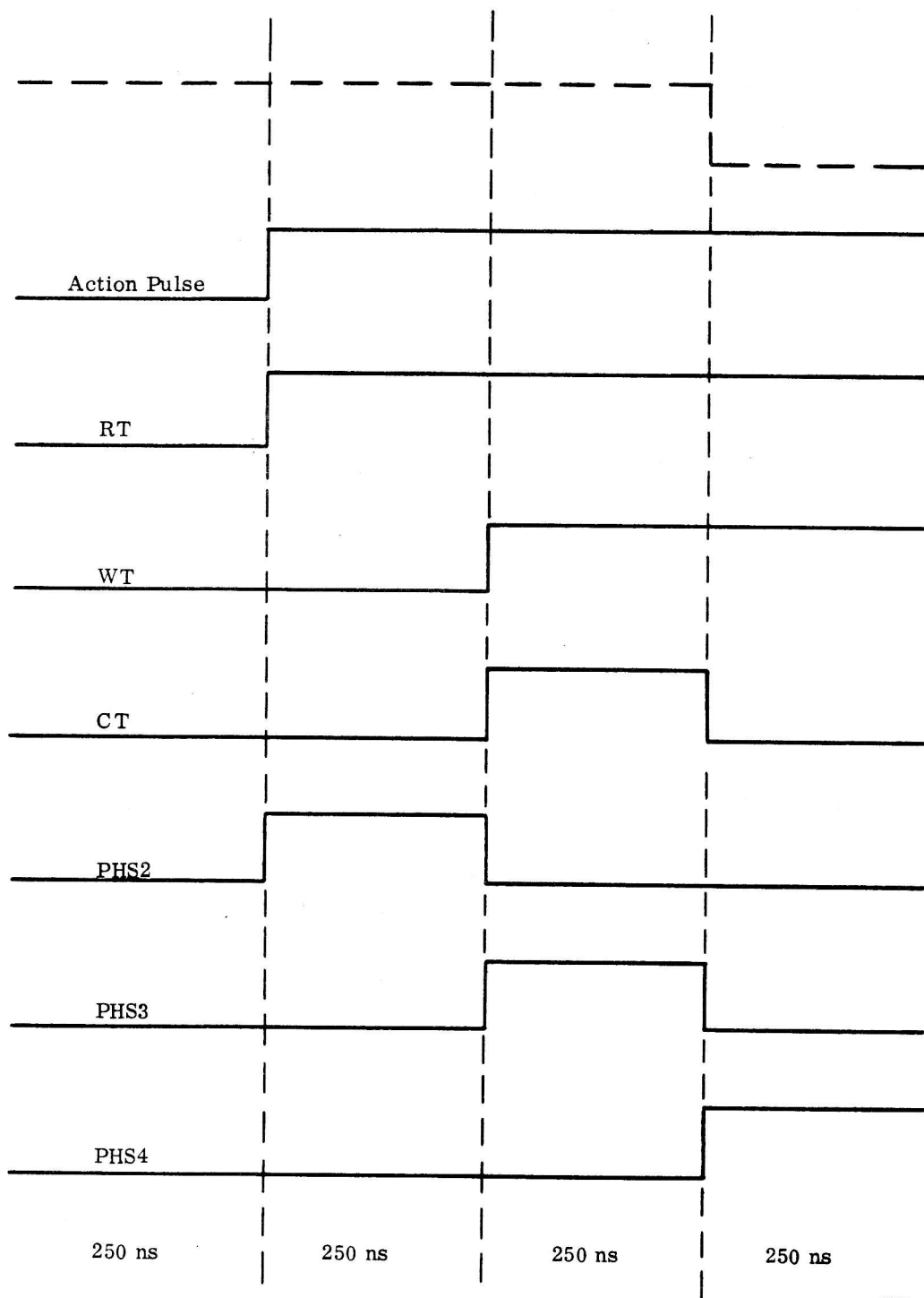


Figure E-1. Westinghouse Divider



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Figure E-2. Phase Relationships

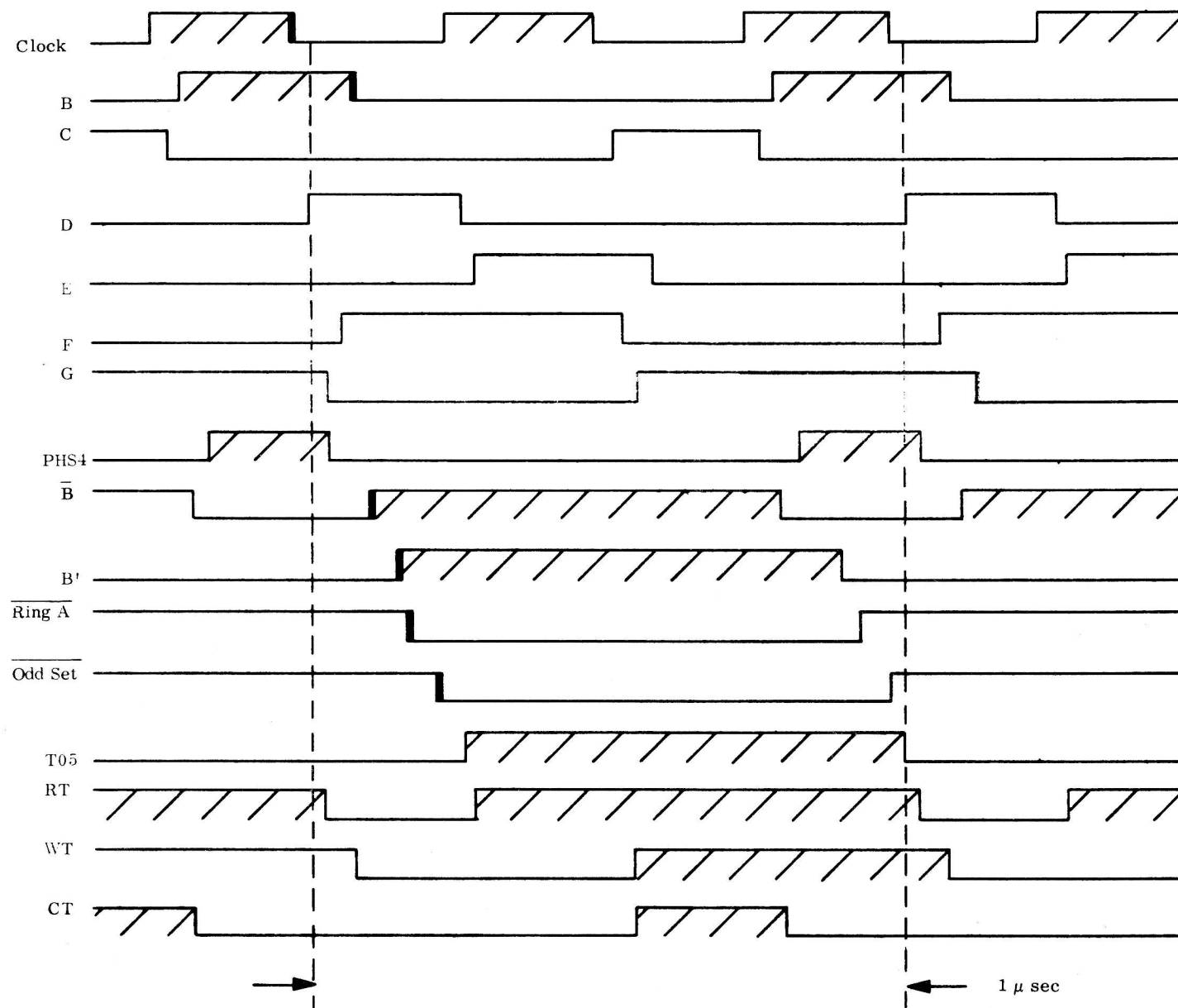


Figure E-3. AGC Timing

almost exactly as they appear in the desired phasing illustrated in Figure E-2. Worst case analysis to demonstrate timing margins assumes that all gates do not provide identical propagation delays but that some gates are faster than others. Using a worst case analysis on any Action Pulse (say T12) is appropriate because the number of gate delays used in generating the pulse is higher than the other basic timing signals (13 to 4). T12 is also appropriate because of the requirement that it be "anded" with PHS4 to generate an INKL set signal in A21 (Figure E-4). If the gate delays that are independent of PHS4 (the last 8 of the 13 gate delays for T12 occur after  $\bar{B}$ ) switch at the faster rate of twelve nanoseconds, T12 and PHS4 will shift away from each other by seventy-two nanoseconds and reduce their overlap from one-hundred and seventy-five nanoseconds to approximately one-hundred nanoseconds (Figure E-5). Whether the reduced signal overlap is sufficient to properly gate the INKL set signal depends upon many of the worst case variables to be generated in a timing analysis.

Another example can be used to show phase shifting due to fast gates switching at twelve nanoseconds. Figure E-6 illustrates the necessary gating to generate a signal  $\overline{WLG}$  enabling data to be written into the L Register. Figure E-7 details the number of delays accumulated from the falling edge of the clock pulse until the data is entered in the L Register. Using the slower switching speed,  $\overline{WLG_S}$  and  $\overline{CLG2G}$  are in phase on paper and the effective write time ( $\overline{WLG} \overline{CLG2G}$ ) is approximately three-hundred nanoseconds (Figure E-8). Using the faster switching speed of twelve nanoseconds per gate,  $\overline{WLG_f}$  and  $\overline{CLG2G}$  again are in correct phase but the faster gate combination has resulted in a shorter effective write time by approximately one-hundred nanoseconds. The shorter  $\overline{WLG_f}$  pulse has been clipped at the end by the shift in "Action Pulse T05," resulting in a similar situation that occurred on T12 illustrated in Figure E-5.

In both cases significant timing margin variations were generated by assuming extreme switching times. The constrictions, if any, placed on the computers timing margins cannot be determined until the additional effect of wire and board capacitance is considered simultaneously with maximum and minimum switching speeds under worst case signal conditions. The signals illustrated were not selected as worst case examples because the worst case signals have not yet been determined — hopefully, the detailed timing analysis will provide them. The examples do illustrate the variability introduced by maximum and minimum gates delays in the "tuned computer" and the need for the timing analysis to determine their complete effect.

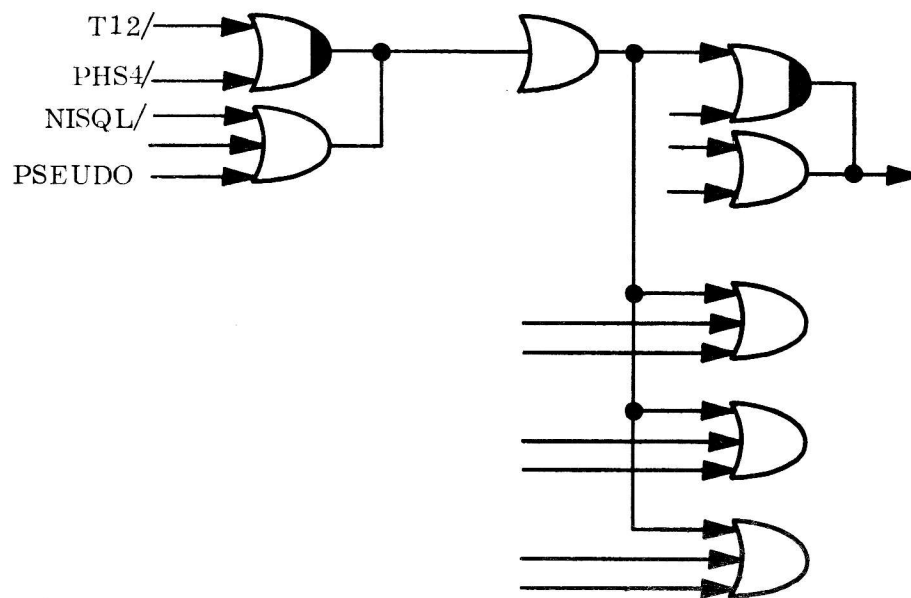


Figure E-4. INKL Set

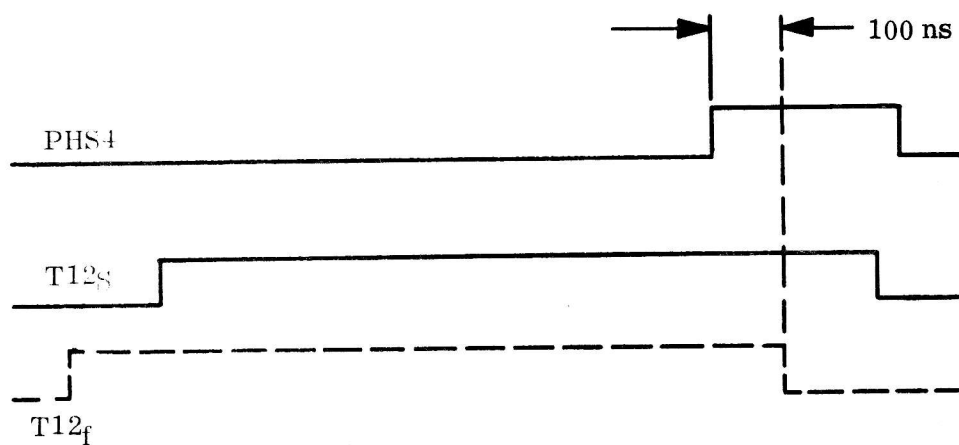
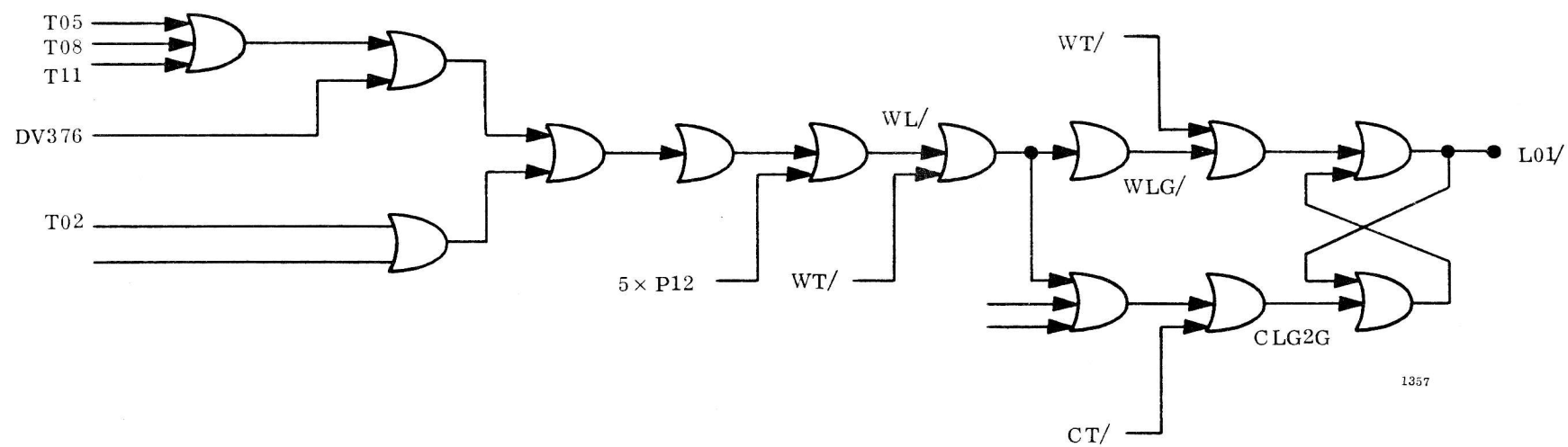


Figure E-5. Phase Slipping



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Figure E-6. Service Gates

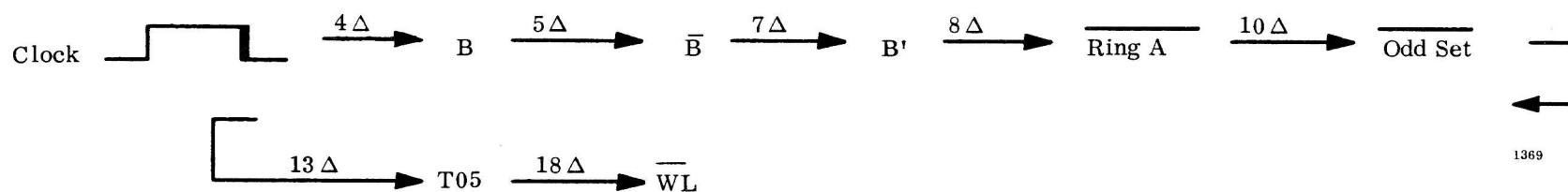


Figure E-7. Propagation Delays

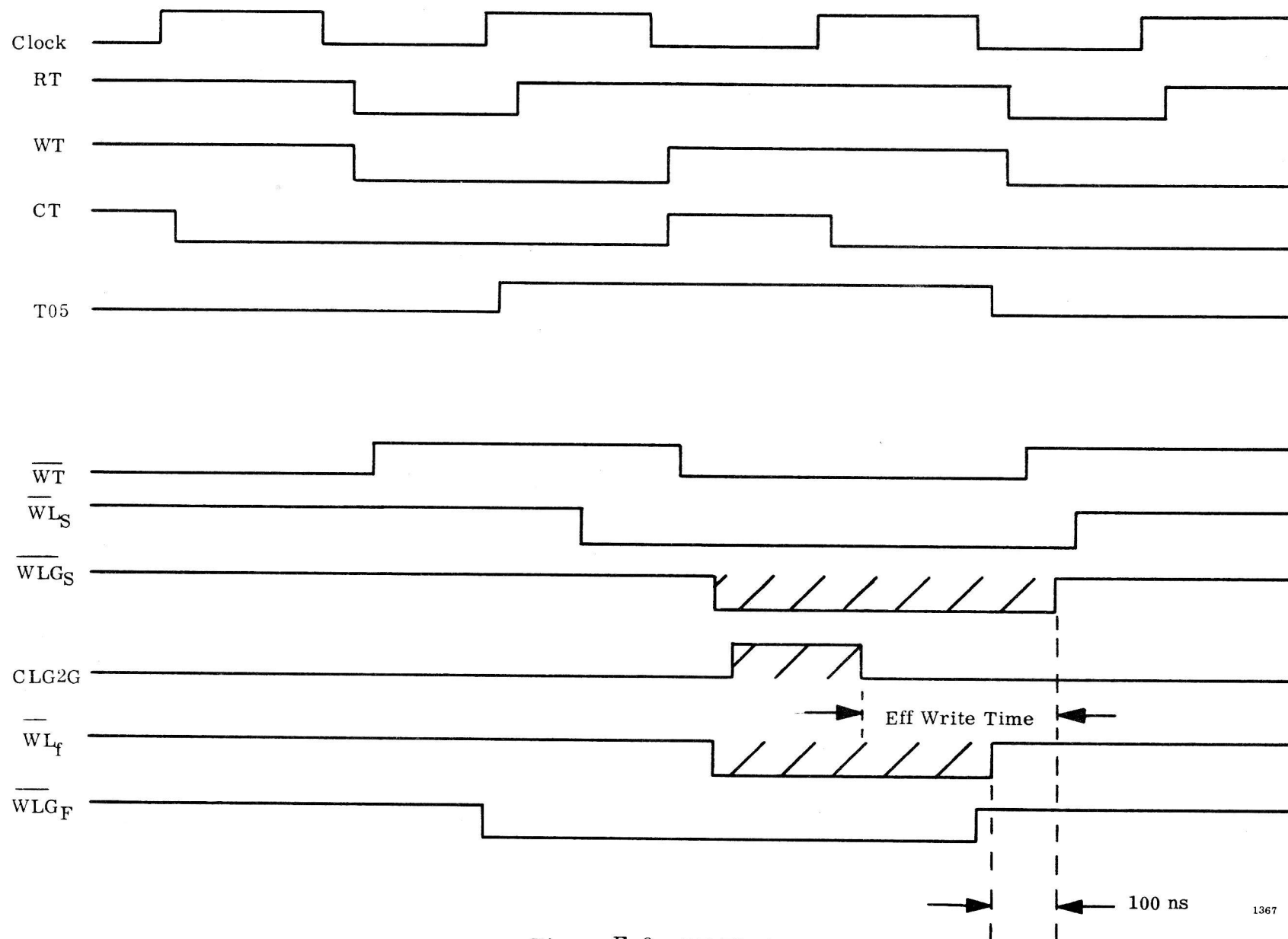


Figure E-8. CP Timing





APPENDIX F  
INTERFACE CIRCUITS  
R. C. Magraudy



## "A" CIRCUIT 2005020B

1. An analysis indicates that the input voltage at pin A is inadequate under worst case conditions. The driving source for pin A is a gate element. This gate element drives another gate and three A circuits. An exact analysis is impossible since the transistor specification is inadequate. ( $V_{be}$  is not specified at the current the transistor is used.)

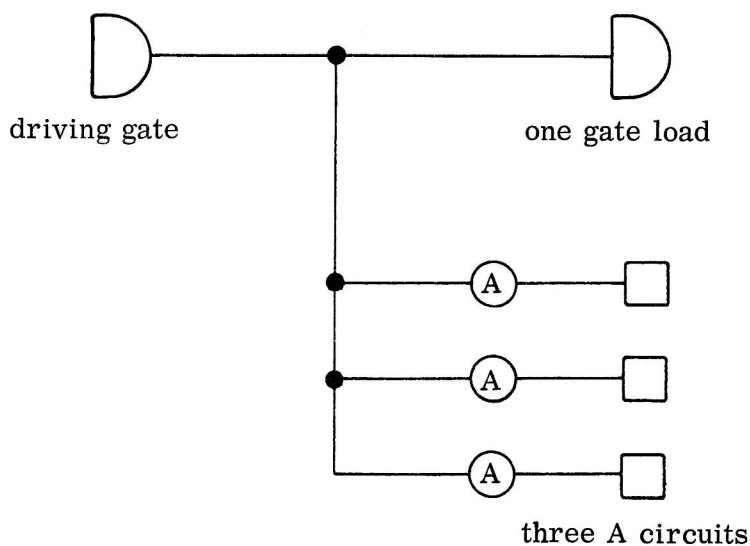
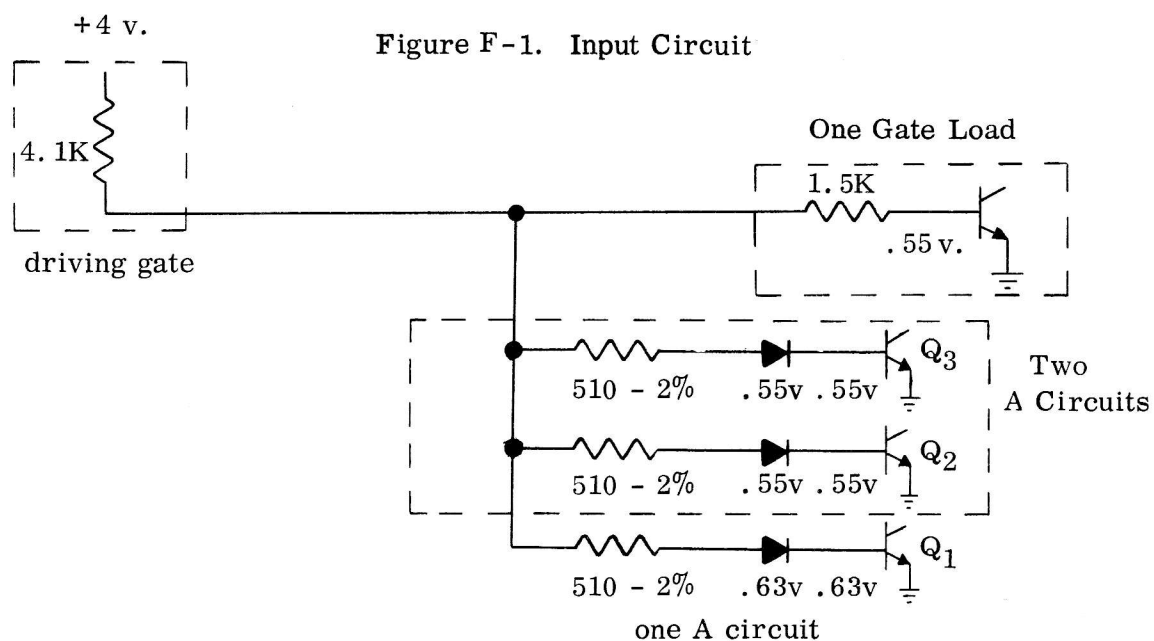


Figure F-1. Input Circuit

Figure F-2. Equivalent Circuit at  $75^{\circ}\text{C}$



At  $+75^{\circ}\text{C}$  the  $V_{be}$  and diode voltage drops are reduced by about 90 mv, or are equal to about 0.55 volts minimum and 0.63 volts maximum. Applying Thévenin's theorem the equivalent circuit reduces to that shown in Figure F-3.

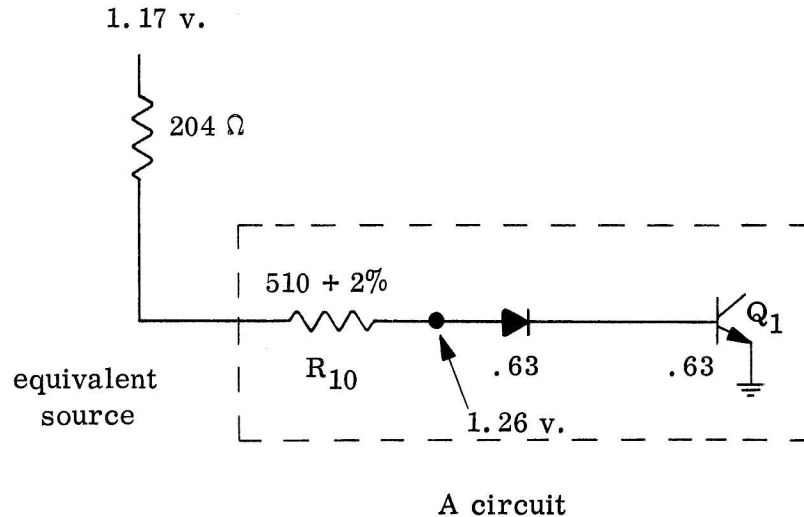


Figure F-3. Reduced Circuit

The magnitude of the voltage from the equivalent circuit is not large enough to produce a current through resistor R<sub>10</sub>. Therefore, the transistor Q<sub>1</sub> will not turn on.

2. Paragraph 5.0 of Factory Test Plan 187196 indicates that upon changing the power supply voltage and ambient temperature, the circuit specifications should remain the same. The changes in C3 and C4 could be as great as 12 percent at  $70^{\circ}\text{C}$ . This alone would cause the circuit to fail to meet its specifications. The low temperature specification in Paragraph 5.2.2 specifies the input voltage at  $12.2 \pm 0.1\text{V}$ . Lowering the input voltage to this value could bring the zener diodes, CR7 and CR9, out of conduction. The purpose of this test is questioned.
3. The width of the pulse produced by the "A" circuit is a function of many component parameters. It is understood that C3 and C4 are selected, in order to make possible the selection of R7. Care should be taken to assure adequate selection procedures. Unfavorable combination of parameters might still make the selection of R7 impossible within the constraints of the table on 2005020B. For example, the voltage pin V can vary between 13 and 11.8 volts, the turns ratio of T<sub>1</sub>



can vary  $\pm 3$  percent, the winding resistors of T1 can vary  $\pm 2$  percent, diode drops can vary, and R14 can vary  $\pm 2$  percent.

4. Pin 2 of transformer T1 is referenced to a positive voltage. This voltage is obtained via a voltage divider across a forward biased diode and is, therefore, a fixed fraction of a diode drop

$$\left( \frac{R3}{R26 + R3} \times V_{\text{DIODE}} \right)$$

Since the forward voltage drop of CR1 must be exceeded before current flows into C3 and C4, the input threshold voltage is

$$V_{\text{DIODE}} - \left( \frac{R3}{R26 + R3} \right) V_{\text{DIODE}}$$

Where it is assumed that the forward voltage drop across CR1 equals the forward voltage drop across CR3. Or

$$V_{\text{THRESHOLD}} = \left( 1 - \frac{R3}{R26 + R3} \right)$$

Where  $R3 = 1000 \Omega$ ,  $V_{\text{THRESHOLD}} = 1/3 V_{\text{DIODE}}$  and from  $25^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  the threshold would change about 30 mv. If  $R3 = 510\Omega$  the threshold would vary 45 mv from  $25^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

#### XT CIRCUIT 2005020B

The XT circuit contains transformer 1006319. This transformer is tested under conditions similar to the conditions in the test specification for the XT circuit. There is one important difference, however. The period of the pulse train in the transformer specification is greater than the period of the pulse train may be in the XT circuit specification. The duty cycle of the signal driving the transformer is such that there exists a net dc current through the primary. Since there is no specification imposed on the maximum tolerable primary direct current component, no firm conclusion can be drawn about the circuit. Although the circuit specification causes more dc primary current to flow than the transformer specification, the worst-case condition exists where the transformer is used to produce the sync signal (page 10 ICD No. LIS 370-10004). Here the repetition rate is  $1.024 \times 10^6$  cycles per second, and the pulse width is  $0.5 \pm 0.25 \times 10^{-6}$  seconds.

It is difficult to determine if the effects of this high dc current are detrimental. Among the effects are: (1) the transformer will saturate during the cycle causing the output pulses to be shorter than the input pulses; (2) the higher than normal currents will cause the transistor to dissipate higher than normal power; and (3) a larger than normal output pulse results from the high dc currents.



To determine these currents, the following equivalent circuits were used.

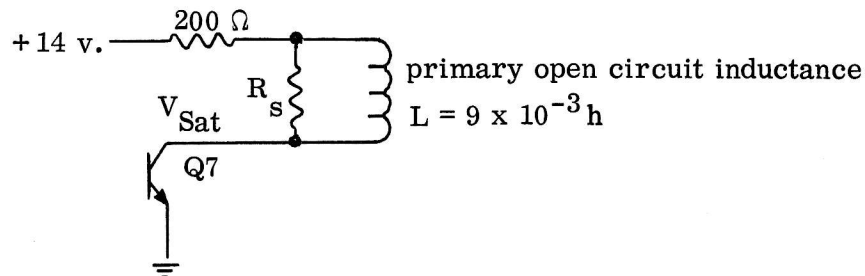


Figure F-4

$R_s$  is the secondary load reflected to the primary. This circuit indicates the conditions during the time that Q7 is saturated and the transformer is not saturated. The circuit during recovery is as follows:

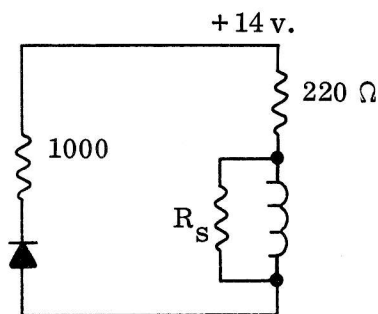
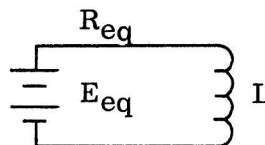


Figure F-5

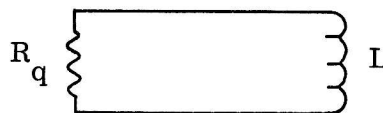
To reach equilibrium, it must be true that the increase in magnetizing current, during the time Q7 is saturated, is equal to the decrease in magnetizing current when Q7 is nonconducting. Thevenin's equivalent circuits for Figures F-4 and F-5 are:



$$R_{eq} = \frac{200 \times R_s}{200 + R_s}$$

$$E_{eq} = \frac{14 - V_{Sat}}{200 + R_s} \times R_s$$

Figure F-6. Equivalent Circuit for Figure F-4



$$\text{where } R_q = \frac{(200 + 100) R_s}{200 + 1000 + R_s}$$

Figure F-7. Equivalent Circuit for Figure F-5

The peak current  $I_p$  is

$$I_p = \frac{E_{eq}}{R_{eq}} - \left( \frac{E_{eq}}{R_{eq}} - I_o \right) e^{-\frac{R_{eq} t_1}{L}}$$

where  $t_1$  is the pulse width.

The minimum current  $I_o$  is

$$I_o = I_p e^{-\frac{R_q t_2}{L}}$$

where  $t_2$  is the time Q7 is nonconducting.

Thus

$$I_p = \frac{E_{eq}}{R_{eq}} - \left( \frac{E_{eq}}{R_{eq}} - I_p e^{-\frac{R_q t_2}{L}} \right) e^{-\frac{R_{eq} t_1}{L}}$$

$$I_p = \frac{\frac{E_{eq}}{R_{eq}} (e^{\frac{R_{eq} t_1}{L}} - 1)}{e^{\frac{R_{eq} t_1}{L}} - e^{-\frac{R_q t_2}{L}}}$$

For the case where the secondary load is  $100\Omega$ , as in the 1.024 mc sync circuit,  $R_s = 400\Omega$  and

$$R_{eq} = 133$$

$$E_{eq} = 9.2V$$

$$R_q = 300$$

Where the period is  $0.5 + 0.25 \mu s$  and the rate 1.024 mc



$$t_1 = 0.75 \times 10^{-6} \text{ secs}$$

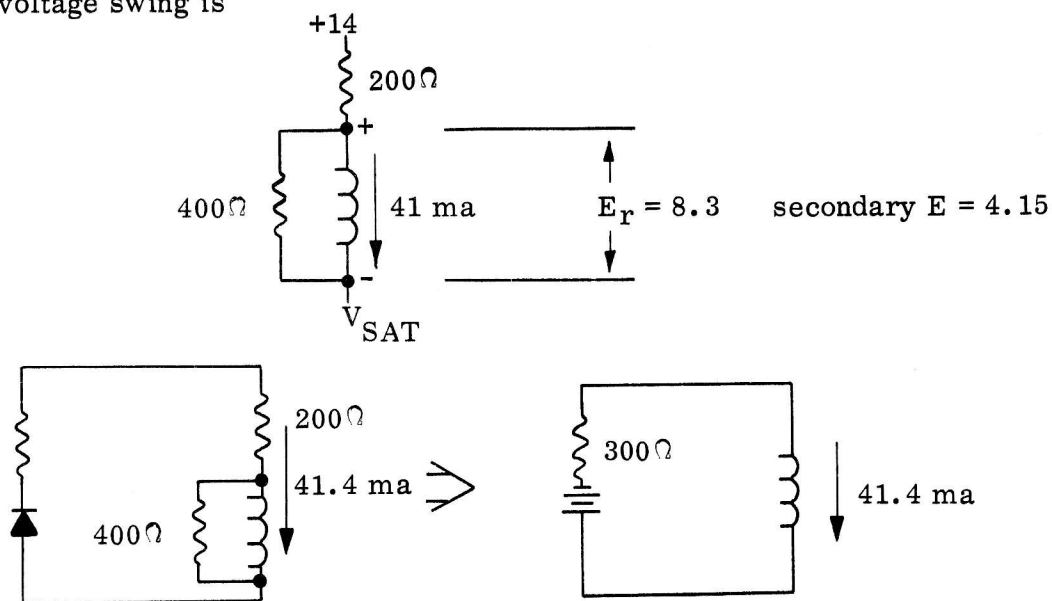
$$t_2 = \frac{10^{-6}}{1.024} - 0.75 \times 10^{-6} = (0.976 - 0.75) \times 10^{-6}$$

$$t_2 = 0.226 \times 10^{-6}$$

$$I_p = 41.4 \text{ ma}$$

$$I_o = 41.0 \text{ ma}$$

Thus the total voltage swing is



$$300 \times 41.4 \text{ ma} = 12.42$$

$$E = 12.42 + V_d \approx 13V$$

$$E \text{ at the secondary} = 6.5V$$

$$\text{Total swing} = 6.5 + 4.15 \approx 10.7 \text{ volts}$$

The  $\beta$  of the transistor is between 30 and 40 minimum at  $25^\circ\text{C}$  (assuming  $\beta = 40$ ), then at  $0^\circ\text{C}$   $\beta = 34$ ,

$$I_b = \frac{4V - 0.7V}{4.1K} = \frac{3.3}{4.1K} = 0.805 \text{ ma}$$

$$\beta I_b = 27.4 \text{ ma}$$

This implies that the transistor cannot support 40 ma under the worst-case conditions. Thus, the pulse width will decrease and transistor dissipation increase. But maximum



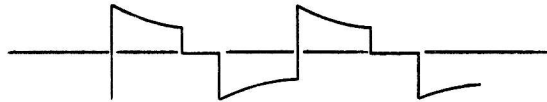


dissipation

$$\leq \frac{(7)^2}{200} = 245 \text{ mw}$$

Most likely the dissipation would be about 1/2 of this. In either case the ratings of the transistor will not be exceeded.

In conclusion, tests should be made to the **XT** circuit that reflect the actual usage. For the case examined, the output voltage will have the following shape



where the flat part of the output voltage indicates where  $\beta I_p$  = magnetizing + load current. If further tests are not imposed on the circuit then additional requirements must be imposed on the transformer.



APPENDIX G

BLOCK II DSKY: HIGH TEMPERATURE

LOW VOLTAGE RELAY OPERATION

B. C. Dutcher



Reference was made to the drawings: 2005918, 2005953, 2005952, and 1006282. The operation of a DSKY latching relay may be studied with the following definitions:

VIN	= Raw 28V power
VPS	= Drop in the power supply diode
V28	= 28V common voltage
V28L	= 28V alarm low trip point
VY	= Y-line driver drop
VX	= X-line driver drop
VR	= DSKY regulator drop (in the power supply module)
VC	= Cable drops
VD	= Series diode drop
RT	= The coil resistance at temperature T
VDSKY	= The input voltage at the DSKY

Then the DSKY input voltage is

$$VDSKY = VIN - VPS - VR - VC = V28 - VR - VC \quad (1)$$

The voltage available to set the relay is

$$\begin{aligned} VS &= VIN - VPS - VR - VC - VX - VY - VD = V28 - VR - VC \\ &\quad - VX - VY - VD = VDSKY - VX - VY - VD \end{aligned} \quad (2)$$

The effective voltage available to reset the relay, i. e., that voltage which would produce a current through RT equal to the net reset current,

$$VRS = \frac{VSX_{10}}{10 + RT} \quad (3)$$

The test voltage for the relay at room temperature (to produce the same current) must be

$$V_{TEST} = \frac{VRS RT_{25}}{RT} \quad (4)$$

The relay latching voltage is specified to be NMT 18V from -55°C to +125°C, and NMT 13V at 25°C with an operate time of NMT 10MS.



Four cases have been considered, Case I shows the original analysis. A value of  $3.9 \times 10^3$  PPM/ $^{\circ}$ C was used to calculate RT. Case II shows the results of the latest specifications VX and VY. Case III assumes a lower limit on the 28V common of 23.0V. The input under this condition may be as high as 24.2V. The alarm indication will not occur until the 28-volt common drops to approximately 21.6V. Case IV assumes the output of the DSKY regulator to be 23.0V. The 28-volt common may be as high as 24.4V and the input as high as 25.6V under this condition.

Hence, there may be a range of voltage over which the DSKY may not operate but a voltage alarm is not indicated for Cases III and IV. It should be noted that the pull in voltage for a relay which has been inactive for a period of time is generally higher than that measured under the relay test conditions. The pull in voltage may also increase after many cycles of use.

Case I

V28	=	V28L = 21.6V
VR + VC	=	1.6V
VX + VY	=	2.2V (original limits)
VD	=	0.7V
T	=	89 $^{\circ}$ C (80 $^{\circ}$ C module temperature)
R25	=	1K
VPS	=	1.2V
VS	=	17.1V
VRS	=	15.2V
V <sub>TEST</sub>	=	12.2V
(VIN	=	22.8V, VDSKY = 20.0)

Case II

VX + VY	=	1.6V (probable specification), otherwise the same as I.
VS	=	17.7
VR	=	15.7
V <sub>TEST</sub>	=	12.5
(VIN	=	22.8, VDSKY = 20.0)



<u>Case III</u>	V28	= 23.0V, otherwise the same as I
	VS	= 18.5
	VRS	= 16.1
	VTEST	= 12.9V
	(VIN	= 24.2V, VDSKY = 21.4V)

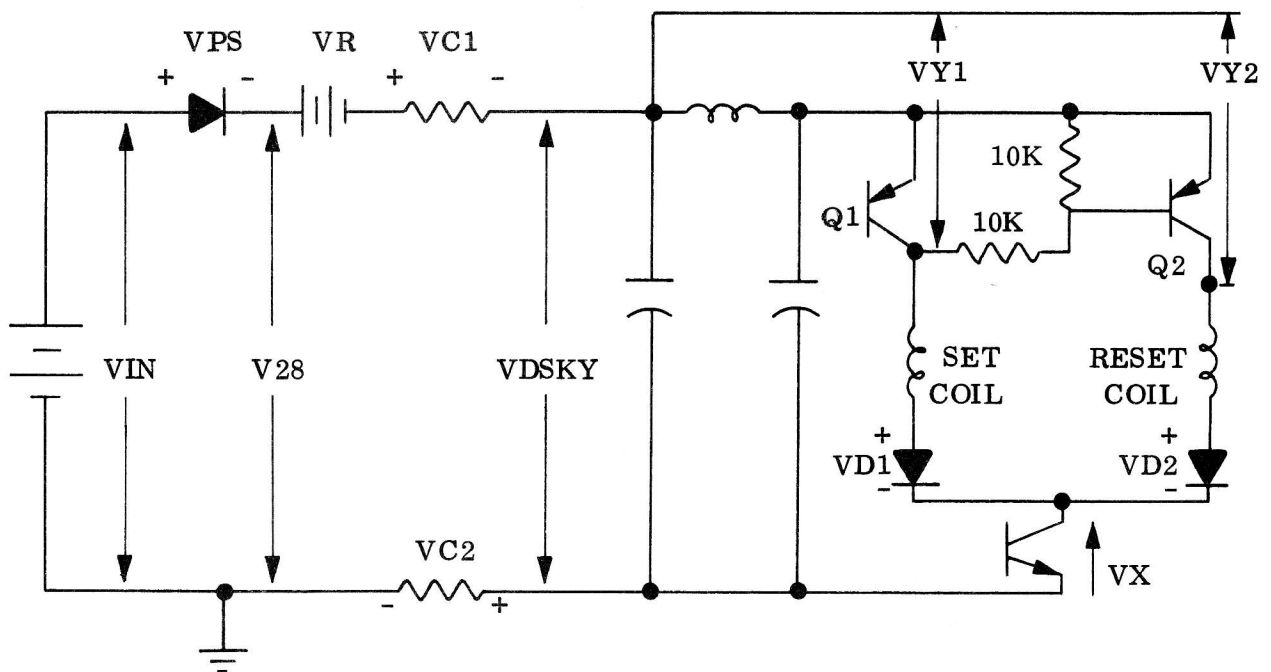
Case IV      (V28 - VR) = 23.0, VC = 0.2, otherwise the same as I

VS                = 19.7

VRS               = 17.4

VTEST           = 13.9V

(VIN               = 25.6V, VDSKY = 22.8V)



$$VC = VC1 + VC2, \quad VY = VY1 \text{ or } VY2, \quad VD = VD1 \text{ or } VD2$$

```

      SET  : Q1 ON   Q2 OFF
RESET : Q1 OFF  Q2 ON

```

Figure G-1. DSKY Relay Circuit



APPENDIX H

WORK TO BE ACCOMPLISHED

E. I. Hughes



## 1.0 INTRODUCTION

In the original design review report each of the topics reviewed by that committee was placed into one of four categories. The categories were

- A - Adequate
- B - Marginal
- C - Inadequate
- D - Indeterminate

This appendix provides a convenient cross-reference for those topics which have been placed into Categories C or D. Section 2 of this appendix details the work remaining to resolve those indeterminate items into one of the three definite categories: A, B, or C. Section 3 lists those tasks which must be done to correct presently-known deficiencies in the design. It also includes some tasks which will probably be required as a result of deficiencies determined in the continued design review listed in Section 2.

## 2.0 DESIGN REVIEW

The referenced design review report placed certain aspects of the Apollo guidance computer and associated equipments in an "indeterminate" category. This category included those items which had not been reviewed or for which considerable additional study is required before the designs can be classified as acceptable or unacceptable. Therefore, the first task is the completion of the design review to the extent necessary to resolve any indeterminacies listed in the design review report. The remainder of this section lists those specific tasks which are known to require additional design review or study. Others may develop as the review continues.

### 2.1 FUNCTIONAL ASPECTS

This task includes study of the oscillator fail alarm, the restart philosophy, and the interrupt and counter increment loading on the program.

### 2.2 MECHANICAL DESIGN

It is presently understood that NASA will specify the finish system for the airborne equipment, and it is presumed that the contractor has no responsibility for the finishes of the equipments. There are still materials compatibility and corrosion problems associated with the use of magnesium in the new computer structure. Considerable testing will be required in order to resolve this difficulty.





A thermal model of the magnesium computer has been made and loaded with dummy heat sources. That model must still be subjected to a thorough engineering evaluation.

### 2.3 POWER SUPPLY

The original review suggested the possibility of thermal runaway of one of the driver transistors. Design data was not available to support or refute that possibility. The purpose of this task is to develop that data.

### 2.4 TIMING ANALYSIS

This is a major analytical effort. Some time must be devoted to preparing a suitable plan of attack and then carrying out the analysis in detail. This analysis must be done on an operating production computer, such as C-1 or C-2, and will also require full-time use of a computer test set and a program analyzer console. Timing margins must be developed in detail at room temperature, and adequate tests must be made at the temperature extremes to determine whether the computer design is adequate.

### 2.5 ERASABLE MEMORY

Since the erasable memory drive circuits are not worst-case designed, it is necessary to develop considerable data on the magnetic core modules to determine whether conditions are favorable for a marriage of the driver circuits with the magnetics. These tests must be done over the temperature range and for core modules produced by both RCA and EMI. One operable (but not necessarily deliverable) erasable memory module from each vendor will be needed. It will be necessary, in addition, to rent time on a core memory tester at one of the vendor's facilities to accomplish the tests.

### 2.6 MEMORY DRIVER CIRCUITS

A satisfactory analysis of the design of the memory driver circuits has not been developed. The effort of this task will provide such a design analysis.

### 2.7 FIXED MEMORY MECHANICAL DESIGN

This task provides the effort to do a complete engineering evaluation of the new mechanical design for the rope modules.



## 2.8 COMPUTER INTERFACE

### 2.8.1 Signal Distribution and Grounding

It will be necessary to make a complete review of the grounding and shielding for both the command module and the Lunar Excursion Module looking outward from the computer, in order to determine if a satisfactory signal distribution and grounding philosophy exists.

### 2.8.2 Power Distribution and Grounding

The same tasks must be provided for power distribution and grounding and for determining the nature of the power sources.

## 2.9 ELECTROLUMINESCENT PANELS

The electroluminescent panels and the relays and circuits associated with those panels have been quite troublesome. An investigation will be made into the possibility of substituting incandescent segmented displays for the present electroluminescent panels.

## 2.10 SIGNAL LAYERS

Significant difficulty with the conventional multilayer circuit boards has reopened the question of utilizing the "signal layer" process for interconnecting the flatpacks. A detailed review must be made of the signal layer as compared with the multilayer boards.

## 2.11 MODULE QUALIFICATION TESTING PLAN

The recommendation of the review committee has been to cancel the present plans to do qualification testing of the computer modules. This decision should be reviewed for those modules such as the ropes, oscillator, power supply, and erasable memory, which are considered critical. If qualification testing of those modules is not provided, a thorough engineering evaluation should be substituted.

## 2.12 MISSION PROGRAMS

The computer logic design imposes severe restrictions on the mission programs, but these restrictions appear not to have been documented. Additional review is required to determine exactly what these restrictions should be and whether the programmers are abiding by them.



### 2.13 FACTORY TEST PROGRAMS

It will be necessary to make a careful review of the programs which are used during the acceptance testing of the computer. It is suspected that these programs have not been especially designed to stress the logic noise and timing situations within the computer and to provide a worst-case test for the memories. Therefore, careful review and reformulation of the program will be necessary before the actual programming effort can begin.

### 2.14 COUPLING DATA UNIT

A detailed design review of the CDU was not attempted by the previous design review committee. Therefore, a detailed review will be required. This will include the logic of the CDU's as well as an analysis of the analog-to-digital conversion circuitry, power supply, and a more careful survey of the mechanical design and thermal analysis.

### 2.15 GROUND SUPPORT EQUIPMENT

The original design review of the GSE was very superficial. A detailed review of the GSE requirements, design, and mechanization will be required.

## 3.0 DESIGN CHANGE TASKS

This section details those tasks which are required to correct those designs which have already been put into Category C: Inadequate. It will also attempt to predict which of the design reviews discussed above will result in redesign effort.

### 3.1 VOLTAGE FAILURE ALARM

This circuitry will be redesigned to cause the overvoltage condition to short circuit the outputs of the power supplies.

### 3.2 COUNTER FAILURE ALARM

The logic of this alarm is known to be faulty and a logic design change is required.

### 3.3 MAINTENANCE AND LOGISTICS

This task will include the development and documentation of a maintenance and logistics plan for the computer. This plan will include the process of recertification of a repaired computer.



### 3.4 MECHANICAL DESIGN

Several minor problems exist in the present mechanical design. The cover of the computer cannot stand the pressurization. The rope header vibrates with a high Q. These must be corrected.

### 3.5 POWER SUPPLY CIRCUITS

The power supply must be redesigned to include the overvoltage protection circuit which is driven by the voltage alarms. Additional engineering effort is required to reduce the noise output of the power supply to an acceptable level.

### 3.6 LOGIC NOISE MARGIN

This task includes the effort needed to determine the actual margins between the noise thresholds of the logic circuits and the noise voltages which will be produced in this computer. This work must be accomplished on a production version of the computer. Analyses must be made at the temperature extremes as well as at room temperature. Logic overloads in the existing design must be eliminated and circuits must be reallocated among the various computer modules to eliminate the bad noise generating situations. It will also be necessary to rewrite portions of the wire-wrap program to include the electrical constraints determined by the engineers doing the redesign of the logic.

### 3.7 TIMING MARGINS

Task 2.4, Timing Analysis, will probably result in some redesign of the computer logic to correct marginal timing situations. This task (3.7) covers the work to accomplish that redesign. The redesigns must be tested experimentally on a computer.

### 3.8 STANDBY LOGIC

This task includes the effort to redesign the logic of the standby flip-flop and of the standby indicator.

### 3.9 ERASABLE MEMORY MODULE

There are two independent efforts to be performed under this task. The first is a new mechanical design of the module such that it can tolerate both the temperature shocks and sustained vibration. The second effort is the result of the electrical evaluation of the module, covered under Task 2.5. It will be necessary to revise the core and module procurement specifications to correct any design deficiencies of the erasable memory. The two designs need not be accomplished using identical modules.



### 3.10 MEMORY CIRCUITS

The worst-case analysis of the memory selection and sensing circuits (Task 2.6) will probably result in minor circuit modifications. This task will cover those modifications.

### 3.11 FIXED MEMORY MODULE

Task 2.7 provided an exploratory environmental test of the fixed memory module. This task covers any redesign which results from that engineering evaluation.

### 3.12 OSCILLATOR

The oscillator circuit presently uses parts which cannot be qualified to the flight environment. This task includes the effort needed to redesign the oscillator to remove those parts from the circuit.

### 3.13 INTERFACE CIRCUITS

The only effort presently envisioned under this task is a minor redesign of the synch input to the "A" circuit. This input presently overloads the micrologic driving it.

### 3.14 INDICATOR DRIVER MODULES

These DSKY modules contain the latching relays which drive the electroluminescent panels. Regardless of the outcome of Task 2.9, which re-examines the decision to use the electroluminescent panels, some redesign will be necessary in the indicator driver modules. This task is intended to support that design. The magnitude of the task will depend on the detailed findings of the review done under Task 2.9. If the electroluminescent panels are retained, the present circuit problems should be solved by specifying a new latching relay.

### 3.15 PIECE PARTS

This task is intended to include the effort needed to revise the flight processing specifications as well as the procurement specifications for the micrologic, the multilayer boards, the relays, and other piece parts which are known to be troublesome.

### 3.16 TEST PROCEDURES

This task is intended to include that effort which is required to complete the documentation necessary to support the qualification tests and the acceptance tests of the computer and the DSKY and the various modules. This task also includes the effort



necessary to write the factory test program which the computer will run during its qualification and acceptance tests, and the effort to redesign the module acceptance tests.

### 3.17 DOCUMENTATION

This task is intended to supplement the work performed in Task 2.1 and is required to bring the various documents controlling the computer to a workable level. Documents of specific importance are interface control documents, procurement specifications, end-items specifications, and a programmers' manual.

### 3.18 COUPLING DATA UNIT

This task includes the redesign effort which may be required by virtue of the design review required in Task 2.14.

### 3.19 GROUND SUPPORT EQUIPMENT

There are some minor problems to be cleaned up in the GSE. This task is intended to include the design effort required for those tasks as well as for any other design deficiencies discovered by virtue of the work done under Task 2.15. This task also includes the effort required to design the marginal testing capability into the computer GSE.

