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APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 15

BLOCK I APOLLO GUIDANCE COMPUTER

SUBSYSTEM

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CONTENTS

Paragraph		Page
15-1	INTRODUCTION	15-1
15-6	THE BLOCK I AGC SUBSYSTEM	15-3
15-7	COMPUTER OPERATIONS	15-9
15-8	AGC Subsystem Organization	15-9
15-10	Timer	15-9
15-13	Sequence Generator	15-11
15-17	Central Processor	15-12
15-20	CP Register Manipulations	15-16
15-27	Adder	15-18
15-34	Parity Block	15-21
15-37	Memories and Addressing	15-21
15-43	Input Information and Priority Control	15-29
15-45	Binary Input Data and Interrupt	
	Priority Control	15-30
15-50	Incremental Input Data and the Counter	
	Priority Control	15-37
15-53	Output Information and the Output Control	15-39
15-55	AGC Outputs to DSKY's	15-39
15-57	Controlled Pulse Bursts	15-39
15-60	AGC Outputs to CSM	15-40
15-62	AGC Outputs to Downlink Telemetry	15-40
15-64	Display and Keyboards	15-41
15-66	Keyboards	15-41
15-72	Relay Matrices	15-42
15-77	Non-Matrix Relays	15-45
15-80	INSTRUCTIONS	15-47
15-81	Word Formats and Instruction Types	15-47
15-85	Machine Instructions	15-49
15-90	Interpretive Instructions	15-54
15-98	AGC PROGRAMS	15-63
15-106	Sunrise Programs	15-64

CONFIDENTIAL

FR-2-115

ILLUSTRATIONS

Number		Page
15-1	Block I AGC	15-4
15-2A	Logic Tray Assembly	15-5
15-2B	Memory Tray Assembly	15-6
15-3	Harness Tray	15-7
15-4	Navigation Panel DSKY	15-8
15-5	Main Panel DSKY	15-8
15-6	DSKY's (Front View)	15-8A
15-6A	NOR Gate	15-8GG
15-7	AGC Subsystem Organization	15-10
15-8	Clock, Scalars, and Time Counters	15-11
15-9	Adder Input Register and Output Gates	15-19
15-10	Summation of Two Binary Numbers Consisting of a Sign Bit and Three Value Bits	15-20
15-11	Core Ropes, Rope Modules and Address Banks	15-29
15-12	Word Formats	15-48

TABLES

Table		Page
15-0	AGC Subsystem Input and Output Signals	15-8C
15-1	Information Flow Between CP Registers, Write Amplifiers, and Memory	15-13
15-2	Module Locations of CP Registers Bits	15-15
15-3	Addressing	15-22
15-4	CP Register Assignments	15-24
15-5	E Register Assignments I	15-25
15-6	IN AND OUT Register Bit Assignments	15-31
15-7	Interrupt Motions	15-36
15-8	Counter Priority Control Inputs	15-38
15-9	Actions Initiated by Relay Band 14 in the Navigation Panel DSKY	15-43
15-10	Actions Initiated by Relay Bank 14 in the Main Panel DSKY	15-44
15-11	Actions Initiated by Relay Bank 15 in the Navigation Panel DSKY	15-44

TABLES (cont)

Number		Page
15-12	Machine Instructions	15-50
15-13	Interpretive Instruction	15-55
15-14A	Program SUNRSE33 -- Program Sections . . .	15-66
15-14B	Program SUNRSE33 -- Memory Map.	15-67
15-14C	Program SUNRSE38 -- Program Sections . . .	15-67A
15-14D	Program SUNRSE38 -- Memory Map.	15-67B
15-14E	Program SUNRSE45 -- Program Sections . . .	15-67C
15-14F	Program SUNRSE45 -- Memory Map.	15-67D
15-15	E Register Assignment II for Sunrise Programs .	15-69

15-1. INTRODUCTION

15-2. This is the fifteenth issue of the AGCIS, which is published to inform the technical staff at MIT/IL and Raytheon about the Apollo guidance computer (AGC) subsystems. The various computer subsystems are listed in paragraph 1-5. This issue is an overall description of the Block I AGC subsystem. Other issues describe in more detail the various sections and programs of the Block I AGC subsystem.

15-3. A Block I AGC subsystem consists of one Apollo guidance computer (AGC), one Display and Keyboard (DSKY) built into the navigation panel, and one DSKY built into the main panel. The AGC has a Fixed Memory (composed of Mo-perm magnetic cores arranged in core ropes) and an Erasable Memory (composed of ferrite cores arranged in an array). All logic is built from solid state integrated NOR gates contained in transistor cans. The AGC has its own integral power supply.

15-4. An AGC subsystem is a control computer (real time computer) with many features of a general purpose computer. An AGC is a parallel digital computer, which operates with 16-bit words, single address instructions, and at a clock rate of 1.024 Mc. Double precision, triple-precision, and vector double-precision operations are built into the machine. The AGC employs a ONE's complement number system with fixed binary point and overflow correction. Input signals to the AGC subsystem and output signals from the AGC subsystem can be binary information (DC signals or continuous pulse trains), incremental data (pulses counted), or controlled pulse bursts (computer number of pulses).

15-5. Most modern computers, large business machines in particular, are designed such that various programs can be inserted and executed. The AGC differs from these computers in that programs are wired in and can be changed only by replacing the Fixed Memory (either completely or in part) into which the program is wired. Therefore, it is good practice to define an AGC program as the entire content of the Fixed Memory. An AGC program consists of various program sections (sub-programs).

15-5A. An AGC program section can be written in basic machine language (Regular Machine Instructions), in interpretive language (Interpretive Instructions), or in both languages. Program portions written

CONFIDENTIAL

FR-2-115

in basic language operate faster than portions written in interpretive language because interpretive portions require extra time to interpret instructions. Portions written in interpretive language require less space for program storage than portions written in basic language because of the subroutine character of Interpretive Instructions. Furthermore, the interpretive language considerably simplifies the programming of complicated mathematical operations. The interpretive language is used mainly in program sections dealing with astronomical computations. Many of the control operations that the computer has to carry out are written in basic language and the interpretive language is used to simplify multiprecision and complicated vector operations. In conclusion one can say, the AGC is a very fast computer when operating in the basic machine language, and it is a very powerful machine when operating in the interpretive mode.

15-6. THE BLOCK I AGC SUBSYSTEM

15-6A. The Block I AGC subsystem consists of one Apollo guidance computer (AGC), one Navigation Panel DSKY, and one Main Panel DSKY. The AGC consists of one Tray A, one Tray B, one Tray C, an end connector assembly, and a coldplate (figure 15-1). Space is also provided for two spare trays. Tray A contains logic modules A1 through A40 (figure 15-2A) and Tray B contains modules B1 through B33 (figure 15-2B). Trays A and B are plugged into end connectors 05A4J4 and 05A4J3 respectively which are interconnected with end connector 05A4J5 that provides the AGC input and output connections.

15-6B. Tray C contains two harnesses (figure 15-3). Harness A interconnects plug 05A3P3, which plugs into end connector 05A4J5, with plug 05A3P1 and receptical 05A3J1. (No connections between plug 05A3P1 and receptical 05A3J1 are provided.) Plug 05A3P1 provides AGC connections to and from other subsystems of the G&N system (PSA, IMU, Optics, etc.) and the Navigation Panel DSKY. Harness B interconnects plug 05A3P2 and receptical 05A3J2. Plug 05A3P2 provides connections to and from G&N subsystems which are not connected to the AGC but to other spacecraft systems. A third harness, which is mounted to the Connector Cover Plate, connects plugs 05A5P1 and 05A5P2 with plug 05A5P3. Plugs 05A5P1 and 05A5P2 mate with recepticals 05A3J1 and 05A3J2 respectively. (No connections are provided between plugs 05A5P1 and 05A5P2.) Plug 05A5P3 provides connections to and from various spacecraft systems (the Downlink equipment, the Uplink equipment, SCS, etc.) and the Main Panel DSKY.

15-6C. The Block I DSKY's are shown in figures 15-4 through 15-6. The jack on the back of the Navigation Panel is designated 05A6J1, the jack on the back of the Main Panel DSKY, 05A8J1.

15-6D. All input and output connections of the AGC and both DSKY's are listed in table 15-0. This table has been derived from NASA Drawings 1006079, 1006080, 1006164, 1006165, 1006166, 1006167, 1006181, 1006183, 1006251, 1006252, and from Digital Development Memo No. 75 (Revision 3), all generated by MIT/IL. Column one of the table contains identification numbers of the input and output lines or signals. The letter S indicates a signal line, the letter R, a return line. Columns two through seven contain the pin number of the AGC and DSKY connectors to which the various signal lines are connected. Refer to figures 15-3 through 15-5 for the plug and jack numbers. Columns

eight and nine contain the signal names used in the drawings and in Digital Development Memo 75 respectively. The last column contains a short description of the signals.

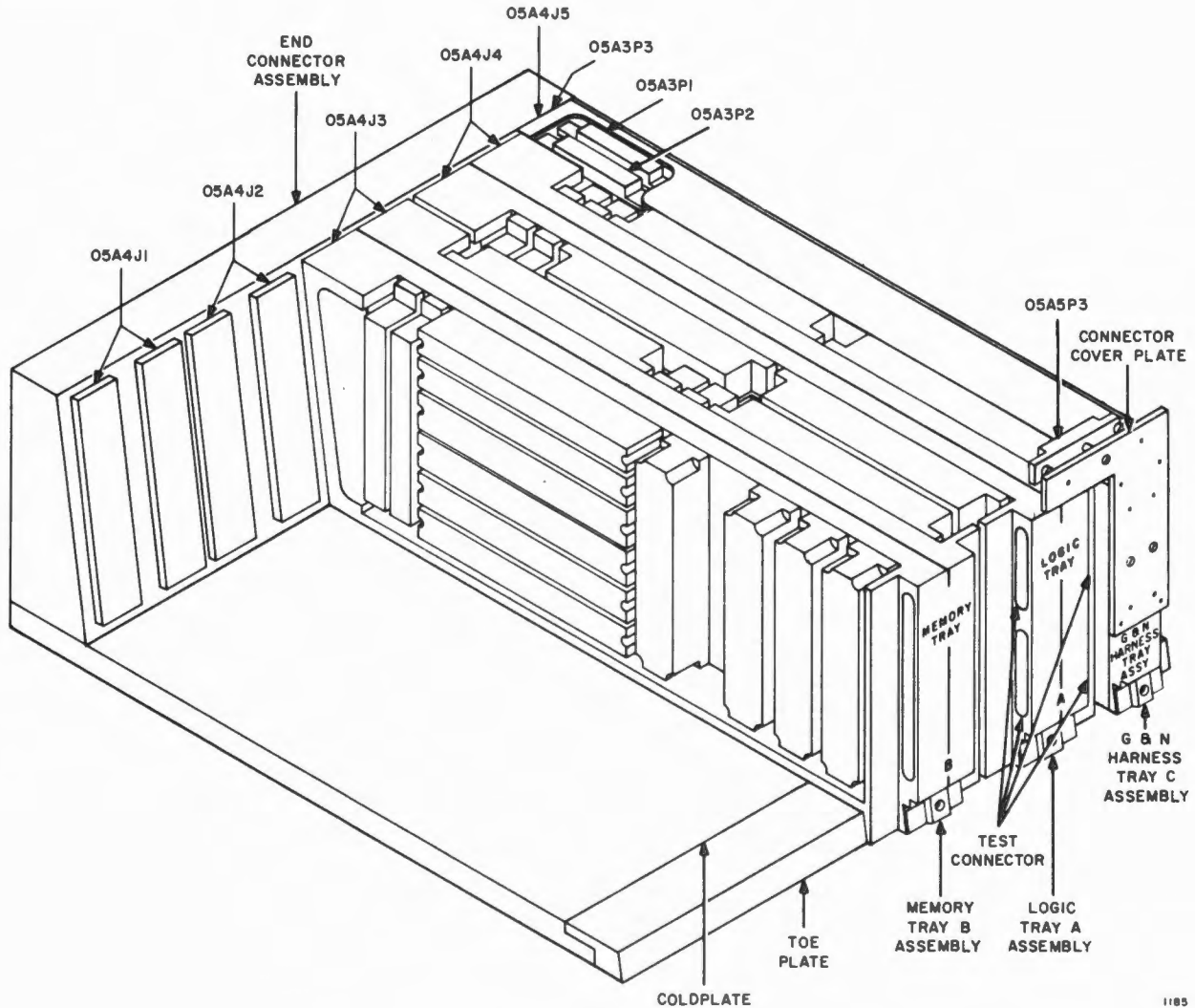
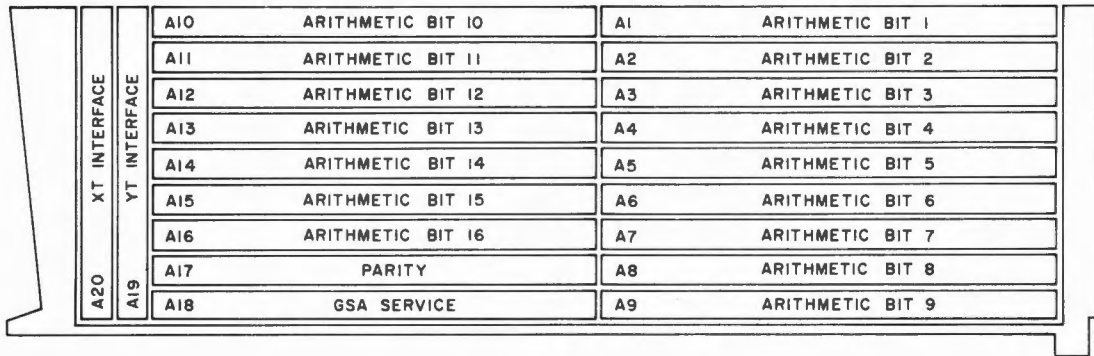


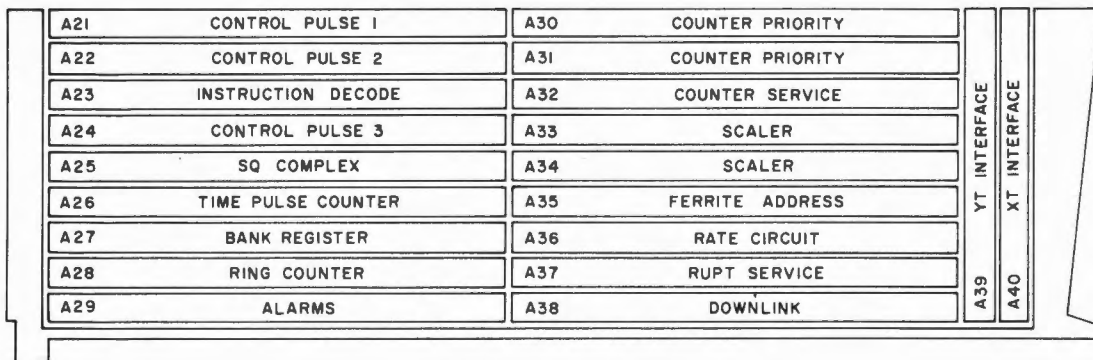
Figure 15-1. Block I AGC

15-6E. All logic of the Block I AGC is built from solid state silicon integrated NOR gates with three inputs. Refer to figure 15-6A. If one input of a NOR gate is connected to a positive potential of about 1 volt, the output potential of the NOR gate is about 0.2 volts. If all inputs used are connected to a positive potential of about 0.2 volts or less,

(text continued on page 15-8GG)



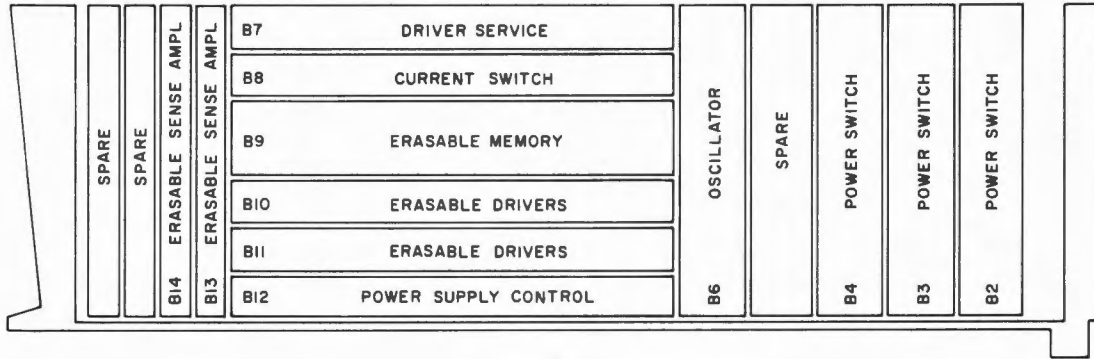
LEFT PANEL



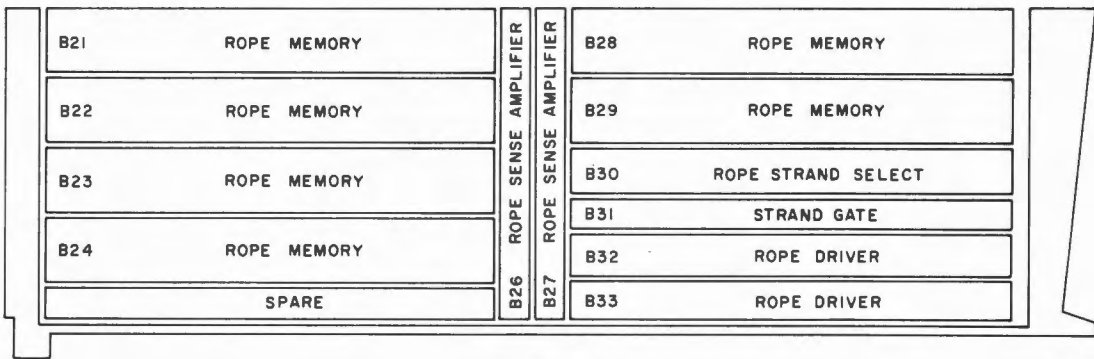
RIGHT PANEL

0203

Figure 2A. Logic Tray Assembly



LEFT PANEL



RIGHT PANEL

0202

Figure 2B. Memory Tray Assembly

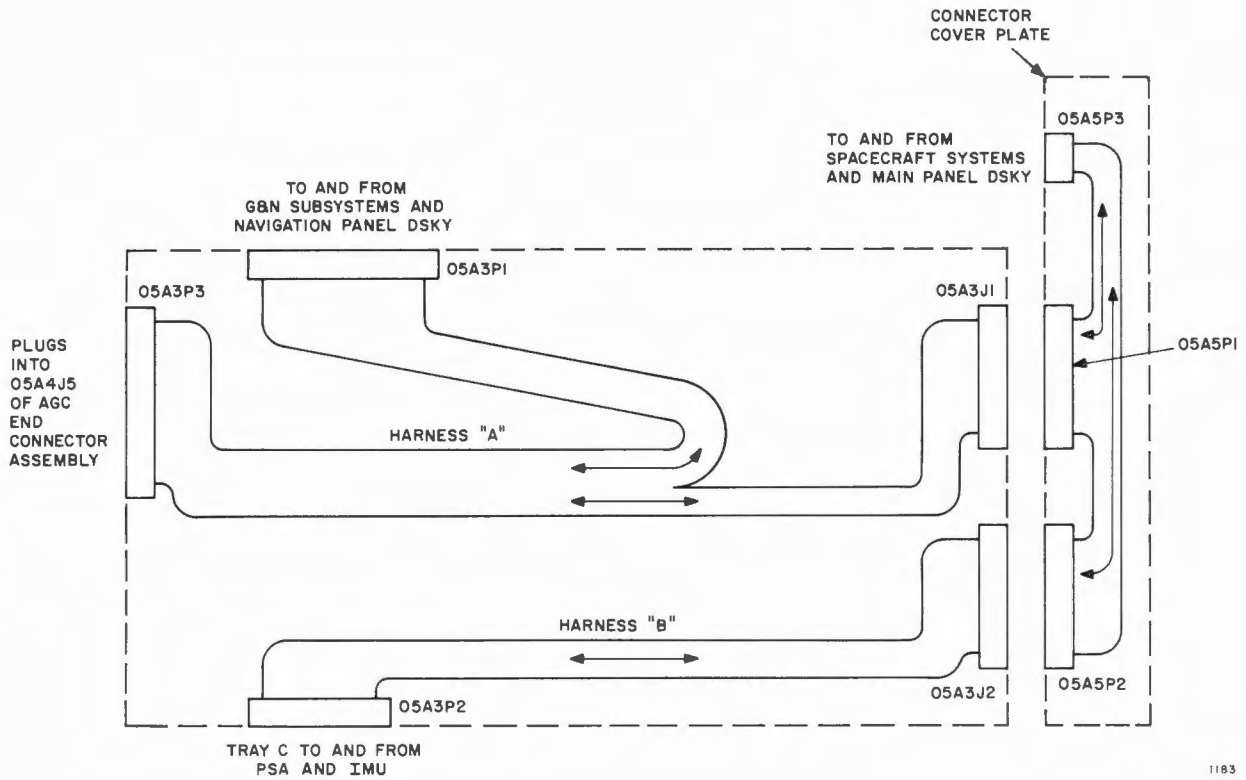
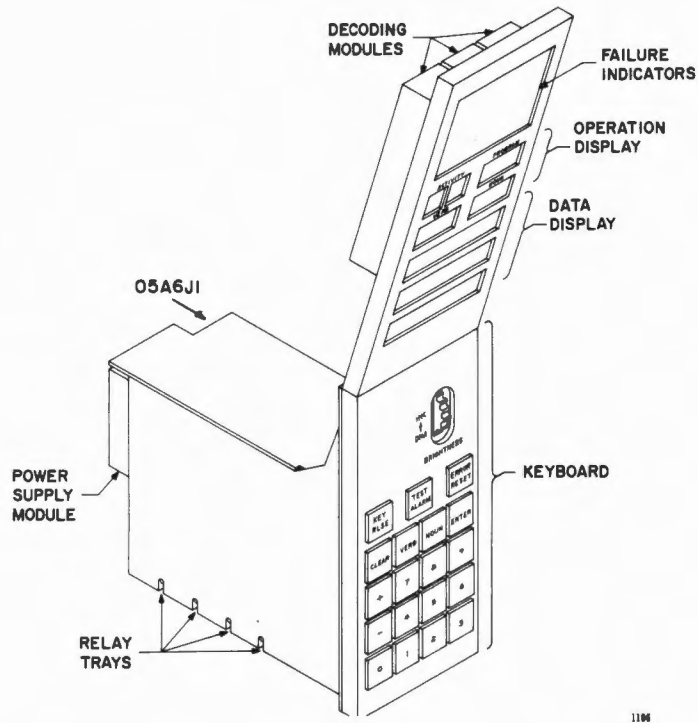


Figure 15-3. Harness Tray

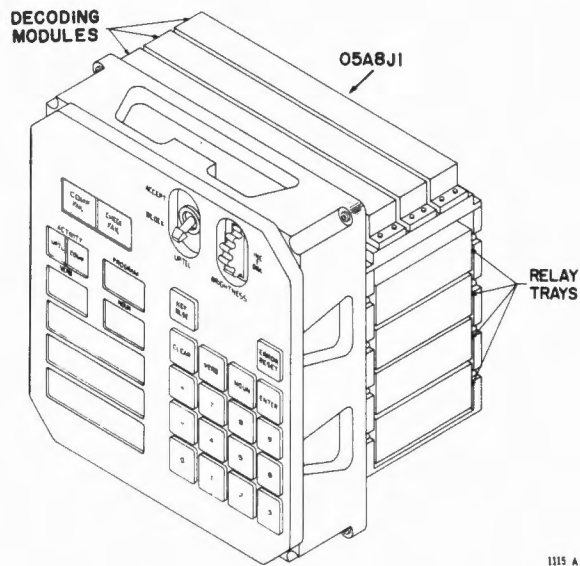
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15-7



11M

Figure 15-4. Navigation Panel DSKY



1115 A

Figure 15-5. Main Panel DSKY

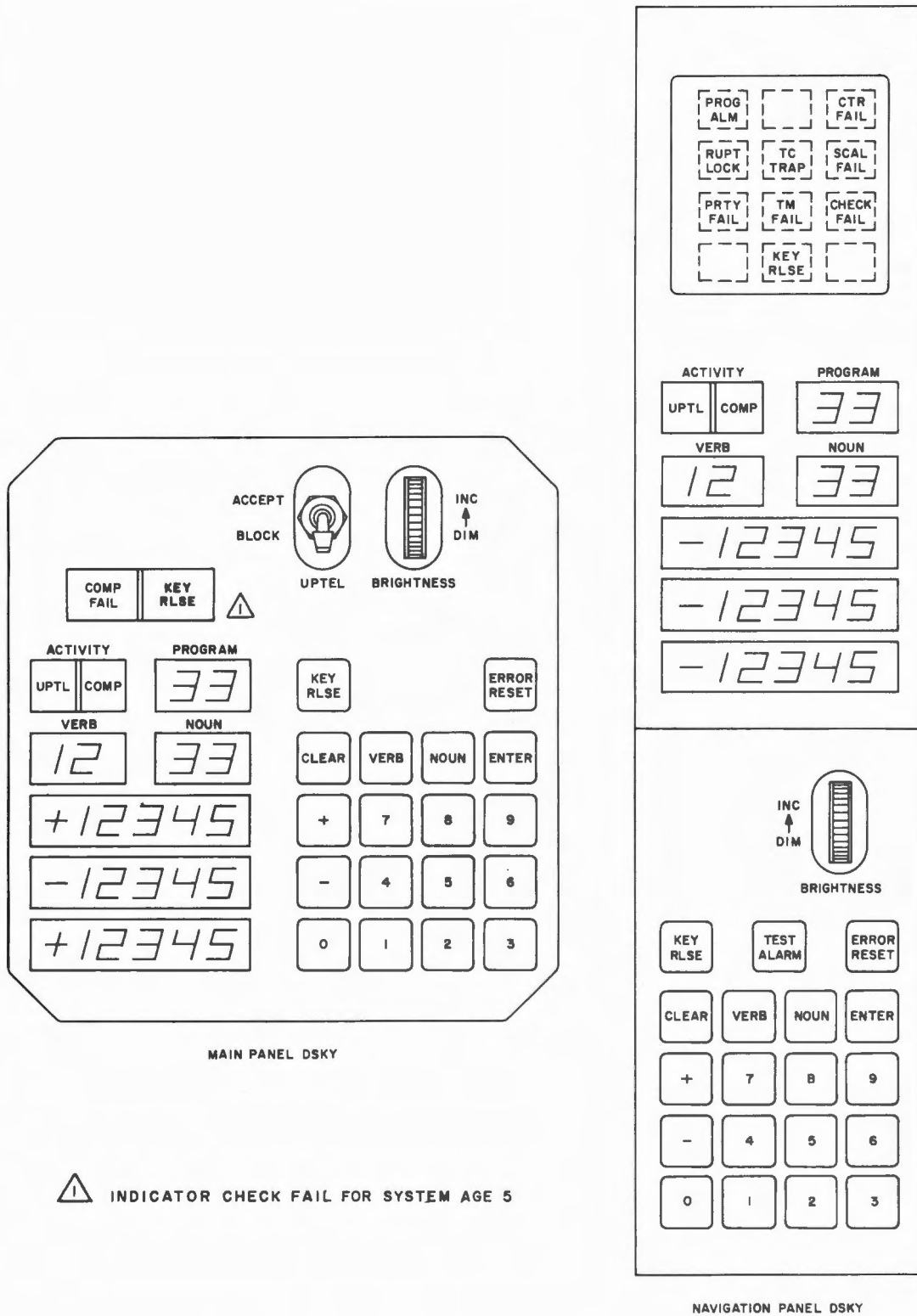


Figure 15-6. Front View of DSKY's

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
001 S R	4302 4303		224 226	224 226			MASTER CLOCK (1024KCPS)	MASTER CLOCK	1.024 mpps pulses generated by AGC Clock for CM master timing.
011 S R	4228 4328		034 035	094 095			ENG. ON	ENGINE ON	102.4 kpps pulse trains generated by AGC to turn on SM engine.
014 S R	4224 4324		190 191	190 191			DLNK START	DLNK START	AGC words (16-bit) to be sent to ground stations are entered into register OUT 4 and transferred serially to the NAA Telemetry Programmer. These words are under the control of signals (pulses) DLNK START, DLNK END, and DLNK SYNC which are generated by the NAA equipment. Serial DLNK DATA signals (pulses) are generated by the Downlink Converter within the AGC.
015 S R	4424 4524		192 193	192 193			DLNK END	DLNK END	
016 S R	4225 4325		194 195	194 195			DLNK SYNC	DLNK SYNC	
017 S R	4625 4626		098 099	090 091			DLNK DATA	DLNK DATA	
024 S R	4425 4525		123 124	123 124			ULNK 0	ULNK 0	Uplink information is received by uplink equipment in the spacecraft and forwarded in serial form (pulses ULNK 0 and ULNK 1) to the AGC. The AGC enters the serial information into counter UP-LINK and converts it into 15-bit AGC words.
025 S R	4226 4326		125 126	125 126			ULNK 1	ULNK 1	
026 S R	4612 4613		100 101	092 062			POWER FAIL	AGC POWER FAIL	In case of a failure in the AGC power supply, relay K1 in the power supply closes a contact which turns on indicator COMP PWR FAIL on the Main Display and Control Panel.
101 S R	4607 4611	119 120					SWITCH COMMON	COMMON	Refer to signal description for lines 105 through 107.
102 S R	4708 4611	086 087					MARK	MARK	
103 S R	4808 4611	088 089					$\overline{\text{MARK}}$	$\overline{\text{MARK}}$	
104 S R	4908 4611	054 055					ZERO ENCODER	ZERO OPT	

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
105 S R	5008 4611	016 017					OPTMS 1	OPT MODE SW 1	
106 S R	4709 4611	018 019					OPTMS 2	OPT MODE SW 2	
107 S R	4809 4611	020 021					OPTMS 3	OPT MODE SW 3	
108 S R	4419 4519	156 157					X+	OPT +X	<p>Incremental pulses received from Optics CDU X encoder and CDU Y encoder. Pulses 108 and 109 are used to increment and decrement the content of counter OPT X, and pulses 110 and 111 to increment and decrement the content of counter OPT Y.</p>
109 S R	4220 4320	123 124					X-	OPT -X	
110 S R	4420 4520	230 231					Y+	OPT +Y	
111 S R	4221 4321	190 191					Y-	OPT -Y	
114 S R	4706 4806	163 164					X+	+X OPT CDU	<p>Bursts of 3.2 kpps generated in the AGC to drive the Optics CDU's. The Optics CDU X (shaft angle CDU) is driven by signal 114 in the positive direction and by signal 115 in the negative direction. The Optics CDU Y (trunnion angle CDU) is driven by signal 116 in the positive direction and by signal 117 in the negative direction.</p>
115 S R	4906 5006	130 131					X-	-X OPT CDU	
116 S R	4707 4807	235 236					Y+	+Y OPT CDU	
117 S R	4907 5007	197 198					Y-	-Y OPT CDU	

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
118 S R	4212 4312	056 057					X+	+X CDU	Incremental pulses received from IMU CDU X, IMU CDU Y, and IMU CDU Z encoders. Pulses 118 and 119 are used to increment and decrement the content of counter CDU X, pulses 120 and 121 to increment and decrement the content of counter CDU Y, and pulses 122 and 123 to increment and decrement the content of counter CDU Z.
119 S R	4412 4512	058 059					X-	-X CDU	
120 S R	4213 4313	024 025					Y+	+Y CDU	
121 S R	4413 4513	026 027					Y-	-Y CDU	
122 S R	4214 4314	232 233					Z+	+Z CDU	
123 S R	4414 4514	192 193					Z-	-Z CDU	
124 S R	4215 4315	158 159					FAIL	CDU FAIL	
126 S R	4402 4502	064 065					X+	CDU X+	Bursts of 3.2 kpps generated in the AGC to drive the IMU CDU's. The IMU X is driven by signal 126 in the positive direction and by signal 127 in the negative direction. The IMU CDU Y and the IMU CDU Z are driven in a similar way by signals 128 through 131.
127 S R	4403 4503	030 031					X-	CDU X-	
128 S R	4404 4504	237 238					Y+	CDU Y+	
129 S R	4405 4505	199 200					Y-	CDU Y-	
130 S R	4406 4506	165 166					Z+	CDU Z+	
131 S R	4407 4507	097 098					Z-	CDU Z-	
132 S R	4415 4515	125 126					ΔV_{X+}	+DV _X	Refer to signal description for lines 134 through 137.
133 S R	4216 4316	092 093					ΔV_{X-}	-DV _X	

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
134 S R	4416 4516	194 195					$\Delta V_Y +$	+DV _Y	Incremental pulses received from PIPA X, PIPA Y, and PIPA Z. Pulses 132 and 133 are used to increment and decrement the content of counter PIPA X, pulses 134 and 135 to increment and decrement the content of counter PIPA Y, and pulses 136 and 137 to increment and decrement the content of counter PIPA Z.
135 S R	4217 4317	160 161					$\Delta V_Y -$	-DV _Y	
136 S R	4417 4517	127 128					$\Delta V_Z +$	+DV _Z	
137 S R	4218 4318	094 095					$\Delta V_Z -$	-DV _Z	
138 S R	4418 4518	060 061					PIPA FAIL	PIPA FAIL	In case of a PIPA failure, a 102.4 kpps pulse train is supplied by the PIPA's which sets bit position 11 of register IN2.
139 S R	4207 4307	132 133					PIPA INTERROGATE	PIPA INTERROGATE	Continues 3.2 kpps pulse trains generated by the AGC to Interrogate the PIPA's.
140 S R	4208 4308	099 100					PIPA CLOCK	PIPA SWITCHING	
141 S R	4219 4319	028 029					IMU FAIL	IMU FAIL	In case of an IMU failure, a 102.4 kpps pulse train is supplied by the IMU which sets bit position 12 of register IN2.
142 S R	4209 4309	066 067					X+	+DX	Bursts of 3.2 kpps generated in the AGC to drive the IMU gyros. The X gyro is driven by signal 142 in the positive direction and by signal 143 in the negative direction. The Y and the Z gyro are driven in a similar way by signals 144 through 147.
143 S R	4210 4310	032 033					X-	-DX	
144 S R	4211 4311	239 240					Y+	+DY	
145 S R	4408 4508	201 202					Y-	-DY	
146 S R	4409 4509	167 168					Z+	+DZ	
147 S R	4410 4510	134 135					Z-	-DZ	

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description	
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1				
148 S R	4411 4511	101 102					GYRO RESET	GYRO RESET	102.4 kpps pulse train is generated in the AGC to reset the IMU gyros.	
149 S R	4702 4802	068 069					800 CPS SET	800 PPS SET	Continues pulse trains generated in the AGC and transmitted to the PSA.	
150 S R	4902 5002	034 035					800 CPS RESET	800 PPS RESET		
151 S R	4703 4803	241 242					3.2 KC SET	3.2K PPS SET		
152 S R	4903 5003	203 204					3.2 KC RESET	3.2K PPS RESET		
153 S R	4704 4804	169 170					25.6 KC SET	25.6K PPS SET		
154 S R	4904 5004	136 137					25.6 KC RESET	25.6K PPS RESET		
155 S R	4705 4805	103 104					CONVERTER SYNC (12.8KC)	12.8K PPS		
156 S R	4905 5005	070 071					DISCRET SIG CARRIER (102.4KC)	DISCRET SIGNAL CARRIER		
157 S R	4616 4617	036 037					AGC POWER FAIL NAV PANEL LIGHT	AGC POWER FAIL		In case of a failure in the AGC power supply, relay K1 in the power supply is energized which turns an indicator COMP PWR FAIL on the Navigation Display and Control Panel and is also sent to the telemetry system.
158 S R	4909 4611	152 153					K1	K1		DC signals supplied by relays K1, K2, K3, K4, K12, and K5 in the IMU. Signal 158 indicates mode ZERO ENCODER and sets bit position 1 of register IN3. Signal 159 indicates mode COARSE ALIGNMENT and sets bit position 2. Signal 160 indicates mode LOCK CDU's and sets bit position 3. Signal 161 indicates mode FINE ALIGNMENT (Continued on next page)
159 S R	5009 4611	154 155					K2	K2		
160 S R	4700 4611	188 189					K3	K3		

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
161 S R	4810 4611	222 223					K4	K4	and sets bit position 4. Signal 162 indicates mode ATTITUDE CONTROL and sets bit position 5. Signal 163 indicates mode ROLL RE-ENTRY and sets bit position 7 of register IN3. Refer to signals 307 through 315.
162 S R	4910 4611	224 225					K12	K12	
163 S R	5010 4611	226 227					K5	K5	
164 S R	4608 4611	228 229					TR SWITCH	TRN SW	DC signal supplied by Transfer Switch of IMU. Signal indicates that AGC has control over relays K1 through K5, and K12 in IMU, and sets bit position 6 of register IN3.
165 S R	4610 4611	121 122					COMMON	COMMON	+VDC supplied by AGC to IMU for the generation of signals 158 through 164. Refer to signals 307 through 315.
166	4603	234					BACK UP SIGNAL	BACK UP SIGNAL	+28VDC test point.
167 S R	4301 4201	001 073					28 VDC- A-Bus	+28V Bus A	+28VDC Bus A from PSA Junction Box to AGC Power Supply
168 S R	5001 4901	139 207					28 VDC- B-Bus	+28V Bus B	+28VDC Bus B from PSA Junction Box to AGC Power Supply
169 S R	4501 4401	002 074					0 VDC- A-Bus	0V Bus A	0VDC Bus A from PSA Junction Box to AGC Power Supply
170 S R	4701 4801	208 140					0 VDC- B-Bus	0V Bus B	0VDC Bus B from PSA Junction Box to AGC Power Supply
171	4304	196					TEMP MON 1	TEMP MON 1	Not used
172	4305	162					TEMP MON 2	TEMP MON 2	
173	4306	129					TEMP MON 3	TEMP MON 3	
175	4604	096					+3V A	3V A	Not used
176	4605	062					+13V A	13V A	

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
177	4606	063					0V	0V	Not used
178	4609	053					SHLD GRD	SHIELD GROUND GROUP IV	
179	4615	022 023 156 157 158 159 160					SHLD GRD	SHIELD GROUND GROUP V	
181	4611								Common signal return for signals 101 through 107, 158 through 165, 201 through 205, and 207 through 210.
183 S R	4724 4824	205 206					STAR PRES		Not used
201 S R	4718 4611	218 219	218 219	218 219	034 069	006 007,003	KEY CODE 1	KEY CODE 1	+13VDC signals supplied by DSKY's which set bit positions 1 through 5 of register INO.
202 S R	4818 4611	183 184	183 184	183 184	035 069	008 009,003	KEY CODE 2	KEY CODE 2	
203 S R	4918 4611	150 151	150 151	150 151	036 069	010 011,003	KEY CODE 3	KEY CODE 3	
204 S R	5018 4611	117 118	117 118	117 118	037 069	012 013,003	KEY CODE 4	KEY CODE 4	
205 S R	4719 4611	084 085	084 085	084 085	038 069	014 015,003	KEY CODE 5	KEY CODE 5	
206 S R	4819		049 050	049 050		016 017,003	KEY RESET	KYBD RESET	+13VDC signals supplied by DSKY's. Signals 206 and 209 control the Interrupt Priority Control. Signals 207 and 208 control the Alarm Control.
207 S R	4919 4611	014 015			039 069		TEST ALARM	TEST ALARM	
208 S R	5019 4611	220 221	220 221	220 221	048 069	018 019,003	ERROR RESET	ERR LGHT RESET	

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
209 S R	4720 4611	012 013			049 069		KEY RESET	KYBD RESET	Refer to signal description for lines 206 through 208.
210 S R	4720 4611	185 186	185 186	185 186	047 069	020 021, 003	OR OF C1 → C22 (NAV DSKY) OR OF C23 → C33 (MAIN DSKY)	OR OF RELAYS C1 - C22 (NAV DSKY) OR OF RELAYS C23 - C33 (MAIN DSKY)	
211	5020	003	003	003	070	209	SPARE	SPARE	
212	4717	075	075	075	071	211	POWER SYNC N	POWER SUPPLY SYNC N	800 pps sync signal generated in AGC and supplied to Navigation Panel DSKY power supply.
213	4621	141	141	141	072	213	SPARE	SPARE	
214 S R	4711 4618, 4620	210 211	210 211	210 211	073 082	215 216, 208	OUT 0 1	OUT 0 1	Refer to signal description for lines 220 through 228.
215 S R	4811 4618, 4620	175 176	175 176	175 176	074 082	217 218, 208	OUT 0 2	OUT 0 2	
216 S R	4911 4618, 4620	142 143	142 143	142 143	060 082	219 220, 208	OUT 0 3	OUT 0 3	
217 S R	5011 4618, 4620	109 110	109 110	109 110	028 082	221 222, 208	OUT 0 4	OUT 0 4	
218 S R	4712 4618, 4620	076 077	076 077	076 077	029 082	223 224, 208	OUT 0 5	OUT 0 5	
219 S R	4812 4618, 4620	041 042	041 042	041 042	030 082	225 226, 208	OUT 0 6	OUT 0 6	

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

CONFIDENTIAL

FR-2-115

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
220 S R	4912 4618, 4620	004 005	004 005	004 005	031 082	227 228, 208	OUT 0 7	OUT 0 7	+ VDC signals supplied by bit positions 1 through 15 of register OUT0. These signals control the latched relays in the DSKY, which in turn control displays on the DSKY and other subsystems of the AGE.
221 S R	5012 4618, 4620	212 213	212 213	212 213	061 082	229 230, 208	OUT 0 8	OUT 0 8	
222 S R	4713 4618, 4620	177 178	177 178	177 178	062 082	231 232, 208	OUT 0 9	OUT 0 9	
223 S R	4813 4618, 4620	144 145	144 145	144 145	063 082	233 234, 208	OUT 0 10	OUT 0 10	
224 S R	4913 4618, 4620	111 112	111 112	111 112	014 082	235 236, 208	OUT 0 11	OUT 0 11	
225 S R	5013 4618, 4620	078 079	078 079	078 079	015 082	237 238, 208	OUT 0 12	OUT 0 12	
226 S R	4714 4618, 4620	043 044	043 044	043 044	016 080	239 240, 208	OUT 0 13	OUT 0 13	
227 S R	4814 4618, 4620	006 007	006 007	006 007	017 082	241 242, 208	OUT 0 14	OUT 0 14	
228 S R	4914 4618, 4620	214 215	214 215	214 215	018 082	176 177, 208	OUT 0 15	OUT 0 15	
229 S R	5014 4618, 4620	179 180	179 180	179 180	040 082	178 179, 208	PROGRAM ALARM	PROGRAM ALARM	
230 S R	4715 4618, 4620	146 147	146 147	146 147	041 082	180 181, 208	COMPUTER ACTIVITY	COMPUTER ACTIVITY	
231 S R	4815 4618, 4620	113 114	113 114	113 114	019 082	182 183, 208	TL FAIL ALARM	TELEMETRY ALARM	
232 S R	4915 4618, 4620	080 081	080 081	080 081	032 082	184 185, 208	CHECK FAIL ALARM	PROGRAM CHECK FAILURE ALARM	
233 S R	5015 4618, 4620	045 046	045 046	045 046	033 082	186 187, 208	SCALER FAIL ALARM	SCALER FAIL ALARM	
234 S R	4716 4618, 4620	008 009	008 009	008 009	044 082	188 189, 208	PARITY FAIL ALARM	PARITY FAIL ALARM	

CONFIDENTIAL

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
235 S R	4816 4618, 4620	216 217	216 217	216 217	043 082	190 191, 208	COUNTER FAIL ALARM	COUNTER FAIL ALARM	+VDC signals generated in the AGC. Signals 229, 230, 236, 231, and 232 are provided by bit positions 1 through 5 of register OUT 1 respectively. Signals 233, 234, 235, 237, and 238 are provided by various circuits. All Signals control non-latched relays in the DSKY's which in turn control indicators on the DSKY's.
236 S R	4916 4618, 4620	181 182	181 182	181 182	053 082	192 193, 208	KEY RLSE	KEY RELEASE	
237 S R	5016 4618, 4620	148 149	148 149	148 149	051 082	194 195, 208	RUPT LOCK ALARM	RUPT LOCK ALARM	
238 S R	4817 4618, 4620	115 116	115 116	115 116	064 082	196 197, 208	TC TRAP ALARM	TC TRAP ALARM	
239	4203	173	173	173	056	207	SIGNAL GRD	GND	Signals supplied by the AGC for the DSKY's.
240	4204	174	174	174	055	001	+3V B	+3V B	
241	4205	108	108	108	057	139	+13V B	+13V B	
242 S R	4917 4620	082 083	082 083	082 083	020 082	198 199, 208	POWER SYNC (800CPS)	POWER SUPPLY SYNC M	800 cps sync signal generated in AGC and supplied to Main Panel DSKY power supply.
243	4206	040	040	040	059	073	+28V COMPUTER	28V COMP	+28VDC supplied by the AGC for the DSKY's.
244 S R	5017 4618, 4620	047 048	047 048	047 048	042 082	200 201, 208	TIMING (1.5CPS)	TIMING	Action Request signal supplied by Timer to DSKY's for flashing of VERB and NOUN displays.
245					001	173			SHIELD
246 S R	4920 4611		051 052	051 052		004 005, 003	BLOCK UP LINK	BLOCK UPLNK	+VDC signal supplied by switch UPTTEL on the Main Panel DSKY if in position ACCEPT. The signal sets bit position 6 of Register INO.
247	4624	209	209	209	075	202	SPARE	SPARE	SHIELD
248	4627	010	010	010	045	022	SPARE	SPARE	
249	4630	011	011	011	046	024	SPARE	SPARE	
250					027	027		SHLD GND GP III	
251	4202	039	039	039	058	002	SIGNAL GRD (KEYBOARD)	KEY BD GND	

(See page 15-8EE for line 252)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
301					003		ENCODER ZEROING	C5	
302					004		CDU FAIL	C6	
303					005		PIPA FAIL	C7	
304					006		IMU FAIL	C8	
305					007		SPARE	C9	
306					008		COMMON	COMMON	
307					021		ZERO ENCODER	C1	
308					022		COARSE ALIGN	C2	
309					023		LOCK CDU'S	C3	
310					024		FINE ALIGN	C4	
311					025		ROLL REENTRY	C11	
312					026		COMMON	COMMON	
313					011		LAMP TEST SW		

(Continued on next page)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description	
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1				
314					012		LAMP HIGH	C10 ATT CONTROL HI	<p>The diagram shows a vertical dashed line separating the AGC side from the IMU side. On the AGC side, there are inputs for BIT POSITION 1 OF IN3 through 6 OF IN3, RET, and +VDC. On the IMU side, there are relays K1 through K5. Signal 158 connects BIT POSITION 1 OF IN3 to K1. Signal 159 connects BIT POSITION 2 OF IN3 to K2. Signal 160 connects BIT POSITION 3 OF IN3 to K3. Signal 161 connects BIT POSITION 4 OF IN3 to K4. Signal 162 connects BIT POSITION 5 OF IN3 to K12. Signal 163 connects BIT POSITION 6 OF IN3 to K5. Signal 164 connects RET to a common terminal. Signal 165 connects +VDC to a common terminal. All relay contacts are connected to a common vertical bus on the right.</p>	
315					013		COMMON ATTITUDE CONTROL LAMP	COMMON ATT CONTROL		
316					065		ZERO OPT	C12		Not used
317					066		STAR TRACKER ON	C13		Not used
318							SPARE			
319							SPARE			
320							SPARE			
321							SPARE			
322							SPARE			
323							SPARE			
324							SPARE			
325							SPARE			

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
326					009		OR OF ALARMS	OR OF ALARMS	
327					010		ALARM COMMON	COMMON	
328					002		CONDITION LAMP TEST	COND. LAMP TEST	Refer to signals 301 through 306
329									
330					082		GROUP II RETURN GROUND	COMMON RETURNS (SHIELD)	
331					067		OPT COMMON	COMMON (SHIELD)	
401									DC signals supplied by relays in the Main Panel DSKY to turn on indicators CDU FAIL, ACCEL FAIL, OR IMU FAIL respectively on the Main Display and Control Panel.
402					080		CDU FAIL	C6	
403					081		PIPA FAIL	C7	
404					082		IMU FAIL	C8	
405					083		SPARE	C9	Spare connection
406					084		COMMON	COMMON	Returns for signals 402 through 405

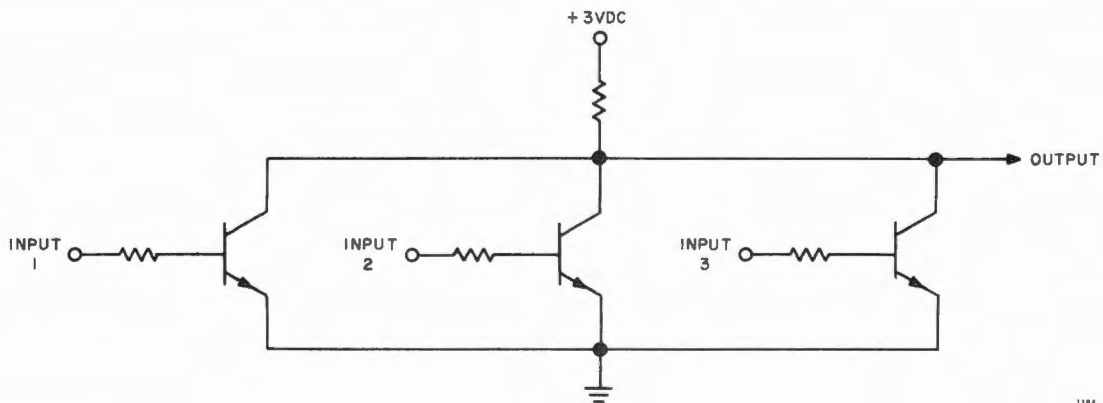
AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
407									
408									
409									
410									
411									
412						085	PROGRAM ALARM	PROGRAM ALARM	+VDC signals supplied by relays in the Main Panel DSKY and sent to the NAA Telemetry Programmer, which collects information for downlink transmission. Similar signals are generated by relays in the Navigation Panel DSKY and used to turn on indicators PROG ALM, COMP ACTIVITY, TM FAIL, CHECK FAIL, SCAL FAIL, PRY FAIL, CTR FAIL, KEY RLSE, RUPT LOCK, and TC TRAP. Thus, the signals sent to ground via the Main Panel DSKY contain the same information as is displayed on the Navigation Panel DSKY.
413						086	COMPUTER ACTIVITY	COMPUTER ACTIVITY	
414						087	TL FAIL ALARM	TELEMETRY ALARM	
415						088	CHECK FAIL ALARM	PROGRAM CHECK FAILURE ALARM	
416						089	SCALER FAIL ALARM	SCALER FAIL ALARM	
417						090	PARITY FAIL ALARM	PARITY FAIL ALARM	
418						091	COUNTER FAIL ALARM	COUNTER FAIL ALARM	
419						092	KEY RLSE	KEY RELEASE	
420						093	RUPT LOCK ALARM	RUPT LOCK ALARM	
421						094	TC TRAP ALARM	TC TRAP ALARM	
422						099	CRC GND	CRC COMMON	
423 S R						078 079	BLOCK UPLNK	BLOCK UPLNK	+VDC signal supplied by switch UPTL on the Main Panel DSKY if in position ACCEPT.
424						095	ENCODER ZEROING	C5	Refer to signal description for lines 425 through 427.

AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line	Connecting Pin of						Name Used on Drawing	Name Used on DD Memo 75	Signal Description
	05A4J5 05A3P3	05A3P1	05A3J1 05A5P1	05A5P3	05A6P1	05A8P1			
425						096	CDU FAIL	C6	+VDC signals supplied by relays in Main Panel DSKY and sent to the NAA Telemetry Programmer, which collects information for telemetry transmission. Signal 424 indicates that IMU CDU's are being zeroed. Signals 425 through 427 are similar to signals 402 through 404 except they are used as downlink information instead of turning on indicators CDU FAIL, ACCEL FAIL, or IMU FAIL.
426						097	PIPA FAIL	C7	
427						098	IMU FAIL	C8	
428						100	CRC SUPPLY	CRC +5V	+5VDC line from NAA Telemetry Programmer
429								COMMON D RETURNS	
708	4126		235				CNTRL 1		Test signals from the Computer Test Set to test the AGC Power Supply.
709	4127		236				CNTRL 2		
713	4130		239				MT LO		
714	4129		238				MT HI		
	4125		234				CNSHLD		
	4128		237				MTSHLD		
	4619		187	187			SHLD GRD		
			107	107			SHLD GRN		
252					069	003	GROUP III RETURN GROUND		

the output potential is about 1 volt. Thus, a logical ONE is represented by a positive potential of approximately 1 volt and a logical ZERO by a positive potential of about 0.2 volt. Since each NOR gate inverts voltage levels, a logical ZERO can represent either a data ZERO or a data ONE dependent on the operational location of a gate, and a logical ONE can represent a data ONE or a data ZERO. A data ONE is represented by a logical ONE (positive potential of approximately 1 volt) at the input of the write amplifiers, and a logical ZERO (positive potential of about 0.2 volt). At the output of the Write Amplifiers, a logical ONE (positive potential of approximately 1 volt) represents a data ZERO, and a logical ZERO (positive potential of approximately 0.2 volt) represents a data ONE.



1184

Figure 15-6A. NOR Gate

15-7. COMPUTER OPERATIONS

15-8. AGC SUBSYSTEM ORGANIZATION

15-9. The organization of the AGC subsystem is illustrated in figure 15-7. The AGC subsystem can be divided into the following major sections:

- | | |
|-----------------------|--------------------------|
| a. Timer | f. Priority Control |
| b. Sequence Generator | g. Output Control |
| c. Central Processor | h. Display and Keyboards |
| d. Erasable Memory | j. Interface Circuitry |
| e. Fixed Memory | k. Power Supply |

15-10. TIMER

15-11. The Timer consists of the Clock, Scaler A, the Time Pulse Generator, and the Start-Stop Logic. The Clock is driven by a 2.048 Mc oscillator of which the frequency varies less than 5 parts per 10^8 parts when operating at $40^{\circ}\text{C} \pm 0.5^{\circ}\text{C}$. The ageing rate of the oscillator is 1.7 parts per 10^9 parts per day at 40°C . The oscillator is electronically controlled to compensate for frequency variations caused by temperature changes and the oscillator frequency varies less than 3 parts per 10^7 parts when operating between 20°C and 50°C .

15-11A. The Clock provides pulse rates of 1.024 Mc, 512 kc, and 102.4 kc. The 102.4-kc pulses are fed into the 17-stage Scaler A which drives the 16-stage Scaler B (figure 15-8). The last stage of Scaler B supplies an output pulse about every 23.3 hours. The output of stage 10 of Scaler A causes the TIME 1 counter to be incremented every 10-msec. An overflow of counter TIME 1 increments counter TIME 2 every 163.84 sec. Counters TIME 1 and TIME 2 allow counting time up to 31 days. In addition to the 10-msec pulses, other timing signals are provided by Scaler A for various systems of the CM.

15-12. The Time Pulse Generator accepts 1.024-Mc pulses from the Clock and generates a timing signal every 0.977 μsec . (time signals T01 through T12). The twelve timing signals are generated every 11.7 μsec which is designated a Memory Cycle Time (MCT). These signals are needed in the SQG and other sections of the AGC. The Start-Stop Logic generates stop signals as the result of failures within the computer or signals received from the AGC Test Set. In addition, the Start-Stop Logic generates a clear signal which causes the computer to restart.

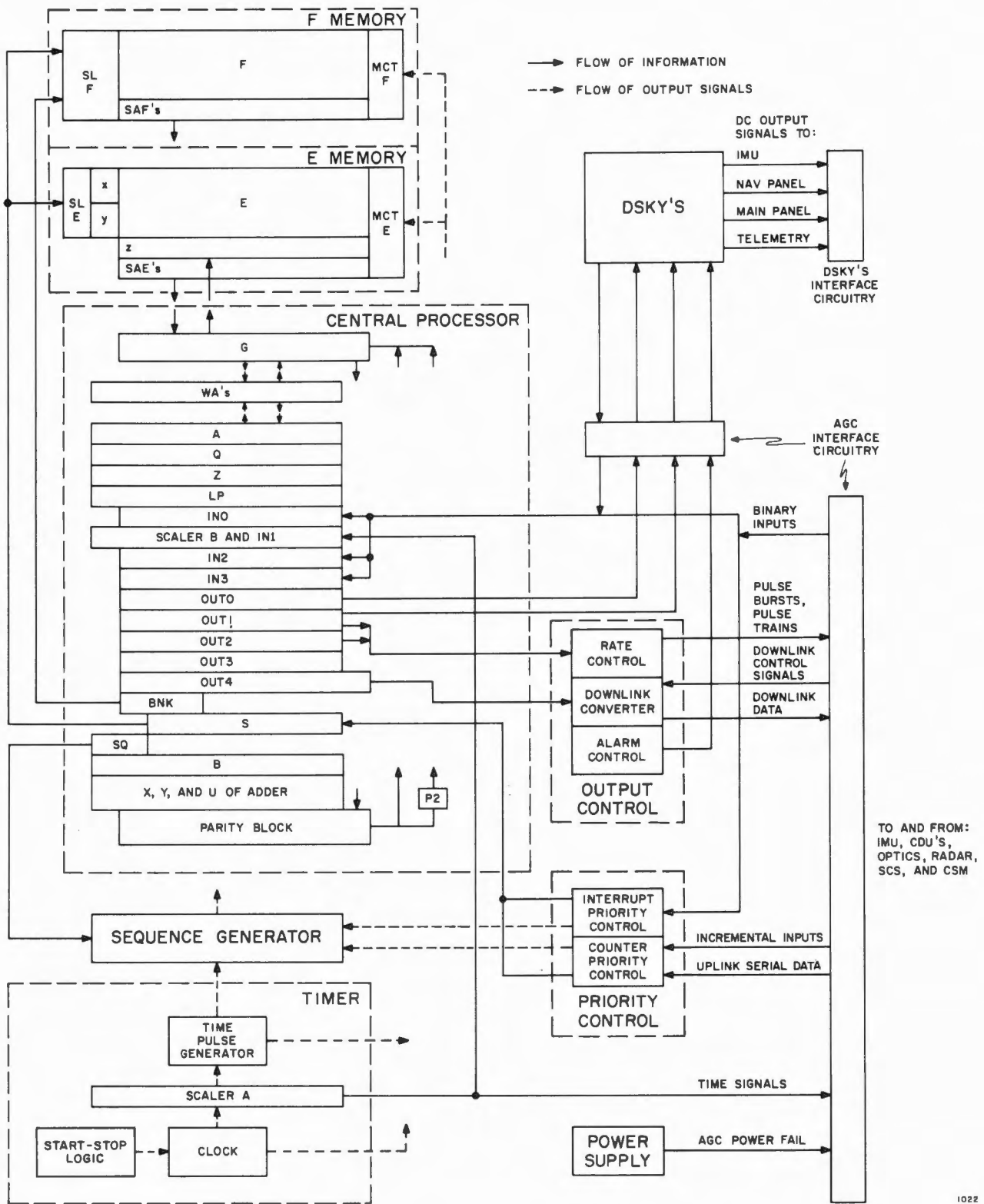


Figure 15-7. Machine Organization

UNIT	OUTPUT
CLOCK	102,400 PPS
SCALER A, STAGE 1	51,200 PPS
SCALER A, STAGE 10	100 PPS \equiv 10 MSEC/PULSE INTERVAL
SCALER A, STAGE 11 AND COUNTER T1, BIT POSITION 1	20 MSEC/PULSE INTERVAL
SCALER A, STAGE 17 AND COUNTER T1, BIT POSITION 7	1.28 SEC/PULSE INTERVAL
SCALER B, STAGE 1 AND COUNTER T1, BIT POSITION 8	2.56 SEC/PULSE INTERVAL
SCALER B, STAGE 7 AND COUNTER T1, BIT POSITION 14	163.84 SEC/PULSE INTERVAL
SCALER B, STAGE 8 AND COUNTER T2, BIT POSITION 1	327.68 SEC/PULSE INTERVAL
SCALER B, STAGE 12 AND COUNTER T2, BIT POSITION 5	1 HR AND 1642.88 SEC/PULSE INTERVAL
SCALER B, STAGE 16 AND COUNTER T2, BIT POSITION 9	23 HR AND 1086.08 SEC/PULSE INTERVAL \approx 23.3 HR/PULSE INTERVAL
COUNTER T2, BIT POSITION 14	\approx 31 DAYS/PULSE INTERVAL

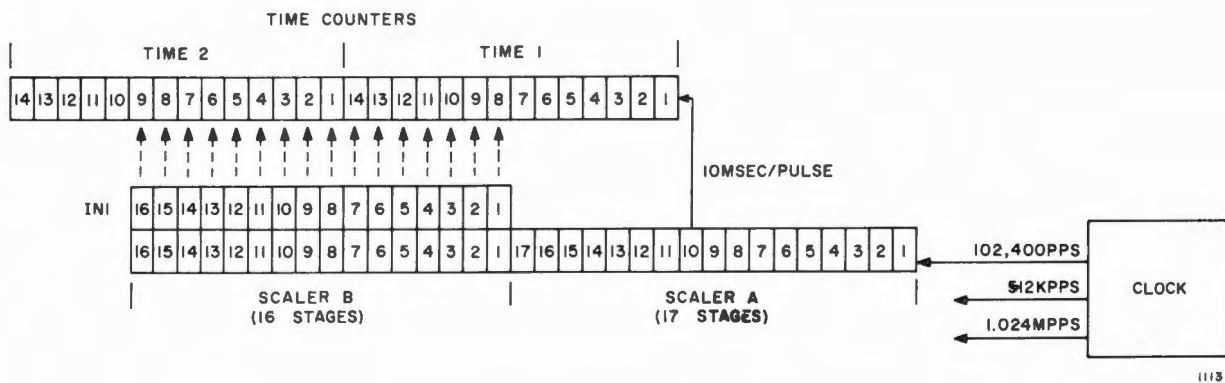


Figure 15-8. Clock, Scalers, and Time Counters

15-13. SEQUENCE GENERATOR

15-14. The Sequence Generator (SQG) generates a set of control pulses whenever a time signal (T01 through T12) is received from the Time Pulse Generator. Each such set of control pulses is called an Action. The control pulses control various registers and gates in the Central Processor (CP) and other sections of the AGC. All Machine Instructions (Regular, Involuntary, and Miscellaneous Instructions) consist of one, two, or more subinstructions; each subinstruction consists of twelve Actions numbered 1 through 12. The execution of one subinstruction takes one MCT.

15-15. The execution of a Regular Instruction (Basic and Extra Code Instructions) is initiated by entering its order code into register SQ. A program is executed by entering one Basic Instruction after another into the CP, and transferring the order codes of Basic Instructions and Extra Code Instructions (the latter are derived from Basic Instructions

CONFIDENTIAL

FR-2-115

by the CP) into register SQ.

15-16. Involuntary Instructions (Priority Program Instructions and Counter Instructions) are executed at the request of the Priority Control. The Priority Program Instructions (Interrupt and Resume) cause the SQG to interrupt the execution of the program section currently being executed in favor of a program section of higher priority, and to resume the execution of the interrupted program section. Counter Instructions cause the SQG to increment (by one), decrement (by one), and shift the content of a counter (by adding a ZERO or a ONE in the lowest bit position). Counter instructions are performed in between the execution of Regular Instructions upon request of the Counter Priority Control.

15-17. CENTRAL PROCESSOR

15-18. The Central Processor (CP, figure 15-7) consists of various registers, the Adder, the Parity Block, and the Write Amplifiers (WA's). The operation of each register in the CP is defined in table 15-1. All CP registers are integrated NOR gate flip-flop registers which can be read nondestructively. All circuits serving the CP registers, as well as the WA's, are composed of integrated NOR gates.

15-19. Most of the CP registers consist of sixteen bit positions, which are numbered 16 through 1. The sixteen-bit registers carry sixteen bits of information but no parity bit. The bit positions of registers G and OUT4, and the input lines to the Parity Block, all of which carry a parity bit, are numbered 15 through 0. The Write Amplifiers are numbered 16 through 1; the parity bit does not require a WA. In figure 15-7, all registers with bit positions 16 through 1 are moved to the left with respect to the registers with bit positions 15 through 0. Most IN and OUT registers contain the same information in bit positions 16 and 15 and for this reason are shown shorter. The BNK register consists of only five bit positions, which are numbered 15 through 11. Registers S and SQ consist of twelve and four bit positions respectively, numbered 1 through 16. Table 15-2 indicates in which of the 16 arithmetic modules (figure 15-2) the bit positions of the various registers are located. (Register BNK and the Parity Block are located in another module.) Normally the number of bit positions agrees with the number of modules. However, bit position 0 is located in module 15, and bit position 15 is located in module 16 for registers storing bits 0 through 15.

TABLE 15-1

INFORMATION FLOW BETWEEN CP REGISTERS,
WRITE AMPLIFIERS, AND MEMORY

Register			Control Pulse	Read and Write Lines of Write Amplifiers (WA)																Parity Bus
Octal Address	Initials	Name		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
				16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
0	A	Accumulator	RA RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WA WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WALP	16 SG	15 SG	14 OV	13	12	11	10	9	8	7	6	5	4	3	2	1	-
1	Q	Return Address Register	RQ RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WQ WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
2	Z	Program Counter	RZ RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WZ WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
3	LP	Low Order Product Register	RLP RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WLP WSC	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	16	15
			WALP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
4	IN 0	Input 0 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
5	IN 1	Input 1 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
6	IN 2	Input 2 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
7	IN 3	Input 3 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
10	OUT 0	Output 0 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
11	OUT 1	Output 1 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
12	OUT 2	Output 2 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
13	OUT 3	Output 3 Register	RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
14	OUT 4	Output 4 Register	WSC	15	-	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	BNK	Memory Bank Select Register	RSC	15	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-	-
			WSC	15	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-	-

0571-1

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CONFIDENTIAL

15-13

CONFIDENTIAL

FR-2-115

TABLE 15-1

INFORMATION FLOW BETWEEN CP REGISTERS,
WRITE AMPLIFIERS, AND MEMORY (cont)

Register			Control Pulse	Read and Write Lines of Write Amplifiers (WA)															Parity Bits			
Octal Address	Initials	Name		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2		1		
	B C	Buffer Register with direct output B and complement output C	RBO RB RC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			WB	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
	U X Y	Adder with input registers X and Y, and output gates U	RU	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			WX WY	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
	S	Address Register	WS	-	-	-	-	12	11	10	9	8	7	6	5	4	3	2	1			
	SQ	Sequence Register	NISQ WSQF WSQG	16 SG	15 OV	14	13	-	-	-	-	-	-	-	-	-	-	-	-			
		Parity Block	WP	15 SG	-	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	G	Memory Buffer Register		RG	15		14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Function	c(S)	Control Signal																		
		Direct	Any Other Address	WG1G, WG5G	WG	15 SG	-	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
		CYR	0020	WG2G, WG4G	WG	14 SG	-	13	12	11	10	9	8	7	6	5	4	3	2	1	15	
		SR	0021	WG2G, WG5G	WG	15 SG	14 SG	-	13	12	11	10	9	8	7	6	5	4	3	2	1	-
		CYL	0022	WG3G, WG6G	WG	1 SG	-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	
		SL	0023	WG3G, WG5G	WG	1 SG	15 SG	-	-	14	13	12	11	10	9	8	7	6	5	4	3	2
	G	Memory Buffer Register		SBF SBE ZID	-	15 SG	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0020 through 1111		Erasable and Fixed Memory			-	15 SG	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

0571-1

15-14

CONFIDENTIAL

Changed 2 July 1964

FR-2-115

CONFIDENTIAL

TABLE 15-2
MODULE LOCATIONS OF CP REGISTER BITS

REGISTER	ARITHMETIC MODULES															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A, Q, Z, LP, IN1, B, U, X, Y,	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
INO, IN2, IN3, OUT 0, OUT 1, OUT 2,	15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OUT 4, G,	15	0	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SQ	15	15	14	13	X											
S	X				12	11	10	9	8	7	6	5	4	3	2	1

1108

CONFIDENTIAL

FR-2-115

15-20. CP REGISTER MANIPULATIONS

15-21. Registers A, Q, Z, and LP, the four input registers (IN 0, 1, 2, and 3), the five output registers (OUT 0, 1, 2, 3, and 4), and the BNK register are addressable. The other CP registers are not addressable. A register is addressable when it can be selected for readout or write-in by entering the proper address into register S. The non-addressable registers and some addressable registers can be gated for readout or write-in by means of control pulses generated in the SQG without having the address of that register contained in register S. Table 15-1 lists all the read (R) and write (W) control pulses which affect the registers. Control pulses RSC and WSC are applied to all addressable flip-flop registers for readout or write-in, but only that register which is addressed when RSC or WSC is applied is read out or written into. All other control pulses listed in table 15-1 carry the initials of a register behind the R or W, indicating that these control pulses are able to read out or write into the corresponding initialed register directly.

15-22. A word is transferred from one CP register to another by gating the inputs of the receiving register and the outputs of the transmitting register at the same time. This allows a word to flow from one register through the WA's to the receiving register. The flow of data to and from the WA's occurs on two different sets of lines, the read and the write lines. One word is transferred from one CP register to one or more other CP registers during one Action. Gating a word from a register into the WA's is straight-forward. Editing, (shifting or cycling) when required, is accomplished by gating the inputs of registers A and G.

15-23. A word contained in registers A, Q, Z, LP, IN, OUT (except OUT 4), or BNK can be gated from any one of these registers into the WA's of corresponding bit positions. This is true also for the B register, which has a direct output designated B and a complement output designated C. The Adder output gates, which are designated, U contain fourteen value bits (bits 1 through 14) which are fed into WA1 through WA14. The overflow bit (bit 15) is fed into WA15. Normally the sign bit (bit 16) is fed into WA16. Whenever angular data are dealt with, the overflow bit is fed into WA15 and WA16, and the sign bit of U is discarded (refer to paragraph 15-27). Registers S and SQ and the Parity Block cannot be read into the WA's. Whenever register G is read into the WA's by control pulse RG, the content of its bit position 15 is fed into both WA16 and WA15, as indicated in table 15-1. The parity bit (bit 0), contained in bit position 0 of register G, is not sent to a WA but rather directly to input line 0 of the Parity Block.

15-24. Registers Q, Z, B, X, Y, and the OUT registers are written into straight forward (into corresponding bit positions). Input registers IN0, IN2, and IN3 are connected to the interface circuits and loaded from there. Bit positions 15 and 16 contain bit 15 of the input word. Register IN1 is part of Scaler B (figure 15-8) and allows reading the time information contained in the Scaler. Output registers OUT0, OUT1, and OUT2 are connected to the DSKY's via the interface circuits as well as to the Rate Control. The OUT registers can be read into register G by addressing these registers. Register OUT4 provides telemetry information to the Downlink Converter, and cannot be read into register G. Register OUT3 is a spare register which can be used as an input or an output register after adding the proper interconnections. Register BNK can be read out of and written into straight forward; registers S and SQ can only be written into. Registers S and BNK control the selection logic of the Fixed and Erasable memories, and the SQ register accepts the order codes for the SQG.

15-25. A word contained in the WA's can be written into register A straight forward with control pulse WA, or it can be shifted one position to the right with control pulse WALP (write A and LP). From table 15-1 it can be seen that if WALP is applied, bit position 1 of register A accepts information from WA02, bit position 2 from WA03, etc. If a bit is present at WA15, it is fed into bit position 14 of register A, and, if a bit is present in WA16, it is fed into both positions 15 and 16 of register A. The content of WA01 is entered into bit position 14 of register LP if control pulse WALP is applied. When control pulse WLP (write LP only) is applied, bits 2 through 14 of any word present in the WA's are shifted also one position to the right as the word is transferred to the LP register, however, WA1 feeds bit positions 15 and 16 of register LP. The contents of WA15 and WA16 are lost. Registers A and LP form a double-length shifting accumulator (when control pulses WALP, RLP, and WLP are applied), which is required for the execution of instructions multiply (MP) and divide (DV). Normally, register A is used as a 16-bit accumulator.

15-26. Five alternatives for writing into register G are provided as shown in table 15-1. Control pulse WG normally causes any information present at Write Amplifiers WA01 through WA14 to be entered into bit positions 1 through 14 of register G; the information contained in WA16 is transferred into bit position 15 of register G and any bit contained in WA15 is discarded. Whenever a word in register G is to be transferred to Erasable Memory, bit position 0 of register G has to be filled by a parity bit generated in the Parity Block or stored in register P2. Control pulse GP (generate parity) or RP2 (read P2) enters

CONFIDENTIAL

FR-2-115

the parity bit into bit position 0 of register G. If register S contains address 0020, gates servicing register G cause the word to be entered into register G to cycle one position to the right. Address 0021 causes a shift to the right, 0022 a cycle to the left, and 0023 a shift to the left. During cycle operations, the information contained in WA16 and WA14 through WA01 is cycled one place and entered into bit positions 15 through 1 of register G. During shift operations, the information contained in WA14 through WA02, or WA13 through WA01, is shifted one place and entered into bit positions 13 through 1, or 14 through 2 of register G; the information contained in WA16 is entered into bit position 14 or 1 as well as into bit position 15 of register G. The cycled or shifted information is normally transferred from register G to register 0020, 0021, 0022, or 0023 in Erasable Memory, but the information can also be returned to the WA's and other CP registers, as in the case of the DV instruction. Any transfer of information from the WA's to register G has to take place before Action 10, if the information is to be written into Erasable Memory immediately.

15-27. ADDER

15-28. The basic arithmetic unit of the AGC is the Adder, which is able to add two numbers at a time. The Adder has two input registers (X and Y) and a bank of output gates (U). The two numbers to be added can be positive or negative or one positive and the other negative. Normally, an addition is carried out in the ONE's complement number system. Values of fourteen bits can be added, and the Adder generates an additional bit in case of overflow or underflow. Control pulse WY resets both the X and Y registers; therefore, the Y register must be loaded first. The arithmetic sum of the two values is available at output gates U within 3 μ sec after entering the second operand. The delay is caused by carry propagation. The adder, on command, can also add the positive quantity one to a number fed into X or Y. This operation also required 3 μ sec.

15-29. As shown in figure 15-9, the bit positions of the Adder registers are numbered 16 through 1. No parity bit is entered into the Adder. Whenever an operand is gated from register G into one of the input registers, its sign (SG) is entered into bit positions 15 and 16. A plus is represented by ZERO, a minus by ONE. Entering a sign bit into position 15 is equivalent to providing an additional value bit (either plus or minus zero which is represented by a ZERO or a ONE) in front of the fourteen-bit value. In case of overflow or underflow, the Adder replaces the previous value bit (plus or minus zero) in position 15 by a value bit one (plus or minus one, represented by a ONE or a ZERO). This additional output is labeled OV (overflow or underflow bit). Position 16 of output gates U always contains the correct sign of the sum.

15-18

CONFIDENTIAL

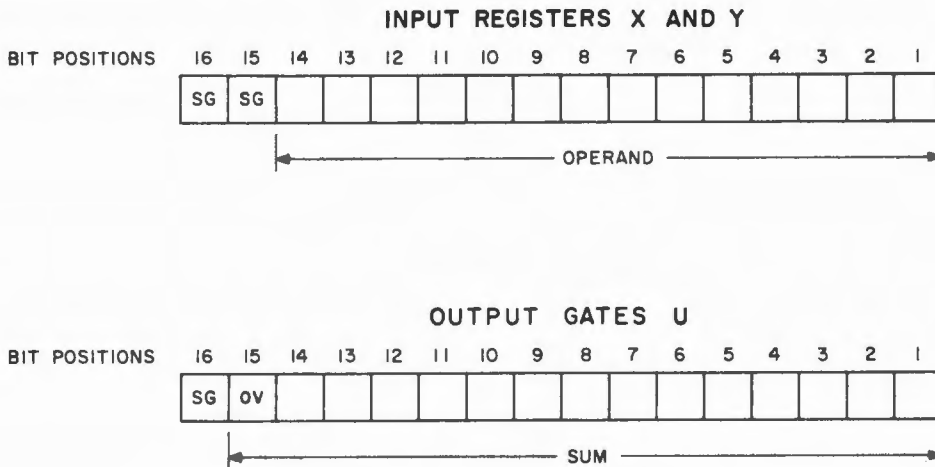
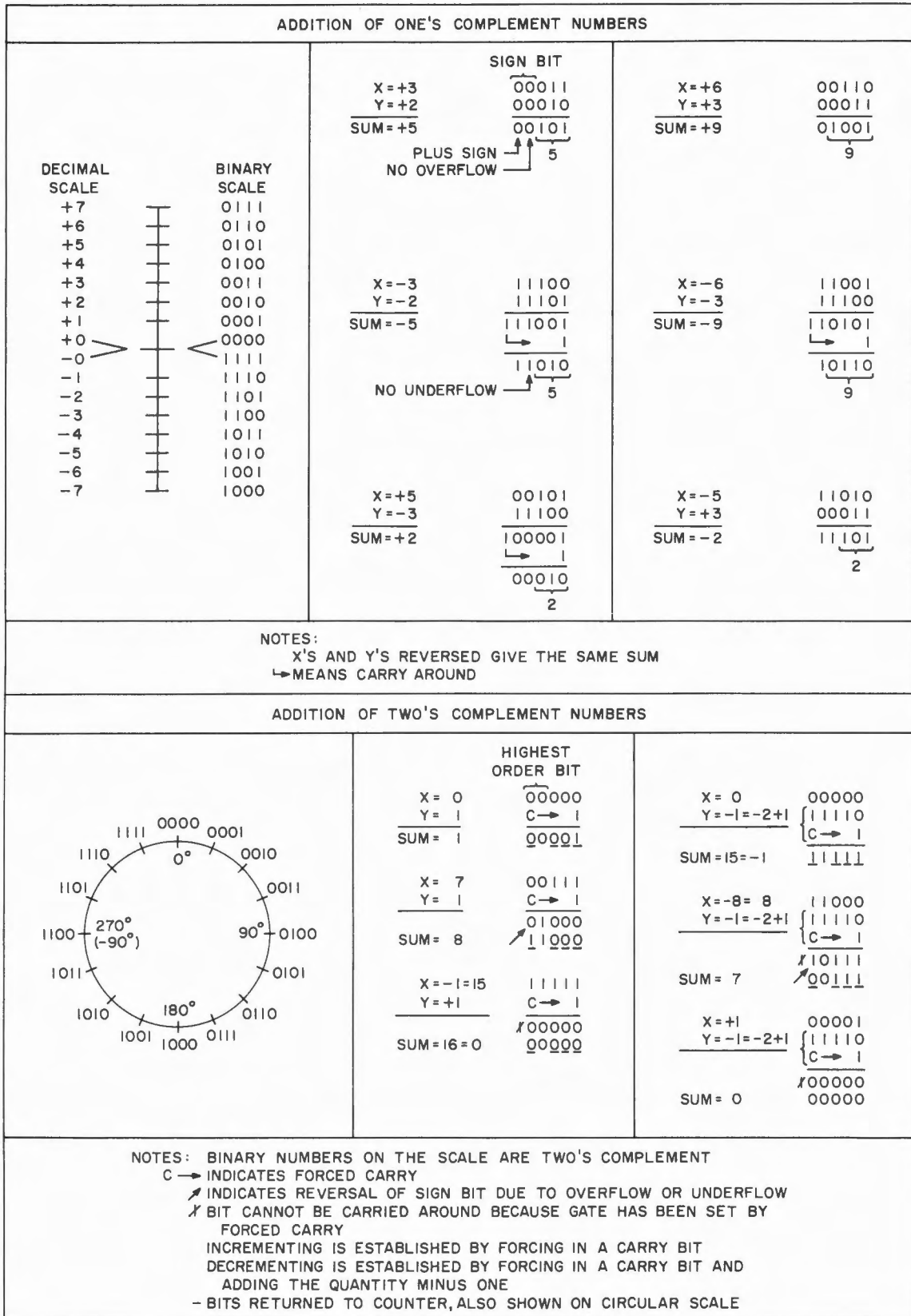


Figure 15-9. Adder Input Registers and Output Gates

15-30. The upper half of figure 15-10 illustrates the principle of adding two three-value bit numbers when performing general additions. In reality, the largest octal number resulting from a general addition as provided by output gates U, is +77777, the smallest is -77777. When counters are incremented or decremented, only the quantity one is added to or subtracted from whatever might be contained in a counter. When the content of a counter has to be shifted one position to the left, this is accomplished by adding the quantity to itself. The way in which the content of a counter is incremented, decremented, or shifted depends on the purpose of a counter.

15-31. The Time Counters (registers 0035, 0036, 0037, and 0040 in Erasable Memory) and the Rate Counters (0042, 0043, and 0057) are only incremented. The Overflow Counter (0034) and the PIPA Counters (0044, 0045, and 0046) are incremented and decremented. In case any one of the counters mentioned is addressed, an addition is performed in ONE's complement numbers as illustrated in the upper part of figure 15-10, except that the quantity to be added is always plus or minus one. The largest octal number which can be stored in a counter is +37777, the smallest -37777.

15-32. The CDU Counters (0047, 0050, and 0051), the OPT Counters (0052 and 0053), Counters TRKRX and TRKRY (0054 and 0055) are incremented or decremented. In case any one of the counters mentioned is addressed, an addition is performed in TWO's complement numbers



1152A

Figure 15-10. Summation of Two Binary Numbers Consisting of a Sign Bit and Three Value Bits

quantity 00000 (i. e. +00000 in a Counter), and 180° by 40000 (i. e. -37777). The quantity 40000 decremented by 1 is 37777 (i. e. +37777) and incremented by one is 40001 (i. e. -37776). Thus, 360° are equivalent to 2^{15} incrementations.

15-33. The UPLINK Counter (0041) and the TRKR R Counter (0056) are used for serial to parallel conversion. Any addition is performed as illustrated in the upper part of figure 15-10, except that the sign is reversed in case of overflow and that end-around carry is prevented. For details refer to paragraphs 2-111 through 2-117.

15-34. PARITY BLOCK

15-35. The Parity Block generates a new parity bit for each 15-bit word entered into it and allows testing parity by comparing the new parity bit of a word with the original parity bit of the same word. (The purpose of the parity bit is explained in paragraph 15-81.) A word might be transferred directly from a CP register (bits 1 through 14, and 16) into the Parity Block without a parity bit or from Erasable or Fixed Memory via register G with a parity bit. A new parity bit can be entered into the single-bit register P2 by applying control pulse WP2, or it can be entered directly into bit position 0 of register G by applying control pulse GP. Read pulse RP2 transfers a parity bit from P2 into position 0 of register G. Control pulse TP (test parity) opens a gate and allows a signal, which is generated in case of incorrect parity (new parity bit not equal to original parity bit), to trigger an alarm signal, the effect of which will be described in another issue of the AGCIS. Whenever a word is transferred from a location with an address smaller than 0030 (as indicated by the content of register S), control pulse TP is prevented from triggering an alarm.

15-36. The Parity Block also generates a signal, which is needed when addressing Fixed Memory and used to minimize noise. This signal is derived from bits 1 through 9 of each word entered into the Parity Block at the same time the parity bit mentioned in paragraph 15-35 is generated.

15-37. MEMORIES AND ADDRESSING

15-38. The Erasable (E) Memory is a coincident-current ferrite core array capable of storing 1024 sixteen-bit words, however, only 1008 storage locations are used. The selection logic SLE (figure 15-7) together with the x and y selection, the z drivers, and the sense amplifiers SAE's and memory cycle timer MCT E makes it possible to read information stored in register G into E memory or to write information stored in E memory into register G. Readout of the E memory is destructive; therefore, information required for later use must be restored.

CONFIDENTIAL

FR-2-115

15-39. The selection logic SLE and SLF is under the control of registers S and BNK which can be considered as the input registers of the selection logic. Any location in E memory, and any addressable register in the CP is addressed simply by putting the proper 10-bit address into register S, independent of the content of register BNK, as indicated in table 15-3. Table 15-4 lists the assignments of the addressable CP locations. Some low address locations in E memory are reserved for storing words which were shifted or cycled, for data of an interrupted program, and for twenty registers which are used as counters (CTR) as indicated in table 15-5. The remaining registers are available for general erasable storage (GE). Memory Cycle Timers MCT E and MCT F generate strobe signals which sequence the operation of E memory and F memory respectively.

15-40. The Fixed (F) Memory consists of three core ropes, capable of storing 24,576 sixteen-bit words. The selection logic SL and the sense amplifiers SAF's and the memory cycle timer MCT F make it possible to address a certain location in F memory and to read its contents into register G. Information stored in F memory is wired in, can not be destroyed during read out, and can be read out as often as required.

15-41. Fixed Memory can be divided into fixed-fixed (FF) memory and fixed-switchable (FS) memory as shown in table 15-3. Any location in FF memory is addressed by putting the proper address into register S, independent of the contents of register BNK. Whenever a word in FF memory is addressed, a ONE in either bit position 11 or 12, but never in both, is present in register S. If a ONE is present in both bit positions 11 and 12, a location in FS memory is addressed. Twenty-two different address banks in FS memory are covered by the same real addresses, as indicated in table 15-3. In order to address a location in a certain bank, the selection logic automatically considers the content of register BNK. Program sections written in basic language only are stored in Banks 03 through 14, sections written (partly or completely) in interpretive language are stored in banks 21 through 34. Each core rope consists of two Rope Modules and each module contains four banks of locations as indicated in figure 15-11. A core rope module is a plug-in unit similar to a logic module.

(Text continued on page 15-29)

15-22

CONFIDENTIAL

TABLE 15-3
ADDRESSING

Register Groups		Octal Address		Pseudo Address (Decimal)	Contents of BNK [△]					Contents of S [△]														
		Real	Pseudo		15	14	13	12	11	12	11	10	9	8	7	6	5	4	3	2	1			
CP	A, Q, Z, LP	0000 - 0003	Same	0 - 3	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	X	X			
	IN	0004 - 0007	Same	4 - 7	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	1	X	X		
	OUT	0010 - 0014	Same	8 - 12	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1	X	X	X		
	BNK	0015	Same	13	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1	1	0	1		
	No Bit Location	0016 - 0017	Same	14, 15	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1	1	1	X		
E	Special	0020 - 0027	Same	16 - 23	X	X	X	X	X	0	0	0	0	0	0	0	0	1	0	X	X	X		
	Spares	0030 - 0033	Same	24 - 27	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1	0	X	X		
	CTR	0034 - 0057	Same	28 - 47	X	X	X	X	X	0	0	0	0	0	0	X	X	X	X	X	X	X		
	GE	0060 - 1777	Same	48 - 1023	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X		
FF	BANK 01	2000 - 3777	Same	1024 - 2047	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X		
	02	4000 - 5777	Same	2048 - 3071	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X	X		
F	FS	03	6000 - 7777	6000 - 7777	3072 - 4095	0	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X	X		
		04	6000 - 7777	10000 - 11777	4096 - 5119	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	
		05	6000 - 7777	12000 - 13777	5120 - 6143	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	
		06	6000 - 7777	14000 - 15777	6144 - 7167	0	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		07	6000 - 7777	16000 - 17777	7168 - 8191	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		10	6000 - 7777	20000 - 21777	8192 - 9215	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		11	6000 - 7777	22000 - 23777	9216 - 10239	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		12	6000 - 7777	24000 - 25777	10240 - 11263	0	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		13	6000 - 7777	26000 - 27777	11264 - 12287	0	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		14	6000 - 7777	30000 - 31777	12288 - 13311	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		21	6000 - 7777	42000 - 43777	17408 - 18431	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		22	6000 - 7777	44000 - 45777	18432 - 19455	1	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		23	6000 - 7777	46000 - 47777	19456 - 20479	1	0	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		24	6000 - 7777	50000 - 51777	20480 - 21503	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		25	6000 - 7777	52000 - 53777	21504 - 22527	1	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		26	6000 - 7777	54000 - 55777	22528 - 23551	1	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
		27	6000 - 7777	56000 - 57777	23552 - 24575	1	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
30	6000 - 7777	60000 - 61777	24576 - 25599	1	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X		
31	6000 - 7777	62000 - 63777	25600 - 26623	1	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X		
32	6000 - 7777	64000 - 65777	26624 - 27647	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X		
33	6000 - 7777	66000 - 67777	27648 - 29671	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X		
34	6000 - 7777	70000 - 71777	28672 - 29695	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X		

[△] X means 0 or 1.

TABLE 15-4
CP REGISTER ASSIGNMENTS I

Octal Address	Initials	Name and Purpose
0000	A	Accumulator
1	Q	Return Address Register
2	Z	Location Counter
3	LP	Low Order Product Register
} See table 15-1 for operation		
0004	IN0	Input Register 0
5	IN1	Input Register 1, part of Time Scaler B
6	IN2	Input Register 2
7	IN3	Input Register 3
} See table 15-6 for bit assignments		
0010	OUT0	Output Register 0
11	OUT1	Output Register 1
12	OUT2	Output Register 2
13	OUT3	Spare Register, not connected, could be used as an IN or OUT Register
14	OUT4	Output Register, provides Downlink data
0015	BNK	Bank Register contains 5 bit positions for storing Bank Numbers
0016	RELINT	No bit positions, is addressed to release program interrupt inhibit in Interrupt Priority Control
17	INHINT	No bit positions, is addressed to activate interrupt inhibit in Interrupt Priority Control

CONFIDENTIAL

CONFIDENTIAL

TABLE 15-5
E REGISTER ASSIGNMENT I

Octal Address	Initials	Name and Purpose
0020 21 22 23	CYR SR CYL SL	Cycle Right Shift Right Cycle Left Shift Left } See table 15-1, for operation
0024 25 26 27	ZRUPT BRUPT ARUPT QRUPT	Stores last content of register Z at execution of instruction RPT Stores last content of register B at execution of instruction RPT Stores last content of register A at execution of RPT Transfer Routine Stores last content of register Q at execution of RPT Transfer Routine
0030 31 32 33		Spare Spare Spare Spare
0034	OVCTR	Overflow Counter is incremented or decremented by instructions PINC and MINC if an overflow or underflow occurs during the execution of instructions add (AD K) or subtract (SU K). (Interrupting routines must preserve the content of OVCTR or avoid overflow or underflow.)
0035	TIME 2	Main Time Counter stores high order time quantities. This counter is incremented by instruction PINC every time that counter TIME 1 overflows. Counter TIME 2 overflows about every 31st day. See figure 15-8.
0036	TIME 1	Main Time Counter stores low order time quantities. This counter is incremented by instruction PINC every 10 msec. Counter TIME 1 overflows every 163.84 sec which increments counter TIME 2.

Changed 2 July 1964

CONFIDENTIAL

15-25

CONFIDENTIAL

FR-2-115

TABLE 15-5
E REGISTER ASSIGNMENTS I (cont)

Octal Address	Initials	Name and Purpose
0037	TIME 3	Time counter 3 initiates the execution of program section T3RUPT. This counter is preset under program control and incremented by instruction PINC every 10 msec at the same time that counter TIME 1 is incremented. When overflow occurs, control signal RP1 is generated in the Interrupt Priority Control, which causes the execution of: instruction RPT, RPT Transfer Routine TIME3RPT, program section T3RUPT, and the Task due. See table 15-8.
0040	TIME 4	Time counter 4 initiates the execution of program section T4RUPT. This counter is preset under program control and incremented by instruction PINC every 10 msec (5 msec later than counters TIME 1 and TIME 3). When overflow occurs, control signal RP3 is generated in the Interrupt Priority Control, which causes the execution of: instruction RPT, RPT Transfer Routine TIME4RPT, and program section T4RUPT. See table 15-8.
0041	UPLINK	This counter converts serial uplink data into parallel information. The content of the counter is shifted to the left by adding a ZERO in bit position 1 by means of instruction SHINC, or is shifted to the left by adding a ONE in bit position 1 by means of instruction SHANC. This occurs each time an ULNK0 or ULNK1 signal is received from Uplink. When the flag bit of an uplink word (first bit is always a ONE) moves into bit position 16 (figures 2-39 through 2-41), control signal RP5 is generated in the Interrupt Priority Control, which causes the execution of instruction RPT, which in turn initiates the execution of RPT Transfer Routine UPLINKRPT and program section UPRUPT (Uplink and Radar Processor). See table 15-8.

CONFIDENTIAL

CONFIDENTIAL

TABLE 15-5
E REGISTER ASSIGNMENTS I (cont.)

Octal Address	Initials	Name and Purpose
0042	OUTCR1	Out counter 1 is for the IMU and the IMU CDU's. This counter is preset under program control and incremented by instruction PINC whenever a drive pulse is sent to the IMU or the IMU CDU's. Overflow of counter OUTCR1 causes the clearing of bit position 9 through 16 of register OUT2.
0043	OUTCR2	Out counter 2 is for the Optics and the thrust control. This counter is preset under program control and incremented by instruction PINC whenever a drive pulse is sent to the Optics or the thrust control. Overflow of counter OUTCR2 causes the clearing of bit positions 4 through 8 of register OUT2.
0044	PIPA X	This input counter is incremented or decremented by instructions PINC and MINC each time a +DVX or -DVX signal is received from PIPA X. This input counter is incremented or decremented by instructions PINC and MINC each time +DVY or -DVY signal is received from PIPA Y. This input counter is incremented or decremented by instructions PINC and MINC each time a +DVZ or -DVZ signal is received from PIPA Z. This input counter is incremented or decremented by instructions PINC* and MINC* each time a +XCDU or -XCDU signal is received from IMU CDU X.
0045	PIPA Y	
0046	PIPA Z	
0047	CDU X	

* Whenever register S contains address 0047, 50, 51, 52, or 53, the Adder is signaled to add angular data instead of linear data (normal operation).

CONFIDENTIAL

CONFIDENTIAL

TABLE 15-5
E REGISTER ASSIGNMENTS I (cont)

Octal Address	Initials	Name and Purpose
0050	CDU Y	This input counter is incremented or decremented by instructions PINC* and MINC* each time a +YCDU or -YCDU signal is received from IMU CDU Y. This input counter is incremented or decremented by instructions PINC* and MINC* each time +ZCDU or -ZCDU signal is received from IMU CDU Z.
0051	CDU Z	
0052	OPTX	This input counter is incremented or decremented by instructions PINC* and MINC* each time an OPT +X or OPT -X signal is received from Optics CDU X. This input counter is incremented or decremented by instructions PINC* and MINC* each time an OPT +Y or OPT -Y signal is received from Optics CDU Y.
0053	OPTY	
0054	TRKRX	This input counter is reserved for star tracker and radar tracker x information. This input counter is reserved for star tracker and radar tracker y information. This input counter is reserved for converting serial radar data (range, range rate, etc.) into parallel information. The content of the counter is shifted to the left by adding a ZERO in bit position 1 by instruction SHINC, or is shifted to the left by adding a ONE in bit position 1 by instruction SHANC each time a + or - signal is received from the radar tracker. When overflow occurs, a control signal RP5 is generated, which causes the same actions as described for counter 0041 (UPLINK).
0055	TRKRY	
0056	TRKRR	
0057	OUTCR3	Out counter 3 is reserved for radar. This counter is preset under program control and incremented by instruction PINC whenever a drive pulse is sent to the radar. Overflow of counter OUTCR3 causes clearing of bit positions 1 through 3 of register OUT2.

* Whenever register S contains address 0047, 50, 51, 52, or 53, the Adder is signaled to add angular data instead of linear data (normal operation).

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

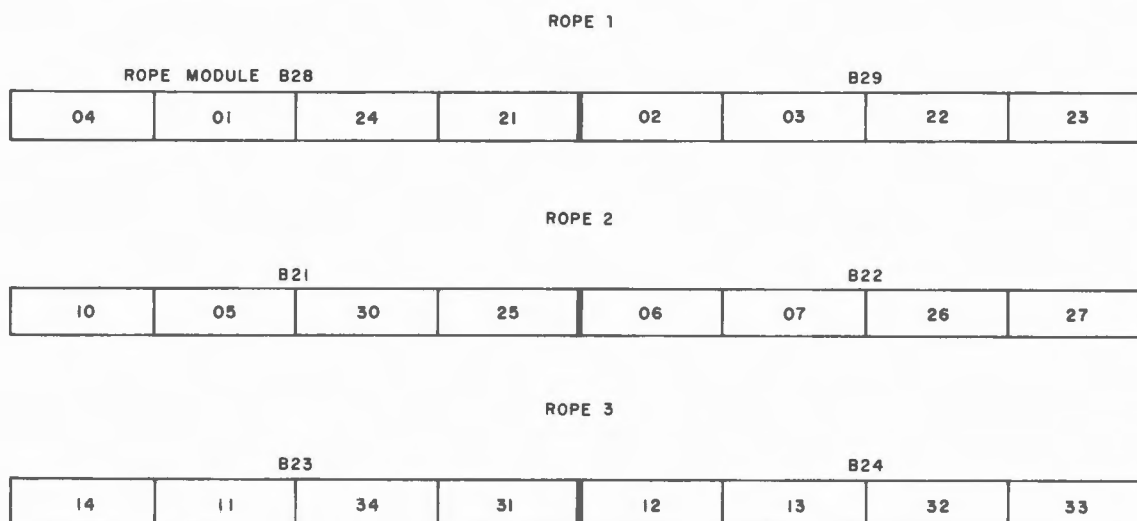


Figure 15-11. Core Ropes, Rope Modules, and Address Banks

1110

15-42. All words stored in E and F memory consist of sixteen bits; fifteen bits of information in bit positions 15 through 1 and one parity bit in bit position 0. Whenever a word is transferred from E or F memory into register G, bits 0 through 15 of that word are gated from their positions in E or F memory into the corresponding bit positions of register G. The same is true also for any transfer from register G to E memory, as indicated in the last two entries of table 15-1. Bit position 15 might contain the sign bit of a data word or any other information. The E and F memories are controlled such that one word can be transferred from them into register G prior to Action 7 of an MCT, and one word can be transferred from register G to E memory after Action 9 of an MCT (except the repetitive loops of instructions MP and DV). Control signal SBF or SBE cause transfer from E or F memory to register G, and control signal ZID causes a word to flow from register G to E memory. Signals SBF, SBE, and ZID are generated by the Memory Cycle Timing (figure 15-7).

15-43. INPUT INFORMATION AND PRIORITY CONTROL

15-44. Input information to the AGC subsystem can be binary data or incremental data which is entered into an input register and/or the Priority Control via the AGC interface circuitry. Some signals controlling the Downlink Converter are also entered into the AGC via the interface circuitry.

CONFIDENTIAL

FR-2-115

15-45. BINARY INPUT DATA AND INTERRUPT PRIORITY CONTROL

15-46. Binary input data can be a dc signal which is generated at the DSKY, at the Optics, or by a relay in the IMU. These signals are fed through the AGC interface circuitry (figure 15-7) and set a bit position (one flip-flop) of register IN0, IN1, or IN2. Binary input information can also be a pulse train received from the SCS, the CDU's the IMU, etc. The pulse trains are fed into a transformer within the AGC interface circuitry and they also set a bit position of the same input registers. Each of these input registers is reset at write time (the time the content of that register is transferred to another CP register). The bit assignments of the input registers are indicated on the first page of table 15-6.












15-47. Some of the binary data is also entered into the Interrupt Priority Control via the AGC interface circuitry. This data causes the Interrupt Priority Control to generate signals RP4, TRP4, or TRP2 as indicated in table 15-7. The overflow of some counters causes the Interrupt Priority Control to generate signals RP1, RP3, and RP5 as mentioned in table 15-5. Signal DKEND, which is received from the Downlink Converter, causes the Interrupt Priority Control to generate signal RP6. Any one of the above signals causes the Interrupt Priority Control to signal the SQG to execute instruction RPT. Instruction RPT interrupts the execution of a program section or routine in favor of one of higher priority. Table 15-7 describes the various operations the computer performs once the Interrupt Priority Control has been activated.

15-48. The RPT instruction transfers the content of registers Z and B to register ZRUPT and BRUPT (table 15-5) and initiates the execution of the proper RPT Transfer Routine. The RPT Transfer Routine transfers the content of registers A and Q to registers ARUPT and QRUPT, and transfers program control to the interrupting program section. Before the execution of the interrupting program section is completed, it returns the content of registers QRUPT and ARUPT to registers Q and A. Instruction RSM, the last instruction of the interrupting program section, returns the content of registers BRUPT and ZRUPT to registers B and Z. Instruction RSM also causes the SQG to resume the execution of the interrupted program section.

15-49. The Interrupt Priority Control prevents an interrupting program section from being interrupted. Instead, the Interrupt Priority Control preserves any request for the execution of a program section of higher priority until the complete execution of the interrupting program

(text continued on page 15-37)

TABLE 15-6
IN AND OUT REGISTER BIT ASSIGNMENT

REGISTER	OCTAL ADDRESS	BIT POSITION 															
		16,15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
IN0	0004	MARK (102) [RP4 KEYRUPT]	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	INHIBIT UPSYNC 	ACCEPT UPLINK (246)	KEY CODE BITS [TRP4 KEYRUPT]					
												5 (205)	4 (204)	3 (203)	2 (202)	1 (201)	
IN1	0005	16 BITS REPRESENTS CONDITION OF TIME SCALER B (BITS 16 THROUGH 1)															
IN2	0006	PARITY ALARM 	SPARE	SPARE	IMU FAIL (141)	PIPA FAIL (138)	CDU FAIL (124)	SPARE	SPARE	SPARE	SPARE	SPARE	TIME SIGNALS 				
					SCANNED BY T4RUPT			[TRP2]					200 PPS	400 PPS	800 PPS	1600 PPS	
IN3	0007	OR OF C RELAYS (210)	OPTICS MODE BITS - SCANNED BY T4RUPT					SPARE	SPARE	IMU MODE BITS - SCANNED BY T4RUPT							
			5 (106)	4 (105)	3 (104)	2 SPARE	1 (107)			7 (163)	6 (164)	5 (162)	4 (161)	3 (160)	2 (159)	1 (158)	
OUT0	0010	RELAY WORDS				RELAY BITS											
		4 (228)	3 (227)	2 (226)	1 (225)	11 (224)	10 (223)	9 (222)	8 (221)	7 (220)	6 (219)	5 (218)	4 (217)	3 (216)	2 (215)	1 (214)	
OUT1	0011	SPARE	SPARE	ENGINE ON 	SPARE	SPARE	BLOCK DOWNLINK 	ID WORD 	SPARE	RUPT TRAP RESET  [TRP2]	SPARE	CHECK FAIL ALARM (232)	TELEMETRY ALARM (231)	KEY RELEASE (236)	COMPUTER ACTIVITY (230)	PROGRAM ALARM (229)	
OUT2	0012	OUTCR1 						OUTCR2 				OUTCR3 					
		-	+	IMU CDU'S	IMU GYRO'S	X	Y	Z	-	+	OPT X CDU	OPT Y CDU	THRUST	RADAR A	RADAR B	RADAR C	
IN OR OUT3		SPARE REGISTER, NOT CONNECTED															
OUT4		16 BITS FOR DOWNLINK DATA (BITS 15 THROUGH 0)															


SEE NEXT PAGE FOR NOTES

TABLE 15-6 (cont)
IN AND OUT REGISTER BIT ASSIGNMENTS

Note

- 0 Numbers in () indicate interface signal numbers (column one of table 15-0) of input signals setting IN registers or output signals supplied by OUT registers.
- Names in [] indicate an associated RP or TRP signal generated in the Interrupt Priority Control and the associated RPT routine to be executed.
- 407 DC signal generated in AGC is fed into this bit position.
- 601 Time signals generated in AGC are fed into these bit positions.
- 615 DC signal generated in AGC is fed into this bit position to initiate the execution of RESTART.
- 1107 DC signal generated in AGC to reset Error Tray Flip-Flop in Interrupt Priority Control.
- 1109 DC signal which controls Downlink Converter to generate a downlink identification word.
- 1110 DC signal which controls Downlink Converter to block downlink data transmission.
- 1113 DC signal which controls Rate Control to generate signal 011.
- 1201 DC signals which control Rate Control.
- 1204 DC signals which control Rate Control. Bit position 8 through 5 control the generation of signals 114 through 117.
- 1209 DC signals which control Rate Control to generate signals 126 through 131 and 142 through 147.

TABLE 15-7
INTERRUPT MOTIONS

Level of Priority	Initiating Action	Signal Generated in Interrupt Priority Control	Instruction and RPT Transfer Routine Executed	Further Actions Caused
1	Overflow of TIME3 counter	RP1	RPT TIME3RPT	1. Execution of major routine T3RUPT of Task Control (Issue 12A). 2. Execution of Task due.
2	Presently none	TRP2	RPT ERRORRPT	1. Execution of subroutine ERRUPT. 2. Processing of alarm information
3	Overflow of TIME4 counter	RP3	RPT TIME4RPT	Execution of T4RUPT to: transfer next word to DSKY's drive IMU CDU's and Optics CDU's collect current IMU and Optics Mode bits check IMU and Optics mode scan IMU FAIL, PIPA FAIL, and CDU FAIL bit, and display failures check downlink rates.
4	KEYCODE signal from a DSKY	TRP4	RPT KEYMARPT	1. Execution of KEYRUPT to process mark and mark accept information. 2. Execution of program section Keyboard and Display to process keycode information.
	Signal MARK from Optics	RP4		
5	Flag bit of word in UPLINK counter or TRKR R counter moving into bit position 16 	RP5	RPT UPLINRPT	1. Execution of UPRUPT. 2. Execution of program section Keyboard Display to process keycode information.
6	Signal DKEND from Downlink Converter	RP6	RPT DOWNLRPT	Execution of DOWNRUPT to supply telemetry to register OUT4 for downlink equipment

 See figure 2-39 through 2-41.

15-36

CONFIDENTIAL

Changed 18 December 1964

FR-2-115

CONFIDENTIAL

section. Sometimes it is desirable to inhibit program interruptions. This can be done by executing instruction INHINT (NSX 0017). Instruction RELINT (NDX 0016) releases the inhibition of a program interrupt. Executing INHINT or RELINT addresses location 0017 or 0816 respectively (see table 15-4) which in turn signals the Interrupt Priority Control to inhibit any program interruption, or to release the program interruption.

15-50. INCREMENTAL INPUT DATA AND THE COUNTER PRIORITY CONTROL

15-51. Incremental inputs are individual pulses which are fed through a transformer within the AGC interface circuits to the Counter Priority Control. The overflow of certain counters listed in table 15-5 causes the generation of incremental pulses which are also fed to the Counter Priority Control. Incremental pulses may represent a positive or a negative quantity of equal magnitude. To accomplish serial-to-parallel conversion a word is shifted one position to the left by adding a ZERO or ONE in bit position 1.

15-52. The Counter Priority Control receives input data on 33 different lines as indicated in table 15-8; 18 lines are for increment requests, 11 are for decrement requests and 4 are for shift requests. Each incremental input pulse is first stored in the Counter Priority Control. The Counter Priority Control then addresses the proper counter and signals the SQG to execute the following instructions:

- a. PINC (positive increment)
- b. MINC (negative increment or decrement)
- c. SHINC (shift by adding a ZERO in bit position 1)
- d. SHANC (shift and add, i. e. shift by adding a ONE in bit position 1).

The SQG executes this instruction as soon as permissible after the complete execution of a Regular Instruction. If more than one incremental input signal is present at the same time, the priority chain (part of Counter Priority Control) decides the sequence in which the input data is to be handled. The level of priority decreases as the address of the counters increases. The AGC is capable of accepting incremental input data at a maximum rate of 85 kpps.

CONFIDENTIAL

TABLE 15-8
COUNTER PRIORITY CONTROL INPUTS

Input Number	Level of Priority	Input Signal	Instruction Executed
1 2	1 1	Overflow } occurs during the ex- Underflow } ecution of instruction } AD K or SU K	PINC OVCTR MINC OVCTR
3 4 5 6	3 2 4 5	10 msec time signal from Scaler A Overflow of counter TIME1 10 msec time signal from Scaler A 10 msec time signal which occurs 5 msec later than input signals 3 and 5	PINC TIME1 PINC TIME2 PINC TIME3 PINC TIME4
7 8	6 6	ZERO from Uplink ONE from Uplink	SHINC UPLINK SHANC UPLINK
9 10 11	7 8 20	Signal from register OUT2, bits 9 through 16 Signal from register OUT2, bits 4 through 8 Signal from register OUT2, bits 1 through 3	PINC OUTCR1 PINC OUTCR2 PINC OUTCR3
12 13 14 15 16 17	9 9 10 10 11 11	+DVX from PIPA X -DVX from PIPA X +DVY from PIPA Y -DVY from PIPA Y +DVZ from PIPA Z -DVZ from PIPA Z	PINC PIPA X MINC PIPA X PINC PIPA Y MINC PIPA Y PINC PIPA Z MINC PIPA Z
18 19 20 21 22 23	12 12 13 13 14 14	+XCDU from IMU CDU X -XCDU from IMU CDU X +YCDU from IMU CDU Y -YCDU from IMU CDU Y +ZCDU from IMU CDU Z -ZCDU from IMU CDU Z	PINC CDU X MINC CDU X PINC CDU Y MINC CDU Y PINC CDU Z MINC CDU Z
24 25 26 27	15 15 16 16	OPT+X from Optics OPT-X from Optics OPT+Y from Optics OPT-Y from Optics	PINC OPTX MINC OPTX PINC OPTY MINC OPTY
28 29 30 31 32 33	17 17 18 18 19 19	Reserved for signals from star tracker and/or tracking radar	PINC TRKR X MINC TRKR X PINC TRKR Y MINC TRKR Y SHINC TRKR R SHANC TRKR R

15-53. OUTPUT INFORMATION AND THE OUTPUT CONTROL

15-54. Output information from the AGC can be binary dc signals, pulse trains, or controlled pulse bursts. Most output information is supplied to the interface circuitry by register OUT0, register OUT1, and the Output Control consisting of the Rate Control, the Downlink Converter and the Alarm Control. Some additional output signals are supplied directly to the interface circuitry. Registers OUT0 and OUT1 supply binary dc signals to the DSKY's via the interface circuitry. Data contained in some bit positions of register OUT1 and all bit positions of register OUT2 regulate the Rate Control. The Rate Control generates continuous pulse bursts of 3200 pps and delivers them to transformers within interface circuitry. The Downlink Converter supplies serial downlink data pulses which also terminate at transformers within the interface circuitry. The Alarm Control generates dc signals which represent failures in various sections of the AGC. These alarm signals are displayed on the Navigation Panel DSKY. An additional dc signal, AGC POWER FAIL, is generated in the power supply and displayed on the main panel. The Timer provides time pulse signals to transformers within the interface circuitry.

15-55. AGC OUTPUTS TO DSKY'S

15-56. The dc signals provided by registers OUT0 and OUT1 (refer to table 15-6) are set and cleared under program control. All bit positions of register OUT0 control relay matrices in the DSKY's. Bits 1 through 5 of register OUT1 control indicators PROG ALM, COMP ACTIVITY, KEY RLSE, TM FAIL, and CHECK FAIL on the Navigation Panel DSKY. The Alarm Control generates dc signals which control indicators CTR FAIL, RUPT LOCK, TC TRAP, SCALER FAIL, and PRTY (parity) FAIL.

15-57. CONTROLLED PULSE BURSTS

15-58. Register OUT2 is set under program control. Bit positions 9 through 16 are cleared by the overflow of counter OUTCR1, bit positions 4 through 8 by the overflow of counter OUTCR2, and bit positions 1 through 3 by the overflow of counter OUTCR3 (table 15-6). Bits 9 through 15 (bit 15 contained in bit position 15 and 16) control the Rate 1 Control, bits 4 through 8 the Rate 2 Control, and bits 1 through 3 the Rate 3 Control. The Rate 1 Control generates pulses CDUX+,

CONFIDENTIAL

FR-2-115

CDUX-, CDUY+, CDUY-, CDUZ+, CDUZ-, +DX, -DX, +DY, -DY, +DZ, and -DZ on 12 different output lines. The Rate 1 Control pulses drive the IMU CDU's or the IMU gyros. The Rate 2 Control generates pulses +XOPT CDU, -XOPT CDU, +YOPT CDU, -YOPT CDU, +THRUST and -THRUST in 6 different output lines. The Rate 2 Control pulses drive the Optics and control thrust. The Rate 3 Control generates pulses which drive the radar.

15-59. Each of the three Rate Controls generates a predetermined number (n) of 3200 pps drive pulses on a certain output line by:

- (1) setting the content of counter OUTCR1, OUTCR2, or OUTCR3 to (40000-n)
- (2) setting register OUT2 properly
- (3) counting the pulse sets released by Rate Controls 1, 2, or 3 to the content of OUTCR1, OUTCR2, or OUTCR3
- (4) clearing the proper section of register OUT2 at overflow of OUTCR1, OUTCR2, or OUTCR3.

For example, bits 14, 13, and 11 of register OUT2 must be set to send CDUX+ drive pulses on the IMU CDU X+ line which drives the X IMU CDU in the positive direction.

15-60. AGC OUTPUTS TO CSM

15-61. Bit positions 13 through 15 of register OUT1 regulate the Rate 4 Control. The Rate 4 Control is able to send 3200 pps pulse trains on three output lines for the period the corresponding bit position of register OUT1 is set. These outputs are supplied to the CSM for controlling the S-IVB engine. Signal AGC POWER FAIL and various timing signals are also supplied to the CSM.

15-62. AGC OUTPUTS TO DOWNLINK TELEMETRY

15-63. Register OUT4 is set under program control and provides information to be sent to ground stations via Downlink Telemetry. Downlink Converter, which is under the control of signals received from the CSM telemetry system and signals provided by bit positions 9 and 10 of register OUT1, generates the AGC serial downlink data. The

15-40

CONFIDENTIAL

Downlink Converter generates signal DKEND (see table 15-7) to reload register OUT4 after the word previously contained in the register has been sent downlink. The downlink data generated by the Downlink Converter is sent to the CSM telemetry system where it is transmitted to ground stations together with downlink data from other CSM systems.

15-64. DISPLAY AND KEYBOARDS

15-65. The Navigation Panel DSKY and the Main Panel DSKY (figures 15-4 through 15-6) allow an operator to communicate with the AGC. Commands and information (dc signals) can be fed into the AGC and requested information can also be displayed. In addition, the DSKY's provide various dc signals which control other G&N subsystems and CSM systems. Various indicators are provided to indicate certain operational conditions and failures. Each DSKY consists of a keyboard, various displays, a number of relays, and an integral power supply. The relays control the displays and initiate signals used in other subsystems and systems.

15-66. KEYBOARDS

15-67. Each DSKY has 10 digit keys (0 through 9) and 8 operation keys (+, -, CLEAR, VERB, NOUN, ENTER, KET RLSE, and ERROR RESET). These 18 keys, when depressed, generate 18 different five-bit key codes, which are fed into bit positions 1 through 5 of register IN0 (table 15-7). Only one key code can be generated at a time due to the way in which the contacts of the 18 keys are interconnected. Any key code bit entered into bit positions 1 through 5 of register IN0 causes the Interrupt Priority Control to generate signal TRP4 and to initiate certain interrupt actions as shown in table 15-7. When none of the keys are depressed, the keyboard sends signal KYRST to the Interrupt Priority Control. This signal KYRST resets its Keyboard Trap circuitry indicating that no other keyrupt action is presently requested.

15-68. Function KEYRUPT (table 15-7) interrogates bit positions 1 through 5, and bit position 15, of register IN0 to determine if the Interrupt Priority Control was triggered by a key code bit, or a signal (MARK or ACC MARK) entered into bit position 15. If information in bit position 15 triggered the program interruption, function KEYRUPT processes the MARK or ACC MARK signal (refer to note A of table 15-6). If a key code bit caused the program interruption, program control is transferred to program section Keyboard And Display for processing the keyboard information.

CONFIDENTIAL

FR-2-115

15-69. The ERROR RESET key does two things when pressed. It enters a five-bit key code in register IN0 as previously described. When this occurs, program section Keyboard and Display clears bit positions 1, 4, 5, 7, and 10 of register OUT1 (table 15-6). In addition, the ERROR RESET key generates a dc signal which resets the Alarm Control (figure 15-7). This allows an astronaut to check whether an error signal is generated by a program (PROGRAM ALARM, TELEMETRY ALARM, CHECK FAIL, RUPT TRAP, or BLOCK DOWNLINK) or by the Alarm Control (COUNTER FAIL, RUPT LOCK, TC TRAP, or PARITY FAIL) is permanent or intermittent.

15-70. The TEST ALARM key, which is provided on the Navigation Panel DSKY only, sends signal ALTST to the Alarm Control to set the alarm flip-flops. When the TEST ALARM key is pressed the alarm flip-flops are set and indicators COUNTER FAIL, RUPT LOCK, TC TRAP, and PARITY FAIL light.

15-71. The UPTL switch, which is provided on the Main Panel DSKY only, controls the reception of Uplink data. If this switch is in position BLOCK, information or commands can not be entered into the AGC subsystem by Uplink. This prevents interference with any operation an astronaut may want to perform.

15-72. RELAY MATRICES

15-73. Both the Navigation Panel and the Main Panel DSKY contain 14 relay banks, each containing 11 latched relays. However, only 13 banks are used. Each of the 13 banks is addressed by a certain relay word (various combinations of bits 12 through 15 in register OUT0, table 15-6). A relay within an addressed bank is energized by applying one relay bit (bits 1 through 11 of register OUT0) to that relay.

15-74. Eleven banks of relays in each DSKY, which are addressed by relay words 01 octal through 13 octal, control the character displays (PROGRAM, VERB, NOUN, and three 5-digit displays registers) and indicator UPTL ACTIVITY. The indicator COMP ACTIVITY is controlled by a relay outside the relay matrix.

15-75. One bank of relays in each DSKY is addressed by relay word 14 octal. This bank generates signals which control relays and displays in the IMU and the telemetry subsystem. Refer to tables 15-9 and 15-10.

TABLE 15-9
ACTIONS INITIATED BY RELAY BANK 14
IN THE NAVIGATION PANEL DSKY

Relay Energized by Relay Bit	Actions Taken
1	Generates signal 307 (ZERO ENCODER) which controls relay K1 of IMU.
2	Generates signal 308 (COARSE ALIGN) which controls relay K2 of IMU.
3	Generates signal 309 (LOCK CDUS) which controls relay K3 of IMU.
4	Generates signal 310 (FINE ALIGN) which controls relay K4 of IMU.
10	Generates signal 314 (ATTITUDE CONTROL) which controls relay K12 of IMU.
11	Generates signal 311 (ROLL RE-ENTRY) which controls relay K5 of IMU.
6	Generates signal 302 (CDU FAIL) which controls indicator CDU FAIL on the Data Viewer of the Navigation Control and Display Panel.
7	Generates signal 303 (PIPA FAIL) which controls indicator PIPA FAIL on the Data Viewer of the Navigation Control and Display Panel.
8	Generates signal 304 (IMU FAIL) which controls indicator IMU FAIL on the Data Viewer of the Navigation Control and Display Panel.
5	Generates signal 301 (ENCODER ZEROING) which controls indicator ENCODER ZEROING on the Data Viewer of the Navigation Control and Display Panel.
9	Spare

CONFIDENTIAL

FR-2-115

TABLE 15-10
ACTIONS INITIATED BY RELAY BANK 14
IN THE MAIN PANEL DSKY

Relay Energized by Relay Bit	Actions Taken
6	Generates signal 402 (CDU FAIL) which controls indicator CDU FAIL on the Main Display and Control Panel, and signal 425 (CDU FAIL) which is sent to the CSM telemetry system.
7	Generates signal 403 (PIPA FAIL) which controls indicator PIPA FAIL on the Main Display and Control Panel, and signal 426 (PIPA FAIL) which is sent to the CSM telemetry system.
8	Generates signal 404 (IMU FAIL) which controls indicator IMU FAIL on the Main Display and Control Panel, and signal 427 (IMU FAIL) which is sent to the CSM telemetry system.
5	Generates signal 404 (ENCODER ZEROING) which is sent to the CSM telemetry system.
1 thru 4 9 thru 11	Spare

TABLE 15-11
ACTIONS INITIATED BY RELAY BANK 15
IN THE NAVIGATION PANEL DSKY

Relay Energized by Relay Bit	Actions Taken
1	Generates signal 316 (ZERO OPT) which controls Optics.
2	Generates signal 317 (STAR TRKR ON) which controls Star Tracker.
3 thru 11	Spare

Any bank 14 relay in either DSKY may generate an OR signal which is entered into bit position 15 of register IN3 (table 15-6). In the Navigation Panel DSKY eleven signals are OR'ed (tables 15-9 and 15-11) and in the Main Panel DSKY three signals are OR'ed (table 15-10). The OR signal is supplied to bit positions 16 and 15 of register IN3.

15-76. The relay word 15 octal addresses a bank of relays in the Navigation Panel DSKY only. The signals generated by these relays are described in table 15-11. The relay word 16 octal addresses a bank of relays in the Main Panel DSKY only. None of these relays is presently used.

15-77. NON-MATRIX RELAYS

15-78. Each DSKY also contains 12 simple (non-latched) relays of which 10 are presently used to display various auxiliary information and generate various auxiliary signals. Bits 1 through 5 of register OUT1 are under program control. These bits initiate dc signals on 5 different lines, and each line controls one relay in each DSKY. These five relays on the Navigation Panel DSKY control indicators PROG ALM, TM FAIL, CHECK FAIL, KEY RLSE, and COMP ACTIVITY. (Indicator CHECK FAIL indicates improper keyboard manipulation, i. e. pressing wrong keys.) The Alarm Control (figure 15-7) generates dc signals on another 5 lines which control another set of 5 relays on each DSKY. The five relays on the Navigation Panel DSKY control indicators CTR FAIL, RUPT LOCK, TC TRAP, SCALER FAIL, and PRTY FAIL. Fail signals PROG ALM, TM FAIL, CHECK FAIL, CTR FAIL, RUPT LOCK, TC TRAP, SCALER FAIL, and PRTY FAIL are OR'ed and the OR signal is sent to the IMU.

15-79. All 10 signals which are generated by the 10 non-matrix relays in the Main Panel DSKY are fed into the CSM telemetry system. An OR signal of the eight failure signals controls indicator COMP FAIL (Computer Fail) on the Main Panel DSKY.

15-80. INSTRUCTIONS**15-81. WORDS FORMATS AND INSTRUCTION TYPES**

15-82. Data words, instruction words, and address words consist of sixteen bits when stored in Fixed or Erasable Memory. The bits are numbered 0 through 15 reading from right to left. As indicated in figure 15-12, bit position 0 is always reserved for the parity bit, P. The parity bit provides a simple means of detecting single errors or any uneven number of errors when reading out of Fixed or Erasable Memory. If the number of ONE's contained in bit positions 1 through 15 is an even number, bit position 0 contains a ONE. This brings the total number of ONE's contained in a word to an uneven number. If the number of ONE's contained in bit positions 1 through 15 is an uneven number, bit position 0 contains a ZERO. This leaves the total number of ONE's contained in a word at an uneven number. Bit position 1 contains the lowest order digit and 15 the highest. Data words stored in Fixed or Erasable Memory consist normally of a sign bit (SG) in position 15, fourteen value bits, and the parity bit. A ZERO in position 15 represents a plus sign, a ONE a minus sign.

15-83. Two types of instructions can be written in an AGC program: Basic Instructions and Interpretive Instructions. A Basic Instruction is composed of a three-bit order code in bit positions 15 through 13, a twelve-bit address code (relevant address) in bit positions 12 through 1, and the parity bit. The order code of an Interpretive Instruction consists of seven bits. An Interpretive Instruction Word can contain two such order codes in bit positions 14 through 8, and 7 through 1, or one such order code plus a seven-bit code. The seven-bit code indicates the number of Interpretive Instruction Words immediately following the first instruction word a string (group) of Interpretive Instruction and Address Words. An Interpretive Instruction Word is stored in F memory in its incremented and complemented form, and identified by a ONE in bit position 15. An Interpretive Address Word is stored in F memory in its incremented form. Normally, an Interpretive Address Word contains a ZERO in bit position 15 to distinguish it from an Interpretive Instruction Word. If an Interpretive Address Word is not the first one of an address string, it may contain a ONE in bit position 15. An interpretive string consists of a string (group) of Interpretive Instruction Words and a String of Interpretive Address Words.

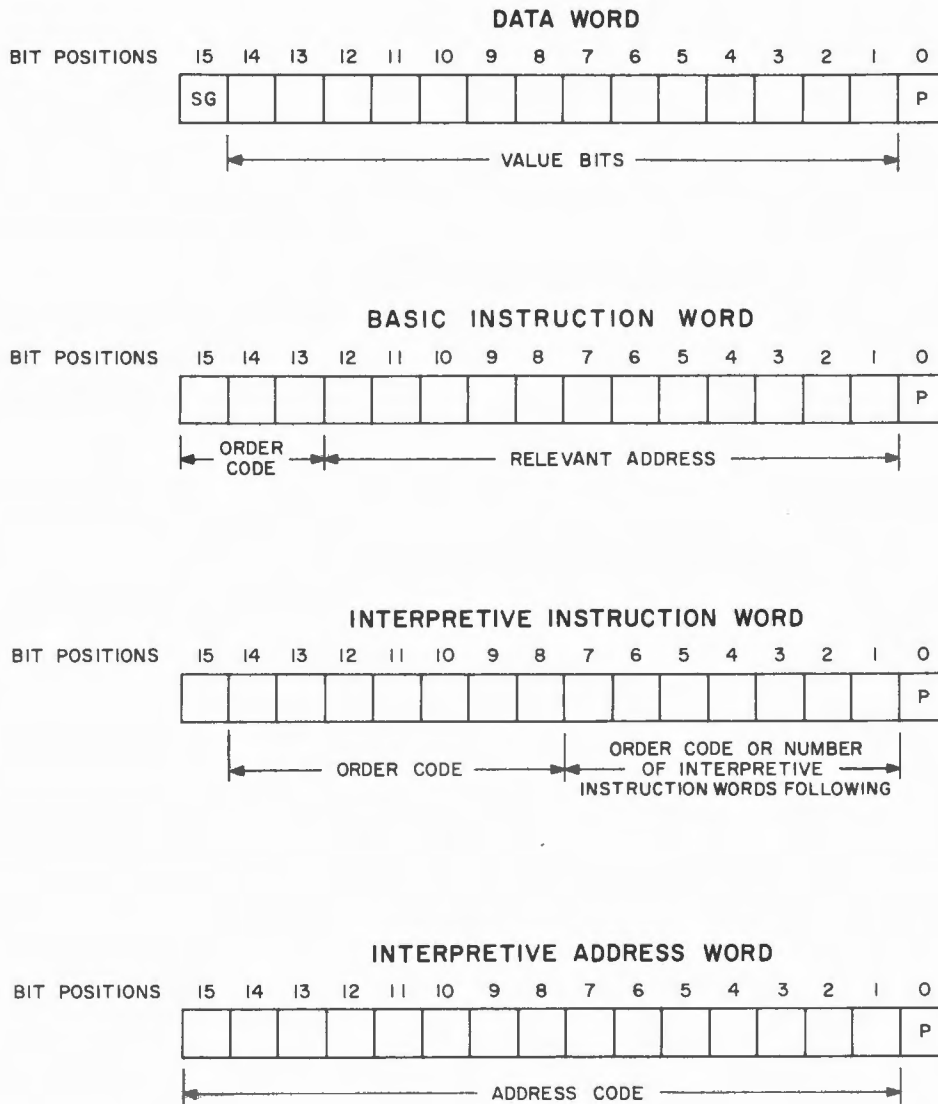


Figure 15-12. Word Formats

15-84. The variety of instruction types provided for the AGC can be divided into two main groups: Machine Instructions, which are built into the Sequence Generator (SQG) and Interpretive Instructions, which are built into program section Interpreter.

15-85. MACHINE INSTRUCTIONS

15-86. All Machine Instructions are listed in table 15-12. Order codes are given in octal numbers. A Machine Instruction consists of one, two, or more subinstructions. A subinstruction is defined as a sequence of 12 Actions. An Action is defined as a set of control pulses (paragraph 15-14). A subinstruction is executed in one MCT (11.7 msec). The Machine Instruction can be grouped into Regular Instructions, Involuntary Instructions and Miscellaneous Machine Instructions. Table 15-12 also lists the number of MCT's required to execute the various Machine Instructions. The MCT listed for the Extra Code Instructions includes the time needed to derive the order code for the instruction. All Machine Instructions are analyzed in Issue 2 of the AGCIS.

15-87. Regular Instructions can be divided into Basic Instructions and Extra Code Instructions. Basic Instructions can be written into a program, which is normally stored in F memory and executed as their order codes are entered into the SQ register (paragraph 15-15). The Extra Code Instructions cannot be written into a program. Their order codes are derived by indexing Basic Instructions (modifying with underflow additions) and are executed as the modified order codes are entered into register SQ. Basic and Extra Code Instructions are Regular Instructions, since their execution is under the control of programs. The symbol K after the instruction codes represents the relevant address of the data to be processed.

15-88. The Involuntary Instructions can be divided into Priority Program Instructions and Counter Instructions. The execution of Interrupt Instruction RUPT is initiated by RP and TRP signals (paragraph 15-47). Instruction RSM (resume) is really a special instruction, NDX 0025, but has been added to the group of Priority Program Instructions since it concludes a program interruption. The execution of Counter Instructions PINC, MINC, SHINC, and SHANC is initiated by incremental pulses (paragraphs 15-51 and 15-52). Counter Instructions do not interrupt the execution of a program and cause only a small delay in the execution.

TABLE 15-12
MACHINE INSTRUCTIONS

Initials	Purpose	Order Code		Subinstruction	Execution Time in MCTs
		Written into Program	Entered into SQ		
REGULAR INSTRUCTIONS					
Basic Instructions					
TC K	Transfer Control to K	0	00	TC0	1
XCH K	Exchange Data in A with Data of K	3	03	XCH0, STD2	2
CS K	Clear A and Subtract Data in K	4	14	CS0, STD2	2
TS K	Transfer Data to K	5	15	TS0, STD2	2
MSK K	Mask (AND) with Data from K	7	17	MSK0, STD2	2
AD K	Add Data from K and count on overflow or underflow	6	16	AD0, STD2	2
	In case of overflow			also PINC	3
	In case of underflow			also MINC	3

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TABLE 15-12
MACHINE INSTRUCTIONS (cont)

Initials	Purpose	Order Code		Subinstruction	Execution Time in MCTs
		Written into Program	Entered into SQ		
NDX K	Index (Modify) Next Instruction	2	02	NDX0, NDX1	2
CCS K	Count, Compare, and Skip with Data at K	1	01	CCS0, CCS1	2
Extra Code Instructions					
SU K	Subtract Data from K and count on overflow or underflow	6	13	SU0, STD2	4
	In case of overflow			also PINC	5
	In case of underflow			also MINC	5
MP K	Multiply with Data at K	4	11	MP0, MP1, MP3	10
DV K	Divide by Data at K	5	12	DV0, DV1, STD2	18

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TABLE 15-12
MACHINE INSTRUCTIONS (cont)

Initials	Purpose	Subinstruction	Execution Time in MCTs
INVOLUNTARY INSTRUCTIONS			
Priority Program Instructions			
RPT	Interrupt program	RPT1, RPT3, STD2	3
RSM	Resume program	NDX0, RSM	2
Counter Instructions 			
PINC	Increment content of addressed counter	PINC	1
MINC	Decrement content of addressed counter	MINC	1
SHINC	Shift content of addressed counter	SHINC	1
SHANC	Shift content of addressed counter and add one	SHANC	1

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TABLE 15-12
MACHINE INSTRUCTIONS (cont)

Initials	Purpose	Subinstruction	Execution Time in MCTs
MISCELLANEOUS MACHINE INSTRUCTIONS			
Start Instructions			
GO	Computer GO	GO	1
TCSA	Start at specified address	TCSA	1
Display and Load Instructions			
OINC	Display content of addressed location	OINC	1
LINC	Load addressed location	LINC	1



Whenever register S contains an address between 0047 and 0053, the Adder is signaled to add angular data instead of linear data (normal operation).

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FR-2-115

15-89. Some Miscellaenous Instructions are provided for starting, loading, and testing the AGC. Instruction GO can be initiated by an astronaut, the start sequence, an alarm, or test equipment.

15-90. INTERPRETIVE INSTRUCTIONS

15-91. All Interpretive Instructions are listed in table 15-13. Order codes are given in octal numbers. An Interpretive Instruction is defined as a sequence of Basic Machine Instructions. The Interpretive Instructions can be written into a program, as can any Basic Instruction. However, the Interpretive Instructions are decoded by the Interpreter, which transforms them into a sequence of Basic Instructions.

15-92. The Interpreter is a highly sophisticated program section the purpose of which is to execute program portions written in interpretive language (paragraph 15-6 and Issue 12). The Interpreter consists of approximately 1500 Regular Instructions and contents. Interpretive program portions are composed of Interpretive Instructions (Interpretive Instruction Words and Interpretive Address Words, as shown in figure 15-12). Basic program portions are composed of Regular Instructions. Interpretive program portions consist of one or more program strings (word groups). Each program string has an instruction string (group of Interpretive Instruction Words) followed by an address string (group of relevant Interpretive Address Words). Interpretive program portions are able to perform double-precision (DP), triple-precision (TP), and vector double-precision (V) operations.

15-93. As indicated in figure 15-12, the order code of an Interpretive Instruction consists of seven bits, permitting 128 different order codes. The Interpretive Instructions can be grouped into Dual Quantity Instructions, Single Quantity Instructions, Index Register Instructions, and Miscellaneous Interpretive Instructions (table 15-13).


15-94. Dual Quantity Instructions operate with two quantities, one contained in the MPAC (multiprecision accumulator) or the VAC (vector accumulator) and other stored at locations K, K + 1, etc. For some instructions the quantity N is written into a program instead of an address K. Address K defines the first location of a double-precision quantity, a triple-precision quantity, or a vector expression. A double-precision quantity is stored at K and K + 1 (28 value bits and two sign bits), a triple-precision quantity is located at K, K + 1, and K + 2 (42 value bits and three sign bits), and a vector is stored at K
(text continued on page 15-61)

15-54

CONFIDENTIAL

Table 15-13

INTERPRETIVE INSTRUCTIONS

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Direct Address	Indexed Address	Min	Ave	Max
Dual Quantity Instructions - DP and TP Operations 						
DAD K	DP Add	034	036	91	123	174
TAD K	TP Add	074	076	112	144	195
DSU K	DP Subtract	044	046	99	131	182
TSU K	TP Subtract	114	116	121	153	204
BDSU K	DP Subtract Backwards	050	052	105	137	188
DMP K	DP Multiply	054	056	171	203	254
DMPR K	DP Multiply and Round	110	112	181	217	274
DDV K	DP Divide	064	066	283	315	777
BDDV K	Backwards DP Divide	070	072	301	333	795
TSRT N	TP Shift Right	104	106	143+21m	162+21m	201+21m
TSLT N	TP Shift Left	060	062	78+25n	97+28n	136+31n
TSLC K	TP Shift Left and Count	100	102	77+0n	105+37n	152+40n
SIGN K	Set Sign into MPAC	120	122	82	101	139
BPL K	Branch on Plus	160	162	111	116	146
BZE K	Branch on Zero	140	142	111	116	146
BMN K	Branch on Minus	020	022	111	116	146
BHIZ K	Branch on High Order Quantity Zero	040	042	106	106	132

CONFIDENTIAL

15-55

CONFIDENTIAL

FR-2-115

TABLE 15-13
INTERPRETIVE INSTRUCTIONS (continued)

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Direct Address	Indexed Address	Min	Ave	Max
Dual Quantity Instructions - Vector Operations △₁						
VAD K	Vector Add	134	136	170	202	253
VSU K	Vector Subtract	014	016	181	211	264
BVSU K	Vector Subtract Backwards	144	146	281	311	364
VXSC K	Vector Times Scalar	010	012	330	430	510
DOT K	Vector Dot Product	164	166	477	521	580
VPROJ K	Vector Project	174	176	727	741	870
VXV K	Vector Cross Product	170	172	830	874	937
MXV K	Matrix Times Vector	124	126	1597	1629	1680
VXM K	Vector Times Matrix	130	132	1595	1627	1678
VSRT N	Vector Shift Right	150	152	330	350	382
VSLT N	Vector Shift Left	154	156	85+100n	100+102n	120+105n
Dual Quantity Instructions - Sundry						
ITC K	Interpretive Transfer Control	004	006	103	106	131
STZ K	Store Zero	024	026	65	86	112
BOV K	Branch on Overflow	030	032	106	107	134

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TABLE 15-13
INTERPRETIVE INSTRUCTIONS (continued)

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Direct Address	Indexed Address	Min	Ave	Max
Single Quantity Instructions - DP and TP Operations △ 2						
SIN	DP Sin Function	103	107	808	876	916
COS	DP Cos Function	113	117	859	937	1007
ASIN	DP Arcsin Function	063	067	1357	1436	1856
ACOS	DP Arccos Function	073	077	1336	1419	1839
DSQ	DP Square	133	137	136	156	168
SQRT	DP Square Root	123	127	336	363	814
ABS	Absolute Value	053	057	48	76	96
DMOVE	DP Move	153	157	60 + Loading		
TMOVE or TP	TP Move or Declare TP	003	007	64 + Loading or 64		
VSQ	Vector Square	043	047	465	510	575
ABVAL	Vector Absolute Value	033	037	892	937	1299
UNIT	Normalize Vector to Unit Vector	023	027	1886	1944	2890
V MOVE	Vector Move	013	017	60 + Loading		
VDEF	Vector Define	173	177	116	128	138

TABLE 15-13
INTERPRETIVE INSTRUCTIONS (continued)

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Direct Address	Indexed Address	Min	Ave	Max
Single Quantity Instructions - Sundry △₂						
COMP	Complement	143	147	41	100	162
SMOVE	SP (Single Precision) Move	163	167	64 + Loading		
Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Index Reg 1 (T=1)	Index Reg 2 (T=2)	Min	Ave	Max
Index Register Instructions						
AXT T, N	Address to Index True (load index register with given number)	011	015	73	92	103
AXC T, N	Address to Index Complement (load index register with complement number)	111	115	74	93	104
INCR T, N	Increment Index Register	061	065	78	98	109
LXA T, K	Load Index Register Direct from Address	021	025	78	97	108
LSC T, K	Load Index Register Complemented from Address	031	035	76	95	106

15-58

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-13
INTERPRETIVE INSTRUCTIONS (continued)

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Index Reg 1 (T=1)	Index Reg 2 (T=2)	Min	Ave	Max
Index Register Instructions (continued)						
SXA T, K	Store Indexed Quantity in Address	041	045	77	96	117
XCHX T, K	Index Register Exchange	051	055	79	98	109
XAD T, K	Add to Index Register	071	075	83	102	113
XSU T, K	Subtract from Index Register	101	105	81	100	111
AST T, N	Address to Step True	121	125	73	92	108
TIX T, K	Transfer on Index	131	135	86	105	116
Miscellaneous Interpretive Instructions						
EXIT	Leave Interpretive Mode	001		63	81	91
RTB K	Return to Basic Mode	005		75	95	105
NOLOD	No Load	141		53	71	81
LODON	Load Indicator ON	171		53	71	81
ROUND	Round to DP	145		51	72	89
ITCQ	Interpretive Transfer Control to Address Stored in QPRET	175		80	95	110
ITA K	Interpretive Transfer of Address	151		70	88	108

Changed 29 May 1964



CONFIDENTIAL

15-59

CONFIDENTIAL

FR-2-115

TABLE 15-13
INTERPRETIVE INSTRUCTIONS (continued)

Initials	Name and Purpose	Order Code		Execution Time (MCTs)		
		Index Reg 1 (T=1)	Index Reg 2 (T=2)	Min	Ave	Max
Miscellaneous Instructions (continued)						
ITCI K	Interpretive Transfer Control Indirect	155		69	77	97
SWITCH N	Turn Switch on	161		125	140	155
SWITCH N, K	Branch on Switch on	161		125	140	155
NOTES:  m means the number of 14 bit shifts n means the number of single bit shifts  Load and store times in MCTs are as follows:						
Function		SP	DP	TP	Vector	
Loading		68	68	74	150	
Storing in Storage			96	102	166	
Storing in Push-Down List			53	59	123	

through $K + 5$ (28 value bits and two sign bits for each of the three vector components). The highest order part of a quantity is always located at the first address, i. e., K . Thirty-one different Dual Quantity Instructions are provided, but each can refer to a direct address K or an indexed address K , therefore, sixty-two different order codes apply. An indexed address K is derived by modifying a given address with the content of one of the two Index Registers.

15-95. Single Quantity Instructions operate only with a quantity normally contained in the MPAC or VAC. These instructions can enter a quantity into an accumulator before the execution of the instruction, for this reason different order codes are provided for direct and indexed addressing. Sixteen different Single Quantity Instructions and thirty-two different order codes are listed in table 15-13.

15-96. Index Register Instructions operate with the content of one of the two index registers provided. The letter T after the initials of an instruction indicates the number of the index register to be used. Eleven different Index Register Instructions and twenty-two different order codes to indicate which index register is used are listed in table 15-13.

15-97. Finally, Twelve Miscellaneous Interpretive Instructions with ten different order codes are listed at the end of table 15-13

15-98. AGC PROGRAMS

15-99. Many programs have been created for the AGC during the last two years. Most of them were used to develop and test various techniques and are only of interest to MIT/IL members designing programs. The programs which are of interest to others are those which have been or will be wired into core ropes.

15-100. So far, the following five AGC programs have been selected for wiring into core ropes:

Eclipse	NASA Drawing No. 1003203
Artemis	NASA Drawing No. 1021100
Moonglow	NASA Drawing No. 1021101
SUNRSE33	NASA Drawing No. 1021102
SUNRSE38	NASA Drawing No. 1021102

Program Eclipse has been developed for the "breadboard" AGC and is used with system AGE4. Program Artemis has been developed for testing AGC subsystems at the factory. Program Moonglow is similar to program Eclipse, except that the program has been rearranged and existing program sections have been improved. Program Moonglow will be used with systems AGE4. The Sunrise programs represent the first family of Block I mission programs. Program SUNRSE33 (revision 33 of program Sunrise) is the first Sunrise program which has been wired into core ropes (three sets), and program SUNRSE38 is the final version of program Sunrise which will be wired into several core rope sets. Programs SUNRSE33 and SUNRSE38, which are identical except for core rope module B21, will be used to test the first AGE systems.

15-101. An AGC program is defined as the entire content of F memory (paragraph 15-5). An AGC program can be broken down in two ways: physically and functionally. Physically, an AGC program consists of various program sections. A program section may consist of several major routines which are composed of minor routines and subroutines. A subroutine is a sequence of instructions which starts at a location with a symbol (name) and ends at the next location with a symbol.

CONFIDENTIAL

FR-2-115

15-102. An AGC program can execute or perform various functions; these functions are categorized into the following three classes:

- Mission Functions
- Auxiliary Functions
- Utility Functions

15-103. Mission Functions such as prelaunch alignment, system test, free-fall integration, navigation, etc. are operations directly concerned with an Apollo Mission. A Mission Function may consist of several Function Phases (not to be confused with Major Mission Phases as defined in paragraphs 1-11 through 1-19). A Function Phase may require the execution of several Jobs, Tasks, and other routines. A Job is a routine which has been assigned a certain priority of execution (paragraph 12-4). A Task is a routine which must be executed at a certain time (paragraph 12-7). The various Jobs, Tasks, and other routines, which have to be executed as a certain Mission Function is performed, may be embedded in various Mission Program Sections (program sections mainly concerned with Mission Functions) as well as Auxiliary Program Sections and Utility Program Sections (program sections mainly concerned with Auxiliary and Utility Functions).

15-104. Auxiliary Functions such as start computer, accept information, display information, control optics, etc. are operations executed automatically at the occurrence of certain events, requests, or commands. Auxiliary Functions may require the execution of Jobs, Tasks, or other routines. The various Jobs, Tasks, and other routines, which have to be executed as a certain Auxiliary Function is performed, may be embedded in various Auxiliary Program Sections as well as in various Utility Program Sections.

15-105. Utility Functions are operations which are not directly concerned with Mission Functions or Auxiliary Functions but support them. The Utility Functions are embedded in the Utility Program Sections. The execution of Jobs is controlled by the Job Control, (Executive, paragraph 12-9). The execution of Tasks is controlled by the Task Control (Waitlist, paragraph 12-69). The execution of most Mission Functions is controlled by the Master Control (paragraph 16-). The Interpreter executes program portions written in interpretive language (paragraphs 15-92 and 6-4). Some basic routines, which are used in the execution of interpretive program portions, are situated in program section RTB Routines. Most routines needed when switching between memory banks are situated in program section Interbank Communication. The routines needed to transfer program control at the occurrence of certain interrupt signals (paragraph 15-48) are situated in program section RPT and GO Transfer Routines.

15-106. SUNRISE PROGRAMS

15-107. Programs SUNRSE33 and SUNRSE38 consist of 20 program sections which are listed in tables 15-14A and 15-14C in the same sequence as they appear in the program listings. Mission Program Sections are marked M, Auxiliary Program Sections A, and Utility Program Sections U. Tables 15-14B and 15-14D are memory maps using the program section numbers of tables 15-14A and 15-14C. For E register assignments of programs SUNRSE33 and SUNRSE38, see table 15-15.

15-108. The Sunrise programs have the following Mission Functions built in:

System Tests
Prelaunch Alignment
Free-Fall Integration

The execution of the System Tests is not under the control of the Master Control, only the execution of the Prelaunch Alignment and of Free-fall Integration. Later Block I AGC programs will have additional Mission Functions built in. Provisions have already been made in program SUNRSE33 to execute up to 12 Mission Functions concurrently under the control of the Master Control.

15-109. The Sunrise programs have the three following built in system tests; each is executed individually on request via a DSKY:

AGC Selfcheck
IMU Alignment Test
PIPA Scale Factor Determination

All system tests are contained in program section AGC Selfcheck and System Tests. Later AGC programs will have additional systems tests built in.

15-110. Mission Function Prelaunch Alignment first vertically erects the IMU, which takes about 5 minutes, and then gyro compasses the IMU to a desired azimuth. The gyros compass loop has a time constant of about 17 minutes. The alignment takes the motions of the spacecraft on the launch pad into account. Expected accuracies in the launch pad are 0.2 milliradians in the vertical alignment and 5 in the azimuth alignment. Program sections Prelaunch Alignment and IMU Alignment Routines are involved in the alignment operations.

15-111. Mission Function Free-Fall Integration, as applied in the Sunrise programs, is used for orbital integration only. The free-fall

TABLE 15-14A

PROGRAM SUNRSE33 -- PROGRAM SECTIONS

Program Section			Memory Locations Used	
Number	Name	Class	FF	FS
1	RPT And GO Transfer Routines	U	2000 - 2036	
2	Interpreter	U	4000 - 5652	
			2130	03,6000 - 03,7435
3	Job Control (Executive)	U	2037 - 2123	04,6000 - 04,6351
4	Task Control (Waitlister)	U	2124 - 2127	
			2131 - 2216	04,6352 - 04,6501
5	Master Control (Progress Control)	U	2217 - 2300	04,6502 - 04,6743
6	Fresh Start And Restart	A		04,6744 - 04,7264
7	DOWNRUPT Processor	A	2301 - 2426	
8	T4RUPT Output Control	A	2427 - 2466	10,6000 - 10,7053
9	Modeswitching And Mark	A	2467 - 2515	05,6000 - 05,6675
				05,7740 - 05,7777
				10,7054 - 10,7644
				05,6676 - 05,7344
10	AGC Selfcheck	A		
11	Interbank Communication	U	2516 - 2604	
12	Alarm Processor	A	2605 - 2667	
13	Initialization And Test	M		22,6000 - 22,6304
14	Orbital Integration Initialization	M		22,6305 - 22,7743
				23,6000 - 23,6107
15	Prelaunch Alignment	M		23,6110 - 23,7020
16	RTB Routines	U		23,7021 - 23,7165
17	System Test	M		30,6000 - 30,7356
18	IMU Alignment Routines	A		25,6000 - 25,6624
19	KEYRUPT And UPRUPT Processor	A		04,7265 - 04,7375
20	Keyboard And Display (Pinball)	A	2670 - 3117	21,6000 - 21,7621
				24,6000 - 24,7630

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TABLE 15-14B. PROGRAM SUNRSE33 - MEMORY MAP

ROPE MODULE	B28				B29				B21				B22			
BANK	04	01	24	21	02	03	22	23	10	05	30	25	06	07	26	27
	6000	2000	6000	6000	4000	6000	6000	6000	6000	6000	6000	6000				
		△1														
		△2														
		△3														
		△4														
		△5						△14		△9	△17	△18				
		△7						△15		△10						
		△8						△16								
	△3	△9														
	△4	△11														
	△5	△12			△2		△12		△8							
	△6	△20	△20	△20		△2	△14		△9			6624				
	△19	3117														
								7165								
	7375				5652					7344	7356					
			7630	7621		7435	7743		7644							
										7740						
										△9						
										7777						

REAL
ADDRESSES
OF FIRST
AND LAST
LOCATIONS
USED

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CONFIDENTIAL

15-67

CONFIDENTIAL

FR-2-115

TABLE 15-14C

PROGRAM SUNRSE38 -- PROGRAM SECTIONS

Program Section			Memory Locations Used	
Number	Name	Class	FF	FS
1	RPT and GO Transfer Routines	U	2000 - 2036	
2	Interpreter	U	4000 - 5652	
			2130	03,6000 - 03,7435
3	Job Control (Executive)	U	2037 - 2123	04,6000 - 04,6351
4	Task Control (Waitlister)	U	2124 - 2127	
			2131 - 2216	04,6352 - 04,6501
5	Master Control (Progress Control)	U	2217 - 2300	04,6502 - 04,6743
6	Fresh Start And Restart	A		04,6744 - 04,7264
7	DOWNRUPT Processor	A	2301 - 2426	
8	T4RUPT Output Control	A	2427 - 2466	10,6000 - 10,7053
9	Modeswitching And Mark	A	2467 - 2515	05,6000 - 05,6675
				05,7345 - 05,7416
				05,7740 - 05,7777
				10,7054 - 10,7732
				10,7740 - 10,7765
10	AGC Selfcheck	A		05,6676 - 05,7344
11	Interbank Communication	U	2516 - 2604	
12	Alarm Processor	A	2605 - 2667	05,7634 - 05,7642
13	Initialization And Test	M		22,6000 - 22,6304
14	Orbital Integration Initialization	M		22,6305 - 22,7743
				23,6000 - 23,6107
15	Prelaunch Alignment	M		23,6110 - 23,7020
16	RTB Routines	U		23,7021 - 23,7165
17	System Test	M		30,6000 - 30,7357
				30,7400 - 30,7402
18	IMU Alignment Routines	A		25,6000 - 25,6626
19	KEYRUPT And UPRUPT Processor	A		04,7265 - 04,7375
20	Keyboard And Display (Pinball)	A	2670 - 3117	21,6000 - 21,7621
				24,6000 - 24,7630

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CONFIDENTIAL

TABLE 15-14D. PROGRAM SUNRSE38 - MEMORY MAP

ROPE MODULE	B28				B29				B21				B22			
BANK	04	01	24	21	02	03	22	23	10	05	30	25	06	07	26	27
	6000	2000	6000	6000	4000	6000	6000	6000	6000	6000	6000	6000				
REAL ADDRESSES OF FIRST AND LAST LOCATIONS USED		△1														
		△2														
		△3														
		△4														
		△5														
		△7														
		△8														
	△3	△9						△14			△9	△17	△18			
	△4	△11						△15			△10					
	△5	△12			△2		△12				△9					
	△6	△20	△20	△20		△2	△14									
	△19	3117								△8						
								7165					6624			
											7416	7357				
											7634	7400				
										7732	△12	△17				
		7375				5652				7740	7642	7402				
										△9	7740					
			7630	7621		7435	7743		7765	△9						
										7777						

Changed 2 July 1964

CONFIDENTIAL

15-67B

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

FR-2-115

integration is based on Encke's method. Program sections Orbital Integration Initialization and Orbital Integration are involved in computing position and velocity for an earth orbit whose initial conditions may be specified via a DSKY.

15-112. The Auxiliary Functions which can be performed by a Sunrise program are listed below:

KEYRUPT (accept keyboard information)	}	Described in Issue 17,
UPRUPT (accept uplink information)		
MARK (store Optics information)		
Mark Accept (accept Optics information)		
Display accepted information		
Display data contained in specified locations		
Monitor data contained in specified locations		
Enter data into specified locations		
Request the execution of a Job or a Task		
Set Mission Function and Function Phase		
Restart the computer operation	}	Described in Issues 16 and 17,
Transfer next word to DSKY's		
Drive IMU CDU's	}	Described in Issue 18.
Drive Optics CDU's		
Check IMU mode		
Check Optics mode		
Scan IMU FAIL, PIPA FAIL, and CDU FAIL bit and display failure		
Check Downlink Rate		
Provide the next word for downlink transmission		

15-113. The Utility Functions of the Sunrise programs are the same as those described in paragraph 15-105.

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0

Octal Address	Initials △	Name and Purpose
The following registers are used by program sections Interpreter, Interbank Communication, and Pinball.		
0060	BANKSET	Holds complemented number of the bank in which the interpretive routine currently executed is stored.
0061	ADDR (ADDRWD)	Holds any 9-bit address referring to a Work Area; holds any 10-bit address referring to E memory; holds any 12-bit address for addressing F memory by means of register S; holds first Interpretive Address Word of a string in its true form temporarily; holds number N after decoding an Interpretive Address Word.
0062	ORDER	Holds Interpretive Instruction Word (in its true form) to be decoded; holds second order code of a decoded Interpretive Instruction Word; holds 00000 if no second order code exists or processing of it has been started.
	UPDATRET	Holds return address entered by subroutines UPDATNN and UPDATVB of Pinball.
	CHAR	Temporary storage used by subroutine CHARIN of Pinball.
	ERCNT	Error light reset counter, used by Pinball.
0063	DECOUNT	Scaling and display counter, used by Pinball.
	TEM11 SGNON	Temporary storage used by routines DOT2 and INCRT4 of Interpreter. Sign On indicator, used by Pinball.

CONFIDENTIAL

15-69

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0063	NOUNTEM	Counter for mixed noun fetch, used by Pinball.
	DISTEM	Counter for octal display verbs, used by Pinball.
	DECTEM	Counter for decimal display verbs, used by Pinball.
	DECTEM1	Temporary storage for numbers, used by Pinball.
0064	MODE	Holds 77776 when Interpreter is in DP mode; holds 77775 when Interpreter is in TP mode; holds 77777 when Interpreter is in Vector mode.
	ENTRET	Temporary storage used by subroutine ENTER of Pinball.
0065	LOADIND (NEWEQIND)	Holds 00001 if MPAC or VAC has to be reloaded by the Interpreter; holds 00000 if the present content of MPAC or VAC is to be operated with. Also used as temporary storage by Interpreter.
	MONTEM	Temporary storage used by subroutine MONITOR of Pinball.
0066	WORKLOC (FIXLOC)	Holds address of Work Area currently used by the Interpreter. One out of five addresses is entered by the Job Control.
0067	VACLOC	Holds address of VAC currently used by the Interpreter. VACLOC = WORKLOC + 32D. One out of five addresses is entered by the Job Control.
0070-0075	VBUF	Temporary storage (6 locations) for vector operations of Interpreter.
0070	TEMQS	Temporary storage used by subroutine SWCALL of Interbank Communication.

15-70

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0071	BANKTEM	Temporary storage used by subroutine SWCALL of Interbank Communication.
0072	TEMB (B) SIGNRET	Argument storage used by subroutine ARCCOS of Interpreter. Holds return address entered by subroutine ON of Pinball.
0072-0073	PROGREG MIXTEMP	Temporary storage for program codes, used by Pinball. Temporary storage for mixed noun data, used by Pinball.
0074	ESCAPE2 TAG1	Negative Argument Switch. Contains a TC K instruction during execution of Interpretive Instruction ARCCOS. Holds address of Work Area currently used by the Interpreter, plus zero or one dependent upon whether Index Register X1 or X2 is to be used, or plus two or three dependent upon whether Step Register S1 or S2 is to be used.
0075	AWORD (POLISH) TEMQ3 WDCNT INREL	Holds an Address Word in its true form; holds 10-bit E address of Store Code Address Word. Holds return addresses entered by subroutines DDV K and SQRTDIV. Character Counter, used by subroutine DSPWP of Pinball. Input buffer selector (X, Y, Z, display register) of Pinball.

CONFIDENTIAL

15-71

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0076-0100	BUF	Temporary storage (3 locations) for DP and TP operations of Interpreter. Registers BUF+1 and BUF+2 used as temporary storage by LOAD routine.
0100	SGNDMAX TEM3	Temporary storage used by subroutine TPAGREE of Interpreter. Temporary storage used by subroutine TPAGREE of Interpreter.
0101	TEM2 DSREL	Temporary storage used by subroutines TRAD, DAD1, STD2, DMP1, DDV, DOT2, INCRT2, STB, and CROSS of Interpreter. Temporary storage used by subroutine DAD1 of Interpreter.
0102	TEM4 TEMQ DSMG 1DADDTEM	Temporary storage used by routines DMP1, INCRT4, and CROSS1 of Interpreter. Holds return address entered by routine TPAGREE of Interpreter. Temporary storage used by subroutine DSPIN of Pinball. Mixed noun indirect address storage, used by Pinball.
0103	TEM5 TEMQ2 BASE COUNT	Temporary storage used by routines TRAD, DMP, DAD, and VACCOM of Interpreter. Holds return address entered by subroutine SQRT3 of Interpreter. Temporary storage used by subroutine CROSS1 of Interpreter. Temporary storage used by subroutine DSPIN of Pinball.

15-72

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0104	TEM6	Temporary storage used by subroutine CROSS1 of Interpreter.
	TEM8	Temporary storage used by subroutines ST02, DOT2, and ROUND of Interpreter.
0105	TEM9	Temporary storage used by subroutines POLY, MXV, and VXM of Interpreter.
	WRDRET	Holds return address entered by subroutine 5 BLANK of Pinball.
	WDRET	Holds return address entered by subroutine DSPWP of Pinball.
	DECRET	Holds return address entered by subroutine PUTCOM of Pinball.
0106	21/22REG	Temporary storage used by routine CHARIN of Pinball.
	TEM10	Temporary storage used by subroutine POLY, MXV, and VXM of Interpreter.
	IND	Temporary storage used by subroutine CROSS1 of Interpreter.
0107	MIXBR	Indicator for mixed and normal noun, used by Pinball.
	DVSW	Divide Switch, holds 0000 for normal divide or any other quantity for backward divide of Interpreter.
	SGNOFF	Temporary storage used by subroutine ON of Pinball.
	NVTEMP	Temporary storage used by subroutine NVSUB of Pinball.
	SFTEMP1	Holds high order part of SF constant for Pinball.

CONFIDENTIAL

15-73

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials ⚠	Name and Purpose
0107	DECTEM2	Temporary storage for numeric used by Pinball.
0110	BRANCHQ CODE SFTEMP2	Holds the return address for a branch operation of the Interpreter. Temporary storage used by routine DSPIN of Pinball. Holds low order part of SF constant for Pinball.
0111	COMPON DSEXIT EXITEM BLANKRET	Component counter for UNIT operation of Interpreter. Holds return address entered by subroutine DSPIN of Pinball. Holds return address entered by scale factor select routine of Pinball. Holds return address entered by subroutine 2BLANK of Pinball.
0112	ARETURN LSTPTR RELRET FREERET	Holds return address during the execution of Interpretive Instructions ASIN and ACOS. List pointer for routine GRABUSY of Pinball. Holds return address entered by subroutine RELDSP of Pinball. Holds return address entered by subroutine FREEDSP of Pinball.
0113	ESCAPE CADRTEM	Return Address Switch contains a TC instruction during the execution of Interpretive Instructions ASIN and ACOS. Temporary storage used by GRAB subroutines of Pinball.

15-74

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
The following registers are used by program sections Interpreter and Job Control.		
0114-0123	Job Area 1	Defined by the following 8 locations.
0114-0116	MPAC	Multiprecision Accumulator (MPAC, 3 locations).
0117	IWLOC (LOC)	Holds 12-bit address of Interpretive Instruction Word to be decoded.
0120	AWLOC (ADRLOC)	Holds 12-bit address of last TC INTPRET; holds address of last Interpretive Instruction Word in string currently executed; holds address of any Interpretive Address Word in current string.
0121	OVFIND	Overflow Indicator. Normally holds 00000; holds 00001 or 77776 in case of overflow or underflow.
0122	PUSHLOC	Holds address of next available Pushlist location in bit positions 10 through 1. (Register PUSHLOC of other Job Areas also holds the bank code of the Job occupying that Job Area in bit positions 15 through 11).
0123	PRIORITY	Holds 77777 when this Job Area is available. When this Job Area is in use, the register holds a ZERO in bit position 15 and the priority code of the Job using this Job Area in bit positions 14 through 10. (Register PRIORITY of other Job Areas also holds the address of the assigned Work Area in bit positions 9 through 1) The register may contain this information in noncomplemented form (all Job Areas) or complemented form (Job Areas 2 through 8 only), dependent whether the Job is in the active or dormant state.

Changed 29 May 1964

CONFIDENTIAL

15-75

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0124-0133	Job Area 2	Similar to Job Area 1.
0134-0143	Job Area 3	Similar to Job Area 1.
0144-0153	Job Area 4	Similar to Job Area 1.
0154-0163	Job Area 5	Similar to Job Area 1.
0164-0173	Job Area 6	Similar to Job Area 1.
0174-0203	Job Area 7	Similar to Job Area 1.
0204-0213	Job Area 8	Similar to Job Area 1.
0214	VAC1USE	Holds 00000 when Work Area 1 is in use; holds 00214 when Work Area 1 is available.
0215-0267	Work Area 1	Defined by the following 53 locations.
0215-0254	PUSHLIST	Modified pushlist (32 locations), Work Area addresses 0000 through 0037.
0255-0262	VAC	Vector Accumulator (VAC, 6 locations), Work Area address 0040.
0263-0264	X1, X2	Index Registers 1 and 2, Work Area addresses 0046 and 0047.
0265-0266	S1, S2	Step Registers 1 and 2, Work Area addresses 0050 and 0051.

(continued next page)

15-76

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials ①	Name and Purpose
0267	QPRET	Holds return address, Work Area address 0052.
0270	VAC2USE	Holds 00000 when Work Area 2 is in use; holds 00270 when Work Area 2 is available.
0271-0343	Work Area 2	Similar to Work Area 1.
0344	VAC3USE	Holds 00000 if Work Area 3 is in use; holds 00344 if Work Area 3 is available.
0245-0417	Work Area 3	Similar to Work Area 1.
0420	VAC4USE	Holds 00000 if Work Area 4 is in use; holds 00420 if Work Area 4 is available.
0421-0473	Work Area 4	Similar to Work Area 1.
0474	VAC5USE	Holds 00000 if Work Area 5 is in use; holds 00474 if Work Area 5 is available.
0475-0547	Work Area 5	Similar to Work Area 1.
0550	NEWJOB	A multiple of eight is entered by the Job Control to indicate that the execution of a Job of higher priority has been requested. The tag specifies in which Job Area the active Job of highest priority is located.

CONFIDENTIAL

15-77

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
The following registers are used by program section Task Control only.		
0551-0555	LST1 through LST1+4	Timelist (5 locations), holds times at which executions of Tasks have to be initiated.
0556-0563	LST2 through LST2+5	Addresslist (6 locations), holds addresses of Task to be executed.
The following registers are used by program sections Job Control, Task Control, Function Control, and interrupted or interrupting routines.		
0564	RUPTAGN	Contains 77777 if program control is to return to the interrupted Job upon the completion of a Task; contains 00001 if the next Task is to be executed immediately.
	KEYTEM2	Temporary storage used by KEYRUPT and UPRUPT.
0565	EXECTEM1	Holds back number of the requesting routine, used by Job Control.
	RUPTSTOR	Temporary storage used by Job Control.
	PHASE	Temporary storage used by Function Control.
0566	EXECTEM2	Holds the complete starting or reactivating address of the Job to be executed; used by Job Control.
	PROG	Temporary storage used by Function Control.

15-78

CONFIDENTIAL

FR-2-115

CONFIDENTIAL

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0567	EXECTEM3	Holds the address of a Pushlist register, used by Job Control.
	PHASEDIG	Temporary storage used by Function Control.
	ITEMP3	Temporary storage used by T4RUPT.
	SRRUPT	Temporary storage used by T4RUPT.
0570	EXECTEM4	Temporary storage used by Function Control.
	PHASELP	Temporary storage used by Function Control.
0571	EXECTEM5	Temporary storage used by Function Control.
0572	NEWPRIO	Holds the priority of the active Job of highest priority in bit positions 14 through 10, and the address of a Work Area in bit positions 9 through 1, used by Job Control.
	PHASEWD	Temporary storage used by Function Control.
	NVAL	Holds Δt_R of the requested Task.
	DELT	Holds the tag specifying into which place of the Waitinglist the requested Task is to be entered, used by routine WAITLIST.
0573	ITEMP1	Temporary storage used by routine T3RUPT.
	WTEXTIT	Holds the address used for computing the return address of the requesting routine, used by Load and WAITLIST routine.
	ITEMP2	Temporary storage used by Function Control.

CONFIDENTIAL

15-79

CONFIDENTIAL

FR-2-115

TABLE 15-15

E REGISTER ASSIGNMENT II FOR SUNRSE33 REV. 0 (cont)

Octal Address	Initials △	Name and Purpose
0573	KEYTEMP1 DSRUPTM	Temporary storage used by KEYRUPT and UPRUPT. Temporary storage used by subroutine DSPOUT of T4RUPT.
0574	LOCCTR PHASDATA	Holds the tag specifying the Job Area used by the Job recently requested or reactivated, used by Job Control. Also used as temporary storage by Pinball. Temporary storage used by Function Control.
0575	BANKRUPT	Holds bank code of interrupted program section entered by interrupting program section.
0576-0602 and 0612-1601		Used by various program sections, will be defined later.

△ Symbols in () are used in MIT/IL listings.