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APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 30

BLOCK II APOLLO GUIDANCE

COMPUTER SUBSYSTEM

FR-2-130

RAYTHEON

RAYTHEON COMPANY

SPACE AND INFORMATION SYSTEMS DIVISION

APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 30

BLOCK II APOLLO GUIDANCE

COMPUTER SUBSYSTEM

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30-1. INTRODUCTION

30-2. This is the thirtieth issue of the AGCIS published to inform the technical staff at MIT/IL and Raytheon about the Apollo guidance computer (AGC) subsystems. The various types of computer subsystems are listed in paragraph 1-5 of Issue 1. This issue is an over-all description of the Block II AGC subsystems used in the Command Modules (CM's) and the Lunar Excursion Modules (LEM's). Other issues will describe in more detail the various sections and programs of the Block II AGC subsystems.

30-3. A Block II AGC subsystem used in a CM consists of one Apollo guidance computer (AGC) and two identical Display and Keyboards (DSKY's). One DSKY is mounted in the Navigation Panel of the CM, the other in the Main Panel. A Block II AGC subsystem used in a LEM consists of one AGC and only one DSKY. The CM and LEM Computers are identical except for the programs wired in and some input and output signals. An AGC, including its own power supply, occupies a volume of about 1 cu ft. and weighs approximately 60 lbs. Each DSKY occupies about 1/5 cu ft. and weighs approximately 17 lbs.

30-4. An AGC subsystem is a control computer (real time computer) with many features of a general purpose computer. The AGC's are parallel digital computers which operate with 16-bit words and single address instructions. The clock rate of an AGC is 1.024 Mc (oscillator frequency of 2.048 Mc and word transfer time of approximately 1 μ sec). They employ a ONE's complement number system with overflow bit and fixed binary point. Each Block II AGC contains an Erasable Memory (ferrite core array) capable of storing 2048 words of 16-bits each, and a Fixed Memory (Mo-perm core ropes) capable of storing 36,864 words of 16-bits each. The words stored in the two memories include one parity bit for error detection. All Block II logic is built from only one type of solid state integrated NOR gates contained in flat packages.

30-5. Input signals to the AGC subsystem can be parallel binary information (DC signals), incremental data (pulses counted), or serial binary data. Output signals can also be parallel binary information (DC signals or pulse trains), controlled pulse bursts (computed number of drive pulses), or timing pulses (continuous pulse trains).

30-6. Provision is made to have the AGC's operating either in the standby or the normal mode of operation to save power. When an AGC is in the standby mode, only the Timer is operating to monitor time information. When in the normal mode of operation, the whole subsystem operates.

30-7. Most modern computers, large business machines in particular, are designed such that various programs can be inserted and executed. The AGC differs from these computers since programs are wired in and can be changed only by replacing the Fixed Memory (either completely or in part) into which the program is wired. Therefore, an AGC program should be defined as the entire content of the Fixed Memory. An AGC program consists of various program sections (sub-programs).

30-8. An AGC program section can be written in regular machine language, in interpretive language, or in both. The regular machine language can be expressed with 38 different Regular Instructions, including some double precision operations. More than 100 different Interpretive Instructions, including double precision, triple precision, vector double precision, and matrix operations, are provided for the interpretive language. Program portions written in regular language operate faster than portions written in interpretive language because interpretive portions require extra time to interpret instructions. Portions written in interpretive language require less space for program storage than portions written in basic language because of the subroutine character of Interpretive Instructions. Furthermore, the interpretive language considerably simplifies the programming of complicated mathematical operations. The interpretive language is used mainly in program sections dealing with astronomical computations. Many of the control operations that the computer must perform are written in regular language; the interpretive language is used to simplify multiprecision and vector operations. Thus, the AGC is a fast computer when operating in the regular machine language, and a powerful machine when operating in the interpretive mode.

30-9. THE BLOCK II AGC SUBSYSTEM

30-10. A Block II AGC subsystem used in a CM consists of one Apollo guidance computer (AGC) and two identical Display and Keyboards (DSKY's). A Block II AGC subsystem used in a LEM consists of one AGC and only one DSKY. The AGC, which occupies a volume of about 1 cu ft., consists of one Tray A and one Tray B (figure 30-1). Tray A contains 24 logic modules, 5 interface modules, and 2 power supply modules (figure 30-2). A logic module may contain up to 120 flat packs and measures approximately $9 \frac{3}{4} \times 1 \frac{1}{2} \times \frac{5}{8}$ inches. All other modules also measure $9 \frac{3}{4} \times 1 \frac{1}{2}$ inches but vary in width in multiples of $\frac{1}{8}$ inch. Tray B contains the oscillator module, the alarm module, the erasable memory module, 6 core rope modules, and 8 modules which contain all the drivers and amplifiers for Erasable (E) and Fixed (F) Memory (figure 30-3). All modules, except the core rope modules, are plugged into receptacles mounted in the bottom of the trays. The core rope modules are plugged in from the front.

30-11. The two trays are joined such that the wirewrapped interconnections in the tray bottoms are on the outside (figure 30-1). Both trays are covered on the outside. The AGC is mounted with the logic tray side to a cold plate. The core rope modules can be interchanged without removing the cover of Tray B.

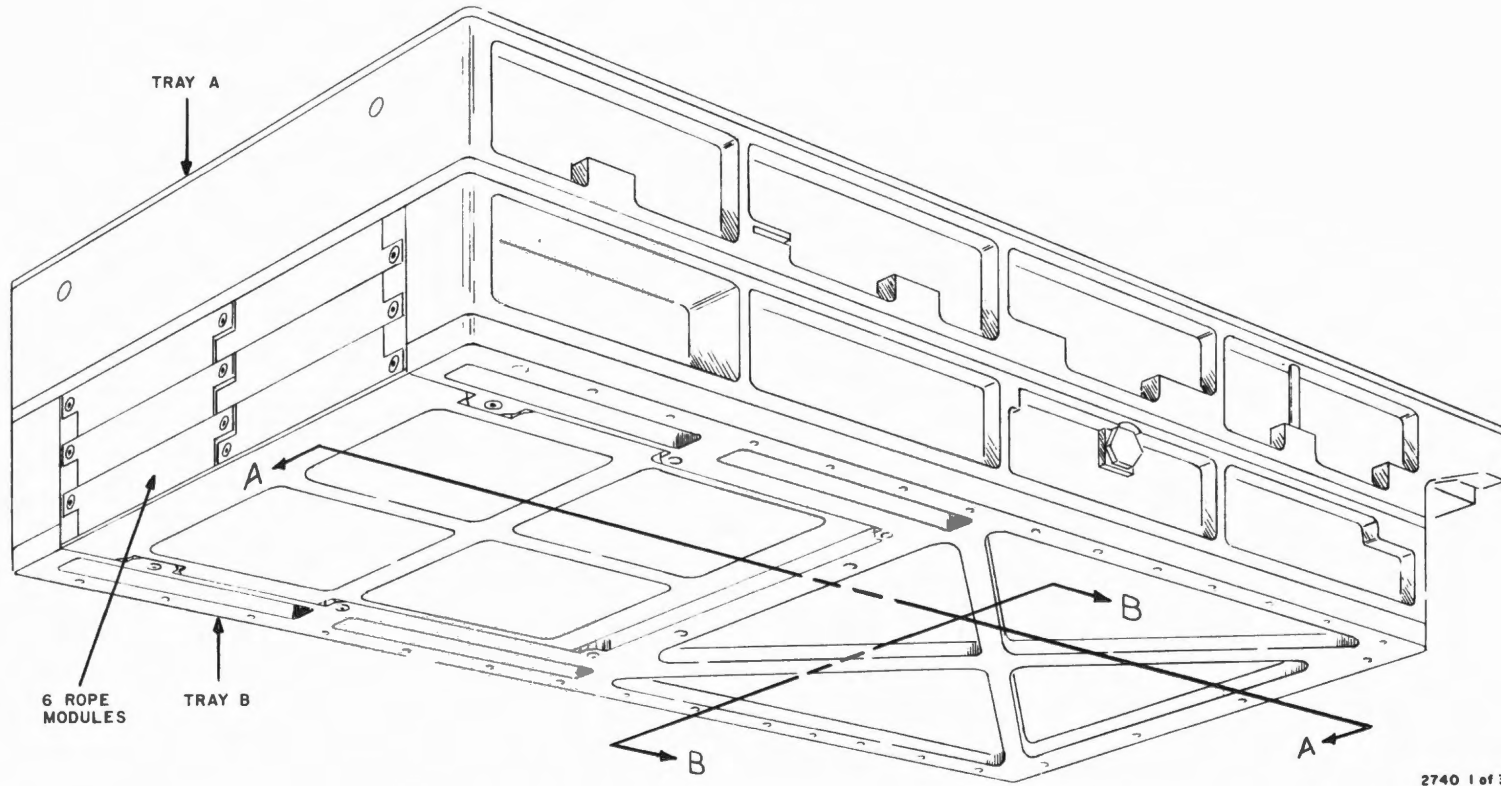
30-12. A 360 pin connector (A51) in figure 30-2 provides all the necessary connections between the AGC and the DSKY's, the G & N system, and the space craft (S/C), i. e., the CM or the LEM. A 144 pin connector (A52) is provided for connecting the AGC to the Computer Test Set (CTS), the Program Analyzer Console (PAC), or any other applicable test equipment.

30-13. A Block II DSKY consists of the main and front housing assembly with covers (figure 30-4). A 91 pin connector (J9) provides all the necessary connections to the AGC, the G & N system, and the CM or the LEM.

30-14. All signals fed into the AGC and the two DSKY's of a CM, and all the signals provided by these three units are described in Appendix A. All signals of the LEM AGC and DSKY are described in Appendix B.

30-15. All Block II logic is built from flat packages each of which contains two solid state silicon integrated NOR gates with three inputs (figure 30-5). If one or more inputs of a NOR gate are connected to a positive potential of approximately 1.5 volts, the output potential of the NOR gate is about 0.2 volt.

(text continued on page 30-12)



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Figure 30-1. Block II AGC (Sheet 1 of 3)

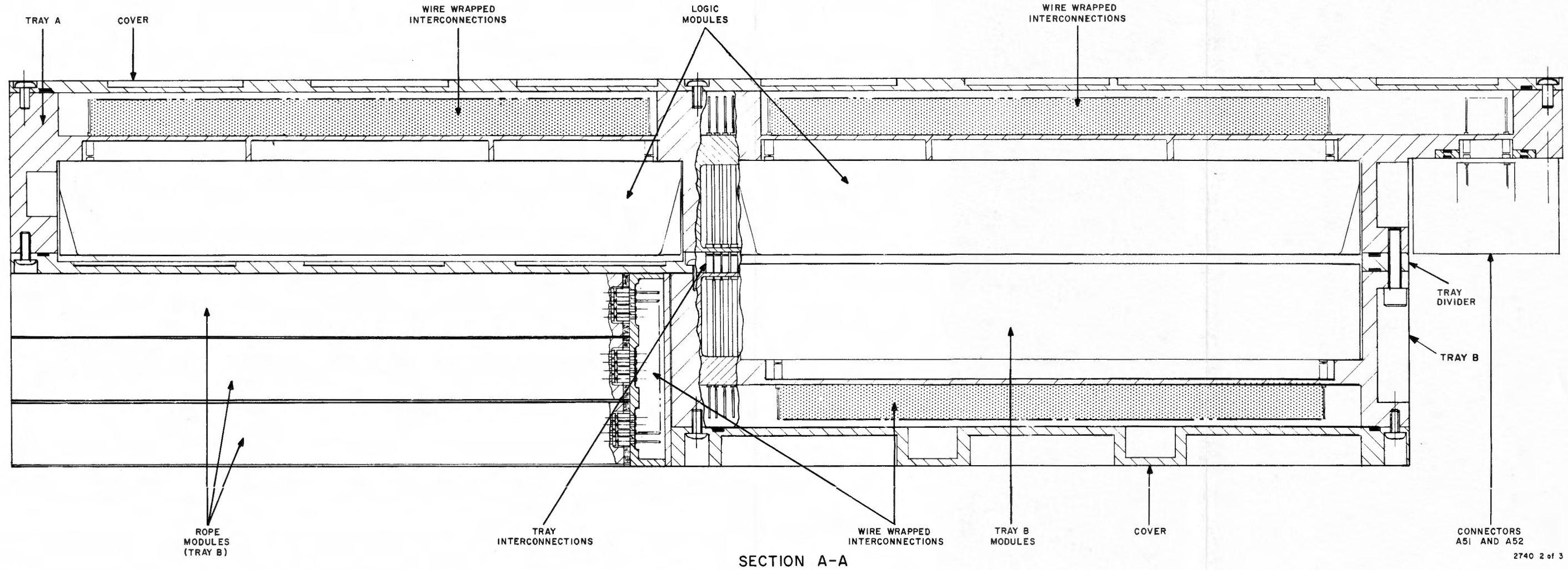


Figure 30-1. Block II AGC (Sheet 2 of 3)

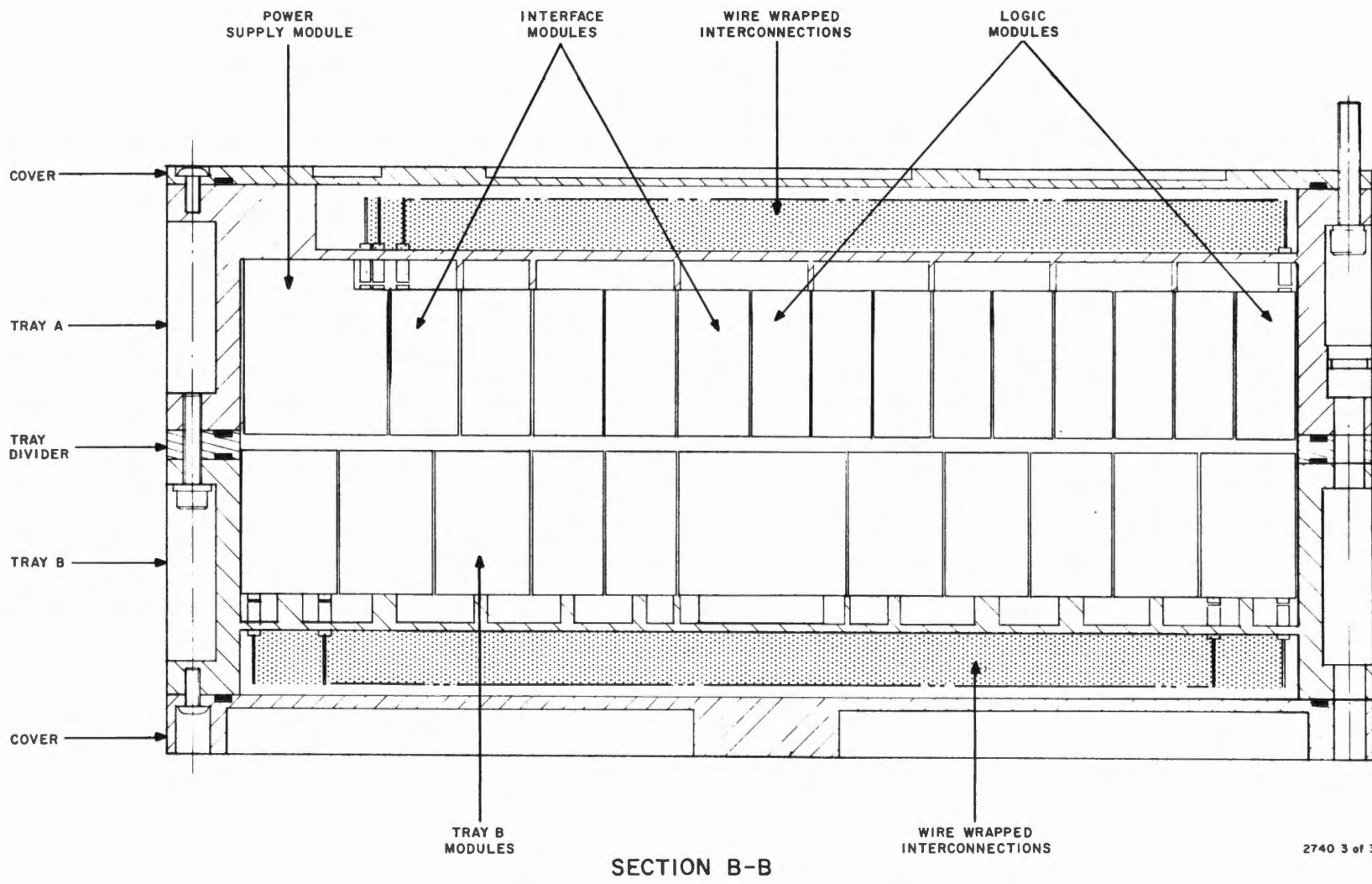
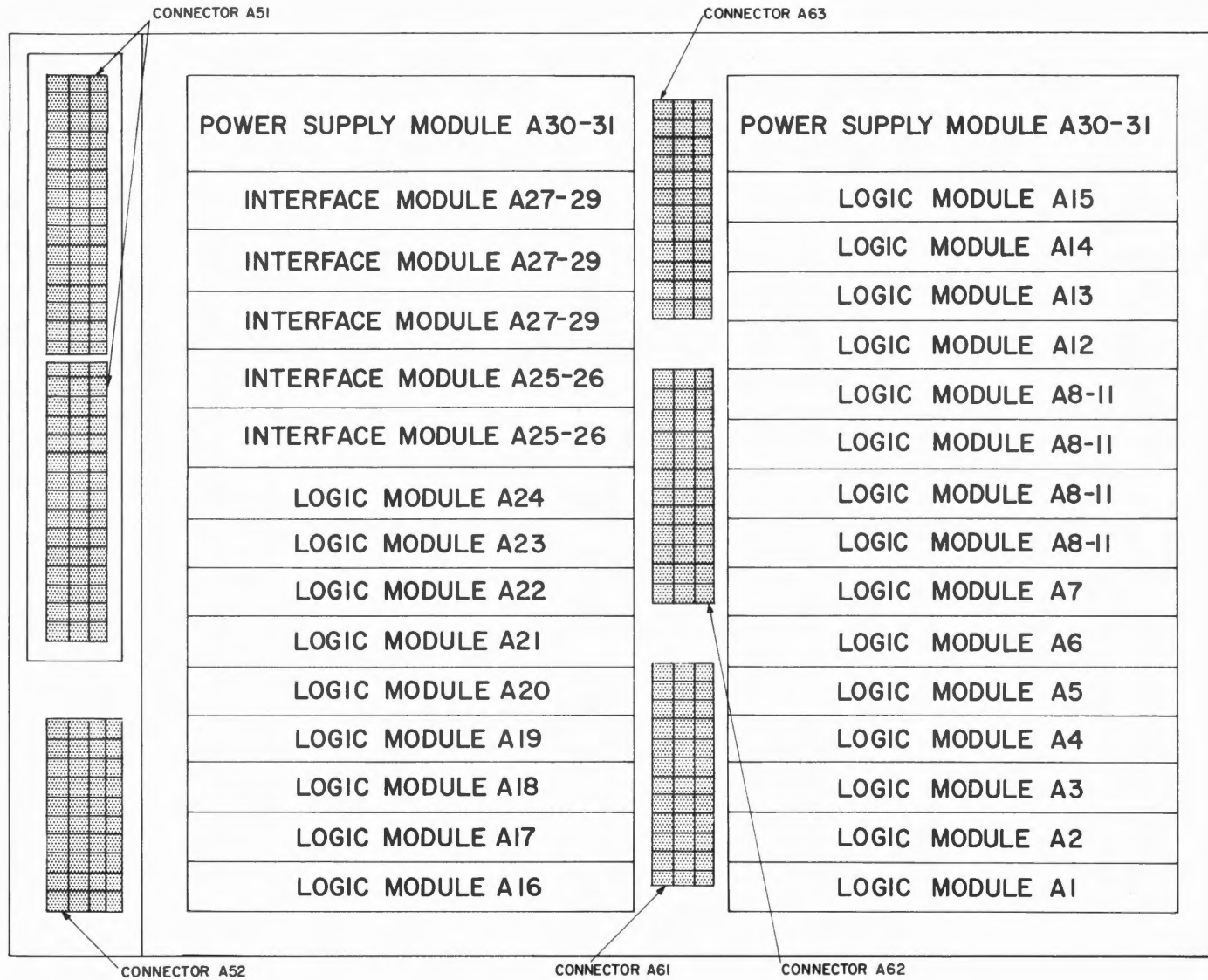


Figure 30-1. Block II AGC (Sheet 3 of 3)



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Figure 30-2. Tray A

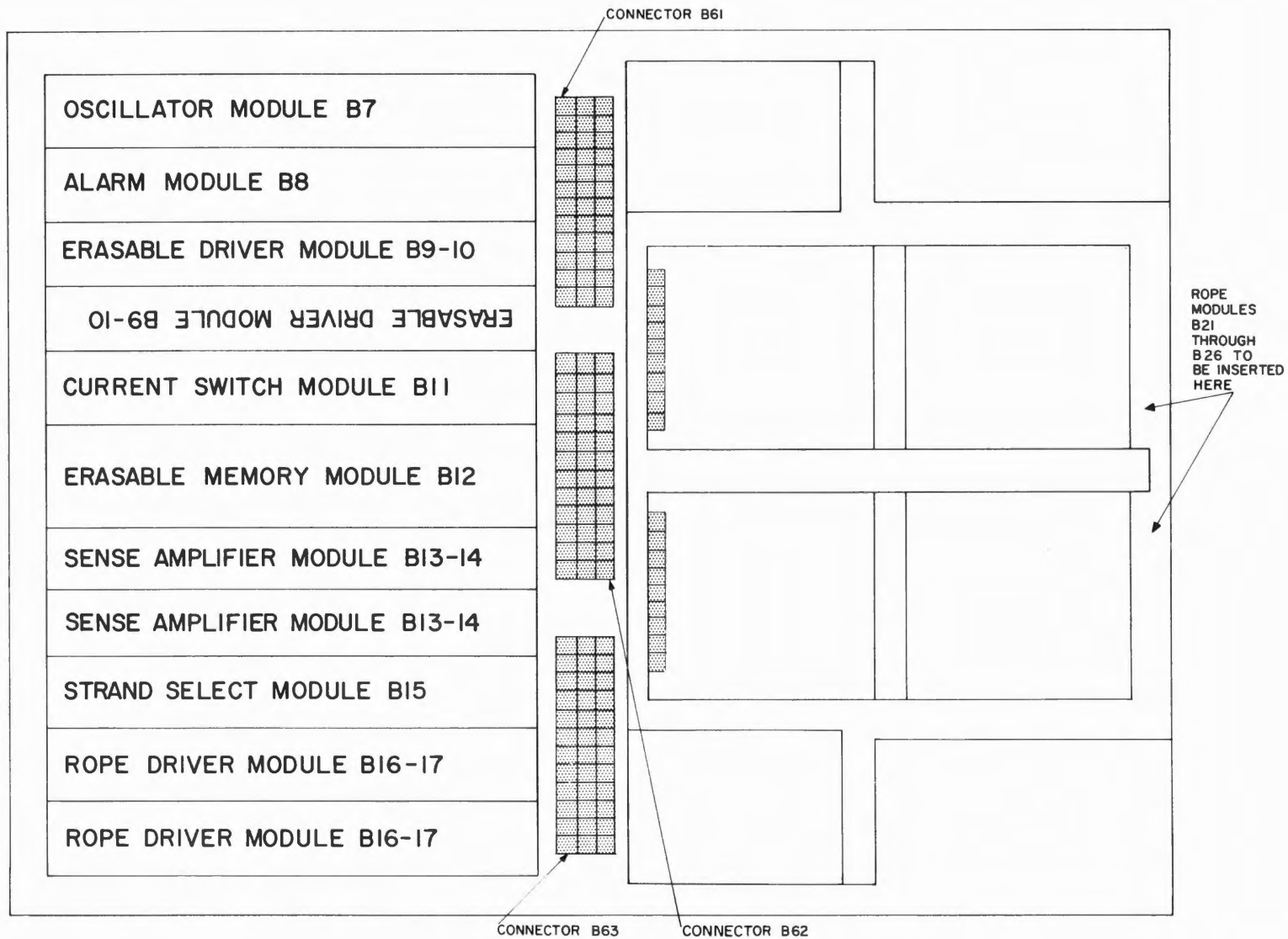


Figure 30-3. Tray B

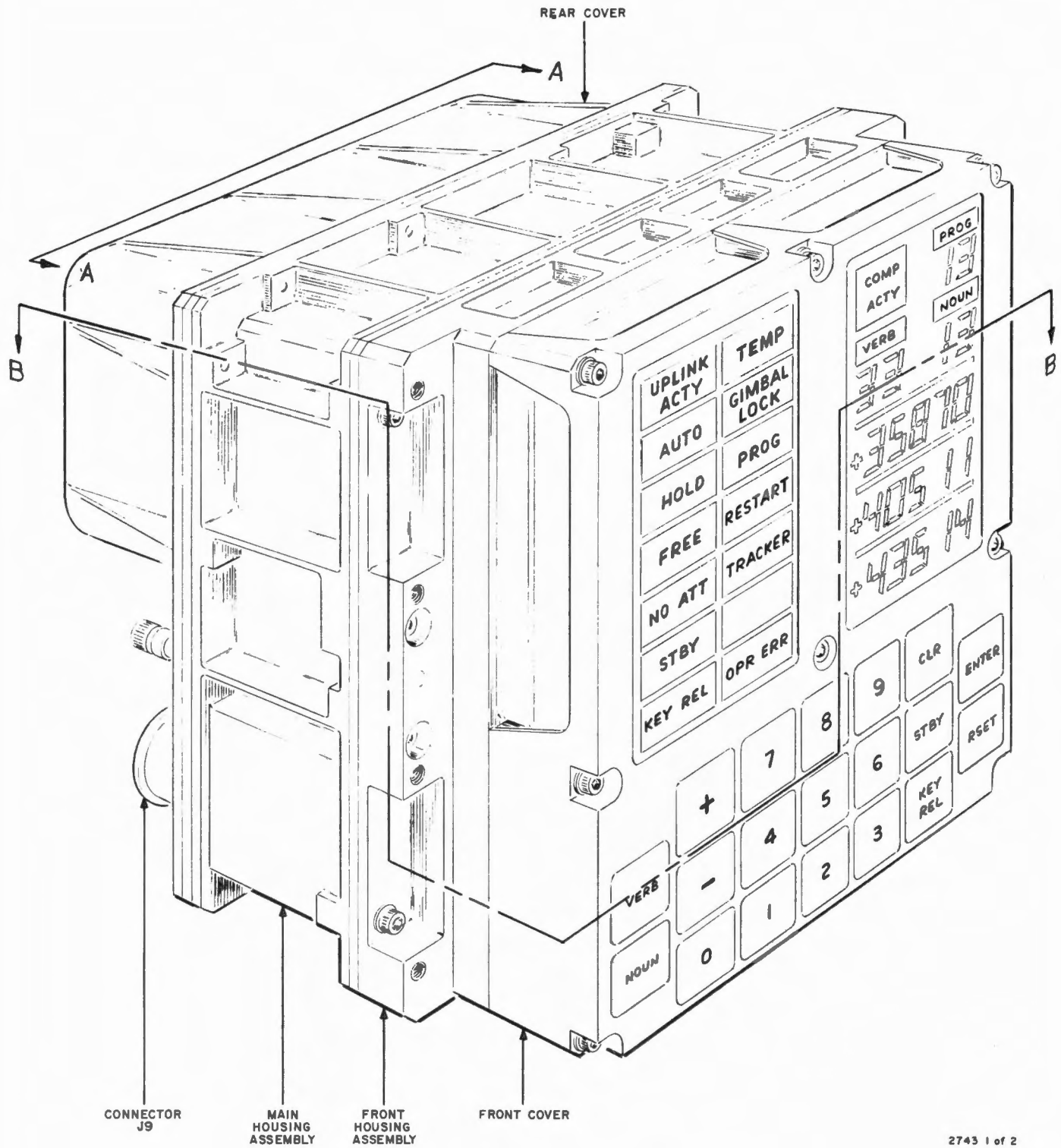
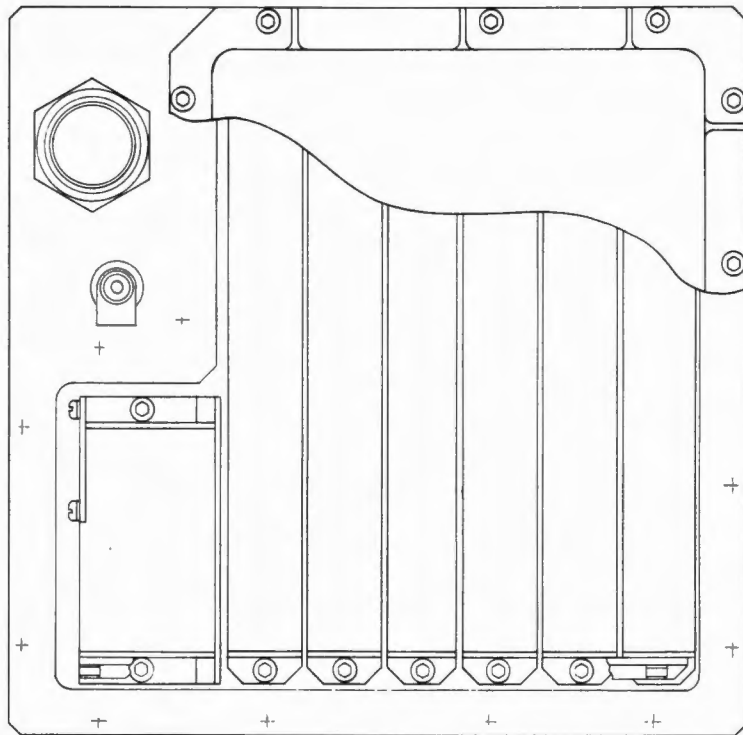
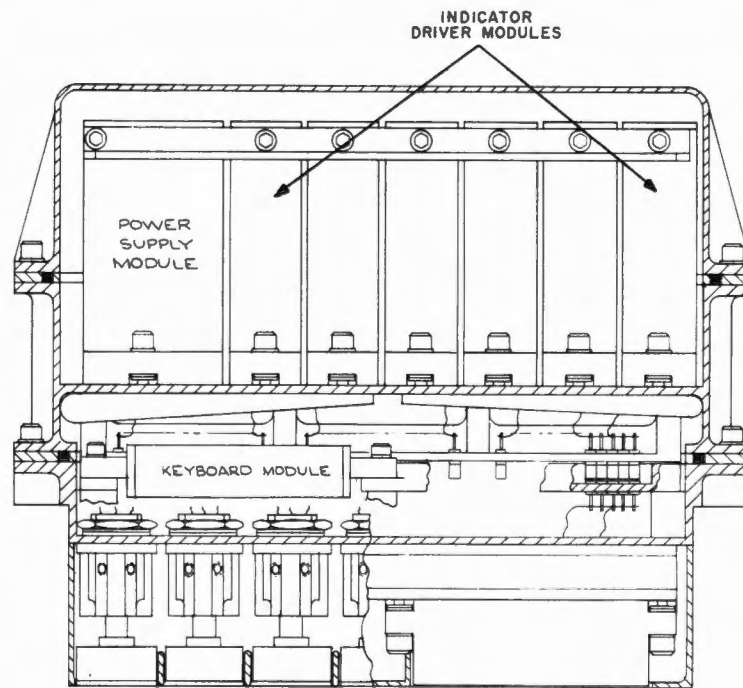


Figure 30-4. Block II DSKY (Sheet 1 of 2)



SECTION A-A



SECTION B-B

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Figure 30-4. Block II DSKY (Sheet 2 of 2)

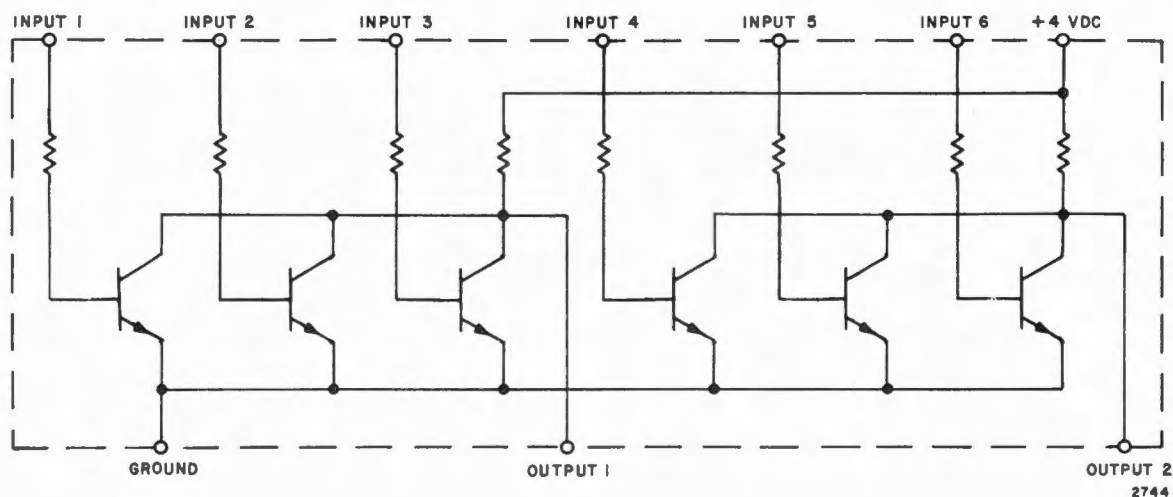


Figure 30-5. Flat Package, Schematic Diagram

If all inputs of a NOR gate are connected to a positive potential of about 0.2 volt or less, the output potential is approximately 1.5 volts. Thus, a logical ONE is represented by a positive potential of approximately 1.5 volts and a logical ZERO by a positive potential of about 0.2 volt. Since each NOR gate inverts voltage levels, a logical ZERO can represent either a data ZERO or a data ONE depending on the operational location of a gate, and a logical ONE can represent a data ONE or a data ZERO. The reference point is the input to the Write Amplifiers where a data ONE is represented by a logical ONE (positive potential of approximately 1.5 volts) and a data ZERO by a logical ZERO (positive potential of about 0.2 volt). At the outputs of the Write Amplifiers, a logical ONE (positive potential of approximately 1.5 volts) represents a data ZERO, and a logical ZERO (positive potential of approximately 0.2 volt) represents a data ONE.

30-15A. Table 30-0 lists all modules of the AGC, the numbers of NASA drawings showing the logic of these modules, and the numbers of the gates contained in the modules.

TABLE 30-0
MODULES AND DRAWING NUMBERS

Module	Drawing Number	Gate Numbers
A1	2005059	38101 - 38491
A2	2005060	37101 - 37459
A3	2005051	30001 - 30457
A4	2005062	36101 - 36460
A5	2005061	39101 - 39461
A6	2005063	40101 - 40441
A7	2005052	33101 - 33459
A8	2005055	51101 - 51463
A9	2005056	52101 - 52463
A10	2005057	53101 - 53463
A11	2005058	54101 - 54463
A12	2005053	34101 - 34467
A13	2005069	41101 - 41244
A14	2005064	42101 - 42457
A15	2005065	35101 - 35460
A16	2005066	43101 - 43460
A17	2005067	44101 - 44464
A18	2005068	45101 - 45456
A19	2005070	46101 - 46461
A20	2005054	31101 - 31459
A21	2005050	32001 - 32658
A22	2005071	47101 - 47460
A23	2005072	48101 - 48458
A24	2005073	49101 - 49443
A25-A26	2005021	-
A27-A29	2005020	-
A30-A31	2005010	-
B7	2005003	-
B8	2005008	-
B9-B10	2005004	-
B11	2005005	-
B12	2005006	-
B13-B14	2005002	-
B15	2005009	-
B16-B17	2005000	-
DSKY	2005900	-
DSKY	2005950	-
D1-D6	2005902	-
D8	2005903	-
Buffer	2014123	-

30-16. COMPUTER OPERATIONS

30-17. The organization of the AGC subsystem is illustrated in figure 30-6. The AGC subsystem can be divided into the following major sections:

- | | |
|-----------------------------|--|
| a. Timer | f. Standby Control |
| b. Sequence Generator (SQG) | g. Alarm Control |
| c. Central Processor (CP) | h. Power Supply |
| d. Erasable (E) Memory | i. Interface (including RHC Converter) |
| e. Fixed (F) Memory | j. Display and Keyboards (DSKY's) |

30-18. TIMER

30-19. The Timer consists of the Clock, the Scalers, and the Time Pulse Generator. The Clock is driven by a 2.048 Mc oscillator. For classified information, refer to Issue 1, paragraph 1-40.

30-20. The Clock provides various signals of 1.024 Mpps, 512 kpps, and 102.4 kpps. Some of these signals are used for driving the Time Pulse Generator, and for timing and gating various logic areas of the AGC. Two 102.4 kpps signals are fed into the 33 stage Scaler, each stage of which divides by two. Stage 10, for instance, supplies 100 pps (one pulse every 10 msec) and the last stage generates a pulse about every 23.3 hours. The last 28 stages of the Scaler can be read out like two 14-bit input channels (registers of the Input-Output Control), thus making time information available to the computer. If the AGC is in the standby mode, only the Clock and the Scaler are operating. When the mode is switched from standby to normal operation, time information is transferred under program control from the Scaler to time counters T2 and T1.

30-21. The Time Pulse Generator generates one time pulse every 0.977 μ sec and a sequence of twelve time pulses (T01 through T12) every 11.7 μ sec, which is referred to as one Memory Cycle Time (MCT). The time pulses control the Sequence Generator and other sections of the AGC.

30-22. SEQUENCE GENERATOR

30-23. The Sequence Generator (SQG) generates a set of control pulses, if required, for the subinstruction being executed whenever a time pulse (T01 through T12) is received. Each such set of control pulses is called an

Action. The control pulses control various registers and gates in the Central Processor (CP), the Input-Output Control, and other sections of the AGC. All Machine Instructions (Regular, Involuntary, and Peripheral or Test Instructions) are composed of one, two, or more subinstructions, each subinstruction consisting of 12 Actions (one MCT).

30-24. The execution of a Regular Instruction (Basic, Extra Code, Channel, or Special Instruction) is initiated by entering its order code into register SQ. When stored in memory, Extra Code and Channel Instructions use the same order codes as the Basic Instructions. However, Extra Code and Channel Instructions are preceded by Special Instruction EXTEND which enters a ONE into bit position EXT of register SQ. When a program is executed, one Regular Instruction after another is transferred from memory into the CP and the order code is entered into register SQ, together with the EXT bit which is entered into bit position SQ-EXT of register SQ.

30-25. Involuntary Instructions (Interrupting Instructions and Counter Instructions) are executed at the request of the Priority Control. Instruction RUPT commands the SQG to interrupt the execution of the program section currently being executed in favor of a programmed operation of higher priority. Instruction RUPT is executed upon request from the Interrupt Priority Control which also supplies the address of the priority program. Instruction RESUME, a Special (Regular) Instruction, orders the SQG to resume the execution of the interrupted program. Instruction GO commands the SQG to restart program execution. This instruction is executed at the occurrence of certain errors.

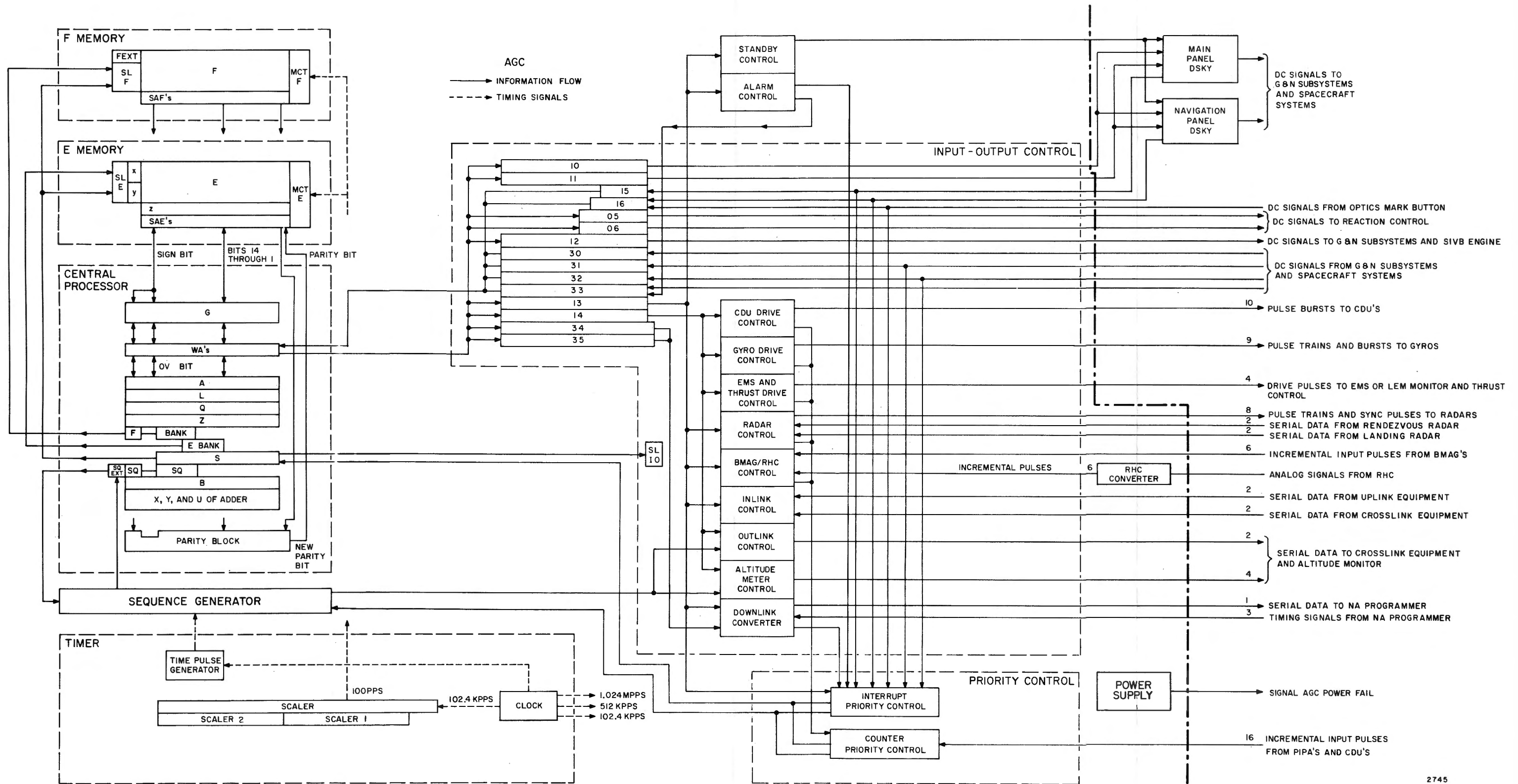
30-26. Counter Instructions cause the SQG to change the content of a specified counter. They are executed upon request from the Counter Priority Control which also supplies the proper counter address. The Counter Instructions are executed between the execution of Regular Instructions, and each delays the program execution by one MCT.

30-27. Peripheral Instructions are executed under the control of the Computer Test Set (CTS) or the Program Analyzer Console (PAC) during the testing of the AGC on the ground.

30-28. The control pulses generated by the SQG can be grouped in five categories:

- a. Read pulses - read content of a register to WA's (for instance, RA reads content of register A to the WA's; content of A is not changed)
- b. Write pulses - clear register and write into it information from WA's (for instance, WA writes into A from the WA's)

(cont)



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Figure 30-6. Block II AGC Subsystem, Machine Organization

- c. Direct read-write - copy content of one register directly (not via WA's) into another register (for instance, A2X copies c(A) into X)
- d. Test pulses - test content of certain bit positions and set branch flip-flops accordingly (for instance, TOV tests for overflow)
- e. Special pulses - enter certain information into the WA's or into a register, or set certain flip-flops, etc.

All control pulses are defined in Issue 32, table 32-4.

30-29. CENTRAL PROCESSOR

30-30. The Central Processor (CP) consists of various registers, the Adder, the Write Amplifiers (WA's), and the Parity Block. All CP registers are NOR gate flip-flop registers which can be read nondestructively.

30-31. All CP registers are shown in figure 30-6. Registers A, L, Q, Z, and B consist of 16-bit positions (flip-flops) each, which are numbered 16 through 1 from left to right. Register FBANK consists of 5-bit positions numbered 16 and 14 through 11. Register EBANK consists of 3-bit positions numbered 11 through 9. Register S consists of 12-bit positions numbered 12 through 1. Register SQ consists of 7-bit positions, one named SQ-EXT and the remainder numbered 16 and 14 through 10. Registers X and Y of the Adder each also consist of 16-bit positions numbered 16 through 1. The 16 output gates (U) of the Adder, and the WA's are also numbered 16 through 1. All registers mentioned so far may contain instructions, addresses, a code, etc., or a number, but do not contain a parity bit. Whenever a number is contained, the lowest order bit is stored in bit position 1, the highest order bit in bit position 14, and the sign bit (a ZERO for a plus sign and a ONE for a minus sign) is stored in bit position 16. Bit position 15 is used for storing any overflow bit (OV).

30-32. Register G, which serves as a buffer between the CP and the memories, consists of 16-bit positions which are numbered 16 through 1. Any parity bit which is received from memory is transferred to the Parity Block but to no CP register. The 16 inputs to the Parity Block are numbered 16 and 14 through 0. No provision is made to enter an overflow bit into the Parity Block.

30-33. CP REGISTER MANIPULATIONS

30-34. Registers A, L, Q, FBANK, EBANK, and Z are addressable; registers B, S, SQ, Y, X, and G are not addressable. A register is addressable when it can be selected for write-in or read-out by entering the proper address into register S.

TABLE 30-1
 INFORMATION FLOW BETWEEN CP REGISTER
 BIT POSITIONS AND WRITE AMPLIFIERS

Octal Address	Ini- tials	Register		Control Pulse	Read and Write Lines of Write Amplifiers (WA's)																	
					16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
0000	A	Accumulator		WA, WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
				WALS Δ	14	13	12	11	10	9	8	7	6	5	4	3	2	1	-	-		
				RA, RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
0001	L	Low Order Accumulator		WL, WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
				WALS Δ	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	13		
				RL, RSC	16	-	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
0002	Q	Return Address Register		WQ, WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
				RQ, RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
0003	EBANK	E Memory Bank Selector		WSC	-	-	-	-	-	11	10	9	-	-	-	-	-	-	-			
				RSC	-	-	-	-	-	11	10	9	-	-	-	-	-	-	-	-		
0004	FBANK	F Memory Bank Selector		WSC	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-			
				RSC	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-		
0005	Z	Program Counter		WZ, WSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
				RZ, RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
0006	BBANK	Both registers EBANK and FBANK		EBANK	WSC	-	-	-	-	-	-	-	-	-	-	-	-	11	10	9		
					RSC	-	-	-	-	-	-	-	-	-	-	-	-	-	11	10	9	
				FBANK	WSC	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-	-
					RSC	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-	-
0007	ZERO	ZERO (non-existing register)		RSC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

Δ WALS also enters content of bit position 16 of G into bit positions 16 and 15 of A if bit position 1 of G contains a ZERO or enters content of output gate 16 of U into bit positions 16 and 15 if bit position 1 of G contains a ONE.

TABLE 30-1
 INFORMATION FLOW BETWEEN CP REGISTER
 BIT POSITIONS AND WRITE AMPLIFIERS (cont)

Register			Control Pulse	Read and Write Lines of Write Amplifiers (WA's)																		
Octal Address	Initials	Name		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
none	B C	Buffer Register with direct output B and complement output C	WB	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			RB, RC	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			RL10BB	-	-	-	-	-	-	10	9	8	7	6	5	4	3	2	1			
none	S	Address Register	WS	-	-	-	-	12	11	10	9	8	7	6	5	4	3	2	1			
none	SQ	Sequence Register	WSQ	16	-	14	13	12	11	10	-	-	-	-	-	-	-	-	-			
none	Y X U	Adder with input registers X and Y and output gates U	WY	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			WY12	-	-	-	-	12	11	10	9	8	7	6	5	4	3	2	1			
			WYD Δ	1	16	-	15	14	13	12	11	10	9	8	7	6	5	4	3	2		
			RU	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
			RUS	15	-	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
none	G	Memory Buffer Register		RG	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
		Function	c(S)	Control Signal																		
		Direct	Any Other Address	WG1G, WG5G	WG	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
		CYR	0020	WG2G, WG4G	WG	14	-	13	12	11	10	9	8	7	6	5	4	3	2	1	16	
		SR	0021	WG2G, WG5G	WG	16	14	-	13	12	11	10	9	8	7	6	5	4	3	2	1	-
		CYL	0022	WG3G, WG6G	WG	1	-	16	14	13	12	11	10	9	8	7	6	5	4	3	2	
		EDOP	0023	WG3G, WG5G	WG	-	-	7	6	5	4	3	2	1	-	-	-	-	-	-	-	

Δ There are exceptions where content of WA 16 is not entered into bit position 1 of Y.

Table 30-1 lists those control pulses in addition to control pulses WSC and RSC. Control pulses WSC and RSC are applied to all addressable registers for write-in or read-out, but only that register, the register of which is contained in register S, is written into or read out.

30-35. A word can be transferred from one CP register to another either via the WA's or directly. Read and Write control pulses (paragraph 30-28) occur simultaneously and gate the read gates of the transmitting and the write gates of the receiving register at the same time and thus allow a word to flow from one register to another via the WA's. (Refer to table 30-1). The flow of information to and from the WA's occurs on two different sets of lines, the read and write lines. When one read pulse and two or three write control pulses occur simultaneously, the same information is entered into two or three registers. Direct read-write pulses transfer information directly from one register to only one other register.

30-36. Information contained in the WA's is written into the corresponding bit position of register A if control pulse WA is applied; information contained in register A is read out to the corresponding WA's if control pulse RA is applied. When control pulse WALs is applied (during a multiplication), the information contained in the WA's is shifted two places to the right while writing into register A whereby the last two bits are shifted into register L. When control pulse WL is applied, information contained in the WA's is written into the corresponding bit positions of register L. Information contained in register L is read into the corresponding WA's by means of control pulse RL except for the content of bit position 16 which is read into WA16 and WA15. Refer to table 30-1.

30-37. Registers Q and Z are written into and read out straight, i. e., from and into the corresponding WA's. Registers FBANK and EBANK are written into and read out straight if address 0003 or 0004 is contained in register S. If register S contains 0006, the content of the WA's is written into or read out straight from register FBANK but shifted eight places as it is written into or read out of register EBANK. Register B is always written into and read out straight; however, the content of register B (by means of control pulse RB) or its complement (by means of RC) can be read into the WA's. Control pulse RL10BB reads only the content of bit positions 10 through 1 into the corresponding WA's.

30-38. Registers S and SQ are written into from the corresponding WA's. Bit position SQ-EXT accepts the EXT bit (paragraph 30-24).

30-39. Both registers Y and X of the Adder are cleared whenever control pulse WY, WY12, or WYD is generated. Control pulse WY writes the content of WA's 16 through 1 into register Y; control pulse WY12 writes only the content of WA's 12 through 1 into register Y. Control pulse WYD cycles the content of the WA's one place to the left as it is written into register Y, thereby doubling the content of the WA's. Information is transferred directly (not via WA's) from register A to register X whenever control pulse A2X is applied. Control pulse RU reads the sum contained in the Adder into the corresponding WA's. Control pulse RUS, which is used in connection with inlink and TWO's - complement operations, reads the content of output gate 15 into WA's 16 and 15.

30-40. Register G is able to exchange information (except the parity bit) with E or F Memory on one side, and with the CP registers on the other side. Words stored in E or F Memory consist of 16 bits numbered 15 through 0 where bit number 0 is the parity bit. If a memory location contains a number, bit position 15 stores the sign bit and bit position 1 the lowest order bit. When a word is transferred from E or F Memory to register G, bit number 15 is entered into bit positions 16 and 15 of register G while bits 14 through 1 are entered into the corresponding bit positions of register G. Entering a sign bit into bit positions 16 and 15 has the effect of providing a sign bit in bit position 16 and a plus or minus zero (ZERO or ONE) in bit position 15, i. e., in front of the fourteen value bits. Likewise, the content of bit positions 16 and 14 through 1 of register G is transferred to bit positions 15 through 1 in E Memory while the new parity bit, which is supplied by the Parity Block, is entered into bit position 0. The content of bit position 15 of register G is not transferred to memory. Consequently, any overflow bit (opposite to sign bit) which might be contained in bit position 15 is lost on the way to memory.

30-41. Whenever register G is read into the CP, the content of its bit positions is transferred to the corresponding WA's. When the content of the WA's is written into register G, normally WA's 16 through 1 are gated into the corresponding bit positions of register G. If register S contains address 0020, 0021, or 0022, the content of WA's 16 and 14 through 1 is cycled one place to the right, shifted one place to the right, or cycled one place to the left, respectively, while writing into bit positions 16 and 14 through 1 of register G (table 30-1). If register S contains address 0023, the content of the WA's is shifted seven places to the right, as requested during the breaking of Interpretive Instruction Words.

30-42. ADDER

30-43. The Adder, the arithmetic unit of the AGC, is able to add two ONE's complement or two cyclic TWO's complement numbers at a time. Normally, an addition is carried out in the ONE's complement number system.

The Adder has two input registers (X and Y) and a bank of output gates (U). Two ONE's complement numbers to be added can be of the same or opposite sign. Numbers containing fourteen value bits can be added; the Adder generates an additional bit in bit position 15 in case of positive or negative overflow. Control pulses WY, WY12, and WYD reset both the X and Y registers; therefore, the Y register must be loaded first or simultaneously with register X. The arithmetic sum of the two values is available at output gate U less than 1 μ sec after both operands have been entered. The Sequence Generator, on command, can enter the positive quantity one (000001) or the negative quantity one (177776) into register X, or force a carry into the Adder.

30-44. As shown in figure 30-7, the bit positions of the Adder registers (X and Y) and the output gates (U) are numbered 16 through 1. (No parity bit is entered into the Adder.) When an operand is gated from E or F Memory into register Y (via register G), its sign (SG) is entered into bit positions 16 and 15. A plus is represented by a ZERO, a minus by a ONE. Entering a sign bit into bit position 15 is equivalent to providing an additional value bit, either a plus or a minus zero (which is represented by a ZERO or a ONE) in front of the fourteen-bit value. When an operand is gated from register A into the corresponding bit positions of register X (control pulse A2X), its sign bit is entered into bit position 16 only. Bit position 15 could receive an overflow bit but, normally, contains the same bit as bit position 16. If an overflow occurs during an addition, the Adder supplies a ONE for a plus overflow, or a ZERO for a minus overflow at output gate 15. This additional output bit is labeled OV. Output gate 16 always contains the correct sign of the sum.

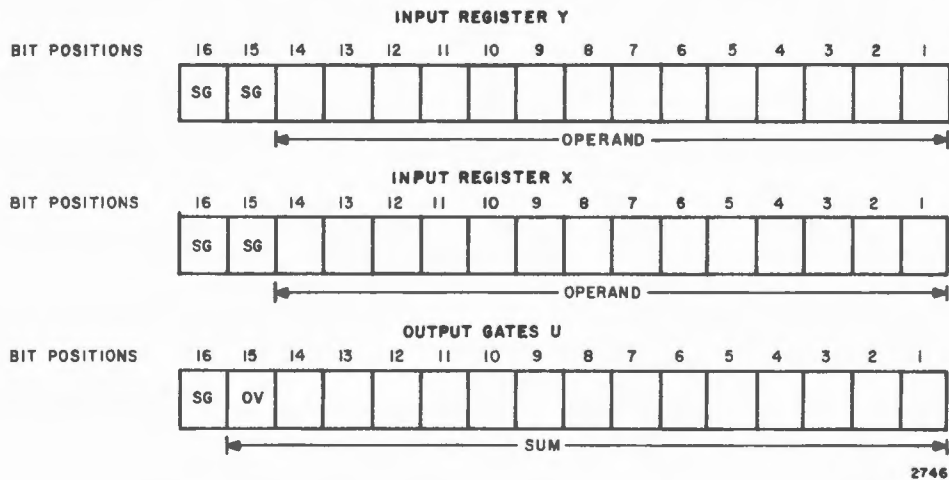


Figure 30-7. Adder Input Registers and Output Gates

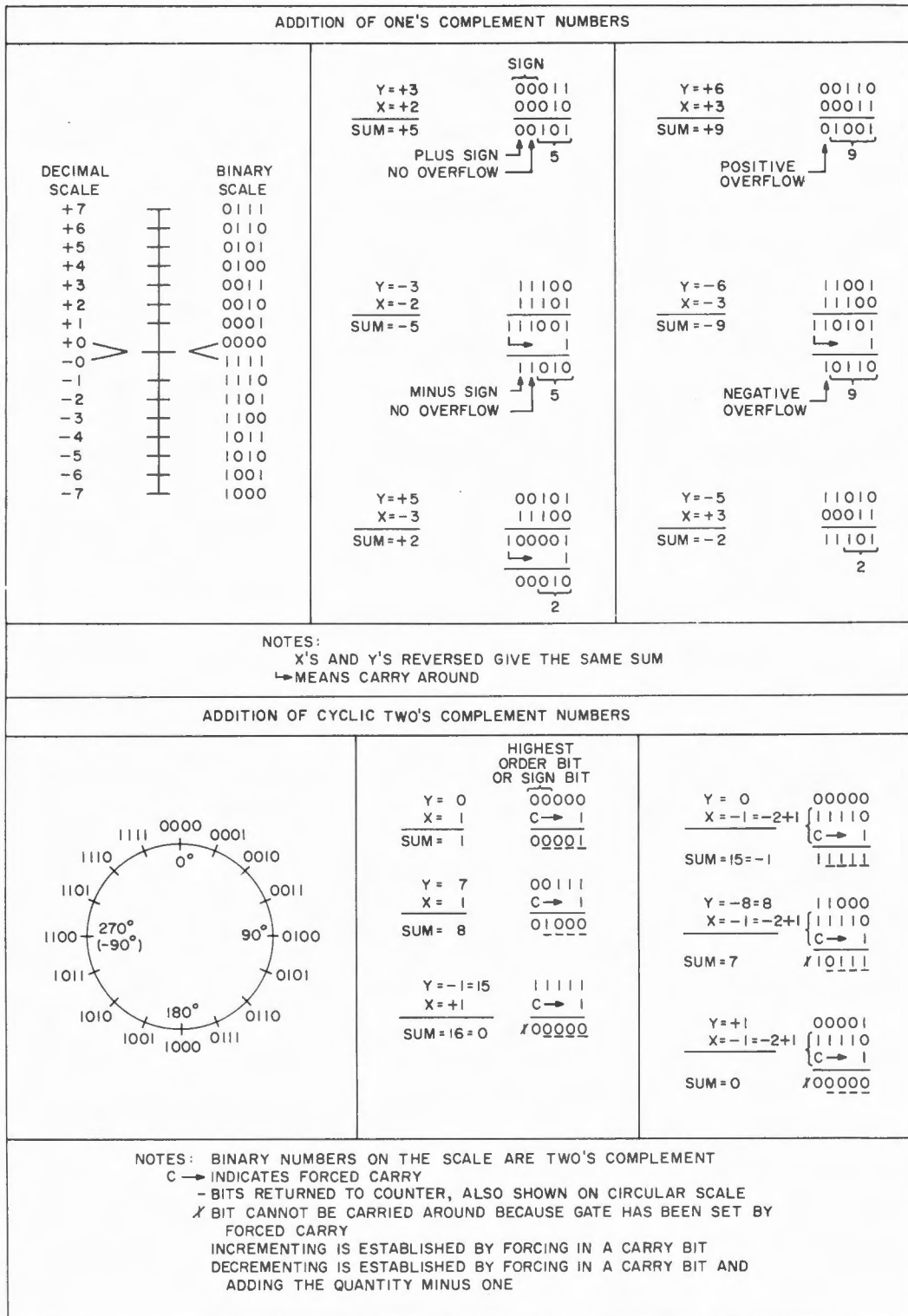
30-45. The upper half of figure 30-8 illustrates the principle of adding two ONE's complement numbers. For simplification, each number consists of two sign bits as normally entered into bit positions 16 and 15 of registers Y and X, and of only 3 value bits instead of 14. In reality, the largest octal number resulting from ONE's complement addition as provided by the sixteen output gates (U) is + 77777 (quantity 077777), the smallest is - 77777 (quantity 100000). Counters are incremented or decremented by adding the quantity plus one or minus one to whatever might be contained in the counter.

30-46. The lower half of figure 30-8 illustrates the principle of adding two cyclic TWO's complement numbers. A cyclic TWO's complement number stored in memory can be interpreted in two different ways. One can consider the fifteen bits stored in bit positions 15 through 1 as 15 value bits representing positive TWO's complement numbers only which express angular information from 0° to 360° . One can also consider the bit stored in bit position 15 as a sign bit and the bits stored in bit positions 14 through 1 as the value bits representing positive TWO's complement numbers which express angles from 0° to plus 180° , or negative TWO's complement numbers which express angles from 0° to minus 180° . The first way of interpretation better explains cyclic TWO's complement operations.

30-47. Whenever cyclic TWO's complement information is transferred from memory, bit 15 is entered into bit positions 16 and 15 of the Adder. Whenever a cyclic TWO's complement sum is transferred from the output gates to E Memory, the content of output gate 15 is entered into bit positions 16 and 15 of register G, and finally read from bit position 16 of register G into bit position 15 of the addressed E Memory location. In reality, the largest octal quantity which can result from a cyclic TWO's complement addition is 77777. In the examples of figure 30-8, four-bit numbers are assumed whereby the highest order bit is entered into two bit positions of register Y or X.

30-48. PARITY BLOCK

30-49. When a word is transferred from memory to the CP, bits 15 through 1 are entered into register G which passes these fifteen bits on to the Parity Block. Bit 0, the parity bit, is transferred from memory directly to the Parity Block where it is stored in the SAP flip-flop (gates 34245/34246). Bits 15 through 1 are fed into a parity tree which generates a new parity bit (PC15). If bits 15 through 1 contain an odd number of ONE's, bit PC15 becomes a ZERO; if they contain an even number of ONE's, bit PC15 becomes a ONE. The new parity bit (PC15) and the original parity bit (bit 0 stored in the SAP flip-flop) are compared and signals PALE (parity alarm) and MPAL/ are generated if the two bits do not agree and if the word was received from memory (octal address 0010 or larger). All sixteen bits (bits 15 through 0) of a word stored in memory must always contain an odd number of ONE's which



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Figure 30-8. Summation of Two Binary Numbers

is established by entering the proper parity bit. The parity bit provides a simple means of detecting single errors, or any odd number of errors when reading out of F or E Memory. Registers 0000 through 0007 do not store a parity bit.

30-50. Bits 16 and 14 through 1 of a word entered into register G from a CP register are passed on to the Parity Block in a similar way; however, no test for correct parity is made and bit CP15 generates signal GEMP which writes the parity bit into E Memory if required.

30-51. MEMORIES

30-52. The Erasable (E) Memory is a coincident-current ferrite core array capable of storing 2048 sixteen-bit words. The selection logic (SLE) (figure 30-6) together with the x and y selection, the z drivers, the 16 sense amplifiers (SAE's), and the memory cycle timer (MCTE) permit addressing certain location in E Memory. Information can be transferred from the addressed location to register G at time pulse T04 or vice versa at time pulse T10. Readout of the E Memory is destructive; however, information can be preserved for later use by writing it back into the addressed location after readout if no new information is to be entered. The selection logic SLE is under the control of registers S and EBANK.

30-53. The Fixed (F) Memory consists of six core rope modules which are built from Mo-perm magnetic cores and is capable of storing 36,864 sixteen-bit words. The addressing scheme employed allows the extension of Fixed Memory to 65,536 words. The selection logic (SLF) together with various drivers, the sense amplifiers (SAF's), and the memory cycle timer (MCTF) make it possible to address a certain location in F Memory and to read its content into register G at T06. Information stored in F Memory is wired in and cannot be destroyed during readout, therefore, it does not have to be preserved for writing back into F memory. The selection logic (SLF) is under the control of registers S, FBANK, and FEXT. Register FEXT, which consists of three bit positions numbered 7 through 5, is addressed like a register in the Input-Output Control.

30-54. ADDRESSING

30-55. The E Memory can be subdivided into eight E Banks (0 through 7) as indicated in table 30-2. Each bank is capable of storing 256 words. The first 8 locations of E-Bank 0 are not used because their addresses are needed to address the CP registers. Another 12 addresses are reserved for addressing special locations and 29 for addressing counters, all of which are part of E-Bank 0. The remaining 207 addresses are used for addressing those locations of E-Bank 0 which are accessible for general use.

30-56. E-Banks 0, 1, and 2 are referred to as Unswitched E Memory because all their locations (as well as the CP registers) can be addressed by entering their addresses into register S without regard to what might be contained (XXX) in register EBANK. E-Banks 3 through 7 are referred to as Switched E Memory because all their locations can be addressed only if the respective bank number is contained in register EBANK. Locations in Unswitched E Memory can also be addressed as locations in Switched E Memory if the proper bank number is contained in register EBANK. Of course, the contents of registers FBANK and FEXT are irrelevant whenever any location in the CP or E Memory is addressed.

(text continued on page 30-32)

TABLE 30-2
E ADDRESSING

Register or Location Groups		Octal Address		c(FEXT)			c(FBANK)					c(EBANK)			c(S)												
		EMA	Real	7	6	5	16	14	13	12	11	11	10	9	12	11	10	9	8	7	6	5	4	3	2	1	
CP		0000-0007	0000-0007 1400-1407	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	y	y	y
Special Locations		0010-0023	0010-0023 1410-1423	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	y	y	y
Counters		0024-0060	0024-0060 1424-1460	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	y	y	y	
General Use		0061-0377	0061-0377 1461-1777	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	y	y	y	y	y	y	y	y	
E-Bank 1		0400-0777	0400-0777 1400-1777	x	x	x	x	x	x	x	x	x	x	x	0	0	0	1	y	y	y	y	y	y	y	y	
E-Bank 2		1000-1377	1000-1377 1400-1777	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	y	y	y	y	y	y	y	y	
E-Bank 3		1400-1777	1400-1777	x	x	x	x	x	x	x	x	0	1	1	0	0	1	1	y	y	y	y	y	y	y	y	
E-Bank 4		2000-2377	1400-1777	x	x	x	x	x	x	x	x	1	0	0	0	0	1	1	y	y	y	y	y	y	y	y	
E-Bank 5		2400-2777	1400-1777	x	x	x	x	x	x	x	x	1	0	1	0	0	1	1	y	y	y	y	y	y	y	y	
E-Bank 6		3000-3377	1400-1777	x	x	x	x	x	x	x	x	1	1	0	0	0	1	1	y	y	y	y	y	y	y	y	
E-Bank 7		3400-3777	1400-1777	x	x	x	x	x	x	x	x	1	1	1	0	0	1	1	y	y	y	y	y	y	y	y	

- 1 x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.
- 2 CP registers and Special Locations will be addressed as E-Bank 0 only under exceptional circumstances.

TABLE 30-3
F ADDRESSING

Register or Location Groups		Octal Address		c(FEXT) ¹	c(FBANK) ¹	c(EBANK) ¹	c(S) ²											
		FMA	Real	7 6 5	16 14 13 12 11	11 10 9	12 11 10 9 8 7 6 5 4 3 2 1											
FEXT-Channel X	Fixed F Memory	F-Bank 02	04000-05777	4000-5777 2000-3777	x x x x x x	x x x x x 0 0 0 1 0	x x x x x x	1 0 y y y y y y y y y y 0 1 y y y y y y y y y y										
		F-Bank 03	06000-07777	6000-7777 2000-3777	x x x x x x	x x x x x 0 0 0 1 1	x x x x x x	1 1 y y y y y y y y y y 0 1 y y y y y y y y y y										
	Common F Memory	F-Bank 00	00000-01777	2000-3777	x x x	0 0 0 0 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 01	02000-03777	2000-3777	x x x	0 0 0 0 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 04	10000-11777	2000-3777	x x x	0 0 1 0 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 05	12000-13777	2000-3777	x x x	0 0 1 0 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 06	14000-15777	2000-3777	x x x	0 0 1 1 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 07	16000-17777	2000-3777	x x x	0 0 1 1 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 10	20000-21777	2000-3777	x x x	0 1 0 0 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 11	22000-23777	2000-3777	x x x	0 1 0 0 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 12	24000-25777	2000-3777	x x x	0 1 0 0 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 13	26000-27777	2000-3777	x x x	0 1 0 1 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 14	30000-31777	2000-3777	x x x	0 1 1 0 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 15	32000-33777	2000-3777	x x x	0 1 1 0 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 16	34000-35777	2000-3777	x x x	0 1 1 1 0	x x x	0 1 y y y y y y y y y y										
		F-Bank 17	36000-37777	2000-3777	x x x	0 1 1 1 1	x x x	0 1 y y y y y y y y y y										
		F-Bank 20	40000-41777	2000-3777	x x x	1 0 0 0 0	x x x	0 1 y y y y y y y y y y										

¹ x means 0 or 1 which does not have an effect on addressing.

² y means 0 or 1 as defined by address.

TABLE 30-3
F ADDRESSING (cont)

Register or Location Groups		Octal Address		c(FEXT) ^{△1}	c(FBANK) ^{△1}	c(EBANK) ^{△1}	c(S) ^{△2}	
		FMA	Real	7 6 5	16 14 13 12 11	11 10 9	12 11 10 9 8 7 6 5 4 3 2 1	
FEXT-Channel X (cont)	Common F Memory (cont)	F-Bank 21	42000-43777	2000-3777	x x x	1 0 0 0 1	x x x	0 1 y y y y y y y y
		F-Bank 22	44000-45777	2000-3777	x x x	1 0 0 1 0	x x x	0 1 v y y y y y y y
		F-Bank 23	46000-47777	2000-3777	x x x	1 0 0 1 1	x x x	0 1 y y y y y y y y
		F-Bank 24	50000-51777	2000-3777	x x x	1 0 1 0 0	x x x	0 1 y y y y y y y y
		F-Bank 25	52000-53777	2000-3777	x x x	1 0 1 0 1	x x x	0 1 y y y y y y y y
		F-Bank 26	54000-55777	2000-3777	x x x	1 0 1 1 0	x x x	0 1 y y y y y y y y
		F-Bank 27	56000-57777	2000-3777	x x x	1 0 1 1 1	x x x	0 1 y y y y y y y y
FEXT Channel 0-3	F-Bank 30	060000-061777	2000-3777	0 x x	1 1 0 0 0	x x x	0 1 y y y y y y y y	
	F-Bank 31	062000-063777	2000-3777	0 x x	1 1 0 0 1	x x x	0 1 y y y y y y y y	
	F-Bank 32	064000-065777	2000-3777	0 x x	1 1 0 1 0	x x x	0 1 y y y y y y y y	
	F-Bank 33	066000-067777	2000-3777	0 x x	1 1 0 1 1	x x x	0 1 y y y y y y y y	
	F-Bank 34	070000-071777	2000-3777	0 x x	1 1 1 0 0	x x x	0 1 y y y y y y y y	
	F-Bank 35	072000-073777	2000-3777	0 x x	1 1 1 0 1	x x x	0 1 y y y y y y y y	
	F-Bank 36	074000-075777	2000-3777	0 x x	1 1 1 1 0	x x x	0 1 y y y y y y y y	
	F-Bank 37	076000-077777	2000-3777	0 x x	1 1 1 1 1	x x x	0 1 y y y y y y y y	

^{△1} x means 0 or 1 which does not have an effect on addressing.

^{△2} y means 0 or 1 as defined by address.

TABLE 30-3
F ADDRESSING (cont)

Register or Location Groups	Octal Address		c(FEXT)	c(FBANK)	c(EBANK) [Ⓜ]	c(S) [Ⓜ]
	FMA	Real	7 6 5	16 14 13 12 11	11 10 9	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel 4	F-Bank 40	10000-101777	2000-3777	1 1 0 0 0	x x x	0 1 y y y y y y y y
	F-Bank 41	102000-103777	2000-3777	1 1 0 0 1	x x x	0 1 y y y y y y y y
	F-Bank 42	104000-105777	2000-3777	1 1 0 1 0	x x x	0 1 y y y y y y y y
	F-Bank 43	106000-107777	2000-3777	1 1 0 1 1	x x x	0 1 y y y y y y y y
	F-Bank 44	110000-111777	2000-3777	1 1 1 0 0	x x x	0 1 y y y y y y y y
	F-Bank 45	112000-113777	2000-3777	1 1 1 0 1	x x x	0 1 y y y y y y y y
	F-Bank 46	114000-115777	2000-3777	1 1 1 1 0	x x x	0 1 y y y y y y y y
	F-Bank 47	116000-117777	2000-3777	1 1 1 1 1	x x x	0 1 y y y y y y y y
FEXT-Channel 5	F-Bank 50	120000-121777	2000-3777	1 1 0 0 0	x x x	0 1 y y y y y y y y
	F-Bank 51	122000-123777	2000-3777	1 1 0 0 1	x x x	0 1 y y y y y y y y
	F-Bank 52	124000-125777	2000-3777	1 1 0 1 0	x x x	0 1 y y y y y y y y
	F-Bank 53	126000-127777	2000-3777	1 1 0 1 1	x x x	0 1 y y y y y y y y
	F-Bank 54	130000-131777	2000-3777	1 1 1 0 0	x x x	0 1 y y y y y y y y
	F-Bank 55	132000-133777	2000-3777	1 1 1 0 1	x x x	0 1 y y y y y y y y
	F-Bank 56	134000-135777	2000-3777	1 1 1 1 0	x x x	0 1 y y y y y y y y
	F-Bank 57	136000-137777	2000-3777	1 1 1 1 1	x x x	0 1 y y y y y y y y

Ⓜ

Ⓜ x means 0 or 1 which does not have an effect on addressing.
 Ⓜ y means 0 or 1 as defined by address.
 Ⓜ Banks 44 through 77 do not exist (paragraph 30-57)

TABLE 30-3
F ADDRESSING (cont)

Register or Location Groups		Octal Address		c(FEXT)			c(FBANK)					c(EBANK) ^①			c(s) ^②											
		FMA	Real	7	6	5	16	14	13	12	11	11	10	9	12	11	10	9	8	7	6	5	4	3	2	1
FEXT-Channel 6	F-Bank 60	140000-141777	2000-3777	1	1	0	1	1	0	0	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 61	142000-143777	2000-3777	1	1	0	1	1	0	0	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 62	144000-145777	2000-3777	1	1	0	1	1	0	1	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 63	146000-147777	2000-3777	1	1	0	1	1	0	1	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 64	150000-151777	2000-3777	1	1	0	1	1	1	0	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 65	152000-153777	2000-3777	1	1	0	1	1	1	0	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 66	154000-155777	2000-3777	1	1	0	1	1	1	1	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y
F-Bank 67	156000-157777	2000-3777	1	1	0	1	1	1	1	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	y	
FEXT-Channel 7	F-Bank 70	160000-161777	2000-3777	1	1	1	1	1	0	0	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 71	162000-163777	2000-3777	1	1	1	1	1	0	0	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 72	164000-165777	2000-3777	1	1	1	1	1	0	1	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 73	166000-167777	2000-3777	1	1	1	1	1	0	1	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 74	170000-171777	2000-3777	1	1	1	1	1	1	0	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 75	172000-173777	2000-3777	1	1	1	1	1	1	0	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 76	174000-175777	2000-3777	1	1	1	1	1	1	1	0	x	x	x	0	1	y	y	y	y	y	y	y	y	y	
	F-Bank 77	176000-177777	2000-3777	1	1	1	1	1	1	1	1	x	x	x	0	1	y	y	y	y	y	y	y	y	y	

^① x means 0 or 1 which does not have an effect on addressing.
^② y means 0 or 1 as defined by address.
^③ Banks 44 through 77 do not exist (paragraph 30-57)

30-57. The F Memory address field provided can be subdivided into 64 F-Banks (octal 00 through 77 as indicated in table 30-3). Each bank is capable of storing 1024 words. Only 36 F-Banks (00 through 43) are built into the AGC, another 28 F-Banks (44 through 77) could be added, which would require some major modifications of the computer.

30-58. F-Banks 00 through 27 are referred to as FEXT-Channel X because all their locations can be addressed by entering their addresses into registers S and FBANK without regard to what might be contained (XXX) in register FEXT. F-Banks 30 through 37 are referred to as FEXT-Channel 0-3 because all their locations can be addressed if channel numbers 0, 1, 2, or 3 (0XX) are contained in register FEXT. F-Banks 40 through 47, 50 through 57, 61 through 67, etc., are referred to as FEXT-Channel 4, 5, 6, etc., respectively, because all their locations can be addressed only if the correct channel number is contained in register FEXT.

30-59. F-Banks 02 and 03 are also referred to as Fixed-Fixed Memory; the other banks of FEXT-Channel X are referred to as Variable-Fixed Memory. All locations in Fixed-Fixed Memory can be addressed by entering their addresses into register S without regard to what might be contained (XXXXX) in register FBANK. All other locations of F Memory can be addressed only if the proper bank number is contained in register FBANK. Locations in Fixed-Fixed Memory can also be addressed like any other location in F Memory if the proper bank number is contained in register FBANK. The content of register EBANK is irrelevant whenever a location in F Memory is addressed.

30-60. Two different classes of pseudo addresses are used: Erasable Memory Addresses (EMA's) and Fixed Memory Addresses (FMA's). When register S contains ZERO's in both bit positions 12 and 11 it indicates that the register contains a real address which represents an EMA. (Refer to table 30-2). When both bit positions 10 and 9 also contain ZERO's it indicates that a CP register or a location in E-Bank 0 is addressed, regardless of the contents of register EBANK. When bit positions 10 or 9 but not both contain a ONE, a location in E-Bank 1 or 2 is addressed regardless of the contents of register EBANK. When bit positions 10 and 9 both contain a ONE, a location is addressed in that E-Bank the number of which is contained in register EBANK.

30-61. The EMA's are composed of four octal digits which represent eleven binary digits (bits) numbered 11 through 1. Bits 11 through 9 indicate an E-Bank number (in many cases contained in register EBANK). Bits 8 through 1 represent that part of the real address which is contained in bit positions 8 through 1 of register S.

30-62. When register S contains a ONE in bit position 12 or 11, or in both, it indicates that the register contains a real address which represents an FMA. (Refer to table 30-3). Whenever bit position 12 contains a ONE, Fixed-Fixed Memory is addressed, regardless of the contents of registers

FBANK and FEXT. Whenever bit position 12 contains a ZERO and bit position 11 a ONE, a location is addressed in that F Bank which is defined by the contents of registers FBANK and FEXT.

30-63. When bit position 16 and 14 of register FBANK both contain ZERO's, or a ZERO and a ONE, and bit position 12 of register S contains a ZERO and bit position 11 a ONE, it indicates that a bank in FEXT-Channel X is addressed in which case the content of register FEXT is irrelevant. When bit positions 16 and 14 of registers FBANK both contain ONE's, a bank in FEXT-Channel 0-3, or 4 through 77 is addressed.

30-64. The FMA's are composed of six octal digits which represent sixteen bits numbered 16 through 1. Bits 16 through 11 indicate an F-Bank number. In many cases this number is contained in register FBANK, or register FEXT and bit positions 13 through 11 of register FBANK. Bits 10 through 1 represent that part of the real address which is contained in bit positions 10 through 1 of register S.

30-65. E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS

30-66. For assignments of E locations 0010 through 0060 refer to table 30-4. Locations 0010 through 0017 are reserved for storing pertinent information of an interrupted program section. Locations 0020 through 0023 are used for storing cycled or shifted data as explained in paragraph 30-41. Locations 0024 through 0060 are counters. Whether the content of a counter is incremented, decremented, diminished (absolute value decreased) or shifted depends on the purpose of the counter. Seven types of counters can be distinguished as shown in the following subparagraphs.

- a. Input counters which contain ONE's complement numbers to be incremented only are time counters 0024 through 0030. Whenever such a counter is addressed, an addition is performed as illustrated in the upper part of figure 30-8, except that the quantity added is always plus one (000001 is entered into register X whereas the counter content is entered into register Y). The largest octal number which can be stored in such a counter is +37777 (37777).
- b. The input counter which contains ONE's complement numbers to be diminished only (absolute value is decreased) is time counter 0031. Whenever this counter is addressed, an addition is performed as illustrated in the upper part of figure 30-8, except that the quantity added is minus one or plus one (177776 or 000001 is entered into register X whereas the counter content is entered into register Y).

- c. Input counters which contain ONE's complement numbers to be incremented and decremented are PIPA counters 0037 through 0041 and BMAG or RHC counters 0042 through 0044. Whenever such a counter is addressed, an addition is performed as illustrated in the upper part of figure 30-8, except that the quantity added is plus one or minus one (000001 or 177776 is entered into register X whereas the counter content is entered into register Y). The largest octal number which can be stored in such a counter is +37777 (37777); the smallest is -37777 (40000).
- d. Input counters which contain cyclic TWO's complement numbers which are incremented and decremented are CDU counters 0032 through 0036. Whenever such a counter is addressed, an addition is performed as illustrated in the lower part of figure 30-8. Control pulse RUS is used instead of control pulse RU to move the overflow bit into bit position 16 of register G (paragraphs 30-46 and 30-47). In reality, the angle 0° is represented by the octal quantity 00000 contained in a counter, 90° by 20000, 180° by 40000, and 270° (-90°) by 60000. Thus, 360° is equivalent to 2^{15} increments.
- e. Input counters which are used for serial to parallel conversion of incoming information are counters 0045 and 0046. Whenever such a counter is addressed and a ZERO has been received, the counter content is shifted left one position and entered into register Y by means of control pulse WYD, and 000000 is entered into register X. When a ONE has been received, the counter content is shifted one position to the left and 000001 is entered into register X. The addition is performed as indicated in the upper part of figure 30-8, with these exceptions: Bit 15 (overflow bit) of the sum is transferred to the counter instead of bit 16 (sign bit) and end-around carry is prevented.
- f. Output counters which are used to control the number of pulses in pulse bursts driving gyros, CDU's etc., are counters 0047 through 0056. Whenever such a counter is addressed, an addition is performed as illustrated in the upper part of figure 30-8, except that the quantity added is minus one or plus one (177776 or 000001 is entered into register X whereas the counter content is entered into Y).
- g. Output counters which are used for parallel to serial conversion of outgoing information are counters 0057 and 0060. When such a counter is addressed, the counter content is shifted left one position and entered into register Y by means of control pulse WYD.

(text continued on page 30-45)

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS

EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks \triangle
0010	ARUPT	Last content of register A is stored here during the execution of a RPT Transfer Routine.		
0011	LRUPT	Last content of register L is stored here during the execution of a RPT Transfer Routine.		
0012	QRUPT	Last content of register Q is stored here during the execution of a RPT Transfer Routine.		
0013		Spare		
0014		Spare		
0015	ZRUPT	Last content of register Z is stored here during the execution of instruction RUPT.		
0016	BBRUPT	Last content of registers EBANK and FBANK is stored here during the execution of a RPT Transfer Routine.		
0017	BRUPT	Last content of register B is stored here during the execution of instruction RUPT.		
0020	CYR	Quantity entered here has been cycled one place to the right by register G.		
0021	SR	Quantity entered here has been shifted one place to the right by register G.		
0022	CYL	Quantity entered here has been cycled one place to the left by register G.		
0023	EDOP	Quantity entered here has been cycled seven places to the right by register G.		
0024	T2	T2P from Sequence Generator	PINC T2	Main Time Counter T2 stores the high order part of reference (clock) time and Main Time Counter T1 stores the low order part. Both counters are preset by program. (Text continued on the next page)
0025	T1	T1P from Timer		

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)


EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks 
0024 0025 (cont)	T2 T1	T2P from Sequence Generator T1P from Timer	PINC T2	Signal TIP is generated every 10 msec and requests the execution of instruction PINC T1. Each time PINC T1 is executed, the content of T1 is incremented by one. Whenever counter T1 overflows (every 163.84 sec), signal T2P is generated which requests the execution of instruction PINC T2. Each time PINC T2 is executed, the content of T2 is incremented by one. (Counter T2 overflows approximately every 31st day.)
0026	T3	T3P from Timer	PINC T3	Time Counter T3 controls the operation of program section Waitlister (Task Control). The counter is preset by the Waitlister. Signal T3P is generated every 10 msec and requests the execution of instruction PINC T3. Each time PINC T3 is executed, the content of T3 is incremented by one. Upon overflow, the Interrupt Priority Control is triggered to initiate the execution of routine T3RUPT of program section Waitlister.

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)


EMA Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks 
0027 T4	T4P from Timer	PINC T4	Time Counter T4 controls the operation of program section T4RUPT Output Control. The counter is preset by this program section. Signal T4P is generated every 10 msec and requests the execution of instruction PINC T4. Each time PINC T4 is executed, the content of T4 is incremented by one. Upon overflow, the Interrupt Priority Control is triggered to initiate the execution of routine T4RUPT of program section T4RUPT Output Control.
0030 T5	T5P from Timer	PINC T5	Time Counter T5 controls the operation of program section Thrust Vector Control. The counter is preset by program. Signal T5P is generated every 10 msec and requests the execution of instruction PINC T5. Each time PINC T5 is executed, the content of T5 is incremented by one. Upon overflow, the Interrupt Priority Control is triggered to initiate the execution of program section Thrust Vector Control.

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)

EMA	Initials	Signal Entered into Counter Priority Control $\triangle 1$	Instruction Executed	Remarks $\triangle 2$
0031	T6	T6P from Timer	PINC T6	Time Counter T6 controls the operation of program section Reaction Control. The counter is preset by program. Signal T6P is generated every 625 μ sec if bit position 15 of output channel 13 contains a ONE and requests the execution of instruction DINC T6. Each time DINC T6 is executed, the content of T6 is diminished by one. When the content reaches zero, the Interrupt Priority Control is triggered to initiate the execution of program section Reaction Control.
0032	XCDU	CDUXP (118)	PCDU XCDU	These input counters store IMU CDU (inertial measurement units coupling display unit) and Optics CDU information. All information is angular and stored in cyclic TWO's complement numbers. The counters are set to zero by program when the CDU's are zeroed. The signals entered into the Counter Priority Control are received from the X, Y, and Z IMU CDU, and from the trunnion and shaft Optics CDU. All signals are incremental pulses which request the execution of certain instructions as listed at the left. The PCDU and MCDU instructions increment and decrement counter contents by one.
0033	YCDU	CDUXM (119)	MCDU XCDU	
		CDUYM (121)	PCDU YCDU	
0034	ZCDU	CDUZP (122)	MCDU YCDU	
		CDUZM (123)	PCDU ZCDU	
0035	TCDU	TRNP (110)	MCDU ZCDU	
		TRNM (111)	PCDU TCDU	
0036	SCDU	SHAFTP (108)	MCDU TCDU	
		SHAFTM (109)	PCDU SCDU	
			MCDU SCDU	

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)

EMA	Initials	Signal Entered into Counter $\triangle 1$ Priority Control	Instruction Executed	Remarks $\triangle 2$
0037 0040 0041	XPIPA YPIPA ZPIPA	PIPXP (132) PIPXM (133) PIPYP (134) PIPYM (135) PIPZP (136) PIPZM (137)	PINC XPIPA MINC XPIPA PINC YPIPA MINC YPIPA PINC ZPIPA MINC ZPIPA	These input counters store PIPA (pulse integrating pendulous accelerometer) information. The counters are set to zero by program at zero acceleration. The signals entered into the Counter Priority Control are received from the X, Y, and Z PIPA's. All signals are incremental pulses which request the execution of certain instructions as listed at the left. The PINC and MINC instructions increment and decrement counter contents by one.
0042 0043 0044	XBMAG YBMAG ZBMAG	BMAGXP BMAGXM BMAGYP BMAGYM BMAGZP BMAGZM	PINC XBMAG MINC XBMAG PINC YBMAG MINC YBMAG PINC ZBMAG MINC ZBMAG	In the CM, these input counters store BMAG (body mounted acceleration gyros) information if bit position 8 of output channel 13 contains a ONE. In the LEM these input counters store RHC (rotational hand controller) information if bit positions 8 and 9 of channel 13 contain ONE's. The counters are set to zero by program. The BMAG/RHC Control gates the incremental pulses received from either the BMAG's (signals 817 through 822), or the PHC Converter into the Counter Priority Control. The pulses entered into the Counter Priority Control request the execution of certain instructions shown at the left. The PINC and MINC instructions increment or decrement counter contents by one.

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)

EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks \triangle
0045	INLNK	INLNKM INLNKP	SHINC INLNK SHANC INLNK	<p>This input counter is used to convert incoming serial uplink or crosslink data into parallel information. If bit position 5 of output channel 13 contains a ZERO, uplink information is stored. If the bit position contains a ONE, crosslink information is stored. The Inlink Control gates either the uplink data (signals 024 and 025) or the crosslink data (signals 080 and 081) into the Counter Priority Control. The pulses entered into the Counter Priority Control request the execution of certain instructions as listed at the left. The SHINC instructions shift the content of a counter one place to the left and enter a ZERO into bit position 1. The SHANC instructions also shift the content one place to the left and enter a ONE into bit position 1. When the flag bit (first bit) of an uplink word (first bit is always a ONE) moves into bit position 16 of the Adder, the Interrupt Priority Control is triggered to initiate the execution of program section UPRUPT.</p>

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)


EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks 
0046	RADAR	RNRADM RNRADP	SHINC RADAR SHANC RADAR	This input counter is used to convert incoming serial rendezvous radar data (CM and LEM) or landing radar data (LEM only) into parallel information. The Radar Control gates either the rendezvous radar data (signals 031 and 032) or the landing radar data (signals 071 and 072) into the Counter Priority Control. The pulses entered into the Counter Priority Control request the execution of certain instructions, as shown at the left. The SHINC instruction shifts the content of a counter one place to the left and enters a ZERO into bit position 1. The SHANC instruction also shifts the content one place to the left and enters a ONE into bit position 1.
0047	GYROS	GYROD	DINC GYROS	This output counter is used to control pulse bursts driving the X, Y, and Z gyros. This output counter is used to control pulse bursts driving the X, Y, and Z gyros. The counter is preset by program section T4RUPT Output Control. Whenever the Gyro Drive Control sends a drive signal to the Counter Priority Control, the execution of instruction DINC GYROS is requested. Each time DINC GYROS is executed, the content of GYROS is (cont next page)

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)

EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks \triangle
0047 (cont)	GYROS	GYROD	DINC GYROS	diminished by one and a related drive pulse (signals 142 through 147) is transmitted if counter GYROS did not contain zero before the execution of DINC GYROS. If the counter contained zero, Gyro Drive Control is reset to stop further transmission of drive pulses related to this counter.
0050 0051 0052 0053 0054	XCDUCOM YCDUCOM ZCDUGOM TCDUCOM SCDUCOM	CDUXD CDUYD CDUZD TRUND SHAFTD	DINC XCDUCOM DINC YCDUCOM DINC ZCDUCOM DINC TCDUCOM DINC SCDUCOM	These output counters are used to control pulse bursts driving the IMU CDU's and the Optics CDU's. The counters are preset by program section T4RUPT Output Control. Whenever the CDU Drive Control sends a drive signal to the Counter Priority Control, the execution of a certain instruction is requested as shown at the left. Each time a DINC instruction is executed, the content of the addressed counter is diminished by one and a related drive pulse (signals 126 through 131 and 114 through 117) is transmitted if the respective counter did not contain zero before the execution of the DINC instruction. If the counter contained zero, the CDU Drive Control is reset to stop further transmission of drive pulses related to that counter.

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)


EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks 
0055	THRUST	THRSTD	DINC THRUST	Output counter THRUST is used to control pulse bursts driving the Thrust Control of the LEM. Output counter EMS is used to control pulse bursts driving the EMS (entry monitor system) of the CM or the LEM monitor. The counters are preset by program. Whenever the EMS and Thrust Drive Control sends a signal to the Counter Priority Control, the execution of a certain instruction is requested as shown at the left. Each time a DINC instruction is executed, the content of the addressed counter is diminished by one and a related drive pulse is transmitted if the respective counter did not contain zero before the execution of the DIM instruction. If the counter contained zero, the Drive Control is reset to zero to stop further transmission of drive pulses related to that counter.
0056	EMS	EMSD	DINC EMS	

TABLE 30-4

E LOCATION ASSIGNMENTS AND COUNTER OPERATIONS (cont)

EMA	Initials	Signal Entered into Counter Priority Control	Instruction Executed	Remarks [△] ₂
0057	OUTLNK	OTLNKM	SHINC OUTLNK	<p>These output counters are used to convert parallel outlink information (CM and LEM) or altitude information (LEM only) into serial data. Outlink or altitude words are entered into a counter by program. Whenever the Outlink Control, or the Altitude Meter Control, sends a signal to the Counter Priority Control, the execution of a certain instruction is requested. When a SHINC instruction is executed, the content of the addressed counter is shifted one place to the left. Each time a ZERO is shifted out, a ZERO is transmitted by the Output Control or the Altitude Meter Control; each time a ONE is shifted out, a ONE is transmitted.</p> <p style="text-align: center;"><u>Output Signals Generated</u></p> <p>A ZERO shifted out of counter OUTLINK: Signal 078</p> <p>A ONE shifted out of counter OUTLINK: Signal 079</p> <p>A ZERO shifted out of counter ALT: Signal 003 or 012</p> <p>A ONE shifted out of counter ALT: Signal 002 or 010</p>
0060	ALT	ALTM	SHINC ALT	

[△]₁ Numbers in () refer to signals listed in Appendices A and B

[△]₂ Refer also to figure 30-6.

Also, 00000 is entered into register X. The addition is performed as indicated in the upper part of figure 30-8, except that bit 15 (overflow bit) of the sum is transferred to the counter instead of bit 16 (sign bit), and that end-around carry is prevented.

30-67. INPUT-OUTPUT CONTROL

30-68. The Input-Output Control consists of various input and output channels, and a number of special circuits (figure 30-6). The output channels are flip-flop registers similar to those of the Central Processor (CP); their contents can be read back into the Write Amplifiers (WA's) and they supply binary DC signals which control either relays in the DSKY's, equipment outside the AGC subsystem, the special circuits within the Input-Output Control, or the Stand-by or the Alarm Control. The DSKY relays in turn control various displays on the DSKY's or generate DC signals controlling other G&N subsystems and spacecraft systems. Two input channels are also flip-flop registers and accept binary DC signals from the DSKY's and the Optics mark button. The other input registers are banks of gates which accept binary DC signals from various G&N subsystems and spacecraft systems.

30-69. The CDU Drive Control, the Gyro Drive Control, and the EMS and Thrust Drive Control generate signals controlling and driving the CDU's, the Gyros, the EMS (entry monitor system) of the CM or the LEM monitor, and the LEM thrust control. The Radar Control generates pulse trains controlling the radars and accepts serial data from the rendezvous and the landing radar to convert it to parallel information which is stored in counter RADAR (0046). The BMAG/RHC Control accepts either incremental pulses from the BMAG's (body mounted acceleration gyros) or the RHC (rotation hand control) Converter and stores it in the BMAG counters (0042 through 0044).

30-70. The Inlink Control accepts serial data from the Uplink or Crosslink equipment and converts it to parallel information which is stored in counter INLNK (0045). The Outlink Control converts parallel information contained in counter OUTLNK (0057) to serial data which is transmitted to the Crosslink equipment. The Altitude Meter Control converts parallel information contained in counter ALT (0060) to serial data which is transmitted to the altitude monitor. The Downlink Converter converts parallel information contained in output channels 34 and 35 to serial data which is sent to the NA programmer. The NA programmer collects telemetry data from various spacecraft systems and arranges it for downlink transmission.

30-71. Seven different Channel (Input-Output) Instructions, a group of Regular Machine Instructions, are provided to transfer information from register A in the CP to an output channel, or vice versa, or from an input channel to register A. Such information flow occurs via the WA's and is also under the

control of the Sequence Generator (SQG). Information which is transferred from register A to a channel is transferred to corresponding bit positions, except for the content of bit position 16 of register A which is always transferred to bit position 15 of an addressed channel if this bit position exists. The content of bit position 15 of register A is never transferred to a channel. Information which is transferred from a channel to register A is also transferred to corresponding bit positions, except for the content of bit position 15 of an addressed channel which is always transferred to bit positions 16 and 15 of register A.

30-72. The main difference between Channel Instructions and other Regular Instructions is the fact that the relevant address of a Channel Instruction always refers to an input/output channel whereas the relevant address of any other Regular Instruction refers to a CP register or a memory location. The relevant address of any Regular Instruction is entered into register S during execution of the instruction and the SQG decides whether to use it as a CP/Memory or a channel address. Channel Instructions can transfer information either wholly or in part, in either direction, between a channel and register A.

30-73. Table 30-5 defines all the input/output channels. There are no channels occupying channel addresses 00 through 02. Channel addresses 01 and 02 can be used to address CP registers L and Q by means of a Channel Instruction. Thus, registers L and Q can be read out and written into from register A like any input/output channel. Addresses 03 and 04 are used to address Scalers 2 and 1, respectively, thus allowing the transfer of time information from the Timer to the CP (paragraph 30-20).

30-74. Channel FEXT, address 07, is used for addressing F Memory as described in paragraphs 30-57 and 30-61. Presently, only bit position 7 is used for addressing while two additional bit positions are provided for increasing the addressing capability.

30-75. OUTPUT CHANNELS

30-76. Output channels 05 and 06, each consisting of eight bit positions (flip-flops), supply DC signals to control the reaction control system (outside the AGC) which in turn controls the reaction control jets. Refer to table 30-5H.

30-77. All fifteen bit positions (flip-flops) of output channel 10 are used to simultaneously control identical relay matrices in each DSKY. Each relay matrix consists of thirteen banks (octal 00 through 14) of up to eleven latching relays each. Bits 15 through 12 of channel 10 select a relay bank in each DSKY for resetting while bits 11 through 1 reset the relays of the selected bank. Relay banks 00 through 10 control the three 5-digit data displays on

TABLE 30-5
INPUT-OUTPUT CHANNELS Δ

Octal Address	Name or Contents	Bit Positions																							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1									
01	L	CP register L, bit positions 16 through 1																							
02	Q	CP register Q, bit positions 16 through 1																							
03	SCALER2	High-order scaler channel, 14 bit positions																							
04	SCALER1	Low-order scaler channel, 14 bit positions																							
05	Outbits, Reaction Control System										Δ_9 (804)	Δ_9 (807)	Δ_9 (808)	Δ_9 (803)	Δ_9 (802)	Δ_9 (805)	Δ_9 (806)	Δ_9 (801)							
06	Outbits, Reaction Control System										Δ_9 (810)	Δ_9 (811)	Δ_9 (812)	Δ_9 (809)	Δ_9 (814)	Δ_9 (815)	Δ_9 (816)	Δ_9 (813)							
07	FEXT (Fixed Extension)										E7/	E6	E5												
10	Outbits DSKY R Relays	RYWD16 (228)	RYWD14 (227)	RYWD13 (226)	RYWD12 (225)	RLYB11 (224)	RLYB10 (223)	RLYB09 (222)	RLYB08 (221)	RLYB07 (220)	RLYB06 (219)	RLYB05 (218)	RLYB04 (217)	RLYB03 (216)	RLYB02 (215)	RLYB01 (214)									
11	Outbits DSKY A Relays	OT1116 Spare (855)	OT1114 Spare (854)	OT1113 Spare (853)	OT1112 Spare (852)	OT1111 Spare (851)	Δ_{14} (850)	Spare (848)	OPEROR (244)	VNFLSH (238)	KYRLS (236)	TMPOUT (258)	UPLACT (235)	COMACT (230)	ISSWAR (229)										
12	Outbits GN&C	ISSTDC (909)	Δ_2 (234)	Δ_2 (233)	Δ_2 (841)	Δ_2 (902)	Δ_2 (906)	Δ_2 (160)	Δ_2 (161)	ENON (011)	ENERIM (196)	ZIMCDU (195)	COARSE (194)	STARON (162)	ENEROP (186)	ZOPCDU (185)									
13	Outbits, AGC	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3	Δ_3							
14	Outbits, gyro and CDU Drives	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4	Δ_4							
15	Inbits, Main Panel Keyboard																	TRAP15, RUPT5 MKEY5 (257)	MKEY4 (256)	MKEY3 (255)	MKEY2 (254)	MKEY1 (253)			
16	Inbits, Nav. Panel Keyboard																		TRAP16B, RUPT6 MRKREJ (102)	MARK (102)	NKEY5 (205)	NKEY4 (204)	NKEY3 (203)	NKEY2 (202)	NKEY1 (201)
30	Inbits, GN&C	Δ_5 (125)	Δ_5 (113)	Δ_5 (141)	Δ_5 (124)	Δ_5 (193)	Δ_5 (158)	Δ_5 (184)	IN3008 Spare (084)	OPCDFL (112)	GUIREL (068)	LFTOFF (007)	S4BSAB (066)	SPSRDY (082)	SMSEPR (067)	ULLTHR (004)									
31	Inbits, Translation and Rotation	GCAPCL (159)	FREFUN (065)	HOLFUN (040)	TRAP31B, RUPT10 TRAN-Z (023)				TRAN+Z (022)	TRAN-Y (021)	TRAN+Y (020)	TRAN-X (019)	TRAN+X (018)	MANR-R (098)	MANR+R (097)	MANR-Y (096)	MANR+Y (095)	MANR-P (094)	MANR+P (093)						
32	Inbits, Impulse	IN3216 Spare (845)	IN3214 Spare (844)	IN3213 Spare (034)	IN3212 Spare (033)	LEMATT (060)	TRAP32, RUPT10 ROLGOF (843)				PCHGOF (842)	TRST10 (832)	TRST9 (831)	MNIM-R (189)	MNIM+R (188)	MNIM-Y (174)	MNIM+Y (173)	MNIM-P (172)	MNIM+P (171)						
33	Inbits, Optics and AGC	Δ_8 Δ_{11}	Δ_8 Δ_{11}	Δ_8 Δ_{11}	Δ_8 Δ_{12}	Δ_8 Δ_{13}			Δ_8 (083)	Δ_8 (061)	Δ_8 (039)	Δ_8 (183)	Δ_8 (107)	Δ_8 (106)	Δ_8 (104)	Δ_8 (069)	Δ_8 (064)	Δ_8 (064)	Spare (840)						
34	Downlink Bits	16 bit positions																							
35	Downlink Bits	16 bit positions																							

- Δ_1 Signal names taken from NASA drawings 2005066 through 2005073. Numbers in () refer to signals listed in Appendices A and B.
- Δ_2 Refer to table 30-5A
- Δ_3 Refer to table 30-5B
- Δ_4 Refer to table 30-5C
- Δ_5 Refer to table 30-5D
- Δ_6 Refer to table 30-5E
- Δ_7 Refer to table 30-5F
- Δ_8 Refer to table 30-5G
- Δ_9 Refer to table 30-5H
- Δ_{10} Refer to table 30-5I
- Δ_{11} Signal supplied by Alarm Control
- Δ_{12} Signal supplied by Inlink Control
- Δ_{13} Signal supplied by Downlink Converter
- Δ_{14} Also generates signal W1110 which controls the restart flip-flop in the start-stop logic

the DSKY's. Banks 11 through 13 control the 2-digit NOUN, VERB, and PROGRAM display, respectively (figure 30-4). Seven relays of bank 14 control seven of the status and caution indicators on the DSKY's (AUTO, HOLD, FREE, NO ATT, GIMBAL LOCK, PROG, and TRACKER).

30-78. Bit positions 1 through 7 (flip-flops) of output channel 11 control seven non-latched relays in the DSKY's. The relays which are controlled by signals COMACT, UPLACT, TMPCAU, KYRLS, and OPEROR control five other status and caution indicators on the DSKY's (COMP ACTY, UPLINK ACTY, TEMP, KEY REL, and OPR ERR, respectively). Signal TMPCAU is generated by "ORing" signals TMPOUT and TEMPIN/. The relay controlled by signal VNFLSH controls the VERB-NOUN flash control, and the relay controlled by signal ISSWAR generates ISS warning signals which are transmitted to various G&N subsystem and spacecraft caution indicators.

30-79. Bit positions 1 through 14 (flip-flops) of output channel 12 provide DC signals controlling various G&N subsystems and the SIVB engine. Refer to table 30-5A.

30-80. Bit positions 1 through 15 (flip-flops) of output channel 13 provide DC signals which control various areas of the AGC. Bit positions 1 through 3 control the radar mode selection and bit position 4 controls another part of the Radar Control. Refer to table 30-5B. Bit positions 5 and 6 control the Inlink Control. Bit position 7 controls the Downlink Converter. Bit positions 8 and 9 control the BMAG/RHC Control. Bit position 10 controls the Alarm Control and bit position 11 the Standby Control. Bit positions 12 through 15 control the Interrupt Priority Control.

30-81. Bit positions 1 through 15 (flip-flops) of output channel 14 also provide DC signals which control various parts of the AGC. Bit position 1 controls the Outlink Control. Refer to table 30-5C. Bit positions 2 and 3 control the Altitude Meter Control, and bit positions 4 and 5 the EMS and Thrust Drive Control. Bit positions 6 through 10 control the Gyro Drive Control and bit positions 11 through 15 the CDU Drive Control.

30-82. Output channels 34 and 35 (flip-flops) provide 16 bit words including a parity bit to the Downlink Converter for downlink transmission.

30-83. INPUT CHANNELS

30-84. In the CM bit positions 1 through 5 (flip-flops) of channel 15 accept five different DC signals from the main panel DSKY keyboard. Bit positions 1 through 5 (flip-flops) of channel 16 accept similar signals from the keyboard of the navigation panel DSKY. Bit positions 6 and 7 (flip-flops) of channel 16 accept two different DC signals from the Optics mark buttons. Any of the

(text continued on page 30-60)

TABLE 30-5A
OUTPUT CHANNEL 12

Bit Position	Channel Output Signal ^①	Purpose in CM	Purpose in LEM
1	ZOPCDU (185)	zero Optics CDU	zero rendezvous radar CDU
2	ENEROP (186)	enable Optics error counter	enable rendezvous radar counter
3	STARON (162)	enable star tracker	use low scale factor for horizon velocity
4	COARSE (194)	enable coarse alignment	same as in CM
5	ZIMCDU (195)	zero IMU CDU's	same as in CM
6	ENERIM (196)	enable IMU error counter	same as in CM
7	ENON (011) ^② ENOFF (013)	turn SPS engine on not used	turn engine on turn engine off
8	TVCNAB (161)	enable SIVB engine thrust vector control	display inertial data
9	S4BTAK (160)	enable SIVB take over	trim plus pitch gimbal
10	ZEROPT (906)	zero Optics	trim minus pitch gimbal
11	DISDAC (902)	disengage Optics DAC	trim plus roll pitch gimbal
12	MROLGT (841)	not used	trim minus roll pitch gimbal
13	S4BSEQ (233)	enable SIV start sequence	except landing radar position command
14	S4BOFF (234)	cutoff SIV engine	enable rendezvous radar lock on
15	ISSTDC (909)	ISS turn on delay completed	same as in CM

① Numbers in () refer to signals listed in Appendices A and B.

② If bit position contains a ONE, signal ENON is generated
If bit position contains a ZERO, signal ENOFF is generated.

TABLE 30-5B
OUTPUT CHANNEL 13

Bit Position	Purpose in CM	Purpose in LEM
1	radar mode selection c	} same as in CM
2	radar mode selection b	
3	radar mode selection a	
4	transmit a control signal to radar	
Selection Bits a b c		Signals generated by Radar Control, used in LEM only
	0 0 0	none
	0 0 1	RRRANG (041), supply rendezvous radar range data
	0 1 0	RRRARA (042), supply rendezvous radar range rate
	0 1 1	none
	1 0 0	LRXVEL (043), supply landing radar X velocity data
	1 0 1	LRYVEL (044), supply landing radar Y velocity data
	1 1 0	LRZVEL (045), supply landing radar Z velocity data
	1 1 1	LRRANG (046), supply landing radar range data
5	inhibit uplink, enable crosslink	} same as in CM
6	block inlink	
7	downlink order bit	
8	enable BMAG counter	enable RHC counter
9	not used	start RHC read
10	test alarm	} same as in CM
11	enable standby	
12	reset trap 31-A	
13	reset trap 31-B	
14	reset trap 32	
15	enable T6RUPT	

△ Numbers in () refer to signals listed in Appendices A and B.

TABLE 30-5C
OUTPUT CHANNEL 14

Bit Position	Purpose in CM	Purpose in LEM
1	transmit one outlink word	same as in CM
2	not used	altitude rate selection
3	not used	transmit one altitude meter word
4	not used	drive thrust
5	drive EMS	drive monitor
6	enable gyro	} same as in CM
7	gyro selection b	
8	gyro selection a	
9	gyro selection c (minus sign)	
10	drive gyro	
Selection Bits c a b		Signals Generated by Gyro Drive Control ^①
0 0 0		none
1 0 0		none
0 0 1		GYXP (142), drive X gyro positive
1 0 1		GYXM (143), drive X gyro negative
0 1 0		GYYP (144), drive Y gyro positive
1 1 0		GYYM (145), drive Y gyro negative
0 1 1		GYZP (146), drive Z gyro positive
1 1 1		GYZM (147), drive Z gyro negative
11	drive Optics CDU S	} same as in CM
12	drive Optics CDU T	
13	drive IMU CDU Z	
14	drive IMU CDU Y	
15	drive IMU CDU X	

① Numbers in () indicate related interface signals listed in Appendices A and B.

TABLE 30-5D
INPUT CHANNEL 30

Bit Position	¹ Channel Input Signal	Indication in CM	Indication in LEM
1	ULLTHR (004)	ullage thrust present	abort
2	SMSEPR (067)	service model separation	stage verification
3	SPSRDY (082)	SPS ready	engine armed
4	S4BSAB (066)	SIVB separation	stage abort
5	LFTOFF (007)	lift off SIVB	horizon velocity low scale
6	GUIREL (068)	guidance reference release	inertial data display
7	OPCDFL (112)	Optics CDU fail	rendezvous radar CDU fail
8	IN3008	spare	spare
9	IMUOPR (184)	IMU operates	same as in CM
10	CTLSAT (158)	Saturn control	four jet selection
11	IMUCAG (193)	IMU caged	} same as in CM
12	CDUFAL (124)	IMU CDU fail	
13	IMUFAL (141)	IMU fail	
14	ISSTOR (113)	ISS turned on request	
15	TEMPIN (125)	temperature within limits	

¹ Numbers in () refer to signals listed in Appendices A and B.

TABLE 30-5E
INPUT CHANNEL 31

Bit Position	Channel ¹ Input Signal	Indication in CM	Indication in LEM
1	MANR+P (093)	+pitch command from manual rotation control	} not used
2	MANR-P (094)	-pitch command from manual rotation control	
3	MANR+Y (095)	+yaw command from manual rotation control	} attitude control out of detention
4	MANR-Y (096)	-yaw command from manual rotation control	
5	MANR+Z (097)	+roll command from manual rotation control	} not used
6	MANR-Z (098)	-roll command from manual rotation control	
7	TRAN+X (018)	+X translation command from manual translation control	} same as in CM
8	TRAN-X (019)	-X translation command from manual translation control	
9	TRAN+Y (020)	+Y translation command from manual translation control	
10	TRAN-Y (021)	-Y translation command from manual translation control	
11	TRAN+Z (022)	+Z translation command from manual translation control	
12	TRAN-Z (023)	-Z translation command from manual translation control	

TABLE 30-5E
INPUT CHANNEL 31 (cont)

Bit Position	Channel ¹ Input Signal	Indication in CM	Indication in LEM
13	HOLFUN (040)	hold function	auto stabilization
14	FREFUN (065)	free function	auto stabilization
15	GCAPCL (159)	guidance control, auto pilot control	G&N control

¹ Numbers in () refer to signals listed in Appendices A and B.

TABLE 30-5F
INPUT CHANNEL 32

Bit Position	Channel ¹ Input Signal	Indication in CM	Indication in LEM
1	MNIM+P (171)	+pitch minimum impulse	thruster 2-4 fail
2	MNIM-P (172)	-pitch minimum impulse	thruster 5-8 fail
3	MNIM+Y (173)	+yaw minimum impulse	thruster 1-3 fail
4	MNIM-Y (174)	-yaw minimum impulse	thruster 6-7 fail
5	MNIM+R (188)	+roll minimum impulse	thruster 14-16 fail
6	MNIM-R (189)	-roll minimum impulse	thruster 13-15 fail
7	TRST9 (831)	not used	thruster 9-12 fail
8	TRST10 (832)	not used	thruster 10-11 fail
9	PCHGOF (842)	not used	pitch gimbal off
10	ROLGOF (843)	not used	roll gimbal off
11	LEMATT (060)	LEM attached	altitude hold
12	IN3212 (033)	spare	spare
13	IN3213 (034)	spare	spare
14	IN3214 (844)	spare	spare
15	IN3216 (845)	spare	spare

¹ Numbers in () refer to signals listed in Appendices A and B.

TABLE 30-5G
INPUT CHANNEL 33

Bit Position	Channel ^① Input Signal	Indication in CM	Indication in LEM
1	-	spare	spare
2	RRPONA (064)	not used	rendezvous radar on automatic
3	RRRLSC (069)	not used	rendezvous radar on low scale
4	ZEROP (104)	zero optics	rendezvous radar data good
5	OPMSW2 (106)	AGC has control	landing radar data good
6	OPMSW3 (107)	star tracker on	landing radar in position 1 (descent)
7	STRPRS (183)	star present	landing radar in position 2 (hover)
8	LVDAGD (039)	not used	landing velocity data good
9	LRRLSC (061)	not used	landing radar on low scale
10	BLKUPL (083)	accept uplink data	} same as in CM
11	no name ^③	inlink too fast	
12	no name ^④	downlink too fast	
13	PIPAFL ^②	PIPA fail	
14	AGCWAR ^②	AGC warning	
15	OSCALM ^②	oscillator alarm	

① Numbers in () refer to signals listed in Appendices A and B.

② Signal is supplied by Alarm Control

③ Signal is supplied by Downlink Converter

④ Signal is supplied by Inlink Control

TABLE 30-5H
OUTPUT CHANNELS 05 AND 06

Bit Position	Channel Output Signal ^①	Purpose in CM ^② ^③	Purpose in LEM ^②
Channel 05			
1	RC + X + P (801)	# 1 RCS + X + P	# 1 RCS 4U
2	RC - X - P (806)	# 2 RCS - X - P	# 2 RCS 4D
3	RC - X + P (805)	# 5 RCS - X + P	# 5 RCS 3U
4	RC + X - P (802)	# 6 RCS + X - P	# 6 RCS 3D
5	RC + X + Y (803)	# 9 RCS + X + Y	# 9 RCS 2U
6	RC - X - Y (808)	#10 RCS - X - Y	#10 RCS 2D
7	RC - X + Y (807)	#13 RCS - X + Y	#13 RCS 1U
8	RC + X - Y (804)	#14 RCS + X - Y	#14 RCS 1D
Channel 06			
1	RC + Z + R (813)	# 7 RCS + Z + R	# 7 RCS 3F
2	RC - Z - R (816)	# 3 RCS - Z - R	# 3 RCS 4F
3	RC - Z + R (815)	#15 RCS - Z + R	#15 RCS 1F
4	RC + Z - R (814)	#11 RCS + Z - R	#11 RCS 2F
5	RC + Y + R (809)	#12 RCS + Y + R	#12 RCS 2S
6	RC - Y - R (812)	# 8 RCS - Y - R	# 8 RCS 3S
7	RC - Y + R (811)	# 4 RCS - Y + R	# 4 RCS 4S
8	RC + Y - R (810)	#16 RCS + Y - R	#16 RCS 1S

① Numbers in () refer to signals listed in Appendices A and B.

② RCS means Reaction Control System

③ P, Y, and R mean pitch, yaw, and roll, respectively.

TABLE 30-5J
INPUT CHANNEL 16

Bit Position	Channel Input Signal [△]	Indication in CM	Indication in LEM
1	NKEY1 (201)	KEY 1	—
2	NKEY2 (202)	KEY 2	—
3	NKEY3 (203)	KEY 3	MARK X MARK Y MARK REJECT
4	NKEY4 (204)	KEY 4	
5	NKEY5 (205)	KEY 5	
6	MARK (102)	MARK	DESCENT + DESCENT -
7	MRKREJ (182)	MARK REJECT	

from Navigation Panel DSKY

from Optics

from Optics

[△] Numbers in () refer to signals listed in Appendices A and B.

signals from the main panel DSKY sets TRAP15 and triggers the Interrupt Priority Control to initiate the execution of sequence RUPT5. Refer to tables 30-5 and 30-5J. Any of the signals from the navigation panel DSKY sets trap TRAP16A and any of the optics signals sets TRAP16B; all signals cause the Interrupt Priority Control to initiate the execution of sequence RUPT6. Input channel 15 serves the DSKY in the LEM the same way as the channel serves the main panel DSKY in the CM. Channel 16 has a different purpose in the LEM than in the CM.

30-85. Bit positions 1 through 15 (gates) of channel 30 accept DC signals from various G&N subsystems and spacecraft systems. Refer to table 30-5D. All incoming signals are inverted, i. e., the presence of a signal is indicated by zero volts and its absence by +28 volts.

30-86. Bit positions 1 through 15 (gates) of channel 31 accept DC signals from the manual rotation control, the manual translation command, etc. Refer to table 30-5E. Any signal fed into bit positions 1 through 6 sets TRAP31A and any signal entered into bit positions 7 through 12, TRAP31B; all these signals trigger the Interrupt Priority Control to initiate the execution of sequence RUPT10. All incoming signals are inverted.

30-87. Bit positions 1 through 11 (gates) of channel 32 accept DC signals from the minimum impulse control, thrust fail indications, etc. Refer to table 30-5F. Any signal entered into bit positions 1 through 10 sets TRAP32 and triggers the Interrupt Priority Control to initiate the execution of sequence RUPT10. All incoming signals are inverted.

30-88. Bit positions 2 through 9 (gates) of channel 33 accept various DC signals from the Optics and the radars. Refer to table 30-5G. Bit position 10 (a gate) accepts a DC signal from the UPTTEL switch. Bit positions 11 through 15 (flip-flops) accept information within the AGC. All incoming signals are inverted.

30-89. SPECIAL CIRCUITS

30-90. CDU Drive Control

30-91. The CDU Drive Control (figure 30-8A) is controlled by bit positions 11 through 15 of output channel 14 (table 30-5C) and the following signals which are supplied by the SQG during the execution of a DINC instruction:

POUT/	generate plus (P) drive pulse
MOUT/	generate minus (M) drive pulse
ZOUT/	generate no more drive pulses

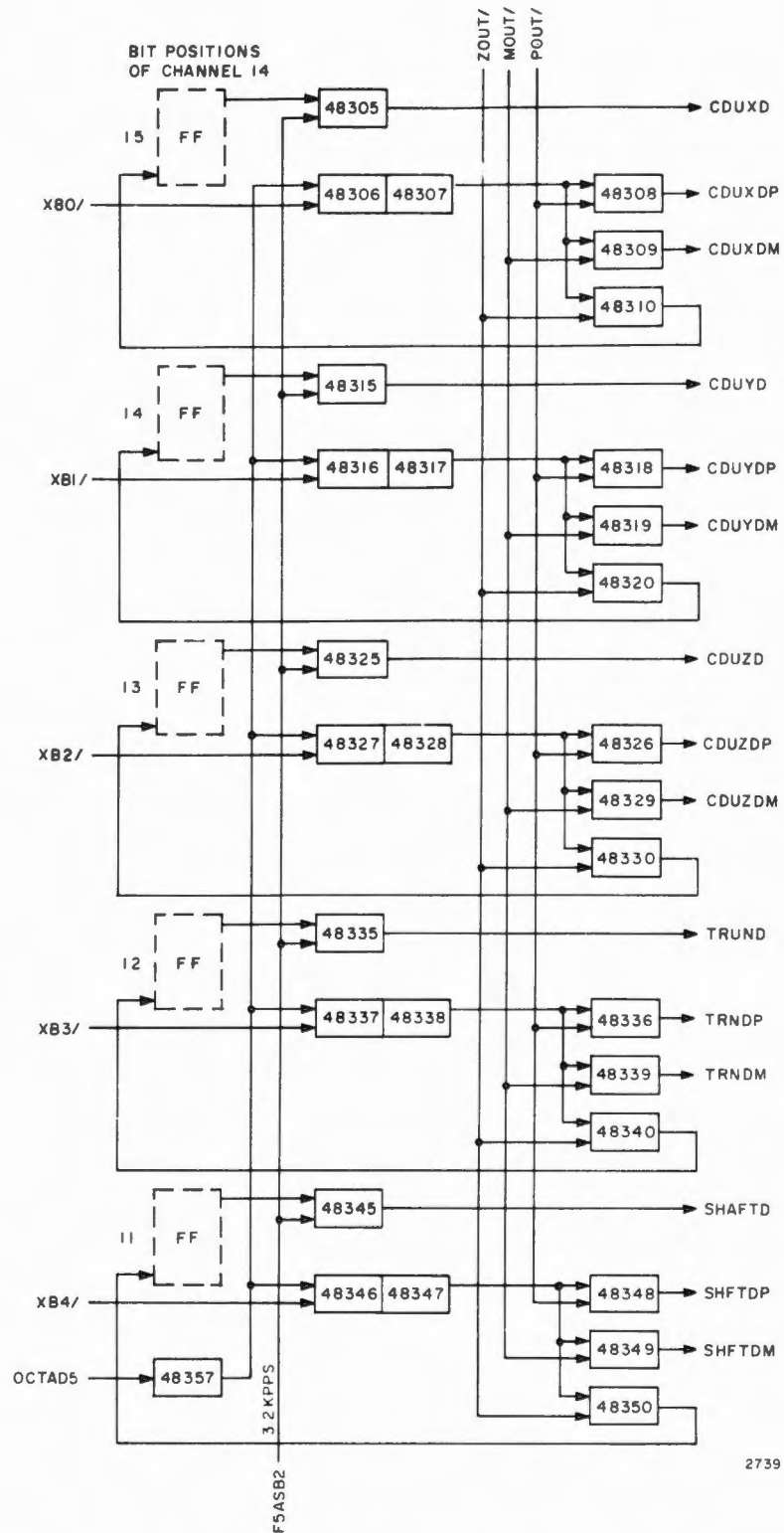


Figure 30-8A. CDU Drive Control

Signals XB0/ through XB4/ and signal OCTAD5 are provided by the address decoding logic when addresses 0050 through 0054 are contained in register S.

30-92. Depending on the inputs, the CDU Drive Control generates the following signals:

CDUXD	}	3.2 kpps signals entered into the Counter Priority Control to request the executions of DINC instructions (table 30-7)	
CDUYD			
CDUZD			
TRNDD			
SHAFTD			
CDUXDP (126)	}	pulses driving the CDU's	
CDUXDM (127)			drive X CDU positive
CDUYDP (128)			drive X CDU negative
CDUYDM (129)			drive Y CDU positive
CDUZDP (130)			drive Y CDU negative
CDUZDM (131)			drive Z CDU positive
TRNDP (114)			drive Z CDU negative
TRNDM (115)			drive T CDU positive
SHAFTDP (116)			drive T CDU negative
SHAFTDM (117)			drive S CDU positive
		drive S CDU negative	

30-93. Signal CDUXD is generated when bit position 15 of output channel 14 contains a ONE, signal CDUYD when position 14 contains a ONE, signal CDUZD when 13 contains a ONE, signal TRUND when 12 contains a ONE, and signal SHAFTD when bit position 11 contains a ONE. More than one of these signals can be generated simultaneously. The P and M signals (126 through 117 listed above) are generated under the control of the Counter Priority Control.

30-94. Once a desired quantity (for instance minus 432) has been entered into a CDUCOM counter (for instance counter XCDUCOM, table 30-4) and output channel 14 has been set properly (a ONE has been entered into bit position 15), the CDU Drive Control generates a corresponding D signal (CDUXD). The D signal sets cell 21 in the Counter Priority Control which then supplies the proper CDUCOM counter address (0050) and triggers the SQG to execute a DINC instruction (DINC XCDUCOM). As the instruction is executed, the cell is reset, an OUT/ signal is generated by the SQG (signal MOUT/ because XCDUCOM contains a negative quantity) and the counter content is diminished by one (to minus 431). A POUT/ or MOUT/ signal coincident with the decoded counter address (signals XB0/ and OCTAD5) causes the CDU Drive Control to release one P or M drive pulse respectively (CDUXDM in our example). Since the priority cell is set again by another D pulse (another CDUXD pulse), the execution of another DINC instruction is requested. This is repeated

until the counter content has diminished to zero. Once the counter contains zero and a DINC instruction is executed, signal ZOUT/ is generated which clears the proper bit position of channel 14 (bit position 15 in our example) thus stopping the transmission of drive pulses.

30-95. Gyro Drive Control

30-96. The Gyro Drive Control (figure 30-8B) is controlled by bit positions 6 through 10 of output channel 14 (table 30-5C) and the following signals which are supplied by the SQG during the execution of a DINC instruction:

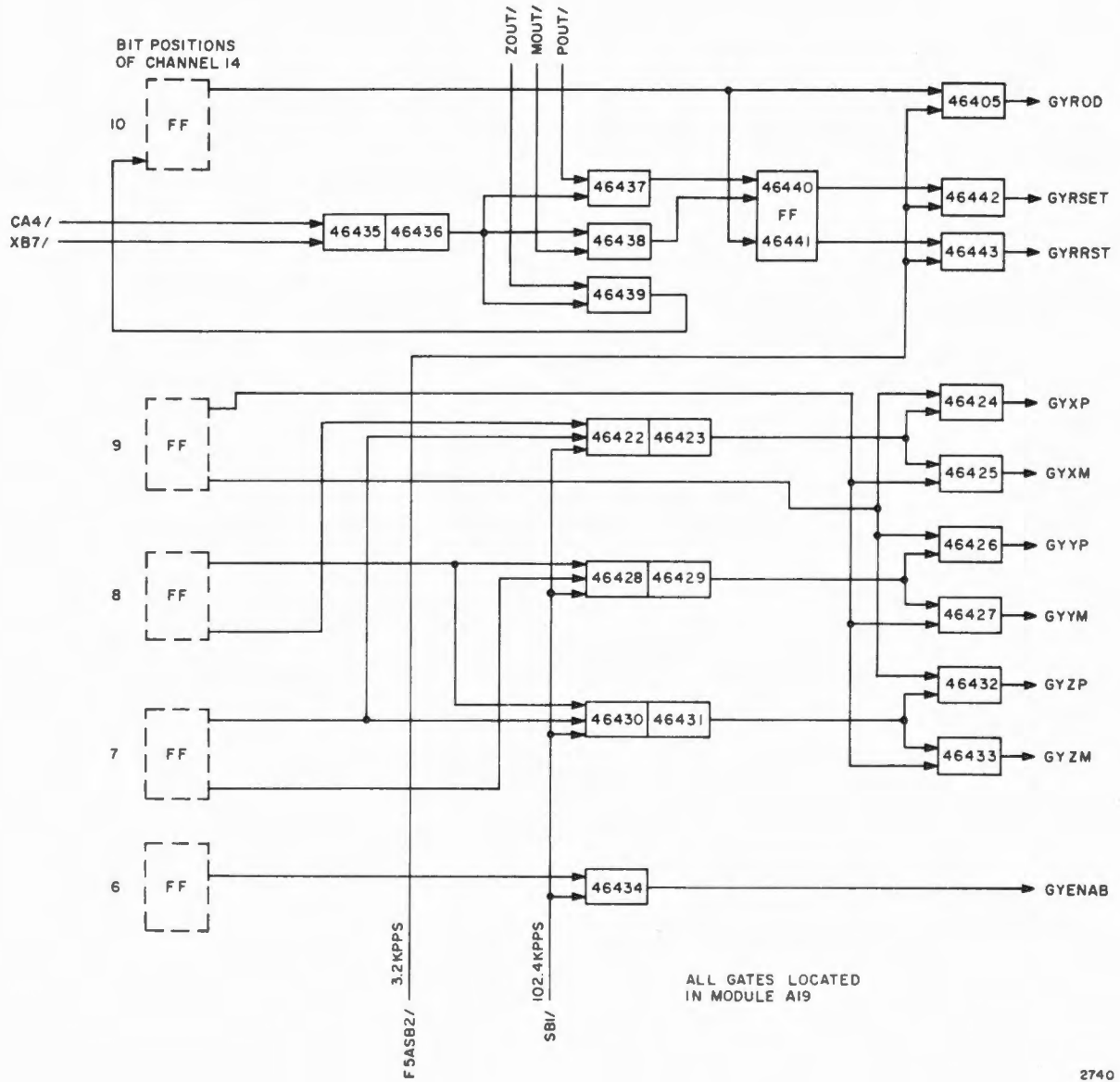
POUT/	generate plus (P) drive pulse
MOUT/	generate minus (M) drive pulse
ZOUT/	generate no more drive pulses

Signals XB7/ and CA4/ are provided by the address decoding logic when address 0047 is contained in register S.

30-97. Depending on the inputs, the Gyro Drive Control generates the following signals:

GYROD	3.2 kpps signal entered into the Counter Priority Control to request the executions of DINC instructions (table 30-7)
GYENAB (192) enable gyro	120 kpps pulse train
GYRRST (148) gyro reset } GYRSET (198) gyro set }	3.2 kpps pulse trains
GYXP (142) drive gyro X positive } GYXM (143) drive gyro X negative } GYYP (144) drive gyro Y positive } GYYM (145) drive gyro Y negative } GYZP (146) drive gyro Z positive } GYZM (147) drive gyro Z negative }	102 kpps pulse trains controlling the gyros

30-98. Signal GYROD is generated when bit position 10 of output channel 14 contains a ONE, and signal GYENAB when position 6 contains a ONE. The P and M signals (142 through 147) are generated according to the content of bit positions 7 through 9 as shown in table 30-5C. If the gyros are not driven (bit position 10 contains a ZERO), GYRRST pulses are transmitted at a rate of 3.2 kpps. When a ONE has been entered into bit position 10 (signal GYROD is transmitted), and a POUT/ or MOUT/ signal is received, the transmission of GYRRST pulses is interrupted and the transmission of GYRSET pulses is started. At the time bit position 10 is reset (contains ZERO, no POUT/ or



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Figure 30-8B. Gyro Drive Control

MOUT/ signals are generated), the transmission of GYRSET pulses is discontinued and the transmission of GYRRST pulses is continued.

30-99. Once the desired quantity (for instance plus 123) has been entered into counter GYROS (table 30-4) and output channel 14 has been set properly (for instance ONE's have been entered into bit positions 6, 7, 9, and 10), the Gyro Drive Control generates drive signal GYROD. This signal sets cell 20 in the Counter Priority Control which then supplies the address of counter GYROS (0047) and triggers the SQG to execute instruction DINC GYROS. As the instruction is executed, the cell is reset, an OUT signal is generated by the SQG (signal POUT/ because counter GYRO contains a positive quantity) and the Counter content is diminished by one (to plus 122). A POUT/ or a MOUT/ signal causes the Gyro Drive Control to generate GYRRST pulses in place of GYRSET pulses. Since the priority cell is set again by another GYROD pulse, the execution of another DINC instruction is requested. This is repeated until the counter content has diminished. Once the counter contains zero and a DINC instruction is executed, signal ZOUT/ is generated which clears bit position 10 of channel 14, thus stopping the transmission of drive pulses and starting again the transmission of GYRRST pulses.

30-100. EMS and Thrust Drive Control

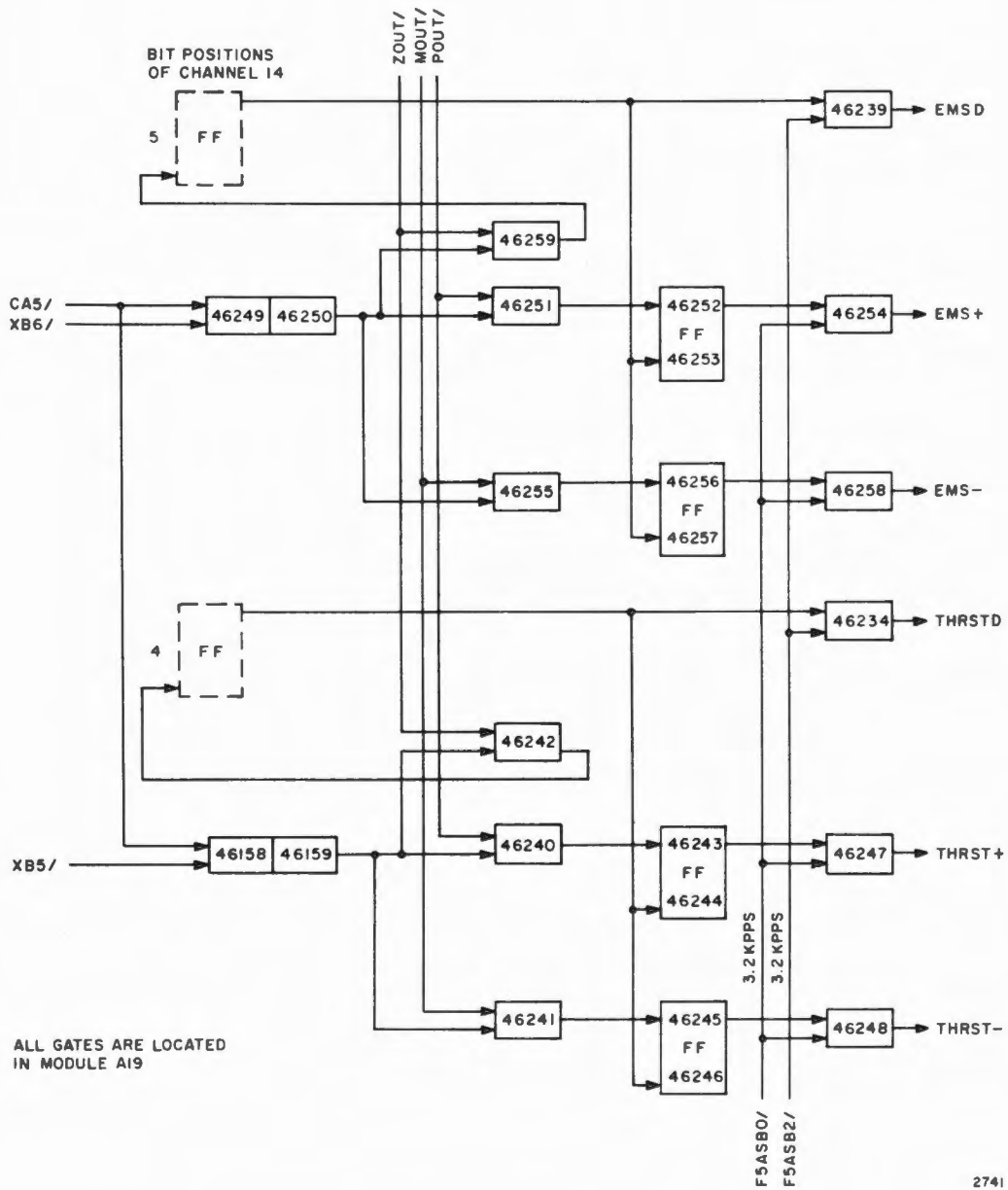
30-101. The EMS and Thrust Drive Control (figure 30-8C) is controlled by bit positions 4 and 5 of output channel 14 (table 30-5C) and the following signals which are supplied by the SQG during the execution of a DINC instruction:

POUT/	generate plus (P) drive pulse
MOUT/	generate minus (M) drive pulse
ZOUT/	generate no more drive pulses

Signals XB5/, XB6/, and CA5/ are provided by the address decoding logic when address 0055 or 0056 is contained in register S.

30-102. Depending on the inputs, the drive control generates the following signals:

THRSTD	}	3.2 kpps signals entered into the Counter Priority Control to request the executions of DINC instructions (table 30-7)	}	3.2 kpps pulse trains
EMSD				
THRUST+ (008)	drive thrust positive	}		
THRUST- (009)	drive thrust negative			
EMS+ (029)	drive EMS or LEM monitor positive			
EMS- (030)	drive EMS or LEM monitor negative			



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Figure 30-8C. EMS and Thrust Drive Control

30-103. Signal THRSTD is generated if bit position 4 of output channel 14 contains a ONE, and signal EMSD if position 5 contains a ONE. The + and - signals (008 through 030 above) are generated according to the content of the same two bit positions.

30-104. Once a desired quantity (for instance plus 246) has been entered into counter THRUST or EMS (counter THRUST for example, table 30-4) and output channel 14 has been set properly (a ONE has been entered into bit position 4), the drive control generates a corresponding D signal (THRSTD). The D signal sets cell 36 in the Counter Priority Control which then supplies the address of the proper counter (0055) and triggers the SQG to execute a DINC instruction (DINC THRUST). As the instruction is executed, the cell is reset, an OUT/ signal is generated by the SQG (POUT/ in the example), and the counter content is diminished by one (to plus 245). A POUT/ or MOUT/ signal causes the drive control to start transmitting + or - drive pulses (THRUST+) at a rate of 3.2 kpps. Since the priority cell is set again by another D signal, the execution of another DINC instruction is requested. This is repeated until the counter content has diminished. Once the counter contains zero and a DINC instruction is executed, signal ZOUT/ is generated which clears the proper bit position of channel 14, thus stopping the transmission of drive pulses.

30-105. Radar Control

30-106. The Radar Control (figure 30-8D) is controlled by bit positions 1 through 4 of output channel 13 (table 30-5B) and accepts the following signals from the radars:

RRIN0	(031)	} Serial data from rendezvous radar (RR)
RRIN1	(032)	
LRIN0	(071)	} Serial data from landing radar (LR), LEM only
LRIN1	(072)	

30-107. Depending on the inputs, the Radar Control generates the following signals:

RRRANG	(041)	supply RR range data	} 3.2 kpps pulse trains controlling the radars
RRRARA	(042)	supply RR range rate data	
LRRANG	(046)	supply LR range data	
LRXVEL	(043)	supply LR X velocity data	
LR YVEL	(044)	supply LR Y velocity data	
LRZVEL	(045)	supply LR Z velocity data	
RRSYNC	(047)	3.2 kpps sync pulses for read out of RR data	
LRSYNC	(051)	3.2 kpps sync pulses for read out of LR data	

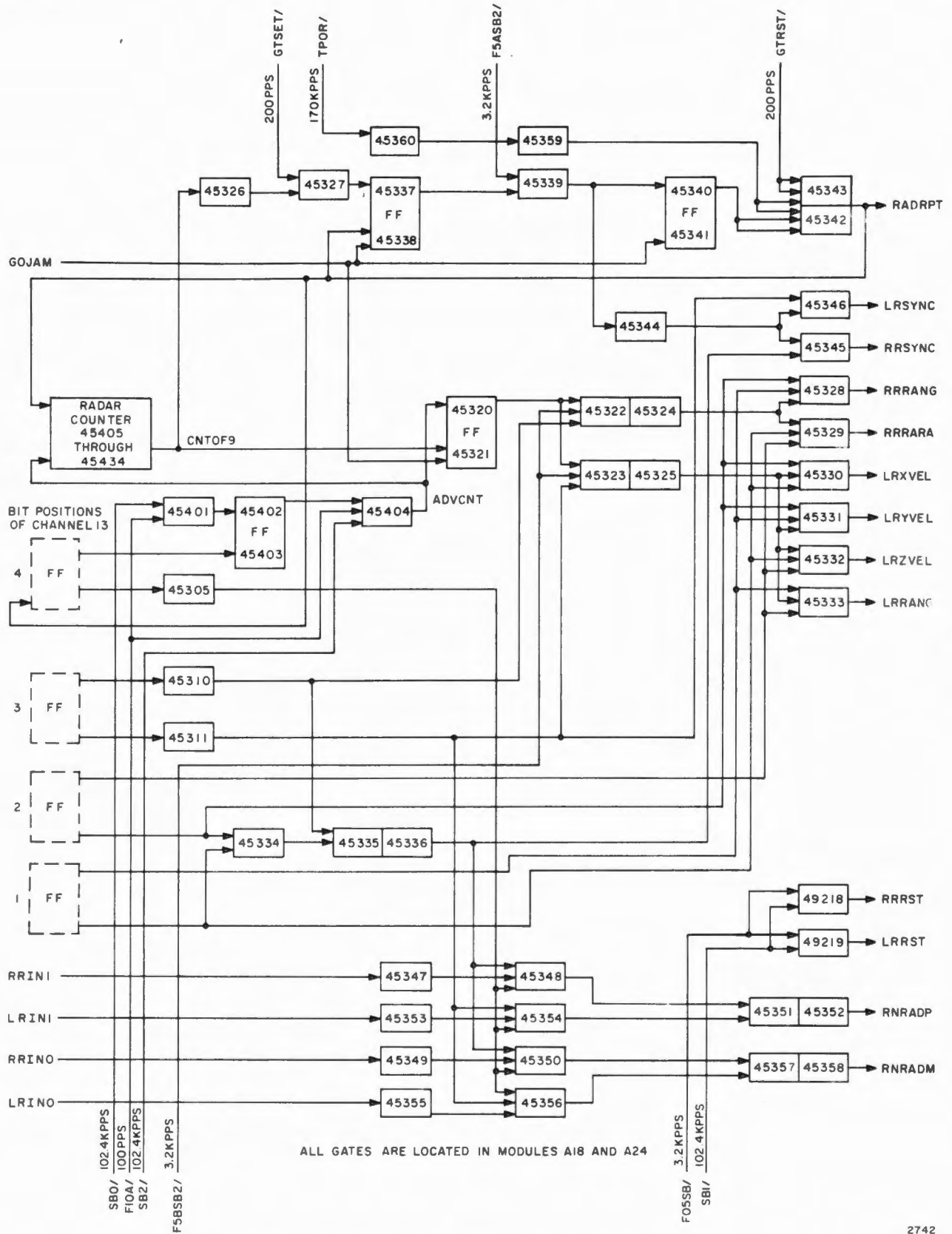


Figure 30-8D. Radar Control

RNRADM } Signals entered into the Counter Priority Control to
 RNRADP } request the execution of a SHINC or SHANC instruction
 (table 30-7)

RADRPT signal sent to Interrupt Priority Control (cell 9) to request
 the execution of sequence RUPT 9.

RRRST (048) }
 LRRST (052) } 3.2 kpps reset pulses sent to RR and LR

30-108. The contents of bit positions 1 through 3 of channel 13 defines which data is to be supplied by the radars (table 30-5B). They also define whether sync pulses are to be sent to the rendezvous radar or to the landing radar and from which radar serial data is to be accepted.

30-109. Once a ONE has been entered into bit position 4, together with the necessary selection bits in bit positions 1 through 3 (for instance, a ONE in bit position 1 only in order to request the rendezvous radar to transmit range data), the following sequence is started thereafter:

- a. Flip-flop 45402/45403 is set at occurrence of first F10A/ signal. As the flip-flop is set, gate 45404 generates signal ADVCNT which sets flip-flop 45320/45321. When this flip-flop has been set, either gate 45324 or 45325 starts to generate a 3.2 kpps bar signal dependent on the content of bit position 3. (In the given example, gate 45324.) The 3.2 kpps bar signal gates either gates 45328 and 45329 or gates 45330 through 45333. Dependent on the content of bit positions 1 through 3, one of the six output gates starts to generate a 3.2 kpps pulse train controlling a radar. (In the example, gate 45328 generates signal RRRANG.)
- b. Signals ADVCNT, 3 μ sec pulses, occur at a rate of 100 pps and trigger the radar counter which starts to generate signal CNTOF9 at the occurrence of the ninth ADVCNT pulse. (The counter has been reset by a signal RADRPT previously.) Signal CNTOF9 resets flip-flop 45320/45321, thus discontinuing the generation of any control signal (described in point (a)) after a period of approximately 80 msec.
- c. At the time signal CNTOF9 occurs (a little more than 80 msec after entering the ONE into bit position 1) and the first GTSET/ signal, flip-flop 45337/45338 is set. Once the flip-flop has been set, gate 45339 starts to generate pulses at a rate of 3.2 kpps. These pulses cause gate 45345 or 45346 to generate sync pulses. (In the example, pulses RR SYNC.)

- d. The first pulse generated by gate 45339 also sets flip-flop 45340/45341. Approximately 4.7 msec thereafter, at the occurrence of signal GTRST/, signal RADRPT is generated. (Signal GTRST/ occurs 4.7 msec after signal GTSET/.) Signal RADRPT is generated approximately 85 msec after the first ADVCNT pulse.
- e. Signal RADRPT causes the following four operations: It resets flip-flop 45337/45338, thus cutting off signal RADRPT and the generation of the sync pulses described in point (c). (Fifteen sync pulses were generated during the 4.7 msec period.) It resets bit position 4, thus resetting flip-flop 45402/45403 and stopping the generation of pulses ADVCNT. It resets the radar counter to zero. It sets cell 9 in the Interrupt Priority Control to request the execution of sequence RUPT9 (table 30-6).
- f. The radar under the control of 3.2 kpps pulse train (signal RRRANG in the given example, see point (a)) and sync pulses (signal RRSYNC, point (c)), returns serial data (pulses RRIN0 and RRIN1 in case of our example). The incoming serial pulses are gated according to the content of bit positions 1 through 4. If a ONE is contained in bit position 4, each RRIN0 or LRIN0 pulse received causes the generation of one RNRADP pulse, and each RRIN1 or LRIN1 pulse received causes the generation of one RNRADM pulse. Each RNRADP pulse, as well as each RNRADM pulse, sets cell 19 of the Counter Priority Control; however, each RNRADP pulse causes the Counter Priority Control to request the execution of an instruction SHINC RADAR while each RNRADM pulse causes it to request the execution of an instruction SHANC RADAR.
- g. Reset pulses RRRST and LRRST are generated by gates 49218 and 49219 all the time and at a rate of 3.2 kpps, which is the same rate with which the sync pulses are generated. The reset pulses occur about halfway between the sync pulses.

30-110. BMAG/RHC Control of the CM

30-111. The BMAG/RHC Control (figure 30-8E) is controlled by bit positions 8 and 9 of output channel 13 (table 30-5B) and accepts the following signals from the body mounted acceleration gyros.

BMGXP	(817)	} incremental signals from the BMAG's
BMGXM	(818)	
BMGYP	(821)	
BMGYM	(822)	
BMGZP	(819)	
BMGZM	(820)	

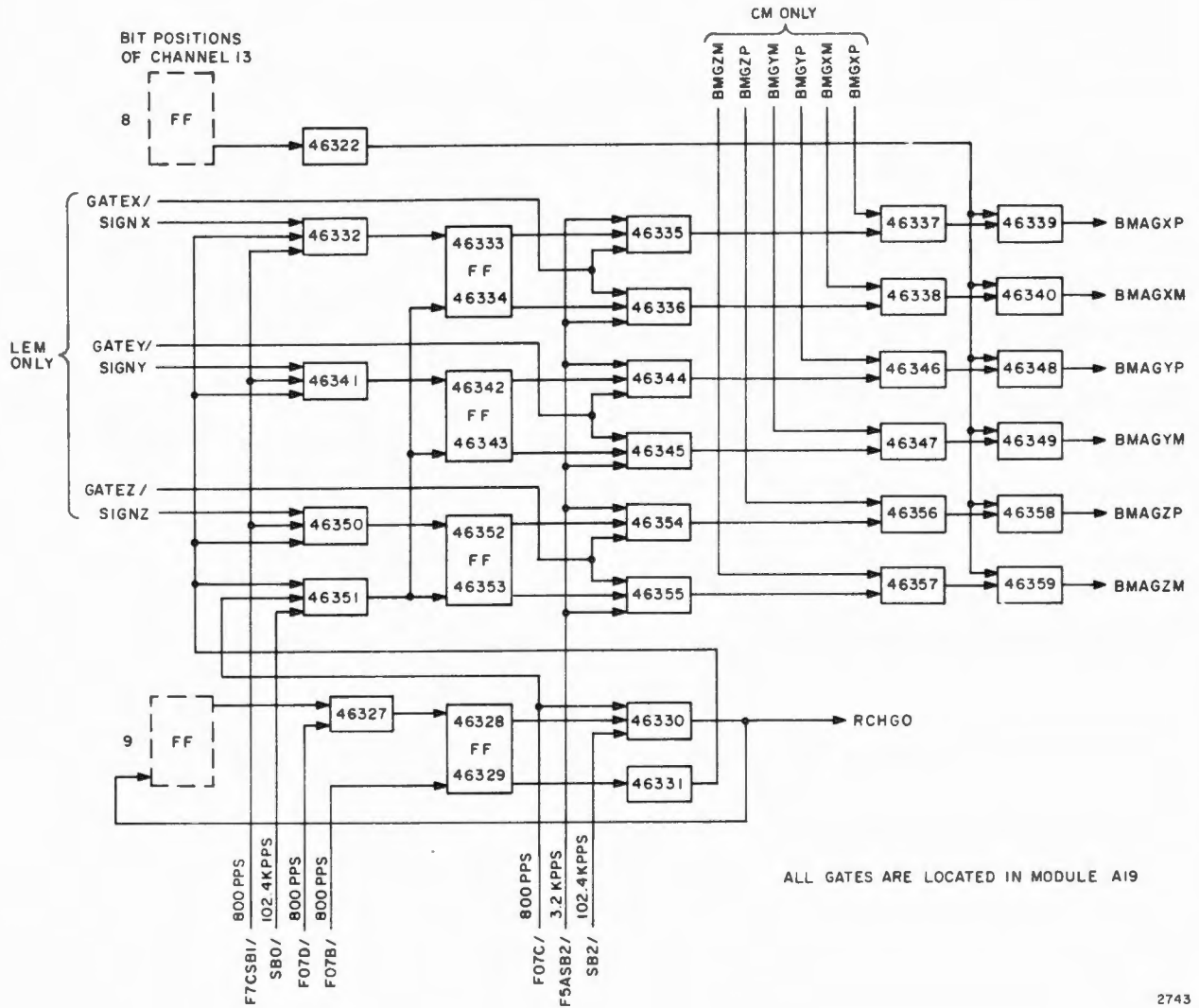


Figure 30-8E. BMAG/RHC Control

30-112. When bit position 8 contains a ONE and bit position 9 a ZERO, the following corresponding pulses are generated whenever one of the incremental input pulses of paragraph 30-111 are received:

BMAGXP	}	Signals entered into the Counter Priority Control to request the execution of a PINC or MINC instruction (table 30-7)
BMAGXM		
BMAGYP		
BMAGYM		
BMAGZP		
BMAGZM		

30-113. BMAG/RHC Control of the LEM

30-114. The BMAG/RHC Control of the LEM is identical to that of the CM but accepts the following signals from the RHC Converter (circuits A of modules A27 through A29):

SIGNX	}	Pulses
SIGNY		
SIGNZ		
GATEX/	}	Pulses varying in length
GATEY/		
GATEZ/		

30-115. When a ONE has been entered into bit position 9 of channel 13, flip-flop 46328/46329 is set at the occurrence of the first F07D/ pulse and reset by a F07B/ pulse approximately 234 μ sec thereafter. During this 234 μ sec period, one pulse RCHGO is generated which resets bit position 9 and which triggers the RHC Converter. During the 234 μ sec period, gates 46332, 46341, and 46351 are enabled to set flip-flop 46333/46334, 46342/46343, or 46352/46353 if signal SIGNX, SIGNY, or SIGNZ, respectively, is received from the RHC Converter in response to the RCHGO signal. Gate 46351 resets shortly thereafter any flip-flop set. Gates 46335, 46336, 46344, 46345, 46354, and 46355 AND the information contained in the three flip-flops, and the information represented by signals GATEX/, GATEY/, and GATEZ/ received from the RHC Converter thus cause the generation of BMAG signals (signals BMAGXP through BMAGZM) accordingly, if bit position 8 contains a ONE. Signals GATEX/, GATEY/, and GATEZ/ are DC signals which vary in length, thus causing the generation of zero to thirty-two BMAG pulses. These pulses enter the Counter Priority Control and each requests the execution of a PINC or MINC instruction as mentioned in paragraph 30-112.

30-116. Inlink Control

30-117. The Inlink Control (figure 30-8F) is controlled by bit positions 5 and 6 of output channel 13 (table 30-5B), and DC signal BLKUPL/ from the Uplink switch and accepts the following signals:

UPL0	(024)	}	serial data from uplink equipment
UPL1	(025)		
XLNK0	(080)	}	serial data from crosslink equipment
XLNK1	(081)		

Signal C45R is provided by the Counter Priority Control when counter INLNK is being addressed and signal BR1/ is generated by the Sequence Generator when the flag bit of an uplink or crosslink word has moved into bit position 16.

30-118. When bit positions 5 and 6 contain ZERO's, and signal BLKUPL/ is present, the Inlink Control generates pulse INLNKM if it received pulse UPL0, and pulse INLNKP if it receives pulse UPL1. These INLNK pulses are used to shift uplink data into counter INLNK as described in tables 30-4 and 30-7. Signal BLKUPL/ means accept uplink data. If bit position 6 contains a ONE, or signal BLKUPL/ is not present, no INLNK signals are generated. When bit position 5 contains a ONE and bit position 6 a ZERO, pulse INLNKM is generated if pulse XLNK0 is received, and pulse INLNKP is generated if pulse XLNK1 is received.

30-119. Each INLNK pulse sets cell 18 in the Counter Priority Control to request the execution of instruction SHINC INLNK (signal INLNKP) or SHANC INLNK (signal INLNKM). Each incoming uplink word as well as each incoming crosslink word starts with a flag bit (a ONE) which is followed by fifteen data bits. Each time a SHINC INLNK or SHANC INLNK instruction is executed, the content of counter INLNK is shifted one place to the left until the flag bit is detected and shifted out (discarded). At this instance, signal BR1/ is generated, which causes the generation of signal UPRUPT to request the execution of the RUPT7 sequence (table 30-6).

30-119A. Flip-flop 46216/46217 is set every 156 μ sec by signal F04A and then enables gates 46203 and 46206 to generate signals INLNKP and INLNKM as described in paragraph 30-118. As flip-flop 46216/46217 is set, it resets flip-flop 46219/46218 in case it was set. Signal C45R is generated each time a SHINC INLNK or SHANC INLNK instruction is executed and sets flip-flop 46219/46218 which, in turn, resets flip-flop 46216/46217 if it was set, thus cutting off gates 46203 and 46206 and enabling gate 46211. In case an inlink or crosslink bit should arrive before flip-flop 46216/46217 is set again, no INLNK pulse is generated but bit position 11 of channel 33 is set to indicate the fact that two uplink or crosslink bits have been received within 156 μ sec.

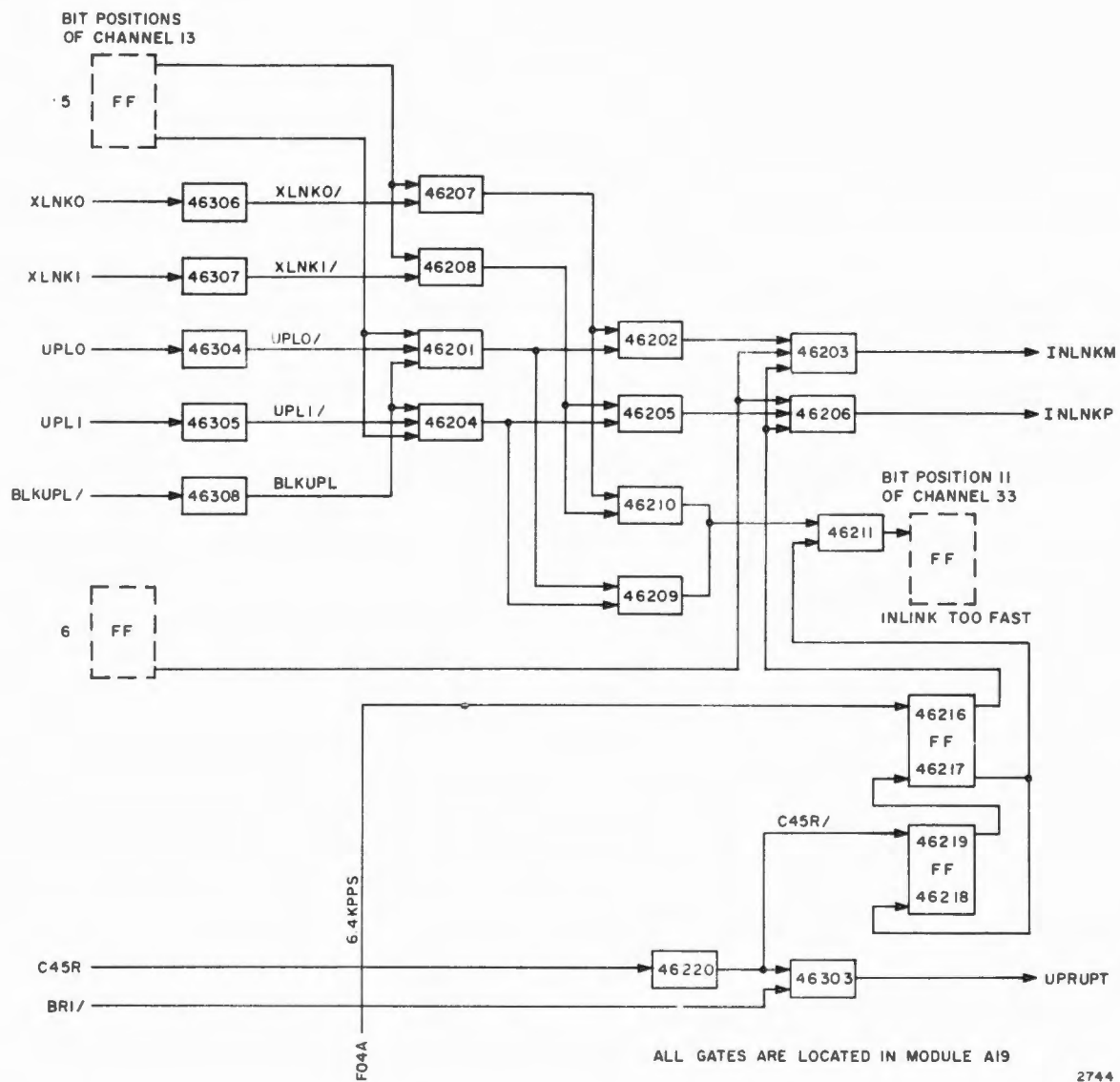


Figure 30-8F. Inlink Control

30-120. Outlink Control

30-121. The Outlink Control (figure 30-8G) is controlled by bit position 1 of output channel 14, and signals BR1 and BR1/ from the SQG. The Outlink Control is able to generate the following signals:

OTLNKM 3.2 kpps signals entered into the Counter Priority Control to request the executions of instruction SHINC OUTLNK (table 30-7)

OTLNK0 (078) }
OTLNK1 (079) } Serial crosslink data

30-122. When a ONE has been entered into bit position 1 of channel 14, the following sequence is started thereafter:

- a. At the occurrence of the first GTSET/ pulse, flip-flop 46138/46139 is set. The GTSET/ pulses are 10 μ sec wide and occur at a rate of 200 pps, or every 5 msec.
- b. Approximately 156 μ sec later, at the occurrence of an F5ASB2/ pulse, one OTLNK1 pulse is generated, flip-flop 46141/46142 is set, and bit position 1 is reset. The F5ASB2/ pulses occur at a rate of 3.2 kpps.
- c. Another 156 μ sec later, at the occurrence of a GTONE pulse, flip-flop 46138/46139 is reset. The GTONE pulses are 10 μ sec wide and occur at a rate of 200 pps, approximately 312 μ sec after the GTSET/ pulses.
- d. Another 156 μ sec later, at the occurrence of an F5ASB0/ pulse, a signal OTLNKM is generated. The F5ASB0/ pulses occur at the same rate as the F5ASB2/ pulses and approximately 3 μ sec earlier.
- e. Another 312 μ sec later, at the occurrence of the next F5ASB0/ pulse, a second signal OTLNKM is generated.
- f. At the occurrence of the next thirteen F5ASB0/ pulses (intervals of 312 μ sec each), thirteen OTLNKM signals are generated.
- g. Thereafter, at the occurrence of a GTSET pulse, flip-flop 46141/46142 is reset, thus discontinuing the generation of OTLNKM signals. Altogether, fifteen OUTLNKM signals are sent to the Sequence Generator.

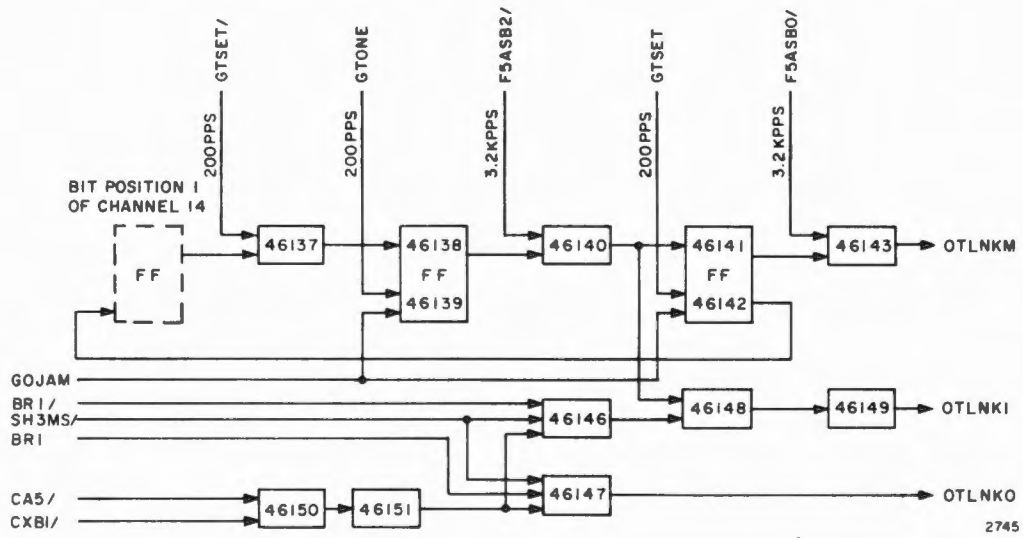


Figure 30-8G. Outlink Control

30-122A. Each OTLNKM pulse causes the execution of instruction SHINC OUTLNK (table 30-4). Each time this instruction is executed, the content of counter OUTLNK is shifted one place to the left and the bit shifted out is converted into an OTLNK signal. If the bit shifted out is a ZERO, signal OTLNK0 is generated; if it is a ONE, signal OTLNK1 is generated. The OTLNK1 signal generated as described in point (b) of the previous paragraph is the flag bit of the crosslink word, while the fifteen OTLNK0 and OTLNK1 signals generated thereafter represent data bits of the same crosslink word.

30-122B. When a new crosslink word has been entered into counter OUTLNK and a ONE has been entered into bit position 1 of channel 14, the operation described in paragraphs 30-122 and 30-122A is repeated.

30-123. Altitude Meter Control

30-124. The Altitude Meter Control (figure 30-8H) is controlled by bit positions 2 and 3 of output channel 14, and signals BR1 and BR1/ from the SQG. The control is able to generate the following signals:

ALTM 3.2 kpps signals entered into the Counter Priority Control to request the executions of instruction SHINC ALT (table 30-7).

ALT0 (003)	}	serial altitude meter data
ALT1 (002)		
ALRT0 (012)		
ALRT1 (010)		

ALTSNC (028) 5.13 msec sync signal

30-125. When bit position 2 of channel 14 contains a ZERO, signals ALT0 and ALT1 are generated. When bit position 2 contains a ONE, signals ALRT0 and ALRT1 are generated instead. Bit position 3 has a purpose similar to bit position 1 for the Outlink Control. When a ONE has been entered into bit position 3, the following sequence is started thereafter.

- a. At the occurrence of the first GTSET/ pulse, flip-flop 46124/46125 is set and the generation of signals ALTSNC begins. (For a description of timing pulses, refer to paragraph 30-123).
- b. Approximately 156 μ sec later, at the occurrence of an F5ASB2/ pulse, an ALT1 or ALRT1 pulse (dependent on the content of bit position 2) is generated, flip-flops 46127/46128 and 46130/46131 are set, and bit position 3 is reset.

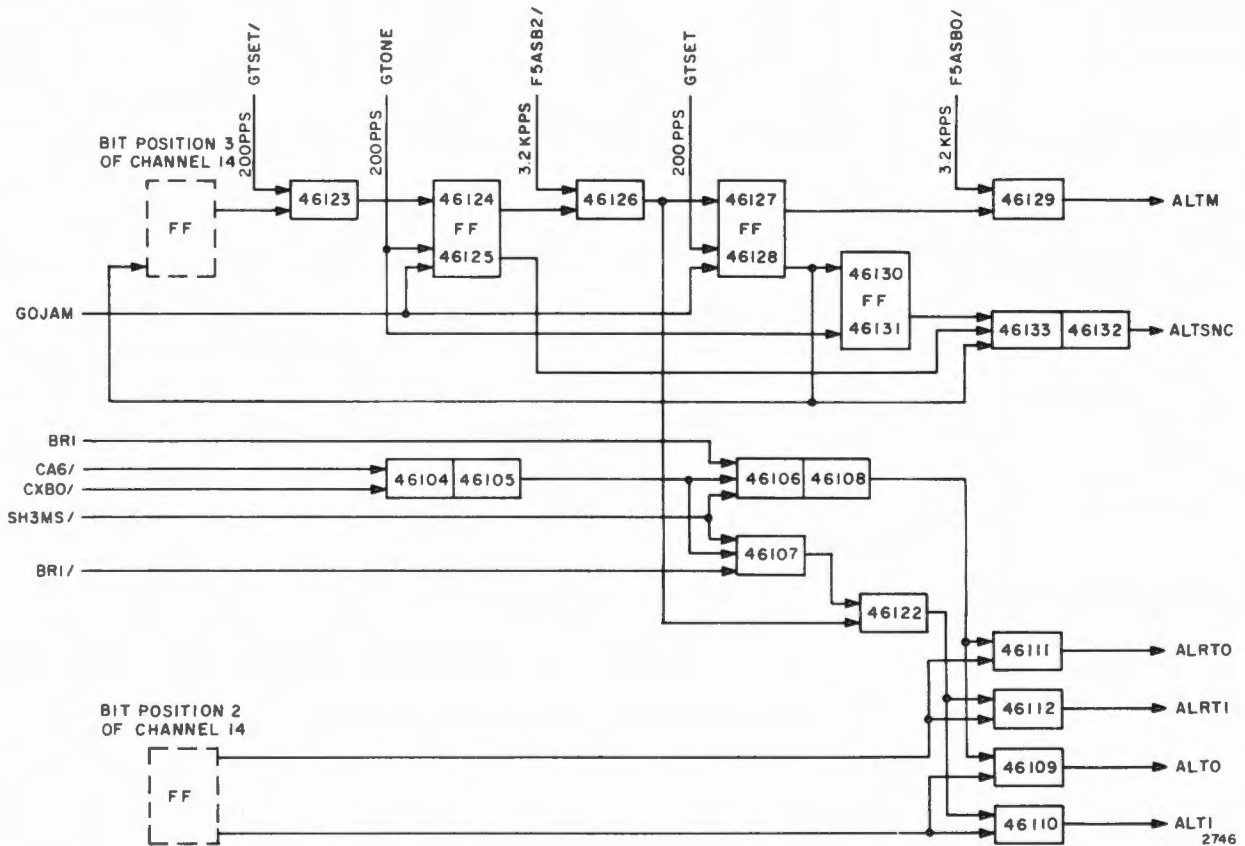


Figure 30-8H. Altitude Meter Control

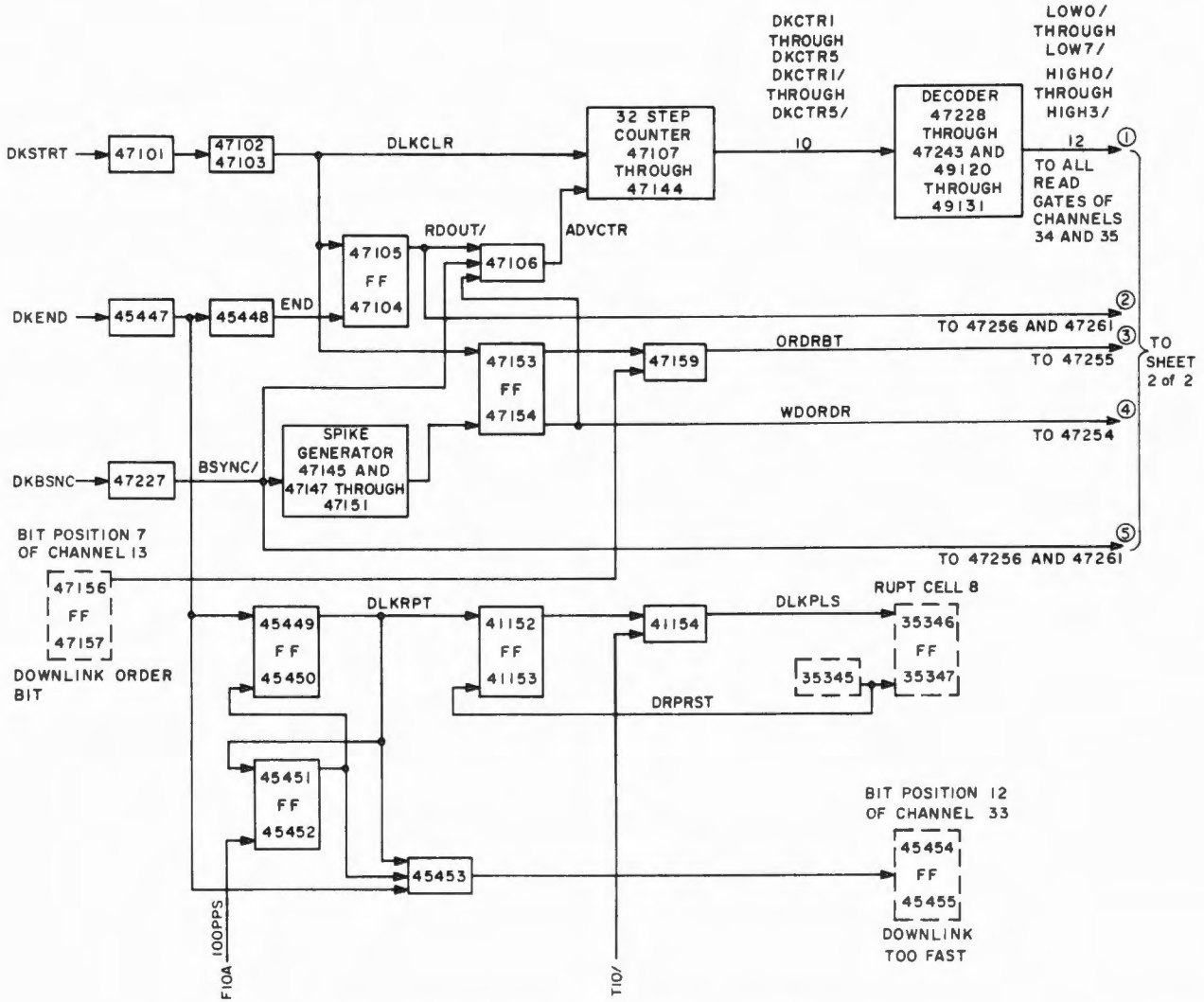
- c. Another 156 μ sec later, at the occurrence of a GTONE pulse, flip-flop 46124/46125 is reset.
- d. Another 156 μ sec later, at the occurrence of an F5ASB0/ pulse, a signal ALTM is generated.
- e. Another 312 μ sec later, at the occurrence of the next F5ASB0/ pulse, a second signal ALTM is generated.
- f. At the occurrence of the next thirteen F5ASB0/ pulses, thirteen ALTM signals are generated.
- g. Thereafter, at the occurrence of the GTSET pulse, flip-flop 46127/46128 is reset, thus discontinuing the generation of ALTM signals.
- h. Approximately 312 μ sec later, at the occurrence of the next GTONE pulse, flip-flop 46130/46131 is reset, thus suspending signal ALTSNC, the generation of which started 5.3 msec earlier, as mentioned in point (a).

30-125A. Each ALTM pulse causes the execution of instruction SHINC ALT (table 30-4). Each time this instruction is executed, the content of counter ALT is shifted one place to the left and the bit shifted out is converted into an ALT or ALRT signal, dependent on the content of bit position 2. If the bit shifted out is a ZERO, signal ALT0 or ALRT0 is generated; if it is a ONE, signal ALT1 or ALRT1 is generated. The ALT1 or ALRT1 signal mentioned in point (b) of the previous paragraph is the flag bit of the altitude meter word.

30-125B. When a new altitude meter word has been entered into counter ALT and a ONE has been entered into bit position 3 of channel 14, the operation described in paragraphs 30-125 and 30-125A is repeated.

30-126. Downlink Converter

30-127. The Downlink Converter (figure 30-8J) is able to convert the following information into serial data: content of bit position 7 (downlink order bit) of channel 13, contents of bit positions 15 through 0 of channel 34, and contents of bit positions 15 through 0 of channel 35 in this sequence. (For numbering of bit positions, refer to figure 30-8J and paragraph 30-71. Bit position 0 contains the parity bit.) The command module AGC is generating all 33 data bits, the LEM AGC only the first 17. The Downlink Converter is controlled by the following signals received from the NA Programmer:



GATES ARE LOCATED IN MODULES A13, A18, A22, AND A24

2747 1 of 2

Figure 30-8J. Downlink Converter (Sheet 1 of 2)

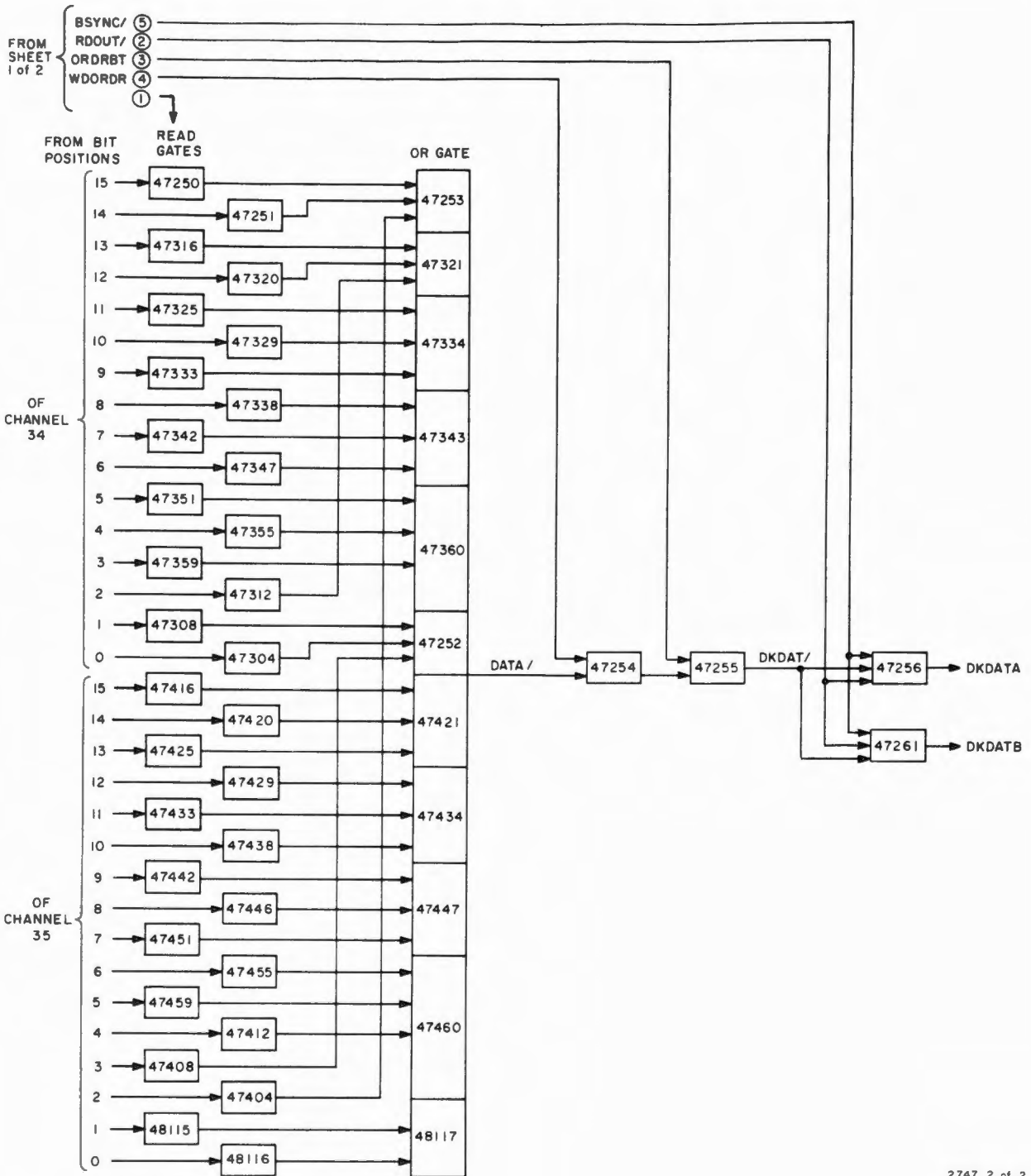


Figure 30-8J. Downlink Converter (Sheet 2 of 2)

DKSTRT (014) Start transmission of a downlink word (33 or 17 bits).
 DKBSNK (016) Send one data bit, the 3 μ sec pulses (33 or 17) are received at intervals of approximately 20 μ sec.
 DKEND (015) End of downlink word.

Each time a DKBSNK pulse is received, the Downlink Converter generates a signal DKDATA (017) and a signal DKDATB (085). Both signals are alike and are a ZERO when the bit position contains a ONE. When a complete downlink word has been transmitted, cell 8 in the Interrupt Priority Control is set to request the execution of program section DOWNRUPT which enters new information into bit position 7 of channel 13 into all bit positions of channel 34 and into all bit positions of channel 35, if applicable. The Downlink Converter sets bit position 12 of channel 33 when the transmission of two downlink words is requested at an interval shorter than 10 msec.

30-127A. Signal DKSTRT, a 3 μ sec pulse, causes the generation of pulse DLKCLR which clears (resets to zero) the 32 step counter and sets flip-flops 47105/47104 and 47153/47154. In the set position, the first flip-flop generates signal RDOUT/ which controls gates 47106, 47256, and 47261. The second flip-flop generates signal WDORDER and a bar signal which is fed into gate 47159. Gate 47159 generates signal ORDRBT if bit position 7 of channel 13 contains a ONE. Each DKBSNC signal, a 3 μ sec pulse, received causes the generation of a BSYNC/ pulse which is fed into gates 47256 and 47261. Each BSYNC/ pulse is also fed into gate 47106; however, the first BSYNC/ pulse after pulse DKSTRT has no effect on gate 47106 since it is kept in the on position by signal WDORDER. All BSYNC/ pulses cause the generation of a spike (short pulse) and the first resets flip-flop 47153/47154. As the flip-flop is reset, signal WDORDER is discontinued, thus allowing gate 47106 to generate an ADVCTR pulse in response to each subsequent BSYNC/ pulse. Each ADVCTR pulse advances the 32 step counter one step. The 10 outputs of the counter are decoded and the 12 outputs of the decoder are used to control the 32 read gates of channels 34 and 35.

30-127B. At the occurrence of the first DKBSNC pulse, gate 47254 is kept in the on position by signal WDORDER. If bit position 7 of channel 13 contains a ONE, signal ORDRBT turns gate 47255 on and signals DKDATA and DKDATB are generated; if bit position 7 contains a ZERO, the two output signals are not generated. At the occurrence of the subsequent 32 (or 16) DKBSNC pulses, no signal WDORDER or ORDRBT is present and the DKDATA and DKDATB pulses are generated according to the contents of bit positions 15, 14,1 and 0 of channel 34 and bit positions 15, 14.....1 and 0 of channel 35 if applicable. The bit positions are selected by the output signals of the decoder as mentioned in the previous paragraph. When signal DKEND is received, a 3 μ sec pulse, signal END, is generated, which resets flip-flop 47105/47104, thus stopping the generation of further DKDATA and DKDATB signals. Signal DKEND also causes setting cell 8 in the Interrupt Priority

Control. Furthermore, the frequency with which the DKEND pulses occur is checked and bit position 12 of channel 33 is set when the interval between two DKEND pulses is less than 10 msec. The DKEND signal in the LEM occurs after the seventeenth DKBSNK pulse, the DKEND pulse in the CM occurs after the thirty-third DKBSNK pulse.

30-128. PRIORITY CONTROL

30-129. The Priority Control consists of the Interrupt Priority Control and the Counter Priority Control.

30-130. INTERRUPT PRIORITY CONTROL

30-131. The Interrupt Priority Control is triggered at the occurrence of certain events to interrupt the execution of a program section currently being executed in favor of a programmed operation of higher priority. The events can be an overflow occurring in certain counters, certain incoming signals, a failure, etc. Refer to table 30-6. At the occurrence of such an event, the start-stop logic or a cell in the Interrupt Priority Control is set.

30-131A. If the Interrupt Priority Control receives one of the signals listed below, the start-stop logic (gates 37227 through 37254, 37259, 41101 through 41105, 41237 through 41240, 45222 and 45224) generates signals GOJAM/, GOJAM, and MGOJAM.

ALGA	caused by a parity fail, a rupt lock, a TC trap, or a watchman failure (paragraphs 30-141B through 30-141L).
STR T1	caused by a voltage failure (paragraph 30-141R)
STR T2	caused by an oscillator failure (paragraph 30-141U)
SBY	from Standby Control when being switched to standby mode
MSTRTP	caused by signal MSTRT from peripheral equipment (Appendix C) if MSTRT remains for a period from 157 to 470 μ sec.

Signal STR T2 causes the start-stop logic to generate the GOJAM signals immediately and forces the Time Pulse Generator into time T12. The other input signals cause the generation of the GOJAM signals at the next time 12. The GOJAM signals are terminated at the execution of instruction GO (signal GOJ1).

30-131B. Signals GOJAM/ and GOJAM cause the execution of instruction GO (paragraphs 32-283 through 32-285), which is followed by the execution of instruction TC 4000 to then execute program section Restart. Furthermore, signals GOJAM/ and GOJAM set the restart flip-flop (gates 41237/41238) and reset a number of circuits in the AGC. The restart flip-flop then causes the generation of signal RESTART (232) which controls DSKY indicator RESTART. The generation of signal RESTART can also be caused by the presence of signal ALTEST, i. e., if bit position 10 of output channel 13 contains a ONE, Signal RESTART is turned on by signal GOJAM and is turned off by signal ERRST or signal SBYEXT; and signal RESTART remains on as long as a ONE is

contained in bit position 10 of output channel 13. Signal ERRST is generated if signal CAURST (208) is received or if a ONE is contained in bit position 10 of output channel 11. Signal SBYEXT is generated by the start-stop logic. Program section Restart clears various locations in E Memory, enters certain quantities into other E memory locations, and sets certain bit positions of the output channels.

30-132. If a RUPT cell has been set, the Interrupt Priority Control does three things: it signals the Sequence Generator to execute instruction RUPT, it supplies the address of the proper RUPT Transfer Routine, and it resets the cell upon the execution of instruction RUPT. Instruction RUPT interrupts the execution of the current program section and transfers control to the proper RUPT Transfer Routine. Ten different RUPT Transfer Routines are provided. Instruction RUPT and the RUPT Transfer Routines preserve pertinent information contained in the CP registers by storing it in locations 0010 through 0017 (table 30-4). Finally, the RUPT Transfer Routine transfers control to the program section to be currently executed. A small routine and instruction RESUME, the last instruction of the interrupting programmed operation, return the pertinent information to the CP registers and cause the SQG to resume the execution of the interrupted program section.

30-133. Whenever two or more interrupt requests have been made (two or more RUPT cells have been set) simultaneously, the Interrupt Priority Control first selects the request of highest priority (lowest priority number) and carries it out; the other requests are carried out after the first request has been satisfied. Thus, current requests are carried out in the order of assigned priorities.

30-134. Once an interrupt request has been made and is being carried out, its execution cannot be interrupted by a request of higher priority. Thus, interruption of an interrupting operation is prevented. Assigned priorities have an effect only on selecting the next request to be carried out.








30-135. Sometimes it is desirable to inhibit any interruption of a program being executed. This can be done by executing instruction INHINT. Instruction RELINT then is used to release the inhibition of a program interrupt.

30-136. COUNTER PRIORITY CONTROL

30-137. The Counter Priority Control is triggered at the occurrence of certain events to increment, decrement, diminish, or shift the content of a counter. The events can be time pulses generated in the AGC, signals received from other equipment or drive pulses generated in the AGC. Refer to table 30-7. Incremental signals received from the outside are fed directly or via the BMAG/RHC Control into the Counter Priority Control and request







(Text continued on page 30-72).

TABLE 30-6
INTERRUPT MOTIONS

Priority Level Number	Initiating Event 	RUPT Cell Set (Gates)	Further Actions Caused 
0	Occurrence of signal ALGA, START1, START2, or MSTRT	RUPT0 (37226 through 37229)	Execution of instructions GO and TC 4000 Execution of Restart Sequence.
1	Content of Counter T6 diminishes to zero 	RUPT1 (35306 through 35309)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 1. Execution of program section Reaction Control.
2	Overflow of Counter T5 	RUPT2 (35310 through 35313)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 2. Execution of program section Trans Vector Control.
3	Overflow of Counter T3 	RUPT3 (35315 through 35318)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 3. Execution of routine T3RUPT of program section Waitlister (Task Control). Execution of Task due.
4	Overflow of Counter T4 	RUPT4 (35322, 35323, 35325, 35326)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 4. Execution of routine T4RUPT of program section T4RUPT Output Control. Transfer of information to DSKY's via output channel 10, or driving CDU's, or checking IMU or Optics mode, etc.
5	Arrival of a KEY bit from main panel DSKY 	RUPT5 (35327 through 35329)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 5. Execution of function KEYRUPT which requests the execution of Job CHARIN of program section Keyboard and Display to process keyed in data.

(cont)

TABLE 30-6
INTERRUPT MOTIONS (cont)

Priority Level Number	Initiating Event 	RUPT Cell Set (Gates)	Further Actions Caused 
6	Arrival of a KEY bit from navigation panel DSKY 	RUPT6 (35333 through 35335)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 6. Execution of function KEYRUPT which requests the execution of Job CHARIN of program section Keyboard and Display to process keyed in data.
6	Arrival of a Mark bit from Optics 	RUPT6 (35333 through 35335)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 6. Execution of function KEYRUPT and routine MARK to process optics data.
7	Appearance of flag bit in bit position 16 when content of counter INLNK is shifted 	RUPT7 (35339 through 35341)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 7. Execution of function UPRUPT which requests the execution of Job CHARIN of program section Keyboard and Display to process data received via inlink or crosslink. (See paragraphs 30-116 through 30-119A.)
8	Arrival of signal DKEND (015) from NA Programmer 	RUPT8 (35345 through 35347)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 8. Execution of program section DOWNRUPT to enter new data downlink transmission into bit position 7 of channel 13 and into all bit position of channels 34 and 35 (LEM 34 only) (See paragraphs 30-126 through 30-127B.)

(cont)

TABLE 30-6
INTERRUPT MOTIONS (cont)

Priority Level Number	Initiating Event △4	RUPT Cell Set (Gates)	Further Actions Caused △1
9	Occurrence of signal RADRPT from Radar Control	RUPT9 (35220, 35222, 35223)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 9. Execution of program section Radar to process data from a radar. (See paragraphs 30-105 through 30-109.)
10	Arrival of a rotation or translation command (093 through 098 and 018 through 022) from the hand controller △2	RUPT10 (35221, 35223, 35225)	Execution of instruction RUPT. Execution of RUPT Transfer Routine 10. Execution of program section Hand Control to carry out commanded motion.

△1 The names of some RUPT Transfer Routines and of some program sections have been arbitrarily chosen until official names are available.

△2 Also refer to table 30-4.

△3 Also refer to table 30-5.

△4 Numbers in () refer to signals listed in Appendices A and B.

TABLE 30-7

COUNTER PRIORITY CONTROL INPUTS 



Priority Level Number and Priority Cell Number (Input Gate)	Event	Instruction Executed
1 (31129)	Overflow of counter T1	PINC T2
2 (31136)	10 msec time signal from Scaler 1	PINC T1
3 (31143)	10 msec time signal from Scaler 1	PINC T3
4 (31229)	10 msec time signal from Scaler 1	PINC T4
5 (31236)	10 msec time signal from Scaler 1	PINC T5
6 (31243)	10 msec time signal from Scaler 1	DINC T6
7 (31102)	Signal CDUXP (118)	PCDU XCDU
7 (31109)	Signal CDUXM (119)	MCDU XCDU
8 (31115)	Signal CDUYP (120)	PCDU YCDU
8 (31124)	Signal CDUYM (121)	MCDU YCDU
9 (31202)	Signal CDUZP (122)	PCDU ZCDU
9 (31209)	Signal CDUZM (123)	MCDU ZCDU
10 (31215)	Signal TRNP (110)	PCDU TCDU
10 (31224)	Signal TRNM (111)	MCDU TCDU
11 (31303)	Signal SHAFTP (108)	PCDU SCDU
11 (31309)	Signal SHAFTM (109)	MCDU SCDU
12 (31315)	Signal PIPXP (132)	PINC XPIPA
12 (31324)	Signal PIPXM (133)	MINC XPIPA
13 (31402)	Signal PIPYP (134)	PINC YPIPA
13 (31409)	Signal PIPYM (135)	MINC YPIPA
14 (31415)	Signal PIPZP (136)	PINC ZPIPA
14 (31424)	Signal PIPZM (137)	MINC ZPIPA
15 (32502)	Signal BMAGXP (817) 	PINC XBMAG
15 (32509)	Signal BMAGXM (818) 	MINC XBMAG

TABLE 30-7

COUNTER PRIORITY CONTROL INPUTS ^① (cont)

Priority Level Number and Priority Cell Number (Input Gate)	Event	Instruction Executed
16 (32515)	Signal BMAGYP (821)	PINC YBMAG
16 (32524)	Signal BMAGYM (822)	MINC YBMAG
17 (32602)	Signal BMAGZP (819)	PINC ZBMAG
17 (32609)	Signal BMAGZM (820)	MINC ZBMAG
18 (32615)	Signal INLNKP (024)	SHINC INLNK
18 (32624)	Signal INLNKM (025)	SHANC INLNK
19 (32629)	Signal RNRADP (031)	SHINC RADAR
19 (32636)	Signal RNRADM (032)	SHANC RADAR
20 (32643)	Signal GYROD (142 through 147)	DINC GYROS
21 (31329)	Signal CDUXD (126, 127)	DINC XCDUCOM
22 (31336)	Signal CDUYD (128, 129)	DINC YCDUCOM
23 (31343)	Signal CDUZD (130, 131)	DINC ZCDUCOM
24 (31429)	Signal TRUND (114, 115)	DINC TCDUCOM
25 (31436)	Signal SHAFTD (116, 117)	DINC SCDJCOM
26 (31443)	Signal THRSTD (LEM only) (008, 009)	DINC THRUST
27 (32529)	Signal EMSD (029 and 030)	DINC EMS
28 (32536)	Signal OTLNKM	SHINC OUTLNK
29 (32543)	Signal ALTM (LEM only)	SHINC ALT

^① Numbers in () refer to signals listed in Appendices A and B
Also refer to table 30-4.

^② Refer to paragraphs 30-110 through 30-115

^③ Refer to paragraphs 30-116 through 30-119

^④ Refer to paragraphs 30-105 through 30-109

^⑤ Refer to paragraphs 30- 95 through 30- 99

^⑥ Refer to paragraphs 30-90 through 30-94

^⑦ Refer to paragraphs 30-100 through 30-104

^⑧ Refer to paragraphs 30-120 through 30-122

^⑨ Refer to paragraphs 30-123 through 30-125

the execution of an incrementing or decrementing instruction. The incremental signals (pulses) may represent a positive or a negative quantity of equal magnitude. Serial data received from outside the AGC is fed into the Inlink or Radar Control (figure 30-6) which gates it into the Counter Priority Control. When a ZERO is received, the content of a counter is shifted one place to the left and a ZERO is entered into bit position 1; when a ONE is received, the content is also shifted one place but a ONE is entered into bit position 1. Whenever one of the events previously described occurs, a cell in the Counter Priority Control is set. One cell is provided for each priority level.

30-138. If a cell has been set, the Counter Priority Control does three things: first, it signals the Sequence Generator (SQG) to execute instruction PINC (positive increment), MINC (negative increment or decrement), DINC (diminish absolute quantity), PCDU (positive increment of cyclic TWO's complement information), SHINC (shift and enter a ZERO in bit position 1), or SHANC (shift and enter a ONE in bit position 1); second, it supplies the address of the proper counter; and third, it resets the priority cell upon the execution of the requested Counter Instruction. The Counter Instruction is executed as soon as the execution of a Regular Instruction is completed.

30-139. If more than one request for incrementing, decrementing, diminishing, or shifting the content of a counter has been made during the execution of a Regular Instruction, the requested operations are carried out according to assigned priorities. The levels of priority decrease as the addresses of the counters increase. All requested counter operations are carried out before the next Regular Instruction is executed.

30-140. ALARM CONTROL

30-141. The Alarm Control consists of several digital fault detectors, several analog fault detectors, and a warning integrator which works with some of the detectors. Most of these circuits are shown on NASA drawings 2005069, 2005072, 2005073, and 2005008. Many of the signals generated by the Alarm Control are listed in Appendix C. Indication of Optics CDU fail, IMU CDU fail, IMU fail, and temperature within limits, is produced outside the AGC and is received via input channel 30 (table 30-5D).

30-141A. DIGITAL FAULT DETECTIONS

30-141B. Parity Fail

30-141C. The Parity Block generates signals PALE and MPAL/ when it detects incorrect parity (paragraph 30-49). Signal PALE causes the alarm control gates 41116 through 41118 to generate signal ALGA unless signal NHALGA

(Appendix C) is provided by peripheral equipment. Signal ALGA causes the start-stop logic to restart computer operation.

30-141D. Rupt Lock

30-141E. If a program interrupt lasts too long, or if program interruptions occur in too short intervals, the alarm control gates 41107 through 41118 generate signal MRPTAL/, and also signal ALGA when signal NHALGA is not applied. Signal ALGA causes the start-stop logic to restart computer operation. The terms "too long" and "too short" are phase dependent and may vary from 80 msec to 240 msec.

30-141F. TC Trap

30-141G. If consecutive TC K and/or TCF F instructions are executed for too long, or if these instructions are executed in too short intervals, the alarm control gates 41119 through 41128 and 41116 through 41118) generate signal MTCAL/, and also signal ALGA when signal NHALGA is not applied. Signal ALGA causes the start-stop logic to restart computer operation. The terms "too long" and "too short" are phase dependent and may vary from 5 msec to 15 msec.

30-141H. Watchman

30-141J. If location 0067 is not addressed within a certain period, the alarm control gates 49110 through 49118 generate signals WATCHP and MWATCH/. Signal WATCHP causes the generation of signal ALGA (gates 41116 through 41118), except when signal NHALGA is applied, and causes the restart of computer operation. The duration of the period is phase dependent and may vary from 0.64 sec to 1.92 sec.

30-141K. Counter Fail

30-141L. If Counter Instructions are executed consecutively for too long (i. e., if locations 0024 through 0056 are addressed for too long) or if a Counter Instruction is not being executed once its execution has been requested, the alarm control gates 49435 through 49443 and 41132 through 41151 generate signals DOFILT and MCTRAL/. The term "too long" is phase dependent and may vary from 0.625 msec to 1.875 msec. Signal DOFILT causes the generation of signal FILTIN (gates 41208 through 41216, paragraph 30-141AA) which is fed into the warning integrator (paragraph 31-141AB). Depending on the frequency with which signal FILTIN occurs, the warning integrator may generate signal FLTOUT. Signal FLTOUT causes the generation of signals CGCWAR (237) and MWARNF/ (gates 41223, 41224, and 41227) and enters

a ONE into bit position 14 of input channel 33 (gates 41225/41226 and 44258). An AGC program can make use of the bit stored in channel 33.

30-141M. PIPA Fail

30-141N. If no PIPA pulse (signals 132 through 137) is received from any PIPA during a 312.5 μ sec period, or if a + and - PIPA pulse from the same PIPA is received simultaneously, or if the time period between the arrival of a + and a - PIPA pulse from one PIPA is too long, the alarm control gates 48149 through 48154, 48252 through 48257, 49303 through 49308, and 48101 through 48105 generate a signal which enters a ONE into bit position 13 of input channel 33. The term "too long" is phase dependent and may vary from 1.28 sec to 3.84 sec. Bit position 13 of channel 33 (gates 48106 through 48108) supplies signal PIPAFL and gate 41106 signal MPIPAL/. The AGC program makes use of the bit stored in channel 33 to set ISS warning and program caution relays in the DSKY's.

30-141P. ANALOG FAULT DETECTIONS

30-141Q. Voltage Fail

30-141R. If an AGC voltage (+28VAC, +14VDC BPLUS, +4VDC) is out of limits, the voltage alarm (module B08) generates signal VFAIL. If this signal is present for a period between 157 and 470 μ sec, and if inhibit signal NHVFAL (912) is not present, the alarm control gates 41201 through 41207 generate signals STRT1 and MVFAIL. Signal STRT1 causes the start-stop logic to restart computer operation unless line STRT1 is connected to ground (see STRT1 of Appendix C).

30-141S. When the AGC operates in the standby mode, signal FILTIN is generated simultaneously with signal STRT1 (gates 41208 through 41216). Depending on the frequency with which signal FILTIN occurs, the warning integrator may generate signal FLTOUT and cause the subsequent actions described in paragraph 30-141L.

30-141T. Oscillator Fail

30-141U. If the oscillator stops, i. e., if the Q2A pulses which are similar to the clock pulses CLK (signal 001) are not generated, the oscillator alarm (module B08) generates signal STRT2 within 250 msec. Signal STRT2 causes the start-stop logic to restart computer operation immediately, i. e., without waiting for the next time pulse T12. Signal STRT2 also enters a ONE into bit position 15 of input channel 33 (gates 41232/41233 and 44257) which provides signal OSCALM. Signal MOSCAL/ is provided by gate 41231. An AGC program can make use of the bit stored in channel 33.

30-141V. When the AGC operates in the standby mode, the oscillator alarm is without power and 250 msec is required after switching to normal operation to be operative thus avoiding an erroneous failure indication at mode switching.

30-141W. Scaler Fail

30-141X. If stage 17 of the Scaler fails to produce pulses (signal FS17, 0.78125 pps), the scaler alarm (gate 32258 and module B08) generates signal SCAFAL. Signal SCAFAL causes the alarm control gates 41224 and 41222 to generate signals CGCWAR (237) and MSCAFL/, and to enter a ONE into bit position 14 of input channel 33 (gates 41225/41226 and 44258). Signal DOSCAL from peripheral equipment prevents FS17 pulses from producing SCAS17 pulses and can be used to test the scaler alarm circuits.

30-141Y. If stage 10 of the Scaler produces more than 200 pps instead of 100 pps (signal FS10), the double frequency scaler alarm (gates 30057 through 30059, 41242, 41243, 34253, and module 08) generates signals 2FSFAL, SCADBL, and MSCDBL/. Signal SCADBL causes the generation of signal FILTIN as signal DOFILT does. The actions caused by signal FILTIN are described in paragraph 31-141L and apply here as well. Signal DBLTST from peripheral equipment causes the Alarm Control to use FS09 pulses instead of FS10 pulses to produce SCAS10 pulses and can be used to test the double frequency scaler alarm circuits.

30-141Z. WARNING INTEGRATOR

30-141AA. The warning integrator generates signal FLTOUT if the following events occur repeatedly within a certain time.

- Counter fail (paragraph 30-141L)
- Voltage fail (paragraph 30-141S)
- Double frequency scaler fail (paragraph 30-141Y)
- Test alarm (a ONE is entered into bit position 10 of output channel 13)

Signal DOFILT from the counter fail detection, a signal from the voltage fail detection, signal SCADBL from the double frequency scaler fail detection, and signal ALTEST from bit position 10 of channel 13 set the first warning filter flip-flop (gates 41211/41212) which is reset by pulse F14B occurring every 160 msec. The second filter flip-flop (41214/41215), which is controlled by the output of the first flip-flop and signal F14B, cannot produce more than one FILTIN pulse per 160 msec, no matter how many signals were received from the fail detections.

30-141AB. Approximately six consecutive FILTIN pulses cause the warning integrator to generate signal FLTOUT for about 5 sec. Signal FLTOUT causes the generation of signals CGCWAR and MWARNF, and signal SCAFAL causes the generation of signals CGCWAR and MSCAFL/. Non-consecutive FILTIN pulses may also cause the warning integrator to generate signal FLTOUT if the frequency of FILTIN pulses is 0.9 pps or higher. Once signal FLTOUT is being generated, it will remain if FILTIN pulses occur at a frequency of 0.6 pps or more.

30-141AC. ASSOCIATED SIGNALS

30-141AD. Light Test

30-141AE. Entering a ONE into bit position 10 of output channel 13 allows testing DSKY relays and indicators which cannot be controlled by a program. Bit position 10 of channel 13 generates signal ALTEST which controls the start-stop logic, the Alarm Control, and the Standby Control. In the start-stop logic, signal ALTEST causes the generation of signal RESTR T (232) which operates DSKY indicator RESTART (paragraph 30-131B). In the Alarm Control, signal ALTEST causes the generation of signal FILTIN (paragraph 30-141AA). Signal FILTIN causes the generation of signal CGCWAR (237) which lights an indicator in the spacecraft and which enters a ONE into bit position 14 of channel 33 (paragraph 30-141L). In the Standby Control, signal ALTEST causes the generation of signal SBYLIT (231) which operates DSKY indicator STBY.

30-141AF. When bit position 10 of output channel 13 is reset to contain ZERO, the generation of signal RESTR T is terminated immediately and the DSKY indicator RESTART is turned off; if no counter failure, no voltage failure, and no double frequency scaler failure is present, signal FILTIN is terminated and the CGC warning indicator in the spacecraft will be turned off within 5 sec; and signal SBYLIT is terminated immediately and the STBY indicator turned off.

30-141AG. Alarm Reset

30-141AH. Depressing key RSET on a DSKY produces signal CAURST (208) and a ONE contained in bit position 10 of output channel 11 generates signal W1110. Both signals generate signal ERRST which resets the restart flip-flop (paragraph 30-131B) and terminates the generation of signal RESTR T (232). Terminating signal RESTR T has the effect of turning on DSKY indicator RESTART and turning off the caution indicator(s) in the spacecraft.

30-141AJ. STANDBY CONTROL

30-141AK. The Standby Control (gates 45141 through 45159, 41234 through 41236, and 42457) allow switching computer operation from the normal mode of operation to standby and vice versa. Switching to standby is established by first entering a ONE into bit position 11 of channel 13 to enable the Standby Control and then pressing the STBY button on a DSKY for a period of .64 to 1.92 sec. Normal operation is resumed by again pressing the STBY button for .64 to 1.92 sec.

30-141AL. Pressing the STBY button produces signal SBYBUT (207). When the button is pressed during normal operation, if signal SBYBUT is present for .64 to 1.92 sec, and if bit position 11 of channel 13 contains a ONE, then signals SBYREL/, SBYLIT, SBY, and STNDBY/ are generated. When the button is pressed a second time, if signal SBYBUT is present for .64 to 1.92 sec, the four output signals of the Standby Control are terminated.

30-141AM. Signal SBYREL/, which operates two relays in the Power Supply turns off the switchable +4 and +14 voltage lines, thus putting the AGC into a low power mode, where only the Clock and the Scaler operate and some timing and auxiliary signals are generated. Signal SBYLIT (231) turns on DSKY indicator STBY. Signal SBYLIT is also generated when signal ALTEST occurs during light test (paragraph 30-141AE). Signal SBY causes the start-stop logic to generate GOJAM commands (paragraph 30-131A). Signal SBY also causes the generation of an SBYEXT pulse (up to 10 msec long) which causes the start-stop logic to turn off signal RESTART (paragraph 30-131B). Signal STNDBY/ allows the Alarm Control to generate signal FILTIN in case of a voltage failure (paragraph 30-141S) which causes an AGC warning. An AGC warning can also occur in the standby mode due to a scaler failure (paragraph 30-141W) but not due to a counter failure, a double frequency scaler failure, or an alarm test (paragraph 30-141AA).

30-142. DISPLAY AND KEYBOARDS

30-143. The two DSKY's (figure 30-4) allow an operator in the command module (CM) to communicate with the AGC. Commands (in coded form) and data can be entered into the computer by punching it into a DSKY keyboard. As a key is depressed (except key STBY), input channel 15 or 16 (table 30-5) accepts the corresponding 5-bit key code and the Interrupt Priority Control initiates the execution of program section Keyboard and Display (table 30-6, priority levels 5 and 6, and paragraph 30-84). This program section then processes each 5-bit code information as keyed in, assembles commands or data, and carries out any command punched in or stores inserted data in the specified location.

30-144. Switching the AGC from normal mode of operation to standby is established by punching in Verb-Noun combination Enable Standby, which enters a ONE into bit position 11 of output channel 13, and by pressing key STBY for .64 to 1.92 sec. Switching the AGC from standby to normal operation is done by pressing key STBY for .64 to 1.92 sec (paragraphs 30-141AJ through 30-141AM).

30-145. Information keyed in is displayed automatically as well as any information which is to be displayed on command. Such information is entered into output channel 10 (table 30-5) under program control (program sections Keyboard and Display and T4RUP T Output Control). Output channel 10 controls relay matrices in the DSKY's which, in turn, control the numeric displays and some caution indicators (paragraph 30-77). Some other indicators are controlled by output channel 11 (paragraph 30-78). Indicators STBY and RESTART are controlled by hardware originated signals (paragraphs 30-141AM and 30-131B, respectively); all other displays are under program control.

30-145A. Each DSKY contains a relay matrix consisting of thirteen banks (octal 00 through 14) of up to eleven latching relays each. The latching relays are set or reset by means of relay words entered into output channel 10 (table 30-5). Bit positions 15 through 12 of a relay word contain a bank number which addresses the proper relay bank; any ONE or ZERO in bit positions 11 through 1 sets or resets the respective relay in the addressed bank. Relay banks 00 through 10 control the three 5-digit data displays, each digit display being composed of seven segments and each sign display of three segments. Banks 11 through 13 control the 2-digit NOUN, VERB, and PROGRAM displays, respectively.

30-145B. The nine relays of bank 14 control eight DSKY status and caution indicators and the PIPA's as described below.

<u>Relay</u>	<u>Function</u>
AUTO	operates indicator AUTO, controlled by bit 1 $\triangle 1$
HOLD	operates indicator HOLD, controlled by bit 2 $\triangle 1$
FREE	operates indicator FREE, controlled by bit 3 $\triangle 1$
NO ATT	operates indicator NO ATT, controlled by bit 4 $\triangle 1$
SPARE	operates a spare indicator, controlled by bit 5 $\triangle 1$
GIMBAL LOCK	operates indicator GIMBAL LOCK, controlled by bit 6 $\triangle 1$

<u>Relay</u>	<u>Function</u>
SPARE	enables the PIPA's, controlled by bit 7 $\triangle 1$
TRACKER	operates indicator TRACKER, controlled by bit 8 $\triangle 1$
PROG CAUTION	operates indicator PROG, controlled by bit 9 $\triangle 1$

$\triangle 1$ of a relay word contained in channel 10; the relay word contains the relay word code 14 in bit positions 15 through 12.

Relays GIMBAL LOCK, TRACKER, and PROG CAUTION also operate a caution indicator on the condition annunciator.

30-145C. Each DSKY also contains 12 non-latching relays which are used as follows:

<u>Relay</u>	<u>Function</u>
COMP ACTY	controlled by bit position 2 of channel 11 (signal 230), operates DSKY indicator COMP ACTY,
UPLINK ACTY	controlled by bit position 3 of channel 11 (signal 235), operates DSKY indicator UPLINK ACTY,
TEMP CAUTION	controlled by signal TMPCAU (258), i. e., by bit position 4 of channel 11 and signal TEMPIN/, operates DSKY indicator TEMP,
KEY REL	controlled by bit position 5 of channel 11 (signal 236, pulse modulated), operates DSKY indicator KEY REL which flashes,
OPR ERROR	controlled by bit position 7 of channel 11 (signal 244, pulse modulated), operates DSKY indicator OPR ERR which flashes,
FLASH	controlled by bit position 6 of channel 11 (signal 238), operates the verb-noun flash circuit in the DSKY,
ISS WARNING	controlled by bit position 6 of channel 11 (signal 229) generates signals ISS WARNING (324 and 351) which operate inertial subsystem warning indicators in the spacecraft but none on the DSKY's,
INJ SEQ START	controlled by bit position 13 of channel 12 (signal 233), operates the injection sequence start control in the spacecraft,

<u>Relay</u>	<u>Function</u>
CUTOFF	controlled by bit position 14 of channel 12 (signal 234), operates the SIVB engine,
RESTART	controlled by start-stop logic (signal 232, paragraph 30-13B), operates DSKY indicator RESTART,
CIRCUIT	controlled by the Alarm Control (signal 237, paragraph 30-141AB), operates an indicator in the spacecraft but none on the DSKY,
STBY	controlled by the Standby Control (signal 231, paragraph 30-141AM), operates indicator STBY,

Relays TEMP and RESTART operate a caution indicator on the condition annunciator as do relays GIMBAL LOCK, TRACKER, and PROG CAUTION.

30-146. All information transmitted from the AGC to the DSKY's is also sent to the ground stations via output channels 34 and 35 (paragraph 30-82) and downlink. Thus, the ground stations are informed about what is going on in the spacecraft and what actions the spaceborne crew is taking.

30-147. An operator at a ground station can communicate with an AGC in a spaceborne CM in a similar way as an operator in the spacecraft. In this case, commands and data are entered into the AGC via the uplink equipment and counter INLINK (table 30-4). Counter INLINK accepts the same 5-bit key codes as input channels 15 and 16, except that each key code is transmitted three times and entered in counter INLINK three times. Routine UPRUPT makes uplink information available to program section Keyboard and Display for processing as described in paragraph 30-143. Of course, the spacecraft crew is able to observe any actions taken by a ground station and has the capability to prevent any interference from the ground.

30-148. INSTRUCTIONS

30-149. WORD FORMATS AND INSTRUCTION TYPES

30-150. Instruction words, address words, and data words consist of sixteen bits when stored in E or F Memory. The bits are numbered 15 through 0 as indicated in figure 30-9. Bit position 0 is always reserved for the parity bit (paragraph 30-48).

30-151. Normally, a data word represents a ONE's complement quantity with a sign bit in bit position 15, the highest order bit in bit position 14 and the lowest order bit in bit position 1 (paragraphs 30-43 through 30-45). If a data word represents a cyclic TWO's complement number, bit positions 15 through 1 contain value bits only and no sign bit (paragraph 30-46).

30-152. Two types of instructions can be written in an AGC program: Regular Machine Instructions and Interpretive Instructions (paragraph 30-8). A Regular Instruction, normally, is composed of a 3-bit order code in bit positions 15 through 13 and a 12-bit relevant address in bit positions 12 through 1.

30-153. A Regular Machine Instruction which refers to E Memory only may be composed of a 5-bit order code and a 10-bit address. The 5-bit order code consists of a regular (whole) order code in bit positions 15 through 13 and a quarter code in bit positions 12 and 11, with an assumed binary point between bit positions 13 and 12. This allows one to express all order codes in fractional octal number. (The quarter codes are $0/4 = .0$, $1/4 = .2$, $2/4 = .4$, $3/4 = .6$.)

30-154. Channel Instructions (paragraph 30-69) are composed of a 6-bit order code and a 9-bit address. The 6-bit order code consists of a whole order code in bit positions 15 through 13 and an eighth code in bit positions 12 through 11. (The eighth codes are: $0/8 = .0$, $1/8 = .1$, $2/8 = .2$, $3/8 = .3$, $7/8 = .7$).

30-155. The order code of an Interpretive Instruction consists of seven bits. An Interpretive Instruction Word may contain two such order codes in bit positions 7 through 1 and 14 through 8. An Interpretive Instruction Word is incremented by one and complemented (by the Yul programming system) before it is stored in F memory; therefore, it contains a ONE in bit position 15.

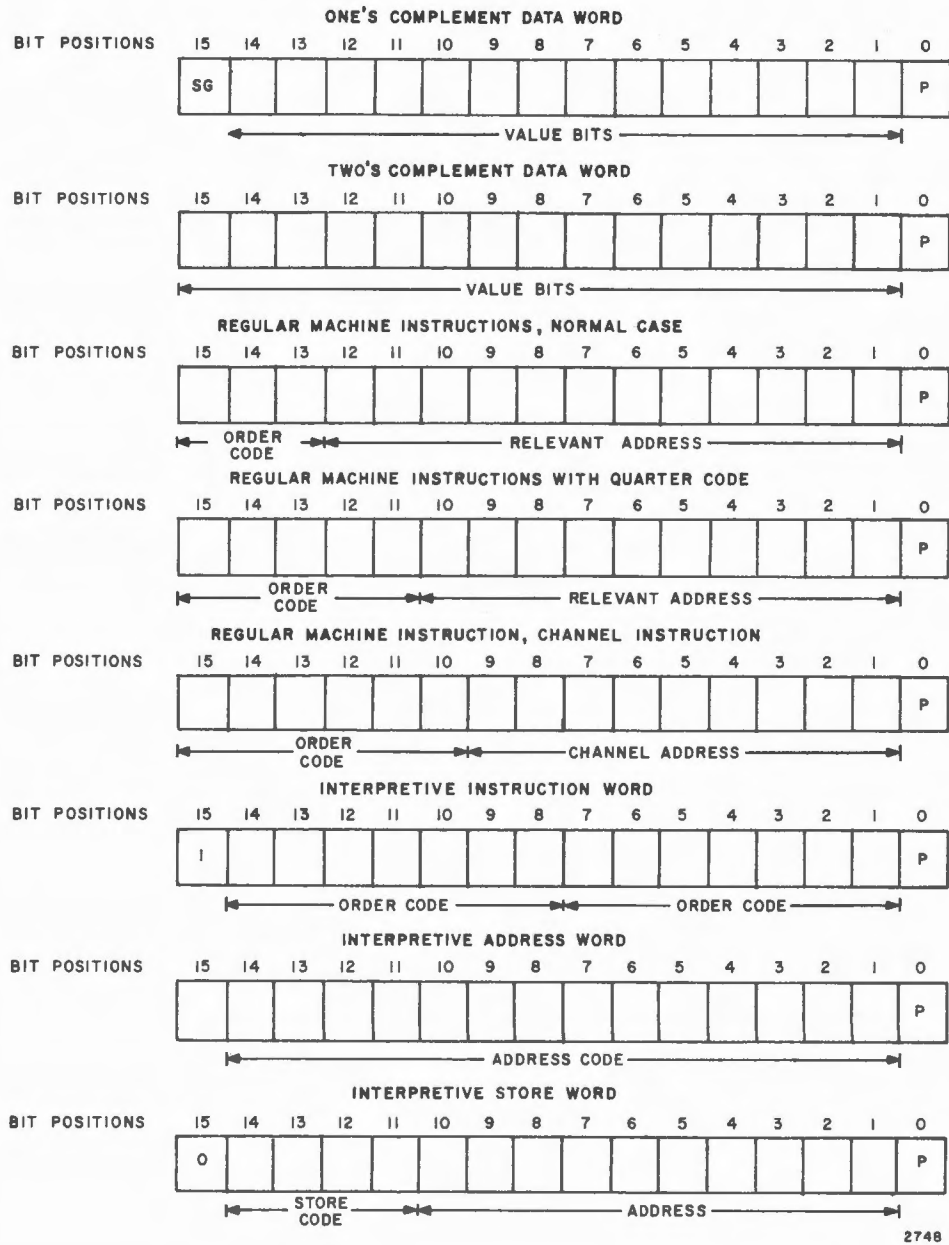


Figure 30-9. Word Formats

An Interpretive Address Word is incremented by one before it is stored in F Memory and contains up to 15 address bits. Each Interpretive Instruction Word is followed by as many (two, one, or none) Interpretive Address Words as required by the order codes contained in the Interpretive Instruction Word. Interpretive Store Words contain a store code in bit positions 14 through 11 and an E Memory address in bit positions 10 through 1. An Interpretive Store Word is incremented by one before it is stored in F Memory and contains a ZERO in bit position 15 to distinguish it from an Interpretive Instruction Word.

30-156. MACHINE INSTRUCTIONS

30-157. The Machine Instructions can be grouped in Regular, Involuntary, and Peripheral Instructions (table 30-8). Regular Instructions can be written into a program and are executed when transferred from memory to the Central Processor and the Sequence Generator (paragraph 30-24). Involuntary Instructions cannot be written into a program and are executed at the occurrence of certain events or signals during normal operation (paragraphs 30-25 and 30-26). Peripheral Instructions also cannot be written into a program and are executed under the control of the Computer Test Set (CTS) or the Program Analyzer Console (PAC) during testing (paragraph 30-27).

TABLE 30-8
MACHINE INSTRUCTION TYPES

Group	Type	
Regular Instructions	Basic Instructions Extra Code Instructions	Sequence changing instructions Fetching and storing instructions Modifying instructions Arithmetic and logic instructions
	Channel Instructions Special Instructions	
Involuntary Instructions	Interrupting Instructions Counter Instructions	
Peripheral Instructions	Sequence changing test instructions Display and load test instructions	

30-158. REGULAR INSTRUCTIONS

30-159. Regular Instructions can be subdivided into Basic, Extra-Code, Channel, and Special Instructions. A regular instruction word consists of

three order code bits and twelve address bits as shown in figure 30-9. Three order code bits allow only eight different order codes. In order to double the number of order codes, a fourth order code bit is provided by the AGC. This fourth order code bit is entered into bit position SQ-EXT of register SQ upon the execution of instruction EXTEND. Normally, bit position SQ-EXT contains a ZERO in which case Basic Instructions are executed. Whenever instruction EXTEND is executed, a ONE is entered into bit position SQ-EXT and an Extra-Code Instruction or Channel Instruction is executed thereafter. After most Extra-Code Instructions, and all Channel Instructions, bit position SQ-EXT is reset to ZERO. Thus, sixteen different order codes can be represented by the three order code bits and the extend bit.

30-160. When E Memory is addressed, bit positions 12 and 11 of register S both contain ZERO's (table 30-2). When F Memory is addressed, bit position 12 or 11, or both, contain a ONE (table 30-3). This makes it possible to use bits 12 and 11 as additional order code bits (quarter code bits, paragraph 30-153) whenever all instructions using the same regular (whole) order code are restricted to the use of E Memory. On the other hand, an instruction word that contains ZERO's in bit positions 12 and 11 may represent an instruction which is restricted to the use of E Memory while an instruction word that contains a ONE in bit position 12 or 11, or in both, and the same regular order code, may represent an instruction which is restricted to the use of F Memory. In this case, a part of the address becomes part of the order code.

30-161. Instruction CA, for instance, is represented by regular order code 03 (table 30-9) and refers to either E Memory or F Memory. The octal point can be thought of as being located between bits 13 and 12 of the instruction word stored in memory. Instruction DAS is represented by order code 02.0 (bits 12 and 11 are ZERO's), LXCH by 02.2 (bit 11 is a ONE), INCR by 02.4 (bit 12 is a ONE), and ADS by 02.6 (bits 12 and 11 are ONE's). The last four instructions refer to E Memory only. All five instructions mentioned are Basic Instructions because bit SQ-EXT (equivalent to bit 16 of a word in memory) is a ZERO. Extra-Code Instruction DCA is represented by order code 13, and refers to E as well as F Memory. Extra-Code instructions MSU, QXCH, AUG, and DIM are represented by order codes 12.0, 12.2, 12.4, and 12.6, respectively, and refer to E Memory only. All instructions which refer to E Memory only do not enter bits 12 and 11 into register S.

30-162. Instruction CCS is represented by order code 01.0 and refers to E Memory only. Instruction TCF refers to F Memory only because it can be represented by order code 01.2, 01.4, or 01.6 (bits 12 and 11 are really a part of the address). All instructions which refer to F Memory only enter bits 12 and 11 into register S.

TABLE 30-9
ORDER CODE STRUCTURE

Quarter Codes	Regular Order Codes of Basic Instructions								Quarter Codes		
	00.	01.	02.	03.	04.	05.	06.	07.			
.0	TC	CCS	DAS	CA	CS	NDX	AD	MSK	.0		
.2		TCF	LXCH			DXCH			.2		
.4			INCR			TS			.4		
.6			ADS			XCH			.6		
Eighth Codes	Regular Order Codes of Extra Code Instructions								Quarter Codes		
	10.	11.	12.	13.	14.	15.	16.	17.			
.0	READ	DV	MSU	DCA	DCS	NDX	SU	MP	.0		
.1	WRITE		BZF				QXCH		AUG	BZMF	.2
.2	RAND	DCA									
.3	WAND						AUG		.4		
.4	ROR	DIM									.6
.5	WOR						RUPT		.7		
.6	RXOR	.7									
.7	RUPT						.7				

30-163. When channels (input/output registers) are addressed, bits 12, 11, and 10 of the instruction word contain ZERO's; therefore, these three bits can be used as additional order code bits (eighth code bits, paragraph 30-154) whenever an instruction is restricted to the use of channels. Channel Instructions READ through RXOR (table 30-9) are represented by order codes 10.0 through 10.6.

30-164. Special Instructions are Basic Instructions (bit position SQ-EXT contains a ZERO) which are defined by special 15-bit codes. Whenever the instruction word is 0.0003, 0.0004, or 0.0006, instruction RELINT, INHINT, or EXTEND, respectively, is executed instead of instruction TC K. Whenever the instruction word is 5.0017, instruction RESUME is executed instead of instruction NDX E.

30-165. Instructions CYR, SR, CYL, and EDOP have unusual characteristics. They are represented by addresses 0020, 0021, 0022, and 0023, respectively, and may be combined with many Regular Instruction codes. These addresses can be used as fractional order codes .0020, .0021, .0022, and .0023 in a similar way as quarter and eighth codes. Instruction TS CYR, for instance, cycles the quantity one place to the right as the quantity is entered into location 0020. Instruction TS SR shifts the quantity one place to the right as the quantity is entered into location 0021. Instruction TS CYL cycles the quantity one place to the left as the quantity is entered into location 0022. Instruction TS EDOP shifts the quantity seven places to the left as the quantity is entered into location 0023. Refer to table 30-1.

30-166. Regular Instructions can also be classified as Sequence Changing Instructions, Fetching and Storing Instructions, Modifying Instructions, Arithmetic and Logic Instructions, and Channel or Input/Output Instructions as shown in table 30-10 at the end of this section. This table also lists the subinstructions of which each instruction is composed (paragraph 30-23). The execution of each subinstruction takes one MCT or approximately 11.7 μ sec.

30-167. Sequence Changing Instructions

30-168. Five instructions belong in this class, which can be broken into two categories:

Transfer Control Instructions - TC K, TCF F
Decision Making Instructions - CCS E, BZF F, BZMF F

The transfer control instructions determine a single path as defined by the programmer. Instruction TC K transfers control to any location in the central processor (CP) (except locations 0003, 0004, and 0006), E Memory or F Memory, and stores a return address in register Q.

Instruction TCF F transfers control to a location in F Memory only without storing a return address. Both are Basic Instructions; TC K needs only a regular order code whereas TCF F also makes use of address bits 12 and 11 which appear as quarter codes .2, .4, and .6.

30-169. The decision making instructions branch to alternate program paths in response to defined conditions. Instruction CCS E can branch in four different ways depending on whether register A contains a positive non-zero quantity, plus zero, a negative non-zero quantity, or minus zero. Instruction BZF F branches to an alternate program path only if A contains zero; BZMF F branches to one alternate branch on a negative quantity or on zero. Instruction CCS E is a Basic Instruction which uses quarter code .0. Instructions BZF F and BZMF F are Extra-Code Instructions which can refer to F Memory only. Address bits 12 and 11 appear as quarter codes .2, .4, and .6.

30-170. Fetching and Storing Instructions

30-171. Nine instructions belong in this class which can be broken into three categories:

Copying instructions	-	CA K
		CS K
		DCA K
		DCS K
Storing instruction	-	TS E
Exchange instructions	-	XCH E
		LXCH E
		QXCH E
		DXCH E

The copying instructions are used for entering data into the accumulator A, or in the double precision accumulator A, L. Instructions CA K and CS K are Basic Instructions without quarter codes; DCA K and DCS K are Extra-Code Instructions without quarter codes.

30-172. The storing instruction is used to store partial or final results in E Memory. It is a Basic Instruction which refers to E Memory and the CP only, and requires quarter code .4.

30-173. The exchange instructions are used to exchange data between the single or double precision accumulator and E Memory. Three of the exchange instructions are Basic Instructions; one is an Extra-Code Instruction. All exchange instructions contain a quarter code.

30-174. Modifying Instructions

30-175. Two instructions belong in this class: NDX E and NDX K. The modifying instructions are to create new instructions by indexing existing instruction words with index quantities. Instruction NDX E is a Basic Instruction which refers to E Memory or the CP only and requires quarter code .0. Instruction NDX K is an Extra Code Instruction which can refer to any location and does not need a quarter code. This instruction automatically enters a ONE into bit position SQ-EXT; thus, the computer recognizes the indexed instruction as an Extra-Code Instruction. Both instructions use the same mnemonic code; the Yul compiler then enters the proper octal order code.

30-176. Arithmetic and Logic Instructions

30-177. Eleven instructions belong in this class which can be broken into five categories:

Basic ONE's complement arithmetic operations -
AD K, SU E, MP K, DV E

Add-and-store instructions - ADS E, DAS E

Incrementing instructions - INCR E, AUG E, DIM E

Basic TWO's complement arithmetic operations - MSU E

Boolean operations - MSK K

The functions of these instructions are described in table 30-10. The operation of the Adder is discussed in paragraphs 30-42 through 30-46. Three instructions can refer to any location and do not need a quarter code while the other eight instructions can refer to E Memory and the CP only and require a quarter code.

30-178. Instructions INCR E, AUG E, and DIM E test for overflow. Whenever time counter 0025 is addressed and an overflow occurs, the incrementing of time counter 0024 is initiated. Whenever time counter 0026, 0027, or 0030 is addressed and an overflow occurs, transfer of program control to certain program sections is initiated (table 30-4).

30-179. Channel Instructions

30-180. Seven instructions belong in this class which can be broken into two categories:

Read instructions - READ H, RAND H, ROR H, RXOR H

Write instructions - WRITE H, WAND H, WOR H

The seven instructions can also be broken into four categories:

Straight read and write instructions - READ H, WRITE H

AND instructions - RAND H, WAND H

OR instructions - ROR H, WOR H

Exclusive OR instruction - RXOR H

The functions of these instructions are described in table 30-10. All Channel Instructions are eighth code instructions. CP registers L and Q can be read out and written into by means of the Channel Instructions when channel address 01 or 02, respectively, is used (paragraphs 30-71 and 30-72).

30-181. Special Instructions

30-182. Eight instructions belong in this class which can be broken into two categories:

Instructions consisting of a certain order code plus a special address code - RELINT, INHINT, EXTEND, RESUME

Instructions consisting of certain addresses which can be combined with many order codes - CYR, SR, CYL, EDOP

The functions of these instructions are described in table 30-10 and in paragraphs 30-135, 30-164, and 30-165.

30-183. INVOLUNTARY INSTRUCTIONS

30-184. The Involuntary Instructions can be divided into Interrupting and Counter Instructions. The Interrupting Instructions cannot be written into a program although they contain order codes. These order codes are supplied by the computer and entered into register SQ under the control of the Interrupt Priority Control at the occurrence of certain events or signals. Whenever an Interrupting Instruction is executed, the execution of a current program section is interrupted and another program section, as defined by the event, is executed instead (table 30-6 and paragraph 30-132).

30-185. Counter Instructions do not have an order code and are executed under the control of the Counter Priority Control at the occurrence of certain signals or events. Whenever a Counter Instruction is executed, the execution of the current program is delayed for about 12 μ sec and the counter specified by the signal is incremented, decremented, etc. (table 30-7 and paragraph 30-138).

30-186. PERIPHERAL INSTRUCTIONS

30-187. The Peripheral Instructions can be broken into three categories:

Transfer instruction - TCSAJ

Instructions reading from or writing into E and F Memory -
FETCH K, STORE E.

Instructions which read data out of or into channel - INOTRD H,
INOTLD H.

TABLE 30-10
MACHINE INSTRUCTIONS

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	Description ① ④										
REGULAR INSTRUCTIONS													
Sequence Changing Instructions													
TC K	00.	TC0	"Transfer Control to K" Takes next instruction from K and stores return address (I+1) in Q.										
TCF F	01.2 01.4 01.6	TCF0	"Transfer Control to Fixed F" Takes next instruction from F without changing c(Q).										
CCS E	01.0	CCS0 STD2	"Count, Compare, and Skip on E" Branches according to c(E) and stores in A the c(E) diminished by one.										
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%; text-align: center;">c(E)</th> <th style="width: 30%; text-align: center;">Transfers to</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">positive nonzero</td> <td style="text-align: center;">I+1</td> </tr> <tr> <td style="text-align: center;">plus zero</td> <td style="text-align: center;">I+2</td> </tr> <tr> <td style="text-align: center;">negative nonzero</td> <td style="text-align: center;">I+3</td> </tr> <tr> <td style="text-align: center;">minus zero</td> <td style="text-align: center;">I+4</td> </tr> </tbody> </table>		c(E)	Transfers to	positive nonzero	I+1	plus zero	I+2	negative nonzero	I+3	minus zero	I+4
c(E)	Transfers to												
positive nonzero	I+1												
plus zero	I+2												
negative nonzero	I+3												
minus zero	I+4												
BZF F	16.2 16.4 16.6	BZF0 STD2	"Branch on Zero to Fixed F" Branches according to c(A).										
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 70%; text-align: center;">c(A)</th> <th style="width: 30%; text-align: center;">Transfers to</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">plus or minus zero</td> <td style="text-align: center;">F (subinstruction STD2 is not executed)</td> </tr> <tr> <td style="text-align: center;">non zero</td> <td style="text-align: center;">I+1 (subinstruction STD2 is executed)</td> </tr> </tbody> </table>		c(A)	Transfers to	plus or minus zero	F (subinstruction STD2 is not executed)	non zero	I+1 (subinstruction STD2 is executed)				
c(A)	Transfers to												
plus or minus zero	F (subinstruction STD2 is not executed)												
non zero	I+1 (subinstruction STD2 is executed)												

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	Description ① ④			
REGULAR INSTRUCTIONS						
Sequence Changing Instructions (cont)						
BZMF F	12.2 12.4 12.6	BZMF0 STD2	"Branch on Zero or Minus to Fixed F" Branches according to c(A).			
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">c(A)</th> <th style="text-align: center;">Transfers to</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">zero or negative nonzero</td> <td style="text-align: center;">F (subinstruction STD2 is not executed)</td> </tr> <tr> <td style="text-align: center;">positive nonzero</td> <td style="text-align: center;">I+1 (subinstruction STD2 is executed)</td> </tr> </tbody> </table>	c(A)	Transfers to	zero or negative nonzero
c(A)	Transfers to					
zero or negative nonzero	F (subinstruction STD2 is not executed)					
positive nonzero	I+1 (subinstruction STD2 is executed)					
Fetching and Storing Instructions						
CA K	03.	CA0 STD2	"Clear and Add K" Enters c(K) into A. Takes next instruction from I+1.			
CS K	04.	CS0 STD2	"Clear and Subtract K" Enters the complemented c(K) into A. Takes next instruction from I+1.			
DCA K	13.	DCA0 DCA1 STD2	"Double Clear and Add K" Enters c(K, K+1) into A and L. Takes next instruction from I+1.			
DCS K	14.	DCS0 DCS1 STD2	"Double Clear and Subtract K" Enters the complemented c(K, K+1) into A and L. Takes next instruction from I+1.			

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

$\triangle 1$ Symbolic Instruction Word	$\triangle 2$ Order Code	$\triangle 3$ Sub- instructions Executed	Description $\triangle 1$ $\triangle 4$
REGULAR INSTRUCTIONS			
Fetching and Storing Instructions (cont)			
TS E	05.4	TS0 STD2	"Transfer to Storage E" If A does not contain an overflow quantity, instruction enters c(A) into E and takes next instruction from I+1. If A contains a positive overflow, instruction enters c(A) without overflow bit into E, enters plus one into A, and takes next instruction from I+2. If A contains a negative overflow, instruction enters c(A) without overflow bit into E, enters minus one into A, and takes next instruction from I+2.
XCH E	05.6	XCH0 STD2	"Exchange A and E" Exchanges c(A) with c(E). Takes next instruction from I+1.
LXCH E	02.2	LXCH0 STD2	"Exchange L and E" Exchanges c(L) with c(E). Takes next instruction from I+1.
QXCH E	12.2	QXCH0 STD2	"Exchange Q and E" Exchanges c(Q) with c(E). Takes next instruction from I+1.
DXCH E	05.2	DXCH0 DXCH1 STD2	"Double Exchange A and E" Exchanges c(A, L) with c(E, E+1). Takes next instruction from I+1.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	Description ① ④
REGULAR INSTRUCTIONS			
Modifying Instructions			
NDX E	05.0	NDX0 NDX1	"Index Next Basic Instruction with E" Adds c(E) to c(I+1) and takes sum as next instruction.
NDX K	15.	NDXX0 NDXX1	"Index Next Extra-Code Instruction with K" Adds c(K) to c(I+2) and takes sum as next instruction. Retains the ONE in bit position SQ-EXT.
Arithmetic and Logic Instructions			
AD K	06.	AD0 STD2	"Add K" Adds c(K) to c(A) and stores sum in A. Takes next instruction from I+1.
SU E	16.0	SU0 STD2	"Subtract E" Subtracts c(E) from c(A) and stores the difference in A. Takes next instruction from I+1.
MP K	17.	MP0 MPI MP3	"Multiply K" Multiplies c(K) by c(A) and stores double precision product in A and L (signs in A and L agree). Takes next instruction from I+1.

TABLE 30-10

MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	① ④ Description
REGULAR INSTRUCTIONS			
Arithmetic and Logic Instructions (cont)			
DV E	11.0	DV0 DV1 DV3 DV7 ③ DV6 DV4 ⑤ STD2	"Divide by E" Divides double precision quantity c(A, L) by c(E), stores quotient in A and remainder in L. Takes next instruction from I+1. Signs of b(A) and b(L) need not agree. Sign of remainder equals sign of dividend.
ADS E	02.6	ADS0 STD2	"Add to Storage E" Adds c(A) and c(E), stores sum with overflow bit in A and sum without overflow bit in E.
DAS E	02.0	DAS0 DAS1 STD2	"Double Add to Storage E" Adds c(A, L) and c(E, E+1) and stores sum without overflow bit in E and E+1. Enters plus one into A in case of positive overflow, minus one in case of negative overflow, and plus zero in case of no overflow. Enters plus zero into L and takes next instruction from I+1.
INCR E	02.4	INCR0 STD2	"Increment E" Adds plus one to c(E) and stores incremented quantity in E. Takes next instruction from I+1.
AUG E	12.4	AUG0 STD2	"Augment E" Increases the magnitude of the quantity contained in E by one and stores the augmented quantity in E. Takes next instruction from I+1.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

$\triangle 1$ Symbolic Instruction Word	$\triangle 2$ Order Code	$\triangle 3$ Sub- instructions Executed	Description $\triangle 1$ $\triangle 4$
REGULAR INSTRUCTIONS			
Arithmetic and Logic Instructions (cont)			
DIM E	12.6	DIM0 STD2	"Diminish E" Decreases the magnitude of the quantity contained in E by one and stores diminished quantity in E. Takes next instruction from I+1.
MSU E	12.0	MSU0 STD2	"Modular Subtract E" Subtracts cyclic TWO's complement number in E from cyclic TWO's complement number in A and stores difference expressed in ONE's complement number in A. Takes next instruction from I+1.
MSK K	07.	MSK0 STD2	"Mask with K" AND's c(A) with c(K) and stores logical product in A. Takes next instruction from I+1.
Channel Instructions			
READ H	10.0	READ0 STD2	"Read H" Enters c(H) into A. Takes next instruction from I+1.
WRITE H	10.1	WRITE0 STD2	"Write H" Enters c(A) into H. Takes next instruction from I+1.
RAND H	10.2	RAND0 STD2	"Read and AND H" AND's c(A) and c(H) and stores logical product in A. Takes next instruction from I+1.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	④ Description
REGULAR INSTRUCTIONS			
Channel Instructions (cont)			
WAND H	10.3	WAND0 STD2	"Write and AND H" AND's c(A) and c(H), and stores logical product in A and H. Takes next instruction from I+1.
ROR H	10.4	ROR0 STD2	"Read and OR H" OR's c(A) and c(H), and stores logical sum in A. Takes next instruction from I+1.
WOR H	10.5	WOR0 STD2	"Write and OR H" OR's c(A) and c(H), and stores logical sum in A and H. Takes next instruction from I+1.
RXOR H	10.6	RXOR0 STD2	"Read and Exclusive OR H" Forms exclusive OR from c(A) and c(H), and stores result in A. Takes next in- struction from I+1.
Special Instructions			
EXTEND	00.0006	STD2	"Extend" Enters a ONE into bit position SQ-EXT. The next instruction, taken from I+1, is an Extra- Code Instruction.
INHINT	00.0004	STD2	"Inhibit Interrupt" Sets inhibit interrupt switch in Interrupt Priority Control to pre- vent interruption of program execution. Takes next instruc- tion from I+1.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

$\triangle 1$ Symbolic Instruction Word	$\triangle 2$ Order Code	$\triangle 3$ Sub- instructions Executed	$\triangle 1$ Description $\triangle 4$
REGULAR INSTRUCTIONS			
Special Instructions (cont)			
RELINT	00.0003	STD2	"Release Inhibit Interrupt" Resets inhibit interrupt switch to allow program interruption in favor of a programmed operation of higher priority. Takes next instruction from I+1.
RESUME	05.0017	NDX0 RSM3	"Resume Interrupted Program" Takes next instruction from location 0017 and enters content of location 0015 into Z. Thus, execution of the interrupted program section is resumed.
CYR	.0020	$\triangle 6$	"Cycle Right" Cycles quantity, which is entered into location 0020, one place to the right.
SR	.0021	$\triangle 6$	"Shift Right" Shifts quantity, which is entered into location 0021, one place to the right.
CYL	.0022	$\triangle 6$	"Cycle Left" Cycles quantity, which is entered into location 0022, one place to the left.
EDOP	.0023	$\triangle 6$	"Edit Operator" Shifts quantity, which is entered into location 0023, seven places to the right.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	④ Description
INVOLUNTARY INSTRUCTIONS			
Interrupting Instructions			
RUPT	10. 7	RUPT0 RUPT1 STD2	"Interrupt Program Execution" Takes next instruction from address supplied by Interrupt Priority Control. Stores c(B) in location 0017 and c(Z) in location 0015.
GO	00. 00. 4000	GOJ1 TC0	"Go" Takes next instruction from loca- tion 04000 in E Memory.
Counter Instructions			
PINC C	none	PINC	"Plus Increment C" Adds one to c(C) and stores incremented quantity in C.
MINC C	none	MINC	"Minus Increment C" Subtracts one from c(C) and stores decremented quantity in C.
DINC C	none	DINC	"Diminish Increment C" De- creases the magnitude of the quantity contained in C by one and stores diminished quantity in C.
PCDU C	none	PCDU	"Plus CDU C" Adds one to cyclic TWO's com- plement number in C and stores incremented quantity in C.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	④ Description
INVOLUNTARY INSTRUCTIONS			
Counter Instructions (cont)			
MCDU C	none	MCDU	"Minus CDU C" Subtracts one from cyclic TWO's complement number in C and stores decremented quantity in C.
SHINC C	none	SHINC	"Shift Increment C" Shifts c(C) one place to the left and enters a ZERO into bit position 0 of C.
SHANC C	none	SHANC	"Shift and Add Increment C" Shifts c(C) one place to the left and enters a ONE into bit position 0 of C.
PERIPHERAL INSTRUCTIONS			
TCSAJ K	00.	TCSAJ3 STD2	"Transfer control to specified address K" Takes next instruction from address which is supplied by GSE.
FETCH K	none	FETCH0 FETCH1	"Fetch K"; displays c(K) on GSE. Address K is supplied by GSE.
STORE E	none	STORE0 STORE1	"Store E"; data supplied by GSE is entered into E by GSE. Address E is also supplied by GSE.

TABLE 30-10
MACHINE INSTRUCTIONS (cont)

① Symbolic Instruction Word	② Order Code	③ Sub- instructions Executed	① Description ④
PERIPHERAL INSTRUCTIONS (cont)			
INOTRD H	none	INOTRD	"In Out Read H"; displays c(H) on GSE. Channel address H is supplied by GSE.
INOTLD H	none	INOTLD	"In Out Load H"; data supplied by GSE is entered into H by GSE. Channel address H is supplied by GSE.

- ① Address symbol K can represent any address in the Central Processor (CP), E Memory or F Memory.
Address symbol F can represent an address in F Memory only.
Address symbol E can represent an address in the CP or E Memory only.
Address symbol H can represent any channel address.
Address symbol C can represent any counter address.
- ② Entered into SQ, or SQ and S.
- ③ The execution of each subinstruction, except DV0 and DV4, takes one MCT or about 11.7 μ sec. DV0 and DV4 together require 1 MCT.
- ④ Address symbol I represents address of instruction described.
Register symbols A, L, Q, B, S, SQ, and G refer to registers defined in table 30-1.
Expression c(K) means "content of location (or register) K".
- ⑤ Execution of these seven subinstructions takes only six MCT's.
- ⑥ The code which can be used with any K or E instruction, is contained in register S. Whenever address 0020, 0021, 0022, or 0023 is contained in register S, register G cycles or shifts the quantity it receives from a CP register before that quantity is transferred to one of the four locations (paragraph 30-41).

ISSUE 30
APPENDIX A

COMMAND MODULE AGC SUBSYSTEM
INPUT AND OUTPUT SIGNALS

All input and output lines or signals passing through connector A51 of the AGC, and connectors J9 of the Main Panel DSKY and the Navigation Panel DSKY are listed in table 30A-1 of this appendix. Information is arranged by order of line or signal numbers frequently referred to in the main body of this issue. The numbers of the connecting pins of connectors A51 and J9 are given in columns 2 through 4 of the table while various signal names are listed in columns 5 and 6. The various types of interface circuits provided are described in figure 30A-1. A short description of the signals is contained in the last column of table 30A-1. Numbers preceded by an A or B indicate module numbers.

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
001	516 616	-	-	CLK { XC001H XC001L	MASTER CLOCK	Gate 37137 of the Timer generates 1.024 Mpps signal CLK which controls interface circuit 1XT of A25. Master clock output pulses are used in various spacecraft systems.
002	358 458	-	-	ALT1 { XA002H XA002L	NC	Gates 46109 and 46110 of the Altitude Meter Control (par 30-123 through 30-125) generate serial data pulses ALT0 and ALT1 which control interface circuits 5XT and 4XT of A29.
003	357 457	-	-	ALT0 { XA003H XA003L	NC	
004	558	-	-	DE004 ULLTHR	ULLAGE THRUST PRES	Interface circuit 1D of A29 receives DC signals from the spacecraft and feeds gate 44101 of bit position 1 of channel 30 (table 30-5D).
007	657	-	-	DE007 LFTOFF	LIFT OFF (SIVB)	Interface circuit 2D of A29 receives DC signals from the spacecraft and feeds gate 44113 of bit position 5 of channel 30 (table 30-5D).
008	354 454	-	-	THRST+ { XA008H XA008L	NC	Gates 46247 and 46248 of the EMS and Thrust Drive Control (par 30-100 through 30-104) generate signals THRST+ and THRST- which control interface circuits 8XT and 9XT of A29.
009	353 453	-	-	THRST- { XA009H XA009L	NC	
010	356 456	-	-	ALRT1 { XA010H XA010L	NC	Gates 46111 and 46112 of the Altitude Meter Control (par 30-123 through 30-125) generate serial data pulses ALRT0 and ALRT1 which control interface circuits 7XT and 6XT of A29.
012	355 455	-	-	ALRT0 { XA012H XA012L	NC	
011	613	-	-	ENON CB011	SPS ENG ON/OFF	Bit position 7 of channel 12 (table 30-5A) controls gates 43228 and 43229 to generate signals ENON and ENOFF which control interface circuits 19C and 18C of A26. DC output signals control the spacecraft engine.
013	513	-	-	ENOFF CB013	NC	
014	133 233	-	-	Y-014H } Y-014L } DKSTRT	DLNK START	Interface circuits 1Y, 2Y, and 3Y of A27 receive pulses from the NA programmer and feed gates 47101, 45447, and 47227 of the Downlink Converter (par 30-126 and 30-127).
015	132 232	-	-	Y-015H } Y-015L } DKEND	DLNK END	
016	130	-	-	Y-016H } Y-016L } DKBSNC	DLNK SYNC	
	230	-	-			

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
017	352 452	-	-	DKDATA { X-017H X-017L	DLNK DATA	Gate 47256 of the Downlink Converter (par 30-126 and 30-127) generates signal DKDATA which controls interface circuit 1XT of A28. The serial data pulses are fed into the NA Programmer.
018 019 020 021 022 023	655 555 654 554 653 553	- - - - - -	- - - - - -	DE018 TRAN+X DE019 TRAN-X DE020 TRAN+Y DE021 TRAN-Y DE022 TRAN+Z DE023 TRAN-Z	+X TRANS COMM (MAN) -X TRANS COMM (MAN) +Y TRANS COMM (MAN) -Y TRANS COMM (MAN) +Z TRANS COMM (MAN) -Z TRANS COMM (MAN)	Interface circuits 4D through 9D of A29 receive DC signals from the manual translation control and feed bit positions 7 through 12 (gates 44216 through 44220, and 44232) of channel 31 (table 30-5E).
024 025	129 229 128 228	- - - -	- - - -	YG024H } UPL0 YG024L } YG025H } UPL1 YG025L }	ULNK0 ULNK1	Interface circuits 4Y and 5Y of A27 receive serial data pulses from the uplink equipment and feed gates 46304 and 46305 of the Inlink Control (par 30-116 through 30-119).
028	413	-	-	ALTSNC CB028	NC	Gate 46132 of the Altitude Meter Control (par 30-123 through 30-125) generates signal ALTSNC which controls interface circuit 17C of A26.
029 030	350 450 349 449	- - - -	- - - -	EMS+ { XA029H XA029L EMS- { XA030H XA030L	ENTRY VEL + NC ENTRY VEL - NC	Gates 46254 and 46258 of the EMS and Thrust Drive Control (par 30-100 through 30-104) generate signals EMS+ and EMS- which control interface circuits 10XT and 11XT of A29.
031 032	127 227 126 226	- - - -	- - - -	YG031H } RRIN0 YG031L } YG032H } RRIN1 YG032L }	NC NC	Interface circuits 6Y and 7Y of A27 receive serial data pulses from the rendezvous radar and feed gates 45349 and 44347 of the Radar Control (par 30-105 through 30-109).
033 034	- -	- -	- -	DE033 IN3212 DE034 IN3213	SPARE CHN 32-12 NC SPARE CHN 32-13 NC	Interface circuits 3D and 4D of A26 are able to receive DC signals and feed bit positions 12 and 13 (gates 44134 and 44137) of channel 32 (table 30-5F).
039	630	-	-	DE039 LVDAGD	NC	Interface circuit 17D of A28 is able to receive DC signals and feeds bit position 8 (gate 44123) of channel 33 (table 30-5G).

(cont)

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
040	641	-	-	DE040 HOLFUN	HOLD FUNCTION	Interface circuit 7D of A28 receives DC signal from the auto stabilization and feeds bit position 13 (gate 44233) of channel 31 (table 30-5E).	
041	348 448	-	-	RRRANG { XA041H XA041L	NC	Gates 45328 through 45333, 45345, and 45346 of the Radar Control (par 30-105 through 30-109) generate control signals (90 msec bursts of 100 kpps) RRRANG, RRRARA, LRXVEL, LRYVEL, LRZVEL, LRRANG, RRSYNC, and LRSYNC which control interface circuits 4XT through 11XT of A28. Gates 49218 and 49219 generate timing signals (3.2 kpps) RRRST and LRRST which control interface circuits 2XT and 3XT of module A25.	
042	347 447	-	-	RRRARA { XA042H XA042L	NC		
043	344 444	-	-	LRXVEL { XA043H XA043L	NC		
044	343 443	-	-	LRYVEL { XA044H XA044L	NC		
045	342 442	-	-	LRZVEL { XA045H XA045L	NC		
046	341 441	-	-	LRRANG { XA046H XA046L	NC		
047	346 446	-	-	RRSYNC { XA047H XA047L	NC		
048	345 445	-	-	RRRST { XC048H XC048L	NC		
051	340 440	-	-	LRSYNC { XA051H XA051L	NC		
052	339 439	-	-	LRRST { XC052H XC052L	NC		
060	523	-	-	DE060 LEMATT	LEM ATTACHED		Interface circuit 14D of A27 receives DC signals from spacecraft and feeds bit position 11 (gate 44131) of channel 32 (table 30-5F).
061	530	-	-	DE061 LRRLSC	NC		Interface circuit 18D of A28 is able to receive DC signals and feeds bit position 9 (gate 44126) of channel 33 (table 30-5G).
064	629	-	-	DE064 RRPONA	NC	Interface circuit 1D of A27 is able to receive DC signals and feeds bit position 2 (gate 44105) of channel 33 (table 30-5G).	
065	541	-	-	DE065 FREFUN	FREE FUNCTION	Interface circuit 8D of A28 receives DC signal from the auto stabilization and feeds bit position 14 (gate 44233) of channel 31 (table 30-5E).	

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
066 067 068	640 540 557	- - -	- - -	DE066 S4BSAB DE067 SMSEPR DE068 GUIREL	SIVB SEPARATE/ABORT SM SEPARATE GUID REF RELEASE	Interface circuits 9D, 10D of A28, and 3D of A29 receive DC signals from the spacecraft and feed bit positions 4, 2, and 6 (gates 44110, 44104, and 44116) of channel 30 (table 30-5D).
069	529	-	-	DE069 RRRLSC	NC	Interface circuit 2D of A27 is able to receive DC signals and feeds bit position 2 (gate 44108) of channel 33 (table 30-5G).
071 072	125 225 124 224	- - -	- - -	YG071H } LRIN0 YG071L } YG072H } LRIN1 YG072L }	NC NC	Interface circuits 8Y and 9Y of A27 are able to receive serial data pulses and feed gates 45355 and 45353 of the Radar Control (par 30-105 through 30-109).
078 079	518 618 517 617	- - -	- - -	OTLNK0 { XA078H XA078L OTLNK1 { XA079H XA079L	"0" BIT CROSS OUT NC "1" BIT CROSS OUT NC	Gates 46147 and 46149 of Outlink Control (par 30-120 through 30-122) generate serial data pulses OTLNK0 and OTLNK1 which control interface circuits 6XT and 7XT of A27. Outputs are provided for the cross link equipment but not connected.
080 081	123 223 122 222	- - -	- - -	YG080H } XLNK0 YG080L } YG081H } XLNK1 YG081L }	"0" BIT CROSS IN NC "1" BIT CROSS IN NC	Interface circuits 10Y and 11Y of A27 are able to receive serial data pulses from the cross link equipment and feed gates 46306 and 46307 of the Inlink Control (par 30-116 through 30-119). Inputs are not connected.
082	636	-	-	DE082 SPSRDY	SPS READY	Interface circuit 13D of A28 receives DC signals from the spacecraft and feeds bit position 3 (gate 44107) of channel 30 (table 30-5D).
083	538	-	-	DE083 BLKUPL/	ACCEPT UPLNK	Interface circuit 12D of A28 receives DC signals from the UPTTEL switch and feeds gate 46308 of Inlink Control (par 30-116 through 30-119).
084	638	-	-	DE084 IN3008	SPARE CHN30-08 NC	Interface circuit 11D of A28 is able to receive DC signals and feeds bit position 8 (gate 44122) of channel 32 (table 30-5D).
085	351 451	-	-	DKDATB { X-085H X-085L	DLNK DATA NC	Gate 47261 of the Downlink Converter (par 30-126 and 30-127) generates signal DKDATB which controls interface circuit 1XT of A29. The signal is identical to signal 017.

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
086	639	-	-	+28VDC RD086	66/67	Resistor 5R of A28 provides +28VDC for external equipment.
087	647	-	-	+28COM RD087	40/65/83/60	Resistors 1R and 2R of A28 in parallel provide +28VDC for external equipment.
088	-	-	-	-	40/65/83/60	Provided with signal 087.
091	537	-	-	+28COM RD091	40/65	Resistor 8R of A28 provides +28VDC for external equipment.
093	628	-	-	DE093 MANR+P	+PITCH MAN ROT	Interface circuits 3D through 8D of A27 receive DC signals from manual rotation control and feed bit positions 1 through 6 (gates 44201 through 44205, and 44215) of channel 31 (table 30-5E).
094	528	-	-	DE094 MANR-P	-PITCH MAN ROT	
095	627	-	-	DE095 MANR+Y	+YAW MAN ROT	
096	527	-	-	DE096 MANR-Y	-YAW MAN ROT	
097	626	-	-	DE097 MANR+R	+ROLL MAN ROT	
098	526	-	-	DE098 MANR-R	-ROLL MAN ROT	
101	620	-	-	+28COM RD101	SPARE NC	Resistor 6R of A27 provides +28VDC for external equipment.
102	549	-	-	DE102 MARK	MARK	Interface circuit 13D of A29 receives DC signals from Optics and feeds bit position 6 (gate 45225) of channel 16 (table 30-5J).
103	550	-	-	DE103 MRKRST	MARK RESET	Interface circuit 11D of A29 receives DC signals from Optics and resets bit positions 6 and 7 (via gate 45233) of channel 16 (table 30-5J).
104	649	-	-	DE104 ZEROP	ZERO OPT	Interface circuits D12, D10, and D14 of A29 receive DC signals from the Optics and feed bit positions 4, 5, and 6 (gates 44111, 44114, and 44117) of channel 33 (table 30-5G).
106	650	-	-	DE106 OPMSW2	OPT MODE SW2 (AGC CONTRL)	
107	648	-	-	DE107 OPMSW3	OPT MD SW3 (STR TR ON)	

(cont)

TABLE 30A-1
 COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings [△]	Name Used in DD Memo 185 [△]	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
108	152	-	-	YG108H } YG108L } SHAFTP	OPT+X (SHAFT)	Interface circuits 7Y through 10Y of A29 receive incremental pulses from the Optics CDU's and feed the counter priority control gates 31302, 31309, 31215, and 31224, and the alarm control gates 49439 and 49440, par 30-141L.
109	252	-	-	YG109H } YG109L } SHAFTM	OPT-X (SHAFT)	
110	151	-	-	YG110H } YG110L } TRNP	OPT+Y (TRUNN)	
111	251	-	-	YG111H } YG111L } TRNM	OPT-Y (TRUNN)	
	150	-	-			
112	525	-	-	DE112 OPCDFL	OPT CDU FAIL	Interface circuits 10D and 9D of A27 receive DC signals from the Optics CDU's and the ISS, and feed bit positions 7 and 14 (gates 44119 and 44139) of channel 30 (table 30-5D).
113	625	-	-	DE113 ISSTOR	ISS TURN ON REQUEST	
114	338	-	-	SHFTDP { XA114H { XA114L	+X OPT CDU (SHAFT)	Gates 48348, 48349, 48336, and 48339 of the CDU Drive Control (par 30-90 through 30-94) generate drive pulses SHFTDP, SHFTDM, TRNDP, and TRNDM which control interface circuits 8XT through 11XT of A27. The output pulses drive the Optics CDU's.
115	438	-	-	SHFTDM { XA115H { XA115L	-X OPT CDU (SHAFT)	
116	337	-	-	TRNDP { XA116H { XA116L	+Y OPT CDU (TRUNN)	
117	437	-	-	TRNDM { XA117H { XA117L	-Y OPT CDU (TRUNN)	
	336	-	-			
118	148	-	-	YG118H } YG118L } CDUXP	+X CDU (OUT GMBL)	Interface circuits 11Y of module A29, and 1Y through 5Y of A28 receive incremental pulses from the IMU CDU's and feed the counter priority control gates 31102, 31109, 31115, 31124, 31202, and 31209, and the alarm control gates 49437 and 49438 (par 30-141L).
119	248	-	-	YG119H } YG119L } CDUXM	-X CDU (OUT GMBL)	
120	147	-	-	YG120H } YG120L } CDUYP	+Y CDU (INN GMBL)	
121	247	-	-	YG121H } YG121L } CDUYM	-Y CDU (INN GMBL)	
122	146	-	-	YG122H } YG122L } CDUZP	+Z CDU (MID GMBL)	
123	246	-	-	YG123H } YG123L } CDUZM	-Z CDU (MID GMBL)	
	145	-	-			
	245	-	-			
	144	-	-			
	244	-	-			
124	624	-	-	DE124 CDUFAL	CDU FAIL (ISS)	Interface circuit 11D of A27 receives DC signals from the CDU's and feeds bit position 12 (gate 44133) of channel 30.

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COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
125	524	-	-	DE125 TEMPIN	TEMP WITHIN LIMITS	Interface circuit 12D of A27 receives DC signals from the IMU and feeds bit position 15 (gate 44142) of channel 30 and gate 45262 of the Alarm Control.	
126	334	-	-	CDUXDP { XA126H	CDU +X (OUT GMBL)	Gates 48308, 48309, 48318, 48319, 48326, and 48329 of the CDU Drive Control (par 30-90 through 30-94) generate drive pulses CDUXDP through CDUZMD (column 5) which control interface circuits 4XT through 7XT of A25 and 2XT and 3XT of module A26. The output pulses drive the IMU CDU's.	
	434	-	-	{ XA126L			
127	333	-	-	CDUXDM { XA127H			CDU -X (OUT GMBL)
	433	-	-	{ XA127L			
128	332	-	-	CDUYDP { XA128H			CDU +Y (INN GMBL)
	432	-	-	{ XA128L			
129	330	-	-	CDUYDM { XA129H			CDU -Y (INN GMBL)
	430	-	-	{ XA129L			
130	329	-	-	CDUZDP { XA130H	CDU +Z (MID GMBL)		
	429	-	-	{ XA130L			
131	328	-	-	CDUZDM { XA131H	CDU -Z (MID GMBL)		
	428	-	-	{ XA131L			
132	139	-	-	YG132H } PIPAX+	+DVX (STROBED)	Interface circuits 6Y through 11Y of A28 receive incremental pulses from the PIPA's and feed gates 53461, 53361, 53362, 54461, 54361, and 54362 of the Counter Priority Control. The Counter Priority Control generates signals PIPXP, PIPXM, PIPYP, PIPYM, PIPZP, and PIPZM which set the priority cells and which are fed into gates 49440 through 49442 of the Alarm Control (par 30-141L).	
	239	-	-	YG132L } PIPAX+			
133	138	-	-	YG133H } PIPAX-	-DVX (STROBED)		
	238	-	-	YG133L } PIPAX-			
134	137	-	-	YG134H } PIPAY+	+DVY (STROBED)		
	237	-	-	YG134L } PIPAY+			
135	136	-	-	YG135H } PIPAY-	-DVY (STROBED)		
	236	-	-	YG135L } PIPAY-			
136	135	-	-	YG136H } PIPAZ+	+DVZ (STROBED)		
	235	-	-	YG136L } PIPAZ+			
137	134	-	-	YG137H } PIPAZ-	-DVZ (STROBED)		
	234	-	-	YG137L } PIPAZ-			
139	327	-	-	PIPINT { XC139H	PIPA INTERR	Gates 49208 and 49204 of the Timer generate pulses PIPINT and PIPASW which control interface circuits 9XT and 10XT of A25. The output pulses interrogate and switch the PIPA's at a rate of 3.2 kpps.	
	427	-	-	{ XC139L			
140	326	-	-	PIPASW { XC140H	PIPA SWCH		
	426	-	-	{ XC140L			
141	623	-	-	DE141 IMUFAL	IMU FAIL	Interface circuit 13D of A27 receives DC signals from the IMU and feeds bit position 13 (gate 44136) of channel 30 (table 30-5D).	

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
142	121	-	-	GYXP { XB142H	+X GYRO SELECT	Gates 46424 through 46427, 46432, 46433, and 46443 of the Gyro Drive Control (par 30-95 through 30-99) generate drive pulses GYXP through GYZM (column 5) and reset pulses GYRRST which control interface circuits 2XT and 3XT of A27, A28, and A29, and 5XT of A27. The output pulses drive and reset the gyros in the IMU.
143	221	-	-	{ XB142L		
	120	-	-	GYXM { XB143H	-X GYRO SELECT	
	220	-	-	{ XB143L		
144	119	-	-	GYYP { XB144H	+Y GYRO SELECT	
	219	-	-	{ XB144L		
145	118	-	-	GYYM { XB145H	-Y GYRO SELECT	
	218	-	-	{ XB145L		
146	321	-	-	GYZP { XB146H	+Z GYRO SELECT	
	421	-	-	{ XB146L		
147	320	-	-	GYZM { XB147H	-Z GYRO SELECT	
	420	-	-	{ XB147L		
148	318	-	-	GYRRST { XA148H	GYRO RESET	
	418	-	-	{ XA148L		
149	323	-	-	800 SET { XC149H	800 PPS SET	Gates 49209 and 49210 of the Timer generate 800 pps signals which control interface circuits 10XT and 11XT of A26. The timing pulses are provided for external equipment.
	423	-	-	{ XC149L		
150	322	-	-	800 RST { XC150H	800 PPS RESET	
	422	-	-	{ XC150L		
151	316	-	-	3200A { XC151H	3.2 KPPS A	Gates 49211 through 49213 and 49215 of the Timer generate 3200 pps signals which control interface circuits 4XT through 7XT of A26. The timing pulses are provided for external equipment.
	416	-	-	{ XC151L		
152	315	-	-	3200B { XC152H	3.2 KPPS B	
	415	-	-	{ XC152L		
153	-	-	-	3200C { XC153H	3.2 KPPS C NC	
	-	-	-	{ XC153L		
154	-	-	-	3200D { XC154H	3.2 KPPS D NC	
	-	-	-	{ XC154L		
155	117	-	-	12 KPPS { XC155H	12.8 KPPS (PWR SUP SYNC)	Gate 49217 of the Timer generates 12 kpps signals which control interface circuit 9XT of A26. The timing pulses are provided for external equipment.
	217	-	-	{ XC155L		
158	534	-	-	DE158 CTLSAT	S/C CNTRL OF SAT	Interface circuits 18D of module A27 and 14D of A28 receive DC signals from the spacecraft and feed bit position 10 (gate 44128) of channel 30 (table 30-5D) and bit position 15 (gate 44235) of channel 31 (table 30-5E).
159	536	-	-	DE159 GCAPCL	G/C AUTOPILOT CNTRL	

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
160	112	-	-	S4BTAK CB160	SIVB TAKE OVER ENABLE TVC ENABLE STAR TRACKERS ON	Bit positions 9, 8, and 3 (gates 43332, 43160, and 43312) of channel 12 (table 30-5A) generate signals S4BTAK, TVCNAB, and STARON which control interface circuits 20C, 23C, and 22C of A26. The interface circuits operate circuits in the spacecraft and the star tracker.
161	412	-	-	TVCNAB CB161		
162	312	-	-	STARON CB162		
166	652	-	-	+28COM RD166	+28V COMP. (TP)	Resistor 6R of A29 provides +28VDC for external equipment.
167	{ 161 261 361 461 561 661	-	-	WD167	+28 A BUSS	AGC power inputs connected to power supplies, modules 30 and 31.
168	{ 159 259 359 459 559 659	-	-	WD168	+28 B BUSS	
169	{ 160 260 360 460 560 660	-	-	WD169	0V A, B BUSS	
171	646	-	-	DE171 MNIM+P	MIN IMPULSE +PITCH	Interface circuits 17D and 18D of A29 and 1D and 2D of A28 receive DC signals from the minimum impulse control (spacecraft) and feed bit positions 1 through 4 (gates 44236, 44238, 44240, and 44242) of channel 32 (table 30-5F).
172	546	-	-	DE172 MNIM-P	MIN IMPULSE -PITCH	
173	645	-	-	DE173 MNIM+Y	MIN IMPULSE +YAW	
174	545	-	-	DE174 MNIM-Y	MIN IMPULSE -YAW	
175	552	-	-	+4VDC RD175	4VA (TP)	Resistors 7R, 8R, and 9R of A29 provide +4VDC, BPLUS, and 0VDC for external equipment.
176	651	-	-	BPLUS RD176	14VA (TP)	
177	551	-	-	0VDC RD177	0V (TP)	

(cont)

TABLE 30A-1
COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
182	548	-	-	DE182	MRKREJ	REJECT MARK	Interface circuits 15D and 16D of A29 and 15D of A27 receive DC signals from the Optics and the IMU and feed bit position 7 (gate 45229) of channel 16 (table 30-5J), bit position 7 (gate 44120) of channel 33 (table 30-5G), and bit position 9 (gate 44125) of channel 30 (table 30-5D).
183	547	-	-	DE183	STRPRS	STAR PRES	
184	622	-	-	DE184	IMUOPR	IMU OPERATE	
185	313	-	-	ZOPCDU	CB185	ZERO OPT CDU	Bit positions 1 and 2 (gates 43302 and 43310) of channel 12 (table 30-5A) generate signals ZOPCDU and ENEROP which control interface circuits 16C and 13C of A26. The interface circuits operate the Optics CDU's and the Optics.
186	614	-	-	ENEROP	CB186	ERR CNTR ENABLE OPT	
188	644	-	-	DE188	MNIM+R	MIN IMPULSE +ROLL	Interface circuits 3D and 4D of A28 receive DC signals from the minimum impulse control (spacecraft) and feed bit positions 5 and 6 (gates 44244 and 44237) of channel 32 (table 30-5F).
189	544	-	-	DE189	MNIM-R	MIN IMPULSE -ROLL	
191	515 615	-	-	CDUCLK	{ XC191H XC191L	CDU CLOCK (51.2 KPPS)	Gate 49223 of the Timer generates pulses CDUCLK which control interface circuit 8XT of A25. The 51.2 kpps signals are provided for the CDU's.
192	317 417	-	-	GYENAB	{ XB192H XB192L	GYRO COMM ENABLE	Gate 46434 of the Gyro Drive Control (par 30-95 through 30-99) generates pulses GYENAB which control interface circuit 1XT of A26. Output pulses control gyros in the IMU.
193	522	-	-	DE193	IMUCAG	IMU CAGE	Interface circuit 16D of A27 receives DC signal from IMU and feeds bit position 11 (gate 44130) of channel 30 (table 30-5D).
194	514	-	-	COARSE	CB194	COARSE ALIGN ENABLE	Bit positions 4, 5, and 6 (gates 43320, 43322, and 43330) of channel 12 (table 30-5A) generate signals COARSE, ZIMCDU, and ENERIM which control interface circuits 12C, 11C, and 10C of A26. The interface circuits operate the IMU mode control.
195	414	-	-	ZIMCDU	CB195	ZERO IMU CDU's	
196	314	-	-	ENERIM	CB196	ERR CNTR ENABLE IMU	
197	325 425	-	-	PIPDAT	{ XC197H XC197L	PIPA DATA PULSE	Gate 49206 of the Timer generates PIPDAT pulses which control interface circuit 11XT of A25. The 3.2 kpps signal is fed into PIPA's.

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
198	319 419	-	-	GYRSET { XA198H XA198L	GYRO SET	Gate 46442 of the Gyro Drive Control (par 30-95 through 30-99) generates pulses GYRSET which control interface circuit 4XT of A27. Output pulses operate gyros.	
199	102 202	-	-	RD199H RD199L	TEMP MON 1	Connected only to pins 309 and 409 of both plugs A62 and B62.	
201	601	-	51	DE201	NKEY1 or KEY1	KEY CODE 1 (N)	DC signals DE201 through DE205 are generated in the keyboard of the navigation panel DSKY by pressing any key except key STBY and are received by interface circuits 4D through 8D of A25 which feed bit positions 1 through 5 (gates 45201, 45205, 45209, 45213, and 45217) of channel 16 (table 30-5J).
202	501	-	78	DE202	NKEY2 or KEY2	KEY CODE 2 (N)	
203	401	-	77	DE203	NKEY3 or KEY3	KEY CODE 3 (N)	
204	301	-	76	DE204	NKEY4 or KEY4	KEY CODE 4 (N)	
205	201	-	79	DE205	NKEY5 or KEY5	KEY CODE 5 (N)	
206	103	49	-	D-206	MAINRS or KEYRST	KEYBD RESET (M)	DC signals D-206 through D-209 are generated in the keyboards of the DSKY's and received by interface circuits 1D, 2D, 3D, and 9D of A25. Signal D-207 is caused by pressing a STBY key and operates the Standby Control (gate 45151, par 30-141AJ through 30-141AM). Signal D-208 is caused by pressing a RSET key and operates the start-stop logic (gate 45222) to reset the restart flip-flop (gates 41237/41238, par 30-131B). Signals D-206 and D-209 are caused by pressing any key, except key STBY, and reset channel 15 or first positions 1 through 5 of channel 16 (table 30-5J) respectively.
207	502	28	28	D-207	SBYBUT or STBY	STANDBY (NM)	
208	402	48	48	D-208	CAURST or RSET	RESET (LGHT) (NM)	
209	101	-	49	D-209	NAVRST or KEYRST	KYBD RESET (N)	
210	115	75	75	W-210		SPARE (NM)	Spare connection.
211	302	30	-	+28COM	RD211	+28 KYBD (M)	Resistors 1R, 2R, and 3R of A25 in parallel provide +28VDC for the main panel DSKY.
212	504	-	7	ELSNCN	CC212	POWER SUPPLY SYNC N	Gate 49249 of the Timer generates signal ELSNCN (800 pps) which controls interface circuit 34C of A25. The interface circuit pulses a DSKY power supply.

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
213	-	74	74	W-213	SPARE	Spare pin in DSKY's.	
214	404	2	2	RLYB01	CE214	Bit positions 1 through 15 (gates 44305, 44311, 44317, 44323, 44329, 44335, 44341, 44347, 44353, 44359, 44405, 44411, 44417, 44423, and 44429) of channel 10 (table 30-5) generate signals RLYB01 through RYWD16 (column 5) which control interface circuits 33C through 19C of A25. The output DC signals operate the relay matrices in the DSKY's (par 30-145A and 30-145B).	
215	304	9	9	RLYB02	CE215		
216	204	22	22	RLYB03	CE216		
217	605	41	41	RLYB04	CE217		
218	505	66	66	RLYB05	CE218		
219	405	3	3	RLYB06	CE219		
220	305	10	10	RLYB07	CE220		
221	205	23	23	RLYB08	CE221		
222	606	42	42	RLYB09	CE222		
223	506	67	67	RLYB10	CE223		
224	406	12	12	RLYB11	CE224		
225	306	11	11	RYWD12	CE225		
226	206	24	24	RYWD13	CE226		
227	607	43	43	RYWD14	CE227		
228	507	68	68	RYWD16	CE228		
229	407	27	27	ISSWAR	CB229	Bit positions 1 and 2 (gates 43401 and 43412) of channel 11 (table 30-5) generate signals ISSWAR and COMACT which control interface circuits 18C and 17C of A25. The interface circuits operate relays ISS WARNING and COMP ACTY (par 30-145C).	
230	307	26	26	COMACT	CB230		
231	207	25	25	SBYLIT or STBY	CB231	STANDBY LGHT	Gate 45157 of the Standby Control generates signal SBYLIT which controls interface circuit 16C of A25. The interface circuit operates relay STBY (par 30-145C).
232	608	44	44	RESTRT	C-232	RESTART	Gate 41240 of the start-stop logic (par 30-131B) generates signal RESTRT which controls interface circuit 15C of A25. The interface circuit operates relay RESTART (par 30-145C).
233	508	69	69	S4BSEQ	CB233	SIVB INJ SEQ STRT	Bit positions 13 and 14 (gates 43451 and 43460) of channel 12 (table 30-5A) generate signals S4BSEQ and S4BOFF which control interface circuits 14C and 13C of A25. The interface circuits operate relays INJ SEQ START and CUTOFF (par 30-145C).
234	408	18	18	S4BOFF	CB234		

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
235	308	47	47	UPLACT CB235	UPLINK ACTIVITY	Bit positions 3 and 5 (gates 43413 and 43426/43427) of channel 11 (table 30-5) generate signals UPLACT and KYRLS which control interface circuits 12C and 11C of A25. The interface circuits operate relays UPLINK ACTY and KEY REL (par 30-145C).
236	208	46	46	KYRLS CB236	KEY RELEASE (FLASH)	
237	604	45	45	CGCWAR C-237	CGC WARNING	Gate 41227 of the Alarm Control generates signal CGCWAR which controls interface circuit 10C of A25. The interface circuit operates relays CIRCUIT (par 30-145C).
238	609	70	70	VNFLSH CB238	VERB/NOUN (FLASH)	Bit position 6 (gates 43435/43438) of channel 11 (table 30-5) generates signal UNFLSH which controls interface circuit 9C of A25. The interface circuit operates relays FLASH (par 30-145C).
239	{104 105	8	8	0VDC or WD239	DISKY GND	Ground and +14V connection between AGC and DSKY's.
240		1	1	SIGNAL GRD BPLSSW or WD240	14V B (SWITCHED)	
241	116	73	73	W-241	SPARE	Spare line.
242	509	7	-	ELSNCM CC242	POWER SYNC M	Gate 49250 of the Timer generates signal ELSNCM (800 pps) which controls interface circuit 8C of A25. The interface circuit pulses a DSKY power supply.
243	106	21	-	WD243 +28COM or +28V	+28V (M)	+28VDC output provided by Main Panel DSKY. See signal 355.
244	409	72	72	OPEROR CB244	OPERATOR ERROR (FLASH)	Bit position 7 (gates 43440/43441) of channel 11 (table 30-5) generates signal OPEROR which controls interface circuit 7C of A25. Interface circuit operates relays OPR ERROR (par 30-145C).
246	-	13	13	W-246	SPARE	Spare pin on DSKY's.
251	602	-	30	+28COM RD251	+28 KYBD (N)	Resistors 1R, 2R, and 3R of A26 in parallel provide +28VDC for the navigation panel DSKY.

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description		
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY					
253	603	51	-	DE253	MKEY1 or KEY1	DC signals DE253 through DE257 are generated by the keyboard of the main panel DSKY (pressing any key except key STBY) and received by interface circuits 6D through 10D of A26 which feed bit positions 1 through 5 (gates 45101, 45105, 45109, 45113, and 45117) of channel 15 (table 30-5).		
254	503	78	-	DE254	MKEY2 or KEY2			
255	403	77	-	DE255	MKEY3 or KEY3			
256	303	76	-	DE256	MKEY4 or KEY4			
257	203	79	-	DE257	MKEY5 or KEY5			
258	309	71	71	TMPCAU	CB258	TEMP CAUTION	Gate 41230 of the Alarm Control generates signal TMPCAU when signal TMPOUT or signal TEMPIN/ is present. Signal TMPCAU controls interface circuit 6C of A25 which operates relays TEMP CAUTION (par 30-145C). Signal TMPOUT (temperature out of limits) is supplied by bit position 4 of channel 11; signal TEMPIN (temperature within limits) is supplied by line 125 which also feeds bit position 15 of channel 30.	
324A 324C 324O	- - -	- - -	81 Δ 82 Δ 80 Δ	SD324A WD324C WD324O	ISS WARNING	ISS WARNING None None	NC NC NC	Connections to contacts of relay ISS WARNING which is operated by signal 229.
325A 325C 325O	- - -	- - -	32 14 15	SD325A WD325C WD325O	CIRCUIT	AGC WARNING INHIBIT PIPA PULSE TORQ. None	NC	Connections to contacts of relay CIRCUIT which is operated by signal 237.
326A 326C 326O	- - -	- - -	34 6 17	SD326A WD326C WD326O	SPARE	SPARE (100-7) None None	NC NC NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 7 (par 30-145B).
328A 328C 328O	- - -	- - -	56 16 33	SD328A WD328C WD328O	SPARE	SPARE (1100-5) (SL) None None	NC NC NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 5 (par 30-145B).
338A 338C 338O	- - -	- - -	37 19 Δ 61	SD338A WD338C WD338O	INJ SEQ START	G HIGH LIGHT Signal not mentioned G HIGH RET	NC NC NC	Connections to contacts of relay INJ SEQ START which is operated by signal 233.

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
340A 340C 340O	- - -	- - -	36 85 \triangle 60	SD340A WD340C WD340O	CUTOFF	G LOW LIGHT NC Signal not mentioned G LOW RET NC	Connections to contacts of relay CUTOFF which is operated by signal 234.
342A 342O	- -	- -	84 55	SD342A WD342O	CIRCUIT	AGC (WARNING) None	Connections to contacts of relay CIRCUIT which is operated by signal 237. Contacts control AGC warning indicator on the condition annunciator.
343 344	- -	- -	38 40	W-343 W-344	115V 400 ~ 115V 400 ~ RET	115V VARIABLE 400 CPS SIG 115V VARIABLE 400 CPS RET	115VAC power for illumination of keys.
345 346	- -	- -	5 4	WD345 WD346	DIMMER DIMMER	DSKY DIMMER CONTROL SIG DSKY DIMMER RET	Connections from power supply to dimmer control.
347 348 349 350	- - - -	- - - -	64 65 62 63	W-347 W-348 W-349 W-350	5V STATUS POWER (LVWHI) 5V STATUS POWER RET (LVWLO) 5V CAUT POWER (LVYHI) 5V CAUT POWER RET (LVYLO)	5V STATUS LGHT PWR HI 5V STATUS LGHT PWR LO 5V CAUT LGHT PWR HI 5V CAUT LGHT PWR LO	5VDC power for illumination of indicators.
351A 351C	- -	- -	83 54	ISS WARNING	SD351A WD351C	ISS (WARNING) None	Connections to contacts of relay ISS WARNING which is operated by signal 229.

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description		
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY					
352A 352C 353	- - -	- - -	31 \triangle 53 \triangle 57	SD352A WD352C WD353	G&N CAUTION RESTART ALARM COMMON	PGNS (CAUTION) None RETURN (342, 351, 352)	Line 352A is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, and TEMP CAUTION (par 30-145B and 30-145C) and control the G&N caution indicator. Line 352C is connected to a contact of relay RESTART. Line 353 is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, TEMP CAUTION, CIRCUIT, and ISS WARNING.	
354A 354C 354O	- - -	- - -	35 59 58	SD354A WD354C WD354O		STANBY None RETURN	NC NC NC	Connections to contacts of relay STBY which is operated by signal 231.
355	107	-	21	WD355	+28COM or +28V	+28V (N)		+28VDC output provided by Navigation Panel DSKY. See signal 243.
407A 407C 407O	- - -	37 19 \triangle 61	- - -	SD407A WD407C WD407O	INJ SEQ START	INJ SEQU STRT (SIVB) None INJ SEQU STRT RET		Connections to contacts of relay INJ SEQ START which is operated by signal 233.
409A 409C 409O	- - -	36 85 \triangle 60	- - -	SD409A WD409C WD409O	CUTOFF	CUT OFF CMD (SIVB) None CUT OFF CMD RET	NC	Connections to contacts of relay CUTOFF which is operated by signal 234.
437 438	- -	38 40	- -	W-437 W-433	115V 400 ~ 115V 400 ~ RET	115V VARIABLE 400 CPS SIG 115V VARIABLE 400 CPS RET		115VAC power for illumination of keys.
439A 439C	- -	83 54	- -	SD439A WD439C	ISS WARNING	ISS WARNING LGHT None	NC	Connections to contacts of relay ISS WARNING which is operated by signal 229.
440A 440C	- -	31 \triangle 53 \triangle	- -	SD440A WD440C	G&N CAUTION RESTART	G/N CAUTION LGHT None	NC	Line 440A is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, and TEMP CAUTION (par 30-145B and 30-145C) which control the G&N caution indicator. Line 440C is connected to a contact of relay RESTART. Line 450 is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, TEMP CAUTION, CIRCUIT, and ISS WARNING.

Changed 28 January 1966

30A-17

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TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description		
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY					
441A 441O	- -	84 55	- -	SD441A } WD441O }	CIRCUIT None	AGC WARNING LGHT None	NC NC	Connections to contacts of relay CIRCUIT which is operated by signal 237. Contacts control AGC warning indicator on the condition annunciator.
442 443	- -	5 4	- -	RD442 WD443	DIMMER DIMMER	DSKY DIMMER CONTROL SIG DSKY DIMMER CONTROL RET		Connections from power supply to dimmer control.
444A 444C 444O	- - -	56 16 33	- - -	SD444A } WD444C } WD444O }	SPARE	SPARE (1100-5 (SL) None None	NC NC NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 5 (par 30-145B).
445A 445C 445O	- - -	34 6 17	- - -	SD445A } WD445C } WD445O }	SPARE	SPARE (1100-7) None None	NC NC NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 7 (par 30-145B).
446 447 448 449	- - - -	62 63 64 65	- - - -	WD446 WD447 WD448 WD449	5V CAUT POWER (LVYHI) 5V CAUT POWER RET (LVYLO) 5V STATUS POWER (LVWHI) 5V STATUS POWER RET (LVWLO)	5V CAUT LGHT PWR HI 5V CAUT LGHT PWR LO 5V STATUS LGHT PWR HI 5V STATUS LGHT PWR LO		5VDC power for illumination of indicators.
450	-	57	-	WD450	ALARM COMMON	RETURN 439-441		See lines 440A and 440C.
451A 451C 451O	- - -	32 14 15	- - -	SD451A } WD451C } WD451O }	CIRCUIT	AGC WARNING Signal not mentioned None	NC NC	Connections to contacts of relay CIRCUIT which is operated by signal 237.

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
452A 452C 452O	- - -	81 Δ 82 Δ 80 Δ	- - -	SD452A } WD452C } WD452O }	ISS WARNING	ISS WARNING NC None NC None NC	Connections to contacts of relay ISS WARNING which is operated by signal 229.
453A 453C 453O	- - -	35 59 58	- - -	SD453A } WD453C } WD453O }	-	STANDBY NC None NC None NC	Connections to contacts of relay STBY which is operated by signal 231.
801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816	209 109 610 510 410 310 210 110 611 511 411 311 211 111 612 512	- - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - -	RC+X+P CB801 RC+X-P CB802 RC+X+Y CB803 RC+X-Y CB804 RC-X+P CB805 RC-X-P CB806 RC-Y+X CB807 RC-X-Y CB808 RC+Y+R CB809 RC+Y-R CB810 RC-Y+R CB811 RC-Y-R CB812 RC+Z+R CB813 RC+Z-R CB814 RC-Z+R CB815 RC-Z-R CB816		+X/+PCH, +PCH/-X/+YAW +X/-PCH, -PCH/+Z +X/+YAW, +YAW/-X/+PCH +X/-YAW, -YAW/-X/+PCH -X/+PCH, +PCH/-X/-YAW -X/-PCH, -PCH/+Z -X/+YAW, +YAW/-X/-PCH -X/-YAW, -YAW/-X/-PCH +Y/+RLL +Y/-RLL -Y/+RLL -Y/-RLL +Z/+RLL, +RLL/(+Y, +Z) +Z/-RLL, -RLL/(-Y, +Z) -Z/+RLL, +RLL/(+Y, -Z) -Z/-RLL, -RLL/(-Y, -Z)	Bit positions 1 through 8 of channels 5 and 6 (gates 43105, 43111, 43117, 43123, 43129, 43135, 43141, 43147, 43259, 43254, 43249, 43244, 43239, 43224, 43223, and 43205) generate signals RC+X+P through RC-Z-R (column 5) which control interface circuits 5C through 1C of A25 and 34C through 24C of A26 which operate the reaction control system in the SM (first signal name in column 6) or the CM (second name).
817 818 819 820 821 822	158 258 157 257 156 256 155 255 154 254 153 253	- - - - - - - - - - - -	- - - - - - - - - - - -	YG817H } YG817L } YG818H } YG818L } YG819H } YG819L } YG820H } YG820L } YG821H } YG821L } YG822H } YG822L }	BMGXP BMGXM BMGYP BMGYM BMGZP BMGZM	+PITCH BMAG -PITCH BMAG +ROLL BMAG -ROLL BMAG +YAW BMAG -YAW BMAG	Interface circuits 1Y through 6Y of A29 receive pulses from the body-mounted acceleration gyros and feed gates 46337, 46338, 46346, 46347, 46356, and 46357 of the BMAG/RHC Control (par 30-110 through 30-112).
831 832	643 543	- -	- -	DE831 DE832	TRST9 TRST10	NC NC	Interface circuits 5D and 6D of A28 are able to receive DC signals and feed bit position 7 and 8 (gates 44239 and 44241) of channel 32 (table 30-5F).

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at			Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description	
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY				
840	621	-	-	DE840 IN3301	SPARE CHN 33-01 NC	Interface circuit 17D of A27 is able to receive DC signals and feeds bit position 1 (gate 44102) of channel 33 (table 30-5G). Not used, spare.	
841	213	-	-	MROLGT CB841	NC	Bit position 12 (gate 43450) of channel 12 (table 30-5A) generates signal MROLGT which controls interface circuit 15C of A26. The interface circuit is able to control external equipment.	
842 843	532 632	- -	- -	DE842 PCHGOF DE843 ROLGOF	NC NC	Interface circuits 16D and 15D of A28 are able to receive DC signals and feed bit positions 9 and 10 (gates 44243 and 44245) of channel 32 (table 30-5F).	
844 845	- -	- -	- -	DE844 IN3214 DE845 IN3216	SPARE CHN 32-14 NC SPARE CHN 32-16 NC	Interface circuits 5D of A26 and 10D of A26 are able to receive DC signals and feed bit positions 14 and 15 (gates 44140 and 44143) of channel 32 (table 30-5F). Not used, spares.	
848 850 851 852 853 854 855	- - - - - - -	- - - - - - -	- - - - - - -	OT1108 CB848 OT1110 CB850 OT1111 CB851 OT1112 CB852 OT1113 CB853 OT1114 CB854 OT1116 CB855	SPARE CHN 11-08 NC SPARE CHN 11-10 NC SPARE CHN 11-11 NC SPARE CHN 11-12 NC SPARE CHN 11-13 NC SPARE CHN 11-14 NC SPARE CHN 11-16 NC	Bit positions 8 and 10 through 15 (gates 48422, 49252, 49253, 49254, 48427, 48432, and 48437) of channel 11 (table 30-5) generate signals OT1108 and OT1110 through OT1116 (column 5) which control interface circuits 6C through 1C and 9C of A26. Not used, spares.	
858 859 860	142 242 141 241 140 240	- - - - -	- - - - -	A-858H } A-858L } A-859H } A-859L } A-860H } A-860L }	- - - - -	NC NC NC	Each line is connected to an RHC converter (one each in A27, A28, and A29). Each feeds the BMAG/RHC Control (figure 30-6 and par 30-113 through 30-115). Not used.

(cont)

TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

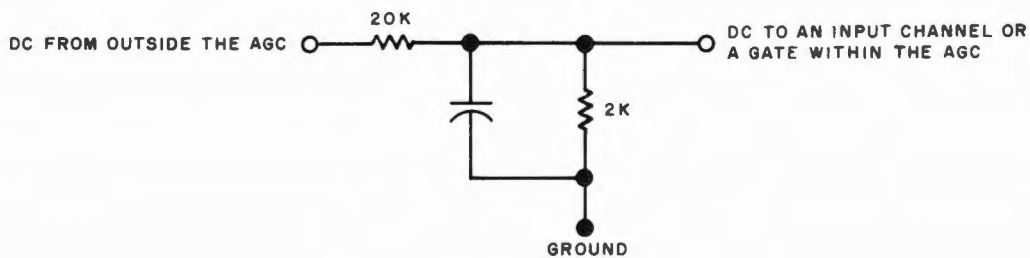
Line or Signal Number	Connecting Pins at			Name Used on Drawings $\triangle 1$	Name Used in DD Memo 185 $\triangle 3$	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
861	520	-	-	+28COM RD861	66	Resistor 7R of A27
863	637	-	-	+28COM RD863	SPARE NC	Resistor 7R of A28
865	539	-	-	+28COM RD865	SPARE NC	Resistor 6R of A28
866	635	-	-	+28COM RD866	SPARE NC	Resistor 9R of A28
867	535	-	-	+28COM RD867	SPARE NC	Resistor 1R of A27
868	634	-	-	+28COM RD868	SPARE NC	Resistor 2R of A27
869	642	-	-	+28COM RD869	SPARE NC	Resistor 3R of A28
870	619	-	-	+28COM RD870	SPARE NC	Resistor 8R of A27
874	658	-	-	+28COM RD874	4/7/68	Resistor 1R and 2R of A29 in parallel
875	-	-	-	-	4/7/68	-
876	633	-	-	+28COM RD876	SPARE NC	Resistor 3R of A27
877	656	-	-	+28COM RD877	SPARE NC	Resistor 3R of A29
878	533	-	-	+28COM RD878	SPARE NC	Resistor 4R of A27
879	519	-	-	+28COM RD879	SPARE NC	Resistor 9R of A27
901	324 424	-	-	25 KPPS XC901H } XC901L }	25.6 KPPS (PWR SUP SYNC)	Gate 49220 of the Timer generates 25KPPS pulses which control interface circuit 8XT of A26. Pulses are provided to operate power supplies in the space-craft.
902	212	-	-	DISDAC CB902	DISENGAGE OPTICS DAC	Bit position 11 (gate 43342) of channel 12 (table 30-5A) generates signal DISDAC which controls interface circuit 21C of A26. The interface circuit operates the Optics.
903 904	521 542	- -	- -	+28COM RD903 +28COM RD904	14VB (AGC OPERATE) NC 171-174/188/189	Resistors 5R of A27 and 4R of A28 provide +28VDC.
906	113	-	-	ZEROPT CB906	ZERO OPTICS	Bit position 10 (gate 43340) of channel 12 (table 30-5A) generates signal ZEROPT which controls interface circuit 14C of A26. The interface circuit operates the Optics.
907	556	-	-	+28COM RD907	102-104/107/106/182/183	Resistors 4R and 5R of A29 in parallel provide +28VDC.
908	-	-	-	-	102-104/106/107/182/183	

} provide +28VDC

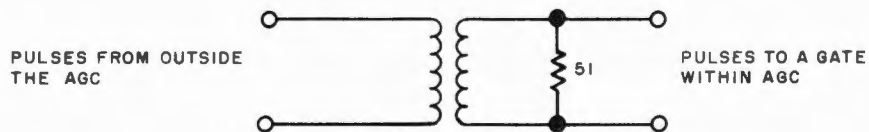
TABLE 30A-1

COMMAND MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

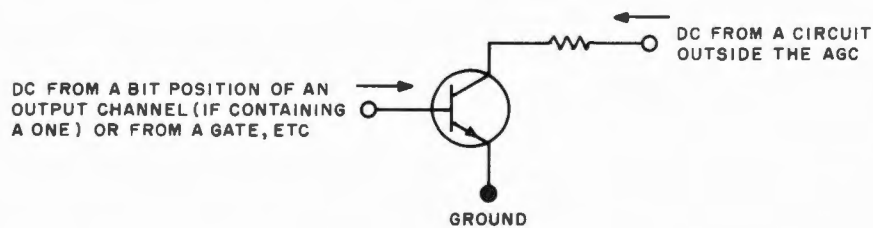
Line or Signal Number	Connecting Pins at			Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description
	A51 of AGC	J9 of Main Panel DSKY	J9 of Nav Panel DSKY			
909	114	-	-	ISSTDC CB909	ISS TURN ON DELAY CmplT	Bit position 15 (gate 48445) of channel 12 (table 30-5A) generates signal ISSTDC which controls interface circuit 8C of A26. The interface circuit operates the ISS.
910 911	216 215	- -	- -	W-910 W-911	CNTRL 1 (ACE) (LOW) CNTRL 2 (ACE) (HIGH)	
912	214	-	-	D-912 NHVFAL	INHIBIT POWER FAIL	Interface circuit 1D of A26 receives DC signal from spacecraft and feeds gates 41204 and 41205 of the Alarm Control (par 30-141R).
<p>¹ Pin numbers and signal names were taken from NASA drawings 2005020, 2005021, 2005900, and 2005950; and from the AGC BLOCK II COMPUTER WIRE LIST.</p> <p>² For DSKY's 200B, 200C, 200M, and 600M, pin numbers apply to 85 pin connector of adapter cable.</p> <p>³ NC means AGC not connected to external equipment.</p>						



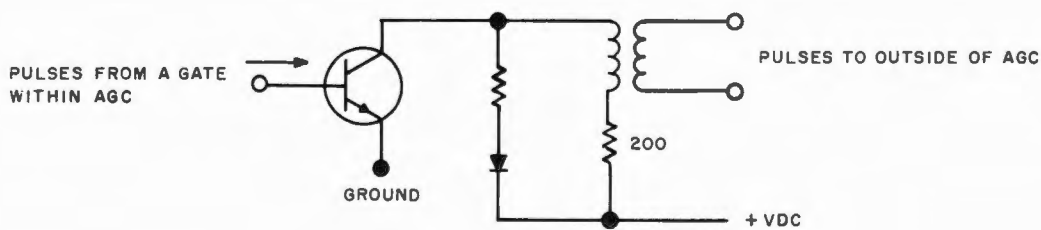
INPUT CIRCUIT D



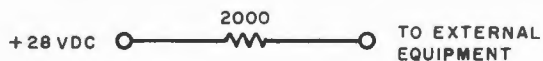
INPUT CIRCUIT Y



OUTPUT CIRCUIT C



OUTPUT CIRCUIT XT



OUTPUT CIRCUIT R

Figure 30A-1. Interface Circuits

ISSUE 30
APPENDIX B

LUNAR EXCURSION MODULE AGC SUBSYSTEM
INPUT AND OUTPUT SIGNALS

All input and output lines or signals passing through connector A51 of the AGC and connector J9 of the DSKY are listed in table 30B-1 of this appendix. Information is arranged by order of line or signal numbers frequently referred to in the main body of this issue. The numbers of the connecting pins of connectors A51 and J9 are given in columns 2 and 3 of the table while various signal names are listed in columns 4 and 5. The various types of interface circuits provided are described in figure 30B-1. A short description of the signals is contained in the last column of table 30B-1. Numbers preceded by an A or B indicate module numbers.

TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS

Line or Signal Number	Connecting Pins at		Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description
	A51 of AGC	J9 of DSKY			
001	516 616	-	CLK { XC001H XC001L	MASTER CLOCK	Gate 37137 of the Timer generates 1.024 Mpps signal CLK which controls interface circuit 1XT of A25. Master clock output pulses are used in various spacecraft systems.
002	358 458	-	ALT1 { XA002H XA002L	ALT MTER '1'	Gates 46109 and 46110 of the Altitude Meter Control (par 30-123 through 30-125) generate serial data pulses ALT0 and ALT1 which control interface circuits 5XT and 4XT of A29.
003	357 457	-	ALT0 { XA003H XA003L	ALT MTER '0'	
004	558	-	DE004 ULLTHR	ABORT	Interface circuit 1D of A29 receives DC signals from the spacecraft and feeds gate 44101 of bit position 1 of channel 30 (table 30-5D).
007	657	-	DE007 LFTOFF	LIFT OFF NC	Interface circuit 2D of A29 receives DC signals from the spacecraft and feeds gate 44113 of bit position 5 of channel 30 (table 30-5D).
008	354 454	-	THRST+ { XA008H XA008L	INCR THR RATE DESC EN	Gates 46247 and 46248 of the EMS and Thrust Drive Control (par 30-100 through 30-104) generate signals THRST+ and THRST- which control interface circuits 8XT and 9XT of A29.
009	353 453	-	THRST- { XA009H XA009L	DECR THR RATE DESC EN	
010	356 456	-	ALRT1 { XA010H XA010L	ALT RATE MTR '1'	Gates 46111 and 46112 of the Altitude Meter Control (par 30-123 through 30-125) generate serial data pulses ALRT0 and ALRT1 which control interface circuits 7XT and 6XT of A29.
012	355 455	-	ALRT0 { XA012H XA012L	ALT RATE MTR '0'	
011	613	-	ENON CB011	ENG ON ASC OR DESC	Bit position 7 of channel 12 (table 30-5A) controls gates 43228 and 43229 to generate signals ENON and ENOFF which control interface circuits 19C and 18C of A26. DC output signals control the spacecraft engine.
013	513	-	ENOFF CB013	ENG OFF ASC OR DESC	
014	133 233	-	Y-014H } DKSTRT Y-014L }	DLNK START	Interface circuits 1Y, 2Y, and 3Y of A27 receive pulses from the NA programmer and feed gates 47101, 45447, and 47227 of the Downlink Converter (par 30-126 and 30-127).
015	132 232	-	Y-015H } DKEND Y-015L }	DLNK END	
016	130	-	Y-016H } DKBSNC	DLNK SYNC	
	230	-	Y-016L }		

(cont)

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TABLE 30B-1
LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description
	A51 of AGC	J9 of DSKY			
017	352 452	-	DKDATA { X-017H X-017L	DLNK DATA	Gate 47256 of the Downlink Converter (par 30-126 and 30-127) generates signal DKDATA which controls interface circuit 1XT of A28. The serial data pulses are fed into the NA Programmer.
018 019 020 021 022 023	655 555 654 554 653 553	- - - - -	DE018 TRAN+X DE019 TRAN-X DE020 TRAN+Y DE021 TRAN-Y DE022 TRAN+Z DE023 TRAN-Z	+X TRANS COMM (MAN) -X TRANS COMM (MAN) +Y TRANS COMM (MAN) -Y TRANS COMM (MAN) +Z TRANS COMM (MAN) -Z TRANS COMM (MAN)	Interface circuits 4D through 9D of A29 receive DC signals from the manual translation control and feed bit positions 7 through 12 (gates 44216 through 44220, and 44232) of channel 31 (table 30-5E).
024 025	129 229 128 228	- -	YG024H } UPL0 YG024L } YG025H } UPL1 YG025L }	ULNK0 ULNK1	Interface circuits 4Y and 5Y of A27 receive serial data pulses from the uplink equipment and feed gates 46304 and 46305 of the Inlink Control (par 30-116 through 30-119).
028	413	-	ALTSNC CB028	ALT METER SYNC NC	Gate 46132 of the Altitude Meter Control (par 30-123 through 30-125) generates signal ALTSNC which controls interface circuit 17C of A26.
029 030	350 450 349 449	- - -	EMS+ { XA029H XA029L EMS- { XA030H XA030L	MONITOR INCR (+) NC MONITOR INCR (-) NC	Gates 46254 and 46258 of the EMS and Thrust Drive Control (par 30-100 through 30-104) generate signals EMS+ and EMS- which control interface circuits 10XT and 11XT of A29.
031 032	127 227 126 226	- -	YG031H } RRIN0 YG031L } YG032H } RRIN1 YG032L }	RRDR IN0 RRDR IN1	Interface circuits 6Y and 7Y of A27 receive serial data pulses from the rendezvous radar and feed gates 45349 and 44347 of the Radar Control (par 30-105 through 30-109).
033 034	- -	- -	- -	SPARE CHN 32-12 NC SPARE CHN 32-13 NC	Interface circuits 3D and 4D of A26 are able to receive DC signals and feed bit positions 12 and 13 (gates 44134 and 44137) of channel 32 (table 30-5F).
039	630	-	DE039 LVDAGD	LRDR VEL DATA GOOD	Interface circuit 17D of A28 receives a DC signal from landing radar and feeds bit position 8 (gate 44123) of channel 33 (table 30-5G).
040	641	-	DE040 HOLFUN	AUTO THROTTLE	Interface circuit 7D of A28 receives DC signal and feeds bit position 13 (gate 44233) of channel 31 (table 30-5E).

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description			
	A51 of AGC	J9 of DSKY						
041	348	-	RRRANG	{ XA041H XA041L	RRDR RANGE GATE	Gates 45328 through 45333, 45345, and 45346 of the Radar Control (par 30-105 through 30-109) generate control signals (90 msec bursts of 100 kpps) RRRANG, RRRARA, LRXVEL, LRYVEL, LRZVEL, LRRANG, RRSYNC, and LRSYNC which control interface circuits 4XT through 11XT of A28. Gates 49218 and 49219 generate timing signals (3.2 kpps) RRRST and LRRST which control interface circuits 2XT and 3XT of module A25.		
042	347	-	RRRARA	{ XA042H XA042L			RRDR RANGE RATE GATE	
043	344	-	LRXVEL	{ XA043H XA043L			LRDR XA VELOCITY GATE	
044	343	-	LRYVEL	{ XA044H XA044L			LRDR YA VELOCITY GATE	
045	342	-	LRZVEL	{ XA045H XA045L			LRDR ZA VELOCITY GATE	
046	341	-	LRRANG	{ XA046H XA046L			LRDR RANGE GATE	
047	346	-	RRSYNC	{ XA047H XA047L			RRDR SYNC FOR READOUT	
048	345	-	RRRST	{ XC048H XC048L			RRDR GATE RESET	
051	340	-	LRSYNC	{ XA051H XA051L			LRDR SYNC FOR READOUT	
052	339	-	LRRST	{ XC052H XC052L			LRDR GATE RESET	
060	523	-	DE060	LEMATT			ATTITUDE HOLD MODE	Interface circuit 14D of A27 receives DC signals and feeds bit position 11 (gate 44131) of channel 32 (table 30-5F).
061	530	-	DE061	LRRLSC			LR RANGE LOW SCALE	Interface circuit 18D of A28 receives DC signals from the landing radar and feeds bit position 9 (gate 44126) of channel 33 (table 30-5G).
064	629	-	DE064	RRPONA	RR POWER ON/AUTO	Interface circuit 1D of A27 receives DC signal from the rendezvous radar and feeds bit position 2 (gate 44105) of channel 33 (table 30-5G).		
065	541	-	DE065	FREFUN	AUTO STABILIZATION	Interface circuit 8D of A28 receives DC signal and feeds bit position 14 (gate 44233) of channel 31 (table 30-5E).		
066	640	-	DE066	S4BSAB	ABORT STAGE	Interface circuits 9D, 10D of A28, and 3D of A29 receive DC signals from the spacecraft and feed bit positions 4, 2, and 6 (gates 44110, 44104, and 44116) of channel 30 (table 30-5D).		
067	540	-	DE067	SMSEPR	STAGE VERIFY			
068	557	-	DE068	GUIREL	DISPLAY INERTIAL DATA			

(cont)

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings $\triangle 1$	Name Used in DD Memo 185 $\triangle 3$	Signal Description
	A51 of AGC	J9 of DSKY			
069	529	-	DE069 RRRLSC	RR RANGE LOW SCALE	Interface circuit 2D of A27 receives DC signals from the rendezvous radar and feeds bit position 2 (gate 44108) of channel 33 (table 30-5G).
071	125	-	YG071H } LRIN0	LRDR IN0	Interface circuits 8Y and 9Y of A27 receive serial data pulses from the landing radar and feed gates 45355 and 45353 of the Radar Control (par 30-105 through 30-109).
072	225 124 224	-	YG071L } YG072H } LRIN1 YG072L }	LRDR IN1	
078	518	-	OTLNK0 { XA078H	"0" BIT CROSS OUT NC	Gates 46147 and 46149 of Outlink Control (par 30-120 through 30-122) generate serial data pulses OTLNK0 and OTLNK1 which control interface circuits 6XT and 7XT of A27. Outputs are provided for the cross link equipment but not connected.
079	618 517 617	-	OTLNK1 { XA078L XA079H XA079L	"1" BIT CROSS OUT NC	
080	123	-	YG080H } XLNK0	"0" BIT CROSS IN NC	Interface circuits 10Y and 11Y of A27 are able to receive serial data pulses from the cross link equipment and feed gates 46306 and 46307 of the Inlink Control (par 30-116 through 30-119). Inputs are not connected.
081	223 122 222	-	YG080L } YG081H } XLNK1 YG081L }	"1" BIT CROSS IN NC	
082	636	-	DE082 SPSRDY	ENGINE ARMED	Interface circuit 13D of A28 receives DC signals from the spacecraft and feeds bit position 3 (gate 44107) of channel 30 (table 30-5D).
083	538	-	DE083 BLKUPL/	ACCEPT UPLNK	Interface circuit 12D of A28 receives DC signals from the UPTTEL switch and feeds gate 46308 of Inlink Control (par 30-116 through 30-119).
084	638	-	DE084 IN3008	SPARE CHN 30-08 NC	Interface circuit 11D of A28 is able to receive DC signals and feeds bit position 8 (gate 44122) of channel 32 (table 30-5D).
085	351 451	-	DKDATB { X-085H X-085L	DLNK DATA (AGS)	Gate 47261 of the Downlink Converter (par 30-126 and 30-127) generates signal DKDATB which controls interface circuit 1XT of A29. The signal is identical to signal 017.
086	639	-	+28VDC RD086	65/60/95	Resistor 5R of A28 provides +28VDC for external equipment.

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle 1	Name Used in DD Memo 185 \triangle 3	Signal Description
	A51 of AGC	J9 of DSKY			
087	647	-	+28COM RD087	4/66/82	Resistors 1R and 2R of A28 in parallel provide +28VDC for external equipment. Provided with signal 087.
088	-	-	- -	4/66/82	
091	537	-	+28COM RD091	159/40	Resistor 8R of A28 provides +28VDC for external equipment.
093	628	-	DE093 MANR+P	+EL (LPD) NC	Interface circuits 3D through 8D of A27 receive DC signals from spacecraft and feed bit positions 1 through 6 (gates 44201 through 44205, and 44215) of channel 31 (table 30-5E).
094	528	-	DE094 MANR-P	-EL (LPD) NC	
095	627	-	DE095 MANR+Y	ATT CONTROL OUT OF DET.	
096	527	-	DE096 MANR-Y	NC	
097	626	-	DE097 MANR+R	+AZ (LPD) NC	
098	526	-	DE098 MANR-R	-AZ (LPD) NC	
101	620	-	+28COM RD101	102/103/182	Resistor 6R of A27 provides +28VDC for external equipment.
102	549	-	DE102 MARK	RATE OF DESCENT (+)	Interface circuit 13D of A29 receives DC signals from the radars and feeds bit position 6 (gate 45225) of channel 16 (table 30-5J).
103	550	-	D-103 MRKRST	RATE OF DESCENT RESET	Interface circuit 11D of A29 receives DC signals from the radars and resets bit positions 6 and 7 (via gate 45233) of channel 16 (table 30-5J).
104	649	-	DE104 ZEROP	RRDATA GOOD	Interface circuits 12D, 10D, and 14D of A29 receive DC signals from the radars and feed bit positions 4, 5, and 6 (gates 44111, 44114, and 44117) of channel 33 (table 30-5G).
106	650	-	DE106 OPMSW2	LRDR RANGE DATA GOOD	
107	648	-	DE107 OPMSW3	LR POSITION 1 (DESC)	
108	152	-	YG108H } SHAFTP	+RR SHAFT	Interface circuits 7Y through 10Y of A29 receive incremental pulses from the rendezvous radar CDU's and feed the counter priority control gates 31302, 31309, 31215, and 31224, and the alarm control gates 49439 and 49440, par 30-141L.
109	252	-	YG108L } SHAFTM	-RR SHAFT	
110	151	-	YG109H } TRNP	+RR TRUNNION	
111	251	-	YG109L } TRNM	-RR TRUNNION	
	150	-	YG110H } YG110L }		
	250	-	YG111H } YG111L }		
	149	-			
	249	-			

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description	
	A51 of AGC	J9 of DSKY				
112	525	-	DE112	OPCDFL	RR CDU FAIL	Interface circuits 10D and 9D of A27 receive DC signals from the rendezvous radar CDU's and the ISS, and feed bit positions 7 and 14 (gates 44119 and 44139) of channel 30 (table 30-5D).
113	625	-	DE113	ISSTOR	ISS TURN ON REQUEST	
114	338 438	-	SHFTDP	{ XA114H XA114L	+RR SHAFT	Gates 48348, 48349, 48336, and 48339 of the CDU Drive Control (par 30-90 through 30-94) generate drive pulses SHFTDP, SHFTDM, TRNDP, and TRNDM which control interface circuits 8XT through 11XT of A27. The output pulses drive the rendezvous radar CDU's.
115	337 437	-	SHFTDM	{ XA115H XA115L	-RR SHAFT	
116	336 436	-	TRNDP	{ XA116H XA116L	+RR TRUNNION	
117	335 435	-	TRNDM	{ XA117H XA117L	-RR TRUNNION	
118	148 248	-	YG118H } YG118L }	CDUXP	+X CDU (OUT GMBL)	Interface circuits 11Y of module A29, and 1Y through 5Y of A28 receive incremental pulses from the IMU CDU's and feed the counter priority control gates 31102, 31109, 31115, 31124, 31202, and 31209, and the alarm control gates 49437 and 49438 (par 30-141L).
119	147 247	-	YG119H } YG119L }	CDUXM	-X CDU (OUT GMBL)	
120	146 246	-	YG120H } YG120L }	CDUY P	+Y CDU (INN GMBL)	
121	145 245	-	YG121H } YG121L }	CDUYM	-Y CDU (INN GMBL)	
122	144 244	-	YG122H } YG122L }	CDUZP	+Z CDU (MID GMBL)	
123	143 243	-	YG123H } YG123L }	CDUZM	-Z CDU (MID GMBL)	
124	624	-	DE124	CDUFAL	CDU FAIL (ISS)	
125	524	-	DE125	TEMPIN	TEMP WITHIN LIMITS	Interface circuit 12D of A27 receives DC signals from the IMU and feeds bit position 15 (gate 44142) of channel 30 and gate 45262 of the Alarm Control.

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description
	A51 of AGC	J9 of DSKY			
126	334	-	CDUXDP { XA126H	CDU +X (OUT GMBL)	Gates 48308, 48309, 48318, 48319, 48326, and 48329 of the CDU Drive Control (par 30-90 through 30-94) generate drive pulses CDUXDP through CDUZDM (column 4) which control interface circuits 4XT through 7XT of A25 and 2XT and 3XT of module A26. The output pulses drive the IMU CDU's.
	434		{ XA126L		
127	333	-	CDUXDM { XA127H	CDU -X (OUT GMBL)	
	433		{ XA127L		
128	332	-	CDUYDP { XA128H	CDU +Y (INN GMBL)	
	432		{ XA128L		
129	330	-	CDUYDM { XA129H	CDU -Y (INN GMBL)	
	430		{ XA129L		
130	329	-	CDUZDP { XA130H	CDU +Z (MID GMBL)	Interface circuits 6Y through 11Y of A28 receive incremental pulses from the PIPA's and feed gates 53461, 53361, 53362, 54461, 54361, and 54362 of the Counter Priority Control. The Counter Priority Control generates signals PIPXP, PIPXM, PIPYP, PIPYM, PIPZP, and PIPZM which set the priority cells and which are fed into gates 49440 through 49442 of the Alarm Control (par 30-141L).
	429		{ XA130L		
131	328	-	CDUZDM { XA131H	CDU -Z (MID GMBL)	
	428		{ XA131L		
132	139	-	YG132H } PIPAX+	+DVX (STROBED)	
	239		YG132L }		
133	138	-	YG133H } PIPAX-	-DVX (STROBED)	
	238		YG133L }		
134	137	-	YG134H } PIPAY+	+DVY (STROBED)	
	237		YG134L }		
135	136	-	YG135H } PIPAY-	-DVY (STROBED)	
	236		YG135L }		
136	135	-	YG136H } PIPAZ+	+DVZ (STROBED)	
	235		YG136L }		
137	134	-	YG137H } PIPAZ-	-DVZ (STROBED)	
	234		YG137L }		
139	327	-	PIPINT { XC139H	PIPA INTERROGATE	Gates 49208 and 49204 of the Timer generate pulses PIPINT and PIPASW which control interface circuits 9XT and 10XT of A25. The output pulses interrogate and switch the PIPA's at a rate of 3.2 kpps.
	427		{ XC139L	3200SB4	
140	326	-	PIPASW { XC140H	PIPA SWITCHING	
	426		{ XC140L	3200SB1	
141	623	-	DE141 IMUFAL	IMU FAIL	Interface circuit 13D of A27 receives DC signals from the IMU and feeds bit position 13 (gate 44136) of channel 30 (table 30-5D).

(cont)

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description
	A51 of AGC	J9 of DSKY			
142	121	-	GYXP { XB142H	+X GYRO SELECT	Gates 46424 through 46427, 46432, 46433, and 46443 of the Gyro Drive Control (par 30-95 through 30-99) generate drive pulses GYXP through GYZM (column 4) and reset pulses GYRRST which control interface circuits 2XT and 3XT of A27, A28, and A29, and 5XT of A27. The output pulses drive and reset the gyros in the IMU.
143	221	-	{ XB142L	-X GYRO SELECT	
144	120	-	GYXM { XB143H	+Y GYRO SELECT	
145	220	-	{ XB143L	-Y GYRO SELECT	
146	119	-	GYYP { XB144H	+Z GYRO SELECT	
147	219	-	{ XB144L	-Z GYRO SELECT	
148	118	-	GYYM { XB145H	GYRO RESET	
	218	-	{ XB145L		
	321	-	GYZP { XB146H		
	421	-	{ XB146L		
	320	-	GYZM { XB147H		
	420	-	{ XB147L		
	318	-	GYRRST { XA148H		
	418	-	{ XA148L		
149	323	-	800 SET { XC149H	800 PPS SET	Gates 49209 and 49210 of the Timer generate 800 pps signals which control interface circuits 10XT and 11XT of A26. The timing pulses are provided for external equipment.
150	423	-	{ XC149L	800 PPS RESET	
	322	-	800 RST { XC150H		
	422	-	{ XC150L		
151	316	-	3200A { XC151H	3.2 KPPS A	Gates 49211 through 49213 and 49215 of the Timer generate 3200 pps signals which control interface circuits 4XT through 7XT of A26. The timing pulses are provided for external equipment.
152	416	-	{ XC151L	3.2 KPPS RESET B	
	315	-	3200B { XC152H	3.2 KPPS RESET C NC	
	415	-	{ XC152L	3.2 KPPS RESET D NC	
	-	-	3200C { XC153H		
	-	-	{ XC153L		
	-	-	3200D { XC154H		
	-	-	{ XC154L		
155	117	-	12 KPPS { XC155H	12.8 KPPS PWR SUP SYNC	Gate 49217 of the Timer generates 12 kpps signals which control interface circuit 9XT of A26. The timing pulses are provided for external equipment.
	217	-	{ XC155L		
158	534	-	DE158 CTLSAT	GUID. RELEASE NC	Interface circuits 18D of module A27 and 14D of A28 receive DC signals from the spacecraft and feed bit position 10 (gate 44128) of channel 30 (table 30-5D) and bit position 15 (gate 44235) of channel 31 (table 30-5E).
159	536	-	DE159 GCAPCL	G/N CONTROL OF S/C	

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of DSKY			
160	112	-	S4BTAK CB160	+PITCH GIMBAL TRIM	Bit positions 9, 8, and 3 (gates 43332, 43160, and 43312) of channel 12 (table 30-5A) generate signals S4BTAK, TVCNAB, and STARON which control interface circuits 20C, 23C, and 22C of A26. The interface circuits operate circuits in the spacecraft.
161	412	-	TVCNAB CB161	DISPLAY INERTIAL DATA	
162	312	-	STARON CB162	HORIZ VEL LO SCALE NC	
166	652	-	+28COM RD166	+28V COMP. (TP)	Resistor 6R of A29 provides +28VDC for external equipment.
167	{ 161 261 361 461 561 661	-	WD167	+28 A BUSS	AGC power inputs connected to power supplies, modules 30 and 31.
168	{ 159 259 359 459 559 659	-	WD168	+28 A BUSS	
169	{ 160 260 360 460 560 660	-	WD169	0V A BUSS	
171	646	-	DE171 MNIM+P	THRUSTER 4D/4S FAIL	Interface circuits 17D and 18D of A29 and 1D and 2D of A28 receive DC signals from the spacecraft and feed bit positions 1 through 4 (gates 44236, 44238, 44240, and 44242) of channel 32 (table 30-5F).
172	546	-	DE172 MNIM-P	THRUSTER 3U/3S FAIL	
173	645	-	DE173 MNIM+Y	THRUSTER 4U/4F FAIL	
174	545	-	DE174 MNIM-Y	THRUSTER 3D/3F FAIL	
175	552	-	+4VDC RD175	4VA (TP)	Resistors 7R, 8R, and 9R of A29 provide +4VDC, BPLUS, and 0VDC for external equipment.
176	651	-	BPLUS RD176	14VA (TP)	
177	551	-	0VDC RD177	0V (TP)	

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description
	A51 of AGC	J9 of DSKY			
182	548	-	DE182 MRKREJ	RATE OF DESCENT (-)	Interface circuits 15D and 16D of A29 and 15D of A27 receive DC signals from the radars and the IMU and feed bit position 7 (gate 45229) of channel 16 (table 30-5J), bit positions 7 (gate 44120) of channel 33 (table 30-5G), and bit position 9 (gate 44125) of channel 30 (table 30-5D).
183	547	-	DE183 STRPRS	LR POSITION 2 (HOVER)	
184	622	-	DE184 IMUOPR	IMU OPERATE	
185	313	-	ZOPCDU CB185	ZERO REN RDR CDU	Bit positions 1 and 2 (gates 43302 and 43310) of channel 12 (table 30-5A) generate signals ZOPCDU and ENEROP which control interface circuits 16C and 13C of A26. The interface circuits operate the rendezvous radar CDU's and the rendezvous radar.
186	614	-	ENEROP CB186	ERR CNTR ENABLE REN RDR	
188	644	-	DE188 MNIM+R	THRUSTER 1D/1S FAIL	Interface circuits 3D and 4D of A28 receive DC signals from the spacecraft and feed bit positions 5 and 6 (gates 44244 and 44237) of channel 32 (table 30-5F).
189	544	-	DE189 MNIM-R	THRUSTER 1U/1F FAIL	
191	515 615	-	CDUCLK { XC191H XC191L	CDU CLOCK (51.2 KPPS)	Gate 49223 of the Timer generates pulses CDUCLK which control interface circuit 8XT of A25. The 51.2 kpps signals are provided for the CDU's.
192	317 417	-	GYENAB { XB192H XB192L	GYRO COMM ENABLE	Gate 46434 of the Gyro Drive Control (par 30-95 through 30-99) generates pulses GYENAB which control interface circuit 1XT of A26. Output pulses control gyros in the IMU.
193	522	-	DE193 IMUCAG	IMU CAGE	Interface circuit 16D of A27 receives DC signal from IMU and feeds bit position 11 (gate 44130) of channel 30 (table 30-5D).
194	514	-	COARSE CB194	COARSE ALIGN ENABLE	Bit positions 4, 5, and 6 (gates 43320, 43322, and 43330) of channel 12 (table 30-5A) generate signals COARSE, ZIMCDU, and ENERIM which control interface circuits 12C, 11C, and 10C of A26. The interface circuits operate the IMU mode control.
195	414	-	ZIMCDU CB195	ZERO IMU CDU'S	
196	314	-	ENERIM CB196	ERR CNTR ENABLE IMU	
197	325 425	-	PIPDAT { XC197H XC197L	PIPA DATA PULSE 3200SB2	Gate 49206 of the Timer generates PIPDAT pulses which control interface circuit 11XT of A25. The 3.2 kpps signal is fed into PIPA's.

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of DSKY			
198	319 419	-	GYRSET { XA198H XA198L	GYRO SET	Gate 46442 of the Gyro Drive Control (par 30-95 through 30-99) generates pulses GYRSET which control interface circuit 4XT of A27. Output pulses operate gyros.
199	102 202	-	RD199H RD199L	TEMP MON 1	Connected only to pins 309 and 409 of both plugs A62 and B62.
201	601	-	DE201	NC	DC signals DE201 through DE205 are received by interface circuits 4D through 8D of A25 which feed bit positions 1 through 5 (gates 45201, 45205, 45209, 45213, and 45217) of channel 16 (table 30-5J).
202	501	-	DE202	NC	
203	401	-	DE203	MARK X (AOT)	
204	301	-	DE204	MARK Y (AOT)	
205	201	-	DE205	REJECT MARK (AOT)	
206	103	49	D-206	KYBD RESET	DC signals D-206 through D-209 are generated by the keyboard of the DSKY and the spacecraft, and received by interface circuits 1D, 2D, 3D, and 9D of A25. Signal D-207 is caused by pressing the STBY key and operates the Standby Control (gate 45141, par 30-141AJ through 30-141AM). Signal D-208 is caused by pressing the RSET key and operates the start-stop logic (gate 45222) to reset the restart flip-flop (gates 41237/41238, par 30-131B). Signal D-206 is caused by pressing any key on the DSKY, except key STBY, and resets channel 15. Signal D-209 resets bit positions 1 through 5 of channel 16 (table 30-5J).
207	502	28	D-207	STANDBY	
208	402	48	D-208	RESET (LGHT)	
209	101	-	D-209	MARK RESET (AOT)	
210	115	75	W-210	SPARE	Spare connection.
211	302	30	+28COM RD211	+28 KYBD	Resistors 1R, 2R, and 3R of A25 in parallel provide +28VDC for the DSKY.
212	504	-	ELSNCN CC212	NC	Gate 49249 of the Timer generates signal ELSNCN (800 pps) which controls interface circuit 34C of A25.
213	-	74	W-213	SPARE	Spare pin in DSKY.

(cont)

TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle		Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of DSKY				
214	404	2	RLYB01	CE214	CHN 10-1	Bit positions 1 through 15 (gates 44305, 44311, 44317, 44323, 44329, 44335, 44341, 44347, 44353, 44359, 44405, 44411, 44417, 44423, and 44429) of channel 10 (table 30-5) generate signals RLYB01 through RYWD16 (column 4) which control interface circuits 33C through 19C of A25. The output DC signals operate the relay matrix in the DSKY (par 30-145A and 30-145B).
215	304	9	RLYB02	CE215	CHN 10-2	
216	204	22	RLYB03	CE216	CHN 10-3	
217	605	41	RLYB04	CE217	CHN 10-4	
218	505	66	RLYB05	CE218	CHN 10-5	
219	405	3	RLYB06	CE219	CHN 10-6	
220	305	10	RLYB07	CE220	CHN 10-7	
221	205	23	RLYB08	CE221	CHN 10-8	
222	606	42	RLYB09	CE222	CHN 10-9	
223	506	67	RLYB10	CE223	CHN 10-10	
224	406	12	RLYB11	CE224	CHN 10-11	
225	306	11	RYWD12	CE225	CHN 10-12	
226	206	24	RYWD13	CE226	CHN 10-13	
227	607	43	RYWD14	CE227	CHN 10-14	
228	507	68	RYWD16	CE228	CHN 10-15	
229	407	27	ISSWAR	CB229	ISS WARNING	Bit positions 1 and 2 (gates 43401 and 43412) of channel 11 (table 30-5) generate signals ISSWAR and COMACT which control interface circuits 18C and 17C of A25. The interface circuits operate relays ISS WARNING and COMP ACTY (par 30-145C).
230	307	26	COMACT	CB230	COMPUTER ACTIVITY	
231	207	25	SBYLIT or STBY	CB231	STANDBY LGHT	Gate 45157 of the Standby Control generates signal SBYLIT which controls interface circuit 16C of A25. The interface circuit operates relay STBY (par 30-145C).
232	608	44	RESTRT	C-232	RESTART	Gate 41240 of the start-stop logic (par 30-131B) generates signal RESTRT which controls interface circuit 15C of A25. The interface circuit operates relay RESTART (par 30-145C).
233	508	69	S4BSEQ	CB233	LRDR POS CMD	Bit positions 13 and 14 (gates 43451 and 43460) of channel 12 (table 30-5A) generate signals S4BSEQ and S4BOFF which control interface circuits 14C and 13C of A25. The interface circuits operate relays INJ SEQ START and CUTOFF (par 30-145C).
234	408	18	S4BOFF	CB234	RR ENABLE LOCK ON	

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description
	A51 of AGC	J9 of DSKY			
235	308	47	UPLACT CB235	UPLNK ACTIVITY	Bit positions 3 and 5 (gates 43413 and 43426/43427) of channel 11 (table 30-5) generate signals UPLACT and KYRLS which control interface circuits 12C and 11C of A25. The interface circuits operate relays UPLINK ACTY and KEY REL (par 30-145C).
236	208	46	KYRLS CB236	KEY RELEASE (FLASH)	
237	604	45	CGCWAR C-237	LGC WARNING	Gate 41227 of the Alarm Control generates signal CGCWAR which controls interface circuit 10C of A25. The interface circuit operates relay CIRCUIT (par 30-145C).
238	609	70	VNFLSH CB238	VERB/NOUN (FLASH)	Bit position 6 (gates 43435/43438) of channel 11 (table 30-5) generates signal VNFLSH which controls interface circuit 9C of A25. The interface circuit operates relay FLASH (par 30-145C).
239	{ 104 105	8	0VDC or SIGNAL GRD WD239	DISKY GRND	Ground and +14V connection between AGC and DSKY.
240		1	BPLSSW or +14VA WD240	14V B (SWITCHED)	
241	116	73	W-241	SPARE	Spare line.
242	509	7	ELSNM CC242	POWER SYNC M	Gate 49250 of the Timer generates signal ELSNMC (800 pps) which controls interface circuit 8C of A25. The interface circuit pulses the DSKY power supply.
243	106	21	WD243 +28COM or +28V	+28V (M)	+28VDC output provided by DSKY. See signal 355.
244	409	72	OPEROR CB244	OPERATOR ERROR (FLASH)	Bit position 7 (gates 43440/43441) of channel 11 (table 30-5) generates signal OPEROR which controls interface circuit 7C of A25. Interface circuit operates relay OPR ERROR (par 30-145C).
246	-	13	W-246	SPARE	Spare pin on DSKY.
251	602	-	+28COM RD251	+28 (203-205/209)	Resistors 1R, 2R, and 3R of A26 in parallel provide +28VDC.

(cont)

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description	
	A51 of AGC	J9 of DSKY				
253 254 255 256 257	603 503 403 303 203	51 78 77 76 79	DE253 MKEY1 DE254 MKEY2 DE255 MKEY3 DE256 MKEY4 DE257 MKEY5	KEY CODE 1 KEY CODE 2 KEY CODE 3 KEY CODE 4 KEY CODE 5	DC signals DE253 through DE257 are generated by the keyboard of the DSKY (pressing any key except key STBY) and received by interface circuits 6D through 10D of A26 which feed bit positions 1 through 5 (gates 45101, 45105, 45109, 45113, and 45117) of channel 15 (table 30-5).	
258	309	71	TMPCAU CB258	TEMP CAUTION	Gate 41230 of the Alarm Control generates signal TMPCAU when signal TMPOUT or signal TEMPIN/ is present. Signal TMPCAU controls interface circuit 6C of A25 which operates relays TEMP CAUTION (par 30-145C). Signal TMPOUT (temperature out of limits) is supplied by bit position 4 of channel 11; signal TEMPIN (temperature within limits) is supplied by line 125 which also feeds bit position 15 of channel 30.	
407A 407C 407O	- - -	37 19 \triangle 61	SD407A } WD407C } WD407O }	INJ SEQ START	LRDR POS CMD (HOVER) None LR HOVER POS RET	Connections to contacts of relay INJ SEQ START which is operated by signal 233.
409A 409C 409O	- - -	36 85 \triangle 60	SD409A } WD409C } WD409O }	CUTOFF	RR AUTO TRK ENABLE RR AUTO ANGLE ENABLE RET None NC	Connections to contacts of relay CUTOFF which is operated by signal 234.
437 438	- -	38 40	W-437 W-433	115V 400 ~ 115V 400 ~ RET	115V VARIABLE 400 CPS SIG 115V VARIABLE 400 CPS RET	115VAC power for illumination of keys.
439A 439C	- -	83 54	SD439A } WD439C }	ISS WARNING	ISS WARNING LGHT None NC	Connections to contacts of relay ISS WARNING which is operated by signal 229.
440A 440C	- -	31 \triangle 53 \triangle	SD440A WD440C	G&N CAUTION RESTART	PGNS CAUTION LGHT NC	Line 440A is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, and TEMP CAUTION (par 30-145B and 30-145C) which control the G&N caution indicator. Line 440C is connected to a contact of relay RESTART. Line 450 is connected to contacts of relays GIMBAL LOCK, TRACKER, PROG CAUTION, RESTART, TEMP CAUTION, CIRCUIT, and ISS WARNING.

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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings \triangle	Name Used in DD Memo 185 \triangle	Signal Description	
	A51 of AGC	J9 of DSKY				
441A 441O	- -	84 55	SD441A } WD441C }	CIRCUIT	LGC WARNING LGHT NC	Connections to contacts of relay CIRCUIT which is operated by signal 237. Contacts control AGC warning indicator on the condition annunciator.
442 443	- -	5 4	RD442 WD443	DIMMER DIMMER	DSKY DIMMER CONTROL SIG DSKY DIMMER CONTROL RET	Connections from power supply to dimmer control.
444A 444C 444O	- - -	56 16 33	SD444A } WD444C } WD444O }	SPARE	SPARE (1100-5) (WL) NC None NC None NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 5 (par 30-145B).
445A 445C 445O	- - -	34 6 17	SD445A } WD445C } WD445O }	SPARE	SPARE (1100-7) NC None NC None NC	Connections to contacts of relay SPARE of bank 14 which is controlled by bit 7 (par 30-145B).
446 447 448 449	- - - -	62 63 64 65	WD446 WD447 WD448 WD449	5V CAUT POWER (LVYHI) 5V CAUT POWER RET (LVYLO) 5V STATUS POWER (LVWHI) 5V STATUS POWER RET (LVWLO)	5V CAUT LGHT PWR HI 5V CAUT LGHT PWR LO 5V STATUS LGHT PWR HI 5V STATUS LGHT PWR LO	5VDC power for illumination of indicators.
450	-	57	WD450	ALARM COMMON	RETURN 439-441	See lines 440A and 440C.
451A 451C 451O	- - -	32 14 15	SD451A } WD451C } WD451O }	CIRCUIT	AGC WARNING (LMP) INHIBIT PIPA (PLS TORQ) (LMP/) None NC	Connections to contacts of relay CIRCUIT which is operated by signal 237.

(cont)

TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings $\triangle 1$	Name Used in DD Memo 185 $\triangle 3$	Signal Description		
	A51 of AGC	J9 of DSKY					
452A 452C 452O	- - -	81 $\triangle 2$ 82 $\triangle 2$ 80 $\triangle 2$	SD452A } WD452C } WD452O }	ISS WARNING	ISS WARNING (LMP) None None	NC	Connections to contacts of relay ISS WARNING which is operated by signal 229.
453A 453C 453O	- - -	35 59 58	SD453A WD453C WD453O		STANBY None None	NC NC NC	Connections to contacts of relay STBY which is operated by signal 231.
801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816	209 109 610 510 410 310 210 110 611 511 411 311 211 111 612 512	- - - - - - - - - - - - - - - -	CB801 CB802 CB803 CB804 CB805 CB806 CB807 CB808 CB809 CB810 CB811 CB812 CB813 CB814 CB815 CB816	RC+X+P RC+X-P RC+X+Y RC+X-Y RC-X+P RC-X-P RC-Y+X RC-X-Y RC+Y+R RC+Y-R RC-Y+R RC-Y-R RC+Z+R RC+Z-R RC-Z+R RC-Z-R	-X/-P/+R, 4U No. 1 +X/-R/-P, 3D No. 6 -X/+P/-R, 2U No. 9 +X/+R/+P, 1D No. 14 -X/+R/+P, 3U No. 5 +X/+P/-R, 4D No. 2 -X/-R/-P, 1U No. 3 +X/-P/+R, 2D No. 10 +Y/+YAW, 2S No. 12 +Y/-YAW, 1S No. 16 -Y/+YAW, 4S No. 4 -Y/-YAW, 3S No. 8 +Z/+YAW, 3F No. 7 +Z/-YAW, 2F No. 11 -Z/+YAW, 1F No. 15 -Z/-YAW, 4F No. 3		Bit positions 1 through 8 of channels 5 and 6 (gates 43105, 43111, 43117, 43123, 43129, 43135, 43141, 43147, 43259, 43254, 43249, 43244, 43239, 43234, 43223, and 43205) generate signals RC+X+P through RC-Z-R (column 4) which control interface circuits 5C through 1C of A25 and 34C through 24C of A26 which operate the reaction control system.
817 818 819 820 821 822	158 258 157 257 156 256 155 255 154 254 153 253	- - - - - -	YG817H } YG817L } YG818H } YG818L } YG819H } YG819L } YG820H } YG820L } YG821H } YG821L } YG822H } YG822L }	BMGXP BMGXM BMGYP BMGYM BMGZP BMGZM	NC NC NC NC NC NC		Interface circuits 1Y through 6Y of A29 receive pulses from the body-mounted acceleration gyros and feed gates 46337, 46338, 46346, 46347, 46356, and 46357 of the BMAG/RHC Control (par 30-110 through 30-112).
831 832	643 543	- -	DE831 DE832	TRST9 TRST10	THRUSTER 2U/2S FAIL THRUSTER 2D/2F FAIL		Interface circuits 5D and 6D of A28 receive DC signals from the spacecraft and feed bit position 7 and 8 (gates 44239 and 44241) of channel 32 (table 30-5F).

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings Δ		Name Used in DD Memo 185 Δ		Signal Description
	A51 of AGC	J9 of DSKY					
840	621	-	DE840	IN3301	SPARE CHN 33-01	NC	Interface circuit 17D of A27 is able to receive DC signals and feeds bit position 1 (gate 44102) of channel 33 (table 30-5G). Not used, spare.
841	213	-	MROLGT	CB841	-ROLL GIMBAL TRIM		Bit position 12 (gate 43450) of channel 12 (table 30-5A) generates signal MROLGT which controls interface circuits 15C of A26. The interface circuit operates external equipment
842 843	532 632	- -	DE842 DE843	PCHGOF ROLGOF	PITCH GIMBAL OFF ROLL GIMBAL OFF		Interface circuits 16D and 15D of A28 receive DC signals from the spacecraft and feed bit positions 9 and 10 (gates 44243 and 44245) of channel 32 (table 30-5F).
844 845	- -	- -	DE844 DE845	IN3214 IN3216	SPARE CHN 32-14 SPARE CHN 32-16	NC NC	Interface circuits 5D of A26 and 10D of A26 are able to receive DC signals and feed bit positions 14 and 15 (gates 44140 and 44143) of channel 32 (table 30-5F). Not used, spares.
848 850 851 852 853 854 855	- - - - - - -	- - - - - - -	OT1108 OT1110 OT1111 OT1112 OT1113 OT1114 OT1116	CB848 CB850 CB851 CB852 CB853 CB854 CB855	SPARE CHN 11-08 SPARE CHN 11-10 SPARE CHN 11-11 SPARE CHN 11-12 SPARE CHN 11-13 SPARE CHN 11-14 SPARE CHN 11-16	NC NC NC NC NC NC NC	Bit positions 8 and 10 through 15 (gates 48422, 49252, 49253, 49254, 48427, 48432, and 48437) of channel 11 (table 30-5) generate signals OT1108 and OT1110 through OT1116 (column 4) which control interface circuits 6C through 1C and 9C of A26. Not used, spares.
858 859 860	142 242 141 241 140 240	- - - -	A-858H } A-858L } A-859H } A-859L } A-860H } A-860L }		PROP PITCH RATE CMD PROP ROLL RATE CMD PROP YAW RATE CMD		Each line is connected to an RHC converter (one each in A27, A28, and A29). Each feeds the BMAG/RHC Control (figure 30-6 and par 30-113 through 30-115).
861 863 865 866 867 868 869 870	520 637 539 635 535 634 642 619	- - - - - - - -	+28COM +28COM +28COM +28COM +28COM +28COM +28COM +28COM	RD861 RD863 RD865 RD866 RD867 RD868 RD869 RD870	160/841/902/906 83 173/174 188/189 831/832 67/68 NC NC		Resistor 7R of A27 Resistor 7R of A28 Resistor 6R of A28 Resistor 9R of A28 Resistor 1R of A27 Resistor 2R of A27 Resistor 3R of A28 Resistor 8R of A27 } provide +28VDC

(cont)

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TABLE 30B-1

LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

Line or Signal Number	Connecting Pins at		Name Used on Drawings Δ	Name Used in DD Memo 185 Δ	Signal Description
	A51 of AGC	J9 of DSKY			
874 875 876 877 878 879	658 - 633 656 533 519	- - - - - -	+28COM RD874 - +28COM RD876 +28COM RD877 +28COM RD878 +28COM RD879	104/64/69 104/64/69 106/107/183 842/843 39/61 7/158 NC	Resistor 1R and 2R of A29 in parallel - Resistor 3R of A27 Resistor 3R of A29 Resistor 4R of A27 Resistor 9R of A27 } provide +28VDC
901	324 424	-	25 KPPS { XC901H XC901L	25.6 KPPS (PWR SUP SYNC)	Gate 49220 of the Timer generates 25KPPS pulses which control interface circuit 8XT of A26. Pulses are provided to operate power supplies in the spacecraft.
902	212	-	DISDAC CB902	+ROLL GIMBAL TRIM	Bit position 11 (gate 43342) of channel 12 (table 30-5A) generates signal DISDAC which controls interface circuit 21C of A26. The interface circuit operates the IMU.
903 904	521 542	- -	+28COM RD903 +28COM RD904	14VB (AGC OPERATE) 171/172	Resistors 5R of A27 and 4R of A28 provide +28VDC.
906	113	-	ZEROPT CB906	-PITCH GIMBAL TRIM	Bit position 10 (gate 43340) of channel 12 (table 30-5A) generates signal ZEROPT which controls interface circuit 14C of A26. The interface circuit operates the IMU.
907	556	-	RD907 +28COM	18-23	Resistors 4R and 5R of A29 in parallel provide +28VDC.
908	-	-	-	18-23	
909	114	-	ISSTDC CB909	ISS TURN ON DELAY CMPLT	Bit position 15 (gate 48445) of channel 12 (table 30-5A) generates signal ISSTDC which controls interface circuit 8C of A26. The interface circuit operates the ISS.
910 911	216 215	- -	W-910 W-911	CNTRL 1 (ACE) (LOW) CNTRL 2 (ACE) (HIGH)	

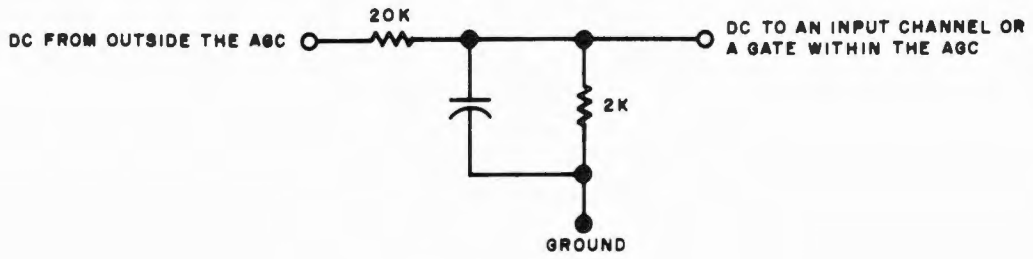
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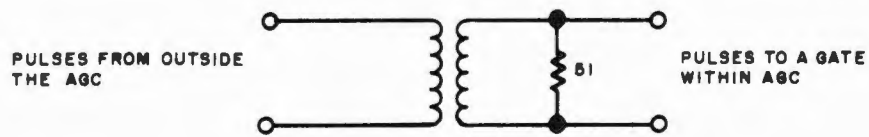
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LUNAR EXCURSION MODULE AGC SUBSYSTEM INPUT AND OUTPUT SIGNALS (cont)

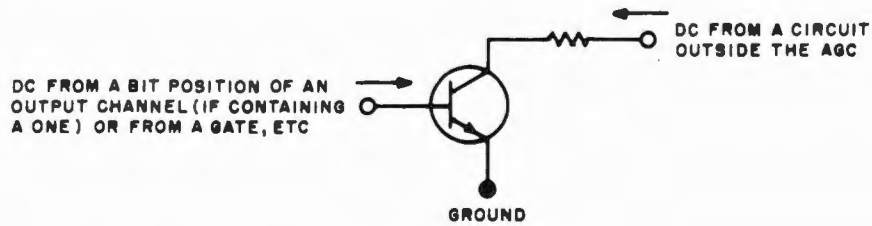
Line or Signal Number	Connecting Pins at		Name Used on Drawings ¹	Name Used in DD Memo 185 ³	Signal Description
	A51 of AGC	J9 of DSKY			
912	214	-	D-912 NHVFAL	INHIBIT POWER FAIL	Interface circuit 1D of A26 receives DC signals from spacecraft and feeds gates 41204 and 41205 of the Alarm Control (par 30-141R).
<p>¹ Pin numbers and signal names were taken from NASA drawings 2005020, 2005021, 2005900, and 2005950; and from the AGC BLOCK II COMPUTER WIRE LIST.</p> <p>² For DSKY's 200B, 200C, 200M, and 600M, pin numbers apply to 85 pin connector of adapter cable.</p> <p>³ NC means AGC not connected to external equipment.</p>					



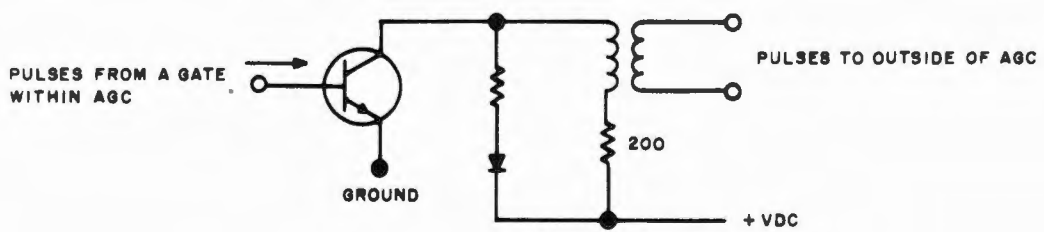
INPUT CIRCUIT D



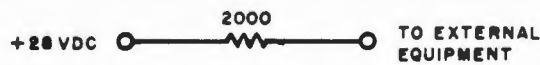
INPUT CIRCUIT Y



OUTPUT CIRCUIT C



OUTPUT CIRCUIT XT



OUTPUT CIRCUIT R

Figure 30B-1. Interface Circuits

ISSUE 30
APPENDIX C

TEST CONNECTOR SIGNALS

All lines or signals passing through connector A52 of the AGC are listed in table 30C-1 of this appendix. Information is arranged in alphabetical order of signal names. The numbers of the connecting pins are given in column 2 while signal descriptions are contained in the last column.

TABLE 30C-1
TEST CONNECTOR SIGNALS

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
ALGA	507	Line is connected to gate 37227 of the start-stop logic and can be used to ground the ALGA input to prevent stop-start operations due to computer failure.
BPLSSW	801	BPLSSW power provided by AGC.
CNTRL1	701	} Lines are connected to the Power Supply (modules A30-31) and can be used to control them.
CNTRL2	702	
DBLTST	811	Line is connected to gate 30057 of the Alarm Control and can be used to test the double frequency alarm (paragraph 30-141Y).
DOSCAL	810	Line is connected to gate 32258 of the Alarm Control and can be used to test the scaler alarm circuits.
MBR1	501	} Signals are generated by gates 36260 and 36262 of the branch flip-flops (BR) when the flip-flops contain a ONE.
MBR2	502	
MCTRAL/	504	Signal is generated by gates 41144 and 41145 of the Alarm Control when a counter alarm occurs.

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings 1	Connecting Pin of Con- nector A52 of AGC 1	Signal Description 2
MDT01	101	<p>Lines are connected to gates 51158, 51258, 51458, 51358, 52158, 52258, 52458, 52358, 53158, 53258, 53458, 53358, 54158, 54258, 54458, and 54358 of the WA's and can be used to insert information into the AGC.</p>
MDT02	102	
MDT03	103	
MDT04	104	
MDT05	105	
MDT06	106	
MDT07	107	
MDT08	108	
MDT09	109	
MDT10	110	
MDT11	111	
MDT12	112	
MDT13	113	
MDT14	114	
MDT15	115	
MDT16	116	
MGOJAM	510	Signal is generated by gate 37251 of the start-stop logic when signal GOJAM occurs.
MGP/	612	Signal is generated by gate 34241 of the Parity Block when a parity bit CP15 is generated.
MIIP	503	Signal is generated by gate 30112 of the Interrupt Priority Control when signal IIP (interrupt in progress) occurs.




(cont)

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
MINHL	511	Signal is generated by gate 30111 of the Interrupt Priority Control when the inhibit interrupt flip-flop is set.
MINKL	512	Signal is generated by gate 32253 of the Counter Priority Control when signal INKL occurs.
MLDCH	611	Line is connected to gate 32220 of the Counter Priority Control and can be used to request the execution of instruction INOTLD.
MLOAD	713	Line is connected to gate 32204 of the Counter Priority Control and can be used to request the execution of instruction STORE E.
MNHNC	604	Line is connected to gate 32240 of the Counter Priority Control and can be used to inhibit counter incrementations.
MNRPT	605	Line is connected to gate 30117 of the Interrupt Priority Control and can be used to inhibit interrupt.
MNHSBF	603	Line is connected to gate 42122 of the F memory cycle timer and can be used to inhibit strobe F.

(cont)

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings 	Connecting Pin of Con- nector A52 of AGC 	Signal Description 
MNISQ	710	Signal is generated by gate 49238 when signal NISQ/ occurs.
MONPAR	707	Line is connected to gate 34245 of the Parity Block and can be used to enter a parity bit.
MONWBK	708	Line is connected to gate 39426 in the SQG and can be used to prevent the generation of control pulse U2BBK.
MONWT	514	This 1.024 Mpps clock signal is generated by gate 37136 of the Timer and is similar to signal CLK (001).
MON800	715	This 800 pps signal is generated by gate 49238 if the Timer is similar to signal FS07A.
MOSCAL/	815	Signal is generated by gate 41231 when signal STRT2 occurs.
MPAL/	508	Signal is generated by gate 34252 of the Parity Control when a parity alarm occurs.
MPIPAL/	716	Signal is generated by gate 41106 of Alarm Control when signal PIPAFL occurs.

(cont)

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
MRAG	616	Signal is generated by gate 33326 when signal RAG/ occurs.
MRCH	706	This signal is generated by gate 49335 when signal RCH/ occurs.
MRDCH	610	Line is connected to gate 32224 of the Counter Priority Control and can be used to request the execution of instruction INOTRD H.
MREAD	714	Line is connected to gate 32211 of the Counter Priority Control and can be used to request the execution of instruction FETCH K.
MREQIN	711	Signal is generated to gate 32230 of the Counter Priority Control when the request for the execution of instruction FETCH K, STORE E, INOTRH H, or INOTLD H has been received.
MRGG	614	Signal is generated by gate 33320 when signal RGG/ occurs.
MRLG	516	Signal is generated by gate 33335 when signal RLG/ occurs.

(cont)

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings \triangle_1	Connecting Pin of Con- nector A52 of AGC \triangle_1	Signal Description \triangle_2
MRPTAL/	506	Signal is generated by gates 41114 and 41115 of the Alarm Control when a RUPT alarm occurs.
MRSC	515	Signal is generated by gate 36459 of SQG when control pulse RSC/ occurs.
MRULOG	313	Signal is generated by gate 33347 when signal RUG/, RUSG/, or RULOG/ occurs.
MSBSTP	609	Not connected.
MSCAFL/	814	Signal is generated by gate 41222 when signal SCAFAL occurs.
MSCDBL /	808	Signal is generated by gate 34254 when signal SCADBL occurs.
MSP	613	Signal is generated by gate 34244 of the Parity Block when a parity bit is entered from memory.
MSQ10	410	} Signals are generated by gates 30140, 30139, 30138, 30028, 30025, 30123, and 30022 of register SQ when the respective bit positions contain a ONE.
MSQ11	411	
MSQ12	412	
MSQ13	413	
MSQ14	414	
MSQEXT	415	
MSQ16	416	

(cont)

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
MSTP	608	Line is connected to gate 37235 of the start-stop logic and can be used to stop computer operation.
MSTPIT/	509	Signal is generated by gate 37244 of the start-stop logic when signal STOP occurs.
MSTRT	607	Line is connected to gate 41101 of the start-stop logic and can be used to start computer operation.
MST1 MST2 MST3	401 402 403	} Signals are generated by gates 36116, 36125, and 36143 of the stage flip-flops (ST) when the flip-flops contain a ONE.
MTCAL/	505	Signal is generated by gates 41127 and 41128 of the Alarm Control when a TC alarm occurs.
MTCSA	404	Signal is generated by gate MTCSA of the SQG when subin-struction TCSAJ3 is executed.
MTCSAI	606	Line is connected to gate 30101 of the Interrupt Priority Control and gates 36112 and 36130 of the SQG and can be used to execute instruction TCSAJ K.
MTHI MTL0	703 704	} Lines are connected to the temperature sensor within the oscillator (module B07) and can be used to check temperature.

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
MT01 MT02 MT03 MT04 MT05 MT06 MT07 MT08 MT09 MT10 MT11 MT12	301 302 303 304 305 306 307 308 309 310 311 312	Signals are generated by gates 37404, 37407, 37411, 37415, 37422, 37427, 37432, 37437, 37442, 37447, 37450, and 37454 of the Time Pulse Generator when time pulses T01 through T12 occur.
MVFAIL/	816	Signal is generated by gate 41207 when signal STRT1 occurs.
MWAG	615	Signal is generated by a BN gate 33255 when signal WAG/ occurs.
MWARNF/	812	Signal is generated by gate 41223 when signal FLTOUT occurs.
MWATCH/	712	Signal is generated by gate 49118 when signal WATCH occurs.

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(cont)

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TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings ①	Connecting Pin of Con- nector A52 of AGC ①	Signal Description ②
MWBEG	316	Signal is generated by gate 33315 when information is written into both registers EBANK and FBANK (address 0006).
MWBG	409	Signal is generated by gate 33135 of register B when information is written into this register.
MWCH	705	Signal is generated by gate 49334 when signal WCH/ occurs.
MWEBG	315	Signal is generated by gate 33303 when information is written into register EBANK (0003).
MWFBG	314	Signal is generated by gate 33311 when information is written into register FBANK (0004).
MWG	709	Signal is generated by gate 33139 when information is written into register G.
MWLG	513	Signal is generated by gate 33218 when signal WLG/ occurs.

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings △₁	Connecting Pin of Con- nector A52 of AGC △₁	Signal Description △₂
MWL01	201	<p>Signals are generated by gates 51153, 51253, 51453, 51353, 521153, 52253, 52453, 52353, 53153, 53253, 53453, 53353, 54153, 54253, 54453, and 54353 when the WA's contain a ONE.</p>
MWL02	202	
MWL03	203	
MWL04	204	
MWL05	205	
MWL06	206	
MWL07	207	
MWL08	208	
MWL09	209	
MWL10	210	
MWL11	211	
MWL12	212	
MWL13	213	
MWL14	214	
MWL15	215	
MWL16	216	
MWQG	408	<p>Signals are generated by gates 33241, 33115, and 33251, of registers S, Y, and Q when information is written into the respective registers.</p>
MWSG	405	
MWYG	407	

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Draw- ings $\triangle 1$	Connecting Pin of Con- nector A52 of AGC $\triangle 1$	Signal Description $\triangle 2$
MWZG	406	Signal is generated by gate 33207 of register Z, when information is written into this register.
NHALGA	809	Line is connected to gate 41118 of the Alarm Control and can be used to inhibit the generation of signal ALGA.
OUTCOM	813	Signal is generated by gate 49339 when signal FF1109/ is present (bit position 9 of channel 11 contains a ONE.
STRT1	601	} Both lines are connected to gate 37228 of the start-stop logic and can be used to ground the STRT1 or STRT2 input to prevent stop-start operations due to power supply or oscillator failure.
STRT2	602	
+4SW	802	+4SW power power provided by AGC.
—	803	} Spare pins
—	804	

TABLE 30C-1
TEST CONNECTOR SIGNALS (cont)

Signal Name Used on Drawing ①	Connecting Pin of Con- nector A52 of AGC ①	Signal Description ②
<p>_____</p> <p>_____</p> <p>_____</p>	<p>805</p> <p>806</p> <p>807</p>	<p>} Spare pins</p>

① Pin numbers and signal names were taken from NASA drawings 2005020, 2005021, 2005900, and 2005950; and from the AGC BLOCK II COMPUTER WIRE LIST.

② Numbers in () refer to signals listed in table 30A-1.

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