APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 3

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AGC INFORMATION SERIES

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AGC INFORMATION SERIES

ISSUE 3

CENTRAL PROCESSOR

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3-1. INTRODUCTION

3-2. This is the third issue of the AGCIS published to inform members of the technical staff at MIT and Raytheon about the AGC and Apollo G & N system. This issue presents a subsystem description of the Central Processor and of registers S, SQ and BNK. Most information pertaining to the Central Processor was originally taken from NASA drawings 1006511, 1006513, 1006515, 1006516, and 1006512. NASA drawings 1006540, 1006541, 1006542, 1006543, 1006544 will show the final configuration of the Central Processor.

3-3. GENERAL

3-4. A basic description of the Central Processor (CP) and of computer manipulations is presented in paragraphs 1-60 through 1-68 of Issue 1. Issue 2 deals with the execution of Machine Instructions. The Central Processor, (figures 1-10, 1-11 and 3-1) consists of six central registers (A, Q, Z, LP, B and G), nine IN and OUT registers, 16 write amplifiers (WA01-WA16), the adder, the parity block, and a variety of service gates. All central registers and the adder consist of sixteen bit positions. One bit position of each register, one of the adder, and one write amplifier are contained in each of the sixteen identical bit sticks. Sticks 1 through 14 store bits 1 through 14 of any data word. Stick 15 stores the overflow bit (bit US) or the parity bit (bit 0) of a word. The sign bit (bit SG) is normally stored in Stick 16. Table 1-6 lists all registers of the CP and registers S, SQ and BNK. All of these registers are integrated NOR gate flip-flop registers.

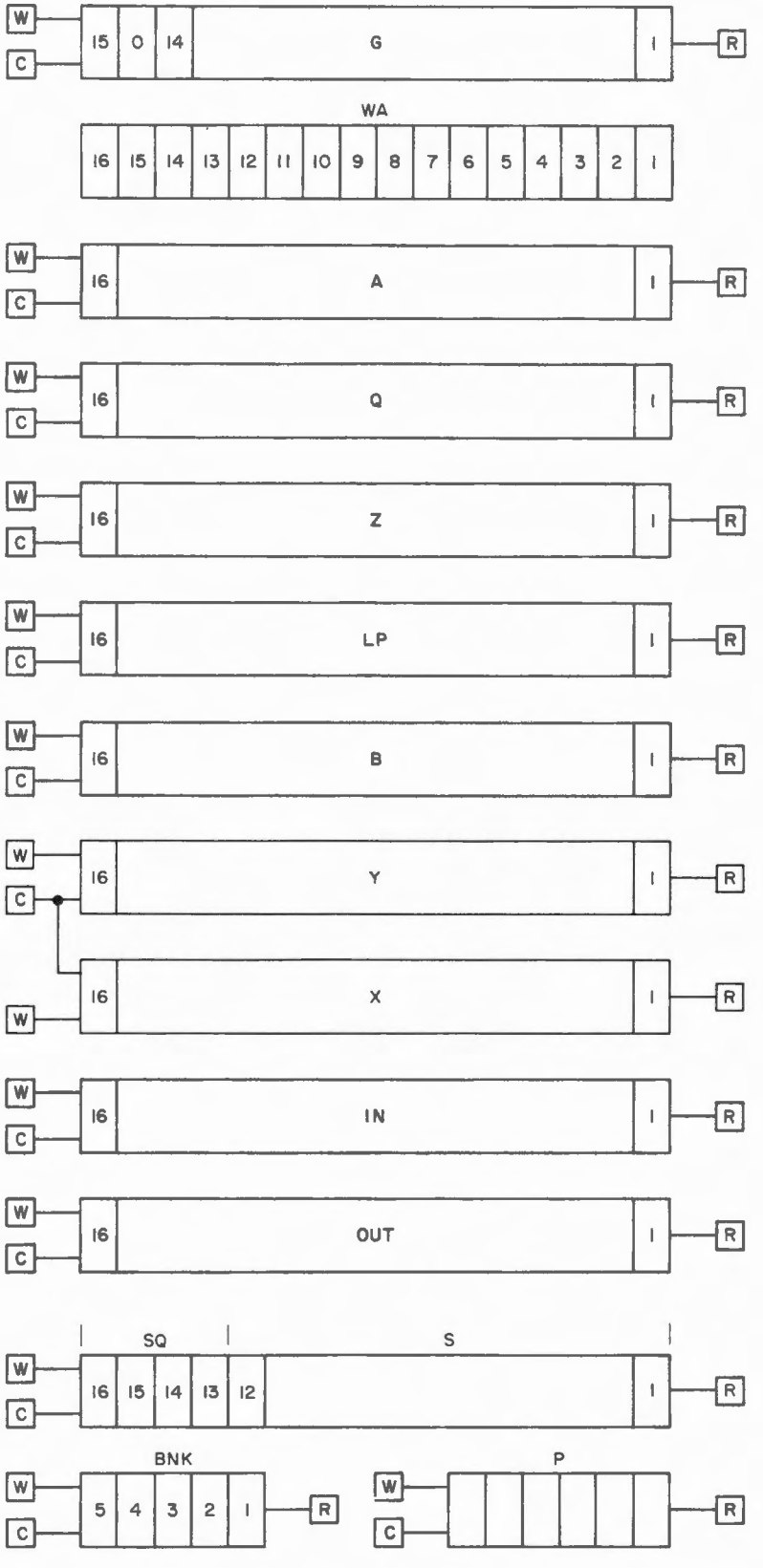

Figure 3-1. Central Processor, Block Diagram

3-5. The Central Processor accepts information entered via the memory buffer (register G) and the input registers (registers IN0 through IN3), to perform certain data manipulations and arithmetic operations (by means of the central registers and the Adder under control of the sequence generator), to test parity and to initiate an alarm in case of incorrect parity (by means of the parity block), and to provide information and control signals through the output registers (OUT0, OUT1, OUT2, and OUT4).

3-6. The function of each register is indicated below:

a. Register A, the accumulator, normally retains information between the execution of individual instructions.

b. Register Q stores the return address after the execution of a TC K instruction. This register also holds the dividend during a DV K instruction and contains the remainder (complement of absolute value).

c. Register Z, the program counter, stores the address of the Basic Instruction to be executed next.

d. Register LP, the low order product storage, is used during the execution of instructions MP K and DV K.

e. Registers IN 0, IN 2, and IN 3 store binary input data.

f. Register IN 1 stores time information as generated by the Time Scaler B.

g. Registers OUT 0, OUT 1, and OUT 2 store binary output data and control signals.

h. Register IN-OUT 3 is a spare register which can be wired as an input or output register.

j. Register OUT 4 provides information for the downlink.

k. Register BNK, the bank register, holds the number of that bank in fixed memory from which information is to be read-out.

l. Register B is mainly used for storing the regular instruction to be executed next.

m. Registers X and Y are a part of the Adder.

n. Register SQ (four bits) and Register S (twelve bits) provide the inputs to the sequence generator and the address selection, hold the order code and the relevant address of an instruction being executed or the address of the instruction to be executed next.

p. Register P is a part of the Parity Block.

q. Register G is the buffer between the CP on one side, E and F memory on the other side.

The IN and OUT register bit assignments are indicated in table 1-7.

3-7. In the AGC a logical ONE is represented by a positive potential of approximately 1 volt and a logical ZERO by a positive potential of about 0.2 volt. Since each NOR gate inverts voltage levels, a logical ZERO can represent either a data ZERO or a data ONE dependent on the operational location of a gate, and a logical ONE can represent a data ONE or a data ZERO. A data ONE is represented by a logical ONE (positive potential of approximately 1 volt) at the input of the write amplifiers, and a data ZERO by a logical ZERO (positive potential of about 0.2 volt). At the output of the write amplifiers, a logical ONE (positive potential of approximately 1 volt) represents a data ZERO, and a logical ZERO (positive potential of approximately 0.2 volt) represents a data ONE.

3-8. OPERATION OF REGISTERS

3-9. The information that is written into a register or read out of a register is indicated in table 1-6. In figure 3-1, most registers are shown as a block with sixteen bit positions accompanied by a write gate W, a clear gate C, and a read gate R. Write-in, clearing, or read-out of information is accomplished by enabling all bit positions of a register simultaneously. Table 1-6 indicates the information that is written into each

register. For the majority of registers, this information is that which is present on write lines 1 through 16. Table 3-1 lists the various signals which are fed into the write, clear and read gates, and indicates the write, clear, and read signals generated by these gates.

3-10. Figure 3-2 illustrates as an example the operation of a single bit position (for instance, bit one) of register Z. Signals CZG, $\overline{\text{WZG}}$, and $\overline{\text{RZG}}$ are produced by register service gates described below. The clear signal occurs during the first 1/4 microsecond of the 3/4 microsecond write pulse, and clears or resets the flip-flop. The information on the write line (in this case $\overline{\text{WL01}}$) coincident with the write control signal $\overline{\text{WZG}}$ is then written into the flip-flop. If the information is a data ONE, the flip-flop is set; if the information is a data ZERO, the flip-flop remains reset. The information bit is read out of the flip-flop by read signal $\overline{\text{RZG}}$ which enables the read gate. The output of the read gate is applied to the write amplifier. This same procedure, described above, occurs simultaneously for all 16 bit positions in the register when the appropriate write, clear, and read pulses are active.

3-11. All of the remaining flip-flop registers of the Central Processor operate in a similar manner as that described for register Z above. The bit information written into these remaining registers may be different from that written into register Z. This can be ascertained from table 3-2, which indicates the information that is gated into the bit positions of each register.

3-12. Register G transfers information from the WA's to E memory, or from E or F memory into the WA's of CP. The G register has several input write functions as indicated in figure 3-3 and table 3-3. The memory sense amplifier outputs (SA01, SA02 etc.) connect directly to the flip-flop inputs which are represented in figure 3-3 by rectangles. Information

TABLE 3-1

REGISTER WRITE, CLEAR, AND READ SIGNALS

Register	Write		Clear		Read	
	Gating Functions	Write Signal	Gating Functions	Clear Signal	Gating Functions	Read Signal
A (0000)	$\overline{WA}$ 234 SEA01	$\overline{WAG}$	$\overline{WA}$ 12	CAG	$\overline{RA}$ 234 SEA02	$\overline{RAG}$
	$\overline{WALP}$ 234	$\overline{WALPG}$				
Q (0001)	$\overline{WQ}$ 234 SEA03	$\overline{WQG}$	SEA09 SEA12	CQG	$\overline{RQ}$ 234 SEA04	$\overline{RQG}$
Z (0002)	$\overline{WZ}$ 234 SEA05	$\overline{WZG}$	SEA14 SEA11	CZG	$\overline{RZ}$ 234 SEA06	$\overline{RZG}$
LP (0003)	$\overline{WLP}$ 234 SEA07	$\overline{WLPG}$	SEA10 SEA13	CLPG	$\overline{RLP}$ 234 SEA08	$\overline{RLPG}$
B	$\overline{WB}$ 234	$\overline{WBG}$	$\overline{WB}$ 12	CBG	$\overline{RB}$ 234 RBQ $\overline{RC}$ 234	$\overline{RBG}$ $\overline{RCG}$
Y	$\overline{WY}$ 234	$\overline{WYG}$	$\overline{WY}$ 12	CUG	$\overline{RU}$ 234 RUS	$\overline{RUG}$
X	$\overline{WX}$ 234	$\overline{WXG}$				
SQ	$\overline{NISQ}$ 234	$\overline{WSQG}$	$\overline{WS}$ 12	CSG	(None)	
S	$\overline{WS}$ 234 MP1	$\overline{WSG}$				
BNK	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB5}$	$\overline{WBKG}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB1}$	CBKG	$\overline{RSC234}$ $\overline{XT1}$ $\overline{XB5}$	$\overline{RBKG}$

TABLE 3-1

REGISTER WRITE, CLEAR, AND READ SIGNALS (continued)

Register	Write		Clear		Read	
	Gating Functions	Write Signal	Gating Functions	Clear Signal	Gating Functions	Read Signal
G	$\overline{WG}$ $\overline{234}$ CA2 ST01 ST02 ST03	$\overline{WG1G}$ $\overline{WG2G}$ $\overline{WG3G}$ $\overline{WG4G}$ $\overline{WG5G}$ $\overline{WG6G}$	$\overline{WG}$ $\overline{12}$ CLGS	CGG	$\overline{RG}$ $\overline{234}$ 6F	$\overline{RGG}$
P	$\overline{WP}$ $\overline{A2}$ $\overline{WPS}$	$\overline{WPG}$	$\overline{WP}$ $\overline{12}$	CPG	$\overline{RP2}$ $\overline{234}$	$\overline{RP2G}$
IN0	(None)		SEA15 ZZZZ	CV0G	$\overline{RSC234}$ $\overline{XT0}$ $\overline{XB4}$	$\overline{RV0G}$
IN2	(None)		$\overline{WSC12}$ $\overline{XT0}$ $\overline{XB6}$	CV2G	$\overline{RSC234}$ $\overline{XT0}$ $\overline{XB6}$	$\overline{RV2G}$
IN3	(None)		$\overline{WSC12}$ $\overline{XT0}$ $\overline{XB7}$	CV3G	$\overline{RSC234}$ $\overline{XT0}$ $\overline{XB7}$	$\overline{RV3G}$
OUT0	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB0}$	$\overline{WW0G}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB0}$	CW0G	$\overline{RSC234}$ $\overline{XT1}$ $\overline{XB0}$	$\overline{RW0G}$
OUT1	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB1}$	$\overline{WW1G}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB1}$	CW1G	$\overline{RSC234}$ $\overline{XT1}$ $\overline{XB1}$	$\overline{RW1G}$

TABLE 3-1

REGISTER WRITE, CLEAR, AND READ SIGNALS (continued)

Register	Write		Clear		Read	
	Gating Functions	Write Signal	Gating Functions	Clear Signal	Gating Functions	Read Signal
OUT2	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB2}$	$\overline{WW2G}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB2}$	CW2AG	$\overline{RSC234}$ $\overline{XT1}$ $\overline{XB2}$	$\overline{RW2G}$
			$\overline{WOVR}$, $\overline{OVF}$ $\overline{CA4}$, XB2			
			GOJAM			
			$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB2}$	CW2BG		
			$\overline{WOVR}$, $\overline{OVF}$ $\overline{CA4}$, XB3			
			GOJAM			
			$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB2}$	CW2CG		
			$\overline{WOVR}$, $\overline{OVF}$ $\overline{CA5}$, XB7			
			GOJAM			
IN or OUT3	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB3}$	$\overline{WW3G}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB3}$ GOJAM	CW3G	$\overline{RSC234}$ $\overline{XT1}$ $\overline{XB3}$	$\overline{RW3G}$
OUT4	$\overline{WSC234}$ $\overline{XT1}$ $\overline{XB4}$	$\overline{WW4G}$	$\overline{WSC12}$ $\overline{XT1}$ $\overline{XB4}$	CW4G	(None)	
	$\overline{XB4}$ $\overline{CA1}$ $\overline{GP}$, $\overline{RP2}$	$\overline{WW4PG}$	$\overline{XB4}$ $\overline{CA1}$ $\overline{GP}$, $\overline{RP2}$	CW4PG		

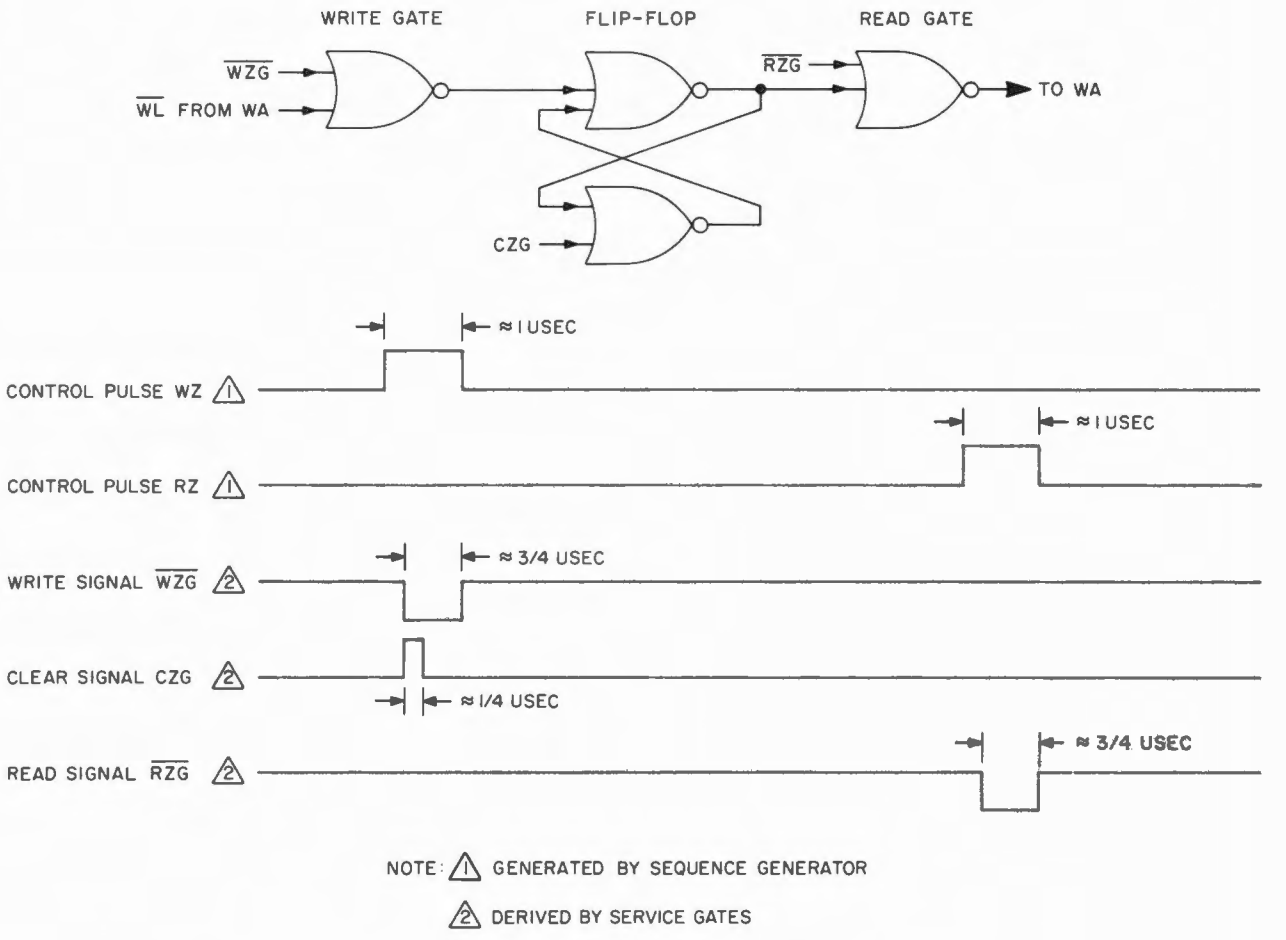

Figure 3-2. Operation of Single Bit Position (Register Z)

TABLE 3-2
WRITE-CONTROL SIGNALS

Bit Position	A Register		Q Register	Z Register	LP Register	
1	$\overline{WL01}$ $\overline{WAG}$	$\overline{WL02}$ $\overline{WALPG}$	$\overline{WL01}$ $\overline{WQG}$	$\overline{WL01}$ $\overline{WZG}$	$\overline{WL02}$ $\overline{WLPG}$	
2	$\overline{WL02}$ $\overline{WAG}$	$\overline{WL03}$ $\overline{WALPG}$	$\overline{WL02}$ $\overline{WQG}$	$\overline{WL02}$ $\overline{WZG}$	$\overline{WL03}$ $\overline{WLPG}$	
3	$\overline{WL03}$ $\overline{WAG}$	$\overline{WL04}$ $\overline{WALPG}$	$\overline{WL03}$ $\overline{WQG}$	$\overline{WL03}$ $\overline{WZG}$	$\overline{WL04}$ $\overline{WLPG}$	
4	$\overline{WL04}$ $\overline{WAG}$	$\overline{WL05}$ $\overline{WALPG}$	$\overline{WL04}$ $\overline{WQG}$	$\overline{WL04}$ $\overline{WZG}$	$\overline{WL05}$ $\overline{WLPG}$	
5	$\overline{WL05}$ $\overline{WAG}$	$\overline{WL06}$ $\overline{WALPG}$	$\overline{WL05}$ $\overline{WQG}$	$\overline{WL05}$ $\overline{WZG}$	$\overline{WL06}$ $\overline{WLPG}$	
6	$\overline{WL06}$ $\overline{WAG}$	$\overline{WL07}$ $\overline{WALPG}$	$\overline{WL06}$ $\overline{WQG}$	$\overline{WL06}$ $\overline{WZG}$	$\overline{WL07}$ $\overline{WLPG}$	
7	$\overline{WL07}$ $\overline{WAG}$	$\overline{WL08}$ $\overline{WALPG}$	$\overline{WL07}$ $\overline{WQG}$	$\overline{WL07}$ $\overline{WZG}$	$\overline{WL08}$ $\overline{WLPG}$	
8	$\overline{WL08}$ $\overline{WAG}$	$\overline{WL09}$ $\overline{WALPG}$	$\overline{WL08}$ $\overline{WQG}$	$\overline{WL08}$ $\overline{WZG}$	$\overline{WL09}$ $\overline{WLPG}$	
9	$\overline{WL09}$ $\overline{WAG}$	$\overline{WL10}$ $\overline{WALPG}$	$\overline{WL09}$ $\overline{WQG}$	$\overline{WL09}$ $\overline{WZG}$	$\overline{WL10}$ $\overline{WLPG}$	
10	$\overline{WL10}$ $\overline{WAG}$	$\overline{WL11}$ $\overline{WALPG}$	$\overline{WL10}$ $\overline{WQG}$	$\overline{WL10}$ $\overline{WZG}$	$\overline{WL11}$ $\overline{WLPG}$	
11	$\overline{WL11}$ $\overline{WAG}$	$\overline{WL12}$ $\overline{WALPG}$	$\overline{WL11}$ $\overline{WQG}$	$\overline{WL11}$ $\overline{WZG}$	$\overline{WL12}$ $\overline{WLPG}$	
12	$\overline{WL12}$ $\overline{WAG}$	$\overline{WL13}$ $\overline{WALPG}$	$\overline{WL12}$ $\overline{WQG}$	$\overline{WL12}$ $\overline{WZG}$	$\overline{WL13}$ $\overline{WLPG}$	
13	$\overline{WL13}$ $\overline{WAG}$	$\overline{WL14}$ $\overline{WALPG}$	$\overline{WL13}$ $\overline{WQG}$	$\overline{WL13}$ $\overline{WZG}$	$\overline{WL14}$ $\overline{WLPG}$	
14	$\overline{WL14}$ $\overline{WAG}$	$\overline{WL15}$ $\overline{WALPG}$	$\overline{WL14}$ $\overline{WQG}$	$\overline{WL14}$ $\overline{WZG}$	$\overline{WL01}$ $\overline{WALPG}$	
15	$\overline{WL15}$ $\overline{WAG}$	$\overline{WL16}$ $\overline{WALPG}$	$\overline{WL15}$ $\overline{WQG}$	$\overline{WL15}$ $\overline{WZG}$	$\overline{WL01}$ $\overline{WLPG}$	
16	$\overline{WL16}$ $\overline{WAG}$	$\overline{WL16}$ $\overline{WALPG}$	$\overline{WL16}$ $\overline{WQG}$	$\overline{WL16}$ $\overline{WZG}$	$\overline{WL01}$ $\overline{WLPG}$	

Bit Position	B Register	X Register	Y Register	S Register
1	$\overline{WL01}$ $\overline{WBG}$	$\overline{WL01}$ $\overline{WXG}$	$\overline{WL01}$ $\overline{WYG}$	$\overline{WL01}$ $\overline{WSG}$
2	$\overline{WL02}$ $\overline{WBG}$	$\overline{WL02}$ $\overline{WXG}$	$\overline{WL02}$ $\overline{WYG}$	$\overline{WL02}$ $\overline{WSG}$
3	$\overline{WL03}$ $\overline{WBG}$	$\overline{WL03}$ $\overline{WXG}$	$\overline{WL03}$ $\overline{WYG}$	$\overline{WL03}$ $\overline{WSG}$
4	$\overline{WL04}$ $\overline{WBG}$	$\overline{WL04}$ $\overline{WXG}$	$\overline{WL04}$ $\overline{WYG}$	$\overline{WL04}$ $\overline{WSG}$
5	$\overline{WL05}$ $\overline{WBG}$	$\overline{WL05}$ $\overline{WXG}$	$\overline{WL05}$ $\overline{WYG}$	$\overline{WL05}$ $\overline{WSG}$
6	$\overline{WL06}$ $\overline{WBG}$	$\overline{WL06}$ $\overline{WXG}$	$\overline{WL06}$ $\overline{WYG}$	$\overline{WL06}$ $\overline{WSG}$
7	$\overline{WL07}$ $\overline{WBG}$	$\overline{WL07}$ $\overline{WXG}$	$\overline{WL07}$ $\overline{WYG}$	$\overline{WL07}$ $\overline{WSG}$
8	$\overline{WL08}$ $\overline{WBG}$	$\overline{WL08}$ $\overline{WXG}$	$\overline{WL08}$ $\overline{WYG}$	$\overline{WL08}$ $\overline{WSG}$
9	$\overline{WL09}$ $\overline{WBG}$	$\overline{WL09}$ $\overline{WXG}$	$\overline{WL09}$ $\overline{WYG}$	$\overline{WL09}$ $\overline{WSG}$
10	$\overline{WL10}$ $\overline{WBG}$	$\overline{WL10}$ $\overline{WXG}$	$\overline{WL10}$ $\overline{WYG}$	$\overline{WL10}$ $\overline{WSG}$
11	$\overline{WL11}$ $\overline{WBG}$	$\overline{WL11}$ $\overline{WXG}$	$\overline{WL11}$ $\overline{WYG}$	$\overline{WL11}$ $\overline{WSG}$
12	$\overline{WL12}$ $\overline{WBG}$	$\overline{WL12}$ $\overline{WXG}$	$\overline{WL12}$ $\overline{WYG}$	$\overline{WL12}$ $\overline{WSG}$
13	$\overline{WL13}$ $\overline{WBG}$	$\overline{WL13}$ $\overline{WXG}$	$\overline{WL13}$ $\overline{WYG}$	$\overline{SQ13}$ $\overline{WSQF}$
14	$\overline{WL14}$ $\overline{WBG}$	$\overline{WL14}$ $\overline{WXG}$	$\overline{WL14}$ $\overline{WYG}$	$\overline{SQ14}$ $\overline{WSQF}$
15	$\overline{WL15}$ $\overline{WBG}$	$\overline{WL15}$ $\overline{WXG}$	$\overline{WL15}$ $\overline{WYG}$	$\overline{WL15}$ $\overline{WSQG}$
16	$\overline{WL16}$ $\overline{WBG}$	$\overline{WL16}$ $\overline{WXG}$	$\overline{WL16}$ $\overline{WYG}$	$\overline{WL16}$ $\overline{WSQG}$

on the write lines (outputs of WAs of CP) is gated through a series of gates, and is written into register G dependent on the address. The particular address causes signals $\overline{WG1G}$ or $\overline{WG2G}$ etc. (table 1-6) to be generated which in turn enable the gates. Normally, $\overline{WG1G}$ is generated and gates the information on write lines 1 through 14 into the G register. $\overline{WG5G}$ enters the content of write line 16 into bit position 15 of register G. However, certain addresses cause signals $\overline{WG2G}$ through $\overline{WG6G}$ to be generated and shift or cycle certain bits into different positions of the register.

3-13. Input registers IN 0, IN 2, and IN 3 are connected directly to the interface circuit and do not have a write gate. Otherwise, the clear, and read signals are applied similar to register Z. The data input to bit positions 15 and 16 of these two registers is identical. Thus, each IN register accepts 15 bits of data.

3-14. Register IN 1 is a part of time scaler B. Its read gate is controlled by read signal $\overline{RVIG}$ the same way as the read gate of register Z is controlled by signal $\overline{RZG}$.

3-15. Registers OUT 0, OUT 1, OUT 2, and OUT 4 are similar in operation to register Z except that bit position 15 is not used. The flip-flops in stick 16 are connected to the read gates of sticks 15 and 16. This causes information contained in bit position 15 to be gated into write amplifiers 15 and 16.

3-16. The write-in, clear and read-out functions of all registers are under control of service gates which are located on various sticks in the computer. Table 3-1 indicates the write, clear, and read signals generated by associated service gates for each register. The write signal is normally generated as a function of a write control signal (e.g. $\overline{WG}$, $\overline{WB}$ etc.) and timing pulse $\overline{234}$. (See figure 3-4). The A, Q, Z, and LP

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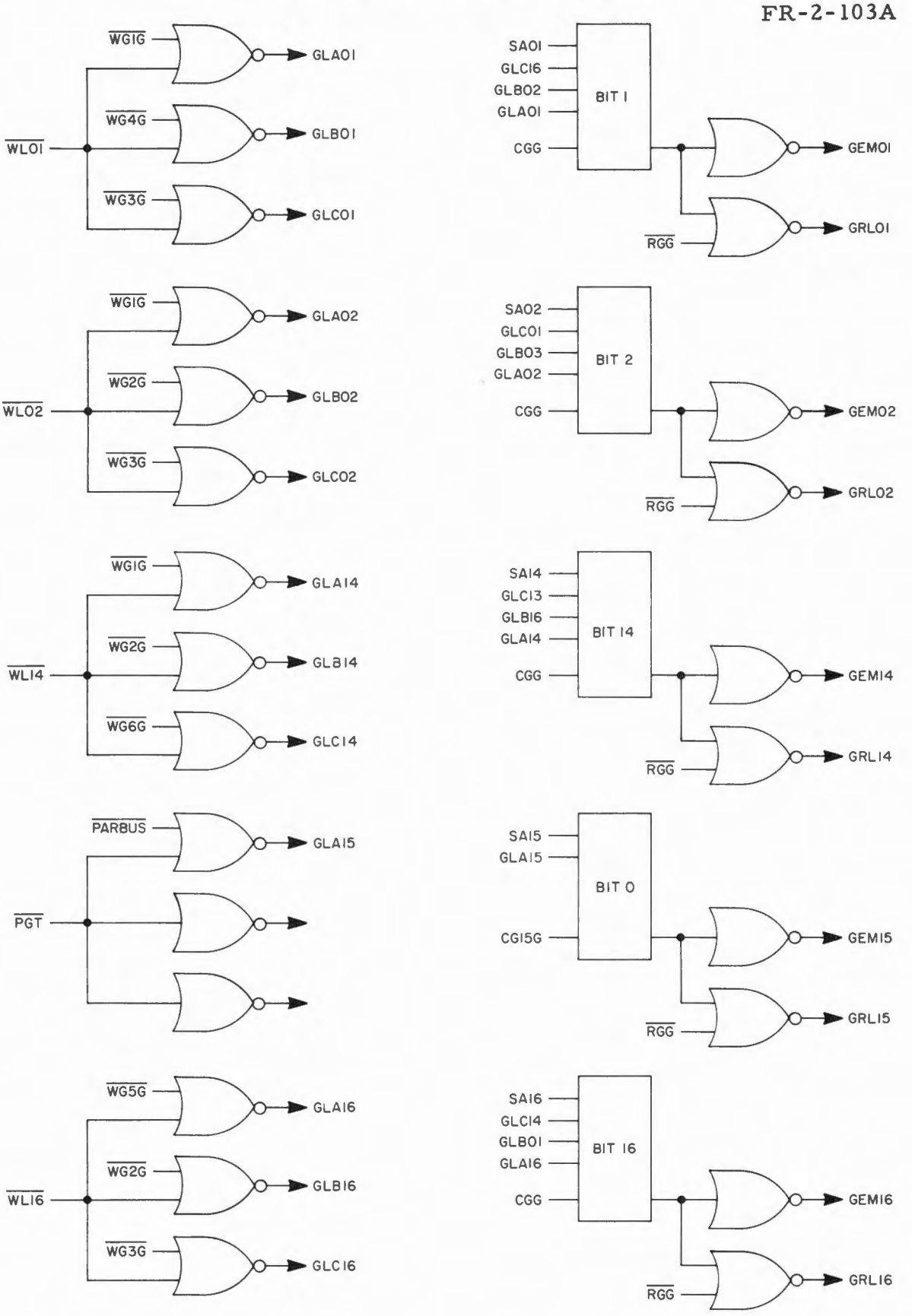

Figure 3-3. G Register

TABLE 3-3

G REGISTER WRITE SIGNAL INPUTS

BIT POSITION	SIGNAL IN			
1	SA01	GLC16	GLB02	GLA01
2	SA02	GLC01	GLB03	GLA02
3	SA03	GLC02	GLB04	GLA03
4	SA04	GLC03	GLB05	GLA04
5	SA05	GLC04	GLB06	GLA05
6	SA06	GLC05	GLB07	GLA06
7	SA07	GLC06	GLB08	GLA07
8	SA08	GLC07	GLB09	GLA08
9	SA09	GLC08	GLB10	GLA09
10	SA10	GLC09	GLB11	GLA10
11	SA11	GLC10	GLB12	GLA11
12	SA12	GLC11	GLB13	GLA12
13	SA13	GLC12	GLB14	GLA13
14	SA14	GLC13	GLB15	GLA14
15	SA15			GLA15
16	SA16	GLC14	GLB01	GLA16

registers incorporate an additional means of generating a write signal. This is indicated by signals SEA01, SEA03, and SEA07 in table 3-3. These signals in turn are a function of memory addressing signals. Thus, the memory addresses 0000 through 0003 (indicated in table 3-1) result in one of the above SEA-- signals which in turn causes a write signal to be produced. As a result, the A, Q, Z and LP registers are addressable. The six different write control signals for register G (para. 3-12) are each generated for a particular editing operation. Two of these control signals are generated at a particular time dependent on the content of register S which is represented by signals CA2, ST01, ST02 and ST03.

3-17. The clear signals are generated, generally, by a write control signal and timing pulse $\overline{12}$ (figure 3-5). Clear signals occur coincident with the first one quarter microsecond interval of the write pulse. Thus, each register is cleared and then immediately written into. The gating functions for generating the Q, Z, and LP register clear signals (as indicated by SEA09 etc. in table 3-1) are result of gating a write control signal and timing pulse $\overline{12}$ or a write control signal with a particular memory address.

3-18. A read signal is normally generated as a function of a read control signal (e.g. $\overline{RG}$, $\overline{RB}$ etc.) and timing pulse $\overline{234}$ (figure 3-6). An additional means of generating a read signal, similar to the write signal, is included for the A, Q, Z, and LP registers as indicated by signals SEA02, SEA04, SEA06, and SEA08 in table 3-1. Read-out of the flip-flop registers is non-destructive. The information stored in each flip-flop is applied to the read gate which is enabled by the read control pulse. The S and SQ registers have no associated read gates. Information contained in these registers is available directly through output amplifiers. Register B has two read gates, one for read-out of the normal content of the register, the other for read-out of complemented content. Register OUT 2 can be read out

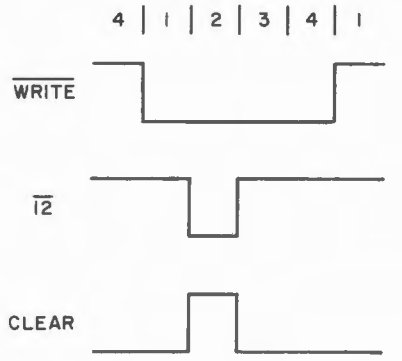

Figure 3-4. Clear Pulse Generation

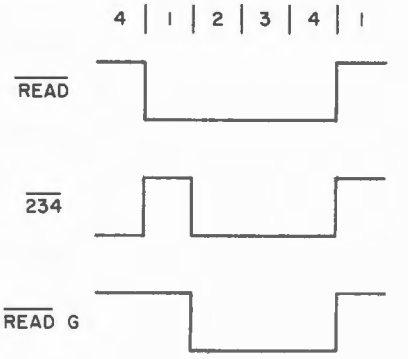

Figure 3-5. Read Pulse Generation

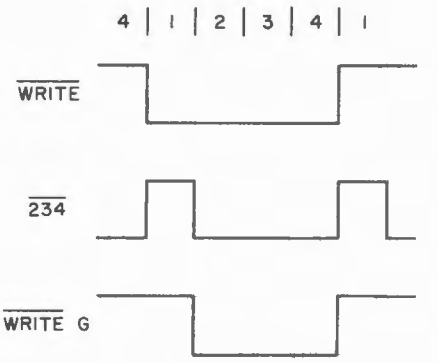

Figure 3-6. Write Pulse Generation

in three bit groups. The read gate of register OUT 4 feeds information into the Downlink circuits instead of into the WA's of the CP.

3-19. WRITE AMPLIFIERS

3-20. There are sixteen write amplifiers, one on each bit stick and each associated with one bit position of each of the registers. The write amplifiers assume the configuration shown in figure 3-7. Gates A through H form an extended NOR gate with 24 inputs. A logical ONE represents a data ONE at these inputs, and a logical ZERO represents a data ZERO. When a ONE arrives at any one of the 24 inputs, the output of the extended NOR gate falls to about 0.2 volt which causes the outputs of gates J and K to rise to approximately 1 volt, providing signals WL--. Gate R is used in connection with the monitor and will be discussed in a later issue. The outputs of gates L, M, N, P and Q fall to about 0.2 volt, providing signal $\overline{\text{WL--}}$.

3-21. OPERATION OF ADDER

3-22. A basic description of the adder is contained in paragraph 1-42 of Issue 1. The adder consists of registers X and Y and associated output and carry gates. The logic for bit positions 1 and 2 of the Adder is shown in figure 3-8. The various signals required to operate the adder are generated by service gates. These signals are indicated in table 3-1.

3-23. The operation of the X and Y flip-flop registers is similar to the operation of register Z (figure 3-2). Signal CUG is the reset signal for both flip-flops. Signal $\overline{\text{WXG}}$ coincident with a logical ONE at the input write gate, sets the X flip-flop. Similarly, $\overline{\text{WYG}}$ coincident with a logical ONE at the input write gate sets the Y flip-flop. A carry bit is sensed for and, if present, is transferred to the next higher order bit position by the carry gate.

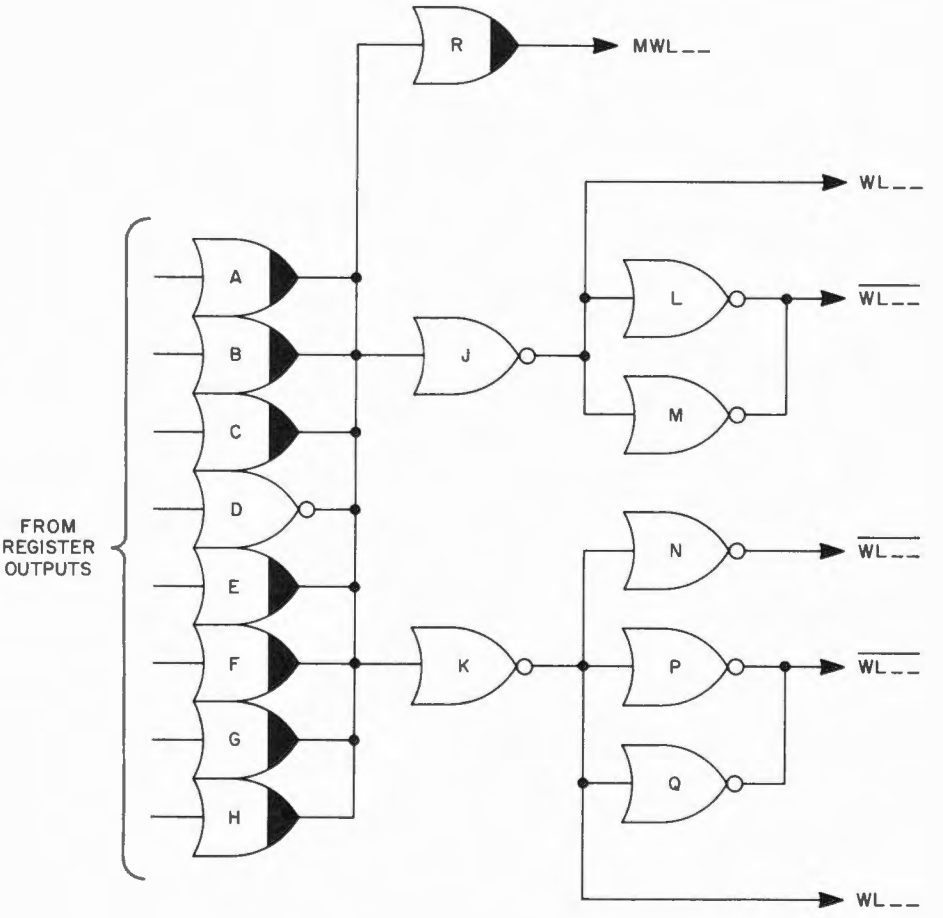

Figure 3-7. Write Amplifier

3-24. A more detailed explanation of the Adder operation follows. (Refer to figure 3-8). The Truth Table (table 3-4) lists the various input and output conditions for a single Adder section (bit position). For instance, if both the x and the y bits are data ONE, and the carry-in bit (ci) is a data ZERO, then a data ZERO has to be generated as a sum (u) bit and a ONE as a carry-out (c_o) bit. The various conditions of u and c_o can be expressed by Boolean equations as follows. (Essential properties of Boolean Algebra have been added for reference.)

$$u = x \cdot \overline{y} \cdot \overline{c_i} + \overline{x} \cdot y \cdot \overline{c_i} + \overline{x} \cdot y \cdot c_i + x \cdot y \cdot c_i$$
$$= (x \cdot \overline{y} + \overline{x} \cdot y) \cdot \overline{c_i} + (x \cdot y + \overline{x} \cdot \overline{y}) \cdot c_i \qquad (1)$$

$$c_o = x \cdot y \cdot \overline{c_i} + x \cdot \overline{y} \cdot c_i + \overline{x} \cdot y \cdot c_i + x \cdot y \cdot c_i$$
$$= x \cdot y + x \cdot c_i + y \cdot c_i = x \cdot y + (x + y) \cdot c_i \qquad (2)$$

+ means OR, · means AND

DeMorgan's Theorem: $\overline{x + y} = \overline{x} \cdot \overline{y}$, $\overline{\overline{x} + \overline{y}} = x \cdot y$, $\overline{x} + \overline{y} = \overline{x \cdot y}$

Idem Point: $x \cdot x = x \quad x + x = x$

Empty Class: $x \cdot \overline{x} = 0$

Universal Class: $x + \overline{x} = 1$

Commutation: $x \cdot y = y \cdot x$, $x + y = y + x$

Distribution: $(x + y) \cdot z = x + y \cdot z$

Association: $(x \cdot y) \cdot z = x \cdot (y \cdot z) = (x \cdot z) \cdot y$

Whenever a carry-out bit is generated, it has to be fed into the next higher section (bit position) of the Adder as carry-in bit c_i. A c_o generated by an addition in bit position 16 normally is fed into bit position 1 as $\overline{\text{CBTI}}$. The purpose of the carry around operation is illustrated in figure 1-8. Whenever a one has to be forced into the Adder, control pulse CI generates signal $\overline{\text{CBTI}}$. This is similar to c_i being fed into bit position 1. (Refer to figure 3-8). If the quantity 000001 is added to 177777, a carry moves from one bit position to the next, and all the way around in approximately 1.6 μsec.

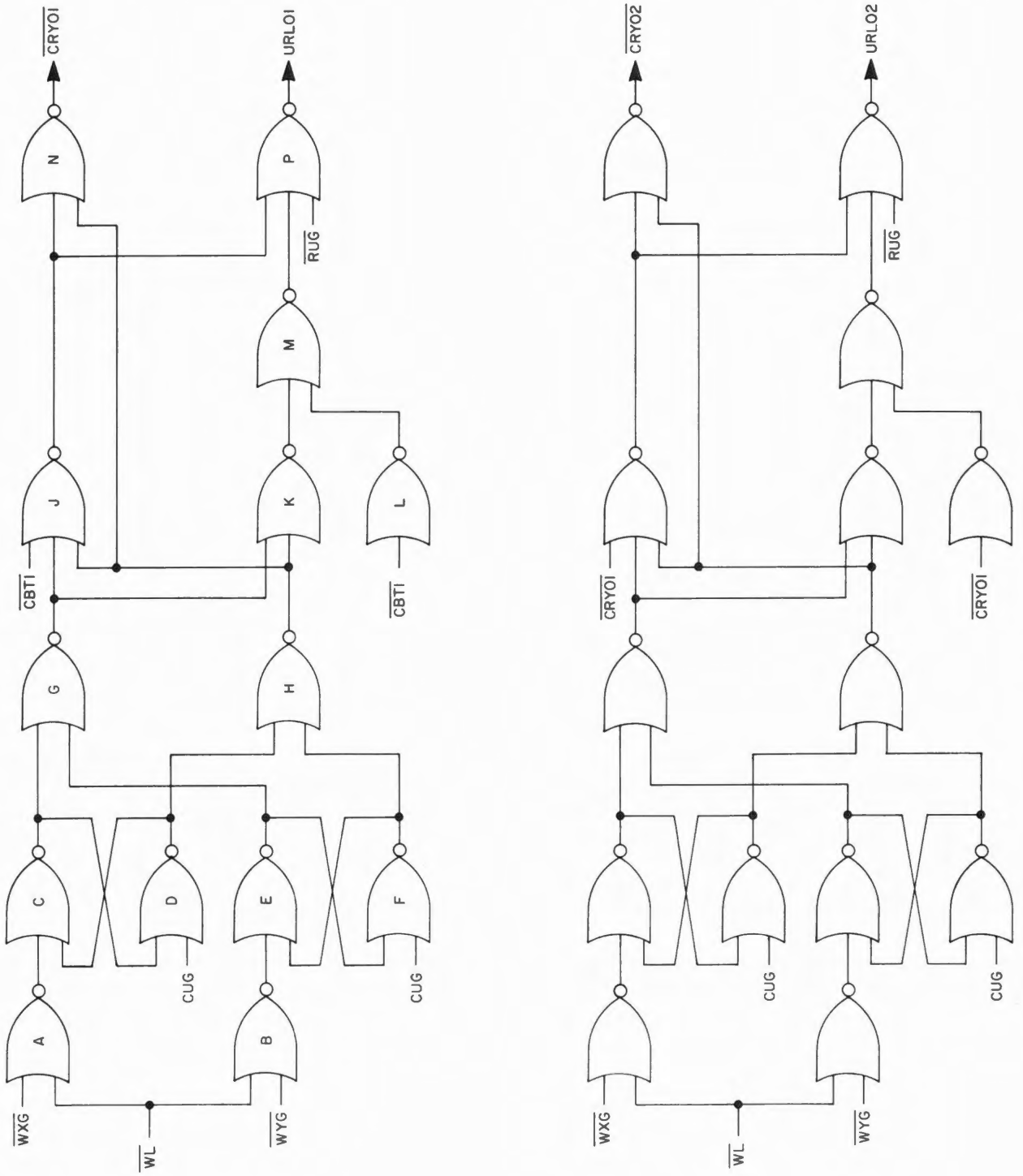

Figure 3-8. Bit Positions 1 and 2 of Adder

TABLE 3-4

TRUTH TABLE FOR ADDITION OF TWO BINARY DIGITS

Inputs		Carry-in	Output SUM	Carry-out
x	y	c_i	u	c_o
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

3-25. The common input of write gates A and B in figure 3-8 is connected to the write line ($\overline{WL}$) on the same stick. The following Boolean equations may be written for the output conditions of the various gates if $\overline{WL}$ is the signal applied to gates A and B.

$$\text{Gate A} \quad \overline{\overline{WXG} + \overline{WL}} = WXG \cdot WL = x$$

$$\text{Gate B} \quad \overline{\overline{WYG} + \overline{WL}} = WYG \cdot WL = y$$

Signal x represents both a data ONE and a logical ONE for information x at the time of control signal WXG. Signal y represent both a data ONE and a logical ONE for information y at the time of control signal WYG.

$$\text{Gate C} \quad \overline{x + x} = \overline{x} \cdot \overline{x} = \overline{x} \qquad \text{for period } \overline{WXG}$$

$$\text{Gate E} \quad \overline{y + y} = \overline{y} \cdot \overline{y} = \overline{y} \qquad \text{for period } \overline{WYG}$$

The first x and the first y represent the outputs of gates A and B; the second x and y represent the outputs of gates D and F.

$$\text{Gate D} \quad \overline{\overline{CUG} + \overline{x}} = \overline{CUG} \cdot x = x \qquad \text{for period } \overline{CUG}$$

$$\text{Gate F} \quad \overline{\overline{CUG} + \overline{y}} = \overline{CUG} \cdot y = y \qquad \text{for period } \overline{CUG}$$

Signals $\overline{x}$ and $\overline{y}$ are the outputs of gates A and F. Summarizing the following equations can be written for period $\overline{CUG} \cdot \overline{WXG} \cdot \overline{WXY}$

Gate C output is $\overline{x}$

Gate D output is x

Gate E output is $\overline{y}$

Gate F output is y

With these outputs the conditions of the remaining gates can be derived for periods $\overline{CUG} \cdot \overline{WXG} \cdot \overline{WYG}$

Gate G $\overline{x + y} = \overline{x} \cdot \overline{y}$

Gate H $\overline{\overline{x} + \overline{y}} = x \cdot y$

Gate L $\overline{c_i} = c_i$

where $\overline{c_i}$ is the input which normally is connected to the next lower bit position (e.g. $\overline{CRY01}$)

Gate J $\overline{\overline{c_i} + \overline{x} \cdot \overline{y} + x \cdot y} = c_i (x + y) \cdot (\overline{x} + \overline{y}) = c_i (\overline{xy} + \overline{xy})$

Gate K $\overline{x} \cdot \overline{y} + x \cdot y = (x + y) \cdot (\overline{x} + \overline{y}) = \overline{xy} + \overline{xy}$

Gate N $\overline{c_i (\overline{xy} + \overline{xy}) + x \cdot y} = [\overline{c_i} + (x + \overline{y}) (\overline{x} + y)] \cdot (\overline{x} + \overline{y})$

$= \overline{c_i} (\overline{x} + \overline{y}) + \overline{xy} = \overline{c_o}$

Gate M $c_i + \overline{xy} + x\overline{y} = \overline{c_i} (x + \overline{y}) (\overline{x} + y) = c_i (\overline{xy} + xy)$

Gate P $\overline{\overline{c_i} (\overline{xy} + xy) + c_i (\overline{x}y + x\overline{y}) + \overline{RUG}}$

$= [c_i + (x + Y) (\overline{x} + \overline{Y})] [(\overline{c_i} + (x + \overline{y}) (\overline{x} + \overline{y})] \, RUG$

$= [(x\overline{y} + \overline{x}y) \overline{c_i} + (\overline{xy}) c_i] \, RUG.$

At the time of signal RUG the content of gate P is read into the write amplifier of the same stick. Note that the term within the brackets is identical with the sum u of equation (1) paragraph 3-24. The complemented carry-out ($\overline{c_o}$) is provided by gate N. Its agreement with equation (2) is proven by recomplementing the expression as follows:

$$c_o = \overline{c}, (\overline{x} + \overline{y}) + \overline{xy} = [c_i + (x \cdot y)] (x + y) = x \cdot y + (x + y) c_i$$

3-26. The normal and forced carries into the Adder are illustrated in figure 3-9. Address location 56 enables gate A, and address 41 enables gate B. If either of these addresses is present, a logical ZERO output results from gate B. This output, coincident with $\overline{\text{SHINC}}$ (indicates presence of a SHINC or SHANC instruction), results in a logical ONE output from gate D which inhibits the normal carry ($\overline{\text{CRY16}}$) function into the first bit position of the adder. Thus end around carry is prevented. An explanation of instruction SHINC is contained in paragraph 2-111. The forced carry input is accomplished through flip-flop G-H. Control pulse C1 is generated by the Sequence Generator during certain instructions, and adds the quantity one to the information in the adder.

3-27. The sign of a sum has to be reversed when angular data is added and if overflow or underflow occurs (paragraph 1-41). Instead of reversing a sign, the AGC feeds the overflow bit (opposite to the sign bit) instead of the sign bit, into Write Amplifier 16. This switching is accomplished as shown in figure 3-10. Gates F and G are enabled when address locations 41, or 47 through 56 are active. Signals URL15 and URL16 represent the outputs of the 15th and 16th bit positions respectively of the Adder. A ONE in bit position 15 coincident with one of the above addresses during the adder read signal ($\overline{\text{RUG}}$) results in output UNL16 as a ONE to WA16. A ONE in bit position 16 of the adder output (in the absence of one of the above addresses) is applied directly to gate J.

3-28. The signal $\overline{\text{RUAC}}$ (read U end around carry) is generated coincident with $\overline{\text{RUG}}$, except when locations 41 or 47 through 56 are addressed, and is applied to stick 16 causing URL16 to be generated. This latter signal is applied to gate J and appears at the output of gate L. Thus, either URL15 or URL16 is generated at the output of gate L.

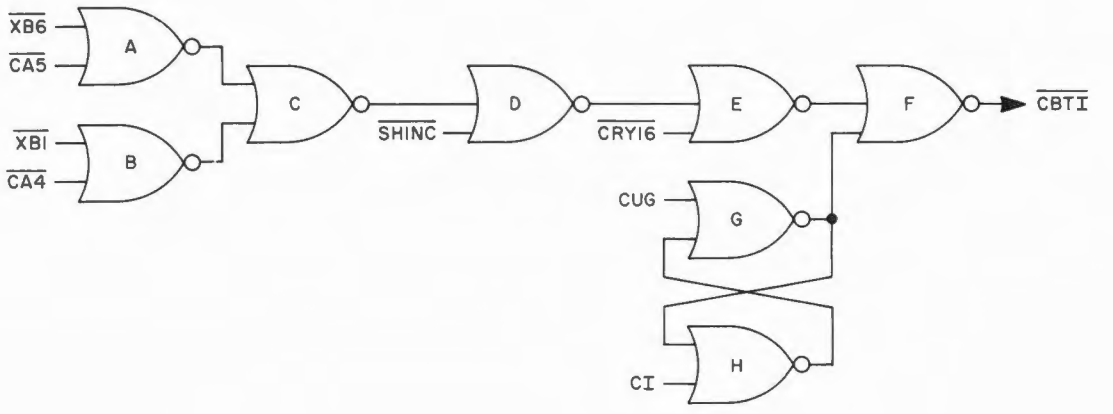

Figure 3-9. Adder End Around Carry

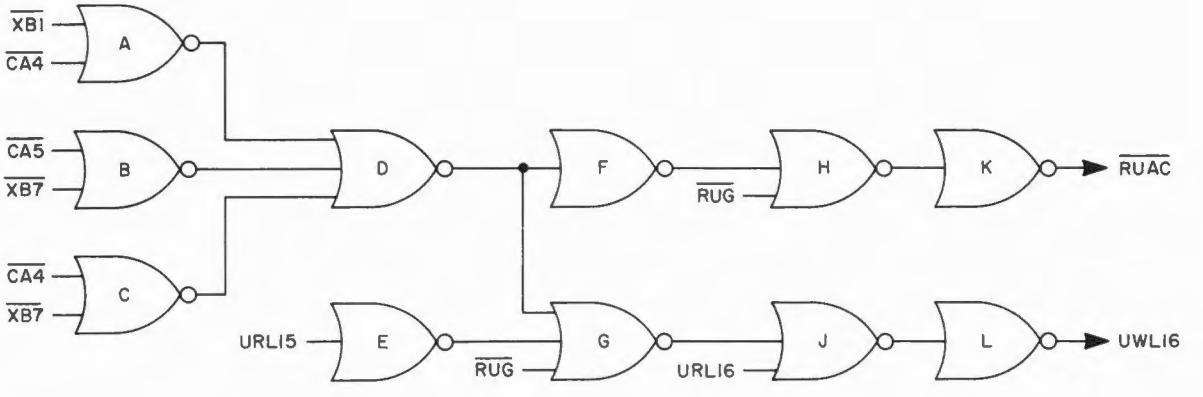

Figure 3-10. Sign Bit Switching

3-29. BANK REGISTER

3-30. The bank register (BNK) is used to select one of the twenty-two banks in fixed memory (each bank consisting of 1024 memory locations). The real and the corresponding pseudo address of each bank are defined in table 1-4. Register BNK has five bit positions, each consisting of a flip-flop, a write gate and an output gate, and is similar in its arrangement to other flip-flop registers. The generation of control signals $\overline{\text{WBKG}}$, CBKG, and $\overline{\text{RBKG}}$ is listed in table 3-1. Register BNK has an address of 15 and is enabled for readout, clear, and write-in by signals $\overline{\text{XT1}}$ and $\overline{\text{XB5}}$ applied to the BNK service gates. Table 3-5 below lists the various inputs generating an output from each bit position of the BNK register.

TABLE 3-5.

BNK REGISTER OUTPUTS

Write Gate Inputs	Flip-Flop Clear Signals	Read Gate Control Inputs	Read Gate Output Info	Output Gate Outputs
$\overline{\text{WL11}}$, $\overline{\text{WBKG}}$	CBKG	$\overline{\text{RBKG}}$	RWL11	R4 $\overline{\text{R4}}$
$\overline{\text{WL12}}$, $\overline{\text{WBKG}}$	CBKG	$\overline{\text{RBKG}}$	RWL12	R3 $\overline{\text{R3}}$
$\overline{\text{WL13}}$, WBKG	CBKG	$\overline{\text{RBKG}}$	RWL13	R2 $\overline{\text{R2}}$
$\overline{\text{WL14}}$, WBKG	CBKG	$\overline{\text{RBKG}}$	RWL14	R1 $\overline{\text{R1}}$
$\overline{\text{WL16}}$, WBKG	CBKG	$\overline{\text{RBKG}}$	RWL16	R0 $\overline{\text{R0}}$

3-31. Data is stored in the five flip-flops of register BNK and information is available at the output gates. Signals R0 through R4 and their complements are fed to the bank selector section along with certain signals generated for memory addressing. If bits 11 and 12 of the S register are both ONEs (table 1-4), one of six rope gates (RPG1-RPG6) will be selected dependent upon the content of the bank register.

3-32. PARITY BLOCK

3-33. The parity circuits (figure 3-11) assure that the words stored in erasable and fixed memory locations above address 0030 are read out correctly. Detected parity errors cause a parity alarm (PAL).

3-34. There are six flip-flops in the bit storage section in figure 3-11 that store information corresponding to the combinations of signals ($\overline{WL01}$-$\overline{WL16}$) applied to the input gates. The six flip-flop outputs labeled A through E are consequently functions of the inputs from the write lines as expressed by the Boolean equations below.

$$A = WL1WL2WL3 + WL1\,\overline{WL2WL3} + \overline{WL1}WL2\overline{WL3} + \overline{WL1WL2}WL3$$

$$B = WL4WL5WL6 + WL4\overline{WL5WL6} + \overline{WL4}WL5\overline{WL6} + \overline{WL4WL5}WL6$$

$$C = WL7WL8WL9 + WL7\overline{WL8WL9} + \overline{WL7}WL8\overline{WL9} + \overline{WL7WL8}WL9$$

$$D = WL10WL11WL12 + WL10\overline{WL11WL12} + \overline{WL10}WL11\overline{WL12} + \overline{WL10WL11}WL12$$

$$E = WL13WL14WL16 + WL13\overline{WL14WL16} + \overline{WL13}WL14\overline{WL16} + \overline{WL13WL14}WL16$$

$$F = \overline{PARBUS}$$

Output F is the parity bit of a word as received from the parity bus (bit position 0 of register G).

3-35. The flip-flop outputs are applied to the parity tree which consists of gates A through P in figure 3-11. The parity tree generates an output from

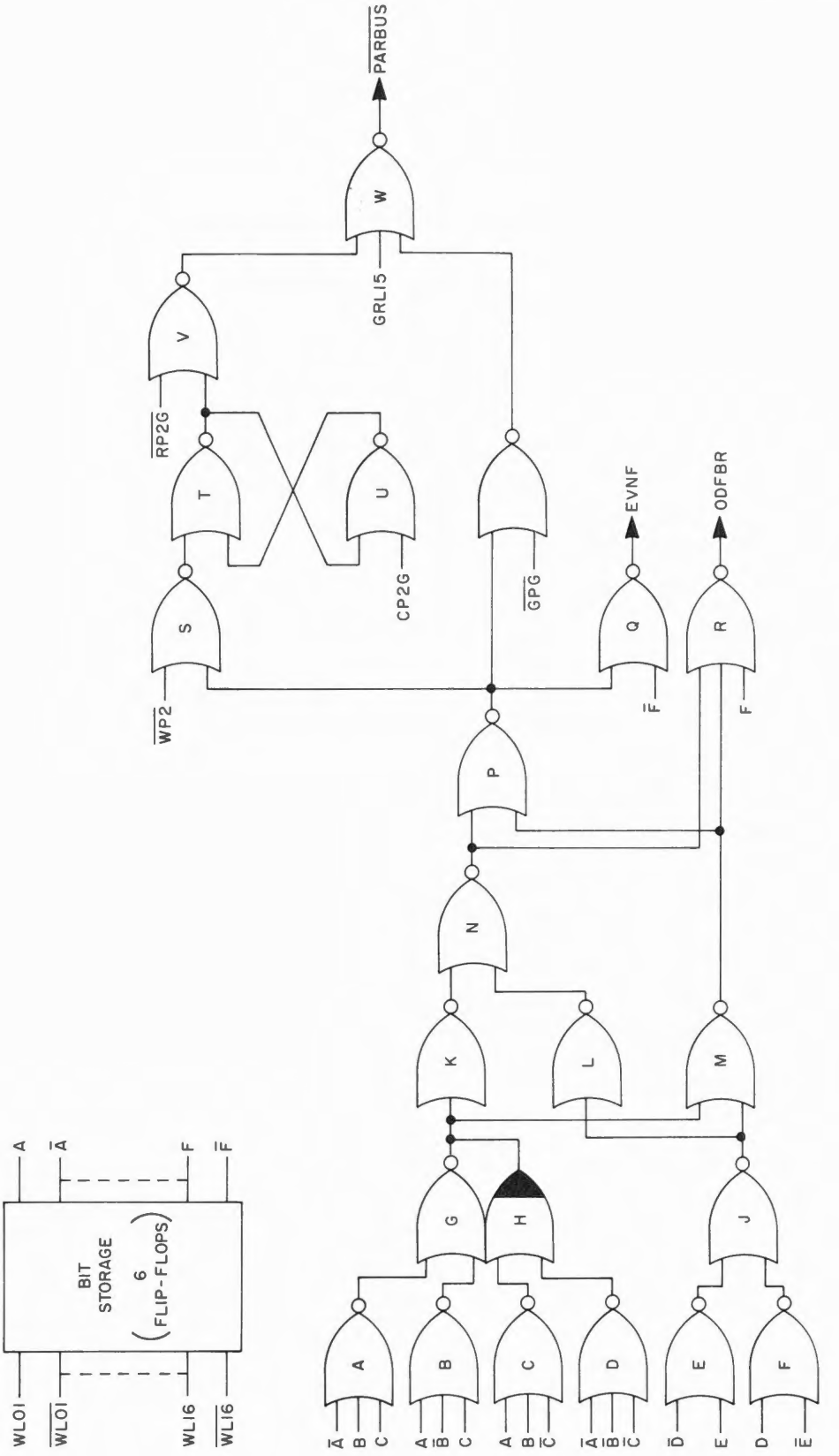

Figure 3-11. Parity Block

gate P as a function of the flip-flop outputs A through E (table 3-6). If the number of ONEs in a word is even (parity bit excluded), the output of the parity tree is a logical ZERO. If the number of ONEs in a word is odd, the parity tree output is a logical ONE. As a Boolean function this is expressed as:

$$F = [(\overline{A}\overline{B}\overline{C} + (\overline{A}BC) + A\overline{B}C) + (AB\overline{C})][(\overline{D}\overline{E}) + (D\overline{E})] + [(\overline{A}\overline{B}C) + (\overline{A}BC) + (A\overline{B}C) + (ABC)][(DE) + (\overline{D}E)]$$

The output of the parity tree is written into the P2 register (flip-flop T-U) coincident with write signal $\overline{WP2}$. The content of this register is read out through gate V at the time of read signal $\overline{RP2G}$.

3-36. An output from the P2 register, or signal GRL15, or an output from the parity tree coincident with $\overline{GPG}$ causes the signal $\overline{PARBUS}$ (gate W) to be generated. This signal in turn is applied to bit stick 15 and causes a ONE to be written into bit position 0 (bit stick 15) of register G whenever a parity bit is applicable.

3-37. Gates Q and R compare the output of the parity flip-flop F with the output of the parity tree. One of these gates generates an output indicating an even (EVNF), the other an odd (ODFBR) number of data ONEs (parity bit excluded) in the word. If the number of ONEs (parity bit excluded) in a word entered into the parity circuits is odd, the parity tree output is a logical ONE thus inhibiting any output from gate Q. If the number of ONEs is even, gate P generates a logical ZERO thus enabling gate Q. If the parity bit of the same word is a data ONE (signal $\overline{PARBUS}$), the output F is a logical ONE, and signal $\overline{F}$ a logical ZERO. If the parity bit is a logical ZERO, F is a logical ZERO and $\overline{F}$ a logical ONE. A logical ONE is generated by gate Q only if the output of gate P and signal $\overline{F}$ are both logical ZEROs, that is, if the number of ONEs (parity bit excluded) is even and if a parity bit does exist. Both inputs to gate P are logical ZEROs if the number of ONEs (parity bit excluded) is odd. A logical ONE is generated by

gate R only if the two inputs to gate P and signal F are logical ZEROs, that is, if the number of ONEs is odd and if there is no parity bit. For other conditions, gates Q and R generate logical ZEROs as shown in table 3-7. The incorrect conditions can be detected by examining signals EVNF and ODFBR.

TABLE 3-6

PARITY TREE OUTPUT VALUES AS A FUNCTION OF A, B, C, D, AND E

A	B	C	D	E	PARITY TREE OUTPUT
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0

TABLE 3-7

GENERATION OF PARITY BIT

Number Of ONEs In Word (Parity Bit Excluded)	Output Of Gate P	Parity Bit In Word	Output F	Output $\overline{F}$	Output EVNF	Output ODFBR
Even	ZERO	ONE	ONE	ZERO	ONE	ZERO
Uneven	ONE	ZERO	ZERO	ONE	ZERO	ONE
Even	ZERO	ZERO	ZERO	ONE	ZERO	ZERO
Uneven	ONE	ONE	ONE	ZERO	ZERO	ZERO