APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 8A

PRIORITY CONTROL

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CONTENTS

ILLUSTRATIONS

8-1. INTRODUCTION

8-2. This is the eighth issue of the AGCIS, which is published to inform the technical staff of MIT/IL and Raytheon about the Apollo guidance computer (AGC) subsystem. This issue contains a functional description of the Priority Control of the Block I AGC subsystem which was discussed briefly in paragraphs 15-43 through 15-52 of Issue 15. Information pertaining to the Priority Control was taken from the following NASA drawings generated by MIT/IL:

1006544
1006546
1006548
1006550
1006558

Information was also obtained from the AGC-4 Interconnection Wirelist, NASA drawing 1006601 (revision F), produced by MIT/IL.

8-3. The Priority Control consists of the Counter Priority Control and the Interrupt Priority Control. The Counter Priority Control updates counters in Erasable Memory (locations 0034 through 0057, tables 15-5 and 15-8) and implements the display and load instruction requests provided by the Computer Test Set. The Interrupt Priority Control transfers program control from a current program section to another program section via a RPT transfer routine (table 15-7) when the proper interrupt request is present.

8-4. COUNTER PRIORITY CONTROL

8-5. The AGC counters are registers in Erasable Memory and are updated when the Counter Priority Control receives an incremental pulse for them. Only one counter can be updated at a time. However, the Counter Priority Control will accept incremental pulses for several counters simultaneously. When incremental pulses for more than one counter are received, the counters are updated in the sequence listed in table 15-5. The counter at location 0034 is always updated first and the counter at location 0057 is always updated last. The Counter Priority Control differentiates between incremental pulses pertaining to increment (PINC), decrement (MINC), shift (SHINC), and shift-and-add-one (SHANC). When an incremental pulse is received, the Counter Priority Control produces the address of the counter to be updated and commands the Sequence Generator to execute the proper counter instruction (PINC, MINC, SHINC, or SHANC). Refer to paragraphs 2-105 through 2-117).

8-6. The Computer Test Set produces display and load instruction requests which, when received by the Counter Priority Control, cause it to command the Sequence Generator to execute instruction OINC or LINC. Instruction OINC (paragraph 2-125) is used to display the content of an addressed location; instruction LINC (paragraph 2-127) is used to enter data into an addressed location.

8-7. INCREMENTING ONLY

8-8. The time counters (locations 0035 through 0040) and the rate counters (locations 0042, 0043, and 0057) can be incremented only. The TIME 2 and TIME 1 counters (table 15-5) comprise the main time counter. The main time counter is incremented at the rate of 100 pps and monitors real time. The TIME 1 counter which has a capacity of 163.8 sec is incremented ever 10 msec. Every 163.8 sec the TIME 1 counter overflows producing signal $\overline{\text{OVF}}$ (figure 5-3). The overflow test gate (figure 8-1) senses the overflow when control pulse $\overline{\text{WOVR}}$ is present. The output of the overflow test gate is sent to the TIME 2 CTR gate and to the TIME 3 and TIME 4 gates in the Interrupt Priority Control. The TIME 2 CTR gate produces an output which increments the TIME 2 counter once every 163.8 sec.

8-9. The TIME 3 and TIME 4 counters are general purpose timers which transfer program control to RPT Transfer Routines TIME3RUPT and TIME4RUPT respectively. The counters are initially set to a predetermined value by program action, then incremented at 100 pps until overflow occurs. Control is then transferred to routine T3RUPT or T4RUPT respectively.

8-10. Rate counters OUTCR1, OUTCR2, and OUTCR3 control the number of drive pulses sent to the IMU gyros, IMU CDU's, Optics CDU's, and TRKR. A rate counter is initially set to a predetermined value by program, then incremented until overflow occurs. The incremental pulses sent to the Counter Priority Control and the drive pulses sent to the IMU gyros, IMU CDU's, Optics CDU's, and TRKR are controlled by the content of register OUT2. When a rate counter overflows, those bit positions of register OUT 2 concerned with the rate counter (paragraphs 15-57 through 15-59) are cleared and the incremental pulses and drive pulses are gated off. The incremental pulses have a frequency of 3200 pps.

8-11. INCREMENTING AND DECREMENTING

8-12. The overflow counter at location 0034 and the input counters at locations 0044 through 0055 can be incremented or decremented. The overflow counter is used during the execution of instructions AD K and SU K. When the accumulator overflows or underflows the Sequence Generator produces signal $\overline{\text{OVF}}$ or $\overline{\text{UNF}}$ respectively (figure 5-3). This overflow or underflow is sensed by the respective detection gate in the Counter Priority Control (figure 8-1) when control pulse $\overline{\text{WOVC}}$ is present. The overflow counter is incremented or decremented by the outputs of the overflow test gate and underflow test gate respectively.

8-13. The input counters monitor data supplied by the PIPA's, IMU CDU's Optics CDU's, and TRKR. These units send incremental pulses to the Counter Priority Control and may increment or decrement the input counters depending on the direction of motion of the units. Incrementing and decrementing signals are sent to the AGC on separate lines.

8-14. SERIAL-TO-PARALLEL CONVERSION

8-15. The UPLINK counter at location 0041 and the TRKR counter at location 0056 are used for serial-to-parallel conversion of binary data. A serial word is converted to a parallel word as described in table 15-5. Incremental pulses indicating either logical ZERO's or

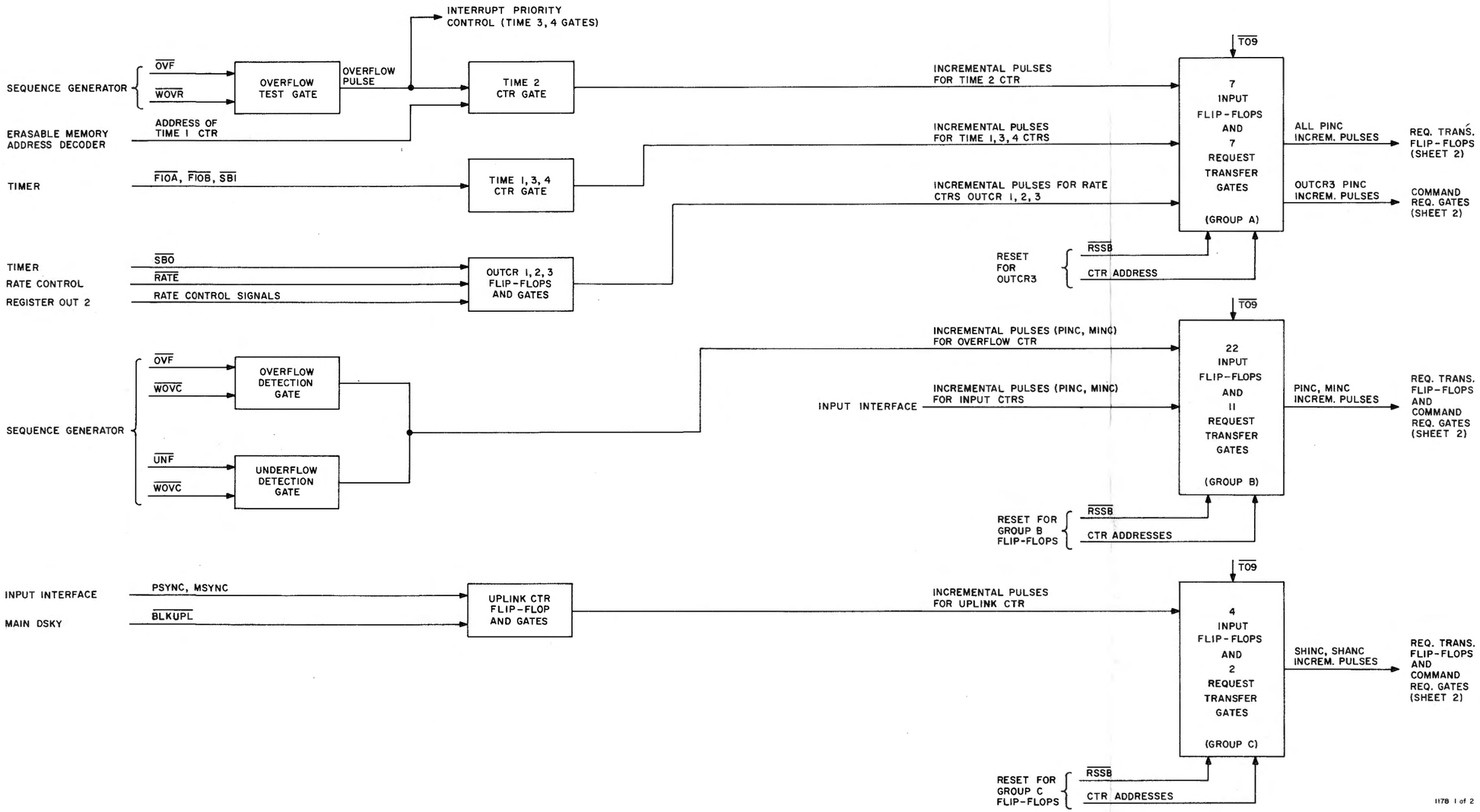

Figure 8-1 Counter Priority Control (Sheet 1 of 2)

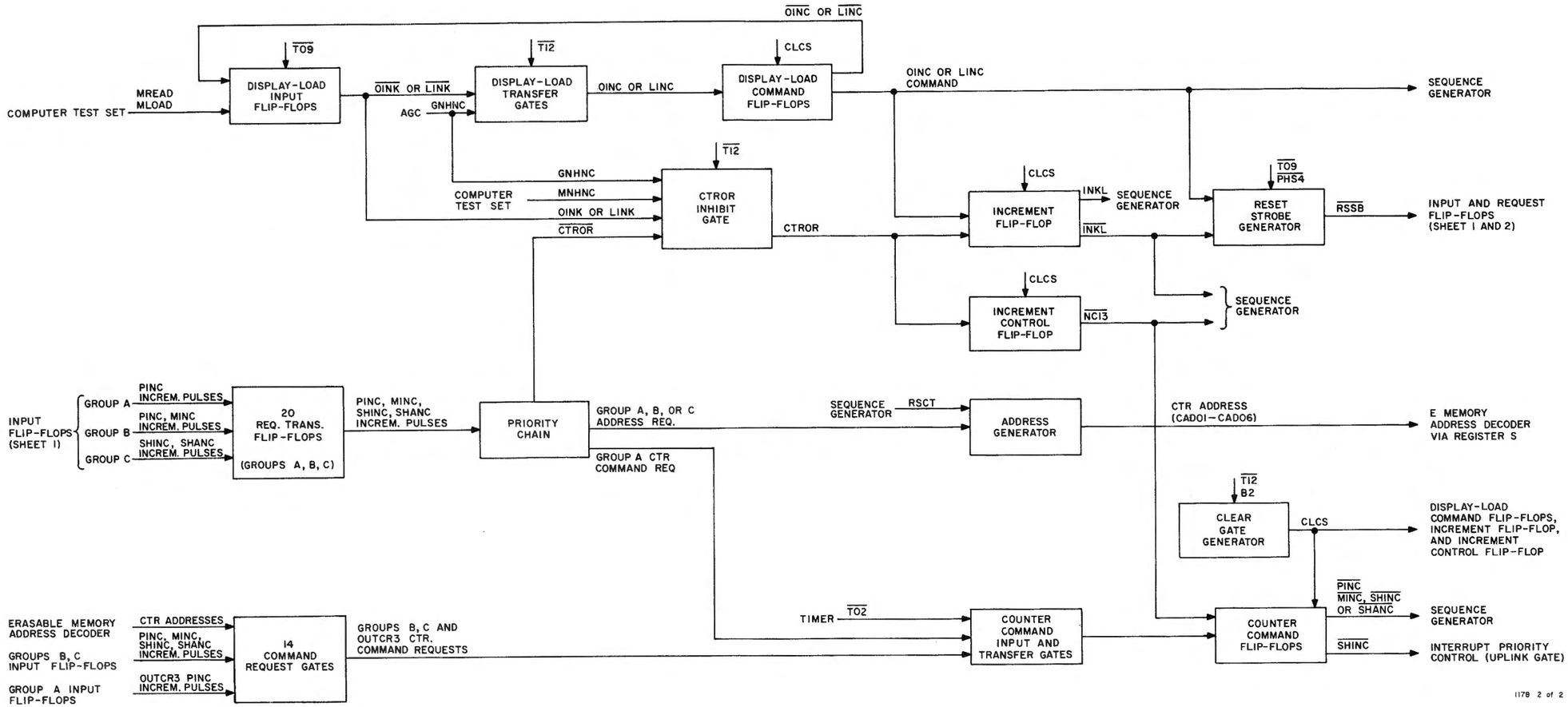

Figure 8-1 Counter Priority Control
(Sheet 2 of 2)

logical ONE's are sent to the Counter Priority Control (figure 8-1) on separate lines to cause either a shift or a shift-and-add-one operation.

8-16. COUNTER ADDRESSING

8-17. Signals for updating the 20 counters are sent to the input flip-flops (figure 8-1). There are three distinct groups of input flip-flops: group A which are associated with the counters to be incremented only; group B which are associated with the counters to be incremented or decremented; and group C which are associated with the counters used for serial-to-parallel conversion. There is one input flip-flop for each incremental input to the Counter Priority Control. Group A contains seven input flip-flops; group B contains 22; and group C contains four. Groups B and C input flip-flops provide two outputs to differentiate between increment and decrement, or shift and shift-and-add-one pulses.

8-18. When an input flip-flop is set, its output conditions a request transfer gate. A request transfer gate is enabled at Time 9 and a request transfer flip-flop is set. The outputs of the request transfer flip-flops feed the priority chain. This priority chain allows the counters to be updated one at a time in a predetermined sequence. Counter requests inhibiting lower priority flip-flops are released later when the address of the updated counter is produced. The output of the priority chain is sent to the address generator to produce the address of the counter to be incremented. Signal $\overline{\text{CTROR}}$ is required to continue this data transfer.

8-19. The priority chain produces signal $\overline{\text{CTROR}}$ when any of the request flip-flops are set. This signal is sent to the increment control flip-flop via the CTROR inhibit gate. The flip-flop generates signal $\overline{\text{NC13}}$ to notify the Sequence Generator an incremental counter input is waiting to be processed. If Computer Test Set (CTS) signals OINK, LINK, and MNHNC are not present, signal $\overline{\text{CTROR}}$ is inverted and transferred at Time 12 to the increment flip-flop and the increment control flip-flop.

8-20. The increment flip-flop sets and produces signals INKL and $\overline{\text{INKL}}$. Both signals are sent to the Sequence Generator to inhibit the execution of the next subinstruction. In addition, signal $\overline{\text{INKL}}$ conditions the reset strobe generator such that signal $\overline{\text{RSSB}}$ is produced every Time 2 when a CTR request is present. The reset strobe generator is conditioned by timing signal $\overline{\text{T09}}$ and strobe signal $\overline{\text{PHS4}}$. Signal $\overline{\text{RSSB}}$ is used in conjunction with the addresses produced by the address decoder to reset the input flip-flops and request transfer flip-flops.

8-21. The increment control flip-flop sets and produces signal $\overline{NC13}$. Signal $\overline{NC13}$ is sent to the Sequence Generator where it produces control pulse RSCT at Time 1. Signal RSCT enters the counter address into register S thereby selecting a counter for incrementing. The counter address is then sent to the address decoder in E memory. Signal $\overline{NC13}$ is also sent to the counter command flip-flops as an enabling pulse.

8-22. PRODUCING PINC, MINC, SHINC, and SHANC COMMANDS

8-23. The outputs from group A request transfer flip-flops, except those associated with OUTCR3, are sent via the priority chain to the command transfer gates to execute signal PINC. Groups B and C counter command outputs, however, must be conditioned by their respective counter addresses so the Sequence Generator will receive only the proper incremental command (PINC, MINC, SHINC, or SHANC). Each priority channel in groups B and C contains a command request gate. This request gate is enabled by the incremental input pulse and the address of the counter to be updated. A command request gate is also provided for the OUTCR3 input flip-flop in group A. This gate must be conditioned by its counter address. Thus the OUTCR3 input flip-flop functions as a group B or C flip-flop (figure 8-1).

8-24. The command transfer gates, which are conditioned by signal $\overline{NC13}$ and enabled at Time 2, provide signals PINC, MINC, and SHINC to the command flip-flops when these counter instructions are to be executed. When instruction SHANC is to be executed, the command transfer gates provide signals SHINC and SHANC to the command flip-flops. (This is done to attain maximum use of Sequence Generator circuitry.) The outputs of the command flip-flops are sent to the Sequence Generator to execute the proper counter instruction. While a counter is being incremented, its address is sent to the associated input flip-flop and request flip-flop. At Time 2, the address and signal $\overline{RSSB}$ reset these flip-flops. At Time 12 the clear gate generator, conditioned by strobe signal B2, produces signal CLCS. Signal CLCS clears the counter command flip-flops, the display-load command flip-flops, the increment control flip-flop and the increment flip-flop.

8-25. PROCESSING DISPLAY AND LOAD REQUESTS

8-26. The Computer Test Set provides the Counter Priority Control with signals MREAD and MLOAD which are the requests for display and load instructions, respectively. When either request is present, the proper display-load input flip-flop (figure 8-1) sets and supplies signal $\overline{OINK}$ or $\overline{LINK}$ to the display-load transfer gates. Signal OINC or LINC from the display-load transfer gates sets the proper display-load command flip-flop at Time 12.

8-27. The output of the display-load command flip-flops (signal OINC or LINC) is sent to the increment flip-flop, reset strobe generator, and the Sequence Generator. The Increment Flip-Flop, when set by signal OINC or LINC, produces signals INKL and $\overline{\text{INKL}}$. Signals INKL and $\overline{\text{INKL}}$ are sent to the Sequence Generator to inhibit the execution of the next sub-instruction. The reset strobe generator is inhibited by signal OINC or LINC. Signals OINC and LINC, sent to the Sequence Generator, execute the display or load instruction. At the following Time 12, signal CLCS from the clear gate generator clears the display-load command flip-flops, the increment flip-flop, and the increment control flip-flop. At Time 9 signal $\overline{\text{OINC}}$ or $\overline{\text{LINC}}$ from the display-load command flip-flops clears the proper display-load input flip-flop.

8-28. Signal OINK, LINK, or MNHNC inhibit incremental counter instructions at the CTROR inhibit gate (figure 8-1). Signal MNHNC is generated by a manual increment inhibit switch on the CTS. Alarm signal GNHNC from the AGC will inhibit the display-load transfer gates and the CTROR inhibit gate (figure 8-1) whenever an alarm signal is received from the AGC.

8-29. INTERRUPT PRIORITY CONTROL

8-30. When a program interrupt request is present, the Interrupt Priority Control (figure 8-2) produces the address of the appropriate RPT Transfer Routine and commands the Sequence Generator to execute instruction RPT. Locations 2000, 2004, 2010, 2014, 2020, and 2024 in Fixed Memory store the first instructions, respectively, of RPT Transfer Routines TIME3RPT, ERRORRPT, TIME4RPT, KEYMARPT, UPLINRPT, and DOWNLRPT (paragraph 2-96). When several program interrupt requests are present, the Interrupt Priority Control processes them individually in the order listed above.

8-31. PRODUCING INTERRUPT REQUESTS

8-32. Request signal RP1 (for TIME3RPT) is generated by the TIME 3 gate. The TIME 3 gate is conditioned by the address of the TIME 3 counter during incrementing and enabled by an overflow pulse from the Counter Priority Control when this counter overflows.

8-33. Request signal TRP2 (for ERRORRPT) is generated by the error trap. The error trap is conditioned by signal RUPT TRAP RESET (bit 7 of register OUT1) and enabled by external fail signals supplied to the AGC via the input interface. Signal TRP2 is not generated in the AGC at present because no fail signals are supplied.

8-34. Request signal RP3 (for TIME4RPT) is generated by the TIME 4 gate. The TIME 4 gate is conditioned by the address of the TIME 4 counter during incrementing and enabled by an overflow pulse from the Counter Priority Control when this counter overflows.

8-35. Request signal TRP4 (for KEYMARPT) is generated by the keyboard trap. The keyboard trap is enabled at Time 1 by keycode bits one through five from the DSKY's. Signal TRP4 also clears register IN0 in the Central Processor so that new data may be received.

8-36. Request signal MKTRP (for KEYMARPT) is generated by the mark trap. The mark trap is enabled at Time 1 by signal MARK from the Optics. Signal MKTRP also clears register IN0 in the Central Processor so that new data may be received.

8-37. Request signal RP5 (for UPLINRPT) is generated by the uplink gate at the completion of a serial-to-parallel conversion. Interrupt routine UPLINRPT transfers the contents of the counter at location 0041 or 0056 into storage. During the execution of instruction SHINC or SHANC, signal $\overline{\text{SHINC}}$, produced by the counter command flip-flops in the Counter Priority Control (figure 8-1) conditions the uplink gate. When the flag bit of the parallel word is shifted into bit position 16, signal $\overline{\text{WL16}}$ is produced and sent to the uplink gate. At Time 6 of instruction SHINC or SHANC, signal $\overline{\text{TSGN3}}$ is produced by the Sequence Generator and is sent to the uplink gate to test for the flag bit. At Time $\overline{\text{A2}}$ the uplink gate then produces signal RP5.

8-38. Request signal DKEND (for DOWNLRPT) is generated by the Downlink Converter at the completion of a parallel-to-serial conversion of binary data. Signal DKEND is applied directly to the request flip-flops.

8-39. A trap consists of two flip-flops connected in series which produce a single pulse output of predetermined duration regardless of the duration of the set pulse. Since interrupt request signals must be approximately 0.25 μsec in duration, timing signals are used to condition the trap input. The keyboard trap, for example, is enabled by a keycode bit which has a long duration, although it is conditioned by the 0.25 μsec timing signal $\overline{\text{A2}}$. A trap is reset by a clear pulse in the same manner as a single flip-flop.

8-40. PROCESSING INTERRUPT REQUESTS

8-41. When a request signal (RP1, TRP2, RP3, TRP4, MKTRP, RP5, or DKEND) is present, the associated request flip-flop sets and produces an output signal (R1, R2, R3, R4, R5, or R6 and complements). This output signal is sent to the address generator and priority chain. The priority chain produces signal $\overline{\text{RUPTOR}}$ which is sent to the Sequence Generator to produce instruction RPT. Instruction RPT always initiates a program interrupt and causes the contents of registers B and Z to be transferred to location 0024 and 0025, respectively, in Erasable Memory. The priority chain processes the interrupt requests in a preassigned order starting with TIME3RPT.

8-42. The address generator produces address 2000, 2004, 2010, 2014, 2020, or 2024 depending on the particular interrupt requested. At Time 2 of subinstruction RUPT3, the Sequence Generator produces control pulses RRPA and WZ which enter the interrupt program address into Register Z. This address is also sent to the request flip-flops.

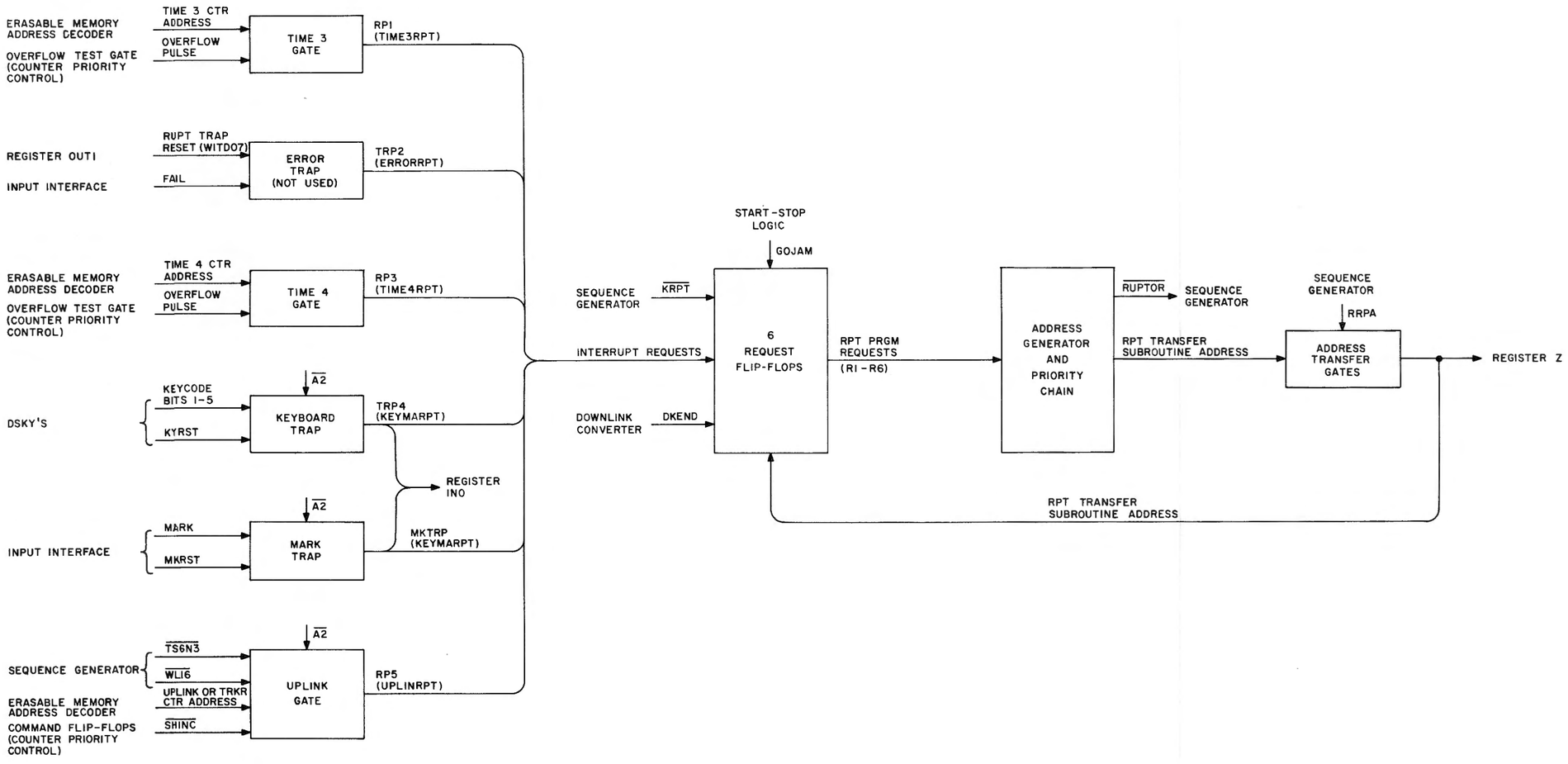

Figure 8-2 Interrupt Priority Control

At Time 3 of subinstruction RUPT3, the Sequence Generator produces control pulses $\overline{\text{KRPT}}$ and RZ. When $\overline{\text{KRPT}}$ occurs at time $\overline{\text{PHS4}}$, the address of the current RPT transfer routine is sensed and the request flip-flop is cleared.

8-43. Signal GOJAM from the Start-Stop Logic (figure 5-1) has priority over all request signals in the Interrupt Priority Control. Signal GOJAM clears all request flip-flops, thereby inhibiting any access to the address generator and priority chain.