

*George Silver*

APOLLO ENGINEERING MEMORANDUM AP-M # 5041

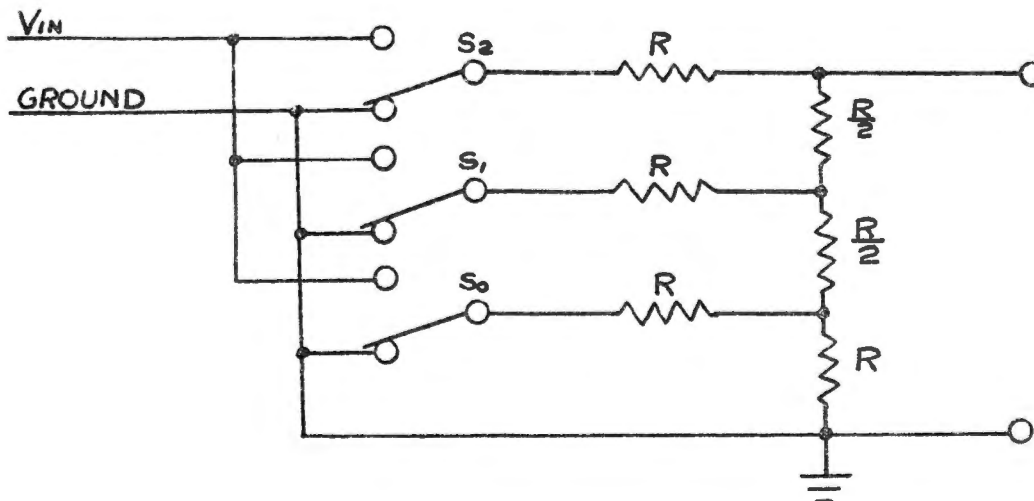
30 November 1964

TO: Distribution  
FROM: Mr. B. Hobbs  
SUBJECT: THE DIGITAL TO ANALOG CONVERTER OF THE ELECTRONIC COUPLING DATA UNIT  
(Paper VII)

This paper is the seventh in a series of papers describing the operation of the electronic CDU. It will present the theory of operation of the digital to analog converter. An hour talk in support of this paper will be given Monday, December 7, 1964 in the SAT conference room.

The conversion of digital information into a dc analog signal by the D/A Converter Module is accomplished in essentially two steps. The digital information is first converted to an 800 cycle analog signal by a voltage ladder decoder. The ac signal is then converted to a dc analog signal by a demodulator that rectifies and filters the ac. In describing the operation of the D/A Converter, the two steps will be described as if they occurred as independent operations. It should be understood, however, that the entire conversion process takes place simultaneously. A functional block diagram of the D/A converter is shown in figure 1.

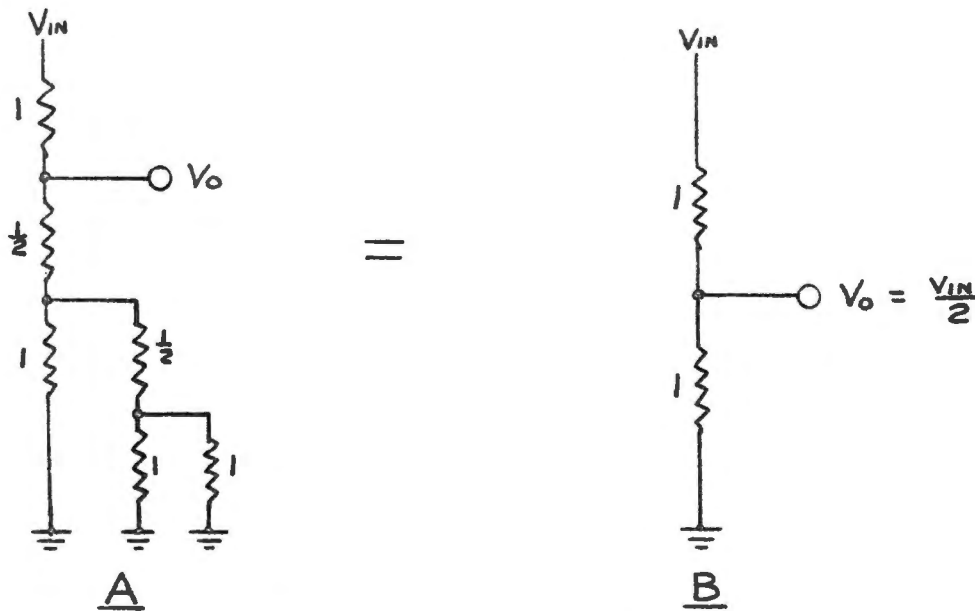
The operation of the voltage ladder decoder will be described first. Accumulated data bits in the error counter of the Error Counter and Logic Module control transistor switches that apply an ac ground or 800 cycles of proper phase to the ladder resistors. A voltage proportional to the binary configuration of the switches is developed and applied to the scaling amplifier. For simplicity, a 3 bit converter will be explained with the understanding that the same theory of operation applies to a converter of any size. The simplified version is shown below.



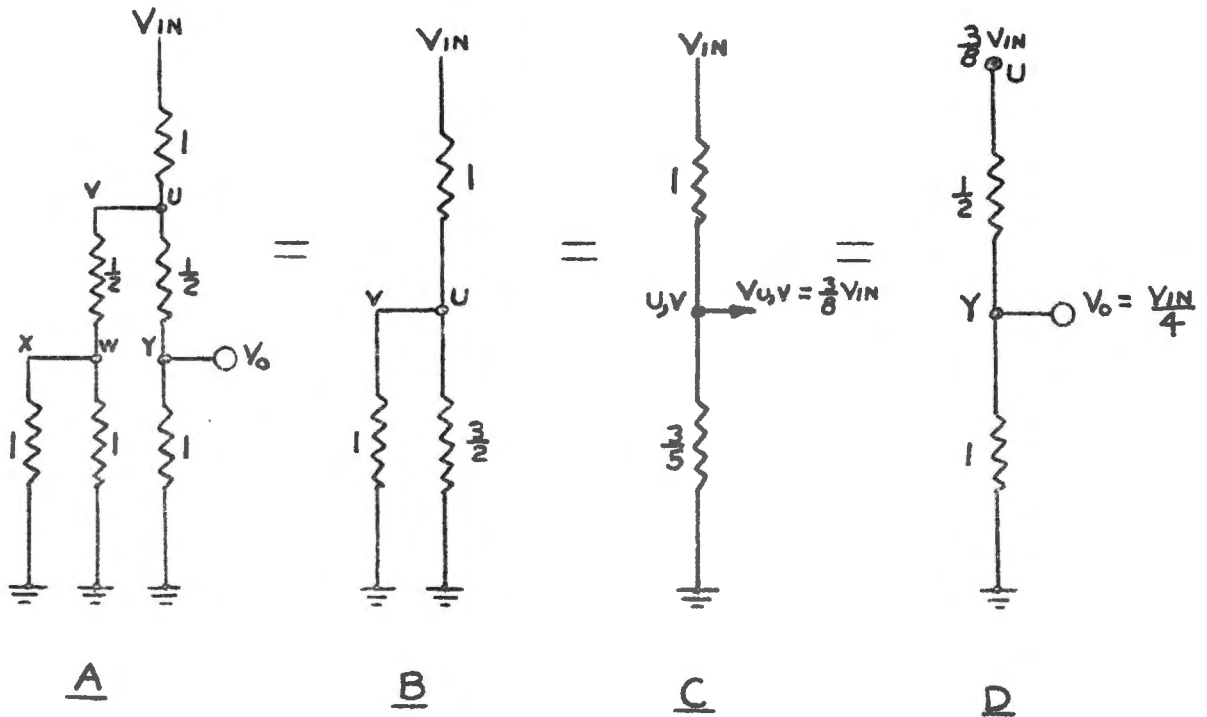
The switches are connected to  $V_{in}$  by a data bit "1" (0 volts) from the error counter located in the Error Counter and Logic Module. The binary weight of each switch is given below.

- $S_2 = 2^2$  Most significant bit
- $S_1 = 2^1$  Second most significant bit
- $S_0 = 2^0$  Least significant bit

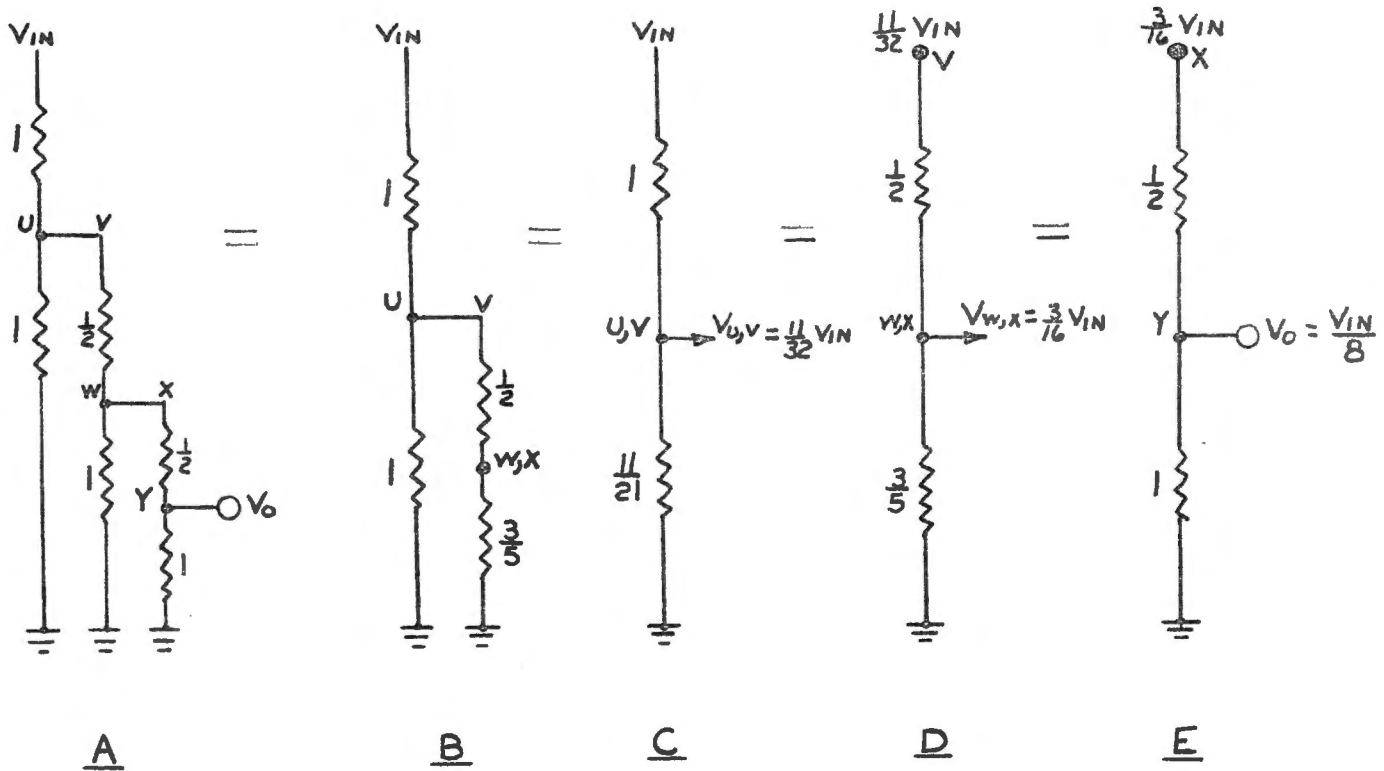
Assume  $S_2$  is activated and applies  $V_{in}$  to the ladder and the remaining switches are left in their normally open position and apply ground. The configuration will be that shown in A below. The solution of the series and parallel resistances show the impedance above and below the output point to be 1, therefore, the voltage is divided by 2 and applied to the scaling amplifier.



With  $S_1$  closed and the remaining switches open, the configuration is as shown in A below. Combining series and parallel resistances produces the equivalent circuit progression A through D. The voltage at point U-V is determined and applied to point U. The simple divider ratio of resistances above and below the output point is used to find the output voltage as shown in the final equivalent circuit D. The output voltage shows that  $V_{in}$  is divided by 4 and applied to the scaling amplifier.



With  $S_0$  closed and the remaining switches open, the configuration is as shown in A below. Combining series and parallel resistances produces the equivalent circuit progression A through E. The voltage at point U-V is found and applied to the divider at point V. In the same manner the voltage at W-X is found and applied to the divider at point X. The output voltage is now found from the divider ratio in the final equivalent circuit E. The output voltage shows that  $V_{in}$  is divided by 8 and applied to the scaling amplifier.



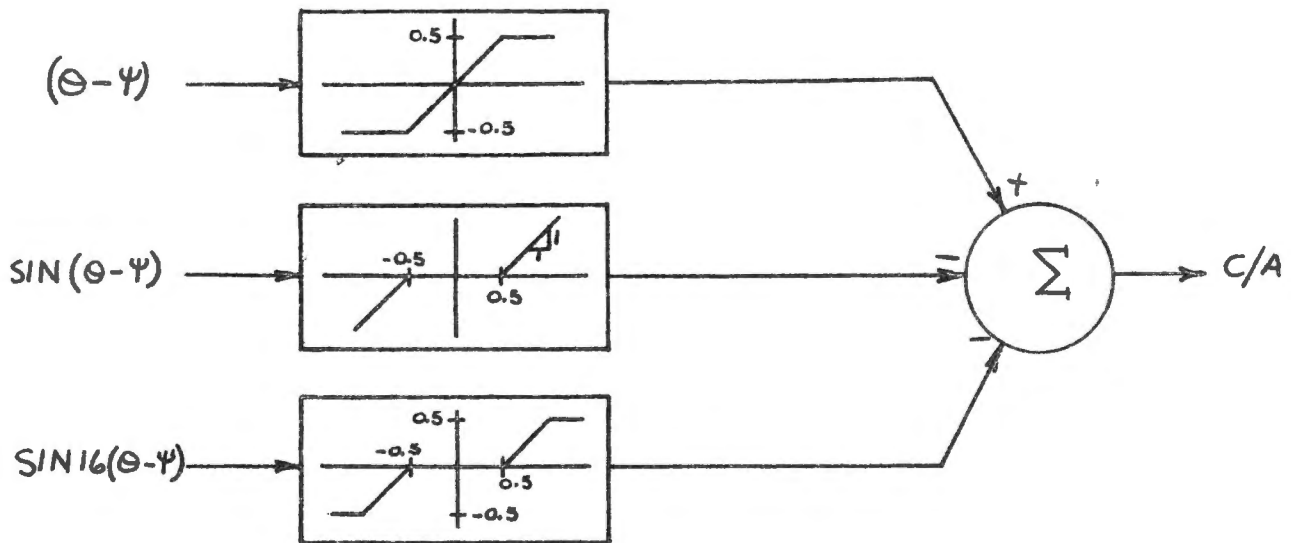
In analyzing the output voltages of the three switch configurations, it is observed that the applied voltage,  $V_{in}$ , is divided by  $2^3$  (8) for the least significant bit,  $2^2$  (4) for the second most significant bit, and  $2^1$  (2) for the most significant bit. The 800 cycles now has an amplitude proportional to the configuration of the data bit controlled switches. A combination of switches activated at the same time will produce an output voltage equal to the sum of the voltages found for each switch individually.

In the actual transistor switching circuit (see figure 3) the data bit inputs to the switches (DD0, DD1, etc.) are normally at a positive voltage, therefore, the switch driver (Q5) is on. This applies ground to the base of the switch (Q6) to keep it turned off. AC ground is applied to the ladder resistor network through Q7. Q7 is forward biased by the 4.7 V zener voltage from CR1 applied to the emitter and by ground applied to the base. If a "1" (0 volts) is applied to DD0, Q5 will turn off and Q6 will turn on applying 2.5 V RMS from T1 to the ladder. The large positive voltage on the base of Q7 will turn it off removing ac ground. The theory of operation is the same for the remaining 8 switches.

The voltage from the ladder is applied to the scaling amplifier and demodulator where the gain is controlled to produce a voltage gradient of 300 m vdc per degree at the output of the D/A converter for use in Attitude Control Mode. In Coarse Align Mode, the ac voltage from the scaling amplifier is applied as an input to the mixing amplifier. (This section of the converter will be explained later in the memo.)

A detailed schematic of the demodulator and scaling amplifier (output stage) is shown in figure 2. Q2 and Q3 along with the feedback network, form an operational amplifier with an ac gain of approximately 3 to 4. The output of the operational amplifier is applied to phase sensitive rectifiers through T1 with a transformation ratio of 1:1.2. The full-wave rectifiers, which consists of both sections of Q4 and Q5, are controlled by an 800 cycle reference signal through T2. If the ladder output is in phase with the reference signal, the proper rectifier switch will be turned on to produce a positive error voltage output. If the ladder output is 180 degrees out of phase with the 800 cycle reference signal, the proper rectifier switch will be turned on to produce a negative error voltage output. The emitter to emitter connection of the transistor sections is to reduce to a minimum the saturation collector to emitter voltage drop. The configuration shown produces voltage drops of opposite polarity at each transistor section, thereby, cancelling the overall drop across the two sections. The rectified ac is filtered by a 2 section RC filter and applied as an error signal to the SCS. The scaling amplifier also provides ac analog voltage to the Flight Director Attitude Indicators (FDIA) and to the mixing amplifier in the Coarse Align Mode. Q1 provides a means of inhibiting the output of the D/A converter even though there is an error accumulation in the error counter. A logic "0" (+ voltage) will inhibit the output of the converter.

In Coarse Align Mode, there is a maximum rate at which the gimbals can move and the read counter continue to track the angle accurately. If the gimbals are limited to a rate less than 71 degrees per second, the read counter will track to within approximately 20 bits of actual gimbal position. A signal out of phase with the ladder voltage and with an amplitude proportional to the difference between the gimbal angle and the angle in the read counter is fed back to rate limit the gimbals. The feedback signals are  $\sin(\theta - \psi)$  from the Coarse System Module and  $\sin 16(\theta - \psi)$  from the Main Summing Amplifier Module. These out of phase signals are summed with the 800 cycle D/A converter signal to produce the input to the mixing amplifier. A block diagram of the mixing circuit and the input diode functions is shown below. The parameters for the diode functions are only approximate.



In the D/A converter presently being proposed for Block II, there will be 9 bits from the Error Counter and Logic Module as inputs. Along with the bits will come + D/A Polarity and - D/A Polarity signals. (See figure 3) These signals will determine if an in-phase or out-of-phase 800 cycle voltage will be applied to the ladder. This in turn will determine if an in-phase out-of-phase signal will be sent to the C/A and FDAI and if a positive or negative dc signal will be sent to the SCS. If a "1" is applied to + D/A Polarity input, Q2 turns off and Q4 turns on applying in-phase voltage to the ladder. If a "1" is applied to - D/A Polarity input, Q1 turns off and Q3 turns on applying out-of-phase voltage to the ladder.

The next paper in this series is entitled, The Digital Logic of the Electronic Coupling Data Unit.

/np

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# D/A CONVERTER MODULE

$K = \text{SCALING CONSTANT FOR DAC}$   
 SENSITIVITY OF 300 MVDC/DEGREE

(SEE FIG 2)

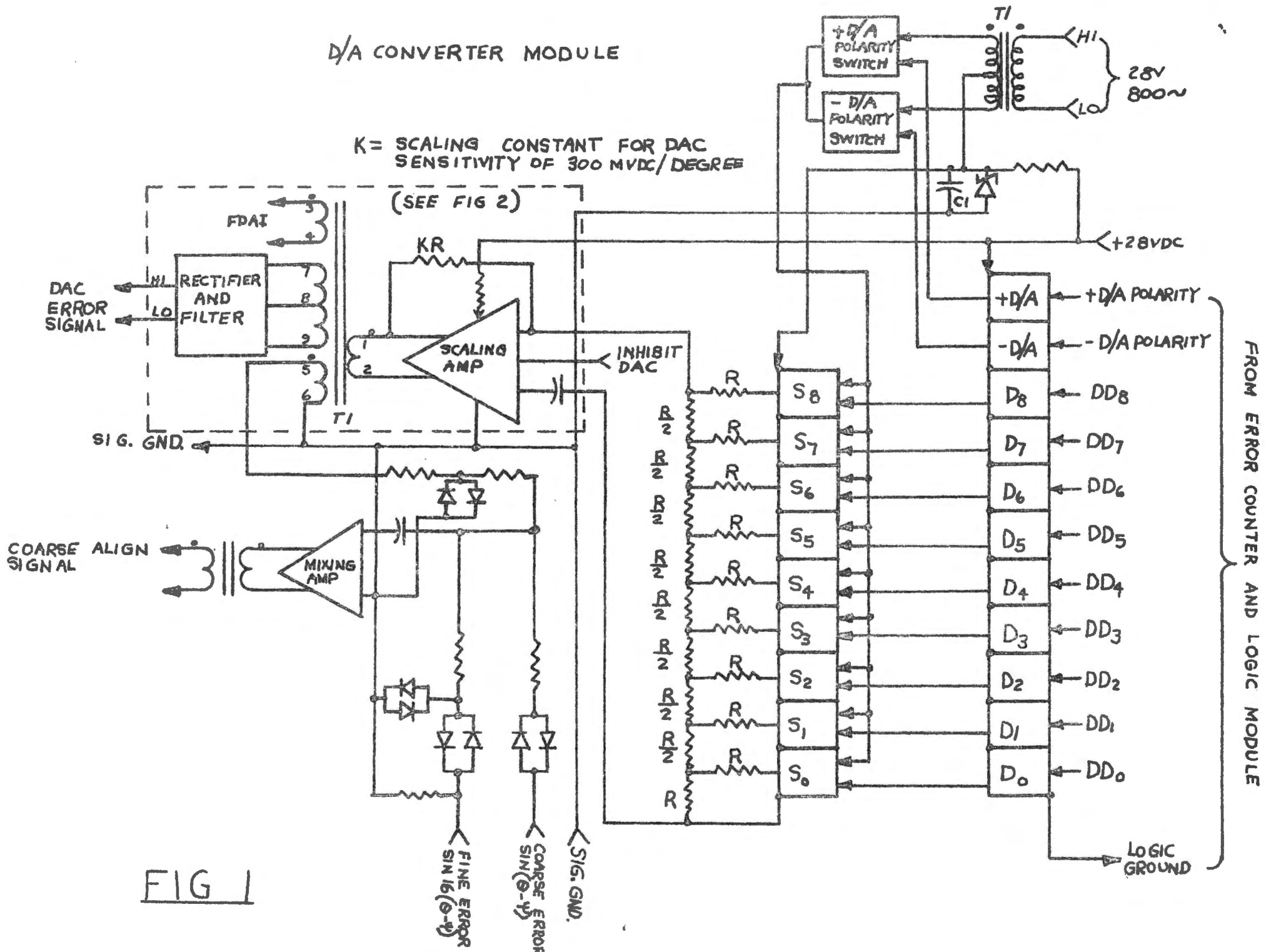
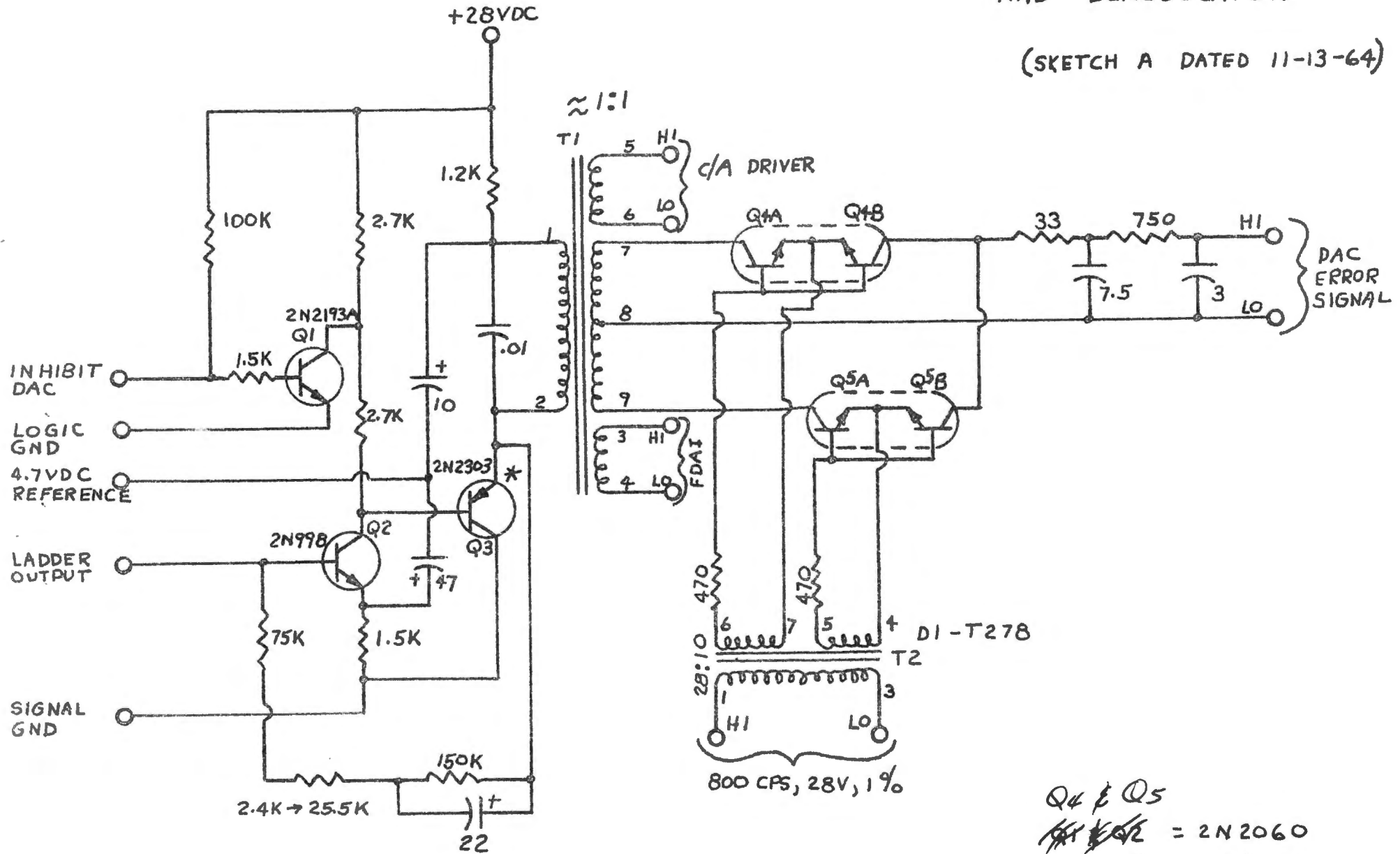


FIG 1

# DAC OUTPUT STAGE AND DEMODULATOR

(SKETCH A DATED 11-13-64)

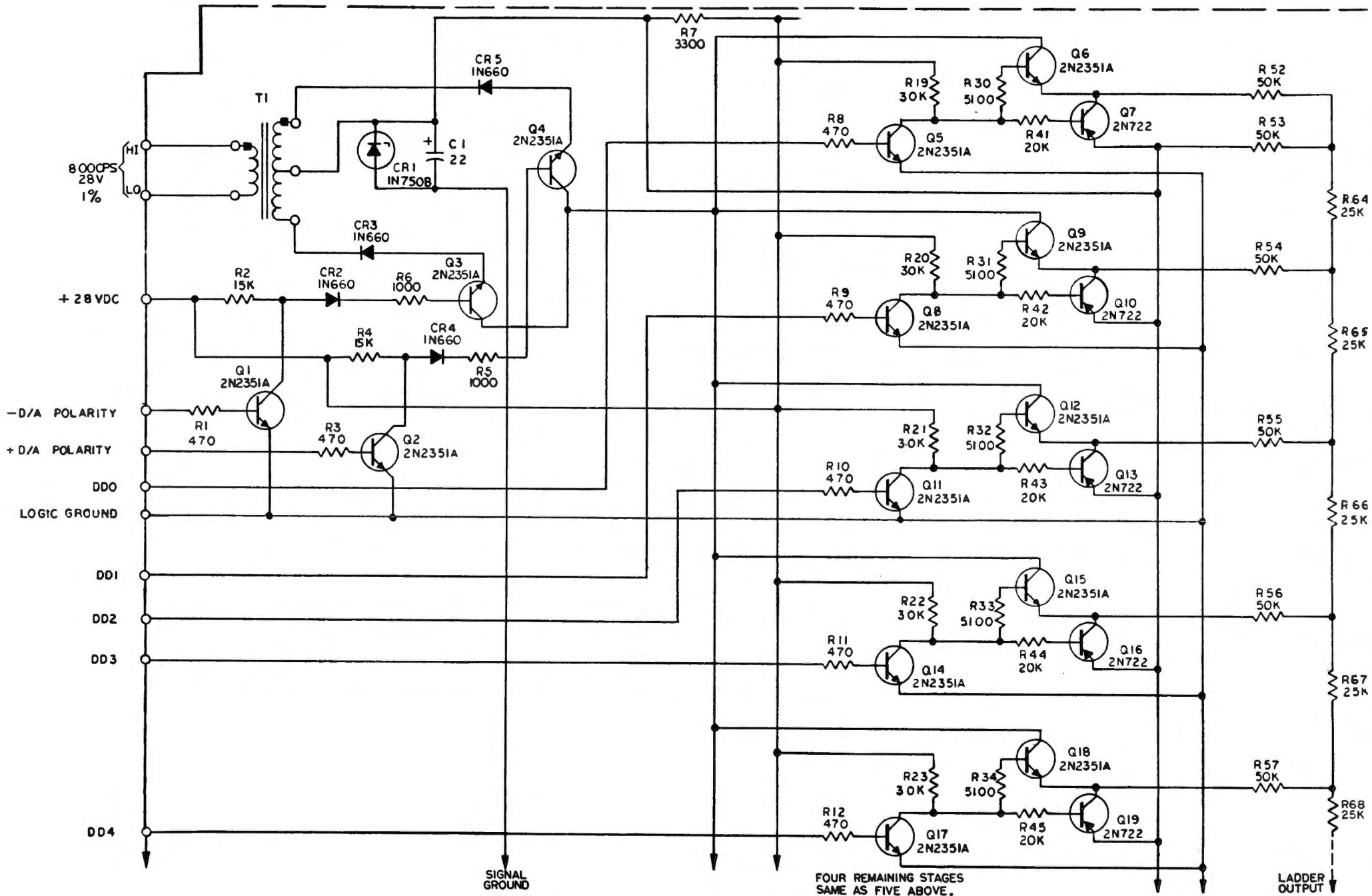


Q4 & Q5  
~~2N2060~~ = 2N2060  
 T1 = BUSH NP505  
 \* = HEAT SINK

FIG 2



FIGURE 3



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