



Apollo

**AUTO-INSTRUCTIONAL PROGRAM
ON
DIGITAL COMPUTER FUNDAMENTALS
FR-3-63**

**TRAINING SECTION
APOLLO FIELD OPERATIONS**

RAYTHEON COMPANY

SPACE AND INFORMATION SYSTEMS DIVISION

RAYTHEON

AN AUTO-INSTRUCTIONAL
TEACHING TEXT
ON
DIGITAL COMPUTER FUNDAMENTALS

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INSTRUCTIONS

The subject of this program is Digital Computer Fundamentals. Knowledge of these fundamentals will provide an understanding of the approach to, and necessity for, the various digital computer techniques and circuits.

The program is presented by auto-instructional techniques called programmed learning. Briefly, these techniques present the information in carefully sequenced small steps called frames. With few exceptions, each step, or frame, requires a written response. However, in order to make a correct response you must pay close attention to the frame content.

The information presented in each frame is placed on the right-hand side of the page. The confirmation of your response is on the left-hand side of the page, next to the succeeding frame.

To prevent your accidentally observing the correct response, we have included a removable page-sized frame cover. This cover is placed on the page under the frame you are studying. After writing in, or "constructing" your response, slide the cover down to the succeeding frame. This will expose the confirmation response to the frame you have just completed.

You will not be able to quickly flip through the pages of the course skipping from "high point to high point" as in an ordinary text. Your complete concentration is required. It is to your advantage to take your time, follow the correct sequence (don't skip around), and carefully think out your response before writing it. When tired, take a break. There is no time limit, you set your own pace.

It is imperative that on those frames requiring written responses you write your response in the area provided for it. A response is required for each blank underlined space. Writing the response is important; it has the effect of making you an active participant in the learning process. You will not be asked to create a response; where required, you will be guided by hints, or cues, within the text, or asked for information previously presented.

After writing your response, immediately slide the cover sheet down, or, where necessary turn the page to confirm your response. This immediate confirmation is vital. The immediate knowledge of the correctness of your response is a strong reinforcement of your learning. We have carefully arranged and phrased the frames to allow a minimum of wrong responses. Should you make a wrong response, return to the frame and cross out your answer, and after re-reading the information presented, write in the correct response.

There is no doubt about the effectiveness of programmed learning; it has been proven. Follow instructions and you will learn more in less time, and learn it better than you would learn by conventional training methods.

Remove your cover sheet, place it under the next frame and use as previously directed.

- i. The following introductory material is presented in the same form as the text. To answer one of the most common questions, and possibly one you are asking yourself, this is not a test, it is a text! Although presented in a different form this information is still a _____ book.

i. text book

- ii. This text differs from the normal text in that it uses an auto-instructional approach, also called programed learning. The subject matter content is carefully sequenced, giving it another name, a Program.

This textbook can also be called a _____.

ii. Program

- iii. Programed learning presents the information in small steps called "frames." This small step you are now reading is a _____.

iii. frame

- iv. Have you noticed that you cannot skip right through? You must take each frame in sequence, read it carefully and then you participate by _____ your response in the blank space.

iv. writing
or placing
or constructing
(or equivalent)

- v. After having written your response you must immediately move the cover sheet down, or turn the page, to confirm your response. If your response is not correct, cross it out. Re-read the frame and then write in the correct _____.

v. response

- vi. If the blank space occurs within a sentence, do not write your response until you have _____ the complete sentence.

vi. read
(or equivalent)

- vii. There will also be frames in which your response will be to write or draw a correct version of the subject matter. Be sure to draw these on the page, or an accompanying sheet of paper, allowing you to check your _____.

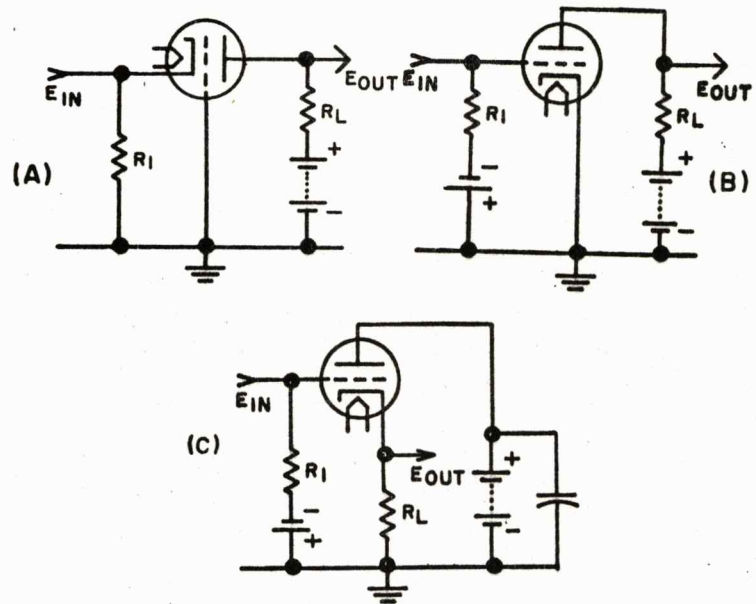
vii. response

viii. You will also find occasional information frames whose contents are presented solely for information - no response of any kind is required. In this case you will be told to "proceed to the next frame." What you are now reading is an example of an informational frame.

Now that you have the idea, start the program.

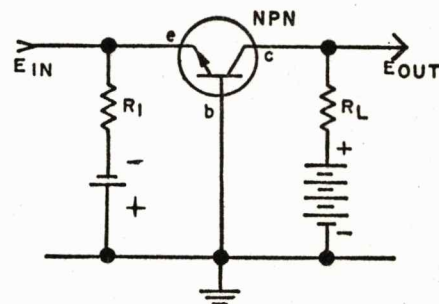
VOLUME I
SEMICONDUCTOR CIRCUITS

1. Tube amplifiers have three general configurations shown in illustrations A, B, and C below. They are (A) the grounded-grid, (B) the grounded-cathode (the most common), and (C) the grounded-plate or cathode follower. Note that "grounded" refers to signal ground, not necessarily DC ground. In transistor amplifiers we again have three configurations, each one equivalent to one of the tube configurations. However, with transistors we use the term "common" instead of "grounded."



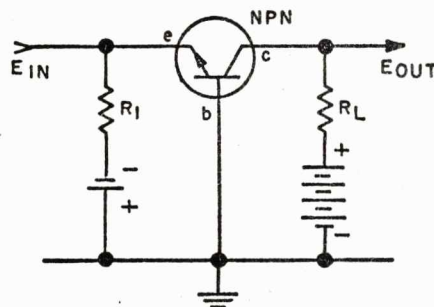
(Proceed to next frame)

2. "Common" refers to the transistor element which is common to both the input and the output circuits. In this basic amplifier the input signal is applied between the emitter and the _____ of the transistor.



2. base

3. The output is taken across the collector and the _____ of the transistor.

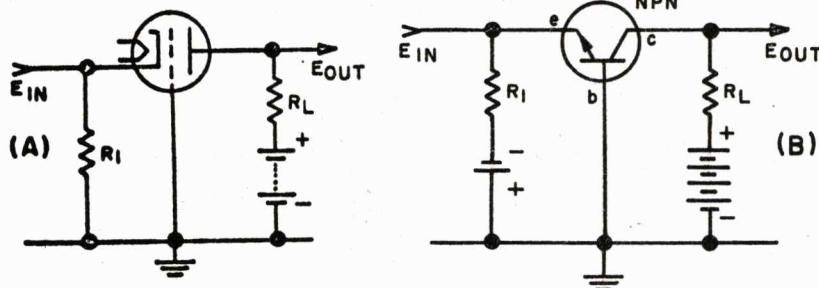


3. base

4. Since the base is common to both the input and the output circuits, we call this a _____ amplifier.

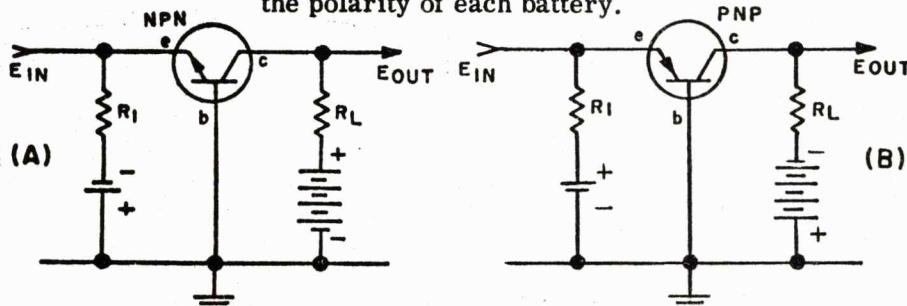
4. common-base

5. In the circuits below, note the similarities between the grounded-grid amplifier (A) and the _____ amplifier (B).



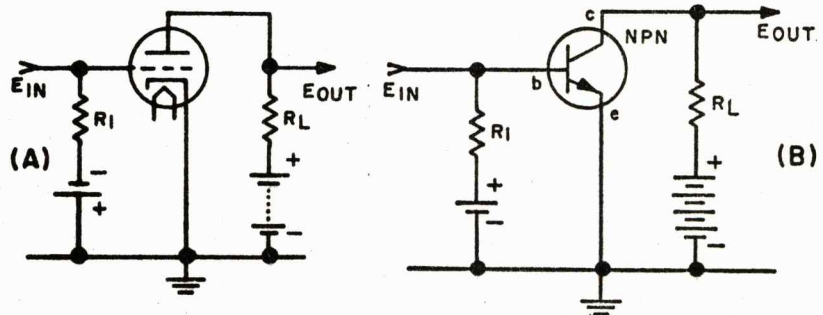
5. common-base

6. In the common-base, and the other two amplifier configurations which follow, we can change from NPN (A) to PNP (B) simply by reversing the polarity of each battery.

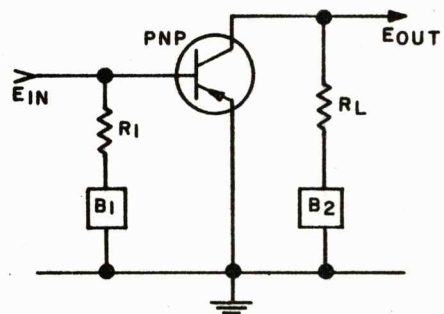


(Proceed to next frame)

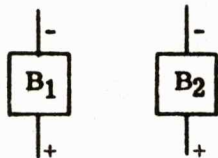
7. Here we have the popular grounded-cathode amplifier (A) and its transistor equivalent (B). Note that the transistor's input is between its _____ and its _____.



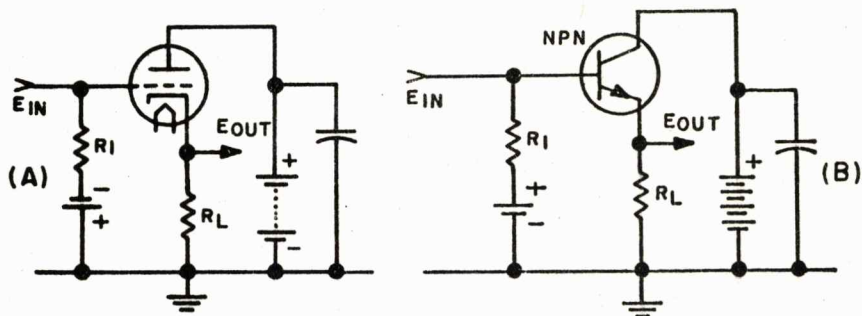
7. base -- emitter
(or vice versa)
8. And the output is taken across the _____ and the _____ of the transistor.
8. collector -- emitter
(or vice versa)
9. Since the emitter is common to both the input and output circuits, we call this a _____ amplifier.
9. common-emitter
10. On the circuit shown below, indicate the proper battery polarities for a common-emitter PNP amplifier.



10.

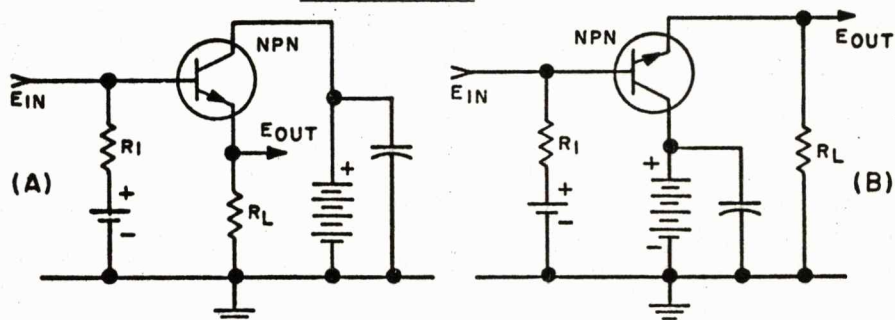


11. Lastly we have the grounded-plate amplifier (A), more commonly called the cathode follower, and the equivalent transistor circuit (B). It takes a close look and a little thought to realize that the input signal is applied between the base and _____ of the transistor.



11. collector

12. Compare circuits (A) and (B) shown below. Note that they are exactly the same and that the collector is at signal ground. However, (B) shows more clearly that the input signal is applied between the transistor's _____ and _____.

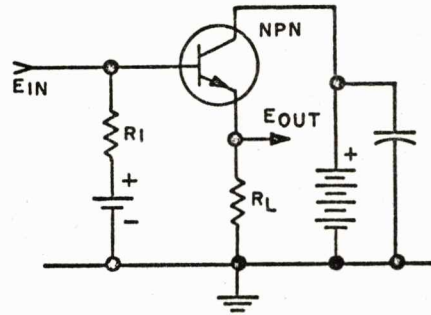


12. base -- collector
(or vice versa)

13. Now it is easy to see that the output signal is taken between the _____ and _____ of the transistor.

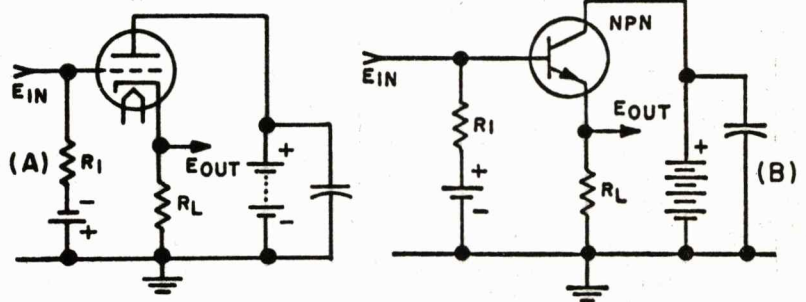
13. emitter -- collector
(or vice versa)

14. So we can call this a common-_____ amplifier.



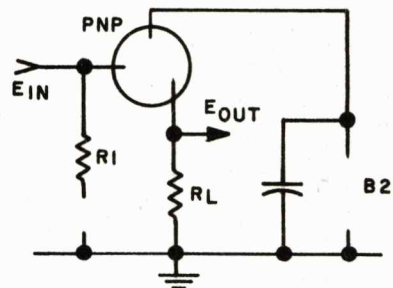
14. collector

15. Just as the tube version (A) is usually called a cathode follower, we often call the common-collector amplifier (B) an _____ follower.

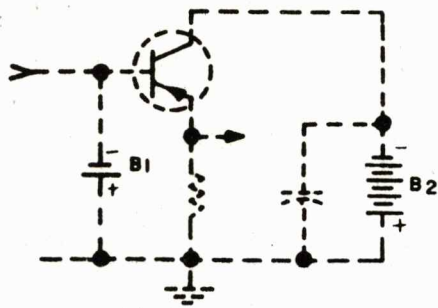


15. emitter

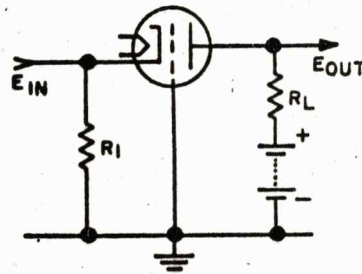
16. Complete the circuit shown below for a PNP emitter follower.



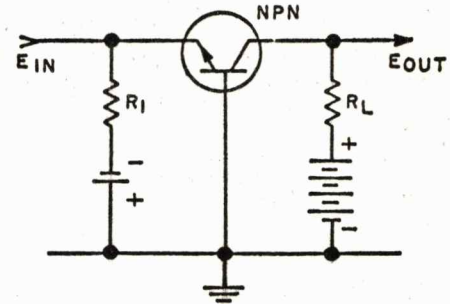
16.



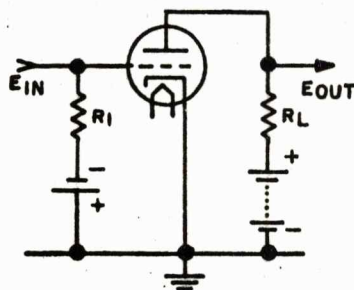
17. For a comparison of the three amplifier configurations with both tubes and transistors, study the circuits shown below. Note particularly the input and output circuits, and the common elements. These circuits may become cluttered with components for biasing, stabilization, feedback, etc., and are sometimes hard to recognize with an unpracticed eye, but the basic configuration must be either common-emitter, common-base, or common-collector.



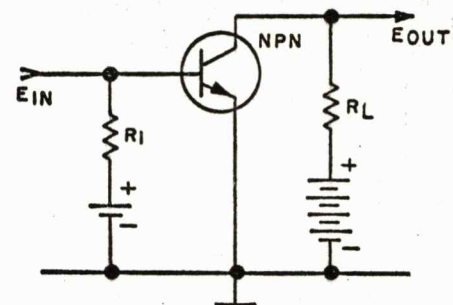
(A) GROUNDING GRID



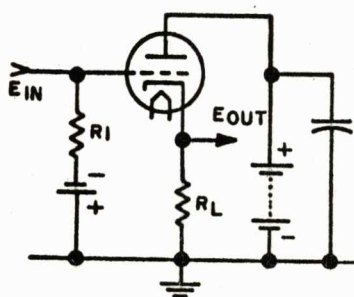
(D) COMMON BASE



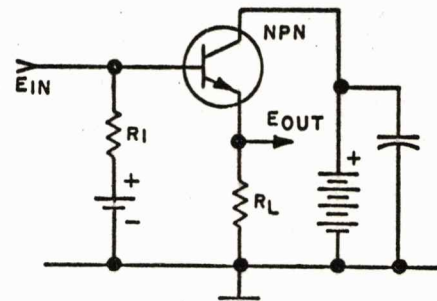
(B) GROUNDING CATHODE



(E) COMMON EMITTER

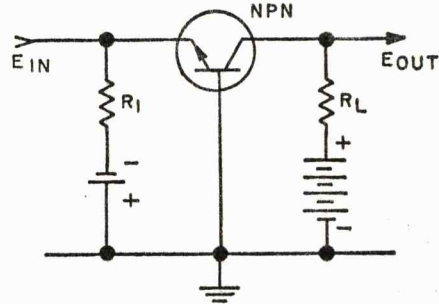


(C) GROUNDING PLATE

(F) COMMON COLLECTOR
(EMITTER FOLLOWER)

(Proceed to next frame)

18. Now let's look at the characteristic input and output impedances of the three transistor amplifier configurations. In the common-base the input signal is applied between the emitter and the base, that is, across the _____ - _____ junction.

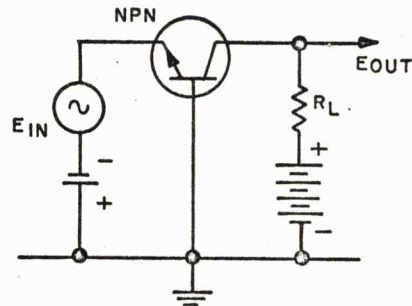


18. emitter-base
(or vice versa)

19. The emitter-base junction, remember, is _____ (forward/reverse) biased.

19. forward

20. Forward bias encourages high conduction across a junction. Therefore the input source sees a _____ (low/high) input impedance.



20. low

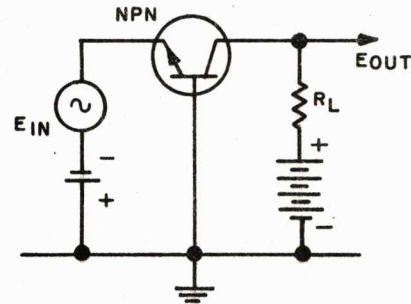
21. The output signal in a common-base amplifier is taken across the _____ - _____ junction.

21. base-collector
(or vice versa)

22. reverse

22. The base-collector junction is always
_____ biased in amplifiers.

23. Since the reverse bias discourages conduction
across the base-collector junction the output
circuit appears as a _____ impedance.



23. high

24. So we see that the common-base amplifier
has a _____ input impedance and a
_____ output impedance.

24. low -- high

25. With a low input impedance (Z_{in}) and a high
output impedance (Z_{out}), we can say that the
common-base amplifier has an impedance gain.
Typical values are 30Ω - 150Ω for Z_{in} and
 $300K$ - $500K$ for Z_{out} , giving an
_____ of several thousand.

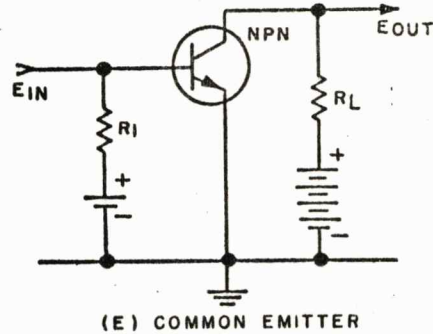
25. impedance gain

26. Let's start a chart showing the characteristics
of our three amplifier configurations. We will
add to this chart as we uncover more information.

	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Low		
Z_{out}	High		
Z_{gain}	High		
	30Ω - 150Ω		
	$300K$ - $500K$		
	$n \times 1000$		

(Proceed to next frame)

27. Now for the common-emitter amplifier. As with the common-base the input signal is applied across the forward biased emitter-base junction. Therefore we expect a Z_{in} .

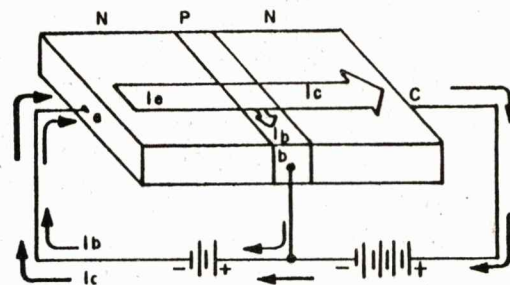


27. low

28. The typical values of common-emitter Z_{in} of 500Ω - 1500Ω are not nearly so low as the 30Ω - 150Ω of the common-amplifier. There is another factor which we will now consider.

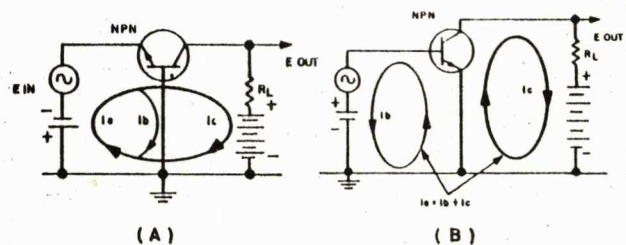
28. base

29. Current flows in a transistor as shown below. That is, a heavy current flows from emitter to collector through the base. The current flow in the base lead is very



29. small, light, low, etc.

30. Here, current flow is shown schematically for common-base (A) and common-emitter (B). Note that in the common-base (A) the signal source must carry a current, while in the common-emitter (B) the signal source carries only a current.



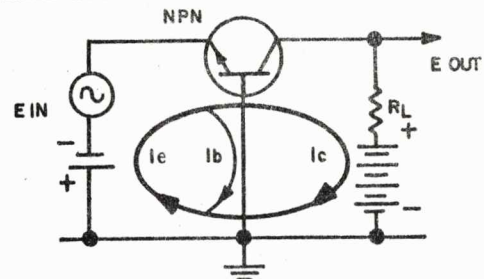
30. large, heavy, etc. --
small, light, etc.

31. low

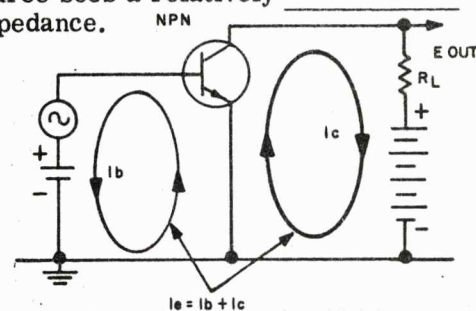
32. high

33. lower

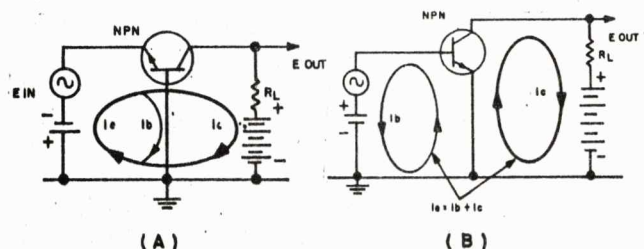
31. With a large current flowing in the input circuit of the common-base, the source "sees" a _____ impedance.



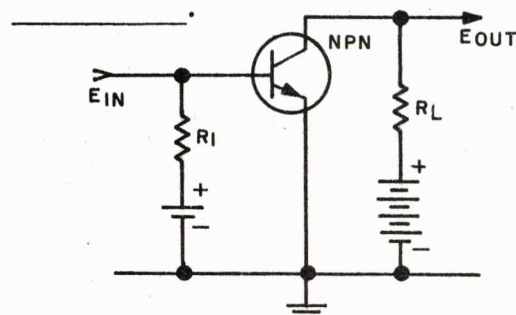
32. On the other hand, with only a small current in the input circuit of the common-emitter, the source sees a relatively _____ impedance.



33. Thus we see that, although both amplifiers have their input circuits across forward biased junctions, the heavy current in the input circuit of the common-base (A) leads to a much _____ impedance than the light current in the input circuit of the common-emitter (B).

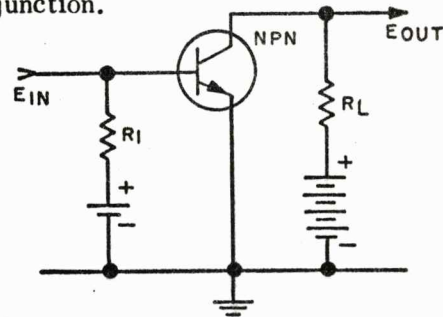


34. Now let's see what the output impedance looks like in the common-emitter amplifier. We said previously that the output signal was taken between the transistor's _____ and its _____.



34. collector -- emitter
(or vice versa)

35. But between the emitter and the collector we have both the reverse biased base-collector junction and the _____ biased emitter-base junction.



35. forward

36. The reverse biased base-collector junction gives a _____ output impedance, as in the common-base amplifier.

36. high

37. However, in the common-emitter amplifier, the forward biased emitter-base junction is in series opposition with the reverse biased base-collector junction. Therefore, the output impedance is considerably _____ (raised/lowered).

37. lowered

38. So while the common-base has a typical output impedance of 300K - 500K, the common-emitter's output impedance is in the order of 30K - 50K.

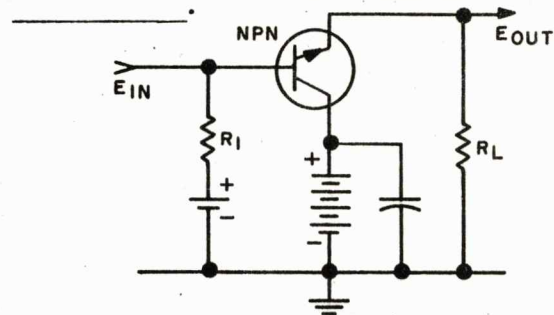
(Proceed to next frame)

39. With a Z_{in} of 1000 Ω and a Z_{out} of 40K, for example, the common-emitter amplifier will have an impedance gain of about _____.

	COMMON-BASE		COMMON-EMITTER		COMMON-COLLECTOR	
Z_{in}	Low	30 Ω - 150 Ω	Low	500 Ω - 1500 Ω		
Z_{out}	High	300K - 500K	High	30K - 50K		
Z_{gain}	High	n x 1000		n x 10		

39. 40

40. Now for the common-collector amplifier, or emitter follower. We have shown that its input is applied between the _____ and the _____.



40. base -- collector
(or vice versa)

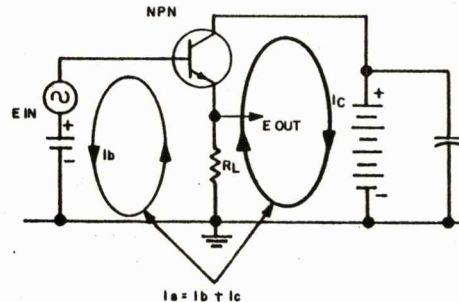
41. The base-collector junction, as in all amplifiers, is _____ biased.

41. reverse

42. With the signal source looking into a reverse biased junction we can expect a _____ input impedance.

42. high

43. Also, the signal source is in a _____ (low, high) current path.



43. low

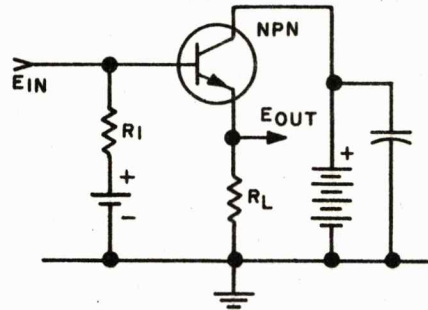
44. With a low current input circuit and a reverse biased input junction, the input impedance will be very _____.

44. high

45. Indeed, Z_{in} for the common-collector amplifier is typically 20K - 500K or more as compared with about 100Ω for the common-base and 1000Ω for the common-emitter.

(Proceed to next frame)

46. The output of the common-collector amplifier is taken from between the _____ and the _____ of the transistor.

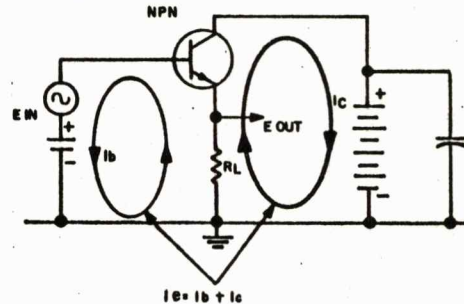


46. collector -- emitter
(or vice versa)

47. With the collector at signal ground, we are not concerned with the _____ biased base-collector junction.

47. reverse

48. The output is taken across the emitter load resistor. Since the full current of the transistor must pass through this resistor we have a _____ output impedance.



48. low

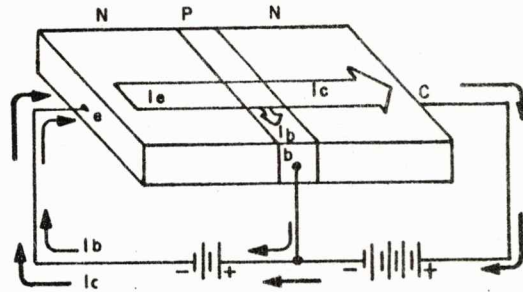
49. With a high Z_{in} of 20K - 500K and a low Z_{out} of 50 Ω - 1000 Ω , the common-collector amplifier has a fractional Z gain.

Take a few seconds now to compare the impedance characteristics of our three amplifier configurations on the chart below.

	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest 30 Ω - 150 Ω	Low 500 Ω - 1500 Ω	Highest 20K - 500K
Z_{out}	Highest 300K - 500K	High 30K - 50K	Lowest 50 Ω - 1000 Ω
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1

(Proceed to next frame)

50. Now let's take a closer look at the current flow in our three amplifier configurations. As illustrated here, $I_e = \underline{\hspace{1cm}} + \underline{\hspace{1cm}}$.



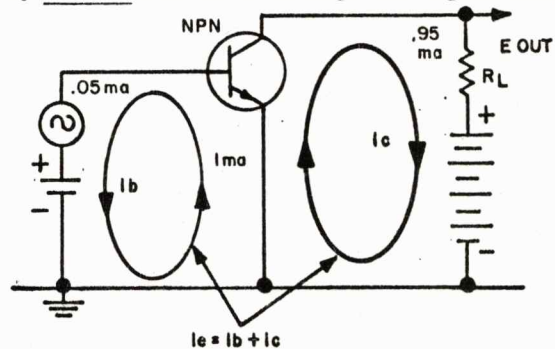
50. $I_e = I_b + I_c$

51. Generally $I_c = 92\%$ to 98% of I_e and $I_b = 2\%$ to 8% of I_e . In our examples we will assume that $I_c = 95\%$ I_e and $I_b = 5\%$ I_e .

(Proceed to next frame)

52. Here we have the common-emitter circuit with static element currents indicated.

Note that for a current of .95 ma through R_L , only _____ ma flows through the signal source.



52. .05

53. That is, I_c is $\frac{.95}{.05} = \underline{\hspace{1cm}}$ times I_b .

53. 19

54. If the amplifier is operated on the linear part of the transistor's characteristic curves, then a small change in I_b will cause a corresponding amplified change in I_c . Since I_c is $19 \times I_b$, the change in I_c will be $19 \times$ the change in I_b .

(Proceed to next frame)

55. For example, if I_b increases by .001 ma ($\Delta I_b = .001$). I_c will increase by $19 \times .001 = \underline{\hspace{1cm}}$ ma (ΔI_c).
55. .019
56. Since I_c changes 19 times as much as I_b , we can say that we have a current $\underline{\hspace{1cm}}$ of 19.
56. gain
57. In mathematical terms, for common-emitter: current gain = $\Delta I_c / \Delta I_b$. (The symbol Δ is the Greek letter delta. In mathematics it means "change in.") Using the same figures: current gain = $\Delta I_c / \Delta I_b = .019 / .001 = \underline{\hspace{1cm}}$.
57. 19
58. In any configuration, the relation $\Delta I_c / \Delta I_b$ is known by the Greek letter β (beta) and is a characteristic of a given type of transistor, just as $\mu = \Delta e_b / \Delta e_c$ is a characteristic of a given type vacuum tube.

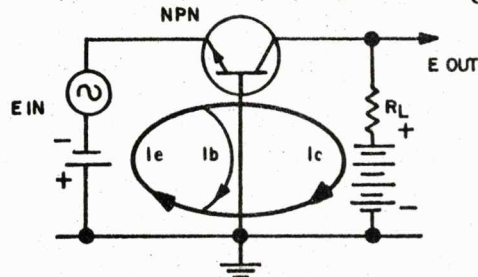
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59. We said that $\beta = \Delta I_c / \Delta I_b$ is a characteristic of a given type of transistor. Also, in the common-emitter configuration, $\Delta I_c / \Delta I_b =$ current gain. Therefore, in the common-emitter configuration, $\beta = \underline{\hspace{1cm}}$.
59. current gain
60. Typical values of common-emitter current gain range from 25 to 50. So we can also say that β for typical junction transistors ranges from $\underline{\hspace{1cm}}$ to $\underline{\hspace{1cm}}$.

	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest $30\Omega - 150\Omega$	Low $500\Omega - 1500\Omega$	Highest $20K - 500K$
Z_{out}	Highest $300K - 500K$	High $30K - 50K$	Lowest $50\Omega - 1000\Omega$
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1
I_{gain}		$\beta = \Delta I_c / \Delta I_b$ 25 - 50	

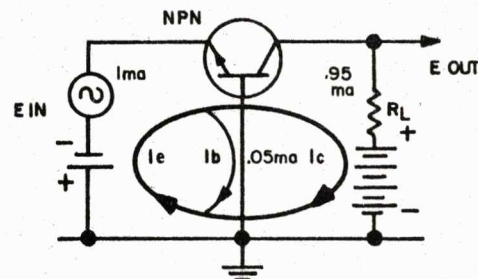
60. 25 -- 50

61. As we can see in this diagram, $\beta = \Delta I_c / \Delta I_b$ does not give us current gain (I gain) for the common-base configuration. Since the signal source is in the emitter circuit, I gain = $\Delta I_c / \Delta I_e$.



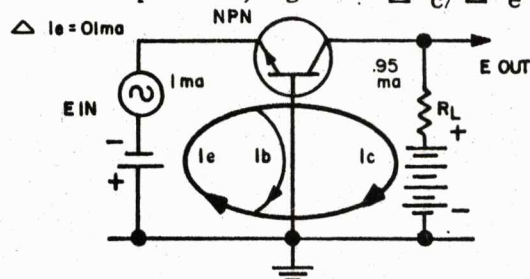
61. I gain = $\Delta I_c / \Delta I_e$

62. However, I_c is only about _____ % of I_e .



62. $I_c = 95\% I_e$

63. With the figures given in the diagram, assuming linear operation, I gain = $\Delta I_c / \Delta I_e =$ _____.



63. .95

64. The relation $\Delta I_c / \Delta I_e$ for any configuration is known by the Greek letter α (alpha). Like β , α is a characteristic of a given type transistor. In the common-base configuration $\alpha = \Delta I_c / \Delta I_e$ is equal to _____.

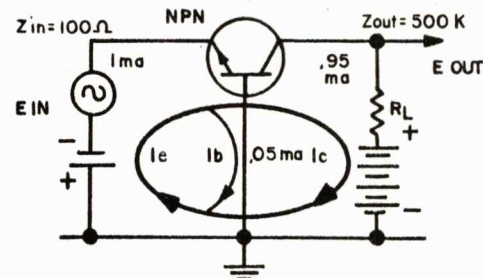
	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest $30\Omega - 150\Omega$	Low $500\Omega - 1500\Omega$	Highest $20K - 500K$
Z_{out}	Highest $300K - 500K$	High $30K - 50K$	Lowest $50\Omega - 1000\Omega$
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1
I_{gain}	$\alpha = \Delta I_c / \Delta I_e$.92 - .98	$\beta = \Delta I_c / \Delta I_b$ 25 - 50	

64. current gain

65. If the common-base configuration has a current gain of less than 1, what good is it? Remember that the common-base has an input impedance in the neighborhood of 100 ohms and an output impedance of 500K or so.

(Proceed to next frame)

66. We can see that a ΔI_e of .1 ma requires that the signal source provides an E_{in} of $\Delta I_e \times Z_{in}$ = .1 ma x 100 ohms = _____ volt.



66. .01

67. Since $I_c = .95 I_e$ and $\Delta I_e = .1$ ma, $\Delta I_c = .95 \times .1$ ma = .095 ma in linear operation. But, this .095 ma is in a 500K circuit. Therefore $E_{out} = \Delta I_c \times Z_{out}$ is in the neighborhood of .095 ma x 500K = _____ volts.

67. 47.5

68. With an E_{in} of .01 volt and an E_{out} of 47.5 volts, this common-base amplifier has a tremendous _____ of 47.5/.01 or 4750.

68. voltage gain

69. Since we have ignored various losses, impedance mismatch, and other factors, we must take these figures with a grain of salt. Nevertheless, they serve to show that the common-base amplifier gives high voltage gain in spite of a current gain of less than one. Realistic values of E_{gain} range from 300 to 1500.

(Proceed to next frame)

70. We can also say that $E_{gain} = I_{gain} \times Z_{gain}$ - (losses, etc.). In the case above, with $Z_{in} = 100 \Omega$ and $Z_{out} = 500K$, $E_{gain} = .95 \times 500000/100 =$ _____ - (losses etc.).

70. 4750

71. In the common-emitter amplifier we have both I_{gain} and Z_{gain} , but the Z_{gain} is much _____ than in the common-base.

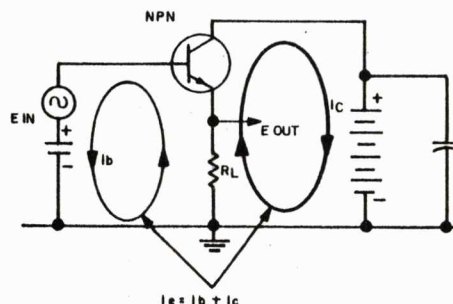
71. lower, less etc.

72. With typical values, $E_{gain} = I_{gain} \times Z_{gain}$
 - losses etc. = 40×40 - losses, etc.
 = 1600 - losses etc. Typical values for common-emitter E_{gain} are 200 - 1000. This is a little
 _____ than for the common-base.

	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest $30\Omega - 150\Omega$	Low $500\Omega - 1500\Omega$	Highest $20K - 500K$
Z_{out}	Highest $300K - 500K$	High $30K - 50K$	Lowest $50\Omega - 1000\Omega$
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1
I_{gain}	$\alpha = \Delta I_c / \Delta I_e$.92 - .98	$\beta = \Delta I_c / \Delta I_b$ 25 - 50	
E_{gain}	300 - 1500	200 - 1000	

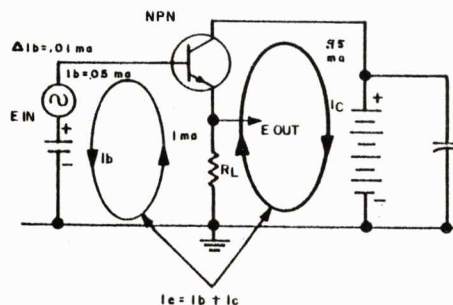
72. less, lower, etc.

73. With your present knowledge of transistor amplifiers you should be able to deduce that current gain for the common-collector amplifier is given by the ratio $\Delta I_{\underline{\quad}} / \Delta I_{\underline{\quad}}$.



73. $I_{gain} = \Delta I_e / \Delta I_b$

74. Using our same values of static element current in linear operation, we see that $I_{gain} = \Delta I_e / \Delta I_b = I_e / I_b = 1 / .05 = 20$. Typical values range from 25 to 50. I_{gain} for the common-collector is practically the same as for the _____.



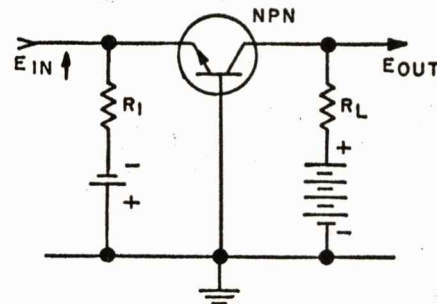
74. common-emitter

75. Although the common-collector has a good current gain, it has an impedance gain of much less than one. The net result is that, like the cathode follower, the emitter follower has a voltage gain of less than one.

	COMMON-BASE		COMMON-EMITTER		COMMON-COLLECTOR	
Z_{in}	Lowest	$30\Omega - 150\Omega$	Low	$500\Omega - 1500\Omega$	Highest	$20K - 500K$
Z_{out}	Highest	$300K - 500K$	High	$30K - 50K$	Lowest	$50\Omega - 1000\Omega$
Z_{gain}	Highest	$n \times 1000$		$n \times 10$	Less than 1	
I_{gain}	$\alpha = \Delta I_c / \Delta I_e,$.92 - .98		$\beta = \Delta I_c / \Delta I_b,$ 25 - 50		$\Delta I_e / \Delta I_b,$ 25 - 50	
E_{gain}	300 - 1500		200 - 1000		Less than 1	

(Proceed to next frame)

76. What about phase inversion in transistor amplifiers? Well, let's look at the NPN common-base first. The emitter is forward biased with a negative potential. So a positive-going E_{in} will cause a/an _____ (increase/decrease) in the forward bias.



76. decrease

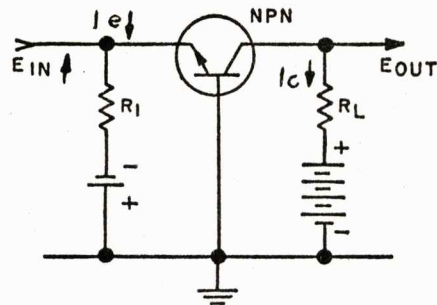
77. The decrease in forward bias in turn causes a/an _____ (increase/decrease) in I_e .

77. decrease

78. The decrease in I_e means we have a/an _____ in I_c .

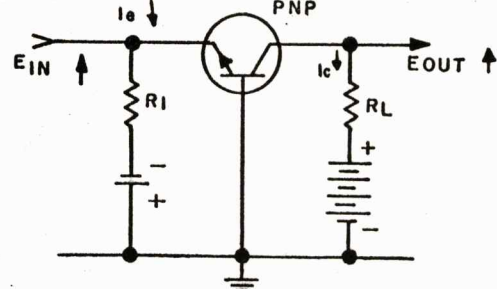
78. decrease

79. The decrease in I_C causes a decrease in the IR drop across R_L resulting in a _____ (positive/negative)-going E_{out} .



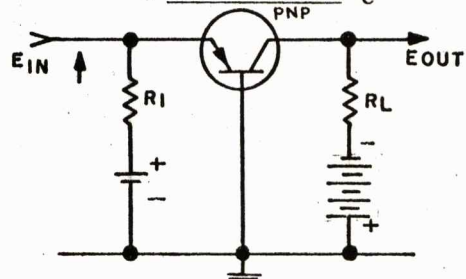
79. positive

80. Therefore, in the common-base amplifier, we _____ (do/do not) have phase inversion.



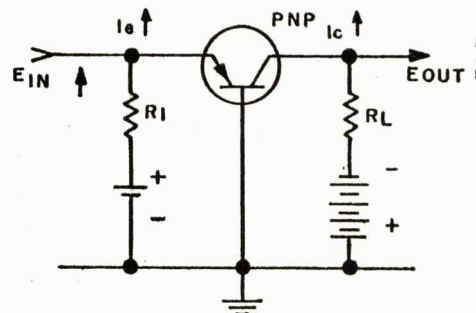
80. do not

81. In a PNP common-base amplifier a positive-going E_{in} will increase the positive forward bias, and thereby _____ I_E .



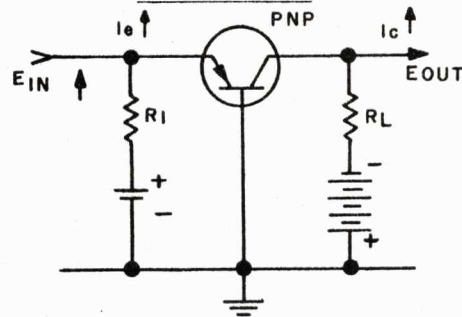
81. increase

82. The resulting increase in I_C causes a/an _____ in the IR drop across R_L .



82. increase

83. Since the collector is reverse biased with a negative potential, the increased IR drop across R_L results in a _____-going E_{out} .

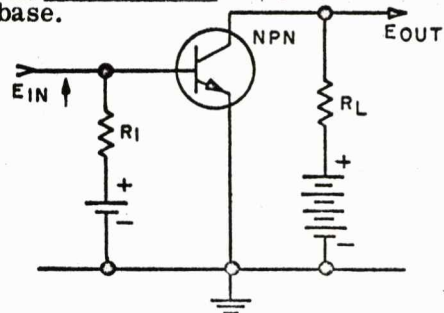


83. positive

84. So we see again that, although they operate differently in some respects, the PNP and NPN versions of a given amplifier produce the same results, in this case absence of phase inversion. You may remember that the tube counterpart, the grounded-grid, also has no phase inversion.

(Proceed to next frame)

85. In the NPN common-emitter amplifier a positive-going E_{in} _____ the positive forward bias at the base.

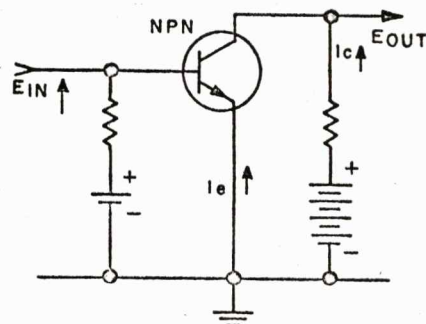


85. increases

86. The increased forward bias causes I_E , and therefore I_C , to _____.

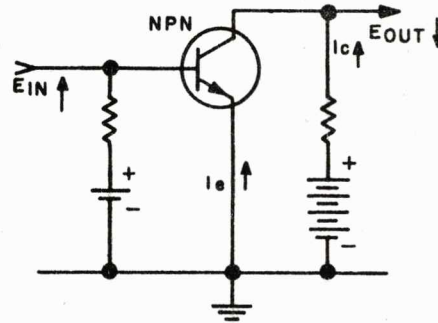
86. increase

87. Increased I_C and the resulting IR drop across R_L cause a _____-going E_{out} .



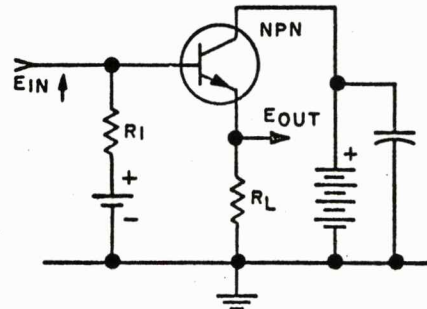
87. negative

88. With a negative-going output from a positive-going input, it is obvious that the common-emitter _____ (does/does not) give phase inversion.



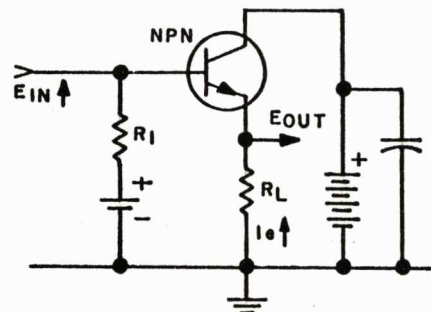
88. does

89. In the NPN common-collector (or emitter follower) amplifier, a positive-going E_{IN} increases the forward bias, causing I_E and the IR drop across R_L to _____.



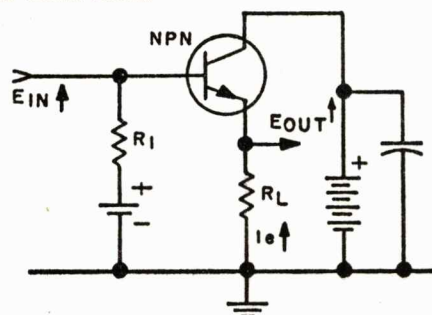
89. increase

90. With an increased IR drop across R_L , E_{out} will also be _____-going.



90. positive

91. So we can conclude that, like the cathode follower, the emitter follower _____ (does/does not) give phase inversion.



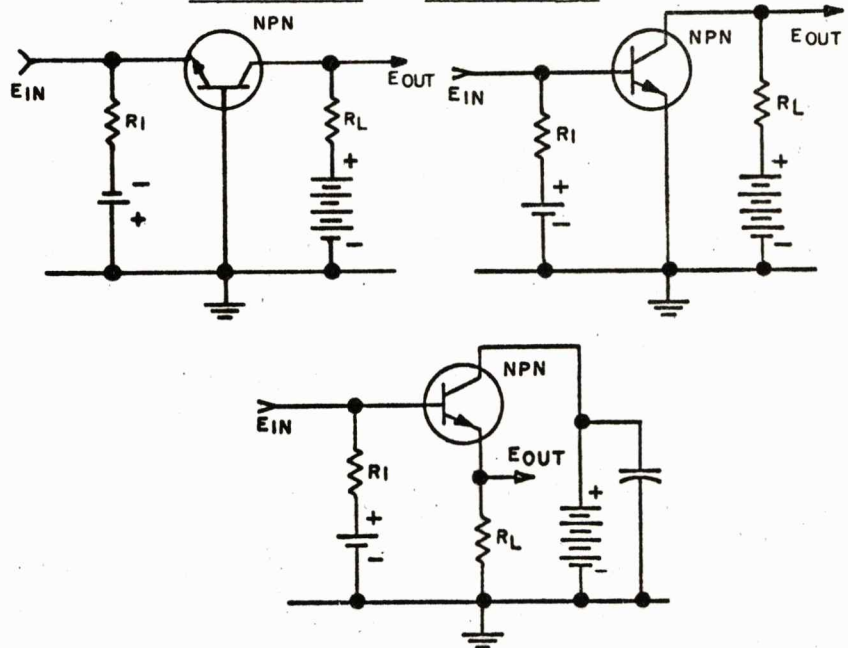
	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest $30\Omega - 150\Omega$	Low $500\Omega - 1500\Omega$	Highest $20K - 500K$
Z_{out}	Highest $300K - 500K$	High $30K - 50K$	Lowest $50\Omega - 1000\Omega$
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1
I_{gain}	$\alpha = \Delta I_c / \Delta I_e,$.92 .98	$\beta = \Delta I_c / \Delta I_b,$ 25 - 50	$\Delta I_e / \Delta I_b,$ 25 - 50
E_{gain}	300 - 1500	200 - 1000	Less than 1
Inversion	No	Yes	No

91. does not

92. Thus far, for the sake of simplicity, our examples of transistor circuits have used separate batteries for forward and reverse bias. In typical applications, values of reverse bias fall in the range of 6 to 60 volts while forward bias is only a few tenths of a volt. Therefore, we should be able, by use of voltage dividing resistors, to obtain _____ bias from the _____ bias battery.

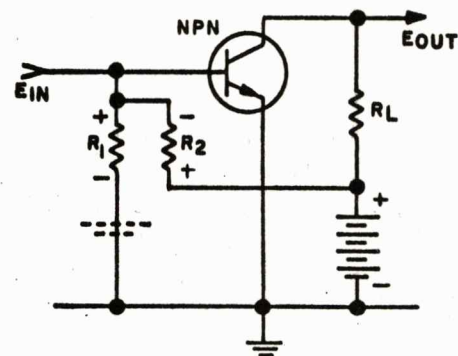
92. forward -- reverse

93. In the three basic circuits below, note that in each case the potential on the transistor's _____ is between the potentials of its _____ and _____.



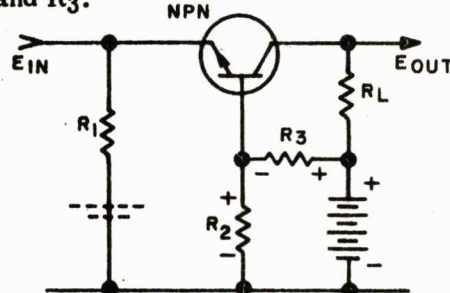
93. base -- emitter -- collector
or
base -- collector -- emitter

94. In this common-emitter circuit below the forward bias battery is eliminated and the base is now biased a little positive with respect to the emitter by the voltage divider composed of _____ and _____.



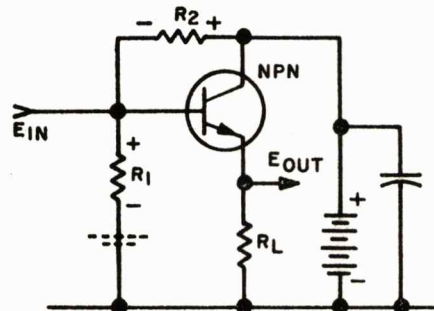
94. $R_1 \leftrightarrow R_2$
(or vice versa)

95. In this common-base amplifier, the base is biased positive with respect to the emitter by the _____ composed of R_2 and R_3 .



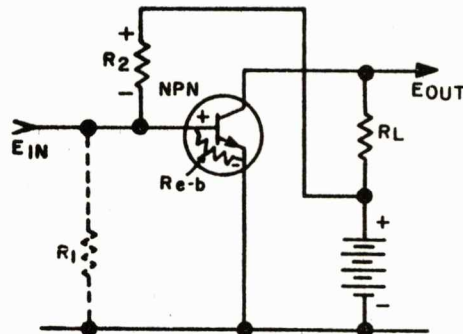
95. voltage divider

96. Again in the common-collector, we derive base bias from the voltage divider consisting of _____ and _____.



96. $R_1 \leftrightarrow R_2$
(or vice versa)

97. In some cases it may be possible to replace R_1 , as shown in this common-emitter circuit, with the internal resistance of the _____ junction.



97. emitter-base
(or vice versa)

98. By simply reversing the battery and the emitter arrow, each of the preceding NPN circuits becomes a perfectly valid _____ circuit.

98. PNP

99. Transistors are much more sensitive to heat than vacuum tubes. Although there is no heat generating filament, any IR drop across the transistor must be dissipated to prevent temperature buildup. Most of the IR drop in a transistor occurs at the reverse biased, high resistance (relatively), base-collector junction. Therefore, most of the heat (I^2R) is developed at the _____ - _____ junction.

99. base-collector
(or vice versa)

100. Without going into detail, we will simply state that a rise in temperature at the base-collector junction leads to an increase in current flow through the transistor. Since the heat generated is equal to I^2R , the increased current leads to _____ (increased/decreased) heating.

100. increased

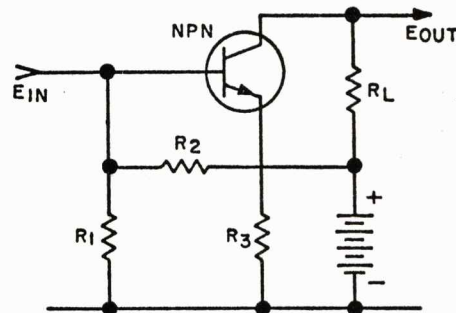
101. Again, the increased temperature leads to increased _____ through the transistor.

101. current

102. We can easily see that this vicious circle of temperature, current, temperature, current ---- quickly leads to the _____ of the transistor.

102. burn out, destruction,
ruin, etc.

103. This thermal-runaway is most serious in the common-emitter configuration. To limit current flow, a limiting resistor (R_3 below) is inserted in the _____ lead.

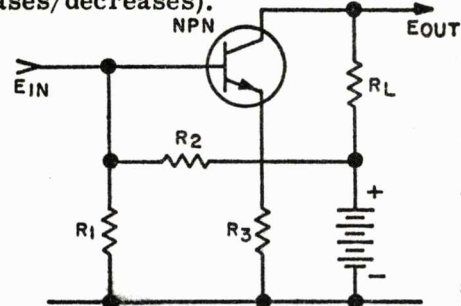


103. emitter

104. As emitter current increases, the $I_e \times R_3$ drop causes the emitter terminal to become more _____ (positive/negative).

104. positive

105. As the emitter terminal becomes more positive, the net emitter-base forward bias _____ (increases/decreases).

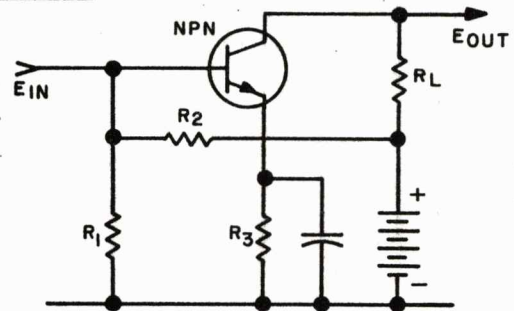


105. decreases

106. The decreased forward bias stabilizes the temperature-current relationship by _____ (increasing/decreasing) the emitter current.

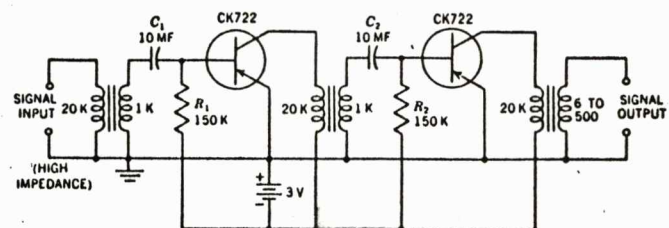
106. decreasing

107. As with a cathode bias resistor, the emitter stabilization resistor may be shunted with a capacitor to prevent degeneration. _____



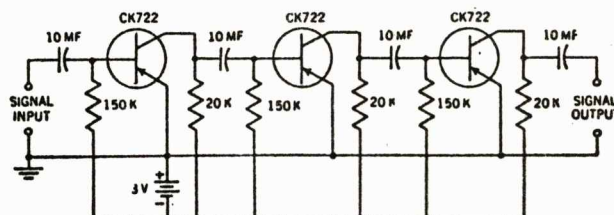
107. bypass

108. In vacuum tubes we have little trouble matching the high impedance output of one stage to the high impedance grid circuit of the next stage. In transistors, however, we have problems. For example, with common-emitter stages, Z_{out} may be 40K and Z_{in} 1K. One approach, shown below, is to use _____ coupling.



108. transformer

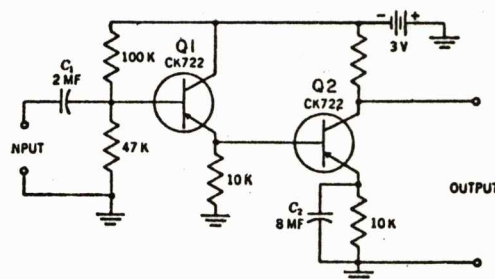
109. But for audio, good transformers are expensive, and cheap transformers give poor frequency response. A second approach, shown here, is to put up with a mismatch and use _____ coupling. Note that an extra stage has been added to make up for the loss in gain.



109. resistance or RC

110. Here is a two stage amplifier with high Z_{in} , high Z_{out} and matched interstage coupling. (Compare impedances on the chart below.)

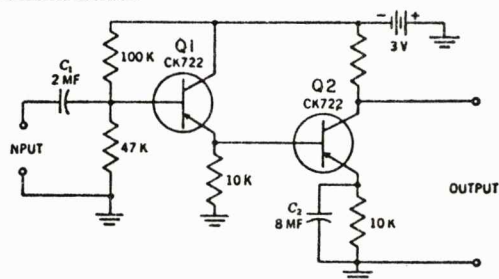
Note that the input transistor is connected in the _____ configura-
tion while the output stage is a _____.



	COMMON-BASE	COMMON-EMITTER	COMMON-COLLECTOR
Z_{in}	Lowest $30\Omega - 150\Omega$	Low $500\Omega - 1500\Omega$	Highest $20K - 500K$
Z_{out}	Highest $300K - 500K$	High $30K - 50K$	Lowest $50\Omega - 1000\Omega$
Z_{gain}	Highest $n \times 1000$	$n \times 10$	Less than 1
I_{gain}	$\alpha = \Delta I_c / \Delta I_e,$.92 - .98	$\beta = \Delta I_c / \Delta I_b,$ 25 - 50	$\Delta I_e / \Delta I_b,$ 25 - 50
E_{gain}	300 - 1500	200 - 1000	Less than 1
Inversion	No	Yes	No

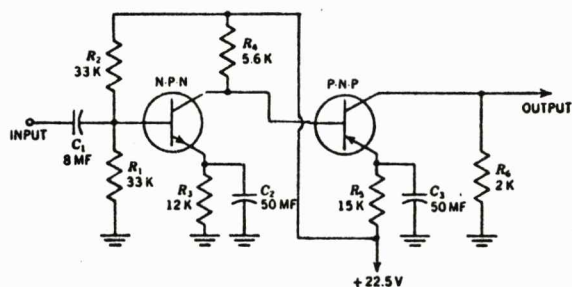
110. common-collector -- common-emitter

111. Notice also in this circuit that direct coupling is used between the _____ of Q1 and the _____ of Q2.



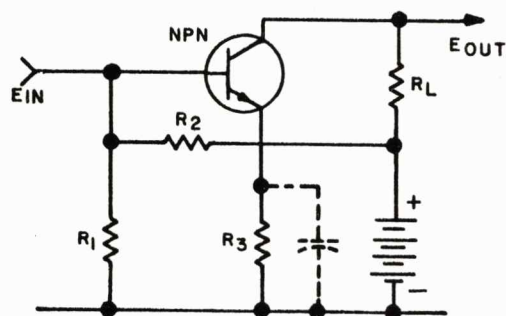
111. emitter -- base

112. This direct-coupled circuit has a voltage gain of about 660. It takes advantage of the "complementary symmetry" of NPN and _____ transistors.



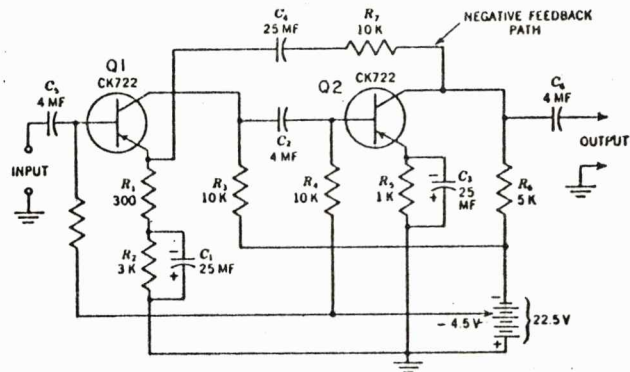
112. PNP

113. As with vacuum tube amplifiers, negative feedback can be used to raise the input impedance. In a single stage, leaving the emitter stabilization resistor, R3, unbypassed, provides the required degeneration or _____.



113. negative feedback

114. In this two stage amplifier, we have negative feedback from the collector of transistor Q2 to the emitter of transistor Q1 through the components _____ and _____.

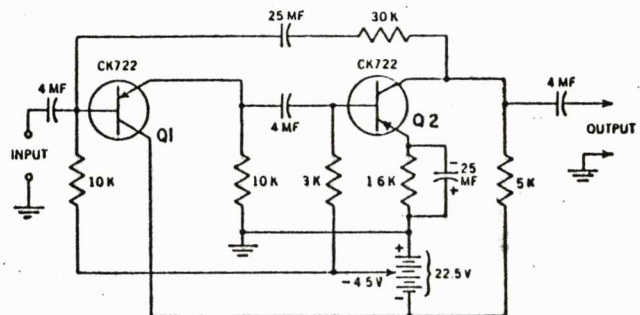


114. R_7 -- C_4
(or vice versa)

115. Note that this feedback is developed across an unbypassed section of the emitter resistance, $R_{\underline{\quad}}$, while stabilization is provided by $R_{\underline{\quad}}$.

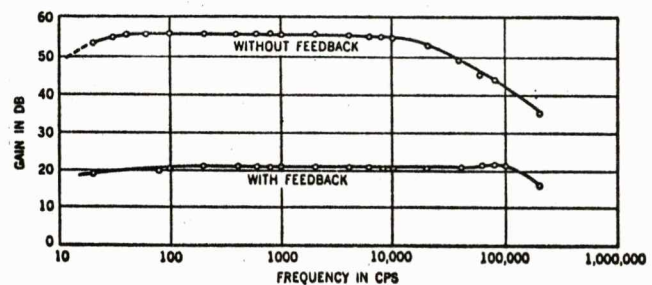
115. $R_{\underline{1}}$ -- $R_{\underline{2}}$

116. Here we have negative feedback from the collector of Q2 to the base of Q1. Note that Q1 is connected as a common-_____.



116. collector

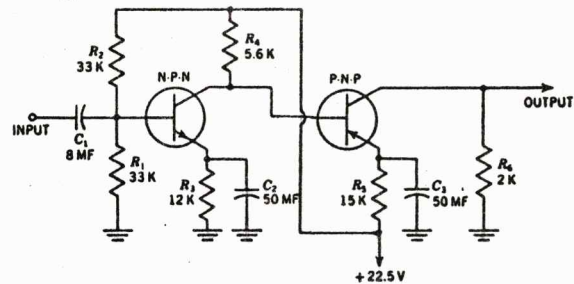
117. Although negative feedback raises the input impedance and flattens the frequency response, as shown here, it also greatly _____ the gain.



The effect of negative feedback on the frequency response of the amplifier.

117. reduces, lowers, etc.

118. Perhaps you have noticed the high values of capacitance used in coupling and bypassing. This is necessary because transistors are current devices, and these capacitors must handle signal currents, rather than signal voltages.



(Proceed to next frame)

119. Let us conclude this section on amplifier circuits with a short discussion of power gain (P_{gain}) and power amplifiers. Since $P = EI$ and $P_{ac} = I^2 Z$, we can also say that $P_{gain} = E_{gain} \times I_{gain}$ and $P_{gain} = (I_{gain})^2 \times \underline{\hspace{2cm}}$.

119. Z_{gain}

120. That is, if an amplifier has a current gain of 10 and a voltage gain of 300, it has a power gain of:

$$P_{gain} = E_{gain} \times I_{gain} = 300 \times 10 = \underline{\hspace{2cm}}$$

120. 3,000

121. Or if we have a current gain of 10 and an impedance gain of 30, $P_{gain} = (I_{gain})^2 \times Z_{gain} = 10^2 \times 30 = \underline{\hspace{2cm}}$.

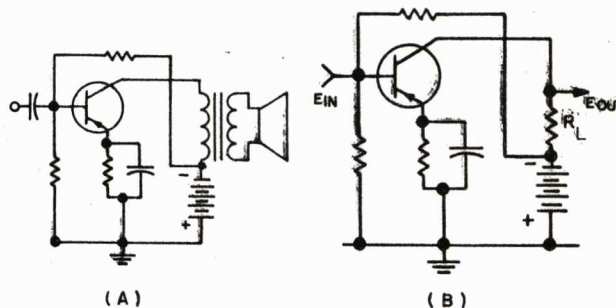
121. 3000

122. A power gain of 3000, or about 35 db, sounds like a lot. However, if P_{in} is in microwatts, we are still dealing in very low power levels. Shown below we have completed our chart by adding typical values of power gain for the three amplifier configurations. You can see that we achieve the greatest P_{gain} in the _____.

	COMMON-BASE		COMMON-EMITTER		COMMON-COLLECTOR	
Z_{in}	Lowest	$30\Omega - 150\Omega$	Low	$500\Omega - 1500\Omega$	Highest	$20K - 500K$
Z_{out}	Highest	$300K - 500K$	High	$30K - 50K$	Lowest	$50\Omega - 1000\Omega$
Z_{gain}	Highest	$n \times 1000$		$n \times 10$	Less than 1	
I_{gain}	$\alpha = \Delta I_c / \Delta I_e,$.92 - .98		$\beta = \Delta I_c / \Delta I_b,$ 25 - 50		$\Delta I_e / \Delta I_b,$ 25 - 50	
E_{gain}	300 - 1500		200 - 1000		Less than 1	
Inversion	No		Yes		No	
P_{gain}	100 - 1000 20 - 30 db		300 - 10,000 25 - 40 db		10 - 100 10 - 20 db	

122. common-emitter

123. Here we have a simple class A audio power amplifier (A). On paper, this circuit appears very similar to the voltage amplifier (B), except that R_L has been replaced by the output _____ and loudspeaker.



123. transformer

124. The power amplifier and voltage amplifier may look alike, but transistor power circuits and the transistors themselves, must be designed to handle larger currents and to dissipate greater amounts of _____.

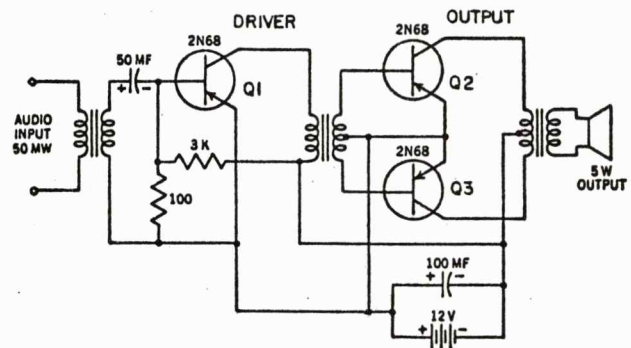
124. heat

125. Although class A push-pull operation offers the same advantages over single-ended operation for transistors as it does with vacuum tubes (lower distortion, more than two times the power, etc.), push-pull transistor audio power amplifiers are usually operated class _____.

125. B

126. The advantage of class B operation is its greater efficiency. In the simplified circuit below, the class B push-pull output stage, Q2 and Q3, draws only 1 ma with no signal input and 550 ma at maximum signal input with 5 watts output to the loudspeaker.

$$\begin{aligned}\text{Thus, efficiency} &= \text{Power Out} / \text{Power In} \\ &= \text{Power Out} / (E_{in} \times I_{in}) = 5 \text{ watts} / (12\text{V} \times .55\text{A}) \\ &= 5 \text{ watts} / 6.6 \text{ watts} = \underline{\hspace{1cm}} \%\end{aligned}$$

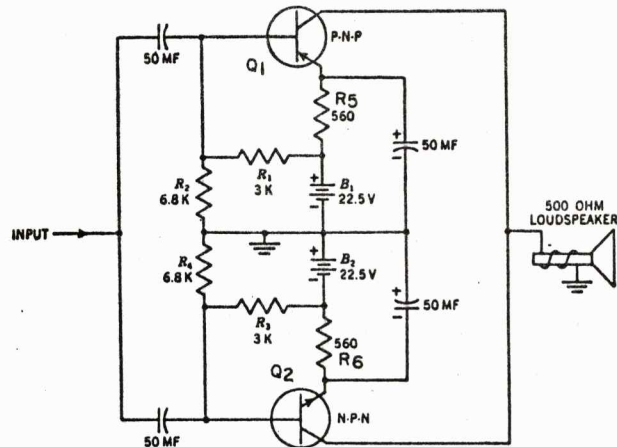


126. 75+

127. By comparison, the class A driver stage, Q1, draws an average current of 100 ma, signal or no signal, and is handling much less audio power. The efficiency of class B means not only lower power consumption, but also less heat buildup within the transistor and more power output from a given transistor type.

(Proceed to next frame)

128. This class A push-pull amplifier avoids the need of center tapped input and output transformers by taking advantage of the complementary symmetry of PNP and _____ transistors.

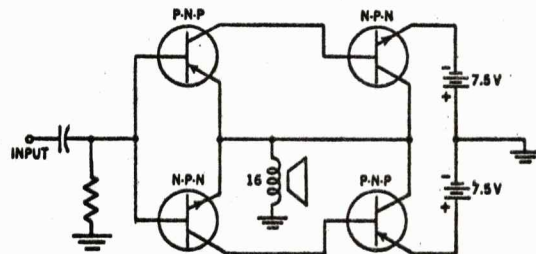


128. NPN

129. In this circuit, note that R_1 , R_2 , R_3 , and R_4 provide emitter-base _____, while R_5 and R_6 are _____ resistors.

129. bias -- stabilizing

130. Here is a simplified circuit of a class B push-pull, direct coupled amplifier. Note that the output impedance is very _____ (high/low).



130. low

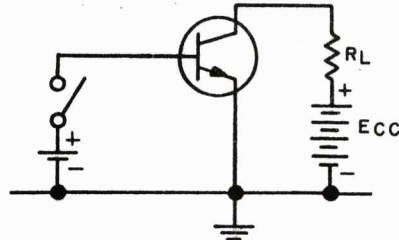
131. In presenting these various amplifier circuits we have not attempted to give a detailed description of their operation. They have been presented merely to give you an idea of the types of amplifier circuits in which transistors are used.

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132. So far, our discussion of transistor circuits has been limited to various types of amplifiers with small signal inputs, such as are used in radio receivers. We will now discuss some of the circuits employed in digital equipment.

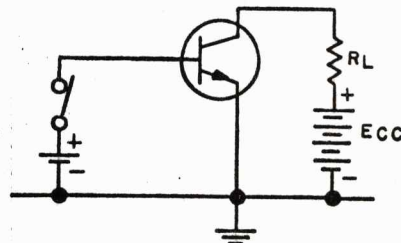
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133. In this circuit, with the switch open, the barrier potential within the transistor will cause _____ (a large/little or no) current to flow through R_L .



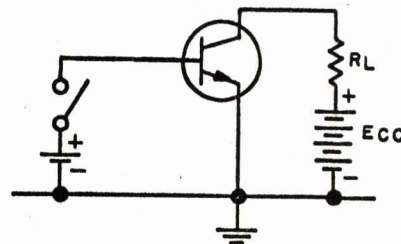
133. little or no

134. With the switch closed, however, a large current will flow through R_L due to the strong _____ bias on the emitter-base junction.



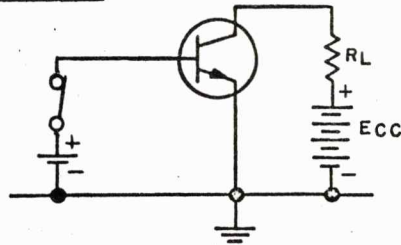
134. forward

135. To look at it another way, with the switch open and the base floating, the transistor acts as a very _____ resistance.



135. high

136. With the switch closed and the base forward biased, the transistor presents a very _____ resistance.



136. low

137. We refer to the high resistance, essentially non-conducting condition of the transistor as OFF, and the low resistance, conducting condition as _____.

137. ON

138. The OFF resistance of the transistor can be increased to several hundred K ohms by grounding the base instead of leaving it floating. The OFF resistance can be further increased by applying .2 volts or more of _____ bias to the emitter-base junction.

138. reverse

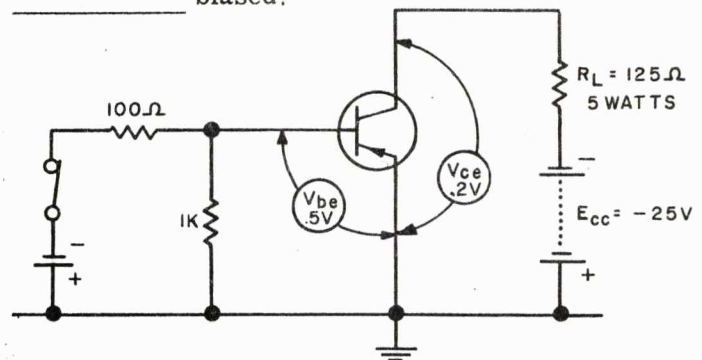
139. In the ON condition, the emitter-collector resistance is reduced to a few ohms by the strong _____ bias at the emitter-base junction.

139. forward

140. Although it is not as efficient as a mechanical switch or relay from the standpoint of ON and OFF resistance, the transistor can perform the switching operation much more rapidly. For example, switching rates of several million times a second are not uncommon. Even in slow speed applications such as control of lights, small motor, transistorized automobile ignition, etc., transistors give more uniform and reliable performance due to the absence of arcing and contact wear.

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141. Here we have a typical PNP transistor switch. With the large forward bias on the base-emitter junction, conduction is so heavy that V_{ce} drops to a level below V_{be} . Since V_{ce} is less than V_{be} , the base-collector junction is actually biased!



TYPICAL VALUES

$I_c = 80\mu A$ SWITCH OPEN
 $I_c = 0.2A$ SWITCH CLOSED
 $I = 10mA$ = CURRENT THROUGH SWITCH
 $V_{ce} = .2V$ SWITCH CLOSED
 $V_{be} = .5V$ SWITCH CLOSED
 INPUT POWER = 15 MILLIWATTS
 LOAD POWER = 5 WATTS

141. forward

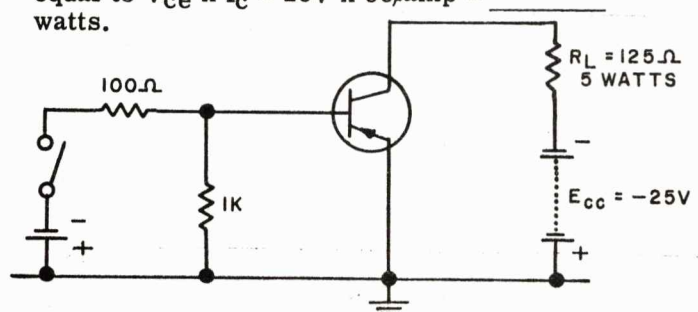
142. We will not attempt to explain here how V_{ce} can be less than V_{be} . However, a transistor operating under these conditions is said to be SATURATED. That is, in saturated operation, the base-collector junction becomes _____ biased.

142. forward

143. The symbol $V_{ce}^{(SAT)}$ is often used to denote the collector-emitter voltage of a transistor in _____ operation.

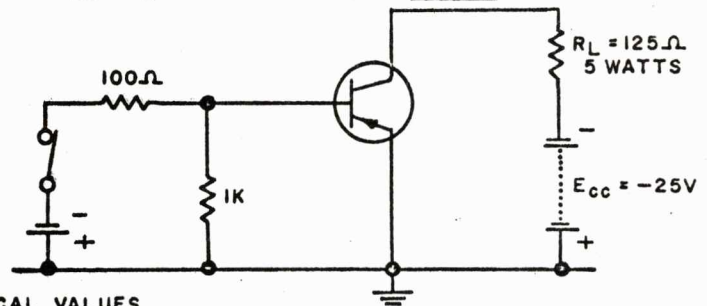
143. saturated

144. Heating in a transistor switch is quite different than in an ordinary amplifier. Using the circuit below, heating in the OFF conditions is equal to $V_{ce} \times I_c \cong 25V \times 80\mu amp \cong$ _____ watts.



144. .002

145. In the ON condition heat is equal to $V_{ce} \times I_c \cong .2V \times .2 \text{ amps} \cong$ _____ watts.



TYPICAL VALUES

$I_b = 80\mu A$ SWITCH OPEN
 $I_b = 0.2A$ SWITCH CLOSED
 $I = 10mA$ CURRENT THROUGH SWITCH
 $V_{ce} = .2V$ SWITCH CLOSED
 $V_{be} = .5V$ SWITCH CLOSED
 INPUT POWER = 15 MILLIWATTS
 LOAD POWER = 5 WATTS

145. .04

146. If we calculate heat during the switching operation, we find, for example, that when $V_{ce} = 12V$, $I_c = 0.1 \text{ amp}$. Therefore, heat = $12V \times .1 \text{ amp} = 1.2 \text{ watts}$. If $V_{ce} = 6V$ and $I_c = .15 \text{ amps}$, heat = $0.9W$. Likewise, when $V_{ce} = 18V$ and $I_c = .05 \text{ amps}$, heat = $0.9W$. So we see the heat developed during switching is much _____ than during ON or OFF periods.

146. greater, larger, etc.

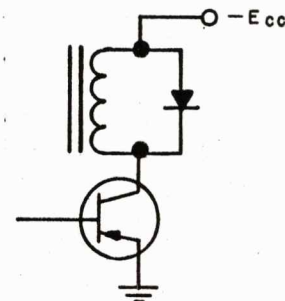
147. The switching time is usually extremely short (a few microseconds at most) compared to ON or OFF time. Therefore, the average heat dissipation, for a given maximum I_c is much _____ in a switching circuit than in an amplifier.

147. less

148. To put it another way, a given transistor can handle much _____ current in a switching circuit than in an amplifier.

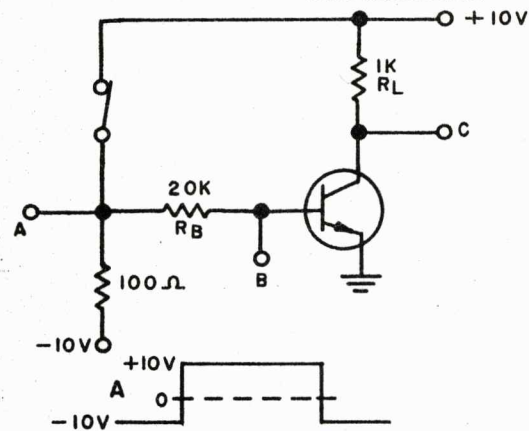
148. more

149. When switching inductive loads, the transistor must be protected from destructive high energy transients. This can be done by shunting the load with an appropriate _____



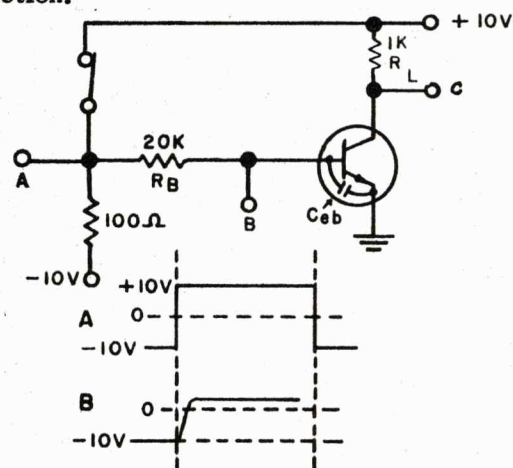
149. diode

150. Now let's consider the transient response (not to be confused with destructive transients) of a typical transistor switching circuit. When the switch is closed and opened, the resulting waveform at point A is a _____ wave.



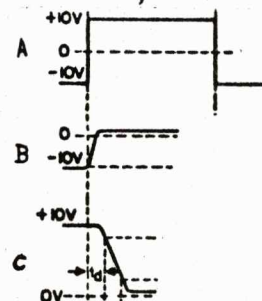
150. square

151. The waveform at point B, however, does not follow exactly the waveform at point A. When the switch is closed it takes a finite time for the emitter-base capacitance to charge through R_B in order to _____ bias the emitter junction.



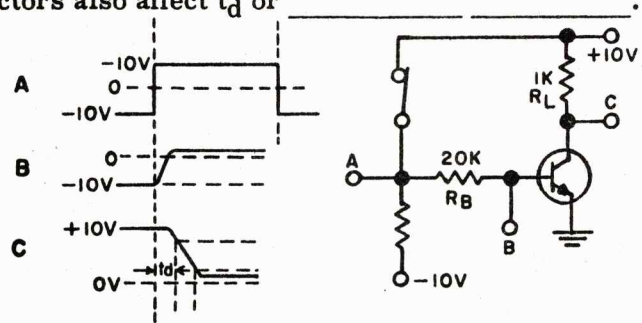
151. forward

152. The time required for I_C to rise (voltage at point C to fall) 10% of its ultimate value is called DELAY TIME, abbreviated _____.



152. t_d

153. The time required for the emitter current to diffuse across the base region, and other factors also affect t_d or

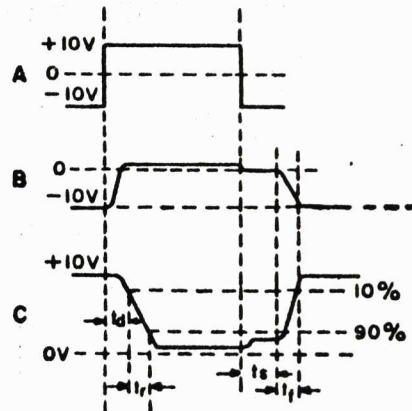


153. delay time

154. Delay time can be reduced by several means, including _____ (increasing/decreasing) the value of R_B and _____ (increasing/decreasing) the OFF bias voltage.

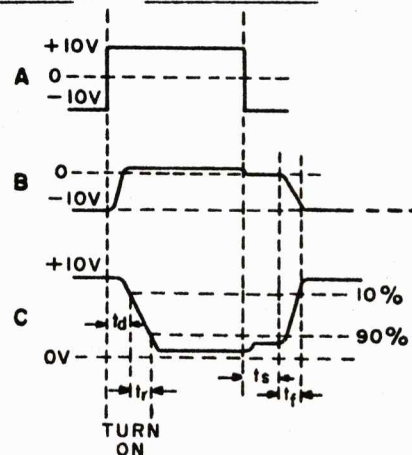
154. decreasing --
decreasing

155. The time required for I_C to rise (V_C to fall) from 10% to 90% of its ultimate value is called RISE TIME, abbreviated _____.



155. t_r

156. The total time from the closing of the switch to 90% of ultimate V_C is referred to as TURN-ON TIME. Turn-on time is equal to _____ plus _____.



156. delay time (or t_d) --
rise time (or t_r)
(or vice versa)

157. Once V_C reaches the 90% point, the transistor is pretty well into saturation. In saturation, remember, the collector becomes _____ biased.

157. forward

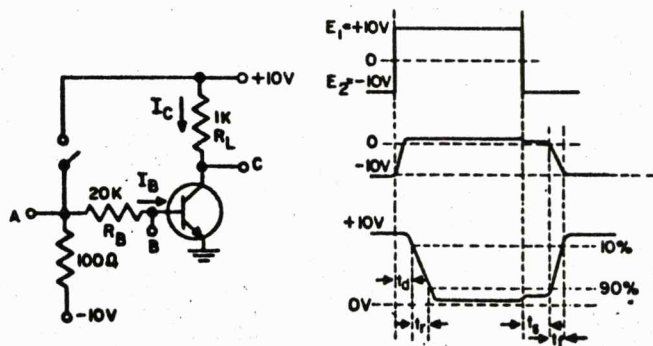
158. The collector now begins emitting carriers due to the _____ bias.

158. forward

159. Some of these carriers, emitted by the _____, become stored in the base region and, in some cases, in the collector region.

159. collector

160. When the switch is opened, these carriers must be removed before the emitter-base junction can return to _____ bias.



160. reverse

161. The time required for the stored carriers to dissipate and V_C to drop to the 90% level is the STORAGE TIME, abbreviated _____.

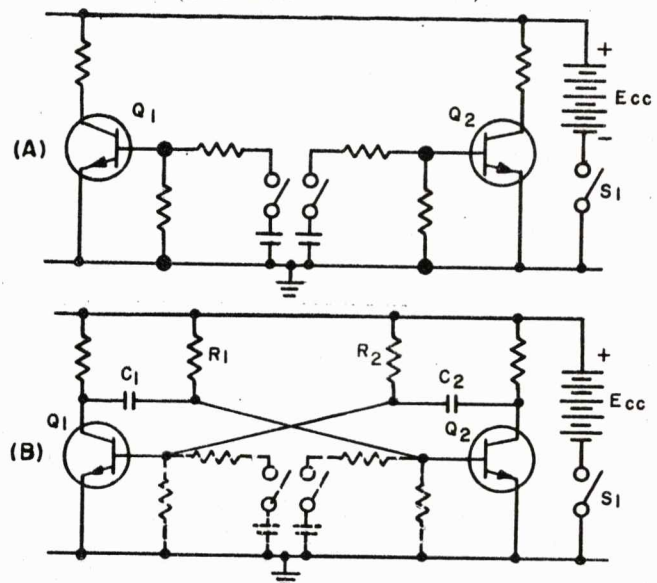
161. t_s

162. Finally the voltage at point C rises to the original +10V. The time required to traverse the 90% to 10% region is the FALL TIME, abbreviated _____.

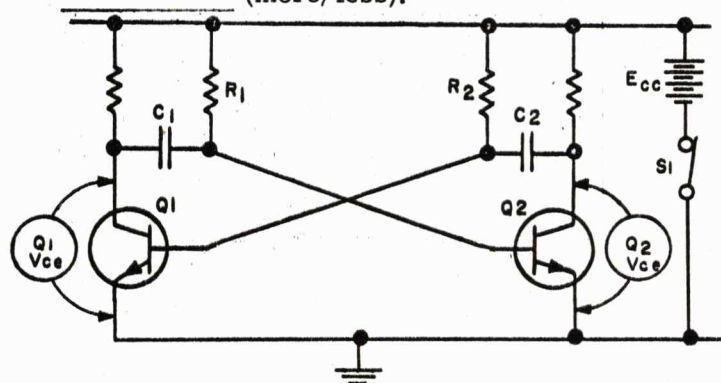
162. t_f

163. In diagram (A) we have two saturated switching circuits placed back to back, or perhaps base to base. By substituting C_1 , C_2 , R_1 and R_2 for the original control components in diagram (B), each transistor now controls the other in an oscillatory fashion. This circuit is one form of multivibrator.

(Proceed to next frame)



164. When switch S_1 is closed, one transistor, let's say Q_1 , is bound to conduct a little more heavily than the other. Since Q_1 is conducting more heavily, its V_{ce} (collector to emitter voltage) is dropping faster than that of Q_2 . This negative going voltage is coupled through C_1 to the base of Q_2 , causing Q_2 to conduct (more/less).

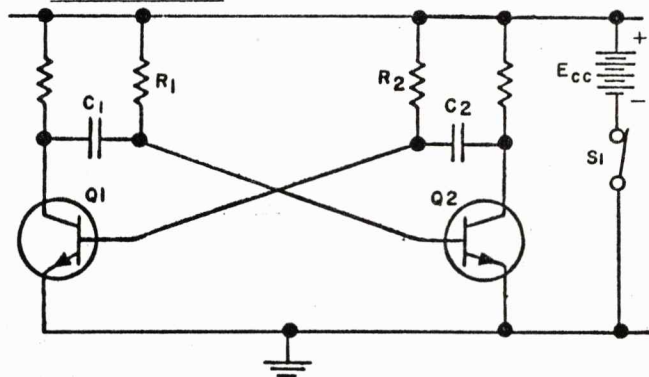


164. less

165. The lowered conduction of Q_2 results in an increase in the V_{ce} of Q_2 . This voltage rise is coupled to the base of Q_1 , causing Q_1 to _____ (increase, decrease) conduction.

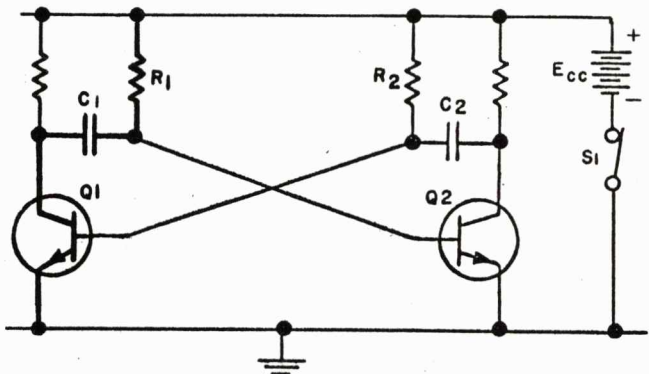
165. increase

166. This cumulative process, which takes place in a fraction of a microsecond, continues until Q_1 is saturated and Q_2 is cutoff. In this condition $Q_1 V_{ce}$ is essentially _____ (ground/ E_{cc}) and $Q_2 V_{ce}$ is essentially _____



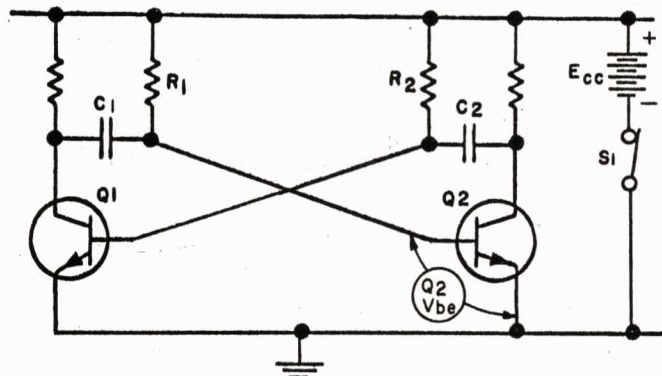
166. ground -- E_{cc}

167. With current through the transistors at a steady state, C_1 now starts to charge up through _____ and _____.



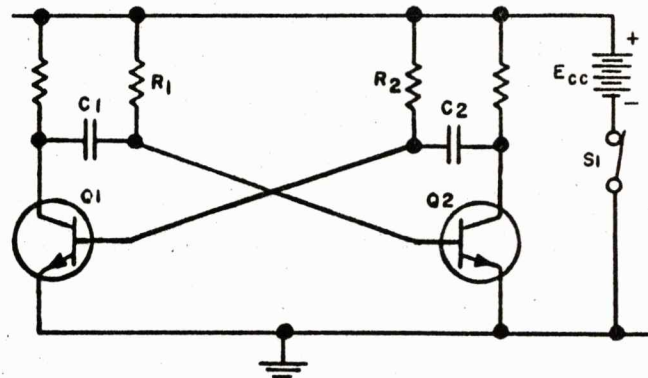
167. Q_1 -- R_1
(or vice versa)

168. As C_1 charges, $Q_2 V_{be}$ starts to rise and eventually (a few microseconds in slow speed multivibrators) Q_2 comes out of cutoff. The resulting conduction causes $Q_2 V_{ce}$ to _____.



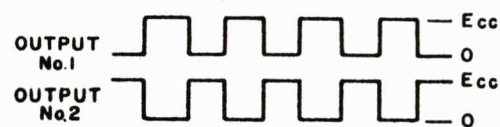
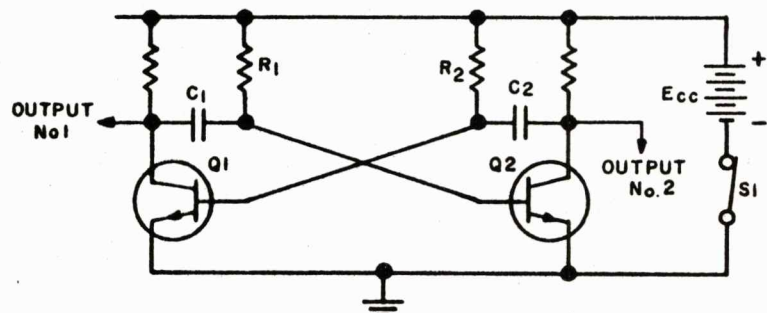
168. decrease, drop, etc.

169. This falling voltage is coupled through C_2 to the base of Q_1 , cutting off Q_1 just as Q_1 previously cutoff Q_2 . This process repeats at a rate determined by the time constants of C_1R_1 and _____.



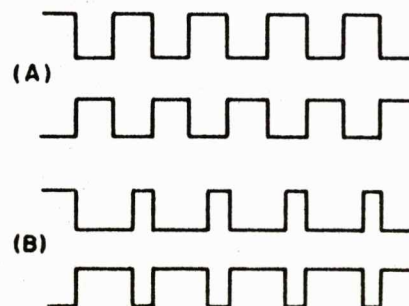
169. C_2R_2

170. Outputs may be taken from the collectors of Q_1 and Q_2 . As shown these two outputs are essentially square waves _____ out of phase with each other.



170. 180

171. If the time constants of C_1R_1 and C_2R_2 are equal, the square waves are symmetrical (A). If, however, the time constants are unequal, _____ square waves result. (B)



171. unsymmetrical

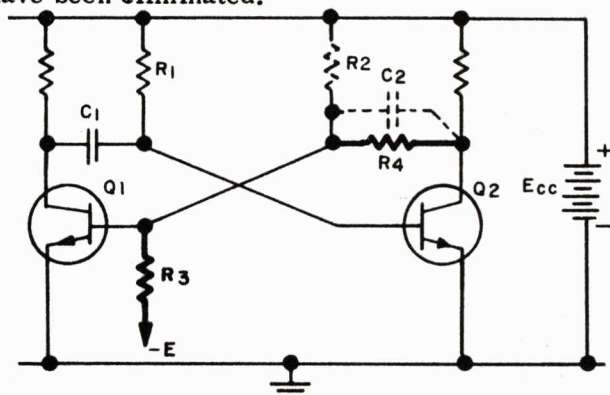
172. Because it is not stable in either of its switched states, this is called an ASTABLE multivibrator. (A means not.) And since it runs freely without any input pulses it is also called a _____-running multivibrator.

172. free-running

173. Although it will run free without input pulses, trigger pulses may be applied to either base to synchronize its operation. Thus, a positive pulse applied to a base shortly before the transistor comes out of cut-off, will trigger the transistor into _____.

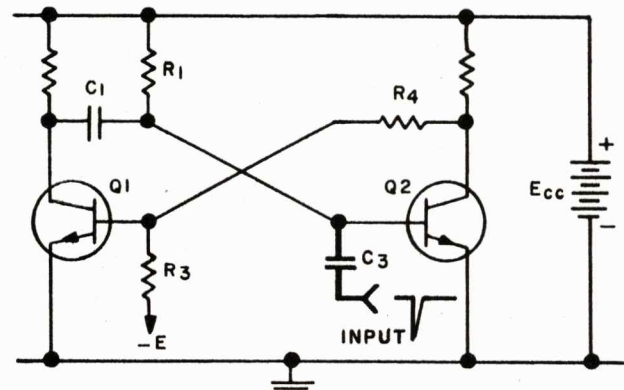
173. conduction

174. Here we have altered the coupling between Q2 collector and Q1 base. When Q1 is ON and Q2 is OFF, the discharging of C1 returns Q2 to conduction as in the free-running multivibrator. But when Q2 is ON and Q1 is OFF Q1 cannot be turned ON because _____ and _____ have been eliminated.



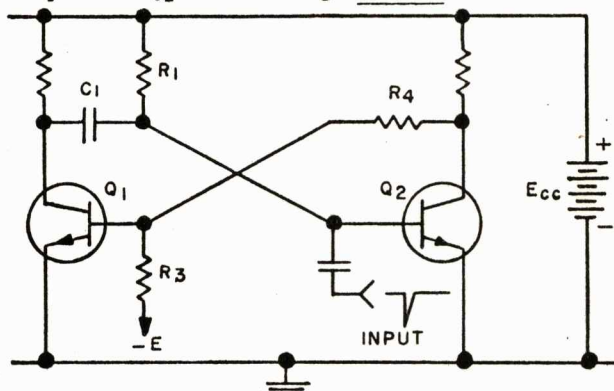
174. C₂ -- R₂

175. Switching states at this point requires a trigger. This pulse can be applied to Q2 base via C3 as a _____ pulse.



175. negative

176. In the stable state, with Q_1 OFF and Q_2 ON, the negative trigger pulse drives Q_2 base into cut-off. The rising voltage at Q_2 collector is coupled to Q_1 base through _____.



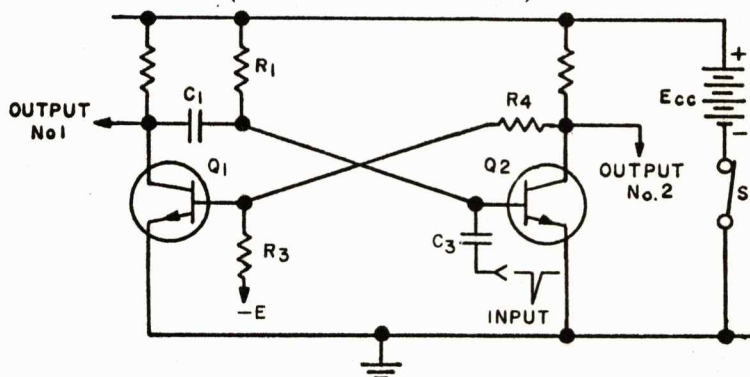
176. R_4

177. As Q_1 comes out of cut-off, Q_2 is driven into cut-off by the falling potential at Q_1 collector, which is coupled to Q_2 base through _____.

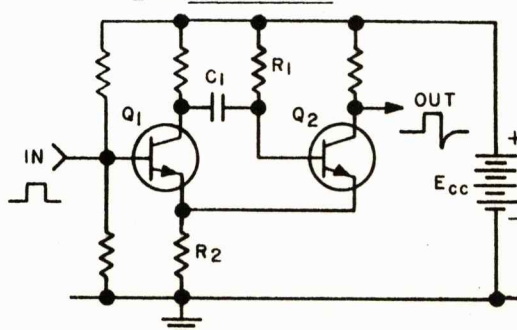
177. C_1

178. So we see that this multivibrator has one stable state (Q_1 OFF, Q_2 ON) and one unstable state (Q_1 ON, Q_2 OFF). Because it has one stable state, we call this a monostable, or one-shot multivibrator. Square wave outputs can be taken from either collector.

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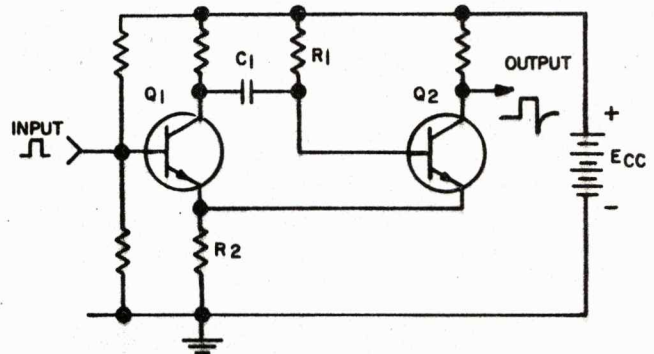


179. Here is an emitter-coupled one-shot multivibrator. In the stable state Q_1 is _____ (ON/OFF) and Q_2 is _____.



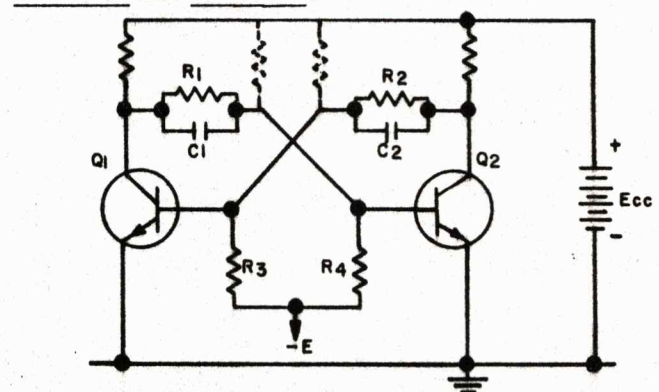
179. OFF -- ON

180. The positive pulse turns on Q_1 which in turn cuts off Q_2 . C_1 then discharges to bring Q_2 out of cut-off. When Q_2 starts to conduct and draws current through R_2 , Q_1 becomes biased by the resulting IR drop across R_2 , and returns to the stable state.



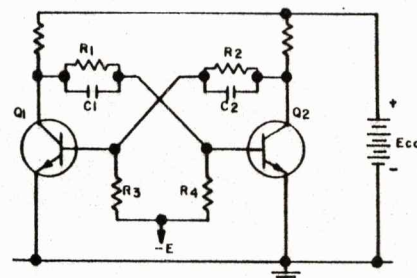
180. reverse

181. This circuit is similar to our astable multivibrator except that: 1) R_1 and R_2 are connected to the collectors Q_1 and Q_2 instead of to E_{cc} ; and, 2) the bases are returned to $-E$ through _____.



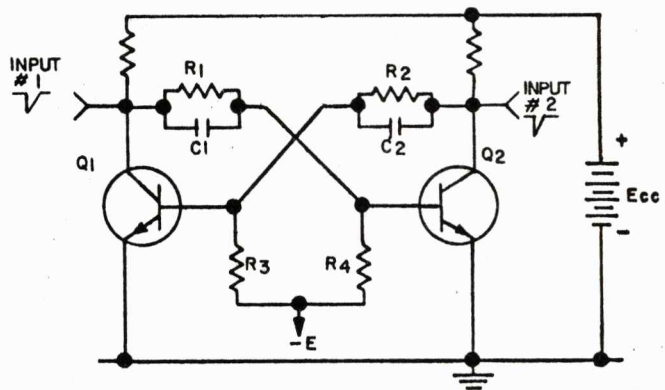
181. R_3 -- R_4
(or vice versa)

182. Since there is no way to discharge C_1 or C_2 towards E_{cc} to bring the base of an OFF transistor out of cut-off, this circuit will not change state without the application of external trigger pulses.



(Proceed to next frame)

183. Here we see negative pulses applied to the collector of Q_1 and Q_2 . Such a pulse at the collector of an ON transistor is shunted to ground by the low internal resistance and has no effect. At the collector of an OFF transistor, the pulse sees a high shunt resistance and is passed through the capacitor to the _____ of the ON transistor.



183. base

184. The negative pulse at the base of the ON transistor, say Q_2 , cuts that transistor off. The rising voltage at Q_2 collector is then coupled through C_2 to turn Q_1 _____, thus completing a change of state.

184. ON

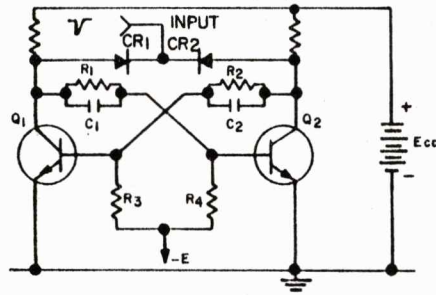
185. The astable multivibrator, remember, is not stable in either state; the monostable multivibrator is stable in one state. This multivibrator is called bistable because it is stable in _____ states.

185. 2 or both

186. And because it seems to "flip" states with one pulse and "flop" back at the next pulse, the bistable multivibrator is referred to as a "flip-flop."

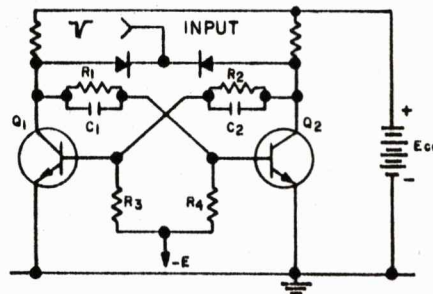
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187. By adding two diodes to this bistable multivibrator, we can use one trigger input point instead of two. Let's assume that Q_1 is ON and Q_2 is OFF. A trigger pulse (negative) at the input point has little tendency to go through CR_1 because Q_1 is ON and Q_1 collector is at essentially _____ potential.



187. 0 volts or ground

188. However, the potential of Q_2 collector is essentially $+E_{cc}$. Therefore, the negative pulse passes through CR_2 to the collector of Q_2 . Since Q_2 is OFF and represents a high impedance, the pulse passes through C_2 to Q_1 base and turns Q_1 _____.

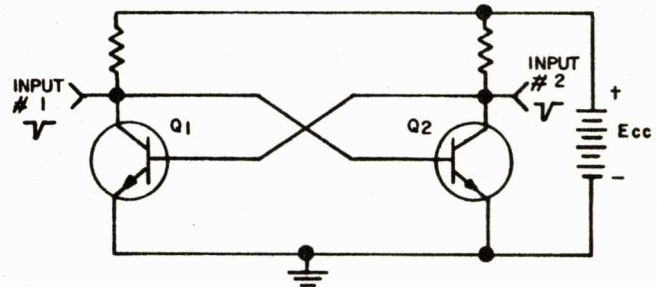


188. OFF

189. Because CR_1 and CR_2 steer the trigger pulse to the proper part of the circuit, they are called _____ diodes.

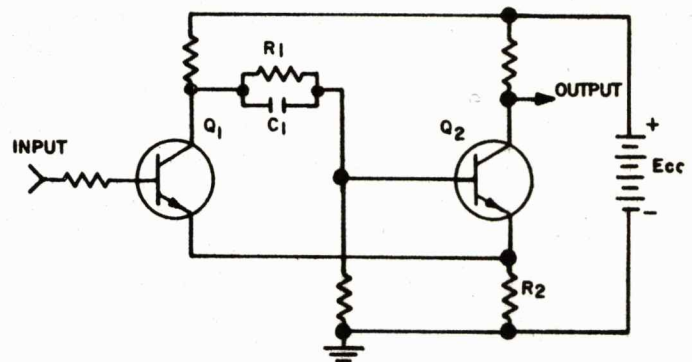
189. steering

190. A DCTL (Direct Coupled Transistor Logic) flip-flop is shown here. Operation is very similar to that of the conventional flip-flop. With Q_1 OFF and Q_2 ON, a negative pulse at Input #1 turns Q_2 OFF. The rising Q_2 V_{ce} then turns Q_1 _____.



190. ON

191. This circuit is one version of a Schmitt trigger. It is a regenerative circuit. Its state depends upon the relation of the input voltage to the emitter potential of Q_1 , as determined by R_2 . When the input voltage is lower than Q_1 emitter potential, Q_1 is _____ (ON/OFF) and Q_2 is _____.



191. OFF -- ON

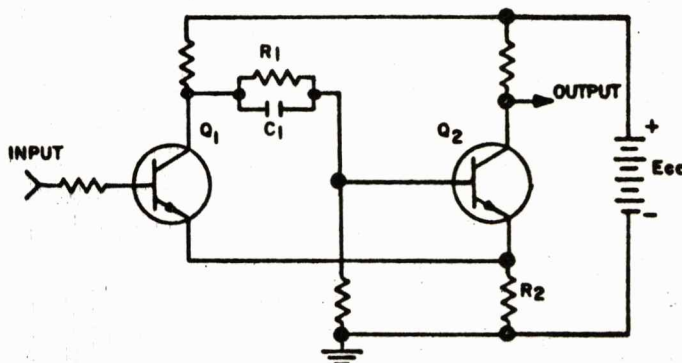
192. As the input voltage increases, a critical value is reached at which Q_1 begins to conduct. The decreasing Q_1 V_{ce} , coupled through C_1 begins to _____ conduction in Q_2 .

192. decrease

193. The decreased conduction of Q_2 and the resulting decrease in IR drop across R_2 cause a regenerative _____ in Q_1 conduction.

193. increase

194. The regenerative action causes a very rapid change of state (Q_1 ON, Q_2 OFF). If the input voltage now decreases, a point is reached where conduction in Q_1 starts to _____.

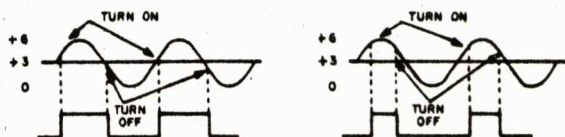


194. decrease

195. The increasing Q_1 V_{ce} and Q_2 V_{be} , again aided by regenerative action, turn Q_2 _____.

195. ON

196. The values of input voltage at which the Schmitt trigger changes state are determined by bias and other circuit operating parameters. In the illustration below we see two different outputs produced from the same sine wave input with two different values of turn-on and turn-off voltage. Note that the turn-off voltage is _____ than the turn-on voltage.



196. less, lower, etc.

197. Because its output depends on the instantaneous value of the input voltage regardless of its shape, and because its strong regenerative action gives extremely short rise time and fall time, the Schmitt trigger is useful for waveform restoration, signal level shifting, squaring of various waveforms, and for DC level detection.

This completes Semiconductor Circuits.

VOLUME II
COUNTING SYSTEMS

1. Before learning binary arithmetic, most students ask themselves this obvious question, "What's wrong with the everyday decimal system of arithmetic that requires that I learn the binary system of arithmetic?"

The answer is that there is nothing wrong with the decimal system as such. It works fine for everyday use such as handling money and for figuring various problems. Mechanical devices work well with the decimal system, witness the adding machines, comptometers, cash registers, etc. However, most of us live in an electronics world. Here decimal arithmetic creates problems. We will first look into some of the problems created by use of decimal arithmetic and then learn how they are overcome by the use of binary arithmetic.

(Proceed to next frame)

2. Imagine if you wish electronic systems that could generate and detect either ten amplitude levels of voltage and/or current; or trains of pulses ranging from one to ten. Of course these can and have been devised, but they are not simple circuits.

Most of the original electronic circuits used for counting by decimal, or tens, required feedback loops, and as a result these circuits were anything but simple. They were relatively _____.

2. complex or complicated
(or equivalent word)

3. One of the reasons for the complexity of electronic circuits using the decimal system is because the decimal system is based upon ten digits.

These are: 0-1- _____
_____.

3. 0-1-2-3-4-5-6-7-8-9

4. To ease the requirements of electronic circuits used for arithmetic purposes (computers, etc.) we can use lesser-known systems of arithmetic based upon values less than ten.

An example would be a system based upon the number eight, called an octal system. An octal system works with only eight digits.

These are: 0-1-_____.

(Fill in the remaining digits.)

4. 0-1-2-3-4-5-6-7

5. Let's keep reducing the number of digits available to us. Imagine a limit of five digits (called quinary). We would then list the following five digits. _____

5. 0-1-2-3-4

6. Fine, but that is still too many digits for our requirements. Assume a limit of two digits. These would be _____ and _____.

6. 1 -- 0
or
0 -- 1

7. The prefix qui stands for five, and quinary stands for arithmetic based on the number 5. The prefix tri stands for three, and trinary represents arithmetic based upon the number 3.

The prefix bi stands for two, and arithmetic based on the number 2 is called _____.

7. binary

8. Binary arithmetic is based on the number _____ and can be represented by the two digits _____ and _____.

8. 2 -- 0 -- 1
or
2 -- 1 -- 0

9. Let us discuss some of the ways in which we can develop binary arithmetic symbols in electronic circuits. Assume two different voltage levels, 0V and +1V.

Your task is to assign one of the binary digits to the 0V level and the other binary digit to the +1V level.

+1V = _____
0V = _____

9. 1 or 0
0 or 1

10. 0 -- 1
(or vice versa)

10. Did you carefully note that the response to the preceding frame stated that you could indicate either voltage level with the 0 or 1 digit?

This brings up an important point; unfortunately there is no industry-wide standard. Depending upon the choice of the manufacturer, or the individual engineer, the choice of a binary digit for a zero voltage level could be either _____ or _____.

11. What other ways are there to electronically represent the binary symbols of 0 and 1?

Many. Let us discuss the more well-known methods. A relay, open or closed. A flip-flop, conducting or non-conducting. Various voltage levels, zero or plus, zero or minus, plus or minus, different values of plus, different values of minus.

For recognition of the binary symbols of 0 and 1, presence or absence is the most often used method. For instance, presence or absence of a hole in a punched card or paper tape. Another method is the presence or absence of a magnetic field, such as on magnetic tape.

We hope you are beginning to see some of the many advantages of the use of binary symbols over decimal symbols in electronic circuits.

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12. Before going too far let us clear up a possible source of confusion. The decimal system is based upon the number 10. The base of the system being the number 10, it is referred to as the "base 10." However, the fundamental number, or base, of the system in use could also be called the "root" or "radix." Should you see those words used, they are also correct and have the same meaning as the word "base."

The decimal system uses the number 10 as its root, or radix. Another way to express this is to say that the decimal system uses the base 10. For the binary system, we would say it uses the base _____.

12. 2

13. We should now have an appreciation of the problems of using decimal symbols and the ease of using binary symbols in electronics. The next step is to review decimal arithmetic. This will act as an introduction to learning binary arithmetic.

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14. To help us learn the subject it is best to review arithmetic as expressed by exponents or powers. There are three rules used in expressing numbers by powers. The first one is simple, it is:

"Any number expressed to the power of 0 is equal to 1."

For example, the base 10 to the power of 0, (written 10^0), equals 1. The base 2 to the power of 0, (written 2^0), equals _____.

14. 1

15. The second of the simple rules used in expressing exponents is:

"A number expressed to a power of 1 is equal to the number itself."

For example, the base 2 to the power of 1, written 2^1 , is equal to 2 itself.

This means that 10^1 is equal to _____.

15. 10

16. As a reminder:

The base 10 to the power of 0 (10^0) = _____.
The base 2 to the power of 1 (2^1) = _____.

16. $10^0 = 1$
 $2^1 = 2$

17. The last rule is: "For powers of 2 or more, the number used in the base is multiplied by itself by the number of times expressed in its power."

Sounds impressive, but if we examine it closely we see that it is relatively simple. In the decimal system we use the base 10. The base 10 to the power of 2 would be a good example to illustrate the simplicity of the rule.

The number used is 10, multiplied by itself the number of times expressed in its power, which is 2, and it is written as 10×10 . Thus $10^2 = 10 \times 10$.

The value of 10^3 is written as _____.

17. $10 \times 10 \times 10$

18. The value of 10^2 , written as 10×10 , is equal to 100. The value of 10^3 , written as $10 \times 10 \times 10$, is equal to _____.

18. 1000

19. Try these examples as an exercise in exponents, or powers, of the base 10.

10^5 is written as _____,
and is equal to _____.

10^7 is written as _____,
and is equal to _____.

19. $10^5 = 10 \times 10 \times 10$
 $\times 10 \times 10 = 100,000$

$10^7 = 10 \times 10 \times 10 \times 10$
 $\times 10 \times 10 \times 10$
 $= 10,000,000$

20. Now let us create a table illustrating the values of exponents of the base 10, the exponents to be from 0 to 9. (If required, use a piece of scrap paper or the back of the preceding page for any figuring.)

$10^0 =$ _____
 $10^1 =$ _____
 $10^2 =$ _____
 $10^3 =$ _____
 $10^4 =$ _____

$10^5 =$ _____
 $10^6 =$ _____
 $10^7 =$ _____
 $10^8 =$ _____
 $10^9 =$ _____

- 20.
- | | | |
|--------|---|---------------|
| 10^0 | = | 1 |
| 10^1 | = | 10 |
| 10^2 | = | 100 |
| 10^3 | = | 1,000 |
| 10^4 | = | 10,000 |
| 10^5 | = | 100,000 |
| 10^6 | = | 1,000,000 |
| 10^7 | = | 10,000,000 |
| 10^8 | = | 100,000,000 |
| 10^9 | = | 1,000,000,000 |

21. Another way of illustrating the table is shown below. Note that the least significant value is to the right.

10^9	10^8	10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1 000 000

(Proceed to next frame)

22. Using the base 10 to any power we can express any decimal number. As shown below the number 3 can be expressed by placing it under the column 10^0 .

10^9	10^8	10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1 000 000

3

The decimal value of 3 can be expressed as 3×10^0 , the equivalent of writing it as 3×1 . The decimal value of 5 can be expressed as _____, and written as _____.

22. 5×10^0
 5×1

23. Let us proceed from a single number to a larger number such as 24. To help us express the decimal number by powers we again use the table of powers of 10. Placing the number 24 with its least significant digit at the right we have:

10^9	10^8	10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1 000 000

2 4

We can break it down to:

$$2 \times 10^1 = 2 \times 10 = 20$$

$$4 \times 10^0 = 4 \times 1 = 4$$

24

Try this method of expressing decimal numbers by the powers of 10, using the number 46.

$$\begin{array}{rcl}
 23. & 4 \times 10^1 & = 4 \times 10 = 40 \\
 & 6 \times 10^0 & = 6 \times 1 = 6 \\
 & & \hline
 & & 46
 \end{array}$$

24. As an exercise in expressing decimal numbers by powers of 10, try the following.

10^9	10^8	10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1 000 000

Numbers 15 and 88.

$$\begin{array}{rcl}
 24. & 1 \times 10^1 & = 1 \times 10 = 10 \\
 & 5 \times 10^0 & = 5 \times 1 = 5 \\
 & & \hline
 & & 15
 \end{array}$$

$$\begin{array}{rcl}
 & 8 \times 10^1 & = 8 \times 10 = 80 \\
 & 8 \times 10^0 & = 8 \times 1 = 8 \\
 & & \hline
 & & 88
 \end{array}$$

25. You should have the idea now, any decimal number can be expressed by powers of 10. The number 74,639 would be expressed as follows:

10^9	10^8	10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1000 000 000	100 000 000	10 000 000	1 000 000

$$\begin{array}{rcl}
 & & 7 & 4 & 6 & 3 & 9 \\
 7 \times 10^4 & = & 7 \times 10 \times 10 \times 10 \times 10 & = & 70,000 \\
 4 \times 10^3 & = & 4 \times 10 \times 10 \times 10 & = & 4,000 \\
 6 \times 10^2 & = & 6 \times 10 \times 10 & = & 600 \\
 3 \times 10^1 & = & 3 \times 10 & = & 30 \\
 9 \times 10^0 & = & 9 \times 1 & = & 9 \\
 & & & & \hline
 & & & & & & 74,639
 \end{array}$$

You try it with the number 5,743.

$$\begin{array}{rcl}
 25. & 5 \times 10^3 & = 5 \times 10 \times 10 \times 10 = 5,000 \\
 & 7 \times 10^2 & = 7 \times 10 \times 10 = 700 \\
 & 4 \times 10^1 & = 4 \times 10 = 40 \\
 & 3 \times 10^0 & = 3 \times 1 = 3 \\
 & & \hline
 & & 5,743
 \end{array}$$

26. Before discussing powers in the binary system, this is a reminder that binary arithmetic is based upon the number 2 and is represented by the digits 0 and 1.

(Proceed to next frame)

27. The rules used in expressing numbers by exponents, or powers, are the same regardless of the base. The first rule stated that a number expressed to the power of 0 is equal to 1. In binary arithmetic the base (also called the root or radix) is 2.

The expression 2 to the power of 0 is written _____ and equals _____.

27. $2^0 = 1$

28. $2^1 = 2$

29. $2 \times 2 \times 2$

30. $2^2 = 4$ -- $2^3 = 8$

31. $2^0 = 1$ $2^5 = 32$
 $2^1 = 2$ $2^6 = 64$
 $2^2 = 4$ $2^7 = 128$
 $2^3 = 8$ $2^8 = 256$
 $2^4 = 16$ $2^9 = 512$

28. The next rule stated that a number expressed to a power of 1 is equal to the number itself. Therefore, 2 to the power of 1 is written _____ and equals _____.

29. The third and last rule was that for powers of 2 or more the number used in the base is multiplied by itself by the number of times expressed in the power. This imposing statement merely means that 2^2 can be written as 2×2 . The value of 2^3 is written as _____.

30. The value of $2^0 = 1$, $2^1 = 2$, $2^2 =$ _____ and $2^3 =$ _____.

31. Once again, let us make a table illustrating the values of exponents, but this time of the base 2. As before the exponents will be from 0 to 9. (If required, use a piece of scrap paper or the back of the preceding page for any figuring.)

$2^0 =$ _____	$2^5 =$ _____
$2^1 =$ _____	$2^6 =$ _____
$2^2 =$ _____	$2^7 =$ _____
$2^3 =$ _____	$2^8 =$ _____
$2^4 =$ _____	$2^9 =$ _____

32. Again we will illustrate the table with the least significant figure to the right.

2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
512	256	128	64	32	16	8	4	2	1

(Proceed to the next frame)

33. Binary arithmetic using the base 2 requires only the digits 0 and 1. Here is how the digits are used.

To show that a value exists we use a 1; where a value does not exist we use a 0. For example:

Try this:

The value of 1. The value of 2. The value of 3

2^2	2^1	2^0
4	2	1
	0	1

2^2	2^1	2^0
4	2	1
	1	0

2^2	2^1	2^0
4	2	1

33. 1 1

34. Here are some additional examples.

The value of 5.

2^3	2^2	2^1	2^0
8	4	2	1
	1	0	1

The value of 6.

2^3	2^2	2^1	2^0
8	4	2	1
	1	1	0

Note carefully that more digits are required to express a number in binary than in decimal. However, it is the value of the digits (0 and 1) that we are interested in.

Try these:

The value of 4.

2^4	2^3	2^2	2^1	2^0
16	8	4	2	1

The value of 10.

2^4	2^3	2^2	2^1	2^0
16	8	4	2	1

34. 100 1010

35. From memory: give the decimal values of the following binary expressions.

10 = _____
 101 = _____
 110 = _____

35. $10 = 2$
 $101 = 5$
 $110 = 6$

36. Let us try expressing a larger number in binary.
 For example, 165.

2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
512	256	128	64	32	16	8	4	2	1

The number 165 expressed in exponents of the base 2 become:

$$\begin{array}{r}
 2^7 - 128 \\
 2^5 - 32 \\
 2^2 - 4 \\
 2^0 - 1 \\
 \hline
 165
 \end{array}$$

The binary expression for the number 165 is _____.

36. 10100101

37. There is an orderly progression of binary symbols starting from the number 1. To see this we can easily build a table starting with the number 1.

You fill in this portion.

2^4	2^3	2^2	2^1	2^0	
16	8	4	2	1	#
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9

2^4	2^3	2^2	2^1	2^0	
16	8	4	2	1	#
					10
					11
					12
					13
					14
					15
					16
					17
					18
					19

- 37.

2^4	2^3	2^2	2^1	2^0	
16	8	4	2	1	#
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19

38. Take the number 22, express it by exponents of the base 2, and by its binary expression.

(A suggestion, if needed, construct the binary table as shown in the preceding pages.)

38.

2^4	2^3	2^2	2^1	2^0
16	8	4	2	1

$$\begin{array}{r}
 2^4 - 16 \\
 2^2 - 4 \\
 2^1 - 2 \\
 \hline
 22
 \end{array}$$

10110

39. 10101 -- 5

40. 10010 -- 5 --
1 0 0 1 0

39. The number 22 expressed in binary is 10110 and requires five binary digits. The binary expression for the number 9 is 1001, requiring four binary digits, called bits.

The number 21 is expressed in binary as _____ and requires _____ bits.

40. Let's try tying together some of the information we have just learned.

The number 26 expressed in binary is 11010, contains 5 bits and can be expressed as a pulse train by 1 1 0 1 0.

The number 18 expressed in binary is _____, contains _____ bits and can be expressed as a pulse train by _____.

41. It is time for us to learn how to convert a binary number to an equivalent decimal number. There are various methods but we will use one of the most popular ways. We will learn, for example, that given the binary number 10110110010, we will convert it to its decimal value of 1458.

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42. You have probably already guessed at the method used; we have been using it all along without mentioning it. Simply express each binary 1 to its power, then add their values.

For example, the binary number 101. The least significant digit is 2^0 , there is no value assigned to the next power, 2^1 , and the most significant digit is equal to 2^2 .

16	8	4	2	1
2^4	2^3	2^2	2^1	2^0
		1	0	1

$$\begin{array}{rcl}
 2^2 & = & 4 \\
 2^0 & = & 1 \\
 & = & 5
 \end{array}$$

The binary number 110 is equivalent to the decimal number _____.

42. 6

43. Another example, using a higher value, the binary number 11100100110.

1024	512	256	128	64	32	16	8	4	2	1
2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1	0	0	1	0	0	1	1	0

1024
512
256
32
4
2

1830

Convert the binary number of 1101101101 to its equivalent decimal number of _____.

43. 877

44. As an exercise: the binary number 10011001101 equals the decimal number _____.

44. 1229

45. We can change a decimal number to a binary number by a method of trial and error. However, a preferred method is to use a procedure that will give us our answer in less time, and with less probability of an error.

(Proceed to next frame)

46. In converting a decimal number to a binary number we divide the decimal number by 2, and note the remainder. Any even number divided by 2 has a remainder of 0, and an odd number divided by 2 will have a remainder of 1.

Examples: $2 \overline{) 2} \quad 0 \text{ Remainder}$

$2 \overline{) 3} \quad 1 \text{ Remainder}$

(Proceed to next frame)

47. For decimal numbers requiring division in two or more steps we keep dividing until the quotient is smaller than 2.

Example: Number 4

$$\begin{array}{r} 0 \\ 2 \overline{) 1} \quad 1 \\ 2 \overline{) 2} \quad 0 \\ 2 \overline{) 4} \quad 0 \end{array}$$

The binary number _____ is equivalent to decimal number 4.

47. 100

48. You probably did it without thinking about it, but to be sure let us point out how you take your vertical list of remainders and write them out horizontally. The bottom number goes on the right as the least significant digit and the top number goes on the left as the most significant digit.

Try this method to convert the decimal number 8 to its equivalent binary number.

48.

$$\begin{array}{r} 0 \\ 2 \overline{) 1} \quad 1 \\ 2 \overline{) 2} \quad 0 \\ 2 \overline{) 4} \quad 0 \\ 2 \overline{) 8} \quad 0 \end{array}$$

Binary 1000 equals decimal 8.

49. Let us try it with larger decimal numbers.

Example: 26

$$\begin{array}{r} 0 \\ 2 \overline{) 1} \quad 1 \\ 2 \overline{) 3} \quad 1 \\ 2 \overline{) 6} \quad 0 \\ 2 \overline{) 13} \quad 1 \\ 2 \overline{) 26} \quad 0 \end{array}$$

Binary 11010 is equal to decimal 26.

Try it with decimal number 75.

49.

	0	
2	1	1
2	2	0
2	4	0
2	9	1
2	18	0
2	37	1
2	75	1

Binary 1001011 equals decimal 75.

50. As you probably surmised, larger decimal numbers are converted the same way, we merely have more steps.

Example: 427

	0	
2	1	1
2	3	1
2	6	0
2	13	1
2	26	0
2	53	1
2	106	0
2	213	1
2	427	1

Binary 110101011 is equal to decimal 427.

Try it with decimal 374.

50.

	0	
2	1	1
2	2	0
2	5	1
2	11	1
2	23	1
2	46	0
2	93	1
2	187	1
2	374	0

Binary 101110110 equals decimal 374.

51. As an exercise convert the following decimal numbers to their equivalent binary numbers.

623 1397

51.

	0	
2	1	1
2	2	0
2	4	0
2	9	1
2	19	1
2	38	0
2	77	1
2	155	1
2	311	1
2	623	1

623 = 1001101111

1397 = 10101110101

	0	
2	1	1
2	2	0
2	5	1
2	10	0
2	21	1
2	43	1
2	87	1
2	174	0
2	349	1
2	698	0
2	1397	1

52.

A method of adding binary numbers would be to convert them to their decimal values, add them in the familiar decimal method, then re-convert the sum to a binary value.

With the use of only two digits, straight binary addition is simple. Once again we must learn some basic rules.

There are three rules, the first is easy:

$$0 + 0 = 0$$

(Proceed to next frame)

53. The next rule is also simple.

$$1 + 0 \text{ (or } 0 + 1) = 1$$

Examples:	1010	010110
	+0100	+100001
	<u>1110</u>	<u>110111</u>

Try these:	10011	101000
	+00100	+010101

53. 10111 111101

54. The last rule is: $1 + 1 = 0$ and carry 1 to the next column.

Take the least significant binary value of $+1$,
which is also the decimal equivalent of $+1$. The
decimal sum is 2, and the binary sum is 10.

To obtain the binary 10 we had to carry a 1
from the 2^0 column to the 2^1 column. Thus
we can see that every time we add a binary
 $1 + 1$, we have a sum of 0 and a carry of 1 to
the next most significant column.

As an exercise:

	101
	+001

54. 110

55. The best way to learn the application is to try
examples illustrating the various conditions
for binary addition.

	Step 1	Step 2	Step 3
An example:	11	11	11
	+01	+01	+01
	<u>0</u>	<u>10</u>	<u>10</u>
Carry	1	1	11
			<u>0</u>

In the example shown, for the first step we
add the least significant digits of $1 + 1$. We
put down a 0 and carry a 1 to the next most
significant column. Note that the carry is
placed below. The second step is to add the
 $1 + 0$ of the next column, and we place the
answer of 1 below the line. The third step is
to add the sum of 1 plus the carry of 1, to
produce a final sum of 0 with a carry of 1.
The answer to this example is the binary sum
of _____.

55. 100

56. Another example:

$$\begin{array}{r}
 101 \\
 +111 \\
 \hline
 010 \\
 \text{Carry} \quad 111 \\
 \hline
 10
 \end{array}$$

In this example, for the least significant digits of $1 + 1$ we put down a 0 and carry a 1. In the next step we add the digits of $0 + 1$, place the answer of 1 below the line, which is then added to the carry for a final sum of 0 and a carry of 1. For the final column we add the digits of $1 + 1$ for a sum of 0 and a carry of 1; to the sum of 0 we add the carry from the preceding column, for a final sum of 1. This procedure gives us a binary sum of 1100.

Try these

$$\begin{array}{r}
 10110 \\
 +11011 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 1011011 \\
 +0110101 \\
 \hline
 \end{array}$$

56. 110001 10010000

57. The preceding examples and problems consisted of adding no more than two binary values. To add three or more binary values, the procedure is identical.

Example:

	Step 1	Step 2	Step 3
	11	11	11
	01	01	01
	10	10	10
	10	10	10
	<u>0</u>	<u>10</u>	<u>10</u>
Carry	1	11	111
		10	10
			<u>0</u>

Step 1: $1 + 1 = 0$ and carry 1, $0 + 0 = 0$, $0 + 0 = 0$.

Step 2: $1 + 0 = 1$, $1 + 1 = 0$ and carry 1, $0 + 1 = 1$, $1 + \text{carry } 1 = 0$ and carry 1.

Step 3: (Add both carries) $1 + 1 = 0$ and carry 1. The sum of the example is 1000.

Try these:

$$\begin{array}{r}
 11 \quad 10 \\
 01 \quad 11 \\
 10 \quad 11 \\
 \hline
 01 \quad 10
 \end{array}$$

57. 111 1010

58. As an exercise:

Add:	10110	110011
	11010	010100
	10100	100011
	<u>01101</u>	<u>110110</u>

58. 1010001 10100000

59. To multiply binary numbers we find that the beginnings are identical to multiplication of decimal numbers. For example:

$$\begin{array}{r} 111 \\ \times 101 \\ \hline 111 \\ 000 \\ 111 \\ \hline \end{array}$$

In binary multiplication we multiply just as in decimal multiplication, but each column is added by binary addition. The answer to the example shown is _____.

59. 100011

60. There is nothing else to say about multiplication of binary numbers. We multiply just as in decimal arithmetic, but we add the columns with binary addition.

As an exercise, do the following problems.

1011	11011
<u>x0110</u>	<u>x00111</u>

60. 1000010 10111101

61. The next step is learning to subtract binary numbers, which is similar to subtraction of decimal numbers.

With the use of only two digits, binary subtraction again provides us with three situations to remember. The first one, if we take one from one (-1) the remainder is _____.

61. 0

62. The next step in binary subtraction is also similar to decimal subtraction.

Taking nothing from one (1-0) the remainder is _____.

62. 1

63. With those two simple rules for binary subtraction we should be able to do the following examples.

$$\begin{array}{r} 111 \\ -010 \\ \hline \end{array} \quad \begin{array}{r} 101 \\ -001 \\ \hline \end{array} \quad \begin{array}{r} 1101 \\ -0101 \\ \hline \end{array}$$

63. 101 100 1000

64. To subtract 1 from 0 we have to borrow and carry. For example:

	Step 1	Step 2	Step 3
10	10	10	10
-01	-01	-01	-01
—	<u>1</u>	Carry 1 <u>1</u>	Carry 1 <u>01</u>

Step 1: To subtract 1 from 0 we borrow a 1 from the next most significant column and place it under the line as the remainder.

Step 2: We must add a carry to the column from which we borrowed.

Step 3: Subtracting the values in the next column: 1-0 equals 1, from this remainder of 1 we subtract the carry of 1: 1-1 equals 0.

Try these:

$$\begin{array}{r} 11010 \\ -00101 \\ \hline \end{array} \quad \begin{array}{r} 10101 \\ -01011 \\ \hline \end{array}$$

64. 10101 01010

65. Let us stress the step where we add a carry to the next most significant column from which we borrowed.

Example: Step 1 Step 2 Step 3 Step 4

110		110	110	110	110
-011		-011	-0 1 1	-0 1 1	-0 1 1
—	Carry	1	1 1	1 1	1 1
		1	1	11	011

- Step 1: 0-1, borrow 1, carry 1.
 Step 2: We must add the subtrahend (number being subtracted) and the carry. 1+1 equals 0 and carry. To indicate zero we have put a line through each 1.
 Step 3: Subtracting, 1-0 equals 1.
 Step 4: Subtracting, 1-0 equals 1; from the remainder of 1 subtract the carry, 1-1 equals 0.

Try this example: 101010
 -001111

65. 011011

66. There's no way out of it; the best way to learn is still to try different examples.

Try these: 110001011
 -000110101

 1101101101
 -0110010110

66. 101010110 0111010111

67. It is difficult to count backwards in electronic circuits. To overcome this difficulty we can use a method of subtraction that permits us to employ addition. This method is called "complementing." Complementing has often been used as a method of "proving" a subtraction problem.

To help us understand complementing we will first illustrate the method using decimal arithmetic, then binary arithmetic.

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68. A definition of the word complement is "the quantity needed to make a thing complete." In our case the thing we are making complete is a number. To make a decimal number complete (complementing the number) is to add to it the number required to make its value 10.

The complement of 0 is 10, of 1 it is 9, of 2 it is 8, of 3 it is 7.

The complement of 6 is ____, and of 9 it is ____.

68. 4 1

69. Complementing by adding to a number to make its value ten is called "tens" complement. As we just noted, every value between 0 and 9 has a tens complement that makes it complete.

Carefully note that when we complement a value to make a tens complement we are raising it by one power. A value of 4 is actually 4×10^0 . The complement of 4 is 6, the total being 10^1 . We raised the value one power when we went from 10^0 to ____.

69. 10^1

70. Here's why we stressed the fact that we raised the value one power. To subtract 3 from 8 leaves 5. But let us assume that we cannot subtract, we can only complement and add. The problem is still the same:

$$\begin{array}{r} 8 \text{ Minuend} \\ -3 \text{ Subtrahend} \\ \hline \end{array}$$

The tens complement of the subtrahend of 3 is 7. Add the complement of 7 to the minuend of 8 for a total of 15. In adding we increased our values from a power of 10^0 to the power of 10^1 . To remove this added power is extremely simple, drop the value of 1 in the column that represents the added power. This means our answer will be the number left standing, which is ____.

70. 5

71. Let's do that again, this time with different values.

$$\begin{array}{r} 9 \text{ Minuend} \\ -6 \text{ Subtrahend} \\ \hline \end{array}$$

The tens complement of the subtrahend 6 is 4. Add the complement of 4 and the minuend of 9, total = 13. Drop the added power, 13. The remainder is 3.

Try it with these values:

$$\begin{array}{r} 7 \\ -1 \\ \hline \end{array}$$

71. The complement of 1 is 9, added to 7, totals 16. Drop the power, 16. Remainder is 6.

72. The method, and results, are the same when we complement with larger values. For example:

$$\begin{array}{r} 33 \\ -16 \\ \hline \end{array}$$

The value of 16 is of course larger than 10, to find its complement we use 100.

The tens complement of the subtrahend 16 is 84. Add the complement of 84 and the minuend of 33, total = 117. Again, we drop the added power, 117. The remainder is 17.

From what is shown in the example above you should be able to figure the proper tens complement and solve the following problem.

$$\begin{array}{r} 7196 \\ -2258 \\ \hline \end{array}$$

72. The complement of 2258 is 7742, added to 7196, totals 14938. Drop the power, 14938. Remainder is 4938.

73. For electronic reasons a better method is with "nines" complement. Using nines complement the steps we take in solving problems are identical, we merely add 1 to our answer.

In the nines complement the complement of 0 is 9, of 1 it is 8, of 2 it is 7, of 3 it is ____, and of 4 it is ____, etc.

73. 6 5

74. Using the nines complement we will do the same examples and problems as on the previous pages.

8 Minuend
-3 Subtrahend

The nines complement of the subtrahend 3 is 6.
Add the complement of 6 and the minuend of 8,
total = 14. Drop the added power, ~~14~~.
Add 1 to the 4, the remainder is 5.

Try it with the values of 9
-6

74. Remainder is 3

75. Let us review what we have just done: 9
-6

The nines complement of the subtrahend 6 is 3.
Add the complement of 3 and the minuend of 9,
total = 12. Drop the added power, ~~12~~. Add
1 to the 2; $1 + 2 = 3$.

The task of dropping the added power, and adding
1 to the answer, can be combined. Merely drop
the 1 of the added power and carry it beneath
the answer, and add them. This is known as
"end around carry."

This doesn't change our approach, it simplifies
it. Prove this to yourself by again trying this
problem. This time use the nines complement
and end around carry.

7
-1

75. The complement of 1 is 8,
added to 7, totals 15.
Drop the power and carry
it beneath the answer,

$$\begin{array}{r} 15 \\ 1 \\ \hline 6 \end{array}$$

Remainder is 6.

76. Once again, let us try it with a larger value:

$$\begin{array}{r} 33 \\ -16 \\ \hline \end{array}$$

The value of 16 is of course larger than 9, for
its nines complement we must use 99.

The nines complement of the subtrahend 16 is
83. Add the complement of 83 and the minuend
of 33, total = 116. Drop the end (added power)
16. Carry the 1 beneath the answer

$$\begin{array}{r} 16 \\ 1 \\ \hline 17 \end{array}$$

Add them for a remainder of

The example given should allow you to figure the
proper nines complement and end around carry
for the following problem:

$$\begin{array}{r} 8342 \\ -1976 \\ \hline \end{array}$$

76. 6366

77. For practice, try these two problems using
nines complement and end around carry.

$$\begin{array}{r} 7617 \\ -5143 \\ \hline \end{array} \quad \begin{array}{r} 98197 \\ -14106 \\ \hline \end{array}$$

77. 2474 84091

78. If we wished we could subtract decimal numbers
using complementing by reducing the value of
our complement and adding different values to
the remainder to make up for the reduction.

Binary, consisting of 1's and 0's, needs only
the very lowest value of complement, a one's
complement. In a one's complement, if we
already have a 1, we need nothing (0) to comple-
ment it. Conversely, if we have nothing (0) we
need a ____ to complement it.

78. 1

79. Reviewing the latter portion of the preceding
page, we simply stated that in a one's complement,
the complement of 0 is ____, and the complement
of 1 is ____.

79. The complement of 0 is 1, and the complement of 1 is 0.

80. In subtraction of binary numbers by complementing, we find complementing an easy task. We must not forget though that we still use the same methods of adding our complement and minuend, and dropping the added power by our end around carry. For example:

10 Minuend
-01 Subtrahend

The one's complement of the subtrahend 01 is 10. Add the complement of 10 and the minuend of 10

10
+10
100

Drop the end (added power) 100
Carry the 1 beneath the answer 00

Add them for a binary value of $\begin{array}{r} 1 \\ 01 \end{array}$

Try this problem $\begin{array}{r} 110 \\ -010 \end{array}$

80. The complement of 010 is 101, added to 110, totals 1011. Drop the power, and carry it beneath the answer

$\begin{array}{r} 1011 \\ 1 \\ \hline 100 \end{array}$

Remainder is 100.

81. Since subtraction of binary numbers using complementing is the most prominent method in electronics, it would be wise if we tried various examples to be very sure we have a good understanding of the method.

Example:	Complemented	End around carry
$\begin{array}{r} 1011011 \\ -0100011 \\ \hline \end{array}$	$\begin{array}{r} 1011011 \\ +1011100 \\ \hline 0000111 \end{array}$	$\begin{array}{r} 1011011 \\ +0000001 \\ \hline 110110 \end{array}$
Carry 1	$\begin{array}{r} 11 \\ 11 \end{array}$	$\begin{array}{r} 111 \\ 100 \end{array}$

Remainder = 111000

Try these problems:

$\begin{array}{r} 100110110 \\ -001101001 \\ \hline \end{array}$	$\begin{array}{r} 1110010110 \\ -0001100100 \\ \hline \end{array}$
--	--

81. 11001101 1100110010

82. Any time you are in doubt you can convert the binary values to decimal values to check your answer.

Try these problems:

$\begin{array}{r} 110100110 \\ -000010000 \\ \hline \end{array}$	$\begin{array}{r} 101101 \\ -011001 \\ \hline \end{array}$
--	--

82. 110010110 10100

83. As mentioned earlier, arithmetic based on the number eight is called an octal or octonary system. The base 8 is often used in computing circuits. The number 8 is also an integral power of 2 ($2^3 = 8$).

Another reason for octal numbering is that representation of an octal digit is simple since any of the eight digits (0-7) can be represented by a maximum of three binary bits ($7 = 111$).

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84. To convert a decimal number to an octal value we use an approach similar to that used to convert a decimal number to a binary number. The octal system being based on the number 8, we will simply divide our decimal number by 8 and keep track of the remainder.

For example: the decimal number 26 divided by 8 is 3, with a remainder of 2.

We write it this way.
$$\begin{array}{r} 3 \\ 8 \overline{) 26} \end{array} \begin{array}{l} 2 \end{array}$$

The next step is to continue to divide by 8. Since 8 cannot go into 3 we place the 3 on the side as the remainder.

$$\begin{array}{r} 8 \overline{) 3} \end{array} \begin{array}{l} 3 \\ 26 \\ 2 \end{array} \leftarrow \text{This is the octal number.}$$

The octal number 32 is equivalent to decimal number 26.

Using this method, what is the octal number for the decimal number 18?

84.
$$\begin{array}{r} 8 \overline{) 2} \end{array} \begin{array}{l} 2 \\ 18 \\ 2 \end{array}$$

Octal 22 equals decimal 18.

85. Larger decimal numbers are converted the same way, we merely have more steps. For example: the decimal value 1547.

$$\begin{array}{r} 8 \overline{) 3} \quad 3 \\ 8 \overline{) 24} \quad 0 \\ 8 \overline{) 193} \quad 1 \\ 8 \overline{) 1547} \quad 3 \end{array}$$

Decimal 1547 is equal to octal 3013.

Convert the decimal number 6241 to its octal equivalent.

85.

$$\begin{array}{r}
 8 \overline{) 1} \quad 1 \\
 8 \overline{) 12} \quad 4 \\
 8 \overline{) 97} \quad 1 \\
 8 \overline{) 780} \quad 4 \\
 8 \overline{) 6241} \quad 1
 \end{array}$$

Decimal 6241 equals
octal 14141.

86.

We previously converted decimal 18 to octal 22, let's prove that octal 22 equals decimal 18. Working with the base 8, we know that 8^0 represents 1, and that 8^1 represents 8. Placing these values in a table with the octal value expressed underneath their respective columns, we have:

8^1	8^0
8	1
2	2

$$2 \times 8^0 = 2 \times 1 = 2$$

$$2 \times 8^1 = 2 \times 8 = 16$$

$$18$$

Try converting the octal number 34 to its equivalent decimal value.

86.

8^1	8^0
8	1
3	4

$$4 \times 8^0 = 4 \times 1 = 4$$

$$3 \times 8^1 = 3 \times 8 = 24$$

$$28$$

Octal 34 equals decimal 28.

87.

As mentioned earlier an advantage of an octal value is that each digit can be expressed by no more than three binary bits.

To express the octal value of 107 in binary we start from the least significant digit and in turn convert each digit to its binary equivalent.

$$\begin{array}{r}
 1 \ 0 \ 7 \\
 001 \overline{) 000} \overline{) 111}
 \end{array}$$

Octal 107 equals binary 1000111.

Try converting the octal value 210 to its binary equivalent.

87.

$$\begin{array}{r}
 2 \ 1 \ 0 \\
 010 \overline{) 001} \overline{) 000}
 \end{array}$$

Octal 210 equals binary
10001000.

88.

To convert a binary number to an octal number we merely reverse the procedure. For example, let us convert binary 1011001 to its octal equivalent.

$$\begin{array}{r}
 001 \ 011 \ 001 \\
 1 \ 3 \ 1
 \end{array}$$

Binary 1011001 equals octal 131.

Try converting binary 110100100 to its octal equivalent.

88. $\begin{array}{c|c|c} 110 & 100 & 100 \\ \hline 6 & 4 & 4 \end{array}$

Binary 110100100 equals
octal 644.

89. Let us go one step further and prove our binary to octal conversions. We just converted binary 110100100 to octal 644. Let's convert each number by its associated powers to its decimal equivalent.

2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
256	128	64	32	16	8	4	2	1
1	1	0	1	0	0	1	0	0

$$\begin{array}{r} 1 \times 2^2 = 4 \\ 1 \times 2^5 = 32 \\ 1 \times 2^7 = 128 \\ 1 \times 2^8 = 256 \\ \hline 420 \end{array}$$

8^2	8^1	8^0
64	8	1
6	4	4

$$\begin{array}{r} 4 \times 8^0 = 4 \\ 4 \times 8^1 = 32 \\ 6 \times 8^2 = 384 \\ \hline 420 \end{array}$$

Decimal 420 = Octal 644 = Binary 110100100

Try converting binary 1011111 to its octal equivalent, then convert both the binary and octal values to their decimal equivalent.

89. $\begin{array}{c|c|c} 001 & 011 & 111 \\ \hline 1 & 3 & 7 \end{array}$

$$\begin{array}{r} 1 \times 2^0 = 1 \\ 1 \times 2^1 = 2 \\ 1 \times 2^2 = 4 \\ 1 \times 2^3 = 8 \\ 1 \times 2^4 = 16 \\ 1 \times 2^6 = 64 \\ \hline 95 \end{array}$$

$$\begin{array}{r} 7 \times 8^0 = 7 \\ 3 \times 8^1 = 24 \\ 1 \times 8^2 = 64 \\ \hline 95 \end{array}$$

Binary 1011111 = Octal 137
= Decimal 95.

This completes Binary Arithmetic.

VOLUME III
BOOLEAN ALGEBRA

1. Boolean algebra is named after George Boole (1815-1864), a mathematician. One of his published works has the full title of "An Investigation of the Laws of Thought on which Are Founded the Mathematical Theories of Logic and Probabilities." This treatise presented the first practical system of applying logic in algebraic form.

The real awakening to the usefulness of Boole's algebra to electricity and electronics came in 1938. A copy of the Transactions of the American Institute of Electrical Engineers contained in article entitled "A Symbolic Analysis of Relay and Switching Circuits." The author of the article was C. E. Shannon of the Bell Telephone Laboratories.

Thus in 1938 Boole's algebra, now known as Boolean Algebra, was applied to telephone switching circuits. Presently its use has extended to include computer type circuits.

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2. It is a valuable working tool providing a firm foundation for proper interpretation of complex logic diagrams.

It presents a convenient method for representing a switching circuit without drawing the circuit. It is useful for translating switching problems into equations, solving the equations, and directly converting the answer into statements or devices.

We are of course discussing _____
Algebra.

2. Boolean

3. Algebra is a collection of symbols and a set of rules governing their manipulation which serves the purpose of a shorthand to ease computation.

In the conventional type of algebra the symbols stand for numbers and the rules of operation are similar to those of boolean algebra. Boolean algebra is an algebra using a shorthand based on formal logic and is applicable to the design and understanding of electrical switching circuits.

The following example illustrates a difference.

Boolean Algebra	Conventional Algebra
$a = 1, b = 1$	$a = 1, b = 1$
$a + b$	$a + b$
$1 + 1 = 1$	$1 + 1 = 2$

Obviously boolean and conventional algebra (are/are not) identical.

3. are not

4. Unlike ordinary algebra, subtraction and division operations are forbidden in boolean algebra equations.

An example is the equation $A(A + B) = A$. You will learn that in boolean algebra the quantity $(A + B)$ is not necessarily 1, it is quite possible to have the quantity $(A + B)$ equal to 0.

In boolean algebra, if $(A + B) = 0$, then in the equation $A(A + B) = A$, $A = 0$.

However, if we divide both sides of the equation by A as in conventional algebra:

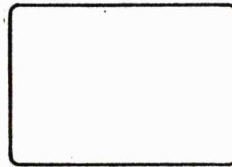
$$\frac{\cancel{A}(A + B)}{\cancel{A}} = \frac{\cancel{A}}{\cancel{A}} \quad (A + B) = 1$$

We should know then that in boolean algebra we cannot _____ and _____.

4. subtract and divide
(or vice versa)

5. All things can be divided into classes. For example, all dwellings, of any type, would be a class. All homes would be a member or sub-class of the class of dwellings. The class and sub-classes must have something in common, in this example they are all dwellings.

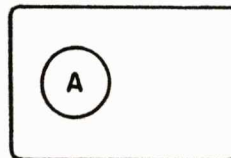
The class of all things with a certain characteristic can be illustrated by a rectangle enclosing all members of the class. This rectangle is called a Venn diagram, named for John Venn, an English Logician.



Class D, all members of the class of dwellings.

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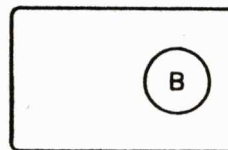
6. A member of the class of dwellings can be shown within the rectangle. On the Venn diagram illustrated below the sub-class of homes, called A, is inserted as a member of class D.



A is a _____ of D.

6. member

7. Another member of the class of dwellings would be all dwellings used only for business purposes. This too can be illustrated as being a member of class D.

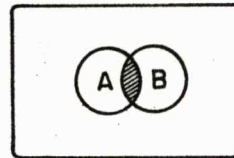


B is a _____ of D.

7. member

8. It is quite possible to have both members A and B overlap. There are undoubtedly some business dwellings doubling in use as domiciles, and some homes that are also used for business. In illustrating them in a Venn diagram we shadow the points of inclusion.

The Venn diagram illustrates that a member of class A can also be a member of class B, and vice versa. This conjunction shows that there are members of both class A and class B.

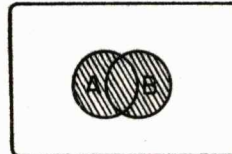


A _____ B
are members of
class D.

8. and

9. Let's apply our logic in a different direction. There are of course homes and business dwellings that are used only as such, plus those that are members of both classes. This can be illustrated in the Venn diagram by shadowing both A and B and the points of inclusion.

This Venn diagram illustrates that we have members of class A or members of class B, or both.



A _____ B is
a member of class D.

9. or

10. Boolean algebra is concerned with belonging or not belonging to a class, to True or False, Yes or No, etc. The letter symbols are only two-valued, and have only the possibilities of being 0 or 1.

With boolean algebra being two-valued, and these values being 0 or 1, we find boolean algebra to be a logical extension of _____ arithmetic.

10. binary

11. Boolean algebra has two classes, or conditions, these are represented by the binary values of _____ and _____.

11. 0 and 1
(or vice versa)

12. Because of its newness, many of the terms and expressions used in boolean algebra are not always used consistently. For example, the sign + is sometimes shown as v, or V, or U. To prevent confusion we will briefly define the following terms, Postulate, Theorem, and Expression.

(Proceed to the next frame)

13. truth

13. We will consider a postulate to be a self-evident truth, that has not yet been proven to be an absolute _____.

14. A theorem will be considered to be a postulate that has been proven to be an absolute truth, and can be considered to be an established principle or law.

Another way of expressing it, a theorem is a proven _____.

14. postulate

15. In this course we will first consider an expression as being a self-evident truth, or _____.

We will then prove it to be a law, or an established principle, called a _____.

15. postulate
theorem

16. Boolean algebra has two classes, or conditions, represented by the binary values of 0 and 1. Another notably different aspect of boolean algebra is the concept of NOT.

The NOT function is one of complementing, or negation. It is a logical method of noting when something is NOT present, therefore, it is absent. For example, when something is NOT true, it is false.

(Proceed to the next frame)

17. The NOT function is indicated by a bar over the symbol. For example, \bar{A} , reads "NOT A," or it can be read "A NOT."

It may also be shown (in other texts) by the symbol for prime. For example, B' would be read as "_____."

17. "NOT B" or "B NOT"

18. There will also be instances where a function is double-notted, written $\bar{\bar{A}}$.

As in any double-negative statement, it is equal to a positive statement. This means that $\bar{\bar{A}} = \underline{\hspace{1cm}}$.

18. $\bar{\bar{A}} = A$

19. The symbol \bar{A} denotes the complement of A. If the value of A is 1, \bar{A} must equal the value of _____.

19. 0

20. The complement of \bar{A} is A, and vice versa. If the value of \bar{B} is 1, B must equal the value of _____.

20. 0

21. In boolean algebra expressions the binary function of 0 and 1 may be assigned to any two-state device. Examples include hydraulic valves that are open or shut, mechanical clutches that are engaged or disengaged, etc.

The binary devices we will work with will be forms of electrical switches. It could be a toggle switch that is on or off, a diode that is conducting or nonconducting, a transistor that is cutoff or in saturation, etc.

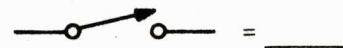
For simplification all circuit representation will be illustrated without an input source or output load. It will also be assumed that the input source is always a binary 1.

(Proceed to the next frame)

22. Throughout this course we will assign the binary value of 1 as being represented by a closed switch. The binary value of 0 will be represented by an _____ switch.

22. open

23. to ensure our understanding of the binary functions as used in this course we can represent them with switches as shown below.



23. 1
0

24. In conventional algebra the symbol + defines "add." However, in boolean algebra it is assigned the meaning "OR." Thus $X + Y$ is read "X OR Y."

The OR function is a parallel function that logically spells out "either - or - or both."

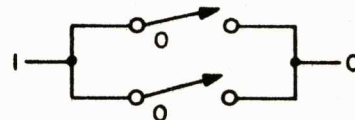
Two switches, one represented by A, one represented by B, which are to be placed as an OR function, would be expressed as $A + B$, and read as A _____ B.

24. A OR B

25. To help us examine each postulate, we will use Single Pole Single Throw (SPST) switch symbols for "representation" of the logic.

One postulate of an OR function is $0 + 0 = 0$.

The OR function being a parallel function we can represent it with parallel switches as shown below.



When reading this function we express it as 0
_____ $0 = 0$.

25. OR

26. Although we will restrict ourselves to discussing the basic parallel OR function, represented by two SPST switches, it should be known that it also holds true for n - switches.

This is expressed as $0 + 0 + 0 + \dots + 0 = 0$

This can be represented as:



This illustrates that logically we can have an indeterminate number of paralleled open switches (0's), the output will still be the binary value of _____.

26. 0

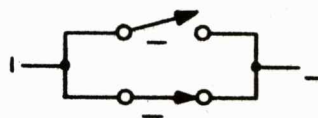
27. Another postulate of an OR function is:

$$0 + 1 = 1$$

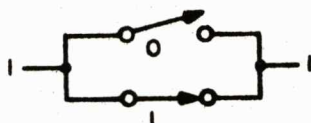
This is the same as in ordinary algebra. It can be expressed as: "In a parallel circuit, if we have either 0 OR 1, the logical sum will be _____."

27. 1

28. The postulate $0 + 1 = 1$ can be represented as shown below: Label the binary values of each switch and the resultant output as expressed by the postulate.



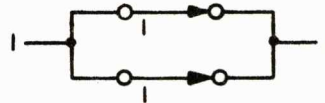
28.



29. The postulate $0 + 1 = 1$ logically tells us that in a parallel OR function of n - switches, it only requires one closed switch to provide a closed path and give us a binary _____ at the output.

29. 1

30. This postulate requires some thought, $1 + 1 = 1$. This does not follow ordinary algebra. Looking at the representation of this postulate will show why.



With either or both switches closed, the output can be no higher than a binary _____.

30. 1

31. Substituting letter symbols for one of the variables may help us grasp the concept of the following expressions.

Let us substitute a letter symbol for the first postulate, $0 + 0 = 0$, giving us $A + 0 = A$.

This means that any switch in parallel with an open switch will behave logically as that switch alone.

If we can prove that statement, the expression $A + 0 = A$ no longer represents a postulate, it will represent a _____.

31. theorem

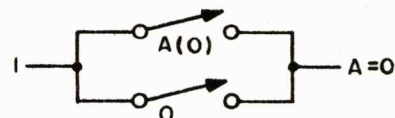
32. To prove that $A + 0 = A$ we will substitute both 0 and 1 for A.

1) Substituting, $A = 0$. $A + 0 = 0$. $0 + 0 = 0$.

2) Substituting, $A = 1$. $A + 0 = 1$. $1 + 0 = 1$.

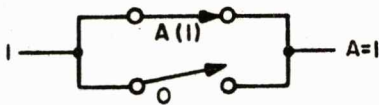
In each substitution we proved that a switch in parallel with an open switch will behave logically as that switch alone.

A representation of the first substitution would be:



You draw the representation of the second substitution.

32.



33. Now we will substitute a letter symbol for the next postulate, $0 + 1 = 1$, this gives us $A + 1 = 1$.

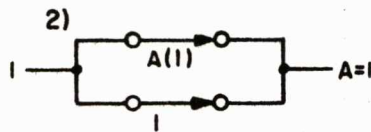
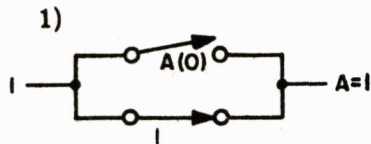
This says that a switch in parallel with a closed switch will behave logically as the closed switch.

1) Substituting, $A = 0$. $A + 1 = 1$. $0 + 1 = 1$.

2) Substituting, $A = 1$. $A + 1 = 1$. $1 + 1 = 1$.

Try drawing the representation for each substitution. Be sure to label each switch and the output.

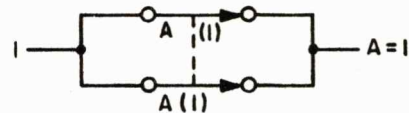
33.



34. For the postulate $0 + 0 = 0$, and $1 + 1 = 1$, we can substitute the symbol A , this gives us $A + A = A$.

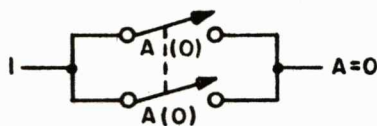
This says that two switches operating together, when placed in parallel behave logically as one switch.

This expression can be represented for one postulate in this manner.



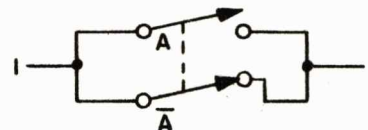
Try drawing the representation for the other expression of $A + A = A$.

34.



35. It is possible to have one switch complement the other, that is, as one is closed the other opens.

This can be expressed as $A + \bar{A} = 1$, and represented as:



This illustrates that in a parallel circuit a switch and its complement behave logically as a closed circuit.

The expression $A + \bar{A} = 1$ is read A A = 1.

35. $A \text{ OR NOT } A = 1$

36. Reviewing the OR function.

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 1 = 1$$

The expressions above were listed as _____.

The expressions below were listed as _____.

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + A = A$$

$$A + \bar{A} = 1$$

36. postulates
theorems

37. In conventional algebra the symbol x defines "multiply." In boolean algebra it is assigned the meaning "AND." Thus $A \times B$ is read "A AND B," and is called the logical product. The AND function is also often expressed as $A \cdot B$, or simply AB .

The AND function is a series function that logically spells out "both _____ and _____."

Two switches, represented by A and B , which are to be placed in an AND function, would be expressed as $A \times B$, and read as A _____ B .

37. $A \text{ AND } B$

38. One postulate of an AND function is $0 \times 0 = 0$.

The AND function being a series function we can represent it with series switches as shown below.



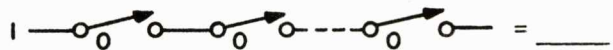
When reading this function we can express it as $0 \text{ AND } 0 = 0$.

38. AND

39. Our discussion so far has been based on two switches in series. It should be apparent that three or more open switches will give the same results.

We can express it as $0 \times 0 \text{ ---- } \times 0 = 0$.

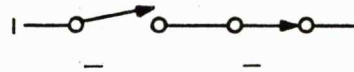
This can be represented as:



39. 0

40. Another postulate of an AND function is $0 \times 1 = 0$.

This can be represented as shown below. Label the binary values of each switch, and the resultant output as expressed by the postulate.



40.



41. The postulate $0 \times 1 = 0$ logically tells us that in a series AND function of n-switches, it requires only one open switch to provide an open path and give us a binary $\underline{\hspace{1cm}}$ at the output.

41. 0

42. A third postulate of an AND function is $1 \times 1 = 1$.

This postulate is represented as shown below, you fill in the binary output value.



42.

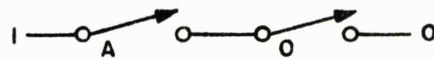


43. To prove our postulates, and develop a theorem, we will substitute letter symbols. For the first postulate, $0 \times 0 = 0$, we have $A \times 0 = 0$.

This states that any switch in series with an open switch behaves logically as an open switch.

- 1) Substituting, $A = 0$. $A \times 0 = 0$. $0 \times 0 = 0$.
- 2) Substituting, $A = 1$. $A \times 0 = 0$. $1 \times 0 = 0$.

A representation of the first substitution would be:



You draw the representation of the second substitution.

43.



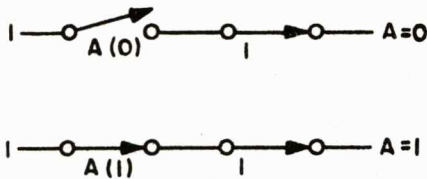
44. Substituting a letter symbol for the postulate $0 \times 1 = 0$, we have $A \times 1 = A$.

This says that a switch in series with a closed switch will behave logically as that switch alone.

- 1) Substituting, $A = 0$. $A \times 1 = A$. $0 \times 1 = 0$.
- 2) Substituting, $A = 1$. $A \times 1 = A$. $1 \times 1 = 1$.

Try drawing the representation for each substitution, be sure to label each switch and the output.

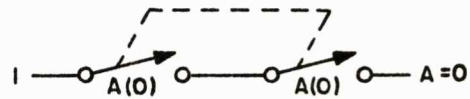
44.



45. For the postulates $0 \times 0 = 0$, and $1 \times 1 = 1$, we can substitute the symbol A , giving us $A \times A = A$.

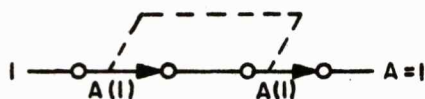
This says that two switches operating together, when connected in series, behave logically as one switch.

Representing one postulate:



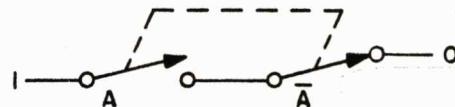
Try drawing the representation of the other postulate.

45.



46. As explained before, it is possible to have one switch complement another, that is, as one is closed the other opens.

This can be expressed as $A \times \bar{A} = 0$, and represented as:



This illustrates that in a series circuit a switch and its complement behave logically as an _____ circuit.

46. open

47. Reviewing the AND function.

$$0 \times 0 = 0$$

$$0 \times 1 = 0$$

$$1 \times 1 = 1$$

The expressions above were listed as _____.

The expressions below were listed as _____.

$$A \times 0 = 0$$

$$A \times 1 = A$$

$$A \times A = A$$

$$A \times \bar{A} = 0$$

47. postulates
theorem

48. Another working tool of boolean algebra is the DeMorgan theorem, also known as the law of dualization. It is of great help in reduction of a complex expression to its minimum value.

DeMorgan's theorem states that the value of $\overline{A + B}$ and the value of $\overline{A} \times \overline{B}$ are equal, and also that the value of $\overline{A} \times \overline{B}$ and $\overline{A + B}$ are equal.

Thus $\overline{A + B} = \overline{A} \times \overline{B}$,

and $\overline{A} \times \overline{B} = \overline{A + B}$.

(Proceed to the next frame)

49. $\overline{A + B} = \overline{A} \times \overline{B}$

When reading this law of dualization it should be read as:

"The expression NOT A OR NOT B equals the expression A AND B NOTTED."

You write out how you should read the other law of dualization.

$$\overline{A} \times \overline{B} = \overline{A + B}$$

49. "The expression NOT A AND NOT B equals the expression A OR B NOTTED."

50. Let's verify the DeMorgan Theorem. For each law of dualization we can assign a 0 and/or a 1 to each symbol. With two laws this gives us a total of eight possible combinations.

An algebraic reminder. A bar over a group of symbols means that the NOT function applies to the entire expression under the bar, also that inversion takes place only after we solve the quantity of the entire expression.

$$\overline{A + B} = \overline{A} \times \overline{B}$$

Rewrite the law of duality as expressed above, with a 0 assigned to each symbol.

50. $\overline{0} + \overline{0} = \overline{0 \times 0}$

51. First, the right side of the equation, we know that $0 \times 0 = 0$, therefore $\overline{0 \times 0} = \overline{0}$, $\overline{0} = 1$.

Doing the left side of the equation, $\overline{0} + \overline{0}$ is equal to $1 + 1 = 1$.

This gives us $1 = 1$.

Thus with 0 assigned to each symbol we find $\overline{A} + \overline{B}$ does equal $\overline{A \times B}$.

You try it with the value of 1 assigned to each symbol.

51. $\overline{A} + \overline{B} = \overline{A \times B}$
 $\overline{1} + \overline{1} = \overline{1 \times 1}$
 $1 \times 1 = 1$, therefore
 $\overline{1 \times 1} = \overline{1}$, $= 0$
 $\overline{1} + \overline{1} = \overline{1}$
 $0 + 0 = 0$
 $0 = 0$

(You can if you desire, as an exercise, verify the same law using combinations of 0 and 1, or 1 and 0 for each symbol.)

52. We can verify the other law of dualization in the same manner, $\overline{A} \times \overline{B} = \overline{A + B}$.

Assigning a 0 to each symbol we get
 $\overline{0} \times \overline{0} = \overline{0 + 0}$

Doing the right side of the equation, we know that $0 + 0 = 0$, therefore $\overline{0 + 0} = \overline{0}$, $\overline{0} = 1$.

Doing the left side, $\overline{0} \times \overline{0} = \overline{0}$, $\overline{0} = 1$.

Thus $1 = 1$

You try verifying that $\overline{A} \times \overline{B} = \overline{A + B}$ with the value of 1 assigned each symbol.

52. $\overline{A} \times \overline{B} = \overline{A + B}$
 $\overline{1} \times \overline{1} = \overline{1 + 1}$
 $1 + 1 = 1$, therefore
 $\overline{1 + 1} = \overline{1}$, $\overline{1} = 0$
 $\overline{1} \times \overline{1} = \overline{1}$, $\overline{1} = 0$
 $0 = 0$

(Again, you can if you desire, as an exercise, verify the same law using 1 and 0, then 0 and 1 for each symbol. Doing this will verify all eight possible combinations.)

53. The expressions and theorems previously discussed involved two variables. In practice we are more likely to be involved with more than two variables. An example might be an OR expression containing four variables, $A + B + C + D$. This could be in series with an AND expression of three variables, $E \times F \times G$. The entire expression would be written $A + B + C + D \times E \times F \times G$. However, this is confusing, is it $A + B + C$ OR $D \times E \times F \times G$? Or is it $A + B + C + D$ AND $E \times F \times G$?

To prevent confusion we place within parentheses any expression whose function is to be placed in series or parallel with another expression. Properly expressed the expression above would read $(A + B + C + D) \times (E \times F \times G)$.

(Proceed to the next frame)

54. The expression $(A + B + C + D) \times (E \times F \times G)$ could be expressed in a less confusing manner by simply dropping the AND sign and using a \cdot , or nothing, as in conventional algebra. The expression would now read:
 $(A + B + C + D) \cdot (E \cdot F \cdot G)$ or
 $(A + B + C + D) \cdot (EFG)$

Write, in its simplest form, the expression $A \times B \times C$ which is to be placed in parallel with the expression $D \times E \times F$.

54. $(ABC) + (DEF)$

55. In addition to the law of dualization there are other laws governing the manipulation of variables. The law of commutation states that as long as the connective (+ or \times) is the same, the position of the elements may be interchanged.

For example, $A + B + C$ is the same as $C + B + A$, or $B + C + A$, etc. Another example; $AB = BA$.

We can readily verify this by substitution of 1 or 0 for each variable.

$$A + B = B + A; A = 1 \text{ and } B = 0; \\ 1 + 0 = 0 + 1; 1 = 1$$

$$AB = BA; A = 1 \text{ and } B = 1; 1 \cdot 1 = 1 \cdot 1; 1 = 1$$

Prove it by trying the same two examples with $A = 0$ and $B = 1$.

55. $A + B = B + A;$
 $0 + 1 = 1 + 0; 1 = 1$

$AB = BA; 0 \cdot 1 = 1 \cdot 0;$
 $0 = 0.$

56. Another law governing the manipulation of variables in the associative law. This states that the elements may be grouped in any quantity as long as they are connected by the same sign.

For example; $A + B + C + D = A + (B + C + D)$
 $= (A + B + C) + (D)$ etc.

$ABCD = (ABC)D = (AB)(CD) = A(BCD)$ etc.

This is readily verified, we will assign a 1 to all variables.

$A + B + C + D; 1 + 1 + 1 + 1; = 1$

$A + (B + C + D); 1 + (1 + 1 + 1); 1 + 1; = 1$

$ABCD; 1 \cdot 1 \cdot 1 \cdot 1; = 1$

$(ABC)D; (1 \cdot 1 \cdot 1)1; 1 \cdot 1; = 1$

Verify it yourself by trying the same examples with A and B = 0, and C and D = 1.

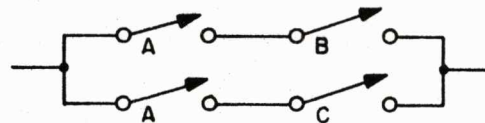
56. $A + B + C + D;$
 $0 + 0 + 1 + 1; = 1$

$A + (B + C + D);$
 $0 + (0 + 1 + 1); 0 + 1; = 1$

$ABCD; 0 \cdot 0 \cdot 1 \cdot 1; = 0$

$(ABC)D; (0 \cdot 0 \cdot 1)1;$
 $0 \cdot 1; = 0$

57. Any switching circuit can be looked upon as a combination of series and/or parallel connections. These combinations may be converted to simpler combinations. For example, taking first the expression AB, placing this in parallel with the expression AC, gives us the following representation.

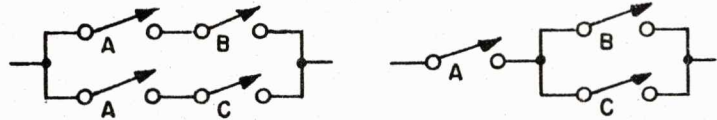


The circuit represented above would be expressed as _____.

57. $AB + AC$

58. Observation will show that the representation of $AB + AC$ can be simplified. We should remember that $A + A = A$.

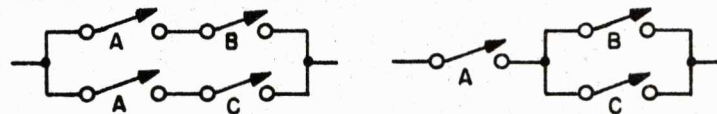
Thus:



We can see that it simplifies to one variable in series with two parallel variables. The simplified version can be expressed as _____.

58. $A(B + C)$

59.



Reviewing what we have done, we have shown that: _____ = _____.

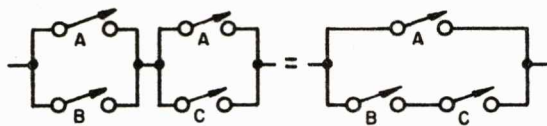
59. $AB + AC = A(B + C)$

60. We have actually been discussing a distributive law. Although the expression $AB + AC = A(B + C)$ closely represents the distributive law of ordinary algebra, it is only by coincidence; it does not hold true for the boolean law of distribution shown below.

$$(A + B)(A + C) = A + (BC)$$

To verify this distributive law draw the representation for both sides of the equation.

60.



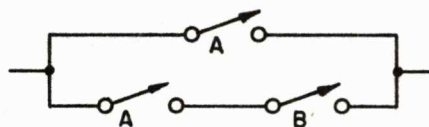
61. There are many theorems used in boolean algebra. The laws just discussed are also theorems, we were able to verify the truth of each law.

In addition to these theorems, and those noted in our discussion of NOT, AND and OR logic, there are many other theorems. For simplification we will discuss one more theorem, verify its truth, and place a list of these and other theorems in an appendix at the back of this book. Placing this list as an appendix will aid in any future reference to theorems.

(Proceed to the next frame)

62. As an example we will take the theorem $A + AB = A$.

It can be represented as:



Looking closely at the circuit it is obvious that it makes no difference whether B is 0 or 1, the logic decision is being made by _____.

62. A

63. $A + AB = A$ can also be verified by a table illustrating all the possible conditions for A and B.

$A + AB = A$

A	B	A	AB	
0	0	0	0	0
0	1	0	0	0
1	0	1	0	1
1	1	1	1	1

The table tells us that when A is 0 and B is 0, the value of A is 0, the value AB is 0, thus $0 + 0 = 0$. The output A is the same as the input A, verifying that $A + AB = A$.

The table illustrated what the truth is for the output of the theorem $A + AB = A$, accordingly the table is called a _____ table.

63. truth

64. In working with boolean algebra, to reduce an expression to its minimal, there will be times when we have to multiply, factor, or both. We will first discuss multiplication.

(Proceed to the next frame)

65. You cannot multiply when the sign between two functions is OR. You can multiply two functions when the sign between them is AND.

In multiplying two terms, we multiply the 1st symbol of the first term against each symbol of the second term. Then we multiply the 2nd symbol of the first term against each symbol of the second term.

For example: $(A + B) (C + D)$

equals: $AC + AD + BC + BD$

Try it with $(D + E) (F + G)$

65. $(D + E) (F + G)$
 $=DF + DG + EF + EG$

66. Another example:

$(A + B + C) (D + E + F)$

$=AD + AE + AF + BD + BE + BF + CD + CE + CF$

Try it with $(M + N + O) (R + S + T)$

66. $(M + N + O)$
 $(R + S + T)$
 $=MR + MS + MT + NR$
 $+ NS + NT + OR + OS$
 $+ OT$

67. When multiplying three terms, we multiply the first two terms, then multiply the resulting sum and the remaining term.

For example:

$(A + B) (C + D) (E + F)$

$= (AC + AD + BC + BD) (E + F)$

$= ACE + ACF + ADE + ADF + BCE + BCF$
 $+ BDE + BDF$

Try it with $(L + M) (N + O) (R + S)$

$$\begin{aligned}
 67. \quad & (L + M) (N + O) (R + S) \\
 & = (LN + LO + MN + MO) (R + S) \\
 & = LNR + LNS + LOR + LOS \\
 & \quad + MNR + MNS + MOR \\
 & \quad + MOS
 \end{aligned}$$

$$\begin{aligned}
 68. \quad & 1) (A + D) (C + F) \\
 & = AC + AF + DC + DF
 \end{aligned}$$

$$\begin{aligned}
 & 2) (R + S) (B + F) (N + O) \\
 & = (RB + RF + SB + SF) (N + O) \\
 & = RBN + RBO + RFN \\
 & \quad + RFO + SBN + SBO \\
 & \quad + SFN + SFO
 \end{aligned}$$

68. As an exercise, multiply:

$$\begin{aligned}
 1) \quad & (A + D) (C + F) \\
 2) \quad & (R + S) (B + F) (N + O)
 \end{aligned}$$

69. To illustrate factoring, we will multiply an expression, then factor the result back to the original expression.

$$\text{For example: } A (B + C)$$

$$\text{Multiplying: } AB + AC$$

To factor we will take the common factor, A, move it outside, and place what is left in parentheses.

$$A (B + C)$$

(Proceed to the next frame)

70. With two terms $(A + B) (C + D)$
 Multiplying; $AC + AD + BC + BD$
 Take out the common factor, A in the 1st term, B in the 2nd term.

$$A (C + D) + B (C + D)$$

Take out the common factor $(C + D)$

$$(C + D)(A + B)$$

Using the associative law we can state the answer as

$$(A + B) (C + D).$$

Try it with $(D + E) (F + G)$

$$\begin{aligned}
 70. \quad & (D + E) (F + G) \\
 & = DF + DG + EF + EG \\
 & = D(F + G) + E(F + G) \\
 & = (F + G) (D + E) \\
 & = (D + E) (F + G)
 \end{aligned}$$

71. With three terms $(A + B) (C + D) (E + F)$

First, multiply these terms, check the results, then proceed to the next frame.

$$\begin{aligned}
 71. \quad & (A + B)(C + D)(E + F) \\
 &= (AC + AD + BC + BD)(E + F) \\
 &= ACE + ACF + ADE + ADF \\
 &\quad + BCE + BCF + BDE \\
 &\quad + BDF
 \end{aligned}$$

$$72. \quad ACE + ACF + ADE + ADF + BCE + BCF + BDE + BDF$$

Taking out the common factors, A in 1st term, B in 2nd term,

$$A(CE + CF + DE + DF) + B(CE + CF + DE + DF)$$

$$\text{Factoring the term } (CE + CF + DE + DF) \\ (CE + CF + DE + DF)(A + B)$$

$$\text{Factoring C in 1st term, D in 2nd term.} \\ \boxed{C(E + F) + D(E + F)}(A + B)$$

$$\text{Factoring } (E + F) \\ (E + F)(C + D)(A + B)$$

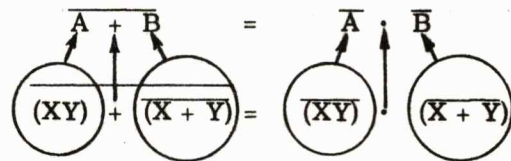
Using the associative law our answer is $(A + B)(C + D)(E + F)$

As an exercise repeat this procedure with the expression $(A + L)(B + N)(C + F)$

$$\begin{aligned}
 72. \quad & (A + L)(B + N)(C + F) \\
 &= (AB + AN + LB + LN)(C + F) \\
 &= ABC + ABF + ANC + ANF \\
 &\quad + LBC + LBF + LNC \\
 &\quad + LNF \\
 &= A(BC + BF + NC + NF) \\
 &\quad + L(BC + BF + NC + NF) \\
 &= (BC + BF + NC + NF)(A + L) \\
 &= B(C + F) + N(C + F)(A + L) \\
 &= (C + F)(B + N)(A + L) \\
 &= (A + L)(B + N)(C + F)
 \end{aligned}$$

73. Many of the logic circuits will have inputs or outputs that are complemented or will be complemented. A not uncommon expression might be $\overline{(XY)} + \overline{(X + Y)}$.

To simplify this expression we must use De Morgan's Theorem.



(Proceed to the next frame)

$$74. \quad \overline{(XY)} + \overline{(X + Y)}$$

$$\text{Equals } \overline{(XY)} \cdot \overline{(X + Y)}$$

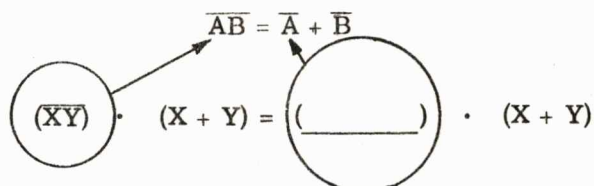
We know that a double negative equals a positive ($\overline{\overline{A}} = A$), therefore we can further simplify the expression:

$$\overline{(XY)} \cdot \overline{(X + Y)} = \underline{\hspace{2cm}}$$

$$74. \quad \overline{(\overline{X}Y)} \cdot \overline{(X + Y)} \\ = (\overline{X}Y) \cdot (X + Y)$$

$$75. \quad \overline{(\overline{X}Y) + (\overline{X + Y})} \\ \text{Equals } \overline{(\overline{X}Y)} \cdot \overline{(\overline{X + Y})} \\ \text{Equals } (\overline{X}Y) \cdot (X + Y)$$

To further simplify we again use De Morgans Theorem



$$75. \quad \overline{(\overline{X}Y)} \cdot (X + Y) \\ = (\overline{X} + \overline{Y}) \cdot (X + Y)$$

$$76. \quad \overline{(\overline{X}Y) + (\overline{X + Y})} \\ \text{Equals } \overline{(\overline{X}Y)} \cdot \overline{(\overline{X + Y})} \\ \text{Equals } (\overline{X}Y) \cdot (X + Y) \\ \text{Equals } (\overline{X} + \overline{Y}) \cdot (X + Y)$$

The next step is to multiply,

$$(\overline{X} + \overline{Y}) \cdot (X + Y) = \underline{\hspace{2cm}}$$

$$76. \quad (\overline{X} + \overline{Y}) \cdot (X + Y) \\ = \overline{X}X + \overline{X}Y + \overline{Y}X + \overline{Y}Y$$

$$77. \quad \overline{(\overline{X}Y) + (\overline{X + Y})} \\ \text{Equals } \overline{(\overline{X}Y)} \cdot \overline{(\overline{X + Y})} \\ \text{Equals } (\overline{X}Y) \cdot (X + Y) \\ \text{Equals } (\overline{X} + \overline{Y}) \cdot (X + Y) \\ \text{Equals } \overline{X}X + \overline{X}Y + \overline{Y}X + \overline{Y}Y$$

One of the theorems discussed early in this book was $\overline{A}A = 0$

Therefore, $\overline{X}X + \overline{X}Y + \overline{Y}X + \overline{Y}Y = \underline{\hspace{2cm}}$

$$77. \quad \overline{X}X + \overline{X}Y + \overline{Y}X + \overline{Y}Y \\ = \overline{X}Y + \overline{Y}X$$

$$78. \quad \text{Reviewing - } \overline{XY + (X + Y)} \\ \text{Equals } \overline{(\overline{X}Y)} \cdot \overline{(\overline{X + Y})} \\ \text{Equals } (\overline{X}Y) \cdot (X + Y) \\ \text{Equals } (\overline{X} + \overline{Y}) \cdot (X + Y) \\ \text{Equals } \overline{X}X + \overline{X}Y + \overline{Y}X + \overline{Y}Y \\ \text{Equals } \overline{X}Y + \overline{Y}X$$

The simplification tells us that when $\overline{X} = 1$ and $Y = 1$, or when $\overline{Y} = 1$ and $X = 1$, the output of the logic circuits will also be a $\underline{\hspace{1cm}}$.

78. 1

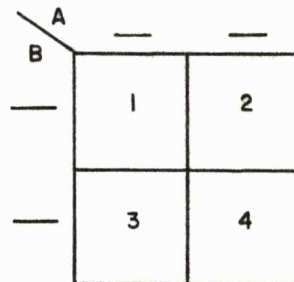
79. The boolean function of a circuit describes the conditions under which the circuit will conduct and transmit a 1. Simplification of a circuit to its minimal expression will show what inputs are required to have the circuit transmit a 1.

The method of simplification using multiplication and factoring has already been discussed. Another method consists of mapping the variables of each expression so that it will visually indicate simplification of an expression. Named after its originator, it is called a "Karnaugh" map.

(Proceed to the next frame)

80. To express an OR function with two variables on a Karnaugh map we draw a square grid containing 2^n blocks, with n being the number of variables. For a two variable OR function we would have 2^2 or four blocks, as shown below.

Note that we label the top and side of the map with each variable, and each block is numbered. You label each side by its two binary values.



80.

	A	0	1
B			
0		1	2
1		3	4

	A	1	0
B			
1		1	2
0		3	4

81.

	A	0	1
B			
0		1	2
1		3	4

81. For an OR function we know that when A is 0 and B is 0 the output is 0. In the Karnaugh map shown below the block corresponding to A = 0 and B = 0 is block 1, its value being zero we ignore it.

When A is 1 and B is 0 the output is 1. This corresponds to block 2. To indicate an output we shade the block. (Another version is to represent an output with a 1 placed in the block.) You shade any other combination of the two variables A and B that will give a 1 output and leave blank any combination that gives a 0 output.

	A	0	1
B			
0		1	2
1		3	4

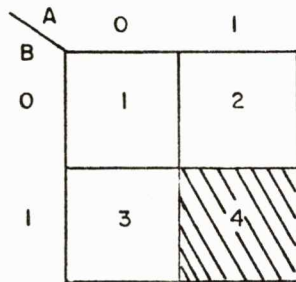
82. The Karnaugh map for a two variable OR function shows an output for the two vertically adjacent blocks, 2 and 4. This adjacency is illustrated by a loop between the two shaded blocks. This indicates that regardless of what B is, when A is 1 there will be an output.

The map also shows an output for two horizontally adjacent blocks 3 and 4 (also illustrated by the loop between the blocks). This indicates that regardless of what A is, when B is 1 there will be an output.

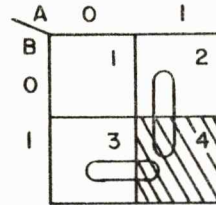
	A	0	1
B			
0		1	2
1		3	4

Based on what has been discussed so far, you should be able to develop a Karnaugh map for a two variable AND function. Try this, then check your results.

82.



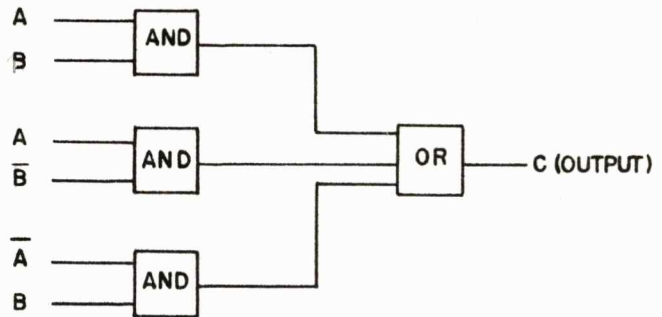
83.



From the Karnaugh map representing the AND function we can see that a block on the extreme end of a column or row when shaded indicates that the combination of these inputs will provide an _____.

83. output

84. A group of AND circuits whose output is applied to an OR circuit can be represented by the block diagram below.

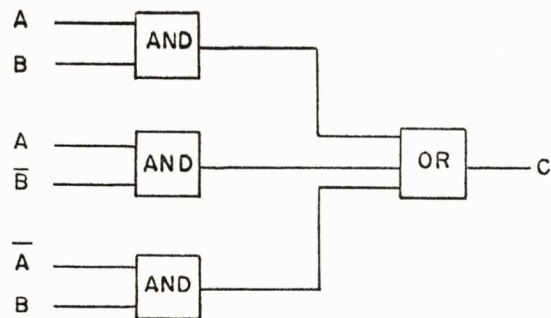


$$AB + A\bar{B} + \bar{A}B = C$$

This diagram tells us that when A is 1 and B is 1, or, when A is 1 and \bar{B} is 1, or, when \bar{A} is 1 and B is 1, we will get an output of 1 at C.

84. This diagram tells us that when A is 1 and B is 1, or, when A is 1 and \bar{B} is 1, or, when \bar{A} is 1 and B is 1, we will get an output of 1 at C.

85.



The output of the block diagram above is expressed as:

$$AB + A\bar{B} + \bar{A}B = C$$

Complete the expression.

85. $AB + \overline{A}\overline{B} + \overline{A}B = C$

86. Let us draw a Karnaugh map of $AB + \overline{A}\overline{B} + \overline{A}B = C$

We have only two variables, A and B. We stated before that we draw a grid containing 2^n blocks, with n being the number of variables. Draw and label the Karnaugh map for the variables A and B.

86.

	A	0	1
B			
0	1	2	
1	3	4	

87. The next step is to fill in the Karnaugh map to indicate what condition(s) of the expression $AB + \overline{A}\overline{B} + \overline{A}B$ will provide an output.

We know that we will get an output when $A = 1$ and $B = 1$, shade this in the Karnaugh map.

	A	0	1
B			
0	1	2	
1	3	4	

87.

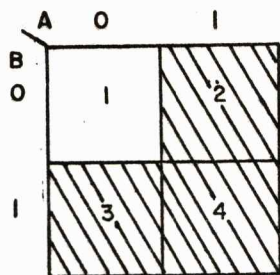
	A	0	1
B			
0	1	2	
1	3	4	

88. Continuing to fill in the Karnaugh map for the expression $AB + \overline{A}\overline{B} + \overline{A}B$. The next function is $A = 1$ and $\overline{B} = 1$. This is done by shading the block that represents $A = 1$, and, since $\overline{B} = 1$, then $B = 0$, and we shade block 2.

	A	0	1
B			
0	1	2	
1	3	4	

You shade in the block that represents $\overline{A}B$.

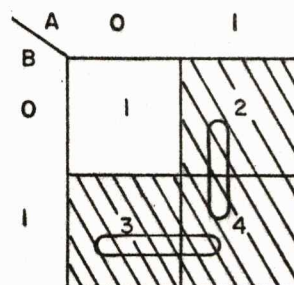
88.

89. $B = 1$

89.

We now have a Karnaugh map that indicates the conditions for the expression $AB + A\bar{B} + \bar{A}B$. To use it we look for two vertically, or horizontally adjacent blocks. In this way we have adjacent blocks at 2 and 4, and 3 and 4. The vertically adjacent blocks of 2 and 4 are under $A = 1$, this tells us that whenever $A = 1$ we will have an output (indicated by the loop). The horizontally adjacent blocks of 3 and 4 tells us that we will have an output when _____ = 1.

90.



Reviewing the Karnaugh map as a minimization of $AB + A\bar{B} + \bar{A}B$, it tells us that all we need for an input to provide an output of 1 is _____ + _____.

90. $A + B$

91. The simplified equation given by use of the Karnaugh map can be verified by simplification using boolean algebra.

$$AB + A\bar{B} + \bar{A}B \text{ (Factor out A)}$$

$$A(B + \bar{B}) + \bar{A}B \text{ (Theorem, } A + \bar{A} = 1)$$

$$A1 + \bar{A}B \text{ (Theorem, } A1 = A)$$

$$A + \bar{A}B \text{ (Theorem, } A + BC = (A + B)(A + C))$$

$$(A + \bar{A})(A + B) \text{ (Theorem } A + \bar{A} = 1)$$

$$1(A + B)$$

$$A + B$$

$$AB + A\bar{B} + \bar{A}B = \underline{\hspace{2cm}}$$

91. $AB + A\bar{B} + \bar{A}B = \underline{A + B}$

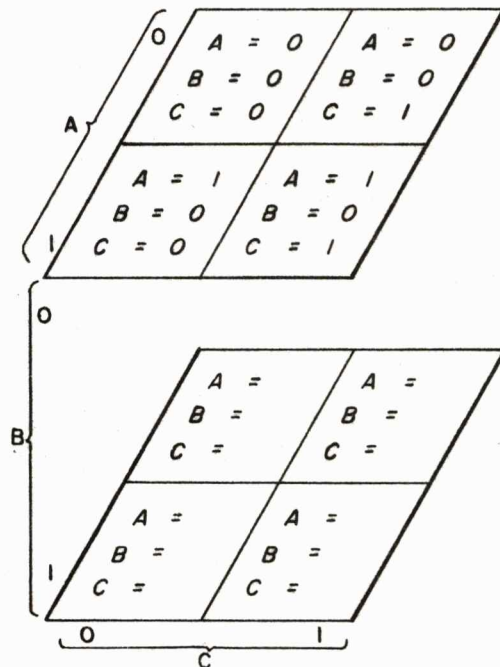
92. To draw a Karnaugh map of three variables we will have 2^3 (8) blocks. For the three variables A, B and C we can have eight combinations, these are:

A = 0	B = 0	C = 0	A = <u> </u>	B = <u> </u>	C = <u> </u>
A = 0	B = 0	C = 1	A = <u> </u>	B = <u> </u>	C = <u> </u>
A = 0	B = 1	C = 0	A = <u> </u>	B = <u> </u>	C = <u> </u>
A = 0	B = 1	C = 1	A = <u> </u>	B = <u> </u>	C = <u> </u>

You complete the other possible combinations.

92. A = 0 B = 0 C = 0
 A = 0 B = 0 C = 1
 A = 0 B = 1 C = 0
 A = 0 B = 1 C = 1
 A = 1 B = 0 C = 0
 A = 1 B = 0 C = 1
 A = 1 B = 1 C = 0
 A = 1 B = 1 C = 1

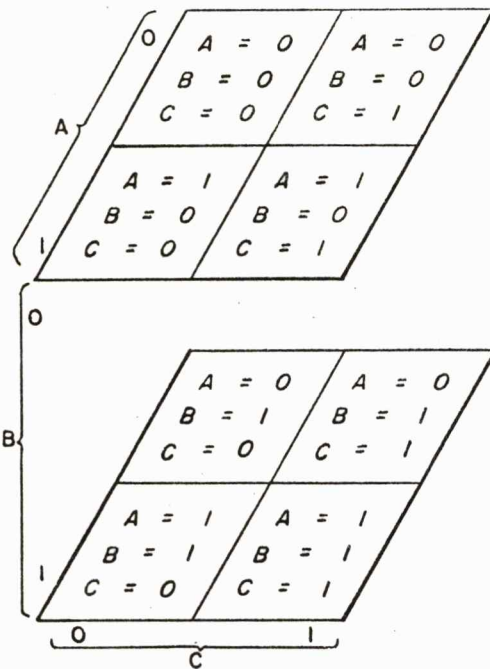
93.



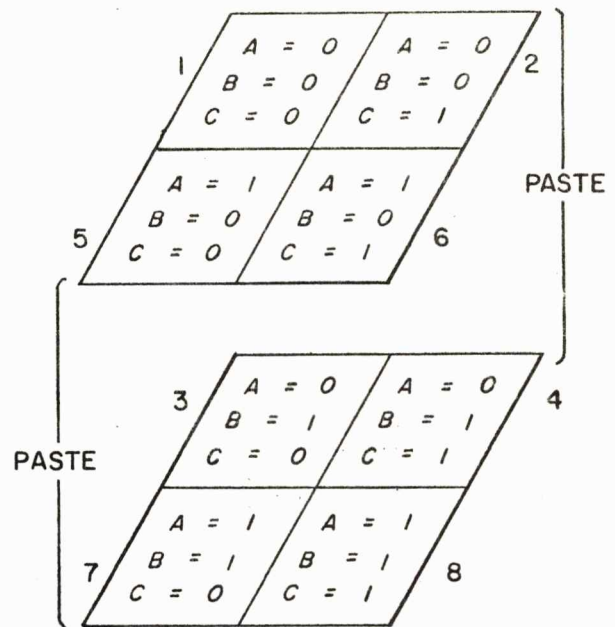
By illustrating the three variables in two planes we can fill in each square to each combination of the three variables. As shown in the upper plane, top-left corner, A = 0, B = 0 and C = 0. For the top-right corner A = 0 and B = 0, but here we are on the 1 side of C.

Complete the illustration by filling in each of the remaining four combinations on the lower plane.

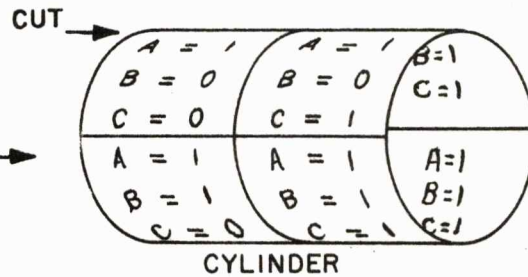
93.



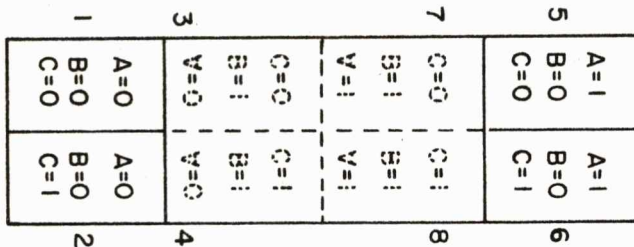
94.



To unfold the cube-shaped map, we paste the two ends to form a cylinder.



Next we cut the cylinder along the line, dividing blocks 1 and 2 from blocks 5 and 6.



Then we roll the cylinder out flat, turning it 90°.

This gives us a three variable Karnaugh map in one plane.

Note carefully that in unrolling the cylinder the binary combinations of AB are 00, 01, 11 and 10. (Normally binary values would be listed in order; 00, 01, 10 and 11.) Note too that the adjacencies in the cube provide the block numbering arrangement shown.

C	AB			
	00	01	11	10
0	1	3	7	5
1	2	4	8	6

(Proceed to the next frame)

95.

		AB			
C		00	01	11	10
	0	1	3	7	5
	1	2	4	8	6

The Karnaugh map shown above can be used to minimize the three variable expression $\overline{A}\overline{B} + AB\overline{C} + A\overline{B}C = D$.

To show an output for the first term, $\overline{A}\overline{B}$, since $\overline{A} = 1$ then $A = 0$; and $\overline{B} = 1$, then $B = 0$; this indicates an output at block 1.

Note Carefully that with only two terms ($\overline{A}\overline{B}$) the output is 1 regardless of the value of C, therefore we indicate an output in both blocks 1 and 2.

For the term $AB\overline{C}$: $A = 1$; $B = 1$; $\overline{C} = 1$, then $C = 0$; this indicates an output in block 7.

You indicate the output for the term $A\overline{B}C$.

95.

		AB			
C		00	01	11	10
	0	1	3	7	5
	1	2	4	8	6

$A\overline{B}C = \text{Block 6}$

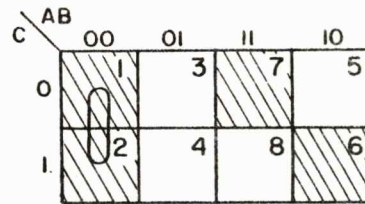
96.

		AB			
C		00	01	11	10
	0	1	3	7	5
	1	2	4	8	6

The map tells us that blocks 1 and 2 are vertically adjacent. Return to frame 94 and corroborate the fact that they are adjacent (horizontally). The shaded blocks 1 and 2 indicate we will get an output when the inputs are $\overline{A}\overline{B}\overline{C}$ or $\overline{A}\overline{B}C$. However, $C + \overline{C} = 1$, any variable having both 1 and 0 in an adjacency can be dropped, thus the map tells us that regardless of the condition of the input to variable C, whenever we have the inputs $\overline{A}\overline{B}$ we (will/will not) have an output.

96. will

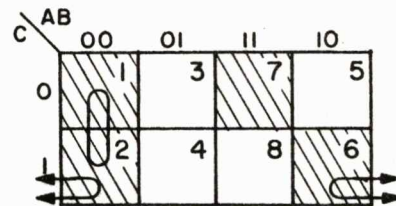
97.



The map also tells us we will have an output when we have inputs ABC , this is indicated by block (s) _____.

97. 7

98.



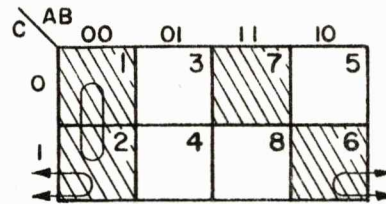
So far we have determined from the map that we will have an output whenever the input is $\bar{A}\bar{B}$, or ABC .

Not readily apparent from the map is the fact that blocks 2 and 6 are actually adjacent. Return to frame 94, note that blocks 2 and 6 (also 1 and 5) are adjacent to each other. This means that in a three-variable map when both end blocks (1 and 5, or 2 and 6) are shaded, this too indicates an output.

This tells us that inputs of $\bar{A}\bar{B}C$, block 2, or the inputs for block 6 of _____, will also provide an output.

98. $\overline{A}\overline{B}C$

99.



Reviewing the inputs required for blocks 2 and 6 we have: $\overline{A}\overline{B}C$ or $A\overline{B}C$.

It makes no difference what value variable A has, the inputs required for an output are $\overline{B}C$.

The map for the expression $\overline{A}\overline{B} + A\overline{B}C + A\overline{B}C = D$ had indicated to us that to get an output the inputs can be $\overline{A}\overline{B} + A\overline{B}C + \overline{B}C$.

Karnaugh maps cannot factor, therefore we can further reduce the expression $\overline{A}\overline{B} + A\overline{B}C + \overline{B}C$ by factoring out \overline{B} .

The final expression then becomes _____.

99. $\overline{A}\overline{B} + A\overline{B}C + \overline{B}C$
 $= \overline{A}\overline{B} + \overline{B}C + A\overline{B}C$
 $= \overline{B}(\overline{A} + C) + A\overline{B}C$

100. Reviewing the use of the three variable Karnaugh map for the expression $\overline{A}\overline{B} + A\overline{B}C + A\overline{B}C$.

The minimal inputs required for an output are $\overline{B}(\overline{A} + C)$, or, $A\overline{B}C$, expressed as: $\overline{B}(\overline{A} + C) + A\overline{B}C$

(Proceed to the next frame)

101. To draw a Karnaugh map of 4 variables we need 2^4 (16) blocks. These blocks are for all possible binary combinations of the 4 variables. The 16 combinations can be listed in binary order as shown.

Note that we have shown A as representing the least significant digit, B the next most significant digit, etc.

D C B A

0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
- - - -
- - - -
- - - -
- - - -
- - - -
- - - -

You fill in the remainder of the binary listing.

101. D C B A

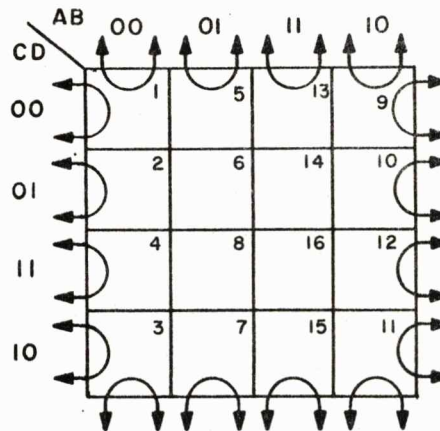
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1

102. A 4 variable Karnaugh map starts as a four-dimension cube, which can be converted to a doughnut shape (torus). The torus can be sliced at one point and opened to form a cylinder. The cylinder can be slit across its length and folded flat to form the following map.

AB		00	01	11	10
CD	00	1	5	13	9
	01	2	6	14	10
	11	4	8	16	12
	10	3	7	15	11

(Proceed to the next frame)

103.



Note that unfolding the four-dimension cube again provides a binary arrangement of 00, 01, 11, and 10. Note too that the adjacencies in the four-dimension cube also provide a different block numbering arrangement.

In addition to normal adjacencies, the loops shown on the map above illustrate that all the blocks on top and bottom, and the blocks on the left and right sides are _____.

103. adjacent

104. As an example let us place the following expression on a 4 variable Karnaugh map.

$$\bar{A}B + A\bar{B}C + \bar{A}\bar{B}\bar{C}\bar{D}$$

	AB			
CD	00	01	11	10
00	1	5	13	9
01	2	6	14	10
11	4	8	16	12
10	3	7	15	11

The term $\bar{A}B$ indicates that an output will be obtained regardless of whether C or D is present or not. To indicate this we shade blocks 5, 6, _____, and _____.

104. 7 and 8
(or vice versa)

105.

$$\bar{A}B + A\bar{B}C + \bar{A}\bar{B}\bar{C}\bar{D}$$

AB \ CD	00	01	11	10
00	1	5	13	9
01	2	6	14	10
11	4	8	16	12
10	3	7	15	11

The term $A\bar{B}C$ indicates an output for either $A\bar{B}CD$ or $A\bar{B}C\bar{D}$. The output for $A\bar{B}CD$ is indicated by shading block 12. To indicate an output for $A\bar{B}C\bar{D}$ we shade block _____.

105. 11

106.

$$\bar{A}B + A\bar{B}C + \bar{A}\bar{B}\bar{C}\bar{D}$$

AB \ CD	00	01	11	10
00	1	5	13	9
01	2	6	14	10
11	4	8	16	12
10	3	7	15	11

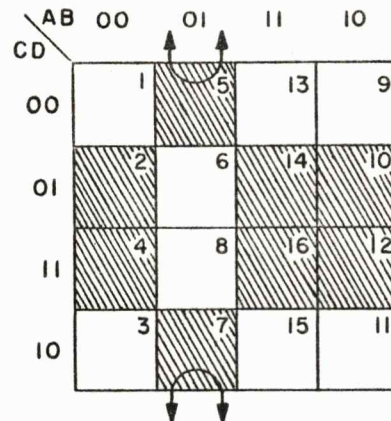
The output for the term $\bar{A}\bar{B}\bar{C}\bar{D}$ is indicated by shading block 1 to complete the map.

In a 4 variable Karnaugh map we loop all adjacencies in quantities of 2, 4, and 8. (Note that a single shaded block still represents an output for the same term indicated by the location of the shaded block.)

For reasons to be explained later we always try for the largest number of adjacencies in a loop. For example, we could have loops through blocks 5 and 6, and again through blocks 7 and 8; however, it is preferable to loop all four blocks.

(Proceed to the next frame)

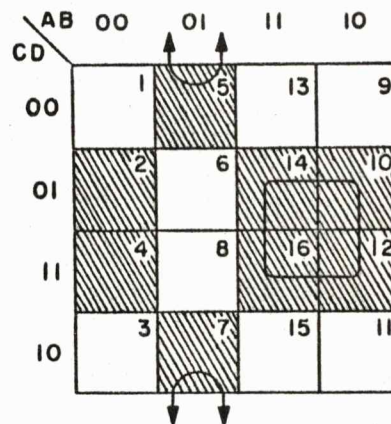
107. We can write the minimum expanded function by visual inspection of the adjacencies as indicated by loops, and writing the minimum term for each loop. We will use the Karnaugh map shown below as an example.



Starting with visual inspection of the loop for blocks 5 and 7 we find that block 5 is $\bar{A}BCD$, block 7 is $ABCD$. Visual inspection tells us that any variable having both 1 and 0 in an adjacency can be dropped. Blocks 5 and 7 thus reduces to a minimum term of _____.

107, $\bar{A}B\bar{D}$

108.

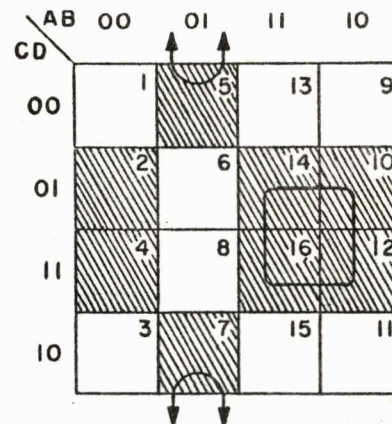


Visual inspection of the four adjacent blocks, 14, 10, 16, and 12, shows the following. Looking first at the horizontal adjacencies of AB, we find for blocks 14 and 10 that both require A, since they also require B and \bar{B} , and since $B + \bar{B} = 1$, we can drop B. This also holds true for blocks 16 and 12.

Visual inspection thus tells us that for the adjacencies of AB, (blocks 14 and 10, and blocks 16 and 12) to have an output we need apply only the variable _____.

108. A

109.

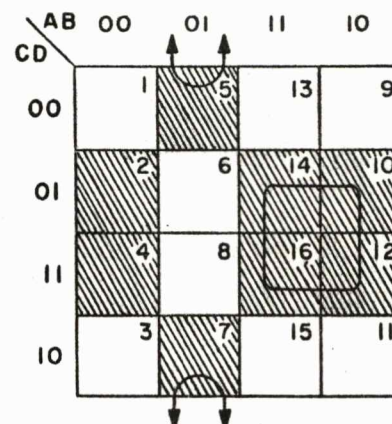


The next step is a similar visual inspection of blocks 14, 16, 10 and 12 for the vertical adjacencies of CD. We find blocks 14 and 16 both require D, and C and \bar{C} can be dropped. This also holds true for blocks 10 and 12.

Visual inspection thus tells us that for the adjacencies of CD, blocks 14, 16, 10 and 12 require an input of the variable _____.

109. D

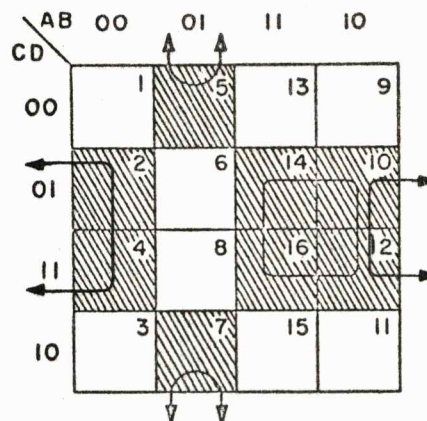
110.



Reviewing the past two frames, we found that for blocks 14, 10, 16 and 12 the adjacencies of AB required only an A. The adjacencies of CD required only a D. Thus the map has allowed us to visually note that the minimum inputs that will provide an output for blocks 14, 10, 16 and 12 are _____.

110. AD

111.

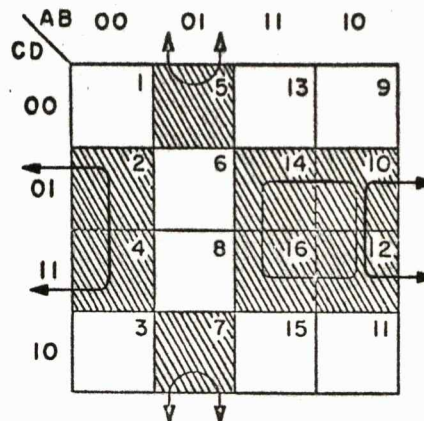


The two previous explanations for reducing a loop of 2 and 4 adjacencies has illustrated the following. Reducing a loop of 2 adjacent blocks (5 and 7) provided a reduction to 3 variables. Reducing a loop of 4 adjacent blocks (14, 10, 16 and 12) provided a reduction to 2 variables. This tells us that it is preferable to try to keep loops in groups of 4 since they reduce to 2 variables.

Having made a loop of 4 with blocks 14, 10, 16 and 12 does not prevent our looping blocks 10 and 12 with blocks 2 and 4 for another loop of 4. This gives us the advantage of being able to reduce to _____ variables.

111. 2

112.

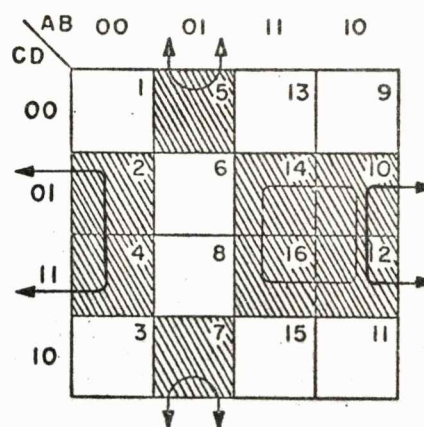


To visually minimize blocks 10, 2, 12 and 4, we can first check the adjacencies of AB for blocks 10 and 2. These show us that A is 1 or 0 and can be dropped, but B is 0 or 0, giving us \bar{B} . The same holds true for blocks 12 and 4.

Checking the adjacencies of CD for blocks 10, 2, 12, and 4, we find that it reduces to D. Thus blocks 10, 2, 12 and 4 can be minimized to the term _____.

112. $\bar{B}D$

113.



Reviewing, we find that the three loops shown above have provided the following minimal expression.

$$\bar{A}\bar{B}\bar{D} + AD + \bar{B}D$$

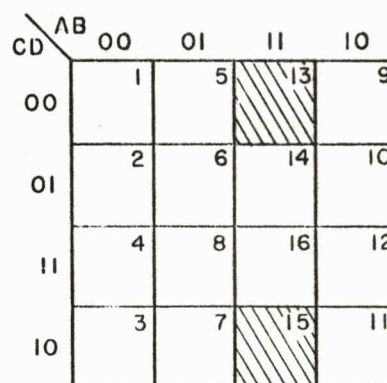
We can if we desire reduce the expression by one term by factoring D out of the last two terms to give us:

$$\bar{A}\bar{B}\bar{D} + D(A + \bar{B})$$

(Proceed to the next frame)

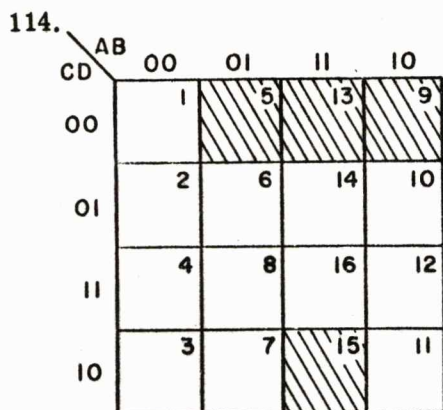
114. To further illustrate the use of a 4 variable Karnaugh map we can use it to reduce the following expression.

$$AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$$



The input $AB\bar{D}$ tells us that we will have an output for $ABC\bar{D}$ or $AB\bar{C}\bar{D}$, thus we shade blocks 15 and 13.

As a first step you shade the blocks for the terms $A\bar{C}\bar{D} + B\bar{C}\bar{D}$

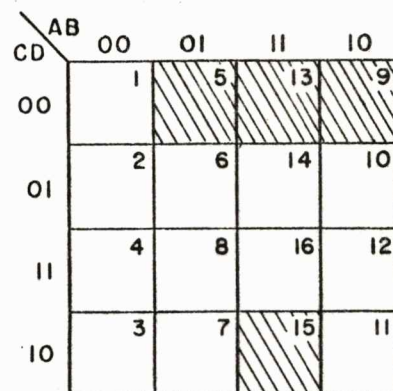


$A\bar{C}\bar{D}$ = blocks 13 and 9

$B\bar{C}\bar{D}$ = blocks 13 and 5

115.

$$AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$$

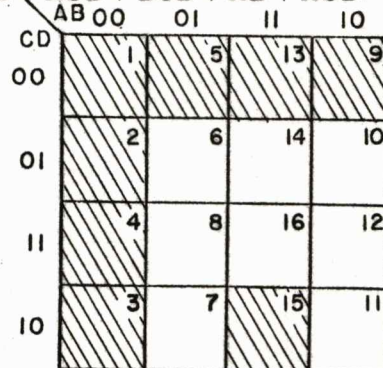


The term $\bar{A}\bar{B}$ tells us that it makes no difference what value CD takes, thus we can shade blocks

115. 1, 2, 4, and 3

116.

$$AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$$

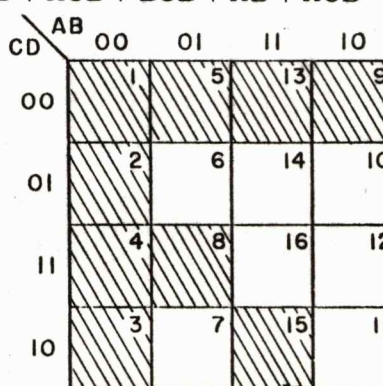


The last term is $\bar{A}CD$, for this term we will shade blocks

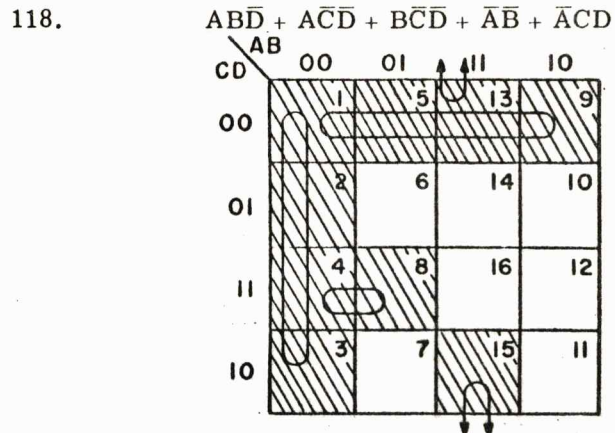
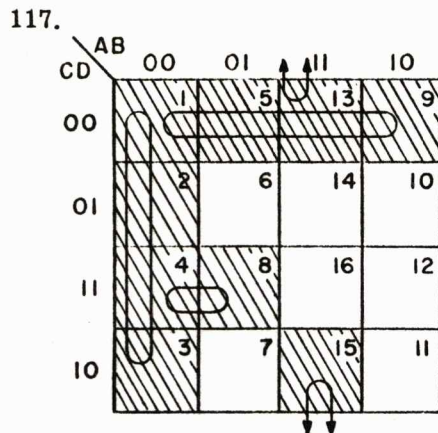
116. 4 and 8

117.

$$AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$$



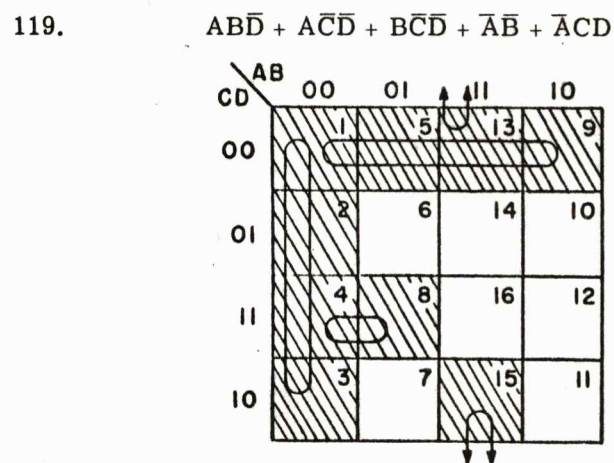
Draw the loops to show all adjacencies of the finished map.



Taking first the adjacencies of blocks 1, 2, 4, and 3. For adjacencies of AB, we have $\bar{A}\bar{B}$ in all four blocks. For adjacencies of CD, in blocks 1 and 2 we have \bar{D} and D, which we drop, leaving \bar{C} . For blocks 4 and 3 we drop D and \bar{D} , leaving C. Again, C and \bar{C} can be dropped, telling us that the minimum term for blocks 1, 2, 4, and 3 is $\bar{A}\bar{B}$.

For the loop of four blocks of 1, 5, 13, and 9, we can see that it reduces to a minimum term of _____.

118. $\bar{C}\bar{D}$

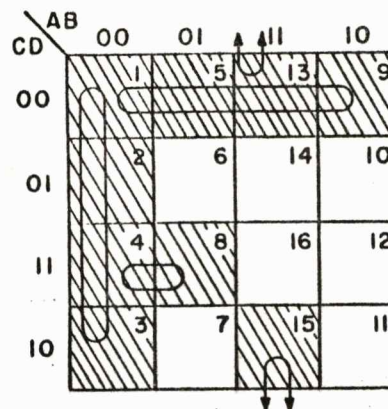


To minimize blocks 4 and 8 for adjacencies of AB, we find both blocks require \bar{A} . For the adjacencies of CD we find both blocks require CD. Therefore, blocks 4 and 8 reduce to the minimum term of _____.

119. $\bar{A}CD$

120.

$$AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$$

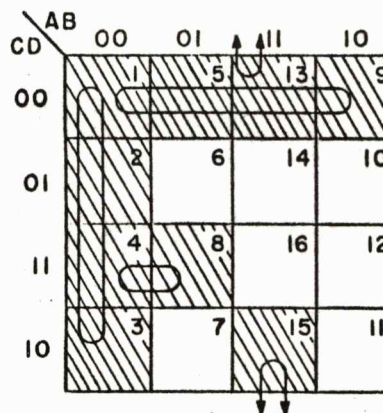


Visualizing the loop for blocks 13 and 15 gives us the minimum term of _____.

120. $AB\bar{D}$

121. Reviewing, we find that using the Karnaugh map we were able to say that for the expression $AB\bar{D} + A\bar{C}\bar{D} + B\bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}CD$ the minimum inputs required were:

$$\bar{A}\bar{B} + \bar{C}\bar{D} + \bar{A}CD + AB\bar{D}$$



This completes Boolean Algebra.

APPENDIX A

BOOLEAN ALGEBRA THEOREMS

$$\begin{array}{ll} A + 0 = A & A0 = 0 \\ A + 1 = 1 & A1 = A \\ A + A = A & AA = A \\ A + \bar{A} = 1 & \bar{A}A = 0 \end{array}$$

$$\begin{array}{l} A + B = B + A \\ AB = BA \\ A + (B + C) = A + B + C \\ A(BC) = (AB)C \\ A(A + B) = A \\ A + AB = A \\ A(\bar{A} + B) = AB \\ A + \bar{A}B = A + B \\ \bar{A}(A + B) = \bar{A}B \\ \bar{A} + AB = \bar{A} + B \\ (A + B)(\bar{A} + C) = AC + \bar{A}B \\ \overline{AB} = \bar{A} + \bar{B} \\ \overline{A + B} = \bar{A}\bar{B} \\ AB = \overline{\bar{A} + \bar{B}} \\ A + B = \overline{\bar{A}\bar{B}} \\ \overline{AB + CD} = (\bar{A} + \bar{B})(\bar{C} + \bar{D}) \\ \overline{(A + B)(C + D)} = \bar{A}\bar{B} + \bar{C}\bar{D} \\ (A + B)(A + \bar{B}) = A \\ AB + A\bar{B} = A \\ A + BC = (A + B)(A + C) \\ A(B + C) = AB + AC \end{array}$$

VOLUME IV
DIGITAL TECHNIQUES
AND LOGIC

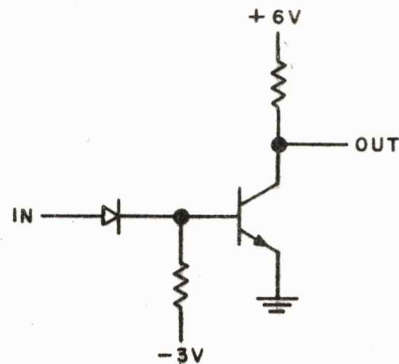
1. Logic is defined as an orderly progression of steps to the solution of a problem. Computer logic involves circuits arranged in such a configuration that the orderly progression of steps to the solution of a problem can be achieved.

(Proceed to the next frame)

2. Practically all computers use binary arithmetic to solve problems. As you recall, binary uses two digits which are _____ and _____.
2. 1 and 0
(vice versa)
3. There are many different ways of representing 1's and 0's but the most common way is to let a binary 1 be represented by one voltage level and to let a binary 0 be represented by another voltage level. Therefore if we let the relatively positive level represent a 1 then the 0 will be represented by a relatively _____ voltage.
3. negative
4. In a system using voltage levels of + 6 and -6 volts, if the 1 is represented by the +6 volt level then the 0 will be represented by the _____ volt level.
4. -6
5. The 1 is not always represented by the relatively positive level. In many computers the relatively negative level is used to represent 1. Therefore we can say that 1 may be represented by either the relatively _____ or _____ level.
5. positive -- negative
or vice versa
6. It is common practice to use 0 volts or ground for one of the voltage levels and therefore only require one power supply. This is possible because we are dealing with DC levels, and 0 volts into the base of a transistor will turn-on or turn-off the transistor depending on the emitter voltage and type of transistor.

(Proceed to the next frame)

7. In the circuit shown, if + 6 volts represents 1 and 0 volts represents 0, the output will be a 1 when the input level is _____ volts (0 or +6).



7. 0 volts

8. The DC levels used to represent 1's and 0's are called logic levels. Therefore, we have a positive logic level and a _____ logic level.

8. negative

9. If the 1 is represented by the positive logic level, the computer is said to use positive logic, so in a computer using positive logic and levels of +3 volts and 0 volts a 1 will be represented by _____ volts.

9. +3

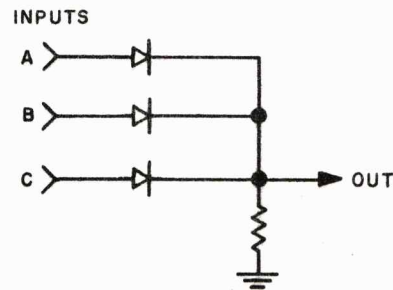
10. If the 1 is represented by the negative logic level, the computer is said to use negative logic. So in a computer where the levels are -3 volts and 0 volts if 1 is represented by -3 volts the computer uses _____ logic.

10. negative

11. The circuits used to solve a problem in an orderly progression of steps are called logic circuits. There are four basic logic circuits. They are the AND, OR, NOT, and INHIBIT circuits. The AND, OR and INHIBIT circuits are also called gates because the output will be gated when the required input conditions are fulfilled.

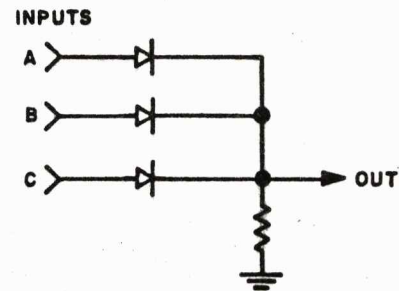
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12. In the gating circuits which follow we will consider input and output levels to be either a ground (binary 0) or a positive level (binary 1). In this circuit a positive level (1) at any one of the three inputs causes that diode to conduct, producing a _____ at the output.



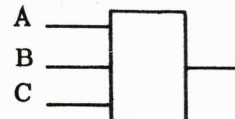
12. positive level or (1)

13. Since a 1 at either A or B or C causes an output 1, this circuit is called an _____ gate.

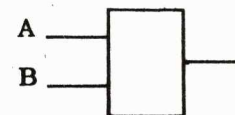


13. OR

14. In Apollo logic diagrams we use the symbol



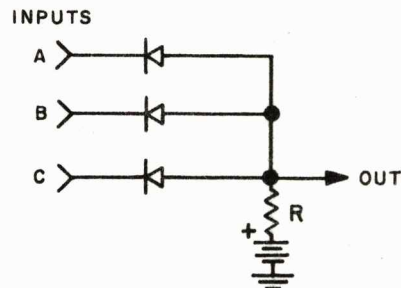
in place of the schematic representation of an OR gate. The symbol



represents an _____ gate with only _____ inputs.

14. OR -- 2

15. Here we have a different circuit. Note that the diodes are reversed and that the bottom of R goes to a +E supply instead of to ground. To get a 1 output from this circuit we must have 1's at all three inputs. That is, if any input is at ground (0) the output is clamped to _____.

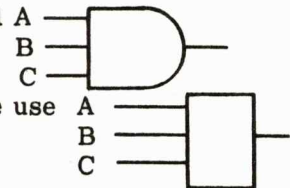


15. ground or 0

16. Since we must have 1's at inputs A and B and C in order to have a 1 output, this circuit is called an _____ gate.

16. AND

17. We will use the logic symbol A B C for the AND gate, just as we use A B C for the _____ gate.



17. OR

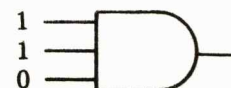
18. For simplicity we have shown only three inputs to the OR and AND gates. In practice any number (2 or more) of inputs can be used. If an AND gate has 7 inputs, _____ input 1's are required for a 1 output.

18. 7

19. To get a 1 output from an 8 input OR circuit, we need _____ 1 input(s).

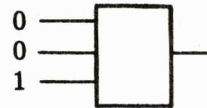
19. one

20. Let's make sure you have these two gates fixed and separated in your mind. This is an _____ gate. Its output, with the inputs shown, is a _____.



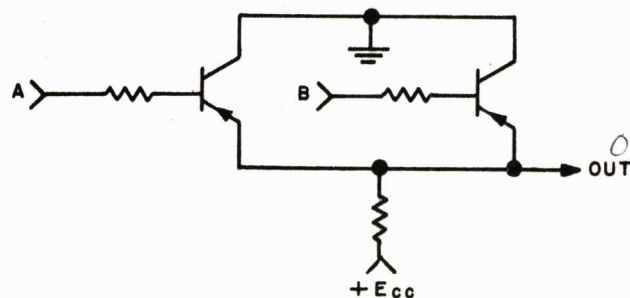
20. AND -- 0

21. And this is an _____ gate with a _____ output.



21. OR -- 1

22. AND and OR gates may use transistors instead of diodes. In this circuit if either transistor is conducting the output is clamped to ground and is therefore a _____ (1/0).

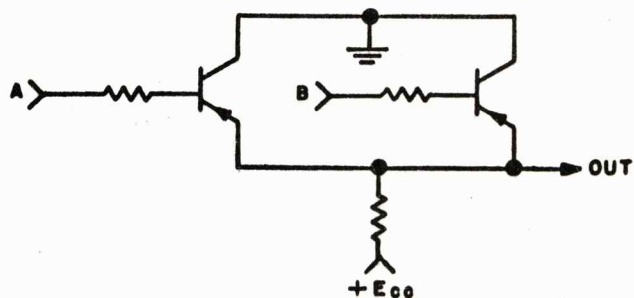


22. 0

23. To get a 1 output requires that both transistors be in _____ (conduction/cut-off).

23. cut-off

24. To cut off one of these transistors it is necessary that its input be a little more positive than $+E_{CC}$ or a _____ (1/0).

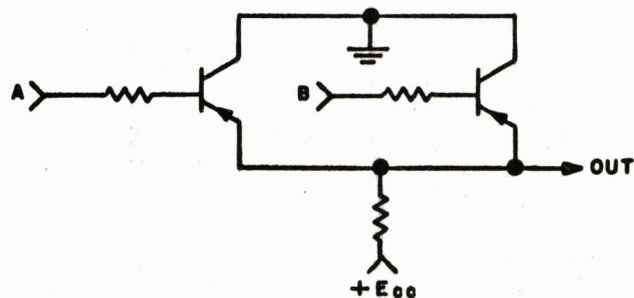


24. 1

25. Therefore, we get a 1 output only when A is _____ (1/0) and B is _____ (1/0).

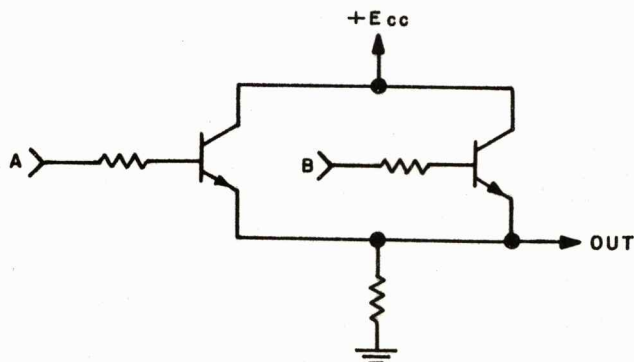
25. 1 -- 1

26. This, then, is an _____ gate.



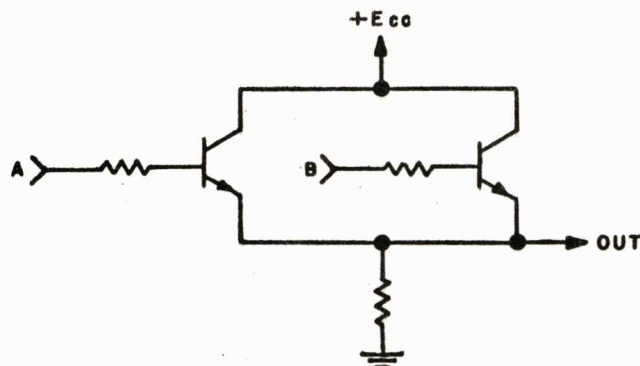
26. AND

27. This circuit differs from the previous one in that it uses NPN transistors and has $+E_{CC}$ and ground interchanged. If A is 1 and B is 0 or vice versa, the output is _____.



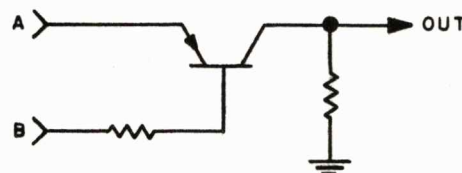
27. 1

28. This, then, is an _____ gate.



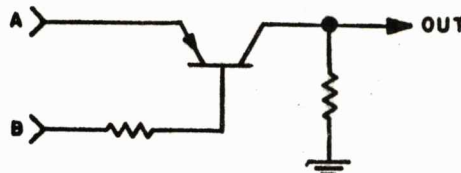
28. OR

29. In this circuit if A and B are both 0 (ground potential) the transistor _____ (will/will not) conduct and the output will be a _____.



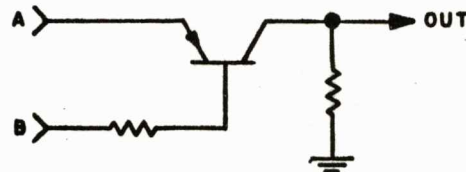
29. will not
0

30. And if A and B are both 1 (same positive potential) the output will be _____.



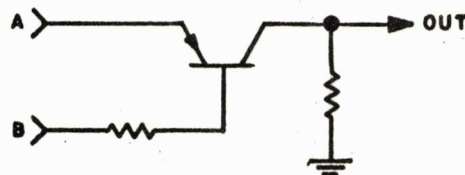
30. 0

31. But if A is 1 and B is 0, the emitter junction is _____ biased, conduction _____ (does/does not) take place and the output is _____.




31. forward -- does -- 1

32. That is, if B is a 1, it inhibits the output of this gate, regardless of the input to A. Therefore, we call this an _____ gate.




32. INHIBIT

33. Since a 1 output requires a 1 at A and a 0 at B, this INHIBIT gate can be thought of as a variation of the AND gate. We can use the symbol

A  where the small circle o indicates

that a 0 is required at this input for a 1 output.

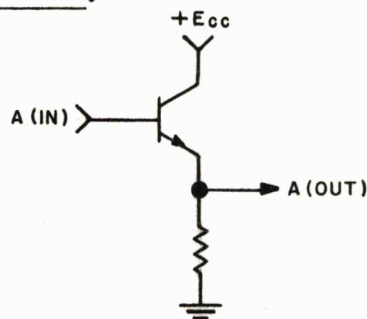
Similarly, a 1 output from this inhibit gate,

A  requires a _____ at A and a

_____ at B.

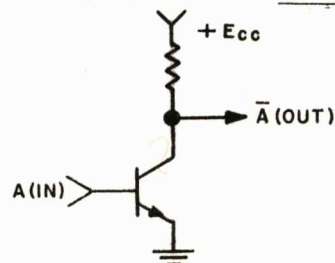
33. 0 at A -- 1 at B

34. If a 0 to input A produces an output 0, and a 1 to input A produces an output 1, as in this emitter follower circuit, we can call the output A. Likewise, if the input were labeled B, the output would be _____.



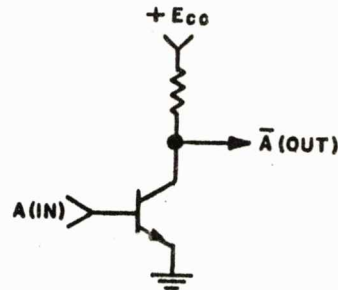
34. B

35. However, with a common-emitter circuit we have inversion. That is, a 0 input produces a _____ output, and a 1 input produces a _____ out.



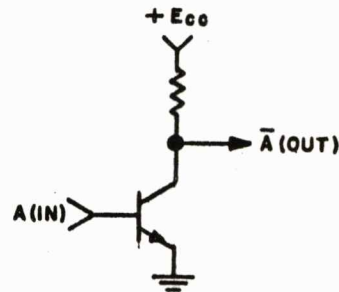
35. 0 produces 1
1 produces 0

36. To indicate that an output was caused by an A input, but has been reversed, we label the output NOT A, written \bar{A} . If the input were labeled B, the output would be _____.



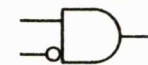


36. NOT B or \bar{B}

37. Since A input gives NOT A output and B input gives NOT B output, etc., this circuit is called a _____ circuit.



37. NOT

38. The symbol for a non-inverting amplifier (emitter follower) is . The symbol for the NOT circuit is . As in the symbol for the INHIBIT gate,  the small circle (o) indicates an inversion. That is, a _____ is required at the input of the NOT circuit for an output 1.

38. 0

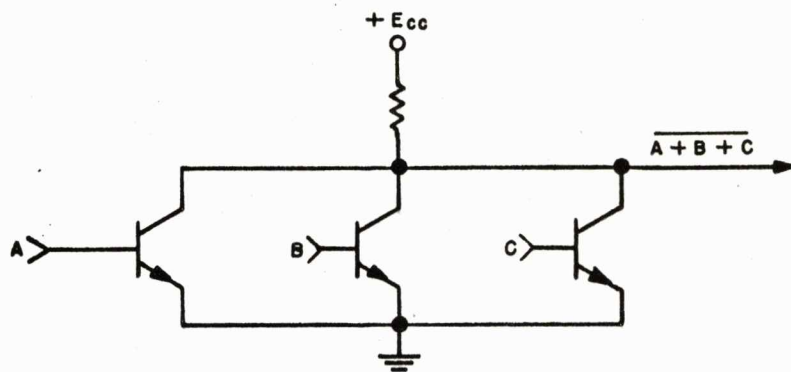
39. In the gates just discussed we saw that certain conditions must be met in order to produce a 1 output. For an AND gate, all inputs must be conditioned with 1's. For an OR gate, only one input needs to be _____ with a 1.

39. conditioned

40. The conditioning levels for an INHIBIT gate to produce an output of 1 are the INHIBIT input is a _____ (0 or 1) and all of the other inputs _____.

40. 0 -- 1

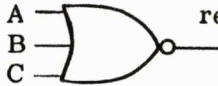
41. Here is a circuit we can use to generate all four of the functions just discussed (AND, OR, NOT, INHIBIT). Note that a 1 input to any of the transistors results in a _____ output.



41. 0

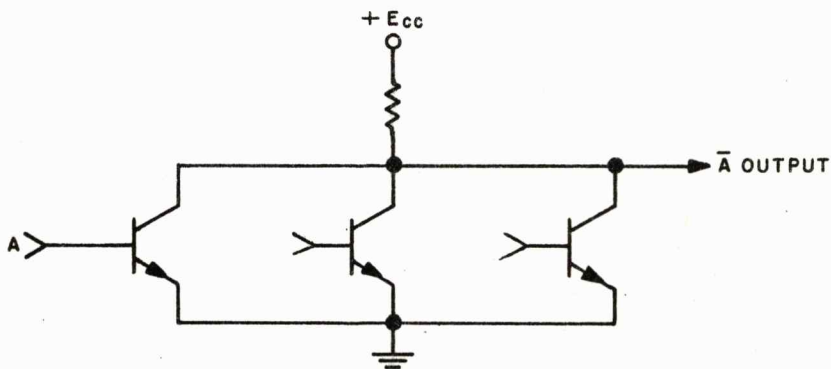
42. The output is 1 only if neither A nor B nor C is a 1. Therefore it is called a _____ gate.

42. NOR

43. The symbol  represents a three input NOR gate. As in the NOT and INHIBIT circuits, the o signifies _____.

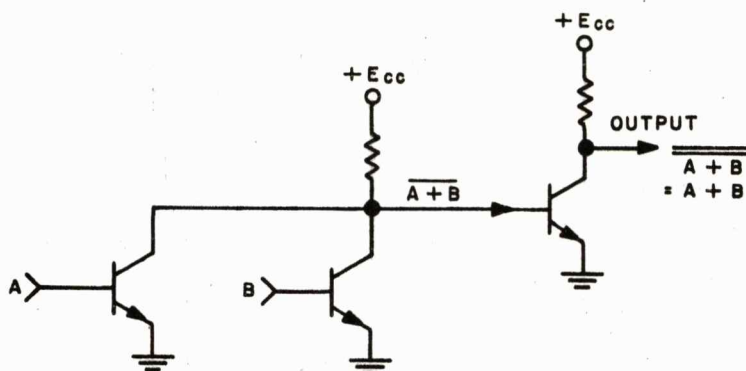
43. inversion, complementing, notting

44. Now let's see how one basic circuit, the NOR, can be used to generate NOT, OR, AND and INHIBIT functions. By using only one input to a NOR gate, illustrated below, the _____ function is generated.



44. NOT

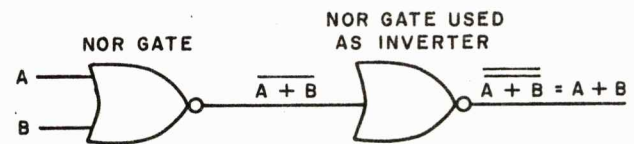
45. Here we have a two input NOR with the output complemented by a NOT circuit. This gives us the complemented NOR function or simply the _____ function, as indicated in the diagram below.



45. OR

46. This truth table shows in another fashion that the complemented NOR function equals the _____ function.

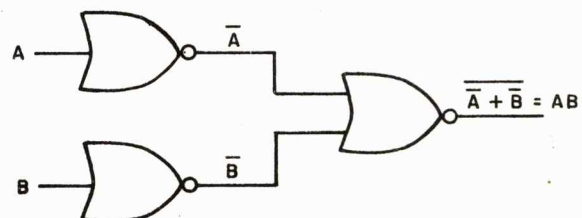
Inputs		Output	
A	B	$\overline{A + B}$	$\overline{\overline{A + B}} = A + B$
0	0	1	0
1	0	0	1
1	1	0	1
0	1	0	1



46. OR

47. Complementing all the inputs to a NOR gate, as shown below, generates the AND function. To confirm this statement, complete the truth table.

Inputs		Output		
A	B	\overline{A}	\overline{B}	$\overline{\overline{A} + \overline{B}} = AB$
0	0			
1	0			
1	1			
0	1			

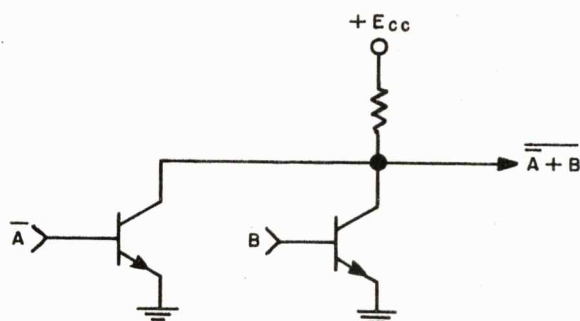


47.

Inputs		Output		
A	B	\bar{A}	\bar{B}	$\bar{A} + \bar{B} = \overline{AB}$
0	0	1	1	0
1	0	0	1	0
1	1	0	0	1
0	1	1	0	0

48. Let us assume that we have available to us a complemented input, it could be either \bar{A} or \bar{B} , and it could be from either a preceding NOR gate or any other inverting circuit. This allows us to use the simple NOR circuit shown below for other purposes. Complete the truth table and note that the output is $\bar{A} + B$.

Inputs		Output	
\bar{A}	B	$\bar{A} + B$	$\overline{\bar{A} + B}$
1	0		
0	0		
0	1		
1	1		



48.

Inputs		Output	
\bar{A}	B	$\bar{A} + B$	$\overline{\bar{A} + B}$
1	0	1	0
0	0	0	1
0	1	1	0
1	1	1	0

49. But $\bar{A} + B = \bar{A}\bar{B} = A\bar{B}$, as confirmed by comparing the truth table below with the completed truth table of the previous frame.

A	B	$\bar{A} \cdot \bar{B}$	$A \cdot \bar{B} = \bar{A} + B$
0	0	$0 \cdot 1 =$	
1	0	$1 \cdot 1 =$	
1	1	$1 \cdot 0 =$	
0	1	$0 \cdot 0 =$	

49.

A	B	$\bar{A} \cdot \bar{B}$	$A \cdot \bar{B} = \bar{A} + B$
0	0	$0 \cdot 1 =$	0
1	0	$1 \cdot 1 =$	1
1	1	$1 \cdot 0 =$	0
0	1	$0 \cdot 0 =$	0

50. So we see that regardless of input \bar{A} , whenever input B is a 1 the output will be 0. Therefore, this NOR gate performs the INHIBIT function, and input B is the _____ input.

Inputs		Output	
\bar{A}	B	$\bar{A} + B$	$\overline{\bar{A} + B} = A\bar{B}$
1	0	1	0
0	0	0	1
0	1	1	0
1	1	1	0

50. INHIBIT

51. To summarize the logic functions that can be generated by a NOR gate, fill in the logic function performed by a three input NOR gate for each set of input conditions below.

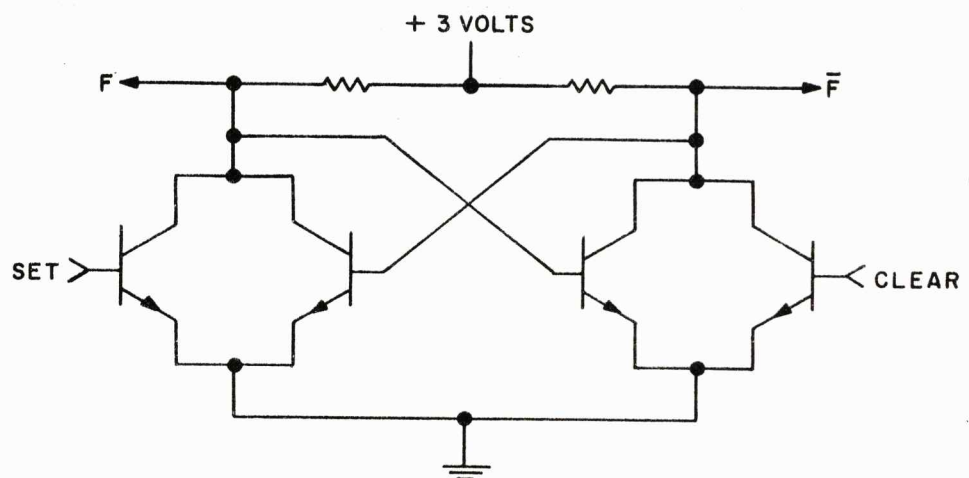
Inputs	Logic Function
$\bar{A}, \bar{B}, \bar{C}$	_____
\bar{A}, \bar{B}, C	_____
A only	_____
A, B, C (Output notted)	_____

51. AND
INHIBIT
NOT
OR

52. By combining the outputs and inputs of two NOR circuits the NOR circuits can also be used as a flip-flop. As you recall, the flip-flop consists of two amplifiers with the collector of each amplifier feeding the base of the other amplifier. Due to this collector to base coupling one amplifier will be conducting and the other will be _____.

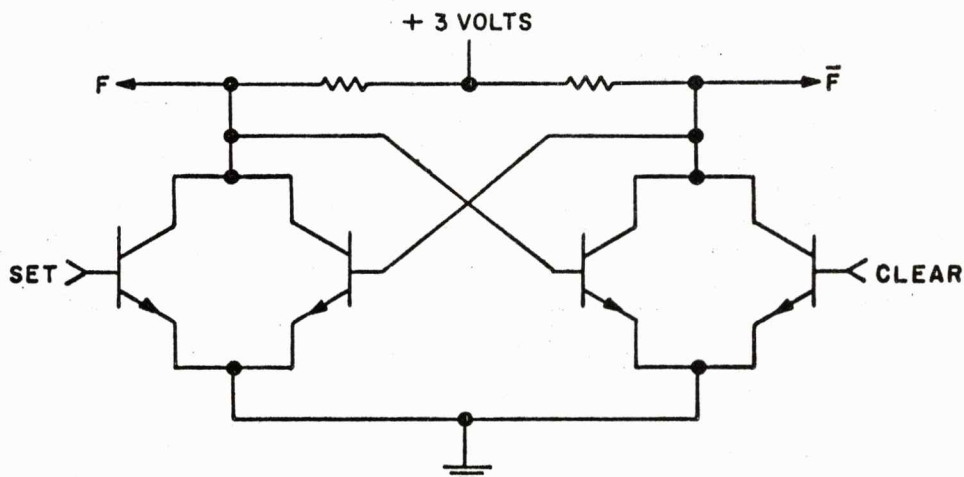
52. cutoff

53. A NOR flip-flop is shown below. The flip-flop consists of two NOR gates each having two inputs. (One of the inputs to each NOR gate is from the output of the other NOR gate. The second input to each NOR gate is external, _____ or _____.)



53. SET
CLEAR

54. If the external inputs to the NOR flip-flop are complementary, any time the SET input equals +3 volts the CLEAR input will equal _____ volts.



54. 0

55. Since one amplifier of the flip-flop is cut-off when the other is conducting, the outputs (F and \bar{F}) are complementary.

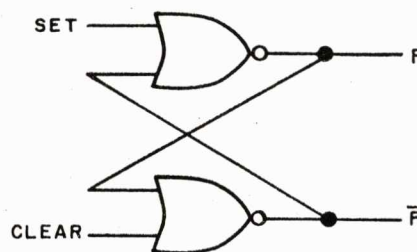
Therefore in the circuit shown, if F equals 0 volts, \bar{F} will equal _____ volts.

55. +3

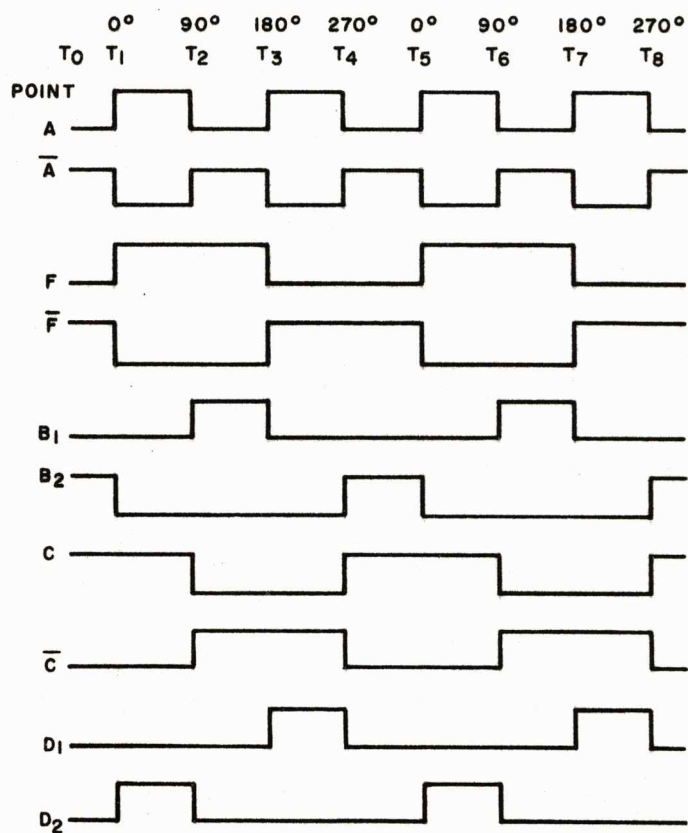
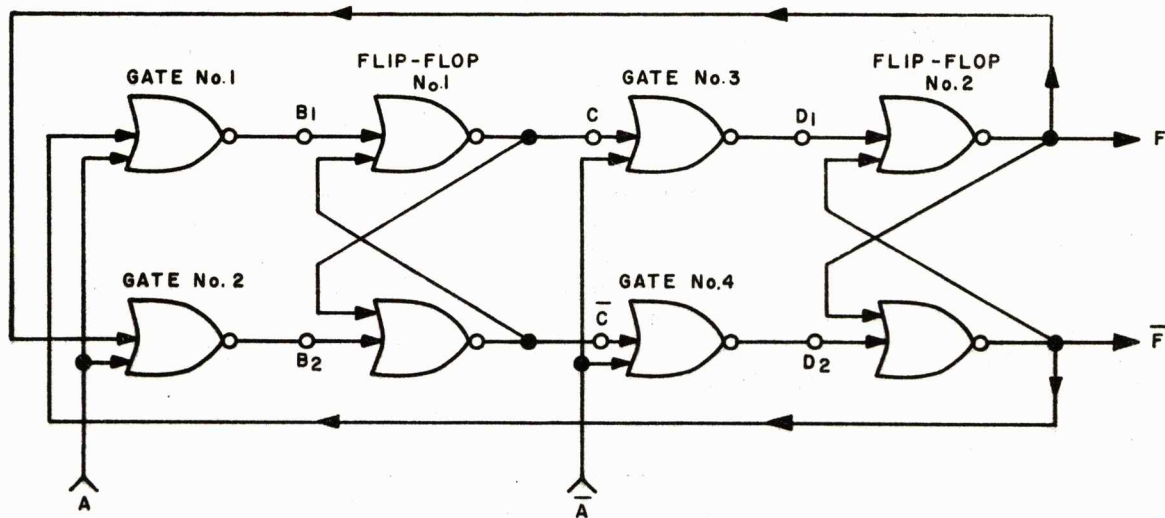
56. Reading the outputs of the circuit shown as binary numbers, if the CLEAR input is a 1, \bar{F} is _____ and F is _____.

56. \bar{F} is 0
 F is 1

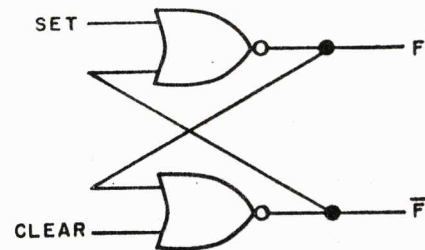
57. The logic symbol showing the two NOR gates used as a flip-flop is:



(Proceed to the next frame)



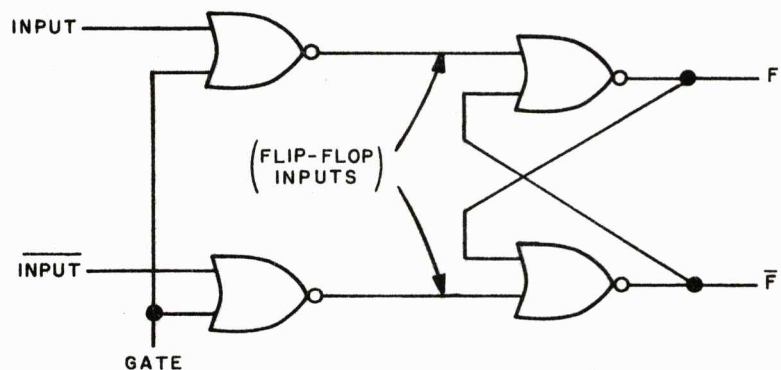
57a. You can see from the logic symbol shown below that the flip-flop will hold, or store its last input until a new input is applied. Because of its bistable nature an important use of a flip-flop is to _____ an input.



57a. STORE

58. One use for the flip-flop is as a storage device. Because of its bistable nature the flip-flop stores the last input until a new input is applied. Many times it is necessary to gate the input as a function of time.

The circuit shown below is a gated flip-flop. A pair of NOR INHIBIT gates are used as the inputs to the flip-flop. We see that whenever the GATE input is a 1, the flip-flop inputs are _____.

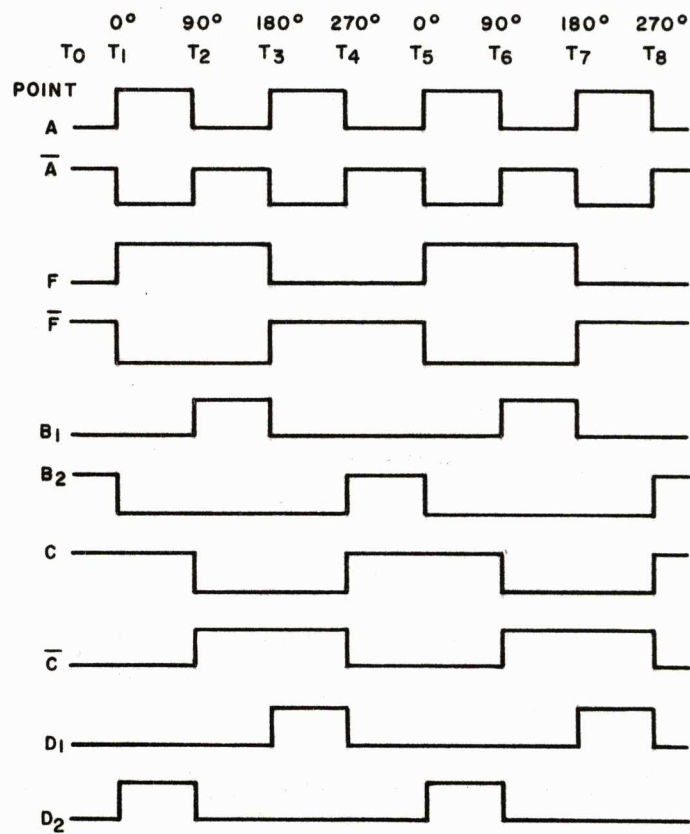
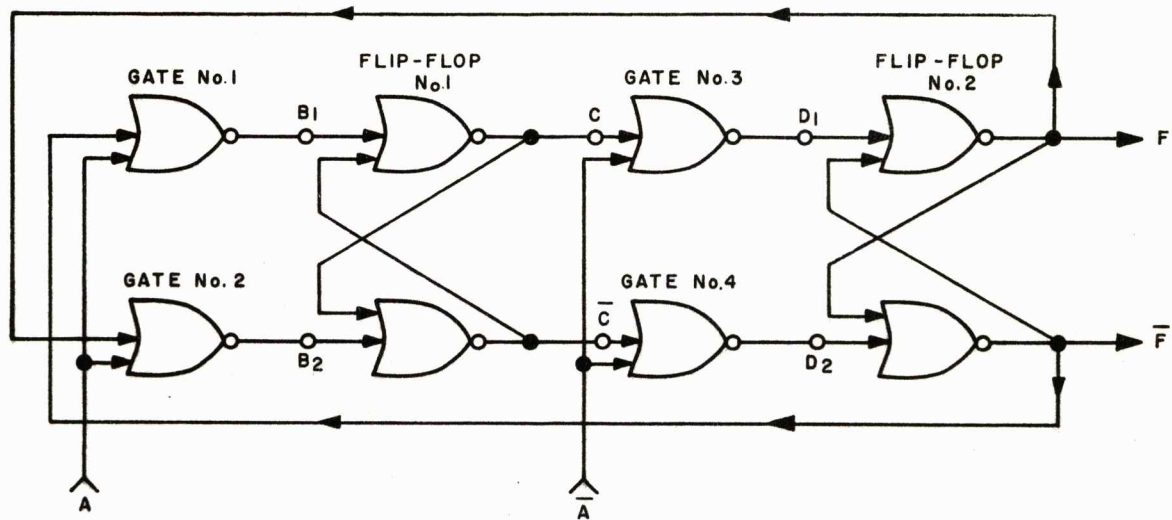


58. 0

59. Therefore we see that so long as the GATE input is a 1 the input to the flip-flop is a 0. Now, if the GATE input goes to a 0, INPUT is a 1, and INPUT is a 0, the flip-flop outputs will be: F = _____ and F-bar = _____.

59. F = 1
F-bar = 0

60. Note that the GATE going to 0 while the input remains the same will not cause the flip-flop to change state. The GATE merely permits (0) or inhibits (1) a change of state when INPUT and INPUT change. Therefore, in the flip-flop shown above the outputs remain F = 1 and F-bar = 0 until GATE = _____, INPUT = _____ and INPUT = _____.



60. GATE = 0
INPUT = 0
INPUT = 1

61. One use for flip-flops is to divide an input frequency into submultiples. A frequency divider, using the gated flip-flops we have just discussed, is shown at the left. Also shown is a timing diagram showing the levels at different points in the circuit in relation to the output.

(Proceed to the next frame)

62. With inputs A and \bar{A} and outputs F and \bar{F} , we see from the timing diagram that the output will complete one cycle when the input has gone through two complete cycles. Therefore, we can say that the input frequency has been divided by a factor of _____.

62. 2

63. If we know the levels of the inputs (A and \bar{A}) and the outputs (F and \bar{F}), we can determine the levels at different points in the circuit. Considering the level at point B₁ in the circuit we see that the inputs to Gate #1 at time T₀ are 0 on input A and 1 from \bar{F} . Therefore, B₁ is a _____ (0 or 1).

63. 0

64. Point B₁ becomes a 1 at times T₂ and T₆ when both inputs to Gate #1 are _____.

64. 0

65. Point B₁ goes to 0 again when A and \bar{F} go to 1 at times _____ and _____.

65. T₃ and T₇.

66. The level at point B₂ changes at different times then at point B₁ but follows the same repetition pattern. The level at point B₂ depends on the levels present at A and _____.

66. F or output F

67. Gate outputs B₁ and B₂ serve as the inputs to Flip-Flop #1. We can see that Flip-Flop #1 changes states only when B₁ or B₂ goes to _____.

67. 1

68. The outputs of Flip-Flop #1 are then applied to Gates #3 and #4 to produce D_1 and D_2 . If we examine the waveforms at D_1 and D_2 we see that they are the same as the waveforms at B_1 and B_2 , but are displaced in time. And if we compare the outputs of Flip-Flop #1 (C and \bar{C}) and Flip-Flop #2 (F and \bar{F}) we see that they too are the same but are displaced in time.

(Proceed to the next frame)

69. phase

69. To put it another way, we can say that the waveforms, at different points in the circuit, are out of phase with one another or that they are _____ shifted.

70. 180°

70. Waves C and \bar{C} are 180° out of phase or \bar{C} is phase-shifted _____ with respect to C .

71. B_1

D_1

B_2

71. For one cycle of output, from time T_1 to time T_5 , there is a phase relationship between the waveforms at points B_1 , B_2 , D_1 , D_2 and the output. We see that D_2 is a 1 for the first 90° of the output cycle, for the second 90° _____ is a 1, for the third 90° _____ is a 1, and for the fourth 90° _____ is a 1.

72. D_2

72. By picking off levels at appropriate points in the divider, external circuits can be gated at 90° intervals. For instance B_1 can be used as a gate at 90° , D_1 at 180° , B_2 at 270° , and _____ at 360° or 0° .

73. Reviewing the divider just discussed we found that it will divide the input frequency by _____.

We also found that by taking outputs from different points in the circuit we can use them to gate operations at specified times or _____ of the output cycle.

73. 2
phases

74. Dividers can be connected in series if higher orders of division are required. The division factor of a series string of dividers is 2^N where N equals the number of dividers. So if there are three dividers in series the division factor is 2^3 or _____.

74. 8

75. In the divider shown below the input frequency is divided by _____.



75. 16

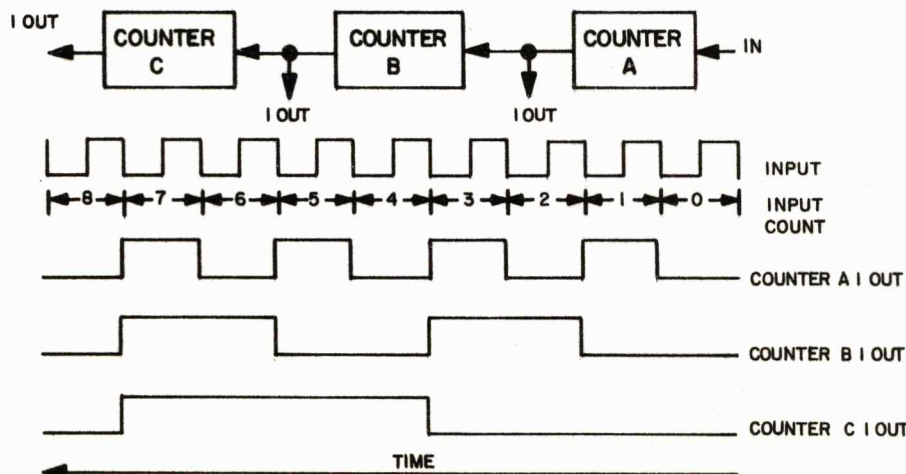
76. The divider output is a square wave which goes through one cycle for a given number of input cycles. Since the divider counts the number of input cycles required to produce one output cycle, it is also referred to as a _____.

76. counter

77. In the divider discussion we said the division factor for a string of dividers is 2^N . Therefore, if we call the divider a counter, the counter is capable of making _____ counts.

77. 2^N

78. As a counter goes through a counting cycle the states of the counters at any time represent a certain count. The count is in reference to the F side of the counter, more commonly referred to as the 1 side of the counter. A truth table for a three-stage counter can be constructed if we draw the waveforms for the 1 side of each counter. The input into the counter is on the right side in order to keep the least significant digit on the right. After studying the illustration complete the truth table by filling in the empty spaces.



TRUTH TABLE

COUNTER			INPUT COUNT
C	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	—	4
1	—	—	5
—	—	—	6
—	—	—	7
—	—	—	8

78. 0
 0 1
 1 1 0
 1 1 1
 0 0 0

79. Now that we have seen how a NOR logic circuit is developed through the use of flip-flops, let's continue the process and develop a logic circuit which will produce an output only for selected counts from a two-stage flip-flop counter. Let's say the outputs from our counter are A and B, and we want circuit outputs when A is 1 and B is 0, or when A is 0 and B is 1, or when A is 0 and B is 0. The first step is to write a boolean expression for our output (F), that is, $F = \underline{\hspace{1cm}}$.

79. $F = A\bar{B} + \bar{A}B + \bar{A}\bar{B}$

80. The next step is to simplify the expression using a Karnaugh map. Constructing our map, we see that the function $A\bar{B}$ will produce an output from block , function $\bar{A}B$ will produce an output from block and function $\bar{A}\bar{B}$ will produce an output from block .

$$F = A\bar{B} + \bar{A}B + \bar{A}\bar{B}$$

		B	
A		0	1
	0	1	2
	1	3	4

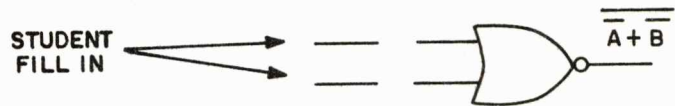
80. 3
 2
 1

81. Now if we examine the Karnaugh map we find by looping adjacent groups of 1's that there is an output when \bar{A} is equal to 1 and when \bar{B} is equal to 1. Therefore if \bar{A} or \bar{B} will give us an output of 1, we can reduce the expression $A\bar{B} + \bar{A}B + \bar{A}\bar{B}$ to .

		B	
A		0	1
	0	1	1
	1	1	0

81. $\bar{A} + \bar{B}$

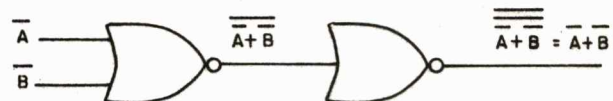
82. If we are going to use NOR gates to produce the function $\bar{A} + \bar{B}$ we must convert the function to a NOR function. This can be done by complementing both sides of the expression ($F = \bar{A} + \bar{B}$ complemented is $\bar{F} = \overline{\bar{A} + \bar{B}}$). We now have an expression which we can generate with a NOR gate.



82.

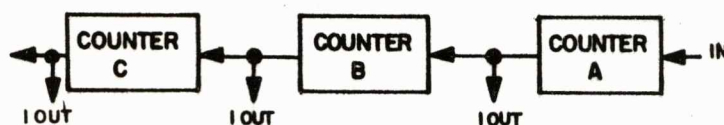


83. The output of our NOR gate is the complement of the function which we require therefore if we apply this function to another NOR gate the output of the second NOR gate will be the complement of the complement, or what we require.



(Proceed to next frame)

84. Having finished that problem, let us try one using three variables. If we have a binary counter capable of representing 8 counts and want an output on counts of 2, 4, and 6, what circuitry will we require? The first step will be to make a function table and from the table derive a boolean expression. From the function table we can write the expression _____ + _____ + _____.



FUNCTION TABLE				
COUNT	COUNTER			FUNCTION
	C	B	A	F
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0
8	0	0	0	0

84. $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$

85. Now let us see if we can simplify the expression with a Karnaugh Map. Putting 1's in the blocks that will produce an output for the expression we find that we can reduce $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$ to

		C	
		0	1
AB	00	0	1
	01	1	1
11	11	0	0
	10	0	0

85. $\bar{A}B + \bar{A}C$
or
 $\bar{A}(B + C)$

86. To generate the output $\bar{A}(B + C)$ using NOR logic we must express the output as a NOR function. That is, the entire expression must be under one bar, as shown below.

$$F = \bar{A}(B + C)$$

$$\bar{F} = \overline{\bar{A}(B + C)} \quad \text{complementing}$$

$$\bar{F} = \bar{\bar{A}} + \overline{(B + C)} \quad \text{applying DeMorgan's theorem}$$

$$(\overline{AB} = \bar{A} + \bar{B})$$

$$\bar{F} = A + \overline{(B + C)} \quad \text{complementing to get function in NOR form.}$$

We have now converted the function $\bar{A}(B + C)$ to a NOR function, $A + \overline{(B + C)}$. The function $\overline{B + C}$ is generated by a NOR gate with inputs of B and C as shown. The output function of $A + \overline{(B + C)}$ is generated by applying inputs of $\overline{B + C}$ and A to a second NOR gate as shown.



86. $(\bar{A})(B + C)$

87. Very good, let's try one using four variables. We now have a four-stage binary counter capable of representing 16 counts and want outputs on counts of 2, 3, 6, 7, 8, 9, 11, 12, 13 and 15. The first step is to construct a function table and write our boolean expression for the required output function.

FUNCTION TABLE					
COUNT	COUNTER				FUNCTION
	D	C	B	A	F
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1
16	0	0	0	0	0

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} \\ + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} \\ + \underline{\hspace{1cm}} + \underline{\hspace{1cm}}.$$

87. $F = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} \\ + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D \\ + \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} \\ + \bar{A}B\bar{C}D + A\bar{B}C\bar{D} \\ + \bar{A}BCD + A\bar{B}CD$

88. Constructing a Karnaugh map for the function we found in the preceding frame, we can loop all of the 1's into three loops of four as shown. From our Karnaugh map we can write our simplified expression. $F = \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}}$

AB \ CD	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	1	1	1
10	0	1	1	0

88. $F = B\bar{D} + \bar{B}D + AD$

89. Now that we have reduced our function to its minimum number of terms, let's see what configuration of NOR gates will generate this function. First we must express our functions in terms of NOR.

$$F = B\bar{D} + \bar{B}D + AD$$

Step 1: $F = (\overline{\bar{B} + D}) + (\overline{B + \bar{D}}) + (\overline{\bar{A} + \bar{D}})$

Applying De Morgan's theorem ($AB = \overline{\bar{A} + \bar{B}}$).

Step 2: $\bar{F} = \overline{(\bar{B} + D) + (B + \bar{D}) + (\bar{A} + \bar{D})}$

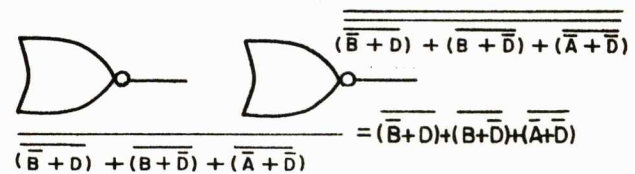
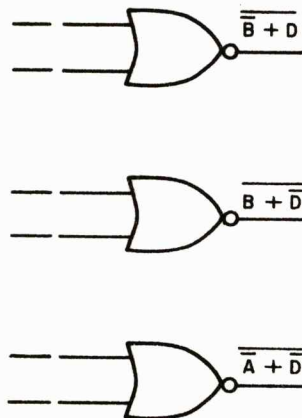
Complementing to get function in form of one NOR expression.

Step 3: $F = \overline{(\bar{B} + D) + (B + \bar{D}) + (\bar{A} + \bar{D})}$

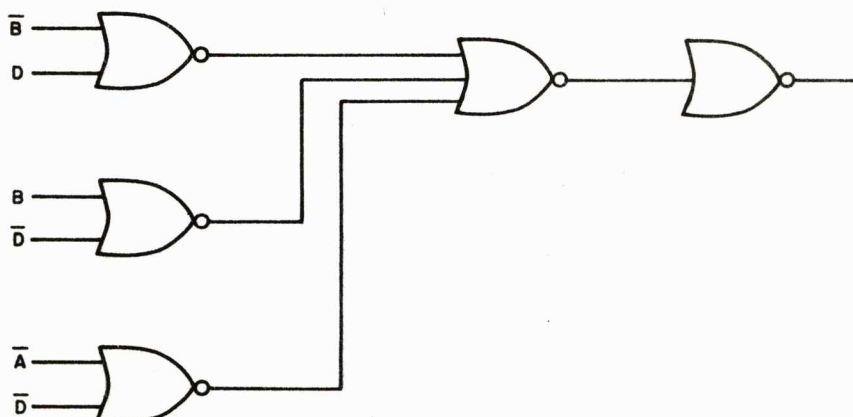
Complementing to invert \bar{F} to F .

(Proceed to the next frame)

90. With inputs of A , \bar{A} , B , \bar{B} , D and \bar{D} available, we can generate the function shown in Step 3 above, using five NOR gates. You connect the five NOR gates to generate the function.



90.



90a. Let's review the method used in developing a logic circuit. First we established the outputs required from our binary counter and wrote a boolean expression for this output. We then transposed this equation to a Karnaugh map, looped the adjacent 1's, and wrote the new equation for the least number of variables. Now, before we can use NOR circuits to generate this expression we must convert it to _____ logic form.

90a. NOR

90b. In converting our expression to NOR logic form we could have taken two successive complements of the expression. Why two? Remember that in complementing an expression you must complement both sides of the equation, and the complement of $F = \underline{\hspace{1cm}}$.

90b. \bar{F}

90c. But after complementing twice, our expression is still not in usable NOR logic form since a NOR gate cannot produce a product directly but only by application of DeMorgan's theorems. After the first complement we must apply DeMorgan's theorems to get our expression in the form of a Notted Sum of Notted Sums ($\bar{F} = \overline{\text{Sum}} + \overline{\text{Sum}} + \overline{\text{Sum}}$). Using a succeeding NOR gate the final complement gives us the usable NOR logic expression $F = \underline{\hspace{1cm}}$.

90c. $F = \overline{(\overline{\text{Sum}} + \overline{\text{Sum}} + \overline{\text{Sum}})}$

91. The expressions we have written so far are called Sum of Products expressions, because we are adding products ($AB + CD$ is product + product). This is not the only way to write an expression. If we were to write it $(A + B)(C + D)$, (sum · sum) we would be writing an expression of the Product of _____.

91. Sums

92. So far we discussed looping 1's but we could have just as easily looped 0's. However, if we loop 0's our Sum of Products expression will be written for the function NOT (\bar{F}) due to being written for an output of 0 instead of 1. The Sum of Products output for loops of 0 will be:

CD \ AB	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	1	1	1
10	0	1	1	0

$$\bar{F} = \bar{B}\bar{D} + \bar{A}BD$$

Complementing to invert \bar{F} to F ;

$$F = \overline{\bar{B}\bar{D} + \bar{A}BD}$$

Applying De Morgan's theorem $\overline{A+B} = \bar{A} \cdot \bar{B}$;

$$F = \overline{\bar{B}\bar{D}} \cdot \overline{\bar{A}BD}$$

Again applying De Morgan's theorem $\overline{\bar{A}\bar{B}} = A + B$;

$$F = (B + D)(A + \bar{B} + \bar{D})$$

On examining our output function we see that it is written as a _____ of _____.

92. Product of Sums

93. Therefore, if we were to write the output function for loops of 0's from a Karnaugh map we would write it as a Product of Sums. In writing a Product of Sums expression, we want our expression to have a sum of zero for the variables in the loop. This means then, that all of our variables must be zero. In order for all of our variables to be zero we will complement all variables with a value 1 and leave alone all variables with a value 0. Let's consider the loop of two on our Karnaugh map just discussed. We want a sum of 0 for common variables A, B, D and since A is 0 we will leave it alone but since B and D are both 1's and $0 + 1 + 1 \neq 0$ ($A + B + D \neq 0$) we must complement B and D to generate a sum of 0.

(Proceed to the next frame)

94. In developing a circuit which will generate the Product of Sums function, we use the same steps as developing a Sum of Products circuit. The first step is to express our function as a NOR function.

$$F = (B + D) (A + \bar{B} + \bar{D})$$

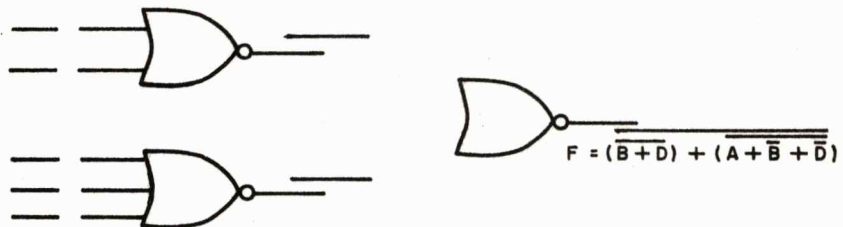
$$\bar{F} = \overline{(B + D) (A + \bar{B} + \bar{D})} \quad \text{complementing}$$

$$\bar{F} = \underline{\hspace{2cm}} \quad \text{applying De Morgan's theorem } (\overline{AB} = \bar{A} + \bar{B})$$

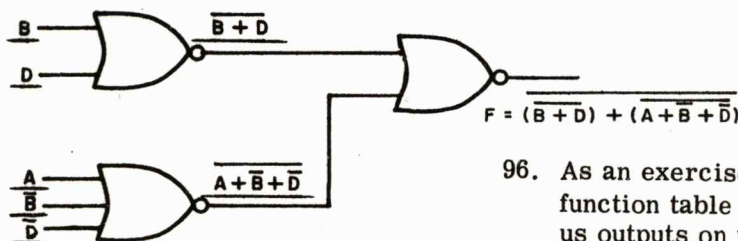
$$F = \underline{\hspace{2cm}} \quad \text{complementing}$$

94. $\bar{F} = \overline{(B + D)} + \overline{(A + \bar{B} + \bar{D})}$
 $F = \overline{\overline{(B + D)} + \overline{(A + \bar{B} + \bar{D})}}$

95. The function $F = \overline{\overline{(B + D)} + \overline{(A + \bar{B} + \bar{D})}}$ (Notted Sum of Notted Sums) can be generated using three NOR gates with inputs A, B, \bar{B} , D and \bar{D} available. Therefore, we find that to generate the Product of Sums function requires less gates than to generate the Sum of Products. Normally, although the functions are the same, one will require less gates than the other. Using the three NOR gates shown, apply inputs and connect the gates to generate the Product of Sums function.



95.



96. As an exercise, you develop a circuit from the function table for the four stage counter to give us outputs on the counts of 1, 2, 5, 6, 8, 10, 12, and 14. Develop a circuit for the Sum of Products and for the Product of Sums. Beginning with the Sum of Products the first step is to write a boolean expression for the output function.

$$F = \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}}$$

96. $F = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D}$
 $+ \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D$
 $+ \overline{A}BCD + A\overline{B}\overline{C}\overline{D}$

97. Now we construct our Karnaugh map and make loops.

CD \ AB	00	01	11	10
00				
01				
11				
10				

97.

CD \ AB	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	0	0	0	0
10	1	0	0	1

98. From our Karnaugh map we can write the simplified expression.

$F = \underline{\hspace{1cm}} + \underline{\hspace{1cm}} + \underline{\hspace{1cm}}$

98. $F = \overline{A}D + \overline{A}B + A\overline{B}\overline{D}$

99. Expressing one function in terms of NOR.

$F = \overline{A}D + \overline{A}B + A\overline{B}\overline{D}$

$F = \underline{\hspace{2cm}}$ applying De Morgan's theorem ($\overline{AB} = \overline{A} + \overline{B}$)

$\overline{F} = \underline{\hspace{2cm}}$ complementing to get NOR function

$F = \underline{\hspace{2cm}}$ complementing to get required function

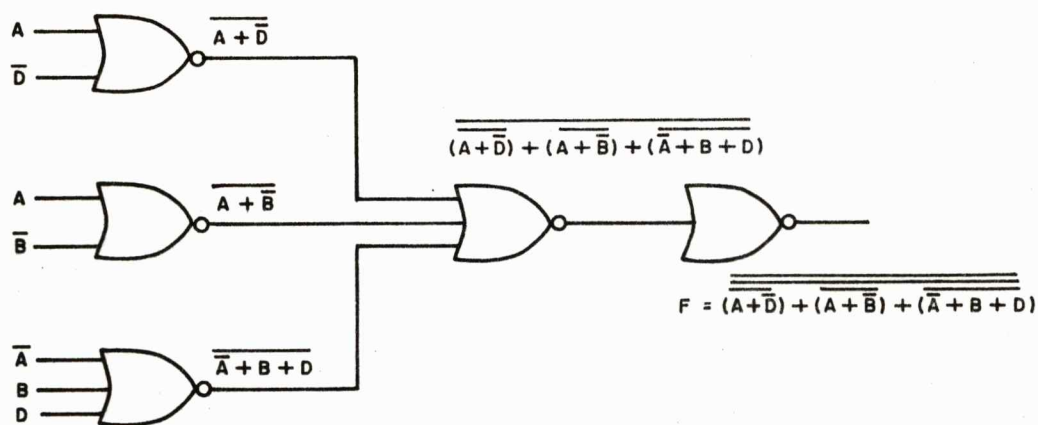
99. $F = \overline{(A + \overline{D}) + (\overline{A} + \overline{B})}$
 $+ \overline{(\overline{A} + B + D)}$

$\overline{F} = \overline{(A + \overline{D}) + (\overline{A} + \overline{B})}$
 $+ \overline{(\overline{A} + B + D)}$

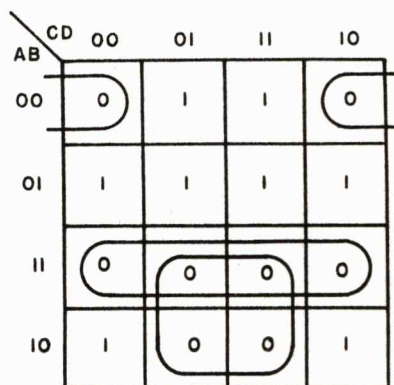
$\overline{\overline{F}} = \overline{(A + \overline{D}) + (\overline{A} + \overline{B})}$
 $+ \overline{(\overline{A} + B + D)}$

100. Draw the circuit showing inputs and outputs of each gate. Inputs A, \overline{A} , B, \overline{B} , D and \overline{D} are available. Draw circuit on left hand page.

100.



101. Now let's solve for the Product of Sums. From the Karnaugh map we can derive the expression $F =$ _____.



101. $F = (A + B + D) (\bar{A} + \bar{B}) (\bar{A} + \bar{D})$

102. Expressing the function in terms of NOR,

$F = (A + B + D) (\bar{A} + \bar{B}) (\bar{A} + \bar{D})$

$\bar{F} =$ _____ Complementing

$\bar{F} =$ _____ Applying
De Morgan's
theorem

$F =$ _____ Complementing

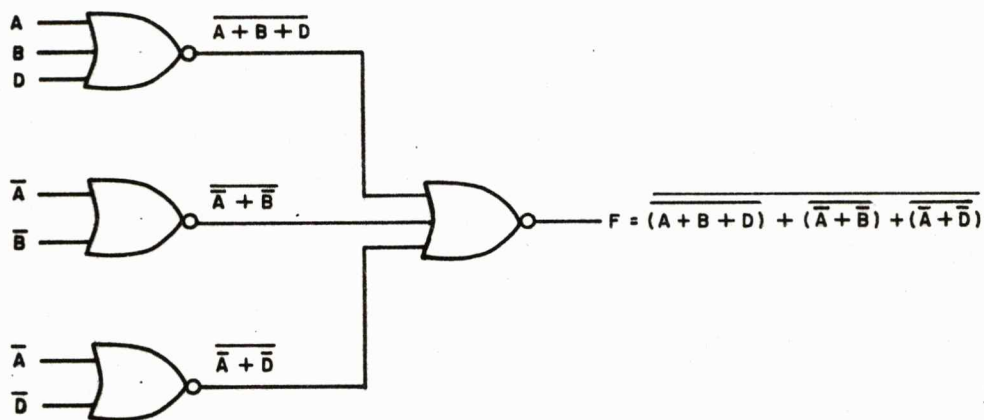
102. $\bar{F} = \overline{(A + B + D)} (\bar{A} + \bar{B}) (\bar{A} + \bar{D})$

$\bar{F} = \overline{(A + B + D)} + \overline{(\bar{A} + \bar{B})} + \overline{(\bar{A} + \bar{D})}$

$F = \overline{\overline{(A + B + D)} + \overline{(\bar{A} + \bar{B})} + \overline{(\bar{A} + \bar{D})}}$

103. Draw the NOR logic circuit showing gate inputs and outputs on the blank left hand page.

103.



104. Let's develop a circuit which will generate the Sum of Products for outputs on the counts of 1, 4, 6, 9, 11, and 14 from a four stage counter. You write the function:

F = _____

104. $F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D}$

105. Draw the Karnaugh map and loop all of the 1's, then reduce the function to its simplest form from the map.

105.

AB \ CD	00	01	11	10
00	0	0	0	1
01	0	0	1	1
11	0	1	0	0
10	1	1	0	0

$$F = \overline{A}C\overline{D} + \overline{A}BC + A\overline{C}D + A\overline{B}\overline{C}$$

106. Express $F = \overline{A}C\overline{D} + \overline{A}BC + A\overline{C}D + A\overline{B}\overline{C}$ as a NOR function.

$$F = \overline{A}C\overline{D} + \overline{A}BC + A\overline{C}D + A\overline{B}\overline{C}$$

106.

$$F = (\overline{A + \overline{C} + D}) + (\overline{A + \overline{B} + \overline{C}}) + (\overline{\overline{A} + C + \overline{D}}) + (\overline{\overline{A} + B + C})$$

Applying De Morgan's theorem ($\overline{AB} = \overline{A} + \overline{B}$)

$$\overline{F} = (\overline{A + \overline{C} + D}) + (\overline{A + \overline{B} + \overline{C}}) + (\overline{\overline{A} + C + \overline{D}}) + (\overline{\overline{A} + B + C})$$

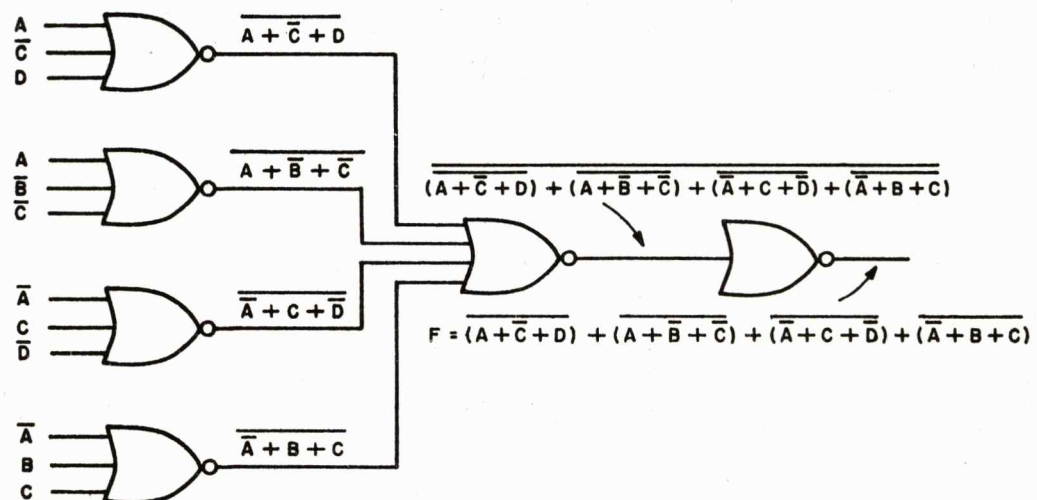
Complementing

$$F = (\overline{A + \overline{C} + D}) + (\overline{A + \overline{B} + \overline{C}}) + (\overline{\overline{A} + C + \overline{D}}) + (\overline{\overline{A} + B + C})$$

Complementing

107. Draw the circuit.

$$F = \overline{(A + \bar{C} + D)} + \overline{(A + \bar{B} + \bar{C})} + \overline{(\bar{A} + C + \bar{D})} + \overline{(\bar{A} + B + C)}$$



108. For your own practice develop the Product of Sums (loop the zeros) circuit to generate an output on the counts of 1, 4, 6, 9, 11 and 14. Go through all of the steps necessary to develop the circuit and compare your results with the response on the following page. (Use remainder of this page and left blank page for work sheet.)

108. Function:

$$F = (A + B + C + D) (\bar{A} + \bar{B} + C + D) (A + \bar{B} + C + D) (\bar{A} + B + \bar{C} + D) \\ (\bar{A} + \bar{B} + \bar{C} + D) (A + B + C + \bar{D}) (A + \bar{B} + C + \bar{D}) (A + B + \bar{C} + \bar{D}) \\ (\bar{A} + B + \bar{C} + \bar{D}) (\bar{A} + \bar{B} + \bar{C} + \bar{D})$$

Karnaugh map and simplified expression:

CD	00	01	11	10
AB	00	01	11	10
00	0	0	0	1
01	0	0	1	1
11	0	1	0	0
10	1	1	0	0

$$F = (A + C) (\bar{A} + \bar{C}) (\bar{B} + C + D) (A + B + \bar{D})$$

Conversion of function to a NOR function:

$$F = (A + C) (\bar{A} + \bar{C}) (\bar{B} + C + D) (A + B + \bar{D})$$

$$\bar{F} = \overline{(A + C) (\bar{A} + \bar{C}) (\bar{B} + C + D) (A + B + \bar{D})}$$

Complementing

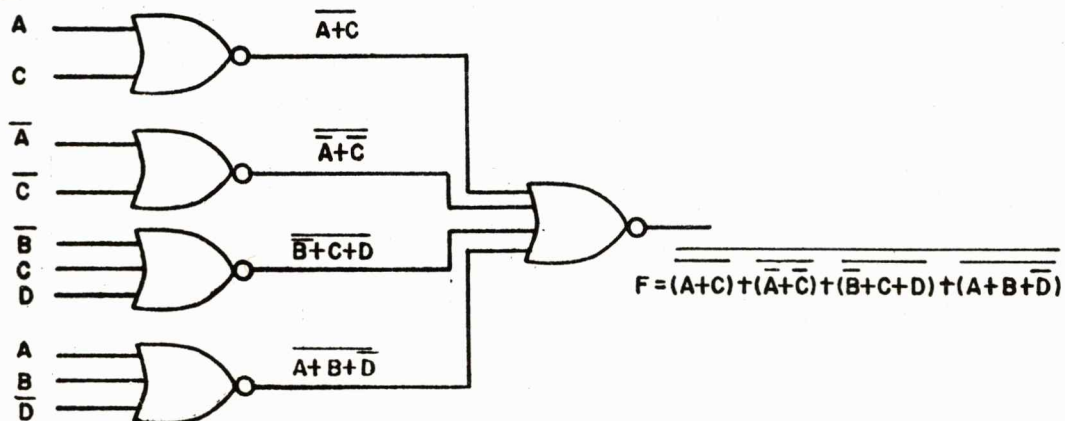
$$\bar{F} = \overline{(A + C) + (\bar{A} + \bar{C}) + (\bar{B} + C + D) + (A + B + \bar{D})}$$

Applying DeMorgan's theorem
($\overline{AB} = \bar{A} + \bar{B}$)

$$\bar{F} = \overline{(A + C) + (\bar{A} + \bar{C}) + (\bar{B} + C + D) + (A + B + \bar{D})}$$

Complementing to get function into NOR function

Circuit:



109. Develop the Product of Sums circuit which will produce outputs on the counts of 1, 4, 5, 6, 8, 9, and 14 from a four stage counter. You write the function: $F =$ _____
- _____

$$\begin{aligned} 109. \quad F = & (A + B + C + D) (\bar{A} + \bar{B} + C + D) (A + \bar{B} + C + D) (\bar{A} + \bar{B} + \bar{C} + D) \\ & (A + \bar{B} + C + \bar{D}) (\bar{A} + \bar{B} + C + \bar{D}) (A + B + \bar{C} + \bar{D}) (\bar{A} + B + \bar{C} + \bar{D}) \\ & (\bar{A} + \bar{B} + \bar{C} + \bar{D}) \end{aligned}$$

110. Draw the Karnaugh map and loop all of the 0's. Then reduce the function to its simplest form from the map.

110.

111. Express as a NOR function:

$$F = (\bar{A} + \bar{B}) (\bar{B} + C) (A + C + D) (B + \bar{C} + \bar{D})$$

AB \ CD	00	01	11	10
00	0	1	0	1
01	0	0	1	1
11	0	0	0	0
10	1	1	0	1

$$F = (\bar{A} + \bar{B}) (\bar{B} + C) (A + C + D) (B + \bar{C} + \bar{D})$$

111.

$$F = (\bar{A} + \bar{B}) (\bar{B} + C) (A + C + D) (B + \bar{C} + \bar{D})$$

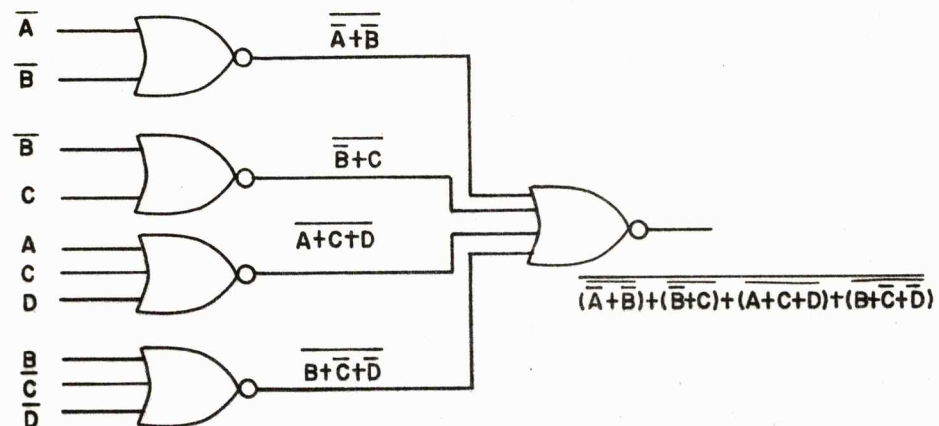
$$F = \overline{(\bar{A} + \bar{B}) (\bar{B} + C) (A + C + D) (B + \bar{C} + \bar{D})} \quad \text{Complementing}$$

$$F = \overline{(\bar{A} + \bar{B}) + (\bar{B} + C) + (A + C + D) + (B + \bar{C} + \bar{D})} \quad \text{Applying De Morgan's theorem } (\overline{AB} = \bar{A} + \bar{B})$$

$$F = \overline{(\bar{A} + \bar{B}) + (\bar{B} + C) + (A + C + D) + (B + \bar{C} + \bar{D})} \quad \text{Complementing}$$

112. Draw the NOR logic circuit for the answer to Frame 111.

112.



113. Develop a NOR logic Sum of Products circuit for outputs of 1, 4, 5, 6, 8, 9 and 14 from a four stage counter. Go through all of the steps necessary to develop the circuit and compare your results with the response. (Use remainder of this page and left blank page for work sheet.)

113. Function:

$$F = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D} + \overline{A}BC\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}BCD$$

Karnaugh map and simplified expression:

CD \ AB	00	01	11	10
00	0	1	0	1
01	0	0	1	1
11	0	0	0	0
10	1	1	0	1

$$F = \overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C} + \overline{A}BC + \overline{B}C\overline{D}$$

Conversion of function to a NOR function:

$$F = \overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C} + \overline{A}BC + \overline{B}C\overline{D}$$

$$F = \overline{(B + C + \overline{D})} + \overline{(\overline{A} + B + C)} + \overline{(A + \overline{B} + \overline{C})} + \overline{(B + \overline{C} + D)}$$

Applying
DeMorgan's
theorem

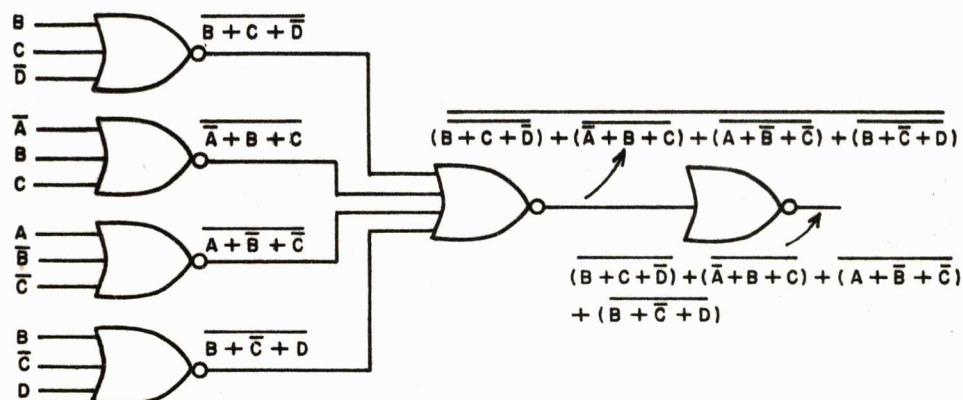
$$\overline{F} = \overline{(B + C + \overline{D})} + \overline{(\overline{A} + B + C)} + \overline{(A + \overline{B} + \overline{C})} + \overline{(B + \overline{C} + D)}$$

Complementing

$$F = \overline{\overline{(B + C + \overline{D})} + \overline{(\overline{A} + B + C)} + \overline{(A + \overline{B} + \overline{C})} + \overline{(B + \overline{C} + D)}}$$

Complementing

Circuit:



114. Now that we have had some practice developing NOR logic circuits let's consider some of the transistor factors that will affect our circuits before proceeding to more sophisticated logic circuits. As you recall from transistor switching circuits, there is a time interval required for a switch to go from one state to the other. This delay, an inherent delay, is found in all logic circuits and must be taken in consideration when developing logic circuits. When a logic pulse is propagated over a serial path, as in a counter, each logic element will add some delay which when summed will give us the _____ delay for the serial path.

114. propagation

115. Even though there is a slight difference in the delay of each logic circuit, a delay figure which can be used for developing a circuit can be obtained by averaging the delays of a large number of logic elements and this figure is called _____ delay.

115. average

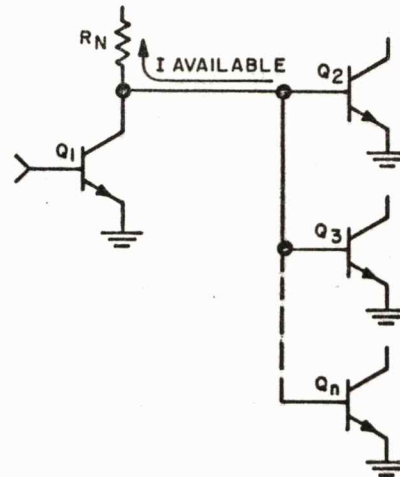
116. Knowing the average delay of each element the total delay over a serial path may be calculated. For example, if the average delay equals 50 nanoseconds per element and there are 5 elements in series the propagation delay will be _____ .

116. 250 nanoseconds

117. The maximum permissible delay in a serial path cannot exceed the clocking interval. Another way of stating this is, one logical operation in a series of logical operations cannot start until the preceding operation is completed. Therefore, it is important that the propagation delay not exceed the _____ delay.

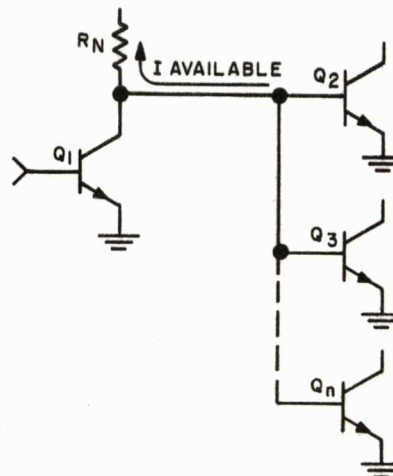
117. maximum permissible

118. The output of one logic circuit is often fed to the inputs of several other logic circuits as shown below. Because the digital information fans-out from the output of Q_1 to the inputs of $Q_2, 3 \dots n$, we refer to this arrangement as fan-_____.



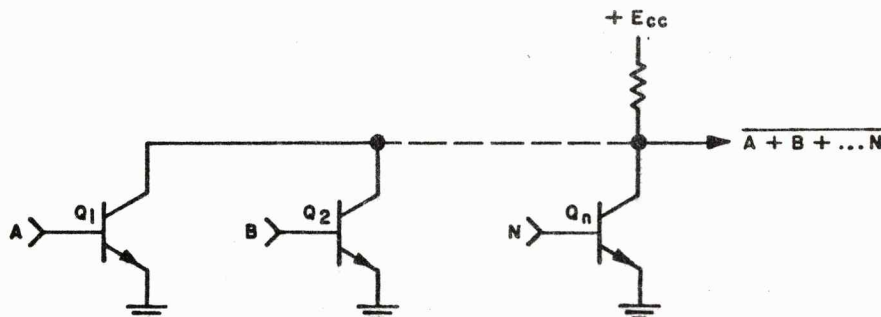
118. out

119. Since the base current at $Q_2, 3, \dots n$ must flow through R_N , the node resistor, we can see that there is a limit to the number of bases that can be driven by the current available from R_N . This limit is usually considered to be 5. That is, we have a maximum fan-out of _____.



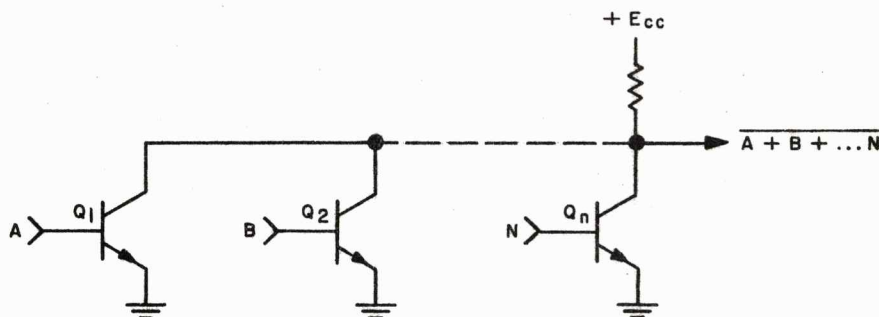
119. 5

120. In the circuit below several transistors, each with its own input, feed a single collector load resistor. This is the opposite of fan-out, described above, and is called fan-_____.



120. in

121. If any transistor of a fan-in is ON, and is therefore in saturation, the potential of the collector buss is in the order of .2 volts. Consequently, even those transistors that are not turned ON by 1's at their bases have a very low value of collector reverse bias, if any, and therefore exhibit a very _____ input impedance.

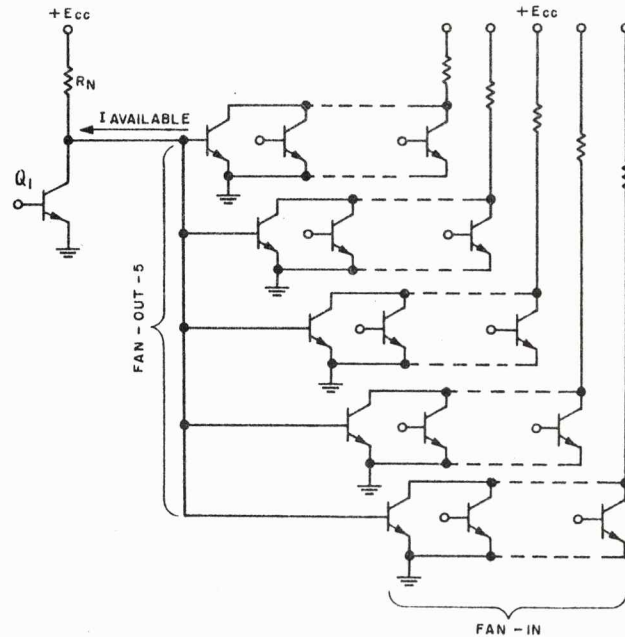


121. low

122. Furthermore, the greater the number of collectors sharing a single collector resistor, the greater is the input loading at each base in the fan-in, and the _____ the resulting input impedance.

122. lower

123. If one base in a fan-out exhibits a much lower impedance than the others, this base will pass a majority of the available current through R_N . The result is a shortage of available base current to drive the other fan-out transistors into saturation. Because one transistor is "hogging" the available current, this phenomenon is called "current-_____."



123. hogging

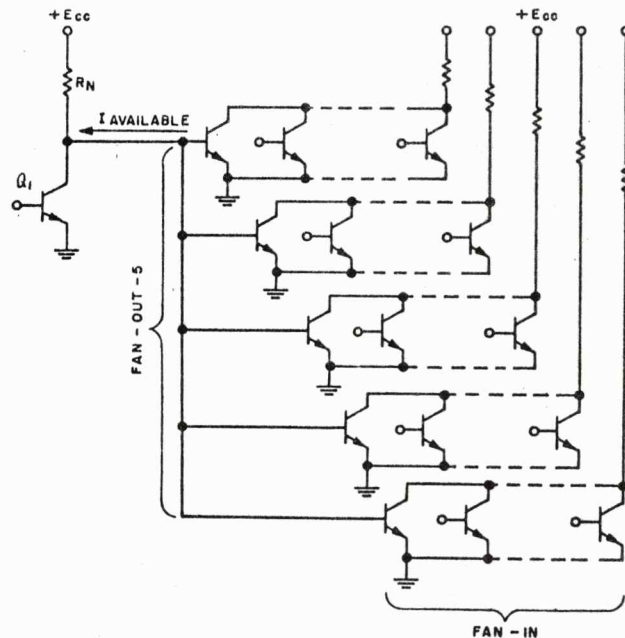
124. The current-hogging problem can be minimized by use of closely uniform base input characteristics, and by a moderate (increase/decrease) in base input resistance.

124. increase

125. In our previous discussions we have assumed that a binary 1 is represented by E_{cc} , generally in the order of +3 to +12 volts in the circuits we have shown, and that a 0 is represented by ground or _____ volts.

125. 0

126. But let's take a closer look at the actual situation. With an E_{cc} of +3 volts, Q_1 OFF, and considering the fan-out base current flowing through R_N , we can see that the fan-out base potential is most apt to be _____ (0/.2/1/3) volt(s).



126. 1

127. And with Q_1 ON, considering typical values of $V_{ce} (SAT)$, the 0 level on the fan-out bases is most apt to be _____ (0/.2/1/3) volt(s).

127. .2

128. In some transistors $V_{ce} (SAT)$ may be as high as .4 volts. So we see that the change in potential between a 0 and a 1 may be rather _____ (large/small).

128. small

129. While the difference in potential between a 0 and a 1 is small, the difference in potential at a base between turn-on and turn-off is even _____.

129. smaller

130. This very small difference between turn-on and turn-off potential makes these circuits susceptible to switching by noise pulses and transients.

(Proceed to the next frame)

131. Now that we have discussed NOR logic and seen how it is used in some circuitry let us see how it is used in an adder. Addition may be performed in either of two ways, serially or in parallel. In a serial adder we add one order of numbers at a time starting with the least significant order and progressing to the most significant order in a series of additions. In a parallel adder all orders from the least significant to the most significant digit are added at the same time.

(Proceed to the next frame)

132. A binary adder is capable of adding two numbers, an augend and an addend. The logic required to perform the addition of two numbers of the same order can be determined by constructing a truth table. From the truth table we can write the boolean expressions for the sum and the carry when the sum and carry are both 1's.

ADDER TRUTH TABLE					
AUGEND	X	0	1	0	1
ADDEND	Y	0	0	1	1
SUM	S	0	1	1	0
CARRY	C	0	0	0	1

SUM = $X\bar{Y}$ + _____

CARRY = _____

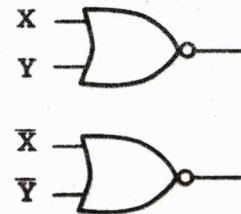
132. $\bar{X}Y$
XY

133. If we are going to use NOR logic to perform the addition process, let us review the means of generating the AND and OR functions with NOR gates. The AND function is produced by _____ the inputs to a NOR gate and the OR function is produced by _____ the output of a NOR gate.

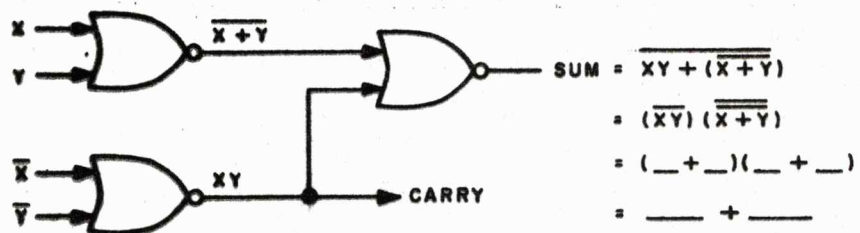
133. complementing
complementing

134. $(\overline{X+Y})$
 XY

134. Using NOR logic if we apply inputs of X and Y and inputs of \overline{X} and \overline{Y} to the two gates shown below the outputs are (+) and respectively.



135. As you can see the carry is generated by a NOR gate with complemented inputs of \overline{X} and \overline{Y} . However, we still haven't generated the sum. The sum can be generated by applying the outputs of the two gates just discussed to a third NOR gate.



135. $(\overline{X+Y})(\overline{X+Y})$
 $XY.XY$

136. The logic circuit we have just discussed will perform only one-half of the addition process in that it has no means for handling the carry from a preceding order of addition. Because it can handle only half the addition process, it is called a half-_____.

136. adder

137. The truth table we discussed earlier was for one order of numbers or for a half-adder. The table below is for a full-adder which will add the carry from the preceding order, carry-in (c_i), and generate a carry for the succeeding order, carry out (c_o). Complete the table.

FULL-ADDER TRUTH TABLE									
AUGEND	X	0	1	0	1	0	1	0	1
ADDEND	Y	0	0	1	1	0	0	1	1
CARRY-IN	C_i	0	0	0	0	1	1	1	1
SUM	S	0	1	1	—	—	—	—	—
CARRY-OUT	C_o	0	0	—	—	—	—	—	—

137. 0 1 0 0 1
0 1 0 1 1 1

138. From the table we can see that there are four combinations of inputs that will produce a sum of 1 and four combinations that will produce a carry of 1. Using the truth table we can write the boolean expressions for the sum and carry.

FULL-ADDER TRUTH TABLE									
AUGEND	X	0	1	0	1	0	1	0	1
ADDEND	Y	0	0	1	1	0	0	1	1
CARRY-IN	C ₁	0	0	0	0	1	1	1	1
SUM	S	0	1	1	0	1	0	0	1
CARRY-OUT	C ₀	0	0	0	1	0	1	1	1

$$\text{SUM} = \overline{X}Y\overline{C}_1 + X\overline{Y}\overline{C}_1 +$$

_____ + _____

$$\text{CARRY} = \text{_____} + \text{_____}$$

+ _____ + _____

138.

$$\text{SUM} = \overline{X}Y\overline{C}_1 + X\overline{Y}\overline{C}_1 + \overline{X}Y C_1 + X\overline{Y} C_1$$

$$\text{CARRY} = XY\overline{C}_1 + X\overline{Y} C_1 + \overline{X}Y C_1 + XY C_1$$

139. The sum function for adding two numbers and a carry from the previous order of addition can be generated using two half-adders. The first half-adder we have just discussed. The second half-adder will have as inputs the outputs of the first half-adder and a carry-in (C₁) from the previous order of addition.

(Proceed to next frame)

140. The function of adding no carry-in or a carry-in of 0 from the previous addition and the sum generated in the half-adder just discussed can be generated by a NOR gate with inputs of C_i , XY and $\overline{X+Y}$ as shown below.

$$\text{OUTPUT} = \overline{C_i + XY + (\overline{X+Y})}$$



$$\begin{aligned} &= \overline{(C_i) (XY) (\overline{X+Y})} \\ &= (\underline{\quad}) (\underline{\quad} + \underline{\quad}) (\underline{\quad} + \underline{\quad}) \\ &= (\underline{\quad}) (\underline{\quad} + \underline{\quad}) \\ &= \underline{\quad} + \underline{\quad} \end{aligned}$$

140. $(\overline{C_i}) (\overline{X+Y}) (X+Y)$
 $(\overline{C_i}) (\overline{XY+XY})$
 $\overline{C_i} \overline{XY} + \overline{C_i} \overline{XY}$

141. The function of adding a carry-in of 1 from the previous addition and the sum generated in the first half-adder just discussed can be generated by a NOR gate with inputs of $\overline{C_i}$ and $X\overline{Y} + \overline{X}Y$ as shown below.

$$\text{OUTPUT} = \overline{\overline{C_i} + X\overline{Y} + \overline{X}Y}$$



$$\begin{aligned} &= \overline{(\overline{C_i}) (X\overline{Y}) (\overline{X}Y)} \\ &= (\underline{\quad}) (\underline{\quad} + \underline{\quad}) (\underline{\quad} + \underline{\quad}) \\ &= \underline{\quad} + \underline{\quad} \end{aligned}$$

141. $(C_i) (\overline{X+Y}) (X+Y)$
 $C_i \overline{XY} + C_i \overline{XY}$

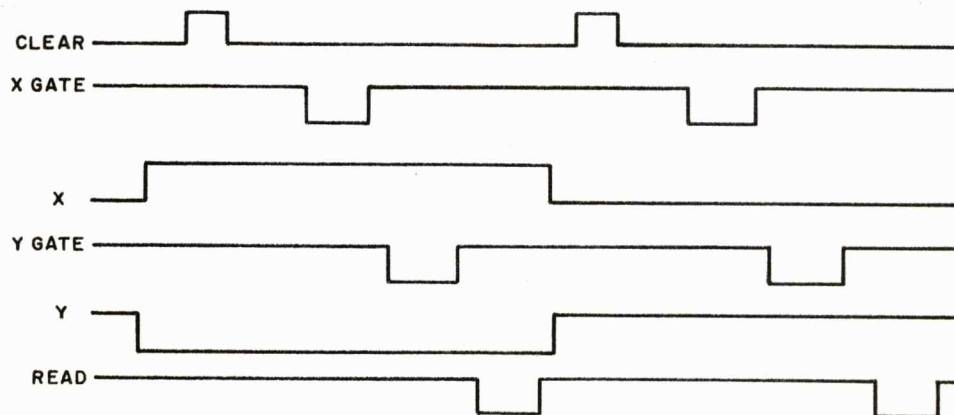
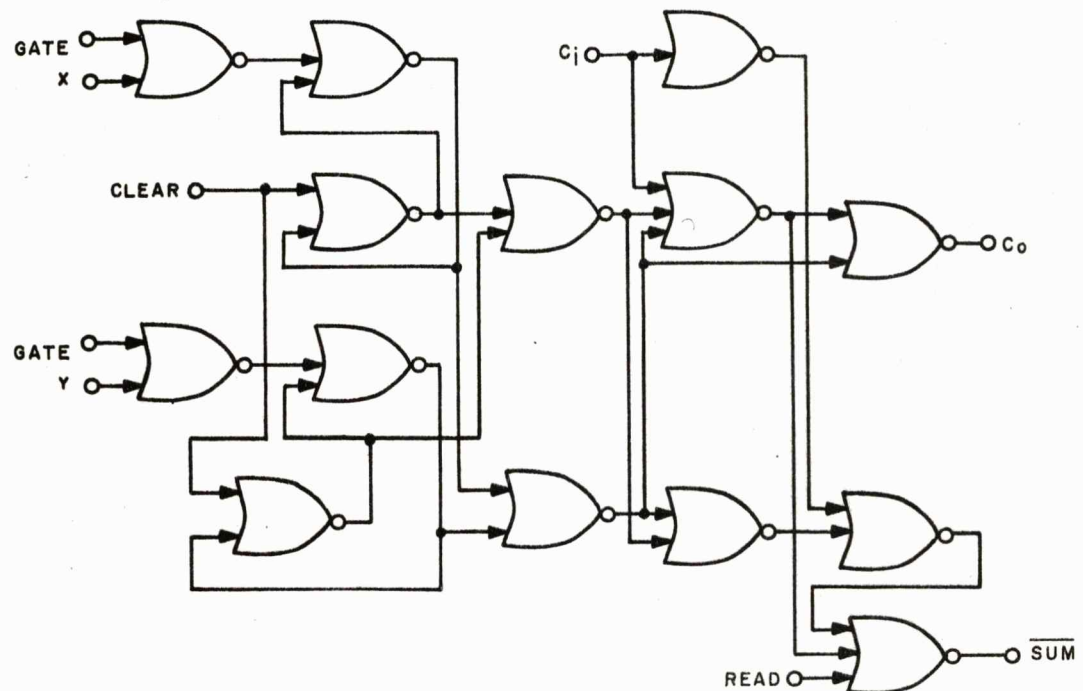
142. The two functions just discussed if combined in an OR gate will produce the full sum for the addition of two numbers and the carry from a previous addition. If the two functions, $C_i \overline{XY} + C_i \overline{XY}$ and $\overline{C_i} \overline{XY} + \overline{C_i} \overline{XY}$ are applied as inputs to a NOR gate the output will be $\overline{\text{SUM}}$ or $\underline{\quad} + \underline{\quad} + \underline{\quad} + \underline{\quad}$.

144. 0 0 0 1 0 1 1 1
1 0 0 1 0 1 1 0

145. Usually in an adder there will only be inputs of X and Y , while for the adder we just discussed we required inputs of X , Y , \bar{X} and \bar{Y} . As you recall, a device which will give us outputs of X and \bar{X} for an input of X is a _____.

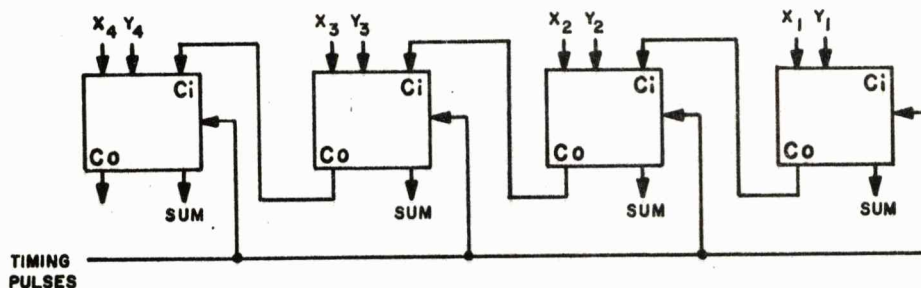
145. flip-flop or bistable multivibrator

146. Gated flip-flops are used in the adder shown below for timing. A timing sequence is shown also. We have discussed the gating functions of the X and Y inputs. The purpose of $CLEAR$ is to reset the flip-flops for the next addition. The $READ$ gate inhibits the output until $READ$ goes to a 0.



(Proceed to next frame)

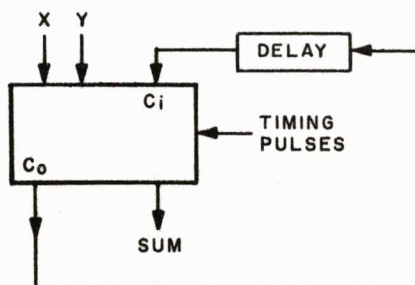
147. As was mentioned earlier, the two ways of adding numbers are serially or in parallel. The parallel adder shown below consists of four full-adders in parallel. The two numbers are applied as shown and the SUM will be generated when the READ input goes to 0. Notice also that the carry-out from one addition goes to the succeeding adder _____.



TRUTH TABLE				
Time	4	3	2	1
X	0	1	0	1
Y	0	0	1	1
C_i	1	1	1	0
C_o	0	1	1	1
Sum	1	0	0	0

147. Carry-in (C_i)

148. When adding two numbers serially, there is only one order of numbers added during a timing interval. Therefore, only one adder is required with a means for delaying the carry from one order of addition to the succeeding order. This delay can be produced by a delay line or a flip-flop. A serial full-adder is shown below with a truth table for adding 01011 and 00101. Complete the truth table.



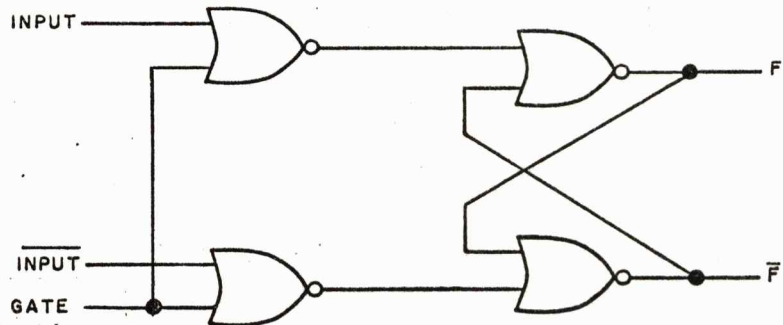
TRUTH TABLE					
Time	5	4	3	2	1
X	0	1	0	1	1
Y	0	0	1	0	1
C_i		1	1	1	0
C_o				1	1
Sum				0	0

148. 1
0 1 1
1 0 0

149. shift

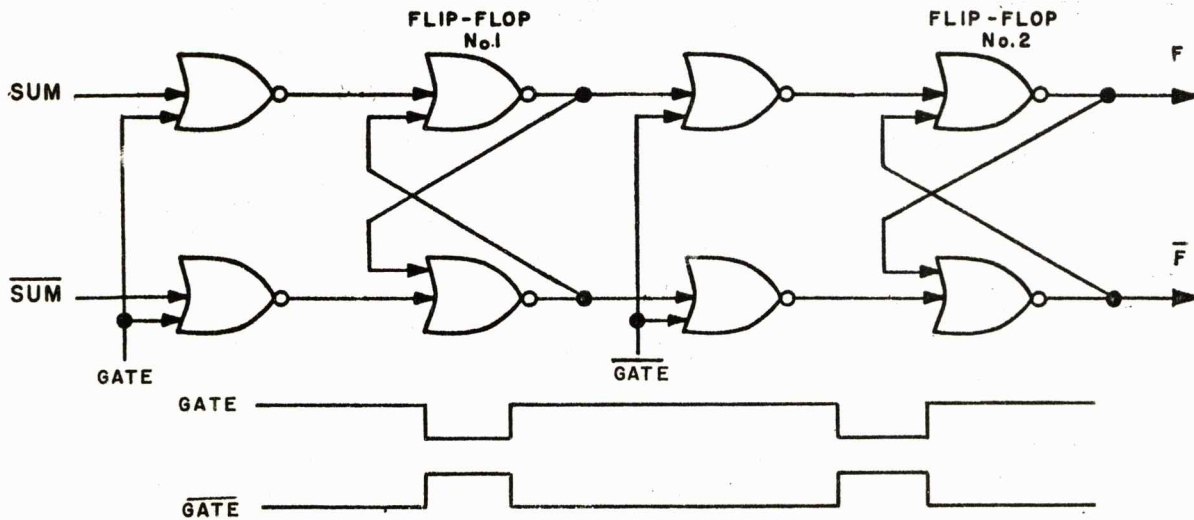
149. When the READ pulse occurs, the sum may be GATED into other circuitry for further computations or it may be shifted into a register to be used later in the timing cycle. Because the sum may be shifted in and out of a register, the register is called a _____ register.

150. A circuit we have discussed previously is the gated flip-flop shown. The flip-flop will accept no new information until the GATE input goes to _____ (0 or 1)



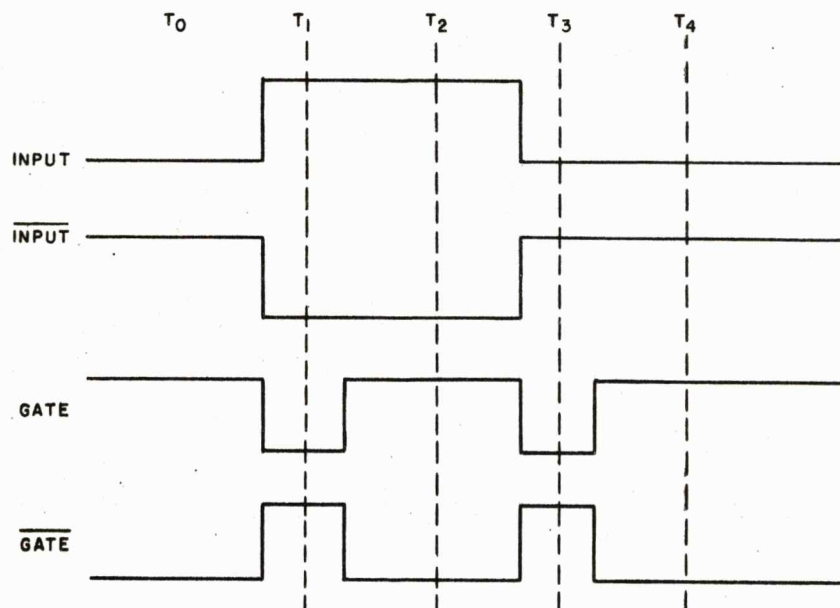
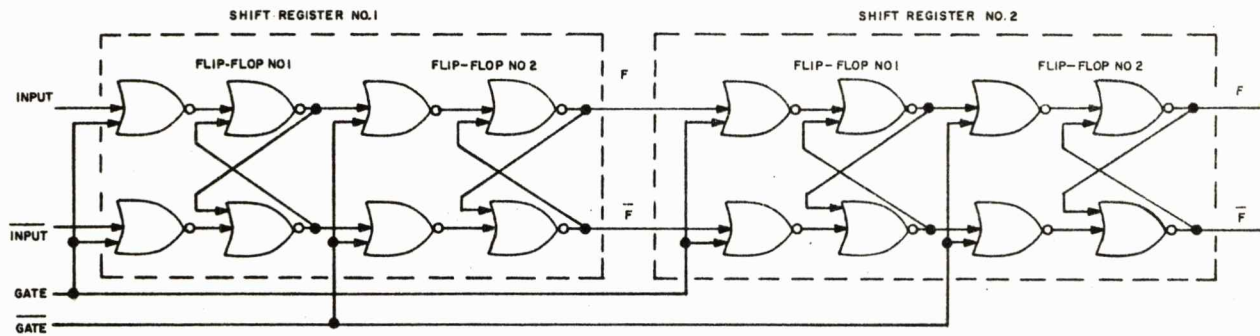
150. 0

151. A shift register must be capable of supplying the information stored to other registers when new information is being shifted into the register. Therefore, a register must consist of more circuitry than just a gated flip-flop. The shift register shown below uses two gated flip-flops with flip-flop #2 gated by the GATE function. When the GATE input is 0 new information will be shifted into flip-flop #1 and when the GATE input goes to 1 (GATE goes to 0) the new information will be shifted into _____.



151. Flip-flop #2

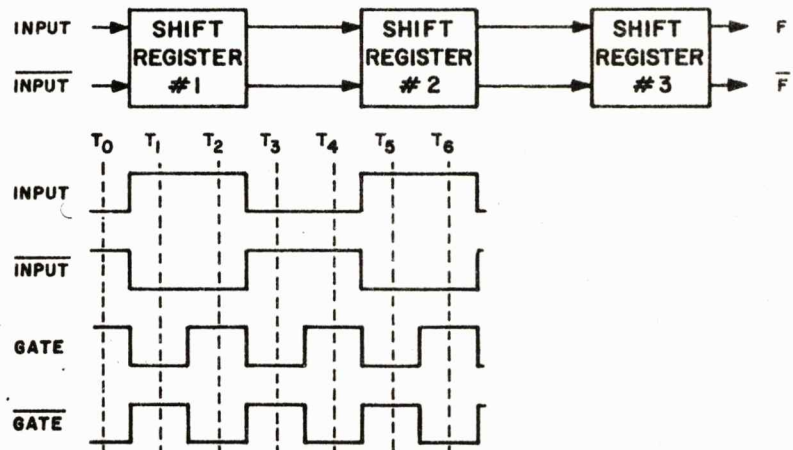
152. Let us examine two shift registers in series as the number 01 is shifted into the register. The outputs will be referenced to the F side of the register.



Time						
Register	Flip-Flop	T ₀	T ₁	T ₂	T ₃	T ₄
1	1	0	1	1	0	0
	2	0	0	1	1	0
2	1	0	0	0	1	1
	2	0	0	0	0	1

(Proceed to next frame)

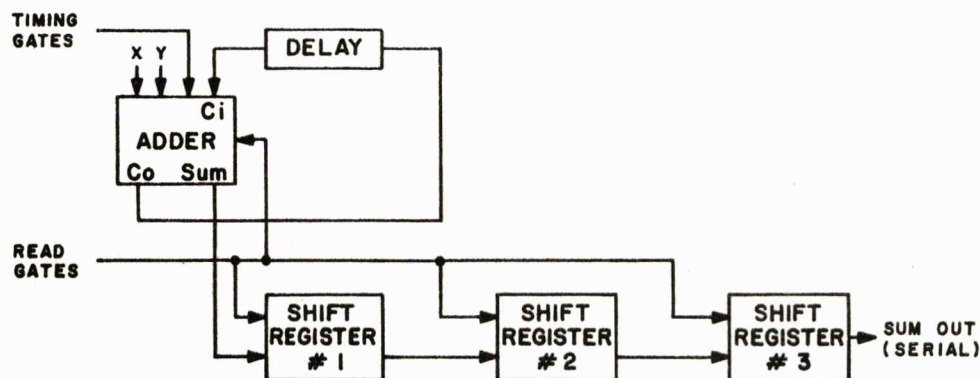
153. Let us now consider a serial shift register consisting of three registers instead of two as previously mentioned. The number to be shifted is 101. Complete the table.



Register	Flip-Flop	Time							
		T ₀	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	
1	1	0	1	1	0	0	1	1	
	2	0	0	1	1	0	0	—	
2	1	0	0	0	1	1	—	—	
	2	0	0	0	0	—	—	—	
3	1	0	0	0	—	—	—	—	
	2	0	0	—	—	—	—	—	

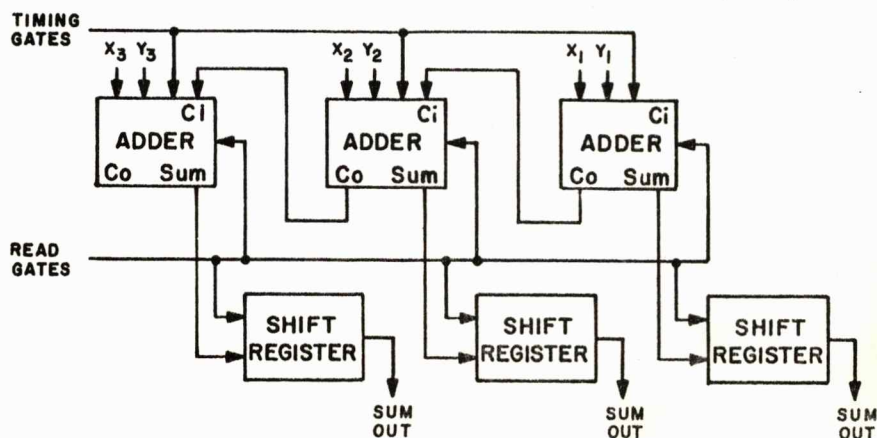
153. 1
 0 0
 1 1 0
 0 0 1 1
 0 0 0 0 1

154. To shift the output of a serial adder into a shift register we will use the serial shift register previously discussed. We will use the READ gates to gate the shift register because the READ gates are used to shift the sum information out of the adder. A serial adder with a shift register is shown below.



(Proceed to next frame)

155. Information may be shifted into a shift register either serially or in parallel. A parallel adder with shift register is shown below. As you recall the sum information is read out of the adder when the READ input goes to 0; therefore, we can gate the inputs to the registers with the READ gates. All of the sum information will be shifted into the registers when _____ READ pulse occurs.



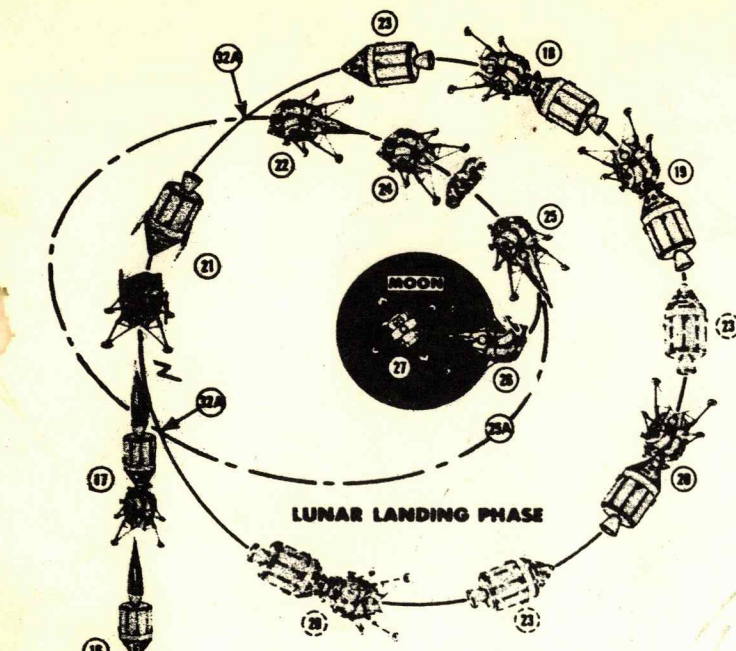
155. one

This Completes Logic.

FRAME COVER

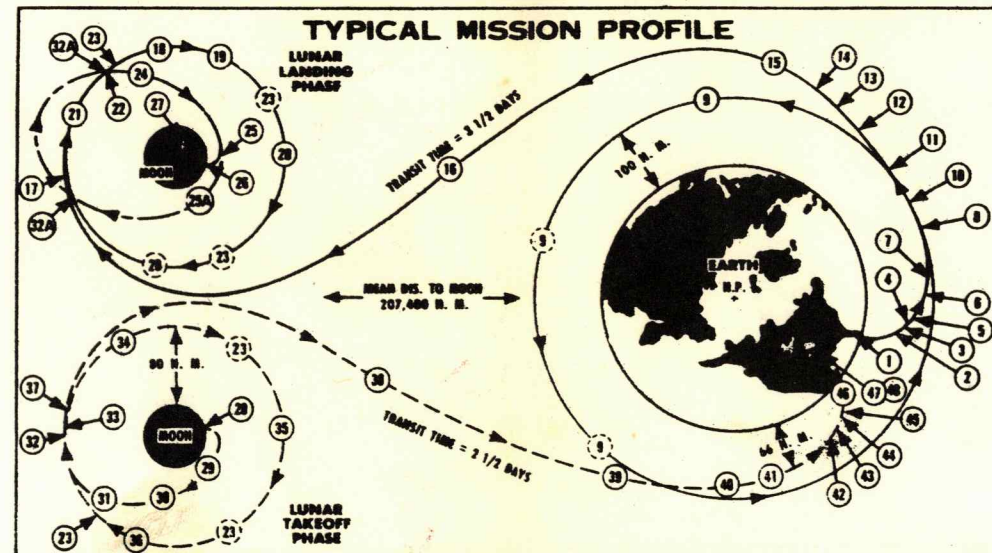
SATURN V APOLLO

LUNAR ORBITAL RENDEZVOUS MODE



SEQUENCE OF OPERATIONS*

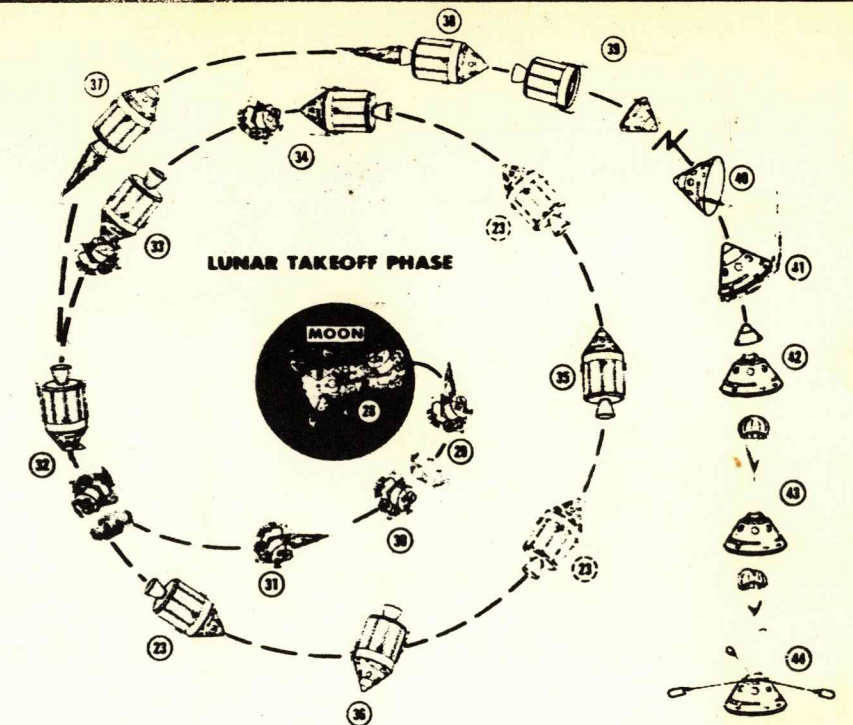
1. S-IC STAGE IGNITION & VEHICLE LAUNCH
2. S-IC STAGE CUTOFF & JETTISON (IGNITE S-IC RETRO & S-II ULLAGE ROCKETS)
3. S-II STAGE IGNITION & THRUST BUILDUP
4. JETTISON S-II AFT INTERSTAGE (AT APPROX. FULL THRUST)
5. LAUNCH ESCAPE SYSTEM JETTISON (AFTER FULL S-II THRUST & VEHICLE STABILIZATION)
6. S-II STAGE CUTOFF & JETTISON (IGNITE S-II RETRO & S-IVB ULLAGE ROCKETS)
7. S-IVB STAGE IGNITION & ORBITAL VELOCITY BUILDUP
8. INSERTION INTO 100 N. M. (185KM) EARTH PARKING ORBIT & S-IVB ENGINE CUTOFF
9. EARTH PARKING ORBIT COAST (CHECKOUT CREW & EQUIPMENT)
10. IGNITE ULLAGE ROCKETS, S-IVB RE-IGNITION & THRUST BUILDUP TO ESCAPE VELOCITY
11. INJECTION INTO EARTH-MOON TRANSIT & S-IVB ENGINE CUTOFF
12. JETTISON FORWARD SECTION OF I.U./APOLLO INTERSTAGE ADAPTER
13. CSM SEPARATION FROM LEM/L.U./S-IVB & CSM TURN AROUND
14. CSM DOCKING TO LEM/L.U./S-IVB
15. JETTISON AFT APOLLO ADAPTER SECTION & I.U./S-IVB
16. MIDCOURSE CORRECTION [IGNITION (S) & CUTOFF (S) OF SM PROPUSSION]*
17. SM IGNITION & BRAKING INTO LUNAR PARKING ORBIT, ENGINE CUTOFF
18. LUNAR PARKING ORBIT COAST (CHECKOUT CREW, EQUIPMENT & LEM)



19. CREW TRANSFER (2 MEN) FROM CM TO LEM
20. PRE-DESCENT LEM CHECKOUT & LANDING SITE RECONNAISSANCE
21. SEPARATE LEM FROM CSM & TURN AROUND LEM TO DESCENT ATTITUDE
22. LEM LANDING STAGE IGNITION & BURNING TO DESCENT ELLIPSE
23. CSM CONTINUES IN LUNAR PARKING ORBIT (1 MAN)
24. LANDING STAGE PROP. CUTOFF & COAST VIA ELLIPTICAL ORBIT TO NEAR LUNAR SURFACE
25. LEM LANDING STAGE RE-IGNITION & BRAKING OUT OF ELLIPTICAL ORBIT
26. LEM HOVER, TRANSLATION, DESCENT MANEUVERS & LUNAR LANDING
27. LUNAR STAY (SCIENTIFIC EXPLORATION, EXPERIMENTS, & SAMPLE GATHERING)
28. LEM LUNAR LAUNCH STAGE IGNITION & LAUNCH (LEAVE LANDING STAGE ON MOON)
29. LUNAR LAUNCH STAGE POWERED ASCENT TO HOHMANN TRANSFER ELLIPSE
30. LUNAR LAUNCH STAGE PROP. CUTOFF & COAST TO LUNAR ORBIT VIA HOHMANN ELLIPSE*
31. MIDCOURSE CORRECTION [IGNITION (S) & CUTOFF (S) OF MAIN PROPUSSION]*
32. MAIN ENGINE FIRING INTO CIRCULAR ORBIT, ENGINE CUTOFF, RENDEZVOUS & DOCKING
33. TRANSFER OF CREW (2 MEN) & SCIENTIFIC MATERIAL FROM LUNAR LAUNCH STAGE TO CM
34. JETTISON LEM LAUNCH STAGE (CONTINUES IN LUNAR ORBIT)
35. CHECKOUT OF CREW & CSM PRIOR TO LUNAR ORBIT ESCAPE
36. CSM ASSUME ATTITUDE FOR LUNAR ORBIT ESCAPE

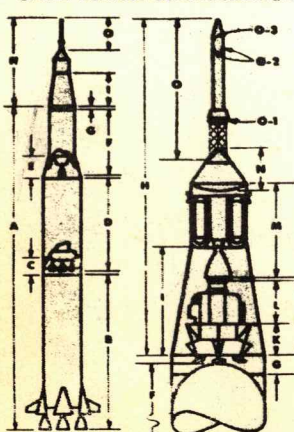
ALTERNATE EMERGENCY PROCEDURE

IF LEM CHECKOUT INDICATES LANDING NOT POSSIBLE, STEPS 25 THRU 32 ARE OMITTED AND THE FOLLOWING STEPS ARE TAKEN TO GET TO NO. 33:
 25A. LEM CONTINUES IN ELLIPTICAL ORBIT COAST
 32A. RENDEZVOUS & DOCKING AT POINT OF ELLIPTICAL & CIRCULAR ORBITS INTERSECTION



37. SM IGNITION, INJECTION OF CSM INTO MOON-EARTH TRANSIT, ENGINE CUTOFF
38. MIDCOURSE CORRECTION [IGNITION (S) & CUTOFF (S) OF SM PROPUSSION]*
39. CM SEPARATION AND JETTISON OF SM
40. CM ESTABLISH RE-ENTRY ATTITUDE
41. CM EARTH ATMOSPHERE RE-ENTRY & AERODYNAMIC MANEUVER TO NEAR LANDING SITE
42. JETTISON FWD. COMPARTMENT HEAT SHIELD (AT 50,000 FT.)
43. DROGUE CHUTE DEPLOYMENT (1 BY MORTAR AT 25,000 FT.)
44. PILOT CHUTE DEPLOYMENT (BY MORTAR AT 15,000 FT.) & DROGUE CHUTE RELEASE
45. MAIN CHUTE DEPLOYMENT (REEFED CONDITION)
46. FINAL DESCENT WITH FULL CHUTE
47. EARTH LANDING AND MAIN CHUTE RELEASE
48. LAND RECOVERY

SPACE VEHICLE CONFIGURATION



TECHNICAL DATA*

DESCRIPTION	MISSION	WEIGHT (LBS.)	LENGTH (FT.)	DIAMETER (FT.)	ENGINE TYPE	TOTAL THRUST (LBS.)	LIQUID PROPELLANT CAPACITY (LBS.)	APPROXIMATE VELOCITIES REQUIRED	
								INJECTION INTO 100 N. M. EARTH ORBIT	INJECTION INTO EARTH-MOON TRANSIT
A. 3 STAGE SATURN V LAUNCH VEHICLE	PAYLOAD TO PARKING ORBIT & ESCAPE VELOCITY	426.5 K	281.2	VARIABLE	5 F-1, 6 S-2	7,500 K (SEA LEVEL)	5,360 K	17,000	21,000
B. S-IC BOOSTER (SEE NOTE B-1)	INITIAL LIFT-OFF	300.0 K	138.0	33.0	5 F-1 LOX/JP-1	7,500 K (SEA LEVEL)	4,400 K	17,000	21,000
C. S-IC/S-II INTERSTAGE ADAPTER	TRANSMITS THRUST FORCES FROM S-IC TO S-II	15.0 K	18.3	33.0	-	-	-	17,000	21,000
D. S-II SECOND STAGE (SEE NOTE B-2)	VEHICLE VELOCITY BUILDUP FOR ORBITAL INJECTION	80.0 K	81.6	33.0	5 J-2 LOX/LH ₂	1,000 K (VACUUM)	930 K	17,000	21,000
E. S-II/S-IVB INTERSTAGE SHROUD	TRANSMITS THRUST FORCES FROM S-IC & S-II TO S-IVB	6.0 K	19.0	27.6 TO 33.0	-	-	-	17,000	21,000
F. S-IVB THIRD STAGE (SEE NOTE B-3)	APOLLO INJECTION INTO EARTH ORBIT AND EARTH-MOON TRANSIT	22.0 K	58.6	21.6	1 J-2 LOX/LH ₂	200 K (VACUUM)	230 K	17,000	21,000
G. LAUNCH VEHICLE INSTRUMENT UNIT (I.U.)	GUIDANCE & CONTROL OF LAUNCH VEHICLE	3.5 K	3.0	21.6	-	-	-	17,000	21,000
H. APOLLO SPACECRAFT	LUNAR BRAKING, ORBIT, LANDING, LAUNCH & EARTH RETURN	36.0 K	83.0	VARIABLE	3 HYPERGOLIC STORABLES	-	76.4 K	17,000	21,000
I. I.U./APOLLO INTERSTAGE ADAPTER	TRANSMITS LAUNCH VEHICLE THRUST TO CSM, HOUSES & SUPPORTS LEM	-	-	12.0 TO 21.6	-	-	-	17,000	21,000
J. LUNAR EXCURSION MODULE (LEM)	MANNED LUNAR LANDING AND TAKE OFF	-	-	15.0 (27.3 WITH LEGS EXTENDED)	2 HYPERGOLIC STORABLES	-	-	17,000	21,000
K. LEM LUNAR LANDING STAGE (SEE NOTE B-4)	LUNAR ORBIT(S) BRAKING, LUNAR HOVERING, TRANSLATION, DESCENT & LANDING	90.0 K	53.4	15.0	1 HYPERGOLIC STORABLE	10.5 K (VACUUM)	-	17,000	21,000
L. LEM LUNAR LAUNCH STAGE (SEE NOTE B-5)	LUNAR LAUNCH & INJECTION INTO LUNAR ORBIT	-	-	15.0	1 HYPERGOLIC STORABLE	3.5 K	-	17,000	21,000
M. SERVICE MODULE (SM) (SEE NOTE B-6)	MIDCOURSE CORRECTIONS, LUNAR BRAKING & ESCAPE PROPUSSION	-	-	12.8	1 HYPERGOLIC STORABLE	-	-	17,000	21,000
N. COMMAND MODULE (CM)	MANNED LUNAR ORBIT & EARTH RETURN, MAIN APOLLO CONTROL	-	-	12.8	NONE	21.9 K	-	17,000	21,000
O. APOLLO LAUNCH ESCAPE SYSTEM (LES)	CREW ESCAPE DURING ABORT	6.6 K	33.8	2.2	3 SOLID FUEL MOTORS	-	-	17,000	21,000
P. 1 TOWER ESCAPE MOTOR	PULLS CM CLEAR OF ABORTED LAUNCH VEHICLE	-	-	-	SOLID FUEL	130 K FOR 3+ SECS.	-	17,000	21,000
Q. 2 TOWER JETTISON MOTOR	JETTISONS TOWER AFTER SUCCESSFUL LAUNCH OR ABORT	-	-	-	SOLID FUEL	33 K FOR 1.2 SECS.	-	17,000	21,000
R. 3 PITCH MOTOR	PROVIDES TURN DIRECTION FOR LES TOWER OR LES/CM	-	-	-	SOLID FUEL	5 K FOR 1.2 SECS.	-	17,000	21,000
FOR VEHICLE (TOTAL)	MANNED LUNAR LANDING AND RETURN	6,000 K	364.2	MAX 33.0	14 MA. 1 PROPUSSION ENG'S	-	-	17,000	21,000

CSM = CM/SM

* UNDERLINED WEIGHTS INCLUDE LIQUID PROPELLANTS; OTHERS ARE DRY

K=1000

PHYSICAL DATA

MEAN DIAM. IN MILES	NAUTICAL STATUTE	EARTH MOON	
		6,875	1,877
		7,917	3,161
		1.0	1/6.0
		AIR	VACUUM
		MEAN	212°
		IN SHADOW	57.2°

NOTES:

1. COAST PERIODS ARE BETWEEN POSITIONS 8 & 10, 11 & 16, 16 & 17, 17 & 22, 24 & 25, 30 & 31, 31 & 32, 32 & 37, 37 & 38, 38 & 41. (NO MAIN PROPUSSION SYSTEM IN OPERATION).
2. ULLAGE ROCKET FIRING REQUIRED BEFORE IGNITIONS 3, 7, AND 10 TO FORCE PROPELLANTS TO BOTTOM OF TANKS BEFORE MAIN PROPUSSION IGNITION.
3. MULTIPLE RESTARTS (AS REQUIRED DURING COAST PERIODS FOR TRAJECTORY CORRECTIONS).
4. * ENGINES THAT USE A FUEL AND OXIDIZER BIOPROPELLANT, STORABLE AT NORMAL TEMPERATURES, THAT IGNITE SPONTANEOUSLY WHEN THE FUEL & OXIDIZER ARE MIXED.
5. AN OPTIMUM FLIGHT PATH USING AN ELLIPTICAL COASTING TRANSFER WITH POWERED FLIGHT AT LAUNCH AND TERMINAL POINTS ONLY (VS. CONTINUOUS BURN) TO CONSERVE PROPELLANTS.
6. - INDICATES SCALE CHANGE IN STAGE AND MODULE SKETCHES.
7. * THESE DIAGRAMS HAVE BEEN PURPOSEFULLY ALTERED IN SCALE AND PERSPECTIVE TO BETTER SHOW CONFIGURATIONS AND OPERATIONAL SEQUENCE, AND ARE FOR INFORMATIONAL PURPOSES ONLY. FOR CLARITY'S SAKE, VERY LITTLE CONSIDERATION HAS BEEN GIVEN TO RELATIVE MOTIONS AND POSITIONS OF THE EARTH VS. THE MOON DURING ELAPSED TIME INTERVALS SHOWN. THIS CHART REPRESENTS ONE OF SEVERAL TYPICAL PROFILES CURRENTLY BEING CONSIDERED AND IS SUBJECT TO CONTINUOUS CHANGE. ALL TECHNICAL DATA SHOWN IS APPROXIMATE.
8. PROPUSSION SYS. CAPABLE OF (A) RESTART (B) GIMBALLING () THROTTLING



MARSHALL SPACE FLIGHT CENTER

EX-5-5004 JANUARY 10, 1966

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RAYTHEON COMPANY

SPACE AND INFORMATION SYSTEMS DIVISION

