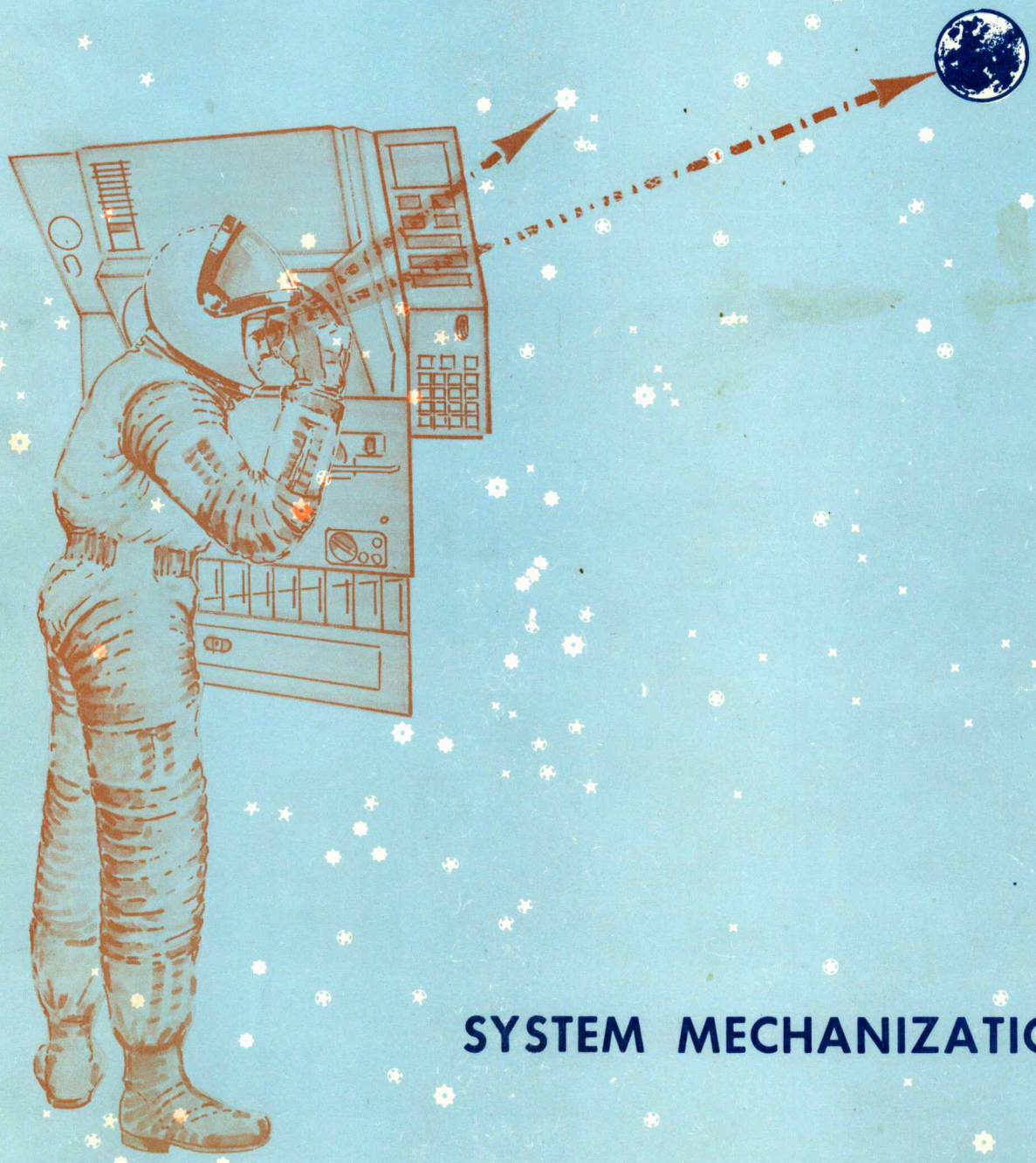
APOLLO GUIDANCE AND NAVIGATION SYSTEM STUDY GUIDE

CM PRIMARY GUIDANCE NAVIGATION AND CONTROL SYSTEM



SYSTEM MECHANIZATION

AC ELECTRONICS DIVISION

GENERAL MOTORS CORPORATION

APOLLO

COMMAND MODULE

PRIMARY GUIDANCE, NAVIGATION AND CONTROL SYSTEM

STUDENT STUDY GUIDE

C/M PGNCS

LEVEL III

SYSTEM MECHANIZATION COURSE SM-2100

PREPARED BY

AC ELECTRONICS

DIVISION OF GENERAL MOTORS

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PREFACE

This student study guide has been prepared by AC Electronics in response to:

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for

System Assembly and Test, Inertial

Measurement Unit, Coupling Display Unit

Power and Servo Assembly - Project APOLLO

This study guide contains training material and should be used for instructional purposes only.

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OBJECTIVES

The intent of this study guide is to give the student a basic understanding of the CM PGNCS system mechanization. The computer hardware input/output interface section is intended to tie together the G&N system. The computer control and operation of the system will be described in future Computer Program Study Guide.

This study guide is used in conjunction with the CM PGNCS Course No. SM-2100. The study guide will be presented to the student on the first day of the class and retained by the student after the course as a reference document. Maximum blank space is available throughout the study guide to accommodate the student's class notes.

The study guide is organized in the sequence of instruction of the course and is divided into 10 major sections. Each section contains the documentation and copies of the visual aids used during the class presentation of the section. A summary is included at the end of each section to be used by the student for review.

The objectives of this study guide are to provide the student with:

a. The course materials organized in the sequence of classroom presentation for self-study.

b. A list of references for further self-study.

c. Section summaries for reviewing.

REFERENCES

The following documents were used in the preparation of this study guide:

LED-540-12	Design Reference Mission Apollo Mission Planning Task Force
R-477	Guidance and Navigation System Operations Plan
R-467	The Complete Sunrise Being a Description of Program Sunrise
R-500	Space Navigation Guidance and Control
R-445	Technical Development Status of Apollo Guidance and Navigation
R-446	Primary G & N System Lunar Orbit Operations (Vol. I and II) Confidential
DD 254	Digital Development Memor # 254 - Revision B, Block II Channel Assignments - 27 April 66
2010082	IMU Auxiliary Schematic
2015563	Two Wire Mechanization of Apollo PIPA Loops
2015564	Two Wire Mechanization of Apollo Stabilization Loop
2015567	Optics Trunnion and Shaft CDU Block Diagram (2 Line)
MH01-01380-216	CMC/Spacecraft Electrical Interface
ND 1021043	Primary Guidance, Navigation, and Control System Manual
2015562	CSM 5-Axis Moding
FH2100	CM PGNCS Student Study Guide

SECTION I

INTRODUCTION TO THE PRIMARY GUIDANCE, NAVIGATION AND CONTROL SYSTEM (PGNCS)

INTRODUCTION

This section describes the PGNCS requirements for the Apollo mission and the relationship of the PGNCS to the spacecraft and the astronaut. The section also briefly discusses the PGNCS functions as related to the Apollo lunar orbit mission phases.

1.1 GUIDANCE, NAVIGATION AND CONTROL REQUIREMENTS

The Apollo PGNCS performs three basic functions: inertial guidance, optical navigation and spacecraft control as shown in Figure 1-1. These three basic functions are discussed below.

1.1.1 INERTIAL GUIDANCE. The inertial guidance portion of the PGNCS employs accelerometers mounted on a gyroscopically stabilized, gimbal-mounted platform and a central data processing element. The inertial guidance system senses acceleration and attitude changes instantaneously and provides attitude control and thrust control signals to the service propulsion and reaction control systems.

1.1.2 OPTICAL NAVIGATION. The optical navigation portion of the PGNCS employs a scanning telescope and sextant to make sightings of celestial bodies and landmarks on the surface of the moon and earth. These sightings are used by the data processing element to:

a. Determine the spacecraft position and velocity.

b. Establish proper alignment of the stable platform.

A digital computer serves as the central data processing element of the PGNCS. It contains a catalog of celestial bodies and is programed to calculate steering, thrust and alignment commands using the information obtained from the optical sightings and the inertial measurement unit. The computer uses data on gravitational fields and celestial perturbations to calculate future position and velocity of the spacecraft.

1.1.3 CONTROLS AND DISPLAYS. The control portion of the PGNCS uses information from the inertial guidance portion to keep the axes that are fixed to the spacecraft structure to remain nearly aligned to the stabilization reference axes. The control portion also functions to keep the spacecraft velocity vector approximately aligned with the stabilization reference velocity vector. A direct statement defining control could be "spacecraft rotational and translational management".

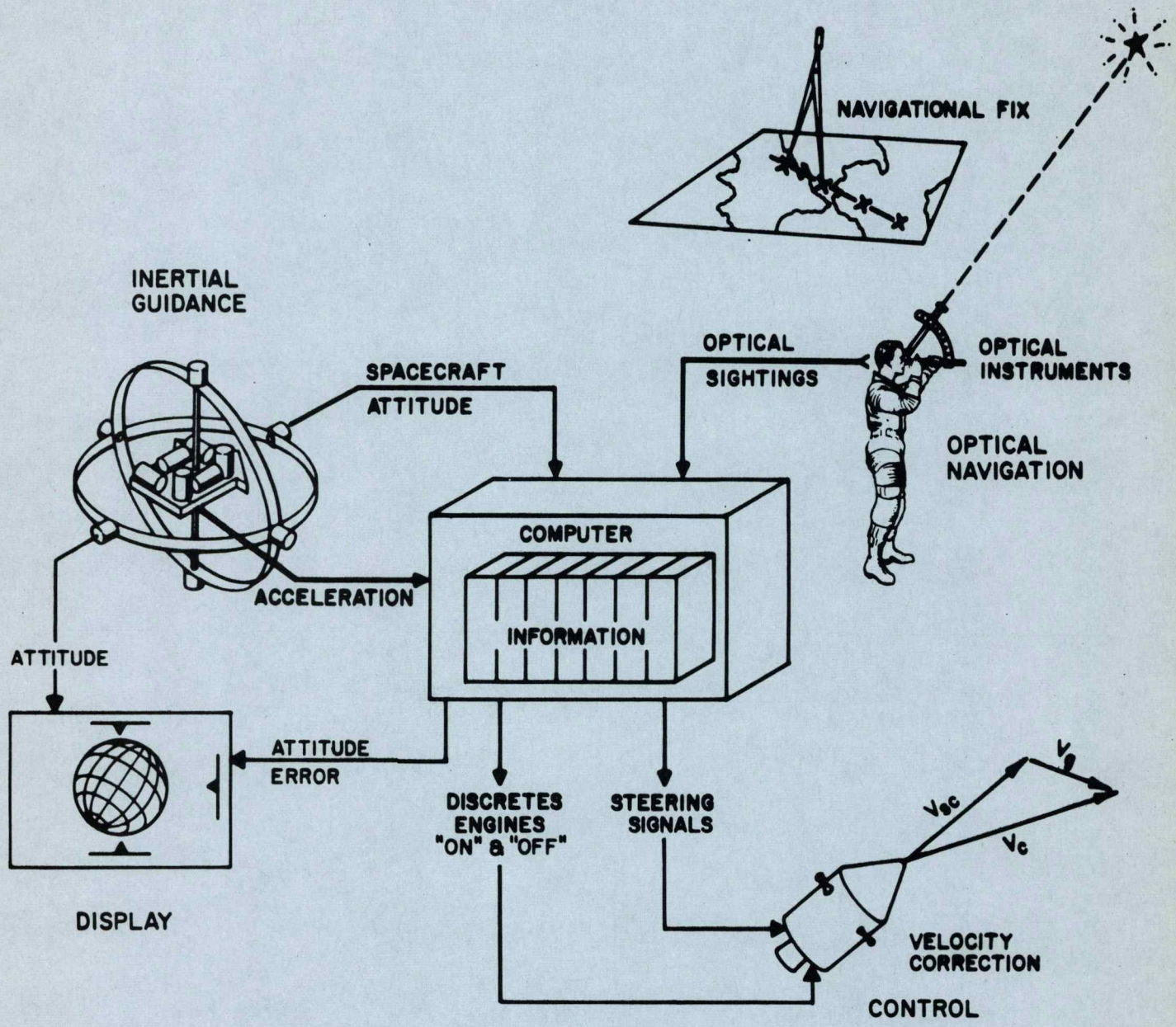


Figure 1-1. PGNCS Requirements

1.2 PGNCS INTERFACE

The Apollo PGNCS has direct interface with six spacecraft systems: the stabilization and control system, service propulsion system, reaction control system, electrical power system, environmental control system and the communication and instrumentation system.

1.2.1 SPACECRAFT SYSTEMS INTERFACE. The PGNCS interface with the various spacecraft systems is illustrated in Figure 1-2 and described in the paragraphs below.

1.2.1.1 Stabilization Control System. The stabilization control system (SCS) is located in the command module and can sense and control spacecraft attitude and velocity changes during any phase of flight. Steering and thrust signals can be generated by either the PGNCS or the SCS.

The stabilization control system consists of two body mounted attitude gyro packages, an accelerometer package, control electronics assembly, gyro display coupler, an attitude set control assembly, two flight director attitude indicators, and the necessary displays and controls to operate and monitor the system. The stabilization control system can operate as a backup system for the PGNCS. Attitude, attitude error, and attitude rate are displayed to the astronauts. Interface signals from the PGNCS to the stabilization control system consist of attitude signals, attitude errors, and technological backup data.

1.2.1.2 Service Propulsion System. The service propulsion system (SPS) provides the thrust capability to change the spacecraft's velocity. The system is normally operated by the PGNCS.

The service propulsion system is utilized for mission abort, midcourse velocity corrections and orbital injections. The system is located in the service module and consists of helium, fuel and oxidizer storage tanks, a gimbaled thrust chamber, propellant control valves and distribution equipment. The service propulsion system operates on a helium-pressurized hypergolic propellant and is capable of developing 21,900 pounds of thrust. The gimbal mechanism allows the thrust chamber to be displaced 0 $\pm 6^{\circ}$ in pitch and 0 $\pm 8^{\circ}$ in yaw.

1.2.1.3 Reaction Control Systems. Two reaction control systems (RCS) are utilized for attitude control and stabilization of the spacecraft. The systems can be operated directly by the PGNCS. One reaction control system is required for the command module and another for the service module. Each system consists of helium, fuel and oxidizer tanks, propellant control valves, fixed thrust chambers and distribution equipment.

The reaction control system of the command module consists of two independent, and equally capable, pressurized reaction jet subsystems. The two subsystems are operated simultaneously and provide three-axis control of the command module. In event one reaction jet subsystem fails, the remaining reaction jet subsystem is capable of providing the control necessary for safe entry. The reaction jet subsystem provides four engine nozzles for each type of maneuver - roll, pitch and yaw. Each of the 12 engines develops a nominal thrust of 100 pounds. The engine exhaust ports are flared into the skin of the command module. The engines are located in the aft equipment and forward parachute compartments of the command module.

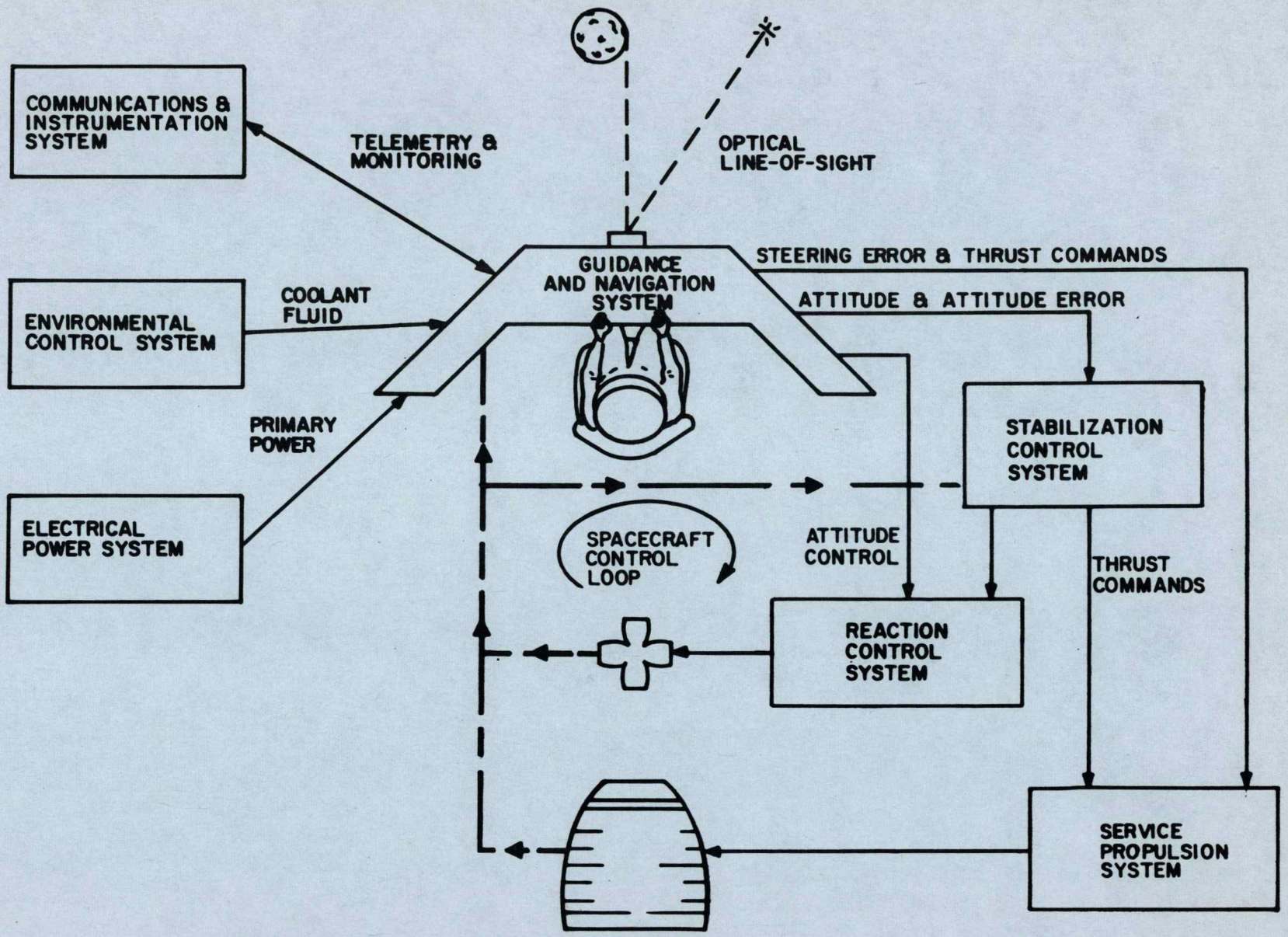


Figure 1-2. PGNCS Spacecraft Interface

The service module reaction control system consists of four equally capable hypergolic propellant pressurized reaction jet subsystems. The subsystems are located in the forward section of the service module and are mounted 90° apart. Each subsystem has four engine nozzles. Eight of the 16 nozzles are used for roll control, four for pitch and four for yaw. Each nozzle provides a nominal thrust of 100 pounds.

1.2.1.4 Electrical Power System. The primary power required to operate the PGNCS are supplied by a hydrox fuel cells in the service module which are used during all mission phases except entry and recovery. Three zinc-silver oxide storage batteries in the command module furnish power during entry and recovery.

The hydrox fuel cells operate in parallel and are capable of producing a 27 to 31 volt dc output. The output is converted by a solid state inverter into 115 volt, 400 cycle power. The DC and AC powers are used for normal PGNCS operation. In case of an emergency, any two cells could meet all power requirements. The modules utilize hydrogen and oxygen as the reactants and potassium hydroxide as the electrolyte. The reactants are stored in tanks that are part of the cryogenic gas storage system which also furnishes oxygen to the environmental control system. The water formed by operating the fuel cells is collected and delivered to the environmental control system as potable water.

Auxiliary electrical power is provided by the three batteries in the command module. Two of these batteries supply supplementary power during peak loads on the fuel cell. The third battery is isolated from the electrical power system and is used only for post-landing loads. A solid state battery charger is provided to recharge any of the three batteries after normal or emergency discharge.

1.2.1.5 Environmental Control System. An environmental control system (ECS) is used to sustain life in space. The system provides breathable atmosphere, acceptable temperatures, food and water, waste disposal and radiation protection. The Apollo environmental control system is essentially a storage type in which the life support elements (breathable gasses, water, food, etc.) are stored and used as needed, and the waste products collected and stored for disposal. However, some features of a regenerative system in which usable material is extracted from the metabolic waste are used in the Apollo environmental control system, especially in the conservation of water.

The environmental control system provides an atmosphere of 100 percent oxygen at approximately 5 psia. Cabin temperature is maintained between 70 and 80° F. and relative humidity between 50 and 60 percent. In addition, a water-glycol coolant fluid is circulated about the temperature sensitive components of the PGNCS and other spacecraft systems for thermal stability. In the event of cabin decompression, the crew pressure suits supply a conditioned oxygen atmosphere of 3.5 psia.

1.2.1.6 Communication and Instrumentation System. The Apollo communication and instrumentation system (C&IS) provides voice, television and telemetry communications with the earth and voice communications between crew members. A television system permits ground viewing of external and remote section of the spacecraft during flight. Telemetry data can be stored when direct communication with the earth is not possible because of the location of earth communication facilities or because the spacecraft is behind the moon. The earth stations can determine spacecraft position and transmit this information to the crew to supplement information obtained from onboard navigational systems. Critical signals of the PGNCS are conditioned and supplied to pulse code modulated (PCM) telemetry equipment for transmission to ground stations. Data transmitted from earth stations can be loaded into the PGNCS.

1.2.2 ASTRONAUT INTERFACES. The astronaut is an active and controlling part of the PGNCS system. He is able to monitor information to and from the PGNCS and can manually duplicate PGNCS control functions. The astronaut activities are classified into the following five types:

a. Take Optical Sighting: The astronauts identify, select, and track celestial objects. The sightings are used to align the inertial reference and determine spacecraft position.

b. Monitor System Performance: Mode, condition, and failure lights are monitored by the astronauts to determine system status. As calculations are performed by the computer, the results are displayed for astronaut evaluation and verification with ground calculated data.

c. Load Data: Data is loaded into the computer through the computer keyboard by the astronaut. The data includes such information as star selection, positional data and system angles.

d. Select Mode of Operation: The astronaut, by means of the displays and controls, can select the equipment modes of operation for the different spacecraft systems required to perform a particular function. In some cases, the sequencing of modes is controlled by the computer. The program being performed by the computer can be selected by the astronaut or initiated internally by the computer.

e. Provide System Backup: In case of PGNCS failure, the astronaut provides manual control of the spacecraft and performs those functions normally performed by the PGNCS.

1.3 PGNCS SUBSYSTEMS

The PGNCS is divided into three major subsystems: inertial, optical, and computer. The PGNCS is designed so that each subsystem can be operated independently during an emergency or backup mode. Therefore, the failure of one subsystem will not place the entire PGNCS out of commission. The three subsystems, or combinations of subsystems, with assistance from the astronaut can perform the following functions:

a. Periodically establish an inertial reference which is used for measurements and computations.

b. Align the inertial reference by precise optical sightings.

c. Calculate the position and velocity of the spacecraft by optical navigation and inertial guidance.

d. Generate attitude error signals and thrust commands necessary to maintain the required spacecraft trajectory.

e. Provide the astronaut with a display of data which indicates the status of the guidance and navigation problem.

f. Provide spacecraft rotational and translational management.

1.3.1 PGNCS SYSTEM EQUIPMENT. The PGNCS (Figure 1-3) consists of a navigation base, inertial measurement unit (IMU), optical assembly, power and servo assembly (PSA), command module computer (CMC), G&N indicator control panel, coupling data unit (CDU), PIPA Electronics Assembly (PEA) a signal conditioner assembly and two display and keyboards (DSKY's).

Figure 1-4 shows the PGNCS equipment installed in the spacecraft. The navigation base is mounted to the spacecraft sidewall and is used as a holding fixture for the IMU and optical assembly. The IMU and optical assembly are attached and precisely aligned to the navigation base. The lower display and control panel comprises the front of the PGNCS structure and contains several individual panels. The panels with displays and controls are located so the astronaut can view and manually operate the controls from a standing position. The PSA, which contains power supplies, amplifiers and miscellaneous electronics, is mounted on a cold plate below the navigation base and indicator control panel. All PSA modules are plugged into a single flat interconnect harness assembly which attaches to the cold plate. Immediately below the PSA is the command module computer and mounted to the left of the CMC is the coupling data unit. The PEA is mounted to the left of the IMU to reduce cable lengths for critical switching signals. The signal conditioners and one DSKY are mounted to the right of the optical assembly and indicator control panel. The various hardware elements are interconnected by a cabling harness.

The following paragraphs present a brief functional description of the three PGNCS subsystems. Figure 1-5 illustrates the signal flow and interface between the subsystems.

1.3.2 INERTIAL SUBSYSTEM. The inertial subsystem consists of the IMU mounted on the navigation base, a portion of the coupling data unit, portions of the power servo assembly and the PIPA electronics assembly. Associated with the inertial subsystem but located on the main display and control panel are the power switches and an IMU cage switch.

The ISS is used in the Primary Guidance, Navigation and Control System to determine the direction and magnitude of the velocity corrections applied to the spacecraft. To conserve fuel, velocity corrections are kept to a minimum and applied only periodically. Therefore, electrical power also can be conserved by limiting the use of the ISS to about 20 percent of the flight time.

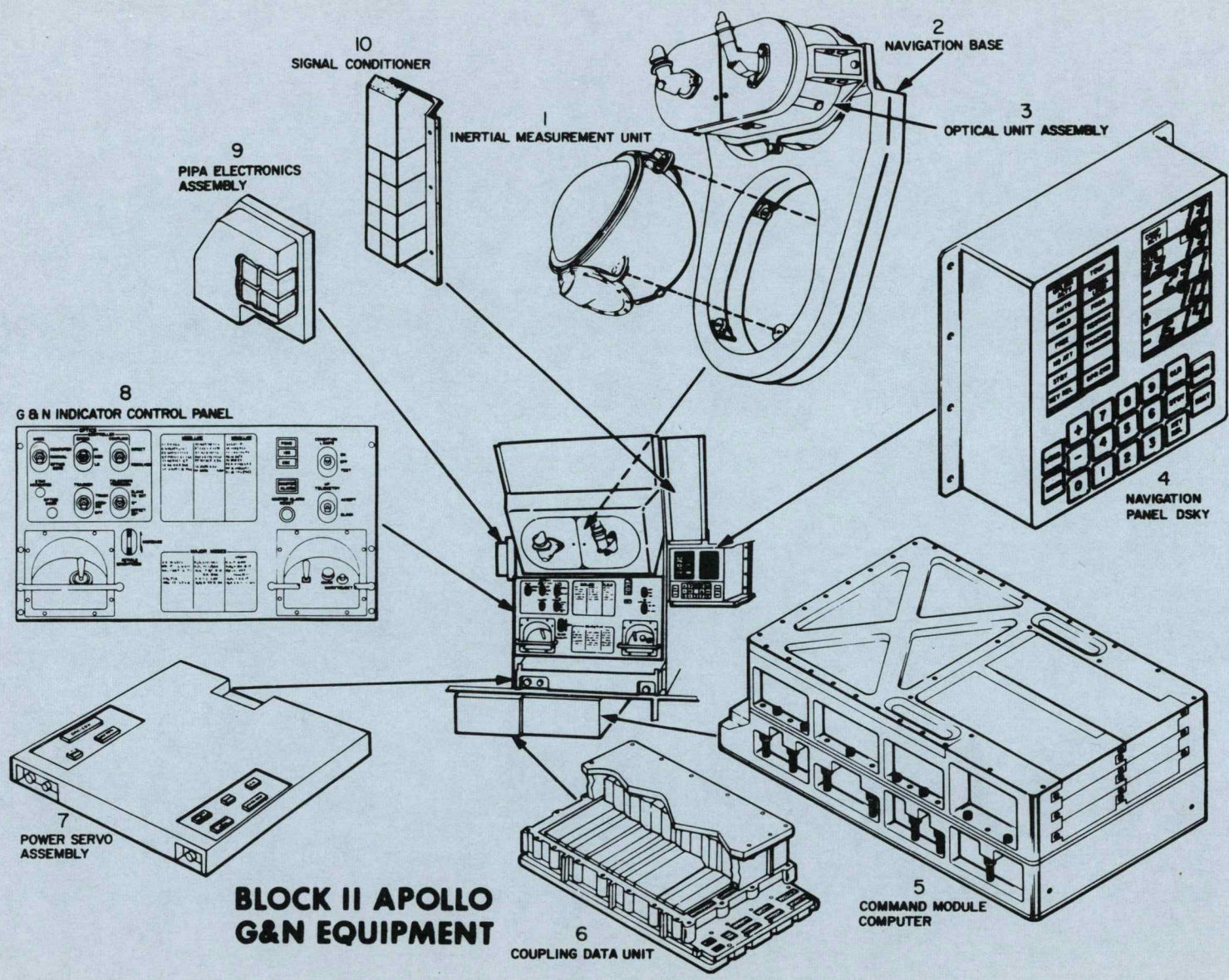


Figure 1-3. PGNCS Equipment

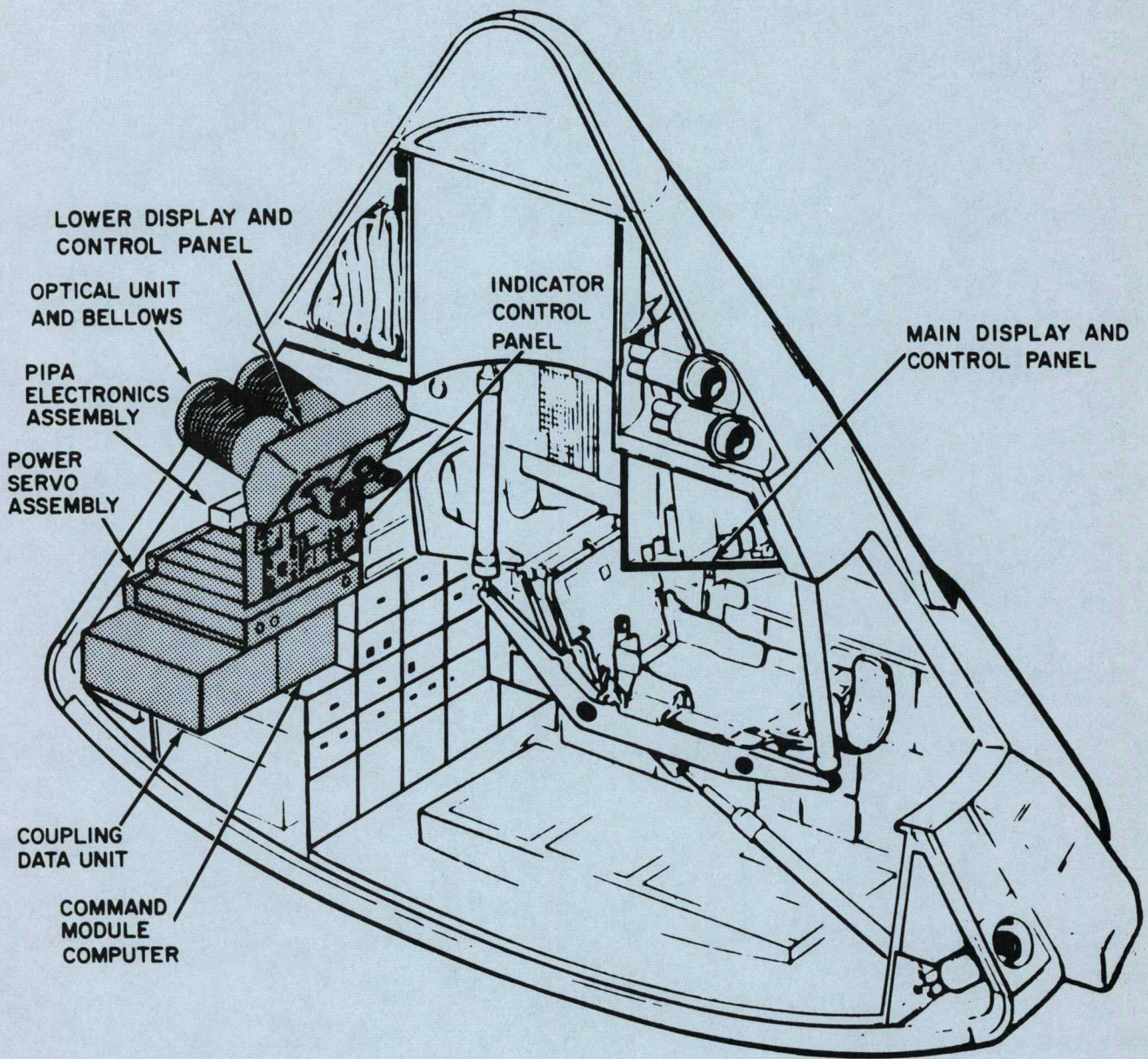


Figure 1-4. Location of PGNCS Equipment in the Spacecraft

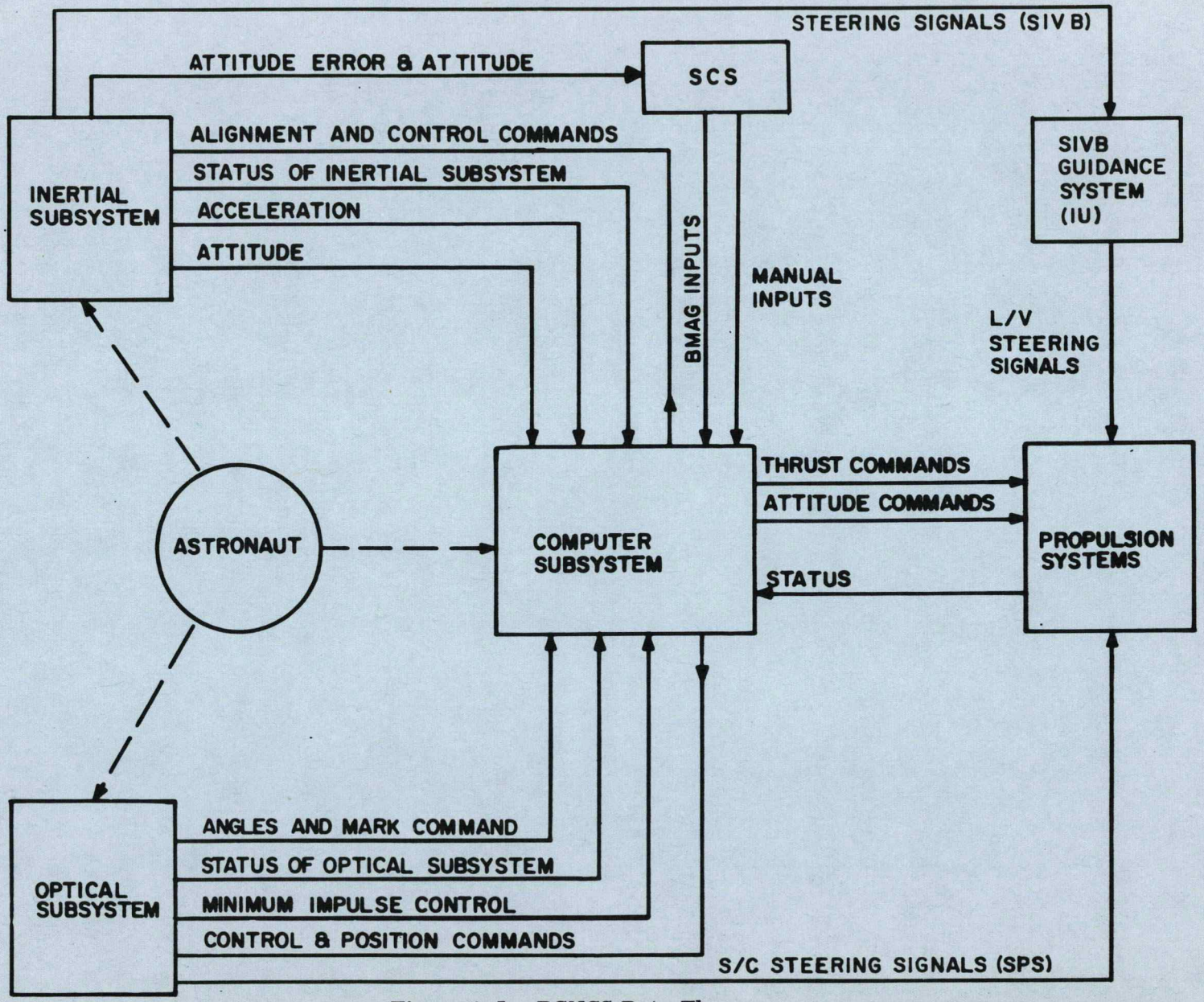


Figure 1-5. PGNCS Data Flow

The inertial subsystem performs three major functions: (1) measures changes in spacecraft attitude, (2) assists in generating steering commands and (3) measures spacecraft velocity changes due to thrust. To accomplish these functions, the IMU provides an inertial reference consisting of a stable member with three degrees of freedom and stabilized by three integrating gyros. When the inertial subsystem is operated prior to launch, the stable member is aligned through a gyro compassing routine and, during flight, it is aligned by sighting the optical instruments on stars. If the inertial subsystem is operated over a prolonged period of time, realignment may be necessary since the gyros which maintain the space referenced stable member may drift and cause an error in flight calculations.

Once the inertial subsystem is energized and aligned, any rotational motion of the spacecraft will be about the gimbaled stable member, which remains rotationally fixed in space. Resolvers, mounted on the gimbal axes, act as angular sensing devices and measure the attitude of the spacecraft with respect to the stable member. These angular measurements are displayed to the astronauts by the flight director attitude indicator (FDAI) and angular changes are sent to the CMC.

Desired spacecraft attitude is calculated in the CMC and compared with the actual gimbal angles. Any difference between the actual and calculated angles causes a digital attitude error signal to be generated by the computer and converted to an analog signal in the CDU. The error signal is sent to the service propulsion system engine gimbal controls to correct the spacecraft attitude and to FDAI for display.

Acceleration of the spacecraft is sensed by three pendulous accelerometers mounted on the stable member with their input axes orthogonal. The resultant signals from the accelerometer loops are supplied to the CMC which then calculates the total velocity.

The modes of operation of the inertial subsystem can be initiated automatically by the CMC or by astronaut selection of computer program through the computer keyboard. The status or mode of operation is displayed on the display and keyboard as determined by data from the computer.

1.3.3 OPTICAL SUBSYSTEM. The optical subsystem consists of the optical assembly mounted on the navigation base, a portion of the CDU, portions of the PSA, and the G&N indicator control panel.

The optical subsystem is used to determine the position and orientation of the spacecraft in space. This is accomplished through the use of a catalog of stars stored in the CMC and celestial measurements. The identity of celestial objects and the schedule of measurements is determined before launch and is based on an optimum plan.

The optical subsystem performs two major functions: (1) provides the CMC with data obtained by measuring angles between lines-of-sight to celestial objects, and (2) provides measurements for establishing the inertial reference.

The optical subsystem contains a sextant and telescope. The sextant is a high magnification and dual line-of-sight device used for precision angular measurements. The telescope has a wide field of view, one line-of-sight device and is used for coarse acquisition of stars and landmarks and orbital tracking of landmarks.

The optical instruments are located side by side on the navigation base. The astronaut makes observations by sighting through the sextant or telescope eyepieces located on the display and control panel. The modes of operation of the optical subsystem are indicated on the G&N indicator control panel and are supplied to the CMC. A sextant hand controller on the front of the G&N indicator control panel is used by the astronaut to position the optical lines-of-sight. Since the field of view of the optical instruments is limited, controls are also provided by which the astronaut can maneuver the entire spacecraft to point the optical instrument in any desired direction. The astronaut initiates a timing mark which causes the CMC to record both optical and inertial angles and the time at the instant the sextant is properly positioned for a measurement.

1.3.4 COMPUTER SUBSYSTEM. The computer subsystem consists of the command module computer and portions of the display and control panels.

The computer subsystem is used to perform space flight data handling and computations. The CMC is a general purpose digital computer employing a core memory, parallel operations and a built-in self-check capability.

Programs stored in the CMC are selected to control and solve flight equations. The selection of programs can be controlled by automatic sequencing or manually by the astronaut.

The computer subsystem performs six major functions: (1) calculates steering signals and engine discretes necessary to keep the spacecraft on the required trajectory during all mission phases, (2) positions the stable member in the IMU to a coordinate system defined by precise optical measurements, (3) positions the optical unit to celestial objects, (4) conducts limited malfunction isolation of the PGNCS by monitoring the level and rate of system signals, (5) supplies pertinent spacecraft condition information to the display and control panels, and (6) supplies discretes to spacecraft controls.

Using information from navigation fixes, the CMC computes deviations from the required trajectory and calculates the necessary corrective attitude and thrust commands. The velocity corrections are controlled by the computer subsystem by processing incremental velocity from the inertial subsystem. Velocity corrections are not made continuously, but rather are initiated at predetermined check points in the flight. The technique of check point velocity corrections reduces fuel consumption, since the engines are used only when a significant correction in velocity is required. The CMC also uses information from celestial measurements to align the stable member in the IMU to a defined coordinate system.

Malfunctions in the PGNCS are detected by the CMC by monitoring critical signals and rates. Lamps on the indicator control panel light to indicate malfunctions.

Numerical displays on the display and keyboard indicate the program being solved by the CMC or the results of calculations. Selection of a computer program or insertion of data into the CMC can be done by the astronaut with a keyboard or by uplink data through the communication and instrumentation system from the ground station.

1.4 PGNCS FUNCTIONS AND RELATION TO MISSION PHASES

Major PGNCS functions associated with the Apollo lunar orbit mission phases include (1) prelaunch IMU alignment, (2) guidance monitor, (3) orbital navigation, (4) inflight IMU alignment, (5) midcourse navigation, (6) attitude control, (7) thrust maneuver, and (8) entry. These functions are used during the mission phases described in Figure 1-6. Table 1-1 tabulates the probable PGNCS functions during each mission phase. The following is a brief description of each function.

1.4.1 PRELAUNCH IMU ALIGNMENT. During prelaunch alignment, the IMU stable member is vertically erected. The stable member is then aligned in azimuth and held to this earth reference through a gyro compassing routine in the computer. Initial azimuth is confirmed by sighting on a ground target with the optics prior to closeout of the command module. See Figure 1-7.

1.4.2 GUIDANCE MONITOR. The PGNCS monitors the SIV-B guidance during earth ascent and translunar injection. At launch, the IMU is switched from an earth reference frame (inertially stabilized). The astronaut then used the PGNCS to monitor the spacecraft flight profile.

1.4.3 ORBITAL NAVIGATION. During earth and lunar orbit, the astronaut checks the orbital trajectory and the alignment of the IMU by means of optical sightings. The astonaut takes sightings by identifying and tracking landmarks with the optical instrument. The computer records optical and IMU gimbal angles and time and calculates the orbital trajectory. See Figure 1-8.

1.4.4 INFLIGHT IMU ALIGNMENT. This IMU alignment will be performed during the following mission phases: (1) earth orbit, (2) translunar coast, (3) lunar orbit and (4) transearth coast. IMU alignment in flight is accomplished by means of optical sightings. The astronaut takes star sightings and the computer records the optical and IMU gimbal angles. The computer then calculates and applies torquing commands necessary to align the IMU. See Figure 1-9.

1.4.5 MIDCOURSE NAVIGATION. This PGNCS function is performed many times during the translunar and transearth mission phases. Midcourse navigation is accomplished by taking star-landmark optical sightings. The computer records the optical angles and the time of sighting. Spacecraft position and velocity can then be updated by the computer. See Figure 1-10.

1.4.6 ATTITUDE CONTROL. This PGNCS function is used during the translunar and transearth coast phases when the ISS is activated. The ISS then provides the inertial reference to maintain the spacecraft attitude. Spacecraft attitude is controlled by CMC operation of the RCS jets using attitude information provided by the IMU.

1.4.7 THRUST MANEUVER. There are two types of thrusting maneuvers associated with the lunar mission: (1) Midcourse corrections which are short duration (minor) thrusting maneuvers and (2) orbital injections which are long duration (major) thrusting maneuvers.

During the minor thrusting maneuver the computer, after calculating the spacecraft position and velocity from a midcourse navigation sighting, determines the need for a midcourse velocity correction. This is done by comparing the actual trajectory

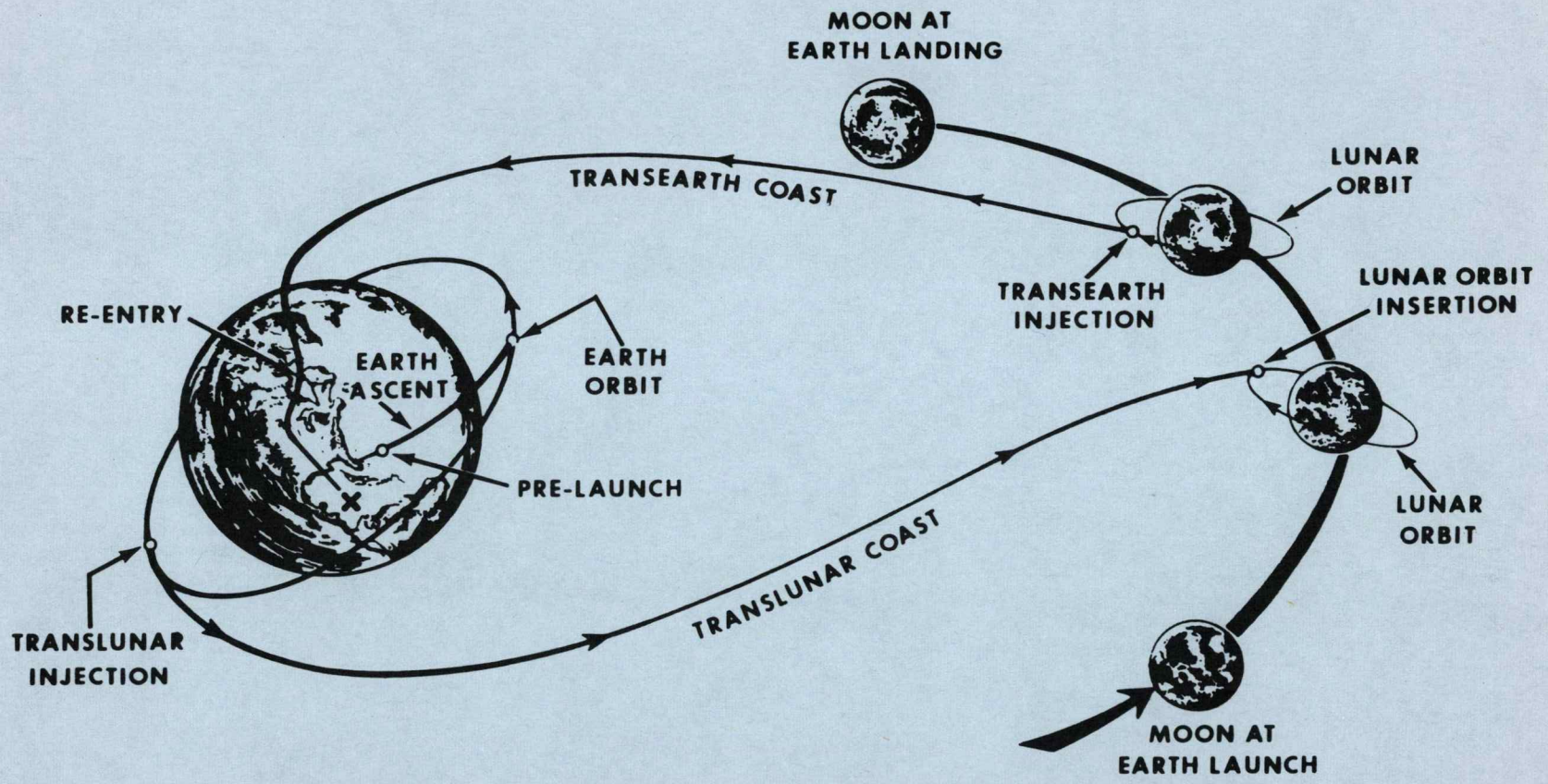


Figure 1-6. Mission Phases Required for a Lunar Orbit

Table 1-1. Normal PGNCS Functions per Mission Phase

LUNAR ORBIT MISSION PHASES	PRELAUNCH IMU ALIGNMENT	GUIDANCE MONITOR	ORBITAL NAVIGATION	INFLIGHT IMU ALIGNMENT	MIDCOURSE NAVIGATION	ATTITUDE CONTROL	THRUST MANEUVER	ENTRY
PRELAUNCH	X							
EARTH ASCENT		X						
EARTH ORBIT			X	X				
TRANSLUNAR INJECTION		X						
TRANSLUNAR COAST				X	X	X	X	
LUNAR ORBIT INSERTION						X	X	
LUNAR ORBIT			X	X		X		
TRANSEARTH INJECTION						X	X	
TRANSEARTH COAST				X	X	X	X	
ENTRY								X

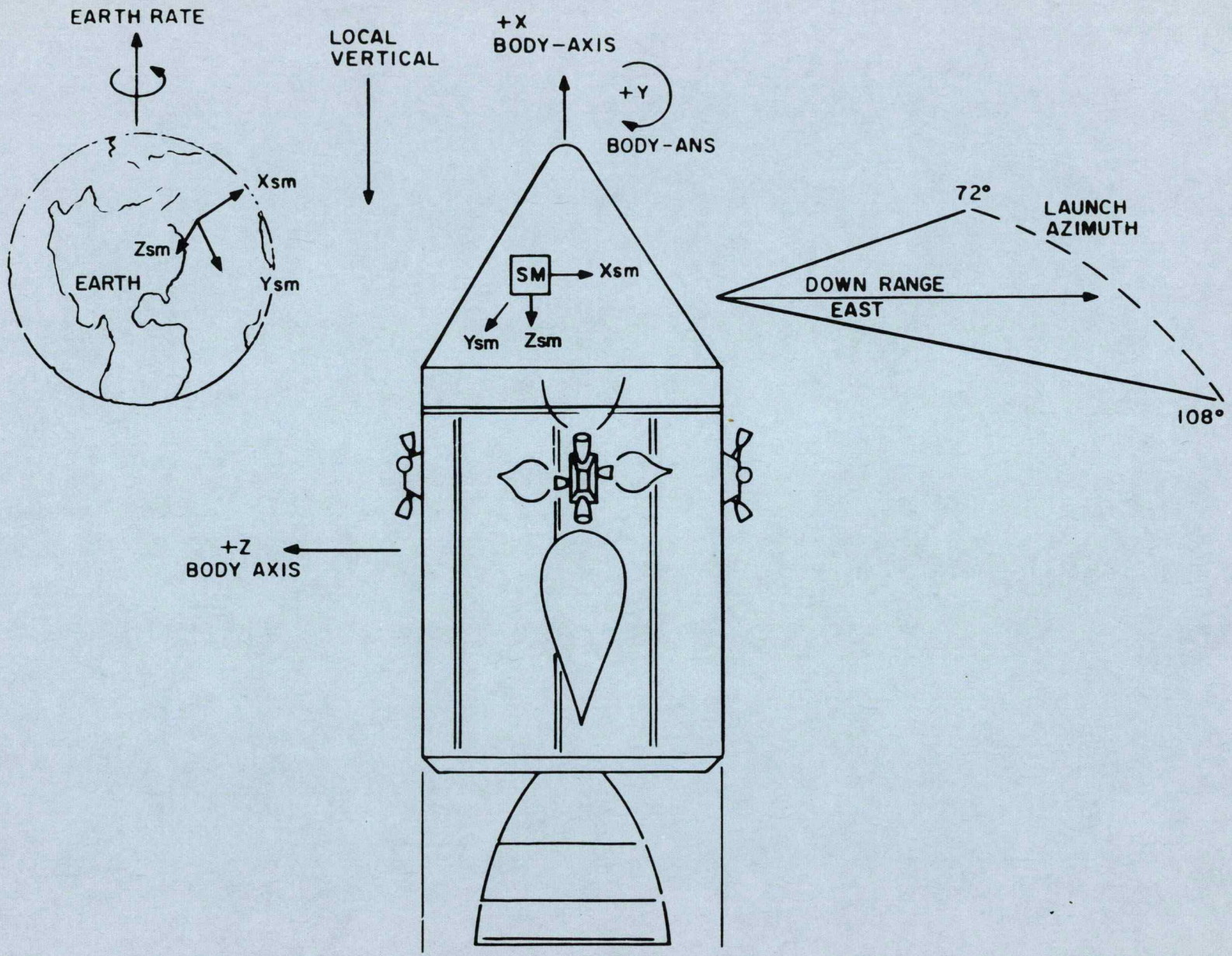


Figure 1-7. **Prelaunch Alignment**

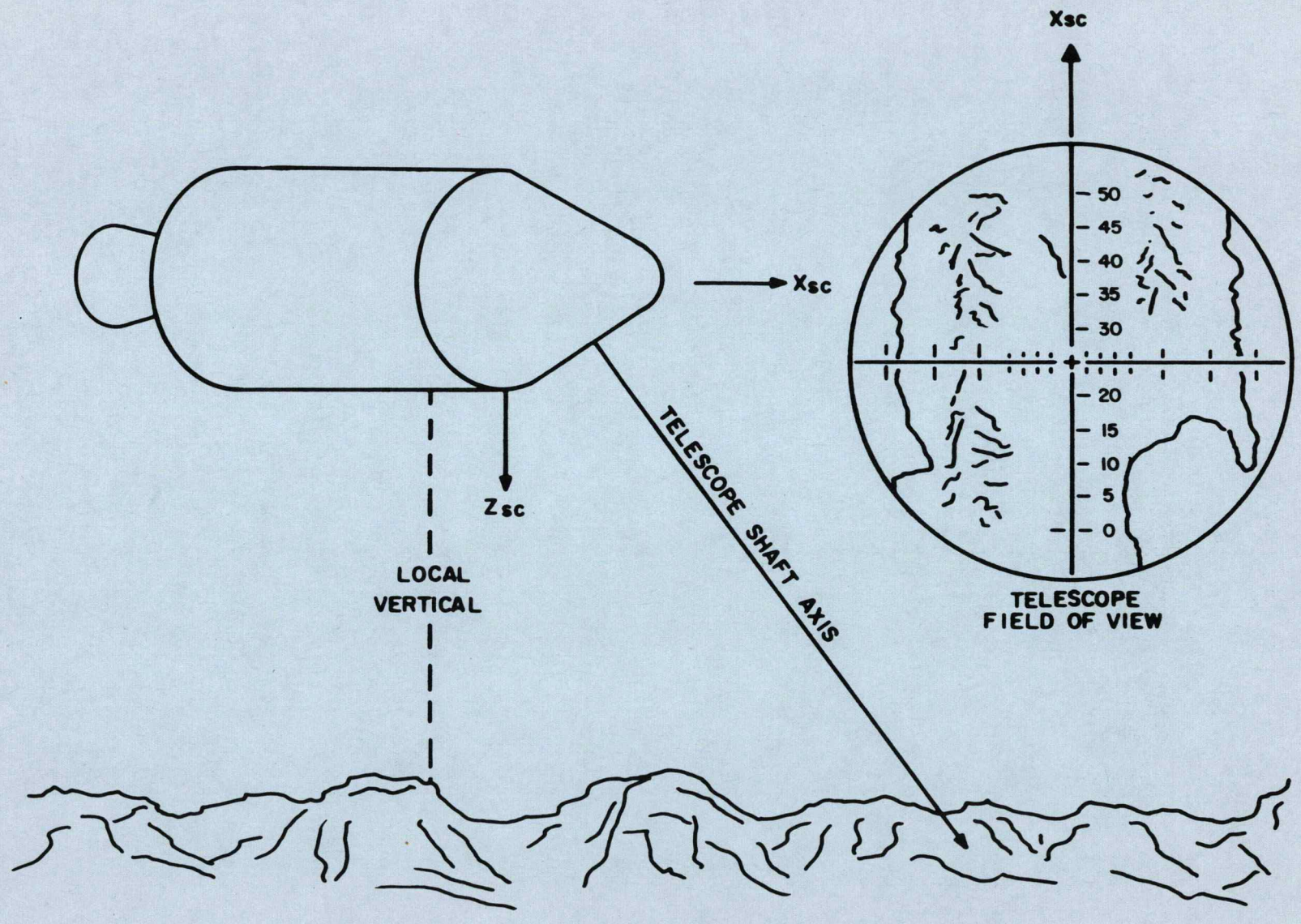


Figure 1-8. Orbital Navigation Sighting

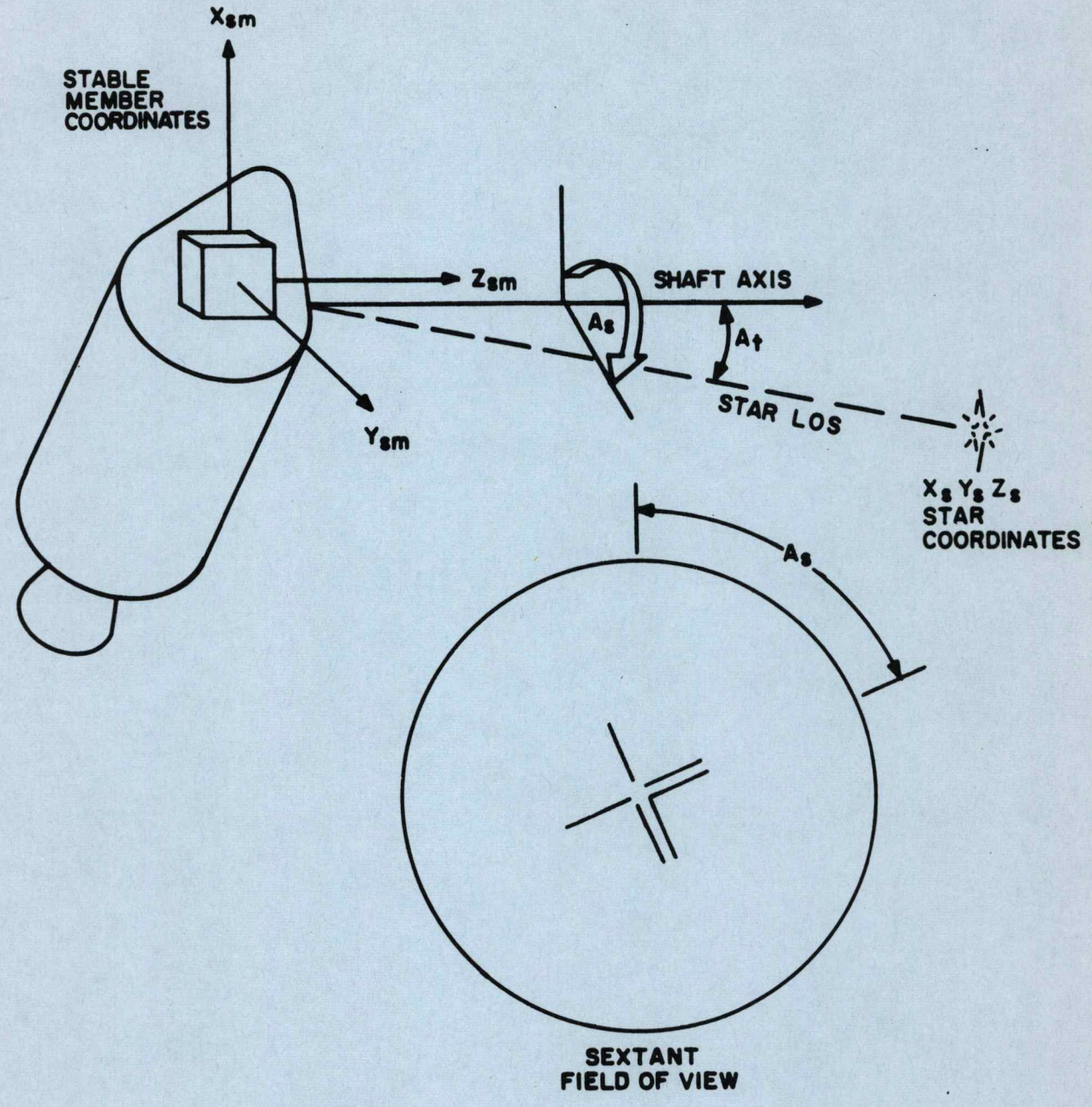


Figure 1-9. IMU Alignment Measurement

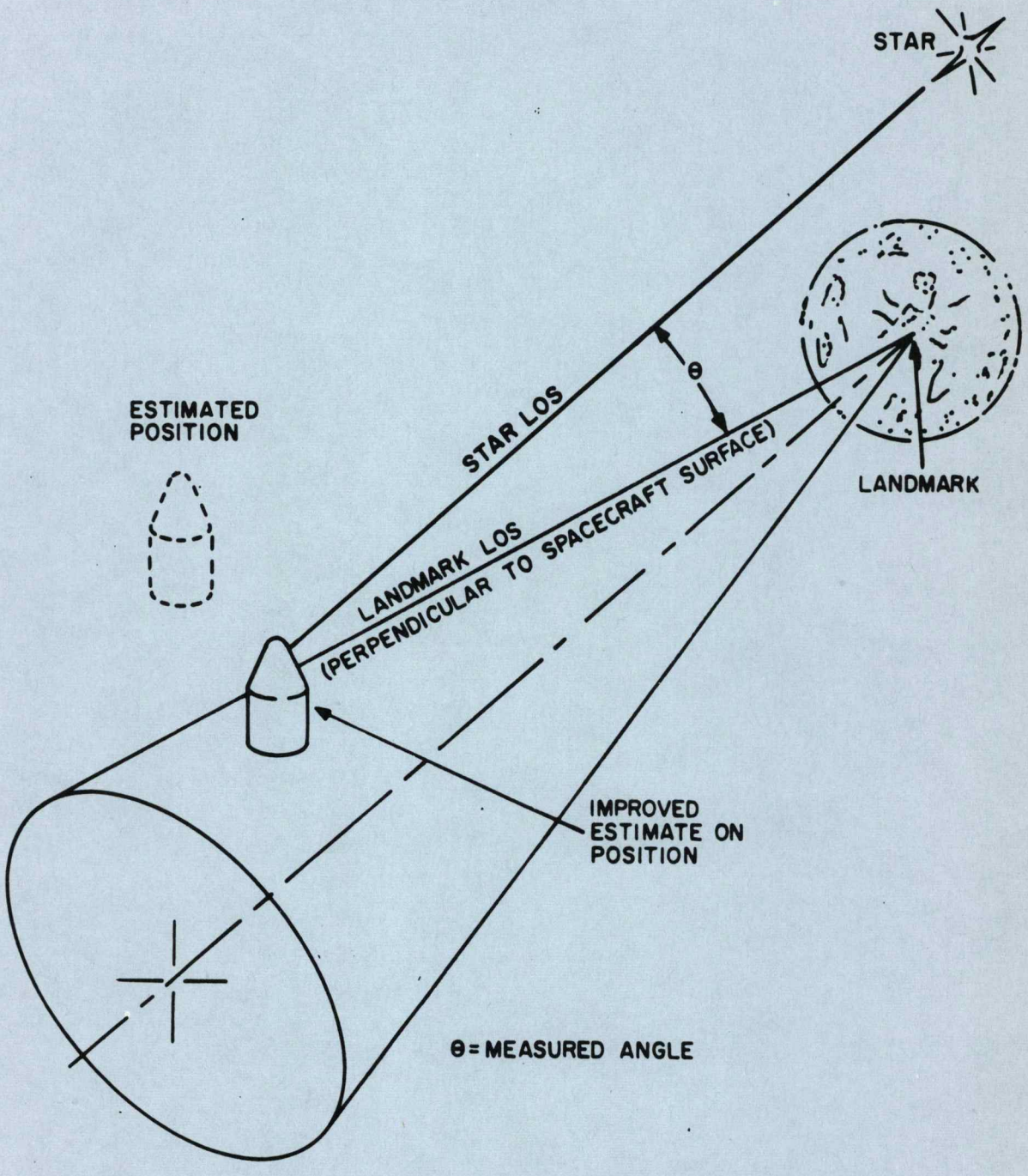


Figure 1-10. Midcourse Position Determination

to the present required trajectory. If a midcourse correction is necessary, the computer calculates the thrust vector and the velocity change needed, repositions the spacecraft, and controls the thrusting of the SPS.

During a major thrusting maneuver, the computer performs as explained in the paragraph above as well as performing SPS steering through the CDU.

1.4.8 ENTRY. This PGNCS function is performed during entry into the atmosphere. The PGNCS controls the flight path of the command module. The computer determines the proper trajectory and steers the command module along this trajectory. Steering is accomplished by rolling the command module about the command module stability axis. This changes the lift to drag ratio of the command module, and thereby varies the trajectory.

1.5 SUMMARY

The PGNCS performs three basic functions: optical navigation, inertial guidance, and control. Optical navigation is accomplished by using a scanning telescope and a sextant. The scanning telescope is used to acquire the celestial object and the sextant is used to accurately measure the angles to these objects. The angles are inserted into a computer which performs the calculations necessary for space navigation.

Inertial guidance is accomplished by the use of an inertially stablized platform. Three stabilization gyros mounted on a three degree of freedom platform to provide inertial stabilization. Three accelerometers, also mounted on the platform, and their associated electronics provide the computer with incremental changes in velocity. These changes in velocity are accumulated in the computer. The computer, using these velocity changes, time and certain constants, then calculates the spacecraft position in space. The stable platform of the inertial measurement unit is also used for an inertial reference in space. From this reference, spacecraft attitude and velocity can be controlled through the control portion of PGNCS.

The PGNCS interfaces with the astronaut and six basic spacecraft systems: the Electrical Power System (EPS), the Environmental Control System (ECS), the Communications and Instrumentation System (C & IS), the Stabilization Control System (SCS), the Reaction Control System (RCS) and the Service Propulsion System (SPS). The PGNCS receives prime power from the EPS, cooling from the ECS and ground information from the C & IS. The PGNCS provides steering and thrusting commands to the SPS and RCS for attitude, thrust and steering control. The PGNCS also provides system information to the C & IS for transmission to the ground stations.

The astronaut:

a. Loads data into the computer.

b. Monitors the systems operation.

c. Can control the mode selection of the system.

d. Provides system backup.

e. Takes optical sightings.

The PGNCS includes the following major components.

a. Navigation Base (NB)

b. Inertial Measurement Unit (IMU)

c. Optical Unit

d. Coupling Data Unit (CDU)

e. Power and Servo Assembly (PSA)

f. Display and Keyboard

g. Command Module Computer (CMC)

h. PIPA Electronics Assembly (PEA)

i. Signal Conditioner

j. G&N Indicator Control Panel

The PGNCS equipment is divided into three subsystems: inertial subsystem (ISS), optical subsystem (OSS) and computer subsystem (CSS).

The PGNCS is required to perform various functions during a lunar orbit mission. These functions and their relationship with the Apollo mission phases for a lunar orbit mission are listed below:

a. Prelaunch IMU alignment - performed prior to final countdown.

b. Guidance monitor - performed during launch and translunar injection.

c. Orbital navigation - performed during earth and lunar orbit.

d. Inflight IMU alignment - performed during earth orbit, translunar coast, lunar orbit and transearth coast.

e. Midcourse navigation - performed during translunar and transearth coast.

f. Attitude control - provides attitude control of the spacecraft.

g. Thrust Maneuver - performed during translunar, lunar orbit injection, transearth injection, and transearth coast.

h. Entry - performed during earth entry.

SECTION II

INERTIAL SUBSYSTEM

INTRODUCTION

This section describes the components that comprise the inertial subsystem (ISS) to a functional block diagram level.

2.1 ISS EQUIPMENT

The ISS consists of the following equipment (figure 2-1):

a. Inertial Measurement Unit (IMU).

b. Navigation Base (NB).

c. Pulsed Integrating Pendulum (PIPA) Electronics Assembly (PEA).

d. Portions of the Power and Servo Assembly (PSA).

e. Portions of the Coupling Data Unit (CDU).

f. Signal Conditioner Assembly (SCA).

2.1.1 INERTIAL MEASUREMENT UNIT. The Inertial Measurement Unit (IMU) is a gimbaled, three-degree-of-freedom gyroscopically stabilized device whose primary functions are:

a. To maintain an inertially referenced coordinate system for spacecraft attitude control and measurement.

b. To maintain three accelerometers in this coordinate system for accurate measurement of spacecraft velocity changes.

The IMU (figure 2-2) consists of three gimbals, of which the inner gimbal is the stable member, as well as having gimbal mounted electronic packages, and six inter-gimbal assemblies which contain resolvers, slip ring assemblies and torque motors. These are contained within the gimbal case.

2.1.1.1 Stable Member. The stable member or inner gimbal is supported by the middle gimbal and is free to rotate 360 degrees about the inner gimbal axis. The stable member (figure 2-3) is machined from a solid block of cold-pressed and sintered beryllium. Holes are bored in the block for mounting three Apollo II IRIG Assemblies, (inertial reference integrating gyros) and three 16 PIP's (pulsed integrating pendulums). Attached to the stable member also are some of the gimbal mounted electronics (GME) modules. These modules are discussed subsequently and are as follows:

a. Three PIP preamplifiers.

b. Two stable member heater assemblies.

c. Temperature alarm, control, and blower control thermostats.

d. Temperature alarm, control, and blower control modules.

e. Ducosyn excitation transformer.

f. Two safety thermostats.

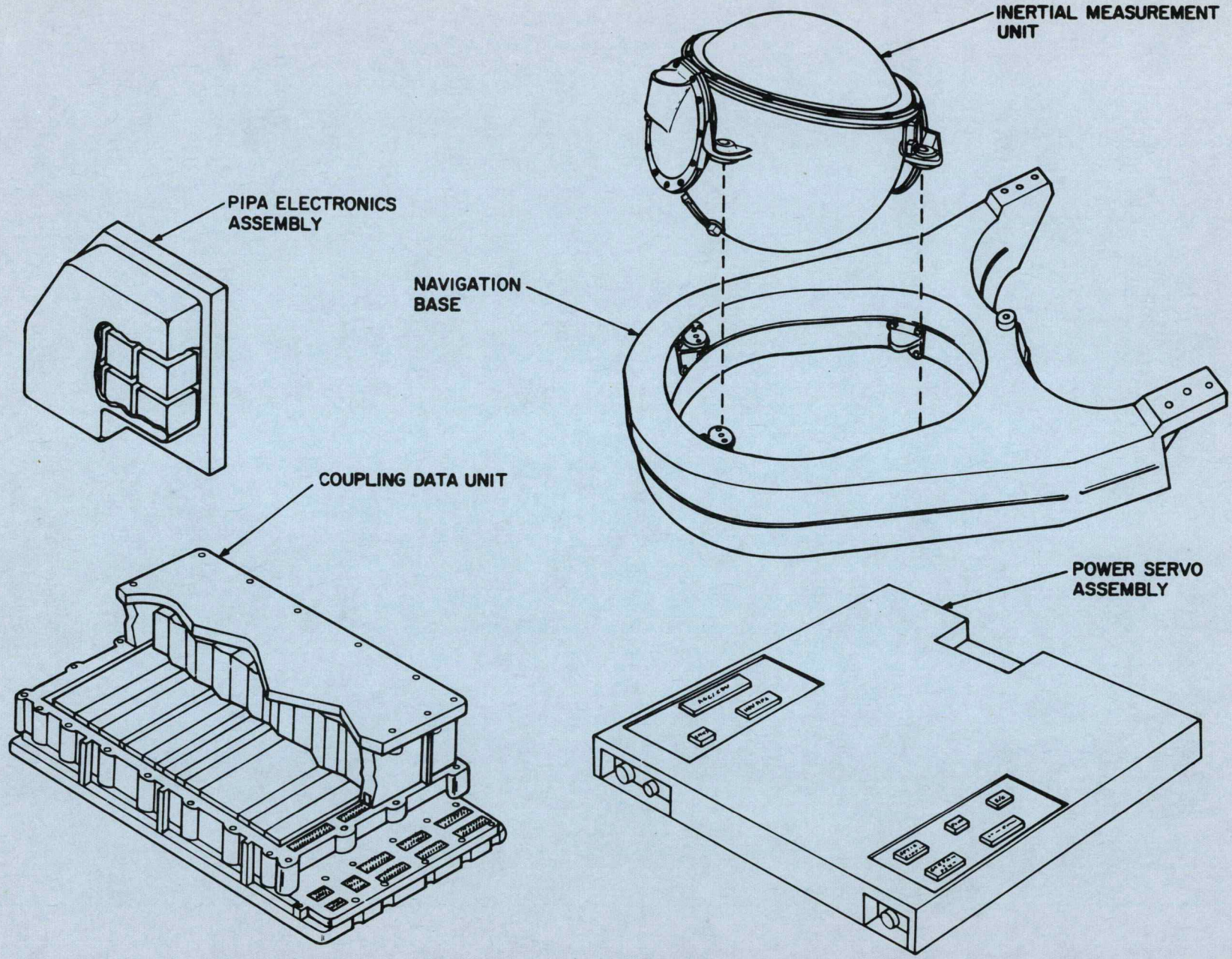


Figure 2-1. ISS Equipment

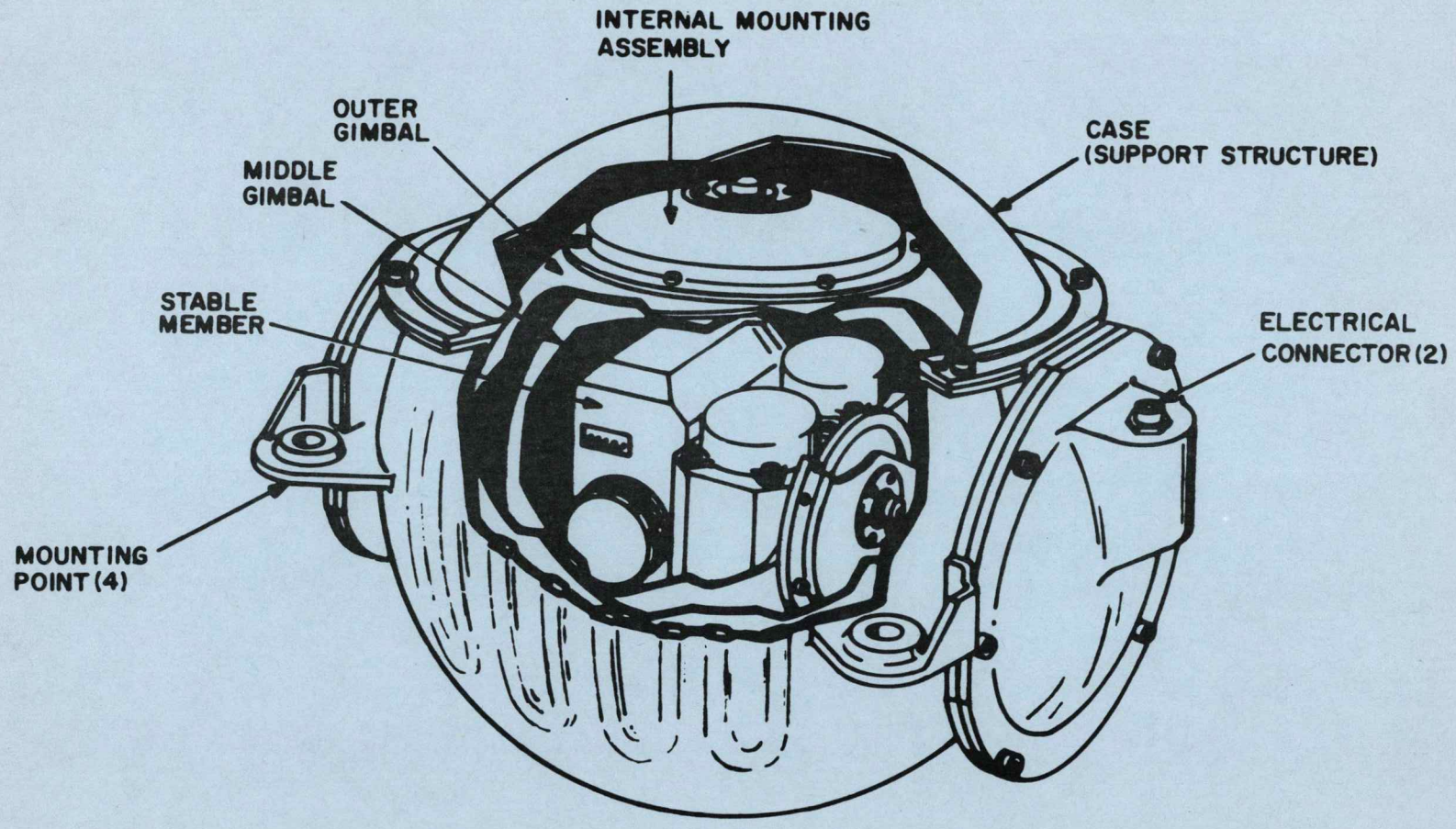


Figure 2-2. Block II Inertial Measurement Unit

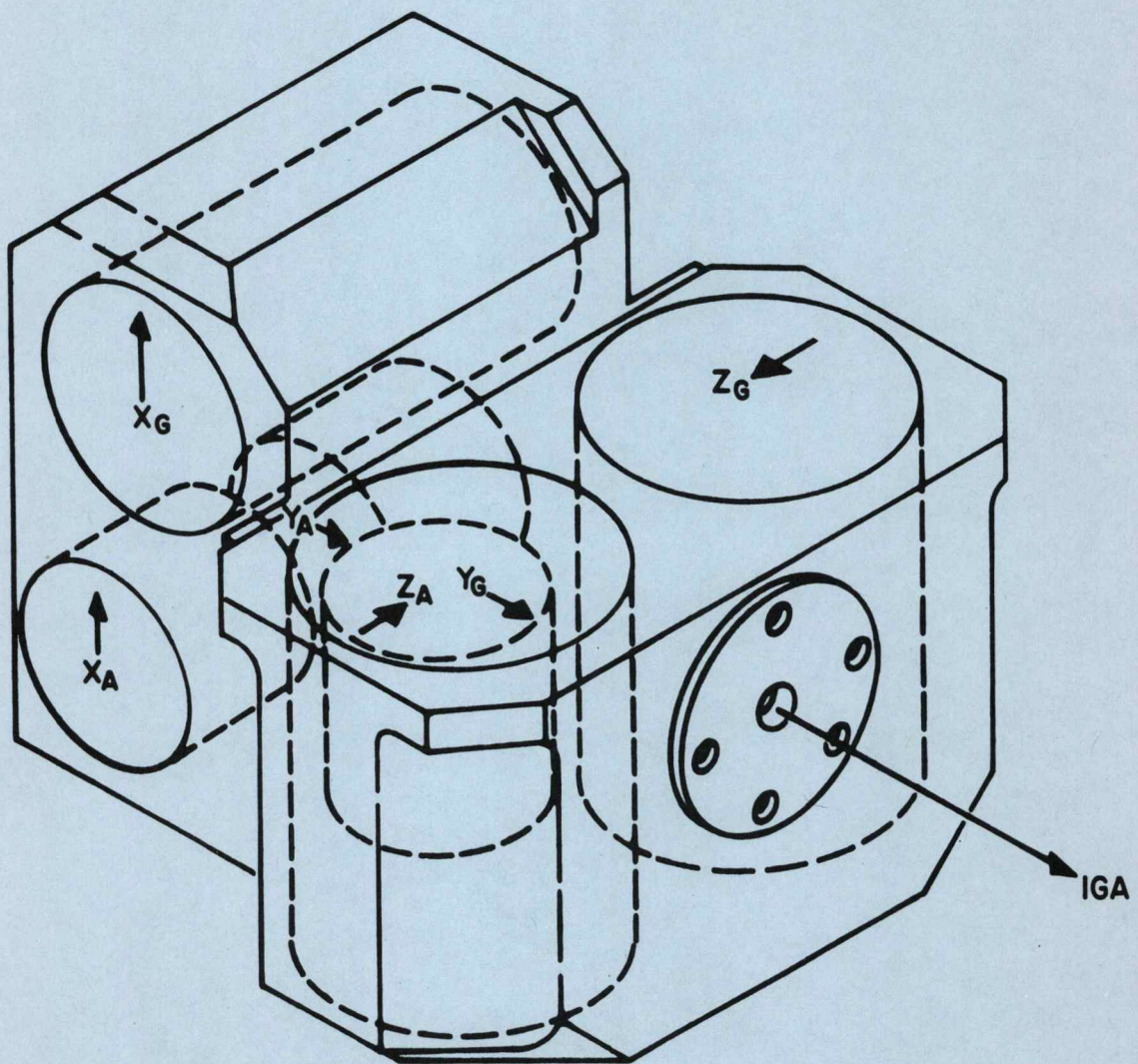


Figure 2-3. Stable Member

2.1.1.2 Inter-gimbal Assembly. An inter-gimbal assembly (figure 2-4) is attached to each end of the stable member and to the middle gimbal to connect these two units and to define the inner gimbal axis. A duplex pair cf low-preload ball bearings are used; one is fixed to, the other floated on a stub shaft within each inter-gimbal assembly. The inter-gimbal assemblies also house a torque motor and the resolvers used for angular data transmission. The stable member power inputs and signal inputs and outputs are routed through a 40-contact slip ring on each end of the inner gimbal axis. Angular data transmission is accomplished by a multispeed transmitter resolver (1X and 16X) mounted on the negative end of the inner gimbal axis (IGA). These resolvers supply 800-cps signals (proportional to the sine and cosine of the inner gimbal angle) to the coupling data unit (CDU). A gyro error resolver (1X) is also on the negative end of the inner gimbal axis and is used in the stabilization loop to transform gyro error into gimbal axis errors. A dc torque motor is mounted on the positive end of the inner gimbal axis. This torque motor which utilizes permanent magnet stators, is used in the stabilization loop to position the stable member.

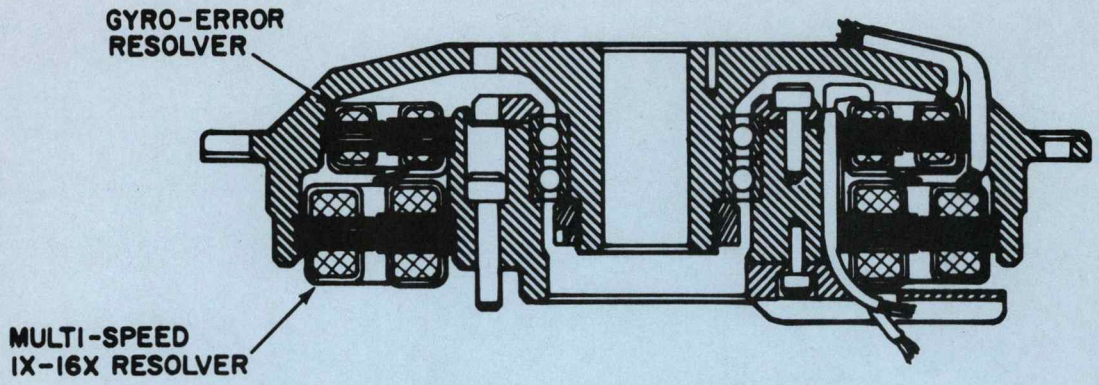
2.1.1.3 Middle Gimbal. The spherical middle gimbal is assembled from two hydroformed hemispherically shaped sections to allow for separation. The hemispheres are of aluminum alloy. The flanges used for assembly of the gimbal are dip brazed to the hemispheres. An inter-gimbal assembly is attached to each end of the middle gimbal and to the outer gimbal to connect the middle and outer gimbals and to define the middle gimbal axis. The inter-gimbal assembly provides 360 degrees of freedom. Each inter-gimbal assembly contains a duplex ball bearing pair (one fixed; one floated) and a 40-contact slip ring for routing electrical inputs and outputs. A multispeed transmitter resolver (1X and 16X) is mounted on the negative end of the middle gimbal axis for angular data transmission and a dc torque motor is mounted on the opposite end of the axis.

2.1.1.4 Outer Gimbal. The general configuration, fabrication and assembly of the outer gimbal is similar to the middle gimbal. An inter-gimbal assembly is attached to each end of the outer gimbal and to the support gimbal to connect the outer and support gimbals and to define the outer gimbal axis. The inter-gimbal assembly provides 360 degrees of freedom for the outer gimbal. Each inter-gimbal assembly contains a duplex ball bearing pair (one fixed; one floated) and a 50-contact slip ring for routing electrical inputs and outputs. A multispeed transmitter resolver (1X and 16X) is mounted on the negative end of the outer gimbal axis and a dc torque motor is mounted on the opposite end of the axis. Other components on the outer gimbal include two axial flow blowers, which circulate air over the middle and support gimbals.

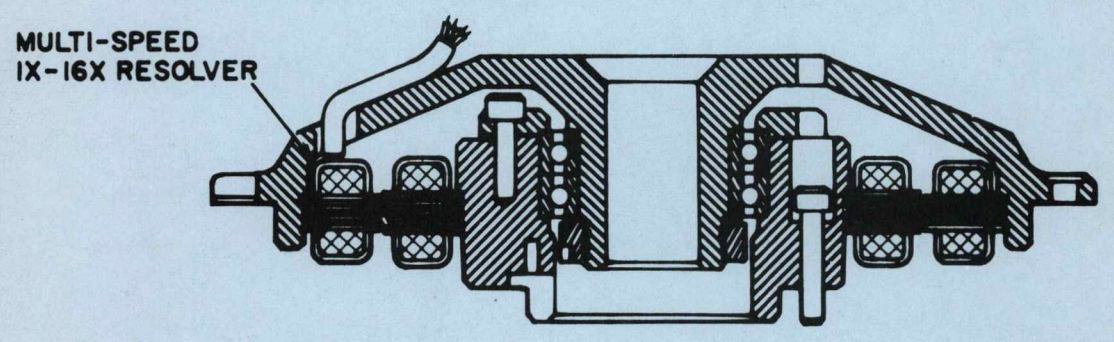
2.1.1.5 Gimbal Case. The gimbal case is spherical in shape and fabricated of aluminum alloy. The outside diameter of the case is approximately 12.5 inches. The gimbal case consists of two main sections which are brazed together. These sections are hydroformed and have integral coolant sections for passage of water-glycol from the environmental system. Mounting flanges are provided for attaching the IMU to the navigation base. Each end of the case contains the inter-gimbal assembly associated with the outer gimbal, and inter-gimbal assembly cover plate and electrical connector for the IMU. In addition, a precision resolver assembly module and blower control relay are also mounted on the gimbal case. The case is hermetically sealed when a top cover plate is installed. Insulation is used to cover the IMU in order to prevent condensation of moisture on the coolant passages.

Figure 2-5 is a representation of the IMU gimbals and their components as they are mounted within the gimbal case.

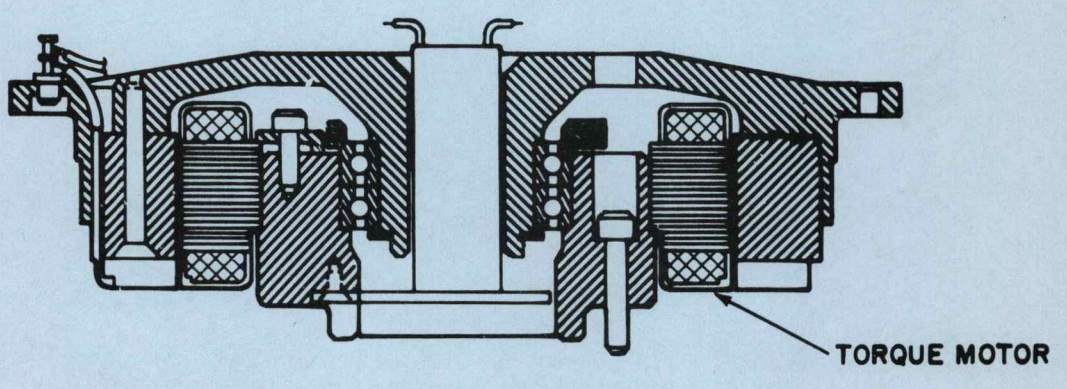
The complete IMU weighs approximately 42 pounds.



INNER GIMBAL AXIS ASSEMBLY SHOWING
MULTI-SPEED RESOLVER & GYRO ERROR RESOLVER



MIDDLE GIMBAL ASSEMBLY SHOWING
MULTI-SPEED RESOLVER



OUTER GIMBAL ASSEMBLY SHOWING
TORQUE MOTOR

Figure 2-4. Inter-gimbal Assembly

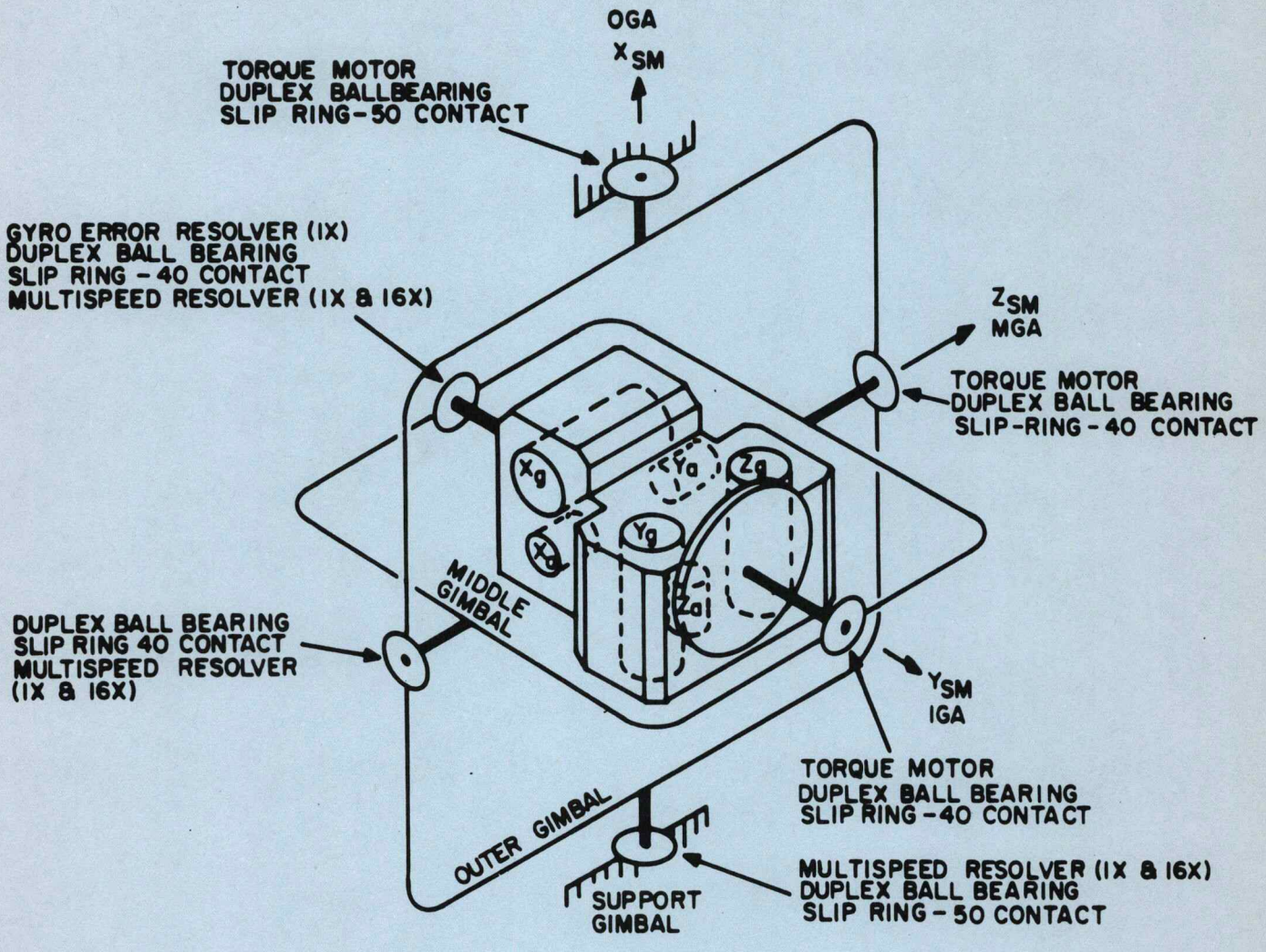


Figure 2-5. IMU Gimbal Assembly and Gimbal Axes

2.1.2 NAVIGATION BASE. The nav base (NB) provides a mounting surface for the IMU and the OUA. The outer shell is constructed by riveting and bonding anodized preformed sheet aluminum alloy panels together. The shell is filled with polyurethane foam. Precisely machined mounting surfaces insure that the plane formed by the IMU mounts is 32°32'23" from the plane formed by the OUA mounts. The nav base is positioned behind the indicator control panel with the OUA along the conical surface of the command module. Refer to figure 2-6. The nav base is constructed with a 20° offset and is approximately 27 inches long, 22 inches wide, and 4.5 inches high.

2.1.3 PIP ELECTRONICS ASSEMBLY. The PIP Electronics Assembly (PEA) contains 12 modular electronics assemblies all of which are functional components within the PIPA loops. The PEA measures approximately 9 inches high, 10 inches wide and 2.6 inches deep. Refer to figure 2-7. It is mounted close to the IMU to avoid line loss in critical current signals. The PEA contains three of each of the following modules.

a. DC differential amplifier and precision voltage reference - regulates torquing supplied through binary current switches.

b. Binary current switch - switches constant current pulses between windings of the PIP torque generators. It also supplies pulses to the CMC forward-backward counter to indicate incremental velocity changes.

c. AC differential amplifier and interrogator - amplifies signals from PIPA signal generator and converts them to plus and minus torque pulses.

d. C/M PIPA calibration - compensates for differences in inductive loading of PIP torque generator windings and regulates balance of plus and minus torques.

2.1.4 POWER AND SERVO ASSEMBLY. The power and servo assembly (PSA) contains encapsulated electronic circuitry for the inertial and optical subsystems. It is approximately 2.75 inches high, 23.1 inches wide, and 22.6 inches deep. Figure 2-8 is a picture of the Block II PSA and figure 2-9 is a layout of the PSA modules. The PSA contains 37 modules mounted on a common frame which inturn is mounted on a coldplate. Table 2-1 identifies each of the PSA modules by name and by function.

2.1.5 COUPLING DATA UNIT. The coupling data unit (CDU) is explained in detail in Section III.

2.1.6 SIGNAL CONDITIONER ASSEMBLY. The signal conditioner assembly (SCA) is explained in detail in Section VIII.

2.2 ISS FUNCTIONS AND INTERFACE

The ISS maintains a platform fixed with respect to a pre-selected inertial reference frame, senses acceleration along the coordinate system defined by the platform orientation, provides the computer with incremental velocity data, and the orientation of the platform with respect to the spacecraft.

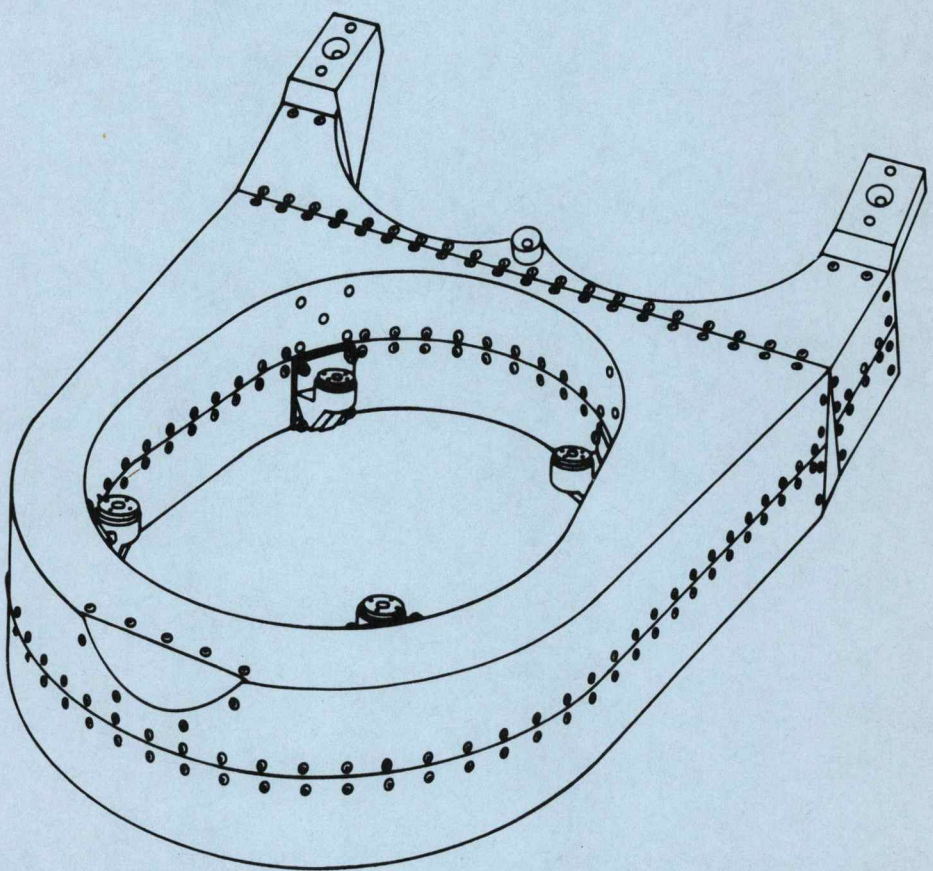


Figure 2-6. Navigation Base

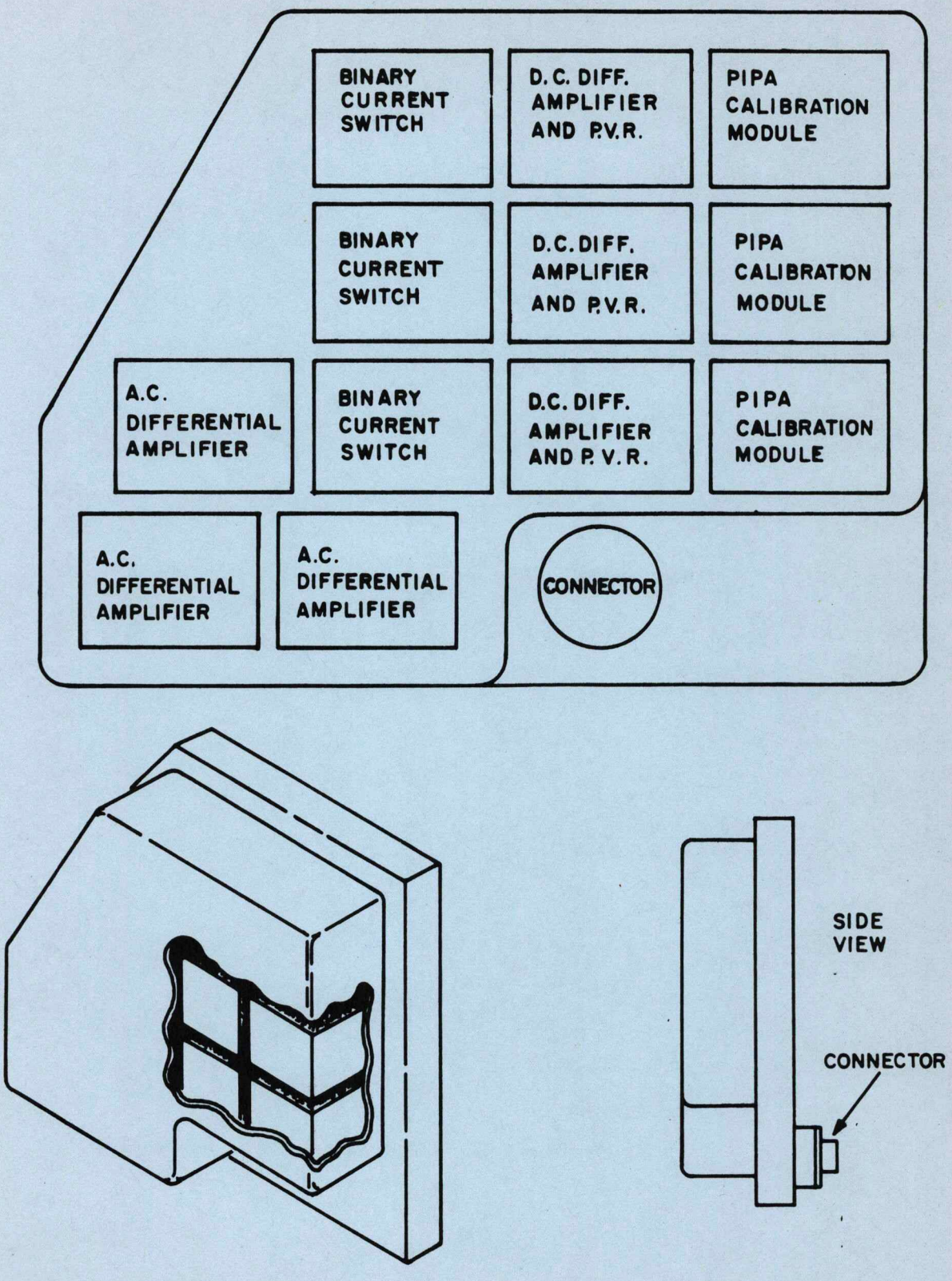


Figure 2-7. PIP Electronics Assembly

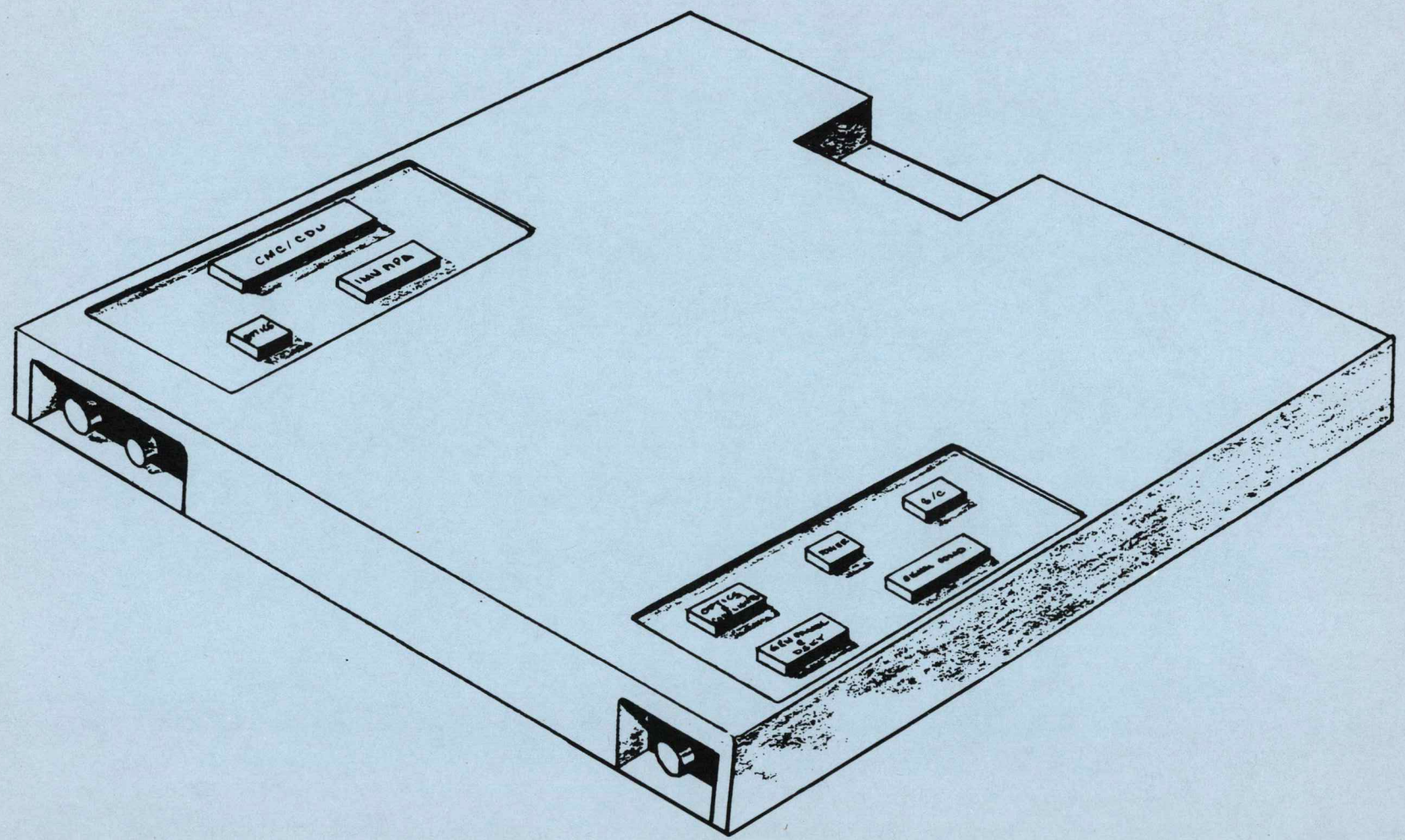


Figure 2-8. Block II Power and Servo Assembly

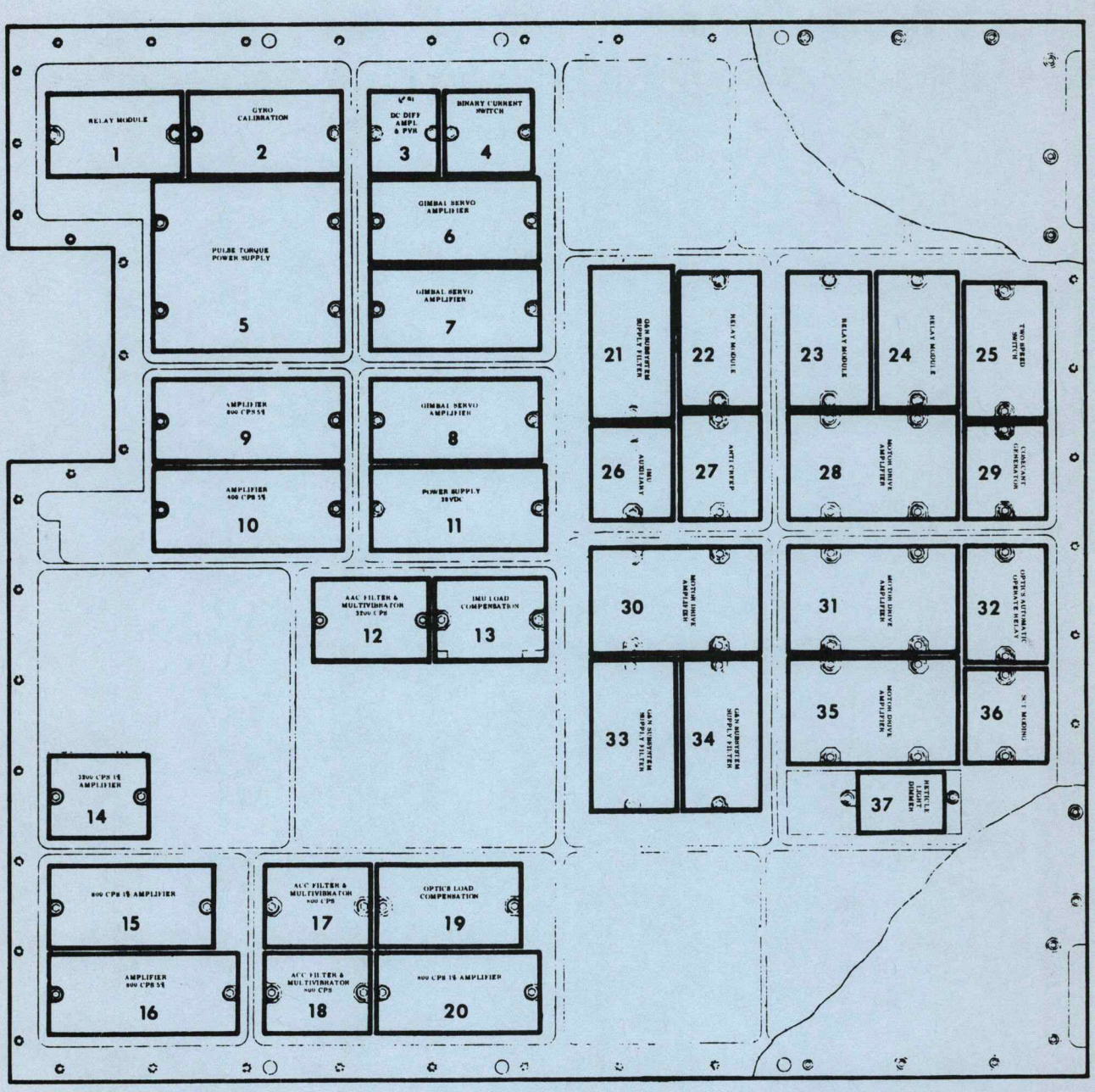


Figure 2-9. Block II Power and Servo Assembly Modules

Table 2-1. PSA Modules

Figure 2-9 Callout Number	Module Name	Module Function
1	Relay Module	Provides relay switching for IMU control.
2	Gyro Calibration Module	Applies plus or minus torque pulses to IRIG's as directed by CMC.
3	DC Differential Amplifier and PVR Module	Supplies precision reference voltage for IRIG pulse torquing current control.
4	Binary Current Switch Module	Switches current pulses to one of the IRIG torque generators to control gimbal position.
5	Pulse Torque Power Supply Module	Supplies +120 vdc to PIPA loops and to fine align electronics. Also supplies +28 vdc, + 20 vdc, and -20 vdc to PIPA loops.
6, 7, and 8	Gimbal Servo Amplifier Modules (X, Y and Z)	Amplifies outer (X), middle (Z), and inner (Y) gimbal error and supplies correction signals to the gimbal torque motors.
9	800 cps 5% Amplifier Module	Supplies 28 volts 800 cps for IMU blowers and PIP heaters. Also supplies 28 volts 800 cps ϕB IRIG wheel power.
10	800 cps 5% Amplifier Module	Supplies 28 volts 800 cps for IMU blowers and PIP heaters and 28 volts 800 cps ϕA IRIG wheel power.
11	-28 vdc Power Supply Module	Supplies power to the three gimbal servo amplifiers in the stabilization loop and the pulse torque power supply to generate -20 vdc for the accelerometer loop.
12	3,200 cps AAC Filter and Multivibrator Module	Regulates operation of the 3200 cps 1% amplifier.
13	IMU Load Compensation Module	Provides power factor correction for the 800 cps 1% and 5% power supplies.
14	3200 cps 1% Amplifier Module	Supplies 3200 cps ducosyn excitation and magnetic suspension voltage. Also used as a reference for gimbal servo amplifier demodulator in all modes of operation except the coarse align mode.
15	800 cps 1% Amplifier Module	Provides IMU resolver excitation and a reference to the FDAI and the 800 cps 5% amplifier.
16	800 cps 5% Amplifier Module	Supplies excitation for trunnion and shaft drive motors in the SXT and SCT.

Table 2-1. PSA Modules

Figure 2-9 Callout Number	Module Name	Module Function
17	800 cps AAC Filer and Multivibrator Module	Supplies and regulates 800 cps voltage to the ISS 1% power amplifier.
18	800 cps AAC Filter and Multivibrator Module	Supplies and regulates 800 cps voltage to the OSS 1% power amplifier.
19	Optics Load Compensation Module	Provides power factor correction for 800 cps 1% and 5% power supplies.
20	800 cps 1% Amplifier Module	Provides resolver and tachometer excitation and a reference for the 800 cps 5% amplifier in the OSS.
21	G&N Subsystem Supply Filter	Filters the 0, 27.5, and 28 vdc power supplies for ISS standby power.
22 23 24	Relay Modules (3)	Provides OSS relay switching control.
25	Two Speed Switch Module	Provides signal selection for switching null seeking servo loops from coarse to fine resolver error detection in the OSS.
26	IMU Auxiliary Module	Indicates out of tolerance conditions on 28 vrms, 3200 cps, 28 vrms, 800 cps, the resolved IRIG preamplifier outputs and IMU temperature. Also provides the IMU turn-on moding discrete.
27	Anti-creep Electronics Module	Removes B+ from OSS motor drive amplifiers when the optics hand controller output drops below certain limits and thus prevents the optics from drifting.
28	Motor Drive Amplifier Module	Drives the SXT shaft motor.
29	Cosecant Generator Module	Maintains constant optics shaft image drive rate regardless of the trunnion angle in the manual resolved OSS mode.
30	Motor Drive Amplifier Module	Drives the SCT shaft motor.
31	Motor Drive Amplifier Module	Drives the SXT trunnion motor.
32	Optics Automatic Operate Relay Module	Provides relays for computer control of optics.

Table 2-1. PSA Modules

Figure 2-9 Callout Number	Module Name	Module Function
33	G&N Subsystem Supply Filter Module	Filters 0, 27.5, and 28 vdc power for ISS operate power.
34	G&N Subsystem Supply Filter Module	Filters 0, 27.5 and 28 vdc power for OSS operate power.
35	Motor Drive Amplifier Module	Drives SCT trunnion motor.
36	SCT Moding Module	Provides SCT trunnion control.
37	Reticle Light Dimmer Module	Provides circuitry for controlling the brightness of the SXT and SCT reticle lamps.

The ISS platform (stable member) alignment must be re-established during flight since the stable member may deviate from its alignment due to gyro drift and during the cycling of the ISS from operate to standby. Two star sightings are required for coarse alignment of the stable member and two sightings are required for fine alignment. The stable member is aligned after the computer manipulates angular data received from the optical subsystem (OSS), combines that with the known spacecraft and IMU angles, and supplies alignment signals to the IMU.

The ISS measures acceleration along the axes of the stable member coordinate system and supplies the incremental velocity data to the computer. The computer calculates the spacecraft's present position and velocity by adding the components of velocity due to gravitational field accelerations with velocity due to thrust (from ISS) and the last known position and velocity. The position data is also used during spacecraft velocity corrections to determine when the proper spacecraft trajectory is obtained and when thrusting can be stopped.

The ISS also generates signals which are used to control spacecraft attitude. Gimbal mounted resolvers measure the alignment of the stable member axes with respect to the spacecraft axes. This angular displacement is fed to the computer and displayed to the astronaut. The astronaut or the computer can command changes to the angular displacement by controlling the firing of the reaction control system or the service propulsion system.

For the purpose of explanation, the inertial subsystem equipment is divided into the functional blocks shown in figure 2-10. The operation and interrelationship of these blocks is described in the following paragraphs.

2.2.1 NAVIGATION BASE (NB). The NB provides a rigid support for the IMU and the optical unit assembly (OUA). The IMU and OUA are precisely aligned on the NB. The NB also provides a shockmount for the IMU and OUA to the spacecraft.

2.2.2 INERTIAL MEASUREMENT UNIT (IMU). The IMU is a three degree-of-freedom gimbal system and uses integrating gyros to detect deviations of the stable member (inner gimbal) with respect to an inertial reference.

The orientation of the stable member, with respect to the spacecraft, is measured by resolvers on the gimbal shafts. The resolver gimbal angle output signals are supplied to the CDU. The resolver signals are also used as a total attitude input to the Flight Directors Attitude Indicator (FDAI) for display to the astronauts.

The IMU uses three Apollo II inertial reference integrating gyros (IRIG's) to sense changes in the orientation of the stable member, and three 16 pulse integrating pendulums (PIP's) to sense changes in velocity.

The IMU gimbals consist of a supporting gimbal or case, an outer gimbal mounted to the case, a middle gimbal mounted to the outer gimbal, and an inner gimbal or stable member mounted to the middle gimbal. Gimbal movement is not limited by stops.

The inner gimbal (stable member) is machined from a solid block of cold-pressed and and sintered beryllium with holes bored in the block for mounting the IRIG's and PIP's. Small electronic assemblies are mounted on the gimbal surface.

The spherical middle and outer gimbals are assembled from two hydroformed, hemispherically shaped, aluminum alloy sections. Two blowers are mounted on the outer gimbal to provide heat transfer from the middle gimbal shell to the coldplate on the IMU support gimbal.

The support gimbal or case is spherical and also fabricated from an aluminum alloy. The case provides a hermetically sealed environment containing air at atmospheric pressure. The case contains a coolant passage formed by roll bonding two sheets of aluminum together except where the passage is located. After the case is formed the unbonded portion is inflated. This method forms a leak free coolant passage.

2.2.3 TEMPERATURE CONTROL SYSTEM. The temperature control system is a thermostatic system that maintains the IRIG and PIP temperatures within their required limits during both IMU standby and operate modes. Heat is applied by end-mount heaters on the inertial components, stable member heaters, and a temperature control anticipatory heater. Heat is removed by convection, conduction, and radiation. The natural convection used during IMU standby modes is changed to blower controlled, forced convection during IMU operating modes. IMU internal pressure is normally between 3.5 and 15 psia enabling the required forced convection. To aid in removing heat, a water-glycol solution passes through coolant passages in the IMU support gimbal. Therefore, heat flow is from the stable member to the case and coolant. The temperature control system consists of the temperature control circuit, the blower control circuit, and the temperature alarm circuit. A separate external temperature control system is also provided for test configurations but will not be discussed in this manual.

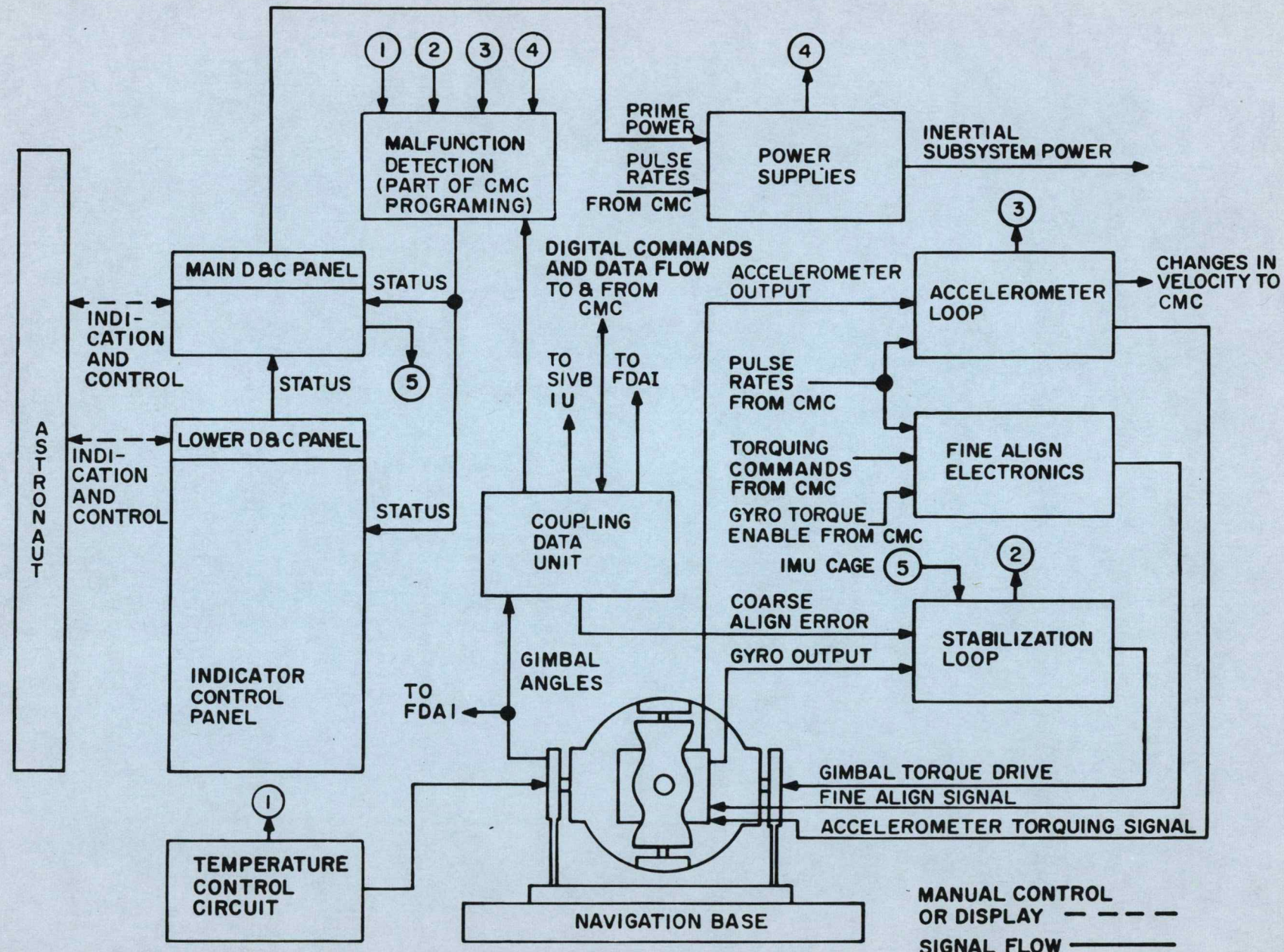


Figure 2-10. Inertial Subsystem Interface

2.2.4 STABILIZATION LOOP. The stabilization loop holds the stable member space referenced to a given coordinate system by isolating the stable member from roll, pitch and yaw motions of the spacecraft. The stable member serves two purposes in the system: (1) acts as a reference for measuring the attitude of the spacecraft and (2) holds the three accelerometers (used in space for measuring acceleration due to thrust) in a fixed coordinate system.

When the stabilization loop holds the stable member inertially referenced, the 25 IRIG's on the stable member generate error signals to indicate any change in the orientation of the stable member with respect to inertial space. The error signals are amplified by the servo amplifiers in the PSA and are supplied to the IMU gimbal torque motors, which reposition the stable member.

When the stabilization loop is energized, the stable member is referenced to the spacecraft by the coarse align loops. The stable member must then be aligned to the desired orientation. The alignment is done in two steps, coarse align and fine align. The coarse align is done first and is accomplished by injecting coarse align signals into the stabilization loop servo amplifiers. The fine align is accomplished by injecting a fine align signal from the CMC into the torque ducosyn of each of the 25 IRIG's. During prelaunch, the stable member is held earth-referenced by supplying the 25 IRIG's with the appropriate torquing signals.

2.2.5 FINE ALIGN ELECTRONICS. The fine align electronics is used for fine alignment of the stable member. The electronics contain a current switch which is turned off and on by commands and timing pulses from the CMC. Using data obtained from optical sightings, the CMC determines the number of command pulses required. The outputs of the current switches are in constant amplitude DC currents and are supplied to the torque ducosyns of the 25 IRIG's.

2.2.6 ACCELEROMETER LOOPS. The accelerometer loops sense change in acceleration due to thrust or drag forces applied to the spacecraft and provide incremental velocity change information to the CMC. The loops consist of three 16 PIP's with mutually perpendicular input axes on the stable member and associated electronics in the PEA and PSA. As acceleration is applied along the input axes of the 16 PIP's, signals are generated and used by the accelerometer loop electronics to generate digital feedback signals which act to restrain the 16 PIP pendulums. Incremental velocity, in the form of pulses, is supplied to the CMC and used in calculating velocity and position data. Timing pulses are supplied from the CMC to the accelerometer loop electronics and are used in the development of torquing signals for the accelerometer.

2.2.7 COUPLING DATA UNIT. The CDU, an all electronic device, is used as an interface element between the ISS and CSS, the OSS and CSS, and the CSS and various controls and displays. It functions primarily as an analog to digital (A/D) or digital to analog (D/A) converter. There are five, almost identical, loops; one each for the inner, middle and outer IMU gimbals and one each for the shaft and trunnion optical axes. The ISS portion of the CDU performs the following functions:

a. Converts IMU gimbal angles from analog to digital form and supplies the CMC with this information.

b. Converts digital signals from the CMC to either 800 cps or direct current signals.

c. Controls the moding of the ISS through logical manipulation of computer discretes.

2.2.8 POWER SUPPLIES. The power supplies operate on 28vdc prime power and are synchronized by pulses from the CMC. Local oscillators in the power supplies allow them to operate independent of the CMC. The outputs of the power supplies are monitored by malfunction detection circuits.

2.2.9 MALFUNCTION DETECTION CIRCUITS. The malfunction detection circuits monitor the power supplies, temperature control circuits, stabilization loop electronics, accelerometer loop electronics and CDU electronics. When a malfunction occurs, the malfunction detection circuits produce a failure signal which is sent to the computer which sends them to the condition indicators on the master caution panel of the main display and control, and to the condition annunciator lamps on the indicator control panel.

2.3 AXES

The stabilization loop operation and the spacecraft error mechanization is based on several sets of axes and angles used to define and mechanize the inertial subsystem. These axes and angle sets are as follows:

a. Spacecraft axes.

b. Stable member axes.

c. IRIG axes.

d. PIP axes.

e. Middle gimbal axes.

f. Outer gimbal axes.

g. Gimbal case axes.

h. Inner, middle, and outer gimbal angles.

Each set of axes is a right hand, orthogonal coordinate system with positive rotation defined by the right hand rule. Figure 2-11 shows the relationship of the IMU to the spacecraft, and figures 2-12 through 2-20 define the sets of axes and the angles.

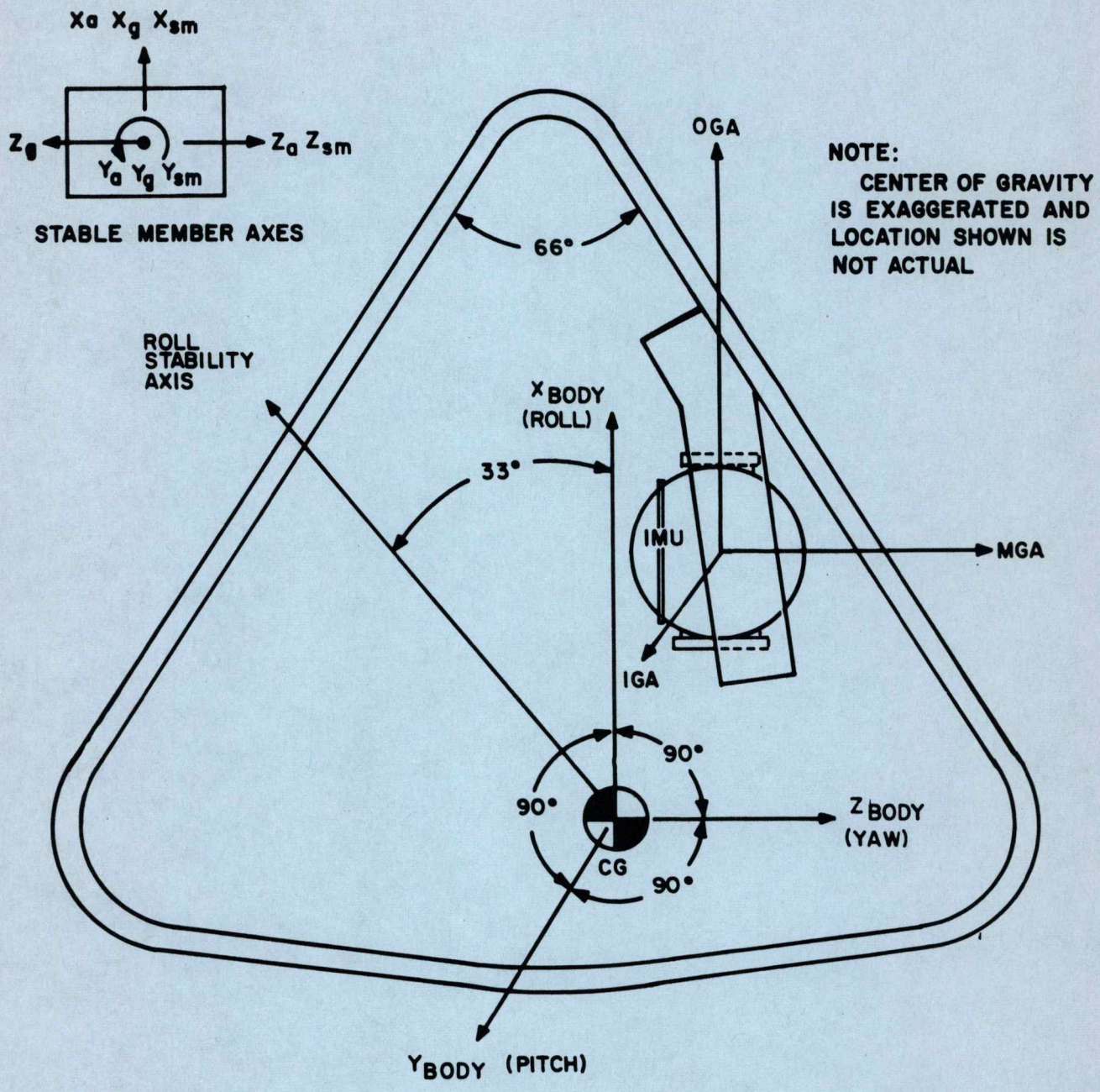
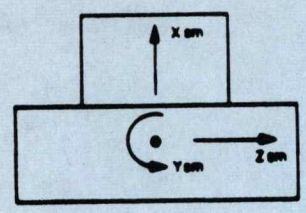
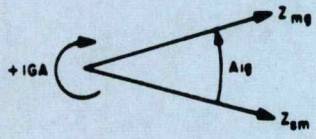


Figure 2-11. Spacecraft and Guidance System Axes



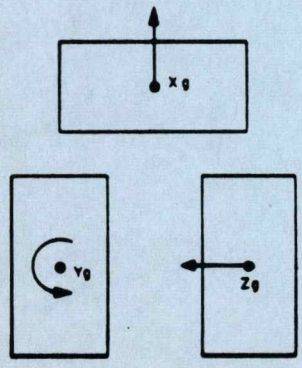
The stable member axes are aligned in a right-hand orthogonal coordinate system. They are used as a reference to align the inertial components and to define the inertial axes during flight.

Figure 2-12. Stable Member Axes



The positive inner gimbal angle is defined as the angle from the stable member Z axis to the middle gimbal Z axis as measured counterclockwise from the stable member. (As viewed from the positive Y inner gimbal axis.)

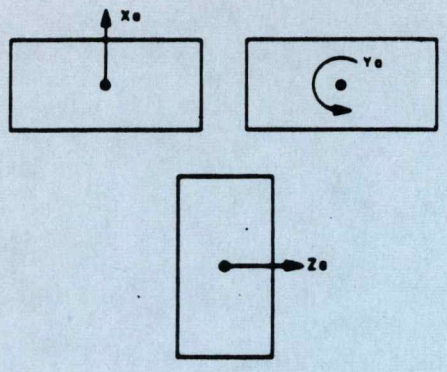
Figure 2-13. Inner Gimbal Angle



The Apollo II IRIG input axes define the positive input axis of the gyros and are fixed parallel with respect to the stable member axes.

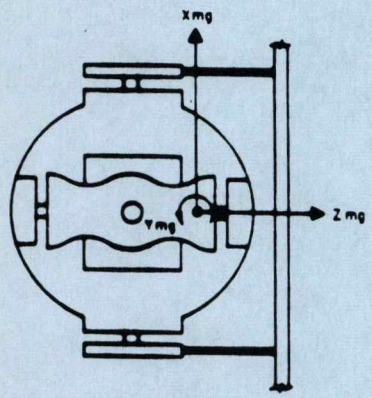
Note that the Z gyro input axis points toward the minus Z_{SM} axis.

Figure 2-14. Apollo II IRIG Input Axes



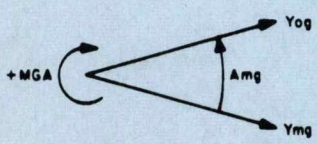
The 16 PIP axes define the positive input axis of the accelerometer and are fixed parallel with respect to the stable member axes.

Figure 2-15. 16 PIP Input Axes



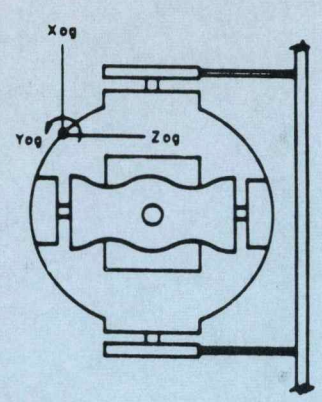
The middle gimbal axes are aligned in a right-hand orthogonal coordinate system. The axes are fixed to the movable middle gimbal. If the inner gimbal angle is set to zero, the axes are then parallel with the stable member axes.

Figure 2-16. Middle Gimbal Axes



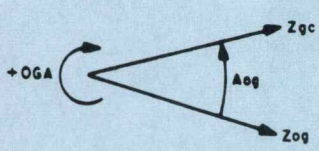
The positive middle gimbal angle is defined as the angle measured counterclockwise from the Y middle gimbal axis to the Y outer gimbal axis. (As seen from the positive Z middle gimbal axis.)

Figure 2-17. Middle Gimbal Angle



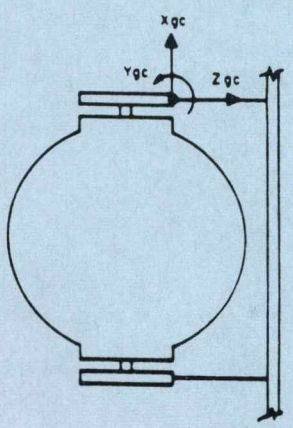
The outer gimbal axes are aligned in a right-hand orthogonal coordinate system. The axes are fixed to the movable outer gimbal. If the inner and middle gimbal angles are set to zero, the axes are then parallel with the stable member axes.

Figure 2-18. Outer Gimbal Axes



The positive outer gimbal angle is defined as the angle measured counterclockwise from the Z outer gimbal axis to the Z gimbal case axis. (As seen from the positive X outer gimbal axis.)

Figure 2-19. Outer Gimbal Angle



The gimbal case axes are orthogonal and fixed to the spacecraft. These axes are utilized as a reference frame when mounting the IMU to the navigation base. When all gimbal angles are set to zero, the axes are parallel with the stable member axes.

Figure 2-20. Gimbal Case Axes

2.4 STABILIZATION LOOP

The purpose of three stabilization loops is to maintain the stable member rotationally fixed with respect to inertial space. This stable, non-rotating platform is used as the reference to maintain the orientation of the accelerometers with respect to the inertial frame of reference and is also used as an attitude reference for the spacecraft.

2.4.1 STABILIZATION LOOP OPERATION. The stabilization loop has three Apollo II IRIG's which sense any rotational changes in the orientation of the stable member. The input axes of the IRIG's are orientated as described in figure 2-14. The gyro error signals are generated whenever the stable member is rotated with respect to inertial space. The error signals are amplified, resolved if necessary, and supplied to the appropriate gimbal torque motor which drives the stable member back to its original position to reduce the gyro error signal to zero. The path of the error signal originating at the gyros and terminating at the torque motors is shown in figure 2-21.

The IRIG output is a 3,200 cps error signal which is proportional to the rotation of the gyro about its input axis. The output of each gyro is amplified by a preamplifier which is an integral part of the IRIG assembly. The amplification is required to achieve a high signal-to-noise ratio through the gimbal slip rings. The Y gyro error signal, E (Yg), then passes directly to the phase sensitive demodulator (DEMOD) located in the gimbal servo amplifier while the X gyro error signal, E(Xg), and the Z gyro error signal, E(Zg), are resolved about the inner gimbal angle by the gyro error resolver. Resolution is required because motion of the spacecraft about the stable member will displace the X and Z gyro input axes away from the outer and middle gimbal axes. Figure 2-22 shows the configuration of the gyro and gimbal axes and the mechanization of the resolver which transforms the gyro errors to gimbal errors. A similar problem of resolution exists with respect to the middle gimbal angle and misalignment of the outer gimbal axis with respect to the X gyro input axis. This misalignment is not mechanized by a resolver because the middle gimbal angle is kept small. The three phase sensitive demodulators convert the 3,200 cps gyro error signals to positive dc or negative dc signals with the polarity being determined by the input phase. The gyro error signals are applied to the servo amplifiers. Due to the poor high frequency response of the IRIG's a method of stabilizing the loop by extending the bandwidth of the loop is required. This is obtained by the addition of compensation networks to the gimbal servo amplifier. The outputs of of the gimbal servo amplifiers drive the gimbal torque motors located on each gimbal axis. The torque motors drive the gimbals to complete the stabilization servo loop.

The initial orientation of the stable member can be changed in either the coarse or fine alignment mode. Signals to reposition the gimbals are injected into the gimbal servo amplifiers during the coarse alignment mode and into the gyros during fine alignment mode. These modes of operation are described in Section IV.

2.4.2 STABILIZATION LOOP MECHANIZATION. The purpose of the stabilization loop is to maintain the stable member aligned with respect to an inertial frame of reference defined by its inertial components, the three IRIG gyros. Any drift of the platform is sensed by these IRIG's and is manifested by a precessional movement of the float of the affected unit. This float displacement results in an output from the IRIG signal microsyn which is then preamplified and sent to the gimbal servo amplifier. The servo amplifier current output is fed to the appropriate torque motors to restore the stable member to its original reference position. As the stable member is returned to its original reference,

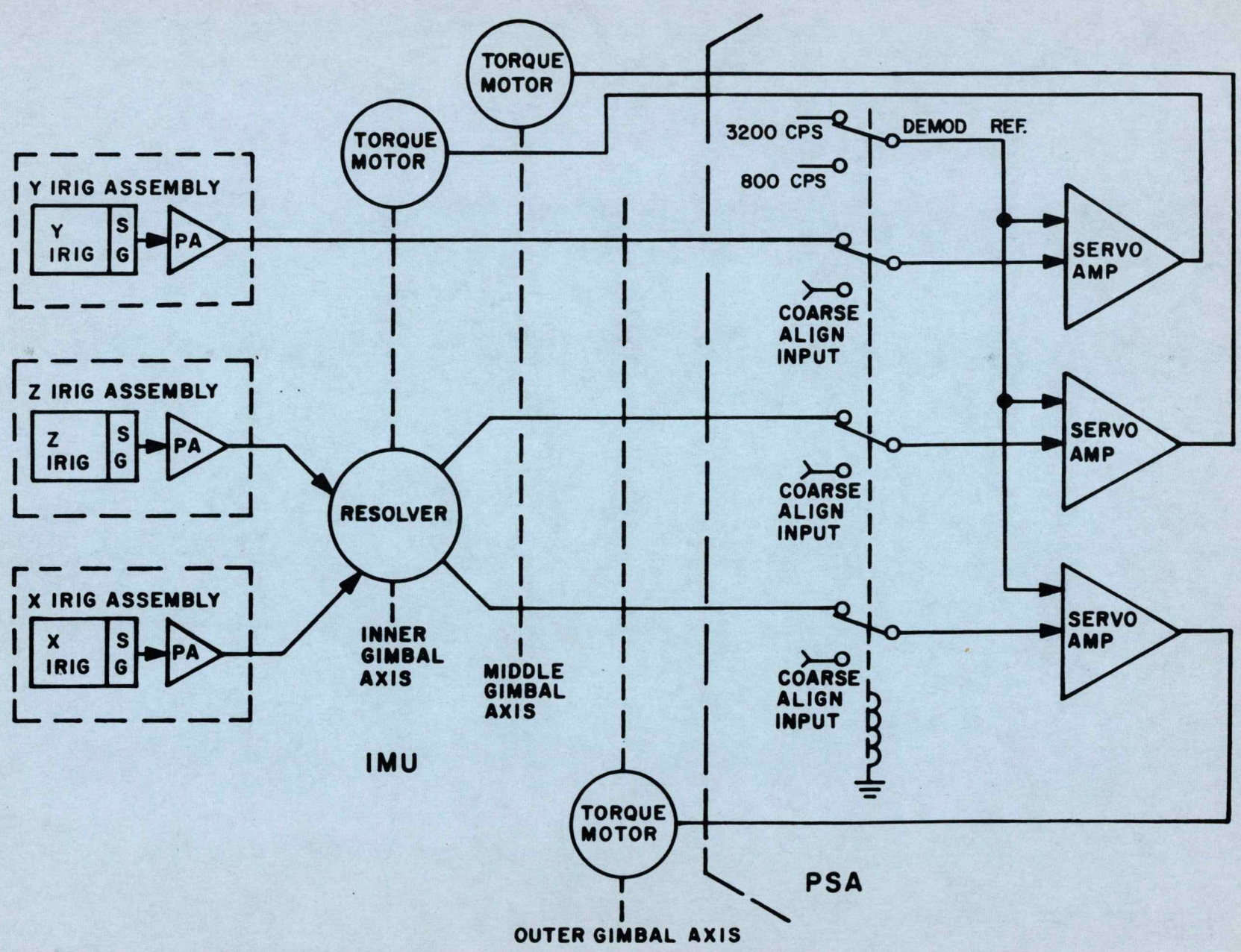
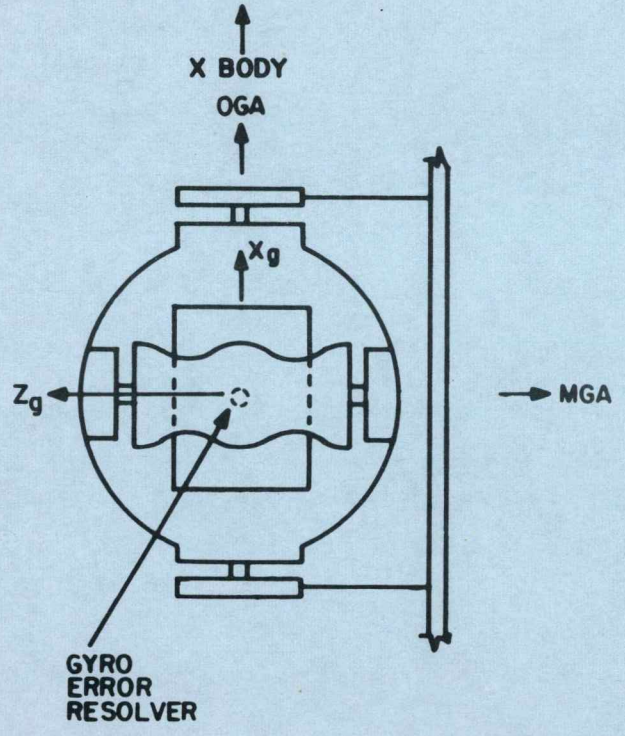


Figure 2-21. Block II Stabilization Loops



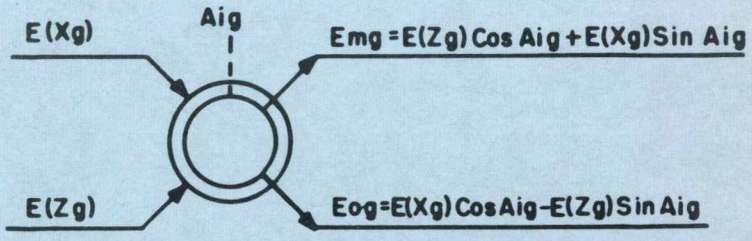


Figure 2-22. Gyro Error Resolver

the movement sensed by the IRIG is opposite in direction but equal in magnitude to the disturbance input and results in a precessional movement of the float. Due to precession, the float returns to its former null position. Since no output is then present from the signal microsyn, the loop is nulled and no further drive signals are applied until another disturbance is introduced into the system.

The components which make up the three stabilization loops are identical with two exceptions. First, the resistances used in series with the torque motor to provide current feedback to the gimbal servo amplifier differ to account for the difference in gimbal inertia. Second, a resolver is required in the middle and outer gimbal loop. This gyro error resolver is shown in figure 2-22. A description of the major components of the stabilization loop follows.

2.4.2.1 Apollo II Inertial Reference Integrating Gyro. The stabilization gyros used in the IMU are the IRIG's. This gyro is a fluid and magnetically suspended, single-degree-of-freedom gyro. It is one of the 25 series of inertial instruments. The 25 designation denotes the case diameter in tenths of inches.

The Apollo II IRIG is constructed like other conventional single-degree-of-freedom gyros. (See figure 2-23.) The gyroscopic wheel assembly spins on preloaded ball bearings. It is enclosed in a sealed, spherical beryllium float. The wheel assembly is driven by a hysteresis synchronous motor in an atmosphere of helium which prevents corrosion of the ferrous parts and also serves to provide good heat transfer within the float. The helium in the float is at a pressure of one-half atmosphere. The motor requires 28 volt, 800 cps, two-phase power. The space between the float and outer case is filled with a "suspension and damping fluid", polybromotrifluorethylene. This fluid is maintained at the same density as the float, thereby "suspending" the float with respect to the case and removing the friction between the float pivot and bearing. The fluid density is kept equal to the density of the float by maintaining the gyro and its fluid at the proper temperature. Two thermistors are submerged in the fluid to indicate fluid temperature.

This fluid also has the effect of damping the float oscillations with respect to the case. The space immediately surrounding the float is entirely filled with fluid. A large part of the non-functional space within the gyro case is consumed by damping blocks which control the damping gap and thereby assist in the control of the damping coefficient.

The Apollo II IRIG utilizes ducosyns for signal and torque generation. A ducosyn consists of a separate magnetic suspension assembly and a separate transducer microsyn mounted as a single coaxial-coplanar unit. The ducosyn contains two separate stators mounted to the case and two separate rotors mounted on a common ring on the float assembly. The inner suspension stator assembly consists of eight outwardly projecting poles which are wound and excited to provide axial and radial magnetic suspension. The outer extremities of these poles are tapered. The inner rotor is the magnetic suspension rotor which is a conic section and unwound. The outer microsyn stator assembly consists of twelve inwardly projecting poles which are wound and used to generate either output signals or torque. The outer rotor is the transducer rotor and consists of eight unwound salient poles projecting outward. In the Apollo II IRIG, the signal generator ducosyn is mounted on the positive output axis end of the float to provide magnetic suspension and to serve as a transducer to provide an electrical analog signal proportional to the position of the float. A torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension and to serve as a transducer to convert an electrical error signal into a torque about the output axis. The IRIG magnetic

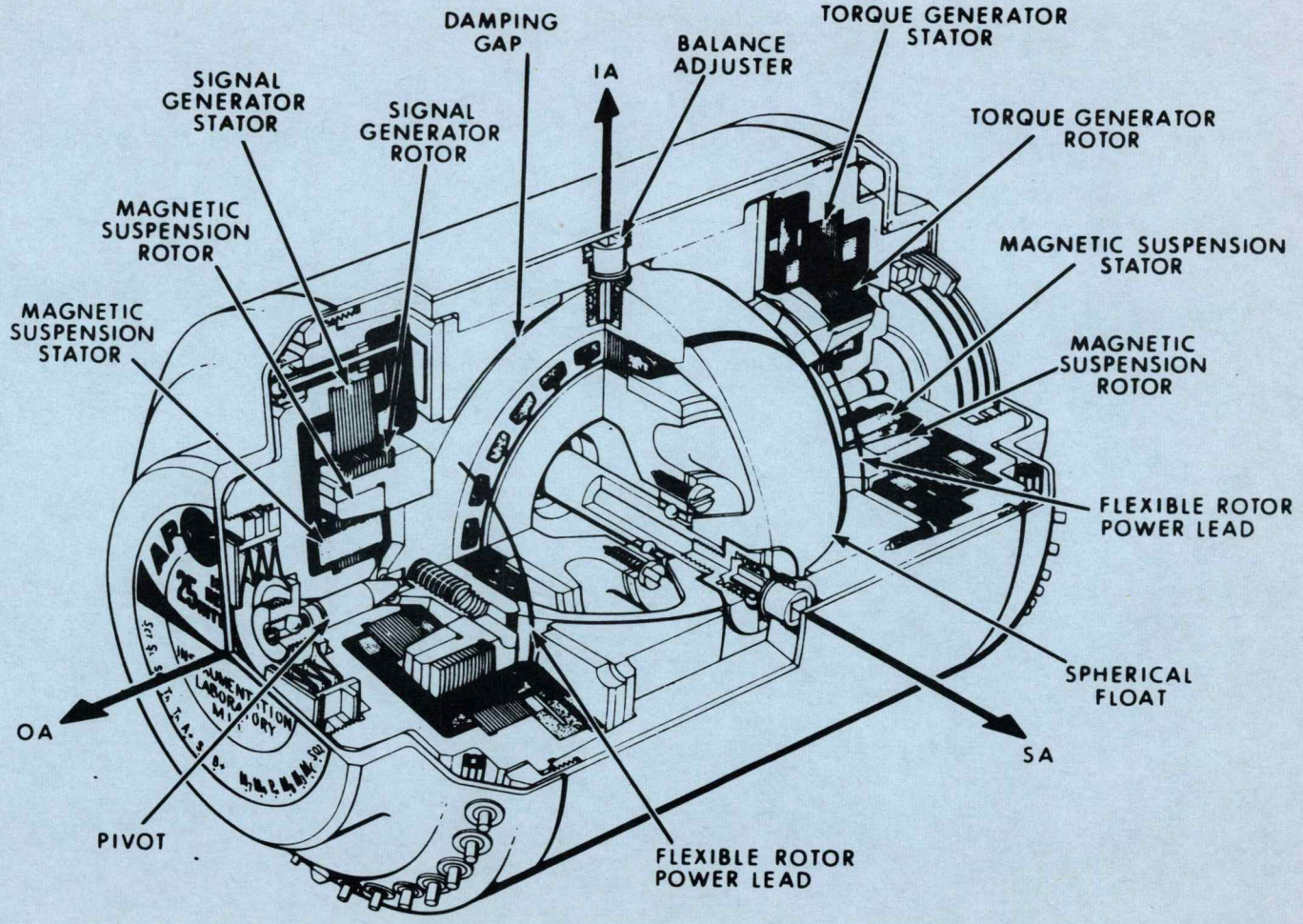


Figure 2-23. Apollo II IRIG (Generalized Pictorial Schematic)

suspension and the primary of the signal generator require a 4 volt, 3,200 cps, single-phase excitation. In addition to the magnetic and fluid suspension, the IRIG also has a set of pivots and bearings on the output axis. In this gyro, the pivots are part of the float assembly. Both the pivots and bearings are made of tungsten carbide. It should be noted that under normal environmental conditions, the pivots of the gyro never touch the bearing.

During final IRIG assembly, a pre-alignment package is added to the signal generator end of the gyro case. Addition of this package makes the gyro a pre-aligned unit. The package contains the following components:

a. Suspension Capacitors.

b. Temperature Sensor Padding Resistors.

c. End Mount Heater.

d. Torque Generator Normalization Components.

e. Signal Generator Preamplifier.

When the gyro is installed in the stable member, a heater is added to the torque generator end.

2.4.2.2 Ducosyn Operation. The ducosyn consists of an eight pole tapered suspension stator and a tapered rotor having no poles. The rotor is made of ferrite and is bonded to a beryllium web which is fixed to the gyro float. In addition to the suspension assembly the ducosyn has a torque generator assembly. This assembly utilizes a 12 pole stator and 8 (salient) pole high permeability alloy rotor which is bonded to the beryllium web. Several sets of stator windings provide for the operating characteristics and repeatability of these characteristics. Excitation during torquing is provided to the stator poles such that four flux fields are built up with maximum flux being present at the center pole of each group of three poles. The rotor pole nearest the center stator pole will tend to align itself to the strongest field near the center pole. For a positive (+) torque command, the strongest field is located at poles 2, 5, 8, and 11, resulting in a counterclockwise rotation of the rotor. This is illustrated in figures 2-24, 2-25, and 2-26. For a negative (-) torque the strongest field is located at poles 3, 6, 9, and 12 for a clockwise rotation of the rotor. There are two additional sets of windings on the torque ducosyn, the reset winding and bias winding. The torquing current applied to the poles is a dc level which tends to magnetize the rotor and stator. Small residual magnetism is adequate cause for changing the torque to current relationship in the ducosyn between torque commands. This would cause the scale factor of the gyro to be inconsistent since it would be a function of previous command polarity and duration. The reset coil has a 3.2 kc excitation present on it at all times and therefore performs a degaussing function on the ducosyn, wiping out any residual magnetism. The bias winding is used to apply a level of reaction torque on the float equal but opposite to any flex lead torques that are present in the gyro. Bias torques on the functioning unit are thereby minimized.

2.4.2.3 Normalization Package. The normalization package (figure 2-27) contains two resistive elements that directly affect torquing scale factor as well as other elements necessary to gyro function. The two resistors are each located in parallel with the torque windings to control the current in the windings to obtain a gyro scale factor of .617981 second of arc per CMC torque pulse to the binary current switch. Also located in the normalization package are the ducosyn suspension capacitors, a thermistor padder resistor, a heater assembly, a bias control resistor, and a signal generator output preamplifier. This assembly makes each gyro a prealigned unit, interchangeable with any other Apollo II IRIG. The normalization components are located on one end of the gyro to form the Apollo II IRIG assembly.

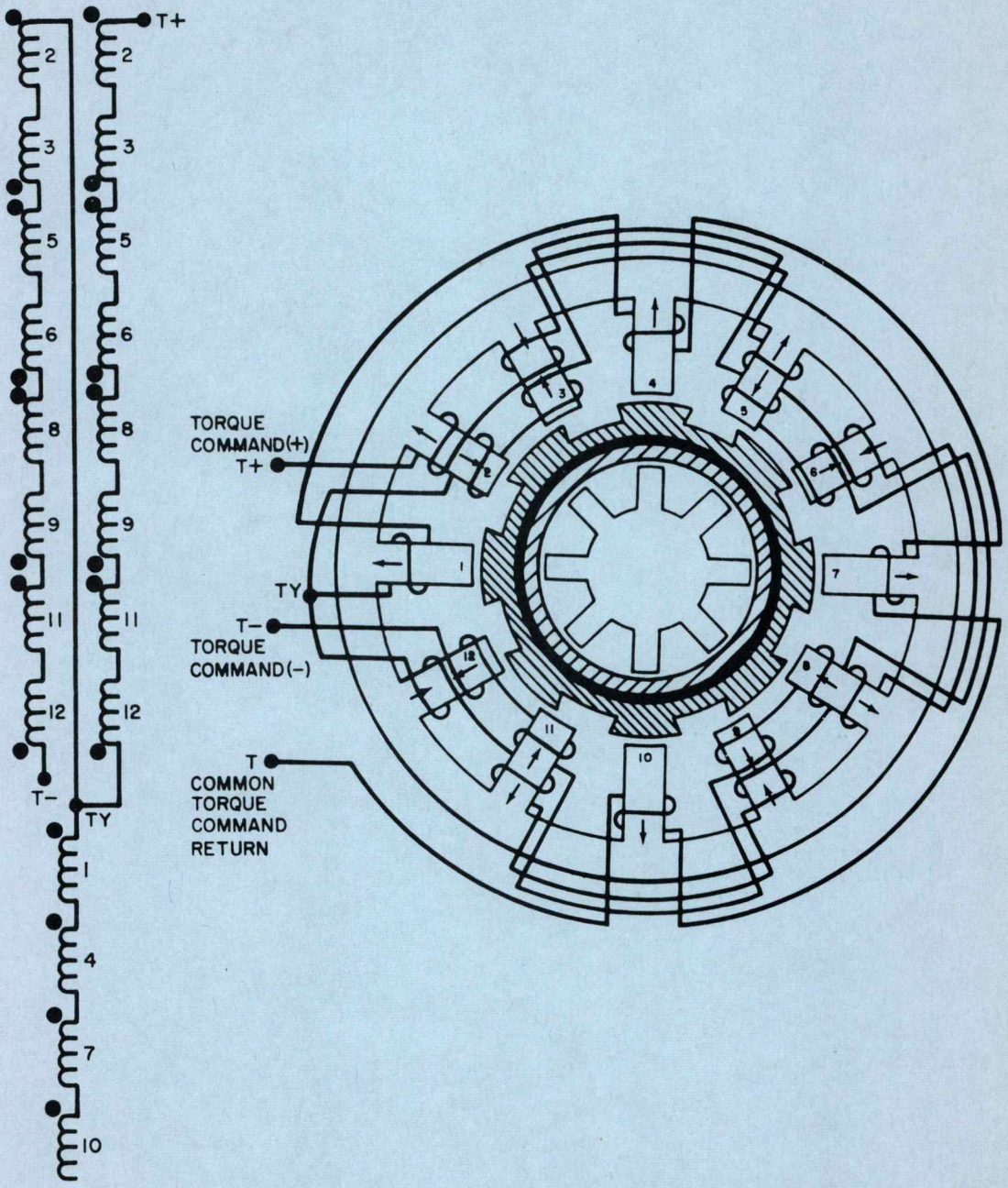


Figure 2-24. Ducosyn Torque Generator

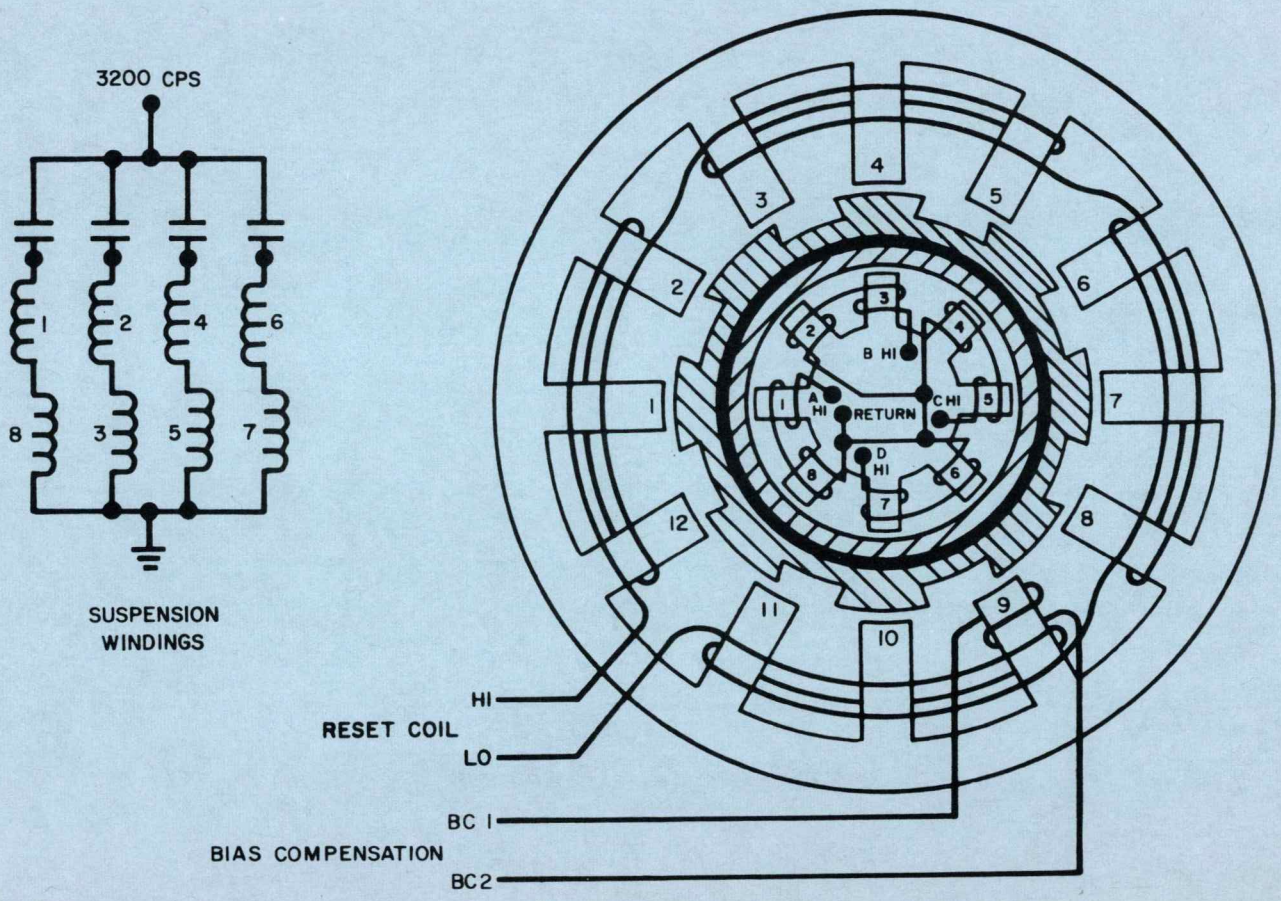


Figure 2-25. Reset, Bias and Suspension Windings (TG Ducosyn)

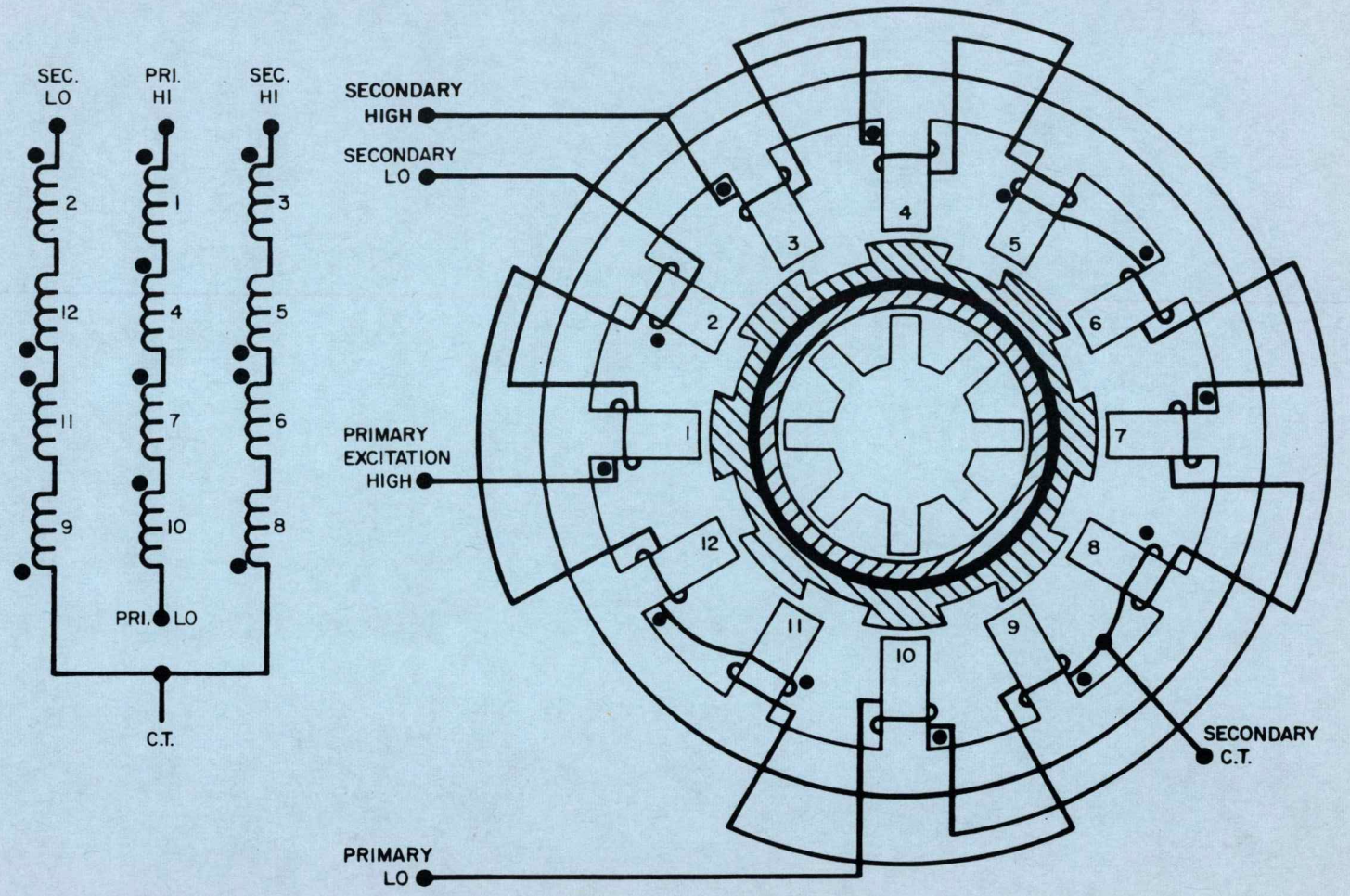


Figure 2-26. Signal Generator (SG Ducosyn)

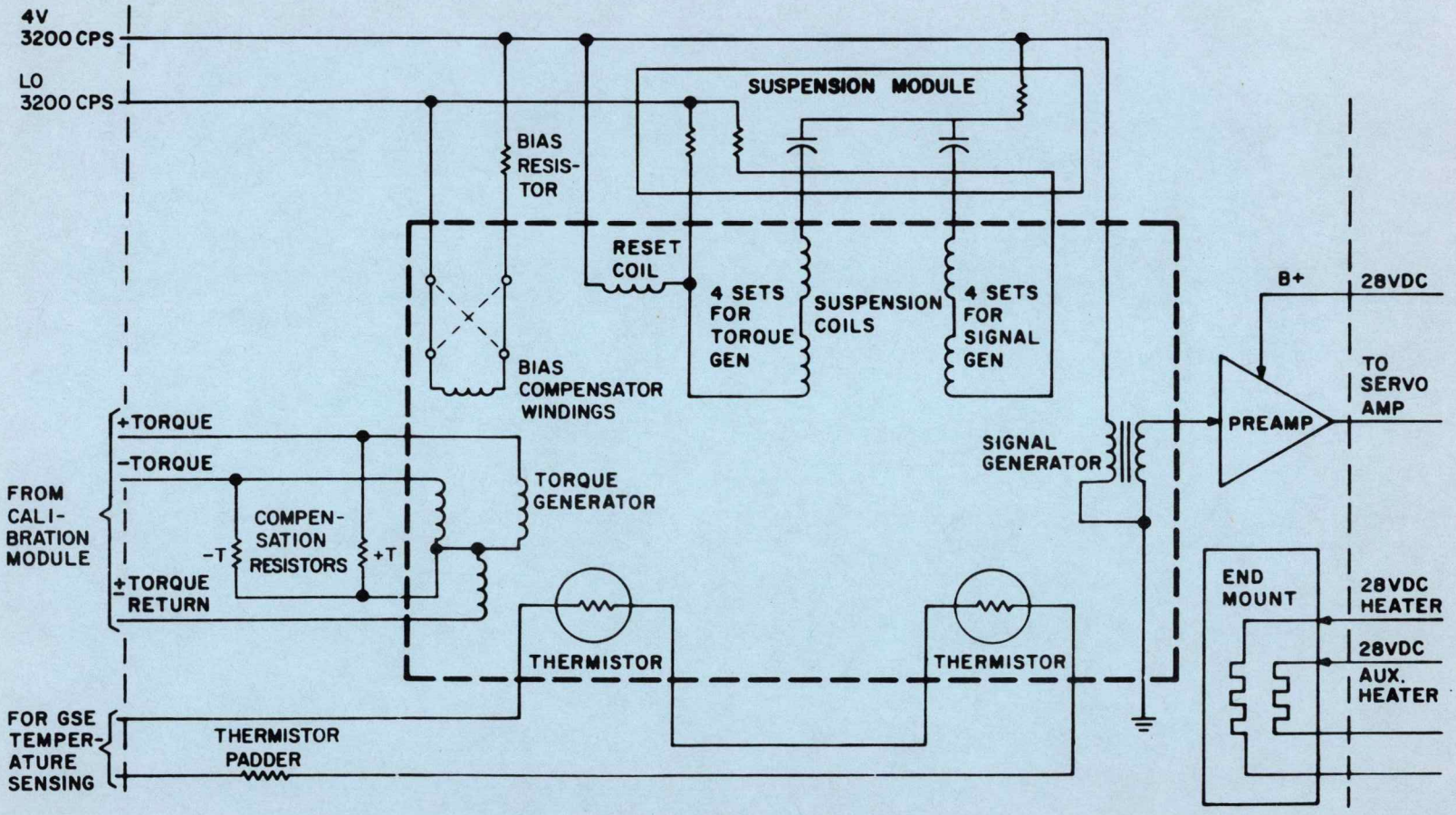


Figure 2-27. Apollo II IRIG Normalizing Assembly

2.4.2.4 IRIG Preamplifier. The gyro error signal from the signal generator is amplified by the IRIG preamplifier to achieve a high signal-to-noise ratio for transmission through the gimbal slip rings to the gimbal servo amplifier. The preamplifiers are each mounted in the gyro assembly and have a gain of 214 volts/volt. The signal input is phase shifted 180° at the output, and saturation outputs of 10 volts rms are obtained with a 46 millivolt input.

2.4.2.5 Resolver. The gyro error resolver in the X and Z loop has a 1 to 1 gain ratio and quadrature generation of less than 50 millivolts. The use of the resolver in the system is to enable the middle and outer gimbals to be controlled only by the Z and X IRIG errors sensed along the gimbal axis. For example, if a disturbance torque occurs about the middle gimbal axis with the stable platform at some angle other than zero, the disturbance will be felt by both X and Z gyros. The resolver sums the components of gyro error that lie along the middle gimbal axis and routes these to the middle gimbal servo amplifier and torque motor only. The same type of operation results with respect to a torque about the outer gimbal axis except that the sum of the gyro error components is routed to the outer gimbal torque motor.

2.4.2.6 Gimbal Servo Amplifier (GSA). The GSA module is used to drive the torque motor when an input voltage is applied. The amplifier module consists of the demodulator, a difference amplifier and power amplifier as well as several compensation networks as shown in figure 2-28. Each gimbal has associated with it one GSA. All three amplifiers are identical. Different gains for the three loops are accomplished by connections through the module connector. This varies the amount of feedback to the difference amplifier. The dc gains of the three amplifiers are as follows:

a. Inner Gimbal Servo Amplifier	16.4 Amps/Volt.
b. Middle Gimbal Servo Amplifier	32.8 Amps/Volt.
c. Outer Gimbal Servo Amplifier	49.2 Amps/Volt.

The demodulator is a full wave diode bridge with an AC reference applied. The bridge changes the 3200 cps gyro error or 800 cps CDU coarse align input into a positive or negative dc signal for further amplification. The reference input is switched between 800 cps and 3200 cps along with the demodulator input by the coarse align relay. The demodulator is followed by a tuned filter to suppress any noise than may be present. The gain of the demodulator is 1 volt dc per volt rms and its output saturation voltage is ±10 vdc.

Compensation networks are used in the amplifier to provide the desired dynamic stabilization loop operation characteristics and for high frequency attenuation at gimbal resonant frequencies. A notch compensation network is used in the feedback loop to increase the high frequency response of the amplifier compensating for the IRIG high frequency attenuation. A series compensation network is used to improve large signal stability by varying the natural phase response of the amplifier as it approaches saturation. Additional current feedback to the power amplifier provides the capability for constant current output independent of load impedance. During coarse align operation the elements of the compensation networks are changed due to the variation in the required gimbal dynamics for this mode.

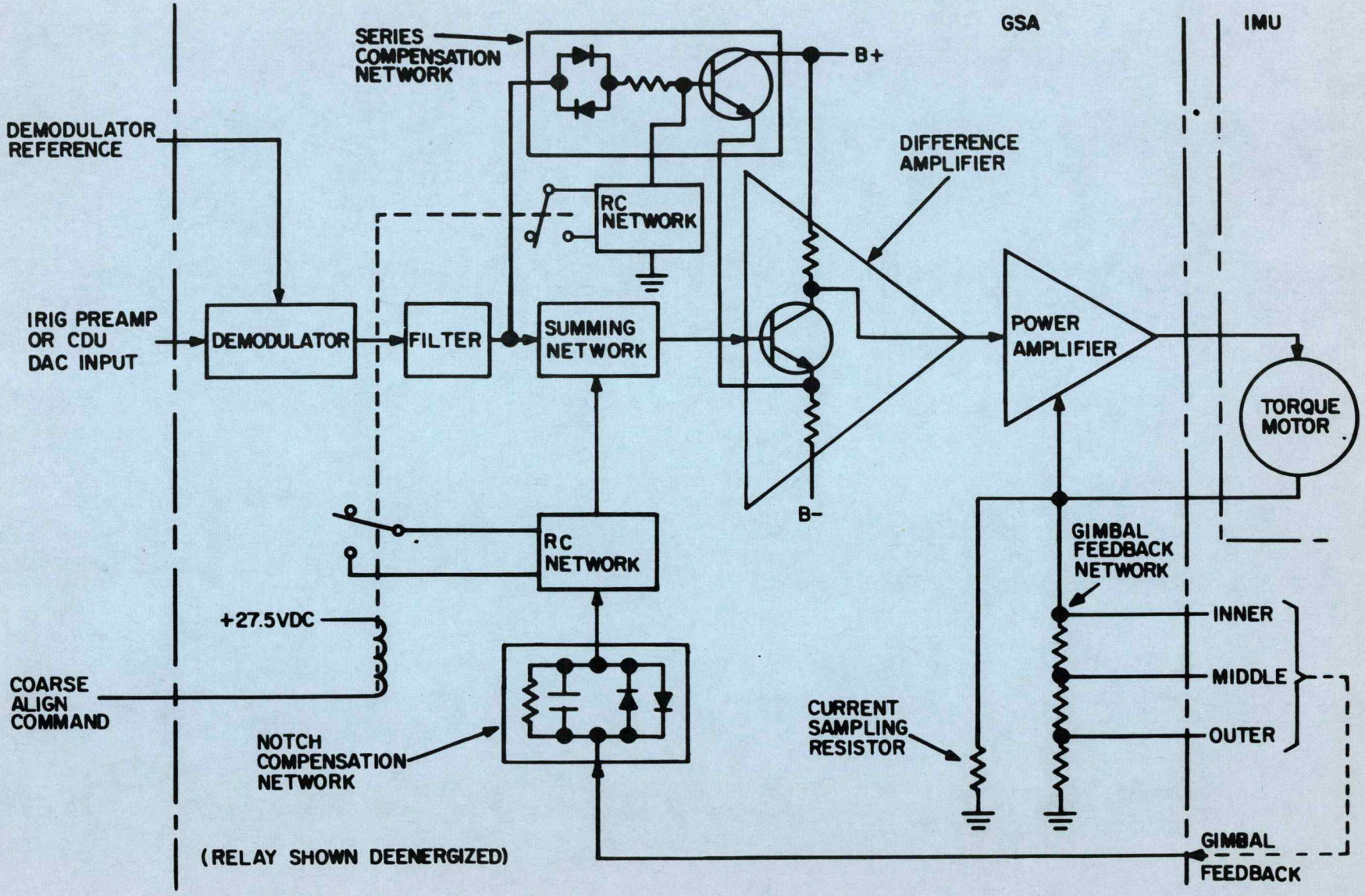


Figure 2-28. Block II Gimbal Servo Amplifier

2.4.2.7 Torque Motor. One dc torque motor is used to drive each gimbal. Two of these, located on the inner and middle gimbals have a sensitivity of 1.12 foot pounds per ampere. The third, located on the outer gimbal has a sensitivity of .906 foot pounds per ampere. The motors are located in the inter-gimbal assembly on the positive gimbal axes.

2.5 FINE ALIGN ELECTRONICS

The purpose of the fine align electronics is to allow the introduction of external loop control driving signals into the stabilization loops during closed loop conditions. By purposely introducing a torque to the IRIG floats through the torque ducosyns it is possible to cause the IMU gimbals to drive to new positions. This permits a fine alignment of the stable member to a desired reference with considerable accuracy. Figure 2-29 shows a block diagram of the complete torquing electronics. When gyro torquing is required during the fine align mode of operation, the computer issues pulses that:

a. Enable the torquing electronics.

b. Select the gyro to be torqued.

c. Select the direction of torquing.

d. Control the amount of torque applied.

The three IRIG's are torqued sequentially by the computer during fine alignment and it is therefore possible for all three gyros to be controlled through one set of torquing electronics. Figure 2-30 shows the CMC pulses and their timing required for gyro torque control of all three gyros. The subsequent discussion illustrates the function of the components in the electronics.

Power for gyro pulse torquing electronics is obtained from the 120 volt dc output of the pulse torque power supply, and 28 volt dc spacecraft prime power.

2.5.1 GYRO CALIBRATION MODULE. The gyro calibration module is located in the power servo assembly (PSA). The gyro calibration module contains the six transistor switches required for the selection of the gyro torque winding to be pulsed. It also contains the gyro compensation components, the current control resistors, and a torquing power enabling relay. A simplified diagram of the calibration module is shown in figure 2-31.

2.5.1.1 Torque Enable Relay. The 102.4 kc computer command (torque enable) is applied to a half-wave rectifier. The rectified signal is filtered and used to drive a transistor into conduction, thereby energizing the torque enable relay. This relay applies 120 vdc and 28 vdc to the pulse torque electronics.

2.5.1.2 Torque Winding Selection Switches. The 6 computer gyro select signals (102.4 kc) $+\Delta\theta_X$, $+\Delta\theta_Y$, $+\Delta\theta_Z$, $-\Delta\theta_X$, $-\Delta\theta_Y$, and $-\Delta\theta_Z$ are applied to 6 gyro select transistor switches through individual transformers and rectifiers. Presence of a select signal on any switch causes the transistor to conduct thereby providing a ground to the selected gyro torque winding and enabling the flow of current through the winding.

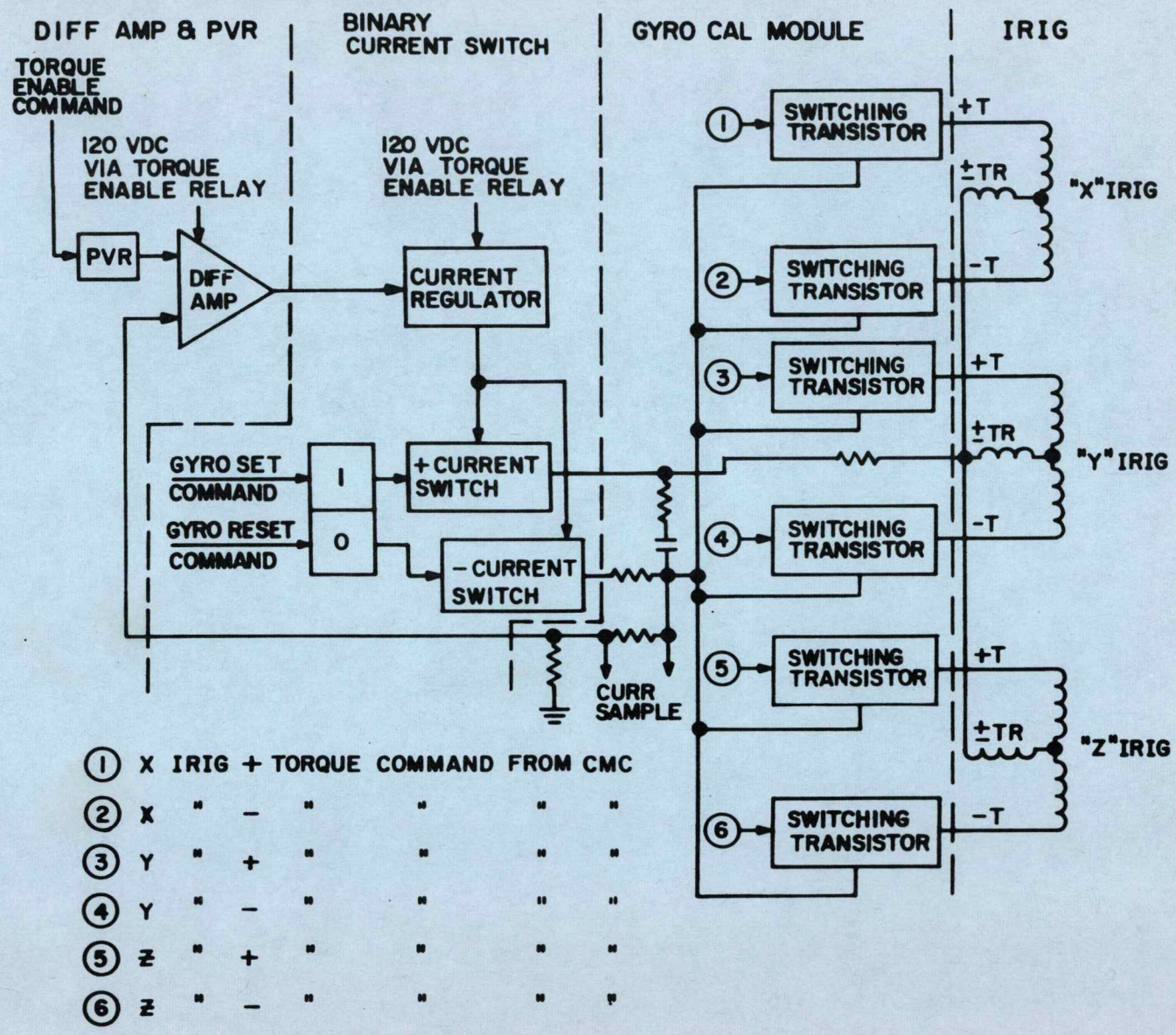


Figure 2-29. Gyro Pulse Torquing Electronics

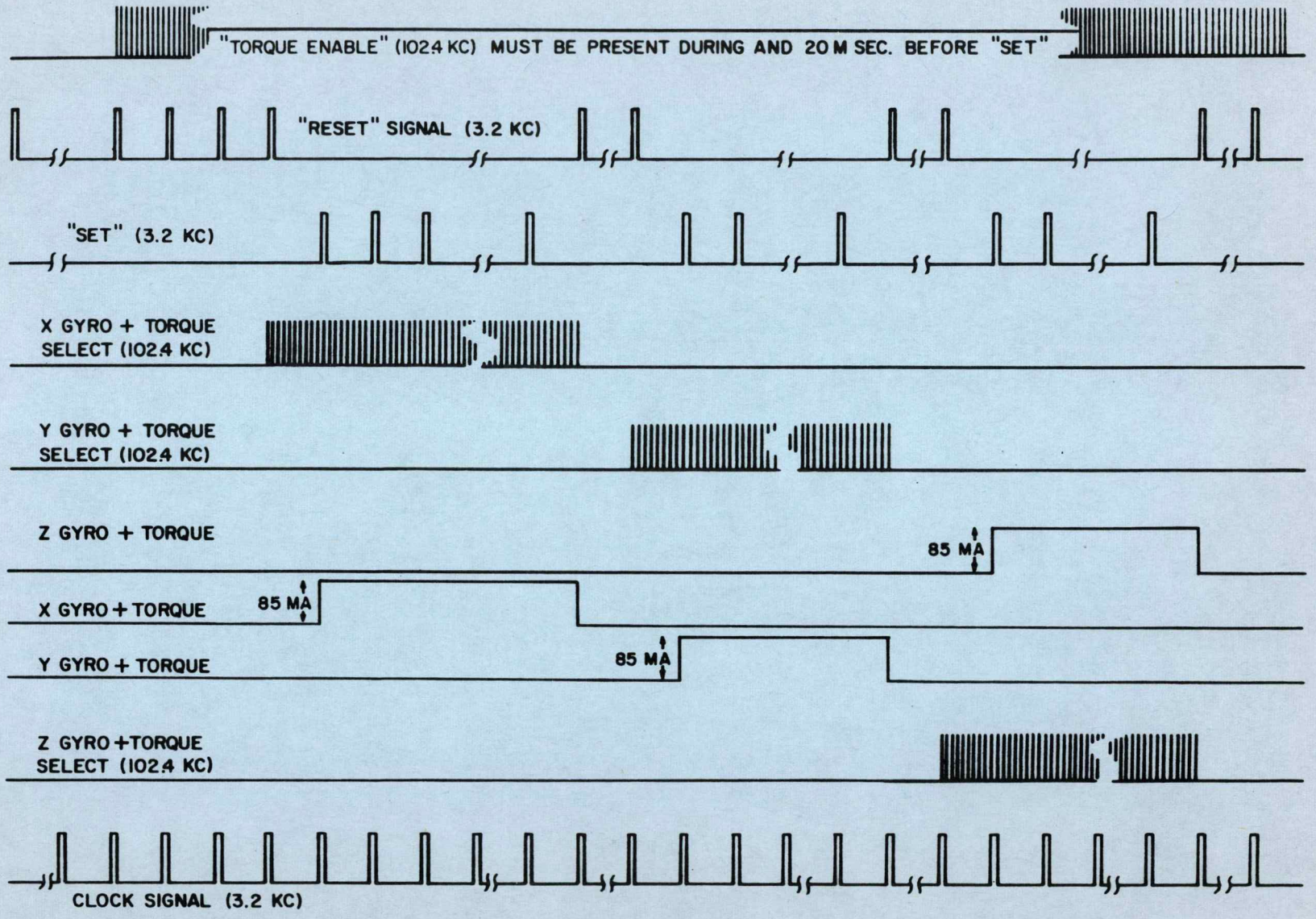


Figure 2-30. Gyro Torque Computer Pulse Timing

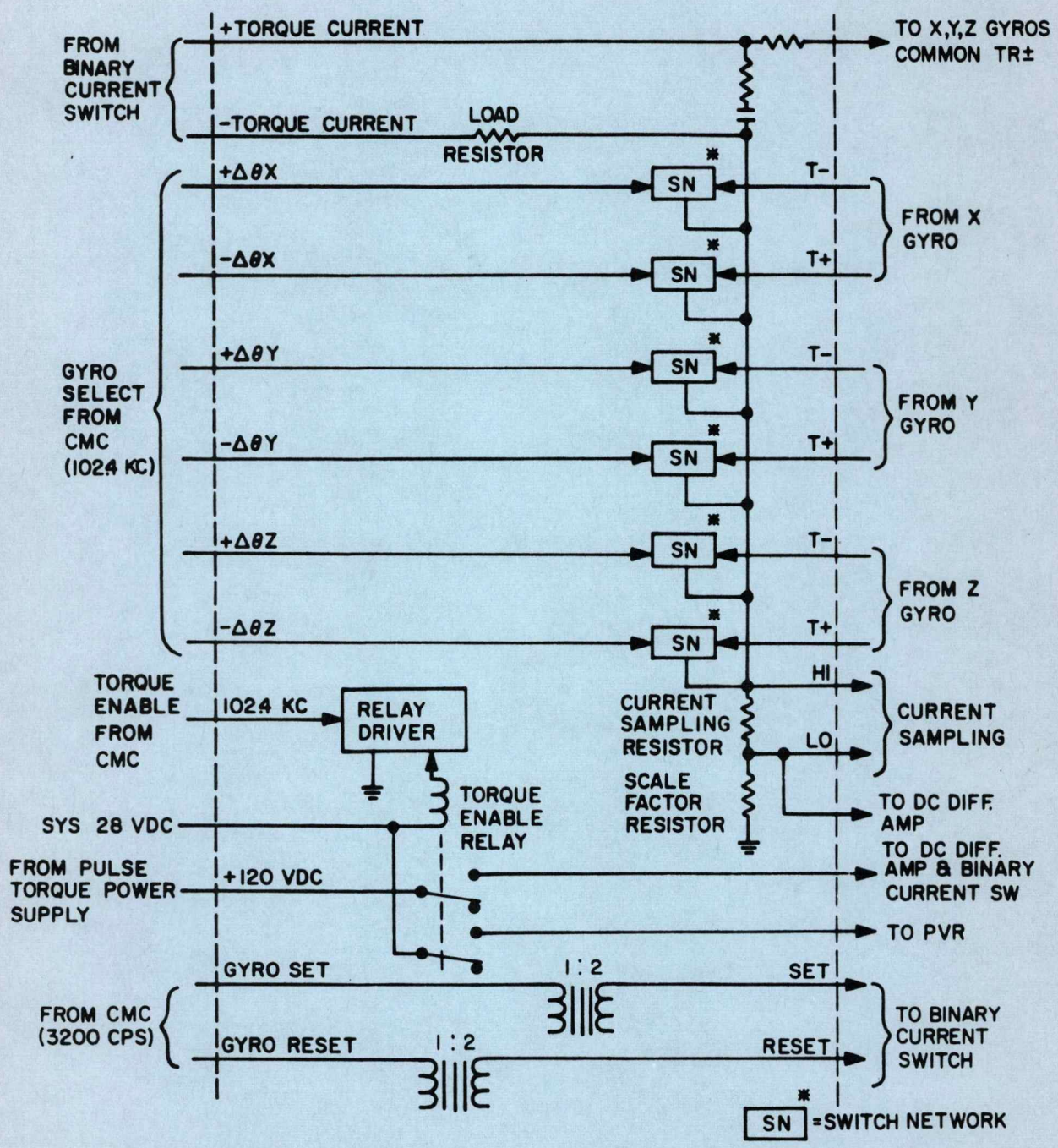


Figure 2-31. Calibration Circuit

2.5.1.3 Compensation and Dummy Load Resistors. A dummy load is located in the calibration module to present a constant impedance to the torque current supply during the time that the torquing loop is enabled. This condition exists just prior to gyro selection and during selection changes.

A current sensing resistor for external monitoring is in series with the current return line feeding the select switches and dummy load. This permits a check of current in the loop. A scale factor resistor is applied to the current sampling resistor low and provides the path to ground for the torque current. The voltage developed across this resistor is nominally 6 volts when the proper operating current is present in the circuit. This voltage is the regulator input to the constant current supply.

2.5.2 BINARY CURRENT SWITCH. The binary current switch converts the CMC set pulses of 3 usec duration to dc current pulses of 312.5 usec or a multiple of 312.5 usec if more than one set pulse is applied. These +T (torque) pulses are applied to the selected gyro through the calibration module and are present as long as set pulses are issued by the CMC. During the periods prior and subsequent to the + T pulses, the binary current switch routes the torque current to the calibration module dummy load. This presents a constant load on the constant current supply at all times to minimize transients. Figure 2-32 is a block diagram of the binary current switch as used in the gyro torquing electronics. The stab loop binary current switch is identical to that used in the accelerometer loop. Inputs of power to the binary current switch are 120 volts through the torque enable relay and regulated voltage of 85 vdc to the current regulator located in the binary current switch module.

2.5.3 CONSTANT CURRENT SUPPLY. The constant current supply for the gyro torquing loop consists of a voltage regulator, precision voltage reference and dc differential amplifier located in one module and the power amplifier (current regulator) in the binary current switch. (Refer to figure 2-33.)

The differential amplifier has two inputs which it compares to control its output voltage. Six volts is applied to one input from the scale factor resistor of the gyro calibration module. The other input is the six volt precision voltage reference, obtained by a zener diode regulated three stage voltage divider. The 120 volt dc B+ voltages to each stage are passively regulated by resistor and zener regulators. Regulation of the amplifier is essential to the maintenance of a constant current to the IRIG torque ducosyns. This is to insure that at all times the torquing electronics scale factor is maintained at .617981 seconds of arc of rotation at the gimbal for each + set torquing pulse applied to the binary current switch from the CMC. This is accomplished by maintaining current to the ducosyn windings at a nominal 85 ma.

2.6 ACCELEROMETER LOOP

The purpose of the three accelerometer loops is to measure the linear acceleration of the stable member along three mutually perpendicular axes and to integrate this data to determine velocity. The velocity data is utilized by the CMC to compute the spacecraft trajectory.

2.6.1 ACCELEROMETER LOOP OPERATION. The accelerometer loops use three 16 PIP's which sense linear acceleration of the stable member. The input axes of the 16 PIP's are oriented as described in figure 2-15. Usable velocity outputs of the PIPA loops to the computer are generated whenever the stable member is accelerated due to thrust applied to the spacecraft or when the guidance and navigation system is subjected to gravitational forces of the moon. The output signals are checked to determine the direction

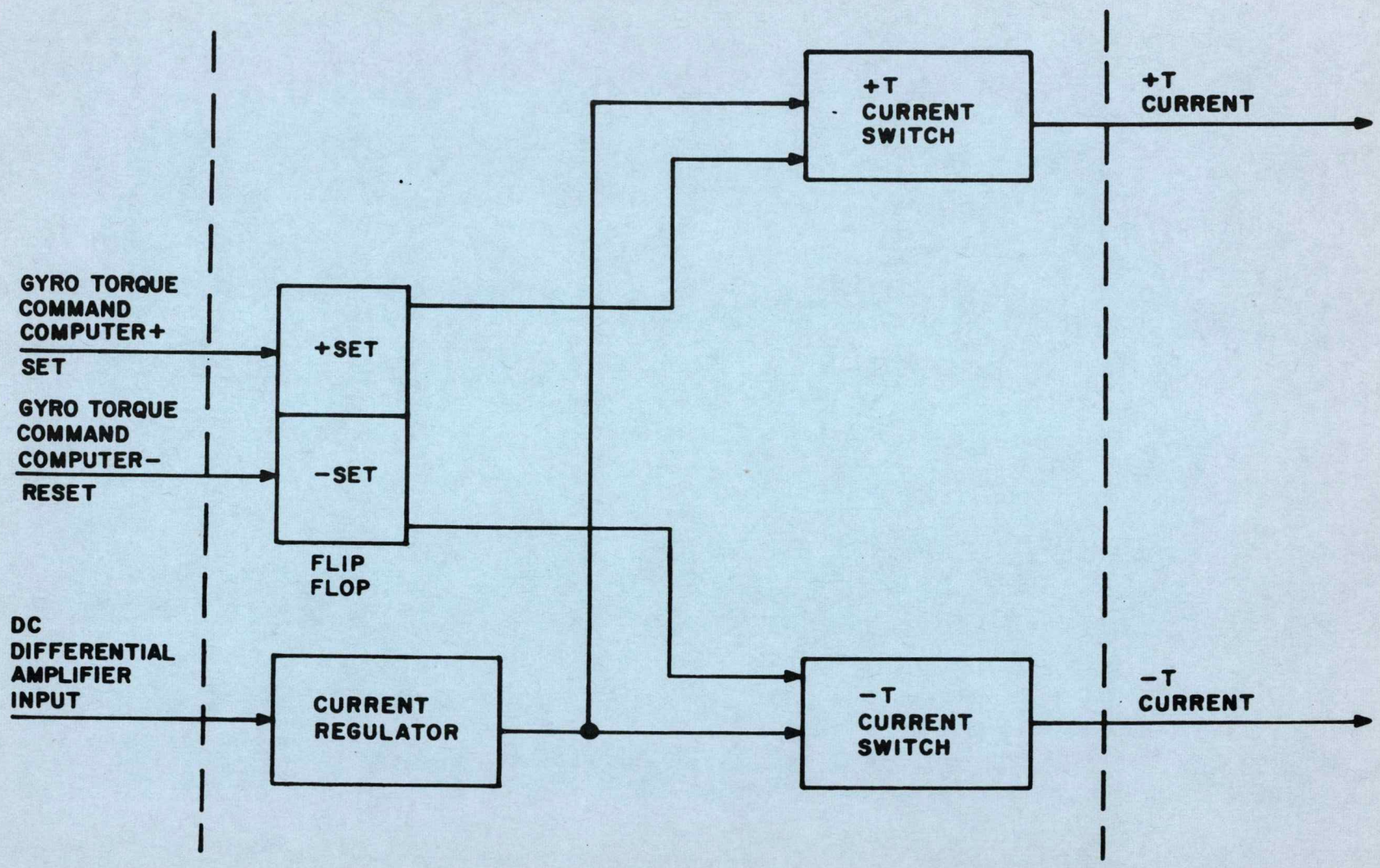


Figure 2-32. Binary Current Switch (Block II Stab Loop)

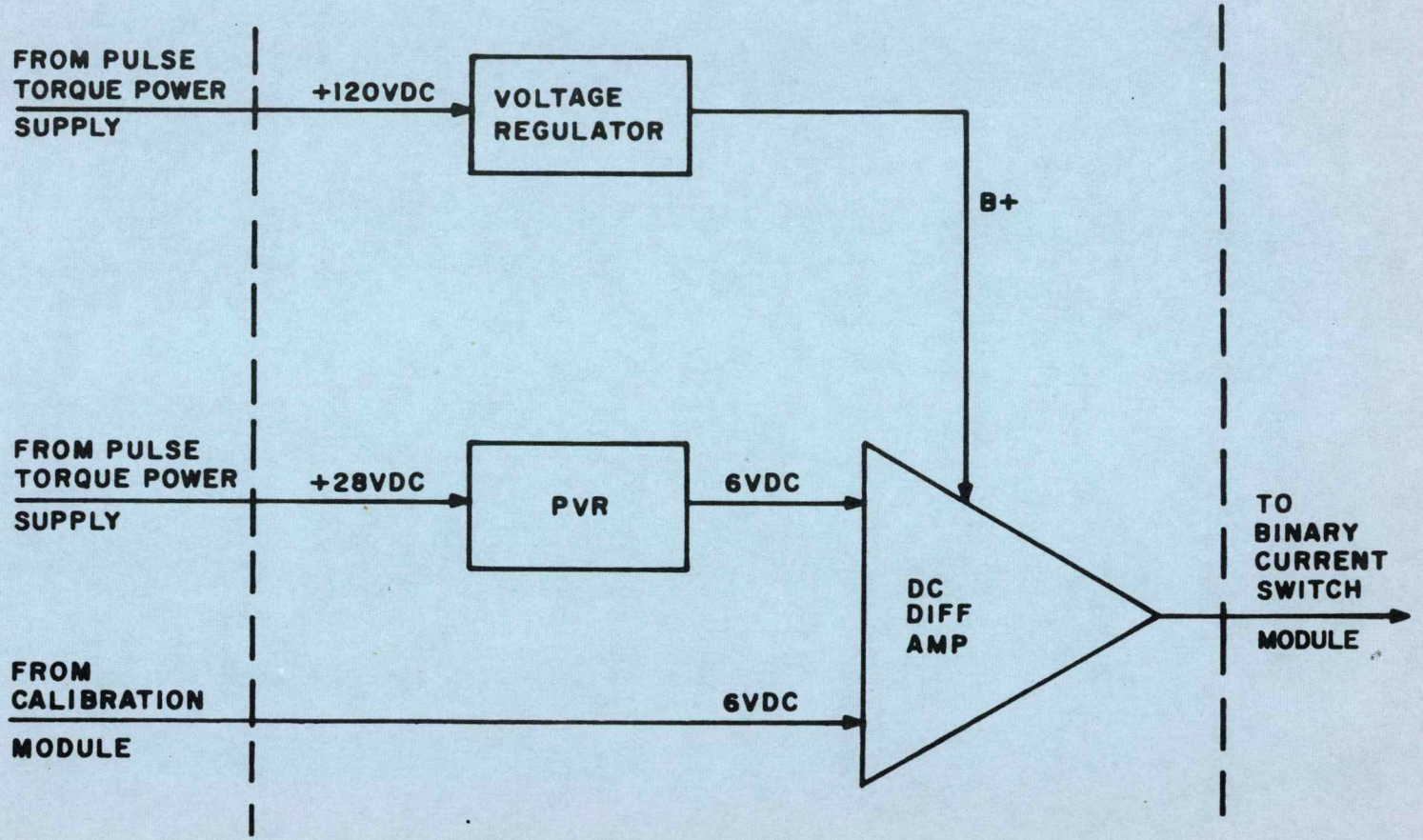


Figure 2-33. Block II DC Differential Amplifier and Precision Voltage Reference

of the acceleration so torquing signals can be generated to torque the 16 PIP's back to null. While this process is occurring, signals, representative of incremental velocity changes, are generated by the loop and sent to the CMC.

A typical accelerometer loop data flow is shown in figure 2-34. The 16 PIP signal generator ducosyn outputs are 3,200 cps error signals which are proportional to the rotation of the pendulum about its output axis. The two outputs are amplified by the preamplifier and routed to the ac differential amplifier. The amplified signals are then transmitted to the interrogator which also receives the interrogator pulse and the switching pulse from the CMC. These inputs to the interrogator are used to generate the TM + SET or TM - SET commands to the binary current switch.

The TM+ SET and TM - SET commands are used to produce plus (+) torque or minus (-) torque outputs from the binary current switch. A data pulse from the computer to the binary current switch is used to generate the positive (P) and negative (N) velocity pulses which are sent to the forward-backward counter in the CMC. The + or - torque output of the binary current switch is sent to the calibration module and then to the PIP torque generator ducosyn where a torque is developed which will move the pendulum back toward null. A feedback signal from the calibration module to the dc amplifier and the precision voltage reference is used to regulate the torquing current supplied by the binary current switch. The positive and negative velocity pulses are routed to the forward-backward counter in the CMC. During normal accelerometer loop operation when no acceleration is being sensed, an equal number of positive and negative pulses are generated. When an acceleration is sensed, more of one type of pulse will be generated. This unbalance produces either plus ΔV or minus ΔV pulses which are routed to the CMC PIPA counter to be accumulated as spacecraft velocity changes. Power inputs to the accelerometer loop are 120 vdc, 28 vdc, +20 vdc, and -20 vdc. The PIP's and preamplifiers are located on the IMU. The pulse torque power supply is located in the PSA. All other components of the PIPA loop are located in the (PEA) PIPA electronics assembly. The PEA is located on the port side of the lower D&C and is a sealed assembly.

2.6.2 ACCELEROMETER LOOP MECHANIZATION. The components which make up the three accelerometer loops are identical. A description of the major components of an accelerometer loop follow.

2.6.2.1 16 PIP. (Refer to figure 2-35.) The 16 PIP is used in the IMU as an acceleration sensitive device. When fixed in its associated accelerometer loop, the 16 PIP becomes an integrating accelerometer. The 16 PIP is basically a pendulum-type device consisting of a cylinder with a pendulous mass unbalance (pendulous float) pivoted with respect to a case. The axis of the pivot defines the PIP output axis (OA). The space between the pendulous float and the case is filled with fluid. A signal generator ducosyn is mounted on the positive end of the output axis to provide magnetic suspension and output signals indicative of rotational position of the float. The torque generator ducosyn also acts as a transducer to convert torque signals, in the form of electrical pulses, into mechanical torque about the output axis. A 2-volt rms, 3,200 cps, single-phase excitation is required for the 16 PIP magnetic suspension windings and the primary winding of the signal generator.

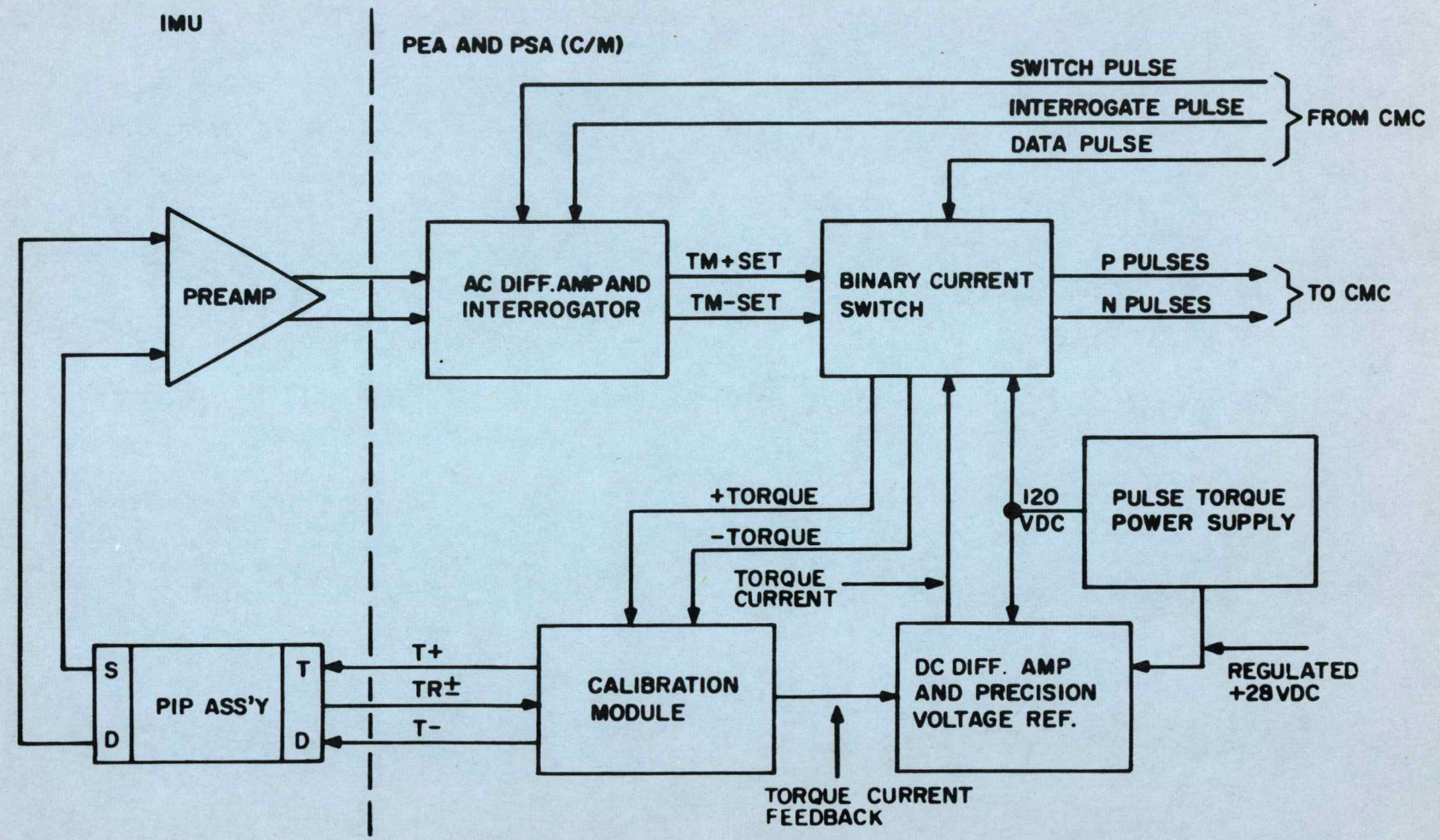


Figure 2-34. Block II Accelerometer Loop

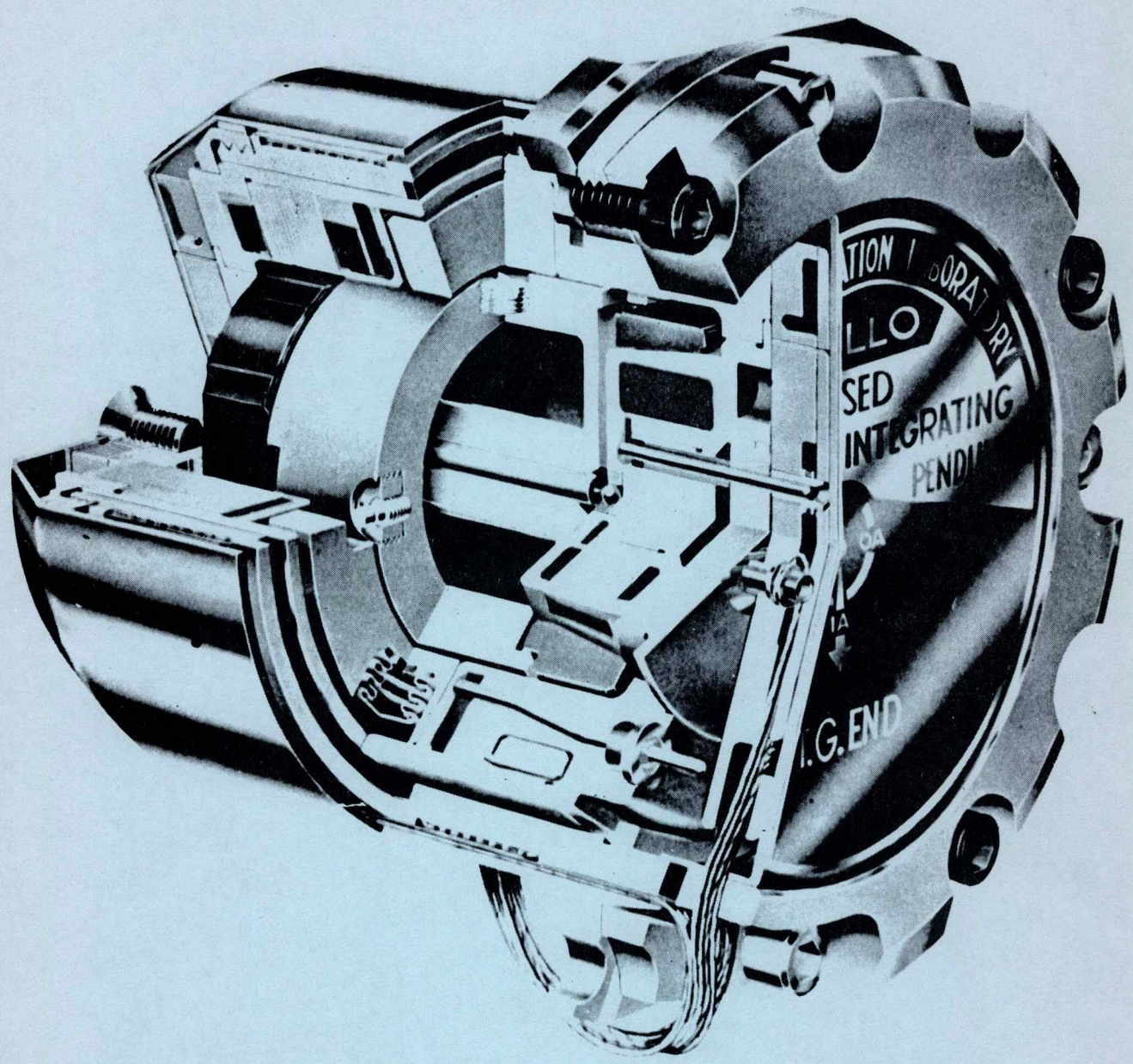


Figure 2-35. 16 PIP

The float body is a cylinder of beryllium which is fitted to a shaft on which the float pivots. The rotors of the ducosyns are mounted on the ends of the float body. The complete float assembly is placed in the main housing assembly and the space serves as both a fluid suspension for the float and as a viscous damping gap for the fluid. The main housing contains a bellows assembly to take up the expansions and contractions of the fluid during heating. The end housings of the 16 PIP contain the ducosyn stators and the pivot bearing. The magnetic suspension units have tapered stator poles and a tapered rotor so that magnetic suspension forces will be developed in both the axial and radial directions. The main housing assembly is completely covered by a case which provides magnetic shielding and a hermetic seal of the unit. Heating coils are placed between the main housing and case to heat the suspension fluid to the proper temperature. All electrical signals for the 16 PIP are routed through the torque generator end of the case.

With an acceleration being sensed along the input axis of the 16 PIP, the float rotates from the null position. This rotation is sensed by the signal generator ducosyns. The reference excitation voltage of the signal generator is synchronized with the CMC clock which is the reference for all system and loop timing.

The output of the secondary of the signal generator ducosyn cosists of two amplitude-modulated, suppressed-carrier signals, one of zero phase and the other of π phase. These two 180-degree out-of-phase signals are phase shifted 45 degrees from the reference excitation by the effect of a resistor in series with the secondary winding, and amplified by a preamplifier mounted on the stable member. Refer to figure 2-36 for pulse relationships in the accelerometer loop.

2.6.2.2 AC Differential Amplifier and Interrogator. The differential amplifier and interrogator are contained in a single module in the PEA.

The amplifier zero and π phase signals from the preamplifier are applied as separate inputs to the ac differential amplifier. The inputs are then summed, amplified and sent to a phase splitter. The two resulting signals are then sent to the interrogator.

The interrogator analyzes the ac differential amplifier outputs to determine the direction of 16 PIP float movement and to generate appropriate torquing commands. Refer to figure 2-37 for a block diagram of the interrogator.

The two amplified ac signals from the ac differential amplifier go to two summing networks and threshold amplifiers. Interrogate pulses (IP) are also being received by the interrogator. The interrogate pulses consist of a train of pulses, two microseconds in width, occurring at 3200 pps and timed to occur 135 degrees after the positive zero crossing of the reference excitation. With this phasing, the interrogate pulses occur at the 90-degree peaks of the zero phase or π phase input signals. The interrogator pulse therefore occurs at the 90-degree peak of the +T signal if the pendulum angle is positive, and at the 90-degree peak of the -T signal if the pendulum angle is negative. The +T and -T signals and the interrogate pulses are "anded" by the summing network and threshold amplifier.

The output of the threshold amplifier furnishes the input to a bi-stable multivibrator (flip-flop). If the flip-flop is already in the + set condition, a succession of +T set pulses will maintain the set condition. The + set condition will persist until the pendulum angle decreases past zero to an angle sufficiently negative to overcome the threshold of the second amplifier. At this time a -T set pulse appears and causes the flip-flop to go to a - set condition.

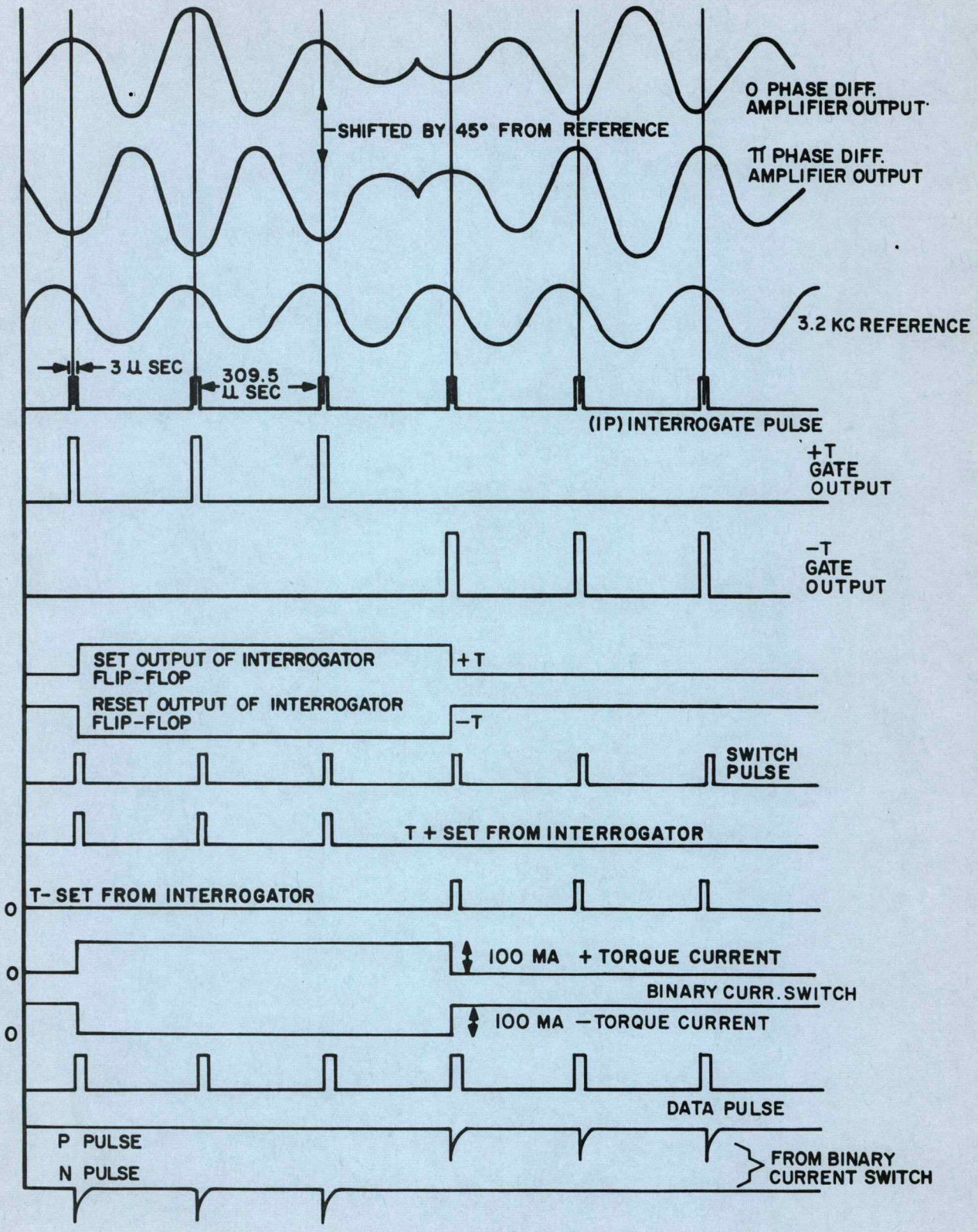


Figure 2-36. Pulse Diagram - PIPA Loop

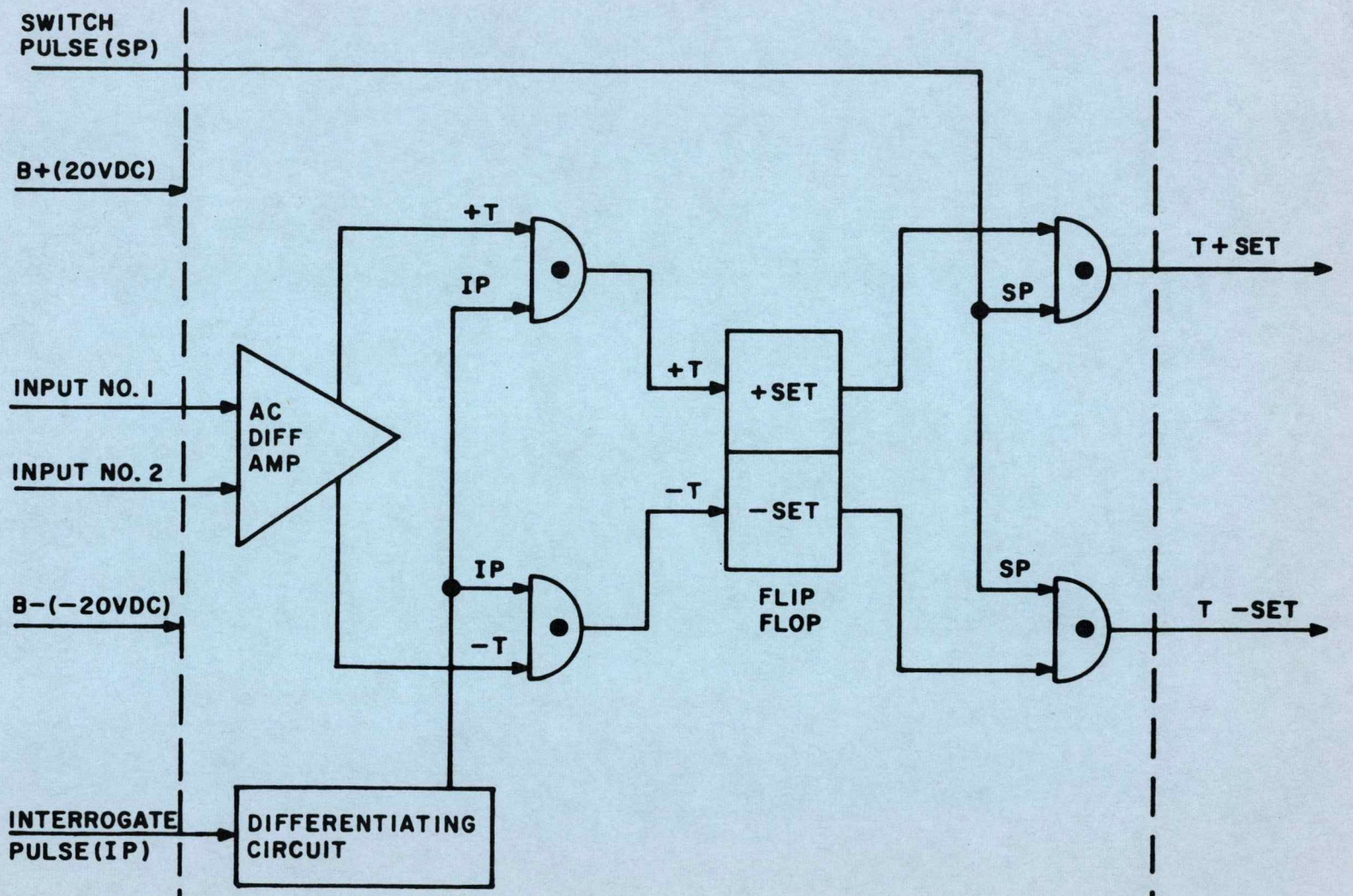


Figure 2-37. Block II AC Differential Amp and Interrogator Module

The outputs of the bi-stable multivibrator go to two "and" circuits which are also driven by the switch pulses. The pulses consist of a train of clock-driven 3200 pps pulses three microseconds in width and timed to occur three microseconds after the leading edges of the interrogator pulses. The outputs of the "and" circuits are called the TM + SET and TM - SET pulse.

2.6.2.3 Binary Current Switch. The binary current switch utilizes the outputs of the interrogator to generate 16 PIP torquing current and velocity change pulses. Refer to figure 2-38 for a block diagram of the binary current switch.

The + T and - T set pulses furnish the input to a flip-flop which controls the + set and - set sides, respectively. If the flip-flop is already in the + set condition, a succession of + T set pulses will maintain the set condition. The + set condition will persist until the pendulum angle decreases past zero to an angle sufficiently negative to enable the interrogator to produce a - T set pulse which will cause the binary current switch flip-flop to go to the - set condition. The outputs of the flip-flop control the two current switches. If the flip-flop is in a + set state, the + set output is applied to the base of a transistor which closes the path from the + 120 volt supply to the 16 PIP + T torquing coils. If the flip-flop is in the - set state, the path to the - T torquing coils is closed.

The outputs of the flip-flop also go to two separate "and" gates where they are "anded" with the data pulses. The data pulses consist of a train of 3 μsec, 3200 pps pulses timed to occur 2 μ sec after the leading edge of the switching pulse. This "anding" produces positive velocity pulses and negative velocity pulses. Each pulse represents an increment of velocity and is defined by the loop scale factor in terms of centimeters-per-second-per-pulse. The positive and negative pulses go to a forward-backward counter in the CMC.

2.6.2.4 Calibration Module. The calibration module (figure 2-39) compensates for the inductive load of the 16 PIP torque generator ducosyns and regulates the balance of the plus and minus torques. The calibration module consists of two load compensation networks in parallel with the torquing coils of the 16 PIP. The torquing coils, along with the compensation network, appear as a resistive load to the output of the binary current switch. A variable resistor regulates the amount of torque developed by the torquing coils. Adjustment of this resistor regulates precisely, and thereby balances, the amount of torque developed by the plus and minus torquing coils. This balancing insures that for a given torquing current an equal amount of torque will be developed in either direction. The odd numbered coils of the torque generator ducosyn are excited to develop a plus torque and the even numbered coils are excited to develop a minus torque.

The calibration module also includes a current sampling resistor in series with the torquing coils. Six volts is developed across this resistor due to the torquing current.

2.6.2.5 Constant Current Source. The constant current source maintains the current through the torquing coils of the torque generator ducosyn at 100 milliamperes. The constant current source contains a precision voltage reference and a differential amplifier. The precision voltage reference is supplied with regulated 28 volt dc, and through the use of precision circuits develops an accurate six volts for use as a reference. The six volts developed by the precision voltage reference is compared with the six volts developed across the current sampling resistor in the calibration module. This comparison is made by the dc differential amplifier. Any deviation of the current switch torquing current from 100 milliamperes will result in a change in the dc differential amplifier voltage output to return the torquing current to 100 milliamps. By accurately maintaining the current at this value the PIPA will maintain a scale factor of 5.85 cm/sec ΔV per pulse output.

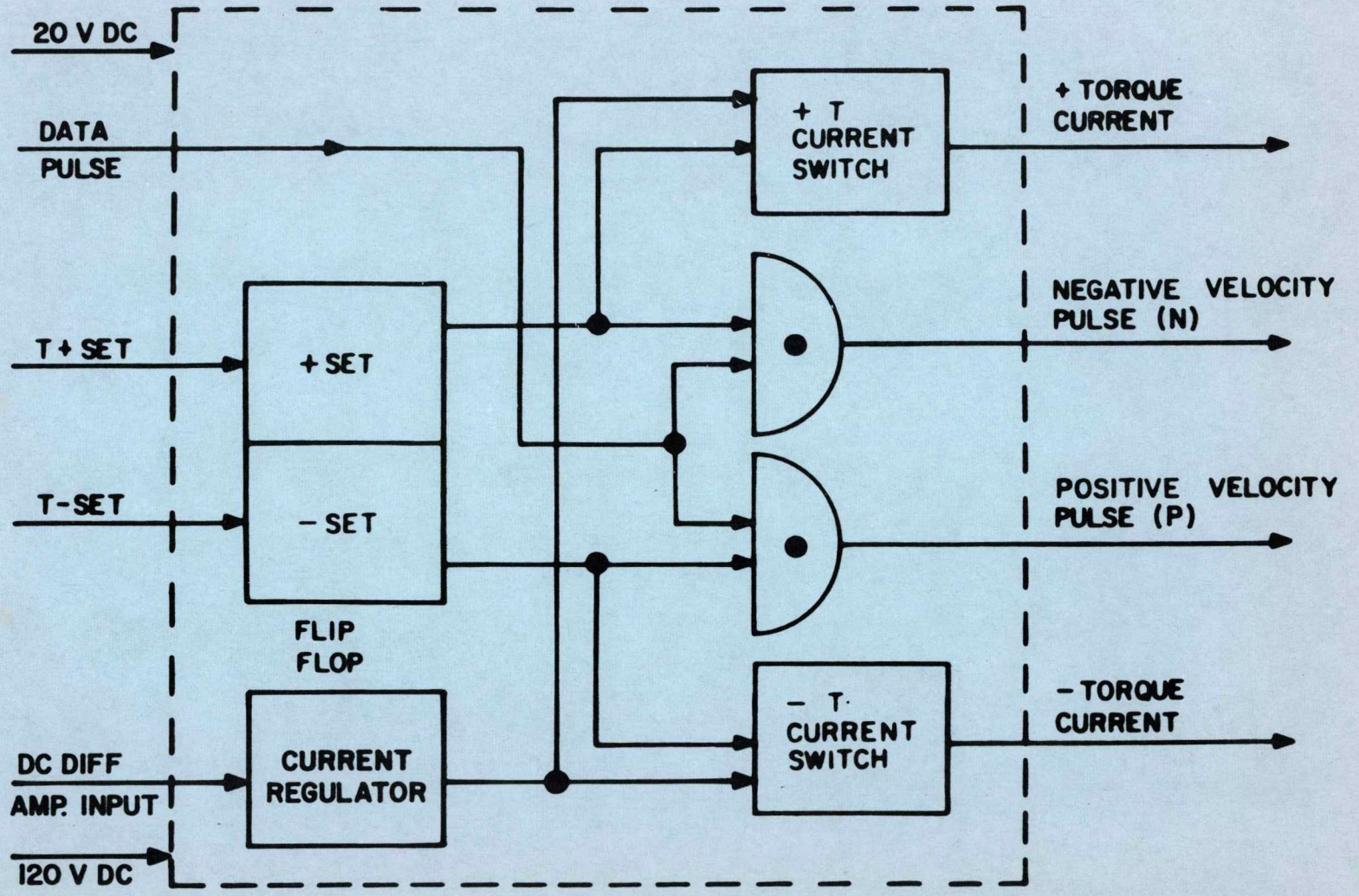


Figure 2-38. Binary Current Switch, Block Diagram

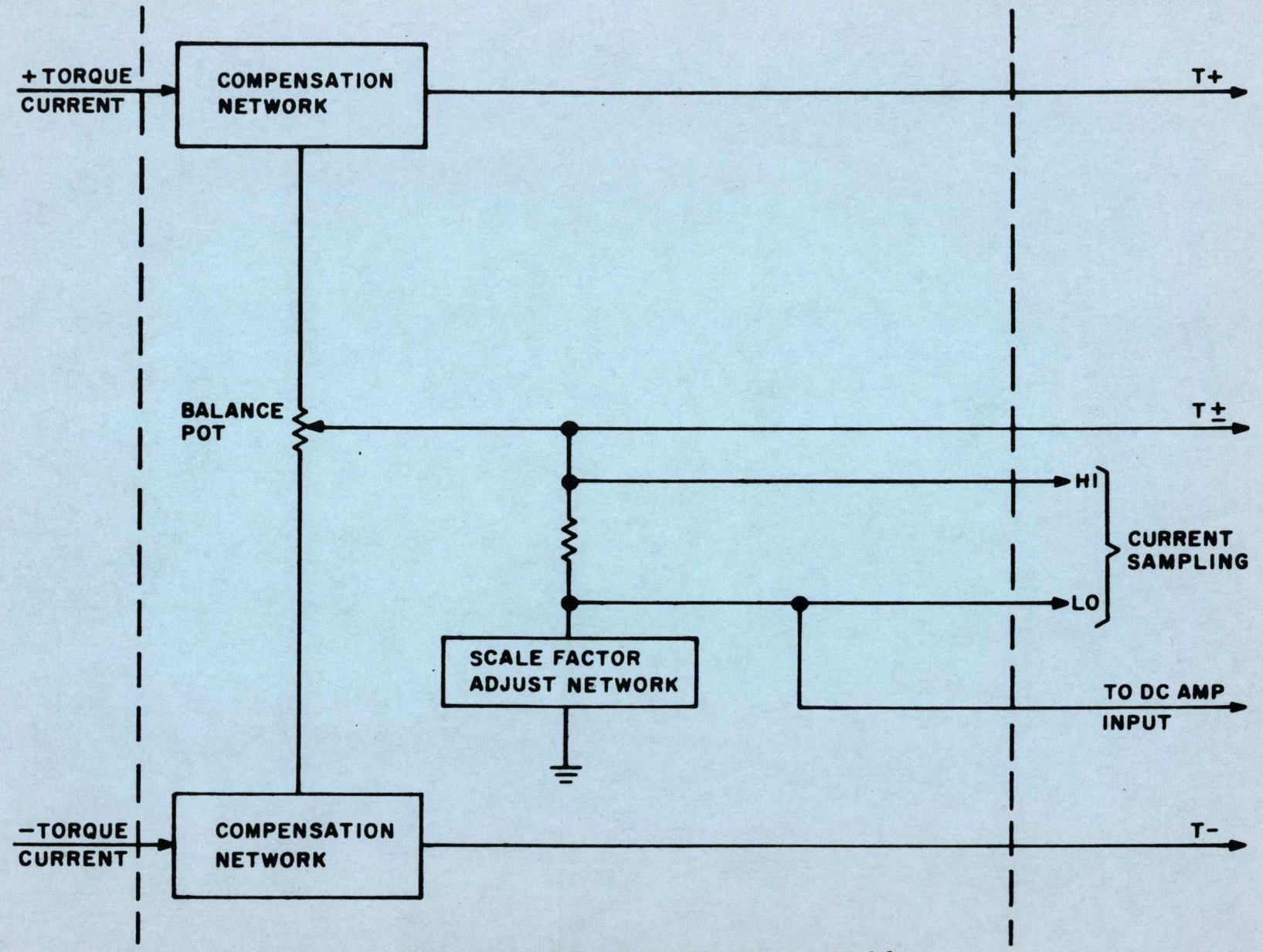


Figure 2-39. Block II PIPA Calibration Module

2.6.2.6 Forward-Backward Counter. A PIPA loop may be mechanized to operate in either of two major modes; the ternary or 3-state mode and the binary mode. In the ternary mode, the PIP is torqued only in the presence of an acceleration input, and when no input is present, the pendulum remains stationary at the null point. This mode, called a ternary mode, has 3 states: plus torque, minus torque and no torque applied. The ternary mode delivers 12 times more velocity resolution than the binary mode. In the Apollo program, the binary mode of operation has been chosen. In this mode, the pendulum is kept continually in motion because current is fed alternately to each torquer. This mode has poorer velocity resolution but can be capable of handling 12 times the maximum input acceleration of the ternary mode. In operation, the PIPA loop is able to handle inputs as high as ±19.1 g's.

The binary mode is further defined as a binary 3-3 mode. The 3-3 refers to the number of torque pulses applied during the pendulum oscillation. It is obvious that since the pendulum is kept constantly in motion, motion about the pendulum null point must be an oscillatory one. Due to the natural frequency of the loop of approximately 500 cps, the pendulum will oscillate at a submultiple of 3.2 kc which is nearest that frequency. This is 533-1/3 cps and results in 3 pulses to the binary current switch for each side of the pendulum cycle, hence 3-3.

If each of these pulses were sent to the computer processing circuitry, it is apparent that the computer would act on a constant train of incremental velocity data even though no velocity is being gained by the spacecraft. The purpose of forward-backward counter is to insure that the data processed, represents an actual gain in velocity and thereby avoid unnecessary processing by the CMC.

The forward-backward counter is located in the computer, however, its action is parallel or independent of the computer processing circuitry and only its output is processed by the CMC. The forward-backward counter is driven by the positive and negative pulses from the binary current switch. During operation of the PIPA loop with no acceleration input, the loop will operate at a rate of three positive pulses and then three negative pulses. The counter counts forward on the positive pulses and then backward on the negative pulses. The counter continues this operation and generates no ΔV pulses to the CMC. However, with an acceleration input to the 16 PIP, the loop no longer operates on the 3-3 ratio and the counter exceeds its capacity and provides ΔV pulses to the input circuitry of the CMC from the forward-backward counter.

SECTION III

COUPLING DATA UNIT

INTRODUCTION

The Coupling Data Unit (CDU) is a completely electronic device developed to replace the electro-mechanical coupling display units used on the Block I Series of Apollo G&N subsystems. See figure 3-1.

3.1 PURPOSE OF THE COUPLING DATA UNIT (CDU)

The CDU performs the following functions (see figure 3-2):

a. Analog to digital conversion of the IMU gimbal angles and optical subsystem trunnion and shaft angles.

b. Digital to analog conversion of computer derived data.

c. Controls the ISS modes of operation using discretes issued by the computer.

d. Contains failure detect circuitry for ISS and OSS CDU failure.

3.2 PHYSICAL DESCRIPTION OF THE CDU

The CDU sealed container contains modular packaged solid state electronics necessary to provide five completely separate CDU channels for use with the inner, middle and outer IMU gimbal resolvers and the shaft and trunnion resolvers of the optical subsystem.

Table 3-1 lists the 32 modules contained in the CDU and figure 3-3 illustrates the location of these modules within the CDU.

Table 3-1. CDU Modules

Module	Quantity
Quadrant select module	5
Coarse system module	3
Digital to analog converter module	5
Main summing amp and quadrature reject module	5
Error angle counter and logic module	5
Read counter module	5
Mode module	1
Interrogate module	1
Digital supply module	1
Digital mode module	1

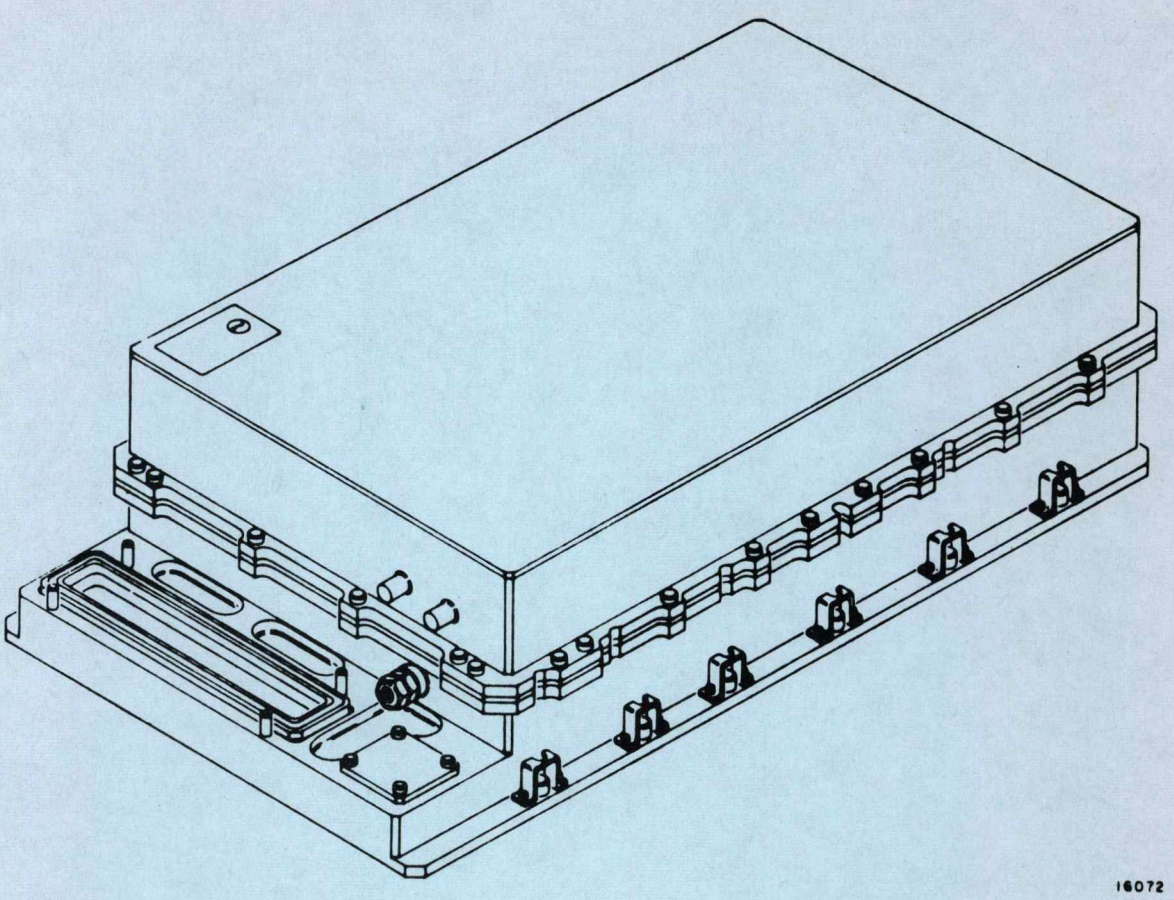


Figure 3-1. Coupling Data Unit

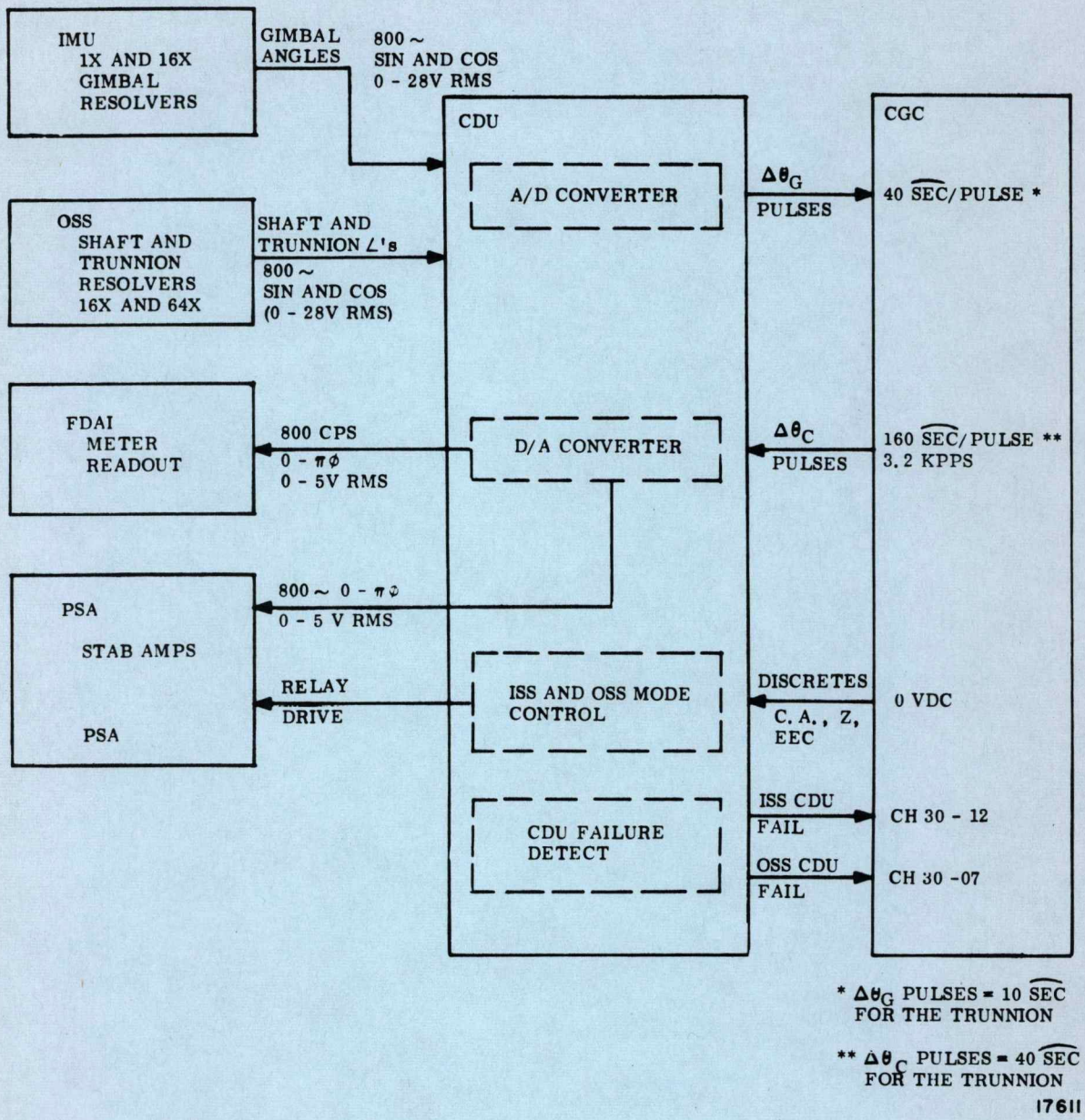


Figure 3-2. CDU Functions

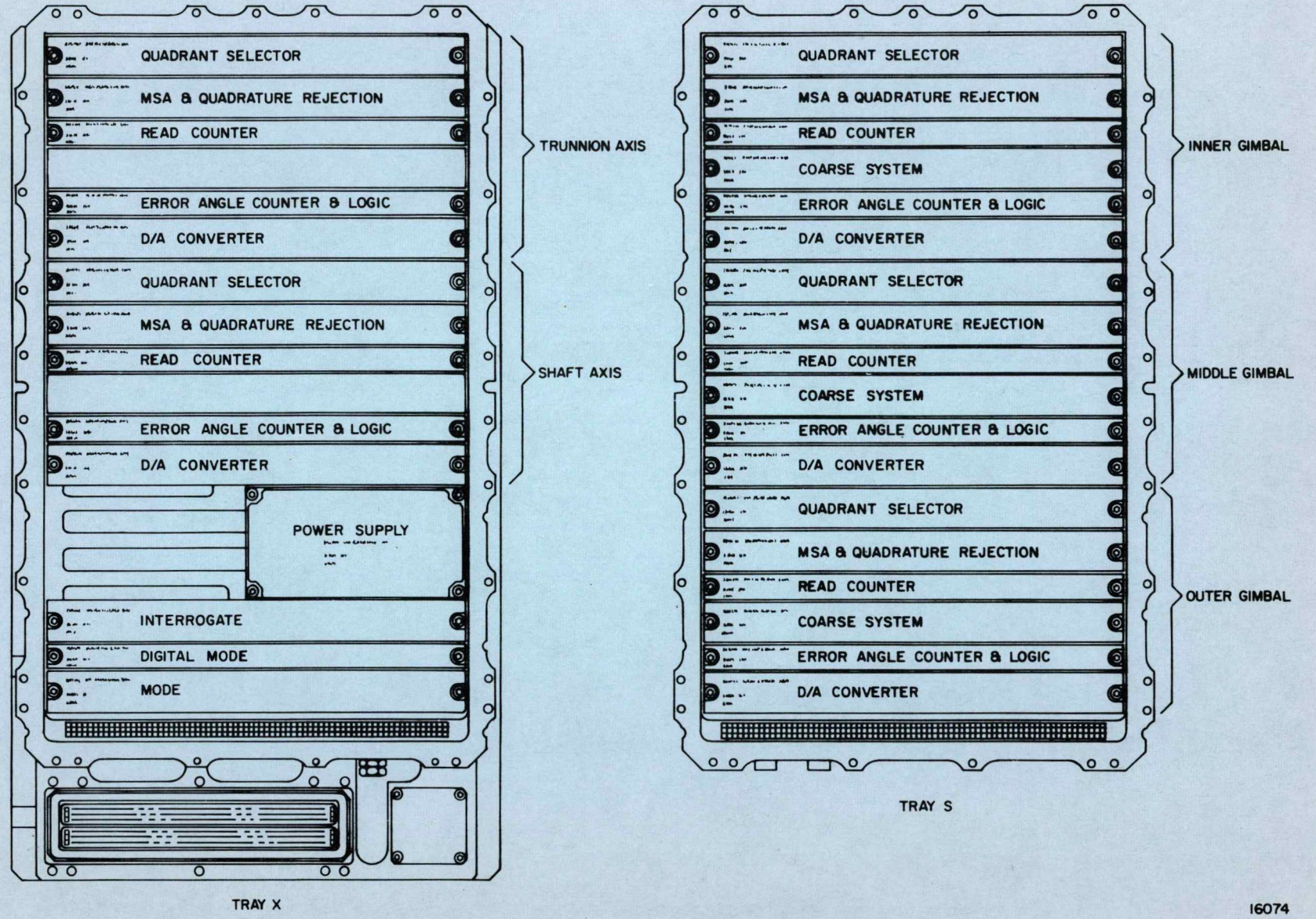


Figure 3-3. CDU Module Location

The mode, interrogate, digital mode and power supply modules are common to all 5 channels of the CDU.

The CDU (figure 3-1) is approximately 20 inches long, 11.3 inches wide and 5.5 inches high. The unit is mounted on a cold plate located below and to the left of the PSA in the lower equipment bay.

The CDU inputs required for normal operation include the following:

a. 28 vdc prime power.

b. 28 v ±1% 800 cps - ISS and OSS.

c. 3200 pps 7 v pulses - gimbal angle commands ($\Delta\theta_C$).

d. Mode control commands.

e. Sine θ and cosine θ (θ is gimbal angle).

f. Sine 16θ and cosine 16θ (θ is gimbal angle or optics shaft angle).

g. Sine 64θ and cosine 64θ (θ is the optics trunnion angle).

Under normal operating conditions, the CDU outputs include the following:

a. Read counter output - gimbal angle position ($\Delta\theta_G$).

b. IMU or optical subsystem coarse align (drive) signals.

c. Attitude error signals to the FDAI.

d. Pitch and yaw steering signals to the SPS

e. SIVB, pitch, yaw and roll steering signals.

The CDU is required to repeat gimbal angles under static conditions to ±59 arc seconds, and under dynamic conditions to ±59 arc seconds for gimbal driving rates up to 71^{o} per second.

3.3 CDU SINGLE CHANNEL FUNCTIONAL DESCRIPTION

The primary functions of the CDU are to convert analog information to digital, digital information to analog and to provide ISS mode control. The analog inputs consist of the 1X and 16X IMU gimbal resolvers and the 16X and 64X optics shaft and trunnion angle resolvers. The inputs to the CDU from the resolvers are a sine or cosine, 0 - 28V RMS (800 cps) signal. The output signal from the CDU to the computer is a serial pulse train with each pulse equivalent to 40 sec of gimbal movement and shaft movement of the optics. For the optics trunnion movement, each pulse equals 10 arc seconds of movement. See figure 3-1.

The 3.2 K pulse/sec trains that the computer sends to the CDU represent an angle with each pulse equal to 160 arc seconds of IMU gimbal movement, optics shaft movement, or each pulse is equal to 40 arc seconds of optics trunnion movement. The pulse trains from the computer are converted to an equivalent analog signal of 800 cps, 0 or $\pi\phi$, 0 to 5 V RMS, which is sent to the ISS, OSS, or the FDAI, depending on the mode of operation selected.

To control the ISS and OSS modes of operation, computer issued discretes are sent to the CDU. These discretes are used within the CDU to drive the counters to zero and to enable the error counter at the proper time. The Coarse Align discrete is buffered within the CDU and then used to provide a ground path for energizing the coarse align relay located in the PSA.

3.3.1 ANALOG TO DIGITAL CONVERSION. The functional block diagram shown in figure 3-4 shows a single analog to digital and digital to analog conversion channel in the CDU. There are three similar channels for the inner, middle and outer IMU gimbals, and two for the optics shaft and trunnion angles.

The analog to digital conversion will be investigated first. This conversion is accomplished by solving the trogonometric identity:

$$\pm \text{Sine}(\theta - \Psi) = \pm \text{Sine}\,\theta\ \text{Cosine}\,\Psi \mp \text{Cosine}\,\theta\ \text{Sine}\,\Psi$$

where: θ = gimbal angle.

Ψ = angle in the read counter.

When the incremental values of Ψ are equal to θ, the equation equals zero and the system is considered nulled.

The CDU inputs from the IMU and optical sensor are the sine and cosine of the 1 and 16 speed gimbal angle resolvers. These inputs are phase shifted and attenuated by the switching logic and coarse fine mixing block (see figure 3-4). The signals are mixed and used as an input to an error detector circuit. The error detector monitors the phase and amplitude of the 800 cps error output of the mixing and attenuation circuit. The phase of the signal determines whether the digital signal to be generated is positive or negative. The amplitude of the mixed signal determines what rate the digital pulses, equivalent to 20 arc seconds of gimbal displacement, shall be generated, 800 pps or 12.8 kpps. The digital pulse train, either 12.8 or .8 kpps, and either up or down, is the input to a 16 bit binary read counter.

The read counter with binary stages designated as 2^0 to 2^{15} counts the pulse train generated by the rate select and up down logic circuitry. The 2^0 (2^{zero}) or least significant bit output is transmitted to the CMC as a $\Delta\theta_G$ gimbal angle change equivalent to a 40 arc second gimbal angle change. This is the only information pertaining to gimbal angles or angular changes transmitted from the CDU to the CMC. During the coarse align mode of operation of the ISS or the optical subsystem, $\Delta\theta_G$ of 160 arc seconds per pulse is transmitted from the 2^2 output stage to the error counter of the CDU. These two stages plus the remainder of the read counter permits the accumulation of the gimbal angle with the least significant bit being equivalent to 20 arc seconds of gimbal angle and the most significant bit (2^{15}) being equivalent to 180^o of gimbal displacement. The read counter can accumulate a total gimbal angle of $359^o59'40''$. The contents of the read counter are not accessible for readout or display at any time.

A/D

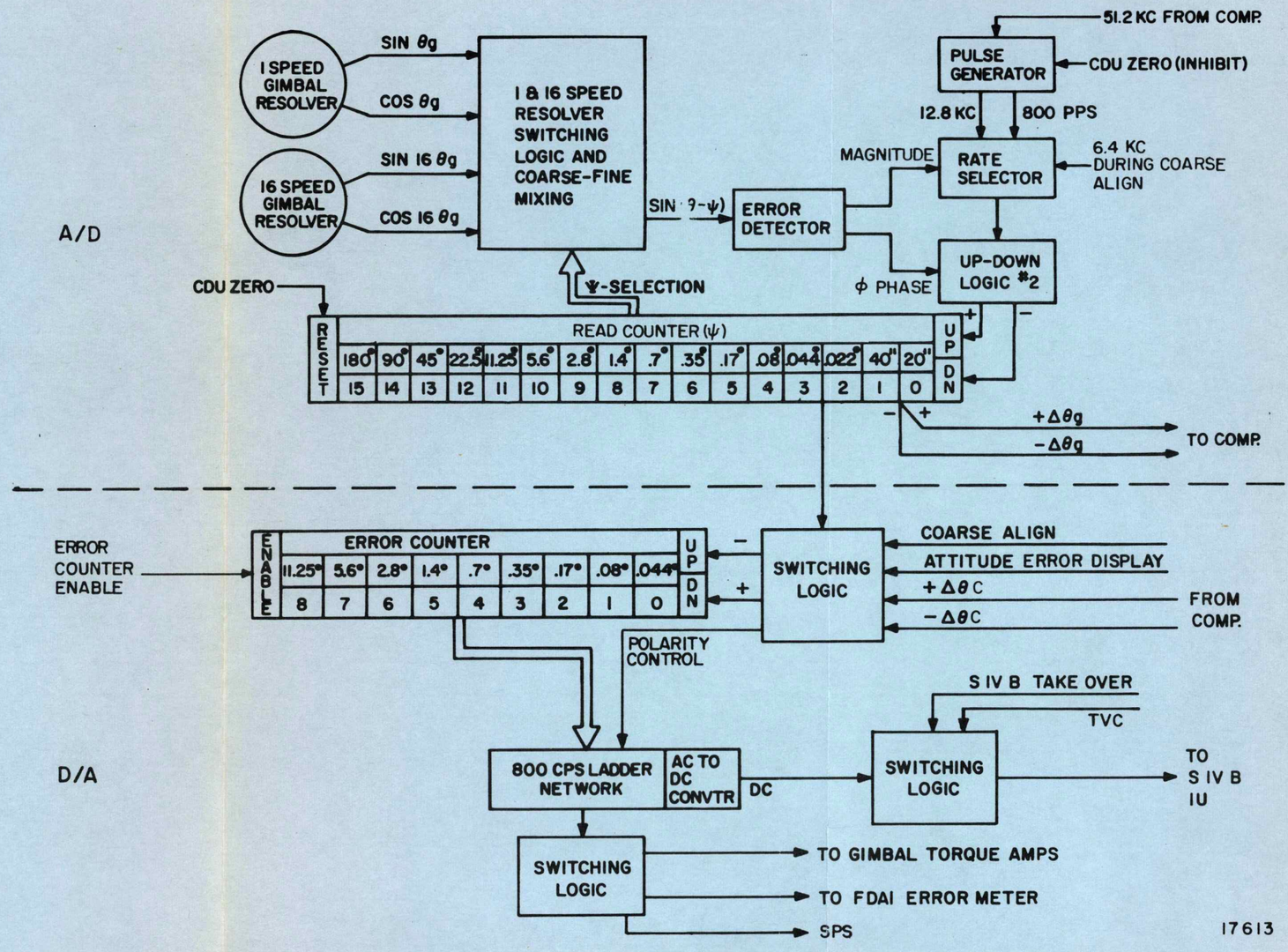


Figure 3-4. CDU Functional Block Diagram

The primary function of the read counter is to provide the incremental Ψ angles to be used in the coarse fine mixing and switching logic for the mechanization of the trigonometric identity sin $(\theta - \Psi)$. When the read counter has accumulated a value Ψ equal to the angle θ, the input to the error detector will be nulled and the read counter will not receive additional input pulses until a change in the gimbal angle again occurs. During certain ISS modes of operation the read counter receives a reset pulse to cause the counter to be set to zero. This command is generally given when the system is energized to allow the gimbals and the read counter to come into agreement with each other prior to utilizing the gimbal angle information stored in the computer.

3.3.2 DIGITAL TO ANALOG CONVERSION. The error counter, a 9 bit (2^0 to 2^8) counter, is used primarily in the conversion of digital data to its analog equivalent. With only one exception, coarse align, the error counter is operated solely from CMC input data. Each pulse into the error counter, whether from the CMC or from the read counter is equivalent to 160 arc seconds of gimbal angle displacement or attitude error. The counter when commanded must be enabled by an error counter enable discrete from the CMC. When attitude error is to be displayed the counter accumulates the pulse train from the computer and maintains that value until the computer either counts the value down or removes the error counter enable discrete. In the coarse align mode of operation the read counter, as it accumulates increasing gimbal angles due to a coarse repositioning of the gimbal, can cause the contents of the error counter to decrease toward zero.

The only output from the error counter is a switching action. When the binary stages of the error counter are switched, switches in the 800 cps ladder network of the digital to analog converter are opened or closed. As the ladder switches are closed an 800 cps analog signal, the amplitude of which is proportional to the contents of the error counter and whose phase is determined by the positive or negative value of the $\Delta\theta_C$ pulses, is generated in the DAC. If the CMC moding control has selected a coarse align or attitude error display mode, the 800 cps signal is used without conversion to dc. If the error counter contents are indicative of a computer calculated steering signal, the 800 cps, 0 or π phase, signal is converted from ac to dc for use as steering input to the SPS gimbal servo amplifiers or the SIVB instrument unit.

The functional block diagram (figure 3-4) is intended solely to illustrate the functional operation of the CDU. Some of the blocks shown can be related directly to the actual operation by title and operation, but the remainder are for illustration purposes only.

3.3.3 ISS AND OSS MODE CONTROL. The CDU receives the ISS and OSS moding discretes from the computer. The discretes are:

a. ISS CDU Zero

b. ISS Error Counter Enable

c. OSS CDU Zero

d. OSS Error Counter Enable

e. CDU Zero Drive

f. ISS Coarse Align

g. ISS Coarse Align

The CDU zero discretes are used within the CDU to drive the counters in the CDU to zero during the IMU Turn On mode when the IMU gimbals are also being driven to a zero angle position. The error counter enable discretes are used within the CDU to enable the error counter during the Coarse Align mode and attitude error display mode of operation. The ISS coarse align discrete is buffered within the CDU and provides a ground path to the coarse align relay in the PSA to energize this relay during the Coarse Align mode of operation.

3.3.4 CDU FAIL DETECT. Both the ISS CDU failure detection and the RR CDU failure detection perform in the same manner. Therefore, only the ISS CDU failure detection will be discussed.

The coarse error (1X resolver outputs) and the fine error (16X resolver outputs) from the inner (I), middle (M), and outer (O) gimbals are used to determine if the resolvers are nulling as they should. The detection is accomplished by rectifying the 800 cps resolver error signals and comparing them with a predetermined voltage specification. When one of the coarse signals exceeds 2.5 vrms or one of the fine signals exceeds 1 vrms an ISS CDU fail is generated.

Special detection circuits are used to detect the limit cycling of the up line in the read counter when the CDU read counter contains the gimbal angle. In this loop as in any servo loop when the loop is nulled a slight oscillation occurs around the null. The error detect circuit recoginzes the changing phases of the signal around null and causes an up line energization or a down line energization to the read counter. Under normal operation this limit cycle is expected to be less than 250 cps. If the limit cycle exeeeds 250 cps, and ISS CDU fail is generated. The limit cycle is checked for the I, M, and O gimbals.

Another "OR" gate in the CDU failure detection section is used as a low level detect circuit. The signals cos $(\theta - \Psi)$ are checked to determine whether their levels drop below 2.5v (rms). If any of these three signals drops below the set level, or the mode module 14 vdc supply drops below 10 vdc the OR gate will send a fail indication to the computer.

3.4 TIMING INTERFACE

In the previous section, the CDU interfaces with the computer, the ISS and the OSS were discussed. In order for the CDU to function as an interface between the computer and the ISS and OSS, synchronization between the timing references used in the CSS, OSS and ISS subsystems is required.

The computer timing is based on a 51.2 KPPS signal and the ISS and OSS timing is based on an 800 cps signal. The CDU uses these two basic timing references to generate its internal timing control and to generate timing pulses which synchronize the computer timing with the ISS and OSS timing.

3.4.1 COMPUTER REFERENCE. The logic circuitry within the CDU generates six pulse trains and two square waves based on the 51.2 kpps timing signal from the computer. Table 3-2 lists these computer referenced timing signals used in the CDU. Figure 3-5 is a related timing diagram.

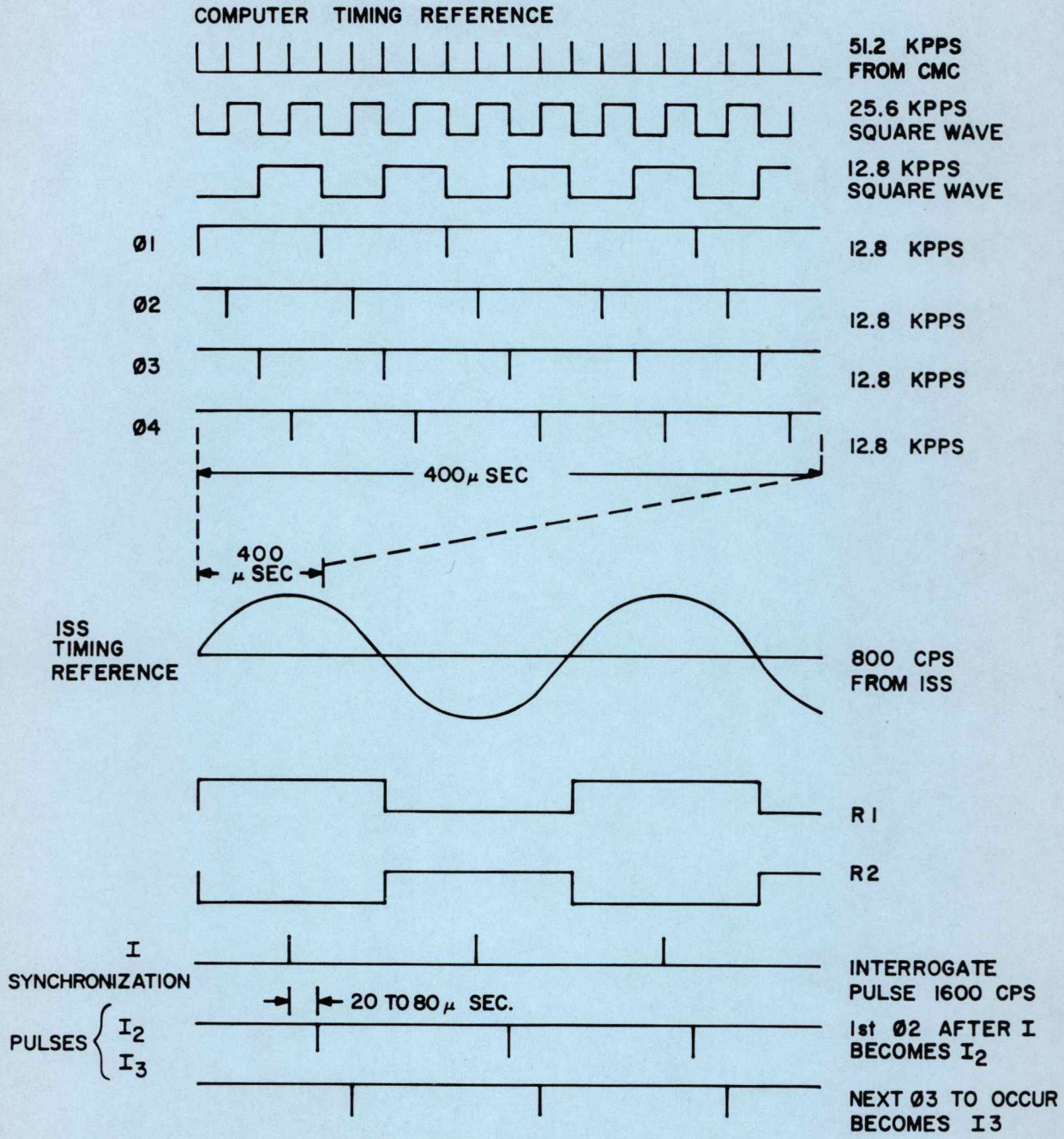


Figure 3-5. CMC and ISS Timing Synchronization

Table 3-2. Computer Referenced Timing Signals

Designation	Frequency	Waveform
	25.6 kpps	Square Wave
	12.8 kpps	Square Wave
$\phi 1$	12.8 kpps	3 μ sec pulse
$\phi 2$	12.8 kpps	3 μ sec pulse
$\phi 3$	12.8 kpps	3 μ sec pulse
$\phi 4$	12.8 kpps	3 μ sec pulse
	6.4 kpps	3 μ sec pulse
	800 kpps	3 μ sec pulse

The 4 VDC power supply in the CDU requires an input synchronized with the computer 51.2 kpps. To meet the power supply requirements, a 25.6 k pulse/sec train is generated by the 25.6 kpps generator. This pulse train is generated by routing the $\phi 2$ and ϕ 4 pulse trains through an OR gate.

The $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$ pulse trains are generated by the clock and decoder logic. These pulse trains are generated by dividing the 51.2 kpps clock pulse train from the computer by four and "and"ing appropriate signals. These pulse trains are used throughout the CDU for synchronization and control. The interval between $\phi 1$ pulses is approximately 80 microseconds, divided into four intervals by $\phi 2$, $\phi 3$ and $\phi 4$. Each interval is, therefore, approximately 20 microseconds.

The clock and decoder logic also contains a two stage binary counter which is driven by the 51.2 kpps clock pulse train from the computer. The 1st stage output is a 25.6 kpps square wave and the 2nd stage output is a 12.8 kpps square wave that is applied to the decoder logic.

The countdown circuit generates an 800 pps $\phi 4$ pulse train used in the read select logic circuit to develop the low rate of read counter incrementing pulses. The countdown circuit also generates a 6.4 kpps $\phi 4$ pulse train, used in place of the normal 12.8 kpps $\phi 4$ pulse train, during the coarse align mode to develop a lower rate of read counter incrementing pulses.

3.4.2 ISS REFERENCE. The logic circuitry within the CDU generates one pulse train and two square waves based on the 800 cps timing signal from the ISS.

Table 3-3 lists the ISS referenced timing signals used in the CDU and figure 3-5 is a related timing diagram.

Table 3-3. ISS Referenced Timing Signals

Designation	Frequency	Waveform
R1	800 cps	Square Wave
R2	800 cps	Square Wave
Interrogate Pulse	1,600 pps	3μ sec pulse

The ISS Reference Generator in the Interrogate Module produces an 800 cps square wave (R_1) which is in phase with the 800 cps sine wave timing signal from the ISS. R_1 is used in the Inner, Middle and Outer Error Counter and Logic Modules and the Digital Mode Module. R_2 is generated in the Error Counter and Logic Modules by inverting R_1.

The ISS Interrogate Generator in the Interrogate Module produces the 3 μ sec., 1600 pps interrogate pulse. One interrogate pulse is issued each time the 800 cps sine wave from the ISS reaches a positive or negative maximum value. Therefore, the interrogate pulse is in phase with the twice the frequency of the ISS timing reference.

3.4.3 SYNCHRONIZATION LINK. The logic circuitry within the CDU Digital Mode Module generates the 1600 cps pulse trains (I_2 and I_3) which are the synchronization links between the ISS and computer timing.

The I_2, I_3 interrogate generator is used to produce the two synchronization pulses; one coincident with the $\phi 2$ timing pulse and the other coincident with the $\phi 3$ timing pulse. The ISS interrogate pulse (I) can occur at any time with respect to the 51.2 kpps CMC clock pulses. The synchronization link between the ISS interrogate pulses and the CMC clock pulses is provided by generating two additional interrogate pulses, I_2 and I_3, at the $\phi 2$ and $\phi 3$ time, respectively, after each occurrence of an I pulse. I_2 and I_3 are then used by other logic circuits for synchronization and control purposes. I_2 will follow I within approximately 20 to 80 microseconds, and I_3 will follow I_2 by approximately 20 microseconds. The logic gate will be reset by $\phi 4$ prohibiting the generation of another I_2 or I_3 until the next occurrence of I. The frequency of I_2 and I_3 will be 1600 cps compared to the 12.8 kpps frequency of $\phi 2$ and $\phi 3$. See figure 3-5.

The synchronization is accomplished by having I_2 and I_3 occur at the frequency of the ISS reference and coincident with the time of occurrence of the $\phi 2$ and $\phi 3$ pulses of the computer reference.

3.5 CDU MODULE INTERCONNECT (SINGLE CHANNEL)

In section 3.2, a description was given of the basic functions performed by the CDU and figure 3-4, CDU Functional Block Diagram, was used to show the signal flow within the CDU. In this section a simplified block diagram of one of the five CDU channels, figure 3-6, will be used to show the actual operation of the CDU, and to relate the operations performed with the modules in which they occur.

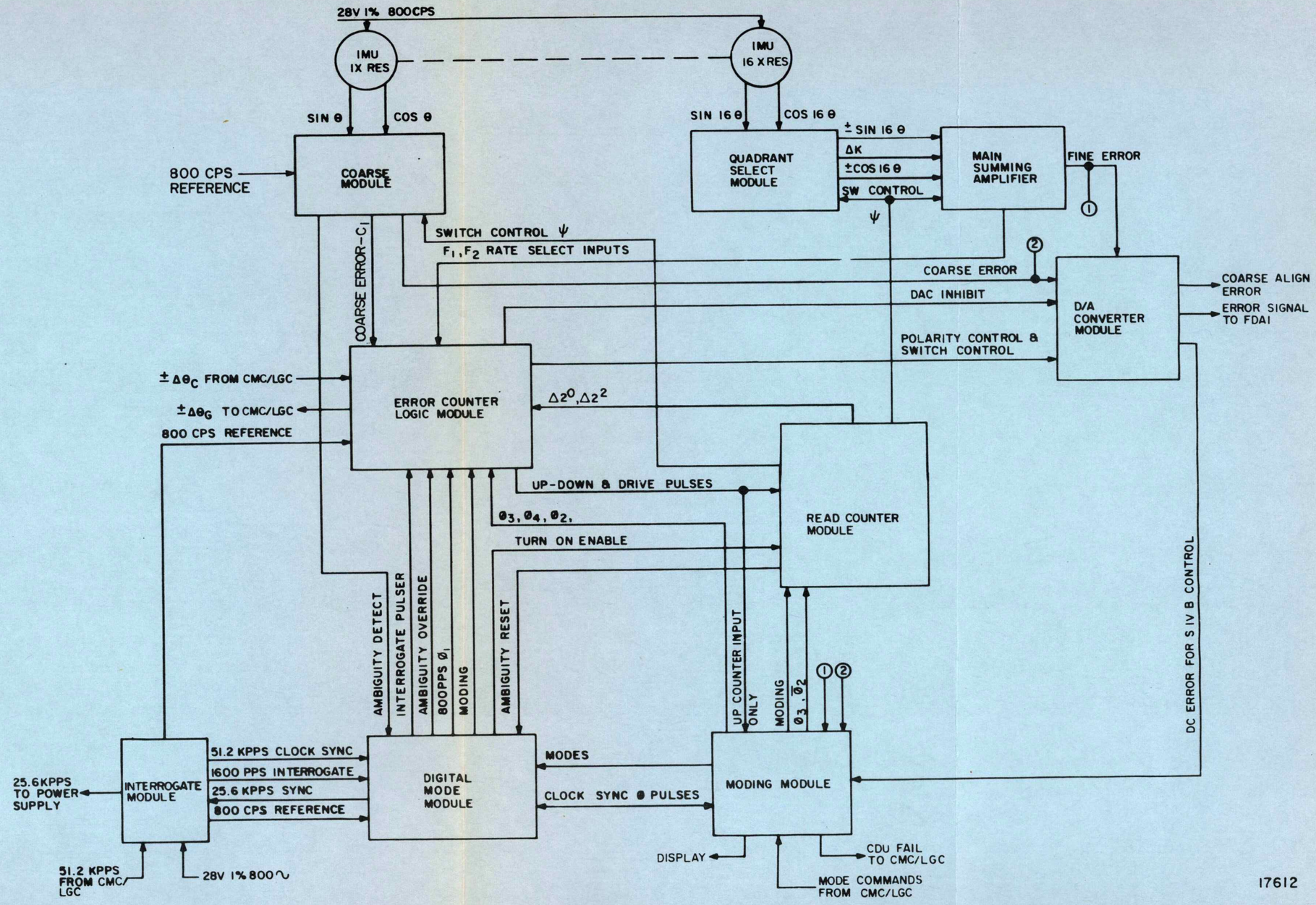


Figure 3-6. Coupling Data Unit (Simplified Block Diagram)

3.5.1 ANALOG TO DIGITAL CONVERSION. The analog signal inputs from the IMU are outputs of the 1X and 16X gimbal resolvers located on the Inner, Middle and Outer IMU gimbals. The resolver outputs represent the sine and cosine of the IMU gimbal angle (θ) and 16 times θ. This is an 800 cps 0 to 28 V RMS signal whose magnitude is a function of the sin or cos of θ or 16θ. The sin θ and cos θ are routed to the coarse module and the sin 16θ and cos 16θ are routed to the Quadrant Select Module.

In the Coarse Module, the sin θ and cos θ are phase shifted and attenuated by the switching logic. Selection of the proper phase for the sin θ and cos θ and the proper attenuation representing the cos Ψ and the sin Ψ, where Ψ is the gimbal angle as indicated by the read counter, will result in the mechanization of the trigonometric equation,

$$\pm \sin(\theta - \Psi) = \pm \sin\theta \cos\Psi + \cos\theta \sin\Psi.$$

In the event that the angular difference between θ and Ψ is greater than approximately 5^{o} a coarse error signal (C_1) will be generated in the coarse module and sent to the coarse fine mix circuitry of the error counter and logic module.

In the quadrant select module and main summing amplifier module sin 16θ and cos 16θ are compared with Ψ in the above trigonometric identity and will result in the generation of fine error signals F_2 and F_1. F_2 will be generated whenever the angular difference between θ and Ψ is greater than approximately $.1^{o}$. F_1 will be generated whenever the difference is greater than approximately 20 sec. Error signals F_2 and F_1 are also routed to the coarse fine mix circuitry of the error counter and logic module.

The phase of the error signals is compared with an in phase and out of phase reference (R_1 and R_2) in the up-down logic and the result of this comparison determines whether the read counter will be counted up or down.

The presence of the error signals C_1, F_2 and F_1 will determine the rate at which the digital pulse will be generated and sent to the read counter. With C_1 or F_2 present the rate at which the read counter will be pulsed is 12.8 kpps. With F_1 present the rate will be 800 pps.

The read counter then is counted up or down depending on the direction of IMU gimbal rotation, until the magnitude of the read counter (Ψ) is equal to the gimbal angle (θ). The trigonometric identity sin ($\theta - \Psi$) is then equal to zero and the loop is considered nulled.

3.5.2 DIGITAL TO ANALOG CONVERSION. The digital signal input from the computer is a 3.2 kpps pulse train representing polarity and magnitude of gimbal angle displacement. In the Coarse Align mode, this gimbal angle displacement represents the direction and amount the computer desires the gimbals to be driven from their present location. In the attitude error display mode, this gimbal angle displacement represents deviations of spacecraft position as indicated by the gimbal angle resolvers.

The computer pulse train ($\pm \Delta\theta_C$) is routed to the error counter and logic module where it is synchronized with $\phi 2$ time and then used to pulse the error counter. The polarity of the $\Delta\theta_C$ pulses is used to control the phase 0 or π of the 800 cps ladder network in the DA converter module. The ladder network of the DAC is controlled by the binary stages of the error counter. To drive the error counter each pulse from the computer equals 160 arc seconds. Each bit from the binary counter equals 13.2 MV RMS or dc in the ladder network. The output of the DAC is sent to the stabilization loop amplifier located in the PSA, when in the coarse align mode and to the FDAI when in the attitude error display mode of operation. The DAC output can also be converted to dc and sent to the SPS gimbal servo amplifiers or the SIVB instrument unit.

When the ISS is in the Coarse Align mode of operation, a feedback loop to the computer and the CDU error counter is established.

The analog signal representing a desired gimbal angle position introduced into stabilization loop amplifier will result in the gimbal torque motors rotating the gimbals a prescribed amount. This gimbal rotation will be detected by the 1X and 16X resolvers resulting in an analog input to the CDU coarse module and quadrant select module. This analog input results in the counting up or down of the read counter. As the read counter is counted up or down, depending on the direction of gimbal angle change, the output of the 1st stage counter flip flop ($\Delta 2^0$) will be sent to the computer to register the gimbal angle changes ($\pm\Delta\theta_G$) and the output of the 3rd stage counter flip flop ($\Delta 2^2$) will be sent to the error counter logic module to decrement the error counter. When the desired gimbal angle (θ) has been reached, the read counter angle (Ψ) will be equal to it and the error counter will again be at zero.

When the contents of the error counter are used to display attitude error, the counter accumulates the pulse train from the computer and maintains that value until the computer either counts down the value or the error counter enable discrete is removed. During this mode of operation, there is no feedback loop between the read counter and error counter.

3.6 CDU COARSE MODULE

The coarse modules of the CDU perform part of the analog to digital conversion discussed in sections 3.3 and 3.5.

The coarse module inputs include:

a. 28 v sine θ.

b. 28 v cos θ.

c. 28 v 800 cps 1% reference.

d. 28 vdc.

e. Twelve switch commands designated DC1 through DC12.

The module outputs include:

a. An 800 cps coarse error signal to a test point, to the DAC, and to the monitoring circuitry.

b. A coarse ternary level signal C1.

c. An 800 cps signal for ambiguity detect (A_d).

d. IMU cage error signal.

3.6.1 THEORY OF OPERATION. It should be recalled from the functional description of the CDU that the circuitry in the CDU is designed to solve the trigonometric equation

$$\pm \sin(\theta - \Psi) = \pm \sin\theta \cos\Psi \mp \cos\theta \sin\Psi$$

where θ is the gimbal angle and Ψ is an incremental angle generated in the read counter of the CDU.

The function of the coarse module is to generate a coarse error signal which results from the comparison of θ and Ψ. The coarse module has been mechanized such that the actual equation used for the comparison of θ and Ψ is:

$$\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi$$

where K is the constant based on the 800 cps reference input, and the sign of the factors in the equation are determined by selection of an in phase or out of phase signal. (See figure 3-8.) The coarse error signal (C_1) is the 800 cps, 0 or $\pi\phi$ output of the Schmitt trigger error detector. C_1 is in phase with the reference when $\Psi > \theta$ and $\pi\phi$ when $\Psi < \theta$, and is generated only when the difference between Ψ and θ is greater than approximately 5^o.

Figure 3-7 illustrates the relationship of the mechanical angles of the gimbals, the read counter bit positions associated with the mechanical angles, and the coarse fine switching associated with each of the read counter bits. It can be noted that bits 2^0 through 2^{11} are associated with fine switching and 2^9 through 2^{15} are associated with coarse switching. The overlap 2^9, 2^{10}, 2^{11} that exists allows a smooth transition from coarse control to fine control. It can also be seen from the diagram that the coarse switching control can only increment the angle Ψ in the equations to a value of 2.8^o. The angles in the coarse switch blocks are mechanical angles of the 1X resolver and the angles of the fine switch blocks are equivalent to the mechanical angle through which a 16X resolver turns. It can be seen that 180^o mechanical angle of the 16X resolver is equal to 11.25^o of mechanical angle for the 1X resolver. It should be remembered, however, that the resolvers on the IMU are not geared but the multispeed system is accomplished by the wiring of the resolver.

A functional block diagram of the coarse module is shown in figure 3-8. The analog inputs to the module, 28 v sin θ, 28 v cos θ, and 28 v 800 cps are transformer-coupled to the resistor attenuation circuits. The maximum output from the transformer secondaries, high to center tap, is 5 v rms, thereby limiting the maximum input to the attenuation circuits to 5 volts times the sine or consine of the gimbal angle. A two-phase output is always available from each of the transformers.

An example of the signals available into the switching circuits is in order. Suppose the gimbal angle is $+30^o$ the transformer outputs are:

5 v rms sin 30^o = 2.5 v rms

5 v rms cos 30^o = 4.33 v rms

The center-tapped secondary of the transformer gives both an in-phase and an out-of-phase signal of equal amplitudes. These signals are used as inputs to two transistorized switches as shown in figure 3-9. A detailed diagram of one switch (S1) is shown in figure 3-9a.

Switch S1 of figure 3-9 consists of a transistor driver, a Q1 of figure 3-9, and the series switch Q2. When the logic equation, given in 3-9b, for DC1 is not satisfied, DC1 is at a logic 0 level (+4 vdc) allowing Q1 to conduct grounding the base of Q2. Switch Q2 will be cut off preventing the transformer output from reaching the attenuation resistor labeled cos 22.5^o. When DC1 becomes a logic 1 switch driver Q1 is cut off biasing Q2 into conduction allowing an ac path to be completed from the high side of the transformer through the transistor through the attenuation circuit to ground completing the current path. All of the switches (S1 through S12) of the coarse module operate in an identical manner but may have different values of attenuation resistors in their loads.

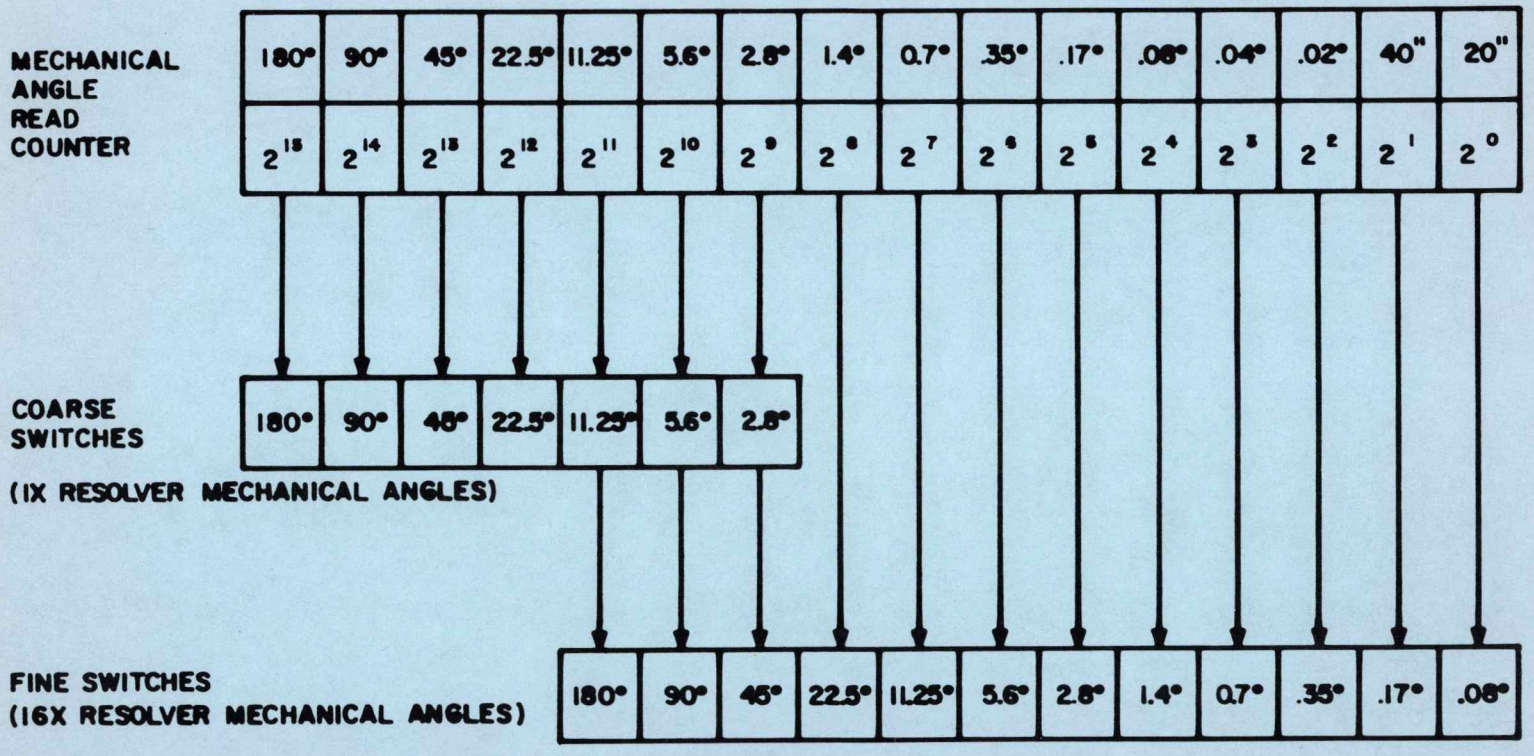


Figure 3-7. Read Counter Relationship to Coarse Fine Switching

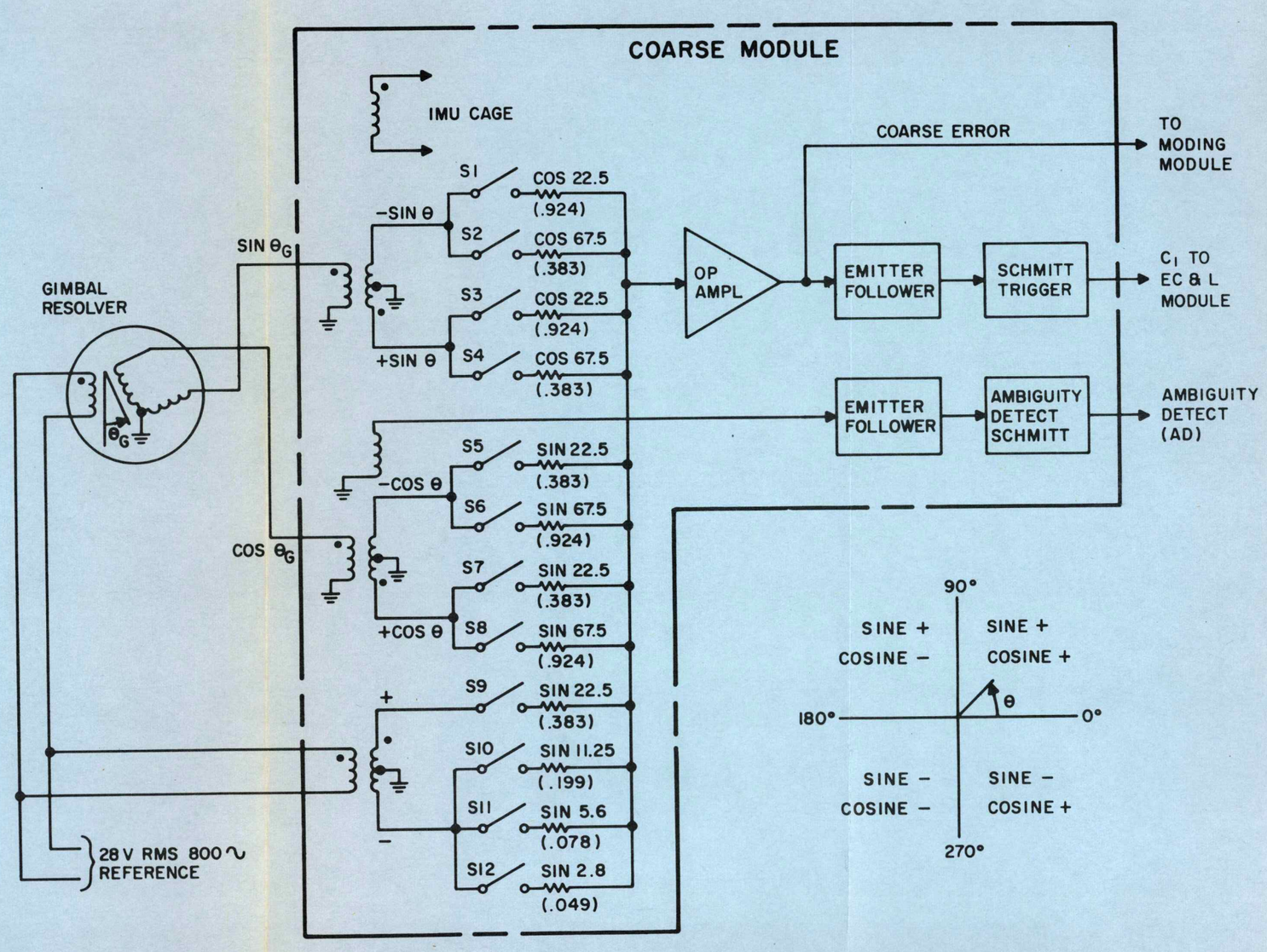
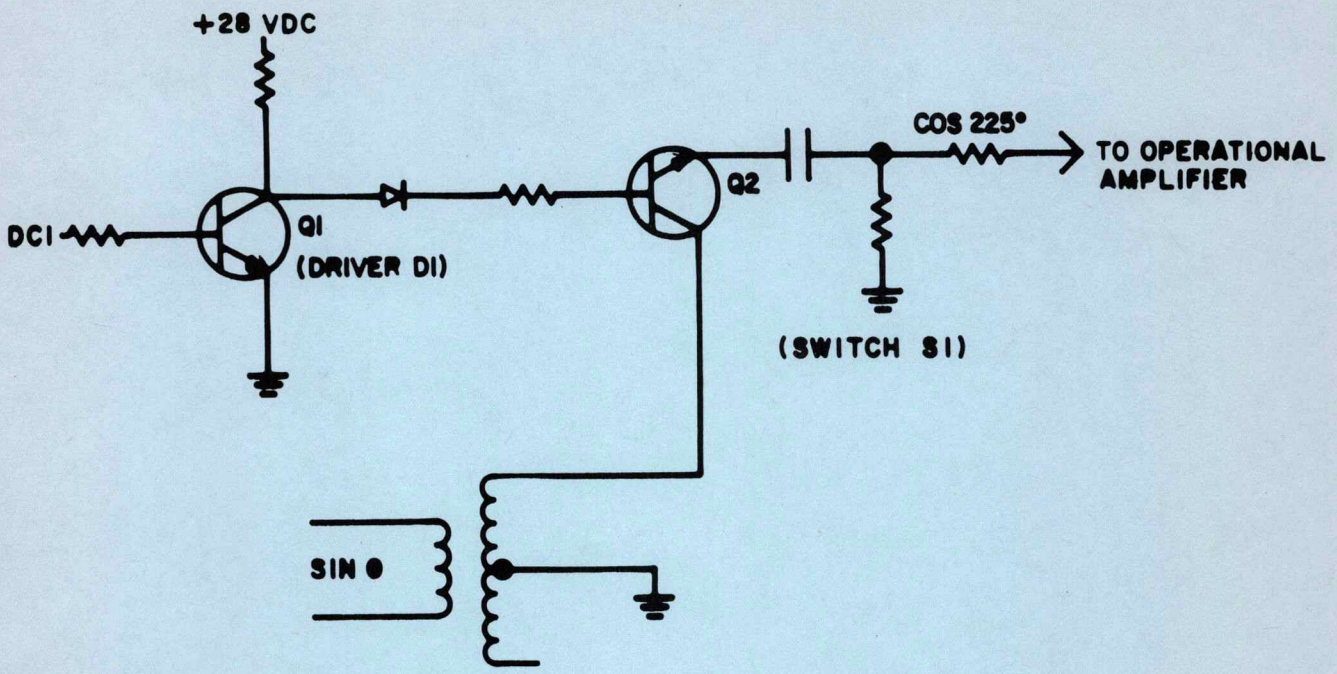


Figure 3-8. CDU Coarse Module Block Diagram



(a) S1 Switch Circuit

$DC1 = \overline{2^{15}}\ 2^{14}\ 2^{13} + 2^{15}\ \overline{2^{14}}\ \overline{2^{13}}$

$DC2 = \overline{2^{15}}\ 2^{14}\ \overline{2^{13}} + 2^{15}\ \overline{2^{14}}\ 2^{13}$

$DC3 = 2^{15}\ 2^{14}\ 2^{13} + \overline{2^{15}}\ \overline{2^{14}}\ \overline{2^{13}}$

$DC4 = \overline{2^{15}}\ \overline{2^{14}}\ 2^{13} + 2^{15}\ 2^{14}\ \overline{2^{13}}$

$DC5 = \overline{2^{15}}\ (2^{14}\ 2^{13} + \overline{2^{14}}\ \overline{2^{13}})$

$DC6 = \overline{2^{15}}\ (\overline{2^{14}}\ 2^{13} + 2^{14}\ \overline{2^{13}})$

$DC7 = 2^{15}\ (2^{14}\ 2^{13} + \overline{2^{14}}\ \overline{2^{13}})$

$DC8 = 2^{15}\ (\overline{2^{14}}\ 2^{13} + 2^{14}\ \overline{2^{13}})$

$DC9 = \overline{2^{12}}$

$DC10 = 2^{11}$

$DC11 = 2^{10}$

$DC12 = 2^{9}$

2^n = n refers to bit in read counter

(b) Coarse Switch Logic Equations

Figure 3-9. Coarse Module Switching Circuit And Logic

In the mechanization of the equation $\sin(\theta - \Psi) = \sin\theta \cos\Psi + \cos\theta \sin\Psi + K \sin\Psi$ a subtraction process is accomplished by proper selection of in phase and out of phase signals available at the transformer outputs. The subtraction is done at the summing input to the operational amplifier in figure 3-8. Figure 3-8 also shows the phase relationship of the sine and cosine of the 1X resolver output with respect to the reference voltage. The sine and cosine signals of the 1X resolver are attenuated by a value proportional to the cosine or sine, respectively, of an indication incremental angle Ψ. The attenuation values chosen are $\pm \sin 22.5^{o}$, $\pm \sin 67.5^{o}$ for the cosine θ signal attenuation and $\pm \cos 22.5^{o}$, $\pm \cos 67.5^{o}$ for the sin θ signal attenuation. The attenuation switches closed are logically chosen so the phase of the signal $\sin\theta(\pm \cos 67.5^{o})$ where the $\pm$ refers to the phase output of the step down transformer, is always out of phase with the values $\cos\theta(\pm \sin 22.5^{o})$ or $\cos\theta(\pm \sin 67.5^{o})$. The logic equations used to determine which switches are closed are included in figure 3-9. A convenient means of determining which switches from S1 through S9 will be closed for a given angle is included in figure 3-10 (Coarse Switching Diagram).

The coarse switching diagram, figure 3-10, illustrates the range of gimbal angles over which each switch is closed. The switch numbers are in agreement with S1 through S9 of figure 3-8.

Therefore, these diagrams can be used simultaneously when analyzing the operations of the coarse module. The ±S on figure 3-10 indicates ± sine switch, the ±C indicates a ± cosine switch, the value of which is shown on the diagram. The R reference indicates the closure of switch S9 applying a reference signal to the summing function. Switch S9 is controlled by the 2^{12} bit of the read counter. The L of the diagram indicates a ladder voltage. The ladder is an attenuation signal controlled by S10, S11, and S12. These switches are in turn controlled by read counter bits 2^{11}, 2^{10}, 2^{9} respectively.

An explanation of the use of figures 3-8, 3-9 and 3-10 in the solving of the trigonometric equation $\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta \sin\Psi + K \sin\Psi$ is now in order. Figures 3-11, 3-12, and 3-13 will also be referred to in the following examples. Figure 3-11 shows the $\sin\theta$, the $\cos\Psi$ attenuation values, and the result of the $\sin\theta \cos\Psi$ at the input to the operational amplifier. Figure 3-12 shows the $\cos\theta$, the $\sin\Psi$ attenuation values, and the result of the $\cos\theta \sin\Psi$ at the input to the operational amplifier. Figure 3-13 shows the result of summing $\cos\theta \sin\Psi + \sin\theta \cos\Psi$ and compares it with the constant and ladder attenuation values of switch S9, S10, S11, and S12. It will be shown in the following examples that through the proper selection of switches the phase of the $\sin\theta$ and $\cos\theta$, and the magnitude of the attenuation values of Ψ will result in the $\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta \sin\Psi + K \sin\Psi$ equation being a null or zero whenever $\Psi = \theta$ within the tolerance of the coarse module ($\approx 5^{o}$).

Example #1: $\theta = 0^{o}$ First Quadrant

From the coarse switching diagram, figure 3-10, for 0^{o} switches R, +C 22.5 and -S 22.5 are closed by the switch control from the read counter and represent $\Psi = 0^{o}$. These correspond with S9, S5 and S3 of figure 3-8. The signal value at the summing junction due to S3 closure is 0 v rms. Figure 3-11. The value due to S5 closure is 5 v $(-\cos 0^{o})(\sin 22.5^{o}) = -5$ v $(.383) = -1.91$ v, or 1.91 volts rms out of phase with the reference excitation. Figure 3-11. This out of phase signal will be added to the output of S9 which is 5 v rms $(\sin 22.5^{o}) = +1.91$ v rms. The two signals are equal in magnitude and opposite in phase, figure 3-12, and therefore cancel at the input to the operational amplifier.

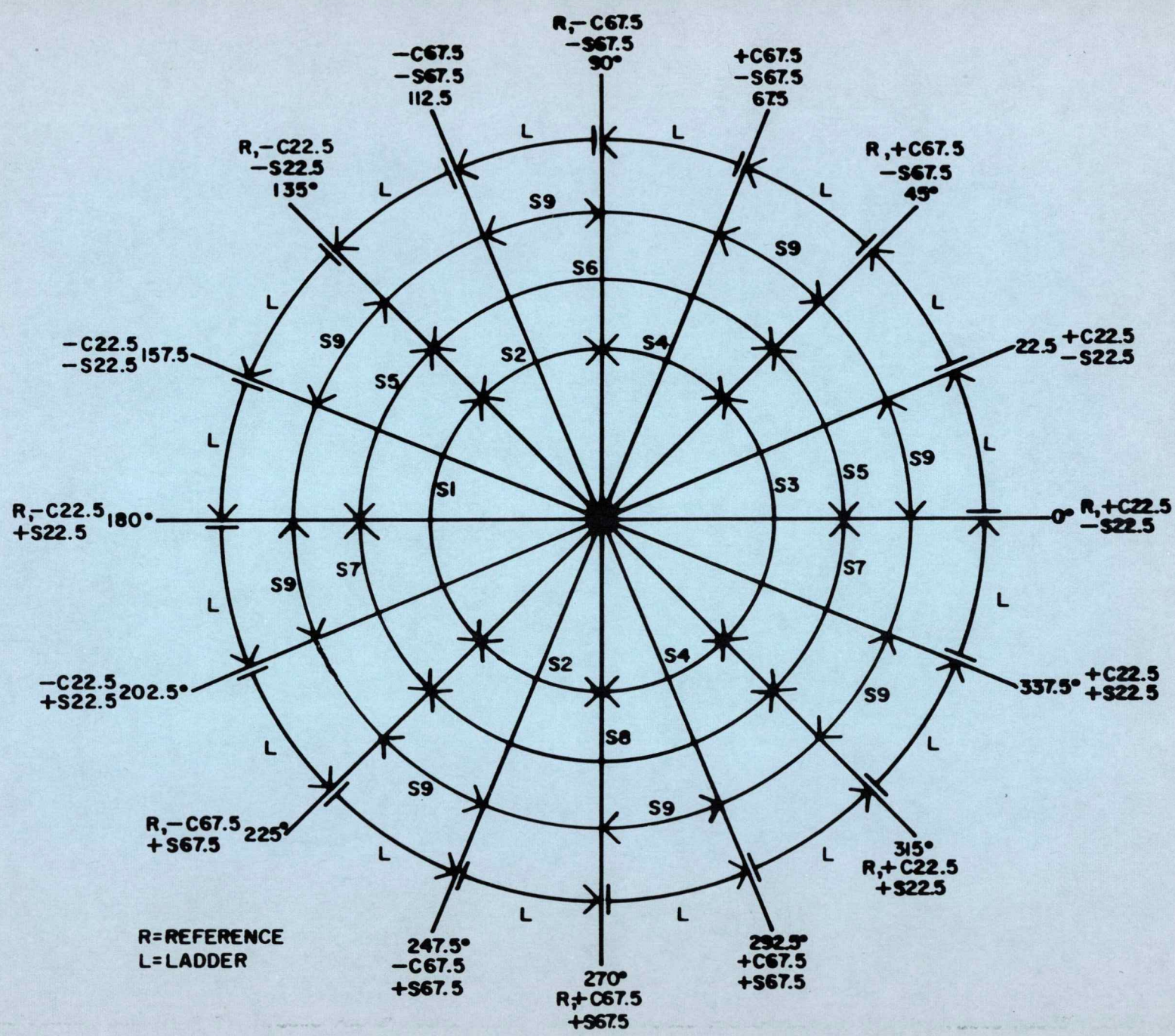


Figure 3-10. Coarse Switching Diagram

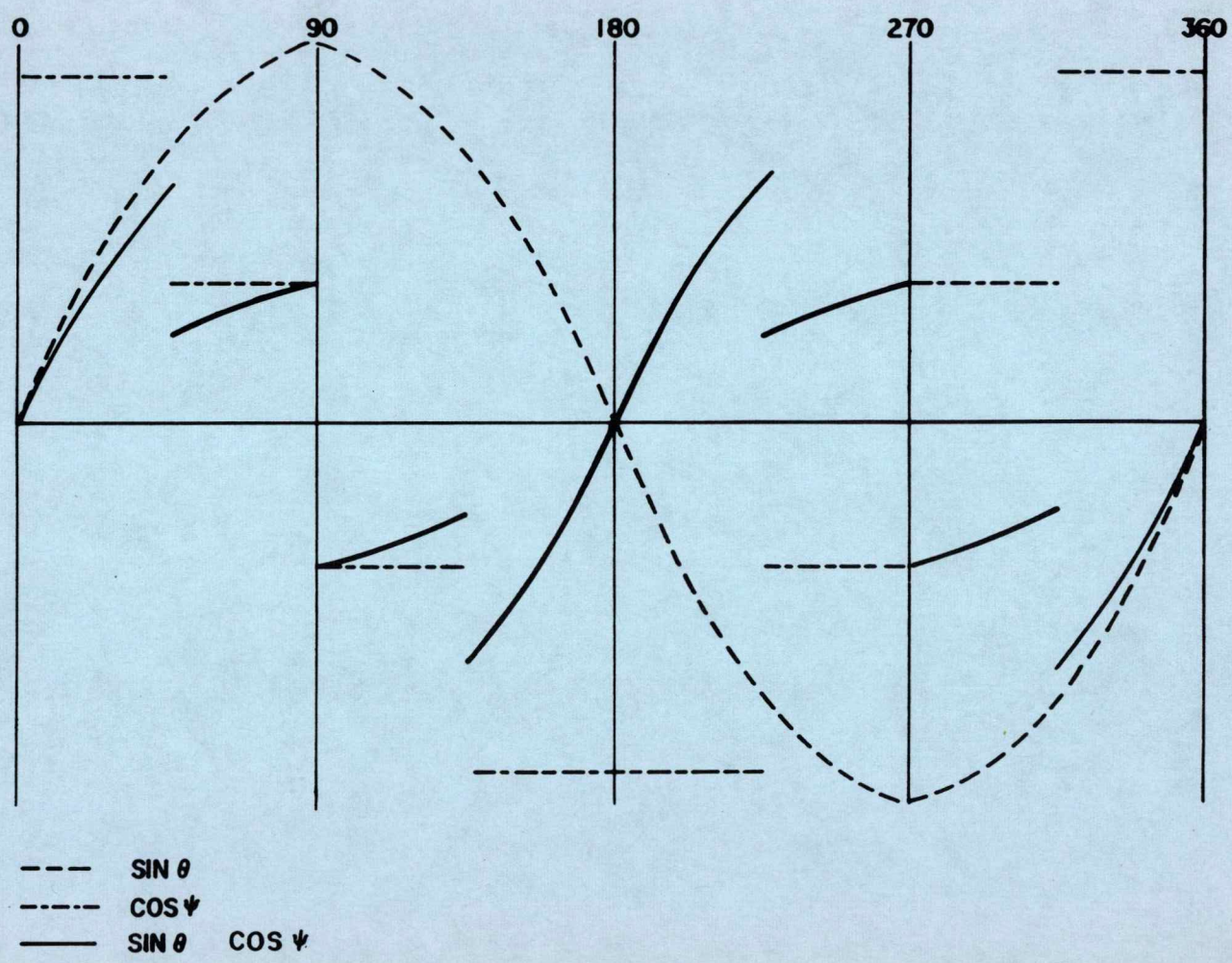


Figure 3-11. Sin θ Cos Ψ

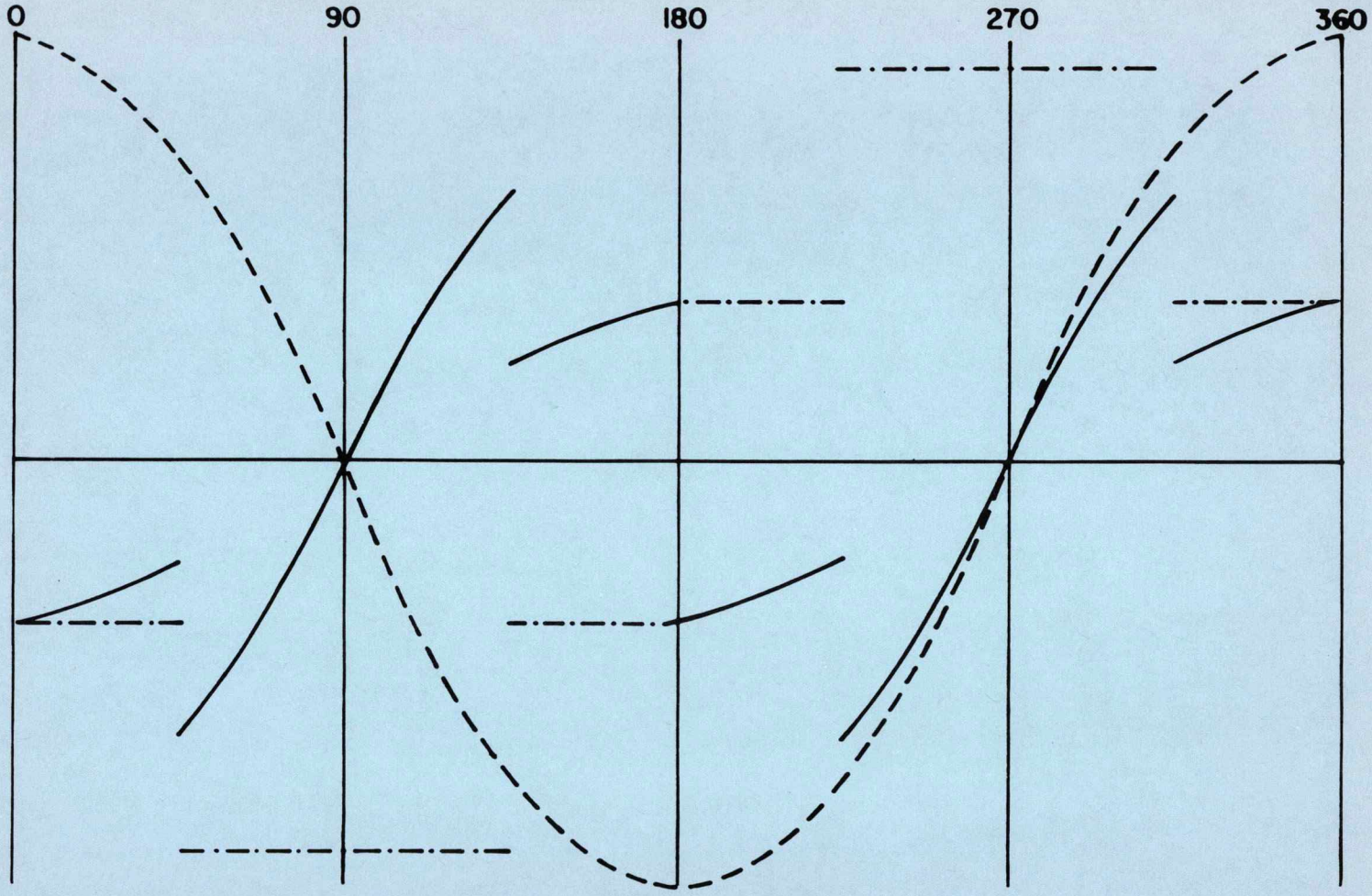


Figure 3-12. Cos θ Sin Ψ

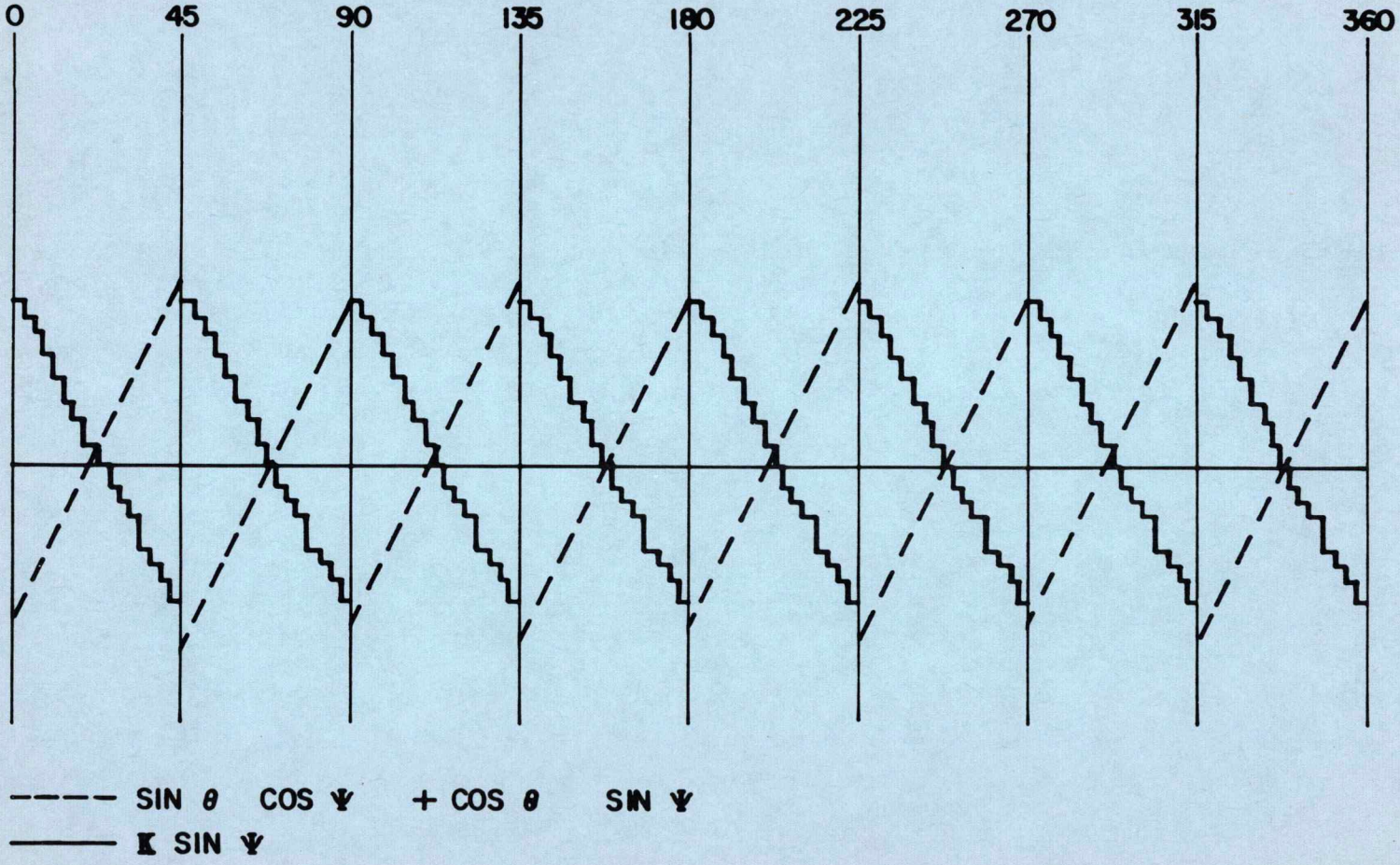


Figure 3-13. Sin (θ - Ψ)

Applying the above values of example 1 to the mechanized equation:

$$\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi$$

$$= 5\text{ v }(\sin 0^{o})(\cos 22.5^{o}) + 5(-\cos 0^{o})(\sin 22.5^{o}) + 5(\sin 22.5^{o})$$

$$= 5\text{ v }(0)(.924) + 5(-1)(.383) + 5(.383)$$

$$= 0 + (=1.91) + (1.91)$$

$$= 0$$

Example #2 $\theta = 135^{o}$ Second Quadrant

From the coarse switching diagram, figure 3-10, for 135^{o} switches R, -C 22.5 and -S 22.5 are closed by the switch control from the read counter and represent $\Psi = 135^{o}$. These correspond with S9, S5 and S1 of figure 3-8. The signal value at the summing junction due to S1 closure is $5(-\sin 135^{o})(\cos 22.5^{o}) = 5(-.707)(.924) = -3.26$ v rms. The value due to S5 closure is $5(-\cos 135^{o})(\sin 22.5^{o}) = 5[-(-.707)](.383) = +1.34$. The value due to S9 closure is $5(\sin 22.5) = 5(.383) = +1.91$. Therefore at the main summing junction the above values are summed together as follows:

$$\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi$$

$$= -3.26 + 1.34 + 1.91$$

$$= -3.26 + 3.25$$

$$= -.01\text{ v rms}$$

This is considered a null since it is well within the tolerance of the coarse module.

Example #3 $\theta = 225^{o}$ Third Quadrant

From the coarse swutching diagram, figure 3-10, for 225^{o}, switches R, -C 67.5, and +S 67.5 are closed by the switch control from the read counter and represent $\Psi = 225^{o}$. These correspond with S9, S8 and S2 of figure 3-8. The signal value at the summing junction due to S2 closure is $5(-\sin 225^{o})(\cos 67.5^{o}) = 5[-(-.707)](.383) = +1.34$. The value due to S8 closure is $5(\cos 225^{o})(\sin 67.5^{o}) = 5(-.707)(.924) = -3.26$. The value due to S9 closure is $= +1.91$. The magnitude and phase of these values are the same as in example 2 and therefore the result will be the same.

A more complex example of attenuation will now be investigated which will require the use of the ladder switches S10, S11, and S12 to satisfy the requirements of the switching circuit.

Example #4 $\theta = 310^{o}$ Fourth Quadrant

From the coarse switching diagram, figure 3-10, for 310^{o}, switches +C 67.5 (S4) + S 67.5 (S8) and L are closed. To determine which of the ladder switches are to be closed it will be necessary to refer to figures 3-7 and 3-9. For the read counter shown in figure 3-7 to represent 310^{o} will require a one in the following bit locations.

180^{o}	2^{15}
90	2^{14}
22.5	2^{12}
11.25	2^{11}
56	2^{10}
309.35	

Referring now to the Coarse Switch logic equations, figure 3-9b it can be determined which of the driver circuits will be at a one (switch closed) position. Since we have 2^{15} and 2^{14} but do not have 2^{13}, the logic for DC 4 (S4) and DC 8 (S8) is satisfied. This agrees with the switch positions as determined from figure 3-10. We have 2^{12} therefore DC 9 (S9) will not be closed. We have 2^{11} and 2^{10} therefore DC 10 (S10) and DC 11 (S11) will be closed.

The signal value at the summing junction of the coarse module, figure 3-8, due to the closure of S4 is, $5 (\sin 310^{o}) (\cos 67.5^{o}) = 5 (-.766) (.383) = -1.47$.

The signal value due to the closure of S8 is $5 (\cos 310^{o}) (\sin 67.5^{o}) = 5 (.643) (.924) = +2.97$.

The signal value due to the closure of the ladder switch S10 and S11 is, $-5 (\sin 11.25^{o}) = -5 (1.99) = -.995$ and $-5 (\sin 5.6^{o}) = -5 (.078) = -.390$.

Applying the above values to the mechanized equation,

$$\sin (\theta - \Psi) = \sin \theta \cos \Psi + \cos \theta \sin \Psi + K \sin \Psi$$

$$= -1.47 + 2.97 - .995 - .390$$

$$= -2.85 + 2.97$$

$$= +0.12 \text{ v rms}$$

which is considered a null since it is well within the tolerance of the coarse module.

The coarse module will function and the coarse error signal C_1 will be generated whenever $\theta_E (\theta - \Psi)$ is greater than approximately 5^{o}. For θ_E less than 5^{o} the output of the operational amplifier is below the triggering level of the Schmitt tirgger and C_1 is not generated. At this point the analog to digital conversion function is continued in the quadrant select and main summing amplifier.

The coarse system module also performs two additional functions: generates the ambiguity detect signal (A_d) and the IMU cage signal. The IMU cage signal is taken from a separate secondary winding of the sin θ transformer T1 and is used during the IMU cage mode to drive the gimbals to their zero positions. To develop the ambiguity detect signal, the output of a separate secondary winding on the cos θ transformer, T2, is applied through an emitter follower to a Schmitt trigger which fires when its input exceeds a nominal value of approximately 12.25 v rms. The Schmitt trigger output is an 800 cps square wave, which will exist when the gimbal angle is between 125 degrees and 235 degrees. The ambiguity detect signal is sent to the ambiguity logic circuit in the digital mode module to prevent the CDU from nulling at an ambiguous angle.

The theory and mechanization of the ambiguity detect circuitry will be discussed in the digital mode module section of the CDU (section 3.12).

3.7 QUADRANT SELECT MODULE AND MAIN SUMMING AMPLIFIER MODULE

The quadrant select module and main summing amplifier and quadrature reject module work together to perform the fine portion of the analog to digital conversion. The quadrant select module and the main summing amplifier and quadrature reject module will be discussed in the same section since together they perform a single function.

3.7.1 QUADRANT SELECT MODULE. The inputs to the quadrant select module are:

a. Cos 16θ

these angles are treated as θ in the description to follow

b. Sin 16θ

c. Switch control signals D1 through D14

The module outputs include:

a. Four 800 cps signals referred to as S1, S2, S3, S4 Cos θ

b. Four 800 cps signals referenced as S1, S2, S3, S4 Sin θ

c. Two 800 cps signals referred to as S12 - 11.25° and S9 - 11.25°

d. Two 800 cps bias signals referred to as S10 ΔK and S13 Δ K.

3.7.1.1 Theory of Operation. The function of the quadrant select module and main summing amplifier and quadrature reject module is to generate two fine error signals which result from the comparison of θ and Ψ. The quadrant select module and main summing amplifier and quadrature reject module have been mechanized such that the actual equation used for the comparison of θ and Ψ is the same as that used by the coarse module. $\sin(\theta - \Psi) = \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi$ where K is a $\cos(\theta - \Psi)$ function from the ladder amplifier and the sign of the factors in the equation are determined by selection of in phase or out of phase signals.

Figure 3-8 shows the relative phase relationships between the sine and cosine signals in each quadrant with respect to a reference and therefore with respect to each other. It can be seen that the signals are out of phase only in quadrants II and IV. The quadrant select circuit will insure that the signals are always properly phased by inverting the phase of the sine θ electrical signal when the θ angle is in quadrants I and IV and inverting the phase of the cosine θ signal when θ is in quadrants III and IV. Figure 3-14 is a block diagram of the quadrant select module and main summing amplifier and quadrature reject module.

The inversion of the signals is done in the following manner. Amplifiers A1 and A2 and switches S5 and S6 are used to invert the sine θ signals. Amplifiers A3 and A4 along with S7 and S8 invert the cosine signals in the appropriate quadrants.

Switches S5, S6, S7 and S8 are closed when the following logic equations are satisified:

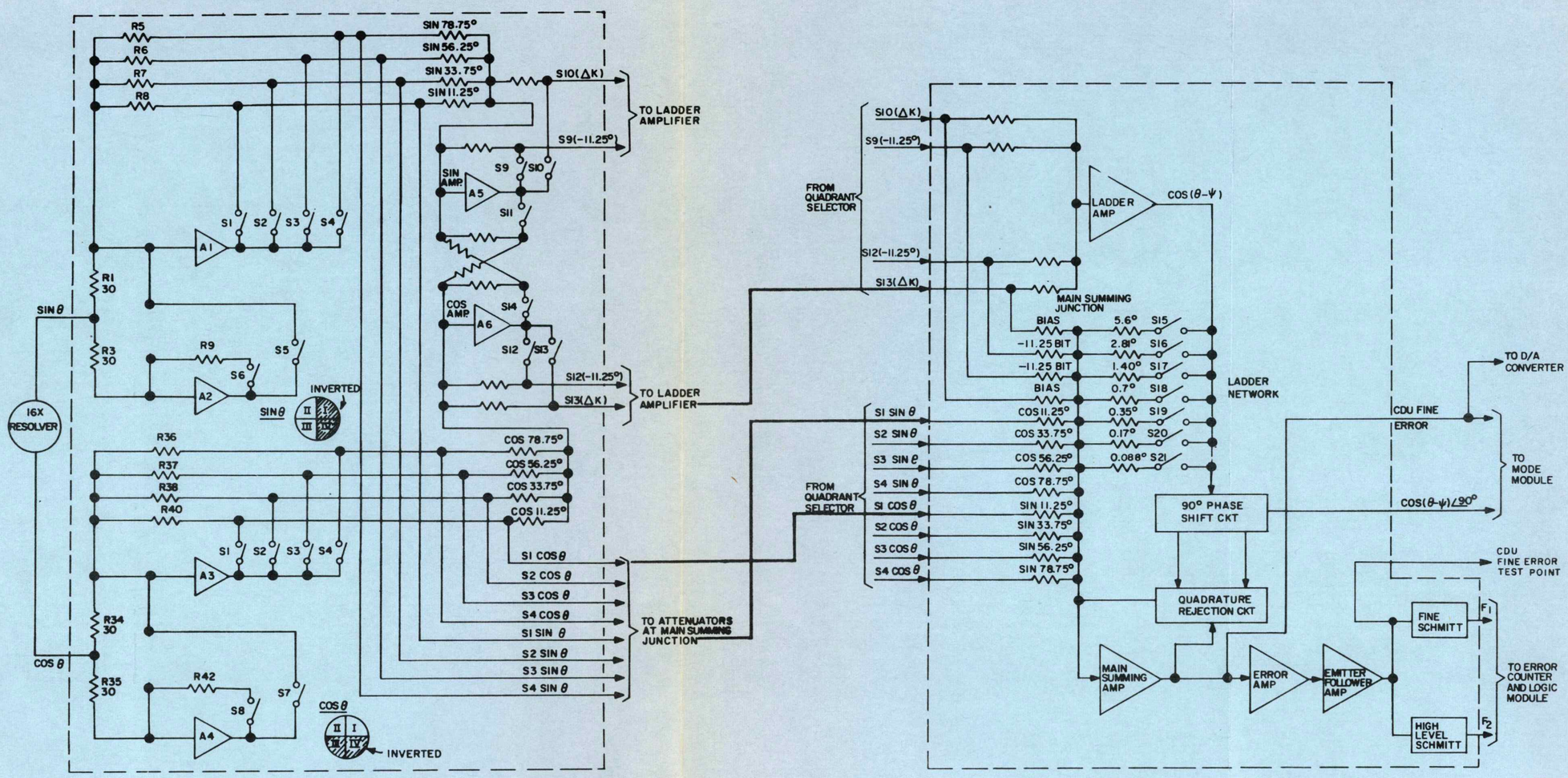
$S5 = 2^{10}\,\overline{2^{11}} + \overline{2^{10}}\,2^{11}$

$S6 = 2^{10}\,2^{11} + \overline{2^{10}}\,\overline{2^{11}}$

$S7 = 2^{11}$

$S8 = 2^{11}$

where the exponent of two refers to the corresponding bit positions in the read counter.



ALL UNSPECIFIED RESISTORS ARE 25K ALL VALUES ARE IN K Ω. REFERENCE DESIGNATIONS CORRESPOND TO SCHEMATIC 2010059.

16181

Figure 3-14. Quadrant Selector Module, Main Summing Amplifier and Quadrature Rejection Module, Block Diagram

Sine θ inversion is done in quadrants I and IV of the angle θ. When inversion is required, S6 is closed and S5 is open. Switch S6 provides a feedback path around A2 and disconnects the output of A2 from the input of A1. The input of A1 is inverted giving the desired output. When no inversion is required, S5 is closed and S6 is open. The inverted output of A2 is applied to the input of A1. Through the summing network the A2 inverted output is twice the amplitude of the normal sine input to A1. The resulting summed inverted signal is reinverted making the output of A1 the same phase as the phase of the sine of the gimbal angle.

Cosine inversion is done in the same manner using A3, A4, S7 and S8. The inversion is done in quadrants III and IV.

Switches S1 through S4 perform two functions. First, they select resistance values which attenuate the properly phased sine and cosine signals for inputing to a main summing. The MSA output, if nulled, will not provide signals to the read counter to change the attenuation switches. If an angle of 33.75° exists at the resolver, the in phase sine signal is inverted by A1 and A2. The in phase cosine signal is not inverted. Switching logic shows that for an angle θ of 33.75°, switch S2 will be closed. The switch closure results in two inputs to the summing amplifier from the attenuation circuits: $-\sin 33.75^\circ \cos 33.75^\circ$ and $+\cos 33.75^\circ \sin 33.75^\circ$. These signals without any additional inputs cause the main summing amplifier to be nulled. If some angle θ were chosen which is not an exact multiple of the angle 11.25°, the attenuation required cannot be accomplished by switches S1 through S4 alone. Additional switching is then performed in the main summing amplifier module ladder circuits.

The logic equations mechanized to control switches S1 through S4 are as follows:

$$S1 = 2^8\, 2^9\, 2^{10} + \overline{2^8}\, \overline{2^9}\, \overline{2^{10}}$$

$$S2 = \overline{2^8}\, 2^9\, 2^{10} + 2^8\, \overline{2^9}\, \overline{2^{10}}$$

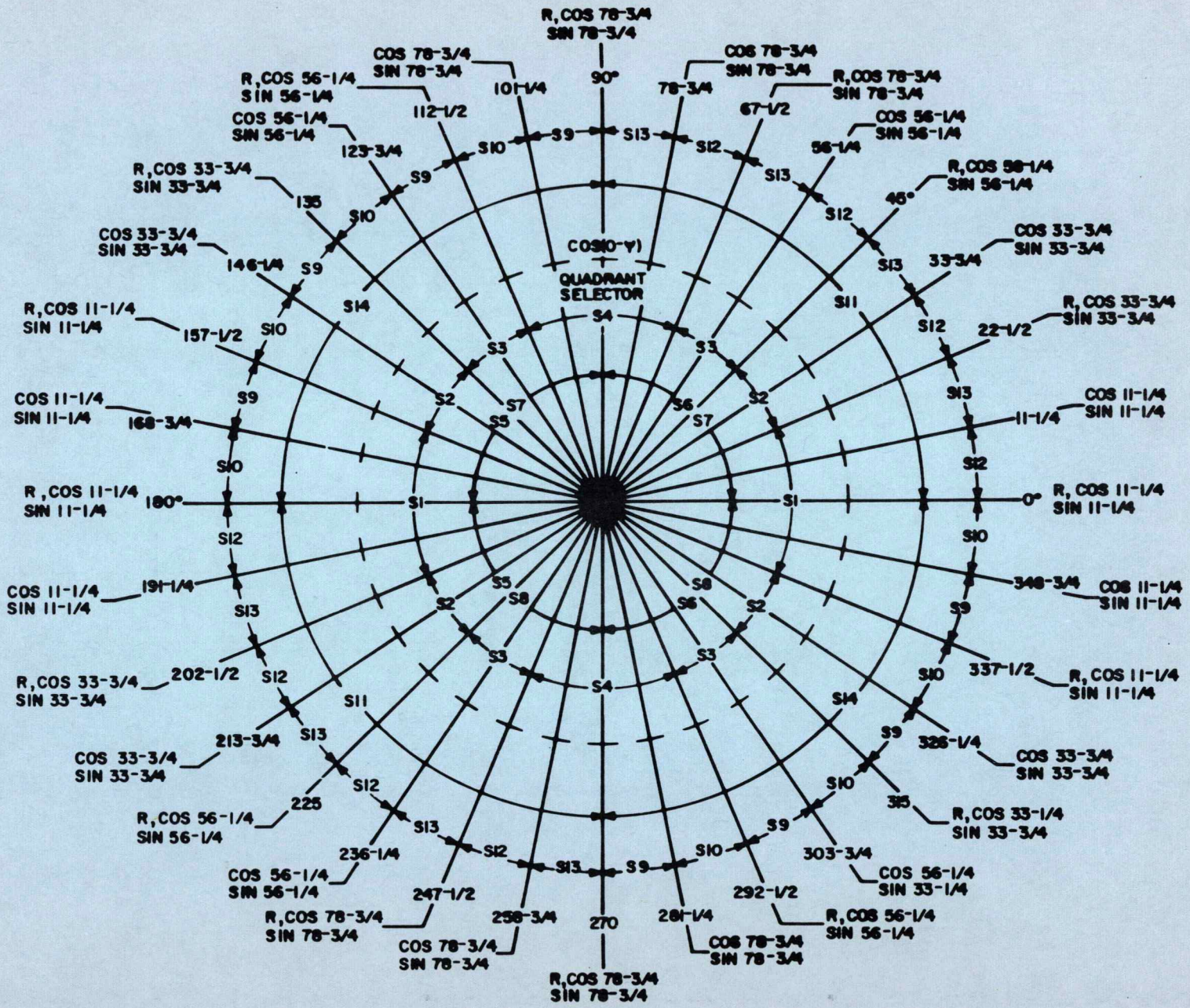
$$S3 = 2^8\, \overline{2^9}\, 2^{10} + \overline{2^8}\, 2^9\, \overline{2^{10}}$$

$$S4 = \overline{2^8}\, \overline{2^9}\, 2^{10} + 2^8\, 2^9\, \overline{2^{10}}$$

where: the exponent of two refers to the corresponding bit in the read counter.

Figure 3-15 illustrates which of the switches S1 through S4 are closed over the various segments of the 360° rotation of the resolver. Note that only one switch is closed at any time.

A second function of the quadrant select module is the generation of an electrical 800 cps signal proportional to the cosine $(\theta - \Psi)$. This function is performed by the sine amplifier A5, the cosine amplifier A6, and switches S9 through S14. The reference equation, $\cos(\theta - \Psi)$, in complete form is $\cos(\theta - \Psi) = \sin\theta \sin\Psi + \cos\theta \cos\Psi$. This equation implies that the two signals must be of the same phase in order to generate the ladder reference $\cos(\theta - \Psi)$.


R, COS 78-3/4
SIN 78-3/4
COS 78-3/4
SIN 78-3/4
R, COS 56-1/4
SIN 56-1/4
COS 56-1/4
SIN 56-1/4
R, COS 33-3/4
SIN 33-3/4
COS 33-3/4
SIN 33-3/4
R, COS 11-1/4
SIN 11-1/4
COS 11-1/4
SIN 11-1/4
R, COS 11-1/4
SIN 11-1/4
COS 11-1/4
SIN 11-1/4
R, COS 33-3/4
SIN 33-3/4
COS 33-3/4
SIN 33-3/4
R, COS 56-1/4
SIN 56-1/4
COS 56-1/4
SIN 56-1/4
R, COS 78-3/4
SIN 78-3/4
COS 78-3/4
SIN 78-3/4
R, COS 78-3/4
SIN 78-3/4
COS 78-3/4
SIN 78-3/4
R, COS 56-1/4
SIN 56-1/4
COS 56-1/4
SIN 33-1/4
R, COS 33-1/4
SIN 33-3/4
COS 33-3/4
SIN 33-3/4
R, COS 11-1/4
SIN 11-1/4
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R, COS 11-1/4
SIN 11-1/4
COS 11-1/4
SIN 11-1/4
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COS 33-3/4
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COS 56-1/4
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COS 33-3/4
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R, COS 56-1/4
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COS 56-1/4
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COS 11-1/4
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COS 33-3/4
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SIN 78-3/4
COS 78-3/4
SIN 78-3/4
R, COS 78-3/4
SIN 78-3/4
COS 78-3/4
SIN 78-3/4
R, COS 56-1/4
SIN 56-1/4
COS 56-1/4
SIN 56-1/4
R, COS 33-3

In the quadrant select circuit the sine and the cosine signals were purposely made to always be out of phase with each other. The inputs to the sine amplifier are sin θ sin 11.25°, sin θ sin 33.75°, sin θ sin 56.25°, or sin θ sin 78.75°, depending on the switch (S1 through S4) selected by the quadrant select circuit. The cosine amplifier inputs are cos θ cos 78.75°, cos θ cos 56.25°, cos θ cos 33.75°, or cos θ cos 11.25°, again dependent on S1 through S4 settings. It should be remembered that the sine and cosine amplifier inputs are always out of phase with each other.

The input signals to the sine and cosine amplifiers are inverted. Each amplifier has two outputs, but switching logic prevents the application of more than one output to the ladder amplifier at any time. Switch S11 switches the output of the sine amplifier to the input of the cosine amplifier and switch S14 switches the output of the cosine amplifier to the input of the sine amplifier. Switches S11 and S14 will never both be closed at the same time. S11 is closed when the θ angles are in the first or third quadrant; S14 will close when the θ angle is in quadrants II or IV. If S14 is closed, the output will be taken from the sine amplifier. The cosine amplifier input is an out of phase signal which is inverted and summed with the in phase signal at the input of the sine amplifier. The summed value is then inverted making it an out of phase signal once again. This signal is connected to the ladder amplifier through switches S9 or S10. Only one of these switches will be closed at any instant. The output of the amplifier then is equivalent to cos $(\theta - \Psi)$ = sin θ sin Ψ + cos θ cos Ψ, where θ is again the angle through which the 16X resolver has rotated (electrically) and Ψ is one of the incremental angles 11.25°, 33.75°, 56.25°, or 78.75°. The cos $(\theta - \Psi)$ signal applied as a reference to the ladder amplifier in the main summing amplifier will always be out of phase with the reference signal and approximately the same amplitude for all inputs to the cos $(\theta - \Psi)$ generator.

The logic equations mechanized to control the switching in the cos $(\theta - \Psi)$ generator are as follows:

$$S9 = \overline{2^7}\ 2^{10} \qquad S12 = \overline{2^7}\ \overline{2^{10}}$$

$$S10 = 2^7\ 2^{10} \qquad S13 = 2^7\ \overline{2^{10}}$$

$$S11 = \overline{2^{10}} \qquad S14 = 2^{10}$$

Figure 3-15 illustrates the operation of these switches and the quadrant select switches through 360 electrical degrees of resolver output. It can be noted from the switching diagram that S11 and S14 alternate when θ goes from 0° to 360° with S11 being on in quadrants I and III and S14 being on in quadrants II and IV. Switches S9 and S10 are used in conjunction with S14 and therefore are on in alternate 11.25° sectors in quadrants II and IV. Switches S12 and S13 operate in alternate 11.25° sectors in quadrants I and III when S11 is energized.

One output from the cos $(\theta - \Psi)$ generator is used as an input to the ladder amplifier of the main summing amplifier module. A second output is always taken from the amplifier selected and is provided as a bias to the main summing amplifier summing junction. This signal is also referred to as a Δ K signal on the mechanization drawings of the CDU. This bias value minimizes the errors generated when mechanizing the cos $(\theta - \Psi)$ equation.

3.7.2 MAIN SUMMING AMPLIFIER AND QUADRATURE REJECTION MODULE. The main summing amplifier and quadrature rejection module (main summing amplifier) must operate in conjunction with the quadrant select module to electrically mechanize the fine portion of the CDU equation, $\sin(\theta - \Psi) = \sin\theta \cos\Psi + \cos\theta \sin\Psi + K \sin\Psi$.

The fine system of the CDU utilizes the quadrant select and the main summing amplifier modules plus the 2^0 through 2^{11} bits of the read counter. The read counter stages provide the switching control signals necessary to null the equation, setting Ψ equal to θ within approximately two bits. The main summing amplifier module inputs include the following:

a. All the 800 cps signal outputs of the quadrant select module.

b. Switch control signals D15 through D21 from read counter stages 2^0 through 2^6.

The outputs of this module include the following:

a. A fine error signal to the DAC (summed output).

b. F1 - a fine ternary output, 800 cps square wave.

c. F2 - a high ternary output, 800 cps square wave.

d. Cos $(\theta - \Psi)$ at 90^o phase angle.

3.7.2.1 Main Summing Amplifier Module Theory of Operation. The main summing amplifier module operation can be broken down into separate functions: summing, quadrature rejection, and F1, F2 generation.

3.7.2.1.a Summing. In the summing operation of the main summing amplifier module, the inputs shown in figure 3-14 are summed at the main summing junction with the output of the quadrature reject circuit and the ladder circuit. The ladder circuit includes the ladder amplifier and switches S15 through S21 and their associated attenuation resistors.

The summing operation is as follows: Assume first that there is no input required from the quadrature reject circuit and that a gimbal angle θ of 11.25^o exists. This gimbal angle is equivalent to an electrical angle of the 16X resolver of 180^o. Figure 3-15 switching logic indicates that switches S1, S6, and S7 of the quadrant select module are closed which gives an input of S1 sin θ (out of phase) and S1 cos θ (in phase) to the main summing amplifier module. These signals, when routed through the attenuation resistors in the MSA module, become sin θ cos 11.25^o and cos θ sin 11.25^o respectively at the junction of the main summing amplifier. These signals, equal in amplitude and opposite in phase, will null each other out. The main summing amplitude input and output are therefore nulled without further switching.

Figure 3-15 also indicates that switches S11 and S12 or S13 are closed at this time. The output of the cos $(\theta - \Psi)$ generator will put an out of phase bias into the main summing junction. If S13 is closed, an out of phase bias value will be applied to the main summing junction. This bias minimizes the error generated in the implementation of the cos $(\theta - \Psi)$ equation. This signal is applied to the ladder amplifier. The ladder amplifier inverts the signal putting it in phase with the 800 cps reference excitation. If the 11.25 bit is selected by switch S12, the ladder amplifier has a bias compensation incorporated in its input gain control circuits. At $\theta = 11.25^{o}$, S13 will be closed.

If a gimbal angle θ is selected which is not an exact multiple of 11.25^{o}, the main summing junction cannot be nulled by the operation of switches S1 through S4 of the quadrant select module alone. If this condition exists, an in phase signal from the ladder amplifier is applied through switches S15 through S21 to attenuate the signal at the junction. Switches S15 through S21 are controlled by bits 2^{0} through 2^{6} of the read counter. Bit 2^{0} controls switch S21. Bit 2^{6} controls switch S15. The remainder of the switches are controlled in the same inverse order from the read counter bits.

Example #1

Assume an angle of $16\theta = 19.65^{o}$ exists. Figure 3-15 again shows that S1, S6, S7, and S13 of the quadrant select module are closed. The resulting signal at the main summing junction is out of phase. The incremental closing of the ladder switches applies an in phase signal to the junction. When the in phase value is equivalent to the out of phase signal from the quadrant select module, the input to the MSA will be nulled. This condition will exist when S15 and S16 of the ladder amplifier are closed. Inserting the values from figure 3-14 into the mechanized equations will show the module operation.

$$\begin{aligned}
\sin(\theta - \Psi) &= \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi \\
&= -\sin(19.65^{o})\cos(11.25^{o}) + \cos(19.65^{o})\sin(11.25^{o}) + K\sin\Psi \\
&= -(.336)(.98) + (.94)(.195) + K\sin\Psi \\
&= -.33 + .183 + K\sin\Psi \\
&= -.147 + K(\sin 8.4^{o}) \\
&= -.147 + .147
\end{aligned}$$

where K is a cos $(\theta - \Psi)$ function and approaches 1 as θ and Ψ approach equality.

If the selected angle is in the next 11.25^{o} sector (i.e. 25^{o}) the switching diagram, figure 3-5, indicates that S11, S12, S2, S6 and S7 will be closed. With this combintion of switches the voltage at the main summing junction from the quadrant select module will be in phase with the reference excitation. Figures 3-16 and 3-17.

$$\begin{aligned}
\sin(\theta - \Psi) &= \sin\theta\cos\Psi + \cos\theta\sin\Psi + K\sin\Psi \\
&= \sin 25\cos(33.75^{o}) + \cos 25\sin 33.75 + K\sin\Psi \\
&= (-.422)(.835) + (.905)(.555) + K\sin\Psi \\
&= -.352 + .505 + K\sin\Psi \\
&= +.153 + K\sin\Psi
\end{aligned}$$

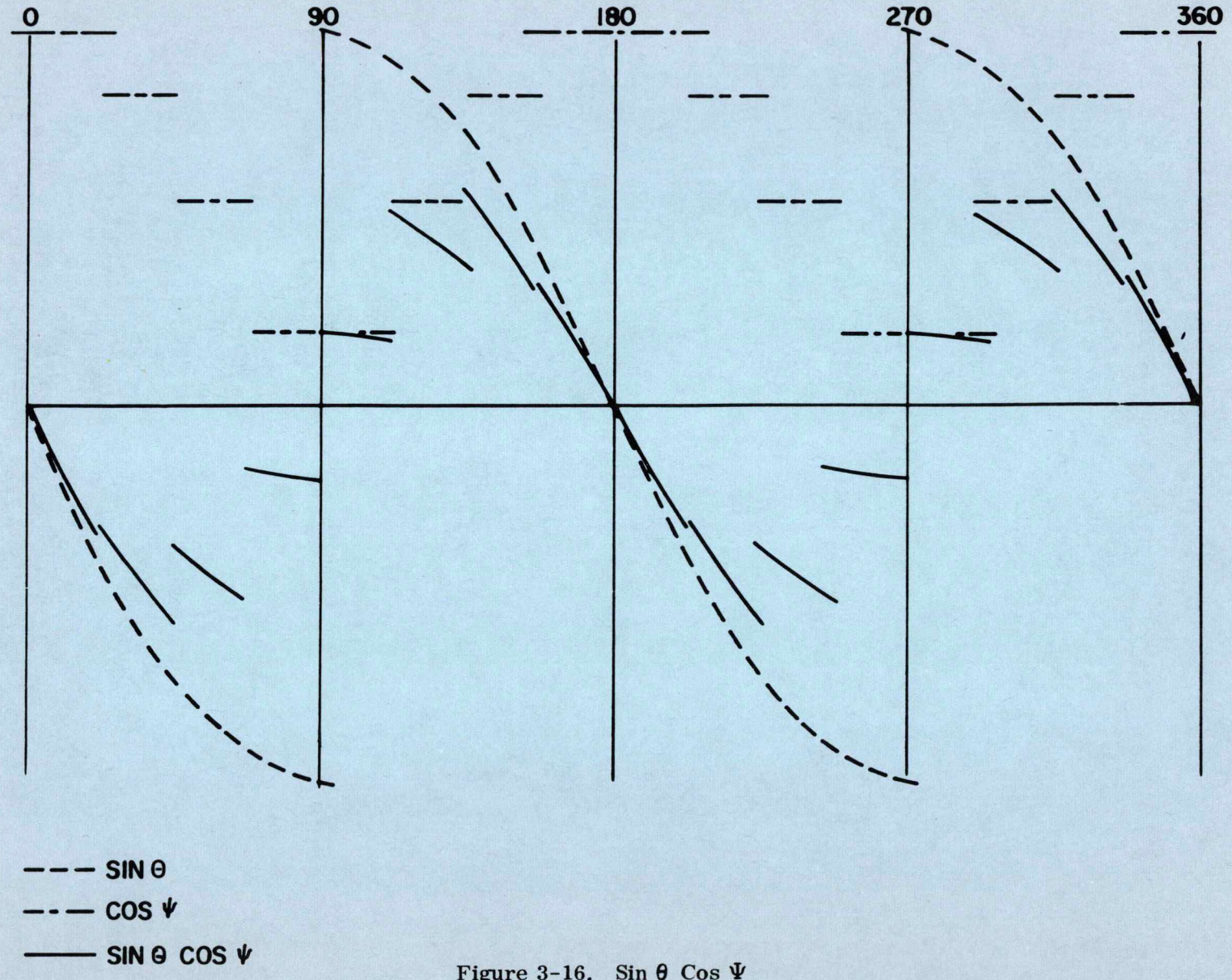


Figure 3-16. Sin θ Cos Ψ

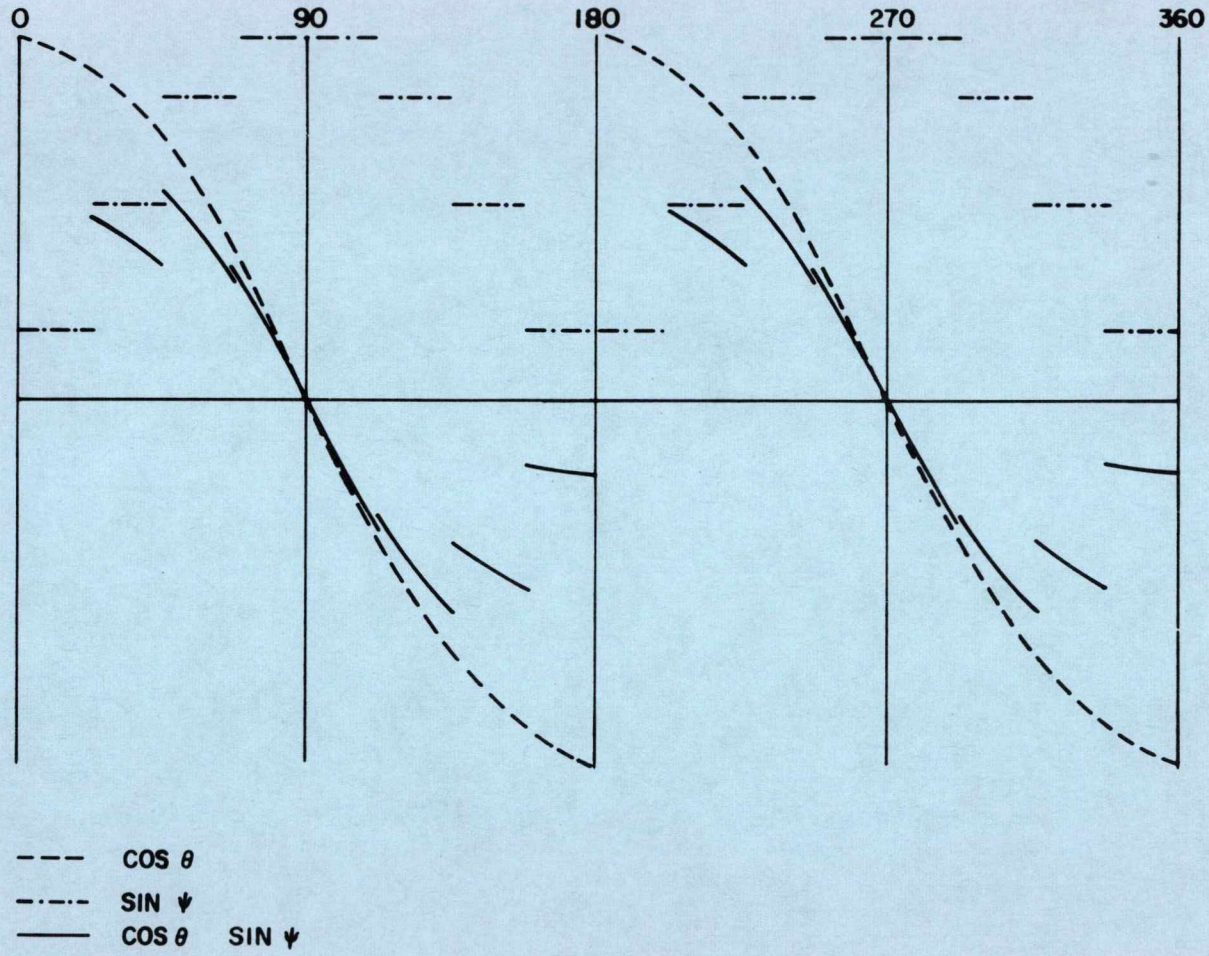


Figure 3-17. Cos θ Sin Ψ

If the ladder switches were closed, the resulting in phase signal (K sin Ψ) will increase the total in phase signal and the circuit will be inoperative. It is necessary to supply an out of phase signal to the junction for nulling with the ladder signal. Switch S12 closure applies a -11.25 bit bias signal to the junction, changing the signal to an out of phase condition which can then be nulled with an in phase signal from the ladder amplifier. The -11.25 signal in the main amplifier input performs the same function as the reference controlled by S9 in the coarse module. It can be seen that in electrical degrees indicated to the right of the ladder switch that the -11.25 input can be nulled out almost completely. With this out of phase signal applied to the summing junction the solution of the sin ($\theta - \Psi$) equation for 25° follows:

sin ($\theta - \Psi$) = + .153 + (-K sin 11.25°) + (K sin 2.53°) where (-K sin 11.25°) is the out of phase signal applied to the junction and K sin 2.53° is the ladder network sum of switches S21, S19, S18, S17 which will be closed for an angle of 25°. See figure 3-18.

sin ($\theta - \Psi$) = + .153 - .199 + .044

= - .002 v rms

This value is well within the theoretical least bit error voltage of 6 mv rms and the equation can be considered nulled.

3.7.2.1.b Quadrature Rejection. In any electrical signal generated by an inductive device such as a resolver, a certain percentage of quadrature component of the signal will be present. This quadrature component, if large enough, could cause the fine error Schmitt to fire, giving an erroneous input to the error counter logic and allowing the read counter to count to a false angle indication. To overcome this possibility, a quadrature reject circuit is incorporated into the main summing amplifier module.

The quadrature component is rejected by taking the cos ($\theta - \Psi$) output of the ladder amplifier, shifting the phase by ninety degrees, and using the cos ($\theta - \Psi$) $\angle 90^{\circ}$ signal to control a phase sensitive modulator and also key a chopper to provide modulation of a signal. The 800 cps output of the main summing amplifier is sampled, amplified, and applied to the input of the phase sensitive demodulator, which uses a 90° phase angle signal for a reference. If the MSA output contains a quadrature component in its output, this value will be demodulated and allowed to charge a capacitor in a filter circuit. The charge on the capacitor polarity will depend on whether the quadrature component was at 90° or 270° with respect to the phase reference.

The ± DC charge on the capacitor is accepted as an input to a chopper (modulator) which is controlled by the cos ($\theta - \Psi$) $\angle 90^{\circ}$ signal. The modulated output is amplified and will be 180° out of phase with respect to the input quadrature component and the quadrature reject circuit. This out of phase signal is applied to the main summing junction and tends to buck out any quadrature component of the voltage present. When the angle $\Psi = \theta$, the total output of the main summing amplifier is less than 6 mv rms.

The output of the cos ($\theta - \Psi$) 90° phase shift circuit is used as one of the CDU fail test points.

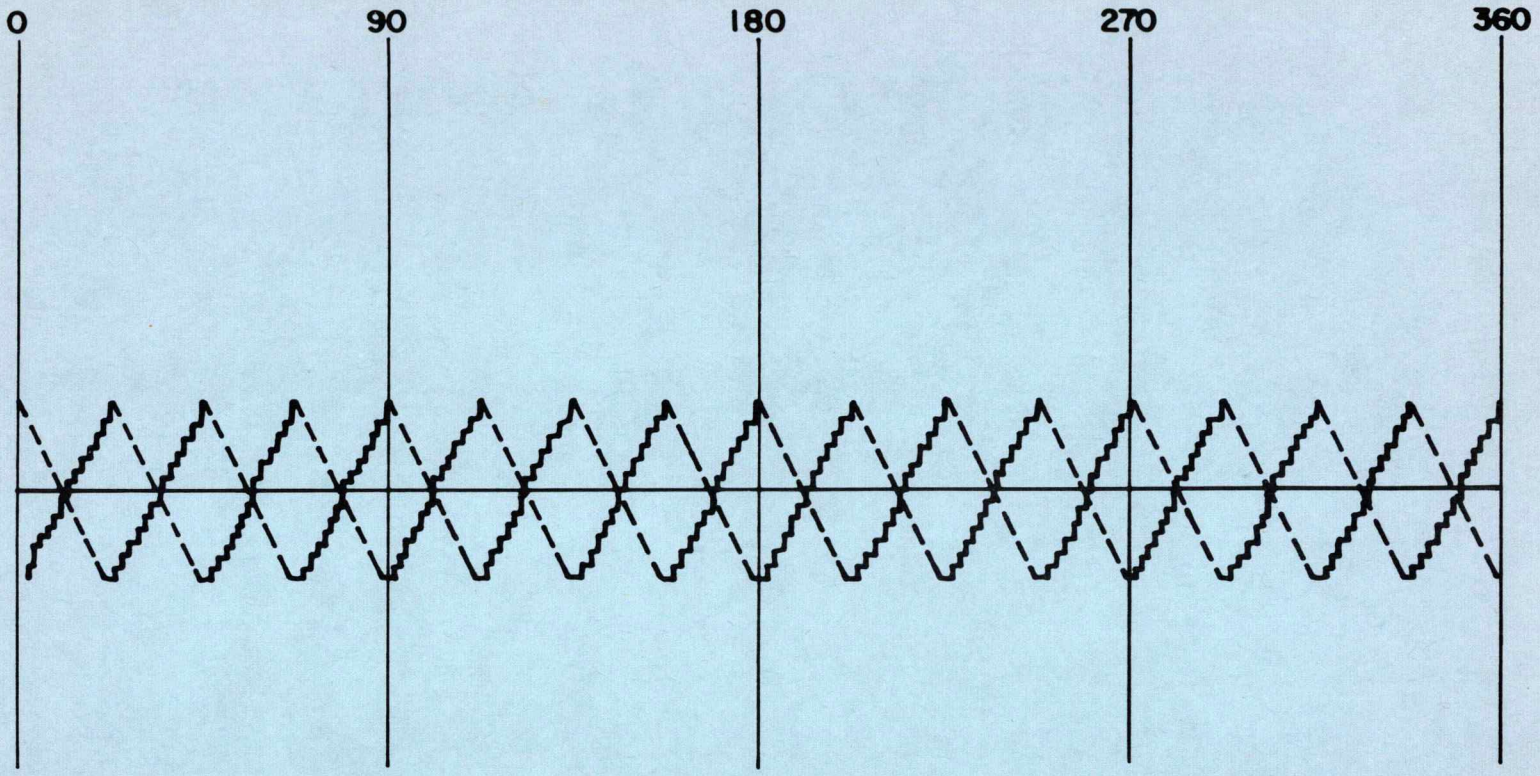


Figure 3-18. Sin (θ - Ψ)

3.7.2.1.c F1, F2 Generation. The main summing amplifier output is the input to an error amplifier. The error amplifier is used to fire two Schmitt triggers, one generating an 800 cps square wave (F1) and the other generating an 800 cps square wave (F2). F1 is used to select low read counter rate and will be generated whenever the read counter is within 20 pulses of reading the gimbal angle. The error amplifier output must be greater than 200 mv peak to peak to fire the fine 1 Schmitt. The fine 2 Schmitt will fire whenever the error amplifier output is greater than 4 v peak to peak.

3.8 READ COUNTER MODULE

The read counter of the CDU contains the circuitry necessary to accumulate, in digital form, the CDU indicated value of the gimbal angle or the optics trunnion or shaft angle. The counter also provides the switching signals used in the coarse module, the quadrant select module, and the main summing amplifier module, for the attenuation of the signals from the attenuation of the signals from the IMU or optics resolvers. The read counter provides the incremental angles Ψ used in the equation, $\sin(\theta - \Psi) = \sin\theta \cos\Psi + \cos\theta \sin + K \sin\Psi$. Five identical read counter modules exist in the coupling data unit.

The read counter inputs include:

a. Incrementing pulses P_I at $\phi 4$ time at 12.8, 6.4 or 0.8 kpps.

b. Up or down commands indicating to the read counter to count up or down.

c. $\overline{\phi 2}$ and $\phi 3$ timing pulses.

d. CDU zero moding discretes.

e. Turn-on enable discrete from the digital mode module. (Q)

The outputs from the read counter module include:

a. $\Delta 2^0$ ($\Delta 2^{\text{zero}}$) gimbal angle changes 40 $\widehat{\text{sec}}$/pulse.

b. $\Delta 2^2$ gimbal angle changes 160 $\widehat{\text{sec}}$/pulse. $\Delta\theta_G$.

c. Switch control signals D1 through D22.

d. Switch control signals DC1 through DC12.

A block diagram of the read counter module is shown in figure 3-19.

3.8.1 READ COUNTER THEORY OF OPERATION. The read counter consists of a series of 16 binary divider circuits, NAND logic elements used as buffer circuits, and NAND logic gates used to set up the control switching in the main summing, quadrant select, and coarse modules. The counter is capable of storing angles from 0^o to 359^o 59' 40". The angular value of each stage of the counter is shown in the block diagram.

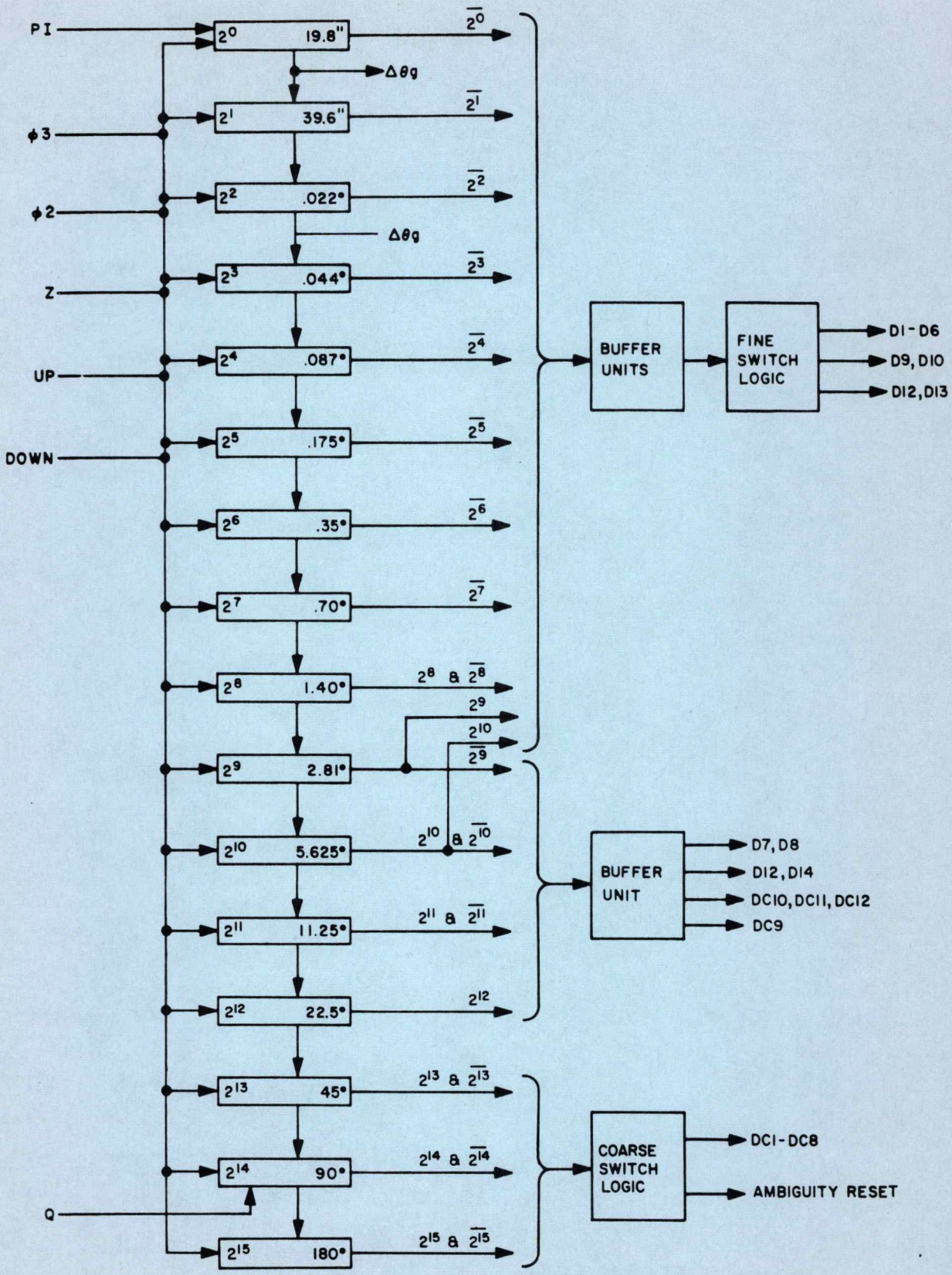


Figure 3-19. CDU Read Counter Module

The read counter will be pulsed at a 12.8 kpps rate when the magnitude of the θ_E signal resulting from the sin (θ - Ψ) comparison is such that C_1 and F_2 are generated. C_1 will be generated when the input to the coarse module Schmitt trigger is greater than 1.6 volts peak to peak. F_2 will be generated whenever the error amplifier output of the main summing amplifier output of the main summing amplifier module is greater than 4 volts peak to peak. The pulse rate to the read counter will be reduced to 800 pps when the read counter is within 20 bits ($\approx$ 0.1 degree) of reading the gimbal angle. At this point C_1 and F_2 will no longer be generated and only F_1 will be present. When the read counter is within 2 bits (40 $\overset{\frown}{\text{sec}}$) of equalling θ the output of the error amplifier will have been reduced to below the 200 millivolt peak to peak nominal triggering level of the fine Schmitt trigger and the system will be nulled.

The direction that the read counter is to be pulsed is determined by the direction of movement of the IMU gimbal. For a positive change of IMU gimbal angle the read counter will be counted up and for a negative change in IMU gimbal angle the read counter will be counted down.

The computer will be kept up to date on the gimbal angle position by the $\pm\Delta\theta_G$ pulses issued from the first stage of the read counter. Each pulse equalling 20 $\overset{\frown}{\text{sec}}$ of gimbal angle.

During the coarse align mode of operation the read counter will be pulsed at a 6.4 kpps rate. $\Delta\theta_G$ pulses from the third stage of the read counter will be sent to the error counter of the pulses equal to 160 $\overset{\frown}{\text{sec}}$ of gimbal angle.

The switching effect that the read counter has on the Quadrant Select Module and main summing amplifier was discussed in sections 3.6 and 3.7.

The effect that the $\Delta\theta_G$ pulses, sent to the error counter and logic module, have on the error counter will be discussed in section 3.9.

3.9 ERROR COUNTER AND LOGIC MODULE

The error counter and logic (EC and L) module is, perhaps, the most complex of the modules of the CDU when considering total inputs, outputs, and interdependent logic circuit elements. The error counter and logic module contains, as the name implies, an error counter, the control logic to allow the error counter and read counter to operate properly, buffer amplifiers to isolate the counter from the D/A switches, and rate select circuits and control logic to select up or down read counter operation, and the rate at which the counter will operate. Figure 3-20 is a block diagram of the error counter and logic module.

The inputs to the EC & L module and the outputs from the module are numerous. There are also numerous signals generated and used within the EC & L module. Table 3-4 is a listing of the signals which will be encountered during the discussion of the EC & L module operation.

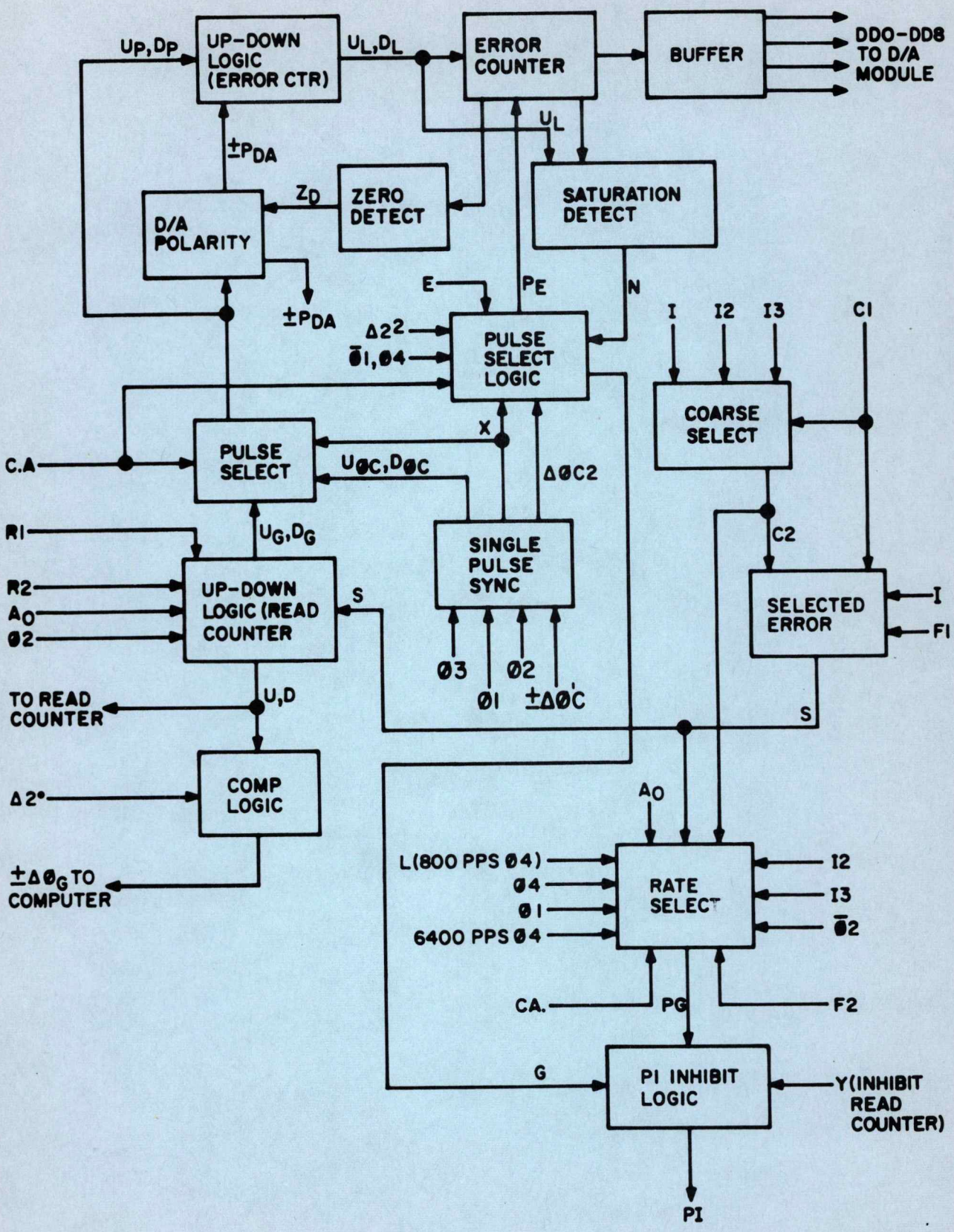


Figure 3-20. Error Counter and Logic Module Block Diagram

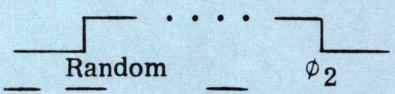
Table 3-4. EC & L Signal List

Letter Designation	Signal	Description
A_d	Ambiguity Detect	Secondary of the cosine 1X resolver Schmitt trigger output. 0ϕ for θ_G between 305^o and 55^o and $\pi\phi$ for θ_G between 125^o and 235^o.
A_o	Ambiguity Override	Issued whenever A_d is present. Forces the read counter to count to 225^o whenever there is a danger of the read counter nulling at an ambiguous angle.
CA	Coarse Align Discrete	CMC issued discrete, 0 level for issued discrete.
C_1	Coarse Ternary Level	800 cps, 0 or $\pi\phi$ square wave occurs when θ_E (θ - Ψ) is $\geq \approx 8^o$. Schmitt trigger fires at 1.6V P to P or greater. If $\pi\phi$ (180 out with respect to 800 ~ Ref. the read counter must count up. 0ϕ the read counter must cound down.
C_2	High Speed Clamp Signal	C_1 . I . M = output of coarse fine F. F. commands the incrementing read counter pulses at the high rate (12.8 kpps)
D	Down Level Command	= $SR_1 + A_o$ commands the read counter to count down. DC level which change only at $\phi 2$ time.
D_G	Down Gimbal Pulses	= $SR_1\ \phi_2$ sent to EC & L module to pulse the error counter up during coarse align. 12.8 kpps at ϕ_2 time.
D_P	Polarity Pulse @ ϕ_2	= $D_{\theta C} + \overline{X}\ C_A U_G$ will cause the error counter to be counted down during coarse align or when $-\Delta\theta_C$ pulses are received from the CMC.
D_L	Down Logic	= $(-P_{PA})$ Up + $(+P_{PA})$ D_P generated in the error counter up down logic. Used to determine up or down count in the error counter.
$D_{\theta C}$	Down CMC Pulse	Generated as a result of the receipt of a $-\Delta\theta_C$ pulse. Occurs at ϕ_2 time following receipt of respective $-\Delta\theta_C$ pulse.
E	Error Counter Enable Discrete	Required to enable pulses to be sent to the error counter.
F_1	Fine Ternary Level Signal	0 or $\pi\phi$ 800 cps square wave exists whenever θ_E $\widehat{20}$ to $\widehat{400}$ seconds equivalent gimbal angle causes read counter to be pulsed at low rate (800 pps) when F_2 and C_1 are not present.

Table 3-4. EC & L Signal List

Letter Designation	Signal	Description
F_2	High Ternary Level Signal	0 or $\pi\phi$ 800 cps square wave exists whenever $\theta_E \geq 0.1^o$ (20 x $\overline{20}$ sec). Causes read counter to be pulsed at high rate 12.8 kpps.
G	Gimbal Pulse Command Inhibit	= $CA\Delta\theta_{C2}$. X . $\overline{N}$ Duration of G is $\phi 1$ to $\phi 1$ time following receipt of a $\Delta\theta_C$ pulse. Inhibits the pulses to the read counter.
I	Interrogate Pulse	1600 cps timing pulse based on 800 cps ISS reference.
I_2 and I_3	Synchronization Pulses	Occur at $\phi 2$ and $\phi 3$ pulse following an I pulse. Act as synchronization between ISS and CMC reference timing.
M	Alternate Sync Pulse	Operates on the coarse select logic to prevent resetting the coarse fine F. F. on alternate interrogate pulses.
N	Saturation Detect	= U_L . 2^7 . 2^8 inhibits error counter U_p pulses when 2^7 and 2^8 stages are at a 1.
$\pm P_{DA}$	Polarity	Set and reset outputs of D/A polarity F. F. Used to apply either 0ϕ or $\pi\varphi$ 800 ~ to error counter ladder output.
P_E	Error Counter Input Pulses	= $E\overline{N}$ ($\Delta\theta_{C2}$ + $CA\ \Delta\ Z^2$) 3.2 kpps transmitted to the error counter at φ 4 time.
P_G	Read Counter Drive Pulses (High or Low rate)	High Rate = H [$S(C_2 + F_2) + A_o$] Low Rate = L [$S\ \overline{C}_2\ \overline{F}_2\ \overline{A}_o$] Sync pulse I_2, I_3, ϕ_1 and ϕ_2 allow change of P_G to high or low rate at next I_2 time preceding H or L pulse or upon receipt of A_o.
P_I	Read Counter Input Pulse	= P_G . $\overline{Y}$. $\overline{G}$ pulse rate of 12.8, 6.4 or .8 kpps to the read counter.
S	Selected Error	= I (C_1C_2 + $F_1\ \overline{C}_2$) 0 or $\pi\phi$ 800 cps. S is required by the up-down logic and rate select logic to determine direction and rate of read counter incrementation.
U	Up Level Command	= S $R_2\ \overline{A}_o$ commands the read counter to count up. DC Level which changes only at ϕ_2 time.
U_G	Up Gimbal Pulses	= S $R_2\ \varphi_2$ sent to EC & L module to pulse the error counter down during coarse align. 12.8 kpps at φ_2 time.

Table 3-4. EC & L Signal List

Letter Designation	Signal	Designation
U_L	Up Logic	= $(+P_{DA})$ Up + $(-P_{DA})$ D_P generated in the error counter up-down logic. Used to determine up or down count in the error counter.
Up	Polarity Pulse @ $\phi 2$	= $U_{\theta C}$ + $\overline{X}$ CA D_G will cause the error counter to be counted up during coarse align or when $+\Delta\theta_C$ pulses are received from the CMC.
$U_{\theta C}$	Up CMC Pulse	Generated as a result of the receipt of a $+\Delta\theta_C$ pulse. Occurs at ϕ_2 time following receipt of respective $\Delta\theta_C$ pulse.
X	Gate Signal	One pulse is generated each time the CDU receives a $\pm\Delta\theta_C$ pulse from the CMC exists from $\phi 1$ to $\phi 3$ time and inhibits read counter pulses to the error counter.
Y	Read Counter Inhibit	
Z_D	Zero Detect	= $\overline{2^0}$, $\overline{2^1}$ . . . $\overline{2^8}$ of the error counter. Prevents error counter from being counted down from zero.
Z	ISS CDU Zero Discrete	From CDU.
θ	Gimbal Angle	Represented by sine and consine of 1X and 16X resolver outputs.
Ψ	Read Counter Angle	
θ_E	Error Angle	Difference between θ and Ψ.
$\pm\Delta\theta_C$	CMC Pulse Train to CDU	Represents desired gimbal angle. 3.2 kpps max. rate to error counter @ 160 $\widehat{sec}$. per pulse.
$\pm\Delta\theta_G$	2^0 stage of Read Counter Output to CMC	Represents gimbal angles as accumulated in read counter. Stored in E memory location 32, 33, 34 of CMC.
B	Ambiguity Reset	= 2^{15} $\overline{2^{14}}$ $\overline{2^{13}}$ (225^o)
Q	Turn on Enable	Sets 90^o bit in the read counter (no longer used)

3.9.1 ERROR COUNTER AND LOGIC MODULE THEORY OF OPERATION. In the following paragraphs the logic flow between the many functional blocks of the EC & L module will be analyzed. The paragraphs of this section will identify the inputs and outputs to the functional blocks and it will be the responsibility of the reader to refer to table 3-4 and figure 3-20 for the required signal description and functional block relationships.

The EC & L module contains the logic circuitry controls for both the read counters and the error counters of the CDU.

3.9.1.1 Error Counter Logic Circuits. The first signal flow to be analyzed will be the inputs to the EC & L module which will result in pulsing the read counter and sending pulses to the computer.

Coarse Select. The coarse select inputs are I, M (I_2 and I_3), C_1 and F_1. The output of the coarse select circuitry is the signal C_2. Whenever a coarse error signal, C_1 is inputed to the coarse select, C_2 will be generated according to the logic equation: $C_2 = C_1 \cdot I \cdot \overline{M} \cdot C_2$ is then sent to the selected error circuitry.

Selected Error. The input to the selected error circuitry are I, C_1, C_2 and F_1. The selected error logic generates a select logic command, S. This signal is an indication to the rate select for the read counter and the read counter up-down logic that an analog error still exists and the read counter must continue incrementing its counter circuits at the rate selected. The signal, S, is generated when the logic equation $S = I (C_1, C_2 + F_1 \overline{C_2})$ is satisfied.

Rate Select. The inputs to the rate select logic are: S, C_2, A_o, I_2, I_3, $\phi 2$, $\phi 1$, $\phi 4$, 800 pps, CA and F_2. The receipt of an S signal from the selected error logic in conjunction with numerous other signals make it possible to generate an incrementing pulse train for the read counter.

These signals are logically manipulated to generate a pulse train, P_G, at rates of 800 pps, 6400 pps or 12.8 kpps. The logic equations are:

P_G = low rate (800 pps) = $L [SC_2 F_2 A_o]$.

P_G = intermediate rate (6400 pps) = (CA 6400 pps $\phi 4$) S.

P_G = high rate (12.8 kpps) = $\phi 4 [S (C_2 + F_2) + A_o]$.

Low rate, 800 pps at $\phi 4$ time, is generated whenever S is present, the coarse level signal is sufficiently nulled to prevent the firing of its Schmitt trigger generating C_1 and C_2, the fine circuit error signal is less than 4 volts P to P, preventing the high level Schmitt in the main summing amplifier from firing, and the ambiguity detect circuit does not indicate an ambiguity condition.

The intermediate counting rate, 6400 pps and $\phi 4$ time, is used only during the coarse align mode of operation which aids in limiting the maximum drive rates of the IMU gimbals to 35 degrees per second. This pulse rate will be generated whenever a coarse align command is present, whenever the error detect circuit indicates either the presence of a coarse or fine analog error (S), and whenever 6400 pps pulse train at $\phi 4$ is present.

The high count rate, 12.8 kpps at $\phi 4$ time, is generated whenever an analog error exists as indicated by S and either a coarse error (C_2) or a fine error above a certain level (F_2), is present. The high count rate is used after the coarse errors are sufficiently nulled to prevent the firing of the coarse Schmitt (C_1) and while the fine two (F_2) error Schmitt firing level is still exceeded.

A second means of generating a high counting rate is, if after the CDU zero discrete has been removed by the computer, an ambiguity override discrete is generated. When the A_o signal is injected into the rate select circuit, a high rate and down count command are generated causing the read counter to count to 225^o.

The timing signals, inputs to the rate select logic, are not required to generate a specific pulse rate. They are used to generate control pulses internal to the rate select circuit to change pulse rates at the next high or low rate pulse following in I_2 timing pulse or on receipt of the ambiguity override gimbal.

The P_G pulse generated according to the rate select logic equation is used to generate P_I according to the following logic equation: $P_I = P_G \overline{G} \cdot \overline{Y}$. Either of two control pulses, G, which is generated by the pulse select logic of the error counter, or U, a read counter inhibit command generated by the digital mode logic, can prevent the generation of the read counter incrementing pulses, P_I. Y is generated during a CDU zero command from the computer. The discrete resets the read counter and prevents the incrementing pulses from driving it. The G control pulse is a pulse that occurs every $\phi 1$ time period following a $\Delta \theta_C$ to the error counter. This will prevent the read counter from incrementing, and possibly from generating a $\Delta 2^2$ pulse from the 2^2 stage output at the time the error counter is incrementing the $\Delta \theta$ command. It is undesirable to have the error counter receive incrementing pulses simultaneously.

Up-Down Logic. In the discussion of the selected error logic, the output signal S was sent to the read counter rate select logic, which was discussed in the previous paragraphs, and to the read counter up-down logic. Along with the S the other inputs to the up-down logic are, R_1, R_2, A_o, and $\phi 2$. The logic equations to be satisfied to generate the read counter control outputs of the up-down logic circuits are:

$U = S R_2 \overline{A}_o$

$D = S R_1 + A_o$

U and D are sent to the read counter and control the direction the counter is incremented. U and D are also sent to the computer logic and are used to control the generation of the pulses sent to the computer.

The other control signals are generated in the up-down logic, U_G and D_G. The logic equation to be satisfied to generate these outputs are:

$U_G = S \cdot R_2 \cdot \phi 2$

$D_G = S \cdot R_1 \cdot \phi 2$

These two signals are used in the pulse selection logic for the error counter and will be discussed when the error counter signal flow is discussed.

Computer Logic. The inputs to the computer logic are $\Delta 2^{o}$, U and D. The logic equations to be satisfied to generate the $\Delta\theta_G$ pulses to be sent to the computer are:

$+\Delta\theta_G = U \cdot \Delta 2^{o}$

$-\Delta\theta_G = D \cdot \Delta 2^{o}$

3.9.1.2 Error Counter Logic Circuits. The signal flow to be analyzed now will be the inputs to the EC & L module which result in pulsing the error counter and sending signals to the D/A converter module.

Single Pulse Sync. The single pulse sync logic receives the $\Delta\theta_C$ pulses from the computer. Other inputs to the single pulse sync logic are $\phi 1$, $\phi 2$, and $\phi 3$ timing pulses. Four signals are generated within this logic according to the following logic equations:

$\Delta\theta_{C2} = [(+\ \Delta^1\theta_C) + (\ \Delta^1\theta_C)\ ]$

$U_{\theta C} = +\ \Delta^1\theta_C$

$D_{\theta C} = -\ \Delta^1\theta_C$

$X = C(\phi 1 - \phi 3)$

The $\Delta\theta C_2$ pulse is synchronized so that it occurs at the $\phi 2$ time following receipt of $\Delta^1\theta_C$ pulse. This pulse train at 3.2 kpps is sent to the pulse selection logic and is used in the logic which generates G.

The $U_{\theta C}$ and $D_{\theta C}$ occur at the rate of the $\Delta^1\theta_C$ input, 3.2 kpps maximum, and are synchronized so that they occur at $\phi 2$ time following receipt of the respective $\Delta^1\theta_C$ pulse. $U_{\theta C}$ and $D_{\theta C}$ are sent to the pulse selection logic.

X is a gate signal which occurs between $\phi 1$ and $\phi 3$ following receipt of a $\Delta^1\theta_C$ pulse. This signal is sent to the pulse selection logic and the pulse select.

From the single pulse sync two signal flow paths exist to control the error counter. One path, from the pulse select logic to the D/A polarity logic, to the up-down logic, determines the polarity of the pulse train sent to the error counter. The other path, from the single pulse sync to the pulse select logic to the error counter, generates the pulse train to the error counter. The path that determines the polarity of the pulse train will be investigated first.

Pulse Select. The inputs to the pulse select are X, $U_{\theta C}$, $D_{\theta C}$, U_G, D_G and CA. The pulse select generates two signals D_P and U_P according to the following equations:

$D_P = D_{\theta C} + \overline{X}\ CA \cdot U_G$

$U_P = U_{\theta C} + \overline{X}\ CA \cdot D_G$

These two signals are sent to the D/A polarity logic and the error counter up-down logic.

D/A Polarity Logic. In the D/A polarity logic the inputs U_P, D_P and Z_d (zero detect) are used to generate $\pm P_{DA}$ according to the following equations:

$$+P_{DA} = U_P \cdot Z_d$$

$$-P_{DA} = D_P \cdot Z_d$$

The $\pm P_{DA}$ signal is sent to the error counter up-down logic and to the D/A converter module which is another module in the CDU.

Error Counter Up-Down Logic. The inputs to the error counter up-down logic are $\pm P_{DA}$, U_P and D_P. The outputs are U_L and D_L and are generated according to the following equations.

$$D_L = (-P_{DA})U_P + (+P_{DA})\, D_P$$

$$U_L = (+P_{DA})\, U_P = (-P_{DA})\, D_P$$

D_L and U_L are sent to the error counter where they are used with the output of the pulse select logic to pulse the counter.

Pulse Select Logic. The inputs to the pulse select logic are X, $\Delta\theta_{C2}$, N, E, $\Delta 2^2$, CA, $\overline{\phi 1}$ and $\phi 4$. Two signals are generated in the pulse select logic according to the following equations:

$$G = CA \cdot \Delta\theta_{C2} \cdot X \cdot \overline{N}$$

$$P_E = E\overline{N}\,(\Delta\theta_{C2} + CA \cdot \Delta 2^2)$$

G is synchronized by $\phi 1$ so that G duration is $\phi 1$ through next $\phi 1$ following receipt of a $\Delta\theta_C$ pulse.

G is sent to the P_I inhibit logic whre it is used to inhibit the generation of the P_I pulses to insure that the read counter will not be pulsed at the same time that the error counter is receiving a $\Delta\theta_C$ pulse input. This, in turn, insures that the error counter will not simultaneously receive a $\Delta\theta_C$ and $\Delta 2^2$ pulse.

P_E is the pulse train which increments or decrements the error counter, at a maximum rate of 3.2 kpps at $\phi 4$ time.

Error Counter. The error counter is a nine stage binary counter. The nine stages, designated 2^0 to 2^8, provide an apparent capability of accumulating 2^9 or 512 pulses, but the counter is mechanized to saturate at 384 pulses. When saturation exists, an N control pulse is generated which is used to prevent the error counter incrementing pulses P_E from increasing the contents of the counter. This insures that no $\Delta\theta_C$ pulses will be lost due to over-counting the error counter.

The error counter, like the read counter, has the capability of being counted up or down. The error counter, however, will not count down through zero. The up or down counting direction is established by the presence of U_L or D_L signals. The contents of the error counter represent only the absolute value of the error angle. The sign of the error angle is determined by the polarity of the D/A converter output.

The polarity of the D/A converter output is controlled by the $\pm P_{DA}$ pulses generated in the D/A polarity logic of the EC & L module.

The error counter logic circuits are conditioned by the zero detect (Z_d) signal. Z_d is issued only when all stages of the error counter are at zero, and establishes the proper polarity to be associated with a magnitude recorded in the error counter. For example, if the error counter is at zero and the computer issued $-\Delta\theta_C$ pulses the counter cannot be counted in the negative direction. The EC & L logic is mechanized so that a Z_d signal will change the D/A polarity from positive to negative and to change the counting direction from down to up on the first $-\Delta\theta_C$ pulse received after zero is reached. In effect the counter is being counted up in a negative direction.

3.10 DIGITAL TO ANALOG CONVERTER MODULE

The digital to analog converter (DAC) module is used in conjunction with the error counter and logic module to generate IMU coarse align signals, attitude error signals for display on the FDAI and dc signals for steering of the SIVB or SPS. The DAC can be separated into two independent operations, digital to analog conversion, and mixing and demodulation.

The DAC inputs include $\pm P_{DA}$ polarity control signals from the EC & L module, nine switch control commands, a DAC inhibit signal, a 28V 1% 800 cps reference, a coarse input from the coarse module and a fine input from the main summing amplifier module.

The outputs of the DAC are a coarse align output, 800 cps signal, to the gimbal servo amplifier, an 800 cps 0 or π phase attitude error signal to the error needles of the FDAI, and DC steering signals. The DC signals from the CDU OSS error counters and DAC modules are used for control of the SPS engine gimbals during thrust vector control.

When the DAC is associated with the OSS operation allowing the CMC to drive the optics shaft or trunnion, the output labeled attitude error is used as a drive command.

The DAC module includes buffer circuits for $\Delta\theta_C$ commands from the computer. These outputs are recognized in the EC & L module as $\pm\Delta\theta'_C$. The $\Delta 2^0$ output from the read counter 2^0 stage is routed through the up-down logic of the EC & L module, comes out as a $\pm\Delta\theta'_g$. The $\Delta\theta'_g$ is buffered in the DAC module prior to the signal being transmitted to the CMC as a $\pm\Delta\theta_g$ pulse. The buffer circuits are not shown on the block diagram of the DAC, figure 3-21.

3.10.1 DIGITAL TO ANALOG CONVERTER THEORY OF OPERATION.

The digital to analog conversion performed in the DAC is accomplished by a ladder decoder arrangement. The ladder switching is controlled by transistorized switches and switch driver circuits which receive their inputs from the error counter in the EC & L module. The ladder outputs are then modified by the DAC output circuit.

3.10.1.1 Digital to Analog Conversion.

Digital to analog conversion in the DAC is accomplished through a ladder decoder. The operation of a typical ladder will be described prior to describing the operation of the entire D to A conversion circuit shown in figure 3-21.

A simplified three bit ladder decoder is shown in figure 3-22. A three bit ladder is described here; however, the nine bit ladder of the DAC functions in exactly the same manner. For illustration purposes, make the assumption that the switches S0, S1, and S2 are controlled by the three least significant bits of the error counter of the EC & L module.

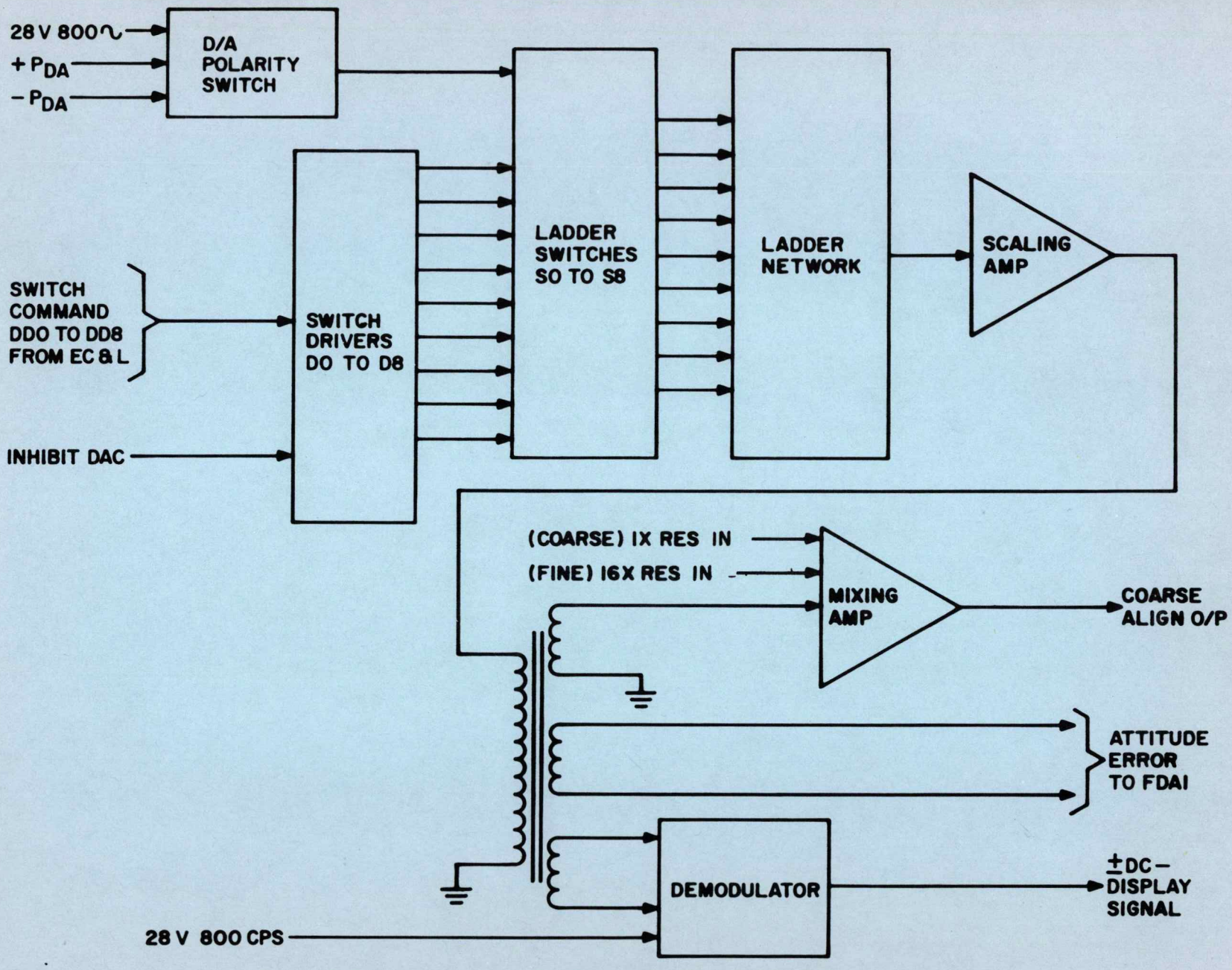


Figure 3-21. Digital to Analog Converter Module Block Diagram

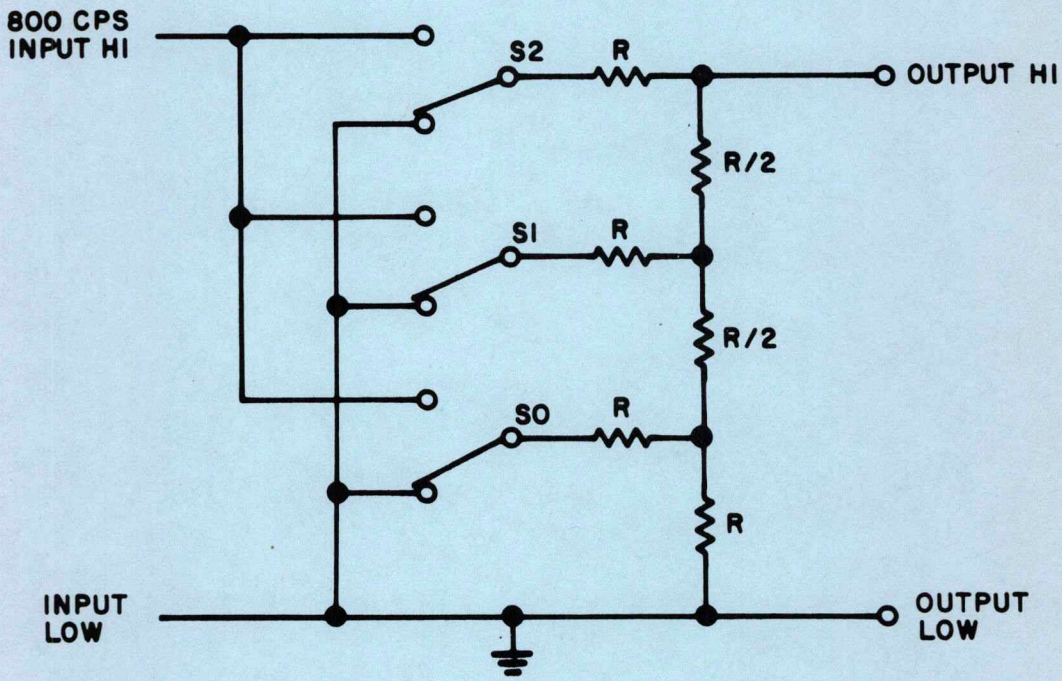


Figure 3-22. Ladder Decoder - Simplified

The resistors of the ladder network are designated as R and R/2-, one value being two times as large as the other. R in the actual DAC ladder is a 50,000 ohm resistance, the R/2, a 25,000 ohm resistance.

It can be shown by series parallel resistance combinations that the resistance to ground at the output point is going to be equal to R/2 regardless of which switch configuration is used, when it is assumed that the dc resistance of the 800 cps input source is zero ohms. With all of the switches opend, as shown, the output voltage level is 0V (rms). If switch S2 is closed, connecting the 800 cps input to the ladder, the input Voltage Vin is divided by two, giving an output V_o of $\frac{Vin}{2}$.

Figure 3-23 illustrates the actual circuitry and equivalent resistance circuit. It can be seen from the equivalent circuit that the output voltage is exactly equal to half the input voltage.

By the use of series-parallel resistance circuits, it can be shown that when S1 alone is closed the output voltage is equal to $\frac{Vin}{4}$, and that when S2 along is closed Vout is equal to $\frac{Vin}{8}$. If a combination of switches is closed, the output will be the sum of the values when individual switches are closed.

Table 3-5 is a truth table which shows how the output voltage will vary for the various switch combinations assuming an input voltage, Vin, a 1 to signify a closed switch, and a 0 to signify an open switch.

The output steps shown in figure 3-24 are not dc steps as shown, but in reality are 800 cps zero or pi phase signals from the 800 cps 1% power supply. The phase of the signal is determined by the $\pm P_{DA}$ circuit located in the EC & L module. In the 9 bit encoder used there are 512 steps from 0v to full output voltage in place of the 8 steps shown. The input voltage to the ladder is 2.50 v(rms) from a step down transformer in the DAC module.

Control of the ladder is provided through the D/A polarity switch, ladder switches S0 to S8, and switch drivers D0 to D8. DAC polarity in reality ladder output phase is controlled by the polarity switch which in turn is controlled by the up-down logic of the EC & L module. The polarity switch contains a transfomer with a center tapped secondary. The center tap to ground line contains a zener diode and capacitor circuit which, whenever the ladder decoder is enabled, provides a positive 4.7 volts bias to a transistor. This controls the grounding of the ladder when a switch is opened. If the switches are all open, the ladder will have a zero output.

The two legs of the transformer each contain a transistor switch which is controlled either by a $+P_{DA}$ or $-P_{DA}$. If the $+P_{DA}$ is selected, the zero phase output of the transformer will supply the ladder excitation voltage. When $-P_{DA}$ is selected, the π phase output is used. Figure 3-25 shows a more detailed view of the mechanization of one stage ladder switching circuits and polarity select. Q4 applies an in-phase reference to the ladder and Q5, when turned on provides the π phase reference to the ladder.

When the error counter stages are at 0, the swtich control signal DDO input to the DAC is at a logic 0 level (+4v), allowing the switch driver transistor Q1 to conduct. The conducting Q1 applies a 0v level to the base of Q3, which when combined with the +4.7 vdc on the emitter, biases Q3 into conduction and prevents Q2 conduction. Q3 when conducting provides an ac ground to the ladder giving 0 v(rms) output.

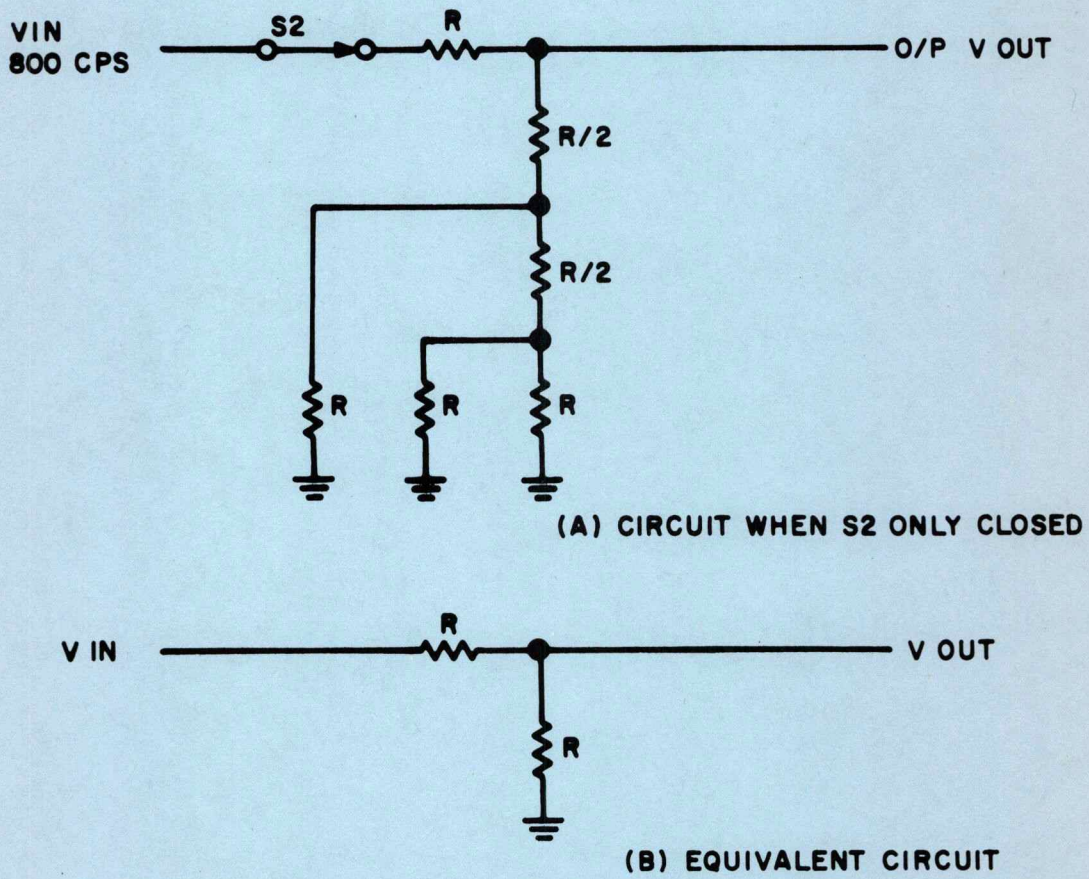


Figure 3-23. Ladder Circuit With S2 Closed

S0	S1	S2	V OUT
0	0	0	0
1	0	0	VIN/8
0	1	0	VIN/4
1	1	0	3/8 VIN
0	0	1	VIN/2
1	0	1	5/8 VIN
0	1	1	3/4 VIN
1	1	1	7/8 VIN

Table 3-5. Ladder Decoder Truth Table

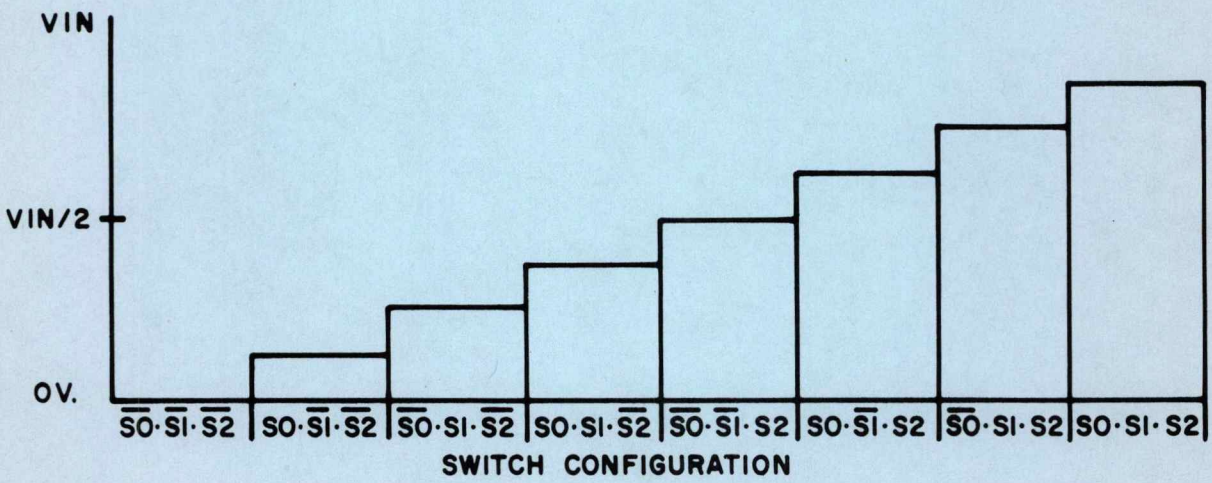


Figure 3-24. Ladder Output Voltage

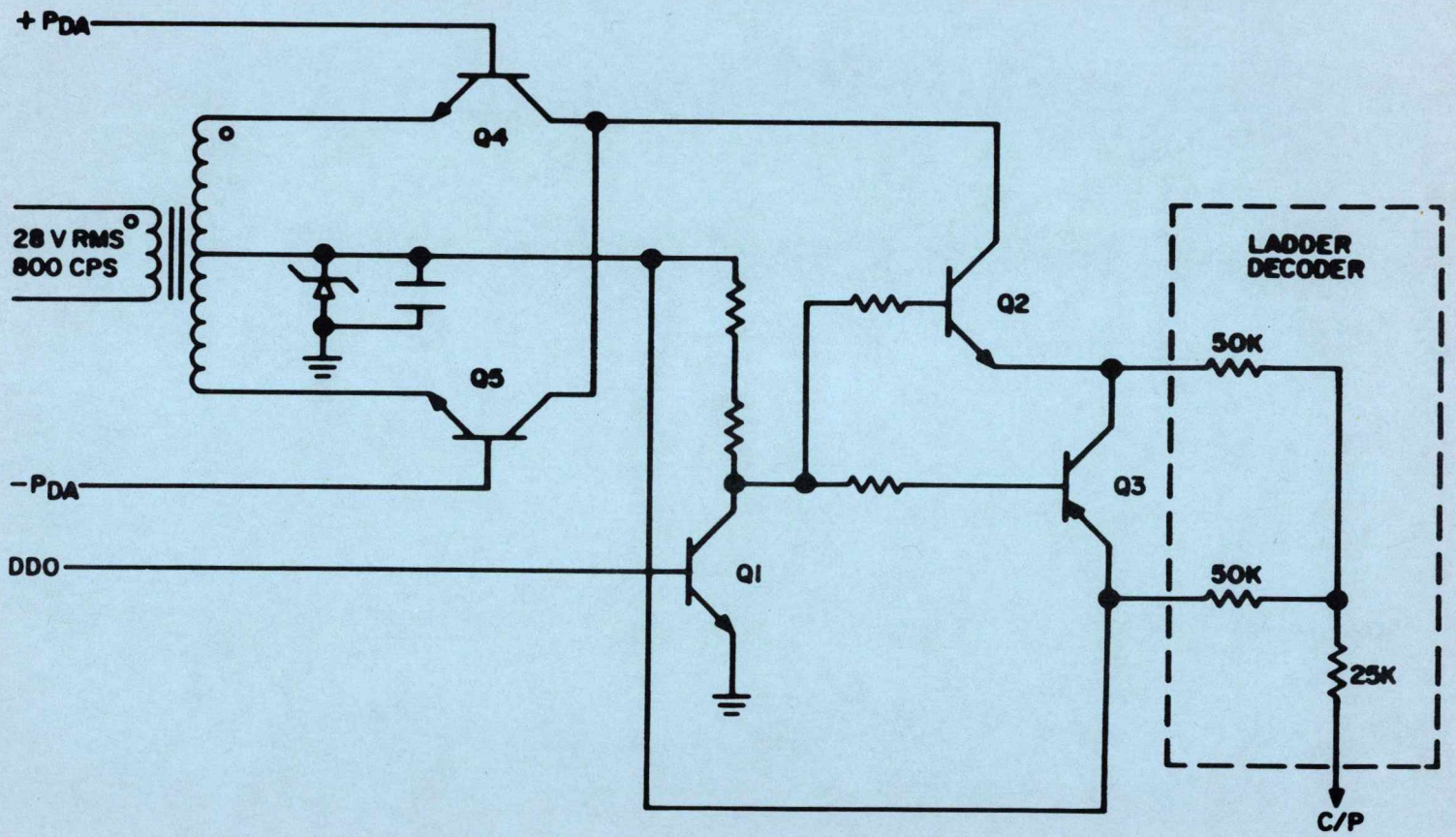


Figure 3-25. DAC Polarity and Ladder Switch Control

When a polarity select, $+P_{DA}$, command is present and Q4 is conducting and a switch command DDO goes to a logic 1 level (0 vdc). Transistor Q1 cuts off, removing the ground from the base of Q3. Q3 is thus biased into cutoff removing the ac ground from this leg of the ladder. When Q1 is cut off the base of Q2 is biased positive with respect to the emitter, thereby allowing Q2 to conduct connecting the 2.5v(rms) zero phase input through conducting Q4 and conducting Q2 to the ladder decoder.

All nine switch inputs to the ladder decoder are mechanized in the same manner as the one shown in figure 3-25. The transformer input, 4.7vdc bias, and polarity select switches are common to all nine ladder switch stages.

The ladder decoder output is amplifierd by a scaling amplifier whose gain is set to give a decoder output of approximately 13.2 mv/pulse where each pulse is equivalent to 160 arc seconds of gimbal angle error. Another way of stating the scale factor is ±300 mv output per degree of error.

The saturation level output of the DAC is equivalent to 384 counts in the error. When this value is combined with the data in the above paragraph, it can be seen that the maximum DAC output is ±5.1 vdc or ±17° of error total displacement.

The scaling amplifier output is transformer coupled and applied to three output circuits.

3.10.1.2 DAC Module Mixing and Output Circuits. The three transformer coupled outputs of the scaling amplifier serve three separate purposes and therefore are treated in three ways. The simplest circuit output is the direct output to the FDAI. The 800 cps in phase or out of phase signals are routed via the main display and control panel switches to the attitude error needles of the FDAI when considering the CDU-ISS channels. These outputs of the CDU-OSS channel DAC's are used as trunnion or shaft drive signals to the motor drive amplifiers of the sextant.

The demodulator in the output circuit is referenced to an 800 cps 28-volt, 1% power supply. The demodulator is a phase sensitive device giving a positive dc output voltage when the ladder output is in phase with the reference and a negative output voltage when the ladder output voltage is out of phase with the reference. The outputs from the CDU-ISS channels include pitch, yaw, and roll steering signals which are routed through the SIVB relay in the mode module to the SIVB IU. The CDU-OSS D/A converters generate the dc pitch and yaw steering signals for SPS steering. These signals are routed through the TVC relay in the mode module.

The DAC mixing amplifier, used only in the CDU-ISS DAC, are used to generate the 800 output needed to coarse align the IMU gimbals. During the coarse align mode, the 800 cps signal is used to drive the gimbals at a maximum rate of 35 degrees per second. The ladder decoder output is mixed with two signals to provide rate limiting. A coarse signal which is proportional to sin $(\theta-\Psi)$, θ being the actual gimbal angle and Ψ being the read counter indicated gimbal, is fed back out of phase with the ladder decoder output. The sin $(\theta-\Psi)$ signal is generated in the CDU coarse module.

A second rate limiting signal is taken from the main summing amplifier module. This signal is proportional to sin $16(\theta-\Psi)$. The fine rate feedback signals provide the primary drive rate control. A special 6400 pps read counter incrementing pulse rate was incorporated into the CDU for use during coarse align to prevent the read counter from counting within 20 pulses of the actual gimbal angle. This allows the rate limiting using the fine signal output to control the drive rate at 35 degrees per second maximum.

3.11 INTERROGATOR MODULE

The interrogator module, a module shared by the five CDU channels, is used to generate a portion of the timing pulses required for CDU operation. A single module of this type is located in the CDU. The interrogator module inputs are:

a. +4 vdc from the power supply.

b. ISS and OSS 28 vdc.

c. ISS and OSS 28v 1% 800 cps.

d. 51.2 kpps pulse train from the CMC.

e. Trunnion cosine ($\theta - \Psi$) from the main summing amplifier.

f. 25.6 kpps from the digital mode module.

g. CDU zero discrete.

The interrogator outputs include:

a. 51.2 kpps pulse train from the digital mode module.

b. 1600 pps interrogate pulse train (ISS).

c. 1600 pps interrogate pulse train (shaft).

d. 1600 pps interrogate pulse train (trunnion).

e. 800 pps $\angle 0^{o}$ reference (R1) (ISS).

f. 800 pps $\angle 0^{o}$ reference (OSS shaft).

g. 800 pps $\angle 45^{o}$ reference (OSS trunnion).

h. 14 vdc for CDU OSS channels.

3.11.1 INTERROGATOR MODULE THEORY OF OPERATION. The interrogator module contains a number of individual circuits, each of which perform a separate function. Figure 3-26 illustrates the major circuits located in the interrogator module.

3.11.1.1 Timing Circuits. Section 3.4 discussed the generation of the timing signals required in the CDU. In doing so the operation of the ISS reference generator (R_1), ISS, shaft and trunnion interrogate pulse generator (I), and the other timing signal generators in the interrogator module were discussed.

The only circuit in the interrogator module left to be discussed is the 14 VDC power supply.

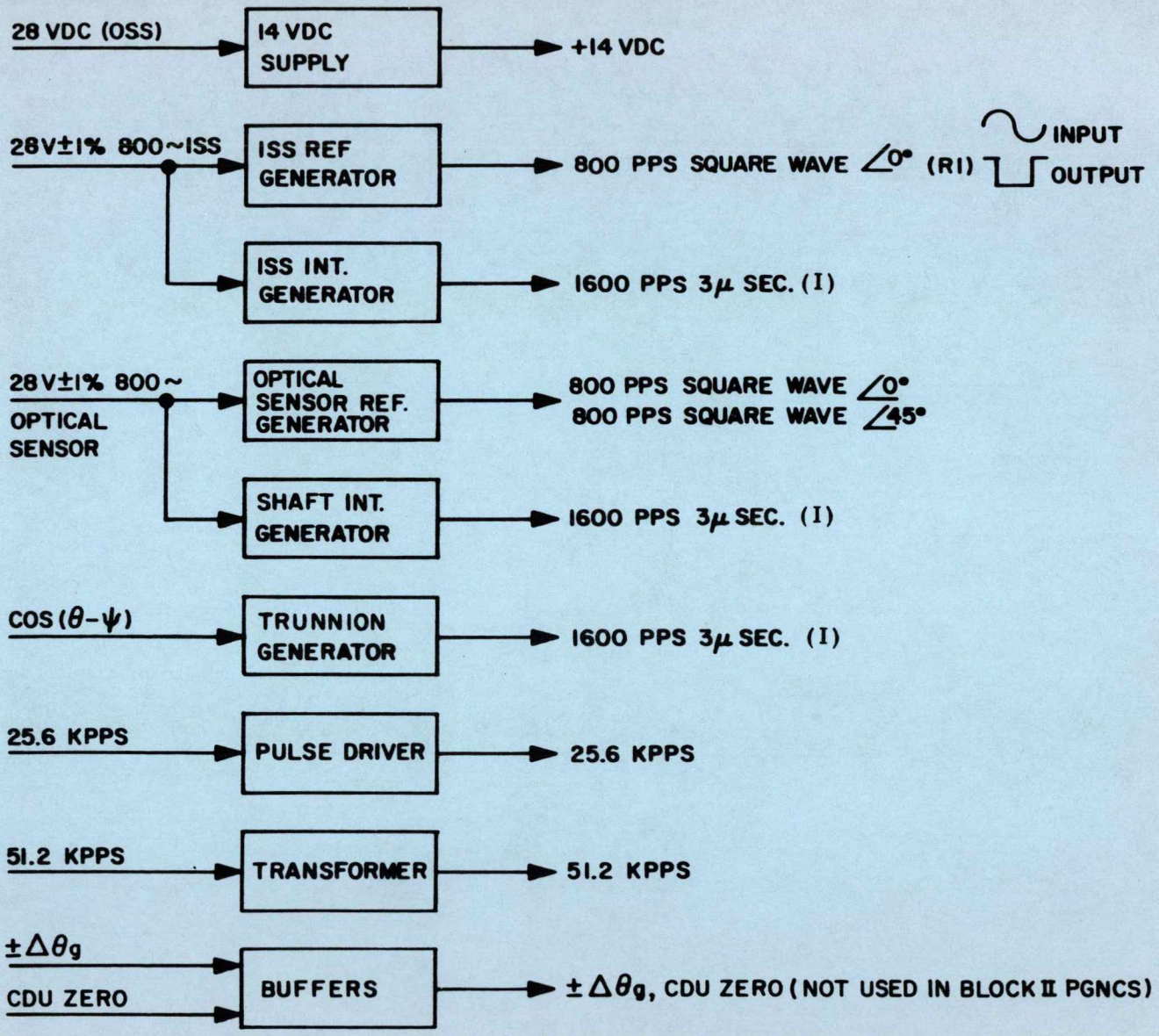


Figure 3-26. Interrogator Module Block Diagram

3.11.1.2 14 VDC Power Supply. The input power for the 14 VDC power supply is 28 VDC. The power supply consists of a single transistor whose bias level is controlled by a zener diode. The power supply outputs provide 14 VDC to the mode module, the D/A converter, and the CDU test connector.

3.12 DIGITAL MODE MODULE

The digital mode module is the fourth type of module in the CDU that is common to the five channels of the CDU associated with the inertial and optical subsystems. The module is used to generate timing pulses, develop mode control signals, and determine whether an ambiguity condition exists. The digital mode module inputs include:

a. Timing and interrogate pulses from the mode module.

b. Ambiguity detect signals from the coarse modules.

c. Moding commands from the mode module.

The digital mode module outputs include:

a. Timing pulses, interrogate pulses and phase drive pulses.

b. Ambiguity override signals.

c. Moding control signals.

3.12.1 DIGITAL MODE MODULE THEORY OF OPERATION. The digital mode module is made up of eleven independent circuits, several of which are identical in operation. A simplified block diagram of the module is shown in figure 3-27.

Section 3.4 discussed the generation of the timing signals required in the CDU. In so doing the operation of the pulse generator, the I_2, I_3 generator, the countdown circuit and the clock and logic circuit was discussed. The remaining circuits in the digital mode module will be considered in this section.

3.12.1.1 Ambiguity Logic. Inherent in the operation of the IMU and the CDU two ambiguous alignment conditions may exist. One is the zeroing of the gimbal angles during the ISS turn on mode, the other ambiguous condition develops as a result of the two gimbal angle positions which represent null conditions for any one read counter indicated angle.

The ISS Turn on Mode originally used the DAC output with the read counter zeroed to zero the IMU gimbals. To insure that the IMU gimbals would not null at an ambiguous angle ambiguity detect circuitry was designed into the CDU that would insure both the IMU gimbals and the read counter being at zero at the end of the IMU Turn on Mode. The ISS Turn on Mode (refer to ISS Turn on Mode, Paragraph 4.1) now uses the Sin θ output of the 1X resolver to drive the gimbals to zero. The possibility of the gimbals nulling at 180° instead of 0° was in this way eliminated, since the gain of the loops make it nearly impossible for the gimbals to remain in an unstable null of 180° for the 90 second duration of the Turn on Mode. The ambiguity detect circuitry originally designed into the CDU for the IMU Turn on Mode is no longer used.

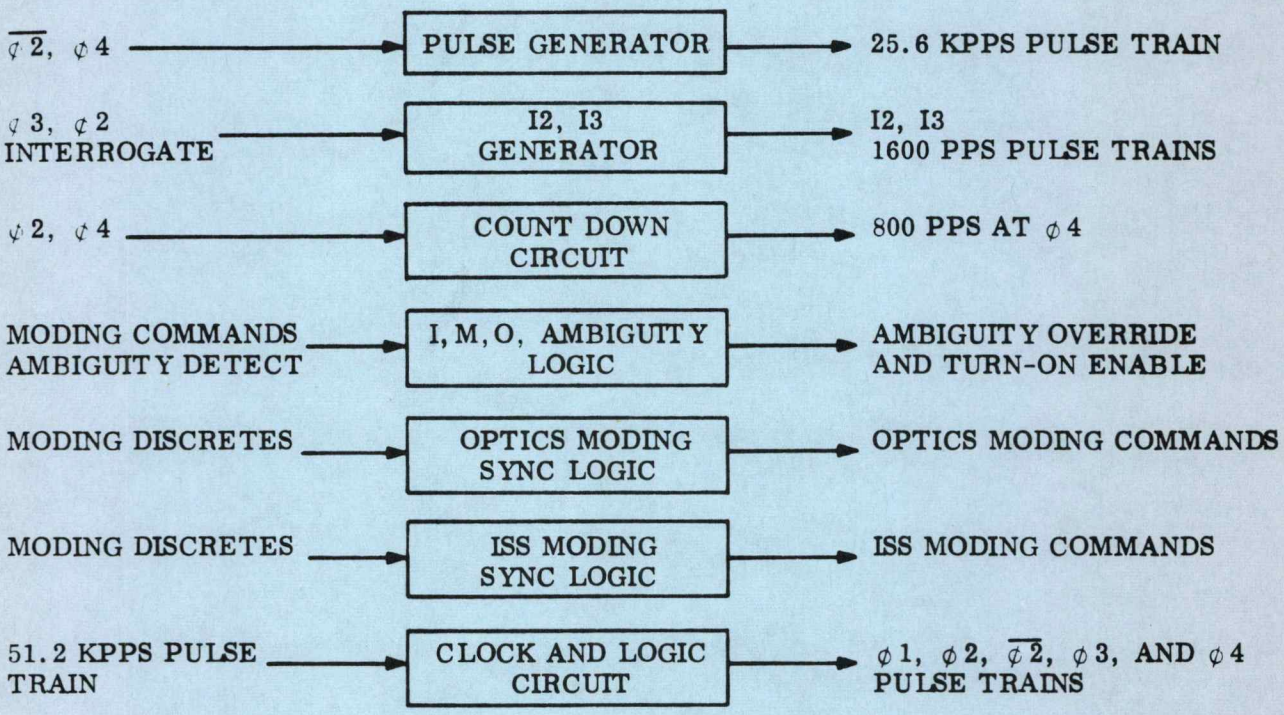


Figure 3-27. Digital Mode Module Block Diagram

In CDU ZERO mode (refer to paragraph 4.2) the read counter is set to zero and allowed to count up again to the gimbal angle. Before the read counter is enabled, however, the 1X cos θ resolver winding is level detected and interrogated with an out-of-phase signal to determine if the gimbal is in the vicinity of 225°. The cos θ signal is out-of-phase when the gimbal is between 90° and 270°. The level gives information to narrow the band of angles containing the ambiguity.

The level detection is made by an emitter follower driven Schmitt trigger in the coarse system module (reference figure 3-8). The firing level of the Schmitt is set at 7.0 V P-P measured at the output of the emitter follower. The Schmitt trigger output is buffered and transformer coupled to the Digital Mode Module where it is "anded" with the interrogate pulse (I) and the out-of-phase reference pulse (R_2). If an out-of-phase signal is detected, the control flip-flop is set and the ambiguity flip-flop is allowed to be set at the first phase 2 time following an interrogate (see figure 3-27A). An ambiguity override signal, A_O, is generated at the completion of CDU ZERO and sent to the Error Counter and Logic Module. It forces the rate-select logic into high speed (12.8 K PPS) and the up-down logic into countdown. The CDU counts down at high speed until it reaches 225° at which time the ambiguity flip-flop is reset by "B" removing the ambiguity override signal. The normal CDU operation will complete the CDU-gimbal readings now that the CDU is out of the ambiguity zone.

3.12.1.2 ISS Moding Sync Logic. The moding of the inertial subsystem is controlled by the CMC generation of a number of discrete signals including:

a. ISS CDU zero (Z).

b. Coarse align (CA).

c. Error counter enable (E).

The first three of these signals are modified by the mode sync logic prior to their being used to control the ISS modes of operation. The modification consists primarily of setting the signals to the CDU logic levels and time phasing the random CMC discretes to be compatible with the CDU internal timing. The moding discretes are routed from the CMC interface through the moding buffers in the mode module. The signals are inverted by the mode module moding buffers. The computer discretes are 0 vdc signals when commanded. The mode sync logic inverts the buffer outputs.

Within the mode sync circuit a digital mode coarse align discrete is generated in addition to the coarse align discretes for the I, M, O channels of the CDU. An inhibit read counter moding command (Y), for use within the CDU, is generated in the mode sync logic by either a CDU zero (Z) discrete or a coarse align discrete (CA), and not an enable error counter (E) discrete.

3.12.1.3 OSS Moding Sync Logic. The optical channels of the CDU require computer discretes for control of CDU operation during sensor moding in the same manner as the inertial subsystem. The computer issues the following discretes associated with the optical CDU channels:

a. OSS CDU zero.

b. OSS coarse align.

c. Error counter enable.

d. Thrust vector control.

Again as in the ISS moding circuits, the first three discretes are buffered by the circuits in the mode module. The buffered signals are then converted to the proper logic levels for CDU moding controls. An OSS read counter inhibit command is generated for CDU internal use whenever the OSS CDU zero discrete is issued by the computer.

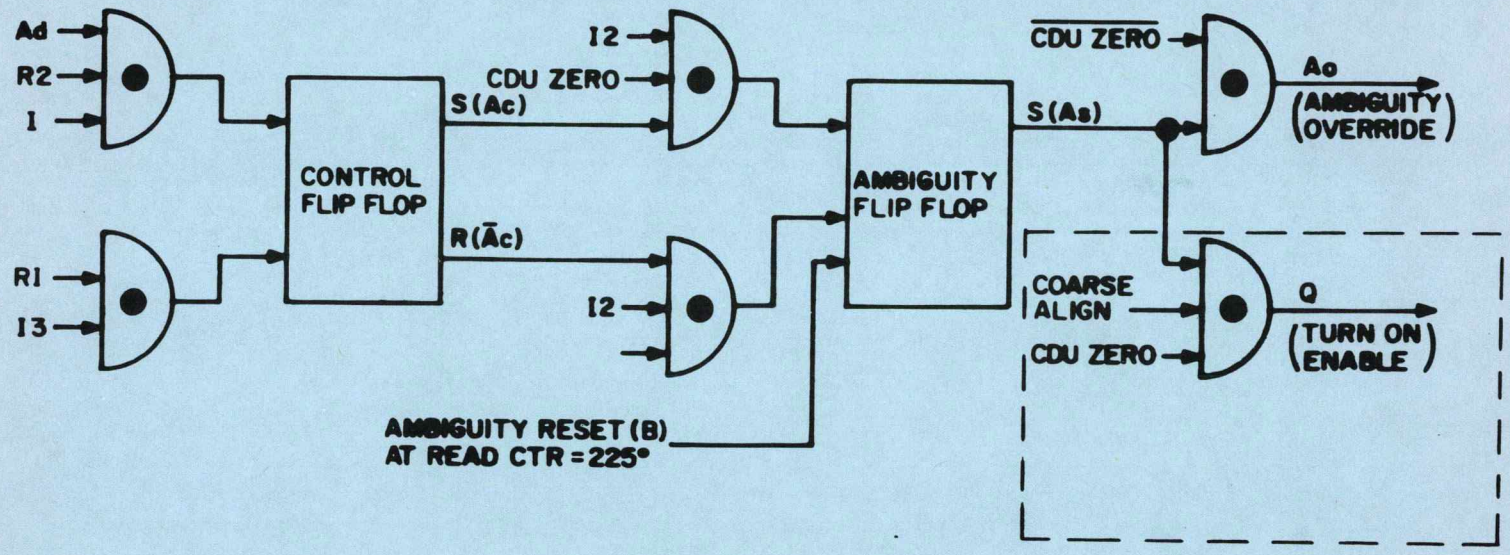


Figure 3-27A. Ambiguity Logic

3.13 MODE MODULE

The mode module of the CDU is utilized primarily as an interface module. This module contains circuits to buffer signals and monitor CDU operation . Direct interface is made between this module and the CMC.

The inputs to the module include:

a. CMC generated mode signals.

b. Timing signals used in the CDU counting circuits.

c. Read counter up line (5 lines).

d. Coarse and fine resolver signals from the coarse modules and the main summing amp modules.

e. ISS and optical subsystem 28 vdc.

f. Analog signals proportional to cos ($\theta - \Psi$).

g. Power supply inputs (4 and 14 vdc).

h. DAC dc generated steering signals.

The mode module outputs include:

a. Buffered moding signals.

b. Four timing signals.

c. ISS and OSS CDU fail signals.

d. 14 vdc power supply output.

e. Steering signals.

3.13.1 MODE MODULE THEORY OF OPERATION. The mode module contains six circuits which will be described separately. (See figure 3-28.)

3.13.1.1 Moding Buffer Circuits. The moding buffer circuits receive inputs from the CMC and the digital mode module. The inputs are the computer discretes: (1) ISS CDU zero, (2) ISS error counter enable, (3) OSS CDU zero, (4) OSS error counter enable, (5) CDU zero drive, (6) OSS CDU zero drive, and (7) ISS coarse align. The buffer circuits for discretes 1 through 4 are identical. The CMC discrete, a zero voltage level for a command, turns on the buffer stage increasing its output voltage to four volts, or a logic zero level as used in the CDU logic mechanization. The transistor bias voltage is taken from either the ISS or the OSS 28 vdc power bus depending on which of the two are present. The logic zero level signal from the moding buffers is used as a drive signal to the digital mode module.

The ISS and OSS CDU zero drive buffers receive a drive signal from the digital mode module. These signals are at a logic one level (0 vdc) when the computer is commanding a CDU zero. The buffer inverts the signal, thereby giving a CDU zero signal in the circuit a logic 0 level when the CMC commands a zero. These signals are routed to the read counter modules, the error counter and logic module and the interrogate module. The logic power for the drive buffers is provided by the 4 vdc CDU power supply.

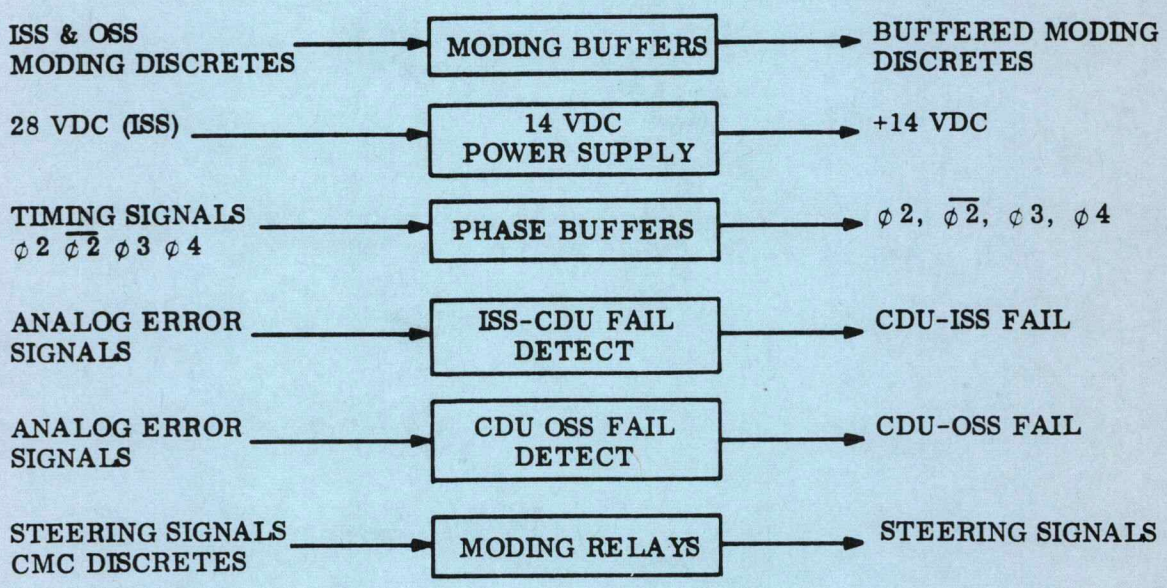


Figure 3-28. Mode Module Block Diagram

The ISS coarse align buffer circuit provides two separate outputs. The buffer consists of a two stage circuit. The first stage accepts the 0 vdc computer discrete and biases a transistor into conduction. The positive going voltage output of the transistor stage is recognized in the CDU as a coarse align discrete. The same signal is used to bias a transistor into conduction. This transistor provides a ground path for the IMU coarse align relay current thereby allowing the relays to energize. The relays are located in the PSA.

3.13.1.2 14 vdc Power Supply. The 14 vdc power supply located in the moding module is identical to the power supply in the interrogator module description. The source of input power for this supply is ISS 28 vdc operate power.

3.13.1.3 Phase Buffer Circuits. The phase buffer inputs include $\overline{\phi 2}$, $\phi 2$, $\phi 3$ and $\phi 4$ drive signals from the digital mode module phase generator circuit. These signals are inverted by a single stage transistor amplifier. The bias supply for the amplifier is provided by the 4vdc CDU power supply. Each buffer circuit is slightly different in design from the other three since each is required to drive varying loads. The phase signals are routed to the error counter and logic module, the read counter module, and the digital mode module.

3.13.1.4 ISS CDU Fail Circuits. The ISS CDU fail circuits can be separated into several independant error detect and logic circuits. The circuits are divided into groups depending on the type of signal being checked for error. Figure 3-29 is a logic block diagram of the CDU error detect circuitry.

Figure 3-29 (a) illustrates the type of error detector circuitry used to determine whether either the coarse error (1X resolver) or the fine error (16X resolver) signals are nulling as they should. The level detectors rectify the 800 cps input signals and charge the capacitor on the driver base circuit. When the coarse signal exceeds 2.5 v (rms) or the fine signal exceeds 1v (rms) the capacitor change is sufficient to bias the transistor into conduction. Any one of the six circuits will cause OR gate (1) in figure 3-29 (c) to provide an input to OR gate (4) the output gate.

Figure 3-29 (b) is one of the circuits used to detect the limit cycling of the up line in the read counter when the CDU read counter contains the gimbal angle. In this loop as in any servo loop when the loop is nulled a slight oscillation occurs around the null. The error detect circuit recognizes the changing phases of the signal around null and causes an up line energization or a down line energization to the read counter. Under normal operation this limit cycle is expected to be less than 250 cps. The limit cycle frequency is checked by the up line limit cycle square wave biasing a transistor on or off. The square wave output of the transistor is differentiated by the RC circuit in its load. The positive spike of the differentiated output is used to charge a capacitor through a diode. The charge on the capacitor is low enough when the limit cycle is less than 250 cps to bias the transistor at cutoff. When the limit cycle exceeds 250 cps the output transistor is biased into conduction. Point (1) in the circuit is the tie point to the common output transistor for the remaining two limit cycle detectors. These inputs feeding the one output transistor make up OR gate (2) in figure 3-29 (c). Any one of the three up lines limiting cycling at too high a rate will cause a fail input to OR gate (4).

Or gate number 3 of figure 3-29 (c) is used as a low level detect circuit. The signals cos $(\theta - \Psi)$ from the main summing amplifier module are checked to determine whether their level drops below 3.5v (rms). If either of these three signals drops below the set level, or the mode module 14 vdc supply drops below 10 vdc the OR gate will give a fail indication.

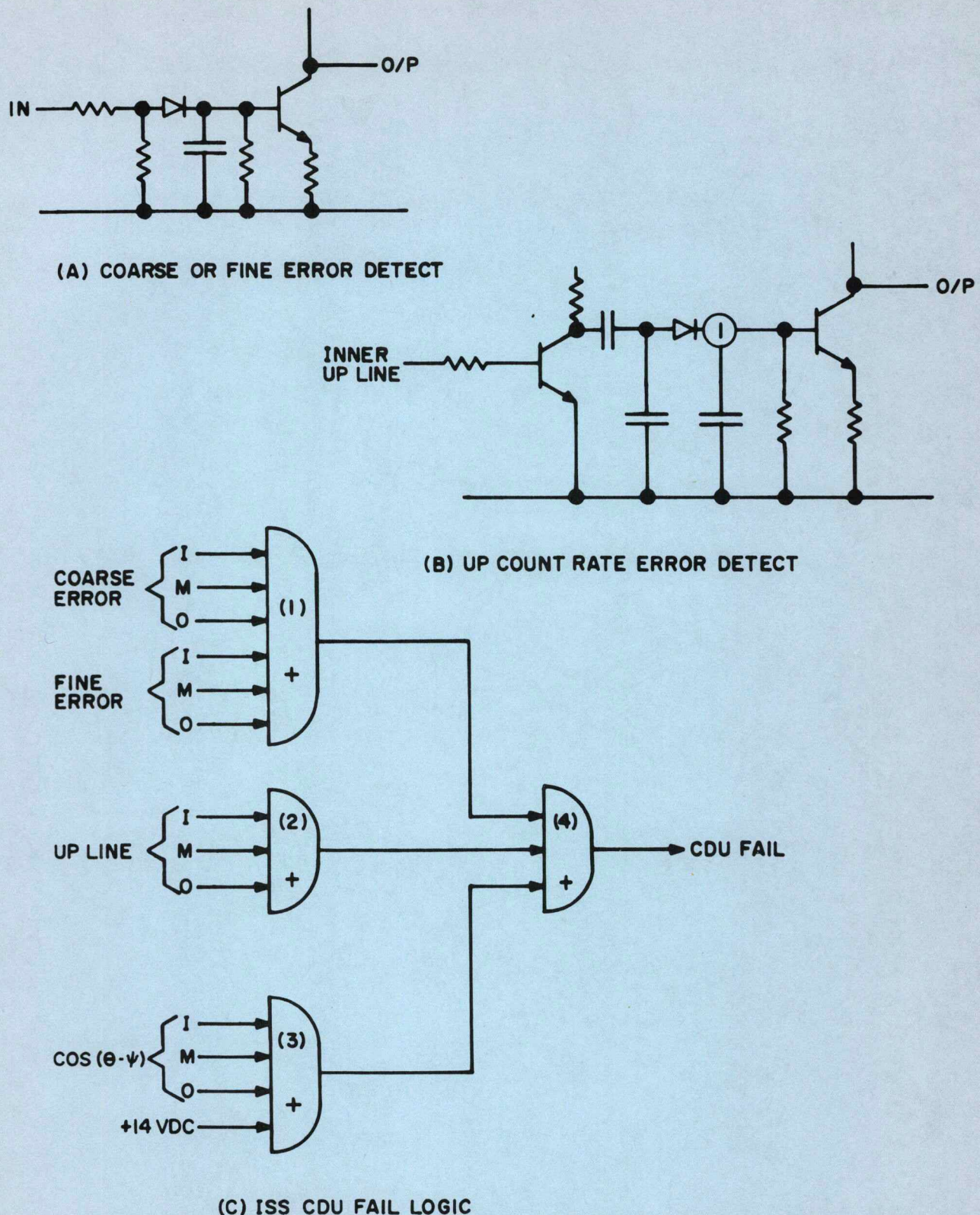


Figure 3-29. CDU Error Detect Circuitry

The output OR gate will accept inputs from the other three OR circuits. If any one of the 13 signals fails to meet the requirements, the CMC receives a CDU fail signal from the fail detect circuit.

3.13.1.5 OSS-CDU Fail Circuit. The OSS-CDU fail circuitry in the mode module performs in exactly the same manner as the fail circuitry for the ISS-CDU. The signal inputs are from the shaft and trunnion channels.

3.13.1.6 Moding Relays. Two sets of relays are contained in the CDU mode module. A set consists of two relays operated in parallel. The relays are used to route steering signals through the mode module. The circuit used for thrust vector control is shown in figure 3-30. The discrete necessary to energize the relay is generated by the CMC. The CMC discrete provides a relay ground through a transistorized relay drive circuit. The energized relays route dc signals developed by the OSS CDU DAC's to the SPS gimbal servo amplifiers. The 28 vrms 800 cps ISS power is applied to the OSS CDU DACS for this mode as the OSS is not necessarily energized during TVC maneuvers.

A second set of relays in the mode module is used to route pitch, yaw and roll steering signals generated in the CDU ISS DACS to the SIVB instrument unit.

3.14 CDU 4 VDC POWER SUPPLY

The 4 vdc power supply shown in figure 3-31, is used to provide regulated output voltage for use in the logic circuitry of the digital mode module, the read counter module, and the error angle counter and logic module. Under full load conditions the power supply is required to provide 4 vdc ±1% at 2.5 to 3 amps of current.

3.14.1 POWER SUPPLY THEORY OF OPERATION. The 4 vdc power supply of the CDU is typical of the power supplies used within the subsystems of the Apollo PGNCS in that it requires a synchronization pulse to drive a multivibrator.

The synchronization pulse, a 25.6 kpps pulse train, is generated in the interrogator module using a 51.2 kpps computer pulse train. The pulse train is inverted and used to key a multivibrator at a 12.8 kc frequency. In the event that the sync pulse should be lost, the multivibrator can free run at approximately 11.5 kc, thereby maintaining a logic power supply in the event a portion of the interrogate module fails.

The 12.8 kc output of the multivibrator is transformer coupled to a driver amplifier stage which has a push pull output circuit. The dc excitation level to the output stage is controlled by a regulator circuit to limit the maximum output voltage from the driver circuit.

The driver output is transformer coupled to a rectifier and filter circuit which normally provides a plus 4 vdc ±1% output. The output voltage is regulated by the comparison and regulator circuit. The 4 vdc output is compared with a reference voltage by a dc differential amplifier. The differential amplifier controls the impedance of a series regulator circuit by controlling the bias on two transistor regulator circuits. When the supply output is 4 vdc, the regulator provides a nominal dc bias to the driver output stage.

If the power supply output increases above the 4 volt level, the differential amplifier in the comparator and regulator block increases the impedance of the series regulator transistors, decreasing the bias voltage to the driver output and thereby reducing the output voltage level. A decrease in output voltage causes the inverse to be true.

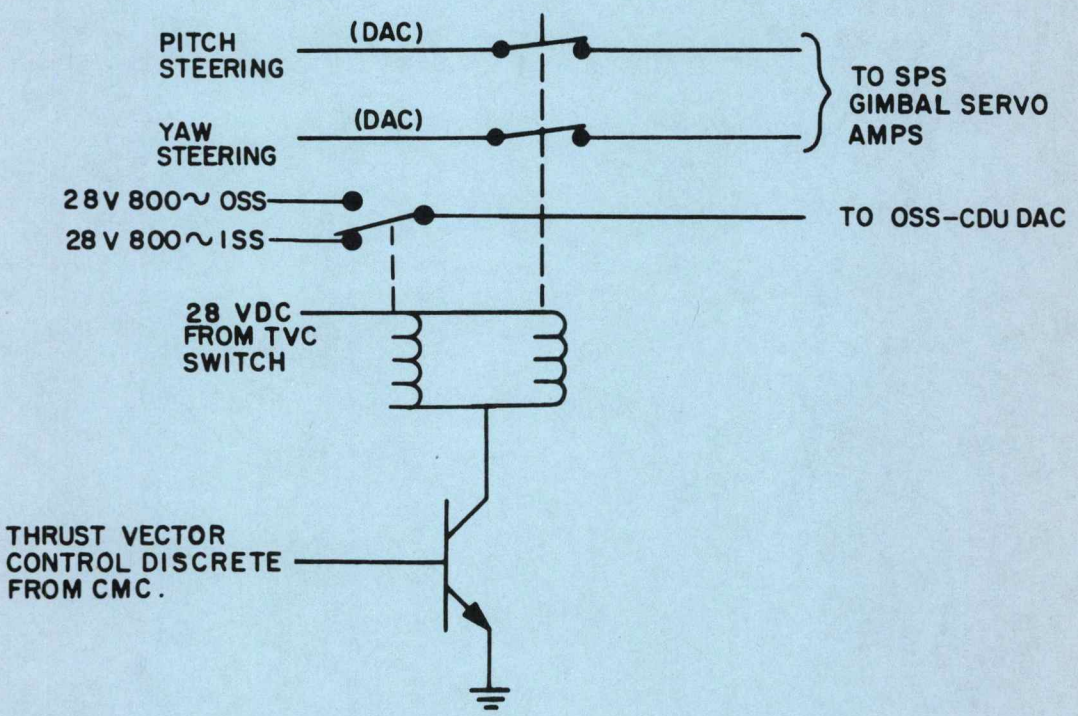


Figure 3-30. Moding Relay Circuit

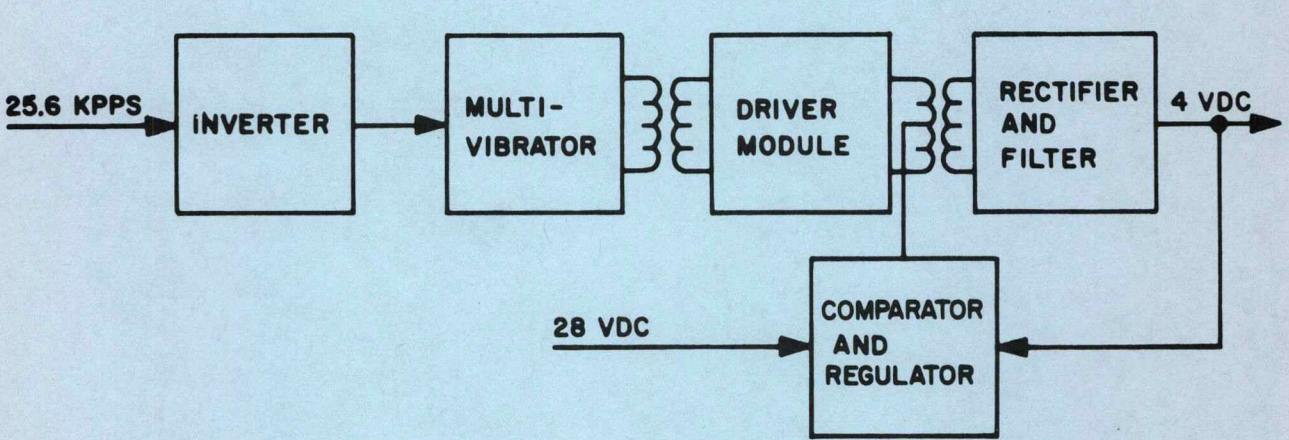


Figure 3-31. CDU 4 vdc Power Supply

3.15 CDU DISCRETES

The CMC issues discretes to the CDU to control the various modes and functions of both the ISS and OSS. All discretes are zero volts (CMC ground). The following is a list of these discretes.

3.15.1 ICDU ZERO. (CH 12-05) The inertial CDU zero discrete clears all three ICDU read counters simultaneously. It also inhibits the transmission of incrementing pulses to the read counters for the duration of the discrete. The CDU zero discrete is present for as long as the read counters are to be held at zero. The minimum duration is approximately 400 milliseconds. The IMU is not changed by the CDU zero discrete. Refer to figure 3-32.

3.15.2 OCDU ZERO. (Ch 12-01) The optics CDU zero discrete clears both shaft and trunnion CDU read counters simultaneously. It also inhibits the transmission of incrementing pulses to the read counters for the duration of the discrete. The CDU zero discrete is present for as long as the read counters are to be held at zero. The minimum duration is approximately 400 milliseconds. Refer to figure 3-33.

3.15.3 ISS ERROR COUNTER ENABLE (CH 12-06) The ISS enable error counter (IEEC) discrete enables all three error counters simultaneously which allows them to accept incrementing pulses ($\pm\Delta\theta_C$) from the CMC. The error counters are normally cleared and inhibited. The enable error counter discrete is used in conjunction with the coarse align enable discrete during the coarse align mode, and the S-4B take-over discrete. The enable error counter discrete is used alone only when display of attitude error signals on the FDAI is required. Refer to figure 3-34.

3.15.4 OSS ERROR COUNTER ENABLE (CH 12-02) The OSS enable error counter discrete enables both OSS error counter simultaneously which allows them to accept incrementing pulses ($\pm\Delta\theta_C$) from the CMC. These error counters are normally cleared and inhibited. This discrete is used during the thrust vector control mode and when the OSS is positioning the optics. Refer to figure 3-35.

3.15.5 COARSE ALIGN ENABLE (CH 12-04) The coarse align (CA) enable discrete enables a relay driver which energizes the coarse align and demodulator reference relays located in the PSA. This connects the coarse align error signal to the gimbal servo amplifiers and changes the reference voltage for the demodulator in the gimbal servo amplifiers from 3.200 cps to 800 cps. The discrete also enables the digital feedback pulses from the read counter to the error counter. The presence of the coarse align enable discrete and the absence of the enable error counter discrete inhibit the incrementing pulses to the read counter. Refer to figure 3-36.

3.15.6 S-4B TAKE-OVER (CH 12-09) Prior to the CMC generating the S-4B take-over discrete, the CMC checks to see if the error counters are in use. If the error counters are in use, the CMC removes the enable error counter discrete and, after a 1/2-second delay, issues the S-4B take-over discrete. The CMC generates the enable error counter discrete 40 milliseconds after the S-4B take-over discrete and, after a 4 millisecond delay, can send $\pm\Delta\theta_C$ pulses to the error counter. The S-4B take-over discrete energizes the control relays which connect the error counter D/A converter dc outputs to the Saturn guidance electronics for Saturn booster vehicle steering control. During this mode, the digital feedback pulses the read counter to the error counter are inhibited and the CMC monitors spacecraft position and velocity by use of the PIPA's and the ISS CDU read counters. Refer to figure 4-12.

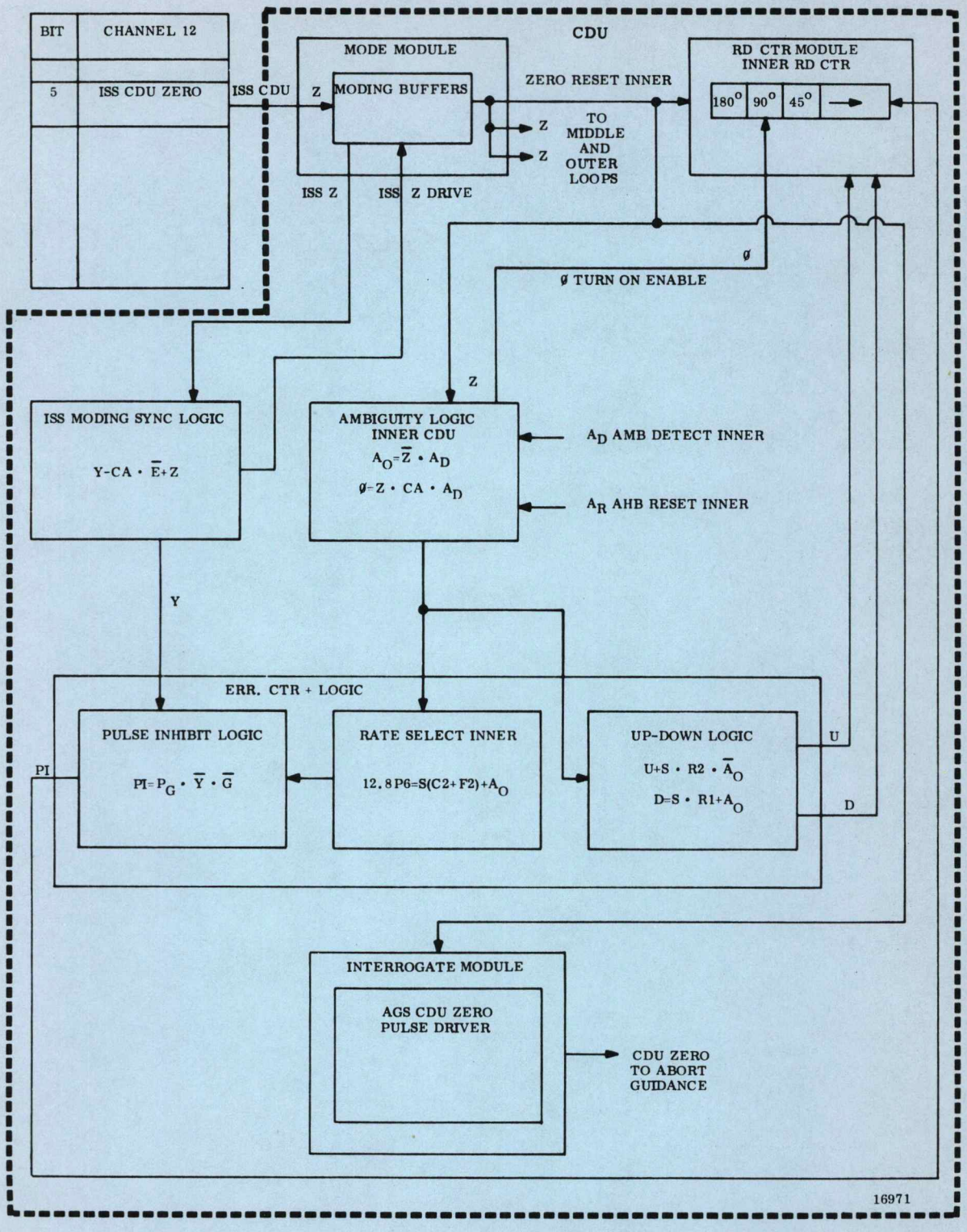


Figure 3-32. ISS CDU Zero Discrete

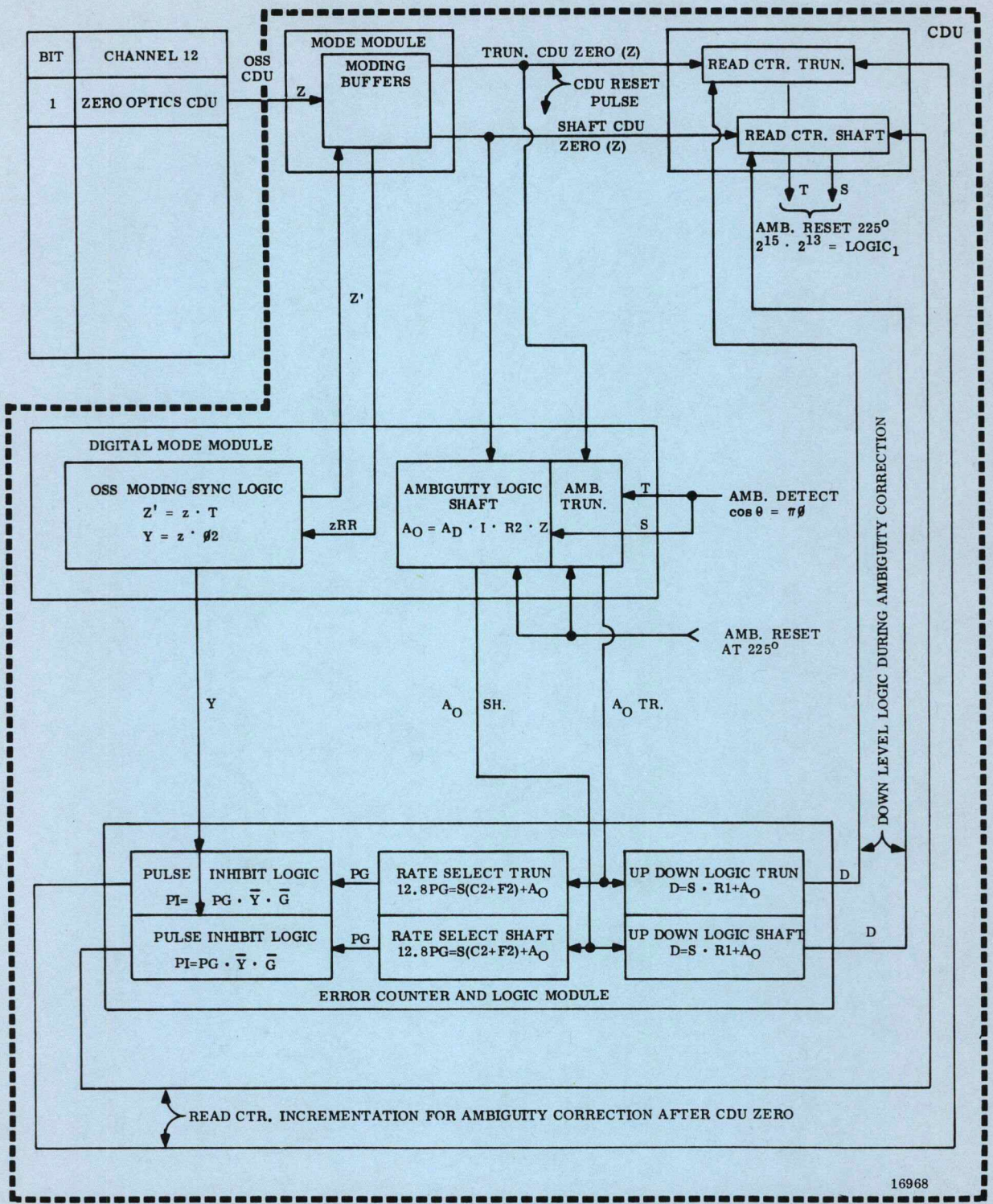


Figure 3-33. OSS CDU Zero Discrete

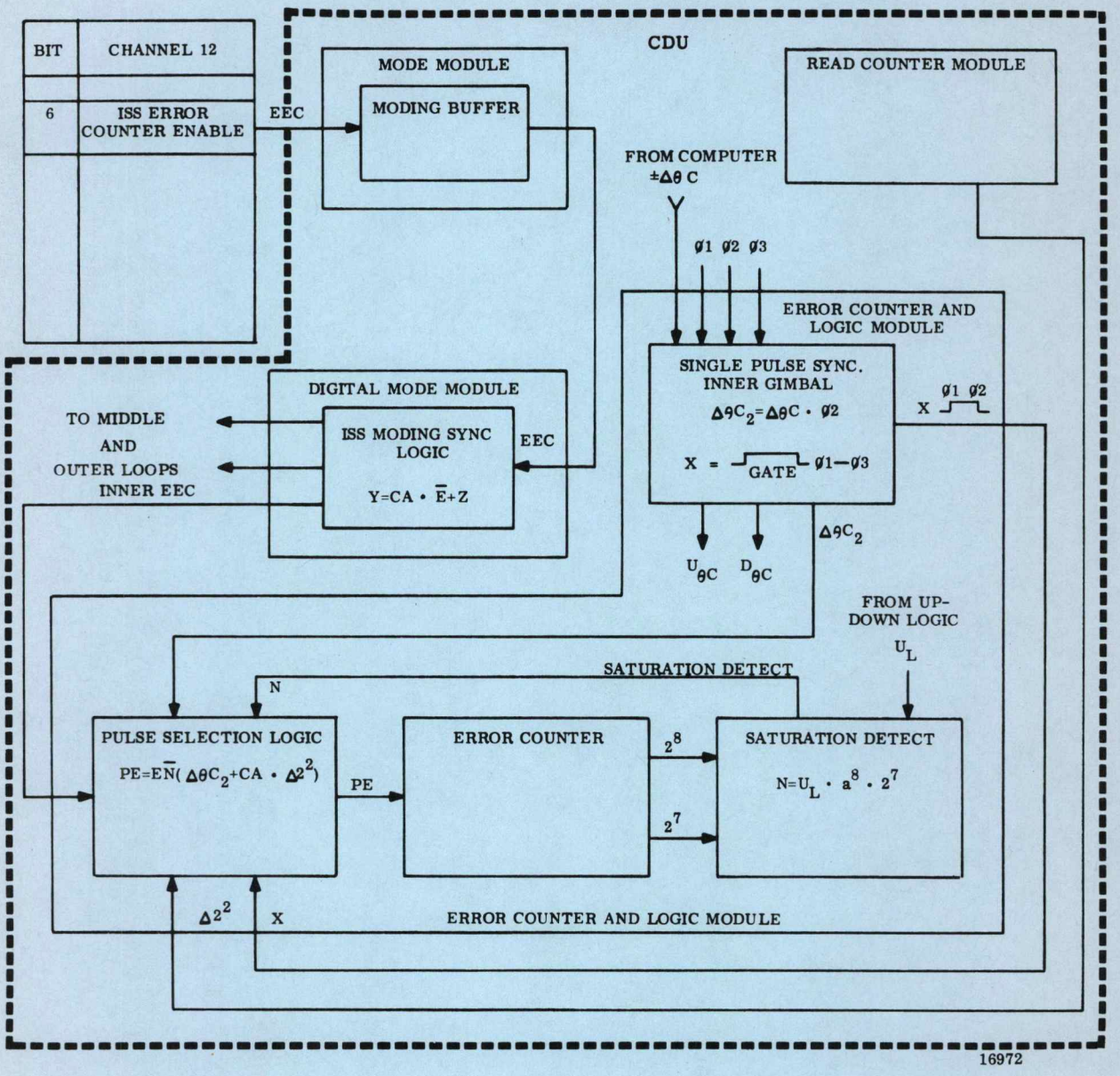


Figure 3-34. ISS Error Counter Enable Discrete

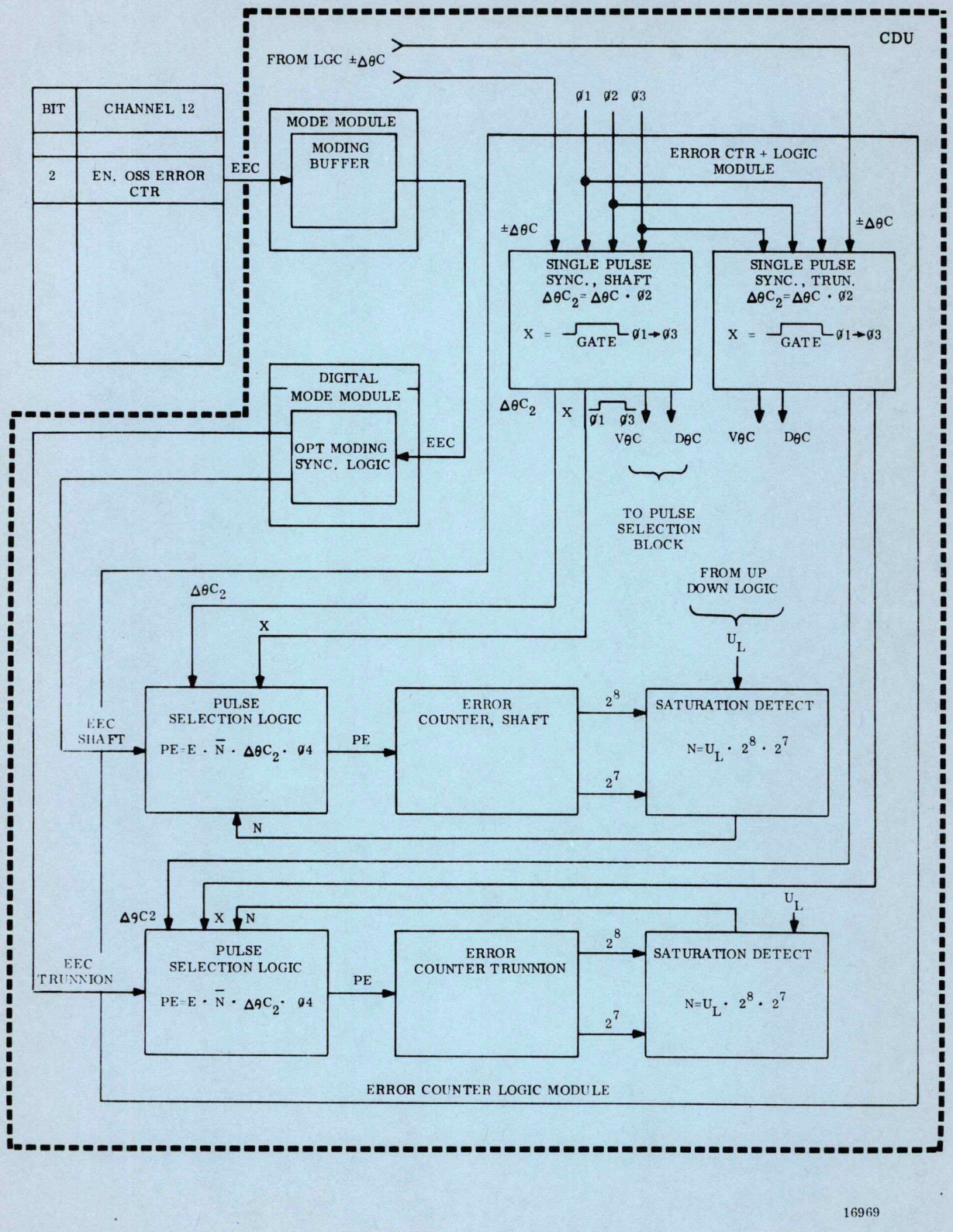


Figure 3-35. OSS Error Counter Enable Discrete

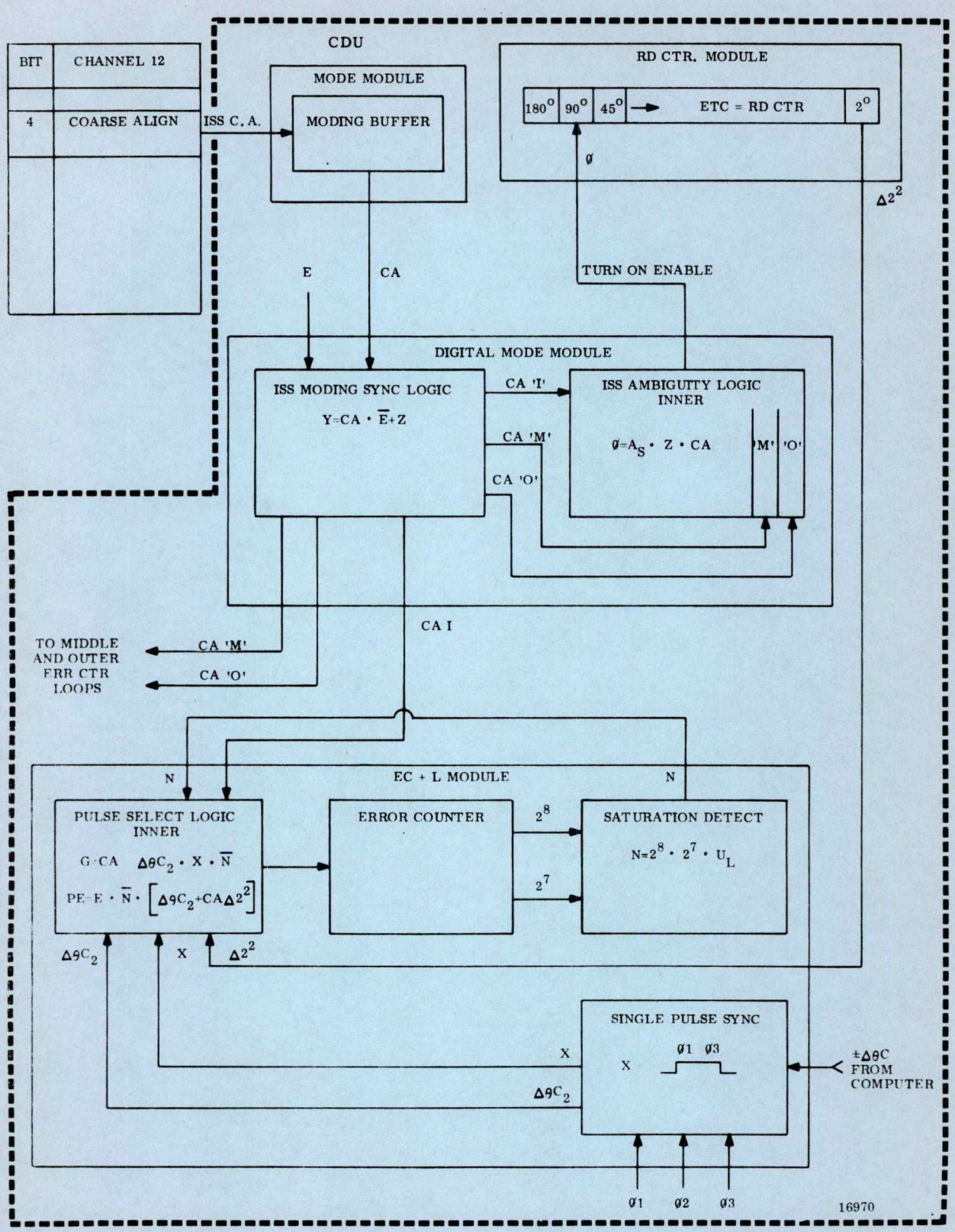


Figure 3-36. Coarse Align Discrete

3.15.7 TVC ENABLE (CH 12-08) The thrust vector control enable discrete is issued by the CMC upon receipt of the SPS ready and spacecraft autopilot control discretes. This discrete is used in the thrust vector control mode of operation as described in paragraph 4.10. Refer to figure 4-14.

3.16 SUMMARY

The CDU modules, each of which were discussed in detail in the preceding paragraphs, will be discussed as a unit. Some of the relationships of the modules to each other will be shown. The power supply module is assumed to be functioning for the following description.

The CDU generates timing pulses for use only within the CDU circuitry. These pulses, including Ø1, Ø2, Ø2 Ø3, Ø4, I, I2, I3, one generated in the interrogate module or the digital mode module. Three sets of interrogate pulses are generated: ISS, shaft, and trunnion. The Ø1 through Ø4 are used in both the optics and inertial channels of the CDU. The timing pulses are buffered in the moding module prior to general distribution within the CDU. The timing pulses are used in the digital logic circuitry of the digital mode module, the read counter Module, and the error counter and logic module.

In the operation of the CDU, moding control discretes from the computer are used to control the operational configuration. The moding discretes (CDU zero, error counter enable, coarse align, SIVB takeover) are associated with the inertial channels of the CDU. The optical channels have the first three plus a thrust vector control discrete associated with their operation. The mode discretes, with the exception of the SIVB takeover and thrust vector control discretes, are buffered in the moding module and then modified to meet the time phasing requirements in the digital mode module. The modified mode commands, all at specific logic levels when commanded, are routed from the digital mode module to the moding module, the error counter module, and the read counter module. The ISS CDU zero discrete is buffered one time after the digital mode module modification, causing it to be an inverted logic level when commanded.

Whenever the CDU is used, it must go through a moding sequence. First, the read counters are reset to zero by the CDU zero discretes. When this command is issued, it is possible to have an ambiguity condition existing; therefore, an ambiguity detect and logic circuit has been incorporated into the coarse module and the digital mode module. This circuitry prevents the read counter, which normally indicates gimbal or optics angles, from reading a false null angle. Reference signals R1 and R2 generated in the interrogate help determine if an ambiguity condition exists.

After completion of read counter zeroing, the CDU may be used as a repeating or a commanding device. The use as a repeating device will be discussed first.

The analog signals equivalent to the sine and cosine of θ and 16θ from the 1X and 16X gimbal resolvers or the 1X and 16X optical sensors must be converted to a digital pulse train. These signals are attenuated in the coarse module, the quadrant select module, and main summing amplifier module. The attenuation is controlled by the stages of the read counter. with the 2^9 through 2^{15} stages being associated with the coarse module and the 2^0 through 2^{11} stages being associated with the main summing amplifier and quadrant select modules.

The attenuated signals above a specified level fire an error detect Schmitt trigger in the coarse module and the main summing amplifier. When these Schmitt triggers are fired giving a C1, F1, or F2 command, logic circuitry in the error counter and logic module route incrementing pulses at 12.8 kpps or 800 pps to the read counter to increment the counter. This counter in turn controls, switches in the three modules associated with coarse fine control, further attenuating the 800 cps analog signal. When the signal is completely attenuated, the read counter contains the gimbal or optics angle.

The read counter count up or down is controlled by logic circuitry in the EC and L module. This same logic circuitry, which uses the phasing of the error signals to determine if an up or down count is required, will determine if the $\Delta 2^{\circ}$ angle sent to the CMC is to be counted as a positive or negative $\Delta\theta$. Whenever the CDU zero mode command is not commanded, the read counter will accumulate gimbal or optical angles. A pulse train indicating a changing angle is sent to the computer.

The CDU can be used as a commanding device as well as a repeating device. In this application it is used as a digital to analog converter using the error counter and logic module and the digital to analog converter module.

A computer generated error counter enable discrete allows the error counter to become operative. The error counter is incremented by $\Delta\theta$ commands from the computer. The logic associated with the error counter determines if the error counter should count up or down and it also determines the polarity of the DAC outputs by generating an output polarity command.

The incremental error counter controls switches in the digital to analog converter which can provide an 800 cps coarse align signal, an 800 cps attitude error signal, or ± dc display signal output. The error counter, a nine bit counter, is limited to a maximum of 384 input pulses before it is considered to be saturated. These values will cause the DAC output to be a maximum of ± 5.1 vdc, or 0 or π $\emptyset$ 5 v(rms).

The contents of the error counter can be incremented or decremented only by the CMC in all modes of operation except coarse align. In this mode the error counter logic will accept $\Delta 2^2$ pulses from the output of the third stage of the read counter. If a + $\Delta\theta$ has been commanded, the phase of the DAC output causes an increasing gimbal angle. The $\Delta 2^2$ pulse train is recognized by the error counter logic and causes the counter to decrement. In this manner the coarse align error signal will tend to null as the actual gimbal angle approaches the desired angle commanded by the computer.

The ladder output of the DAC is mixed with an 800 cps coarse and an 800 cps fine signal from the coarse module and main summing amplifier module respectively.

These error signals, which are analog signals proportional to sin $(\theta - \Psi)$, are used as rate feedback control during the coarse align mode of ISS operation.

The moding module contains circuitry to monitor the operations of the CDU for both the ISS and OSS operational sections of the device. Signals such as the coarse error, fine error, up logic limit cycling, and an output of the cos $(\theta - \Psi)$ generator are monitored either for too high a level, too high a frequency, or too low a level. The CDU issues a CDU fail indication (ISS, or OSS) to the CMC.

SECTION IV

ISS - SYSTEM MODES OF OPERATION

INTRODUCTION

This section of the study guide is primarily concerned with the modes of operation which involve the IMU. This covers both the ISS modes and the PGNCS system modes. These modes interface with the CSS and may be entered by D and C panel switch, by DSKY input and/or by program input. Table 4-1 contains a list of these modes of operation, a list of appropriate CMC input-output channels and a matrix showing the discrete and mode relations.

4.1 ISS TURN-ON MODE

The purpose of the ISS turn-on mode is to initialize the ISS. This is accomplished under program control of the CMC. The following is a list of functions which are initiated by the CMC's T4 rupt routine:

a. zero the IMU gimbal angles.

b. allows the gyro wheels to run up to speed.

c. inhibits the pulse torque power supply for 90 sec.

d. zeros and inhibits the ISS read and error counters in the CDU.

e. zeros the CDU counters in E memory.

The CMC controls the ISS turn-on mode by accepting, issuing, timing and inhibiting selected discretes. The timed sequence for handling these discretes is as follows: The CMC recognizes the ISS operate (CH 30-09) and the ISS turn-on delay request (CH 30-14) discretes as requests for program control of the turn-on sequence. This causes the CMC to remove the ISS enable error counter (EEC) (CH 12-06) and the ISS turn-on delay complete (CH 12-15) discretes if they exist. Then the ISS coarse align (CA) (CH 12-04) and ISS CDU zero (Z) (CH 12-05) discretes are issued and the "NO ATTITUDE" lights on the DSKY's are turned on. This is followed by the inhibiting of the PIPA fail (CH 33-13), ISS CDU FAIL (ICDU) (CH 30-12) and the IMU fail (CH 30-13) discretes. After a 90 second delay, the 90 sec delay complete (CH 12-15) discrete is issued, the "NO ATTITUDE" lamps are turned off, the CDU counters in E memory are set to zero, and the CA and Z discretes are removed. Four seconds later, the PIPA, the ICDU, and the IMU fail inhibits and the 90 sec delay complete discretes are removed.

Standby power is applied to the PGNCS by way of circuit breakers CB58 and/or CB59. To initiate the ISS turn-on mode, ISS operate power must be applied to PGNCS by way of CB56 and/or C57 and the IMU G&N power switch (S2) on the lower equipment bay (LEB). Reference figure 4-1. ISS operate power is applied directly to CH 30-09 (ISS operate) discrete and through the deenergized contacts of the auto cage relay to CH 30-14 (ISS turn-on delay request) and to the cage relays.

ISS - System Modes of Operation	CMC Discretes									D & C Panels				
	Gyro Torque Enable (CH 14-06)	IMU CDU Zero (CH 12-05)	Coarse Align Enable (CH 12-04)	ISS Error Counter Enable (CH 12-06)	SIVB Take-over Enable (CH 12-09)	Thrust Vector Control Enable (CH 12-08)	Optics CDU Zero (CH 12-01)	Optics Error Counter Enable (CH 12-02)	Turn-on Delay Complete (CH 12-15)	IMU Cage (CH 30-11) (S49)	Turn-on Delay Request (CH 30-14)	G & C A/P Control (SPS Ready) (CH 30-03)	IMU Operate (CH 30-09)	S/C Control of Saturn (CH 30-10)
ISS Turn-on		X	X						X		X		X	
IMU CDU Zero		X												
Coarse Alignment			X	X										
Fine Alignment	X													
Attitude Error Display				X										
Inertial Reference														
IMU Cage		X	X							X				
Gimbal Lock			X											
SIVB Take-over				X	X									X
Thrust Vector Control						X		X				X		
Attitude Control				X										

Table 4-1. ISS - System Modes of Operation

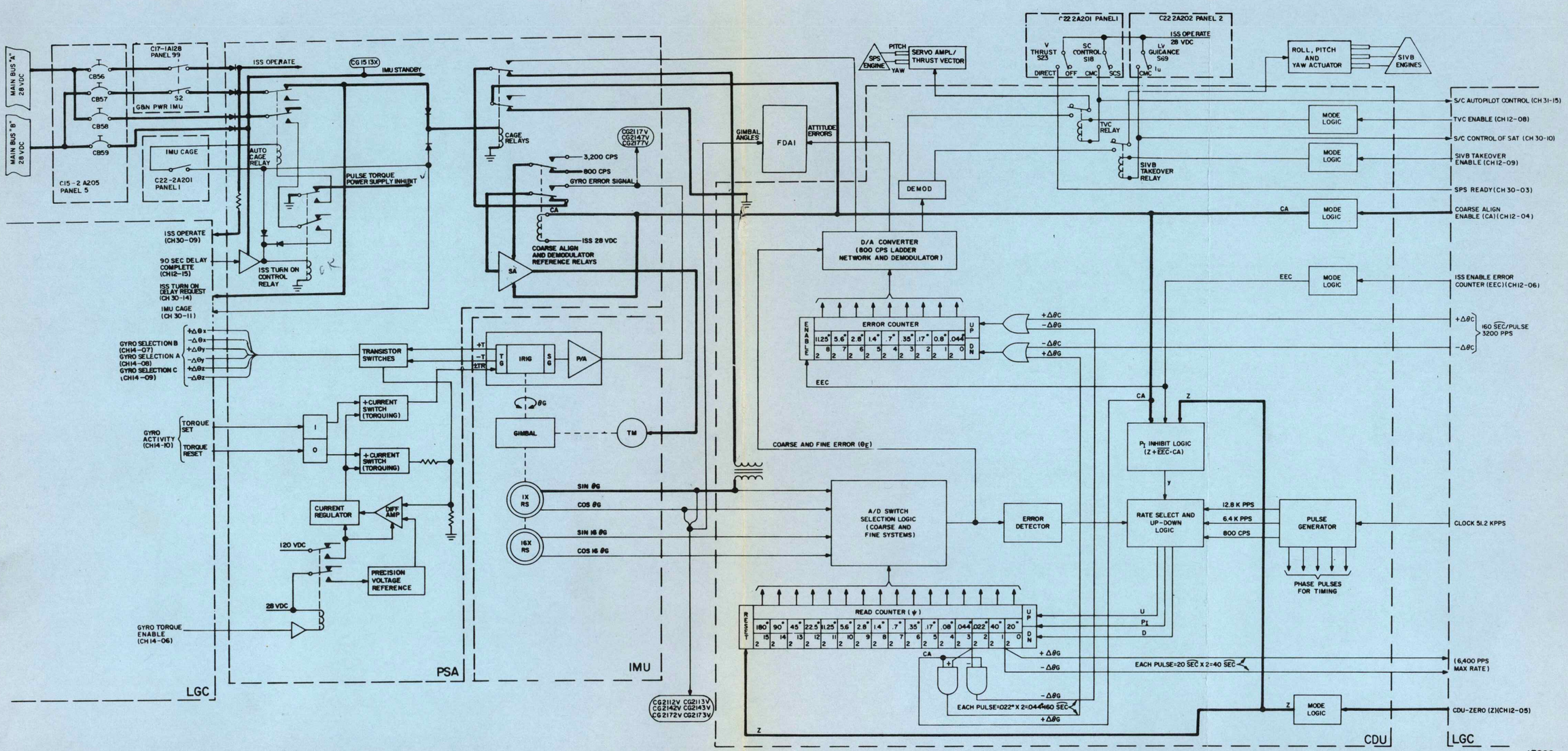


Figure 4-1. IMU Turn-on Mode (Sheet 1 of 2)

The cage relays energize and, in turn, cause the coarse align relays to be energized. The cage relays route the 1X gimbal resolver sine winding outputs through the contacts of the coarse align relays to the respective gimbal servo amplifiers. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled. The operation of the caging loops is discussed further in the IMU cage mode description.

Upon receipt of the ISS turn on delay request discrete, the CMC sends the ISS CDU zero discrete and the coarse align enable discrete to the CDU for a minimum period of 90 seconds. The CDU zero discrete clears the read counters and inhibits the incrementing pulses to the read counters. The coarse align enable discrete provides a redundant means of energizing the coarse align relays.

A second set of deenergized contacts on the ISS turn on control relay routes a ground to the time delay circuit of the pulse torque power supply which inhibits the operation of the power supply and thus prevents accelerometer pulse torquing during the 90 second turn on period. This allows time for the accelerometer floats to be centered and the gyro wheels to run up prior to torquing.

After the 90 second delay has been completed, the CMC sends the ISS turn on delay complete discrete. This discrete acts through a relay driver to energize and latch in the ISS turn on control and the auto cage relays. Refer to figure 4-2.

Energizing the ISS turn on control relay deenergizes the cage relay, removes the ISS turn on delay request discrete, and removes the inhibit from the pulse torque power supply. The computer program can then place the ISS in the inertial reference mode by removing both the CDU zero and the coarse align enable discretes, or it can initiate the coarse align mode by removing only the CDU zero discrete and sending the ISS enable error counter discrete. The IMU turn on circuit will be reset whenever 28 vdc IMU operate power is turned off.

4.2 ISS CDU ZERO MODE

The purpose of the ISS CDU zero mode is to insure synchronization between the inner middle and outer read counter in the CDU and the respective X, Y, and Z CDU counters in E memory. This mode can be entered by inserting a V40 N20 into the DSKY or by computer program. When the computer enters this routine, it will inhibit the ICDU FAIL (CH 30-12) and IMU FAIL (CH 30-13) discretes, issue the ISS CDU zero (CH12-05) discrete and then execute a 320 millisec delay. During this 320 millisec the ICDU read counters are zeroed and inhibited. Refer to figure 4-3. When the delay has been completed, the computer will set the X, Y, and Z CDU counters in E memory to zero and then remove the ICDU zero discrete. The removal of the zero discrete will allow the read counters to increment up to the gimbal angles and the X, Y, and Z CDU counters in E memory will follow along. After another four second delay, the ICDU and the IMU fail inhibits are removed and the ISS CDU zero mode is complete.

4.3 COARSE ALIGNMENT MODE

The coarse align mode of operation is mechanized to allow the computer to rapidly align the IMU to a desired position with a limited degree of accuracy. The computer issues two discretes to the CDU in this mode, coarse align enable (CA) and 40 msec later enable error counter (EEC). Refer to figure 4-4. The CMC has also selected the gimbal to be positioned by setting bit 13, 14, or 15 in CMC output channel 14. The CMC, knowing the actual gimbal angle registered in the read counters, will calculate the desired amount of change of gimbal

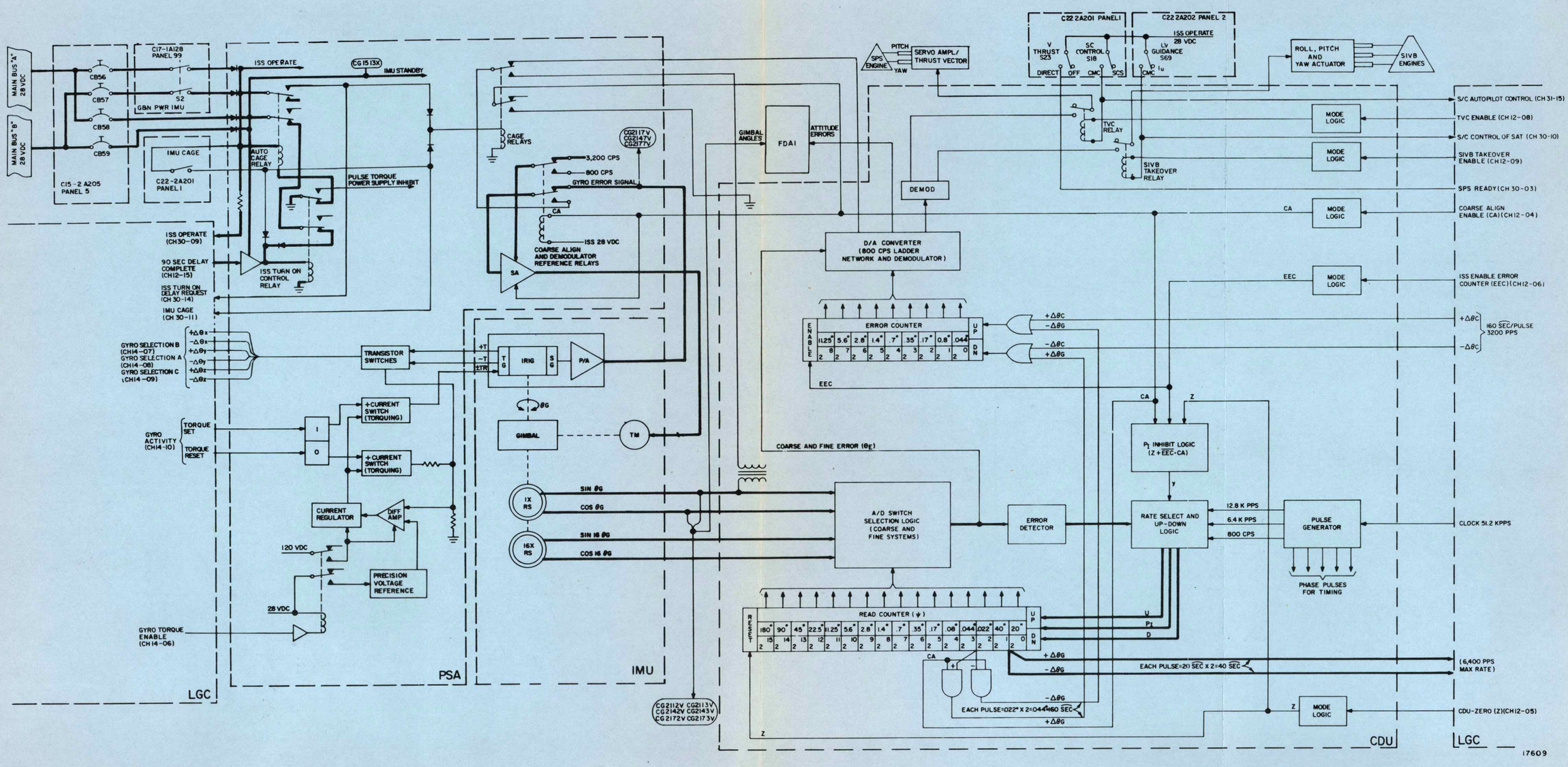


Figure 4-2. IMU Turn-on Mode (Sheet 2 of 2)

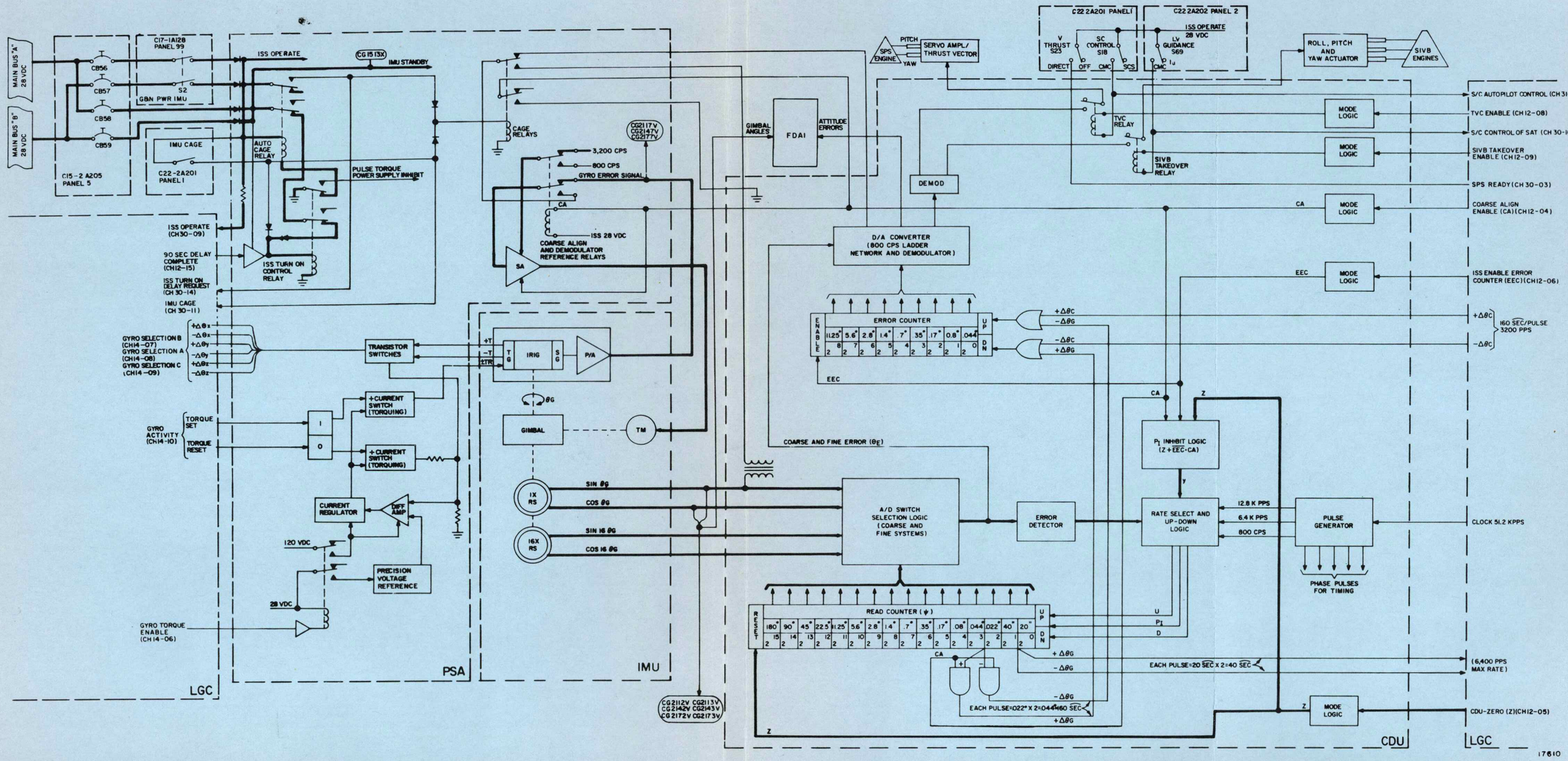


Figure 4-3. IMU CDU Zero Mode

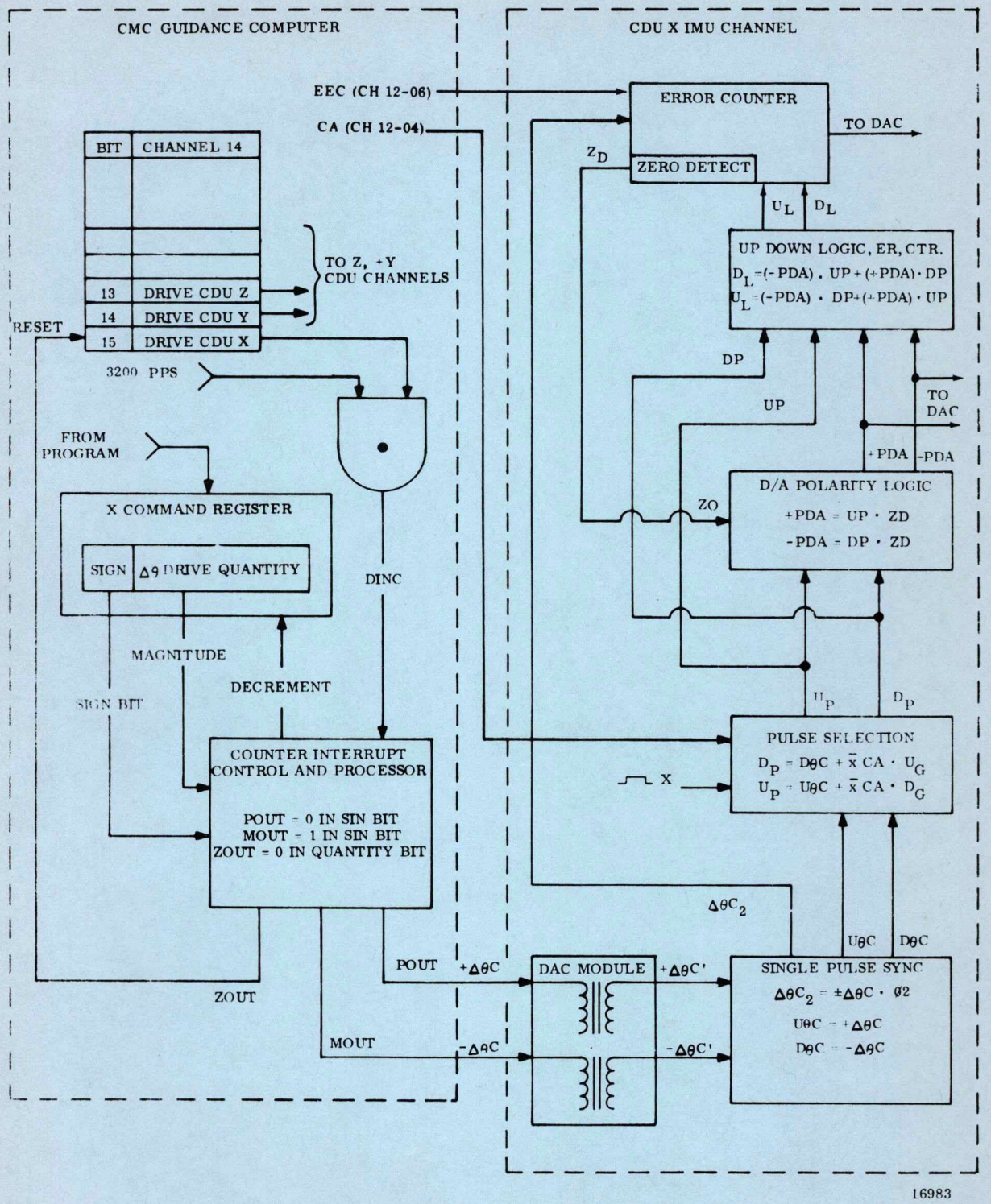


Figure 4-4. Coarse Alignment Mode Interface

angles required to reposition the gimbals to the desired angles and loads this information in the appropriate CMC X, Y, or Z command registers. The CMC converts this change into a number of $\pm \Delta\theta C$ pulses and sends these pulses to the error counters. The $\pm \Delta\theta C$ pulses are sent to the error counters at a rate of 3,200 pps in bursts of 192 pulses. Bursts are sent every 600 millisec. Each $\Delta\theta C$ pulse is equal to a change in gimbal angle of 160 arc seconds. The error counter, having been enabled, accepts the pulses and counts up or down as necessary until all the pulses have been registered.

The ladder decoder in the D/A converter module supplies an 800 cps, amplitude modulated analog error signal equivalent to the digital information in the error counter. Refer to figure 4-5. The ladder decoder signal is summed with a feedback signal and applied through a mixing amplifier, also located in the D/A converter module, to the gimbal servo amplifiers to drive the gimbals to the desired angles. The coarse align error signal output of the mixing amplifier is applied to the gimbal servo amplifiers through the contacts of the coarse align relays located in the PSA. The coarse align relays, which are energized by the coarse align enable discrete acting through the mode logic, switch the input of the gimbal servo amplifiers from the gyro preamplifiers to the coarse align error signal output of the ISS D/A converters. The demodulator reference relay is also energized by the coarse align enable discrete and switches the reference frequency of the demodulator in the gimbal servo amplifiers from 3,200 cps to 800 cps. The coarse align enable discrete also energizes a relay in the gimbal servo amplifiers which switches additional capacitance into the amplifier's compensation networks to tune them for 800 cps operation.

As the gimbals are driven, $\pm \Delta 2^2$ pulses, representing the change in actual gimbal angle, are generated by the read counter and applied to the error counter. The $\pm \Delta 2^2$ pulses are also equal to 160 arc seconds and decrease the $\pm \Delta\theta C$ pulses registered in the error counter. The error counter output to the ladder decoder, therefore, represents the difference between the desired amount of change in gimbal angle and the amount of change actually accomplished. The error counter reaches a null or reads zero, and the gimbals stop moving, when the actual gimbal angle has changed by an amount equal to the total value of the $\pm \Delta\theta C$ pulses sent by the computer to the error counter. The CMC checks the contents of the read counter 2.1 seconds after the CMC has sent the last coarse align torquing pulse to the error counter. If the gimbal angles are not within two degrees of the desired angle, the computer issues an alarm.

The rate at which the gimbals are driven is limited to prevent damage to the gyros and to assure that the read counter can track the gimbal angle accurately. The rate of gimbal movement is limited by feeding back the CDU fine error signal sin 16 $(\theta - \psi)$ to the input of the mixing amplifier located in the D/A converter module. The fine error signal is out of phase with the output of the ladder decoder and has an amplitude proportional to the difference between the actual gimbal angle (θ) and the angle registered in the read counter (ψ). The fine error signal is applied through a voltage limiting circuit to the summing junction of the mixing amplifier where it is summed with the 800 cps ladder decoder output signal. The D/A converter ladder decoder output is applied to the mixing amplifier through a scaling amplifier and a voltage limiting diode network. The scaling amplifier controls the signal gain to produce a scale factor of 0.3 volt rms per degree. The output of the mixing amplifier will be at a null when the D/A converter ladder decoder output, after limiting, is equal to the fine error feedback signal. The fine error signal will be a constant value only when the gimbal and the CDU are going at the same rate and with the gimbal angle leading the CDU angle. Since the CDU is constrained to counting at one of two speeds, the gimbals will be constrained to a rate equal to one of these two speeds. During the coarse align mode, the CDU is constrained to a high counting speed of 6.4 kpps and a low counting speed of 800 cps. At all other times, the high counting speed is 12.8 kpps.

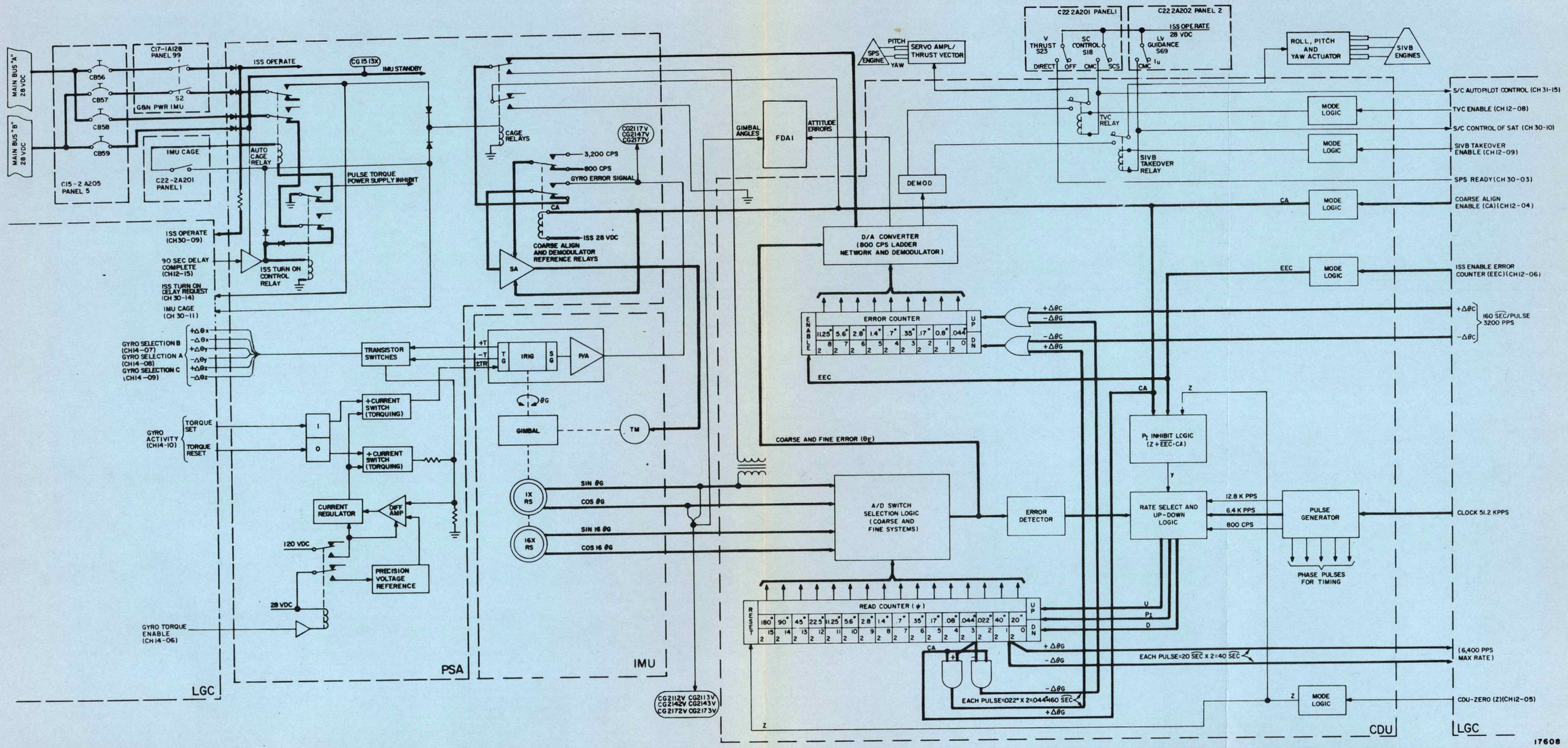


Figure 4-5. Coarse Alignment Mode

If the gimbals are moving at a faster rate than the rate at which the CDU is counting, the fine error signal will increase causing a retarding torque to be developed by the gimbal servo amplifier. If the gimbals are moving at a rate slower than the rate at which the CDU is counting, the fine error signal will decrease causing the gimbal servo amplifier to apply an accelerating torque to the gimbals. By adjusting the gain of the fine error signal into the mixing amplifier, the gimbal drive rate is limited to either 35.5 degrees per second (6.4 kpps CDU counting rate) or 4.5 degrees per second (800 cps CDU counting rate).

4.4 FINE ALIGNMENT MODE

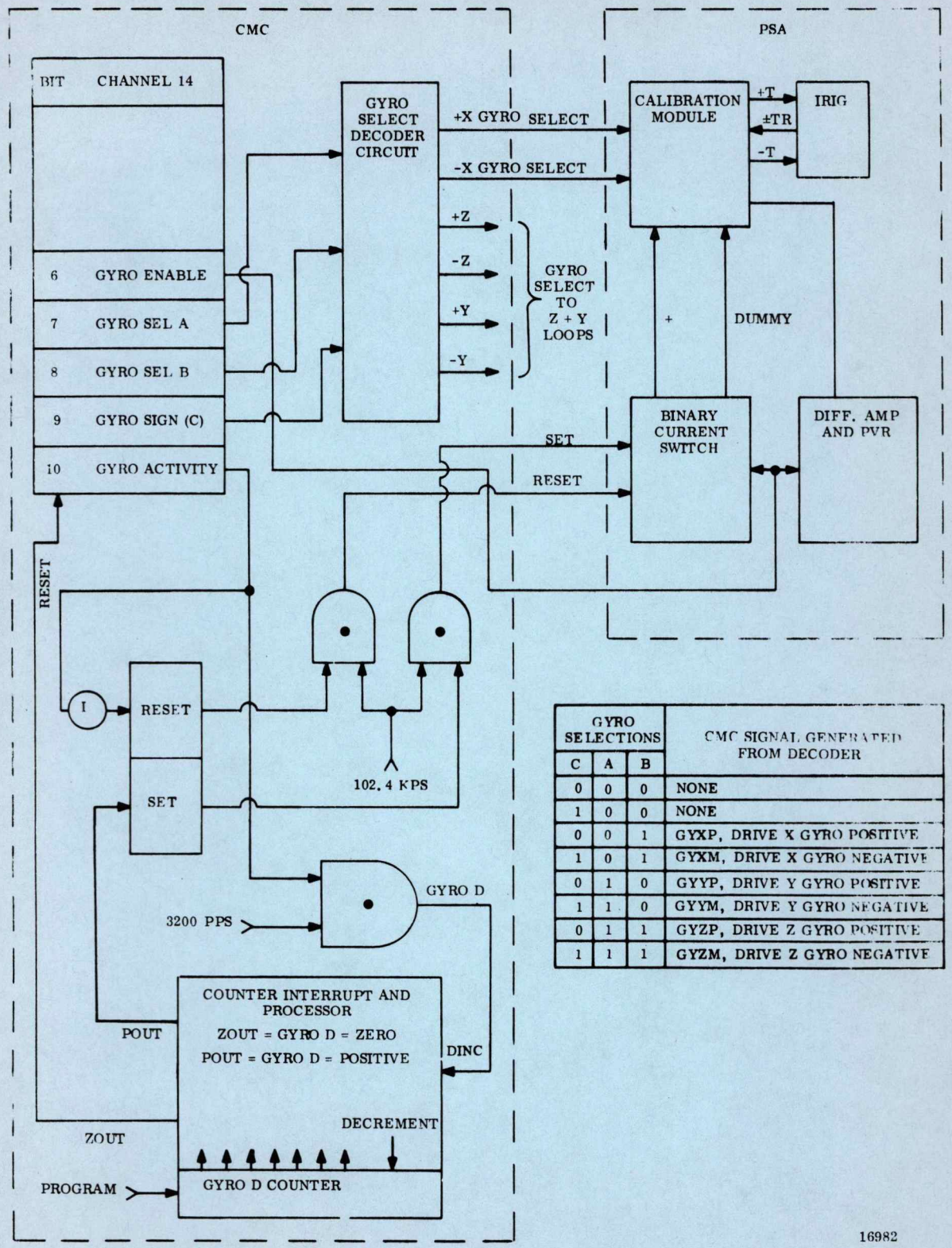
The purpose of the fine align mode is to reposition the stable member to a fine alignment by torquing the gyros. The fine align mode is actually a gyro torquing function accomplished during the inertial reference mode. The torquing current to the gyros is provided by the fine align electronics located in the PSA. The fine align electronics are enabled and controlled by CMC pulses sent directly to the fine align electronics. Refer to figure 4-6. The CMC program will place the desired number of pulses in the gyro D counter and then decrement the counter at the rates of 3200 pulses per second. These pulses are routed to the IRIG's. Each pulse is worth 0.617981 arc seconds of gimbal rotation. Refer to figure 4-7.

The ISS is in the inertial reference mode prior to the enabling of the fine align electronics and returns to that mode when the fine align electronics are disabled. The computer accepts the angular data received from the optical measurements, transforms the S_tLOS, into stable member coordinates, and compares the desired coordinates with the actual coordinates. Differences are used to compute the angular rotation about each stable member axis which will move the stable member to the correct orientation. The fine align electronics torques the gyros on a time shared basis. The CMC sends four types of pulse trains to the fine align electronics. The first pulse train to be sent is the torque enable command which enables the fine align electronics. The second pulse train is a gyro select command which selects a particular gyro and the direction it is to be torqued by means of a switching network which closes the current path through the proper torque ducosyn coil. The third and fourth types of pulse trains are the torque set and torque reset commands which control a binary current switch to start and stop the current flow through the selected torque ducosyn coil. The amount of current flow through the torque ducosyn coils is precisely controlled at a fixed value. The amount of gyro torquing to be accomplished is determined by the amount of time torque current is applied, that is, the time duration between the receipt of the torque set and the torque reset commands. The factor is calculated by the CMC based on optical alignment measurements. The torque ducosyn displaces the gyro float causing the ducosyn signal generator to apply an error signal to the stabilization loop. The stabilization loops drive the gimbals to reposition the stable member. Upon completion of the torquing, the stable member remains fixed in inertial space, and in fine align mode, until the torque enable command is removed, after which the ISS remains in inertial reference mode until further change is commanded.

During the fine align mode, the ISS error counters remain cleared and inhibited. The read counters continue to repeat the gimbal angles and send angular data ($\pm \Delta \theta G$) to the CMC.

4.5 ATTITUDE ERROR DISPLAY

The attitude error display mode supplies attitude error signals to the FDAI. This mode is initiated when the CMC sends the ISS enable error counter discrete to the CDU. Refer to figure 4-8.



GYRO SELECTIONS			CMC SIGNAL GENERATED FROM DECODER
C	A	B	
0	0	0	NONE
1	0	0	NONE
0	0	1	GYXP, DRIVE X GYRO POSITIVE
1	0	1	GYXM, DRIVE X GYRO NEGATIVE
0	1	0	GYYP, DRIVE Y GYRO POSITIVE
1	1	0	GYYM, DRIVE Y GYRO NEGATIVE
0	1	1	GYZP, DRIVE Z GYRO POSITIVE
1	1	1	GYZM, DRIVE Z GYRO NEGATIVE

Figure 4-6. Fine Alignment Mode Interface

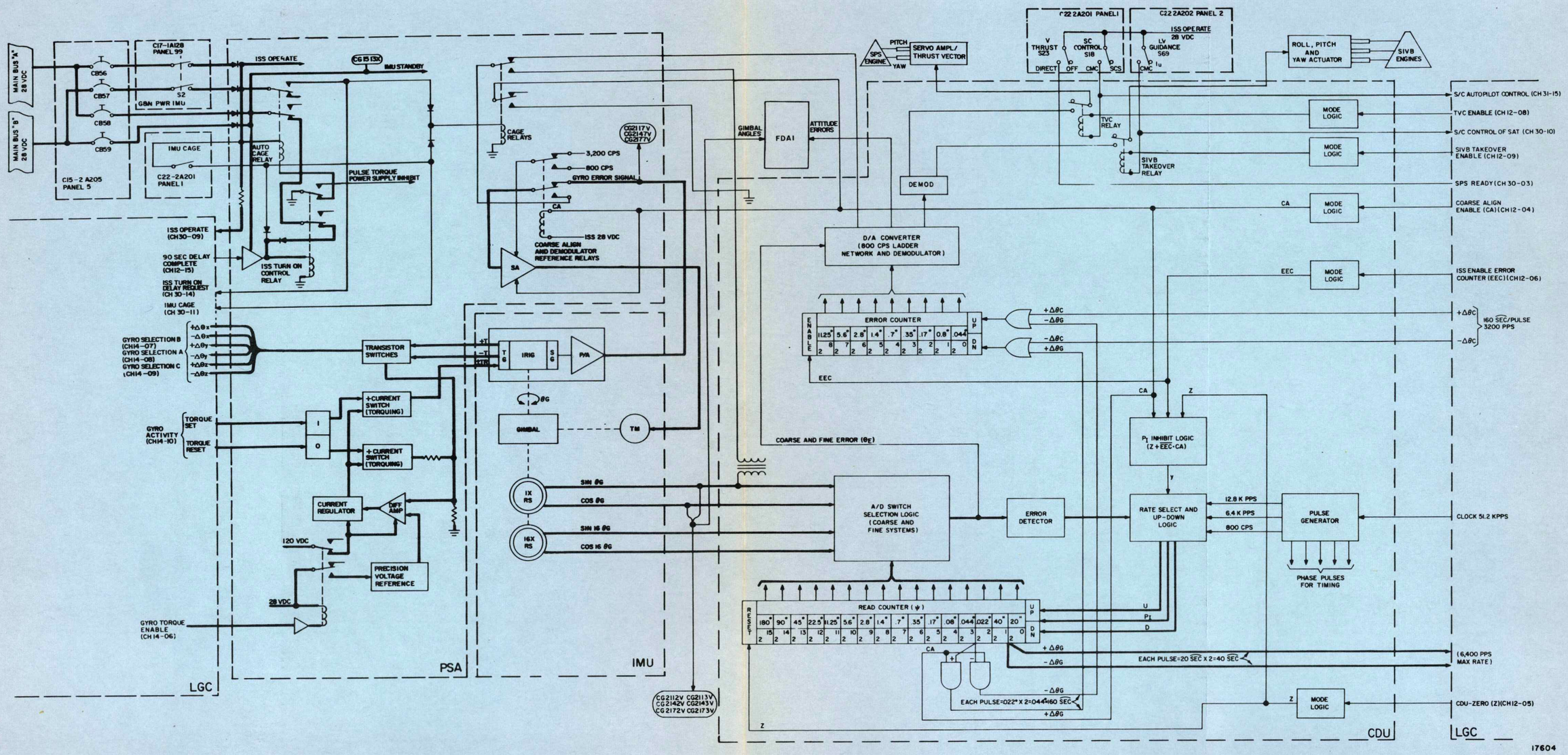


Figure 4-7. Fine Alignment Mode

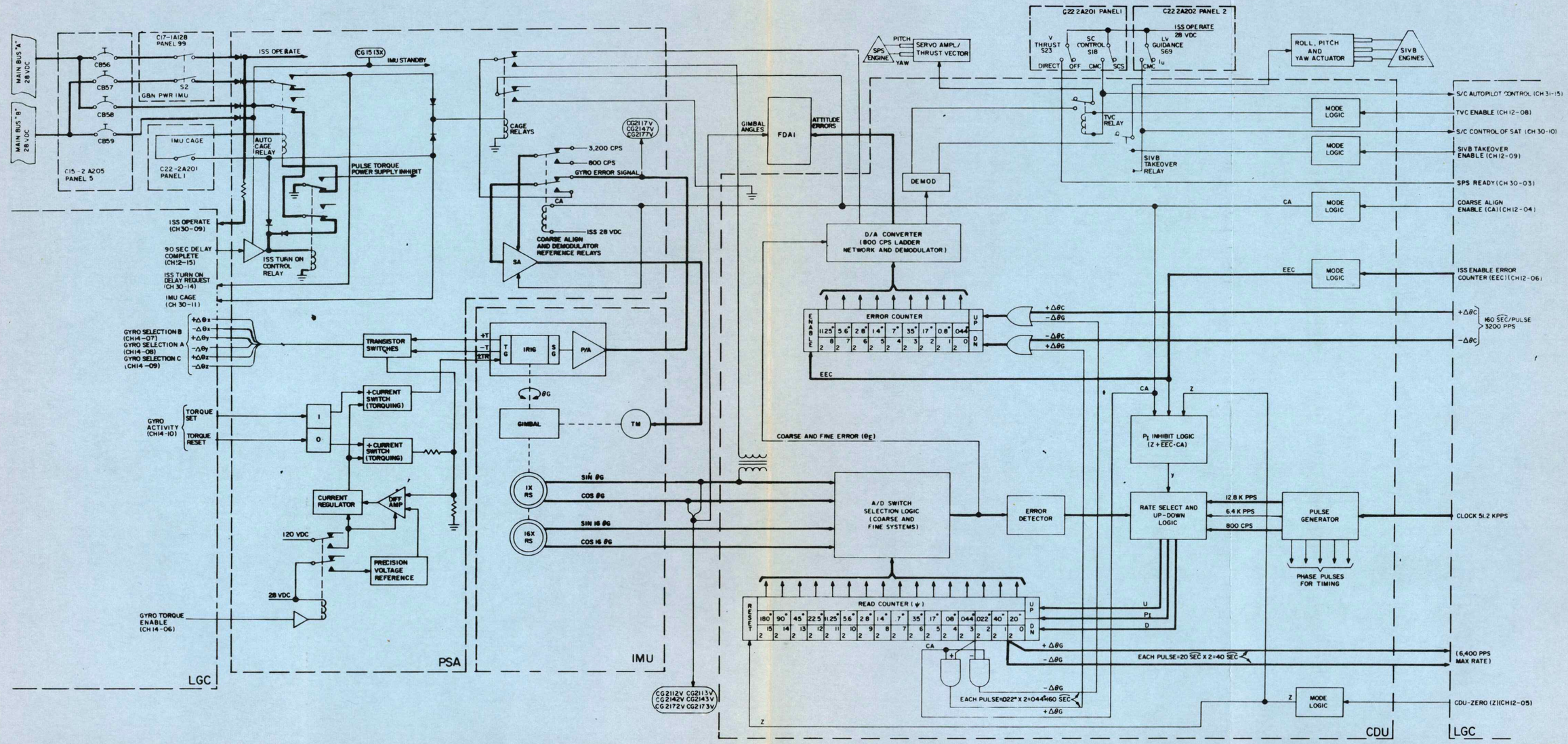


Figure 4-8. Display Attitude Error Mode

The ISS read counters are enabled and register the IMU gimbal angles which are sent to the CMC as $\pm\Delta\theta G$ pulses. The CMC calculates the difference between the actual gimbal angles registered in the read counters and the desired IMU gimbal angles and, if any difference exists, converts this difference into $\pm\Delta\theta C$ pulses which are sent to the error counters. The error counter, having been enabled, accepts the pulses and counts up or down until all pulses are registered. The error counter output is applied to the D/A converters where it is converted into an ac signal proportional to the error counters contents and applied to the FDAI.

Any change in actual gimbal angles causes the read counters to increase or decrease proportionally. If the attitude error increases or decreases, the CMC will send additional $\Delta\theta C$ pulses to decrease or increase, respectively, the error counter contents. The digital information in the error counters is converted into an 800 cps, amplitude modulated, analog error signal by the ladder decoder in the DAC's. This ac signal, representing the difference between the actual gimbal angles and the desired gimbal angles, is applied through the scaling amplifiers to the FDAI.

4.6 INERTIAL REFERENCE MODE

The purpose of the inertial reference mode is to provide a coordinate reference system on which attitude and velocity measurements and calculations may be based. During the inertial reference mode, the stable member is held fixed with respect to inertial space by the stabilization loops. Refer to figure 4-9. The ISS CDU read counters provide the CMC with changes in gimbal angles with respect to the stable member. The ISS is in the inertial reference mode during any operating period in which there is an absence of moding commands. During the inertial reference mode, the fine align electronics is inhibited and the ISS error counters are cleared and inhibited.

4.7 IMU CAGE MODE

The purpose of the IMU cage mode is to set the gimbals to their zero position. During this mode, the 1X gimbal resolver sine winding outputs are fed through the CDU's to the gimbal servo amplifiers to drive the gimbals until the resolver signals are nulled. This mode is a normal part of the ISS turn-on mode and may be initiated by the astronaut, via the IMU cage switch, as an emergency mode to recover a tumbling platform. Refer to figure 4-10. During the ISS turn-on mode, the cage function is safe because the gyro wheels are not turning. However, when used to recover a tumbling platform, the combination of the gimbal drive rates and the precessional torques are sufficient to cause the gyros to be driven into their rotational and radial stops. This action may cause both temporary and permanent bias shifts on the order of several MERU's.

When IMU cage mode is initiated by the astronaut pressing the IMU CAGE switch (S49), the switch is held until the gimbals settle at the zero position (five seconds maximum). The gimbal position may be observed on the FDAI. The IMU CAGE switch routes a 28 vdc discrete signal to the CMC and to the cage relays located in the PSA. The cage discrete energizes the cage relays which in turn cause the coarse align relays, the demodulator reference relay, and a relay in the gimbal servo amplifiers to be energized. The relay in the gimbal servo amplifiers switches additional capacitance into the RC compensation networks to tune them for 800 cps operation. The demodulator reference relay changes the gimbal servo amplifier demodulator reference signal from 3,200 cps to 800 cps. The cage relays switch the 1X gimbal resolver sine winding outputs through the energized contacts of the coarse align relays into the corresponding gimbal servo amplifier inputs. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled which occurs at zero gimbal angle.

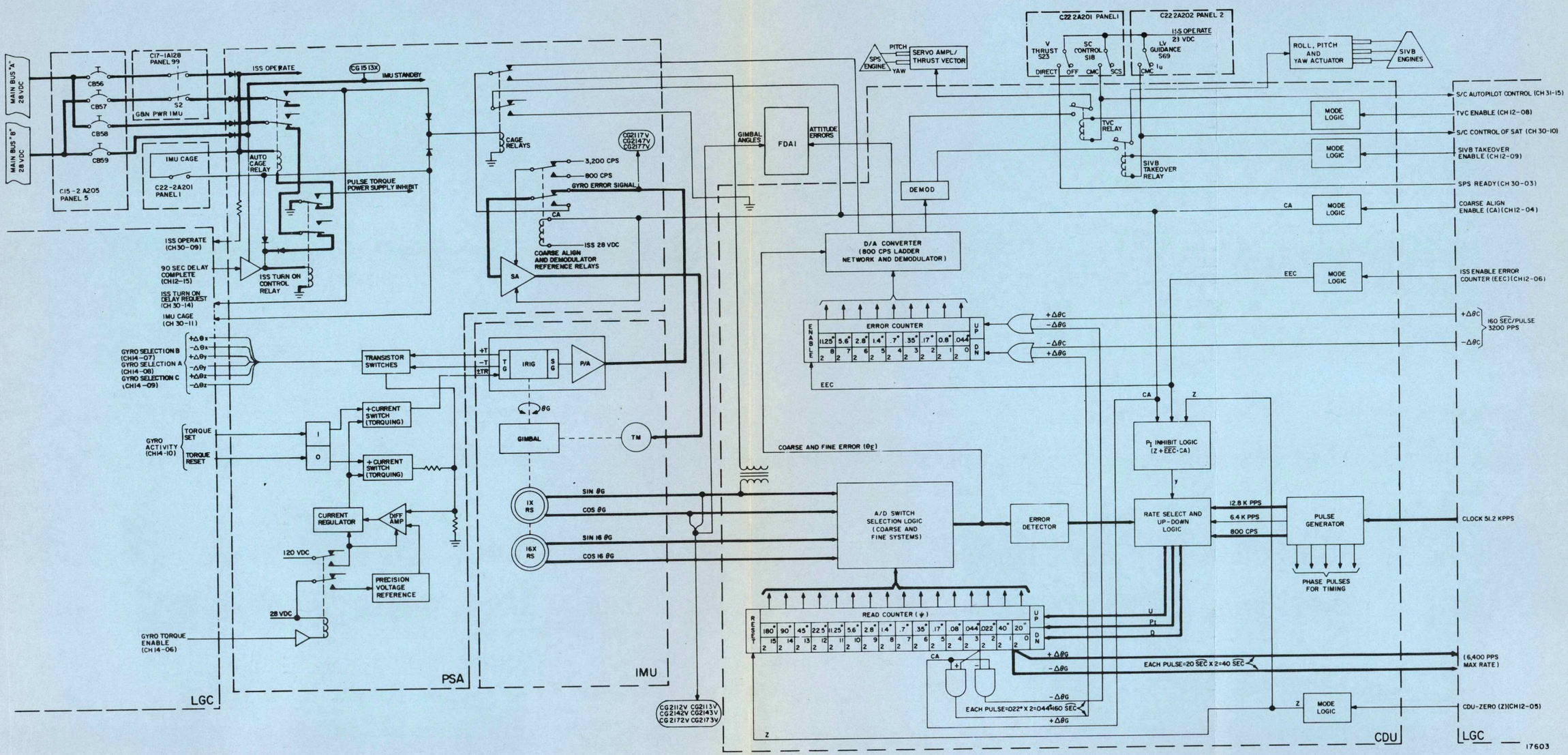


Figure 4-9. Inertial Reference Mode

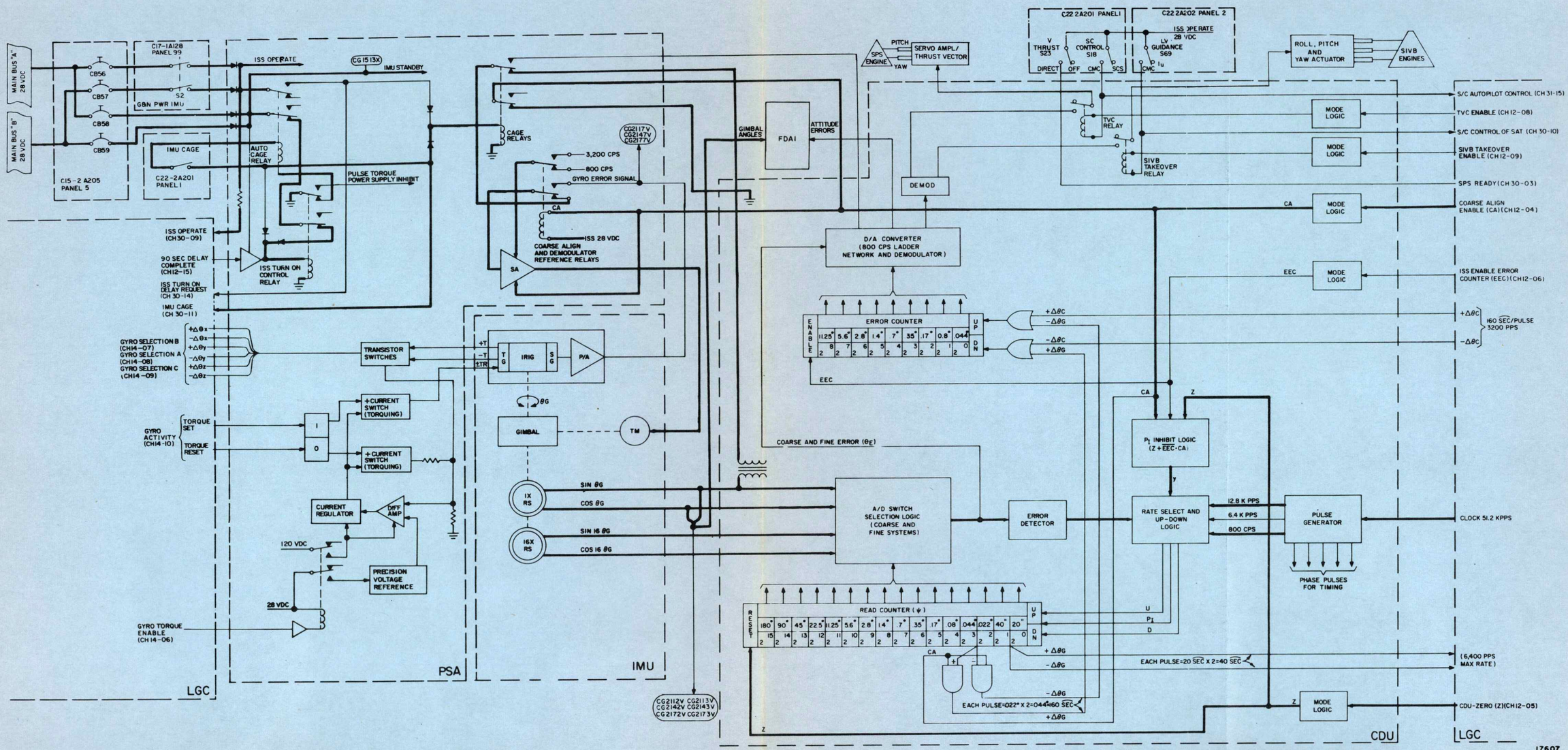


Figure 4-10. IMU Cage Mode

Upon receipt of the IMU cage discrete (CH 30-11), the computer will terminate gyro and ICDU driving, remove ICDU enable error counter and ISS turn-on delay complete discretes, and issue the ISS coarse align and ISS CDU zero discretes. Then the computer will turn on the NO ATTITUDE lamp (DSKY), inhibit PIPA, ICDU and IMU fail discretes, and set the X, Y, and Z CDU and gyro command output counters to zero.

After the IMU CAGE switch is released, the CMC will allow the read counters to settle, then will place the PGNCS in an attitude control mode. During the time the IMU cage discrete is present and while the read counters are settling, the NO ATTITUDE lamp on the DSKY is lighted.

The IMU cage mode will also be entered automatically whenever the IMU is turned on. During the normal turn on sequence, the closure of the ISS OPERATE circuit breaker will route 28 vdc through the deenergized contacts of the ISS turn on control relay to the cage relays. The cage relays energize and cage the gimbals. After the 90 second turn on time delay has been completed the CMC will (if it is on) send the ISS turn on delay complete discrete which will energize the ISS turn on control relay which, in turn, deenergizes the cage relays. If, however, the CMC is off or in standby when the IMU is turned on, the ISS turn on control relay will remain deenergized and the ISS will remain in the IMU cage mode.

If the IMU cage mode is entered as a result of an IMU turn on with the CMC off or in standby, the ISS may be placed in the inertial reference mode by allowing 90 seconds for gyro runup, then pressing the IMU CAGE switch. The IMU CAGE switch will energize and latch the auto cage relay control which removes the ISS 28 vdc which had been energizing the cage relays. With the auto cage relay control latched, the cage relay will deenergize when the IMU CAGE switch is released. Deenergizing the cage relays causes the coarse align relays to be deenergized which connects the gyro error signals to the respective gimbal servo amplifiers. The stabilization loops will maintain the stable member inertially referenced to the orientation established by the caging loops.

4.8 GIMBAL LOCK MODE

The purpose of the gimbal lock mode is to provide the astronaut with a discrete indication of a large middle gimbal angle and to disable the stab loop when gimbal lock actually occurs. This mode is a function of the T4 rupt routine. Every 480 millisec, the T4 rupt routine checks the Z CDU counter in E memory (middle gimbal angle). When the magnitude in this counter is greater than 70.0^{o}, the computer will turn on the GIMBAL LOCK lamp on the DSKY. This light will be turned off as soon as the T4 rupt routine finds the magnitude in this counter below 70.0^{o}. However, if the middle gimbal angle in the Z CDU counter increases to greater than 85^{o} degrees, the computer will light the NO ATTITUDE lamp on the DSKY, issue the ISS coarse align discrete, and inhibit the IMU fail. Issuing the ISS coarse align discretes will open the stab loops, which will reference the platform to the spacecraft. Refer to figure 4-11. The combination of the coarse align (CA) and not the enable error counter (EEC) will prevent the read counters from being incremented. The coarse and fine error signals to the D/A converter will be the only signal inputs to the stab amps. These signals, if any, will cause the gimbals to drive to the angle in the read counter. The astronaut can leave this mode by requesting the coarse alignment mode via DSKY input.

4.9 SIVB TAKE-OVER MODE

The purpose of the SIVB take-over mode is to use the command module guidance system as a backup system for the Saturn guidance system if the Saturn guidance system fails during

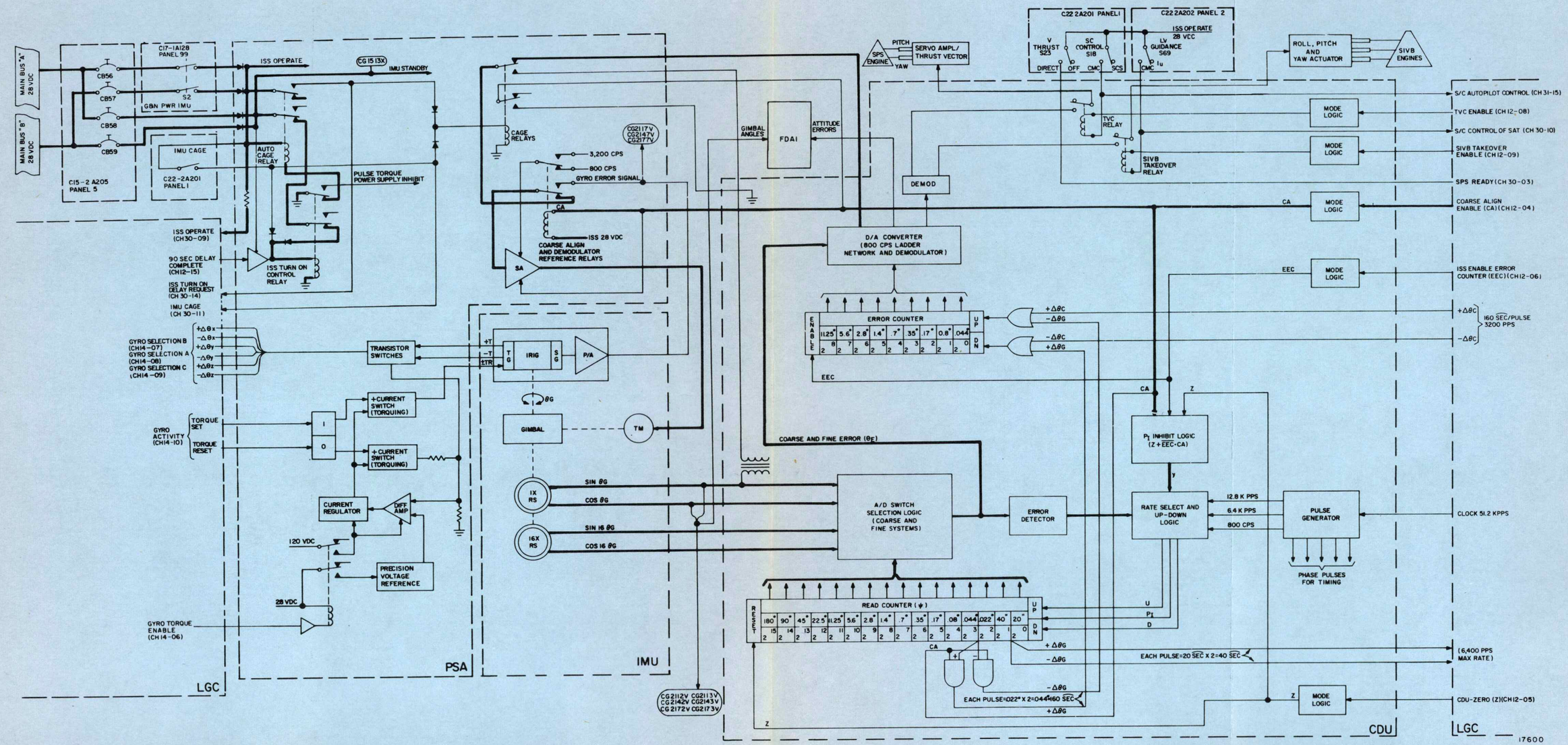


Figure 4-11. Gimbal Lock Mode

earth ascent, earth orbit, or translunar injection. This mode is initiated, by the astronaut, when he repositions the launch vehicle guidance switch (S69) from the 1U position to the CMC position. Closure of this switch routes a +28 vdc discrete to the ISS CDU where it arms the SIVB take-over relays and issues the S/C control of Saturn discrete (CH 30-10) to the CMC. Refer to figures 4-12 and 4-13. Receipt of this discrete causes the CMC to sequence through the following operations:

a. Remove any existing ISS EEC if the error counters are in operation.

b. Delay for a half second and then issue the SIVB take-over discrete (CH 12-09).

c. Delay for another 40 milliseconds and issue the ISS EEC discrete (CH 12-06).

d. Delay for another 4 milliseconds, the CMC starts to load the error counters with appropriate $\Delta\theta C$ pulses.

With the error counters enabled and the D/A converters dc outputs connected to the Saturn guidance system, the CMC can send steering signals to the Saturn guidance system. The CMC calculates the amount of yaw, pitch, and/or roll required for proper spacecraft attitude and determines the amount of $\pm\Delta\theta C$ pulses to be sent to the error counters. The error counters receive the $\pm\Delta\theta C$ pulses and count up or down as required until all pulses have been received. The error counters send this digital information to the D/A converters where it is converted to a dc signal and sent to the Saturn guidance system for attitude control. The CMC monitors the spacecraft response to the attitude signals through the read counters and the PGNCS PIP's. During this mode, the digital feedback signals from the read counters to the error counters are inhibited.

4.10 THRUST VECTOR CONTROL MODE

The purpose of the thrust vector control (TVC) mode is to allow the computer to control the thrusting of the SPS engine. The CMC has control of the gimbaling and the thrusting of the SPS engine. The TVC program requires two discrete inputs. They are SPS ready (CH 30-03), the result of ΔV thrusting switch (S23) in the direct position, and S/C autopilot control (CH 31-15) resulting from the S/C control switch (S18) being placed in the CMC position. Refer to figures 4-14 and 4-15. Closure of the S/C control switch routes a +28 vdc discrete to the optics CDU where it arms a set of relays which, when energized, connect the dc outputs of the optics CDU D/A converters to the SPS engine gimbal amplifiers. The +28 vdc discrete is also routed to the CMC. Receipt of this discrete by the CMC, signals the CMC to issue the thrust vector control discrete. The thrust vector control discrete energizes the control relays which connect the optics CDU D/A converters dc outputs to the SPS engine gimbal amplifiers. The CMC issues the optics D/A enable discrete 40 milliseconds after the thrust vector control discrete. With the optics error counters enabled and the optics CDU D/A converters dc outputs connected to the SPS engine gimbal amplifiers, the CMC can send steering control signals to position the SPS engine gimbals. The CMC calculates the amount of pitch or yaw required for proper trajectory and then determines the amount of $\pm\Delta\theta C$ pulses to be sent to the error counters. The error counters receive the $\pm\Delta\theta C$ pulses and count up or down as required until all pulses have been received. The error counters send this digital information to the D/A converters where it is converted to a dc signal and routed to the SPS engine gimbal amplifiers. The CMC monitors spacecraft response to the engine gimbal steering signals through the ISS CDU read counters and the PGNCS PIP's. During this mode, the digital feedback signals from the read counters to the error counters are inhibited.

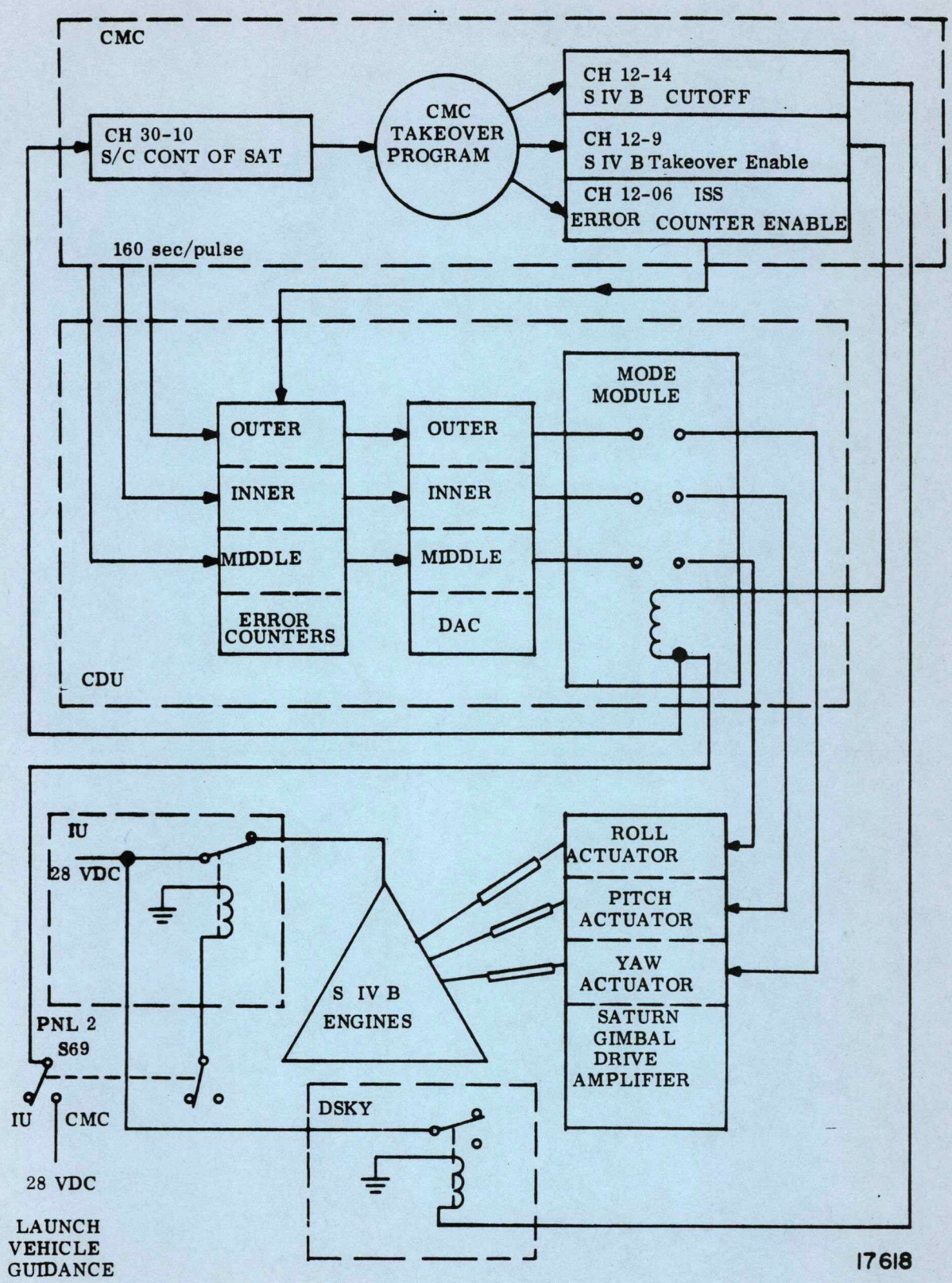


Figure 4-12. SIVB Take-over Mode Interface

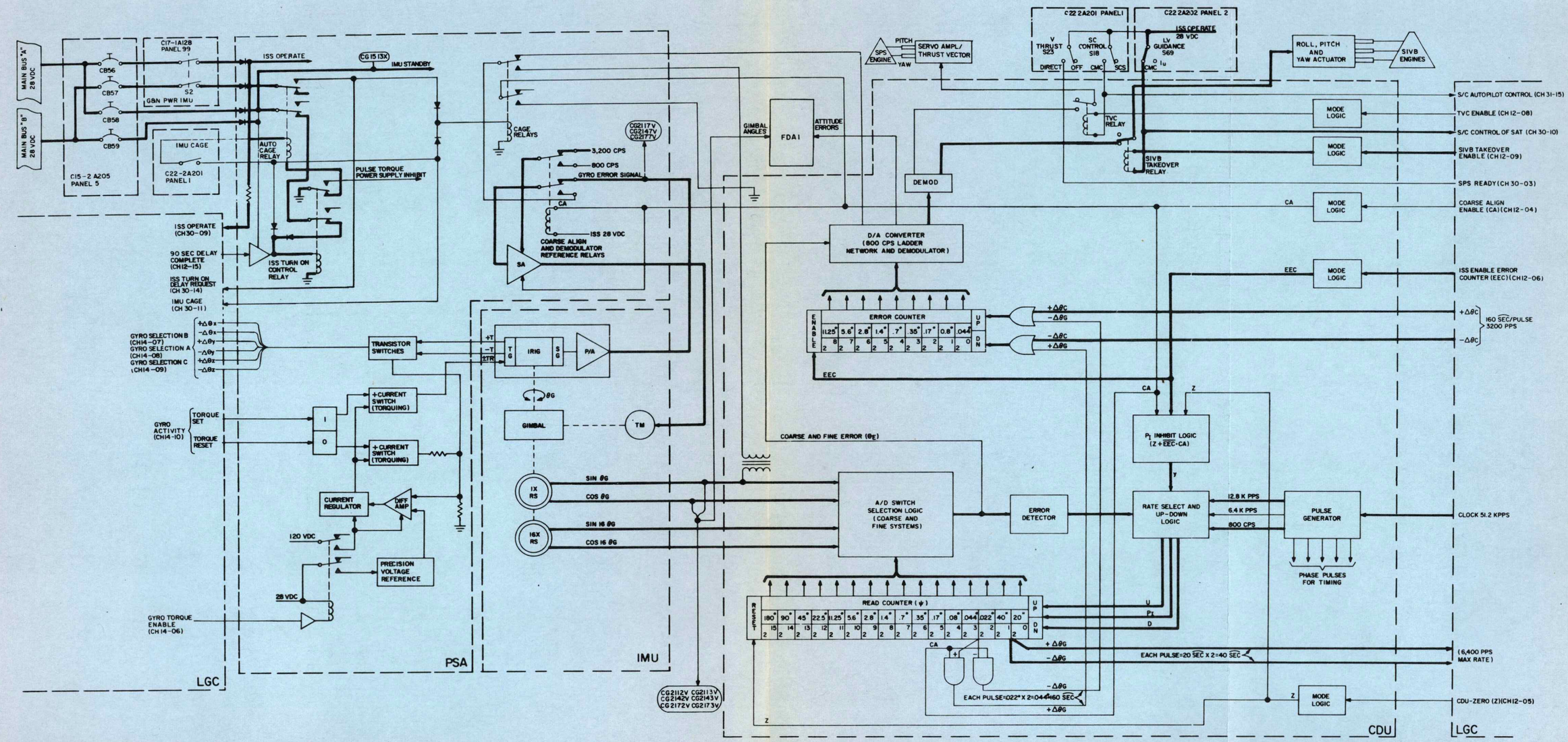


Figure 4-13. SIVB Take-over Mode

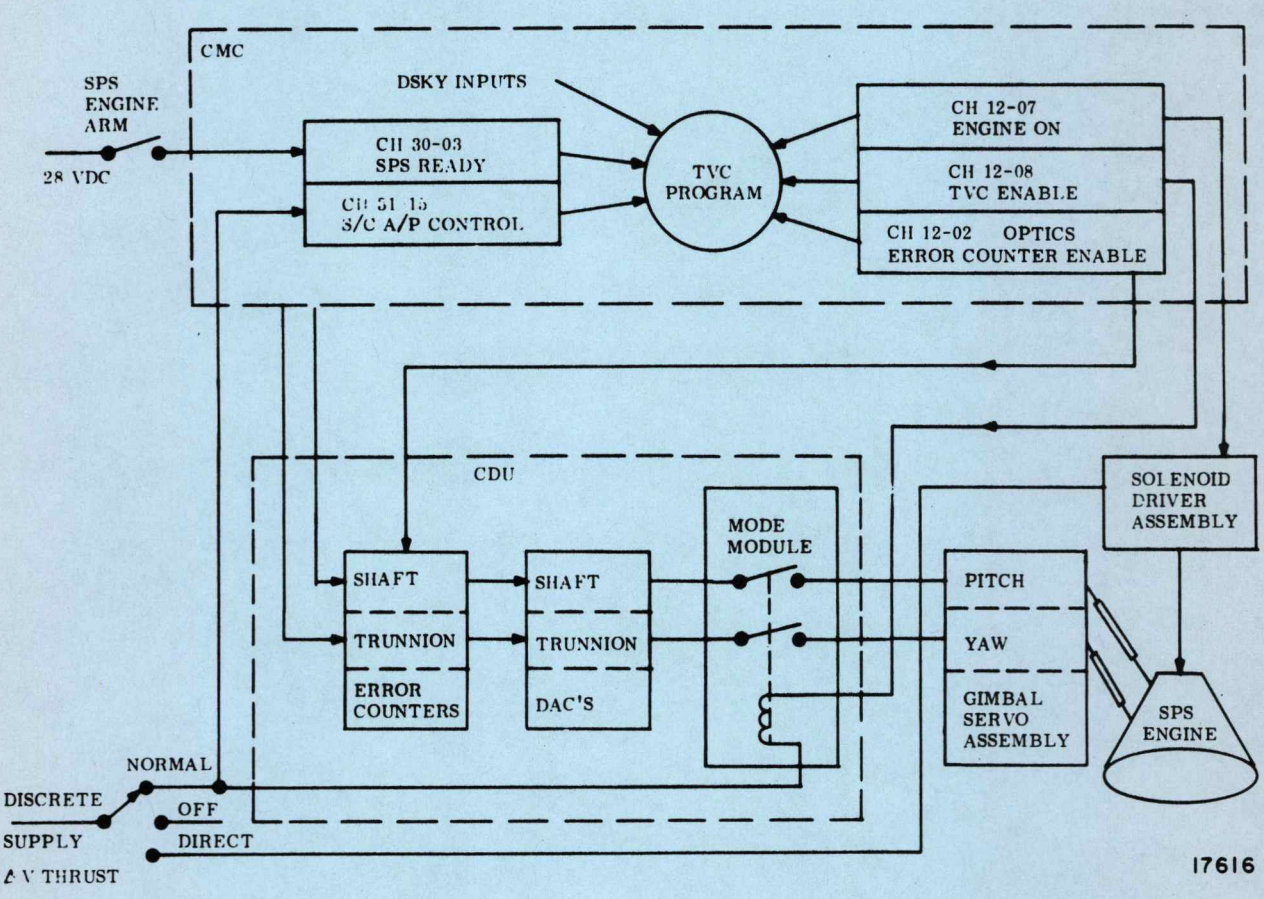


Figure 4-14. Thrust Vector Control Mode Interface

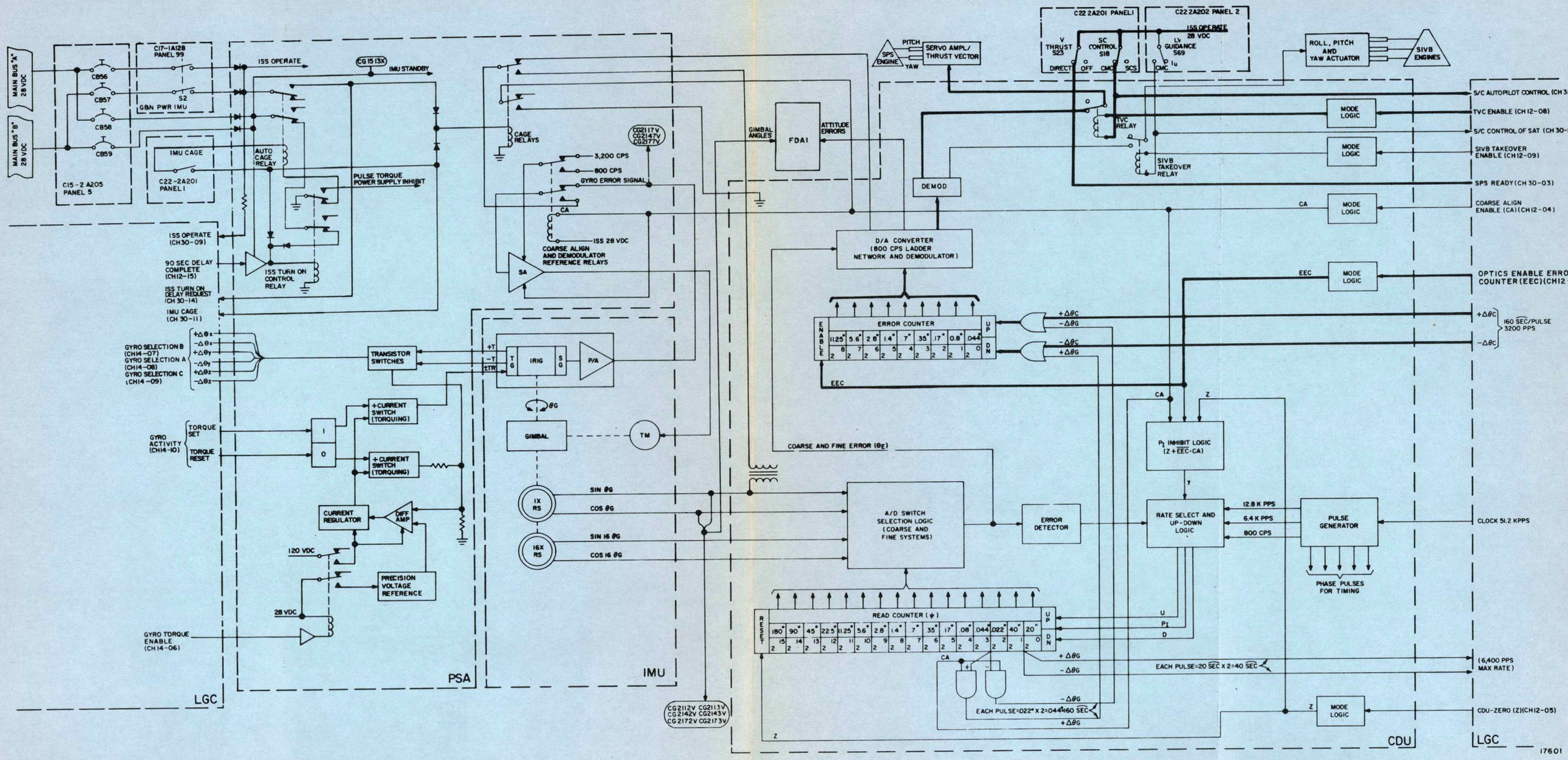


Figure 4-15. Thrust Vector Control Mode

Prior to the CMC issuing the thrust vector control discrete, the CMC checks to see if the optics CDU error counters are in use. If the error counters are being used, the CMC removes the optics D/A enable discrete which inhibits and clears the error counters. The CMC will then issue the thrust vector control discrete.

4.11 ATTITUDE CONTROL MODE

The attitude control mode, a PGNCS mode, utilizes the digital autopilot to maintain spacecraft attitude. The ISS stabilization loops maintain an inertial reference from which spacecraft attitude can be determined. The spacecraft attitude is compared to a desired attitude by the digital autopilot. If an error exists, the RCS jets are used to change the spacecraft attitude. Attitude errors are displayed on the FDAI. Refer to figures 4-8 and 4-16.

During the attitude control mode, the error counter is enabled. The computer sends the desired change in gimbal angle orientation to the error counters. The output of the error counters is developed into an analog error signal (attitude error signal) by the 800 cps ladder network and the output is fed to the FDAI. The computer develops discretes that control the firing of RCS jets and, therefore, change the orientation of the spacecraft. The change in spacecraft orientation is sensed by the IMU stabilization loops and results in changing IMU gimbal angles. The gimbal resolver output is sent to the FDAI to display total attitude and to the summing logic and coarse fine mixing circuit. Resulting digital information is sent to the read counter. The read counter supplies the changing gimbal angle pulses to the CMC. The CMC uses the information in determining when to stop firing the RCS jets. The FDAI error counter is pulsed to zero, nulling the attitude error signal on the FDAI.

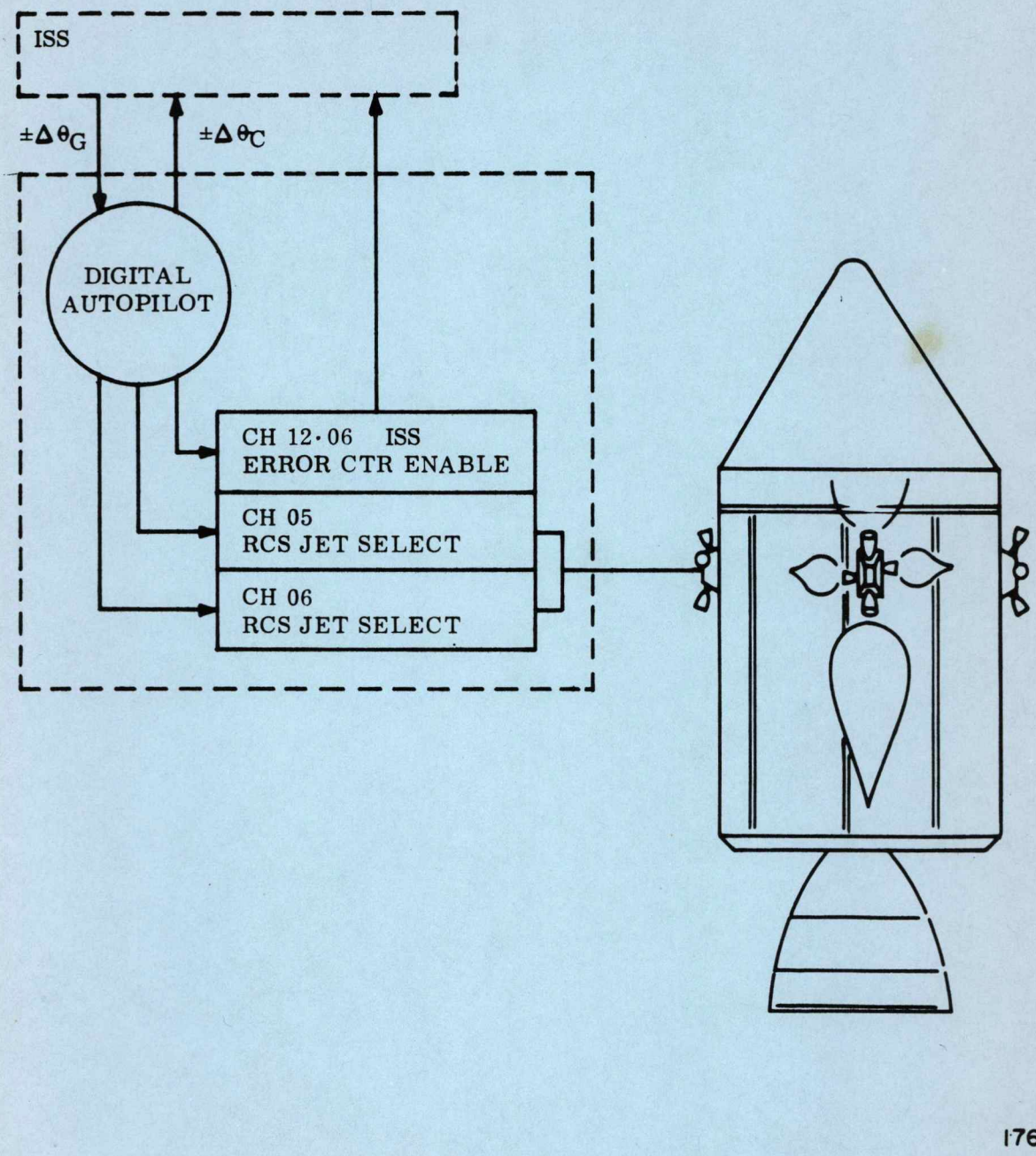


Figure 4-16. Attitude Control Mode

SECTION V

IMU TEMPERATURE CONTROL SYSTEM

INTRODUCTION

The purpose of the IMU Temperature Control System is to maintain the temperature of the IRIG's and PIP's within their required temperature limits. This system is designed to supply and remove heat as required to maintain heat, with minimum power consumption. This system is divided into two functional sections. The first section is used for adding heat to the inertial components, and the second section is used for removing excess heat. Heat is added to the inertial components via resistance wire heaters which are controlled by several different circuits. Excess heat is removed from the stable member by thermostatically controlled fans. Refer to figure 5-1. The IMU is pressurized with dry nitrogen to one atmosphere. This allows the fans to cause a forced convection mode of operation which circulates the dry nitrogen between the middle gimbal and the IMU case. The IMU case contains the ECS's water-glycol heat exchanger. The water-glycol input temperature is approximately 45^{o} F.

The temperature control system is divided into four circuits. All four circuits are shown on figure 5-2. The name and function of each circuit is as follows:

a. The temperature control circuit - adds heat during ISS standby and operate modes.

b. The blower control circuit - removes heat during ISS operate.

c. The temperature alarm circuit - monitors platform temperature during system operation, ISS standby and CSS standby.

d. External temperature circuit - separate heaters and sensors used for platform temperature control below standby.

5.1 TEMPERATURE CONTROL CIRCUIT

The temperature control circuit maintains the gyro and accelerometer temperature. The temperature control circuit consists of a temperature control thermostat and heater assembly, a temperature control module, three IRIG end mount heaters, three IRIG tapered mount heaters, two stable member heaters, and three accelerometer heaters. The thermostat and heater assembly is located on the stable member and contains a mecury-thallium thermostat, a bias heater, and an anticipatory heater. Except for the bias heater, all heaters (a total of 12) are connected in parallel, and are energized by 28 volts dc through the switching action of transistor Q2, which completes the dc return path. The thermostat which senses the temperature of the stable member controls switching transistors Q1 and Q2.

When the temperature falls below 130 (±0.2) degrees Fahrenheit, the thermostat opens, transistors Q1 and Q2 conduct, and current flows through the twelve heaters. Because of the large mass of the stable member, its temperature will increase at a relatively slow rate as compared to the gyros which have a heater in each end mount. The anticipatory heater improves the response of the thermostat to insure that the magnitude of the temperature cycling of the gyros and the accelerometers is as small as possible. When the temperature rises above 130 (±0.2) degrees Fahrenheit, the thermostat closes and the base of transistor Q1 is shorted to ground, cutting off transistors Q1 and Q2 and deenergizing the heaters. The thermostat has a 0.5 degree deadband which is the difference between contact closing with rising temperature and contact opening with falling temperature. The temperature

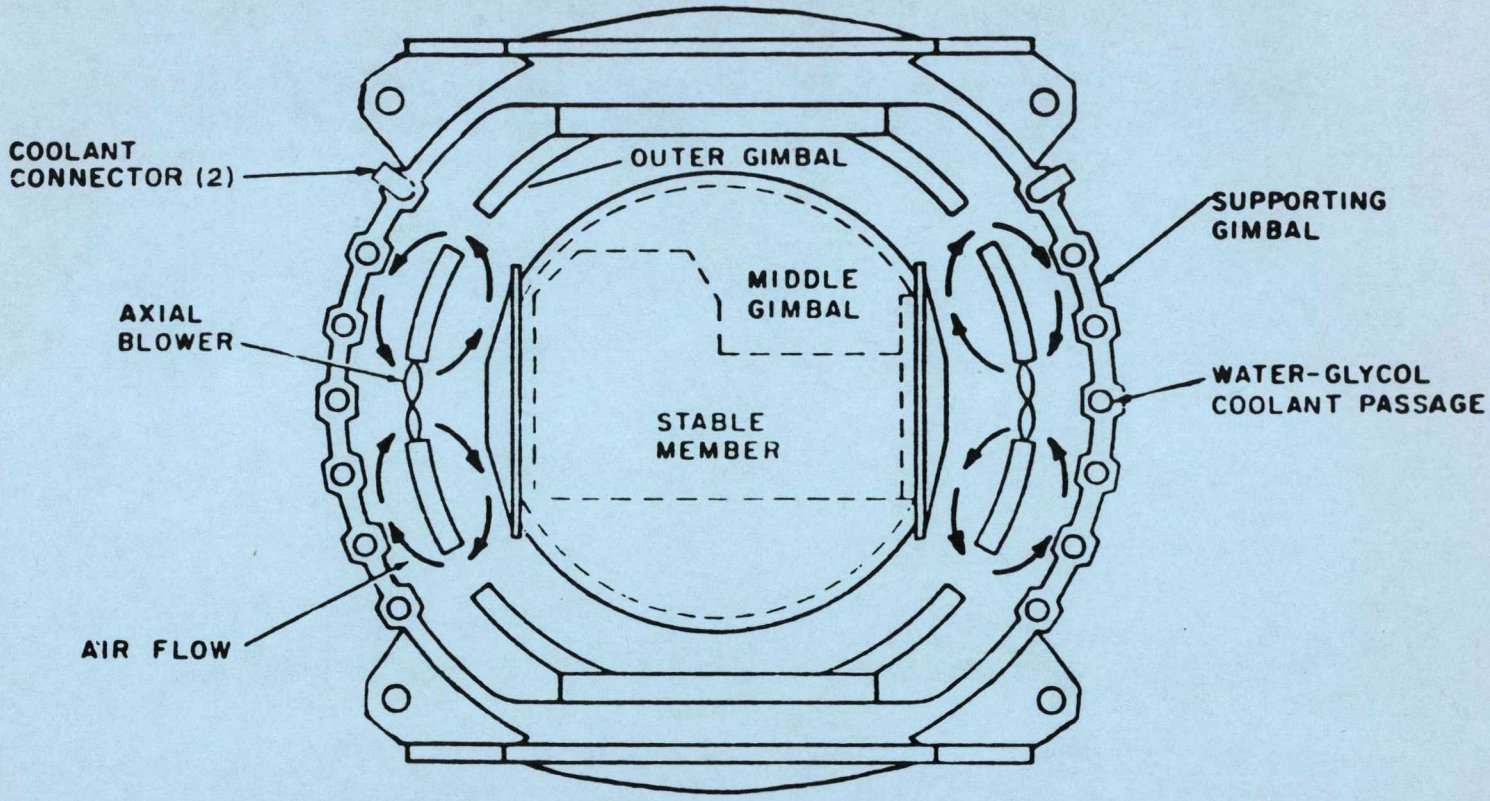


Figure 5-1. Block II Forced Convection in IMU

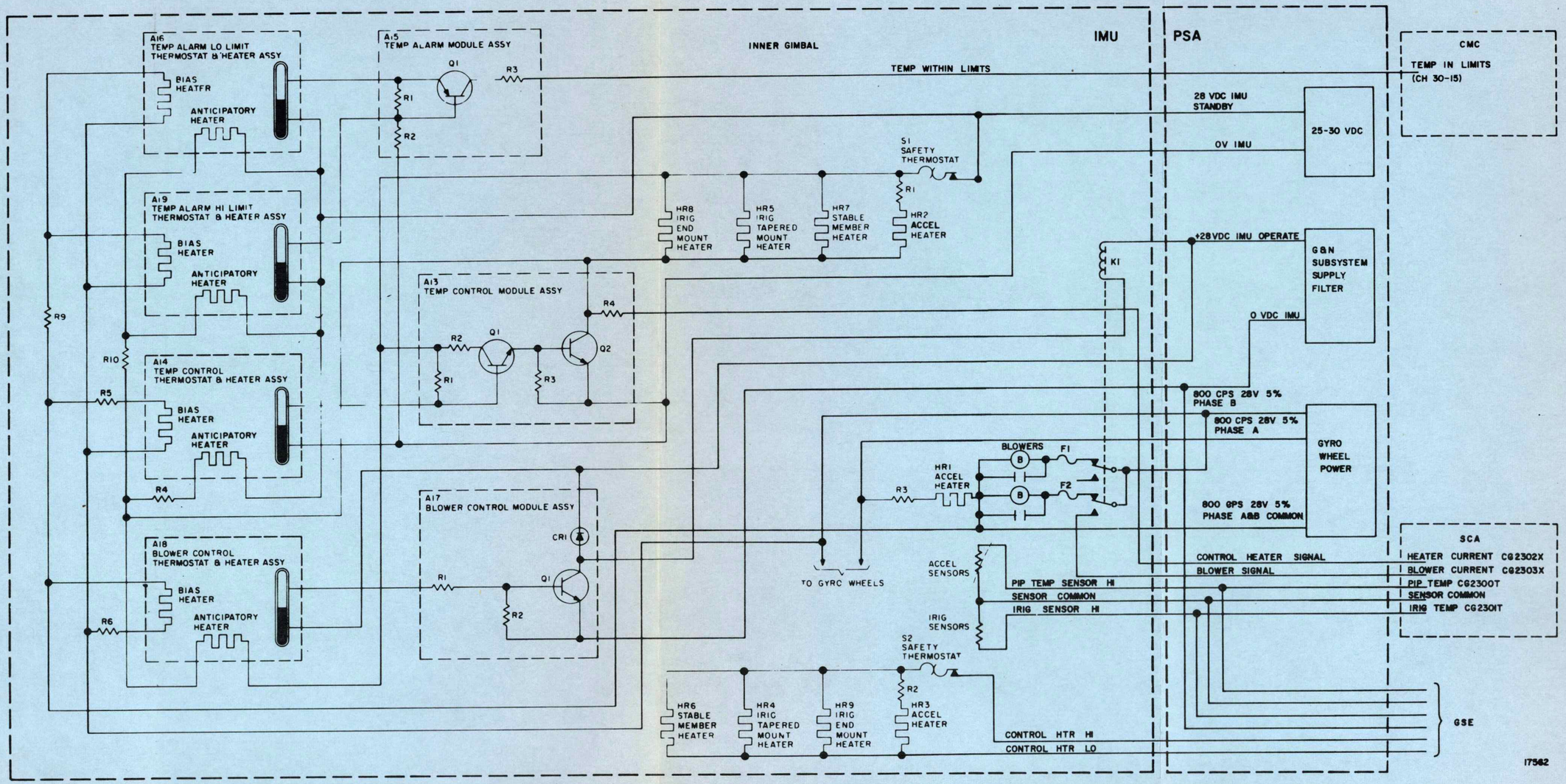


Figure 5-2. Temperature Control System

control circuit will maintain the average of the gyro temperatures at 135 (±1) degrees Fahrenheit under normal ambient conditions. The temperature difference between the gyros and the accelerometers is adjusted by properly proportioning the amount of power in each heater. The balance is obtained by decreasing the current through each accelerometer heater by the proper selection of resistor R1.

During IMU operation, power is applied to the fixed accelerometer heaters to compensate for the additional heat supplied to the gyros by the gyro wheel motor heat dissipation. Power is also applied to a bias heater on the control thermostat. The bias heater supplies a fixed amount of heat to the control thermostat to maintain the proper absolute temperature level of the gyros and accelerometers. The amount of bias heat is determined by the value of R5. The power for the fixed accelerometer heaters and the thermostat bias heater is the -90 degree output from the 28 vac power supply which is also used for gyro wheel power.

The 28 vdc heater power is applied to the heaters through the contacts of a safety thermostat which provides protection against an extreme overheat condition in case a malfunction occurs in the temperature control circuit. The safety thermostat contacts open at 139.5 (±3.0) degrees Fahrenheit and close at 137 (±3) degrees Fahrenheit.

5.2 BLOWER CONTROL CIRCUIT

The blower control circuit maintains IMU heat balance by removing heat. The blower control circuit consists of a blower control thermostat and heater assembly, a blower control module assembly, two axial blowers, and a relay. The contacts of the thermostat contained in the blower control thermostat and heater assembly close at 139 (±0.2) degrees Fahrenheit and remain closed at higher temperatures. Resistor R6 is provided to limit the current through the bias heater in the blower control thermostat and heater assembly. The amount of heat supplied by the bias heater is a constant. If the duty cycle of the temperature control circuit exceeds 50 percent, enough additional heat will be provided by the anticipatory heater to increase the temperature of the blower control thermostat and heater assembly to 139 degrees Fahrenheit. When the thermostat contacts close, transistor Q1 conducts and relay K1 is energized to remove the power from the blowers. The normal duty cycle of the temperature control circuit, with the IMU in a 75 degree Fahrenheit ambient temperature, is approximately 15 to 20 percent. Under this condition the blowers will operate continuously. Only a very low ambient temperature will cause a blower off condition.

Power to the blowers is supplied from the -90 degree output of the 28 volt, 800 cps, 5 percent power supply which also provides gyro wheel motor power. Fused phase shift networks are associated with each blower so that excitation and control current can be supplied from the same source.

5.3 TEMPERATURE ALARM CIRCUIT

The temperature alarm circuit which monitors the temperature control system, consists of a temperature alarm high limit thermostat and heater assembly, a temperature alarm low limit thermostat and heater assembly, and a temperature alarm module assembly. If a high or low temperature is sensed by the thermostats located on the stable member a discrete is sent to the CMC and to the IMU auxilliary module. When the temperature is within the normal range, the low limit thermostat contacts are closed and the high limit thermostat contacts are open. Transistor Q1 is then properly biased for conduction through a grounding system in the CMC.

At temperatures below 126.0 (±0.2) degrees Fahrenheit both the low limit thermostat contacts and the high limit thermostat contacts are open. At temperatures above 134.0 (±0.2) degrees Fahrenheit, both the low limit thermostat contacts and the high limit thermostat contacts are closed. In either case, transistor Q1 is not able to conduct. Non-conduction of transistor Q1 signals the CMC of an alarm condition. There is no differentiation between a high or low temperature alarm. When the CMC senses a temperature alarm, it causes the TEMP and PGNCS lamps to light. When the IMU auxiliary module receives a temperature alarm, it sends the information to telemetry.

5.4 EXTERNAL TEMPERATURE CONTROL CIRCUIT

External temperature control of the IMU is provided by ground support equipment (GSE) control heater circuits in the IMU. The circuits are controlled externally to the airborne equipment by the portable temperature controller or the temperature monitor control panel of the optics inertial analyzer (OIA). The GSE control heater circuitry consists of a safety thermostat, six gyro heaters, two stable member heaters, three accelerometer heaters, temperature indicating sensors, and an IMU standby power sensor which disables the GSE when airborne power is on. The temperature indicating sensors act as the control sensing element of the external control and indicating circuitry. The heaters are connected in parallel. The six gyro temperature indicating sensors (two in each gyro) are connected in series to sense the average temperature of the gyros. The three accelerometer temperature indicating sensors (one in each accelerometer) are connected in series to sense the average temperature of the accelerometers. All of the GSE control heater circuitry is not available as a backup system in flight. The GSE temperature indicating sensors are used as the telemetry sensors during flight.

SECTION VI

DISPLAYS AND CONTROLS PANELS OF THE LOWER EQUIPMENT BAY

INTRODUCTION

This section will deal with the PGNCS controls and displays which are located in the lower equipment bay (LEB). The LEB PGNCS panels are; 1) the indicator control panel (PNL 105), 2) the lighting control panel (PNL 99), and 3) the navigation panel display and keyboard (DSKY) (PNL 106).

6.1 INDICATOR CONTROL PANEL

The indicator control panel is a component part of the OSS (figure 6-1). It provides displays and controls and is equipped with electroluminescent lamps for the following functions:

a. Manual spacecraft maneuvering

b. Manual optics positioning

c. Optics mode control

d. Warning caution and status lamps

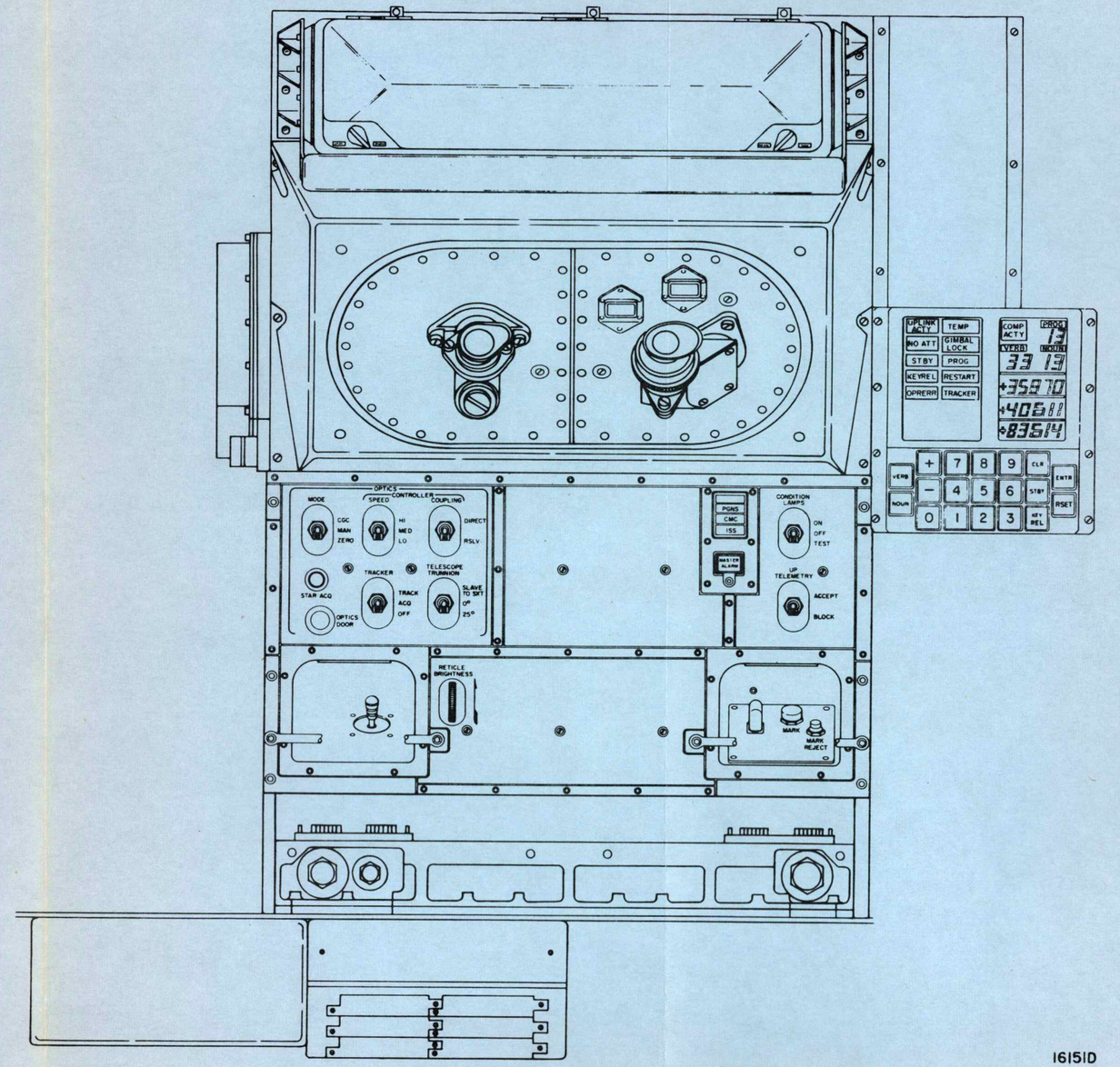
Table 6-1 contains a list of all indicator control panel controls and indicators. This table also gives the function of each control or indicator and a reference to a detailed explanation within this study guide.

6.2 DISPLAY AND KEYBOARD

The Display and Keyboard (DSKY) is a component part of the computer subsystem. Two DSKY's are used in the command module, one is in the navigators station of the main panel D and C and the second is part of LEB. The DSKY's are connected in parallel as far as displays and controls are concerned. Section X of this study guide contains a detailed explanation of the DSKY displays and controls.

6.3 LIGHTING CONTROL PANEL

The lighting control panel contains two G&N power switches. Reference figure 6-2. Switch S1 (optics) is used for applying optics operate power to the OSS. Refer to paragraph 7-4 of this study guide. Switch S2 (IMU) is used for ISS operate power as explained in paragraph 7-2 of this study guide.



16151D

Figure 6-1. Navigation Station (LEB)

Table 6-1. Indicator Control Panel

Control or Indicator	Function	Reference Section
OPTICS MODE selector	Selects circuitry for either zeroing optics, manual control of optics, or CMC control of optics.	9
OPTICS TRACKER selector	Not used.	
OPTICS SPEED CONTROLLER	Varies voltage for optics hand controller use.	9
OPTICS COUPLING CONTROLLER	Selects either direct or resolved positioning of optics.	9
OPTICS TELESCOPE TRUNNION selector	Slaves SCT to SXT S_tLOS or SXT LLOS, or offsets SCT 25° in trunnion angle from SXT LLOS.	9
PGNS condition lamp	Indicates malfunctions in PGNCS equipment.	8
CMC condition lamp	Indicates malfunctions in CMC equipment.	8
ISS condition lamp	Indicates malfunctions in ISS equipment.	8
CONDITION LAMPS selector	Enables condition lamp circuitry or lights condition lamps for test.	8
MASTER ALARM lamp and pushbutton	Indicates failure in PGNCS and allows resetting of alarm circuitry.	8
UP TELEMETRY switch	Allows or blocks telemetry data from ground stations to be entered into CMC.	8
Attitude impulse hand control	Supplies signals to reaction control system to position the spacecraft in attitude.	9
MARK pushbutton	When pressed, sends signals to CMC to record time and optics and gimbal angles.	9
MARK REJECT pushbutton	Cancels input initiated by MARK pushbutton.	9
RETICLE BRIGHTNESS control	Varies voltage to change reticle lamp brightness.	9
Optics hand controller	Supplies signal to drive optics about shaft axis and/or trunnion axis in manual mode.	9
OPTICS DOOR	Not used.	
STAR ACQ lamp	Not used.	

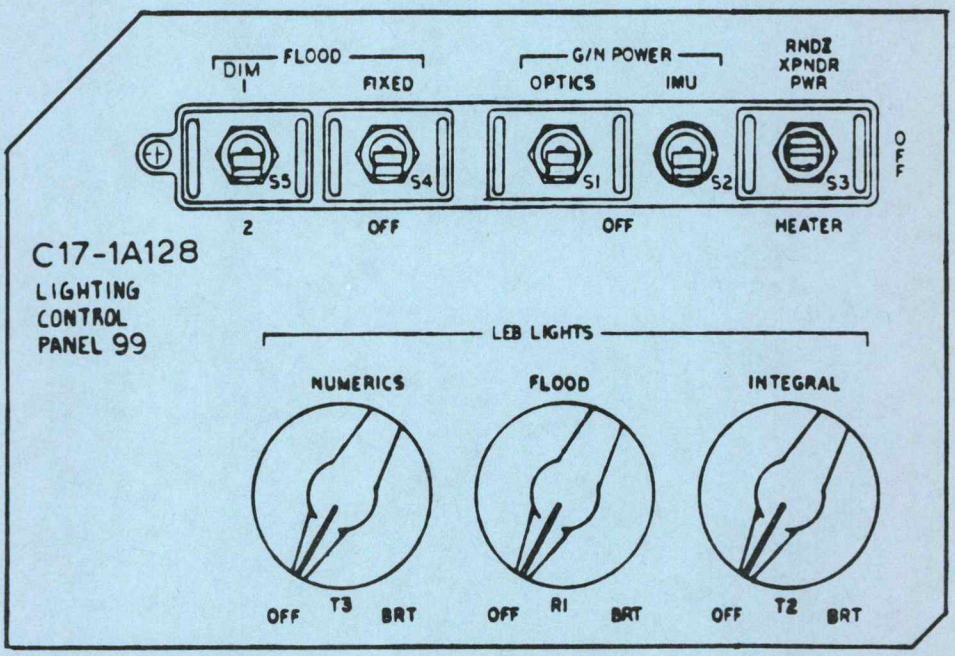


Figure 6-2. Lighting Control Panel

SECTION VII

POWER SUPPLIES AND DISTRIBUTION

INTRODUCTION

The PGNCS receives +28 VDC from main bus A and/or main bus B via circuit breakers. This power is divided into four circuits. This section is devoted to the explanation of this power distribution and the power supply circuits that they supply.

7.1 ISS STANDBY POWER

The +28 VDC ISS standby power is used to supply ISS power during both standby and operating modes. Standby power can only be removed when other arrangements for heater power have been made such as the PSAAM or GSE. In the airborne configuration, standby power is routed through circuit breakers CB58 and/or CB59 and is used to supply the optics eyepiece heaters, the 3200 cps power supply, and the PIPA and IRIG control heaters. Refer to figure 7-1. If standby power is removed when the ISS is operating, the IMU will automatically enter the cage mode of operation. This may damage the gyros.

7.2 ISS OPERATE POWER

The +28 VDC ISS operate power is used to raise the ISS into an operating mode. Power is applied through circuit breakers CB56 or CB57 through the IMU switch (S2) to the PSA. Refer to figure 7-2. ISS operate power is supplied to the ICDU, the SCA, the PIPA pre-amps, gimbal servo amplifiers, and power supply circuits within the PSA. Loss of the ISS operate power will downmode the ISS to standby.

7.3 CMC OPERATE POWER

Power is supplied to the CSS via circuit breakers CB60 and 61. The computer has two modes of operation, standby and operate. These circuit breakers must be closed during both modes. Refer to figure 7-3. The CSS standby power circuits are enabled by either of the circuit breakers. The operate power circuits require both the power input from the circuit breakers and an enable signal from the DSKY standby pushbutton. To downmode the CSS from operate to standby, a V60 (prepare for standby) must be entered via the DSKY. When the CMC completes this routine, it will enable the standby pushbutton and closure of the standby PB now will inhibit the operate power circuits which will downmode the CMC.

7.4 OSS OPERATE POWER

The OSS operate is supplied via circuit breakers CB62 and for CB63 and the G & N power optics switch (S_1). Refer to figure 7-4. 28 VDC OSS operate power is supplied to the motor drive amplifiers, the optics CDU channels, optics relays, the anti creep circuits and the OSS 800 cps power supply.

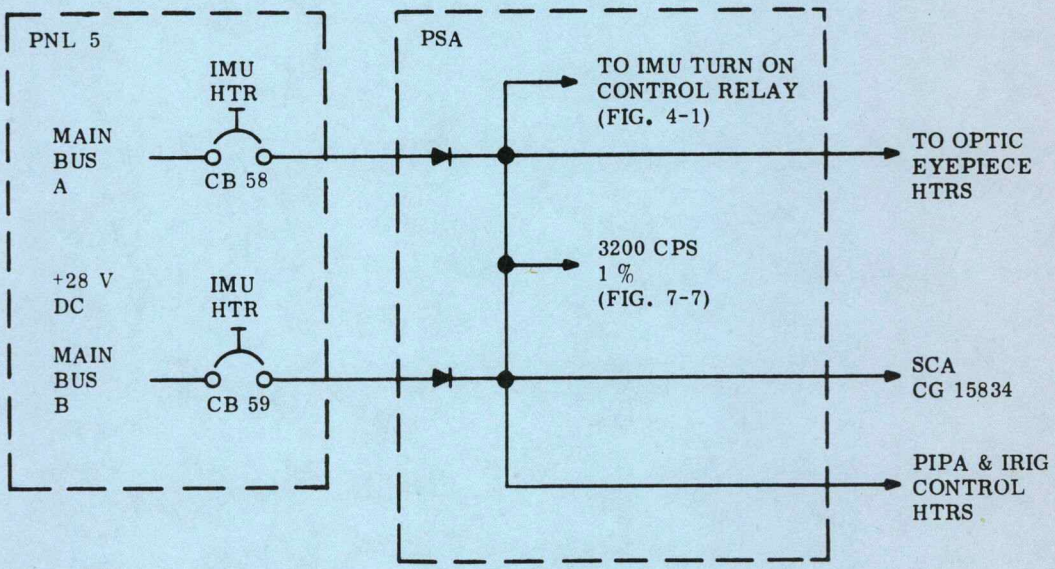


Figure 7-1. ISS Standby Power Distribution

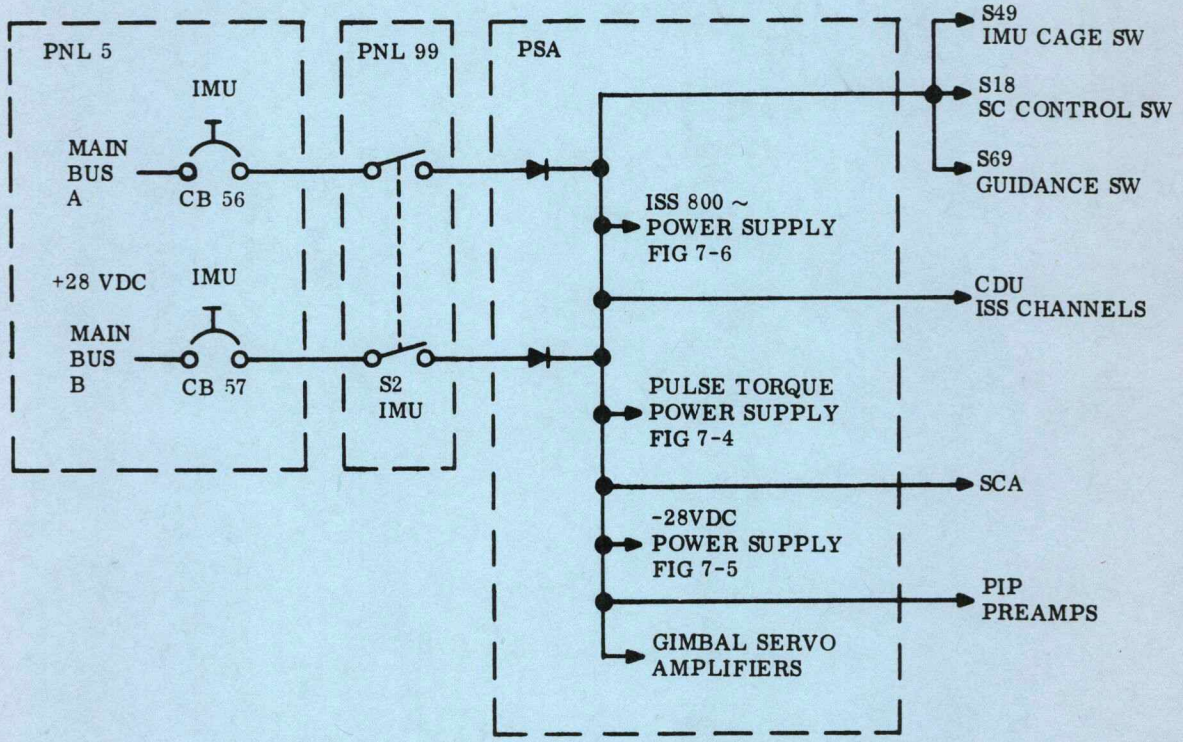


Figure 7-2 ISS OPERATE POWER DISTRIBUTION

Figure 7-2. ISS Operate Power Distribution

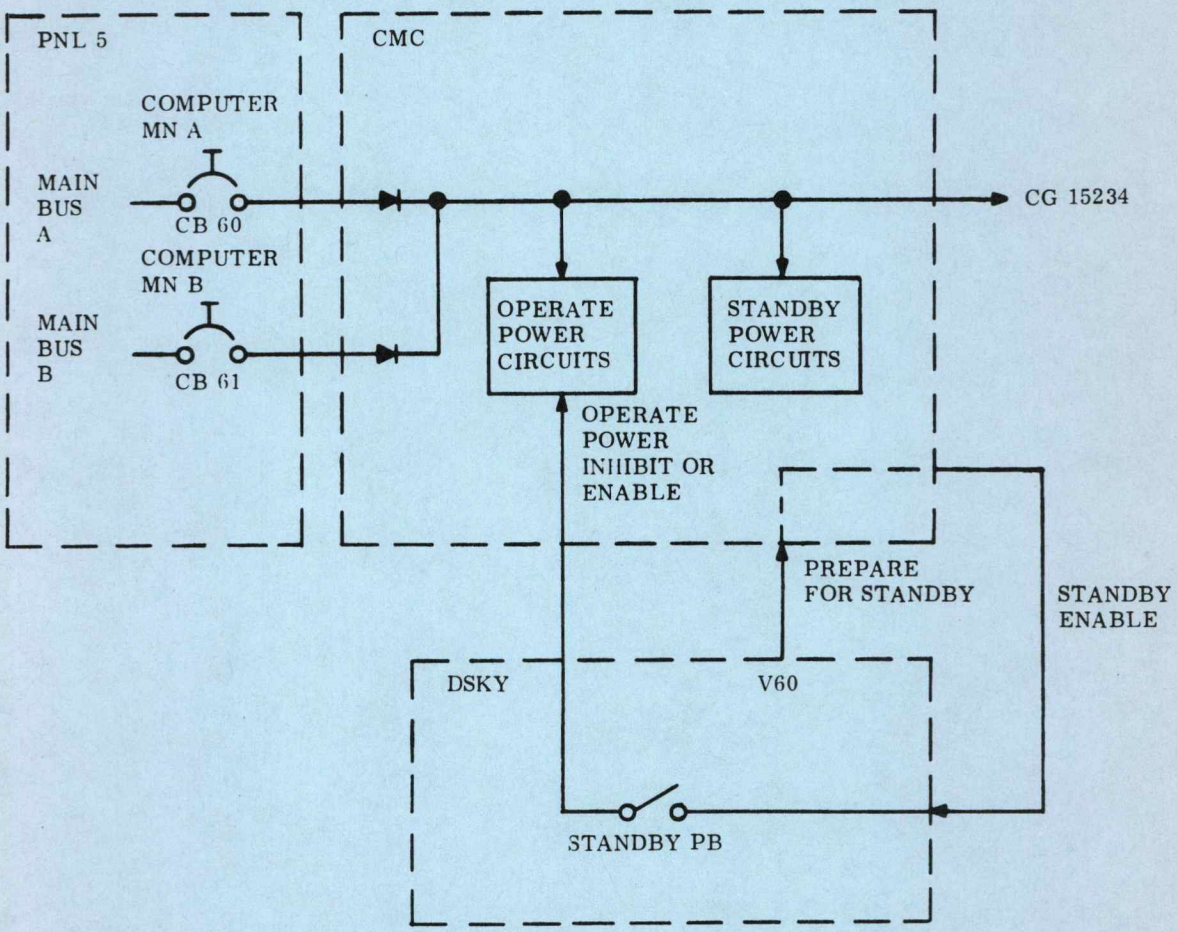


Figure 7-3. +28 VDC CMC Operate Power

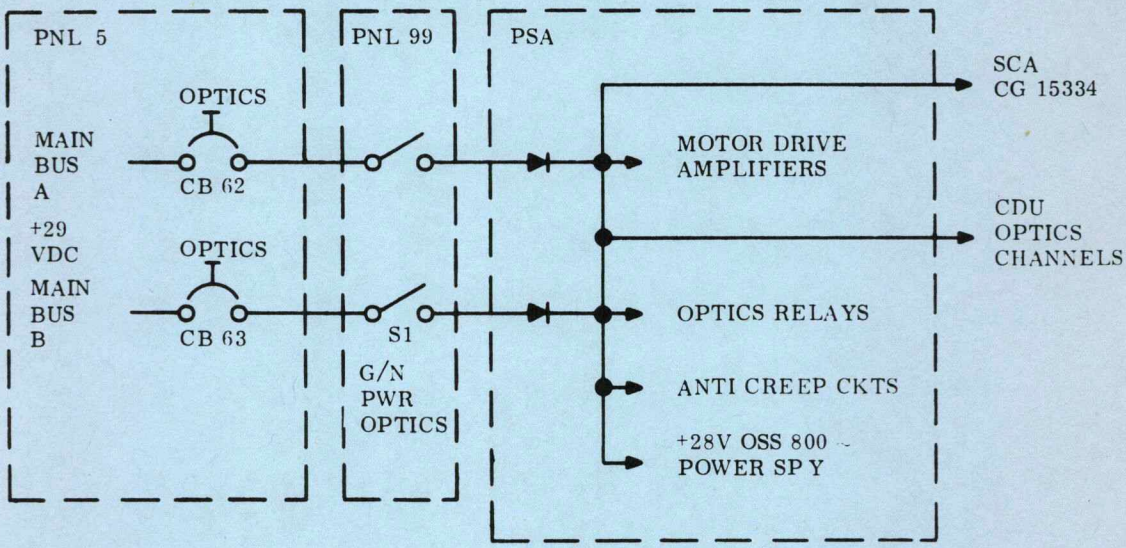


Figure 7-4. OSS Operate Power Distribution

7.5 POWER SUPPLY CIRCUITS

The following is a detailed explanation of the individual power supply circuits within the PGNCS.

7.5.1 PULSE TORQUE POWER SUPPLY. The pulse torque power supply (figure 7-5) provides 120 vdc to the three binary current switches and three dc differential amplifiers in the accelerometer loops, and the binary current switch and dc differential amplifier in the stabilization loop fine align electronics. The pulse torque power supply also provides three individual 28 vdc outputs to the accelerometer loop PVR's, 20 vdc to the three accelerometer loop ac differential amplifier and interrogator modules and the associated binary current switches, and -20 vdc to the ac differential amplifier and interrogator module in the accelerometer loops.

The -20 vdc output is derived from the -28 vdc power supply by using a zener diode as a voltage divider and regulator. The output is regulated at -20 (±0.8) vdc.

The 20 vdc output is derived from 28 vdc prime power by the use of a three transistor series regulator which maintains the output voltage at 20 (±0.55) vdc.

The 120 vdc and 28 vdc outputs are derived from a multivibrator, a power amplifier, and a rectifier and filter. A 12.8 kpps synchronizing pulse is received from the CMC through a buffer transformer in the pulse torque isolation transformer assembly and is applied to an amplifier-inverter. The output of the amplifier-inverter is applied to a multivibrator-chopper causing the multivibrator-chopper to be synchronized at 6,400 cps. A transistorized time delay circuit is incorporated into the emitter circuits of the multivibrator to provide a turnon time delay of approximately 350 milliseconds. During the 90 second IMU turnon mode, 0 vdc is applied through the turnon circuits of the IMU auxiliary assembly module to the time delay circuit which inhibits the 120 vdc and 28 vdc PVR supplies. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a two stage push-pull power amplifier which operates from 28 vdc prime power. The output of the power amplifier consists of a transformer with four secondary windings; one with center tap return for the 120 vdc power supply, and one each for the X, Y, and Z accelerometer loop 28 vdc PVR supplies. The 120 vdc power supply consists of a full wave rectifier whose output is filtered, regulated, and again filtered. The 28 vdc power supplies are identical and consist of a full wave bridge rectifier whose output is filtered, regulated, and again filtered. The PVR time delay circuit inhibits the operation of the regulator in each 28 vdc PVR circuit to provide a six to eight second time delay in the 28 vdc PVR outputs.

7.5.2 -28 VDC POWER SUPPLY. The -28 vdc power supply provides input power to the three gimbal servo amplifiers in the stabilization loops and to the pulse torque power supply to generate -20 vdc for use in the accelerometer loops. The -28 vdc power supply consists of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, and a rectifier and filter. (See figure 7-6.) The 25.6 kpps synchronization pulse input is amplified and inverted for use in synchronizing the multivibrator-chopper at 12.8 kcps. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a push-pull power amplifier. The output of the amplifier is transformer coupled to a full wave rectifier and filter whose positive side is referenced to ground to provide a -27.0 (±1.0) vdc output.

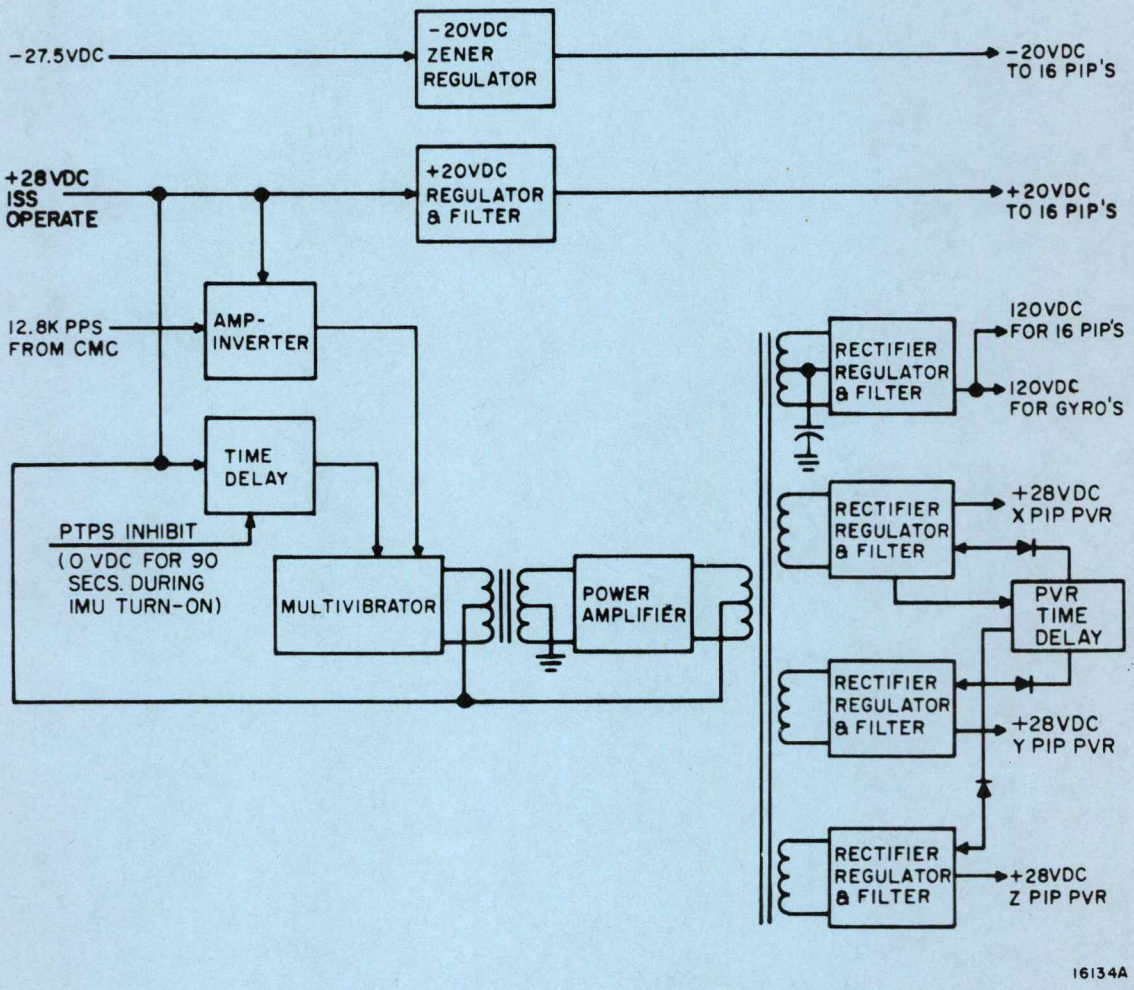


Figure 7-5. Pulse Torque Power Supply

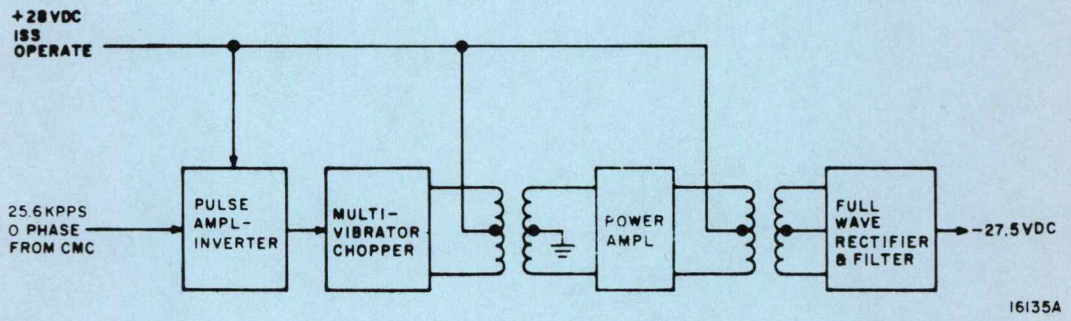


Figure 7-6. -28 VDC Power Supply

7.5.3 ISS 800 CPS POWER SUPPLY. The 800 cps power supply (figure 7-7) consists of four modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and two 5 percent amplifiers. The 1 percent amplifier provides IMU gimbal resolver excitation, gimbal servo amplifier demodulator reference, and FDAI and autopilot reference. The two 5 percent amplifiers provide gyro wheel excitation, IMU blower excitation, and accelerometer fixed heater power. The 1 percent amplifier also provides the input to one of the 5 percent amplifiers whose output is phase shifted -90 degrees. The output of this 5 percent amplifier is applied to the second 5 percent amplifier whose output is also phase shifted -90 degrees, or -180 degrees from the output of the 1 percent amplifier. The outputs of the 1 percent amplifier and the 5 percent amplifiers are applied to their respective loads through the IMU load compensation network which provides a power factor correction.

Zero and pi phase, 800 cps pulse trains from the CMC synchronize the multivibrator at 800 cps. In the absence of the synchronizing pulses, the multivibrator will free run between 720 and 790 cps. The output of the multivibrator controls the operation of the chopper and filter circuit. The filtered chopper output is applied to the 1 percent amplifier. The output of the 1 percent amplifier, in addition to its direct uses, is a feedback signal to the automatic amplitude control circuit. The positive peaks of this feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the multivibrator driven chopper. The bias controls the amplitude of the chopped signal.

The 1 percent amplifier is push-pull in operation with transformer coupled input and output and with overall voltage feedback for gain and distortion control.

The two 5 percent amplifiers are identical in operation. The amplifiers are push-pull in operation and have transformer coupled inputs and outputs. The input transformer primary center tap is connected to the input signal low. The input signal high is applied directly to one side of the primary winding and is also applied through a phase shift network to the other, or out of phase, side of the primary. A feedback signal from the secondary of the output transformer is also applied to the out of phase side of the input transformer primary where it is mixed with the phase shifted portion of the input signal. This mixing results in a -90 degree phase shift in the secondary of the input transformer. The output of the first 5 percent amplifier is used as an input to the second 5 percent amplifier to provide an additional -90 degree phase shift.

7.5.4 OSS 800 CPS POWER SUPPLY. The OSS 800 cps power supply consists of three modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and a 5 percent amplifier. The 1 percent amplifier provides resolver and tachometer excitation and the input to the 5 percent amplifier. The 5 percent amplifier provides SXT and SCT motor excitation. The outputs of the 1 percent amplifier and 5 percent amplifier are applied to their respective loads through the optics load compensation network which provides power factor correction.

The operation of the OSS 800 cps power supply is identical to the operation of the ISS 800 cps power supply except that it does not have two 5 percent amplifiers.

7.5.5 3,200 CPS POWER SUPPLY. The 3,200 cps power supply provides excitation voltage for the signal generator and the magnetic suspension portions of the IRIG and PIP ducosyns. The 3,200 cps output is also used as a reference for the demodulator in the gimbal servo amplifiers.

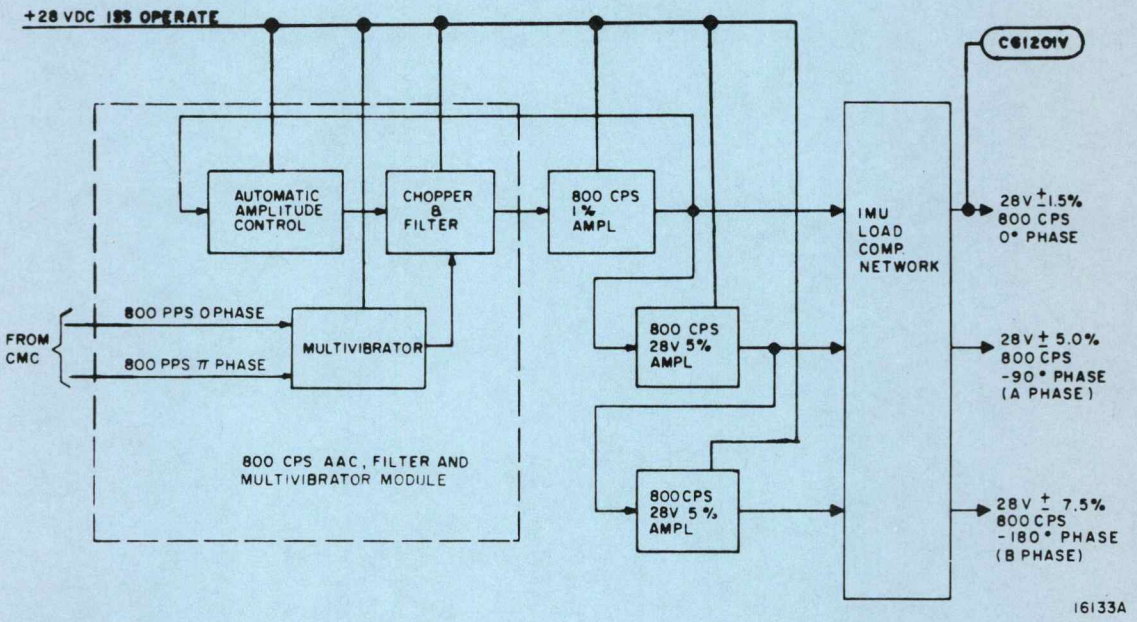


Figure 7-7. 800 CPS Power Supply

The excitation voltage to the signal generators requires both voltage stability and phase stability. To accomplish this stability, the excitation voltage power transmission to the stable member is through a step down transformer on the stable member which reduces the slip ring current and, therefore, voltage drop effects due to slip ring, cable, and connector resistance. In addition, each wire connecting the output of the transformer to the input terminals of each PIP is cut to exactly the same length. The voltage level at the primary of the transformer is fed back to the power supply and is compared to a voltage and phase reference.

The 3,200 cps power supply (figure 7-8) consists of an amplitude control module and a 1 percent power amplifier. The amplitude control module contains an automatic amplitude control circuit, a multivibrator, a chopper, and a filter.

The 3,200 pps pulse trains of zero degree phase and 180 degree phase synchronize a multivibrator. The output of the multivibrator controls the operation of the chopper circuit. The output of the chopper is applied to the 1 percent power amplifier. The 28 v (rms) output of the amplifier is transmitted through the slip rings to the transformer on the stable member where the voltage is stepped down to 2 volts for the accelerometer ducosyns and 4 volts for the gyro ducosyns. A sample of the 28 volt level at the primary of the transformer is fed back through the slip rings to the input of the automatic amplitude control circuit. The positive peaks of the feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the chopper circuit. The dc bias controls the amplitude of the chopper output to the filter.

7.5.6 4 VDC POWER SUPPLY. The 4 vdc power supply (figure 7-9) supplies 4 vdc logic power to the digital logic circuits of the CDU. The 4 vdc power supply is a dc to dc converter type consisting of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, a rectifier and filter circuit, and a difference amplifier and series regulator circuit.

A 25.6 kpps synchronization pulse input is amplified and inverted and used to synchronize the multivibrator-chopper, whose natural frequency is 11.5 kcps. The multivibrator-chopper drives the primary of a transformer which has 28 vdc applied to its center tap. The secondary of the transformer is also center tapped and is coupled to a push-pull power amplifier. The dc input to the power amplifier is supplied through a series regulator. The power amplifier drives the primary of a transformer to develop a 12.8 kcps square wave. The output from the transformer secondary is applied to the rectifier and filter circuit where the 4 vdc output is developed.

The 4 vdc output is fed back to a difference amplifier that produces an output error signal proportional to the difference between the 4 vdc output and a reference voltage level obtained from a zener diode and resistor voltage divider network. The output of the difference amplifier controls the operation of the series regulator to increase or decrease the level of the dc input to the power amplifier as necessary to maintain the power supply output at 4 volts.

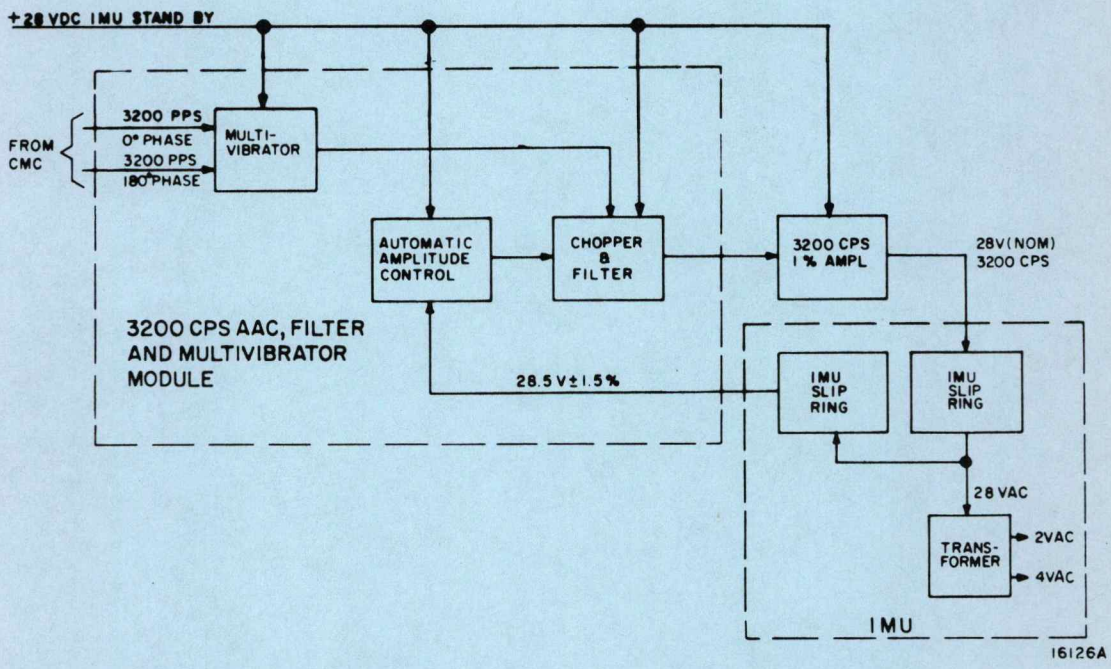


Figure 7-8. 3200 CPS Power Supply

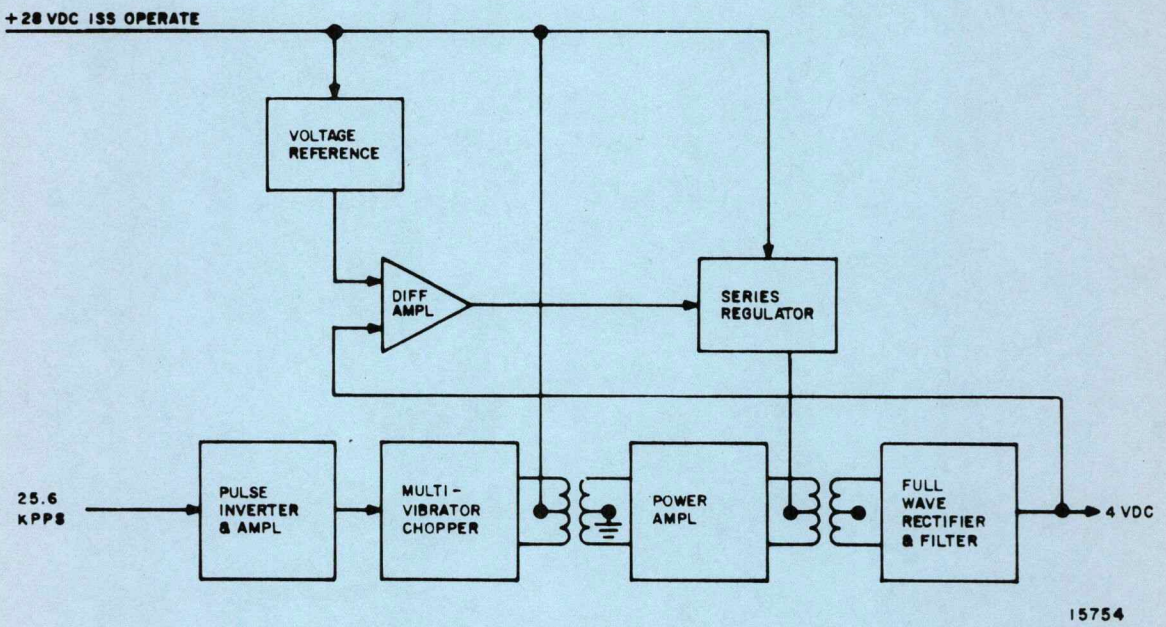


Figure 7-9. 4 VDC Power Supply

SECTION VIII

SIGNAL MONITORING AND DETECTION AND SIGNAL CONDITIONING

INTRODUCTION

The Apollo Primary Guidance and Navigation Control System (PGNCS) airborne instrumentation equipment consists of the Signal Conditioner Assembly (SCA). Since the SCA outputs interface with the Pulse Code Modulator (PCM) which is not part of the PGNCS a description of the PCM operation will be included in this section.

The signal conditioner assembly located in the lower equipment bay receives PGNCS signals and converts them to a form acceptable to the airborne PCM. The PCM then transforms the conditioned signals into a form suitable for telemetry transmitter modulation. The signal conditioner assembly also provides isolation between the component or circuit being monitored and the telemetry system.

8.1 SIGNAL CONDITIONER ASSEMBLY (SCA)

The signal conditioner assembly is located in the upper right corner of the lower equipment bay and contains four modules which condition the various signals monitored in the PGNCS. See figure 8-1.

8.1.1 SIGNAL CONDITIONER ASSEMBLY FUNCTIONS. The signal conditioner assembly performs the following functions:

a. Proper scaling of DC inputs.

b. Conversion of AC signals to representative DC levels whose polarity reflects the phase of the AC input.

c. Conversion of resistor sensor values representing temperature to a DC voltage level.

d. Providing 2.5V bias power to the signal conditioner modules.

Figure 8-2 shows the above conversion as performed by the SCA modules.

8.1.2 BLOCK II SIGNAL CONDITIONER ASSEMBLY. The Block II signal conditioner assembly is made up of the following four modules: (Figure 8-1)

a. DAC, PIPA Temp and 2.5V Bias Module P/N 2010124

b. PIPA and IRIG Module P/N 2010122

c. Gimbal Resolver Module P/N 2010120

d. 120V PIPA Supply Module P/N 2010128

Each module, as the name implies, has been designed to condition particular PGNCS signals for telemetering.

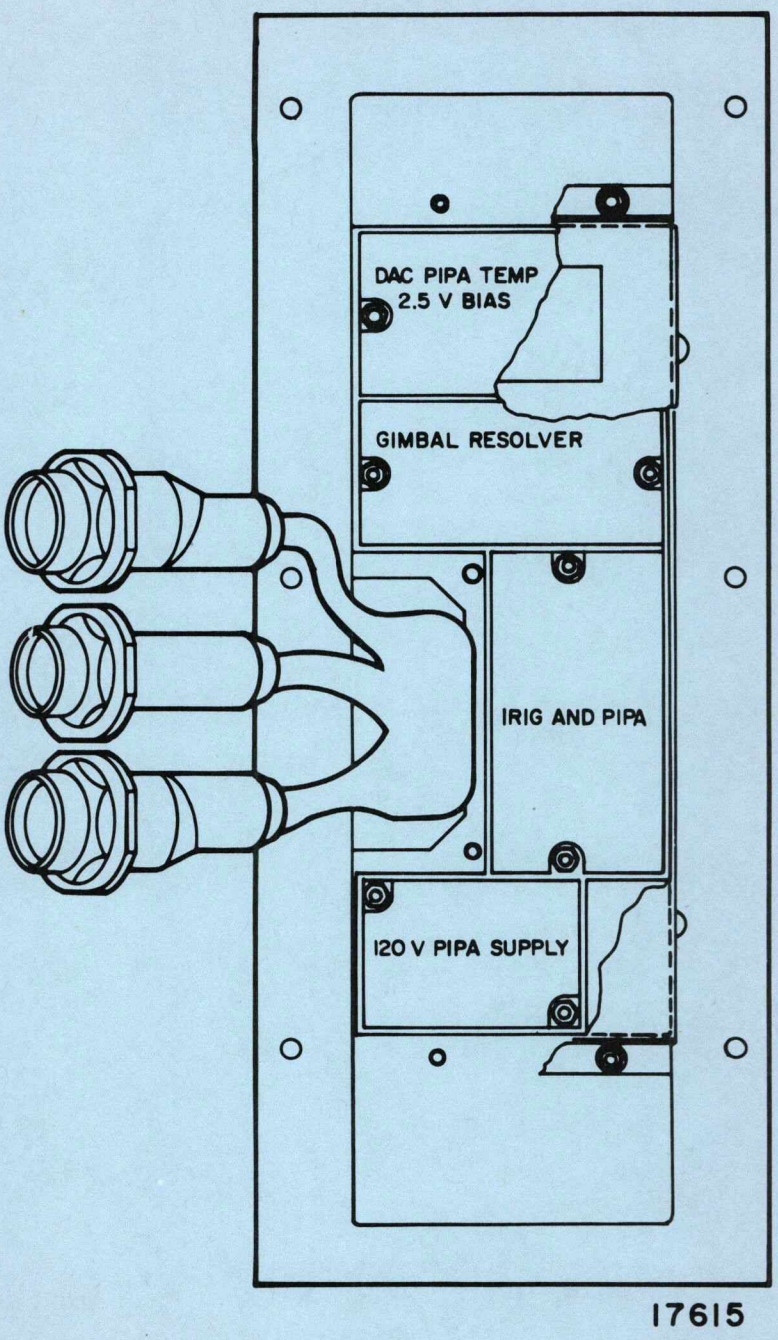


Figure 8-1. SCA Layout

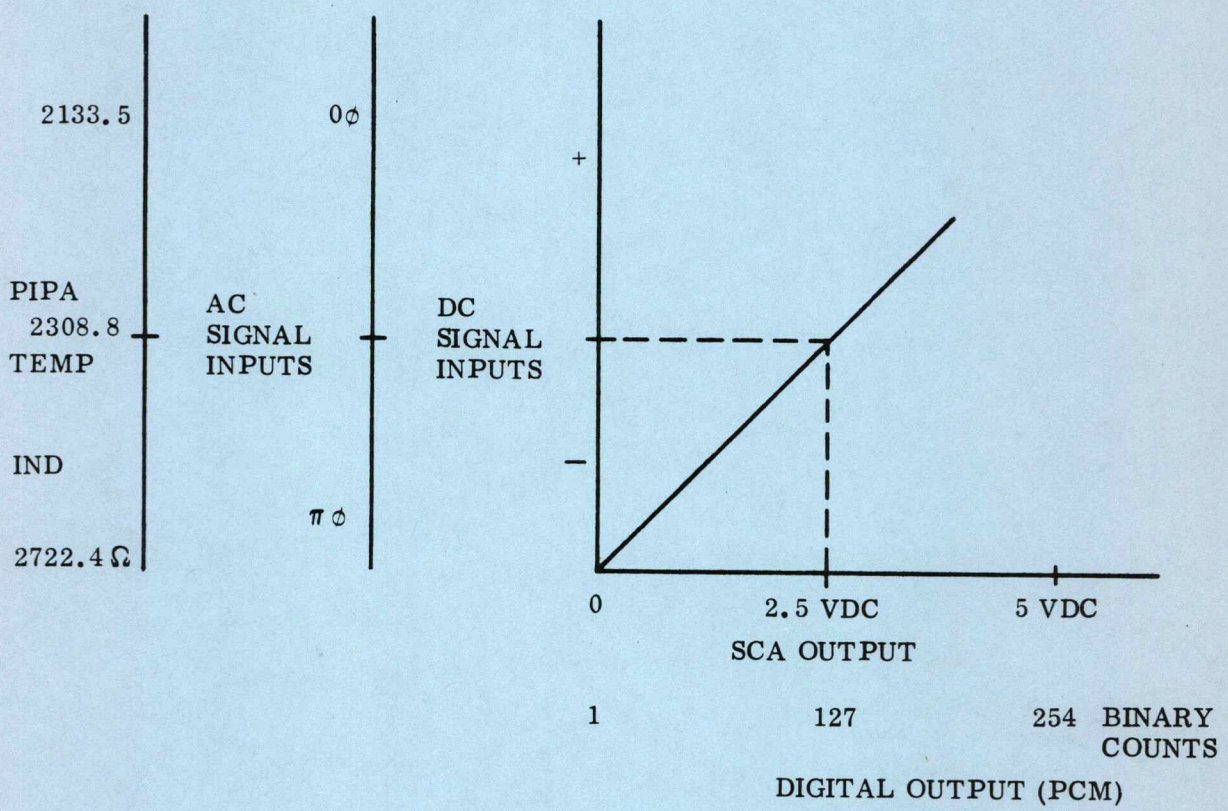


Figure 8-2. Signal Conditioner Assembly Conversions

8.1.2.1 DAC, PIPA Temp and 2.5V Bias Module. The DAC, PIPA Temp and 2.5V Bias module performs the following functions.

Monitors and conditions the 28V ISS standby discrete, the 28V CMC operate discrete, the CMC warning discrete, and the optics power on event.

Monitors and conditions the optics shaft and trunnion digital to analog conversion in the CDU.

Generates the 2.5V telemetry bias voltage.

Monitors and conditions the PIPA temperature.

To perform the above functions this module contains three scaling circuits for conditioning the discrete inputs, two amplifier-demodulating circuits for conditioning the DAC outputs, one power supply circuit and one PIPA temperature amplifier for conditioning the PIPA temperature signal. See figure 8-3. The following paragraphs describe these circuits:

a. The DAC, PIPA Temp and 25V Bias Module contain three scaling circuits that condition discrete dc signals which require attenuation from the normal 0 to 28 vdc level to the 0 to 5 vdc level. To insure isolation between the circuit being monitored and the signal conditioner the incoming dc signal is first applied to a chopper circuit. The chopper modulates an 800 cps square wave with the dc input. The modulated square wave, which is representative of the magnitude and polarity of the dc input is transformer-coupled to a phase sensitive demodulator circuit consisting of two dual emitter/switch transistors.

The switching action of the transistor pairs in both the chopper circuit and the demodulator circuit is controlled by a switch drive circuit consisting of an 800 cps reference signal applied through a transformer to the basecollector junction of each transistor. The switch drive circuit alternately turns on one transistor while the other one is turned off. The output of the demodulator is a pulsating dc signal whose magnitude will be 5 vdc when the discrete is issued. The output of the demodulator is filtered to provide a steady state dc signal output to the PCM.

b. The DAC, PIPA Temp and 2.5V Bias Module contains phase sensitive demodulator circuitry for conditioning the optics trunnion and shaft digital to analog converter outputs. These AC signals are transformer coupled in the signal conditioner for isolation, amplified and demodulated to the 0 to 5 vdc signal level appropriate for the PCM. The demodulation is performed in the same manner as it is in the scaling circuits.

A 2.5 volt dc bias high is connected to the signal low of each module and becomes the reference point for the 0 to 5 volt signal outputs of the signal conditioner modules. In this manner a zero phase ac signal, after conditioning, may be represented as a dc voltage value above the 2.5 volt reference. A pi phase signal, after conditioning, may be represented as a dc voltage value below the 2.5 volt reference. Bipolar dc signals from the PGNCS which may be positive or negative have a zero volt reference, may, after conditioning, be represented in a similar manner.

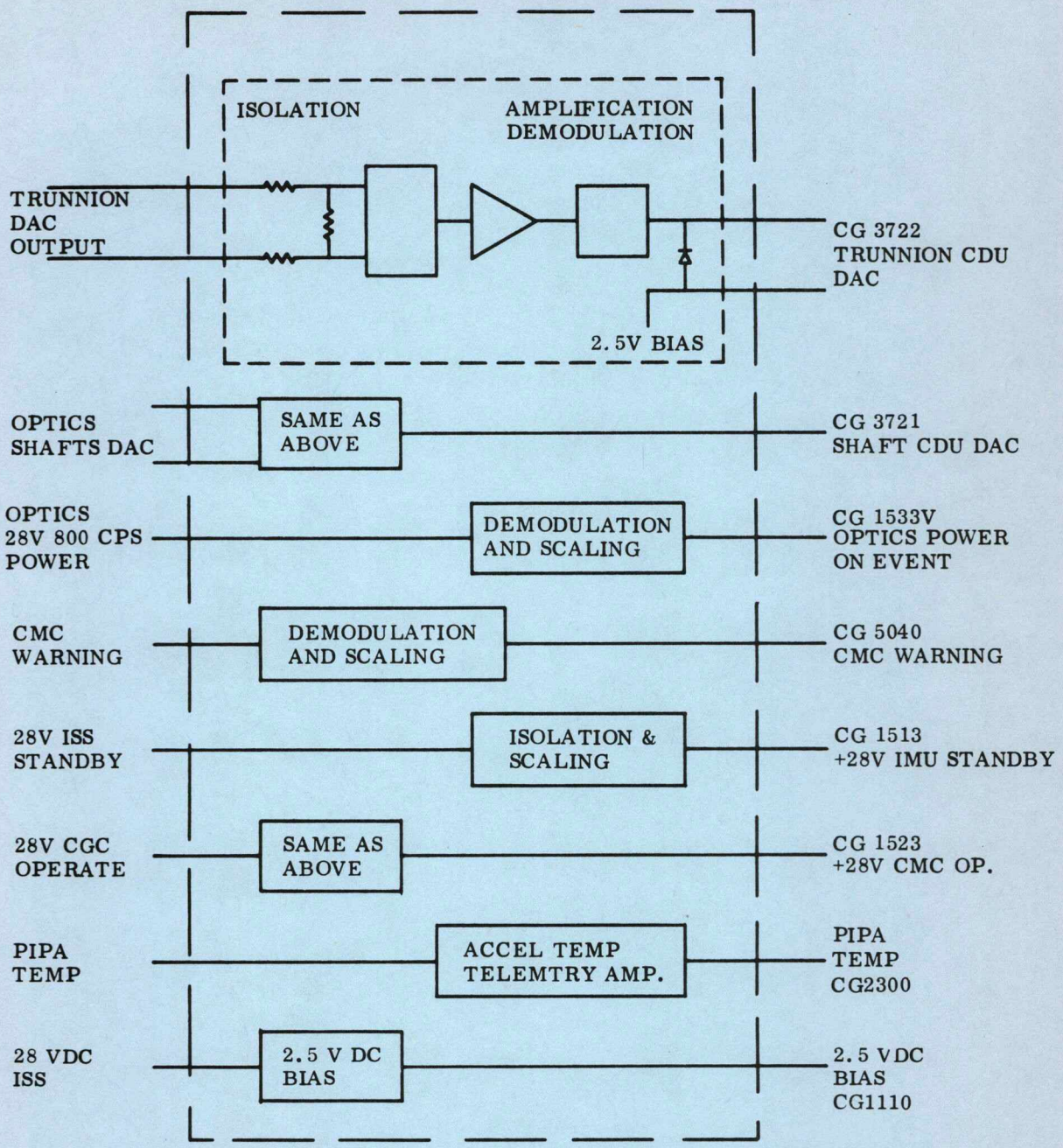


Figure 8-3. DAC, PIPA Temp & 2.5V DC Bias Module

c. The temperature of the Pulse Integrating Pendulous Accelerometers (PIPA) is monitored by the DAC, PIPA Temp and 2.5V Bias Module in the SCA. The sensors, resistors whose resistance increase with an increase in temperature, are located in the PIPA housing and form one branch of a bridge circuit located in the accelerometer temperature telemetry amplifier. Two legs of the bridge circuit are windings of a high gain magnetic amplifier. The output of the magnetic amplifier is filtered and biased at 2.5 vdc. This output will be 2.5 vdc when the PIPA is at the proper temperature for operation, 135^{o}, and the sensor resistance for this temperature will be 2308.8 Ω. As the PIPA temperature increases or decreases, the sensor resistance will increase or decrease resulting in a proportional increase or decrease of signal conditioner module output.

d. The 2.5 vdc required in the signal conditioner for biasing the conditioned signal outputs is generated in the DAC, PIPA temp and 2.5V bias module. This 2.5V dc bias voltage is connected in series with the outputs of the modules requiring the 2.5V bias for proper conditioning of the various signals. The bias high is connected to the signal low of each module to provide the reference point for the 0 to 5 vdc outputs of the SCA module outputs thus providing the capability of monitoring zero and π phase signals.

8.1.2.2 PIPA and IRIG Module. The PIPA and IRIG module in the signal conditioner assembly perform the following functions:

a. Monitors and conditions the X, Y and Z PIPA signal generators output.

b. Monitors and conditions the inner, middle and outer gimbal servo error.

c. Monitors and conditions the 3200 cps discrete excitation power used in the SCA.

To perform the above functions this module contains six amplifier-demodulating circuits for conditioning the PIPA signal generator outputs and the inner, middle and outer gimbal servo error, demodulation circuit for conditioning the 3.2 KC signal. See figure 8-4.

8.1.2.3 Gimbal Resolver Module. The gimbal resolver module in the signal conditioner assembly conditions the sin and cosine outputs of the inner, middle and outer gimbal resolvers. To perform this function the gimbal resolver module contains six phase and amplitude sensitive amplifier-demodulator circuits. Figure 8-5.

8.1.2.4 120V PIPA Supply Module. This module in the SCA conditions the 120V PIPA power supply by dividing it down to 12.3 vdc. This 12.3 volts is then compared to a reference voltage developed across two zener diodes and the result of the comparison is fed into a chopper, or A/C amplifier and a demodulator. The demodulator output is filtered and biased at 2.5 vdc so that the input to the PCM will vary about the bias level proportionately to the changes of the 120 vdc power supply input to the module.

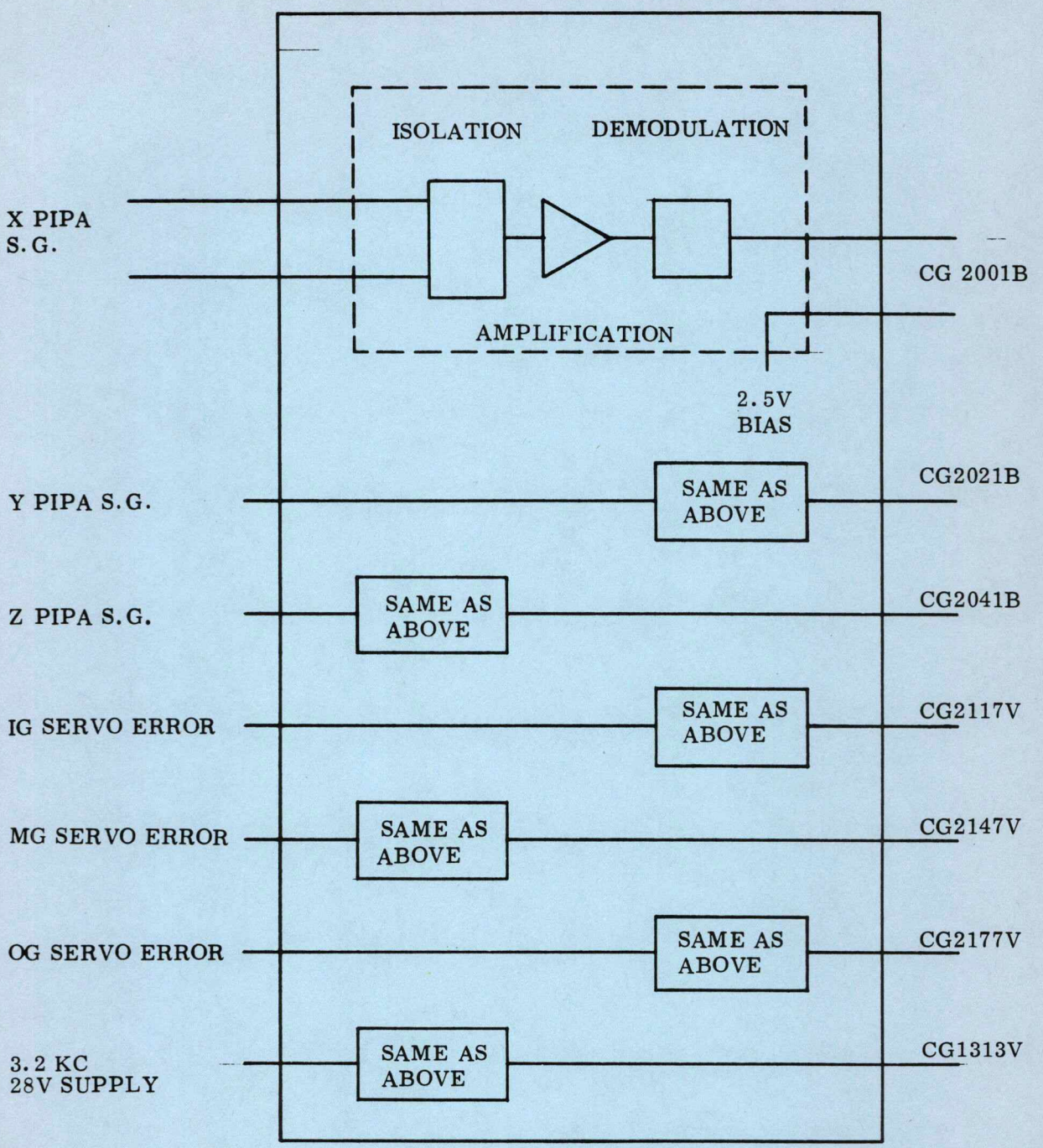


Figure 8-4. PIPA & IRIG Module

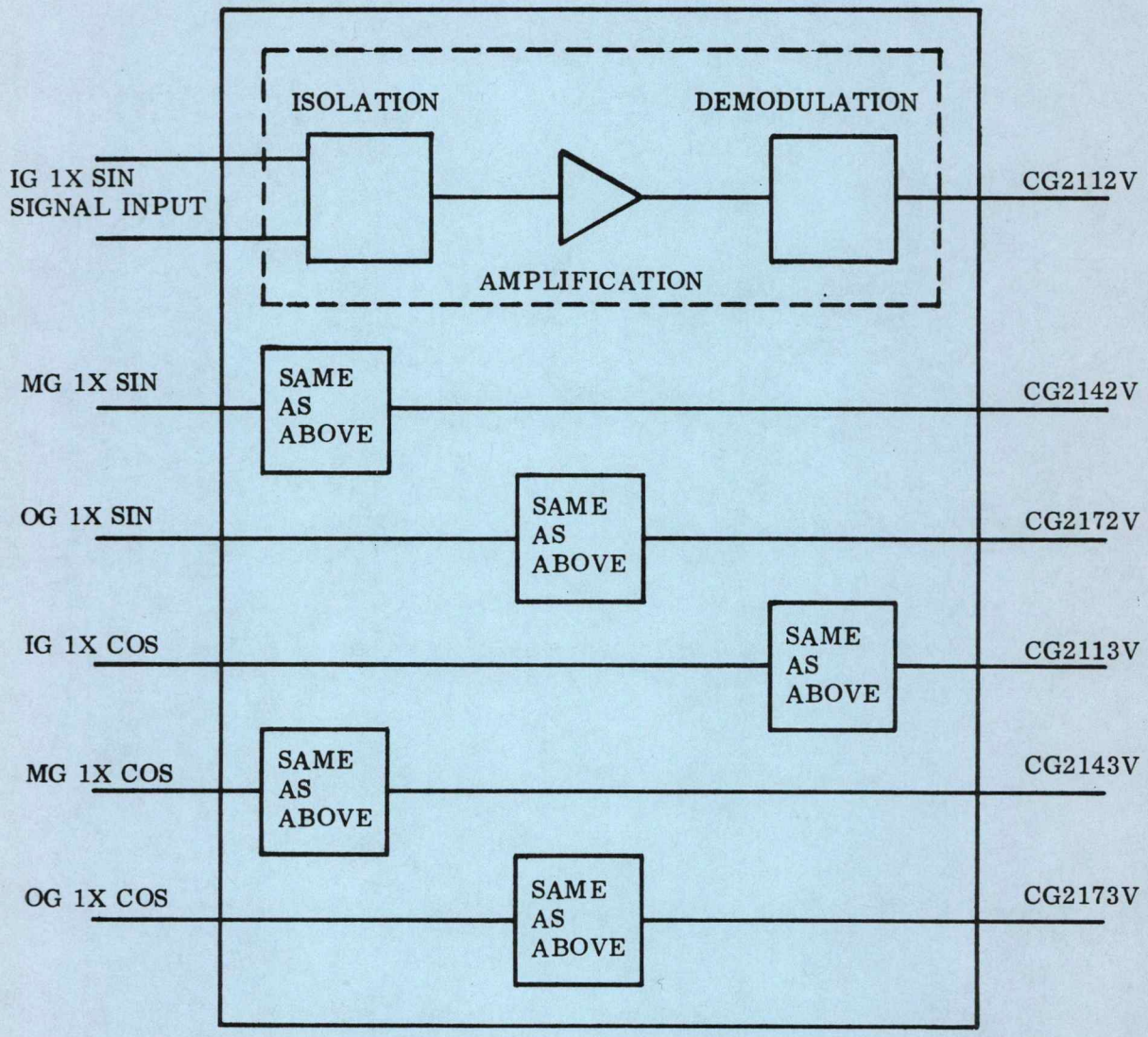


Figure 8-5. Gimbal Resolver Module

8.2 PULSE CODE MODULATOR

The Pulse Code Modulation (PCM) Telemetry Equipment receives and converts data inputs from various sampling points throughout the Spacecraft into a single serial digital output.

Signals entering the PCM Telemetry System for processing are of four general types; low-level analog, high-level analog, parallel digital, and serial digital.

The PGNCS signal conditioner assembly provides high level analog inputs to the PCM and the PGNCS computer supplies serial digital input to the PCM.

Each analog and digital input to the PCM Telemetry Equipment is assigned to a channel. These inputs, or channels, will be combined to provide a serial digital output at one of two rates as determined by the mode of the equipment. The high bit rate mode has an output of 51,200 bits per second, and the low bit rate mode has an output of 1600 bits per second.

A fixed program is provided for sampling each channel and the rate at which it is sampled for each bit rate mode.

Figure 8-6 is a block diagram with representative signals showing the flow of analog information in the PCM.

8.2.1 PCM FORMATS. A detailed analysis of the Normal and Reduced PCM Formats is contained in the subsequent paragraphs.

a. PCM Normal Format - The breakdown of the PCM Normal Format is shown in figure 8-7. The smallest increment of the format is called a bit. This bit has two valves, "1" and "0". A logic "1" is represented by +6.0 ±.5 volts and a logic "0" is represented by 0 + .5, _.0 volts. The bit has a duration of 19.53125 microseconds.

The next higher unit in the Normal Format is the word. It contains 8 bits and, therefore, has a duration of 156.25 microseconds.

The prime frame is the next to largest increment in the normal format. It contains 128 words and, therefore, has a duration of 20 milliseconds.

The largest increment of the normal format is the subframe. It has a duration of 1 second. The subframe contains 50 prime frames, 6400 words, or 51,200 bits.

b. PCM Reduced Format - The breakdown of the PCM reduced format is shown in figure 8-8. As in the normal format, the smallest increment is called a bit. This binary bit is identical to the bit in the normal format except in duration. The reduced format bit is 625 microseconds in duration as opposed to the 19.53125 microsecond duration of the normal format bit.

The next higher increment in the reduced format is the word which contains 8 bits. Its duration is 5 milliseconds.

The prime frame is the largest increment in the reduced format. Its duration is one second, thus making it contain 1600 bits or 200 words.

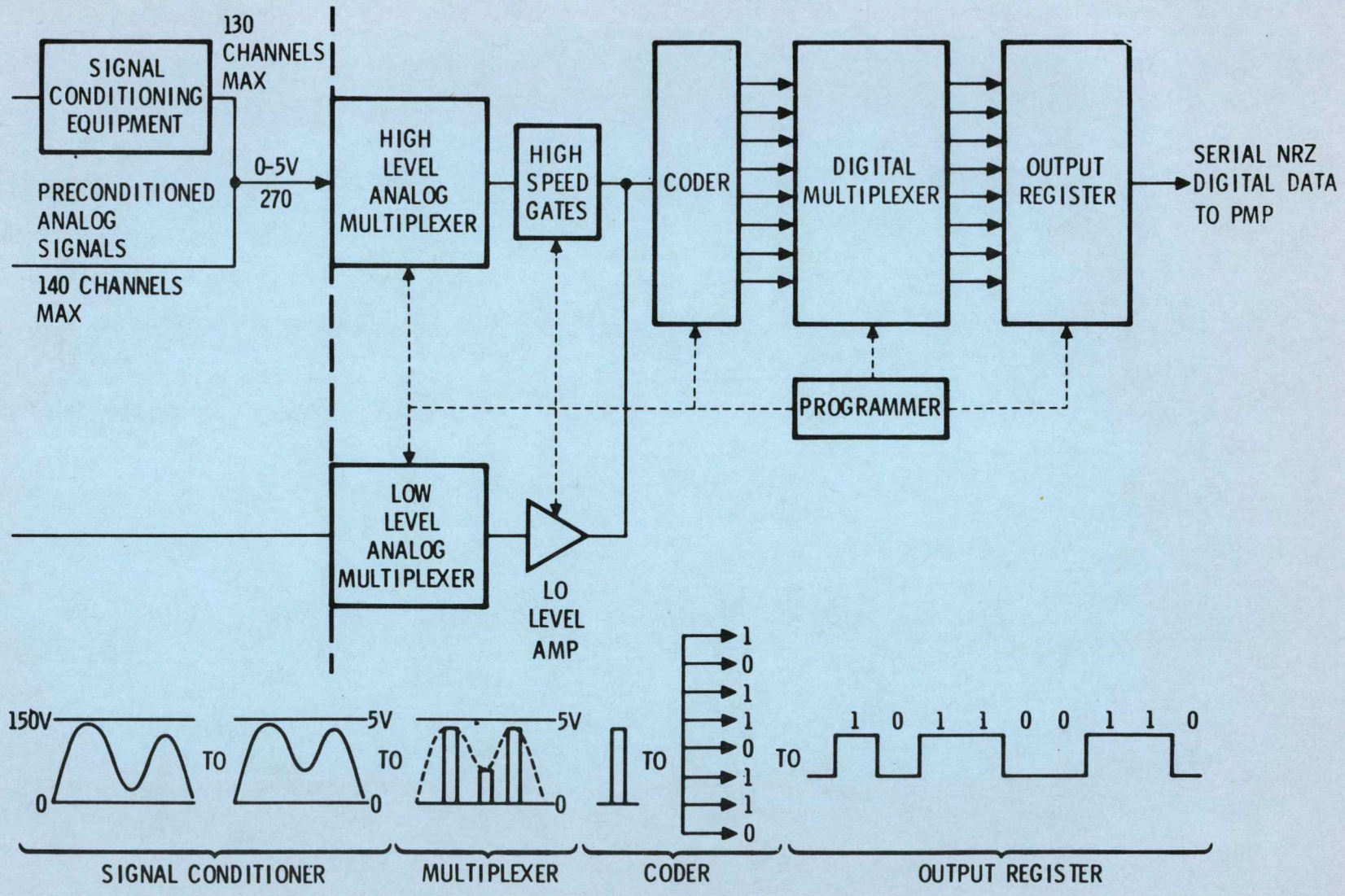


Figure 8-6. PCM Analog Data Flow

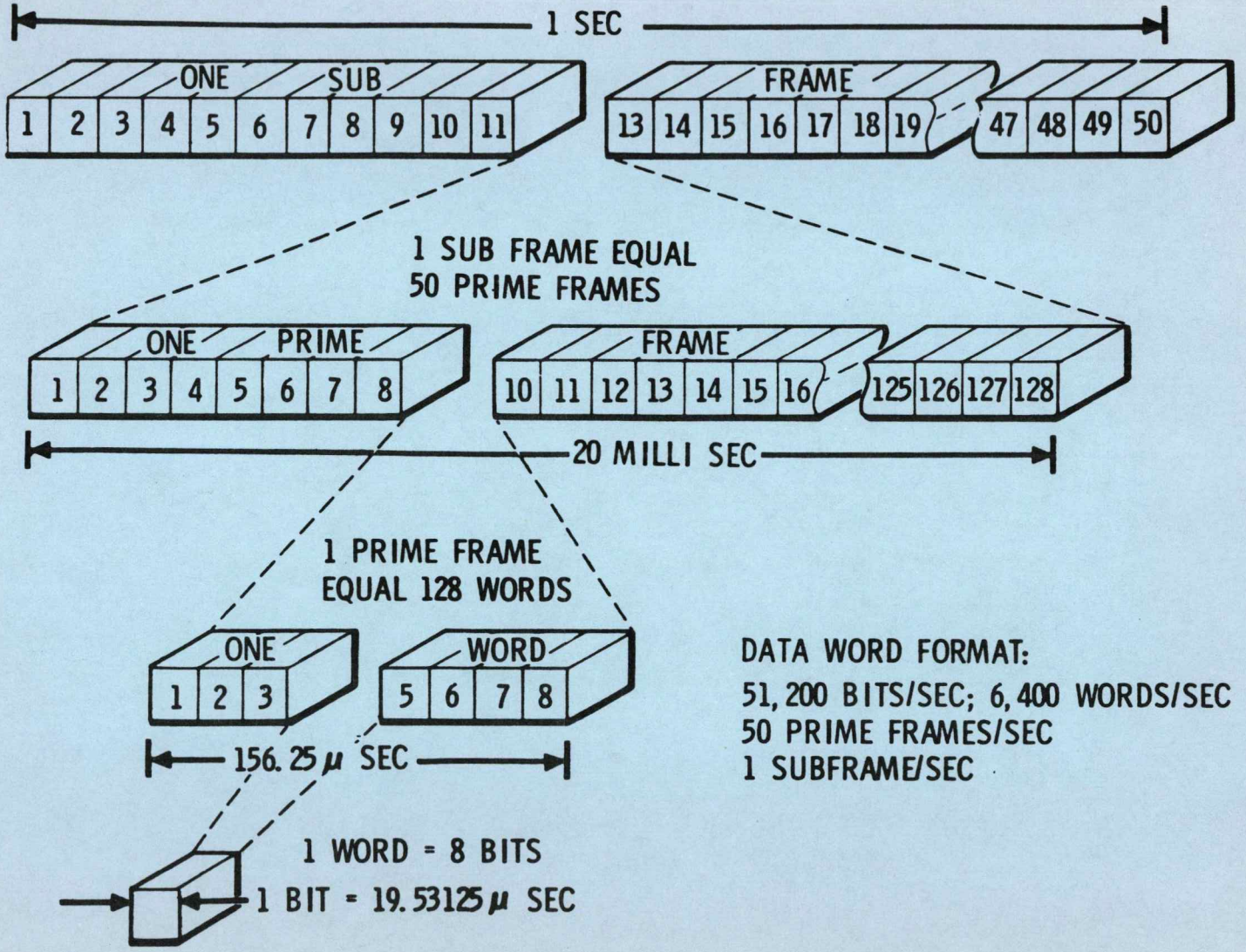


Figure 8-7. PCM Normal Format

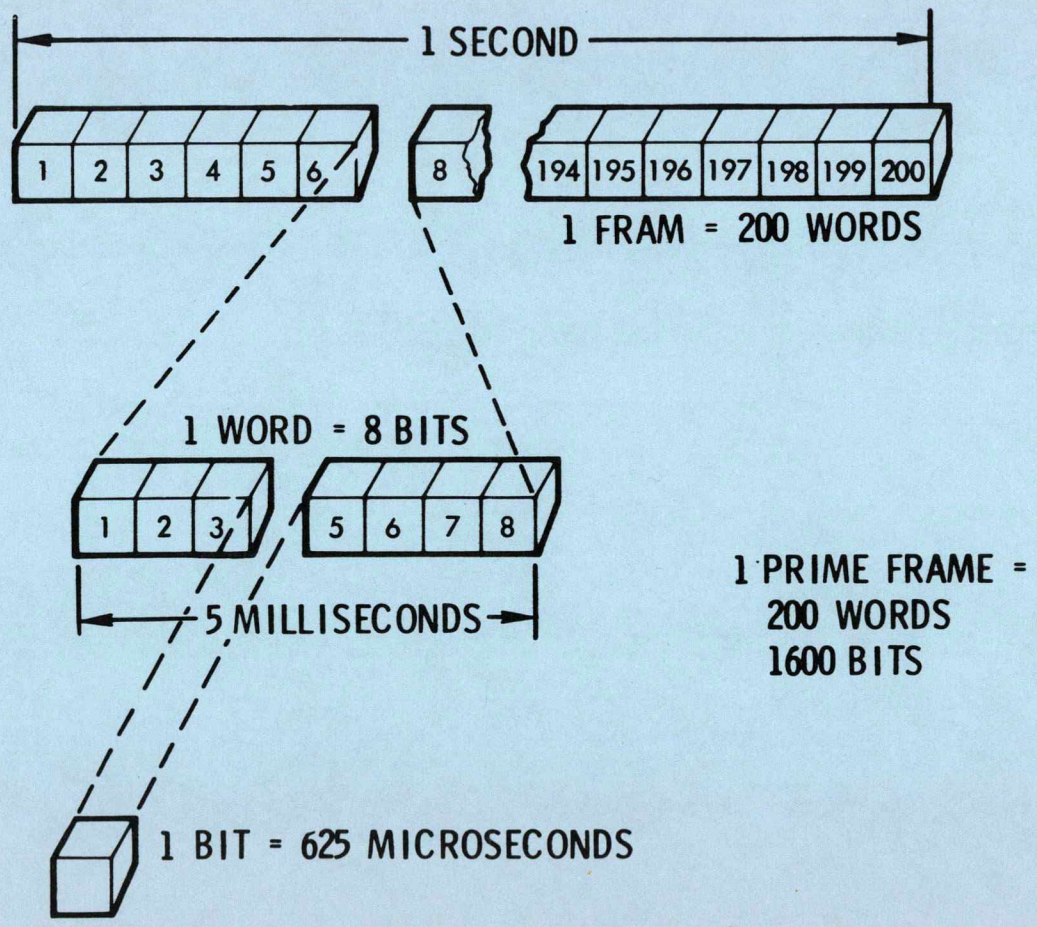


Figure 8-8. Reduced Format

8.2.2 PCM TO PGNCS COMPUTER INTERFACE. The overall synchronization of the telemetry is controlled by the PCM programmer. The telemetry system when transmitting in the normal PCM Format transmits data to the grount at the rate of 50 frames per sec. A frame consists of 128 eight bit telemetry words, five of which are alloted for CMC data. Thus every 20 msec 40 bits of CMC data is sent out, or 50, 40 bit CMC words are sent out each second.

When operating in reduced PCM format 200 eight bit words are transmitted each second. Fifty of these 200 eight bit words are alloted to the CMC data. Therefore when in reduced format the CMC 40 bit words are transmitted 10 times per sec.

To control the transfer of 40 bit data words from the CMC to the PCM, the PCM programmer issues three signals to the CMC.

	Normal	Reduced
BIT RATE	51.2 KC	1.6 KC
TL START Pulse	50 PPS	10 PPS
TL END Pulse	50 PPS	10 PPS

The TL START pulse is handwired into the CMC and releases the 40 bits of the down telemetry CMC format previously loaded into channels 34 and 35. During this transfer of information a counter in the computer (51.2 or 1.6 KC) insures that the information transfer occurs at the proper rate. If the rate of information transfer is too fast a "downlink too fast" discrete is issued to the computer program via input channel 33 bit location 12.

When the 40 bits of the down telemetry CMC format has been transferred to the PCM TL END is issued by the PCM programmer. TL END is handwired into the CMC Program Interrupt Service. This forces a down rupt routine which reloads the next two 16 bit computer word in to the down telemetry format (ch 34 and ch 35) for transfer to the PCM when the next TL START is issued.

8.3 A/B PGNCS MEASUREMENT LIST

The PGNCS signals to be telemetered to the ground stations during flight are listed in table 8-1. These signals will provide sufficient data to thoroughly evaluate the PGNCS performance, consistent with program requirements and the capacity of the telemetry system. The list in table 8-1 also indicates the sampling rate during normal PCM format, and refers to figures in other sections of the book where additional information on the particular signal may be found.

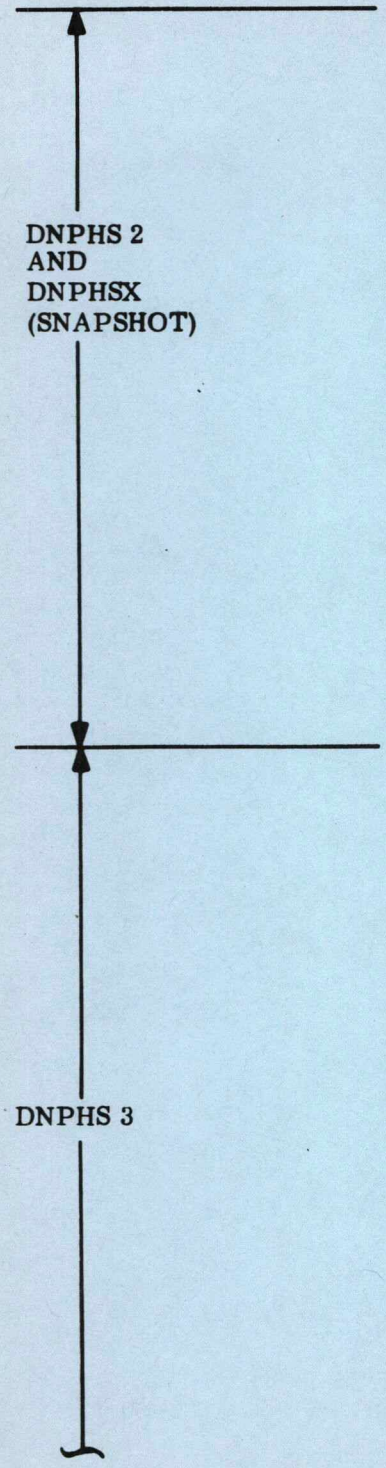
8.3.1 The following paragraphs will contain descriptions of the various signals listed in table 8-1

CG 0001 CMC DIGITAL DATA

40 bits of computer information transmitted 1 per prime frame or 50 times per sec during normal PCM format. Also transmitted 10 times per sec during reduced PCM format. Figure 8-9 is a listing of the information to be sent sequentially from the computer to the PCM in 40 bit increments each time that CG 0001 is gated in the PCM format.

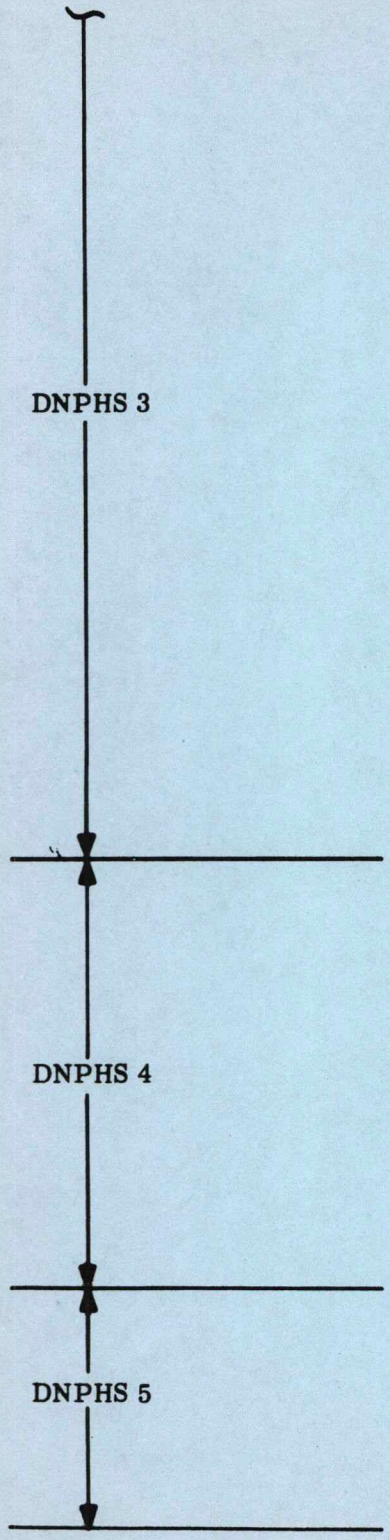
Measurement No.	Measurement Description	Data Limits	S/S	Reference Figures
CG 0001	CMC DIGITAL DATA (40 BIT)		50	8-9
CG 1040 V	120 VDC PIPA SUPPLY DC LEVEL	85 - 135	1	
CG 1110 V	2.5 VDC TM BIAS		1	
CG 1201 V	IMU 28V .8 KC 1% 0 DEG, RMS	0 - 31.1	1	7-7
CG 1331 V	3.2 KC 28V SUPPLY	0 - 31.1	1	
CG 1513 X	+28V IMU STANDBY		10	7-1
CG 1523 X	+28V CMC OPERATE		10	7-3
CG 1533 X	+28V OPTX OPERATE		10	7-4
CG 2001 B	X PIPA SG OUTPUT IN PHASE		50	
CG 2021 B	Y PIPA SG OUTPUT IN PHASE		50	
CG 2041 B	Z PIPA SG OUTPUT IN PHASE		50	
CG 2112 V	IG 1X RESOLVER OUTPUT SIN	-21.5 +21.5	10	
CG 2113 V	IG 1X RESOLVER OUTPUT COS	-21.5 +21.5	10	
CG 2117 V	IG SERVO ERROR IN PHASE		100	
CG 2142 V	MG 1X RESOLVER OUTPUT SIN	-21.5 +21.5	10	
CG 2143 V	MG 1X RESOLVER OUTPUT COS	-21.5 +21.5	10	
CG 2147 V	MG SERVO ERROR IN PHASE		100	
CG 2172 V	OG 1X RESOLVER OUTPUT SIN	-21.5 +21.5	10	
CG 2173 V	OG 1X RESOLVER OUTPUT COS	-21.5 +21.5	10	
CG 2177 V	OG SERVO ERROR IN PHASE		100	
CG 2300 T	PIPA TEMP		1	
CG 3721 V	SHAFT CDU DAC OUTPUT		10	
CG 3722 V	TRUNNION C DU DAC OUTPUT		10	
CG 5040 X	CMC WARNING		10	

Table 8-1. PGNCS A/B Telemetry Measurement List



	(A) CHANNEL 34	(L) CHANNEL 35
1	00000 (LIST ADDRESS)	00437_8
2	PIPA X	PIPA Y
3	PIPA Z	BMAG X
4	BMAG Y	BMAG Z
5	PUSHLOC	PRIORITY
6	LOC	BANKSET
7	DELVX	DELVX+1
8	DELVX+2	DELVX+3
9	DELVX +4	DELVX+5
10	SELFRET	SMODE
11	SFAIL	ERCOUNT
12	IMODES 30	IMODES 33
13	DESOPTT	DESOPTS
14	CDU X	CDU Y
15	CDU Z	CDU T
16	CDU T	CDU S
17	STATE	STATE+1
18	STATE+2	STATE+3
19	REDOCTR	FAILREG
20	OPTMODES	SWSAMPLE
21	DESOPMOD	WTOPTION
22	IMUCADR	OPTCADR
23	THETAD	THETAD+1
24	THETAD+2	DESOPTT
25	MARKSTAT	TIMESAV

Figure 8-9. CG 0001 Listing



	(A) CHANNEL 34	(L) CHANNEL 35
26	DRIFT O	DRIFT O+1
27	DRIFT I	DRIFT I+1
28	DRIFT T	DRIFT T+1
29	GAZIMUTH	GAZIMUTH+1
30	ANG Z	ANG Z+1
31	ANG Y	ANG Y+1
32	ANG X	ANG X+1
33	VLAUN	VLAUN+1
34	WPLATO	WPLATO+1
35	WPLATI	WPLATI+1
36	WPLATT	WPLATT+1
37	INTVEC	INTVEC+1
38	INTVEC+2	INTVEC+3
39	UPLOCK	T6LOC
40	DSPTAB	DSPTAB+1
41	DSPTAB+2	DSPTAB+3
42	DSPTAB+4	DSPTAB+5
43	DSPTAB+6	DSPTAB+7
44	DSPTAB+8D	DSPTAB+9D
45	DSPTAB+10D	DSPTAB+11D
46	TIME 2	TIME 1
47	c(CHAN 11)	c(CHAN 12)
48	c(CHAN 13)	c(CHAN 14)
49	c(CHAN 30)	c(CHAN 31)
50	c(CHAN 32)	c(CHAN 33)

Figure 8-9. CG 0001 Listing

CG 1040V 120 VDC PIPA SUPPLY DC LEVEL

Source of this data is the binary current switch of the pulse torquing assembly of the ISS. The 120 vdc level is conditioned in the signal conditioner assembly, 120 vdc PIPA supply module and is sampled once per second in the normal PCM format.

CG 1110V 2.5 VDC TM BIAS

This signal is a measurement of the 2.5V power supply located in the signal conditioner assembly. The power supply converts an input from the IMU 28V 800 cps 1% 0^{o} power supply, by half wave rectification and zener reference, to a 2.5 vdc output. This output is applied to the outputs of all modules within ghe signal conditioner except the scaling circuits. The signal is sampled 1 per second during normal PCM format.

CG 1201V IMU 28V .8 KC 1% 0 DEG RMS

This signal is a measurement of the IMU 28V 800 ~ 1% 0 deg rms power supply located in the PSA. This supply provides the IMU resolver excitation, stab amplifier demodulation reference, CDU reference, signal conditioner references, and is also used as an input to the 5% amplifier. The samplign rate for this signal si 1 per second during normal PCM format.

CG 1331V 3.2 KC 28V SUPPLY

This signal is a measurement of the 3.2 KC 28V 1% power supply located in the PSA. This power supply provides the IMU with 28 volt power which is then reduced through a transformer to 2 volts and 4 volts for signal ducosyn generator excitation and for magnetic suspension winding excitation for the torque and signal ducosyns of the IRIG's and PIPA's. The sampling rate for this signal is 1 per second during normal PCM format.

CG 1513X +28V IMU STANDBY

This signal is a discrete output of the signal conditioner to the PCM. It is an indication of when standby power has been applied to the IMU by the closure of circuit breaker 58 and/or 59 on panel 5 of the main display and control panel. The discrete output will be a one level (5 vdc) when the IMU standby switch is on and zero level (0 vdc) when IMU standby switch is not on. The sampling rate for this signal is 10 per second during normal PCM format.

CG 1523X +28V CMC OPERATE

This signal is a discrete output of the signal conditioner to the PCM. It is an indication of when computer operate power has been applied to the computer by closure of circuit breaker 60 and/or 61 on panel 5 of the main display and control panel. The signal output will be the same as that for CG 1513X.

CG 1523X +28V OPTX OPERATE

This signal is also a discrete output of the signal conditioner to the PCM. It is an indication of when optics operate power has been applied to the optics by closure of circuit breaker 62 and/or 63 on panel 5 of the main display and control panel and S1 (G&N Pwr Optics) on the lower equipment bay panel 99. The signal output will be the same as that for CG 1513X.

CG 2001B X PIPA S.G. OUTPUT IN PHASE

This signal is a measurement of the X PIPA signal generator in phase output. It is an indication of the operation of the IMU accelerometer loop. The signal source is the GS amplifier of the PIPA electronics assembly. Sampling rate is 50 samples per second during normal PCM format.

CG 2021B Y PIPA S.G. OUTPUT IN PHASE (SAME AS ABOVE)

CG 2041B Z PIPA S.G. OUTPUT IN PHASE (SAME AS ABOVE)

CG 2112V IG 1X RESOLVER OUTPUT SIN

This signal is a measurement of the IMU inner gimbal resolver output which represents the sin of the gimbal angle. The inner gimbal angle is determined by using the combination of measurements CG 2112V and CG2113V. First the measurements are used to determine the quadrant in which the gimbal angle θ is located. Then the sin measurement is compared with a value representing the sine 45^{o} if the measured value is less than the sine 45^{o} constant the sine will be used to determine the gimbal angle. If the measured sine value is greater than the sine 45^{o} constant the cosine measurement will be used to determine the gimbal angle. In this way the 254 PCM counts allowable for one signal can be applied to the sine for 0 to 45^{o} and another 254 counts will be applied to the cos for 45^{o} to 90^{o}. The result is a finer resolution in the determination of the gimbal angle θ. The sampling rate is 10 samples per second in the normal PCM format.

CG 2113V IG 1X RESOLVER OUTPUT COSINE

This signal is used in conjunction with CG 2112.

CG 2117V IG SERVO ERROR IN PHASE

This signal is a measurement of the gimbal servo amplifier input and therefore is an indication of the magnitude and direction of the error existing in the gimbal servo loop. It is a 3200 cps signal whose phase will determine the direction and whose amplitude will determine the magnitude of the error existing in the servo loop. The sample rate is 100 samples per second in the normal PCM format.

CG 2142V MG 1X RESOLVER OUTPUT SINE

See CG 2112V

CG 2143V MG 1X RESOLVER OUTPUT COSINE

See CG 2113V.

CG2147V MG SERVO ERROR IN PHASE

See CG 2117V.

CG 2172V OG 1X RESOLVER OUTPUT SINE

See CG 2112V.

CG 2173V OG 1X RESOLVER OUTPUT COSINE

See CG 2113V.

CG 2177V OG SERVO ERROR IN PHASE

See CG 2117V.

CG 2300T PIPA TEMPERATURE

This signal is a measurement of the temperature of the pulse integrating pendulous accelerometers of the IMU. (See Section 8.1.2.1 paragraph C.)
The sampling rate of this signal is 1 per second during normal PCM format.

CG 3721V SHAFT CDU DAC OUTPUT

This signal is a measurement of the optical system shaft, coupling data unit, digital to analog converter output. This signal is present during the course alignment of the optics subsystem and is also used to provide analog signals for positioning the service propulsion system (SPS) engine gimbals during thrust vector control (TVC). This is an 800 cps signal whose phase is indicative of direction and whose amplitude is indicative of magnitude. The sample rate of this signal is 10 samples per second.

CG 3722V TRUNNION CDU DAC OUTPUT

Same as CG 3722V.

CG 5040 CMC WARNING

This signal is a discrete indication of a CMC malfunction. During normal operation the computer issues a zero level to the signal conditioner module providing a ground for the 3200 cps excitation to the transformer. The transformer output is half wave rectified, and filtered and sent to the PCM. When a computer malfunction occurs, the CMC issues a 1 level which removes the ground to the SCA transformer and causes the output to the PCM to drop to zero. The sampling rate of this is 10 samples per second during normal PCM format. The data source is bit 14 of channel 33 of the CMC. During normal CMC operation this bit is a one level which hold in a relay in the display and keyboard assembly. This relay in turn supplies the necessary ground to the signal conditioner. CMC failure changes bit 14 of channel 33 to a zero, deenergizes the DSKY relay and removes the ground to the signal conditioner.

8.4 CAUTION AND WARNING INDICATION

In order that the astronauts may be made aware of an out-of-tolerance condition in any subsystem without the necessity for continuous monitoring of meters a caution and warning system was devised. (Figure 8-10)

Failures or malfunctions are placed in one of two categories:

Warning - malfunctions which require immediate corrective action and effect crew safety.

Caution - generally will indicate the occurence of one of several malfunctions in a given subsystem which will not require immediate repair or immediately affect crew safety.

Caution and Warning indications are made by three methods. For either a caution or warning situation a 3000 cps tone is heard on each astronaut's headset and the three Master Alarm lights, one on the Commanders and one on the System Engineer's side of the Main Display and Control Panel and one on the Lower Equipment Bay are illuminated.

These lights are mounted in a capsule which can be pushed to trigger a switch. Either of these switches, being pushed, will deactivate the tone and light for all astronauts. In addition to the tone and master alarm lights, an individual caution or warning indicator is lighted to denote the area of malfunction. This light remains on until the situation activating its circuit is corrected: at which time it is extinguished.

The caution and warning indicators are mounted on the Navigator Station MDC and the Lower Equipment Bay.

In addition to the above indicators there are five lights on the LGC Display and Keyboard Assembly which provide additional information about PGNS caution indications. These display lights are for IMU temperature out of tolerance (TEMP), IMU middle gimbal angle greater than 70° (Gimbal Lock), PIPA failure and problems in the LGC program (Prog), conditions in the LGC which require a restart (RESTART) and problems in the Optical Subsystem (Tracker). Whenever one of the above lights are activated, the PGNS light on the Navigator Station MDC panel, all Master Alarm lights, the PGNS light on the LEB and the warning tone will also be activated.

8.4.1 MASTER ALARMS AND AUDIBLE TONE.

The Master Alarms light red and the audible tone sounds whenever any of the caution and warning sensors are activated. Depressing any Master Alarm will extinguish the light and stop the audible tone. The caution and warning light or lights which illuminate at the same time will not go out, however, until the malfunction has been corrected.

The caution indication associated with the PGNCS is the PGNS indication (PGNS). This caution light is illuminated yellow if any of the following conditions is sensed: (1) middle roll gimbal angle is greater than $\pm 70^{\circ}$; (2) deviations in IMU temperature are greater than $\pm 5^{\circ}$ from normal; (3) OSS-CDU failure - indicates one of five possible optics channel failures in the CDU; (4) failure of some program check; (5) restart; (6) PIPA failure during periods when not thrusting. The light is extinguished either by putting the S/C control switch to the stabilization control subsystem (SCS) position or by activating the DSKY RESET pushbutton.

The two warning indications associated with the Primary Guidance and Navigation Control System are the CMC and ISS indications.

a. CMC - This warning light is illuminated red if any one of the following failures occur in the CMC:

1. The Power Supplies (+28V, +14V, +4V).

2. The Double Frequency Scaler Alarm Circuit.

3. The scaler Alarm Circuit.

The light is extinguished by either:

1. Restoration of normal voltage.

2. Placing the spacecraft control switch on the Commander Station to the Stabilization Control Subsystem (SCS) Position.

b. ISS - This warning light is illuminated red if any one of the following failures occur in the Inertial Subsystem:

1. IMU failure due to a failure in the 3.2 KC power supply, the 800 cps 5% supply or the inner, middle or outer gimbal servo error.

2. ISS CDU failure due to +14V loss, fine error high, the read counter or cos $(\theta - \Psi)$ greater than 30^{o}.

3. A PIPA failure during main engine thrusting.

The light is extinguished by placing the SC control switch to the stabilization control subsystem position.

8.5 SUMMARY

The PGNCS instrumentation equipment is the signal conditioner assembly (SCA).

The PGNCS signals to be transmitted back to earth by telemetry for monitoring and recording are routed through the signal conditioner assembly (SCA). The SCA conditions these signals to a form compatible with the Pulse Code Modulator (PCM) which codes these signals for transmission. The signals selected were based on those required to determine that the PGNCS is functioning properly and the rate at which the signals are sampled for transmission was determined by the signal characteristics.

The SCA in its role as an interface element conditions all PGNCS signals to a 0 to 5 vdc range, and routes them to the PCM.

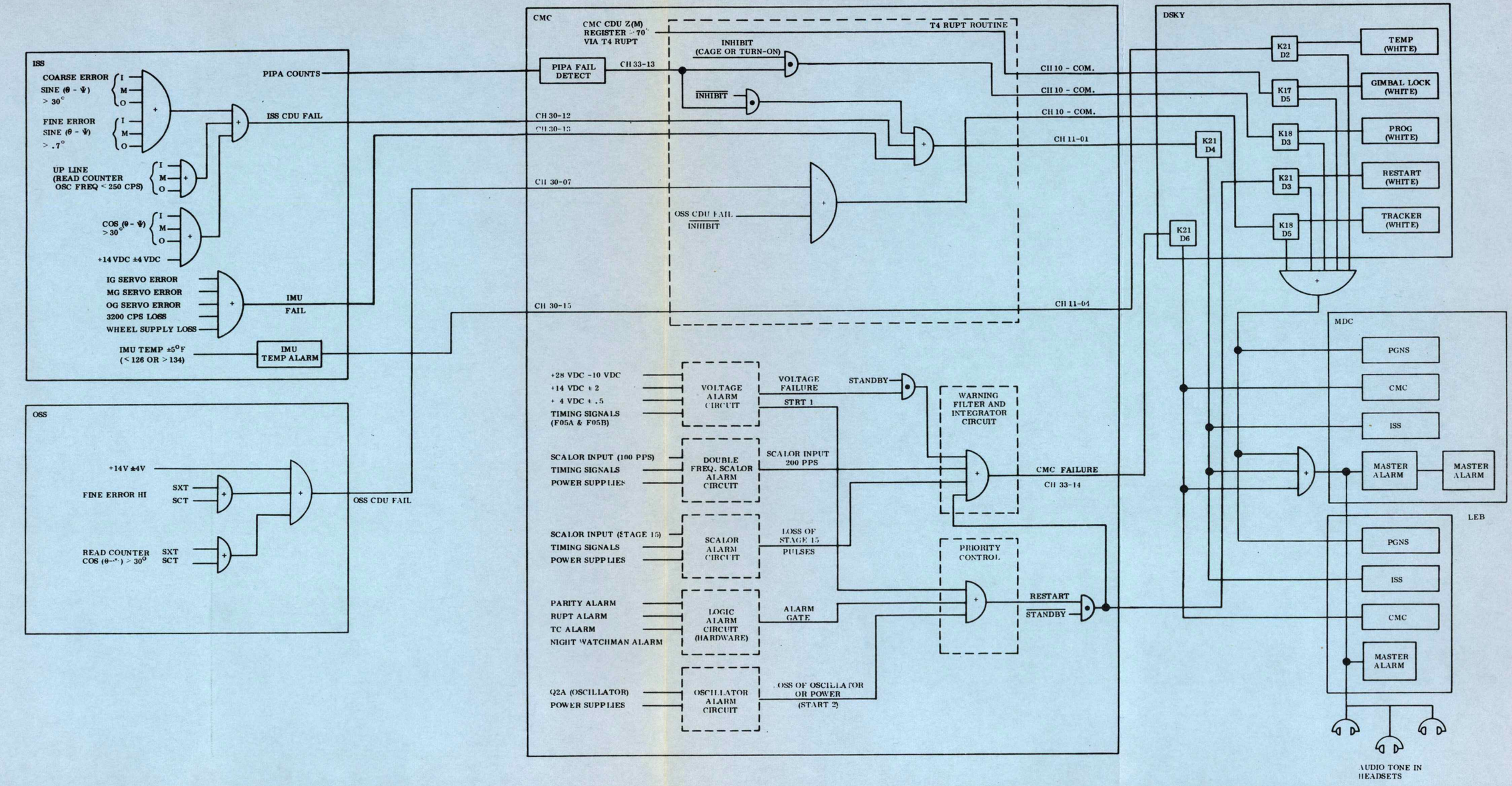


Figure 8-10. Caution and Warning Indication

SECTION IX

OPTICAL SUBSYSTEM

INTRODUCTION

The optical subsystem enables the astronaut to make optical sightings on celestial objects by means of a telescope and sextant. These sightings are used in updating this spacecraft's position and velocity and in aligning the IMU. The celestial bodies serve as the primary reference for navigation of the spacecraft when using the PGNCS.

The taking of optical sightings is a semi-automatic operation and requires the astronaut to point the optical instruments. If the celestial objects cannot be acquired by operating the optical controls alone, the astronaut must change the attitude of the spacecraft by commanding roll, pitch and yaw motion with the spacecraft rotation control.

At the instant the optical sighting is taken, the time of sighting, the angles of the optical instruments and the IMU gimbal angles if the ISS is enabled, are recorded by the CMC. Data pertaining to the location of the celestial objects and programs for navigational calculations have been stored in the CMC. The navigational measurements can be accomplished during earth orbit by measuring the angles to landmarks with the telescope. Midcourse navigation is accomplished by measuring the angle between a landmark and a star with the sextant. The IMU is aligned during flight by measuring the angle between the navigation base and each of two stars with the sextant. Optical sighting data is also used in IMU prelaunch alignment.

In case of a failure in the optics electronics, the astronaut may be required to operate the telescope manually with the universal tool and read the angles off counters on the telescope axes.

9.1 OSS EQUIPMENT

The optical subsystem consists of the following equipment (see figure 9-1):

a. Navigation Base (NB) (Portions)

b. Optical Assembly

c. Coupling Data Unit (CDU) (two channels)

d. Power Servo Assembly (PSA) (portions)

e. G&N Indicator Control Panel (portions)

f. Optical Panel

g. Eyepiece and Storage Assembly

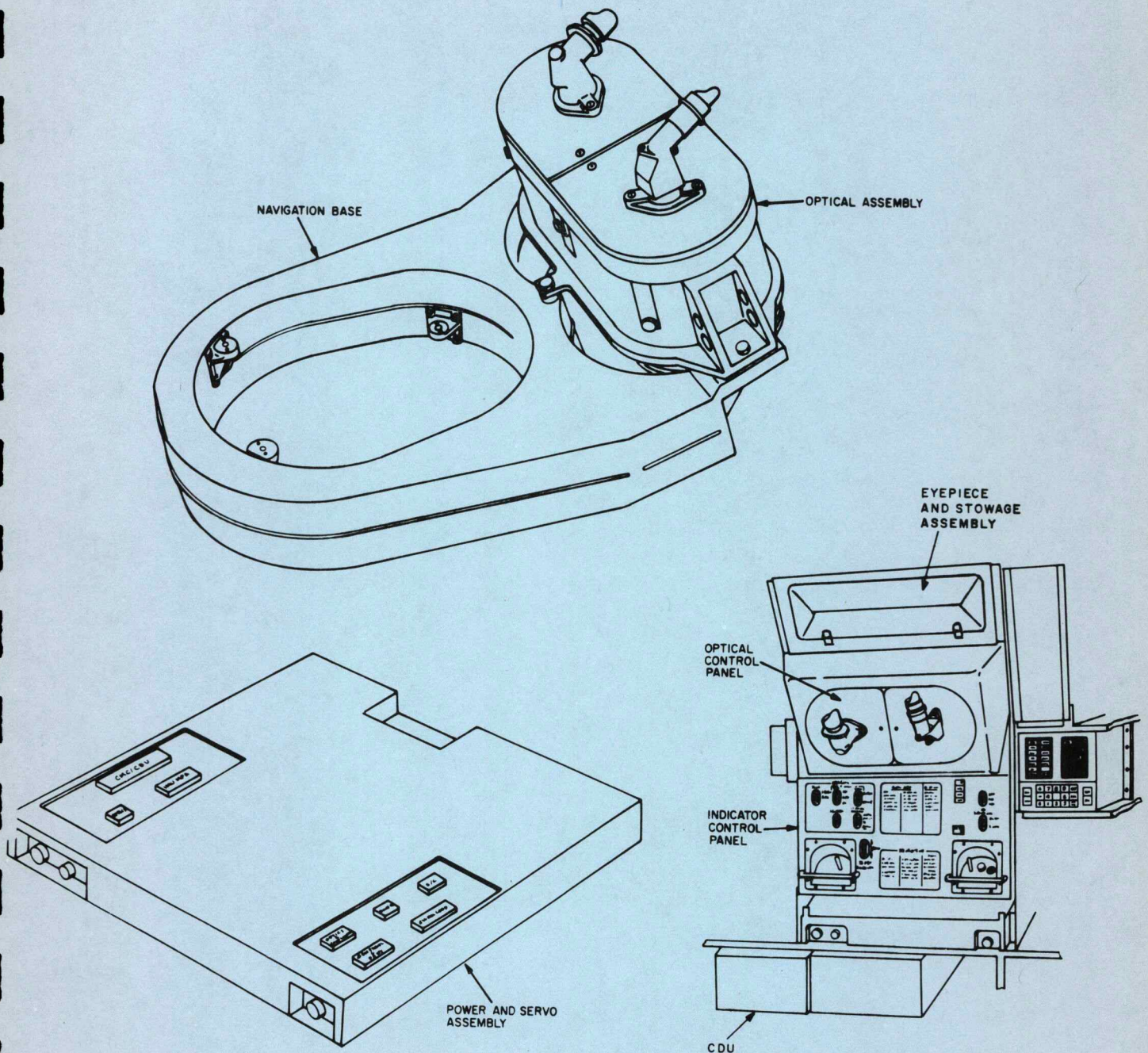


Figure 9-1. Optical Subsystem Equipment

9.2 OSS FUNCTIONAL BLOCKS

For the purpose of this explanation, the optical subsystem equipment is divided into functional blocks as shown in figure 9-2. The operation and interrelationship of these blocks are described in the following paragraphs.

9.2.1 NAVIGATION BASE. The navigation base is used as a holding fixture to provide a rigid support of the optics with respect to the IMU. The optics are fixed in precise alignment to the navigation base. Flexible sealing at the spacecraft opening is supplied by a bellows assembly around the optical instruments.

9.2.2 TELESCOPE. The telescope is mounted beside the sextant to permit parallel lines of sight through an opening in the spacecraft. The telescope, with its large field of view, is used as an aid to the sextant for coarse acquisition in midcourse flight and for measuring angles to landmarks during earth orbit.

The telescope is a refracting type and has magnification power of 1X with a field of view of 60 degrees. The telescope has two degrees of rotational freedom with the shaft axis and trunnion axis defining the axes of rotation. Continuous rotation is physically possible about the shaft axis, which is fixed with respect to the spacecraft, but in operation, is limited to the shaft movement of the sextant. Rotation about this axis defines the shaft angle (A_S). Continuous rotation is also possible about the trunnion axis, which is perpendicular to the shaft axis. Rotation about this axis defines the trunnion angle (A_t). A prism located on the trunnion axis, is rotated to reflect the image into the objective lenses of the telescope. Because of obstructions caused by spacecraft airframe, the line of sight (LOS) of the trunnion has a useful range of approximately 53 1/2 degrees. By rotating the telescope about the trunnion and shaft axes, a maximum field of approximately 107 degrees can be viewed. To control the motion of the telescope line of sight, shaft and trunnion drive rates are normally supplied to the sextant drive circuits, which position the sextant shaft and trunnion. During normal operation, the shaft and trunnion of the sextant and telescope are slaved together. To acquire objects outside the 107 degree field of view, the attitude of the spacecraft must be changed. The shaft and trunnion angles can be read directly from the telescope by counters mounted on the face of the optical panel. A tool is also provided so that the trunnion and shaft angles can be manually positioned.

9.2.3 SEXTANT. The sextant is more precise than the telescope and is used primarily during the midcourse phase for measurement of angles between a landmark and a star or for sighting each of two stars for fine alignment of the IMU. The sextant has two lines of sight, landmark and star. The landmark line of sight (landmark LOS) is fixed with respect to the spacecraft. To align the landmark LOS to a particular landmark, the attitude impulse control, which makes small changes in the spacecraft attitude rates, and the spacecraft rotation control are used. The star line of sight (star LOS) has two degrees of freedom and operates similarly to the telescope in that it can scan a field of approximately 107 degrees. Both the star LOS and landmark LOS have a 1.8 degree field of view and magnifying power of 28X. When looking through the sextant eyepiece, objects in the star and landmark lines of sight are superimposed. By obtaining a coincidence of a star and a landmark, the angle between the two can be measured.

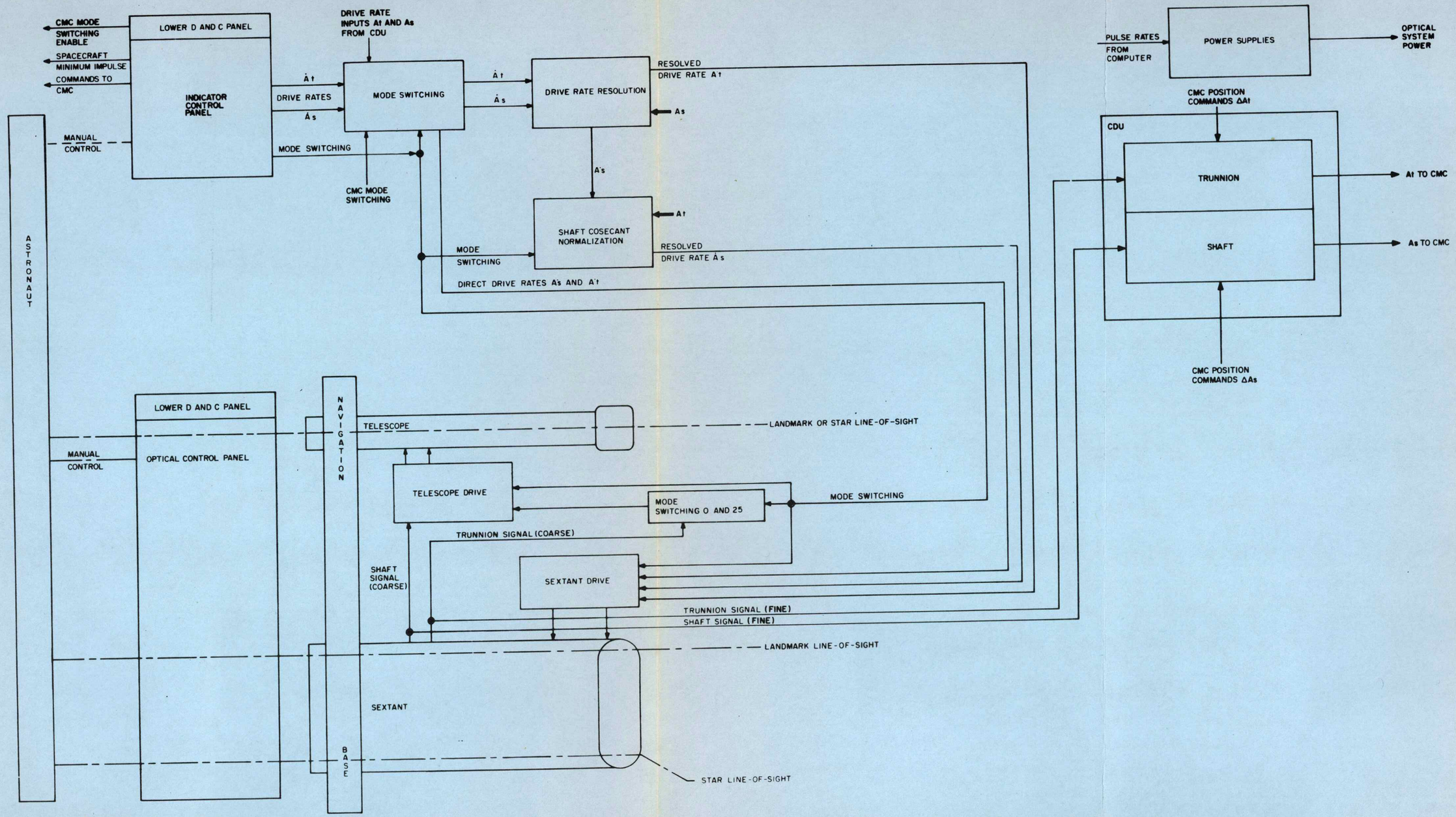


Figure 9-2. Optical Subsystem Interface

9.2.4 SHAFT AND TRUNNION DRIVE. The telescope and sextant drive circuits perform similar functions; they reposition their respective shaft and trunnion axes at the commanded rate. Sextant shaft and trunnion movement can be commanded by the sextant hand controller or the computer. The telescope shaft always follows the sextant shaft. The telescope trunnion can be commanded by mode switching to: (1) follow the sextant trunnion, (2) drive to 0 degrees, or (3) drive to 25 degrees.

9.2.5 CDU OPTICAL CHANNELS. The coupling data unit provides coupling between the CMC and the OSS. The CDU repeats the shaft and trunnion angles and transmits the angular change information to the CMC in digital form. During the computer mode of operation desired sextant (SXT) trunnion and shaft angles are obtained by providing AC inputs to the trunnion and shaft servos from the CMC through the CDU D/A converters. In addition, the CDU OSS digital to analog converters provide DC coupling between the CMC and the service propulsion system (SPS) (used during thrust vector control (TVC) to provide analog signals for positioning the SPS engine gimbals).

The location of the optics shaft and trunnion axes is transmitted to the CDU's through optics resolvers. The resolvers are located on the sextant shaft and trunnion axes and transmit angular information to the CDU's in the form of electrical signals proportional to the sine and cosines of 16X shaft and 64X trunnion angles.

9.2.6 DRIVE RATE RESOLUTION CIRCUIT. The purpose of this circuit is to resolve the sextant hand controller drive rates so the image motion in the eyepiece (left-right for large trunnion angles and up-down) is independent of the shaft angle. Without this resolution, the direction of image movement in response to the sextant hand controller would vary and depend upon the shaft angle. The drive rates are routed through the drive rate resolution circuit by mode switching (resolved or direct) controlled from the indicator control panel. The resolution is accomplished by a resolver on the sextant shaft axis.

9.2.7 SHAFT COSECANT NORMALIZATION CIRCUIT. For easier optical sightings, it is desirable that the rate of image motion (left-right or up-down) in the eyepiece be constant for a given rate input from the sextant hand controller. Since the trunnion angle affects this rate, a resolver on the sextant trunnion axis and a cosecant amplifier are used to resolve the image motion rate. The shaft cosecant normalization circuit conditions the shaft drive rates only and is connected to the sextant hand controller by switching the optics into the resolved mode.

9.2.8 MODE SWITCHING. The mode switching is controlled from the G&N indicator control panel. The switching is performed by relay and selection switches.

9.2.9 DISPLAY AND CONTROL SUBSYSTEM OPERATIONS. The panels used by the optical subsystem to display and control subsystem operation and the panel functions are as follows:

a. The optical panel provides:

(1) A mount for the optical eyepieces.

(2) Manual control of the telescope shaft and trunnion angles.

(3) Readouts of the telescope shaft and trunnion angles.

b. The G&N indicator control panel:

(1) Provides controls for switching optical subsystem modes.

(2) Issues mark commands to the CMC to define the time of measurement and to record shaft and trunnion angles at the time of the discrete.

(3) Issues mark rejects to the CMC to reject time and angle information which was recorded as a result of a mark command.

(4) Supplies commands to the stabilization and control system to enable attitude impulse control of the spacecraft.

(5) Controls the positioning of the optical unit by generating drive rates.

9.2.10 POWER SUPPLIES. The 28 volt 800 cps optics supply, packaged in the PSA, is required to operate the optical subsystem. The power supply operates from 28 VDC prime power and pulse rates from the CMC. Refer to Section VII.

9.2.11 INSTRUMENTATION. The optical subsystem is monitored by three telemetry points. The first of these signals is CG1533X (+28VDC optics operate power). This is a discrete signal which is monitored in the PSA. Section VII is the power distribution section of this manual and it contains a reference to this telemetry point. The other two telemetry points CG3721V and CG3722V (shaft and trunnion CDU DAC outputs) are monitored in the CDU. These signals indicate the magnitude and polarity of the signals in the optics CDU error counters. Section VIII of this manual contains a detailed description of all telemetered signals.

9.3 OPTICAL UNIT ASSEMBLY

The optical unit assembly consists of (1) the optica base, (2) the scanning telescope (SCT), and (3) the sextant (SXT). The position of the optical unit assembly (OUA) in the spacecraft is illustrated in figures 9-3 and 9-4. Limits on the field of view of both SXT and the SCT are imposed by the ablative material on the spacecraft exterior. The total field of view of both instruments is approximately 85^{o}.

9.3.1 OPTICAL BASE. The optical base section houses most of the electro-mechanical components of the SCT and SXT. For the SCT shaft and trunnion axes, these components include: motor generators, gear trains, resolvers and mechanical counters; for the SXT shaft axis, these components include a motor generator, gear box and a resolver. Cutaway drawings of the scanning telescope and sextant, including the optical base equipment, are shown in figures 9-5 and 9-6, respectively. The optics underpanel assembly is fastened to the optical base. It contain s(1) windows for viewing the SCT shaft and trunnion mechanical counters, (2) an input adapter for using the universal tool for operating the SCT manually and (3) the SCT prism housing assembly and eyepiece assembly. The panel also contains the mounting for the eyepiece window and the mounting for the SXT eyepiece assemblies. Attached to the exterior of the optical base are the three mounting points which are mated to the navigation base.

9.3.2 SCANNING TELESCOPE. The cutaway structure of the SCT is shown in figure 9-5. The SCT is mechanized with two axes - shaft and trunnion. The SCT operates such that the head assembly rotates about the shaft axis. The double dove prism, which is located in the head assembly, is the only component which rotates about the trunnion axis. The components which rotates about these axis are capable of 360^{o} of rotation; however, these capabilities are not fully utilized. The SCT is a single line-of-sight (LOS), low power (1X), refracting type of instrument with a 60^{o} instantaneous field of view. The optical schematic of the SCT is shown in figure 9-7. Target search and recognition is possible by direct viewing through the 60^{o} field of view.

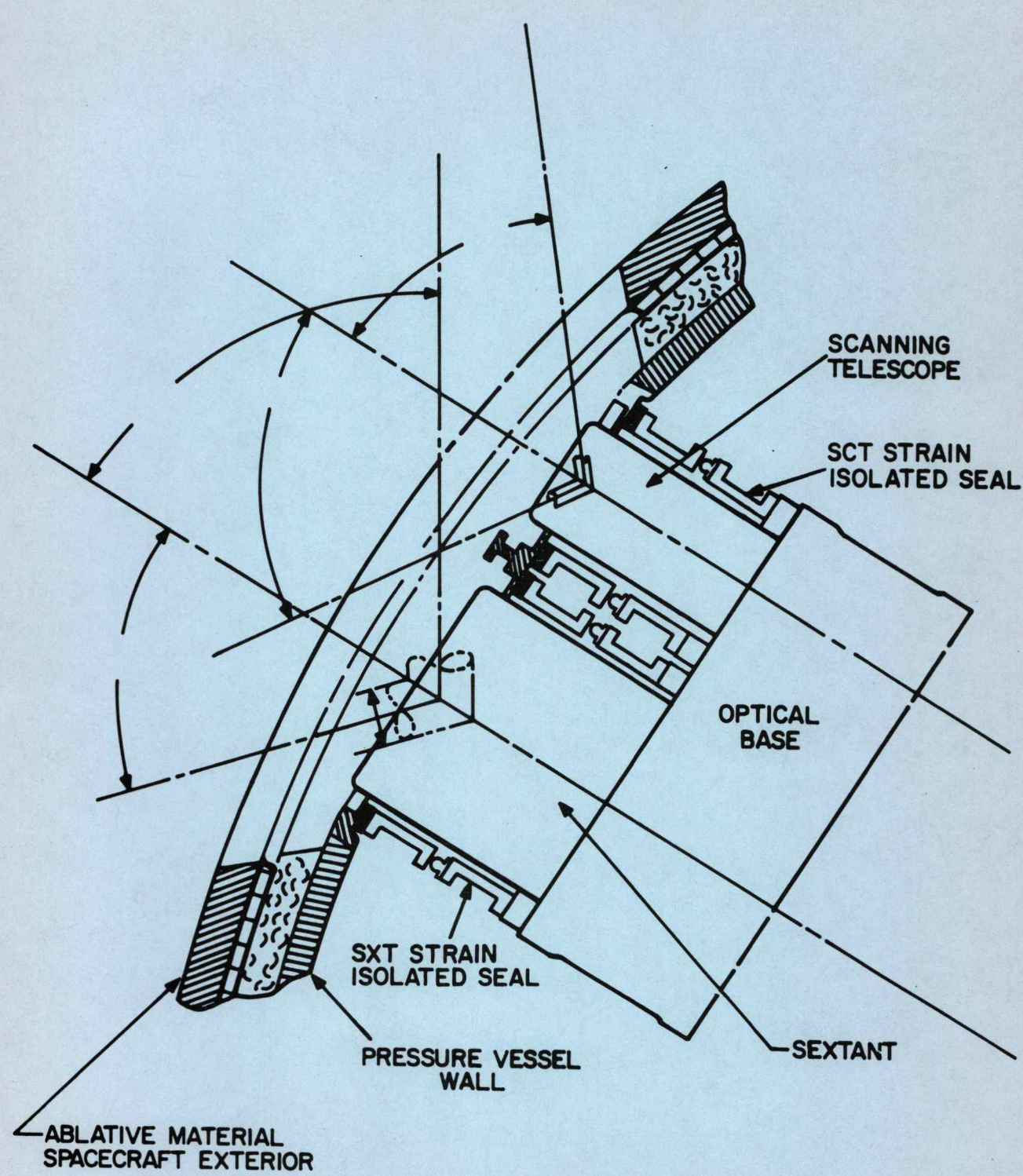


Figure 9-3. Optical Unit Horizontal Cross-section

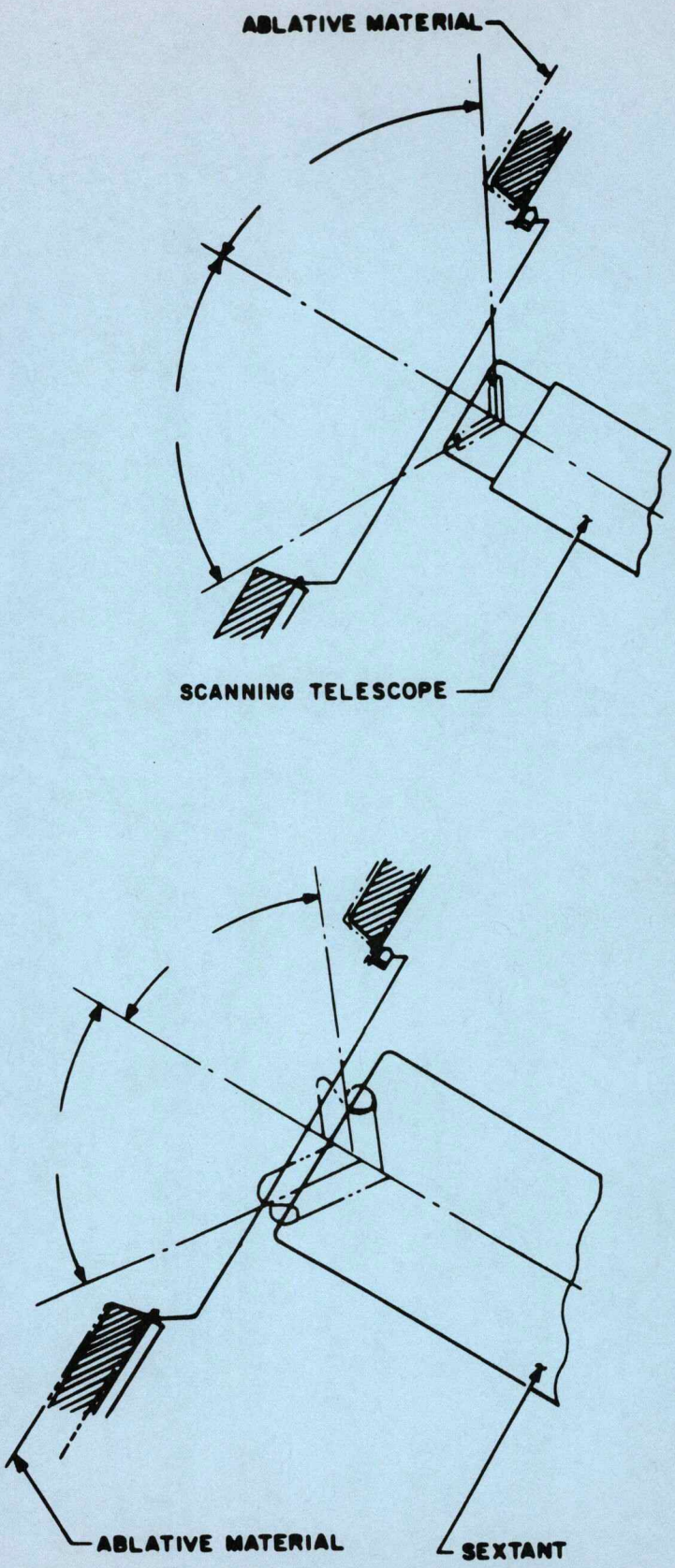


Figure 9-4. SXT and SCT Vertical Cross-section

1. SXT head assembly cover
2. Trunnion pancake resolvers
3. Threaded rod (cover support) (2)
4. Trunnion indexing mirrors and mount assembly
5. Trunnion servo gear box
6. Dummy weight
7. Objective lens assembly
8. Shaft axis assembly
9. Reticle assembly
10. Shaft servo gear box
11. SXT eyepiece assembly
12. Eyepiece window
13. SXT panel assembly
14. Shaft resolvers
15. Coolant passages (not used)
16. Ball mount (3)
17. Optical base
18. Right-angle mirrors
19. Beam splitter

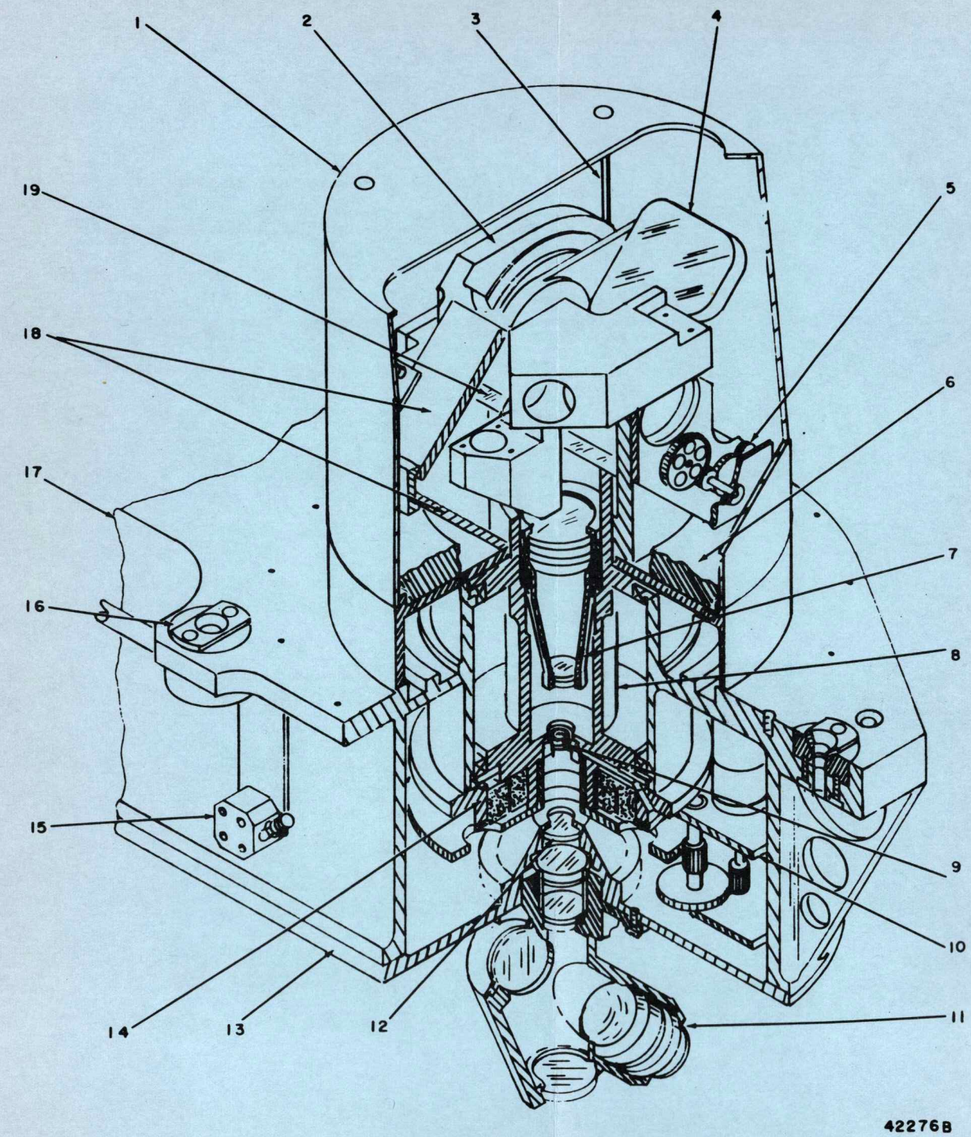


Figure 9-6. Sextant Cutaway

The shaft axis section of the SCT is made up of an outer and inner tube assembly. The outer tube assembly contains the objective lens assembly and the focal plane reticle assembly. Fixed on top of the outer tube assembly is the trunnion axis section which contains the (1) double dove prism and mount assembly, (2) mount support, (3) cam-follower and spring assembly, and (4) trunnion worm drive. The inner tube assembly contains the pechan prism and half of the relay lens system. The remaining half of the relay lens system is secured to the face of the SCT panel.

9.3.2.1 Double Dove Prism. The double dove prism contains two dove prisms which are optically matched and cemented together. This is the first optical element in the SCT to pick up the target image. The target image is inverted by the prism and transmitted to the objective lens assembly. Refer to figure 9-8.

The prism is driven by a worm gear and shaft which extends up the SCT tube. The mechanical gearing of the SCT is shown in figure 9-9. The worm gear shaft is driven by a motor generator in the SCT trunnion gear box which is located in the optical base. Positional accuracy is made possible by the use of an anti-backlash device.

This mechanism is also used to drive the trunnion axis section about the shaft axis by the use of a separate motor generator. The shaft and trunnion axes drives are linked by a differential shaft assembly. The purpose of the differential gear assembly, as shown in figure 9-10, is to permit shaft axis rotation without introducing errors in the trunnion axis and vice versa. The shaft drive gear is pinned to the differential shaft. The trunnion gears rotate freely about the differential shaft. The trunnion drive and positioning gears are connected by a planetary system which is pinned to the differential shaft. This makes (1) rotation of the shaft drive gear possible without the introduction of an error into the trunnion positioning and (2) trunnion drive possible without affecting the shaft drive gear. Two identical counters, displaying the SCT's shaft and trunnion angular position, are located in the optical base. The counters are viewed through lighted windows in the SCT panel and are calibrated to display readouts from 0^{o} to 359.98^{o} with $.002^{o}$ graduations. Manual positioning of the SCT is possible if the electronics fail.

9.3.2.2 Objective Lens Assembly. The objective lens assembly transmits the inverted image from the double dove prism and focuses this image on the reticle plane. The objective lens assembly consists of the cemented double lens fitted into the upper end of the outer tube giving the set a 60^{o} field of view.

9.3.2.3 Reticle. The reticle is located in the outer tube adjacent to the objective lens. It is accurately positioned in the focal plane so that the collimated light from the target image is viewed without any apparent parallax. The reticle cross hair intersection, as shown in figure 9-7, is the reference for the target image. The reticle is illuminated from the edge by four incandescent lamps. Three light-transmitting rods, assembled 120^{o} apart in the reticle plane, direct light from the lamps to the reticle and provide a uniform illumination at any shaft angle.

9.3.2.4 Pechan Prism. The pechan prism, figure 9-11, is located in the end of the inner telescope tube assembly that faces the reticle assembly. This prism erects and transmits the image inverted by the double dove prism. The pechan prism consists of two sections which are separated by a gap.

9.3.2.5 Relay Lens Assembly. The relay lens assembly consists of two groups of lenses: The first group is attached to the inner telescope tube opposite the pechan prism; the second group is secured to the inside face of the telescope panel.

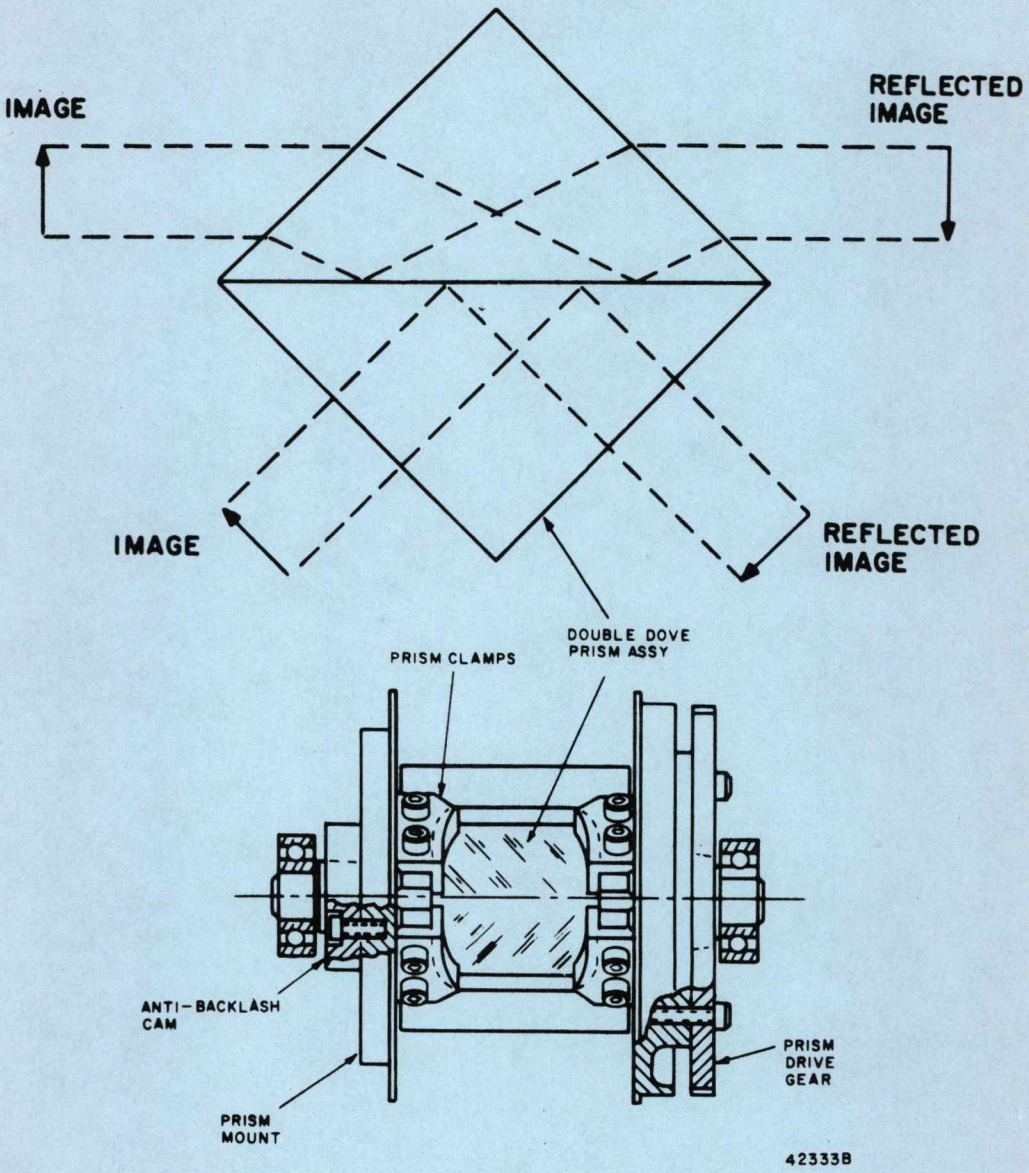


Figure 9-8. Double Dove Prism

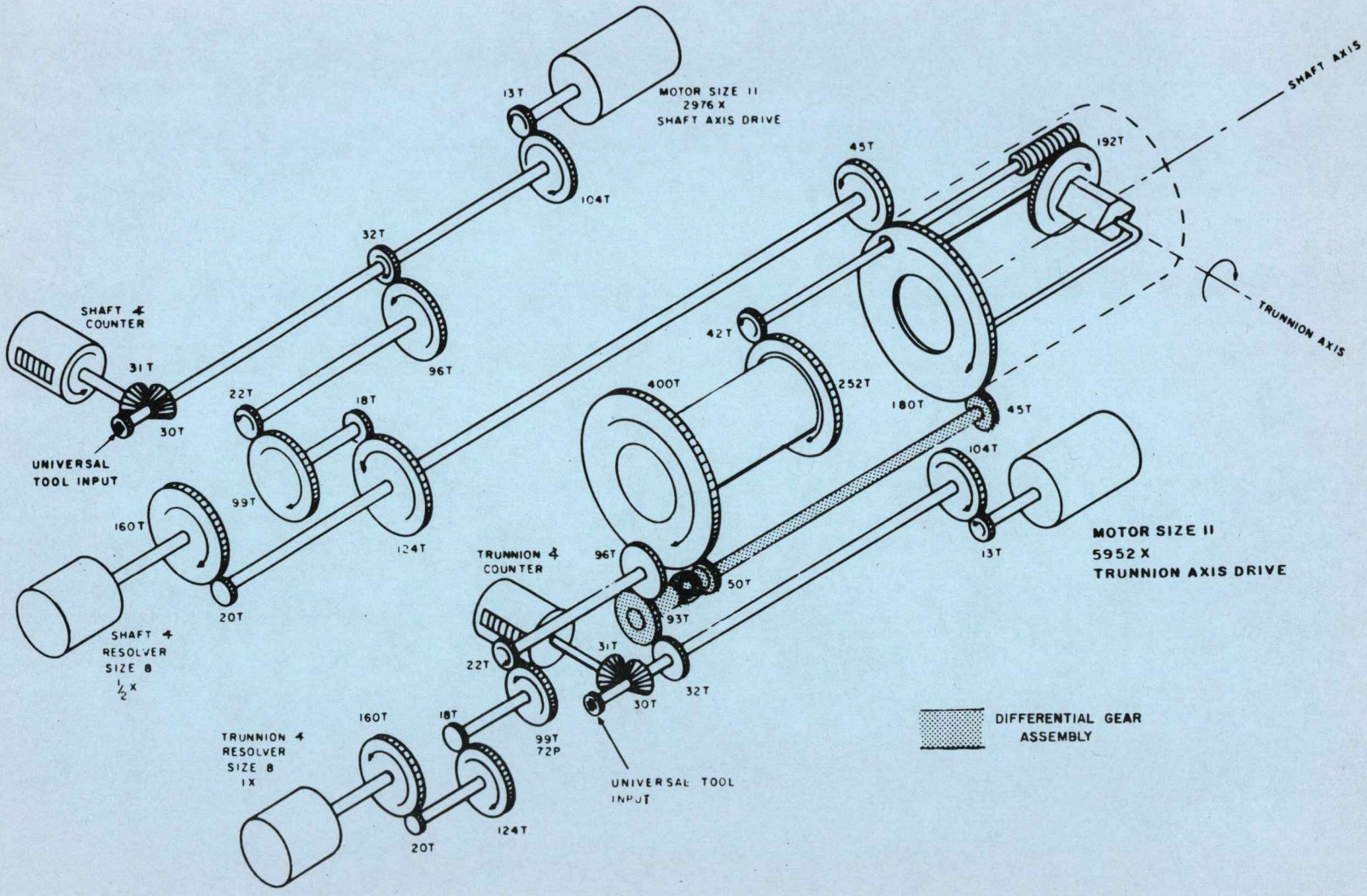


Figure 9-9. SCT Gearing

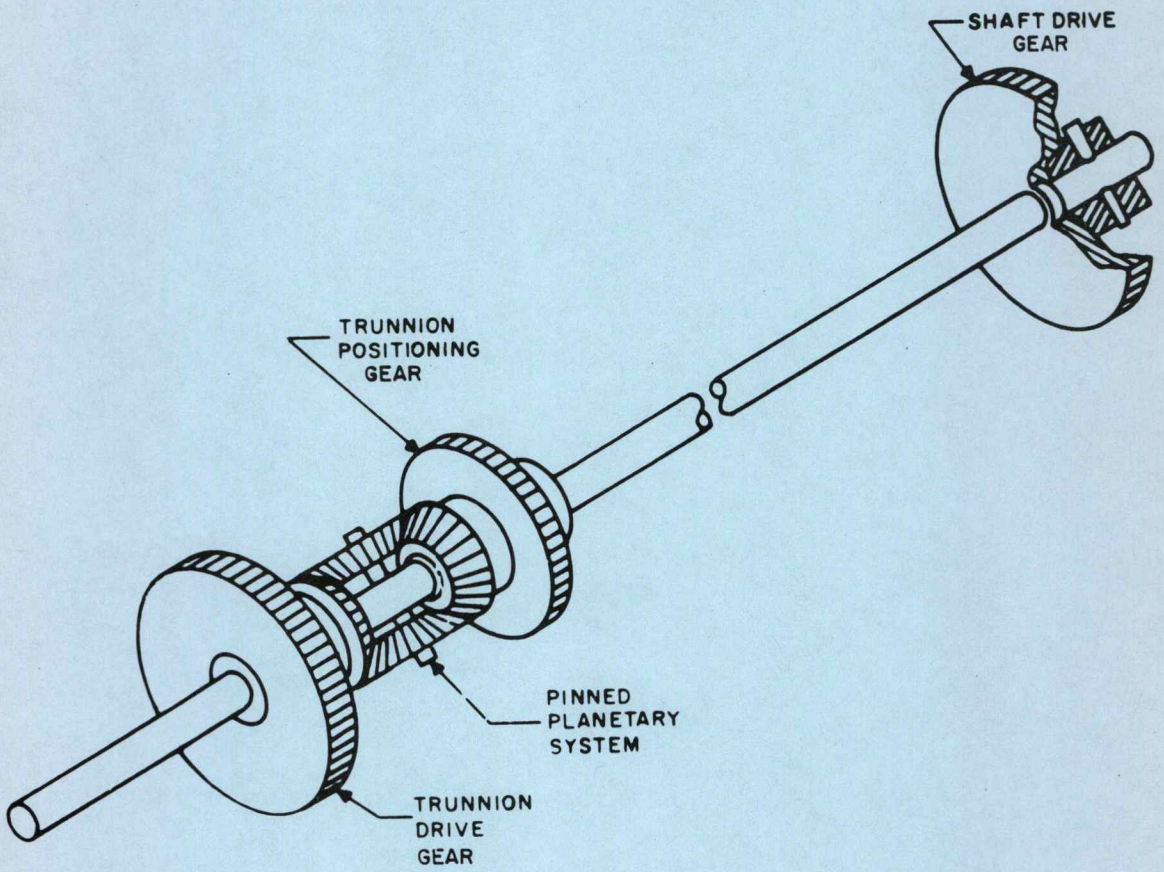


Figure 9-10. Differential Gear Assembly

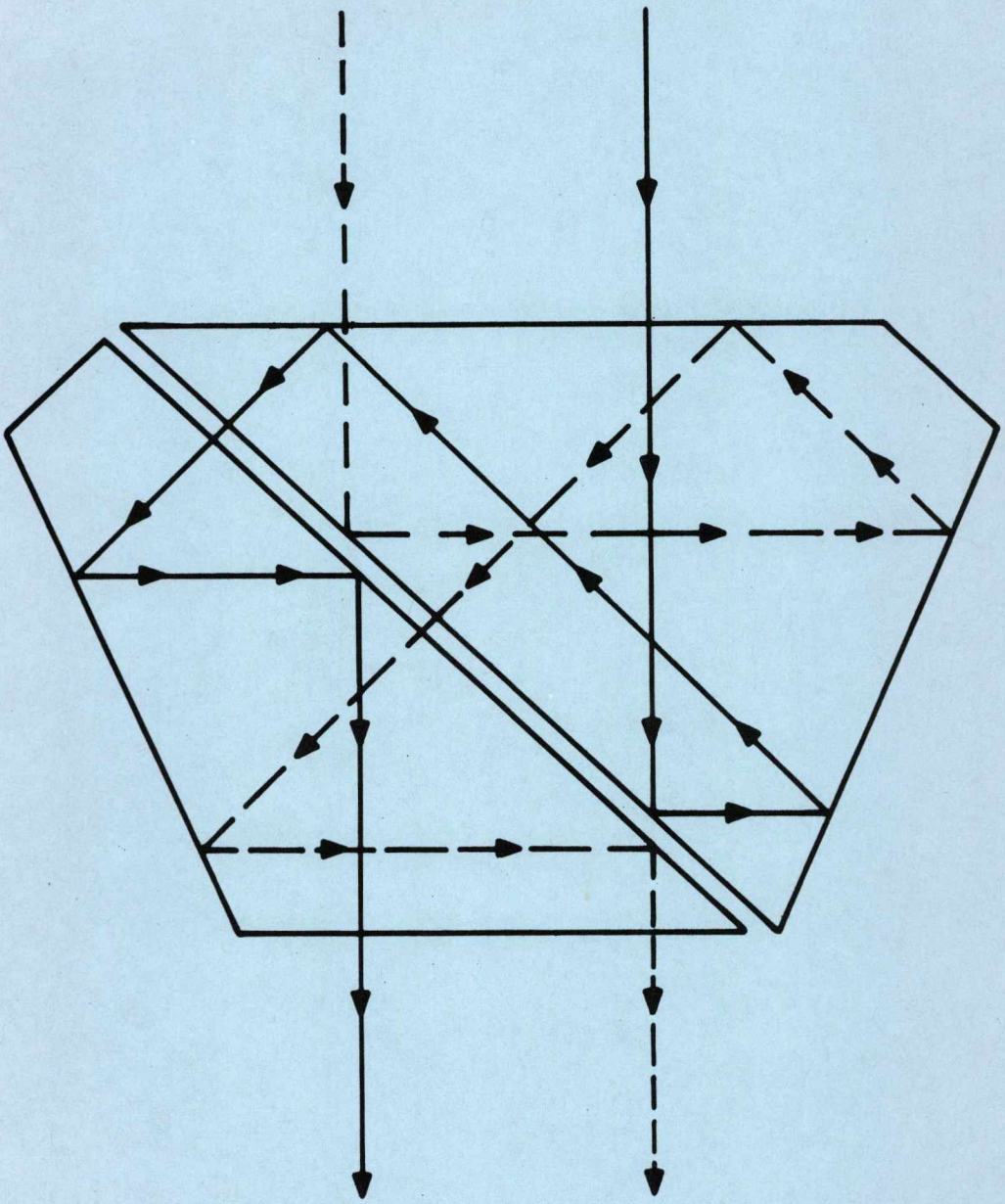


Figure 9-11. Pechan Prism

9.3.2.6 Eyepiece Window and Prism Assembly. The eyepiece window is attached to the SCT panel and provides a seal between the eyepiece components and the SCT components which are exposed to the environmental conditions outside the spacecraft. The window has no optical effect and transmits the target image directly from the relay lens assembly to the eyepiece prisms. The eyepiece prisms transmit the image to the eyepiece lens along a new line of sight (see figure 9-7) so that the center line of the eyepiece lens is not normal, but horizontal, to the optical panel.

9.3.2.7 SCT Eyepiece Assembly. The SCT eyepiece is secured to the SCT prism housing assembly. It consists of three lens assemblies secured into the eyepiece housing. An eye guard assembly made of non-toxic synthetic rubber is attached to the eyepiece housing. The eye guard is adjustable in an axial direction to allow for differences in facial contours.

An SCT long eye relief eyepiece assembly is also provided for use by the astronaut when wearing the helmet of the pressure suit. This unit will allow the astronaut to use the SCT while in the suited condition. The long eye relief eyepiece completely replaces the standard eyepiece and has a rubber guard attached to it which is contoured to match the pressure suit helmet.

9.3.2.8 SCT Optics Light Transmission. When a beam of light passes through an optical instrument, the light intensity will decrease. This decrease in intensity is primarily due to absorption and secondly to scattering. The light losses in the SCT are approximately 30% to 40% of the light impinging on the double dove prism.

9.3.3 SEXTANT. The structure of the SXT is shown on figure 9-6. The SXT is mechanized with two axes, shaft and trunnion. The SXT operates so that the index head portion of the unit rotates about the shaft axis. The components which rotate about the trunnion axis are also located in the index head and include (1) the indexing mirror and its associated trunnion drive motor, (2) resolvers, and (3) gearing.

The SXT is limited to $\pm 270^{\circ}$ of rotation about the shaft axis and to between -5° through $+50^{\circ}$ of rotation about the trunnion axis. The SXT is a multiple line-of-sight (LOS) electro-optical instrument with a 28X magnification and a 1.8° visual field of view. The optical schematic of the SXT is shown in figure 9-12.

The lines-of-sight of the SXT are the star line-of-sight (SLOS) and the landmark line-of-sight (LLOS). The LLOS is fixed within the SXT while the SLOS is moveable as a function of the motion of the indexing mirror about the trunnion and shaft axes. The SXT hardware is divided into two units, the index head assembly and the base section.

The index head assembly contains (1) the index mirror and associated trunnion drive components, (2) the right angle mirrors and (3) a beam splitter.

The base section houses the shaft axis assembly and corresponding drive components such as motor generator, resolver and gearing. It also contains the SXT telescope lens and the reticle. Attached to the base section is the SXT panel assembly which contains the eyepiece window and provides for the mounting of the SXT eyepiece.

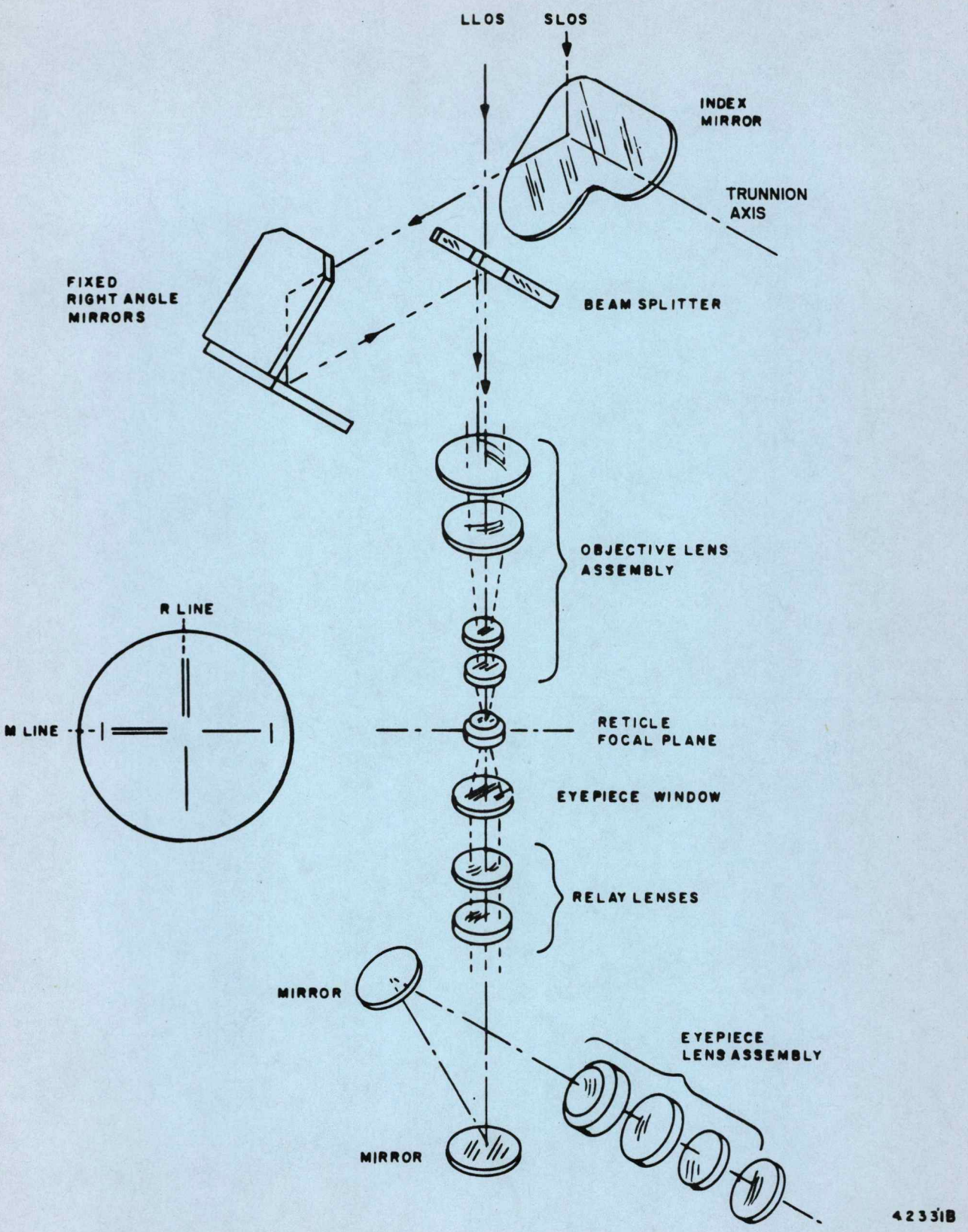


Figure 9-12. SXT Optical Schematic

9.3.3.1 Indexing Mirror Assembly. The indexing mirror is constructed of beryllium with a reflecting surface coated with silicon monoxide. The mirror is lightened, balanced, and pivoted on ball bearings to insure accurate operation. The star image is reflected into the right angle mirrors by the indexing mirror which is controlling the star LOS. As the indexing mirror moves there is an optical multiplication of the angle through which the SLOS moves, i.e., for each one degree of motion of the indexing mirror, there is two degrees of motion of the SLOS (see figure 9-13). In figure 9-13, the light from the star is reflected at a 10^{o} angle to the incident light. In figure 9-13, the mirror which has been moved by 5^{o} now has the star image reflected at an angle of 20^{o} to the incident light, i.e., an increase of 10^{o}. Therefore, it can be seen that the LOS angle increases twice as rapidly as the mirror angle.

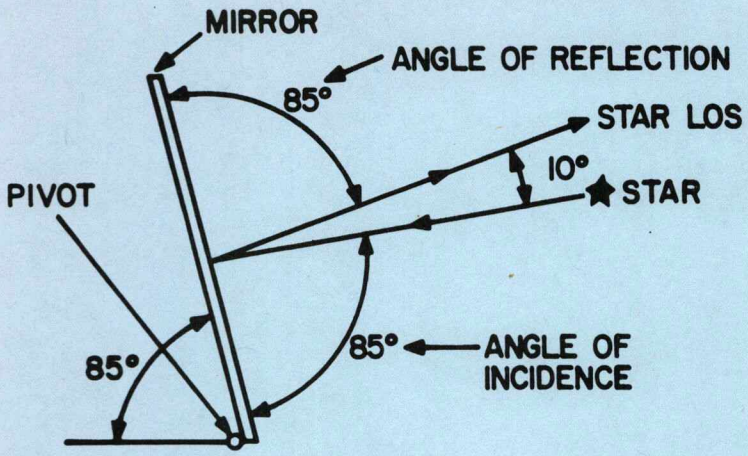
9.3.3.2 Right Angle Mirrors. Two mirrors are fixed at right angles to each other and reflect the star image onto the reflective underside of the beam splitter. Both mirrors are fabricated from beryllium with aluminized reflecting surfaces and a silicon monoxide coating.

9.3.3.3 Beam Splitter. As mentioned previously, the SXT has two visual lines-of-sight, the SLOS and the LLOS, which are viewed simultaneously by the astronaut. When viewed directly, the landmark has a greater intensity of illumination than that produced by the star. For this reason, the star would be obscured by the landmark's brightness. The beam splitter's purpose is, therefore, to transmit both the star and landmark images simultaneously into a common eyepiece in such fashion that they both can be seen. The beam splitter's construction provides for the transmission of one image by total reflection from one surface; the second image is reduced in intensity by partial refraction through the beam splitter. As can be seen in figure 9-12, the land, mark light is refracted through the beam splitter, and the star light is reflected from the bottom of the beam splitter. This introduces both images into the objective lens assembly.

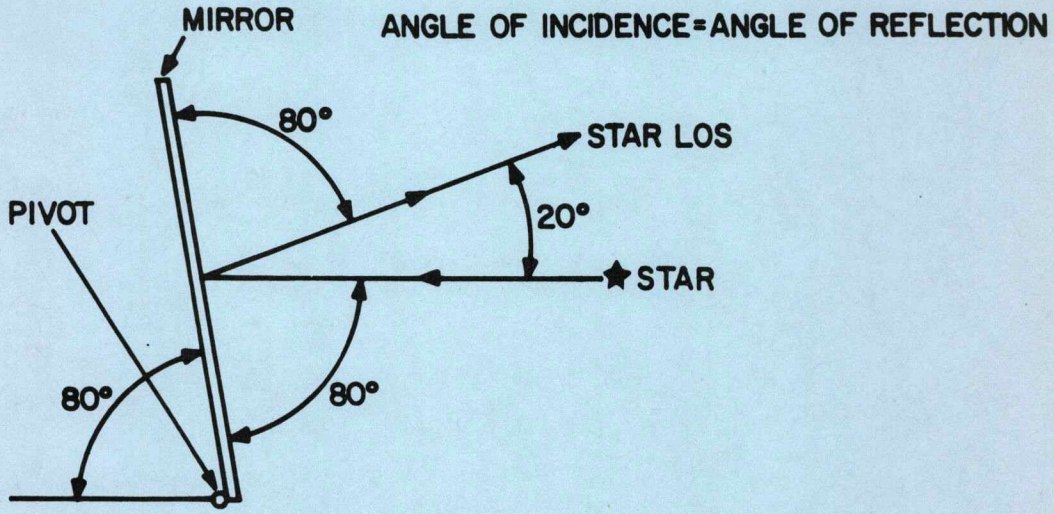
9.3.3.4 SXT Telescope Optics. The SXT telescope optics consists of an objective lens assembly, a reticle and an eyepiece window. The objective lens assembly consists of two objective lenses and two intermediate lenses which form a telephoto-type lens system. The reticle, as shown in figure 9-12, is positioned in focal plane of the objective lens. The illumination of the reticle is provided by four lamps which emit light onto three transmitting rods spaced evenly around the reticle edge. The eyepiece window has no optical effect on the SXT optics and serves as a seal in the SXT panel.

9.3.3.5 SXT Eyepiece Assembly. The eyepiece assembly consists of the eyepiece objective lens, two mirrors and the eyepiece ocular lens. The objective lens, also called relay lens, relays the images to the two fixed mirrors. The mirror provides a change in direction of the lines-of-sight and thereby facilitates the astronauts' use of the SXT. The eyepiece assembly provides 3.4 power magnification of the total 28 power magnification of the SXT.

9.3.3.6 SXT Optics Light Transmission. In the SXT, the light impinging on the indexing and fixed mirrors is decreased by approximately 4% at each mirror which results in about 88% of star light remaining to be reflected by the beam splitter. The beam splitter further reduces the light by approximately 18% with an additional loss of about 52% through the telescope and eyepiece. The net result is a total light transmission of about 35% for the SLOS.



(A)



(B)

Figure 9-13. Motion of Indexing Mirror

In the LLOS, a loss of 89% occurs in the beam splitter. The remaining 11% is further attenuated by 52% which results in an overall transmission of about 5% in the LLOS.

9.3.4 OPTICAL SUBSYSTEM AXES. The shaft and trunnion axes of the optical unit assembly must be related to the axes of the spacecraft in order to define optics orientation with respect to the spacecraft. The optical unit assembly is mounted to the navigation base as shown in figure 9-14. The navigation base is in turn mounted to the spacecraft so that the SCT and SXT centerlines are normal to the spacecraft exterior surface. The shaft axes of both instruments, SCT and SXT, are fixed within the optical assembly along the centerlines of the instruments making these axes displaced 33^{o} above the Z_{SC} axis in the X - Z_{SC} plane. The shaft axis of the SXT defines the landmark line-of-sight (LLOS). The trunnion axes within the SCT and SXT perpendicular to the shaft axes. Prior to each utilization of the optics, it is required that they be driven to an initial or zero orientation. At this time, the shaft axes are driven to a position which is defined as "zero" when the trunnion axes are parallel to the spacecraft Y body axis. The orientation of the SXT reticle at this time is as shown in figure 9-12. The trunnion axes are likewise driven to a "zero" orientation.

In this position, the SLOS is parallel to the LLOS. The axes relationships can be tabulated as follows:

a. Shaft Axes (SA) Displaced up 33^{o} from Z_{SC} axis in X - Z_{SC} plane

b. Trunnion Axes (TA) $\perp$ SA

c. When Optics are "zeroed"

1. TA $/\!/$ Y_{SC} (Body)

2. SLOS $/\!/$ LLOS $/\!/$ Shaft axis (SA)

9.4 ASSOCIATED OPTICAL EQUIPMENT

The following equipment is associated with the Optical Unit Assembly:

a. Navigation Base (NB)

b. Strain Isolated Seal (2)

c. Indicator Control Panel

d. Coupling Data Unit

e. Power Servo Assembly (PSA) (portions).

9.4.1 NAVIGATION BASE. The navigation base (NB), figure 9-14, is a structural part of the PGNCS. The navigation base is designed to provide:

a. A rigid supporting structure for the IMU and optical assembly to retain a precision alignment of these units, and

b. Mounting of the IMU and optical assembly to the spacecraft.

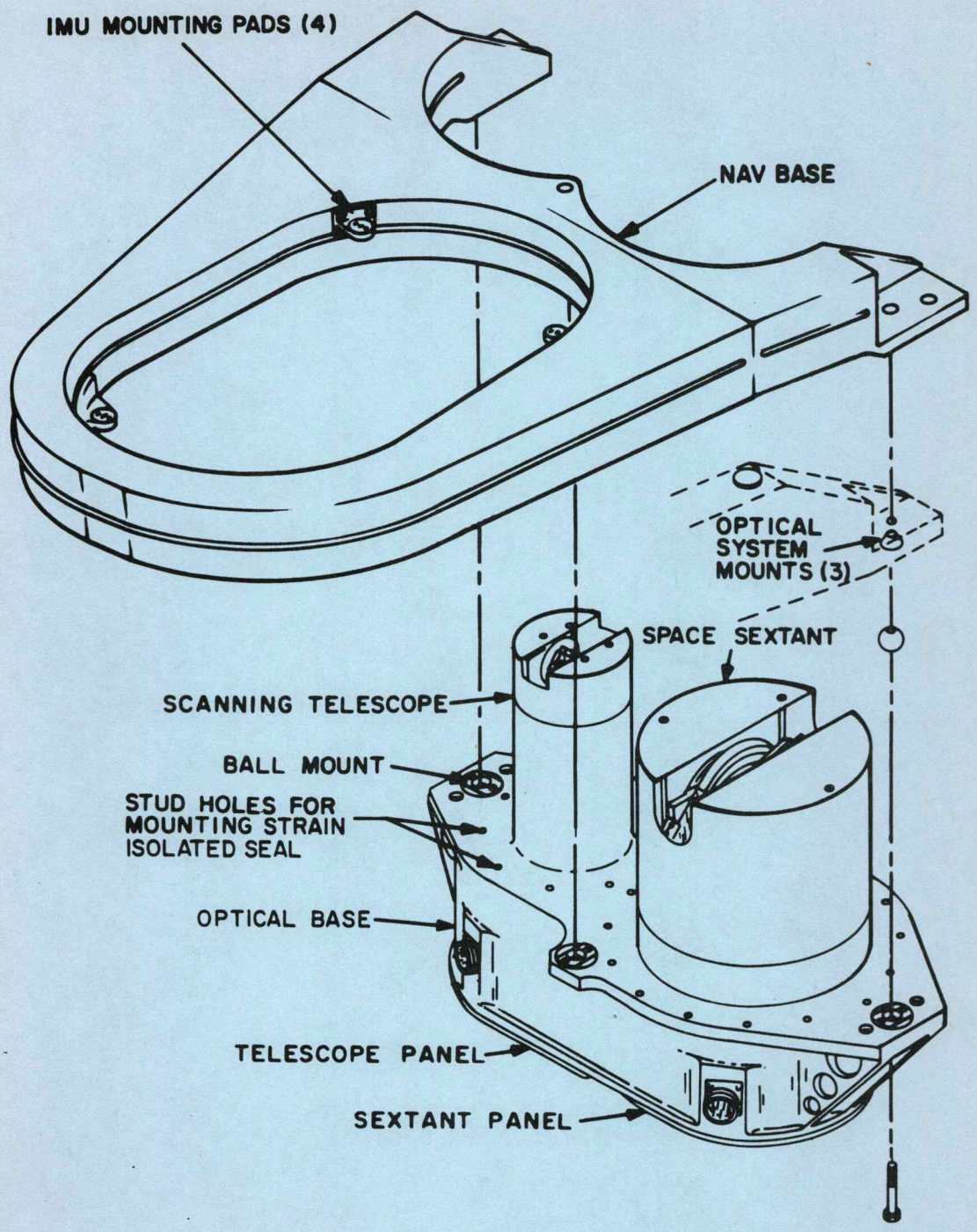


Figure 9-14. Optical Assembly and Navigation Base

The navigation base consists of formed aluminum panels which are riveted together. The aluminum structure is filled with foam to provide the necessary rigidity. Inserts are provided at four points for mounting the IMU and three points for mounting the optical unit assembly. Three mounts, two at the upper end and one at the lower end, attach the navigation base, containing the IMU and optics, to the spacecraft.

9.4.2 STRAIN ISOLATED SEAL. The optical instruments must protrude through the wall of the spacecraft pressure vessel in order to make the accurate navigational sightings. The opening provided for this purpose exposes the interior of the spacecraft to the vacuum. of space, therefore, some means of sealing is required. This sealing is accomplished by the strain isolated seal assemblies. Each assembly consists of one, reference figure 8-1, aluminum tube and one stainless steel tube attached end to end with a sealing ring at the joint. The stainless steel tube is bolted to the spacecraft with a sealing ring provided at the mating surfaces. A separate strain isolated seal is required for each of the optical instruments.

9.4.3 INDICATOR CONTROL PANEL. The G&N Indicator Control Panel is shown in figure 9-15 with the controls associated with the optical subsystem indicated. These include the optics hand controller, the optics moding controls, the attitude impulse controls and the MARK and MARK REJECT buttons. These are the only controls for the operation of the SXT and the primary controls for the SCT. A manual secondary control for the SCT is provided on the SCT panel by the use of the universal tool.

The optics hand controller has two degrees of freedom and is used to input electrical signals to the SXT shaft and trunnion drive loops in order to position the optical lines-of-sight. The optics moding controls consist of: a three position toggle switch which selects the major modes, a three position toggle switch which controls the voltage applied by the hand controller, a two position toggle switch which modifies the manual mode of operation, a three position toggle switch which modifies the operation of the SCT trunnion and an attachment point for the universal tool to open the optics doors.

The attitude impulse controller has three degrees of freedom. It is used for fine rate control of the spacecraft in pitch yaw and roll. The controller contains microswitches which provide discrete outputs. A twist of the controller will provide yaw rate changes. Up and down movements of the controller affect the spacecraft pitch rate while right and left movements of the controller affect the roll rate.

The MARK button is used by the astronaut when manually completing an optical sighting. It directs the CMC to record the position of the SXT shaft and trunnion axes along with the time of sighting. This information is used in the navigational calculations. An erroneous sighting may be cancelled by the MARK REJECT button.

9.4.4 COUPLING DATA UNIT. The identical coupling data unit (CDU) that is used in the ISS is also used as a part of the OSS. Two channels of the CDU are used, one for the SXT shaft axis and one for the SXT trunnion axis. These CDU channels repeat the SXT shaft and trunnion angles and transmit angular change information to the CMC in digital form. The angular data transmission in the trunnion channel is mechanized to generate one pulse to the CMC for five arc-seconds of movement of the SXT trunnion which is equivalent to ten arc-seconds of SLOS movement. The shaft CDU channel issues one pulse for each 40 arc-seconds of shaft movement. The location of the SXT shaft and trunnion axes are transmitted to the CDU's through 16X and 64X resolvers located on the SXT shaft and trunnion axes respectively. This angular information is transmitted to the CDU's in the form of electrical signals proportional to the sine and cosine of 16X shaft angle and 64X trunnion angle.

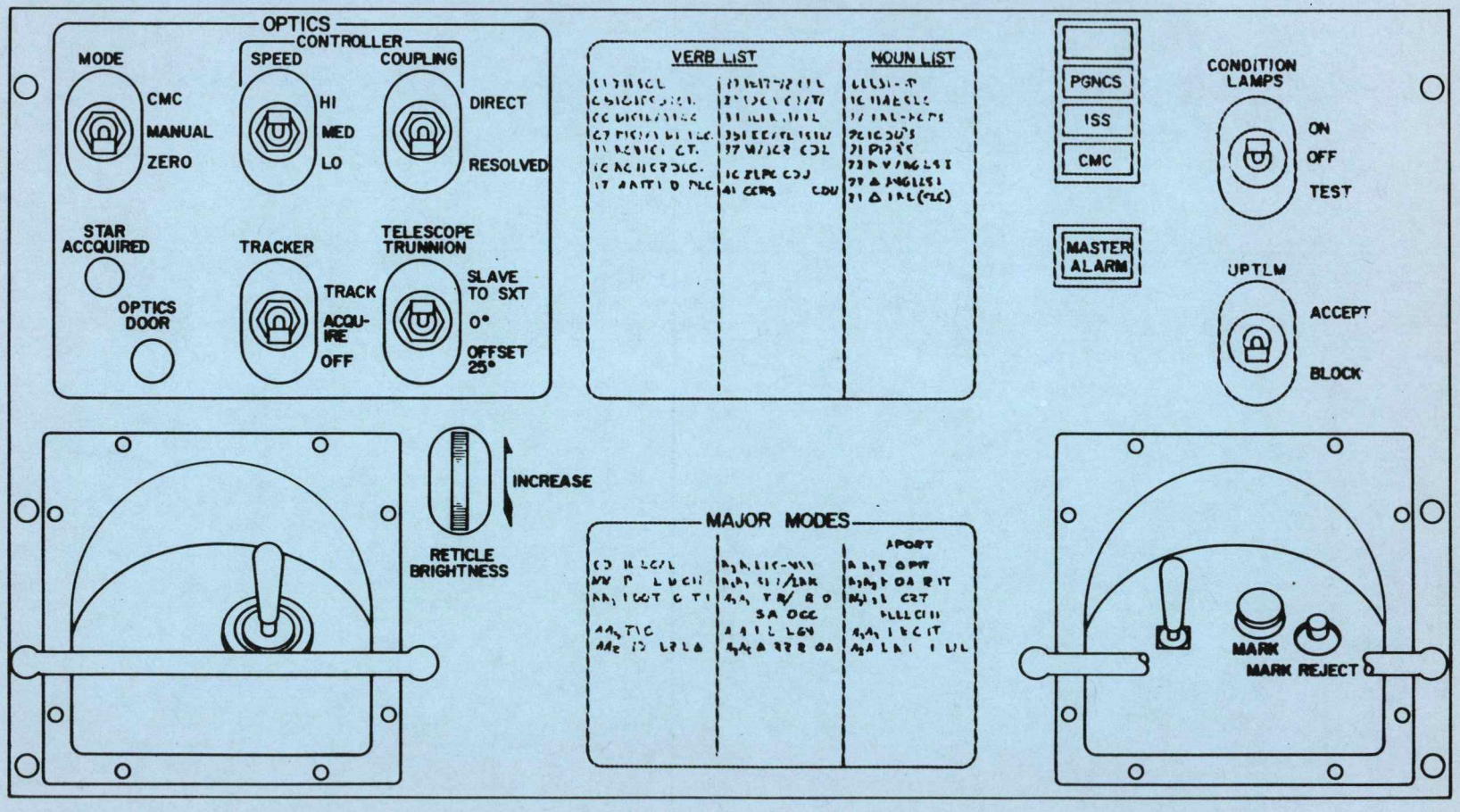


Figure 9-15. Indicator Control Panel

During the computer mode of operation, the CDU provides digital to analog conversion of the CMC output to generate an ac input to the SXT shaft and trunnion servos. This analog input to the SXT axes will drive the SLOS to some desired position. In addition the OSS channels of the CDU perform a second function on a time-sharing basis. During a thrust vector control function, these channels provide digital to analog conversion between the CMC and the service propulsion system (SPS) gimbals.

The operation of the CDU's is the essentially the same as described in Section III.

9.4.5 POWER AND SERVO ASSEMBLY. The electronics that are used to mechanize the optical unit assembly are located in the power and servo assembly (PSA) as described in Section II.

9.5 OPTICAL LOOP MECHANIZATION

The simplified mechanization of the optical loops is shown in figure 9-16. This mechanization will be broken down in later figures to define the specific modes of operation. The SXT is the primary optical instrument and is therefore under the direct control from two possible inputs, the hand controller, and the computer via the digital to analog conversion portion of the CDU optical channels. The electronics associated with the control of the SXT are defined as the integrating servo loops for the trunnion axis and shaft axis. The shaft and trunnion axes of the SCT are slaved to the SXT and are referred to as the position servo loops. The SCT shaft is always slaved to the SXT shaft, but the SCT trunnion may operate independent of the SXT trunnion in various optical modes, as selected by the astronaut. The optical channels of the CDU receive inputs from the SXT resolvers and through analog to digital conversion transmit changes in the SXT shaft and trunnion position to the computer.

The integrating servo loops utilize a selected input to the motor drive amplifier (MDA) to drive a motor in the SXT to position either the SXT shaft or trunnion. A tachometer feedback is provided which can either be supplied directly to the MDA or can first be compensated for in the MDA and then used as a feedback signal. The choice of MDA feedback is dependent upon the mode of operation selected. In order for the computer to obtain positional information from the optical loops, a fine resolver (64X) on the SXT trunnion and a fine resolver (16X) on the SXT shaft provide sine and cosine information to the CDU. This analog information is converted to digital information in the CDU and is transmitted to the CMC as incremental shaft and trunnion positional changes.

The SCT position loop is a coarse resolver system only, with the 1X SXT trunnion transmitter resolver providing an input to the 1X receiver resolver in SCT trunnion and the 1X SXT shaft transmitter resolver providing an input to the 1X receiver resolver in the SCT shaft.

The relay logic shown in figure 9-16 does not necessarily represent a single relay but could be a number of simultaneously energized relays. The electronics used in this mechanization are a part of the PSA. Also shown on this figure are the switches which control the optics moding and their output (represented by a number) when used. These numbers are utilized in the loop mechanization to indicate when a particular item of electronics is activated or when a particular item of electronics is activated or when a particular relay is energized.

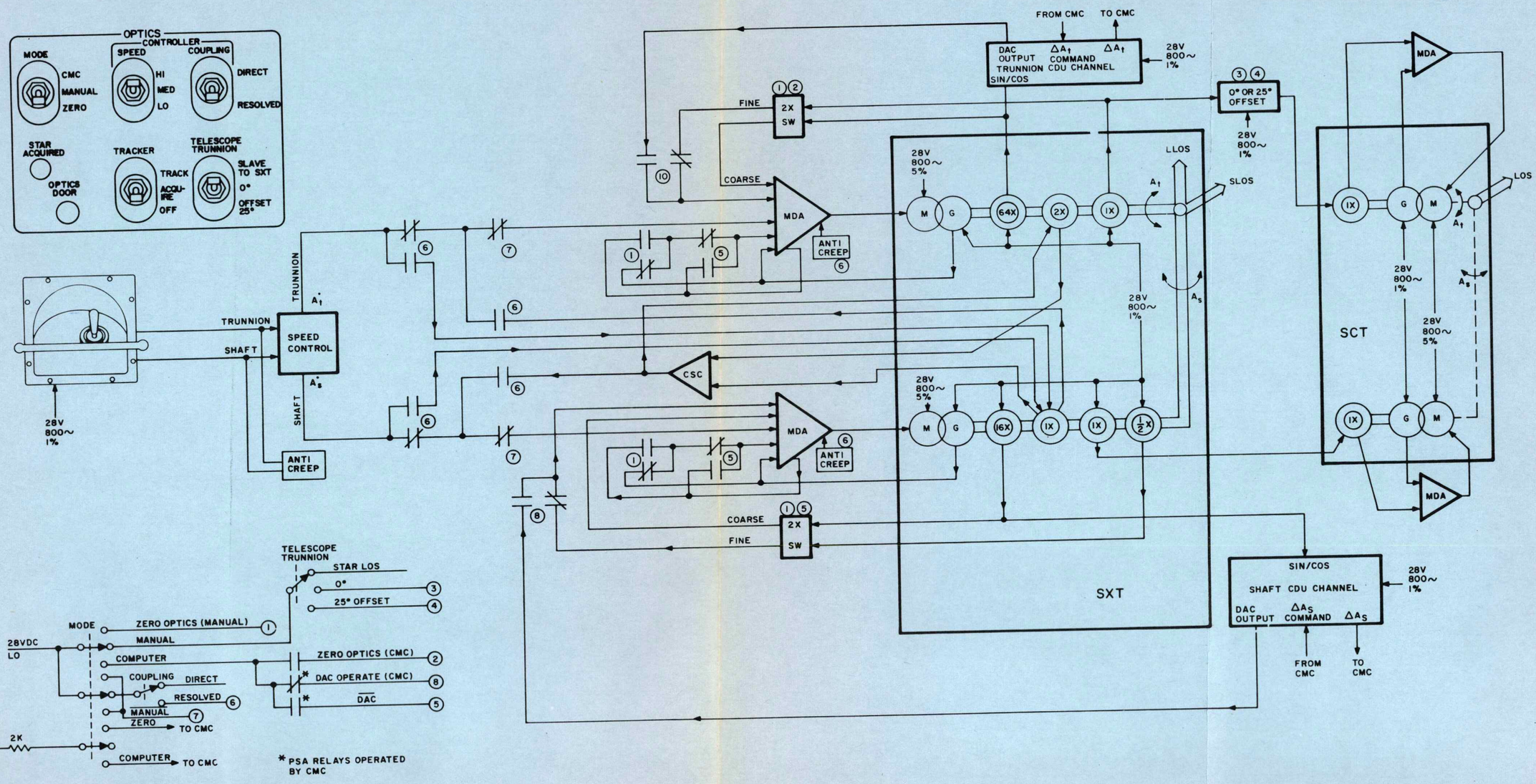


Figure 9-16. Optics Mechanization

The modes of operation for the optical subsystem are selected by the astronaut using the controls located on the indicator control panel. There are three major modes of operation for the OSS.

a. Zero optics

b. Manual control

c. Computer Control

Within each of these modes there are variations which will be described as a part of that mode description.

9.5.1 ZERO OPTICS MODE. During the zero optics mode, figure 9-17, the shaft and trunnion axes of the SXT are driven to their zero positions by taking the outputs of the transmitting resolvers (1X and 64X in trunnion and 1/2X and 16X in shaft) and feeding them through the two-speed (2X) switches to the motor drive amplifier (MDA). The MDA in turn drive loops to null positions as indicated by zero output from the resolvers. The SCT shaft and trunnion axes follow to a zero position. After 15 seconds, the computer will issue a CDU zero discrete and will initialize its shaft and trunnion counters in preparation for receiving new data from the CDU.

The zero optics mode can be selected either manually by the flight crew or by the computer after the computer control mode of operation has been manually selected. The computer selects zero optics by energizing a relay in the PSA via a relay driver, which in turn will energize the two-speed switch. The computer is notified of the zero optics mode by a signal from the mode control swtich when it is in the zero position.

9.5.2 MANUAL MODE OPERATION. The manual mode can be selected to operate under either direct hand control or resolved hand control. Independent control of the SCT trunnion is possible in both of these mode variations.

9.5.2.1 Manual Direct Operation. The manual direct mode mechanization is shown in figure 9-18. When in this mode the hand controller outputs are applied directly to the SXT shaft and trunnion motor drive amplifiers. Forward and back motion of the hand controller command increasing and decreasing trunnion angles, and right and left motion of the hand controller command increasing and decreasing shaft angles respectively. See figure 9-19 for a tabular presentation of the motion of the SXT in various modes. The target image motion is in the R-M coordinate system, the position of which is dependent upon the position of the SXT shaft.

The apparent speed of the image motion can be regulated by the flight crew by selecting either low, medium or high controller speed on the indicator control panel. This regulates the voltage applied to the motor drive amplifier, $A_s^{\cdot}$ and $A_t^{\cdot}$, and therefore the shaft and trunnion drive rates. The maximum rates are approximately 18 degrees per second for the shaft and nine degrees per second for the trunnion.

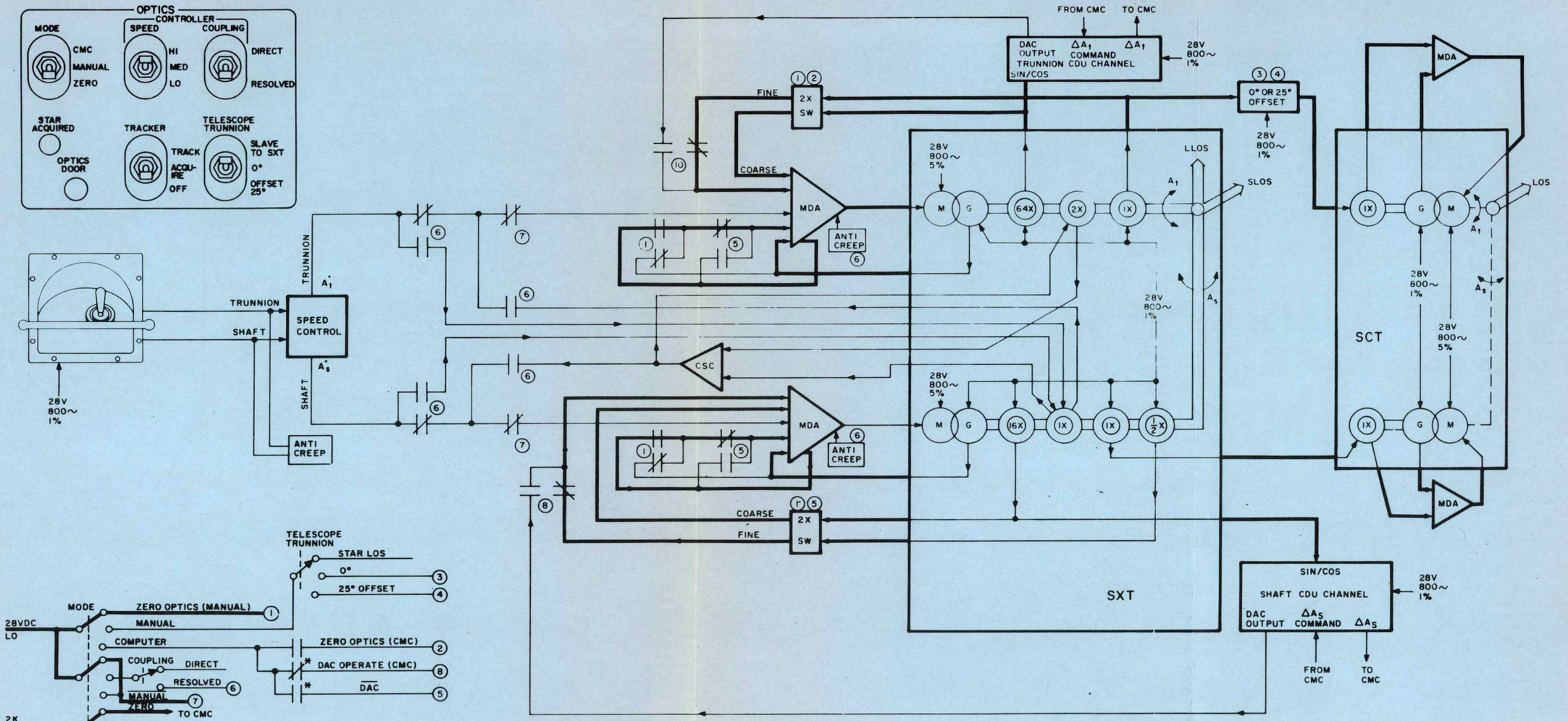


Figure 9-17. Zero Optics Mode (Manual)

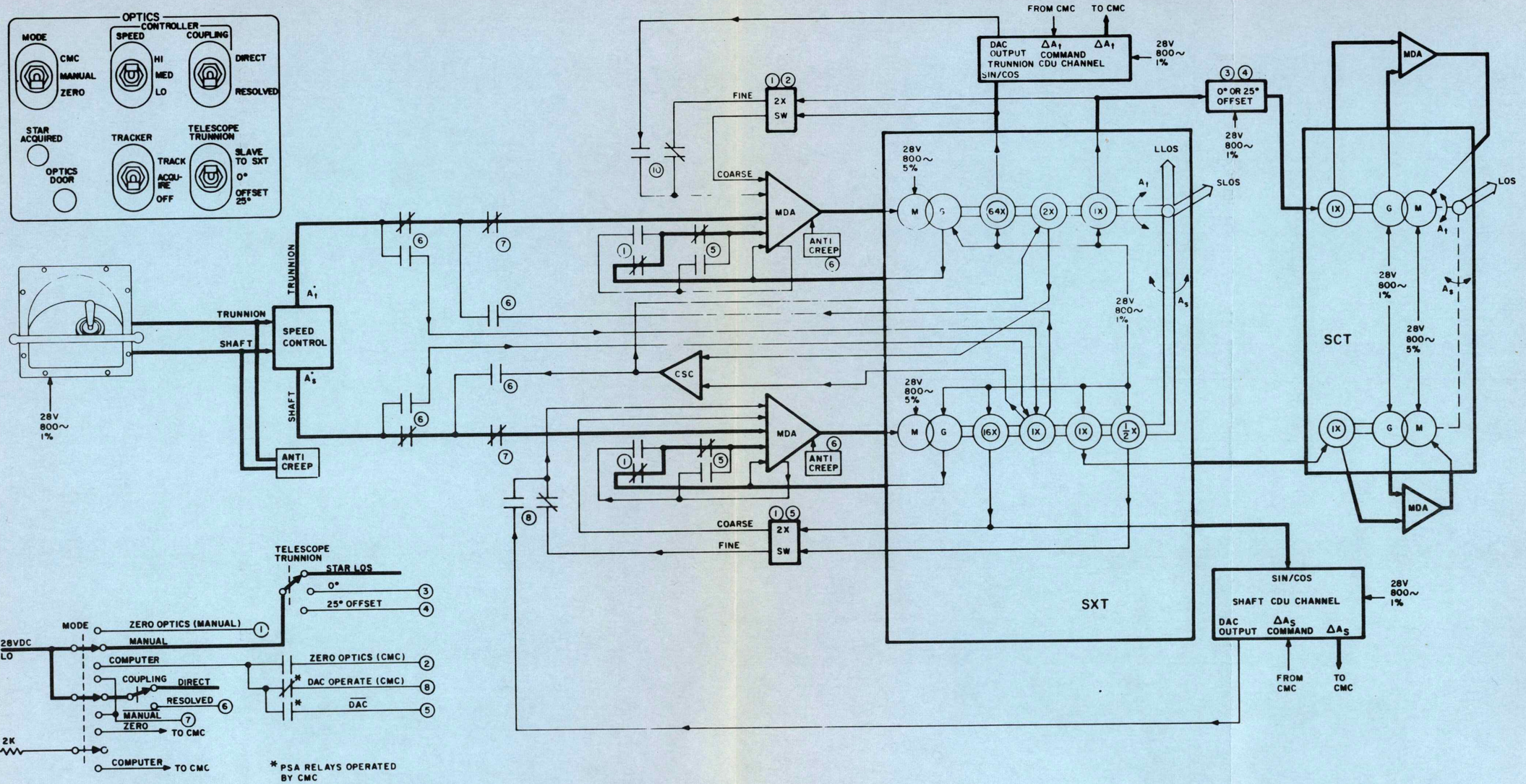
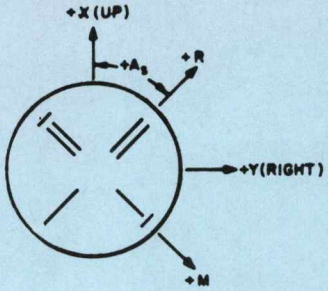


Figure 9-18. Manual Direct Mode



Controller Mode	Controller Motion	Apparent Target Image Motion	CDU Trunnion Readout and SXT Trunnion Angle	CDU Shaft Readout and SXT Shaft Angle
Direct Mode *$-90^{o} < A_s < +90^{o}$ $A_t > 0^{o}$	Down Up Left Right	+ R - R + M - M	Decrease Increase	 Decrease Increase
Resolved Mode *$0^{o} < A_s < 90^{o}$ $A_t > 5^{o}$	Down Up Left Right	- X + X - Y + Y	Increase Decrease Increase Decrease	Decrease Increase Increase Decrease

In direct mode: Movement is along a coordinate system that is rotated through angle A_s.

In resolved mode: Movement is along an X-Y axis (independent of A_s).

*Angular limits are for illustration purposes only.

Figure 9-19. Sextant Image Motion

9.5.2.1.1 Slave Telescope Modes. The slave telescope modes provide for alternate operation of the telescope trunnion while the SXT is being operated manually. The alternate modes are selected by the telescope trunnion switch on the mode control panel. There are three possible selections, SLAVE to SXT, 0^{o} and OFFSET 25^{o}. With this switch in the SLAVE to SXT position the SCT trunnion axis is slaved to the SXT trunnion. This is the normal operating position for the SCT. With the switch in the 0^{o} position the SCT trunnion is locked in a zero position by the application of a fixed voltage to the SCT trunnion 1X receiving resolver. This will cause this position loop to null in a zero orientation. Therefore, the center line of the SCT 60^{o} field-of-view is held parallel to the LLOS of the SXT.

With the switch in the 25^{o} offset position an external voltage is applied to the same 1X receiving resolver which will cause the SCT trunnion position loop to null out so that the center line of the 60^{o} field-of-view is offset 25^{o} (A_t of SCT at 12.5^{o}) from the LLOS of the SXT. This position of the SCT trunnion will allow the landmark to remain in the 60^{o} field-of-view while still providing a total possible field-of-view of 110^{o} if the SCT shaft is swept through 360^{o}.

9.5.2.2 Manual Resolved Operation. The manual resolved mode mechanization is shown in figure 9-20. When in this mode, the hand controller outputs are put through a matrix transformation prior to being directed to the shaft and trunnion motor drive amplifiers. The matrix transformation makes the image motion correspond directly to the hand controller motion. That is, up, down, right and left motions of the hand controller commands the target image to move up, down, right and left, respectively, in the field of view. In other words, the image motion is in the X-Y spacecraft coordinate system. The matrix transformation takes place in two steps. The outputs of the hand controller are routed to the 1X resolver on the SXT shaft. Here the drive signals $A_s^{\cdot}$ and $A_t^{\cdot}$ are transformed by the sine and cosine functions of the shaft angle (A_S). One of the two outputs of the 1X resolver is sent to the SXT trunnion motor drive amplifier. The second output is then resolved through the SLOS angle (A_{LOS}) that the target image motion will be independent of SLOS angle. This is accomplished by the cosecant computing amplifier (CSC) and the 2X computing resolver located on the SXT trunnion axis. See figure 9-21 for a simplified diagram of the shaft drive gain variations. The net result is that the shaft drive rate, $A_s^{\cdot}$ is inversely proportional to the sine of the SLOS angle (ALOS). The speed controller is also operational in this mode.

9.5.2.2.1 Optics-Computer Mark Logic. The MARK and MARK REJECT buttons on the indicator control panel are utilized to instruct the computer that a navigation fix has taken place and that SXT shaft and trunnion position and the time should either be recorded or rejected. The mark command is generated manually by the flight crew which energizes the mark relay. The mark relay transmits a mark command to the computer. If an erroneous mark is made, the mark reject button is depressed which will generate a "mark reject" command to the computer.

9.5.2.3 Computer Mode Operation. The computer controlled operation is selected by placing the moding switch in computer position. The mechanization of this loop is shown in figure 9-22. The functional operation to be performed by the optics is then chosen by the computer program that has been selected by the flight crew. The operation of the SXT under computer control is accomplished by completing the circuit from the CDU digital to analog converters (DAC) to the shaft and trunnion motor drive amplifier. The computer can then provide inputs to these amplifiers via a digital input to the CDU which are converted in the DAC to an 800 cycle signal that can be used by the MDA. This mode is used when it is desired to look at a specific star for which the computer has the corresponding star coordinates. The computer will also know the

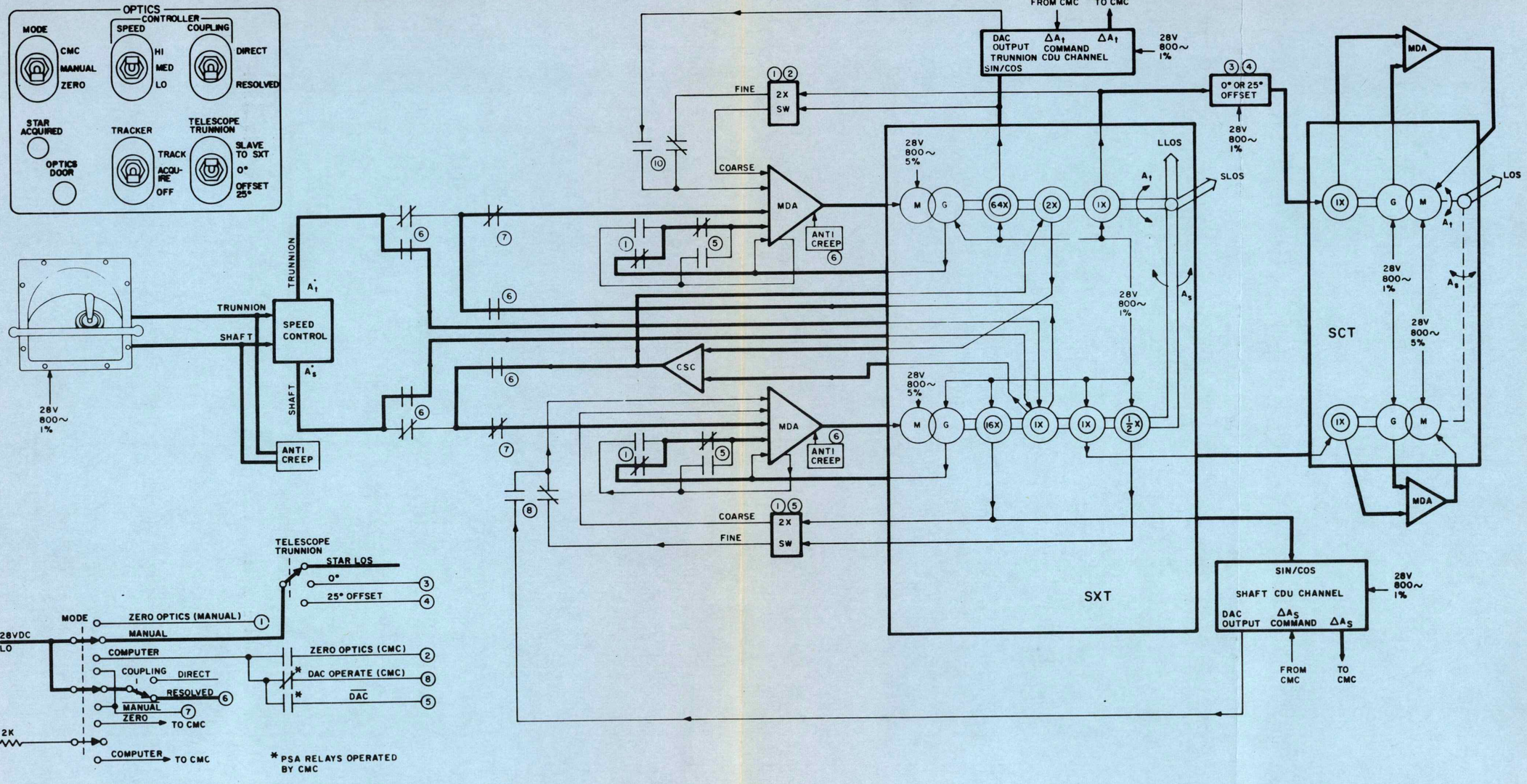
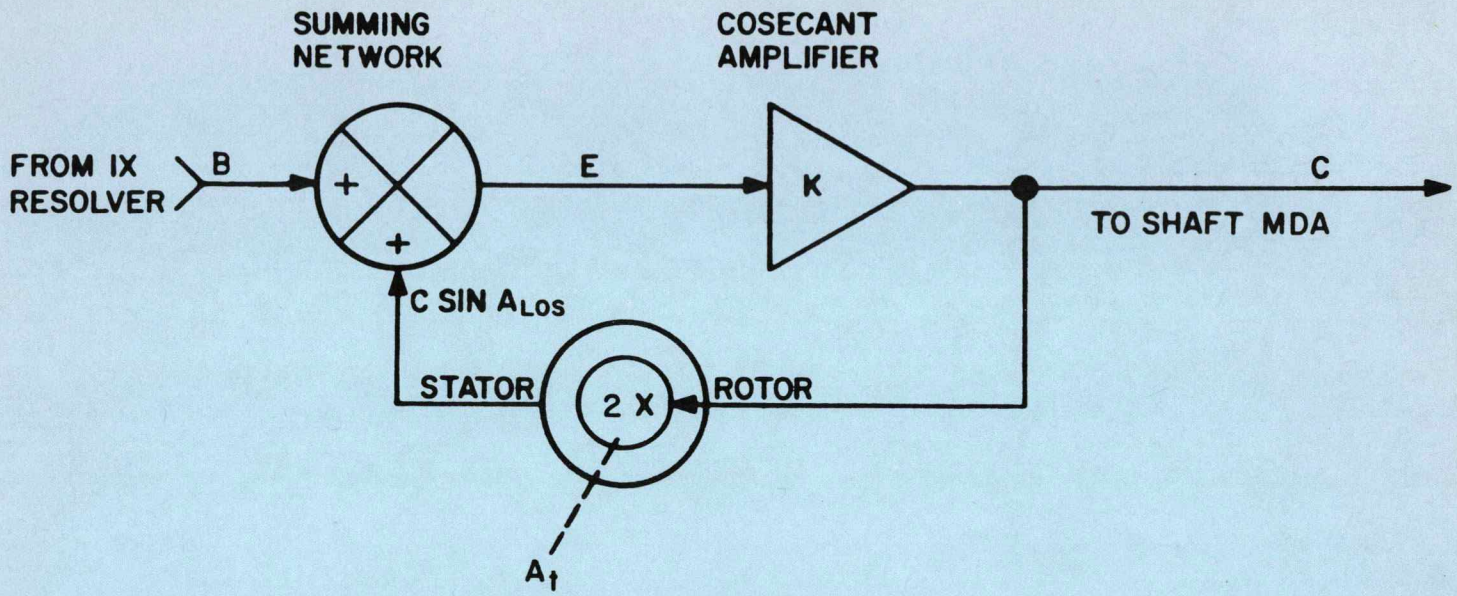


Figure 9-20. Manual Resolved Mode



$$B = \dot{A}_f \sin A_s - \dot{A}_s \cos A_s$$

$$E = B + C \sin A_{LOS}$$

$$C = KE$$

$$C = K(B + C \sin A_{LOS}) = KB + KC \sin A_{LOS}$$

$$C - KC \sin A_{LOS} = KB$$

$$C\ (1 - K \sin A_{LOS}) = KB$$

$$C = \frac{KB}{1 - K \sin A_{LOS}}$$

$$C = \frac{B}{1/K - \sin A_{LOS}} \quad (K \longrightarrow \infty)$$

$$C = \frac{-B}{\sin A_{LOS}} = \frac{\dot{A}_s \cos A_s - \dot{A}_f \sin A_s}{\sin A_{LOS}}$$

Figure 9-21. Gain Variation-Simplified Diagram

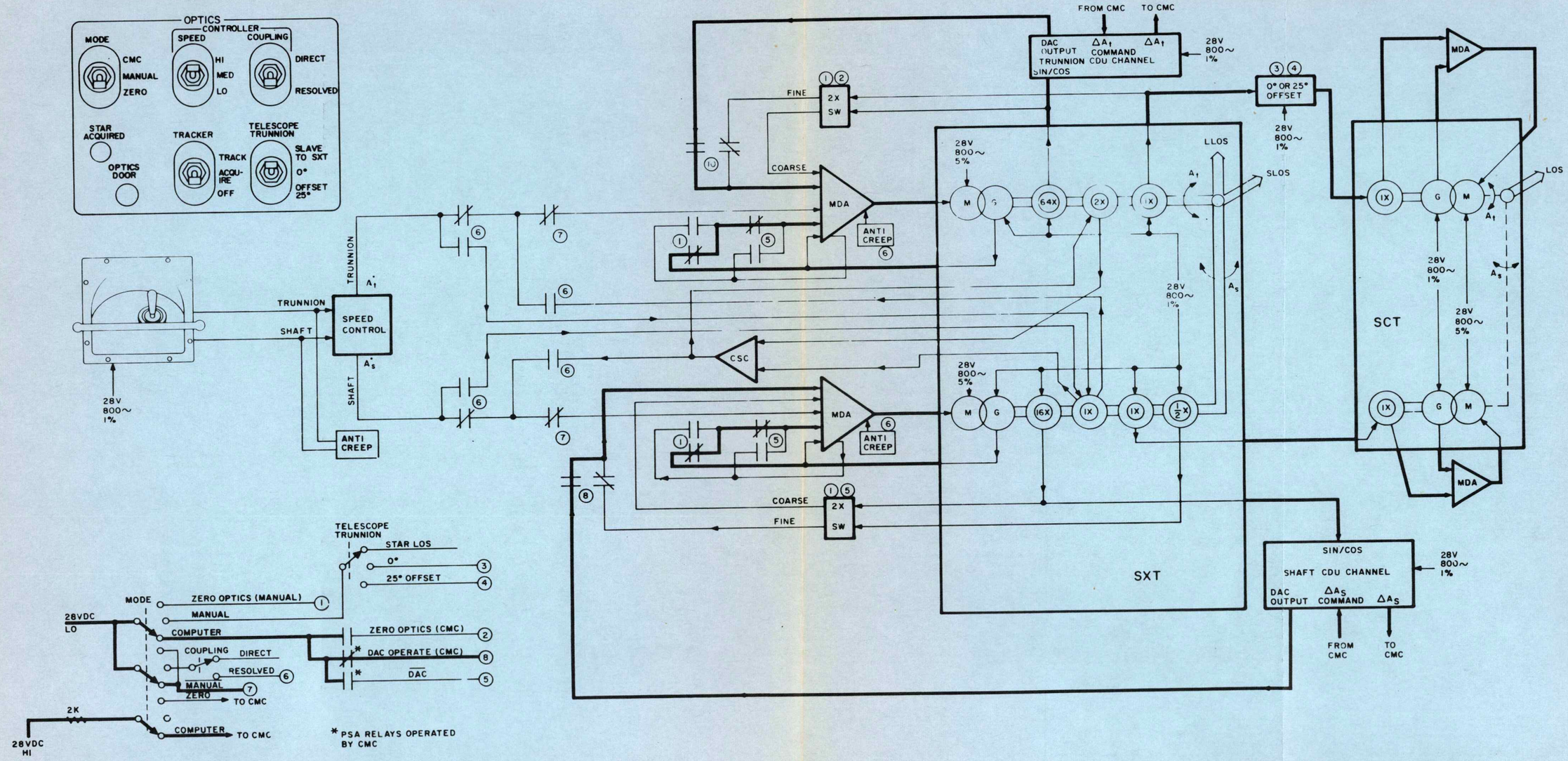


Figure 9-22. Computer Mode

attitude of the spacecraft from the position of the IMU gimbals and will therefore be able to calculate the position of the SXT axes required to acquire the star. The computer can then drive the shaft and trunnion of the SXT to the desired position via the DAC.

In the computer mode, the optics can be zeroed via control relays located in the PSA. The relays are selected by a CMC input into a relay driver in the PSA. These relays generally perform the same function as the indicator control panel switches. The computer controlled zeroing of the optics is the same as was described in paragraph 9.5.1. It should be noted that when the computer selects zero optics, it will also disconnect the DAC from the circuit.

9.6 SUMMARY

The optical assembly consists of an optical base upon which are mounted the scanning telescope and sextant.

Two channels of the CDU are required for use with the optical assembly along with portions of the Indicator Control Panel, and the PSA. Seals are required to seal the openings in the spacecraft pressure vessel that are provided for the sextant and scanning telescope.

The scanning telescope is a low power refracting optical instrument which provides a single 60^{o} field of view. It is used to locate and acquire the desired landmarks and stars on a gross basis. Two axes, the shaft axis and the trunnion axis, are used to define the movement of the SCT field of view.

The sextant is a high power (28X) optical instrument which is used for more accurate navigational sighting. The SXT has two visual lines-of-sight, the star LOS, and the landmark LOS, each of which has a 1.8^{o} field of view. The star and landmark images are made to appear in a single reticle pattern through a system of mirrors and lens. The landmark LOS is fixed parallel to the SXT shaft axis while the star LOS is moveable by rotation about both the shaft and trunnion axes.

The optical mechanization consists of SXT trunnion and shaft integrating servo loops which position the SXT lines of sight in response to inputs from either the hand controller or the CMC. In response to SXT movements, position servo loops drive the SCT trunnion and shaft. Analog data supplied to the optical channels of the CDU representing the SXT position is converted to digital data and sent to CMC. Controls located on the indicator control panel allows the selection of three primary modes; zero optics, manual control and computer control.

The purpose of the zero optics mode is to drive the optical equipment to an initial orientation prior to their utilization in taking an optical sighting. This allows the computer to clear the optical counters which are to be incremented with new data during the process of taking optical sightings.

The manual control allows the flight crew personnel to control the SXT operation via the hand controller. There are two variations of the manual operation, manual direct or manual resolved. In manual direct, the star image moves in the R-M coordinate system, while in the manual resolved mode, the star image moves in a fixed X - Y coordinate system.

The computer mode is selected by the astronaut to provide for computer control of the optics. The CMC can then zero the optics and drive the SXT.

SECTION X

THE COMPUTER SUBSYSTEM

INTRODUCTION

This section of the study guide briefly describes the CSS equipment to a functional block level. A brief description of the CSS organization and functional operation is also presented.

10.1 CSS PURPOSE

The computer subsystem is the control and computational center of the PGNCS. It performs the following functions:

a. Solves the guidance and navigation problems for all mission phases including Saturn Guidance take over capability during the boost phase.

b. Provides control information to the PGNCS, as well as other spacecraft systems.

c. Displays pertinent information to the astronaut and the ground when requested.

d. Provides a means by which the astronaut or ground control can directly communicate with the PGNCS.

e. Provides direct on-off control for the reaction control jets, and service propulsion engines.

f. Monitors its own operation and other PGNCS operations.

10.2 CSS EQUIPMENT

The CSS consists of the Command Module Computer (CMC) and two identical display and keyboards (DSKY's) (see figure 10-1). The CMC is located in the lower center of the lower display and control panel below the power and servo assembly. One DSKY is located on the lower display and control panel and is called the navigation panel DSKY. The other DSKY is located on the main display and control panel and is called the main panel DSKY.

10.2.1 CMC PHYSICAL DESCRIPTION. The CMC measures approximately 24 x 12.5 x 6 inches and weighs approximately 60 pounds. It consumes 10 watts of power during standby operation and 100 watts of power during normal operation. The CMC is mounted on a cold-plate base which is cooled by a water glycol solution flowing through it.

The CMC consists of a logic tray assembly and a memory tray assembly which are mounted back to back (figures 10-2 and 10-3). A tray assembly consists of a tray with the modules and connectors mounted on it. The modules contain the CMC's logic circuitry. The connectors provide the CMC with a hardware interface.

10.2.2 CMC USE. The CMC is a core memory, digital computer with two types of memory: fixed and erasable. The fixed memory permanently stores navigation tables, trajectory parameters, programs and constants. The erasable memory stores intermediate information.

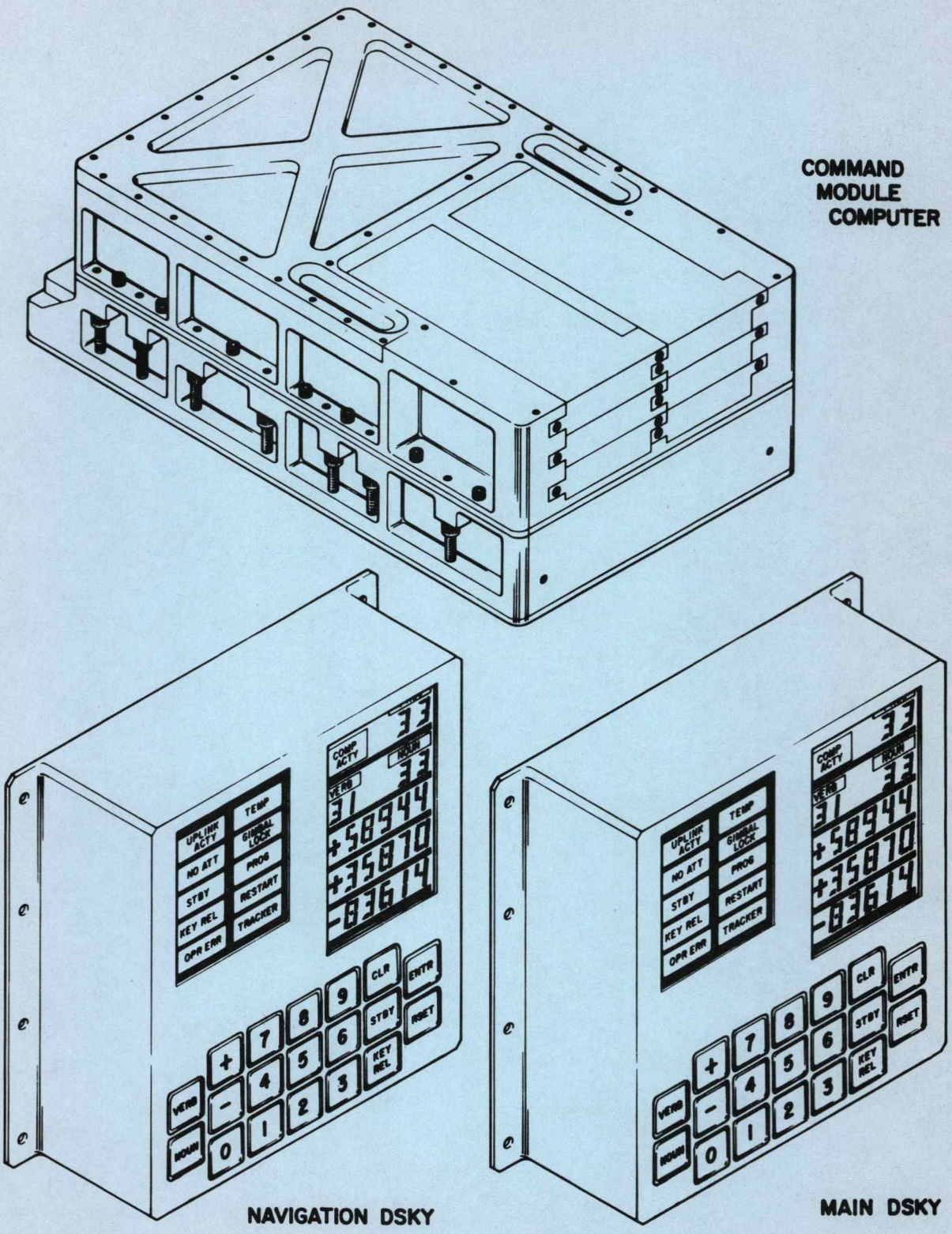


Figure 10-1. CSS Components

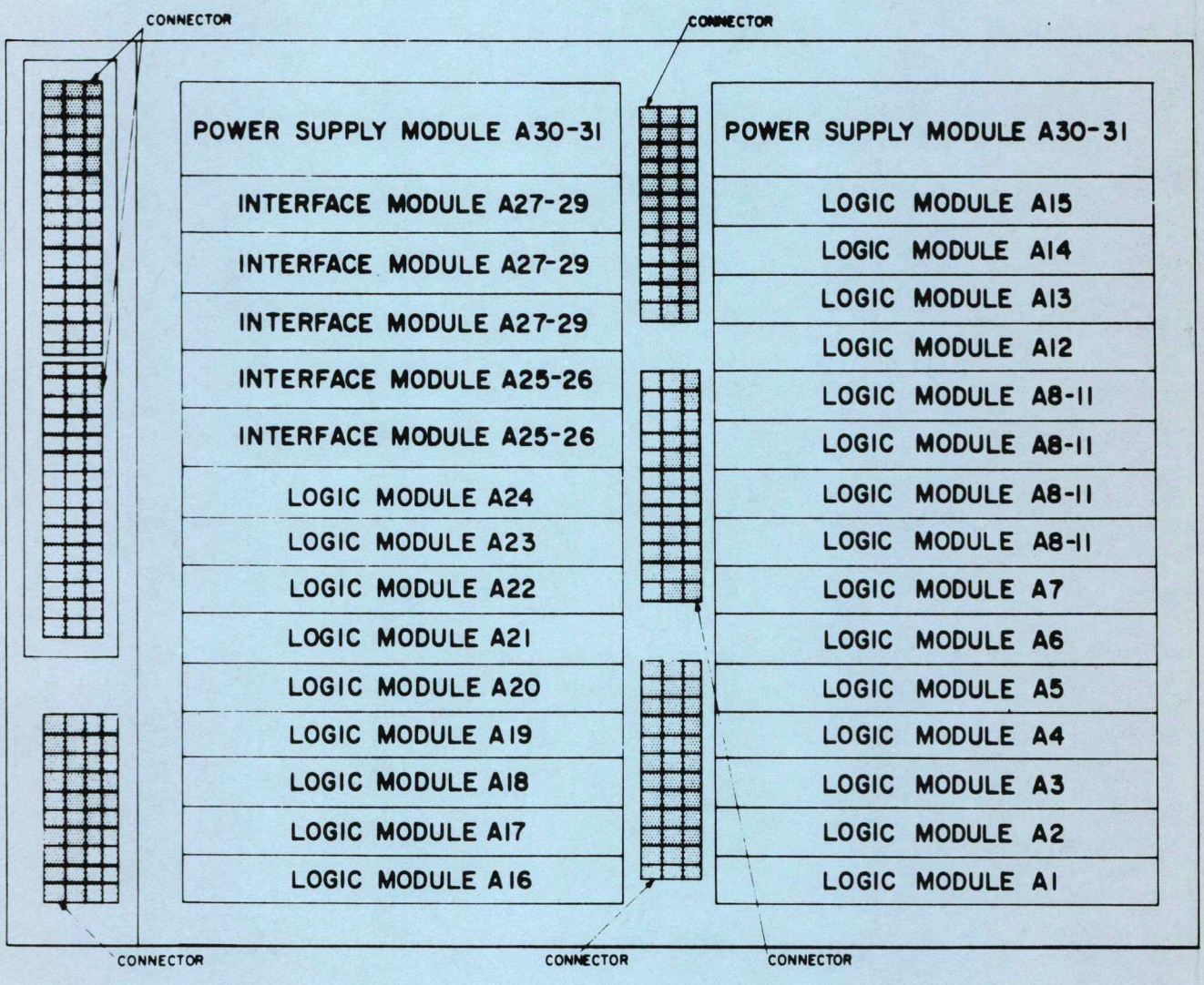


Figure 10-2. Logic Tray A

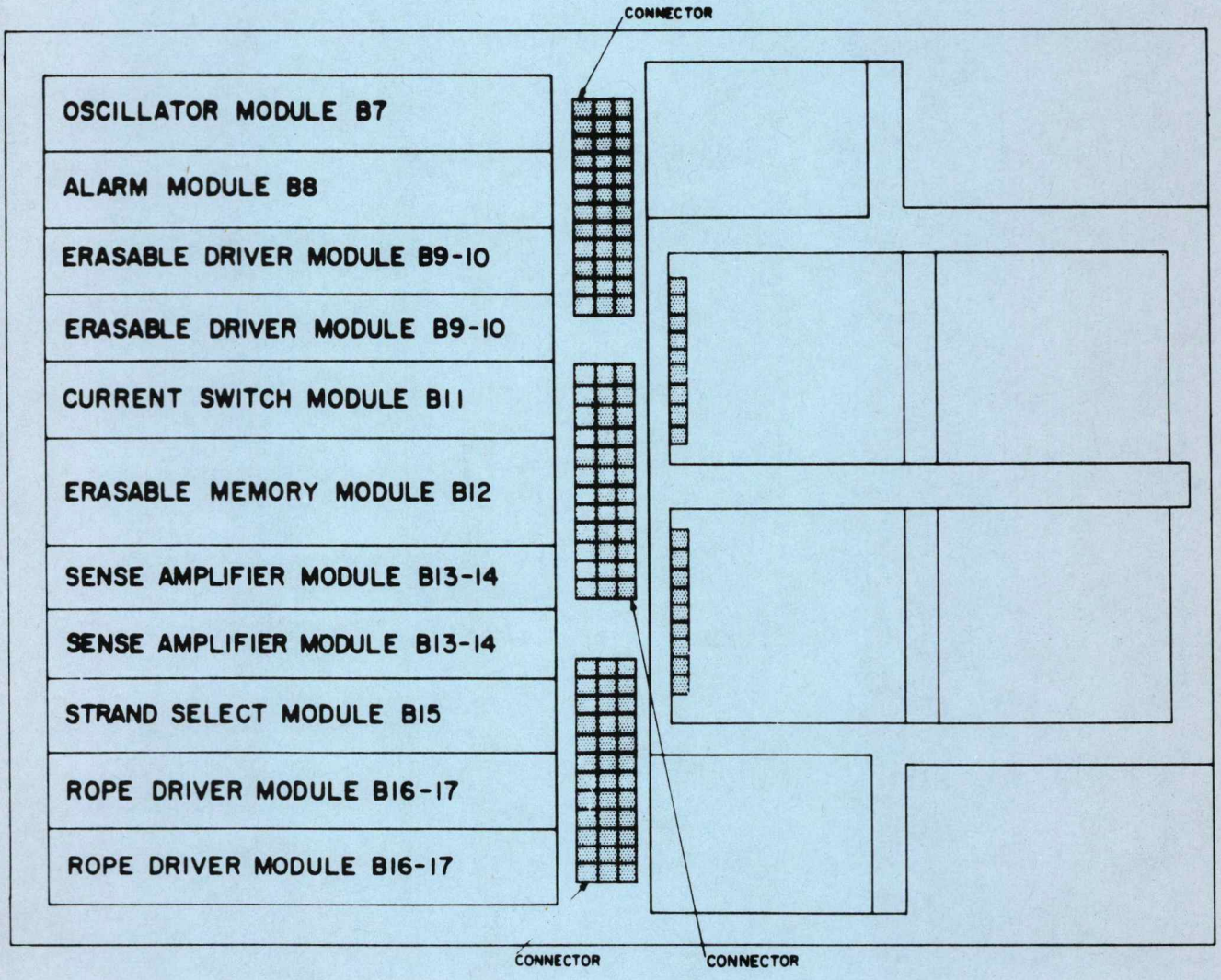


Figure 10-3. Memory Tray B

The CMC processes data and issues discrete control signals, both for the PGNCS and the other spacecraft systems. It is a control computer with many of the features of a general purpose computer. As a control computer, the CMC aligns the stable platform of the inertial measurement unit (IMU) in the inertial subsystem, positions the optical unit in the optical subsystem and issues control commands to the spacecraft. As a general purpose computer, the CMC solves guidance problems required for the spacecraft mission. In addition, the CMC monitors the operation of the PGNCS and and other spacecraft systems.

The CMC stores data pertinent to the flight profile that the spacecraft must assume in order to complete its mission. This data, consisting of position, velocity and trajectory information, is used by the CMC to solve the various flight equations. The results of various equations can be used to determine the required magnitude and direction of thrust required. Corrections to be made are established by the CMC. The spacecraft engines are turned on at the correct time, and steering signals are controlled by the CMC to reorient the spacecraft to a new trajectory, if required. The inertial subsystem senses acceleration and supplies velocity changes to the CMC for calculating the total velocity. Drive signals are supplied from the CMC to coupling data unit (CDU) and stabilization gyros in the inertial subsystem to align the gimbal angles in the IMU Error signals are also supplied to the CDU to provide steering capabilities for the spacecraft. CDU position signals are fed to the CMC to indicate changes in gimbal angles, which are used by the CMC to keep cognizant of the gimbal positions. The CMC receives mode indications and angular information from the optical subsystem during optical sightings. This information is used by the CMC to calculate present position and orientation and is used to refine trajectory information. Optical subsystem components can also be positioned by drive signals supplied from the CMC.

10.2.3 DSKY PHYSICAL DESCRIPTION. The DSKY measures approximately 8 x 8 x 7 inches and weighs about 17.5 pounds. Mounted on the back of the DSKY are six interchangeable driver modules, a 91 pin connector, a filler valve, and a power supply. The driver modules are used in the switching of the data displayed on the DSKY. The connector provides the interface between the DSKY and the CMC. The filler valve is used to pressurize the DSKY to one atmosphere. The power supply module supplies the voltage to light the DSKY indicators.

10.2.4 DSKY USE. The navigation DSKY located on the lower D & C panel and the DSKY located on the main D & C panel provides a two-way communications link between the astronaut and the CMC (see figure 10-1). Through this communications link, the following functions can be performed:

a. Loading of data into the CMC.

b. Display of data from the CMC and data loaded into the CMC.

c. Monitoring of data in the CMC.

d. Display of the CMC modes of operation.

e. System control by the initiation of subsystem and system testing and control of the system's major modes of operation.

f. Requests by the CMC to the system operator to perform actions.

The DSKY's consists of a keyboard, display panel, condition indicators, a power supply and a relay package (see figure 10-1). The keyboard provides the astronaut with the capability of inserting data into the CMC and initiating CMC operations. Through the keyboard, the astronaut can also control the ISS moding and some OSS moding. The DSKY display panel provides a visual indication of data being loaded into the CMC, the CMC activity and CMC program. The display panel also provides the CMC with a means of displaying or requesting data. The condition indicators display PGNCS status.

10.3 CSS ORGANIZATION

Figure 10-4 is a gross block diagram of the CSS. This diagram should be referenced while reading paragraphs 10.3.1 and 10.3.2.

10.3.1 CMC ORGANIZATION. The CMC is functionally divided into seven blocks:

1. Timer.
2. Sequence generator.
3. Central processor.
4. Memory.
5. Priority control.
6. Input - output.
7. Power.

10.3.1.1 Timer. The timer generates all the necessary synchronization pulses to insure a logical data flow from one area to another within the CMC. It also generates timing waveforms which are used by (1) the CMC's alarm circuitry and (2) other areas of the spacecraft for control and synchronization purposes.

10.3.1.2 Sequence Generator. The sequence generator directs the execution of machine instructions. It does this by generating control pulses which logically sequence data throughout the CMC. The control pulses are formed by combining the order code of an instruction word with synchronization pulses from the timer.

10.3.1.3 Central Processor. The central processor performs all arithmetic operations required of the CMC, buffers all information coming from and going to memory, checks for correct parity on all words coming from memory and generates a parity bit for all words written into memory.

10.3.1.4 Memory. Memory provides the storage for the CMC and is divided into two sections: erasable memory and fixed memory. Erasable memory can be written into or read from; its readout is destructive. Fixed memory cannot be written into and its readout is nondestructive.

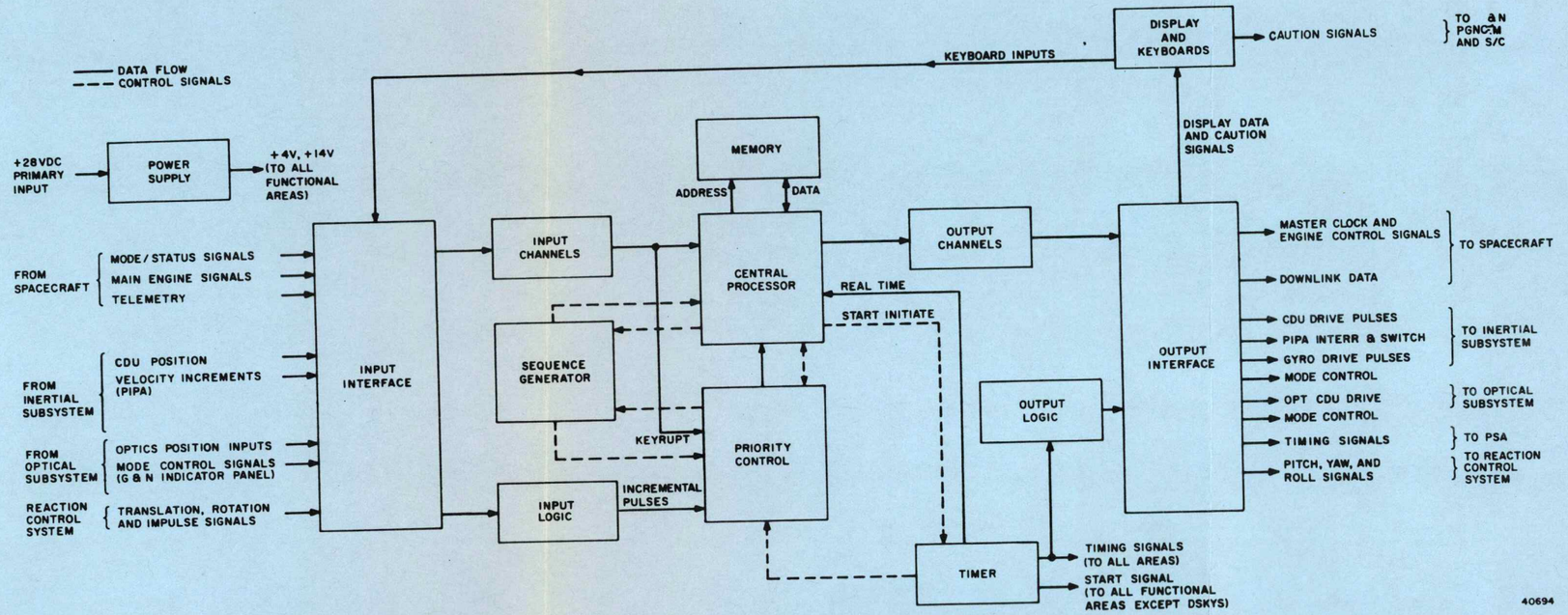


Figure 10.4 CSS Basic Flow

10.3.1.5 Priority Control. Priority control establishes a processing priority of operations which must be performed by the CMC. These operations are a result of conditions which occur both internally and externally to the CMC. Priority control consists of counter priority control and interrupt priority control. Counter priority control initiates actions which update counters in erasable memory. Interrupt priority control transfers control of the CMC to one of several interrupt subroutines stored in fixed memory.

10.3.1.6 Input - Output. The input - output section routes and conditions signals between the CMC and other areas of the spacecraft.

10.3.1.7 Power. This section provides voltage levels necessary for the proper operation of the CMC.

10.3.2 DSKY ORGANIZATION. The DSKY is functionally divided into three blocks:

1. Keyboard.
2. Display indicators.
3. Condition indicators.

10.3.2.1 Keyboard. The keyboard consists of ten numerical keys (pushbuttons), two sign keys, and seven instruction keys. The keys are used to enter data into the computer, place the computer in standby mode or remove it from standby, or release the DSKY so the computer can display data to the astronaut.

10.3.2.2 Display Indicators. The DSKY contains 21 digit display indicators and three sign display indicators. The program, noun, and verb displays each contain two digit positions. Each of the three data displays contains a sign display and five digit display indicators.

10.3.2.3 Condition Indicators. The DSKY contains 14 condition indicators which indicate computer mode of operation and some computer problems and PGNCS malfunctions. Four of the 14 condition indicators are not used in the CM application of the DSKY's which is identical to the LM DSKY.

10.4 COMPUTER SUBSYSTEM OPERATIONS

The CSS interfaces with the ISS, OSS, astronaut and certain spacecraft systems. These interfaces are described in the paragraphs below.

10.4.1 CSS/ISS OPERATIONS. The CSS receives changes in IMU gimbal angles and changes in velocity from the ISS. These changes are accumulated in the CMC. The IMU gimbal positions are used by the CMC to monitor platform orientation. The velocity changes are used by the CMC to calculate the velocity and, by integration, the position of the spacecraft. The CMC also commands ISS moding and monitors certain subsystem components for failures. The components monitored are:

a. CDU inertial channels
b. Accelerometer loops
c. Stabilization loops
d. Power supplies

Inertial subsystem moding, with the exception of IMU cage, is controlled by the computer by the generation of commands to the inertial CDU. The discrete commands issued are CDU Zero, Coarse Align, Error Counter Enable, And SIVB takeover. The generation of the discretes is done automatically through a computer program or by astronaut command through operation of either DSKY. During the coarse align mode of operation the computer provides digital inputs to the Coupling Data Unit. The CDU converts the digital command to an analog signal which is used to reposition the gimbals. During Fine Align the computer provides torquing pulses to the Apollo II IRIG torque ducosyns for fine alignment of the stable platform. The computer also supplies frequency references to the CDU and to the inertial subsystem power supplies.

10.4.2 CSS/OSS OPERATIONS. The optical subsystem is used in conjunction with the computer to determine spacecraft position, velocity, attitude and alignment angles for the inertial subsystem. The primary interface between the optical units and the CSS is via the CDU. Upon completion of a navigation sighting, the sextant trunnion and shaft angles are coupled, via the CDU, to the computer. The computer program uses these angles and time to determine spacecraft position, velocity and attitude. In the event that an IMU alignment is to follow the optical sighting, the program determines the angular corrections necessary to align the IMU to the inertial reference frame.

Under certain combination of OSS control switches on the G&N Indicator Control Panel, it is possible for the computer to control the moding and the positioning of the optics. The astronaut must complete the navigation sighting after the computer positions the optics by tracking and marking on the celestial objects.

The computer monitors the optical subsystem modes of operation to determine what computer operation shall be performed. The mode Zero in the OSS, when manually selected, causes the optics angle counters in the CMC to be zeroed. The computer, in addition to monitoring or controlling the optical subsystem operation, provides timing pulses as references to the OSS power supplies.

10.4.3 CSS/SPACECRAFT. The functions of the PGNCS is to provide guidance, navigation and control for the Apollo spacecraft. Because of this increase in scope, over previous Apollo G&N Systems, the interface with the spacecraft has expanded and now includes the following items:

10.4.3.1 CSS/Saturn Instrumentation Unit. The CSS receives indications of Saturn lift-off and guidance release from the Instrumentation Unit. The receipt of the guidance release discrete causes the CMC to discontinue the gyro-compassing routine and allows the stable member to become inertially referenced. The lift-off signal causes the CMC to begin computing velocity, position and attitude of the spacecraft. The computer compares these data with a reference trajectory, the difference between the two are utilized to determine the need for PGNCS takeover of Saturn guidance. In the event that the crew selects the PGNCS to control Saturn guidance, the computer calculates steering errors, which are converted from digital to analog by the CDU, issues start injection sequence, and Saturn engine on/off commands all of which are coupled to the Saturn IU.

10.4.3.2 CSS/Central Timing Equipment (CTE). The Command Module Computer provides a 1.024 MC frequency reference to the CTE. This enables all command module timing to be referenced to a single time standard.

10.4.3.3 CSS/Communications and Instrumentation System (C and IS). The CSS receives uplink telemetry data and downlink telemetry synchronization pulses from the C and IS. The uplink telemetry data is in the form of five bit codes which are identical to the key codes provided by the DSKY's. The operation of the CSS then can be controlled from the ground station via the uplink telemetry. There are two methods of inserting the uplink telemetry data into the CMC One method is to insert all the uplink data required and thereby exert complete control of the CSS from the ground station. The other method is to insert all the uplink data except the final command for the CMC to process the data. The astronaut then has the option of using the uplink data or not. This data is displayed to the astronaut on the DSKY display panels for his inspection. The downlink telemetry sync pulses are used to regulate the gating of downlink telemetry data to the C and IS. The C and IS receives downlink telemetry data from the CSS. This data can be transmitted at 10 words per second or at 50 words per second (1.6 K bits per second or 51.2 K bits per second, respectively).

The ground station uses part of this downlink data to duplicate the displays and DSKY inputs that have occurred in the spacecraft. The ground station can send commands and data to the CMC in a format similar to the DSKY inputs.

10.4.3.4 CSS/Mission Sequencer. The CSS receives an indication of command module-service module separation and of SIVB separation from the mission sequencer.

10.4.3.5 CSS/Spacecraft Controls. The CSS interface with the spacecraft controls is primarily on-off switching of DC voltages. The following switches on the Main D and C panel have direct effects on the operation of the PGNCS.

a. S/C control of Saturn - Initiates a computer program for boost guidance.

b. ΔV CG Switch - Allows the computer to compensate for the change in the spacecraft center of gravity when the LM is attached. This information is necessary for midcourse correction maneuvers.

c. SC Control - source switch - Selects computer control of the propulsion system.

d. SPS Thrust - Indicates to the CMC that the SPS engine start checklist has been completed and the SPS is ready for thrusting.

e. SC Control - CMC switch - A three position switch - Hold, Free and Auto indicating to the CMC what type of attitude control it should exercise.

The CMC also has inputs from the rotation and translation controls for pilot initiated attitude and positional maneuvers. For attitude control during optical sightings, the navigator utilizes the minimum impulse controller which also has direct inputs to the CMC. For spacecraft maneuvers, whether automatically or manually commanded, the computer issues on/off discretes to the 16 RSC jets on the service module or the 12 RCS jets on the command module. During PGNCS controlled thrusting maneuvers using the SPS, the computer calculates steering signals and issues SPS engine on/off commands.

10.4.4 CSS/ASTRONAUT. The CSS interface with the astronaut is through the DSKY's. The operator of the DSKY can communicate with the CMC by the depression of a sequence of keys on the DSKY keyboard. Each depression of a key inserts a five bit code into the CMC. The CMC responds by returning a code to the DSKY, which controls the display on a particular display panel, or by initiating a CMC operation. The CMC is also capable of initiating a display of information or a request for some action to the operator under its own initiative.

The basic communication language used in the interchange of information is a pair of words known as the VERB and NOUN. Each of these words is represented by a two digit octal number. The VERB specifies that an action of some sort is to be performed while the NOUN, used in conjunction with the VERB, specifies on what the action is to be performed.

10.5 CMC INFORMATION FLOW

The main functions of the CMC are implemented through the execution of programs stored in memory. Programs are written in basic instructions. The order code defines data flow within the CMC. The relevant address selects data that is to be used for computations. The order code of each instruction is entered into the sequence generator which controls data flow and produces a different sequence of control pulses for each instruction. Each instruction is followed by another instruction. In order to specify the sequence in which consecutive instructions are to be executed, the instructions are normally stored in successive memory locations. By adding +1 to the address of an instruction being executed, the address of the next instruction is obtained. Execution of an instruction is complete when the order code of the next instruction is transferred to the sequence generator and its relevant address is in the central processor.

The central processor consists primarily of flip-flop registers. It performs arithmetic operations and data manipulations on information accepted from memory, the input registers and priority control. Arithmetic operations are performed using the binary ones complement numbering system. All operations within the central processor are performed under control of pulses generated by the sequence generator.

The CMC has provisions for handling certain priority programs. Before a priority program can be executed, the current program must be interrupted; however, certain information about the current program must be preserved. This information includes the program counter contents and any intermediate results contained in the central processor. The program counter is a register in the central processor which contains the address of the next instruction to be performed. The priority control produces an interrupt request signal which is sent to the sequence generator. This signal causes the execution of an instruction that transfers the current contents of the program counter and any intermediate results to memory. In addition, the control pulses transfer the priority program address to the central processor and then to memory. As a result, the first instruction word of the priority program is entered into the central processor from memory and the execution of the priority program is begun. The last instruction of each priority program restores the CMC to normal operation if no other interrupt request is present. This is done by transferring the previous program counter and intermediate results from their storage locations in memory back to the central processor.

Certain data pertaining to the flight of the spacecraft is used to solve the guidance and navigation problems required for the Apollo Mission. This data which includes real time, acceleration and IMU gimbal angles (via the CDU) is stored in the erasable memory counters which are updated as soon as new data becomes available. An incrementing process which changes the contents of the counters is implemented by priority control between the execution of subinstructions. Data inputs to counter priority control are called incremental pulses. Each incremental pulse produces a counter address and a priority request signal which is sent to the sequence generator where it functions as an order code. The control pulses produced by the sequence generator transfer the counter address to memory. In addition, the control pulses enter the contents of the addressed counter into the central processor. The contents of the counter are then incremented or decremented.

Real time plays a major role in solving guidance and navigation problems. Real time is maintained within the CMC by the main time counter. The main time counter consists of two erasable memory counters. Incremental pulses are produced in the timer and sent to priority control for incrementing the main time counter every 10 milliseconds.

Continuous drive pulses originate in the CMC's timer. Rate signals, which are bursts of these drive pulses, are used to drive the inertial CDU channels, the gyros and the optical CDU channels. Rate signals are also used for controlling the attitude of the spacecraft. The number of pulses in each burst and occurrence of each burst are controlled by the program. The destination of the various rate signals, as well as the type of rate signals, is also selected by the program. The continuous drive signals are also sent to other areas of the spacecraft where they are used for synchronization and control purposes.

The uplink word from the spacecraft telemetry system is supplied to the CMC as incremental pulse inputs to priority control. As these words are received, priority control produces the address of the uplink counter in memory and requests the sequence generator to execute the instructions which perform the serial-to-parallel conversion of the uplink word. When the serial-to-parallel conversion is complete, the parallel word is transferred to a storage location in memory by the UPRUPT subroutine.

With the DSKY keyboard, the astronaut can load information into the CMC, receive and display information contained in the CMC and initiate any program stored in memory. A keycode is assigned to each keyboard pushbutton. When a keyboard pushbutton on either DSKY is depressed, the keycode is produced and sent to the CMC where it produces the address of a priority program (KEYRUPT) stored in memory and a priority request signal which is sent to the sequence generator. The priority request signal functions as an order code and initiates an instruction for interrupting the program in progress and executing the priority program stored in memory. A function of this program is to decode and process the keycode. A number of keycodes are required to specify an address or a data word. The program initiated by a keycode converts the information from the DSKY keyboard to a coded display format which is transferred to the display portion of the DSKY. The display informs the astronaut that the keycode was received, decoded and properly processed by the CMC.

Word formats, addition schemes, logic implementation, and hardware registers are described in preparation for a detailed description of computer organization.

CMC characteristics are summarized in table 10-1.

10.6 WORD FORMATS

All words are 16 bits long in the computer. There are two basic types of words: data words and instruction words. The format of the words depend on where the words are located. Figure 10-5 shows the word formats in memory (storage) and in the central processor registers.

In memory, data words contain a parity bit, fourteen magnitude bits and a sign bit. A binary "1" in the sign bit indicates a negative number, a binary "0" in the sign bit indicates a positive number. When located in the central processor, bits 1 through 14 are the magnitude bits, bit 15 is the "uncorrected sign" bit, and bit 16 is the sign as before. The "uncorrected sign" bit is used to enable an overflow detection without destroying the sign bit when two numbers are manipulated.

Parity bits are only included in words which are stored in memory.

An instruction word in memory contains a 12 bit address code and a 3 bit order code. Bits 10 through 12 are sometimes used to extend the order code when the work is transferred to the SQ register. The address code normally calls out the location of a word in memory or the central processor. The order code represents an operation which is to be performed on the data whose location is defined by the address code.

10.7 ADDITION SCHEMES

The CMC performs angular data addition and non-angular data addition. The processes involved with these manipulations differ slightly.

10.7.1 NON-ANGULAR DATA ADDITION.

The CMC uses the binary ONE's complement numbering system. In this system, a negative number is the complement of the corresponding positive number. Assume that the CMC uses five bit data words. Figure 10-6 shows how +7 through -7 would be represented by words in memory and the central processor.

Table 10-1. CMC Characteristics

Characteristics	Description
Computer type	Automatic, electronic, digital, general purpose and control
Internal transfer	Parallel
Memory	Random access
Erasable	Coincident current core, capacity = 2048 words
Fixed	Core-rope, capacity = 36,864 words
Word length	Sixteen bits
Number system	Binary ONE's complement
Circuitry type	Flat pack NOR micrologic
Machine instructions	56 total
Regular	42 total
Involuntary	9 total
Peripheral	5 total
Interrupt options	10 total
Memory cycle time (MCT)	12 μ seconds
Add time	24 μ seconds
Multiply time	48 μ seconds
Number of counters	29 total
Downlink telemetry	Asynchronous to computer timing.
Basic clock oscillator	2.048 mc
CMC power supplies	One +4 volt switching regulator
	One +14 volt switching regulator
Logic	Positive
Parity	Odd

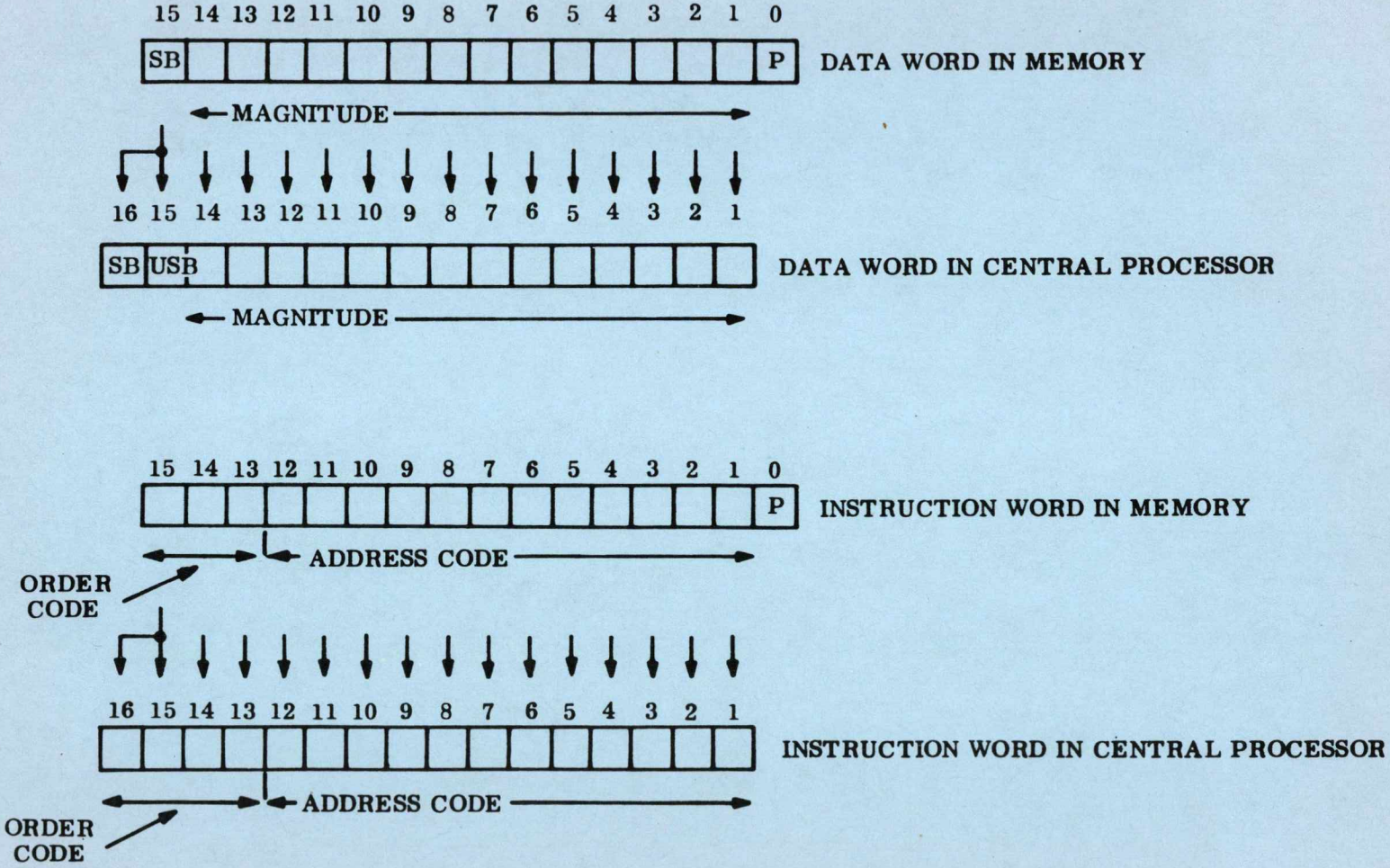


Figure 10-5. Word Formats in Memory and Central Processor

SB	M	M	M	P	
0	1	1	1	0	+7
0	1	1	0	1	+6
0	1	0	1	1	+5
0	1	0	0	0	+4
0	0	1	1	1	+3
0	0	1	0	0	+2
0	0	0	1	0	+1
0	0	0	0	1	+0
1	1	1	1	1	-0
1	1	1	0	0	-1
1	1	0	1	0	-2
1	1	0	0	1	-3
1	0	1	1	0	-4
1	0	1	0	1	-5
1	0	0	1	1	-6
1	0	0	0	0	-7

MEMORY

SB	OUB	M	M	M	
0	0	1	1	1	+7
0	0	1	1	0	+6
0	0	1	0	1	+5
0	0	1	0	0	+4
0	0	0	1	1	+3
0	0	0	1	0	+2
0	0	0	0	1	+1
0	0	0	0	0	+0
1	1	1	1	1	-0
1	1	1	1	0	-1
1	1	1	0	1	-2
1	1	1	0	0	-3
1	1	0	1	1	-4
1	1	0	1	0	-5
1	1	0	0	1	-6
1	1	0	0	0	-7

CENTRAL PROCESSOR

Figure 10-6. Number Representation

The CMC can only add. In order to subtract, the CMC adds the complement of a number. Multiplications are performed by successive additions and shiftings; divisions are performed by successive additions of complements and shiftings.

All adding is performed in the central processor. The CMC's consists of the X, Y and U registers. The X and Y registers are the adder's input registers, i.e., the registers to which the augend and addend are applied. The U register is the adder's output register, i.e., the register at which the sum is found. An overflow occurs during addition when the overflow/underflow bit (OUB) of the U register is a logic 1 and the sign bit (SB) is a logic 0; an underflow occurs when the overflow/underflow bit is a logic 0 and the sign bit is a logic 1.

Figure 10-7 shows the various addition schemes employed by the CMC for manipulating non-angular data. Note in the first case of Example C that the CMC performs (+5) + (-3) and not (+5) - (+3). Example A shows a case of overflow. Example B illustrates end-around-carry and underflow. End-around-carry is a characteristic of the binary ONE's complement numbering system: it is the result of a carry being generated during the addition of the last two binary bits. When this happens, +1 is added to the LSD of the subsum and the sum is then formed. Underflow results when a sum is negative and has a magnitude larger than that expressable with the assigned magnitude bits. End-around-carry and overflow/underflow conditions are mechanized by the CMC. When overflow/underflow occurs, a special counter is incremented or decremented to prevent loss of data.

Summarizing: If the SB and OUB of the sum are identical, then the sign of the sum is determined by the SB, and the magnitude of the sum is determined by the assigned magnitude bits, i.e., the OUB is not taken into consideration; if the SB and OUB of a sum are not identical, then the sign of the sum is determined by the SB, and the magnitude of the sum is determined by the assigned magnitude bits and the OUB. In this case, the OUB becomes the MSD.

One important fact should be noted: the configuration of the magnitude 0 (zero) is not unique but has signs associated with it, i.e., +0 = 00000 and -0 = 11111 in the central processor registers.

10.7.2 ANGULAR DATA ADDITION. The CMC receives pulses indicative of angular displacements from the optical and inertial CDU channels. These pulses enter the CMC through the input interface and are then applied to the counter priority control circuitry.

If the CMC receives a $\Delta\theta$ pulse from the CDU, the contents of the counter in erasable memory associated with this CDU channel will be incremented or decremented by 1. These pulses arrive one at a time; therefore, the CMC only has to add +1 or -1 to the contents of the proper counter. This addition is performed in the adder of the central processor, i.e., the same place where non-angular data is added.

There is no minus sign associated with angular data, i.e., all angles are considered to be positive. Assume five bit counters in erasable memory including the sign bit and parity bit; therefore, four bits are available to determine the granularity of angular data: three magnitude bits and the sign bit. Using four bits, the granularity of a $\Delta\theta$ pulse would be 22.5^{o}, i.e., $360^{o}/16$.

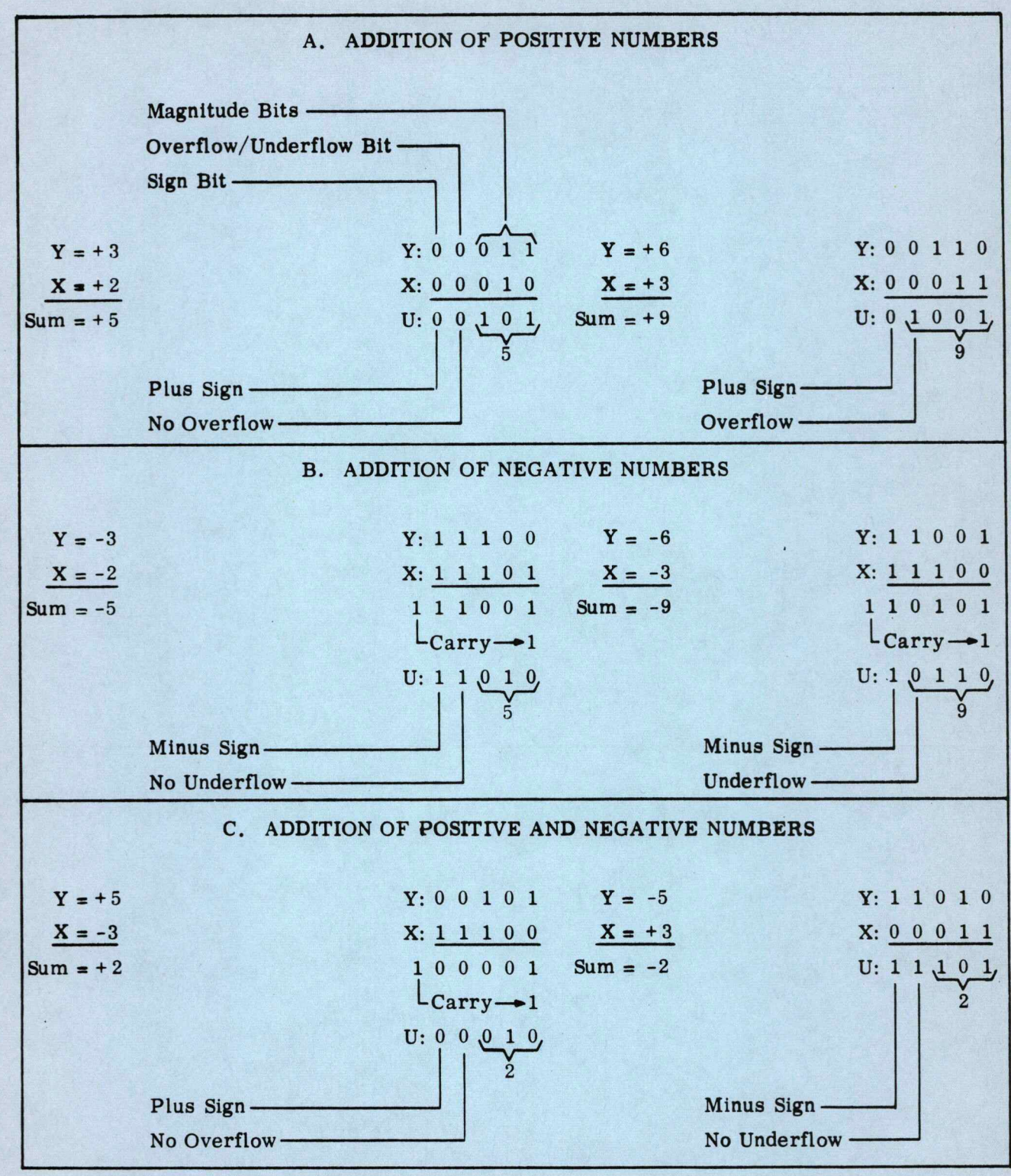


Figure 10-7. Addition Schemes for Non-Angular Data

Table 10-2 shows the 16 possible counter configurations using a five bit counter. Each configuration corresponds to an angular displacement range. For instance, if a CDU read counter were cleared and then incremented to indicate $+83^{o}$, the counter associated with that CDU channel would have a configuration of 00111. This would mean that the CMC had received three $+\Delta\theta$ pulses from the CDU read counter.

The following two examples functionally illustrate the addition of angular data.

Addition of a $+\Delta\theta$ Pulse (figure 10-8)

1. Assumptions:

   A. X ISS CDU counter has a configuration of 01110.

   B. A $+\Delta\theta$ pulse is generated by the X ISS CDU channel and sent to the CMC.

2. Operation:

   A. The Y register is cleared, i.e., it is set to 00000.

   B. The content of the X ISS CDU counter is transferred from erasable memory to the X register of the adder. The content of the X register after this transfer is, therefore, 00111.

   C. A forced end-around-carry is generated.

   D. The contents of the X register, Y register and the +1 produced by the forced end-around-carry are all added together.

   E. The content of the U register is 01000. It is now time to send the updated information back to the X ISS CDU counter in erasable memory.

   F. The information in the SB of the U register is inhibited from entering the sign bit of memory. Instead, the OUB of the U register is sent to the sign bit of the memory location.

   G. The OUB and three magnitude bits of the U register are transferred to the sign bit and three magnitude bits of the X ISS CDU counter. The parity block generates the proper parity and sends it to the parity bit of the counter.

Addition of a $-\Delta\theta$ Pulse (figure 10-9)

1. Assumptions:

   A. X ISS CDU counter has a configuration of 00010.

   B. A $-\Delta\theta$ pulse is generated by the X ISS CDU channel and sent to the CMC.

2. Operation:

   A. The Y register is set to 11110.

Table 10-2. Angular Data Representation

Angle In Degrees	Word In Memory					Word in Central Processor				
	SB	MAG	MAG	MAG	P	SB	OUB	MAG	MAG	MAG
0	0	0	0	0	1	0	0	0	0	0
22.5	0	0	0	1	0	0	0	0	0	1
45	0	0	1	0	0	0	0	0	1	0
67.5	0	0	1	1	1	0	0	0	1	1
90	0	1	0	0	0	0	0	1	0	0
112.5	0	1	0	1	1	0	0	1	0	1
135	0	1	1	0	1	0	0	1	1	0
157.5	0	1	1	1	0	0	0	1	1	1
180	1	0	0	0	0	1	1	0	0	0
202.5	1	0	0	1	1	1	1	0	0	1
225	1	0	1	0	1	1	1	0	1	0
247.5	1	0	1	1	0	1	1	0	1	1
270	1	1	0	0	1	1	1	1	0	0
292.5	1	1	0	1	0	1	1	1	0	1
315	1	1	1	0	0	1	1	1	1	0
337.5	1	1	1	1	1	1	1	1	1	1
0 or 360	0	0	0	0	1	0	0	0	0	0

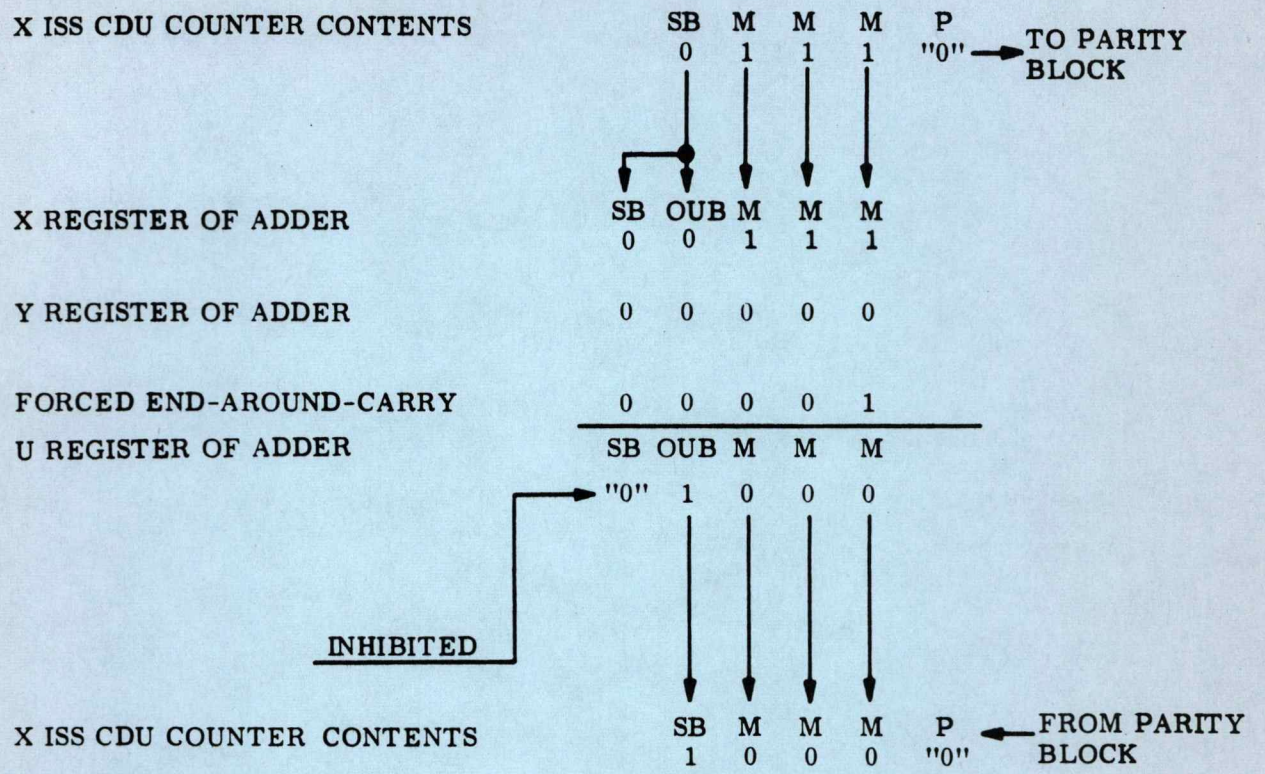


Figure 10-8. $+\Delta\theta$ Pulse Addition

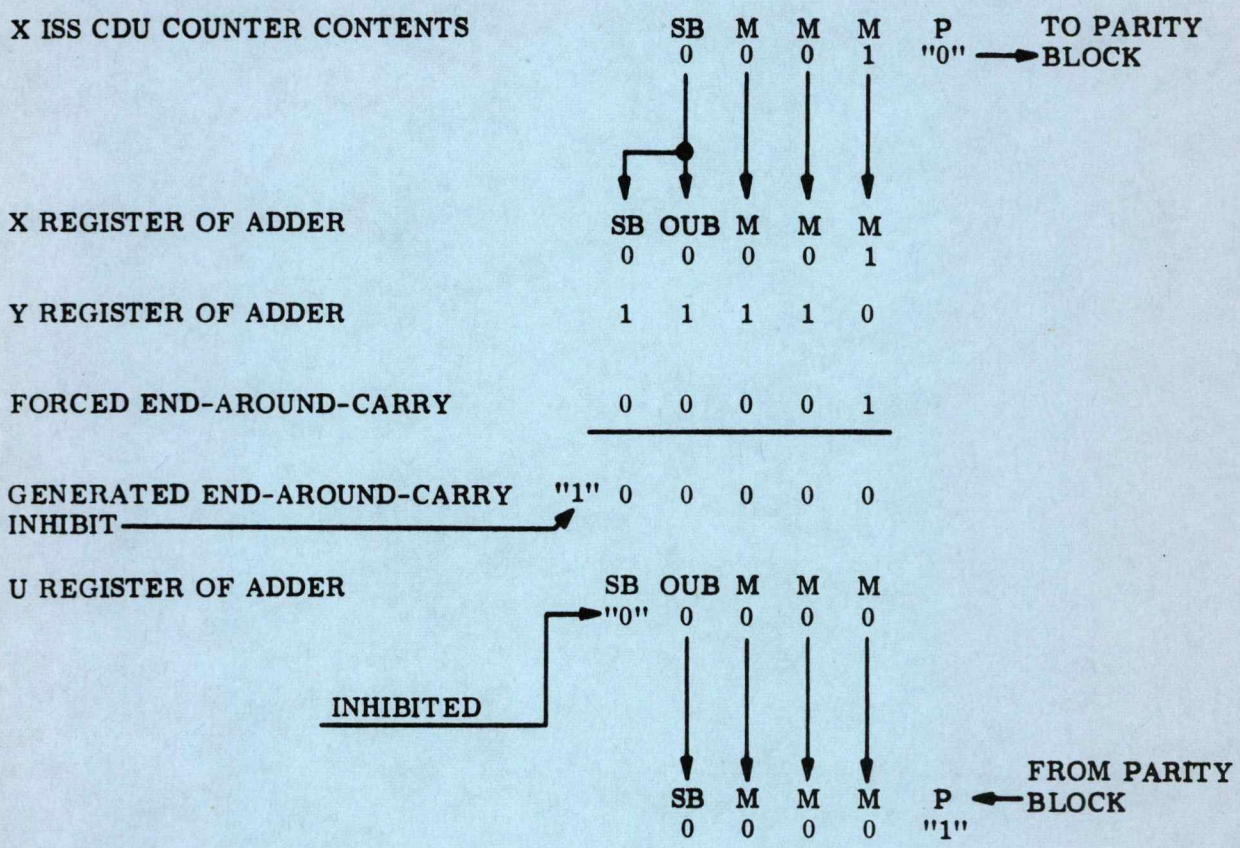


Figure 10-9. $-\Delta\theta$ Pulse Addition

B. The content of the X ISS CDU counter is transferred from erasable memory to the X register of the adder. The content of the X register after the transfer is, therefore, 00001.

C. A forced end-around-carry is generated.

D. The contents of the X register, Y register and the +1 produced by the forced end-around-carry are all added together. Note that the end-around-carry generated by this addition is inhibited because one end-around-carry has already been produced.

E. The content of the U register is 00000. It is now time to send the updated information back to the X ISS CDU counter in erasable memory.

F. The information in the SB of the U register is inhibited from entering memory.

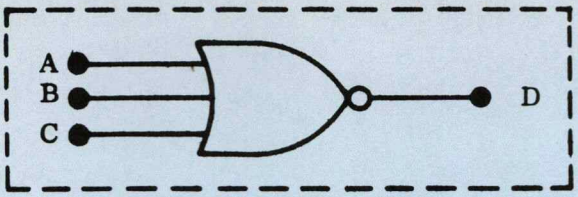
G. The OUB and three magnitude bits of the U register are transferred to the SB and three magnitude bits of the X ISS CDU counter. The parity block generates the proper parity and sends it to the parity of the counter.

10.8 LOGIC IMPLEMENTATION

All logic sticks in the CMC are built up from "micrologic" elements. In the CMC, the prime micrologic element used is a three-input NOR gate. The circuitry for two of these elements is diffused onto a single wafer which is contained in a flat pack. Figure 10-10 shows the accepted symbol for a single NOR gate and the associated truth table. The truth table defines the output logic level (1 or 0) for all possible input combinations. The CMC uses positive logic throughout. A logic 1 is 4 volts, a logic 0 is 0 volts. When inputs A, B or C equal a logic one in the NOR circuit, the associated transistor is biased to an on condition. This results in a path for current flow to ground. The output then falls to nearly 0 volts (logic 0) as indicated by the truth table. If all three inputs equal 0, the output D becomes logic 1.

Although the logic circuits of the CMC are comprised entirely of CMC gates, it is convenient to use the standard AND and OR logic blocks to simplifiy the presentation of later material. Figures 10-10 and 10-11 show the OR, AND, FLIP-FLOP and EXCLUSIVE OR circuits. The NOR gates within the dotted lines show the exact mechanization of the circuits in the simplified systems. The reader should compare the truth tables included in the diagrams with the circuits. Note that a one input NOR gate is just an inverter (figure 10-10).

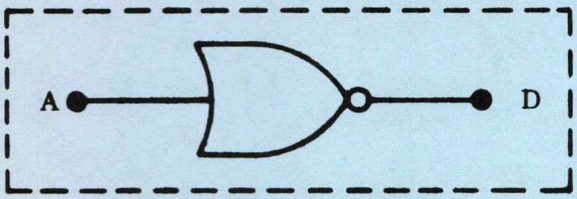
Figure 10-11 shows an EXCLUSIVE OR gate. Its distinguishing feature is that when both inputs are logic one's, the output is a logic zero. A standard OR gate has a logic one output when any or all inputs are logic one's.



"NOR" GATE, SYMBOL

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
D	1	0	0	0	0	0	0	0

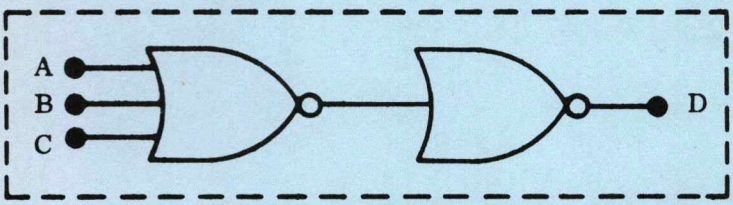
TRUTH TABLE



INVERTER, SYMBOL

A	0	1
D	1	0

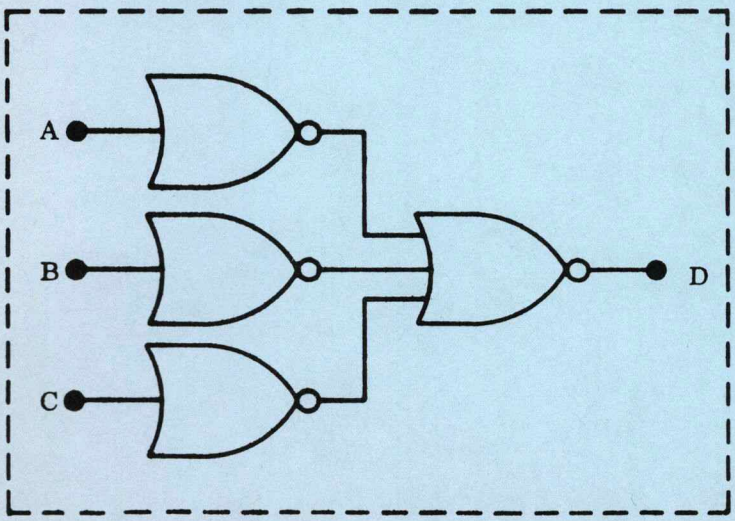
TRUTH TABLE



"OR" GATE, SYMBOL

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
D	0	1	1	1	1	1	1	1

TRUTH TABLE

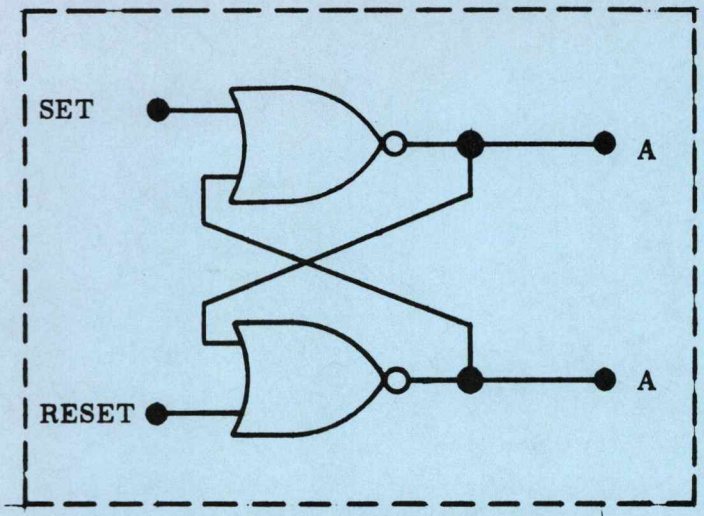


"AND" GATE, SYMBOL

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
D	0	0	0	0	0	0	0	1

TRUTH TABLE

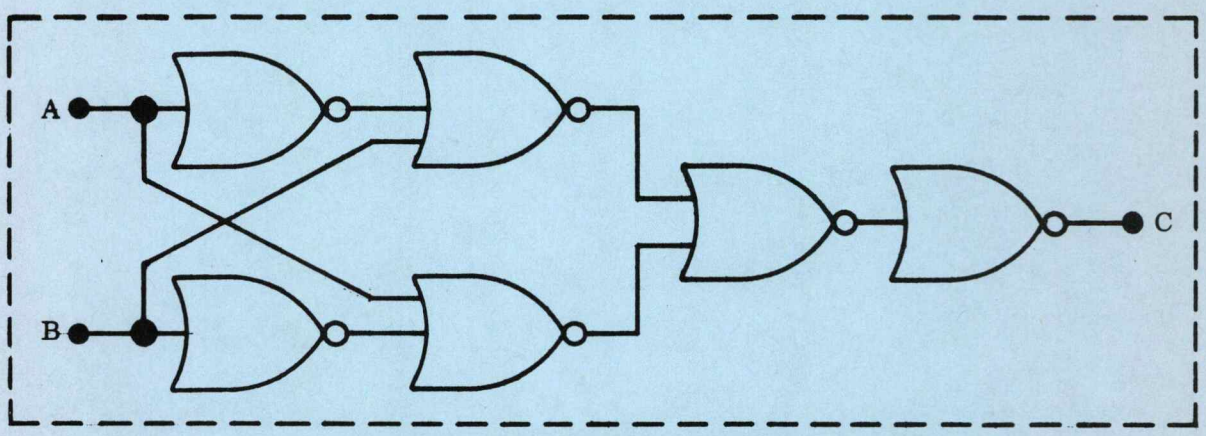
Figure 10-10. Typical Logic Functions



FLIP-FLOP, SYMBOL

	A	A
SET	1	0
RESET	0	1

TRUTH TABLE



"EXCLUSIVE OR", SYMBOL

A	0	0	1	1
B	0	1	0	1
C	0	1	1	0

TRUTH TABLE

Figure 10-11. Logic Functions

10.9 HARDWARE REGISTERS

A hardware register is a device which accepts and stores parallel information. Most of the CMC's registers are 16 bit registers (comprised of 16 storage elements).

The basic storage element for one bit, its read and write service gates, and the pulse required for write-in and read-out are shown in figure 10-12. The register service gates control write-in and read-out. Each bit position (storage element) is cleared coincident with write-in. Data from the write line is applied to the write service gate and is written into the storage element under control of a write control pulse from the sequence generator. Data is read out of a storage element under control of a read control pulse from the sequence generator.

Hardware register use and interface is described in the central processor description, paragraph 10.10.2.

10.10 CMC ORGANIZATION

The CMC can be functionally divided into the following areas:

a. Timer.

b. Central Processor.

c. Sequence Generator.

d. Memory.

e. Priority Control.

f. Input - Output.

g. Power.

Each area (see figure 10-13) will be discussed separately in subsequent paragraphs.

10.10.1 TIMER. The timer generates the timing signals required for operation and synchronization of the computer and is the primary source of timing signals for all spacecraft systems.

The timer is divided into five functional areas (see figure 10-14):

a. Oscillator.

b. Clock divider logic.

c. Scaler.

d. Time pulse generator.

e. Sync and timing logic.

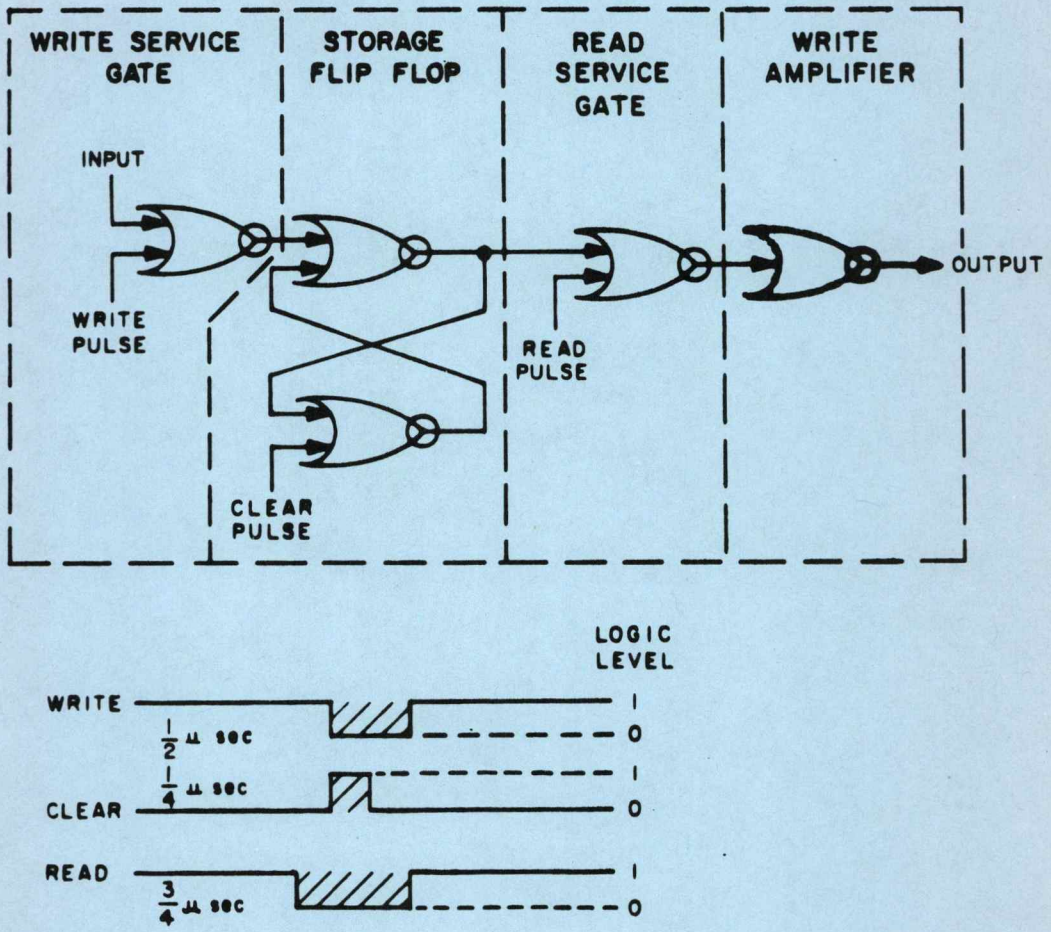


Figure 10-12. Basic Storage Element

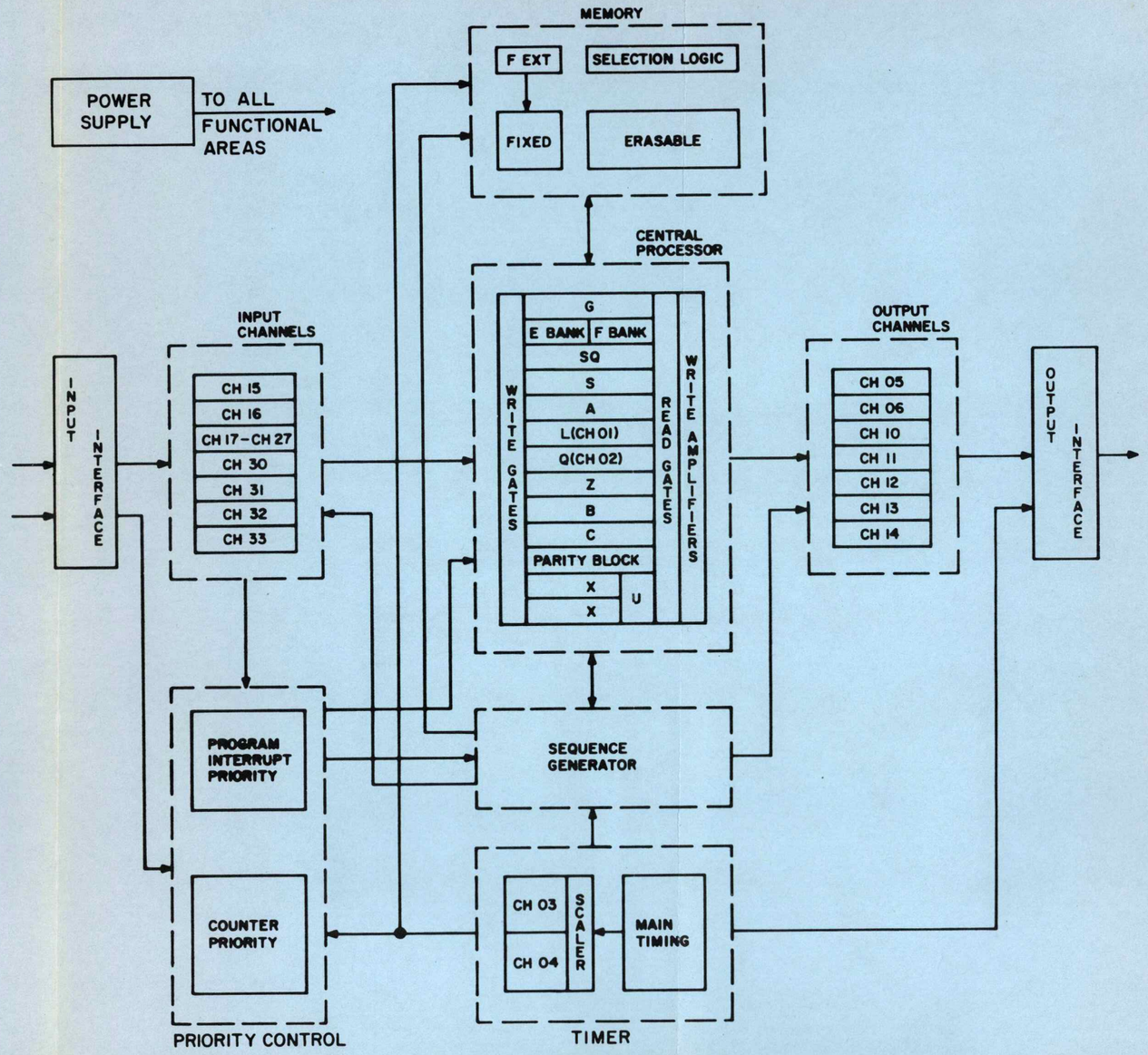


Figure 10-13. Computer Organization

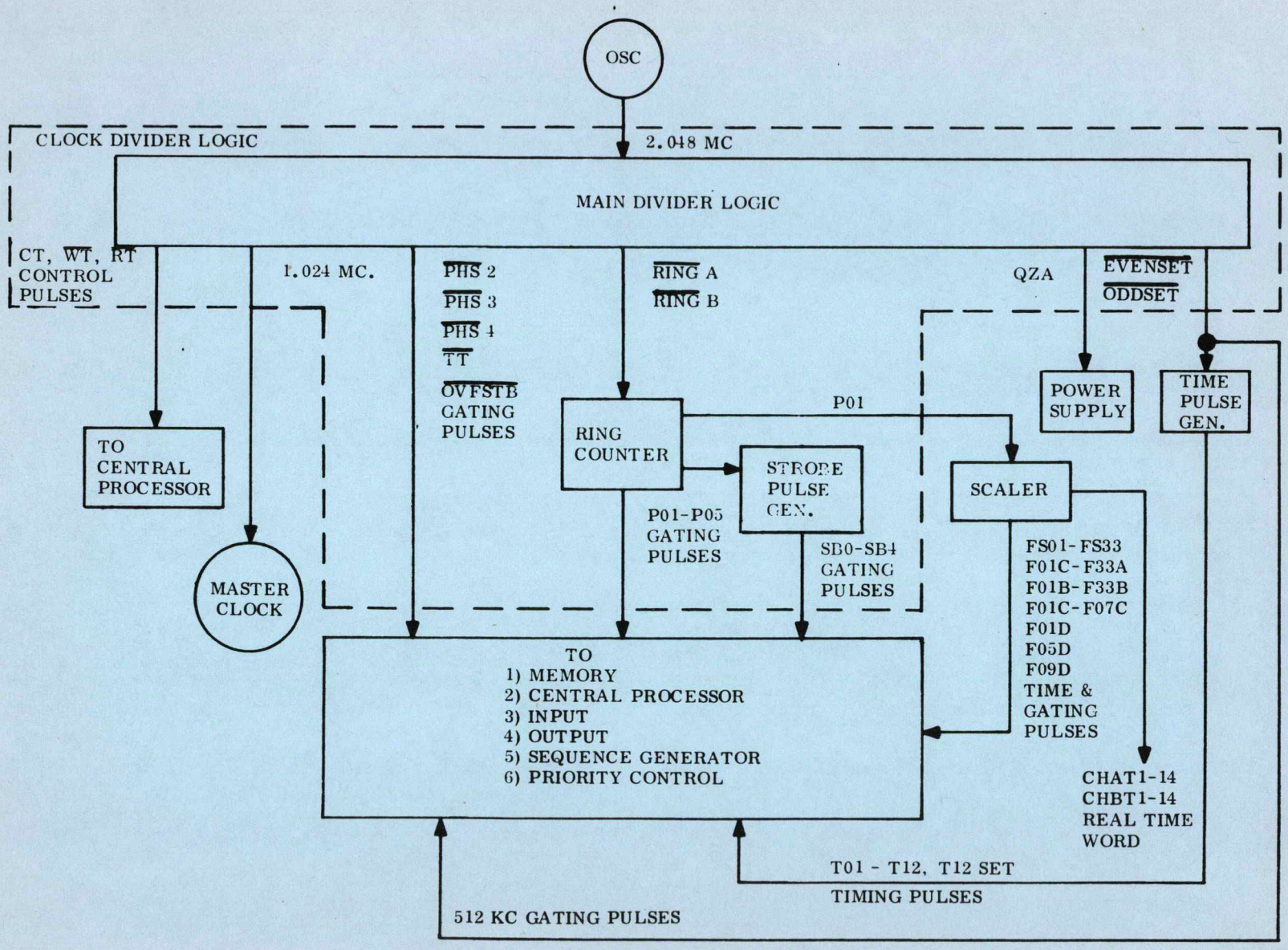


Figure 10-14. Timer, Functional Diagram

The master clock frequency is generated by an oscillator and is applied to the clock divider logic. The divider logic divides the master clock input into gating and timing pulses at the basic clock rate of the computer. Several outputs are available from the scaler, which further divides the divider logic output into output pulses and signals which are used for gating, to generate rate signal outputs and for the accumulation of time. Outputs from the divider logic also drive the time pulse generator which produces a recurring set of time pulses. This set of time pulses defines a specific interval (memory cycle time) in which access to memory and word flow take place within the computer.

The start-stop logic senses the status of the power supplies and specific alarm conditions in the computer, and generates a stop signal which is applied to the time pulse generator to inhibit word flow. Simultaneously, a fresh start signal is generated which is applied to all functional areas in the computer. The start-stop logic and subsequently word flow in the computer can also be controlled by inputs from the Computer Test Set (CTS) during pre-installation systems and subsystem tests.

10.10.1.1 Oscillator. The crystal controlled modified Pierce oscillator circuit generates a 2.048 mc square wave which is applied to the clock divider logic. Temperature compensated components in the oscillator circuit maintain high stability and assure an extremely accurate output frequency. The 2.048 mc signal is the prime source frequency for the timer, and, consequently, for the entire computer and spacecraft.

10.10.1.2 Clock Divider Logic. The clock divider logic is further sub-divided into the main divider logic section, ring counter and strobe pulse generator. The 2.048 mc input from the oscillator is applied to the main divider logic. This circuit divides the input frequency by two, and generates the following outputs: clear, write, and read control (CT, $\overline{\text{WT}}$, $\overline{\text{RT}}$) which are applied to the central processor to produce the signals necessary to clear, write into, and read out the flip-flop registers; 1.024 mc gating pulses ($\overline{\text{PHS2}}$, $\overline{\text{PHS3}}$, $\overline{\text{PHS4}}$, $\overline{\text{OVFSTB}}$, $\overline{\text{TT}}$) which are used throughout the CMC; the master clock signal (CLK) - a 1.024 mc output used to synchronize the other spacecraft systems; and signal QZA which is applied to the oscillator alarm circuit in the power supply to indicate oscillator activity. In addition, the main divider supplies signals ($\overline{\text{RING A}}$ and $\overline{\text{RING B}}$) to drive the ring counter, and signals ($\overline{\text{EVNSET}}$ and $\overline{\text{ODDSET}}$) to the time pulse generator. These latter outputs occur at a 512 kc rate as a result of further division of the 1.024 mc gating rate within the main divider.

The ring counter generates outputs (P01 - P05) at a 102.4 kc rate. The outputs are 5 microsecond pulses and are used for gating and for deriving other timing functions in the CMC. Ring counter outputs are also used to derive the strobe pulses (SB0, SB1, SB2, SB4) from the strobe pulse generator. These outputs also occur at a 102.4 kc rate and are 3 microseconds in width with the exception of SB4, which is a 2 microsecond pulse.

10.10.1.3 Scaler. The scaler consists of 33 identical divider stages. The stages are cascaded so that the frequency division is successive. The first stage is driven by signal $\overline{\text{P01}}$ from the ring counter, and generates outputs at a rate of one-half the input or 51.2 kc. This output and the remaining outputs through stage 17 (0.78125 pps) are used for timing and gating. The outputs appear as signal outputs from flip-flop circuits (FS01 etc.), and 10 microsecond pulse outputs (F01A etc.) at the same frequency as the associated stage. Stages 6 through 19 and 20 through 33 form a 28 bit real time word (CHAT01 - CHAT14, CHBT01 - CHBT14) which indicates time intervals up to 23.3 hours.

10.10.1.4 Time Pulse Generator. The time pulse generator consists of 12 flip-flop circuits and generates timing pulses $\overline{T01}$ through $\overline{T12}$. (See figure 10-15.) This sequence of timing pulses defines one memory cycle time (MCT) within the CMC or a period of 11.97 microseconds, in which word flow takes place. The time pulse generator is driven by inputs ($\overline{EVNSET}$ and $\overline{ODDSET}$) from the main divider logic. Signal $\overline{ODDSET}$ can be inhibited by signal STOP from priority control. Signal STOP, an input from the Computer Test Set (CTS) during preinstallation system and subsystem tests, and subsequently inhibits the time pulses from being generated thus preventing word flow in the CMC. This feature allows individual memory cycle times to be observed during tests.

10.10.1.5 Sync and Timing Logic. The sync and timing logic (start-stop logic) consists of a gating complex which generates various outputs for use within the CMC, and synchronization signals for systems external to the CMC. The inputs to, and outputs from this section are rather extensive.

The ring counter, strobe pulse generator, and the scaler supply inputs to the sync and timing logic. These inputs are used to derive gating and strobe signals for the input and output channels, pulse outputs for the program time counters in memory, and synchronization signals for the computer and DSKY power supplies and for systems external to the computer.

During standby operation, the oscillator, clock divider logic, and the scaler are operative and generate the signals associated with these functional areas. However, the outputs that are significant during this mode of operation are the real time word from the scaler and the synchronization signals to the other spacecraft systems. The real time word continues to be accumulated during standby, and the external systems sync signals continue to be generated.

10.10.2 CENTRAL PROCESSOR. The central processor, figure 10-16, consists of the flip-flop registers, the write, clear, and read control logic, write amplifiers, memory buffer register, memory address register and decoder, and the parity logic. All data and arithmetic manipulations within the CMC take place in the central processor.

Primarily, the central processor performs operations indicated by the basic instructions of the program stored in memory. Communication within the central processor is accomplished through the write amplifiers. Data flows from memory to the flip-flop registers or vice-versa, between individual flip-flop registers, or into the central processor from external sources. In all instances, data is placed on the write lines and routed to a specific register or to another functional area under control of the write, clear, and read logic. This logic section accepts control pulses from the sequence generator and generates signals to read the content of a register onto the write lines, and write this content into another register of the central processor or to another functional area of the CMC. The particular memory location is specified by the content of the memory address register. The address is fed from the write lines into this register, the output of which is decoded by the address decoder logic. Data is subsequently transferred from memory to the memory buffer register. The decoded address outputs are also used as gating functions within the CMC.

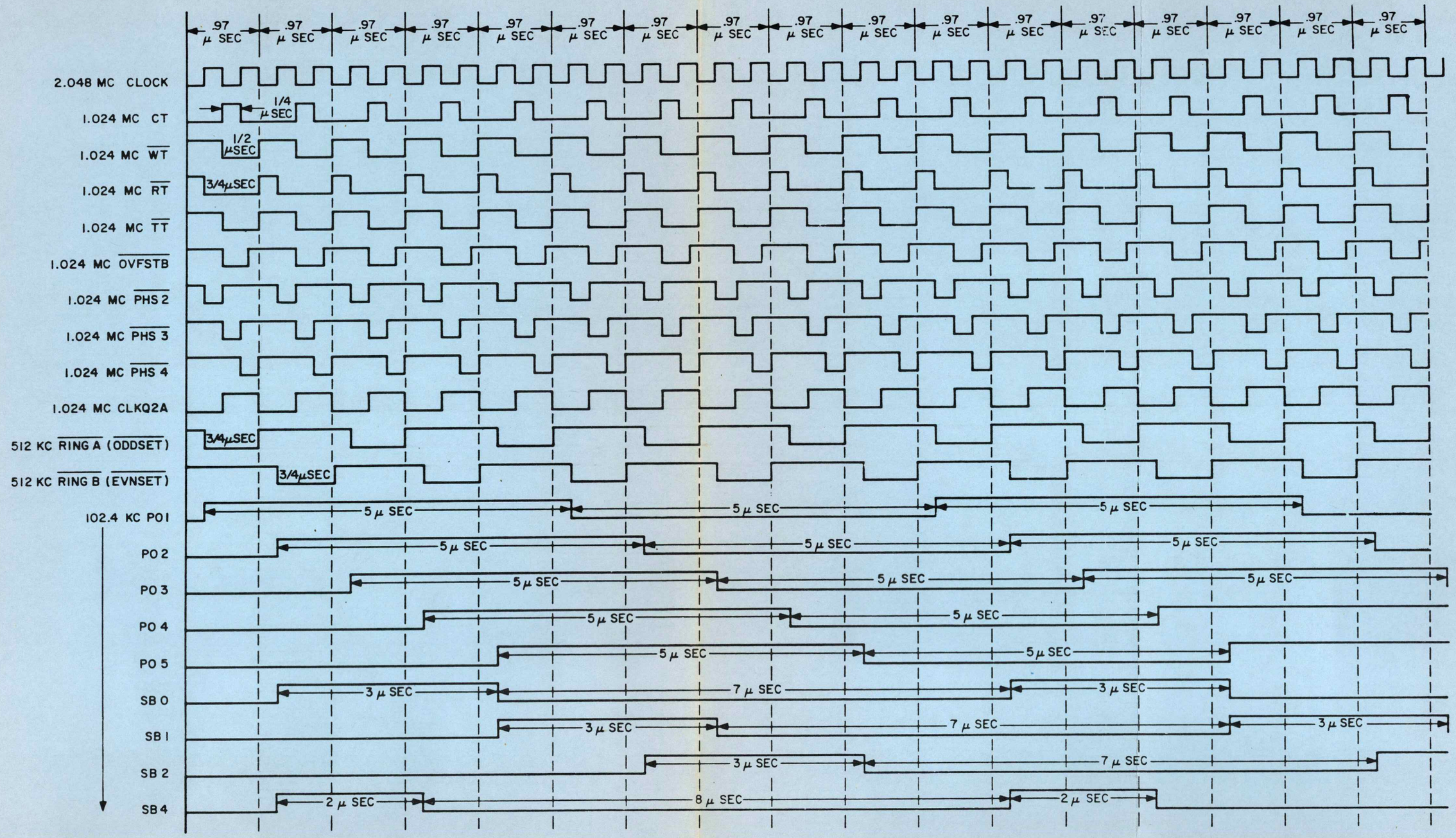
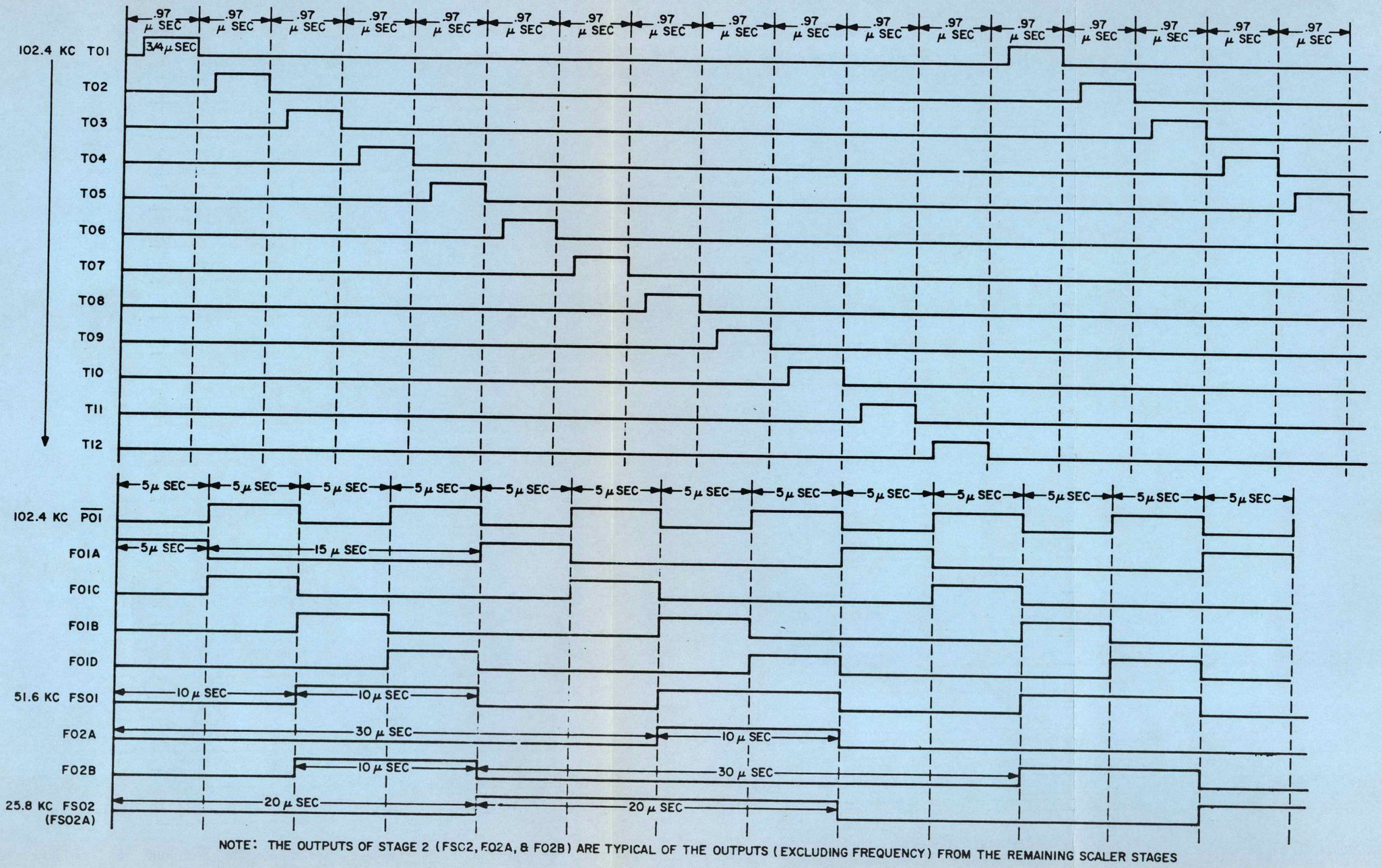


Figure 10-15. Timer Waveforms
(Sheet 1 of 2)



NOTE: THE OUTPUTS OF STAGE 2 (FSC2, F02A, & F02B) ARE TYPICAL OF THE OUTPUTS (EXCLUDING FREQUENCY) FROM THE REMAINING SCALER STAGES

Figure 10-15. Timer Waveforms
(Sheet 2 of 2)

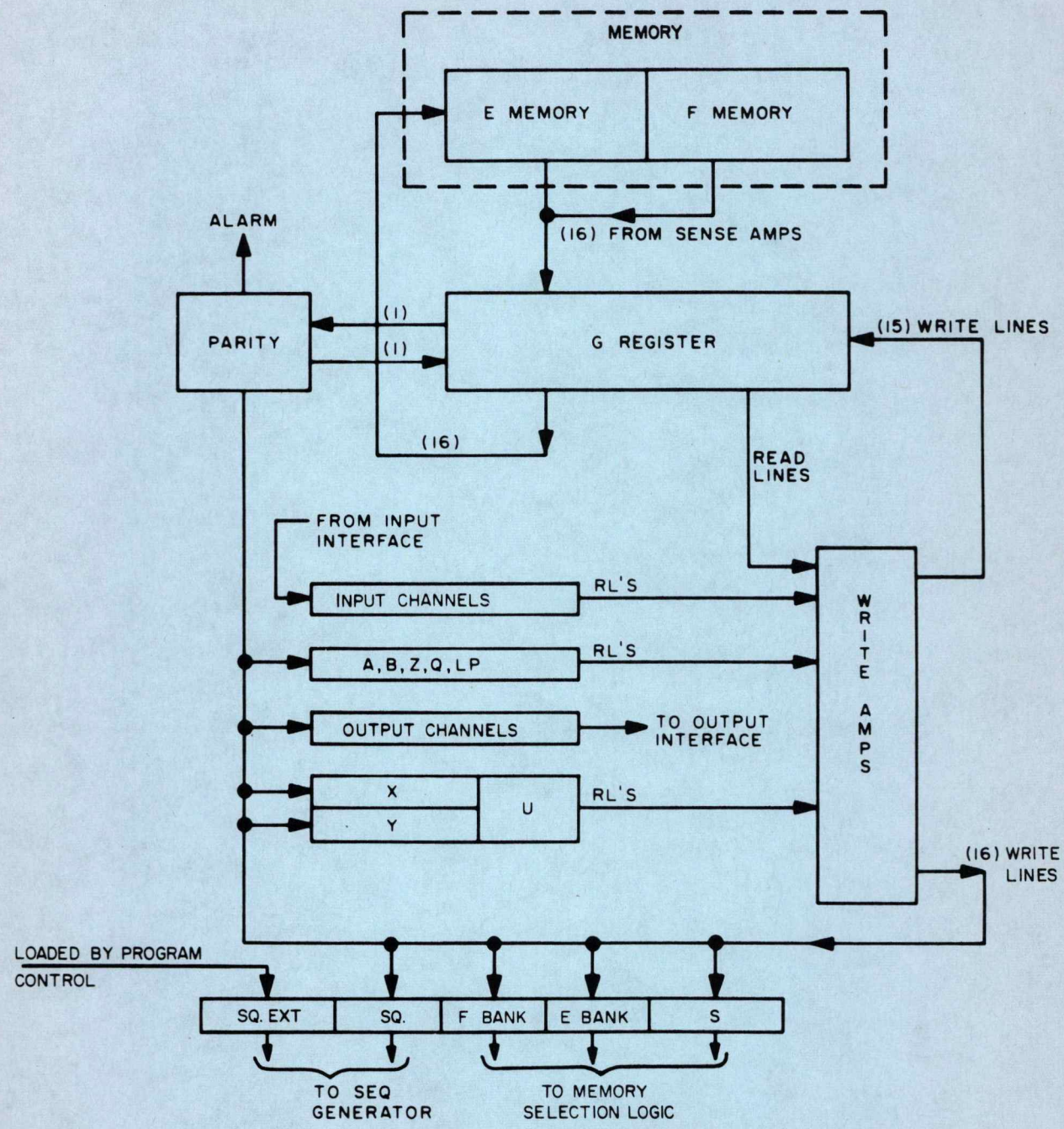


Figure 10-16. Central Processor Block Diagram

The memory buffer register buffers all information read out or written into memory. During readout, parity is checked by the parity logic and an alarm is generated in case of incorrect parity. During write-in, the parity logic generates a parity bit for information being written into memory. The flip-flop registers are used to accomplish the data manipulations and arithmetic operations. Each register is 16 bits or one computer word in length. Data flows into and out of each register as dictated by control pulses associated with each register. The control pulses are generated by the write, clear, and read control logic.

External inputs through the write amplifiers include the content of both the erasable and fixed memory bank registers, all interrupt addresses from priority control, control pulses which are associated with specific arithmetic operations, and the start address for an initial start condition. Information from the input and output channels is placed on the write lines and routed to specific destinations either within or external to the central processor. The CTS inputs allow a word to be placed on the write lines during system and subsystem tests.

10.10.2.1 Registers. Each register can be considered to contain 16 bits, unless otherwise specified. A description of each register in the central processor is given in figure 10-17.

10.10.2.2 Basic Data Flow. Figure 10-16 is a block diagram of the central processor including interface with other computer functional areas. When a word is gated out of memory, it is stored just in register G. Register G is a temporary storage area. If the data came from erasable memory, it is normally restored into erasable memory after it is read into some other register. A parity bit is removed from all words that come from memory. It is routed to the parity block where it is used to make the parity check. It is the interface between register G and the write amps that causes a duplication of the sign bit to form the overflow bit. This overflow bit is not written into the parity block; however, all other registers will receive this bit. There are 16 write amp outputs which can be gated into any of the central processor registers under control of the sequence generator. Words that are to be written into memory must have a parity bit generated for them in the parity block. This parity bit is sent directly to register G where it will join the appropriate word that has been gated into register G via the write amps. Words that are routed from the write amps to register G do not contain the overflow bit. This bit is replaced by the newly generated parity bit. The entire word is then written into erasable memory. In addition to temporarily storing all words to and from memory, register G will cycle or shift words to the right or left when programmed to do so. When shifting words to the left or right, the last bit is lost. However, in cycling, bit 1 becomes bit 16 or bit 16 becomes bit 1. The addresses mentioned will contain the cycled or shifted contents when used with most order codes.

10.10.2.3 Adder. The adder consists of registers X and Y and associated carry gates. The adder is the only true arithmetic manipulation circuitry in the CMC. Its function is to add two numbers together. Provisions are made to handle carries when necessary. The adder has the capability of adding +1 to a number by forcing an end-around-carry.

Register Designation	Address (Octal)	Bits	Name and Purpose
A	0000	16	1. Called the accumulator 2. Usually used to store results of these manipulations: a. Addition b. Subtraction c. Multiplication d. Division e. "AND"ing f. "OR"ing g. "EXCLUSIVE OR"ing
L	0001	16	1. Called the lower order accumulator. 2. Used to store results of these manipulations: a. Multiplication b. Division 3. Sometimes used in channel instructions.
Q	0002	16	1. Called the return address register. 2. Used to store the contents of the Z register, when the computer transfers control to another operation. 3. Used to exchange information with addresses in the central processor or erasable memory.
Z	0005	16	1. Called the program counter. 2. Contains the address of the next instruction word in the program.
B	None	16	1. A buffer register. 2. Used to hold the order code of an instruction. 3. Used to hold address information. 4. Used as a temporary storage of data information. 5. Has the ability to read out its actual contents or the compliment of its contents.
S	None	12	1. Contains the address portion of an instruction.
SQ	None	7 (includes an ext. bit)	1. Referred to as the instruction register. 2. Contains the operand of an instruction word.

Figure 10-17. Register Designation and Function (Sheet 1 of 2)

Register Designation	Address (Octal)	Bits	Name and Purpose
X and Y	None	16 ea.	1. Are referred to as the adder. 2. Performs all arithmetic operations. 3. The output gates of the adder are sometimes called the U register.
G	None	16	1. A buffer between memory and the central processor. 2. All information going to or coming from memory passes through this buffer register. 3. Any parity bit received from memory is transferred to the parity block before going to the central processor.
E-BANK	0003	3	1. Used to complete an address in erasable memory.
F-BANK	0004	8 (includes 3 ext. bits)	1. Used to complete an address in fixed memory.

Figure 10-17. Register Designation and Function (Sheet 2 of 2)

10.10.2.4 Parity Block. The parity block provides a means of self-checking the computer memory and transfer circuits. The parity block must test the parity of words just arriving in the central processor from memory, and also generate a new parity bit for words being stored in erasable memory. Any time a word is read out of memory, its parity must be tested. Every time a word is written into memory, its parity must be generated. The parity block is active during all of the 34 regular instructions and some of the involuntary ones.

The essence of the parity test is as follows:

a. Logically (using NOR logic elements) determine whether the number of ONE's in a word from memory is odd or even (excluding the parity bit).

b. Compare the parity bit with the information found in (a) above. If even, the parity bit should be 1 if the total number of ONE's is to be odd. If odd, the parity bit should be 0 for the same reason.

c. Any other condition except those defined in (b) above is an alarm condition.

The essence of the parity bit generation is as follows:

a. Repeat step (a) above.

b. If there is an even number of ONE's (excluding parity bit), generate parity bit = 1. If there is an odd number of ONE's (excluding parity bit), generate parity = 0.

10.10.2.5 Registers S, SQ, F BANK and E BANK. The Sq register will receive bits 16 and 14 through 10 directly from the write amps under control of the sequence generator. The S register receives bits 1 through 12 from the write amps under control of the sequence generator. The F BANK register will receive bits 16 and 14 through 11 from the write amps under program control. The E BANK register receives bits 9, 10 and 11.

Figure 10-18 is read in the following manner. The octal address is defined by the contents of the S register. For example, the E BANK register is addressed when bits 12 through 1 of the S register contain 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1 respectively. The column titled "Read and Write Lines of Write Amplifiers" is read as follows: In the row associated with the F BANK register, the read pulse associated with that register, read the contents of bits 16 and 14 through 10 of the F BANK register X into the appropriate write amplifiers, i.e., 16, 14 through 10. When information is written into register F BANK, write amplifiers 16 and 14 through 10 are written into the same bit positions of register F BANK. Note that there are two control pulses associated with writing into register A and that one of these pulses reads the outputs of write amps 14 through 1 into bit positions 16 through 3 of register A. Note also that there are five different write control pulses associated with register G which depend on signals WG1G through WG5G. The level of this study guide does not permit detailing the "why's" of the WG's. Suffice to say that the WG's determine which configuration will be written into the G register.

Registers A, L, Q, F BANK, E BANK, and Z are addressable; registers B, S, SQ, Y, X and G are not addressable. A register is addressable when it can be selected for write-in or read-out by entering the proper address into register S.

A word can be transferred from one central processor register to another either via the write amplifiers or directly. Direct transfer, however, takes place only among four of the registers. Read and write control pulses occur simultaneously and gate the read gates of the transmitting register and the write gates of the receiving register simultaneously. This also causes data to flow in parallel from one register to another via the write amps. The flow of information from one register to another via the write amps occurs on two different sets of lines: the read lines and the write lines. When one read pulse and two or three write control pulses occur simultaneously, the same information is entered into two or three registers. Direct read and write pulses transfer information directly from one register to only one other register.

Register				Control Pulse	Read and Write Lines of Write Amplifiers (WA's)															
Octal Address	Initials	Name			16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0000	A	Accumulator		**WRITE**	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
				WRITE	14	13	12	11	10	9	8	7	6	5	4	3	2	1	-	-
				READ	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0001	L	Low Order Accumulator		**WRITE**	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
				WRITE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	13
				READ	16		14	13	12	11	10	9	8	7	6	5	4	3	2	1
0002	Q	Return Address Register		**WRITE**	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
				READ	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0003	EBANK	E Memory Bank Selector		**WRITE**	-	-	-	-	-	11	10	9	-	-	-	-	-	-	-	-
				READ	-	-	-	-	-	11	10	9	-	-	-	-	-	-	-	-
0004	FBANK	F Memory Bank Selector		**WRITE**	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-
				READ	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-
0005	Z	Program Counter		**WRITE**	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
				READ	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0006	BBANK	Both registers EBANK and FBANK	EBANK	**WRITE**	-	-	-	-	-	-	-	-	-	-	-	-	-	11	10	9
				READ	-	-	-	-	-	-	-	-	-	-	-	-	-	11	10	9
			FBANK	**WRITE**	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-
				READ	16	-	14	13	12	11	-	-	-	-	-	-	-	-	-	-

Figure 10-18. Information Flow Between CP Registers Bit Positions and Write Amplifiers (Sheet 1 of 2)

Register			Control Pulse	Read and Write Lines of Write Amplifiers (WA's)															
Octal Address	Initials	Name		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
none	B C	Buffer Register with direct output B and complement output C	**WRITE**	16	15	4	13	12	11	10	9	8	7	6	5	4	3	2	1
			READ	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
			READ	-	-	-	-	-	-	10	9	8	7	6	5	4	3	2	1
none	S	Address Register	**WRITE**	-	-	-	-	12	11	10	9	8	7	6	5	4	3	2	1
none	SQ	Sequence Register	**WRITE**	16	-	14	13	12	11	10	-	-	-	-	-	-	-	-	-
none	Y X U	Adder with input registers X and Y and output gates U	**WRITE**	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
			WRITE	-	-	-	-	12	11	10	9	8	7	6	5	4	3	2	1
			WRITE	1	16	-	15	14	13	12	11	10	9	8	7	6	5	4	3	2
			READ	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
			READ	15			14	13	12	11	10	9	8	7	6	5	4	3	2	1
none	G	Memory Buffer Register	**READ**	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
		Control Signal																		
		WG1G, WG5G	**WRITE**	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
		WG2G, WG4G	**WRITE**	14		-	13	12	11	10	9	8	7	6	5	4	3	2	1	16
		WG2G, WG5G	**WRITE**	16	14	-	13	12	11	10	9	8	7	6	5	4	3	2	1	-
		WG3G, WG6G	**WRITE**	1		-	16	14	13	12	11	10	9	8	7	6	5	4	3	2
		WG3G, WG5G	**WRITE**	-		-	7	6	5	4	3	2	1	-	-	-	-	-	-	-

Figure 10-18. Information Flow Between CP Registers Bit Positions and Write Amplifiers (Sheet 2 of 2)

10.10.3 SEQUENCE GENERATOR. The sequence generator (figure 10-19) contains the order code processor, command generator, and control pulse generator. The sequence generator executes the instructions stored in memory by producing control pulses which regulate the data flow of the computer. The manner in which the data flow is regulated among the various functional areas of the computer and between the elements of the central processor causes the data to be processed according to the specifications of each machine instruction.

The order code processor receives signals from the central processor, priority control, and peripheral equipment (test equipment). The order code signals are stored in the order code processor and converted to coded signals for the command generator. The command generator decodes these signals and produces instruction commands. The instruction commands are sent to the control pulse generator to produce a particular sequence of control pulses depending on the instruction being executed. At the completion of each instruction, new order code signals are sent to the order code processor to continue the execution of the program.

10.10.3.1 Order Code Processor. The order code processor (figure 10-20) consists of the register SQ control, register SQ and decoders, and stage counter and decoders. The register SQ control is regulated by special purpose control pulse NISQ from the control pulse generator. Control pulse NISQ produces clear and write signals for register SQ and initiates a read signal for register B. The clear, read, and write signals place the order code content of register B onto the write lines and into register SQ. The order code signals from the priority control and the peripheral equipment pertain to instructions start, interrupt, and transfer control to specified address. These order code signals cause the SQ control to produce the clear signals. If the order code signal is start or transfer control to specified address, no further action occurs because the order code for each of these instructions is binary 0 000 000. If the order code signal is interrupt, register SQ is set to 1 000 111. Other special purpose control pulses provide regulatory functions within the register SQ control during instruction interrupt and some address - dependent instructions.

Register SQ is a seven-bit register with only six of its bit positions (16 and 14 through 10) connected to the central processor write lines. The seventh (high-order) bit position is the extend bit. This high-order bit position is used for extending the order code field; it contains a ZERO for basic instructions and a ONE for extracode, channel, and interrupt instructions. Bit positions 16, 14, and 13 produce the SQ signals. At any time, only one of the eight possible SQ signals is present to indicate the octal number specified by these bit positions. Bit positions 12 and 11 contain the quarter code. These bits are decoded into one of four QC signals to indicate the octal number specified by these two bit positions. Bit position 10 is not used for basic and extracode instructions; however, it is used for the channel and interrupt instructions.

The stage counter is a three-stage Gray counter especially adapted for various counts other than the Gray code. Most instructions are several memory cycle times (MCT's) long. The stage counter controls the length of each instruction. Most instructions use the two low-order bits of the stage counter. The stage counter always starts an instruction with count 000. Then it may be advanced to 001, 010, or 011 by special purpose control pulses ST1 and ST2 from the control pulse generator. The Gray code count is used for the divide instruction. Control pulse DVST advances the counter through the states, 000, 001, 011, 111, 110, and 100. The control pulse ST2 sets the stage counter to 010 to complete the divide instruction. The content of the stage counter is decoded into the ST code signals. Some of the ST code signals reflect the standard binary count

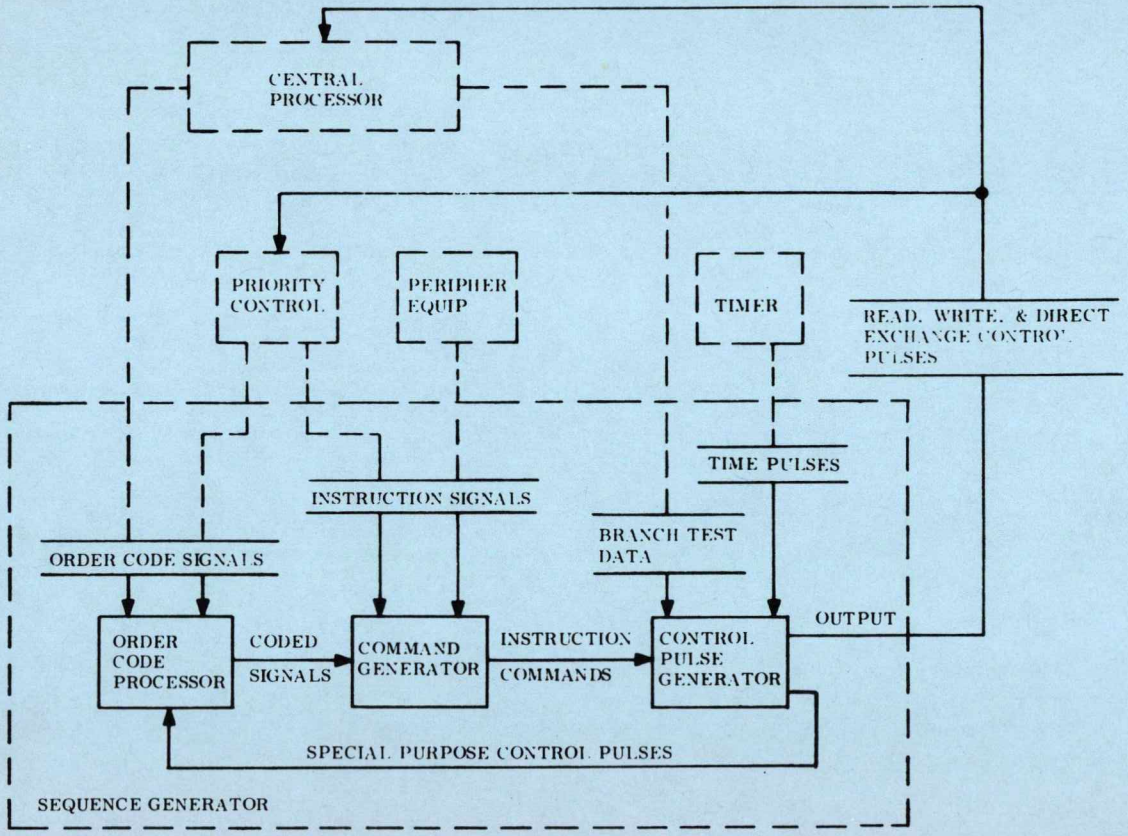


Figure 10-19. Sequence Generator Block Diagram

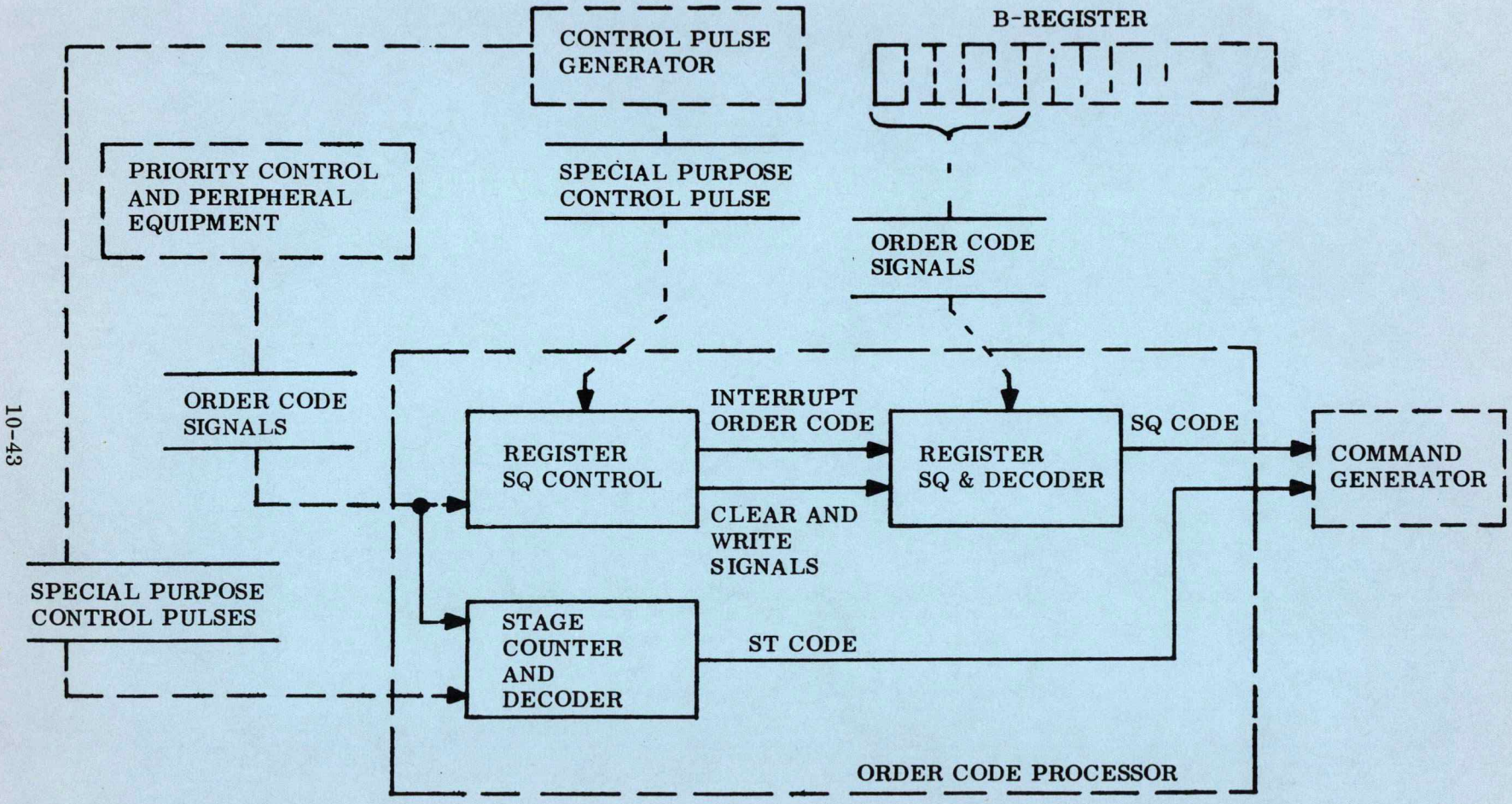


Figure 10-20. Order Code Processor, Block Diagram

from octal 0 through 3, and others reflect the Gray code count of octal 0, 1, 3, 7, 6, and 4. The order code signals from the priority control and the peripheral equipment set the stage counter to a particular state in a manner similar to that in which the SQ register is set. The interrupt order code signal sets the stage counter to 000, the start order code signal sets it to 001, and the transfer control to specified address signal sets it to 011. The outputs of the SQ and stage decoders are sent to the command generator where they are used to produce subinstruction and instruction commands.

10.10.3.2 Command Generator. The command generator (figure 10-21) contains the subinstruction decoder, instruction decoder, and the counter and peripheral instruction control. The subinstruction decoder receives the SQ and ST code signals from the order code processor. These signals represent the order codes of all machine instructions and are decoded into subinstruction and instruction commands. For example, channel instruction WOR has a binary order code 1 000 101 and stage code 000. The SQ code signals SQEXT, SQ0, QC2, and SQR10 are combined with ST code signal ST0 to produce subinstruction command WOR0.

The instruction decoder receives the coded signals from the order code processor in addition to certain subinstruction commands. It produces signals called instruction commands. An instruction command is used for two or more subinstructions as compared to a subinstruction command which is used only for one subinstruction. For example, instruction command IC1 generates a combination of control pulses shared by subinstruction NDX0 and NDXX0. Instruction command IC1 is produced by signals SQEXT, SQ5, and ST0 for subinstruction NDX0 or by signals SQ5, QC0, and ST0 for subinstruction NDXX0. Other instruction commands are produced from subinstruction commands. For example, IC8 is produced by ORing DXCH0 with LXCH0.

The counter and peripheral instruction control receives instruction signals from the priority control and the peripheral equipment. These signals are applied to separate circuits which control the individual counter and peripheral instructions. The instruction signals from the priority control pertain to counter locations and the instruction(s) associated with each location. For example, signal C31A is interpreted as counter 31 address. The content of this location can only be changed by instruction DINC whose subinstruction command is produced by the counter and peripheral instruction control. Another example is signal C42P, interpreted as counter 42 positive increment or signal C42M, counter 42 negative increment. The peripheral equipment supplies instruction signals such as MREAD and MLOAD for the fetch and store instructions, respectively. While the particular instruction is being executed, the counter and peripheral instruction control stores the input signals in the same way that order code signals are stored by register SQ. Since some of the peripheral instructions are several MCT's long, they use the ST code signals. The subinstruction and instruction command outputs of the command generator are used by the control pulse generator in conjunction with time pulses T01 through T12 to produce action pulses.

10.10.3.3 Control Pulse Generator. The control pulse generator (figure 10-22) contains the crosspoint generator, control pulse gates, and branch control. The crosspoint generator receives instruction and subinstruction commands from the command generator and branch commands from the branch control. The crosspoint generator produces an action pulse when a command signal and a time pulse are ANDed. This is called the crosspoint operation. For example, action pulse 5XP12 is produced from subinstruction command DAS0 and time pulse T05. Many instructions use identical action pulses. When this is the case, several command signals such as TC0, TCF0,

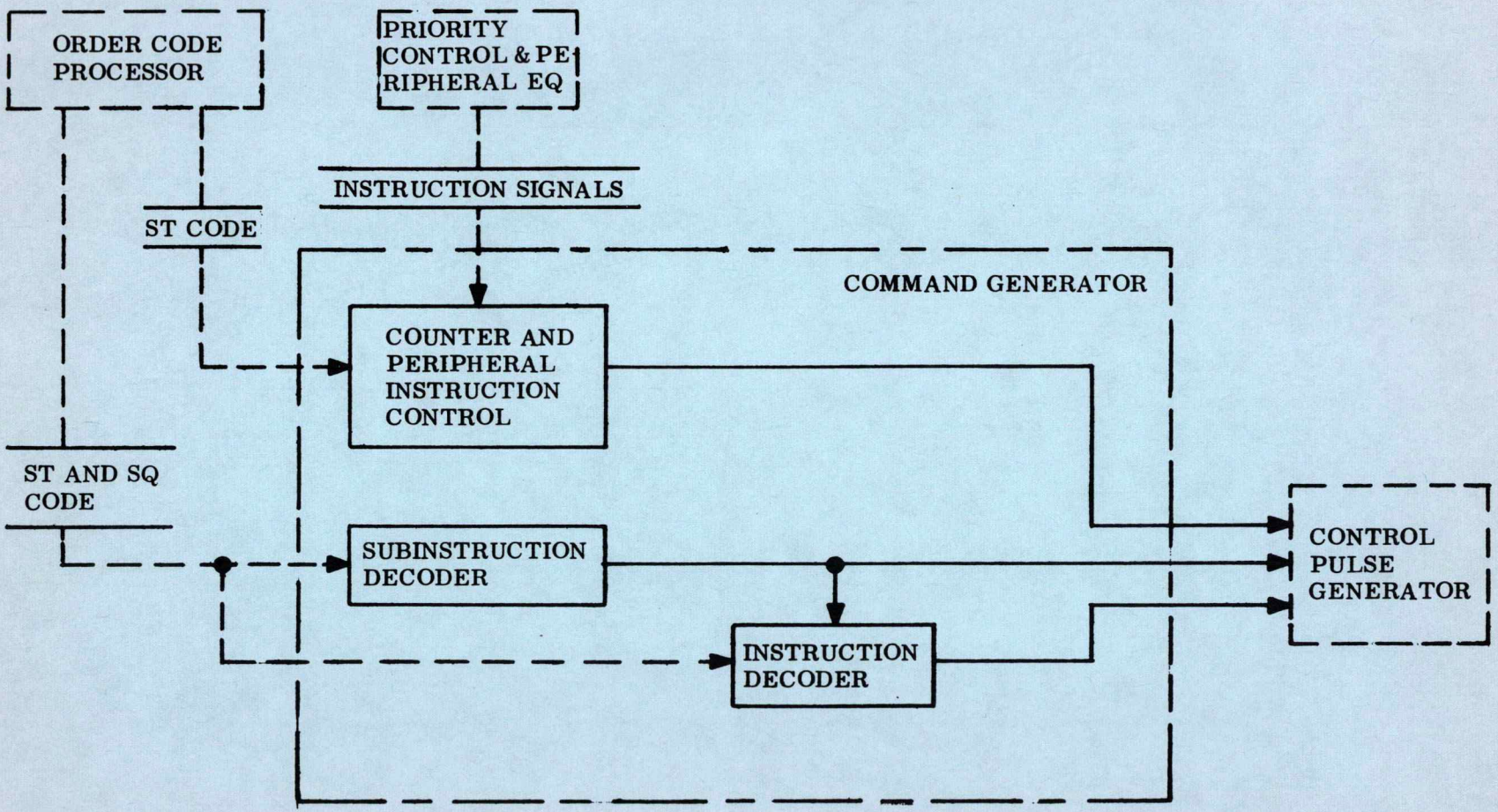


Figure 10-21. Command Generator, Block Diagram

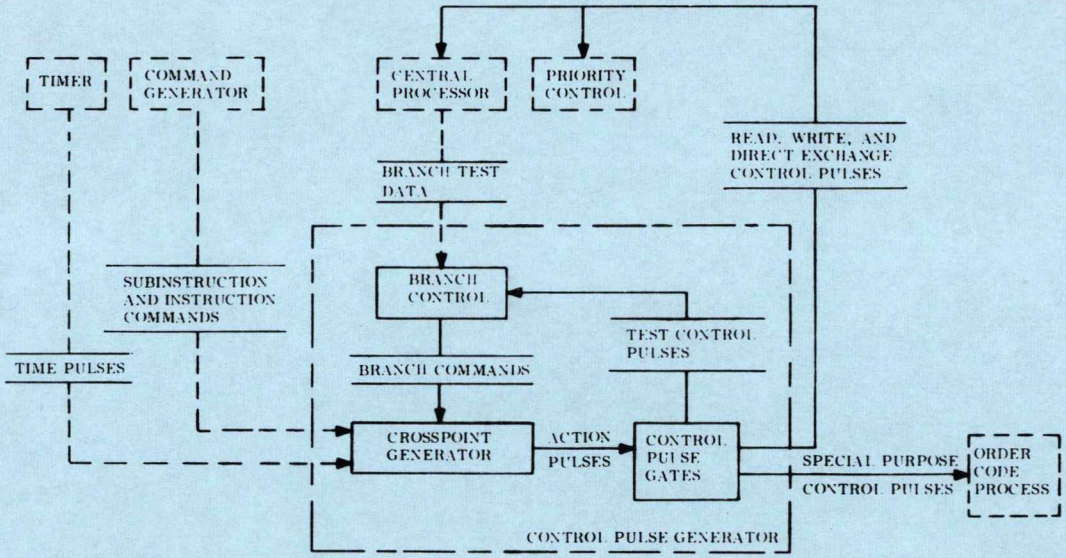


Figure 10-22. Control Pulse Generator, Block Diagram

or IC4 will produce the same action pulse during time period T01. The branch commands are used to change the action pulse that normally is produced at a given time. For example, when certain conditions exist, a branch command will produce action pulse 8XP6 in addition to another action pulse normally produced at time period T08. The action pulses are supplied to the control pulse gates which convert them to specific control pulses for use in instruction execution.

The control pulse gates perform the Boolean NOR function. There is one gate for each control pulse. These gates split the action pulses into as many control pulses as are required for a particular operation. For example, action pulse 3XP6 is converted to control pulses RZ and WQ. Some of the control pulses produced by the control pulse gates are used by the sequence generator. These include the special purpose control pulses which control the operation of the order code processor and the test control pulses which are applied to the branch control. The other control pulse groups, namely the read, write, and direct exchange control pulses are used in the central processor and the priority control.

The branch control is connected to the write lines of the central processor. Data which is placed onto the write lines by read control pulses is tested in the branch control. The branch control contains two stages. Branch 1 normally tests for sign and branch 2 test for full quantities such as plus or minus zero. Both branches test for positive and negative overflow and have the overflow bits written directly into the branch register. Positive overflow is 01 where branch 1 is the high order bit. Negative overflow is 10. The branch commands sent to the crosspoint generator affect the action pulses at given times. The branch control also contains the special instruction flip-flop which controls the execution of instructions RELINT, INHINT, and EXTEND.

10.10.3.4 Register SQ Control. The register SQ control is regulated by special purpose control pulse NISQ from the control pulse generator. Control pulse NISQ causes the register SQ control to produce clear signal CSQG, read signal RBSQ, and write signal WSQG. These signals place the order code (content of register B) onto the write lines and into register SQ at the beginning of each new instruction. The order code signals applied to the register SQ control from the priority control (GOJAM and RUPTOR) and peripheral equipment (MTCSAI) pertain to instructions start, interrupt, and transfer control to specified address, respectively. A distinct priority is associated with each of these three instructions. Instructions interrupt and transfer control to specified address can never be requested when the computer is forcing the execution of the start instruction, which has the highest priority. Certain peripheral instructions occupy the next level of priority, followed by the counter instructions and in turn the transfer control to specified address instruction, which has priority over the interrupt instruction; all six of these instruction categories have priority over basic instructions.

10.10.4 DESCRIPTION OF COMPUTER INSTRUCTIONS

The same instructions, which are directions given to perform specific operations, are the same for the CMC and LGC. Together with data addresses, they constitute the building blocks of a program. Programs are sequential lists of instruction words. There are two general categories of instructions, machine and interpretive. Several types of instructions used in the computer may be categorized as follows:

MACHINE (56)

REGULAR (42)

BASIC (15)

EXTRACODE (12)

CHANNEL (7)

SPECIAL (8)

INVOLUNTARY (9)

INTERRUPT (2)

COUNTER (7)

PERIPHERAL (5)

INTERPRETIVE

The machine instructions can be interpreted and executed directly by using the sequence generator to control the computer operation. The interpretive instructions are a programmer's convenience and must be interpreted under program control, converted to machine instructions and then executed as machine instructions. Table 10-3 lists the machine instructions alphabetically and gives a brief description of each. The reader will find it to his advantage to refer back to this table once he has gained a greater familiarity with the computer. The following symbols are used in table 10-3.

K represents any address in the central processor, erasable memory or fixed memory.

F represents an address in fixed memory only.

E represents an address in the central processor or erasable memory.

H represents any channel address.

C represents any counter address.

A represents the A register on the central processor.

L represents the L register in the central processor.

c(K) represents the contents of K, i.e., the data located in address K.

I, I + 1, I + 2 represents the addresses of successive instruction words stored in memory.

c (I), C (I + 1), C (I + 2) represents the contents of successive instruction words stored in memory.

10.10.4.1 Machine Instructions. The CMC has three classes of machine instructions: regular, involuntary, and peripheral. Regular instructions are programmed and are executed in whatever sequence they have been stored in memory. Involuntary instructions (with one exception) are not programmable and have priority over regular instructions: no regular instruction can be executed when the CMC forces the execution of an involuntary instruction. The peripheral instructions are used during ground testing when the CMC is connected to the CTS or PAC: the CMC cannot perform any program operation during a peripheral instruction.

10.10.4.1.1 Regular Instructions. There are four types of regular instructions: basic, channel, extracode, and special. The difference between the regular instructions is directly related to the way in which the CMC interprets an instruction word. Instruction words stored in memory are called "basic instructions words" and consist of a three bit order code and a twelve bit address code. The order code defines an operation and the address code defines a location.

The contents of the SQ register will determine what instruction the CMC will perform. The SQ register reflects that data transferred into it from memory. The SQ register consists of six bits and one EXT. bit (figure 10-23). A binary point is assumed to be located between bits thirteen and twelve. When an instruction word is transferred from memory to the SQ register, bits 15 through 10 of the word in memory are transferred to bits 16 and 14 through 10 of the SQ register (figure 10-24). In the following paragraph, however, only the transfer of bits 15, 14 and 13 from memory to bits 16, 14 and 13 of the SQ register will be considered.

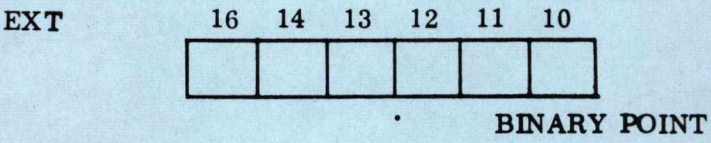


Figure 10-23. SQ Register

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 1 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
AD K	06.	Basic Instruction: add c(K) to c(A); stores result in A; takes next instruction from I + 1 where I is location of AD K.	2
ADS E	02.6	Basic Instruction: adds c(A) to c(E) and stores result in both A and E; takes next instruction from I + 1 where I is location of ADS E.	2
AUG E	12.4	Extra Code Instruction: adds +1 to c(E), if c(E) is positive and -1 if c(E) is negative; stores result in E; takes next instruction from I+1 where I is location of AUG E. NOTE: AUG, DIM and INCR are slightly modified counter increment sequences. Accordingly, if one of this group overflows when addressing a counter for which overflow (during involuntary incrementing) is supposed to cause an interrupt, the interrupt will occur. It should be noted that all three of these instructions unlike the increment sequences, always operate in one's complement, even when addressing CDU counters.	2
BZF F	11.2 11.4 11.6	Extra Code Instruction: takes next instruction from F if c(A) is ±0; otherwise takes next instruction from I + 1 where I is location of BZF F.	1 if c(A) is ±0; otherwise 2
BZMF F	16.2 16.4 16.6	Extra Code Instruction: takes next instruction from F if c(A) is +0 or negative; otherwise takes next instruction from I + 1 where I is location of BZMF F.	1 if c(A) is +0 or negative, otherwise 2
CA K	03.	Basic Instruction: clears c(A) and copies c(K) into A; takes next instruction from I + 1 where I is location of CA K.	2

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 2 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
CCS E	01.0	Basic Instruction: if c(E) is nonzero and positive, takes next instruction from I + 1 where I is location of CCS E, adds -1 to c(E) and stores result in A. If c(E) is +0, takes next instruction from I + 2 and sets c(A) to +0. If c(E) is nonzero and negative, takes next instruction from I + 3, adds -1 to the absolute value of the c(E) and stores result in A. If c(E) is -0, takes next instruction from I + 4 and sets c(A) to +0.	2
CS K	04.	Basic Instruction: clears c(A) and copies $\overline{c(K)}$ into A; takes next instruction from I + 1 where I is location of CS K.	2
CYL	.0022	Special Instruction: cycles quantity, which is entered into location 0022, one place to left.	
CYR	.0020	Special Instruction: cycles quantity, which is entered into location 0020, one place to right.	
DAS E	02.0	Basic Instruction: adds c(A, L) to c(E, E + 1); stores result in E and E + 1; sets c(L) to +0 and sets c(A) to net overflow if address E is not 0000_8. Net overflow is +1 for positive overflow, -1 for negative overflow, otherwise c(A) is set to +0. Takes next instruction from I + 1 where I is location of DAS E. Note: DAS A doubles the contents of the double precision accumulator - implied address code DDOUBL assembles as DAS A. Since the hardware must operate on the low order operands first, consider DAS as the operation code 20001 to which the address E is added to for the instruction.	3
DCA K	13.	Extra Code Instruction: copies c(K, K + 1) into A and L; takes next instruction from I + 1 where I is location of DCA K.	3

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 3 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
DCS K	14.	Extra Code Instruction: copies c(K, K + 1) into A and L; takes next instruction from I + 1 where I is location of DCS K.	3
DIM E	12.6	Extra Code Instruction: adds -1 if c(E) is nonzero and positive and +1 if c(E) is nonzero and negative; stores result in E; if c(E) is ±0, c(E) is not changed; takes next instruction from I + 1 where I is location of DIM E. See NOTE under AUG.	2
DINC C	None	Counter Instruction: adds +1 to c(C) if c(C) is negative; adds -1 to c(C) if c(C) is positive; provides no change if c(C) is ±0; stores result in C, delays program execution for 1 MCT.	1
DV E	11.0	Extra Code Instruction: divides c(A, L) by c(E): stores quotient in A; stores remainder in L; takes next instruction from I + 1 where I is location of DV E. NOTE: The signs of the double length dividend in A & L need not agree. The net sign of the dividend is the sign of c(A) unless c(A) is ±0, in which case it is the sign of c(L). The remainder bears the net dividend sign, and the quotient sign is determined strictly by the divisor and net dividend signs.	6
DXCH E	05.2	Basic Instruction: exchanges c(E, E + 1) with c(A, L); takes next instruction from I + 1 where I is location of DXCH E.	3
EXTEND	00.0006	Special Instruction: Take the next instruction from I + 1, where I is the EXTEND instruction and execute it as an extracode instruction. If I + 1 is INDEX (full operation code 15), the following instruction will also be executed as an extracode.	1
FETCH K	None	Peripheral Instruction: reads and displays c(K) as binary numbers on CTS or PAC where K is address supplied by CTS or PAC.	2

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 4 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
EDOP	.0023	Special Instruction: shifts quantity, which is entered into location 0023, seven places to left.	
COJ	00.	Interrupting Instruction: transfers control to instruction stored in location 4000_8 and proceeds from there.	2
INCR E	02.4	Basic Instruction: adds + 1 to c(E); stores result in E; takes next instruction from I + 1 where I is location of INCR E. See NOTE under AUG.	2
INHINT	00.0004	Special Instruction: Inhibit program interrupts until a subsequent RELINT. Take the next instruction from I + 1 where I was INHINT. NOTE: The inhibition set by INHINT and removed by RELINT in entirely independent of the one set by an interrupt and removed by a RESUME.	1
INOT LD H	None	Peripheral Instruction: loads data supplied by CTS or PAC into location H where H is channel address also supplied by CTS or PAC.	1
INOTRD H	None	Peripheral Instruction: reads and displays c(H) as binary number on CTS or PAC where H is channel address supplied by CTS or PAC.	1
LXCH E	02.2	Basic Instruction: exchanges c(E) with c(L); takes next instruction from I + 1 where I is location of LXCH E.	2
MCDU C	None	Counter Instruction: adds -1 (two's complement) to c(C). NOTE: Incrementing in two's complement modulator notation transfers octal 40000 to 37777 and 00000 to 77777 and is otherwise like one's complement. PCDU and MCDU replace PINC and MINC for counters 0032 through 0036.	1

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 5 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
MINC C	None	Counter Instruction: adds -1 to c(C); delays program execution for 1 MCT. If negative overflow occurs, c(C) is set to -0.	1
MP K	17.	Extra Code Instruction: multiplies c(A) by c(K); stores result in A and L; c(A, L) agree in sign; takes next instruction from I + 1 where I is location of MP K. A zero result is positive unless c(A) = ±0 and c(K) is non-zero with the opposite sign.	3
MSK K	07.	Basic Instruction: AND's c(A) with c(K); stores result in A; takes next instruction from I + 1 where I is location of MSK K.	2
MSU E	12.0	Extra Code Instruction: forms signed one's complement difference between c(A) and c(E) where c(A) and c(E) are unsigned (modular or periodic) two's complement numbers; stores result in A; the method is to form the two's complement difference, to decrement it if it is negative, and to take the overflow-uncorrected sum as the result; takes next instruction from I + 1 where I is location of MSU E.	2
NDX K	05.0	Basic Instruction: adds c(K) to c(I + 1) where I is location of NDX E; takes sum of c(K) + c(I + 1) as next instruction. INDEX 0017 is an implied instruction to resume an interrupted program.	2
NDX K	15.	Extra Code Instruction: adds c(K) to c(I + 1) where I is location of NDX K; sets extra code switch; sum of c(K) + c(I + 1) becomes an Extra Code Instruction which is taken as next instruction. This INDEX will not act as a RESUME.	2
PCDU C	None	Counter Instruction: adds +1 (two's complement) to c(C); delays program execution for 1 MCT. See NOTE under MCDU.	1

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 6 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
PINC C	None	Counter Instruction: adds +1 to c(C); delays program execution for 1 MCT. If positive overflow occurs, the counter is set to +0 and an interrupt is set up if the counter is T3, T4, T5 or set up a PINC for T2 if the counter was T1.	1
QXCH E	12.2	Extra Code Instruction: exchanges c(E) with c(Q); takes next instruction from I + 1 where I is location of QXCH E.	2
RAND H	10.2	Channel Instruction: AND's c(H) with c(A); stores result in A; takes next instruction from I + 1 where I is location of RAND H.	2
READ H	10.0	Channel Instruction: copies c(H) into A; takes next instruction from I + 1 where I is location of READ H.	2
ROR H	10.4	Channel Instruction: Inclusive OR's c(H) with c(A); stores result in A; takes next instruction from I + 1 where I is location of ROR H.	2
RELINT	00.0003	Special Instructions: Removes program interrupt inhibits. Allows interrupts after this instruction subject to the restriction that an interrupt cannot occur while there is plus or minus overflow in A.	1
RESUME	05.0017	Special Instruction: takes next instruction from return address (location of which address is stored in location 0017). This allows the resumption of the interrupted program.	1
RUPT	10.7	Interrupting Instruction: takes next instruction from address supplied by Interrupt Priority Control; stores c(B) (instruction that was to be executed) in location 0017_8; stores c(Z) = I in location 0015_8 where I is assigned location of instruction stored in 0017. This instruction is for machine checkout only.	3

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 7 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
RXOR H	10.6	Channel Instruction: forms the exclusive OR of c(H) and c(A); stores result in A; takes next instruction from I + 1 where I is location of RXOR H.	2
SHANC C	None	Counter Instruction: doubles c(C) and adds +1; stores result in C; delays program execution for 1 MCT. This action amounts to shifting c(C) one digit to the right and adding +1. NOTE: SHANC and SHINC are used to convert incoming serial bit streams into words for parallel access.	1
SHINC C	None	Counter Instruction: doubles c(C); stores result in C; delays program execution for 1 MCT. This action amounts to shifting c(C) one digit to the right. See NOTE under SHANC.	1
SR	.0021	Special Instruction: shifts quantity, which is entered into location 0021, one place to right.	
STORE E	None	Peripheral Instruction: data supplied by CTS or PAC is stored in location E where E is address supplied by CTS or PAC; delays program execution for 2 MCT's.	2
SU E	16.0	Extra Code Instruction: subtracts c(E) from c(A); stores result in A; takes next instruction from I + 1 where I is location of SU K.	2
TC K	00.	Basic Instruction: takes next instruction from K; stores I + 1 in Q where I is location of TC K; if K is 0006 (EXTEND), sets extra code switch and takes next instruction from I + 1; if K is 0004_8 (INHINT), sets inhibit interrupt switch and takes next instruction from I + 1; if K is 0003_8 (RELINT), resets inhibit interrupt switch and takes next instruction from I + 1.	1

Table 10-3. Machine Instructions, Alphabetical Listing (Sheet 8 of 8)

Symbolic Instruction Word	Order Code	Description	Execution Time in MCT's
TCF F	01.2 01.4 01.6	Basic Instruction: takes next instruction from F. Does not change the contents of Q.	1
TCSAJ K		Peripheral Instruction: takes next instruction from K where K is address supplied by CTS or PAC.	2
TS E	05.4	Basic Instruction: if c(A) is not an overflow quantity, copies c(A) into E and takes next instruction from I + 1 where I is location of TS E; if c(A) is a positive overflow quantity, copies c(A) into E, sets c(A) to +1, and takes next instruction from I + 2; if c(A) is a negative overflow quantity, copies c(A) into E, sets c(A) to -1, and takes next instruction from I + 2.	2
WAND H	10.3	Channel Instruction: AND's c(H) with c(A); stores result in H and A; takes next instruction from I + 1 where I is location of WAND H.	2
WOR H	10.5	Channel Instruction: Inclusively OR's c(H) with c(A); stores result in H and A; takes next instruction from I + 1 where I is location of WOR H.	2
WRITE H	10.0	Channel Instruction: copies c(A) into H; takes next instruction from I + 1 where I is location of WRITE H.	2
XCH E	05.6	Basic Instruction: exchanges c(A) with c(E); takes next instruction from I + 1 where I is location of XCH E.	2

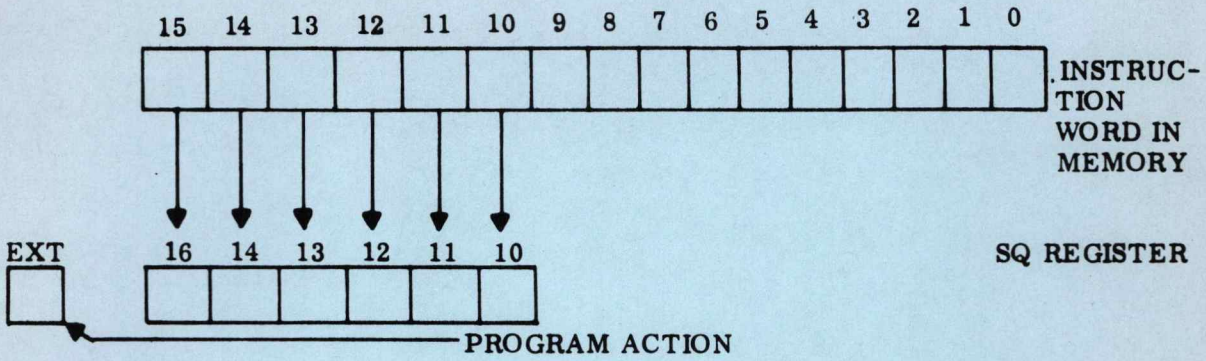


Figure 10-24. Memory to SQ Register Transfer

The three bit order code in the memory basic instruction words has a capability of uniquely defining eight operations: To increase the number of operations defined by the SQ register, bit EXT (extend) is made a 1 or 0 under program control, therefore, bits EXT, 16, 14 and 13 of the SQ register define sixteen operations.

Note the order codes in column 2 of table 10-3. These order codes are determined, in most cases, by the contents of the SQ register. Figure 10-24 shows how the order codes in table 10-3 are related to the actual contents of the SQ register. The instruction defined by figure 10-25 is TS E.

In table 10-3, the instructions can be categorized into three distinct groups by their listings in the order code column.

a. Those that list "None."

b. Those that list four digits to the right of the binary point.

c. Those that list two or three digits with the binary point written to the right of the second digit.

Group a contains the counter and peripheral instructions. There are no order codes associated with these instructions.

Group b contains the special instructions that are address dependent basic instructions. Their order codes are, in part, determined by bits 1 through 12. Those special instructions with no digits to the left of the decimal point can be combined with any basic instruction order code. Those with digits to the left of the decimal point are combined with that basic instruction whose order code appears to the right of the decimal point.

Group c contains the basic, extracode and channel instructions, i.e., all the regular instructions with the exception of the special instructions. Also included in this group are the two interrupt instructions: these are <u>not</u> regular instructions.

Note that the instructions in this group may or may not have a digit to the right of the decimal point. When there is a digit to the right of the decimal point, it is determined by bits 11 and 12 or bits 10, 11 and 12 of the SQ register. When bits 11 and 12 are necessary to extend the order code field, their configuration is called a "quarter code." When bits 10, 11 and 12 are necessary to extend the order code field, their configuration is called an "eighth code." Table 10-4 shows the configuration of the various quarter and eighth codes associated with this group. Note that there are two ways of defining a zero or an even digit to the right of the decimal point. Observe instructions CCS E and TCF F in table 10-3. These instructions are identical if only the digits to the left of the decimal point are considered. There, two instructions can be distinguished, however, if bits 11 and 12 of the SQ register are observed. Note that the content of bit 10 in register SQ is irrelevant because only four cases have to be distinguished and, consequently, a quarter code is sufficient to define the necessary operation. Now observe the instruction in table 10-4 which have digits 1 and 0 to the left of the decimal point in the order code column. There are eight of these instructions and to differentiate between them, bits 10, 11 and 12 of the SQ register are necessary because eight cases must be differentiated. If just bits 11 and 12 were used, only four cases could be distinguished.

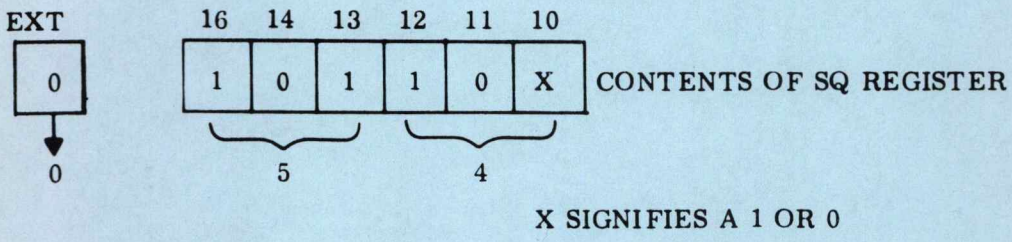


Figure 10-25. Order Code Determination

Basic instructions can be differentiated from extracode and channel instructions by the left hand digit of the order code. If bit EXT in the SQ register is a 0, then the left hand digit is a zero and the instruction is a basic instruction. If bit EXT is a 1, then the left hand digit is a one and the instruction is an extracode or channel instruction.

10.10.4.1.2 Involuntary Instructions. The involuntary instruction class contains two types of instructions - interrupt and counter. The interrupt instructions use the basic instruction word format just as the regular instructions do. However, the interrupt instructions are not entirely programmable. The contents of the order code field and the address field are supplied by computer logic rather than the program. The counter instructions have no instruction word format. Signals which function as a decoded order code specify the counter instruction to be executed and the computer logic supplies the address. The address for these instructions is limited to one of 29 counter locations in memory.

There are two interrupt instructions. One instruction initializes the computer when power is first applied and when certain program traps occur. The other interrupt instruction is executed at regular intervals to indicate time, receipt of new telemetry or keyboard data, or transmission of data by the computer. This interrupt instruction may be programmed to test the computer.

Table 10-4. Quarter and Eighth Codes

EIGHTH OR QUARTER CODES		SQ REGISTER BITS		
		12	11	10
EIGHTH	.0	0	0	0
QUARTER	.0	0	0	X
EIGHTH	.1	0	0	1
EIGHTH	.2	0	1	0
QUARTER	.2	0	1	X
EIGHTH	.3	0	1	1
EIGHTH	.4	1	0	0
QUARTER	.4	1	0	X
EIGHTH	.5	1	0	1
EIGHTH	.6	1	1	0
QUARTER	.6	1	1	X
EIGHTH	.7	1	1	1

X stands for a 1 or 0

There are several counter instructions. Two instructions will either increment or decrement by one the content of a counter location using the one's complement number system. Two other instructions perform the same function using the two's complement number system. Certain counter instructions control output rate signals and convert serial telemetry data to parallel computer data.

10.10.4.1.3 Peripheral Instructions. There are two types of peripheral instructions. One type deals with memory locations and the other type deals with channel locations. The peripheral instructions are not used when the computer is in the spacecraft. They are used when the computer is connected to peripheral equipment during subsystem and preinstallation system testing. The peripheral instructions are not programmable and are executed when all computer program operations have been forcibly stopped. These instructions are used to read and load any memory or channel location and to start the computer program at any specified address. The peripheral instructions and counter instructions are processed identically.

10.10.4.2 Interpretive Instructions. Interpretive instructions, a programmer's convenience and a means of saving memory storage area, must be interpreted under program control, converted to machine instructions and then executed as machine instructions. The coding into interpretive instructions of routines which contain double precision, triple precision, vector, and vector matrix operations results in a considerable saving in program storage area in fixed memory. This saving is achieved at the expense of computer operating speed; however, when operating in basic machine language the computer operates much faster than the equipment with which it interfaces. Since most of the PGNCS problems the computer is required to solve involve complex mathematical equations, the use of interpretive instructions for vector matrix algebra and complex differential calculus is a definite asset.

10.10.4.3 Instruction Data Flow. Examples of instruction data flow are illustrated in figures 10-26a, 10-26b, 10-26c, 10-27a, 10-27b, and 10-27c). Figure 10-26a shows the general flow chart and register utilitzation diagrams for the AD K instruction. Figures 10-26b and 10-26c indicate the detailed subinstruction flow diagrams necessary to produce an AD K instruction. Similar diagrams, figures 10-27a, 10-27b, 10-27c, are presented for the resume instruction.

10.10.5 MEMORY. The CMC has erasable and fixed memories. The erasable memory can be written into and read out of; fixed memory can only be read out of. Erasable memory stores intermediate results of computations, auxiliary program information, and variable data supplied by external inputs from the PGNCS and other systems of the spacecraft. Fixed memory stores programs, constants, and tables. There is a total of 38,912, sixteen bit word storage locations in fixed and erasable memories. It should be noted that the majority of the memory capacity is in fixed memory (36,864 word locations). Both memories are magnetic core storage devices; however, the cores are used differently in each type of memory. It is assumed that the reader is familiar with the basic magnetic properties of a ferrite core as described by a square hysteresis curve. A core is a static storage device having two stable states. It can be magnetized in one of two directions by passing a sufficient current, I, through a wire which pierces the core. The direction of current determines the direction of magnetization. The core will retain its magnetization indefinitely until an opposing current switches the core in the opposite direction. Wires carrying current through the same core are algebraically additive. Sense wires which pierce a switched core will carry an induced pulse.

10.10.5.1 Erasable Memory Core Array. Erasable memory is arranged in a three-dimensional 32 x 64 x 16 core array for a total of 2048 16-bit storage locations. Each bit requires 1 core for its storage. The direction of magnetization determines whether a logic 1 or 0 is stored. The intersection of X planes and Y planes define 16-bit words. There are 64 X planes and 32 Y planes as indicated in figure 10-28.

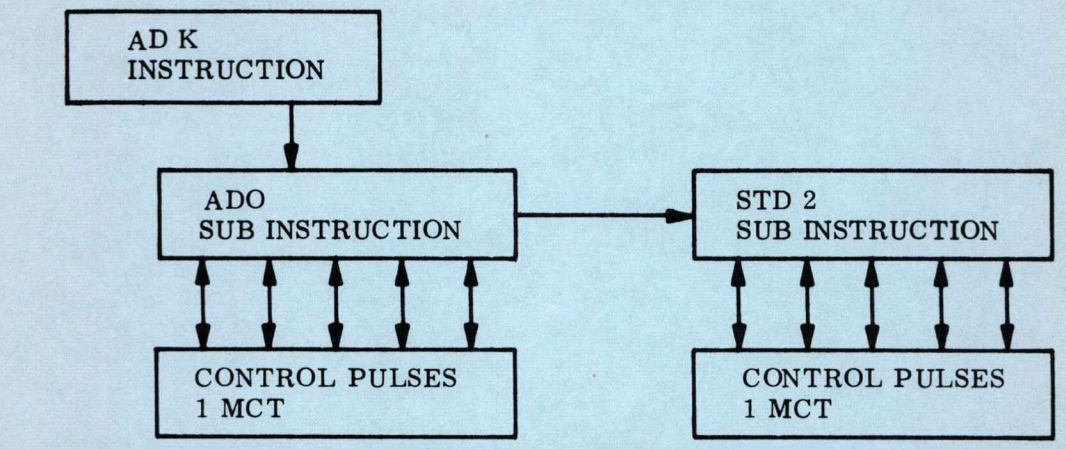
Each core of erasable memory is threaded by four lines: an X selection line, a Y selection line, an inhibit line and a sense line. (See figure 10-29.) Each of the 64 X planes has a unique X selection line threading each core in that plane; each of the 32 Y planes has a unique Y selection line threading each core in that plane. Each of the 16-bit planes has a unique inhibit line threading each core in that plane and a unique sense line threading each core in that plane. Therefore, there is a total of 64 X selection lines, 32 Y selection lines, 16 inhibit lines and 16 sense lines in erasable memory. Readout of the erasable memory cores is destructive. If it is desired to retain the information in erasable memory, it must be written back into erasable memory. To read a core, currents = + 1/2 I are simultaneously passed through the X and Y selection lines threading that core. Note the plus sign associated with the current. Current in the plus direction is a read current; current in the minus direc-

AD K INSTRUCTION

PURPOSE: TO ADD THE CONTENTS OF ANY ADDRESS IN THE CENTRAL PROCESSOR, ERASABLE MEMORY, OR FIXED MEMORY TO THE CONTENTS OF THE A REGISTER AND STORE THE RESULT IN A (ACCUMULATOR).

TAKE THE NEXT INSTRUCTION FROM I + 1 WHERE I IS THE LOCATION OF AD K.

FLOW DIAGRAM



REGISTER UTILIZATION

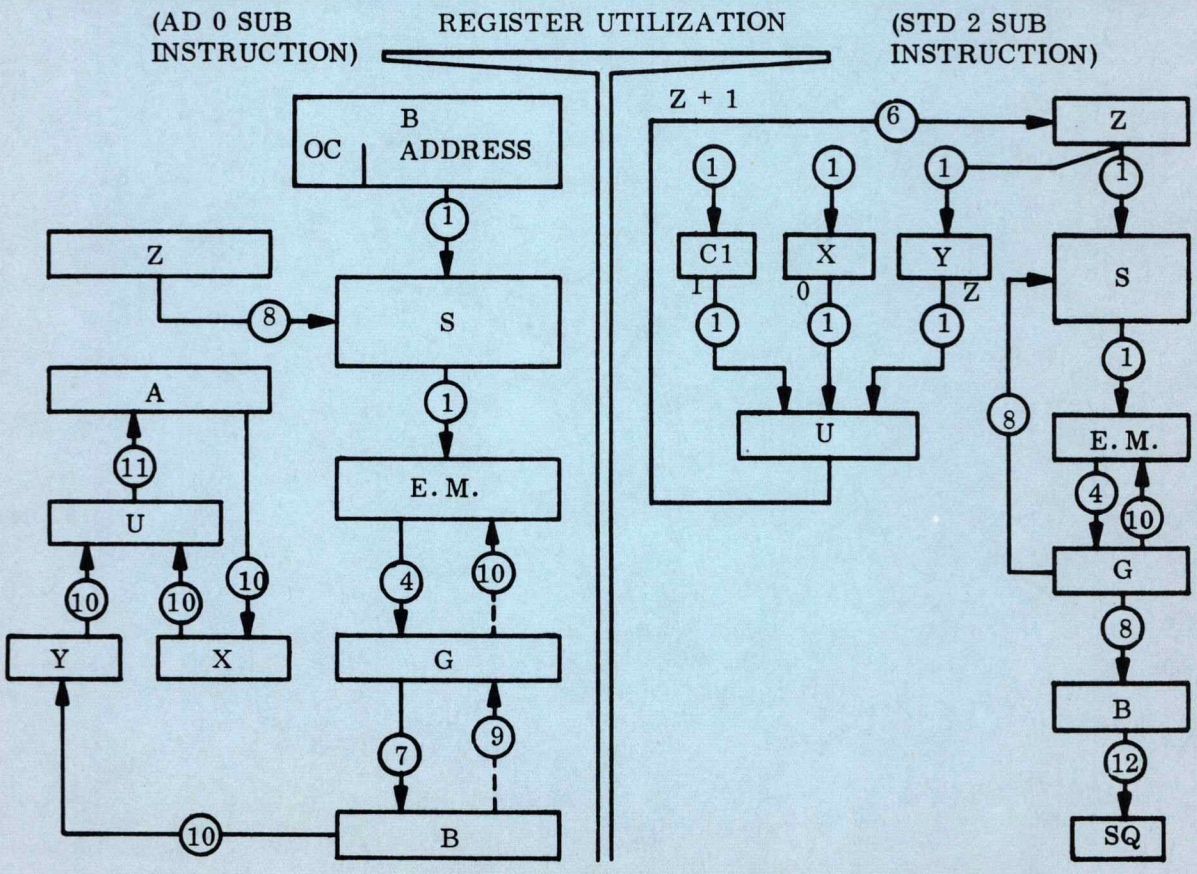


Figure 10-26a. Register Utilization for AD K Instruction, Flow Diagram

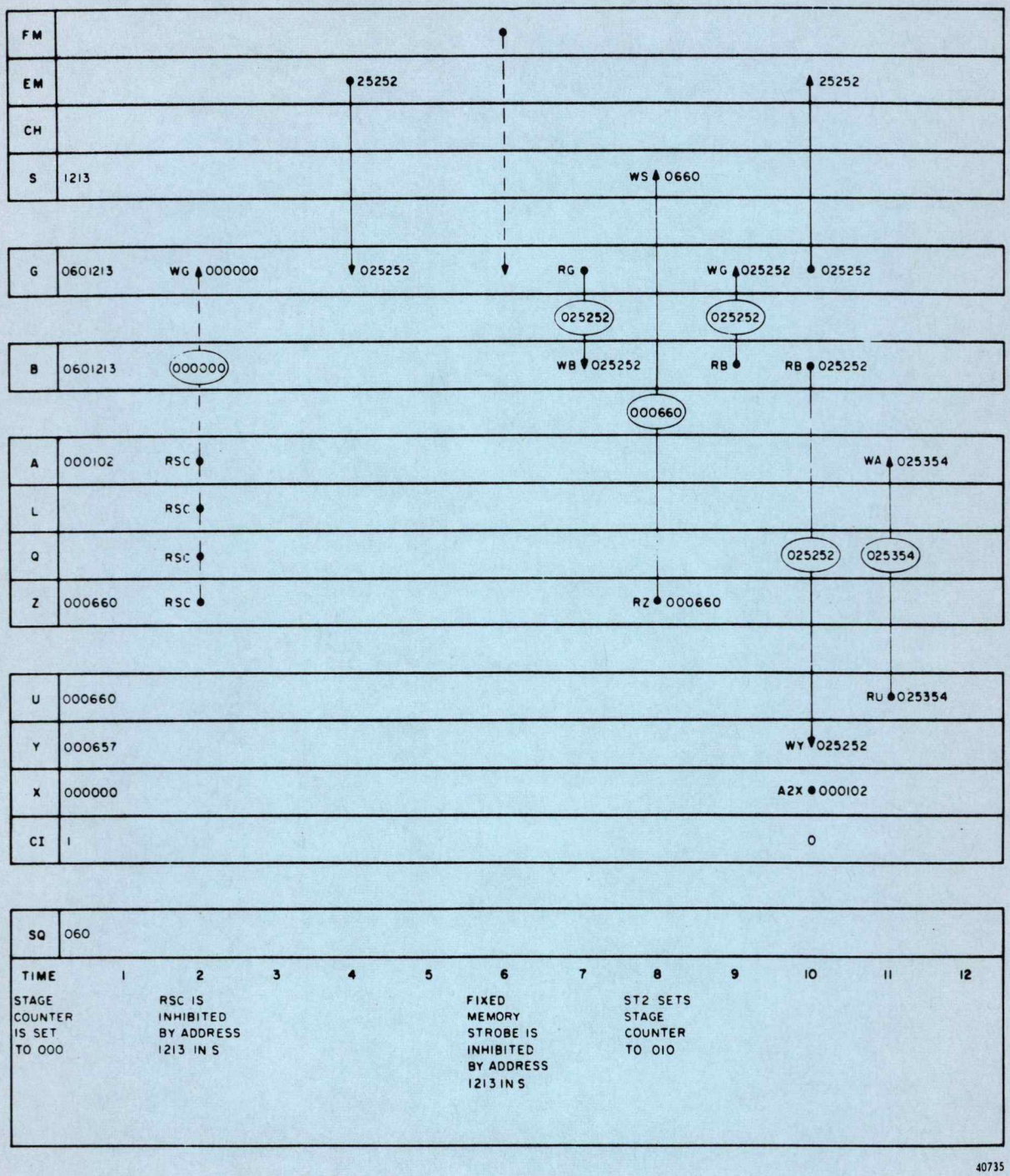


Figure 10-26b. Subinstruction AD0, Data Transfer Diagram

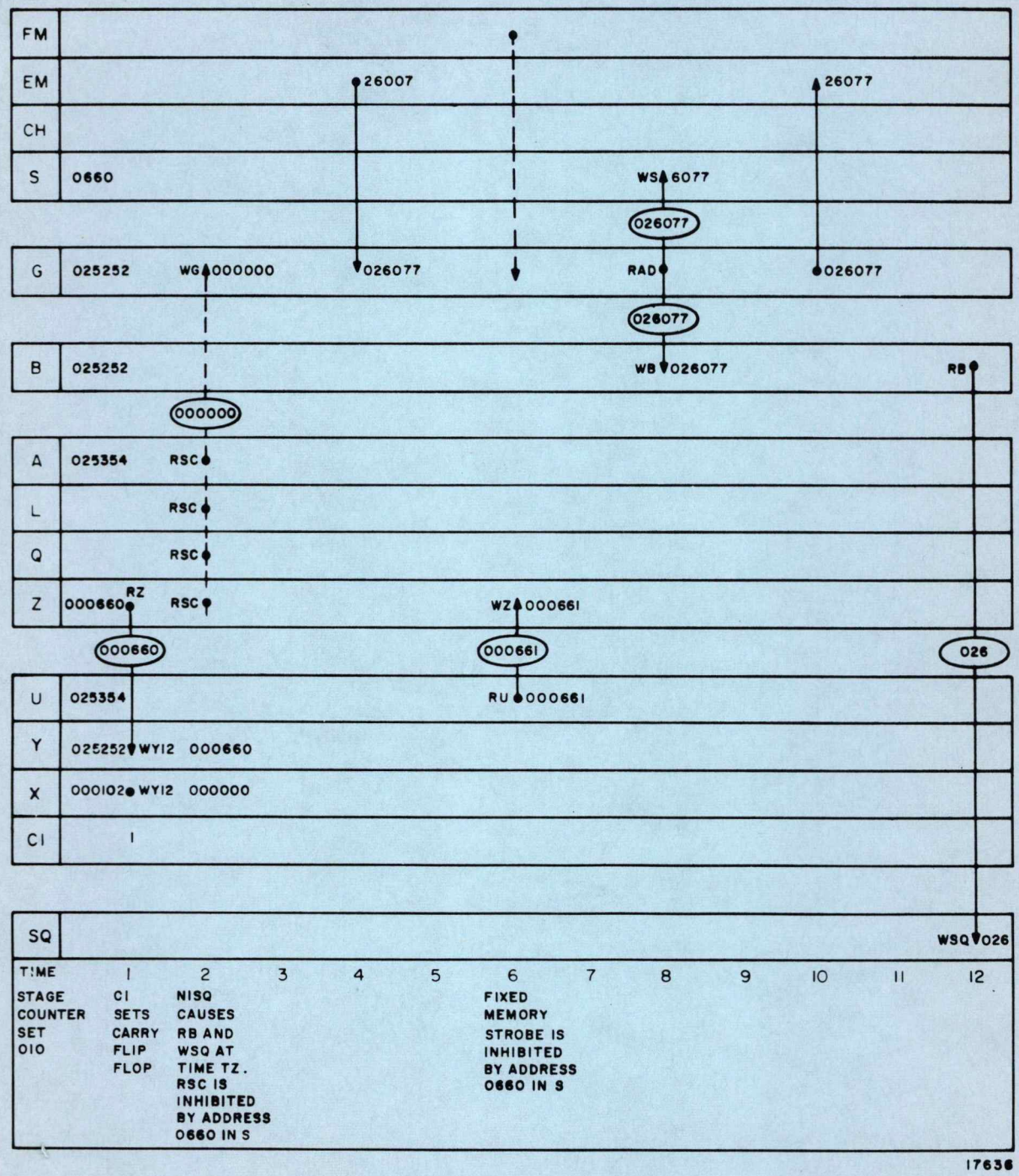


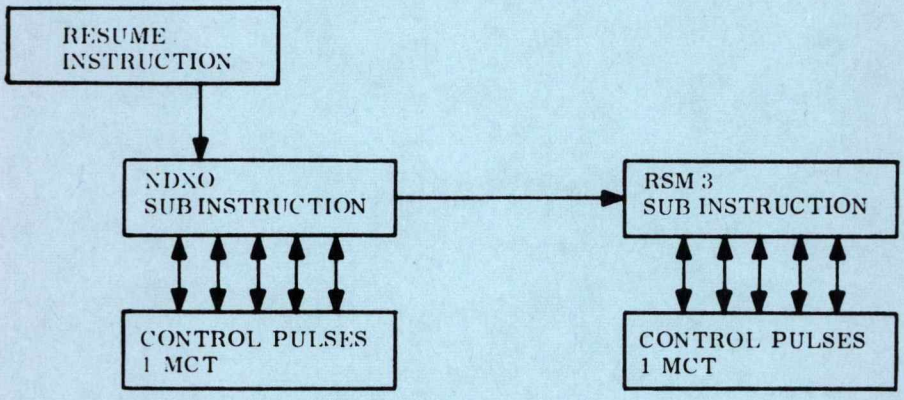
Figure 10-26c. Subinstruction STD2, Data Transfer Diagram

RESUME INSTRUCTION

PURPOSE: TO OBTAIN PREVIOUSLY STORED B AND Z REGISTER INFORMATION FROM ERASABLE MEMORY AND WRITE THEM BACK INTO THEIR RESPECTIVE REGISTERS.

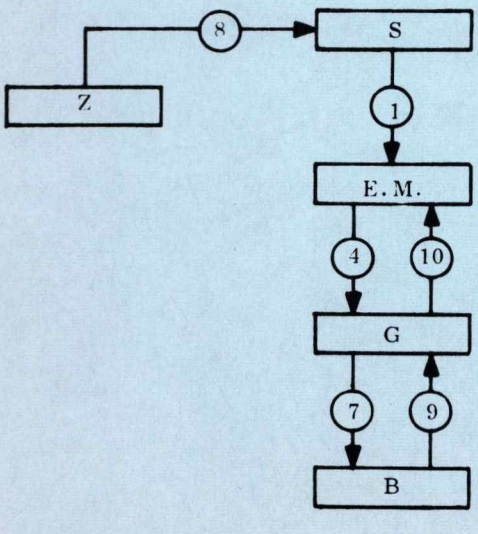
TO TAKE NEXT INSTRUCTION FROM RETURN ADDRESS (B REGISTER).

FLOW DIAGRAM



REGISTER UTILIZATION

(NDXO SUB INSTRUCTION)



(RSM3 SUB INSTRUCTION)

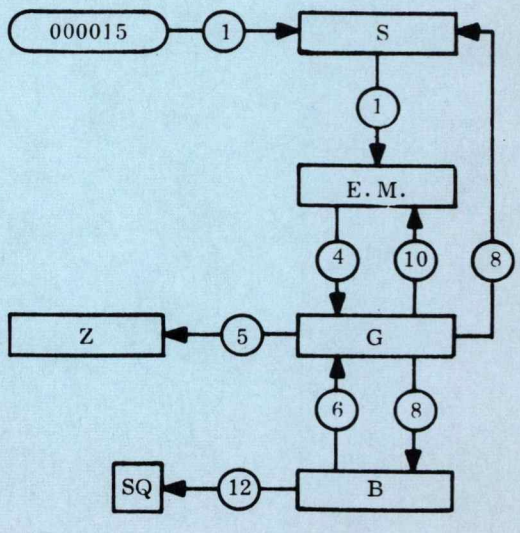


Figure 10-27a. Register Utilization for Resume Instruction, Flow Diagram

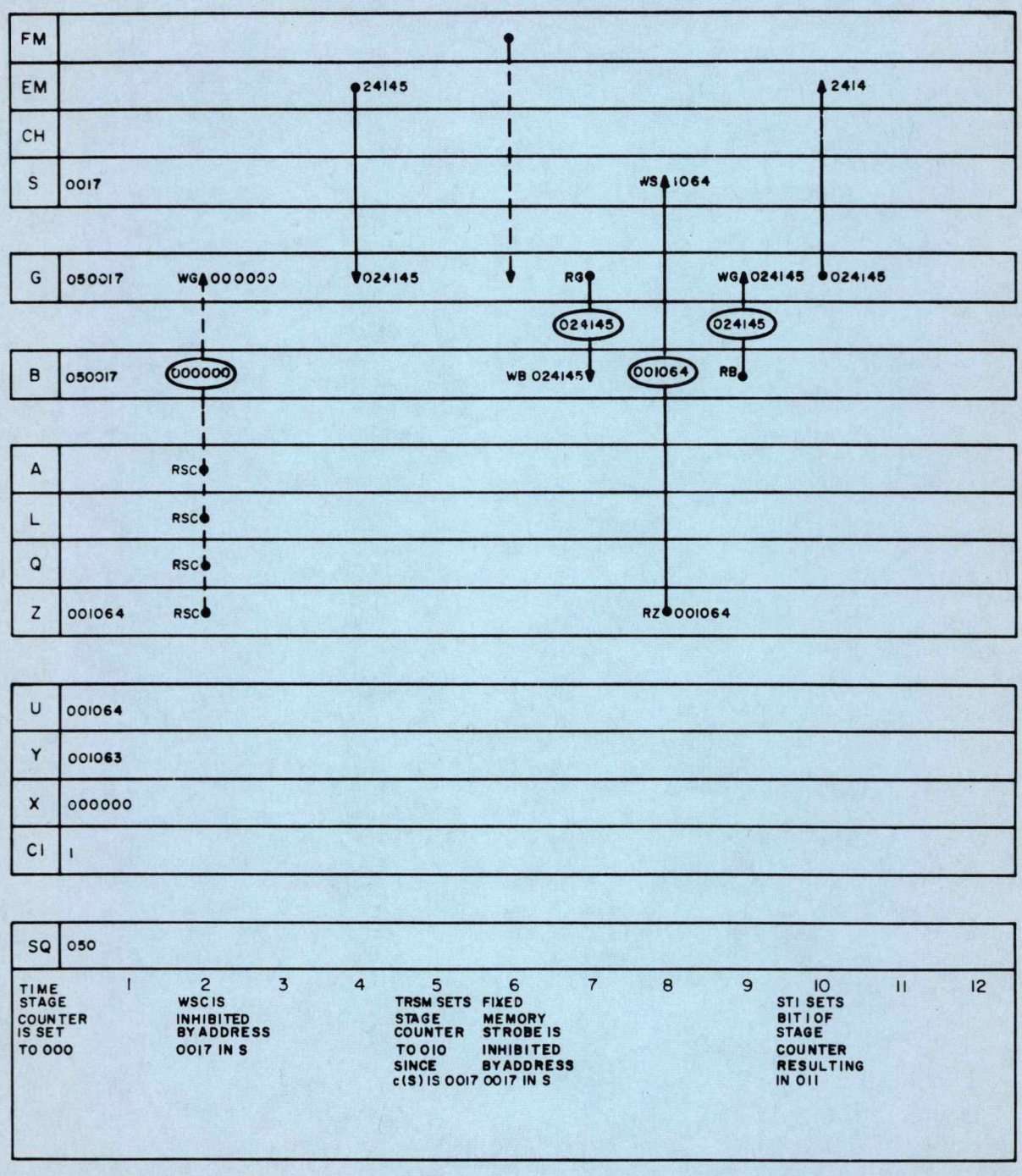


Figure 10-27b. Subinstruction NDX0, with Implied Address Code RESUME, Data Transfer Diagram

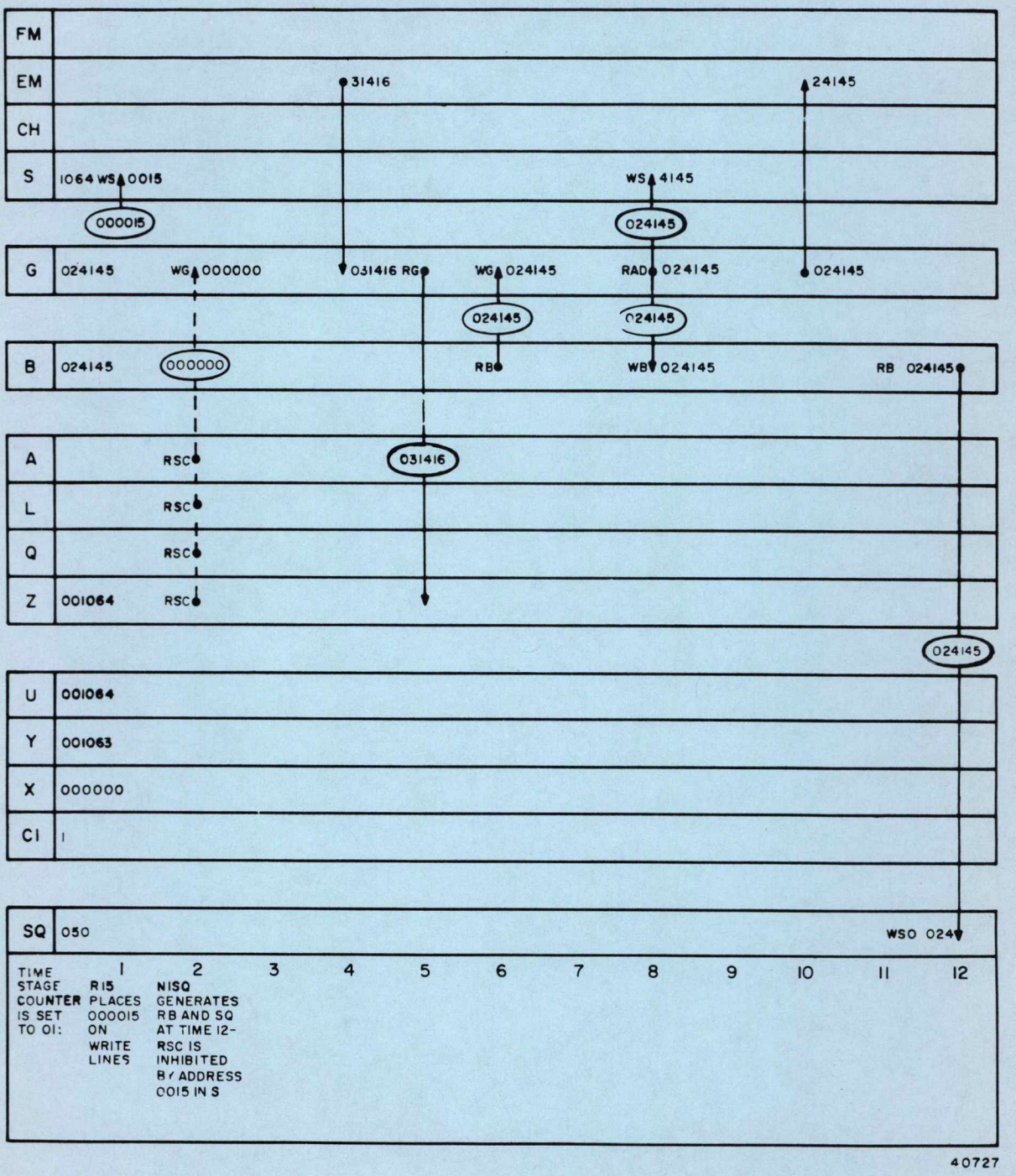


Figure 10-27c. Subinstruction RSM3, Data Transfer Diagram

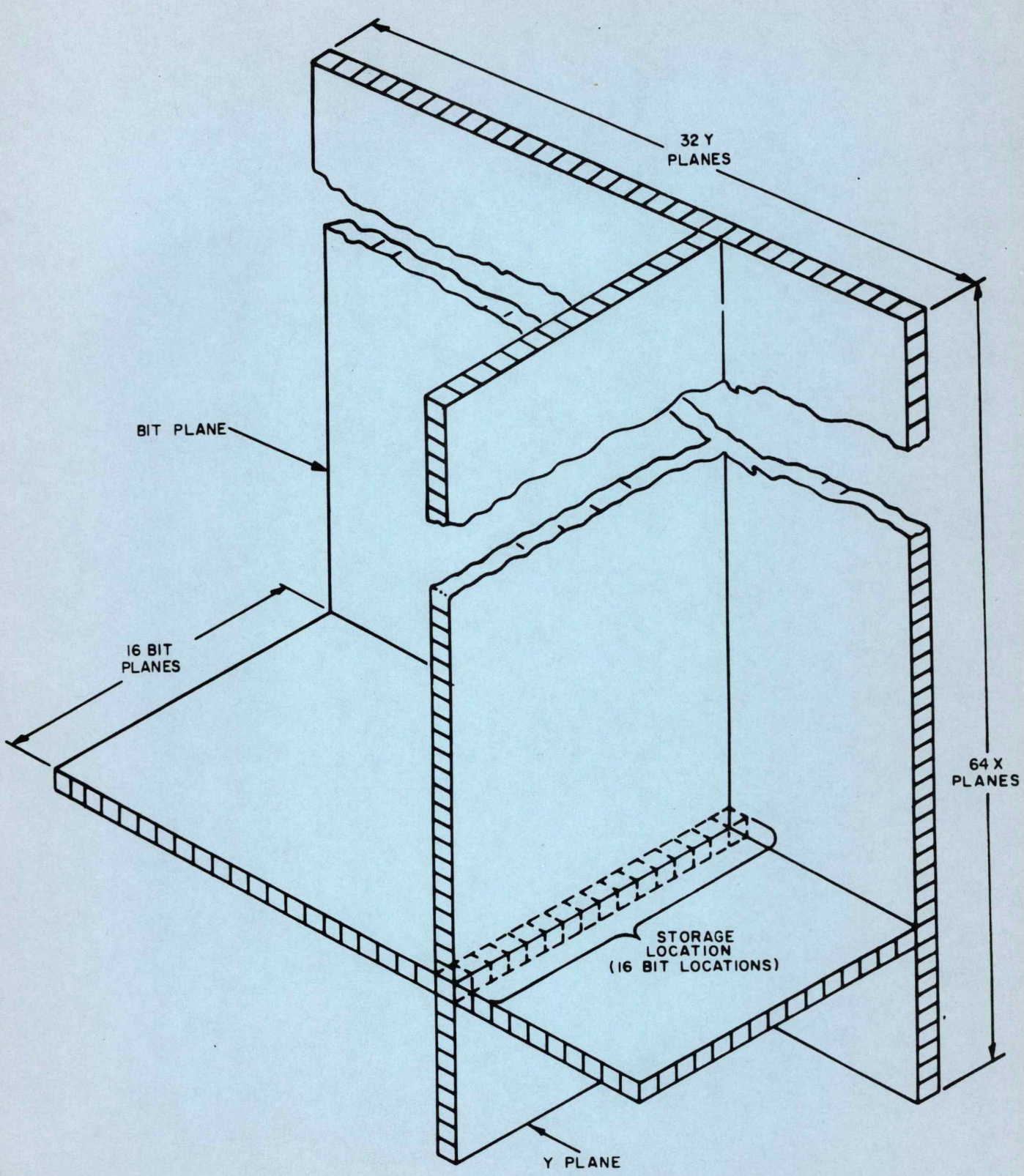
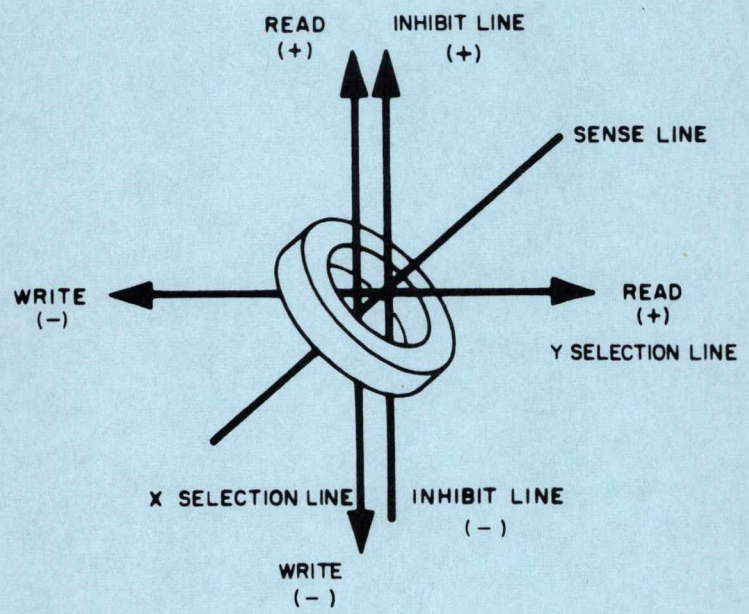


Figure 10-28. Erasable Memory Core Array



FUNCTION	X	Y	INHIBIT
WRITE ONE	$-\frac{1}{2} I_X$	$-\frac{1}{2} I_Y$	0
WRITE ZERO	$-\frac{1}{2} I_X$	$-\frac{1}{2} I_Y$	$+\frac{1}{2} I_i$
READ (CLEAR)	$+\frac{1}{2} I_X$	$+\frac{1}{2} I_Y$	0

Figure 10-29. Erasable Memory Core Threading

tion is a write current. Therefore, the total read current = +I. A read current = +I will try to switch the core to a zero state. If the core was in a one state prior to the generation of the read currents, the core will switch to a zero state and a pulse indicating a logic one will be induced on the sense line. If the core was in a zero state prior to the generation of the read currents, the core will remain in the zero state, no switching will occur, and no pulse will be induced on the sense line; this indicates that a zero was stored in the core. Note that the logic one stored in the core was destroyed after the core was read.

To write a 1 into the core, -1/2 I is passed through the X and Y selection wires. Thus, an attempt is made to switch the core to the 1 state. The two currents add and cause a switching to take place unless it is desired to write a 0 into the core. In this case, the inhibit line will carry + 1/2 I opposing the X selection line current. Thus, the total current passing through the core is -1/2 I. This is not sufficient to switch the core, hence, a logic zero remains in the core. In order to write into a core, it must be cleared. This amounts to reading the core as described above.

The core array consists of 32,768 cores wired as described above. Figure 10-28 shows an X plane and Y plane intersecting to form a word. This intersection represents 16 cores, each core being a bit in the word. A single bit location is defined by the intersection of an X plane, a Y plane, and a bit plane. There are 16 bit planes, each containing 2048 bit locations, e.g., bit number five (5) of every word. Each core in a bit plane is threaded diagonally by a common sense line and vertically by a common inhibit line. (See figure 10-30.) Since a unique sense line threads all cores in a given bit plane, current will be induced into the line if the state of any core is changed. similarly, current through the inhibit line prevents every core in the bit plane from changing to the 1 state during the writing process. Each X plane and each Y plane is threaded by a common selection line. Choosing one of 32 Y and one of 64 X selection lines will choose 1 word of 2048 in erasable memory.

10.10.5.2 Addressing Erasable Memory. Erasable memory is divided into eight banks, each of which is capable of storing 256 (16 bit) words. These banks are named E-BANK 0 through E-BANK 7 (figure 10-31). E-BANK 0 contains 207 locations for general use; the other 49 locations have specific uses: 29 are used for counters, 12 have special functions, 8 are not used. The addresses of the eight unused locations are used to address registers in the central processor. All locations in E-BANK 1 through E-BANK 7 are utilized for general use.

E-BANK 0, 1 and 2 are referred to as unswitched erasable memory because all of their locations (as well as the addressable central processor registers) can be addressed by entering their addresses into register S without regard for what might be contained in register E BANK. E-BANK 3 through E-BANK 7 are referred to as switched erasable memory because all of their locations can be addressed only if the respective bank number is contained in register E BANK. Locations in unswitched erasable memory can also be addressed in the same manner as switched erasable memory if the proper bank number is contained in register E BANK and bits 9 and 10 of register S are logic 1's.

Figure 10-32 is a general block diagram of erasable memory and its associated circuitry. The first twelve bits of an instruction word constitute the address portion of the instruction. These bits are loaded into the S register and then applied to the address decoder. If either bit 11 or bit 12 or both is a logic 1, then fixed memory is being addressed and the erasable memory circuitry is not enabled, i.e., bit 11 and bit 12 of register S must be a logic 0 if erasable memory is to be addressed. If bits 9 and 10 of register S are logic 1's, then register E BANK is enabled and its three bits are also applied to the address decoder.

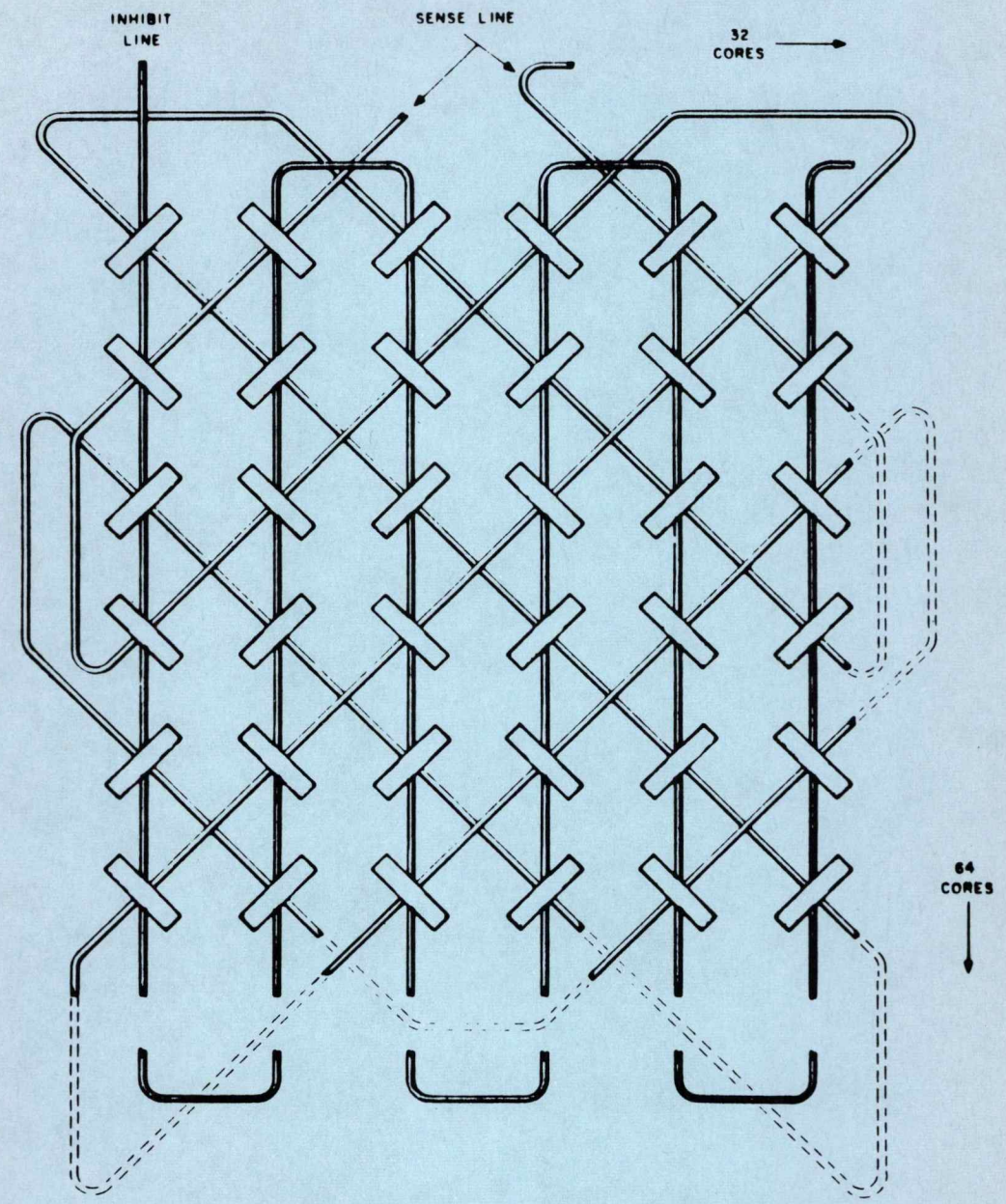


Figure 10-30. Bit Plane

	Register or Location Groups		C(E-Bank)			C(S)											
			11	10	9	12	11	10	9	8	7	6	5	4	3	2	1
Unswitched Erasable Memory	E-Bank 0	Central Processor	x	x	x	0	0	0	0	0	0	0	0	0	y	y	y
			0	0	0	0	0	1	1	0	0	0	0	0	y	y	y
		Special Locations	x	x	x	0	0	0	0	0	0	0	y	y	y	y	y
			0	0	0	0	0	1	1	0	0	0	y	y	y	y	y
		Counters	x	x	x	0	0	0	0	0	0	y	y	y	y	y	y
			0	0	0	0	0	1	1	0	0	y	y	y	y	y	y
		General Use	x	x	x	0	0	0	0	y	y	y	y	y	y	y	y
			0	0	0	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 1		x	x	x	0	0	0	1	y	y	y	y	y	y	y	y
			0	0	1	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 2		x	x	x	0	0	1	0	y	y	y	y	y	y	y	y
			0	1	0	0	0	1	1	y	y	y	y	y	y	y	y
Switched Erasable Memory	E-Bank 3		0	1	1	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 4		1	0	0	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 5		1	0	1	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 6		1	1	0	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 7		1	1	1	0	0	1	1	y	y	y	y	y	y	y	y

Y Means 0 or 1 as defined by address

X Means 0 or 1 which does not have an effect on addressing

Figure 10-31. **Erasable Addressing**

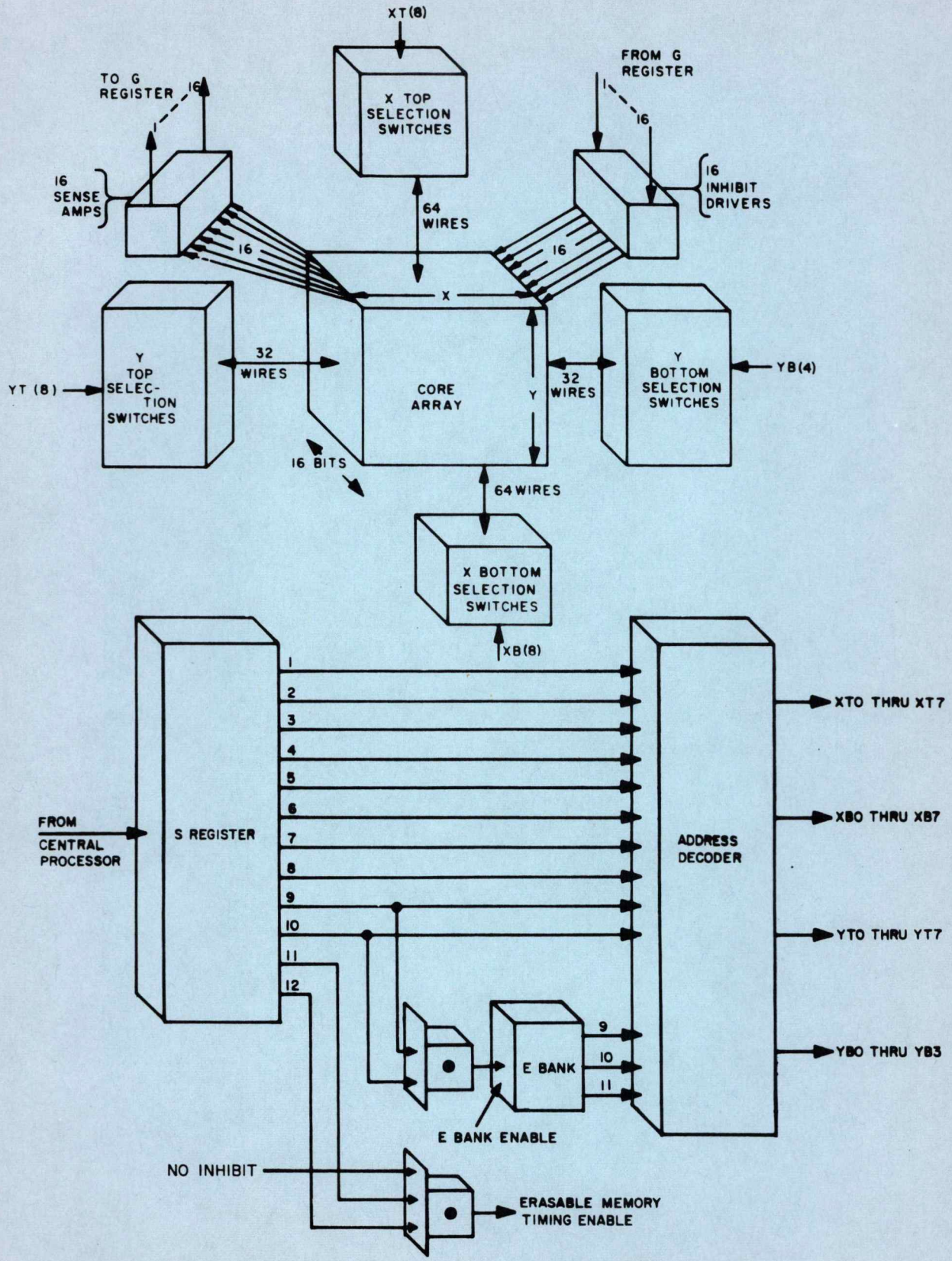


Figure 10-32. **Erasable Memory Block Diagram**

The address decoder generates signals XB0 through XB7, XT0 through XT7, YB0 through YB3 and YT0 through TY7. There are 64X selection and 32Y selection lines associated with erasable memory. A conbination of an X selection and a Y selection line determine a unique location (16 bit) in erasable memory. Figure 10-33 lists the outputs of the address decoder and the inputs required to generate a given output. Note that the address decoder can generate 64 separate combinations of an XT and an XB signal (8 x 8) and 32 separate combinations of a YT and YB signal (8 x 4). Note also that the XB's, XT's and YB's are a result of information located in the S register while the YT's are a result of information located in the E BANK or S registers.

Figures 10-34 and 10-35 are block diagrams of the circuitry involved in determining a particular X and Y selection line so that a unique location can be read from or written into erasable memory.

The following is an example of how a location in erasable memory is addressed. After the example, a detailed view of the selection switches involved will be presented.

Assume that the S register contains 001, 100, 000, 110 and that the E BANK register contains 10^{o}. Using figure 10-33 it is seen that signals XB6, XT0, YB0 and YT4 are logic 1's while the other listed signals are logic 01s; note that bits 11 and 12 of the S register are logic 0's; therefore, erasable memory is addressed. Note also that bits 9 and 10 are logic 1's; therefore, register E BANK selects the YT signal. From figure 10-31 it can be seen that the location addressed is in E BANK 4. Assume that we wish to read the addressed location. In figure 10-35, only the switches that are selected by logic 1 outputs of the address decoder can pass current; therefore, the switches associated with outputs YB0 and YT4 can pass current while the others cannot. Consequently, a Y selection line has been selected. Also, in figure 10-35, only the switches that are selected by the address decoder can pass current. Using the same process as above, it can be seen that an X selection line has been selected, therefore, a specific location (16 bit word) in erasable memory has been read out.

The core switches are not a part of the core array. They are, however, magnetic cores with storage properties. The cores act as small transformers as well as storage devices. The YB0 and YT4 pulses will be generated simultaneously. This causes the switch transistors to be momentarily biased on since their core windings are wired the same as the control pulses. Thus, current will flow in the read direction (from B+ to ground) through one of 32 Y selection wires. In addition, the cores are switched. The cores essentially remember the location which is being read so that the information can be rewritten back into the same location. The information would otherwise be destroyed. To write requires that current be passed in the opposite direction in the same selection wires. The RESET pulse will be routed to all core switches in the selection switch blocks. Only those switches just previously switches will be in a position to switch back to their original state. This will cause the transistors to be biased on, allowing conduction of current in the write direction from B+ to ground. Note that the diodes simply steer the current by acting as blocking diodes.

S Register *												
Signal	10	9	Signal	8	7	Signal	6	5	4	Signal	3	2	1
YT0	0	0	YB0	0	0	XT0	0	0	0	XB0	0	0	0
YT1	0	1	YB1	0	1	XT1	0	0	1	XB1	0	0	1
YT2	1	0	YB2	1	0	XT2	0	1	0	XB2	0	1	0
			YB3	1	1	XT3	0	1	1	XB3	0	1	1
						XT4	1	0	0	XB4	1	0	0
						XT5	1	0	1	XB5	1	0	1
						XT6	1	1	0	XB6	1	1	0
						XT7	1	1	1	XB7	1	1	1

E-Bank			
Signal	11	10	9
YT0	0	0	0
YT1	0	0	1
YT2	0	1	0
YT3Ψ	0	1	1
YT4Ψ	1	0	0
YT5Ψ	1	0	1
YT6Ψ	1	1	0
YT7Ψ	1	1	1

* Bits 11 and 12 are both assumed to be logic 0

Ψ Generated only if bits 9 and 10 of register S are both logic 1

Figure 10-33. Address Decoder

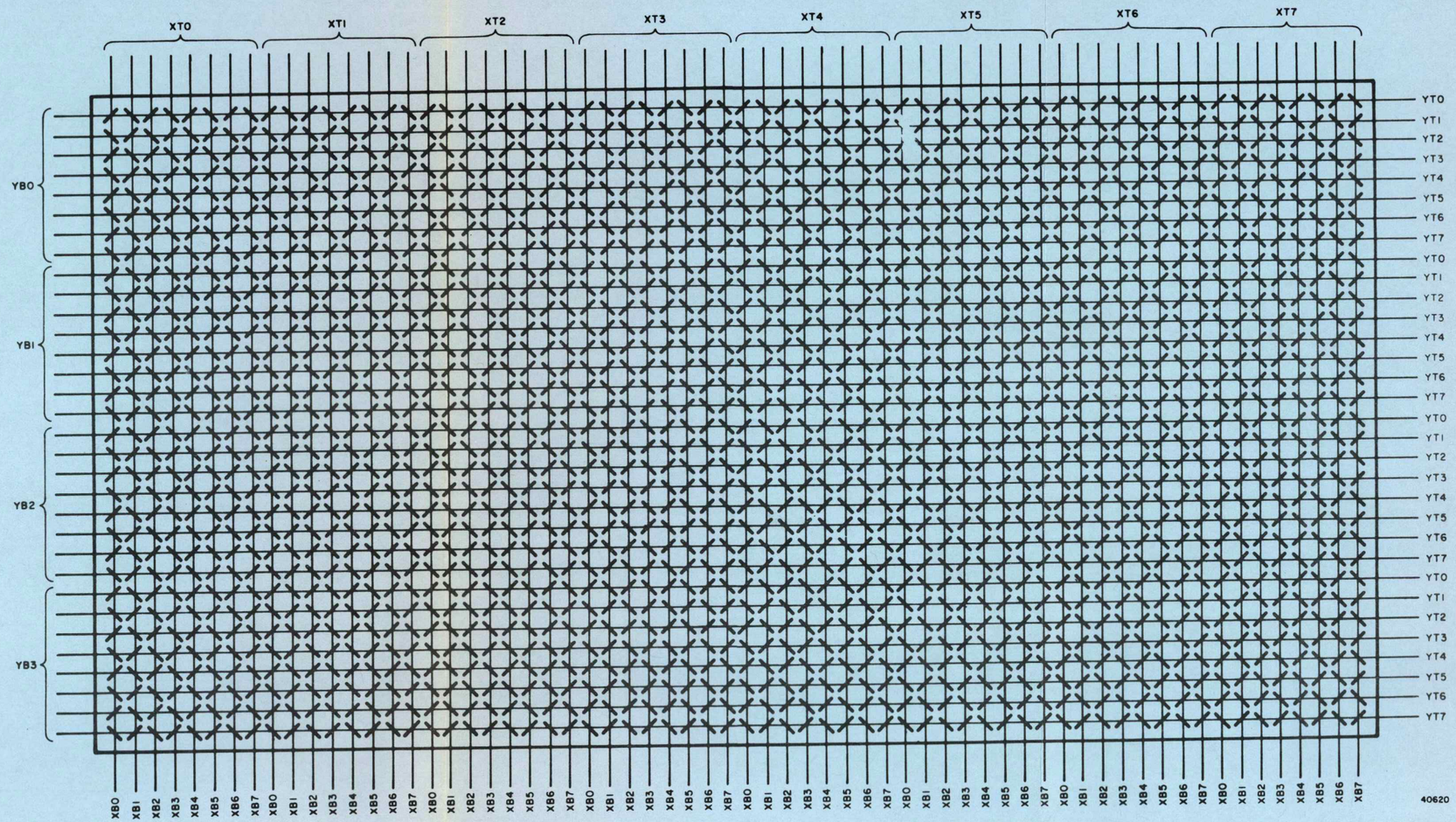
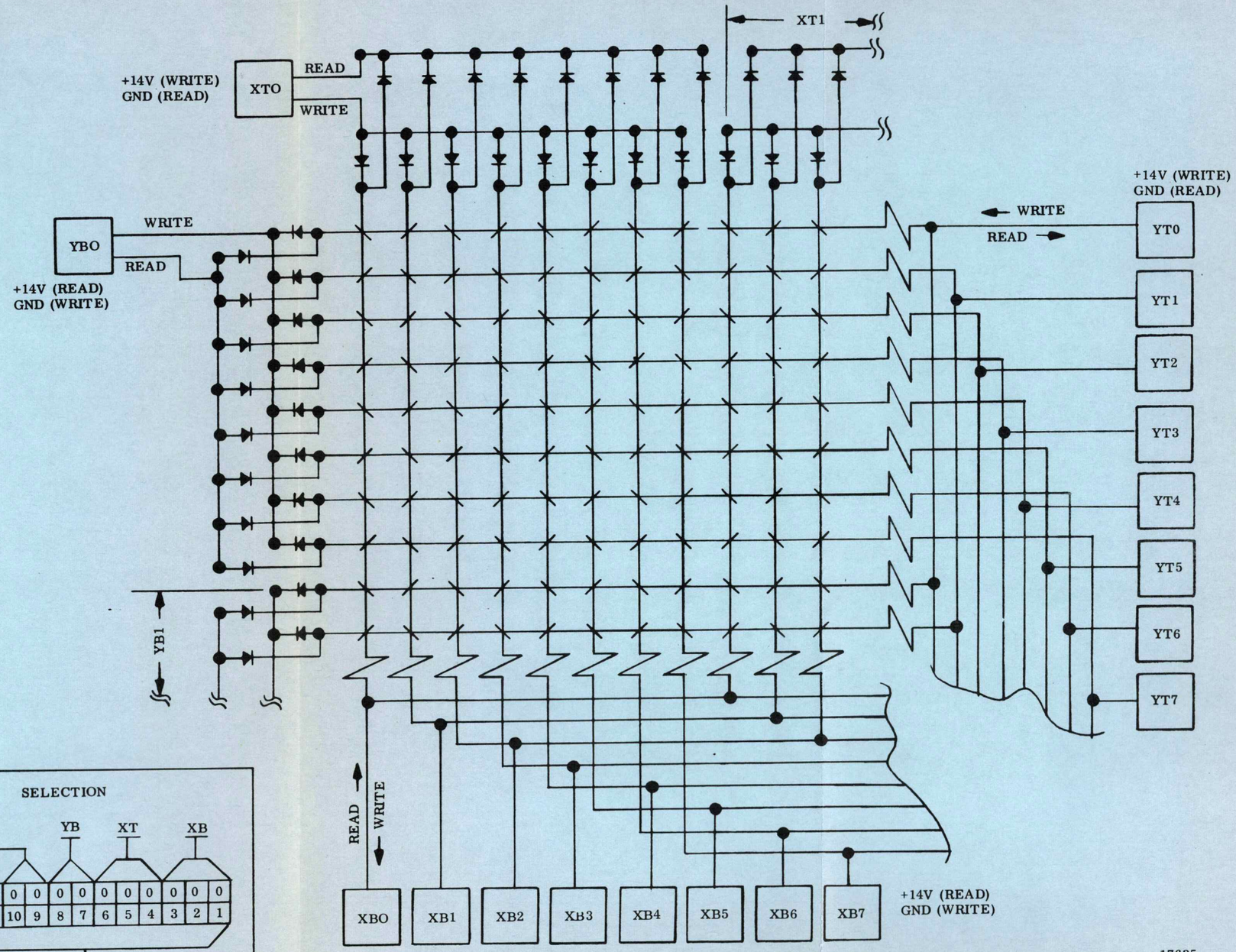
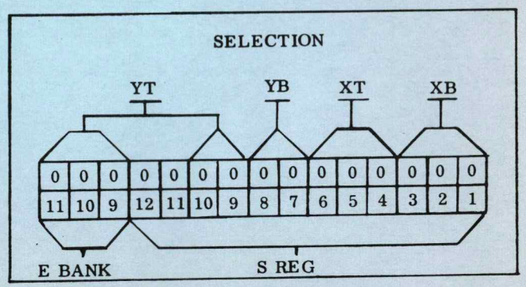


Figure 10-34. X and Y Coordinates





17635

Figure 10-35. Erasable Memory Selection

The X selection circuitry is similar to the Y selection circuitry discussed above. It is the selection of both an X and a Y wire that causes the selection of a 16 bit word. It should be mentioned that whether it is desired to read out or write into erasable memory, the selection procedure and operation of the core switches is the same. If it is desired to simply write a new word into a location, readout will occur, clearing the locations to all zeros. The information read out can be loaded into the G register where it will control the inhibit wires at the time the RESET pulse is issued. All bits in the selected word will switch to a 1 except those which have inhibiting current running through them. The sense amps receive and amplify pulses which are induced into the sense wires during readout. These amplifier pulses are applied to the G register where they are stored as logic ONE's. There are 16 sense amps, one for each bit in the selected word.

Erasable memory timing consists of several flip-flop circuits which produce the timing signals for erasable memory (see figure 10-36). These timing signals are produced in one memory cycle time (T01 through T12). At time $\overline{T03}$ a set signal (SETEK) is generated to enable the core selection switches to be addressed and read strobes (REX and REY) are generated to enable the selected data to be read out of memory. At time $\overline{T04}$, the sense strobe signal (SBE) is generated to enable the sense amplifiers to supply memory data to the G register. At time $\overline{T10}$ information is written into erasable memory using the reset, inhibit, and write strobes. The reset strobes (RSTKX and RSTKY) enable the reset drivers, thereby clearing the addressed memory location prior to writing in data. The inhibit strobe (ZID) enables the inhibit gates and the write strobes (WEX and WEY) enable data to be written into a particular memory address.

10.10.5.3 Fixed Memory Core Array. Figure 10-37 illustrates the use of the magnetic core in the rope core memory. This hypothetical model consists of 4 cores (edge views) labelled CORE 0 through CORE 3. Each core stores one 4-bit word, labelled WORD 0 through WORD 3. The bit configuration of each word is determined by whether the particular sense wires are routed through the hole or around the hole. The associated table in figure 10-37 shows the bit configuration that would be produced on the sense wires if the associated core were switched. Only one core could be switched at any one time. The problem becomes one of selecting the desired core to be switched. A two-bit address could be used to uniquely define any one of 4 cores.

The A and B inhibit lines (along with their complements) represent the bit configuration of the two-bit address. These wires are routed in and out of the 4 cores in order to select only one core.

Assume that it is desired to read WORD 2 from fixed memory. In figure 10-37, the direction of the arrows indicates the direction of current flow. Lines that are broken at the core pierce the core. Lines that are continuous at the core are routed around the core. Before reading a core, a current I is passed through the RESET line switching all cores into one state of magnetism. Currents are then passed through the SET line, $\overline{A}$ line and B line simultaneously in the direction shown. The current I in the SET line attempts to switch all cores back to the original state. However, the inhibit wires, $\overline{A}$ and B, carry current = 1/2 I in the opposite direction in order to oppose the SET current and cancel its effects. All cores except one will receive inhibiting current.

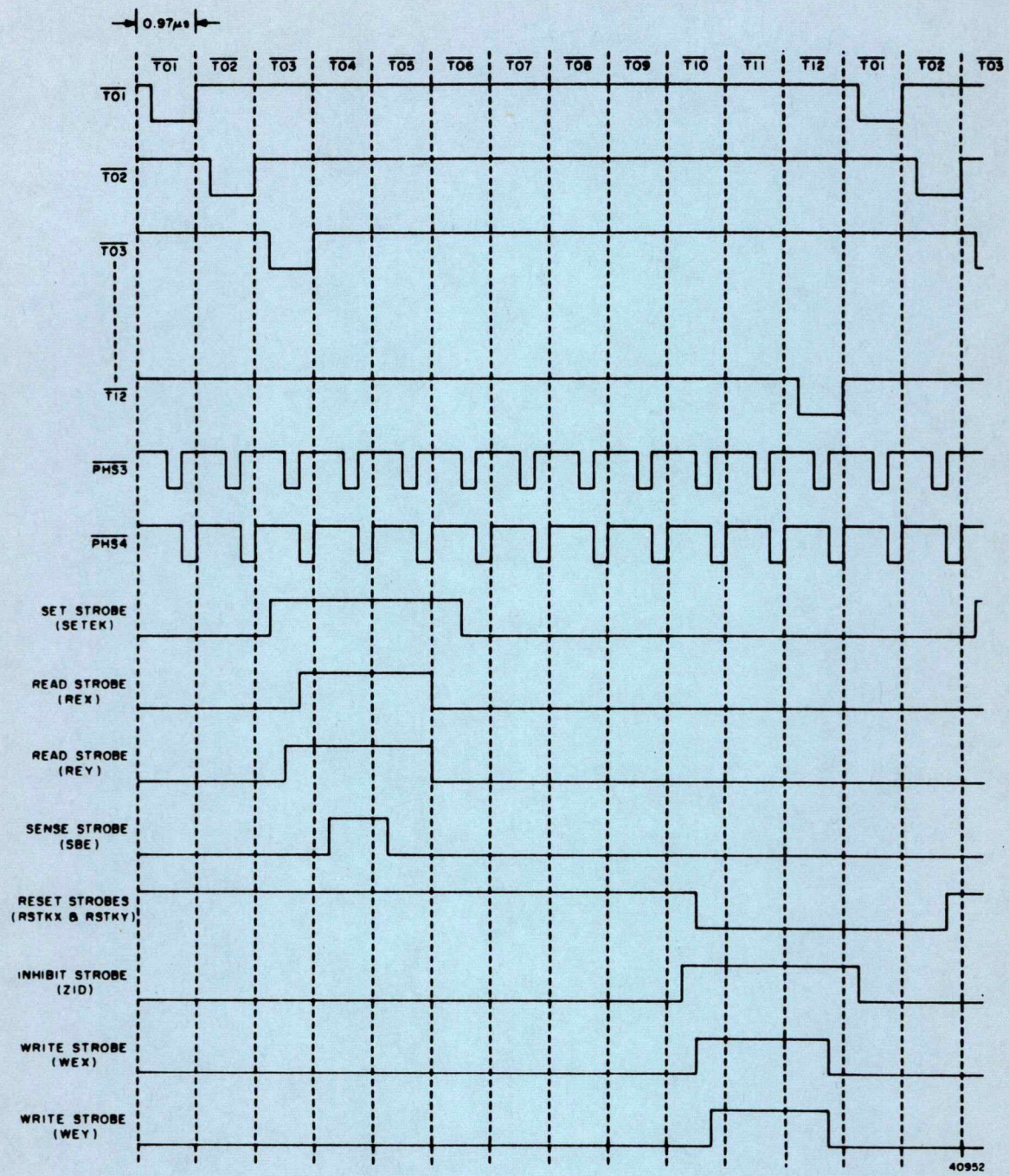
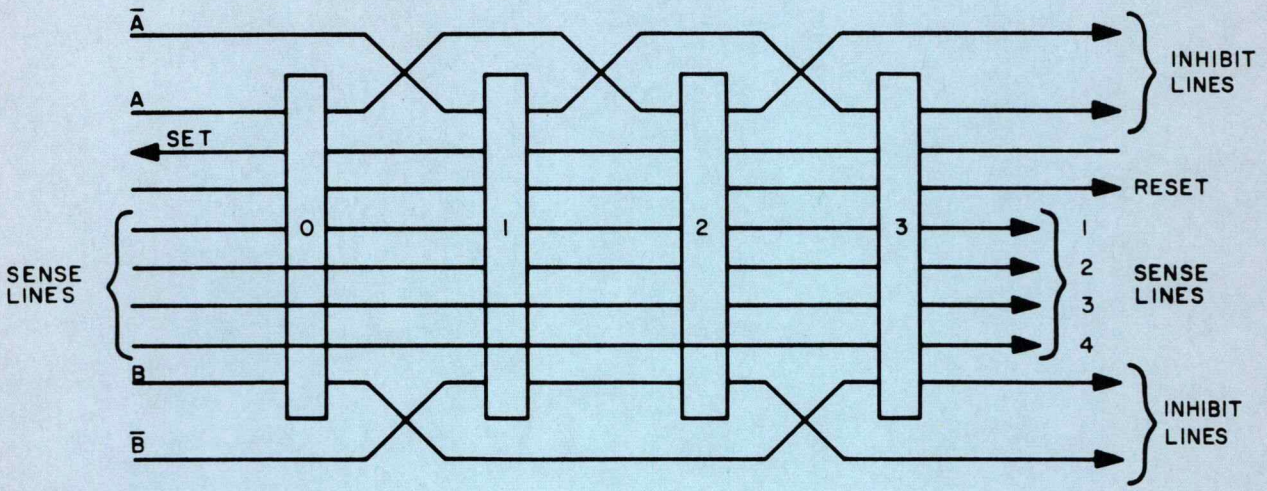


Figure 10-36. Erasable Memory Timing Diagram



	INHIBIT LINES				SENSE LINES				
	A	Ā	B	B̄	4	3	2	1	
CORE 0		X		X	0	0	0	1	WORD 0
CORE 1	X		X		0	0	1	1	WORD 1
CORE 2		X	X		0	1	1	1	WORD 2
CORE 3	X			X	1	1	1	1	WORD 3

X INDICATES INHIBIT LINES NECESSARY TO ENABLE CORE SWITCHING

Figure 10-37. Sample Rope Core

Note that CORE 2 is not pierced by the $\overline{A}$ or B inhibit line. Therefore, CORE 2 changes state. This changing state produces a changing flux field which induces an electrical pulse in all sense lines which pierce the hole. Thus, SENSE lines 1, 2, and 3 will carry a momentary pulse while SENSE line 4 carries no pulse. The pulses represent logic ONE's while the lack of pulses represents a logic ZERO. The table included in figure 10-37 shows how the inhibit lines are wired to inhibit certain cores from switching. Note that if current is assumed to flow in A, it cannot flow in $\overline{A}$. The same idea applies to B and $\overline{B}$. Additional cores could be added to this model by increasing the number of inhibit lines.

10.10.5.4 Addressing Fixed Memory. Fixed memory consists of three ropes (R, S, T). Each rope is divided into two rope modules; B1 and B2, B3 and B4, B5 and B6, respectively. Each rope module is divided into six banks; therefore, each rope consists of 12 banks and, consequently, fixed memory consists of 36 banks. Each bank is capable of storing 1024 (16 bit) words; therefore, fixed memory has a storage capacity of 36,864 (1024 x 36) 16 bit words. Each core of fixed memory stores 12 16 bit words; therefore, there are 3072 (36,864 ÷ 12) cores in fixed memory. Note that 36 does not divide into 3072 evenly. This means that a given core is not completely associated with a particular bank. See table 10-5.

Table 10-5. Fixed Memory Composition

	/F MEM.	/ROPE	/MODULE	/CORE
ROPES	3	-	-	-
MODULES	6	2	-	-
WORDS	36,864	12,288	6,144	12
CORES	3,072	1,024	512	-
BANKS	36	12	6	-
STRANDS	72	24	12	12
MODULE AREAS	24	8	4	-
SENSE LINES	1,152	384	192	192
INHIBIT LINES	84	28	14	14

Fixed memory cannot be written into, and readout is nondestructive. Information stored in fixed memory is determined solely by the configuration of sense wires running through or around the cores; therefore, the stored information cannot be electrically altered; a rewiring of fixed memory would be necessary to change any programs, constant, or tables stored there.

Each rope module consists of 512 cores and 192 sense lines. The 512 cores are divided into four sections of 128 cores each. The 192 sense lines either thread or bypass each core, i.e., all 192 sense lines are associated with each core. The sense lines are divided into 12 strands of 16 lines each; therefore, a given strand defines one of the twelve words stored in each core, i.e., a given strand in a rope module is associated with 512 16 bit words. When a single core in a rope module is switched, (assume that all cores in the other 5 rope modules can be inhibited from switching), a pulse is induced on those m sense lines threading the core; no pulse is induced on the 192-m sense lines bypassing the core. If only one of the twelve strands is enabled, the location defined by the enabled strand and given core is selected. The method of switching a single core in a rope module is to select one of the four 128 core sections and then inhibit 127 of these cores from switching. The 127 cores are inhibited by information stored in bits 1 through 7 of the S register. Note that 7 binary bits have a capability of defining 128 different configurations.

The contents of register S, F BANK and F EXT are used to select locations in fixed memory for readout. Register S is a 12 bit register while F BANK and F EXT are 5 and 3 bit registers respectively. The addressing scheme employed is capable of defining 65,356 unique locations (table 10-6). The fixed memory address field consists of 64 banks. At the present time, only 36 banks (BANK 00_8 through BANK 43_8) are actually built into the CMC; the addressing scheme, however, allows for the addition of 28 extra banks (BANK 44_8 through BANK 77_8) if necessary.

The first 24 banks (BANK 00_8 through BANK 27_8) are referred to as F EXT-channel X. This group is further divided into two sub-groups: fixed-fixed memory and variable-fixed memory. Fixed-fixed memory consists of BANKS 02_8 and 03_8 and can be addressed by two different methods: (1) bits 12 and 11 of register S are 1 and 0 or 1 and 1 respectively, the contents of F BANK and F EXT are irrelevent; (2) bits 12 and 11 of register S are 0 and 1 respectively, the contents of F BANK are 00010 or 00011, the contents of F EXT are irrelevant. It should be noted, therefore, that each location in fixed-fixed memory can be addressed by two different methods. Variable-fixed memory consists of BANKS 00_8, 01_8 and 04_8 through 27_8. These locations are addressed by the S and F BANK registers only: their locations are not addressed by the contents of F EXT.

BANKS 30_8 through 37_8 are referred to as F EXT-channel 0-3. The locations in these banks are addressed if the F EXT register contains 000_2 through 011_2, the F BANK register contains 11000_2 through 11111_2 and bits 12 and 11 of register S are 0 and 1 respectively. "Channel 0-3" is so designated because 000_2 through 011_2 is equivalent to 0_8 through 3_8.

There are four other F EXT-channel groups: F EXT-channel 4 through F EXT-channel 7. Note that the channel numbers are a result of the contents of the F EXT register, e.g., when F EXT contains $101_2 = 5_8$ then the locations in the F EXT-channel 5 group are addressed.

Register or Location Groups		FMA Octal Address	F EXT Register	F Bank Register					S Register											
			7 6 5	16	14	13	12	11	12	11	10	9	8	7	6	5	4	3	2	1
Fixed-Fixed Memory	F-Bank 02	04000-05777	x x x x x x	x 0	x 0	x 0	x 1	x 0	1 0	0 1	y y	y y	y y	y y	y y	y y	y y	y y	y y	y y
	F-Bank 03	06000-07777	x x x x x x	x 0	x 0	x 0	x 1	x 1	1 0	1 1	y y	y y	y y	y y	y y	y y	y y	y y	y y	y y
F EXT Channel X Variable Fixed	F-Bank 00	00000-01777	x x x	0	0	0	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 01	02000-03777	x x x	0	0	0	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 04	10000-11777	x x x	0	0	1	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 05	12000-13777	x x x	0	0	1	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 06	14000-15777	x x x	0	0	1	1	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 07	16000-17777	x x x	0	0	1	1	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 10	20000-21777	x x x	0	1	0	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 11	22000-23777	x x x	0	1	0	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 12	24000-25777	x x x	0	1	0	1	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 13	26000-27777	x x x	0	1	0	1	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 14	30000-31777	x x x	0	1	1	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 15	32000-33777	x x x	0	1	1	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 16	34000-35777	x x x	0	1	1	1	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 17	36000-37777	x x x	0	1	1	1	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 20	40000-41777	x x x	1	0	0	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 21	42000-43777	x x x	1	0	0	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 22	44000-45777	x x x	1	0	0	1	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 23	46000-47777	x x x	1	0	0	1	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 24	50000-51777	x x x	1	0	1	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 25	52000-53777	x x x	1	0	1	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 26	54000-55777	x x x	1	0	1	1	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 27	56000-57777	x x x	1	0	1	1	1	0	1	y	y	y	y	y	y	y	y	y	y
F EXT Channel 0-3	F-Bank 30	060000-061777	0 x x	1	1	0	0	0	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 31	062000-063777	0 x x	1	1	0	0	1	0	1	y	y	y	y	y	y	y	y	y	y
	F-Bank 32	064000-065777	0 x x	1	1	0	1	0	0	1	y	y	y	y	y	y	y	y	y	y

Table 10-6. Fixed Memory Addressing
(Sheet 1 of 3)

Register or Location Groups		FMA Octal Address	F EXT Register	F Bank Register	S Register
			7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
F EXT Channel 0-3	F-Bank 33	066000-067777	0 x x	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 34	070000-071777	0 x x	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 35	072000-073777	0 x x	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 36	074000-075777	0 x x	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 37	076000-077777	0 x x	1 1 1 1 1	0 1 y y y y y y y y y y
F EXT Channel 4	F-Bank 40	100000-101777	1 0 0	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 41	102000-103777	1 0 0	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 42	104000-105777	1 0 0	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 43	106000-107777	1 0 0	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 44	110000-111777	1 0 0	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 45	112000-113777	1 0 0	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 46	114000-115777	1 0 0	1 1 1 1 0	0 1 y y y y y y y y y y
F EXT Channel 5	F-Bank 47	116000-117777	1 0 0	1 1 1 1 1	0 1 y y y y y y y y y y
	F-Bank 50	120000-121777	1 0 1	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 51	122000-123777	1 0 1	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 52	124000-125777	1 0 1	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 53	126000-127777	1 0 1	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 54	130000-131777	1 0 1	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 55	132000-133777	1 0 1	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 56	134000-135777	1 0 1	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 57	136000-137777	1 0 1	1 1 1 1 1	0 1 y y y y y y y y y y
F EXT Channel 6	F-Bank 60	140000-141777	1 1 0	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 61	142000-143777	1 1 0	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 62	144000-145777	1 1 0	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 63	146000-147777	1 1 0	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 64	150000-151777	1 1 0	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 65	152000-153777	1 1 0	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 66	154000-155777	1 1 0	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 67	156000-157777	1 1 0	1 1 1 1 1	0 1 y y y y y y y y y y

Table 10-6. Fixed Memory Addressing
(Sheet 2 of 3)

Register or Location Groups		FMA Octal Address	F EXT Register	F Bank Register	S Register
			7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
F EXT Channel 7	F-Bank 70	160000-161777	1 1 1	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 71	162000-163777	1 1 1	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 72	164000-165777	1 1 1	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 73	166000-167777	1 1 1	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 74	170000-171777	1 1 1	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 75	172000-173777	1 1 1	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 76	174000-175777	1 1 1	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 77	176000-177777	1 1 1	1 1 1 1 1	0 1 y y y y y y y y y y

x means 0 or 1 which does not have an effect on addressing.

y means 0 or 1 as defined by address.

Table 10-6. Fixed Memory Addressing
(Sheet 3 of 3)

Assume that bits 12 and 11 of register S are 0 and 1 respectively. F BANK 00_8 through F BANK 27_8 (F EXT-channel X) are determined by the contents of register F BANK (figure 10-38). F BANK 30_8 through 37_8 (F EXT-channel 0-3) are also determined by the contents of register F BANK (figure 10-38); note, however, that bit 7 of F EXT must be a 0. F BANK 40_8 through F BANK 77_8 are determined by the contents of the F EXT and F BANK registers (figure 10-39). This figure shows how F BANK 54_8 is addressed. Note that bits 16 and 14 of register F BANK are both 1's for all F BANK's except those in F EXT-channel X.

Table 10-6 lists all of the fixed memory addresses (FMA's). Assume again that bits 12 and 11 or reigster S are 0 and 1 respectively. The location in F BANK 00_8 through 27_8 are designated by a five digit octal number which is determined by the contents of the S and F BANK registers. Figure 10-40 illustrates how location 42113_8 is addressed. Note that bits 11 and 12 of register S are not used in determining address 42113_8. The locations in F BANK 30_8 through 37_8 are designated by a six digit octal number which is determined by the contents of the S and F BANK registers and bit 7 of the F EXT register. Figure 10-41 illustrates how location 074356_8 is addressed. The location in F BANK 40_8 through 77_8 are designated by a six digit octal number which is determined by the contents of the S, F BANK and F EXT registers. Figure 10-42 illustrates how location 151444_8 would be addressed.

Figure 10-43 is a block diagram of the selection logic connected with fixed memory.

A fixed memory address is selected by generating several selection signals:

a. Rope select.

b. Module select.

c. Set.

d. Reset.

e. Strand select.

f. Inhibit select.

The rope and module select circuits select one of three ropes (R, S, or T) and one of two modules (HI or LO). Rope modules B1, B3, and B5 are the LO modules. Rope modules B2, B4, and B6 are the HI modules. Therefore, the rope and module select signals select only one module of a particular rope thereby enabling 512 cores or 6144 words (see figure 10-44).

Figure 10-45 illustrates the timing of the remaining selection signals: set, reset, strand, and inhibit. At time $\overline{\text{T08}}$ and $\overline{\text{PHS3}}$, signal IHENV is generated to enable the inhibit driver selection circuits. Refer to figure 10-46. This circuit uses signals S01 through S07 and their NOT functions to generate the inhibit signals necessary to select one of 128 cores in each of the four areas (A, B, C, or D) of each module. This enables four cores or 48 words.

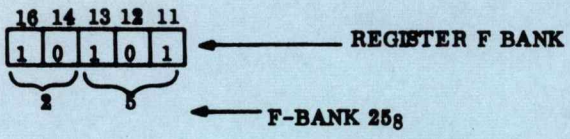


Figure 10-38. F-BANK 00_8 Through 27_8 Determination

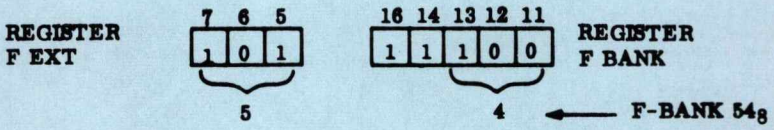


Figure 10-39. F-BANK 40_8 Through 77_8 Determination

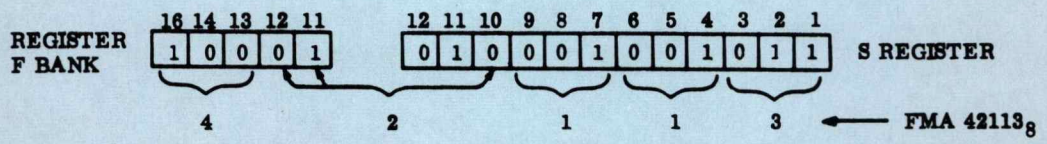


Figure 10-40. FMA 42113_8 Determination

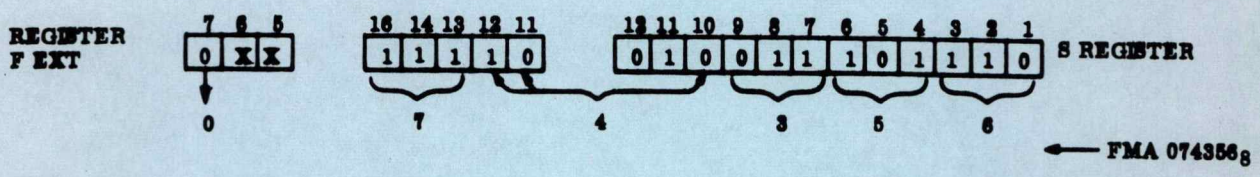


Figure 10-41. **FMA 074356_8 Determination**

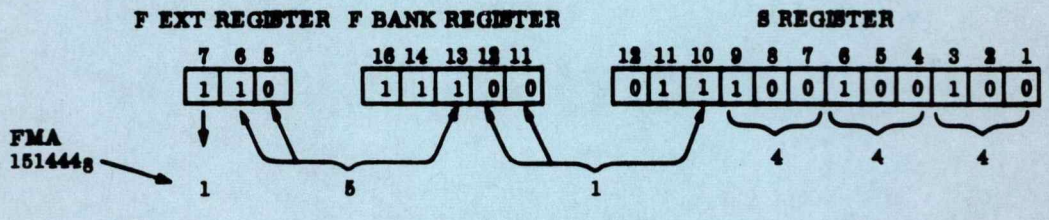


Figure 10-42. **FMA 151444_8 Determination**

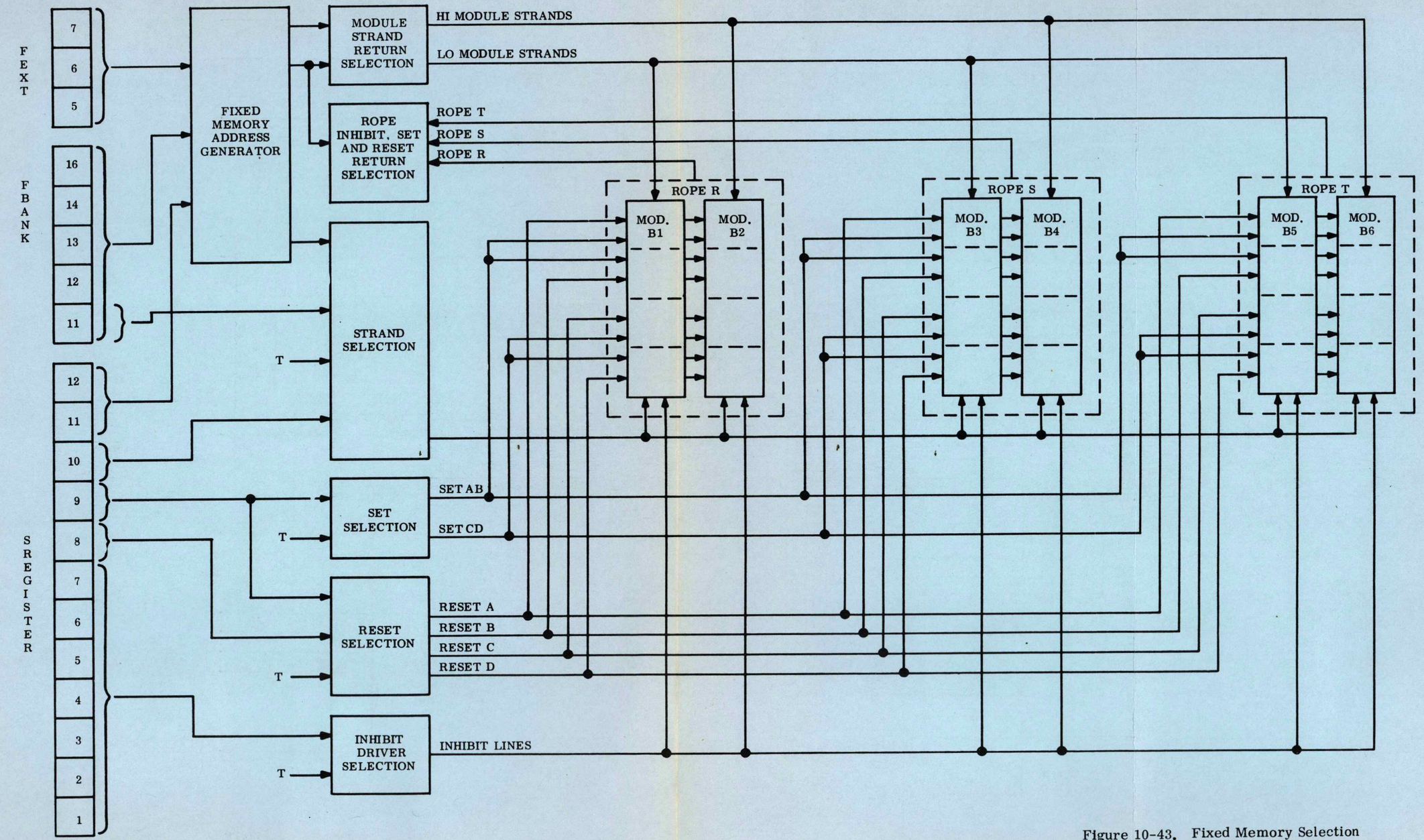


Figure 10-43. Fixed Memory Selection

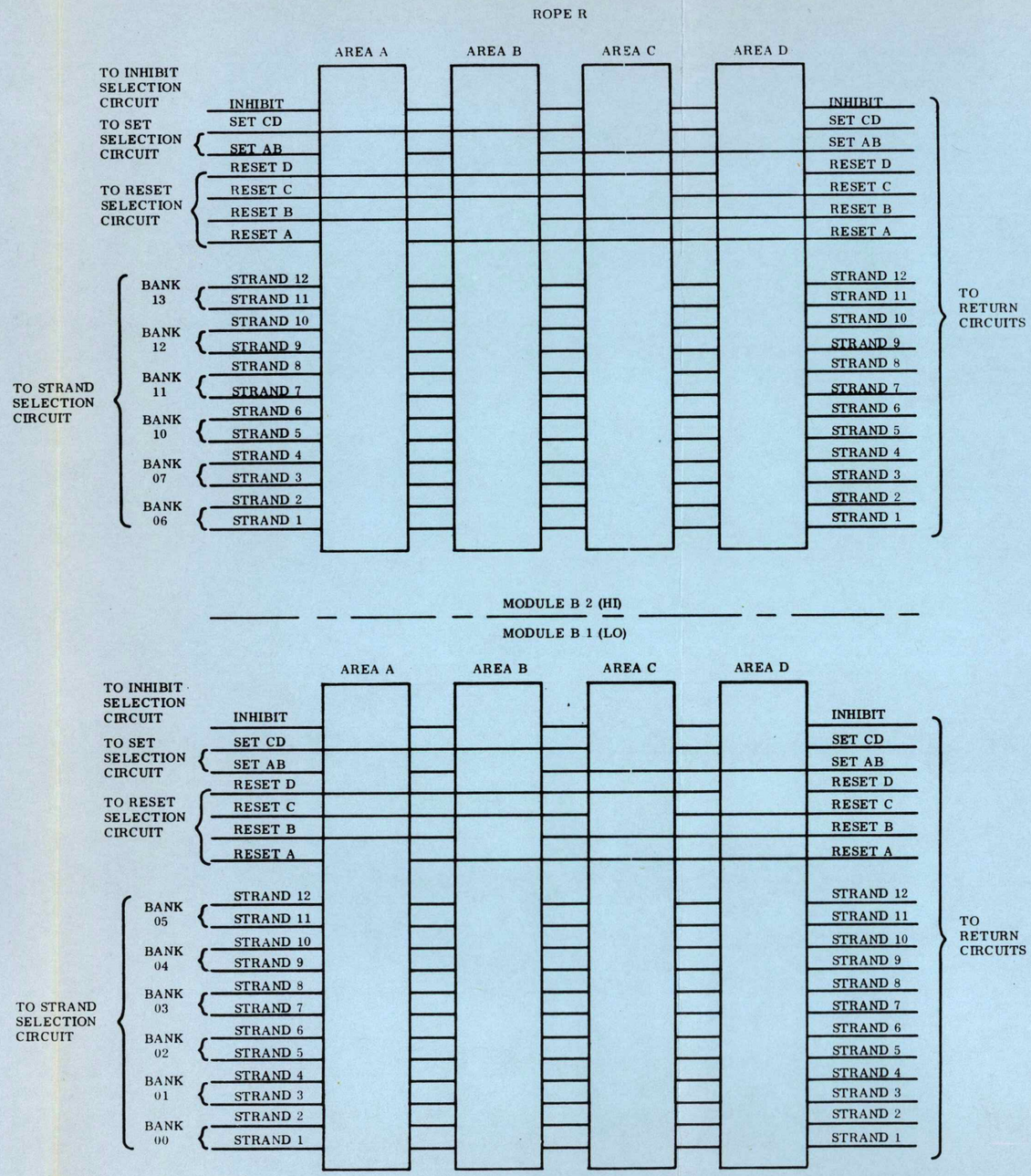


Figure 10-44. Fixed Memory Bank Assignments (Sheet 1 of 3)

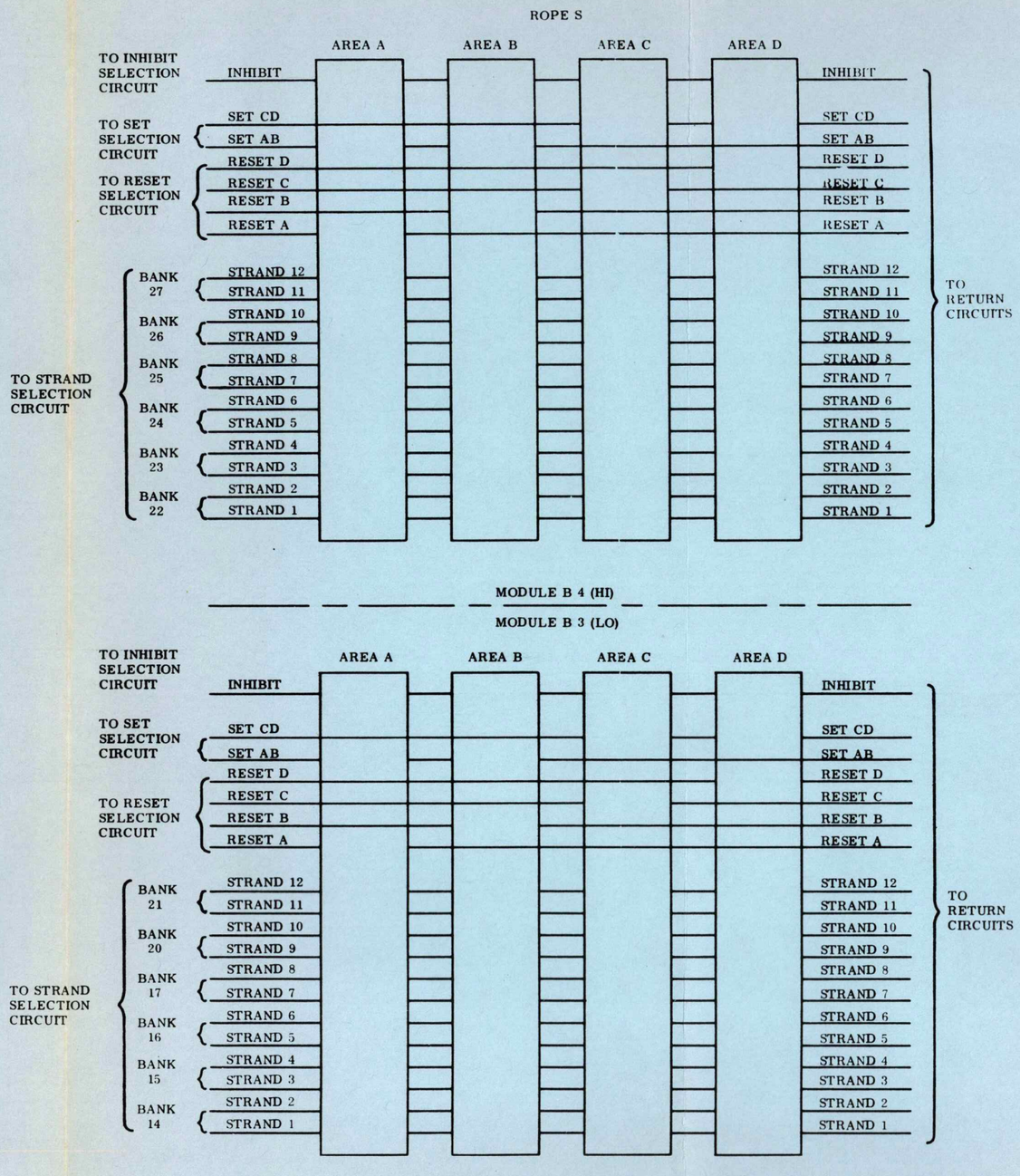


Figure 10-44. Fixed Memory Bank Assignments
(Sheet 2 of 3)

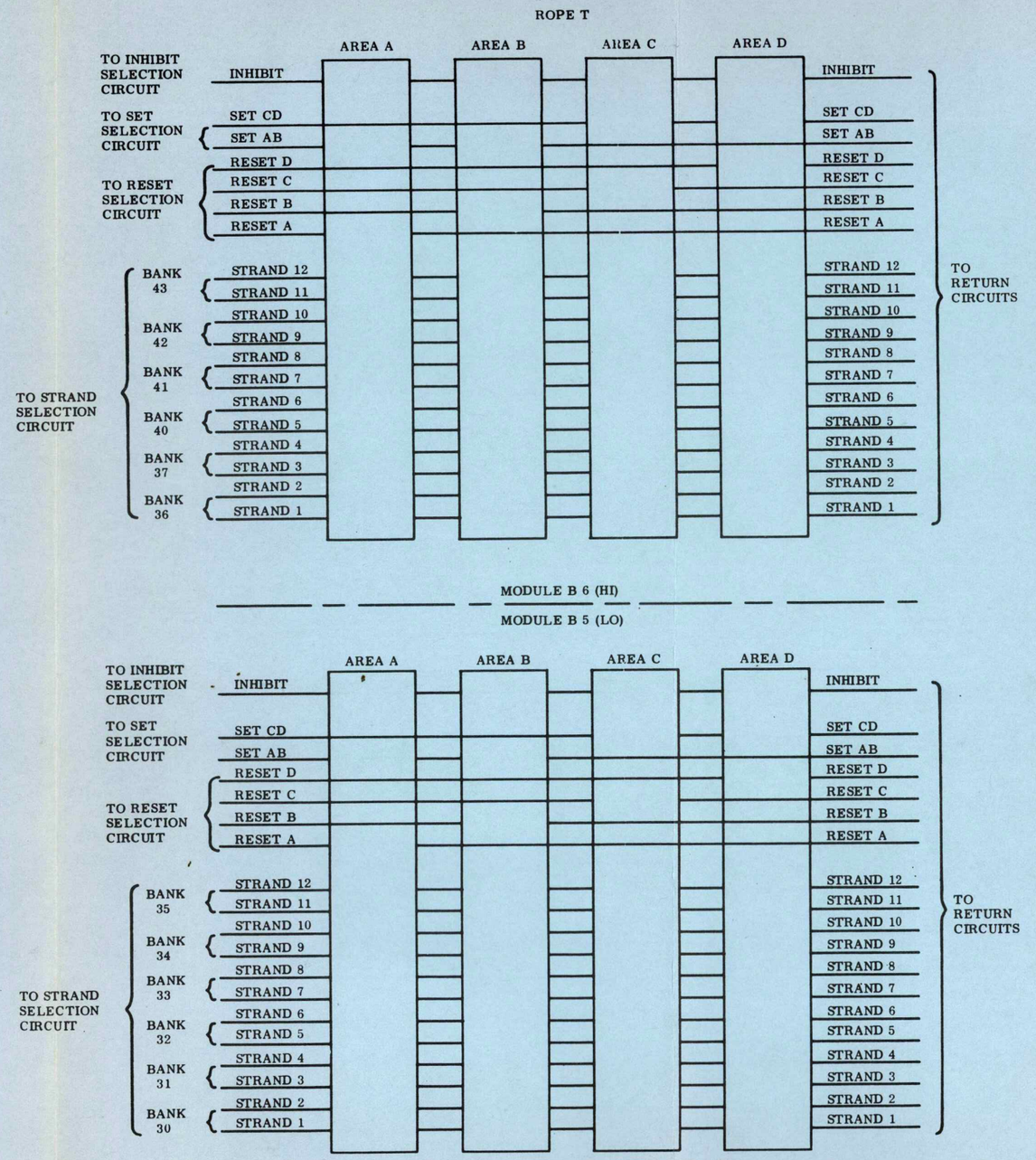


Figure 10-44. Fixed Memory Bank Assignments
(Sheet 3 of 3)

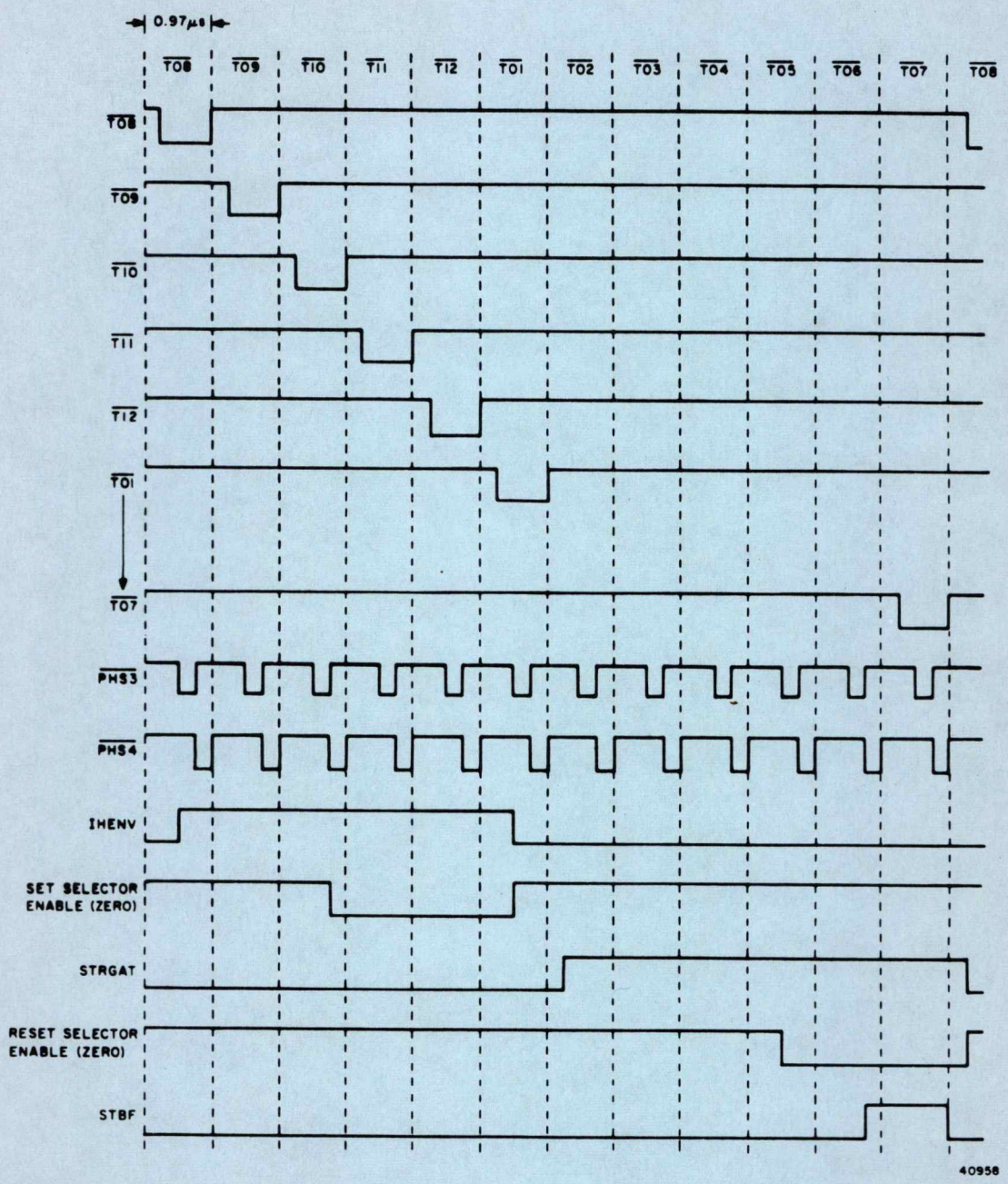


Figure 10-45. Fixed Memory, Timing Diagram

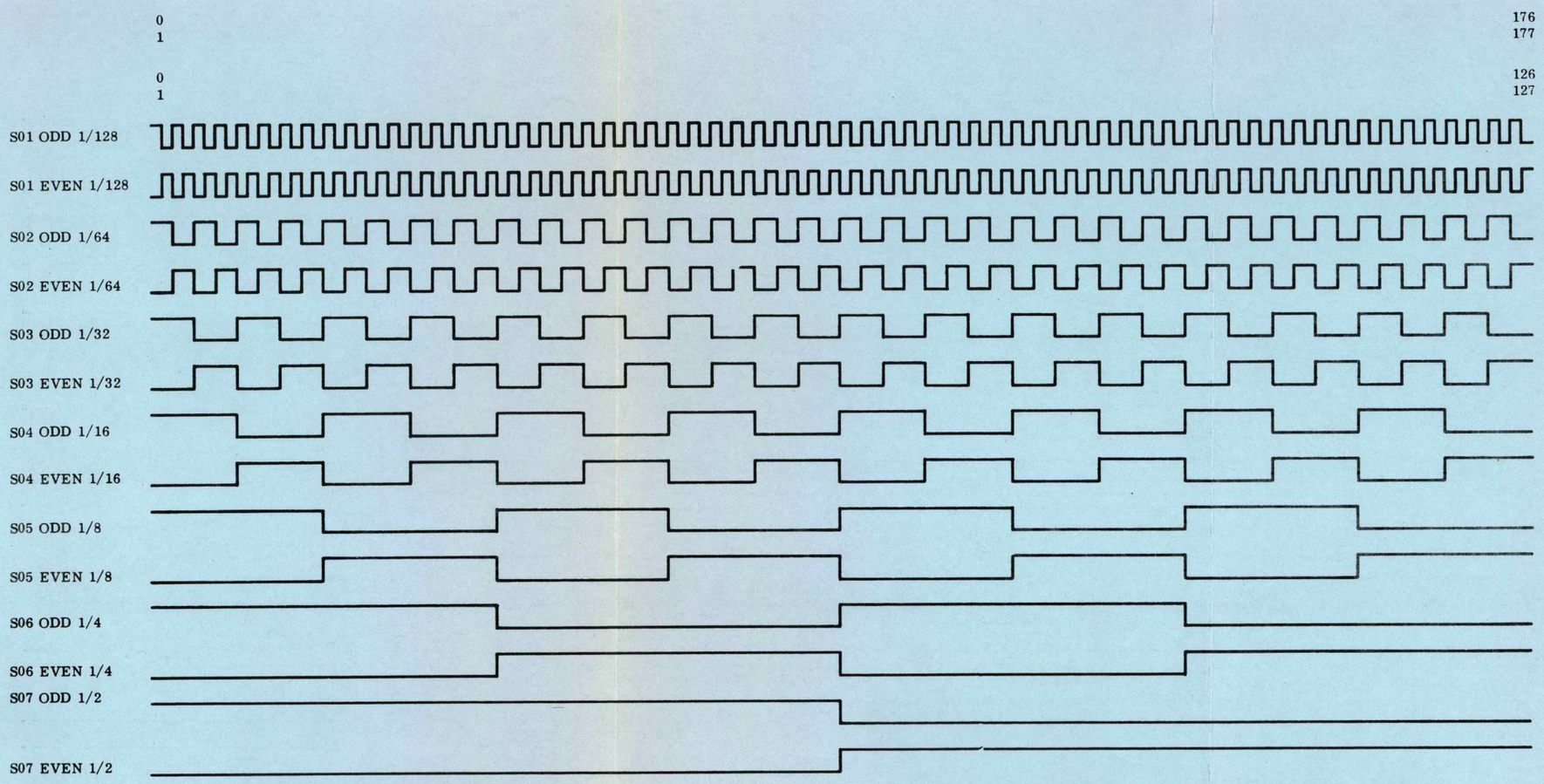


Figure 10-46. Core Selection Via Inhibit Lines (1 of 128 Cores)

At time $\overline{T10}$ and $\overline{PHS4}$, the set selector enable signal is generated to enable the set selection circuit. This circuit uses S09 and $\overline{S09}$ to select two of the four module areas (AB or CD). Each module is divided into four areas of 128 cores each by the reset signals A, B, C, or D. Therefore, the set signal sets one core in each of the two module areas selected. (The actual readout from fixed memory is accomplished by resetting the core that had been set.) Setting two cores enables the readout of 24 words (12 words per core).

At time $\overline{T02}$ the signal STRGAT is generated to enable the strand selection circuit. This circuit uses portions of all three fixed memory registers to select one of 12 strands associated with the selected module thereby selecting two of the 24 words enabled by setting two cores.

At time $\overline{T05}$ and $\overline{PHS3}$ the reset selector enable is generated to enable the reset selection circuit. This circuit uses S08, $\overline{S08}$, S09, and $\overline{S09}$ to generate one of the four reset signals (A, B, C, or D). This signal resets one of the two cores that were set by the set signal causing only one word to be read out of fixed memory. At time $\overline{T06}$ and $\overline{PHS4}$ the signal STBF is generated to enable the readout of the selected word through the sense amplifiers.

10.10.6 PRIORITY CONTROL. Priority control consists of three separate and functionally independent areas: start instruction control, counter instruction control, and interrupt instruction control. See figure 10-47.

The start instruction control restarts the computer following a hardware or program failure. The counter instruction control updates the various counters in erasable memory upon reception of certain incremental pulses. The counter instruction control is also used during test functions to implement the display and load requests provided by the computer test set. The interrupt instruction control forces the execution of the interrupt instruction (RUPTOR) to interrupt the current operation of the computer in favor of a programmed operation of a higher priority.

10.10.6.1 Start Instruction Control. The start instruction control consists of the logic alarms processor and the start-stop generator. The logic alarms processor detects the presence of any one of several abnormal conditions that may occur within the computer and generates an alarm signal (ALGA) whenever any of these conditions exist. These abnormal conditions are:

a. RUPT lock.

b. TC trap.

c. Parity alarm (PALE)

d. Night watchman fail.

A RUPT lock alarm occurs if a program interrupt has been in progress too long (greater than 160 ms) or if an interrupt has not occurred within 160 ms. A TC trap alarm occurs if transfer control (TC) or transfer control to fixed memory (TCF) instructions do not occur within a period of up to approximately 15 milliseconds of each other, or if too many consecutive TC or counter incrementing (INKL) instructions are executed (continuous TC or INKL). A parity alarm (PALE) indicates that a word read out of fixed or erasable memory contains an even number of ones. A night watchman alarm occurs if address 00067 is not addressed by the computer within a

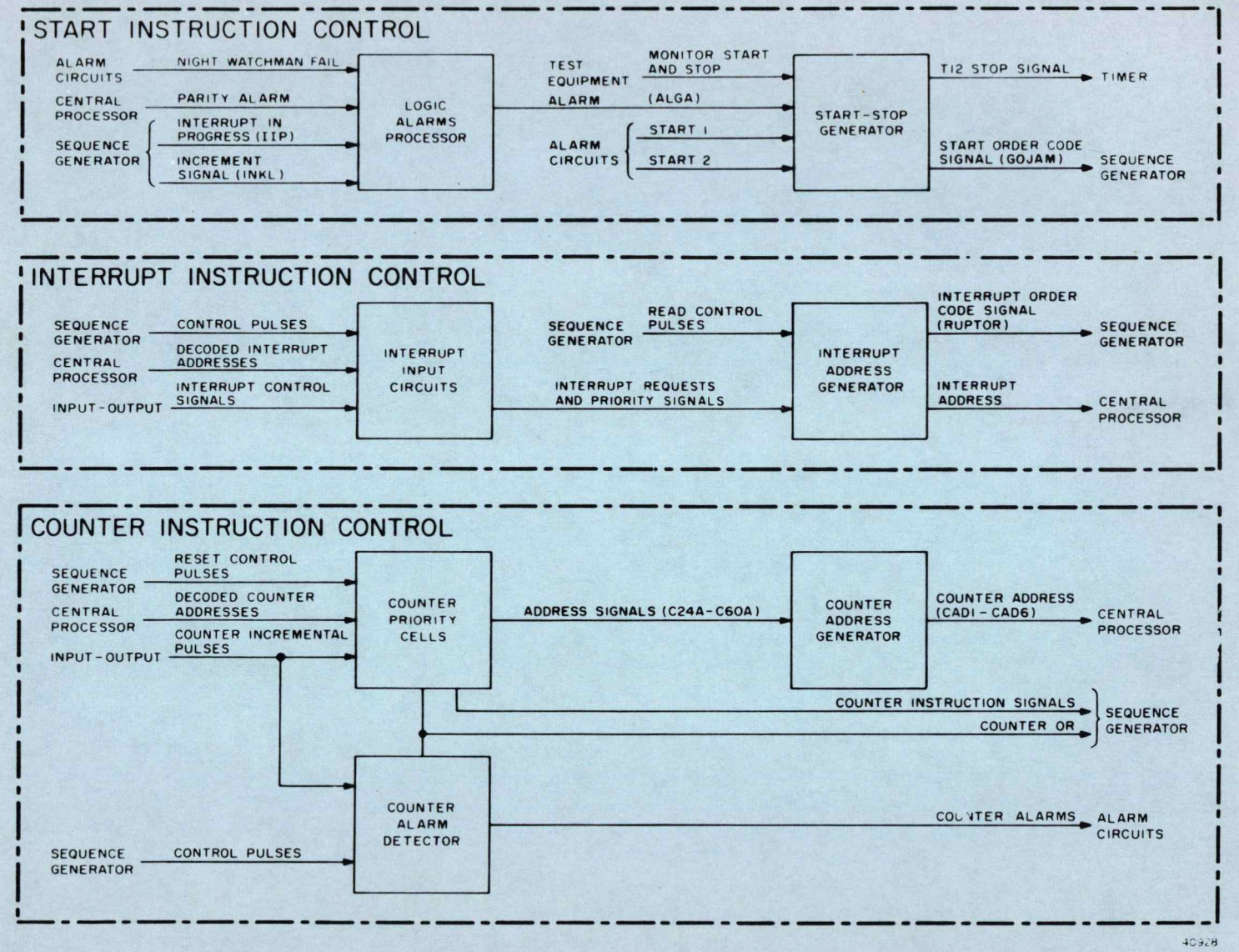


Figure 10-47. Priority Control Functional Block Diagram

period varying from approximately 0.65 seconds to approximately 1.9 seconds. If any of the above alarm conditions exist, alarm signal ALGA is generated by the alarm logic processor and is applied to the start-stop generator.

The start-stop generator generates signal GOJAM to restart the computer in response to the logic alarm signal ALGA at the next T12 time. The restart condition is indicated on the DSKY by the RESTART lamp being illuminated. The start-stop generator simultaneously produces a T12 STOP signal which inhibits the generation of timing pulses $\overline{T01}$ through $\overline{T12}$ in the timer until signal GOJAM has reset all critical circuits in the computer and forces the sequence generator to execute instruction GO. The detection of a computer power supply failure (START 1) or the detection of an oscillator failure (START 2) also causes the computer to restart. In addition, the computer can be started or stopped manually from the peripheral equipment.

10.10.6.2 Counter Instruction Control. A counter is updated when the counter instruction control receives a pulse for a given counter. This digital data consists of changes in velocity, changes in time, changes in gimbal angles, telemetry information, etc. It should be noted that some of these pulses come from within the CMC while others come from various other S/C systems. Counter instruction control may receive pulses for several counters at one time; the CMC, however, can only update one counter at a time. Therefore, the counter instruction control circuitry provides the following five functions.

a. It assigns a priority level to the inputs so that a logical processing order is established when more than one input is received simultaneously.

b. It is able to store an input until the CMC can process it.

c. It generates the address of that location in erasable memory which serves as a counter for that particular input.

d. It develops commands which are sent to the sequence generator to insure that the proper processing occurs. These signals are MINC, PINC, DINC, SHINC, SHANC, PCDU, MCDU and $\overline{INKL}$. Signal $\overline{INKL}$ inhibits the generation of the control pulses defined by the order code held in the SQ register. The sequence generator then develops those pulses necessary to perform a PINC, MINC, etc. instruction.

e. It resets the counter instruction control after the counter instruction has been completed so that other pulse inputs can be processed.

A counter interrupt takes one MCT to be processed. If the counter interrupt occurs during MCT (n), it will be processed during MCT (n + 1) provided, of course, that it is not inhibited by a counter interrupt of higher priority or that the CMC is not in the middle of an instruction.

Table 10-7 lists the 26 counters, their names, priorities, addresses and functions.

Table 10-7. Counter Interrupts

PRIORITY	ERASABLE MEMORY LOCATION (COUNTER)	NAME	REMARKS
1	0024	TIME 2	Stores most significant time word
2	0025	TIME 1	Stores least significant time word
3	0026	TIME 3	Time counter for program waitlist
4	0027	TIME 4	Time counter for T4 RUPT
5	0030	TIME 5	Time counter for thrust vector control
6	0031	TIME 6	Time counter for reaction control
7	0032	ICDU X	Counts ± $\Delta\theta$ pulses from X inertial CDU
8	0033	ICDU Y	Counts ± $\Delta\theta$ pulses from Y inertial CDU
9	0034	ICDU Z	Counts ± $\Delta\theta$ pulses from Z inertial CDU
10	0035	OCDU T	Counts ± $\Delta\theta$ pulses from optics trunnion CDU
11	0036	OCDU S	Counts ± $\Delta\theta$ pulses from optics shaft CDU
12	0037	PIPA X	Counts ± ΔV pulses from X PIPA
13	0040	PIPA Y	Counts ± ΔV pulses from Y PIPA
14	0041	PIPA Z	Counts ± ΔV pulses from Z PIPA
15	0042	BMAG X	Counts ± $\Delta\theta$ pulses from the X BMAG
16	0043	BMAG Y	Counts ± $\Delta\theta$ pulses from the Y BMAG
17	0044	BMAG Z	Counts ± $\Delta\theta$ pulses from the Z BMAG
18	0045	INLINK	Converts serial uplink data into parallel information

(Sheet 1 of 2)

Table 10-7. Counter Interrupts (cont)

PRIORITY	ERASABLE MEMORY LOCATION (COUNTER)	NAME	REMARKS
19	0047	GYRO D	Control pulse bursts which drive the gyros
20	0050	X CDU D	Controls pulse bursts which drive the X CDU
21	0051	Y CDU D	Controls pulse bursts which drive the Y CDU
22	0052	Z CDU D	Controls pulse bursts which drive the Z CDU
23	0053	TRUN CDU D	Controls pulse bursts which drive the optics trunnion CDU
24	0054	SHAFT CDU D	Controls pulse bursts which drive the optics shaft CDU
25	0055	EMSD	Supplies entry velocity to EMS
26	0057	OUTLINK	Converts parallel downlink information into serial data.

NOTE: The lower the priority number, the higher the priority.

(Sheet 2 of 2)

Figure 10-48 is a block diagram of the counter priority control. In this diagram, the inputs are divided into six groups. Each of these groups is associated with the particular counter interrupt instructions which they cause.

GROUP 1: PINC only

GROUP 2: DINC only

GROUP 3: PINC or MINC

GROUP 4: PCDU or MCDU

GROUP 5: SHINC or SHANC

GROUP 6: SHINC only

All of the counter interrupt parameters of each of these groups input to a circuitry block called the priority chain. Included in this block are flip-flops for the storage of the input pulses and the circuitry which establishes the various priorities of the inputs. When a particular input is received, the priority flip-flop associated with that input is set, and the outputs of all the other lower priority flip-flops are inhibited. The request for a particular counter instruction and the address of the appropriate location in erasable memory is then generated. The address generated during the processing of a counter interrupt is also used to reset the appropriate flip-flop in the priority chain. The signal $\overline{\text{INKL}}$ is generated as a result of $\overline{\text{CTROR}}$. $\overline{\text{INKL}}$ is also generated when instructions FETCH, STORE INOTRD or INOTLD are requested by the CTS.

The overall flow of information which occurs during the processing of a counter interrupt input is shown in figure 10-49. In this diagram it is assumed that a PIPA X input is being processed which could be either a plus or minus pulse and result in either a PINC or MINC instruction. These instructions require one MCT to execute.

When a plus or minus PIPA X pulse occurs, it is sent to the appropriate flip-flop in the counter interrupt priority circuits. Assuming plus or minus PIPA X pulse is the highest priority counter interrupt input that requires servicing at the end of the instruction during which it occurred, commands MINC or PINC, signal $\overline{\text{INKL}}$ and address 0037_8 are generated. During the next MCT, the sequence generator develops the control pulses for a MINC or PINC instruction. These instructions cause the six bit address referencing the proper counter in erasable memory, to be sent into the S register through the write amplifiers. Still under control of the MINC or PINC control pulse, the contents of the specified counter is read from erasable memory using the address contained in the S register. The content of the counter is set into the adder circuitry of the CMC where a binary 1 is added or subtracted from it. When the updating process is completed, the updated contents of the counter are stored back into its specified location in erasable memory. This is done under control of the S register which still contains the address of the counter. Having read, updated and written the contents of the counter back into memory, the address held in the S register is used to reset the flip-flop in the counter priority circuitry which requested the servicing. In this case, it is the X PIPA flip-flop. This completes the servicing of the PIPA X input which required one MCT to perform.

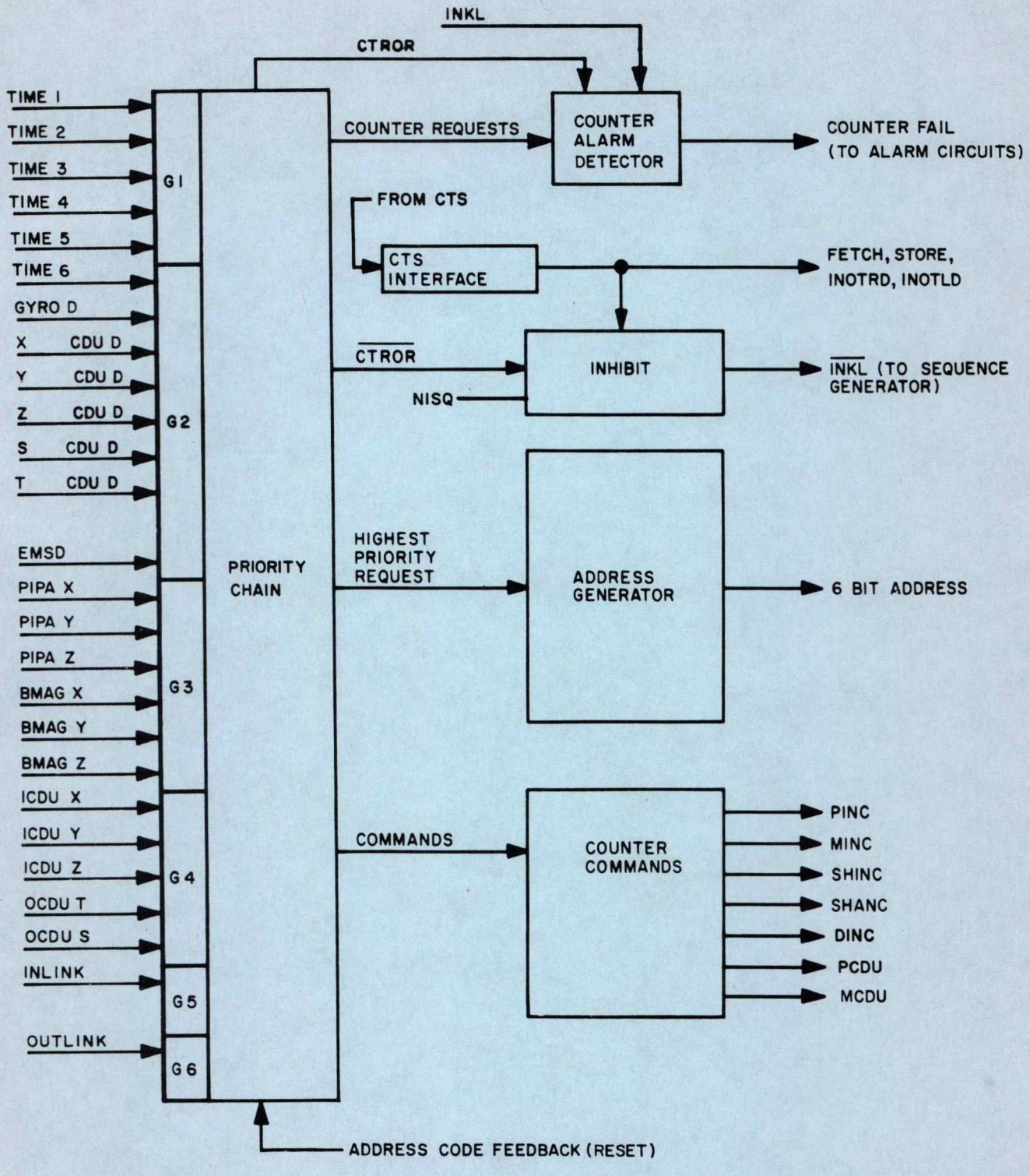


Figure 10-48. **Counter Priority Block Diagram**

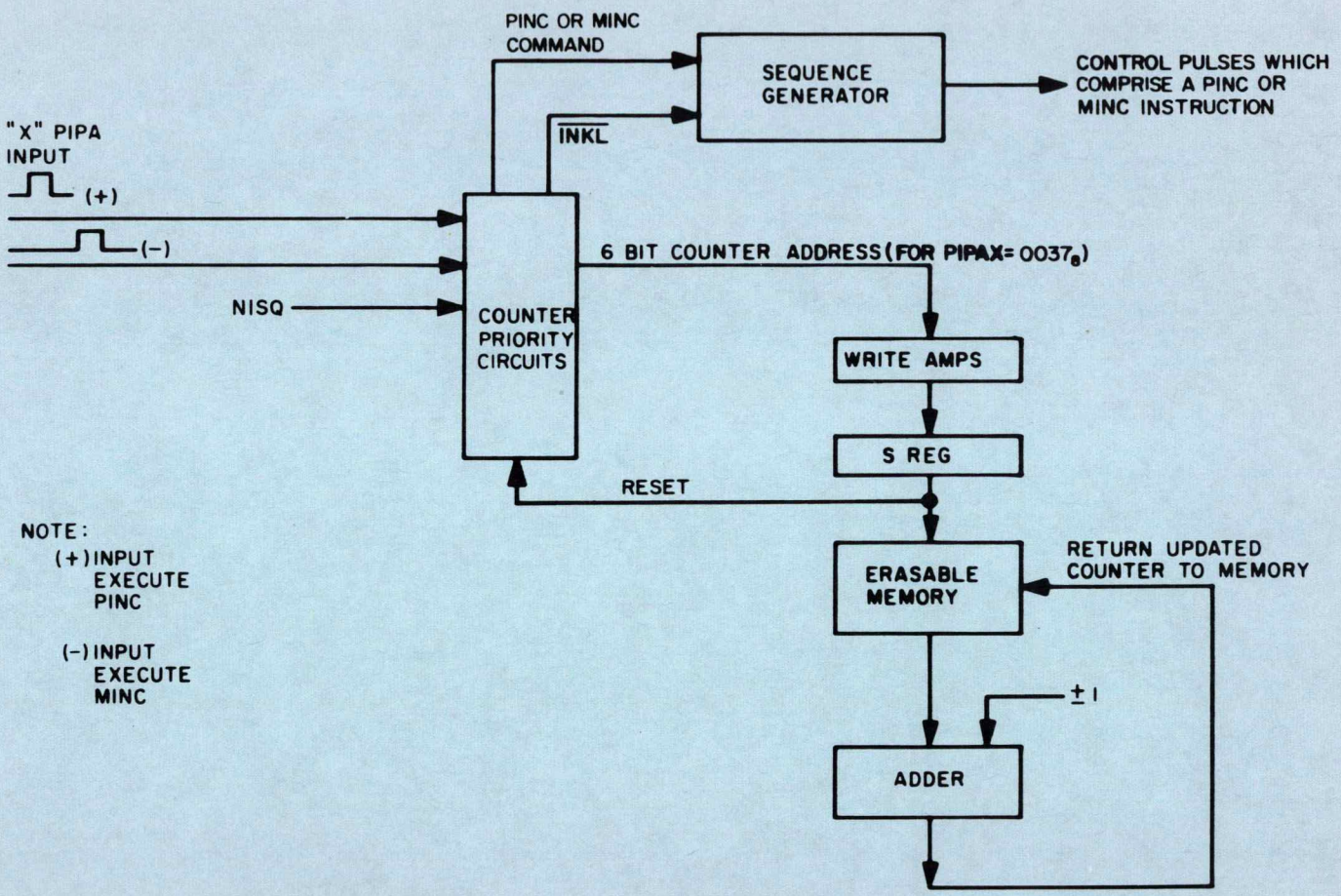


Figure 10-49. Counter Input Interface Flow Diagram

All of the counter interrupt inputs are operated on in essentially the same manner as the PIPA X input. Later in this section, the use of some other counter interrupt inputs and parameters will be presented as they are used in implementing other functions involving the CMC's interface functions.

10.10.6.3 Program Interrupt Priority Control. The T6 RUPT, T5 RUPT, T3 RUPT, T4 RUPT, KEYRUPT 1, KEYRUPT 2, UPRUPT, DOWNRUPT, and HAND CNTRL RUPT interrupt priority control routines are stored in memory and have that order of priority. When a program interrupt request is present, the interrupt priority control produces the address of the appropriate interrupt transfer routine and commands the sequence generator to execute the proper interrupt instructions. Program interrupts cause the suspension of the processing of a particular program and cause a particular routine to be executed. This execution depends upon which input to the program interrupt priority circuitry requires servicing. Table 10-8 lists the program interrupts, their names, initiating events and the actions initiated by their occurrence.

The signals used to request RUPT's 1 through 4 and 7 and 8 have a very short duration (about 1 μ second). However, the requests for RUPT's 5, 6 and 10 have a longer duration. If these long duration signals were used directly to request the processing of an interrupt routine, the request for the routine would still be present when the routine had been processed; therefore, the routine would be processed again. This is an undesirable condition and, consequently, "trap" circuits are used to prevent such a situation. The trap circuitry enables only one 1 μ second pulse to be developed per input request. A reset signal is then required to reset the trap circuitry before another request pulse can be developed. In the case of KEYRUPT 1 or 2, the reset signal is generated by the release of the pushbutton whose depression originally caused the program. In the case of RUPT 10, the reset signals are provided by bits 12, 13 and 14 of output channel 13.

Figure 10-50 is a block diagram of the program interrupt priority control circuitry and its associated inputs.

The request signals for the program interrupts are routed to request flip-flops. The outputs of the flip-flops are interconnected in such a manner that if a higher priority request is present, the outputs of all lower priority request flip-flops are inhibited. Whenever the request for the execution of an interrupt routine is honored, the starting address of the routine is generated and a signal RUPTOR is routed to the sequence generator. The honoring of an interrupt request is enabled at the end of the last MCT of an instruction.

When the request for a program interrupt is honored, the signal RUPTOR forces the order code for the RUPT instruction into the SQ register causing this instruction to be executed. This instruction enables the contents of the Z and B registers to be stored in the erasable memory and, using the generated address, forces control to the starting point of the appropriate interrupt routine. At the beginning of the interrupt routines, the contents of the A and Q registers are stored in the erasable memory. By storing the contents of the B, Z, A and Q registers, the next instruction, the next-next instruction's address, the data being operated on, and the return address of the interrupted program are stored. These quantities are restored in the central processor registers prior to returning control back to the interrupted program when the execution of the interrupt routine is completed.

Table 10-8. Program Interrupts

Interrupt Priority	Name	Initiating Event	Action Initiated
RUPT 1	T6 RUPT	Underflow of TIME 6 counter	Reaction control program termination (fine control)
RUPT 2	T5 RUPT	Overflow of TIME 5 counter	Reaction control program termination (coarse control)
RUPT 3	T3 RUPT	Overflow of TIME 3 counter	Time scheduling of programs to be processed
RUPT 4	T4 RUPT	Overflow of TIME 4 counter	Time scheduling of input/output control programs
RUPT 5	KEYRUPT 1	Depression of pushbutton on main panel DSKY	DSKY keyboard input processing
RUPT 6	KEYRUPT 2	Depression of pushbutton on navigation panel DSKY or depression of the MARK or MARK REJECT pushbutton on G&N indicator control panel	Navigation panel DSKY keyboard input processing or optics data processing for a MARK or MARK REJECT command.
RUPT 7	UPRUPT	A complete word parallelized in the INLINK counter	Uplink data processing
RUPT 8	DOWNRUPT	CMC receipt of telemetry end pulse	Downlink data processing
RUPT 10	HAND CONTROL RUPT	Manipulation of rotational or translational hand controller or throwing a thrust fail switch	Hand and minimum impulse controller input processing.

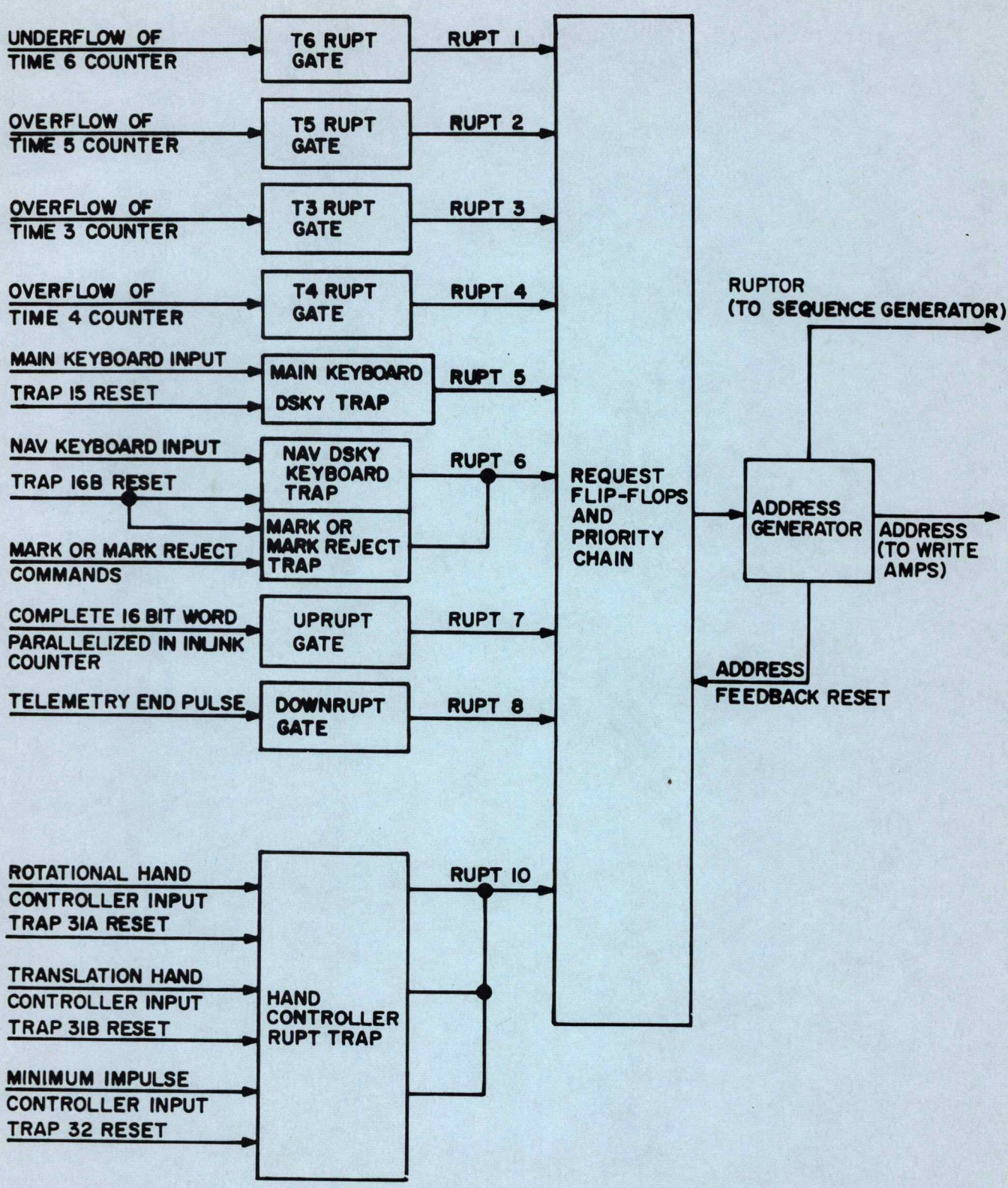


Figure 10-50. Program Interrupt Priority Control

10.10.6.3.1 T6 RUPT Routine. The reaction control program is terminated by the underflow of the TIME 6 counter. This counter is preset to a certain value by program control and then DINCed every 625 μ seconds if bit position 15 of output channel 13 contains a logic one. While the counter is being DINCed, the reaction control program is in process. When the TIME 6 counter underflows, the T6 RUPT routine is terminated.

10.10.6.3.2 T5 RUPT Routine. The T5 RUPT routine is terminated by the overflow of the TIME 5 counter (address 0030_8 in erasable memory). This counter, which is incremented every 10 ms through counter interrupt action (PINC's), is used to time the duration of the reaction control program. The TIME 5 counter is set to overflow minus the time delay required. Overflow terminates the T5 RUPT routine. When the reaction control program is completed, program control is returned to the interrupted program.

10.10.6.3.3 T3 RUPT Routine. The T3 RUPT routine is initiated by overflow of the TIME 3 counter. This counter, which is incremented every 10 ms through counter interrupt action, is used to time the time to initiation of a processing function. The counter is set to overflow minus the time delay required. When the desired time has elapsed, the TIME 3 counter will overflow which initiates the execution of the T3 RUPT routine. The T3 RUPT routine then routes control to the processing function specified to be performed at this time. When completed, control is returned to the T3 RUPT routine which returns control to the interrupted program.

10.10.6.3.4 T4 RUPT Routine. The T4 RUPT routine is executed whenever the TIME 4 counter overflows. Normally, this counter overflows every 120 ms. This counter, like the TIME 3, is incremented every 10 ms.

The T4 RUPT routine performs the following functions:

a. Controls the information displayed on the DSKY's.

b. Monitors and verifies the optics mode switching.

c. Monitors IMU temp, IMU turn-on, IMU, ICDU, and PIPA failures.

d. Monitors for gimbal lock indication.

e. Monitors IMU turn-on.

f. Monitors for downlink and uplink high rate failure indications.

10.10.6.3.5 KEYRUPT 1 Routine. This routine is initiated whenever a key of the main panel DSKY is depressed. The KEYRUPT 1 routine provides for CMC acceptance of the keycode input and initiation of the keycode processing.

10.10.6.3.6 KEYRUPT 2 Routine. The KEYRUPT 2 routine is initiated whenever a key of the navigation panel DSKY is depressed. It is also initiated if the MARK or MARK REJECT pushbutton on the G&N indicator control panel is pushed. The KEYRUPT 2 routine provides for CMC acceptance of the key code input and initiation of the key code processing. If this routine is executed as a result of a MARK REJECT, the associated data (time, gimbal angles, optical angles) is recorded or rejected by the CMC.

10.10.6.3.7 UPRUPT Routine. The UPRUPT routine is initiated whenever a binary 1 is shifted into bit position 16 of the INLINK counter through counter interrupt action. This counter provides a serial to parallel conversion of information sent to the CMC by uplink telemetry. This uplink information is in the form of key codes and the UPRUPT routine performs essentially the same function as KEYRUPT routines for keyboard inputs. The UPRUPT routine accepts the uplink word, checks the validity of the transmission and initiates the processing of the keycode input.

10.10.6.3.8 DOWNRUPT Routine. The DOWNRUPT routine is initiated by the telemetry end pulse from the downlink telemetry converter. This pulse occurs at either 10 or 50 times per second; therefore, the DOWNRUPT routine is executed at these rates. This routine selects the appropriate CMC data to be transmitted downlink and loads it into output channels 34 and 35. The information is then gated out of the CMC in a serial fashion.

10.10.6.3.9 HAND CNTRL RUPT Routine. This will described in the next section (CMC's input and output interface).

10.10.6.4 Alarm Detection Circuits. The alarm detection circuits consist of temperature, voltage, scaler, double frequency scaler oscillator, memory clamping and warning filter and integrator circuits. See figure 10-51.

The IMU stable member temperature is monitored through the temperature alarm circuit. Signal TEMPIN, an indication that the stable member temperature has exceeded its design limits, causes signal TMPCAU to be generated and routed to the DSKY for display (TEMP).

The voltage alarm circuit monitors the +28 vdc, +14 vdc and +4 vdc power and generates signal VFAIL for an out of tolerance or complete failure of any one of the power inputs. Signal VFAIL is conditioned by timing signals and routed to the priority control circuits as signal STRT1 provided it is not inhibited by the CTS signal MVFAL. Signal STRT1 is used in the start instruction control portion of priority control to generate GOJAM. Simultaneously, if the computer is in the standby mode, signal VFAIL and signal STNDBY cause the warning integrator to generate signals CMCWAR and AGCWAR. Signal CMCWAR is routed to a DSKY relay which energizes and causes the CMC warning indicator to illuminate on the caution and warning panel. Signal AGCWAR, a flip-flop output is routed to bit position 14 of channel 33. Signal MVFAIL is also available to the CTS for monitoring.

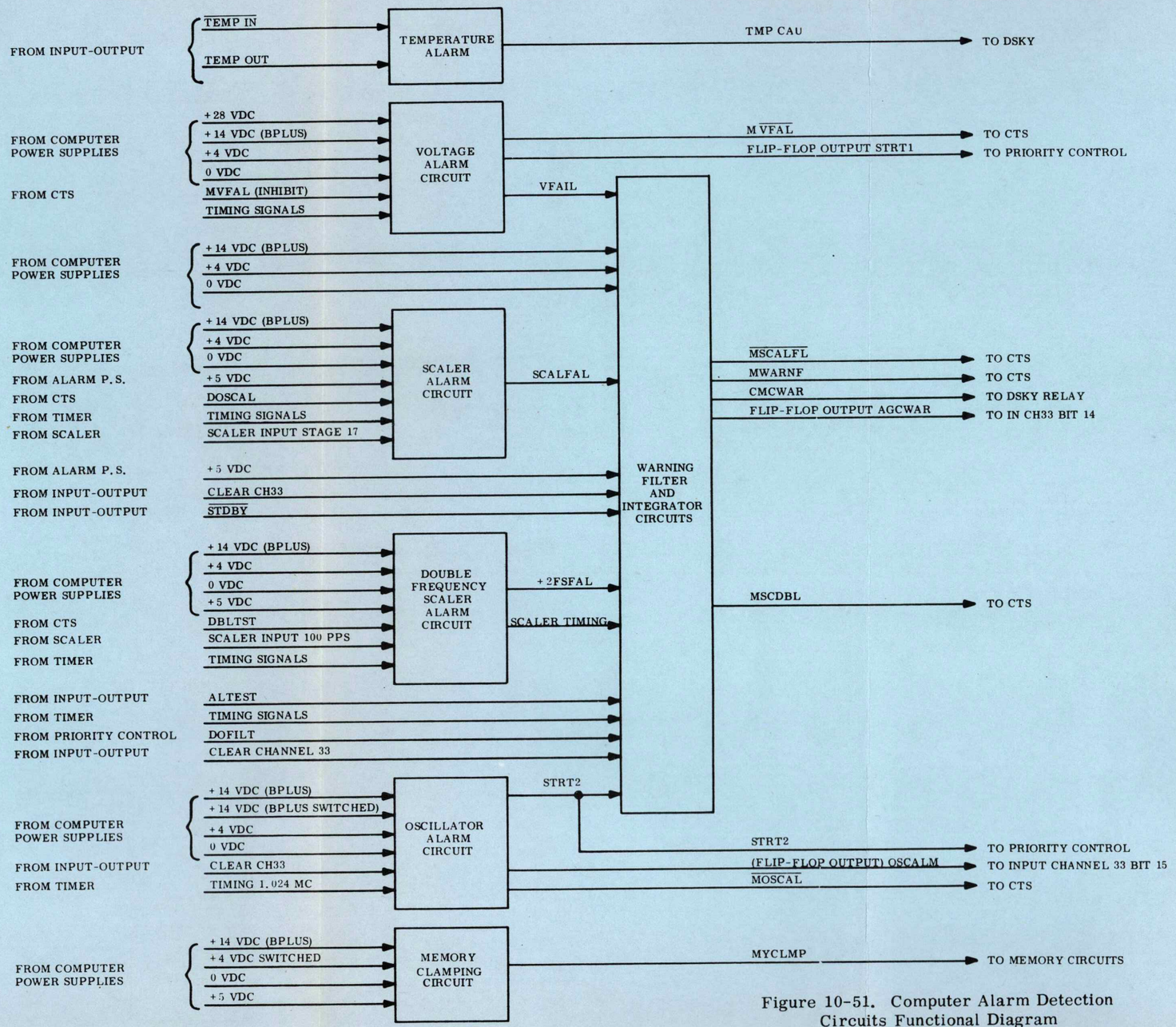


Figure 10-51. Computer Alarm Detection Circuits Functional Diagram

The scaler alarm circuit monitors stage 17 of the scaler and generates signal SCAFAL if stage 17 fails to produce pulses. Signal SCAFAL is used in the warning integrator directly to generate signals CMCWAR and AGCWAR.

Signal DOSCAL, from the CTS, is used to test the operation of the scaler alarm circuit. Signals MSCAFL and MWARNF are available from the warning integrator circuit for CTS monitoring. Signal MSCAFL indicates a scaler failure and MWARNF indicates a CMC warning condition.

The double frequency scaler alarm circuit monitors the 100 pps scaler output and generates signal 2FSFAL whenever the scaler stage is not operating properly. Signal 2FSFAL is used in the warning filter and integrator to generate CMCWAR and AGCWAR. Signal DBLTST, from the CTS is used to test the double frequency scaler alarm circuit. Signal 2FSFAL is also used in the warning filter to generate signal MSCDBL for CTS monitoring.

The oscillator alarm circuit monitors the computer oscillator and generates signals STRT2, OSCALM, and MOSCAL if the oscillator fails. Signal STRT2, is applied to the priority control circuits to generate signal GOJAM and also to a flip-flop to generate OSCALM and MOSCAL. Signal OSCALM is applied to channel 33, bit position 15 and is used internal to the computer. The flip-flop is reset with signal CCH33 (clear channel 33). Signal MOSCAL is available to the CTS for monitoring purposes.

The memory clamping circuit monitors the +4 vdc power and generates signal MYCLMP upon loss of this power. Signal MYCLMP is applied to the memory circuits to inhibit any access to memory.

The warning filter circuit performs logic gating for signals:

a. $\overline{\text{VFAIL}}$ and $\overline{\text{STNDBY}}$

b. 2FSFAL

c. DOFILT

d. ALTEST

Timing signals allow only one of these signals to be gated to the integrator at a time.

The warning integrator circuit monitors the output of the warning filter and generates signal CMCWAR and AGCWAR if 5 successive pulses are received from the warning filter. Signals CMCWAR and AGCWAR will also be generated if signal SCALFAL is present. Signal AGCWAR is a flip-flop output which is applied to channel 33, bit position 14 for use internal to the computer. Signal CMCFAL is routed to the DSKY where it energizes a DSKY relay. The relay causes the CMC warning indicator to light on the caution and warning panel.

10.10.7 CMC'S INPUT AND OUTPUT CHANNEL INTERFACE. In addition to the counter interrupt and the program interrupts previously described, the CMC has a number of other inputs derived from its interfacing hardware. These inputs are a result of the functioning of the hardware or an action by the operator of the spacecraft. The counter interrupts in most cases enable the CMC to process inputs representative of data parameters such as changes in velocity. The program interrupt inputs to the CMC are used to initiate processing of functions which must be processed a relatively short time after a particular function is present. The other inputs to the CMC, in general, enable the CMC to be cognizant of "conditions" which exist in its environment. These inputs are routed to CMC and are available to the CMC's programs through the input channels.

The outputs of the CMC fall in one of the following categories: (1) data, (2) control, (3) condition indications. Some of these outputs are controllable through the CMC's program while others are present as a function of the CMC circuitry. All of the outputs which are controlled by the CMC's programs are developed through the CMC's output channels.

10.10.7.1 CMC Input/Output Channel Bit Assignments. Table 10-9 shows the CMC input/output channel bit assignments. A brief description of the channels and reference information concerning them appears in table 10-10.

10.10.7.2 PIPA Precount Logic. The PIPA precount logic consists of three forward-backward counters and PIPA failure detection circuitry. The forward-backward counters eliminate the PIPA pulses due to the PIPA 3-3 moding so that only PIPA pulse due to an acceleration will cause counter instructions to occur. The PIPA failure detection circuitry generates a PIPA fail (PIPAFL) signal if anyone of three abnormal conditions occur.

When a PIPA is sensing no acceleration, the PIPA loop in the ISS continuously torques the PIPA with a series of three + pulses followed by a series of 3- pulses. The foward-backward counter associated with the particular PIPA loop receives these + and - pulses. The counter counts forward three and then backward three without generating an output. Only when the counter receives more than three positive or negative pulses in a sequence does it generate an output. The output is dependent on the input, in that, a plus output pulse (PIPXP, PIPYP or PIPZP) is generated if the plus input pulses (PIPGX+, PIPGY+ or PIPGZ+) exceed three and a minus output pulse (PIPXM, PIPYM, or PIPZM) is generated if the minus input pulses (PIPGX-, PIPGY- or PIPGZ-) exceeds three. The operation of one of the three forward-backward counters is illustrated in figure 10-52 and table 10-11.

Table 10-9. CMC Input/output Channel Bit Assignments

CHANNEL	NAME	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	CHANNEL
1	L	CP REGISTER L, BITS 16-1															1
2	Q	CP REGISTER Q, BITS 16-1															2
3	SCALER2	HIGH - ORDER SCALER CHANNEL, BITS 14-1															3
4	SCALER1	LOW - ORDER SCALER CHANNEL, BITS 14-1															4
5	PITCH YAW							S/M →	RCS +X -Y	RCS -X +Y	RCS -X -Y	RCS +X +Y	RCS +X -P	RCS -X +P	RCS -X -P	RCS+X+P	5
								C/M →	-YW -X +P	+YW -X -P	-YW -X -P	+YW -X +P	-P +Z	+P -X -YW	-P+Z	+P-X+YW	
6	ROLL							S/M →	RCS +Y -R	RCS -Y +R	RCS -Y -R	RCS +Y +R	RCS +Z -R	RCS -Z +R	RCS-Z-R	RCS+Z+R	6
								C/M →					-R -Y +Z	+R +Y -Z	-R-Y-Z	+R+Y+Z	
7	FEXT									FE7	FE6	FE5					7
10	DSKY R & C	RELAY ADRS 4	RELAY ADRS 3	RELAY ADRS 2	RELAY ADRS 1	RELAY BIT 11	RELAY BIT 10	RELAY BIT 9	RELAY BIT 8	RELAY BIT 7	RELAY BIT 6	RELAY BIT 5	RELAY BIT 4	RELAY BIT 3	RELAY BIT 2	RELAY BIT 1	10
11	DSKY A			ENGINE ON/OFF			CAUTION RESET	TEST CONNEC OUTBIT		OP ERROR LAMP	VN FLASH	KEY RLSE LAMP	TEMP CAUTION LAMP	UPLINK ACTY LAMP	COMP ACTY LAMP	ISS WARNING	11
12	GN&C	ISS TURNON DELAY COMPLETE	SIV B CUTOFF	SIV B INJ. SEQ. START		DENG OPTICS DAC	ZERO OPTICS	SIV B TAKEOVER ENABLE	TVC ENABLE		ENABLE IMU ERR CTR	ZERO IMU CDU	COARS ALIGN ENABLE		ENABLE OPT ERR CTR	ZERO CDU OPTICS	12
13	CMC	ENABLE T6RUPT	RESET TRAP 32	RESET TRAP 31B	RESET TRAP 31A	ENABLE STANDBY	TEST ALARMS		B MAG CTR ENABLE	DNLNK WD ORD	BLOCK INLINK	INHIBIT UPLINK					13
14	IMU	DRIVE CDUX	DRIVE CDUY	DRIVE CDUZ	DRIVE CDU T	DRIVE CDU S	GYRO ACTY	GYRO c	GYRO a	GYRO b	GYRO ENABLE					OUTLINK ACTY	14
15	MAIN DSKY											KEY 5M	KEY 4M	KEY 3M	KEY 2M	KEY 1M	15
16	NAV DSKY									MARK REJECT	MARK	KEY 5N	KEY 4N	KEY 3N	KEY 2N	KEY 1N	16
30	GN&C *	TEMP IN LIM	ISS TURNON REQUEST	IMU FAIL	ICDU FAIL	IMU CAGE	S/G CONTROL OF SAT	IMU OPER		OPTICS CDU FAIL	GUID REF RELEASE	LIFTOFF	SIV B SEPARATE, ABORT	SPS READY	SM SEPARATE	ULLAGE THRUST PRES.	30
31	TRANS & * ROT	G/C AUTO CONTROL	FREE FUNCTION	HOLD FUNCTION	-Z TRANS	+Z TRANS	-Y TRANS	+Y TRANS	-X TRANS	+X TRANS	MANR -R	MANR +R	MANR -Y	MANR +Y	MANR -P	MANR +P	31
32	IMPULSE *					LM ATTACHED					MNIM -R	MNIM +R	MNIM -Y	MNIM +Y	MNIM -P	MNIM +P	32
33	OPTICS * CMC	OSC ALARM	WARNING	PIPA FAIL	DNLNK TOO FAST	UPLNK TOO FAST	BLOCK UPLINK					CMC CONTROL	ZERO OPTICS				33
34	DNLNK1	FIRST OF TWO WORDS															34
35	DNLNK2	SECOND OF TWO WORDS															35
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

* INVERTED LOGIC USED

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Description	References
0			Vacant	
1	1-16	L	Central processor register L	para. 10.5.2.1
2	1-16	Q	Central processor register Q	para. 10.5.2.1
3	1-14	Scaler2	High order scaler - furnishes a 14 bit positive number whose least significant bit has a weight of 5.12 seconds. The period of the number is 23.30 hours. Because of logic propagation delays, this channel should be interrogated more than once to resolve erroneous reads at the time of transition.	
4	1-14	Scaler1	Low order scaler - furnishes a 14 bit positive number whose least significant bit has a weight of 1/3200 second. The period of the number is 5.12 seconds. As above this channel should be interrogated more than once to resolve erroneous reads.	
5	1-8	pitch yaw 1 2 3 4 5 6 7 8	In the service module this channel has 8 bit positions +X+P -X-P -X+P +X-P +X+Y -X-Y -X+Y +X-Y and is associated with the RCS jets. The first letter contained in the bit positions of the figure refers to a translational motion, the second to a rotational motion. For instance, if it were desired to perform a pure positive translation along the X-axis, several different logic configurations could be associated with the bit positions of this channel. a. 1) Bit positions 1 and 4 equal to a logic one 2) All other bit positions equal to a logic zero b. 1) Bit positions 5 and 8 equal to a logic one 2) All other bit positions equal to a logic one c. 1) Bit positions 1, 2, 5, and 8 equal to a logic one 2) All other bit positions equal to a logic zero	(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Description	References
			Note that for a pure translation, the logic levels of the bit positions must be chosen in such a fashion that any rotational motions are cancelled out.	
5	1 2 3 4 5 6 7 8		+P-X+YW -P+Z-R +P-X-YW -P+Z+R +YW-X+P -YW-X-P +YW-X-P -YW-X+P In the command module this channel is associated with the RCS jets. The letters to the right, indicate the command module motion corresponding to a logic 1 in a particular bit location. If, for example, a logic 1 is placed in bit position 5 the CM would experience a + yaw, a + pitch and a translation along the -X axis.	
6	1-8	Roll 1 2 3 4 5 6 7 8	RCS+Z+R RCS-Z-R RCS-Z+R RCS+Z-R RCS+Y+R RCS-Y-R RCS-Y+R RCS+Y-R In the service module this channel is associated with the RCS jets. For instance, if a CM roll is desired it can be accomplished by several different logic configurations in the channel bit positions. a. 1) Bit positions 1 and 3 equal to a logic 1 2) All other bit positions equal to a logic 0 b. 1) Bit positions 5 and 7 equal to a logic 1 2) All other bit positions equal to a logic 0	

(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Designation	References
6	1-8	Roll 1 2 3 4	+R+Y+Z -R-Y-Z +R+Y-Z -R-Y+Z	In the command module this channel is associated with 4 RCS jets. The letter to the right indicate the command module motion corresponding to a logic 1 in a particular bit location.	
7	3 5 6 7	F-EXT	This channel is used to increase fixed memory addressing capability. FE 7 FE 6 FE 5 High Banks 0 X X 30-37 1 0 0 40-43 1 0 1 EMP. 1 1 0 EMP. 1 1 1 EMP.	
10	16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15/16	DSKY R&C	Relay Bit 1 Relay Bit 2 Relay Bit 3 Relay Bit 4 Relay Bit 5 Relay Bit 6 Relay Bit 7 Relay Bit 8 Relay Bit 9 Relay Bit 10 Relay Bit 11 Relay Address 1 Relay Address 2 Relay Address 3 Relay Address 4	The information contained in this channel is routed to the DSKYs. The different configurations light various displays on the DSKY's. Bits 1-11 are associated with column selection signals and bits 12 12-15 are associated with roll selection signals determining a specific position in a relay matrix.	Para. 11.1 Para. 11.3

(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Designation	Reference
11	15	DSKY A	The information in this channel is routed to the DSKY.	
	1		ISS Warning - lights a DSKY caution light	Table 11-3
	2		Light Computer Activity Lamp	Table 11-3
	3		Light Uplink Activity Lamp	Table 11-3
	4		Light Temperature Caution Lamp	Table 11-3
	5		Light Keyboard Release Lamp	Table 11-3
	6		Flash verb and noun lamps	Table 11-3
	7		Light operator error lamp	Table 11-3
	8		Spare	
	9		Test connector outbit	
	10		Caution reset	
	11		Spare	
	12		Spare	
	13		Engine On	
	14		Engine Off	
	15		Spare	
12	15	GN&C	This channel consists of 15 bits. The outbits are dc signals sent to the S/C and PGNC systems.	
	1		Zero CDU optics	
	2		Enable optical error counter	
	3		Spare	
	4		Coarse align enable	
	5		Zero IMU CDU	
	6		Enable IMU error counter	
	7		Engine on/off	Figure 4-14
	8		Thrust vector control enable	Figure 4-14
	9		SIVB takeover enable	Figure 4-12
	10		Zero optics	
	11		Disengage optic DAC	
	12		Spare	
	13		SIVB Inj. Seq. start	
	14		SIVB cutoff	
	15		ISS turn on delay complete	

(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Description	References
13	15	CMC		
	1-4		Spares	
	5		Uplink inhibit	
	6		Block inlink	
	7		Downlink word order	
	8		BMAG CTR enable	
	9		Spare	
	10		Test alarms	
	11		Enable standby	
	12		Reset Trap 31A	
	13		Reset Trap 31B	
	14		Reset Trap 32	
	15		Enable T6 RUPT	
14	15	IMU		
	1		Outlink activity	
	2-5		Spare	
	6		Gyro enable	
	7		Gyro b	
	8		Gyro a	
	9		Gyro c	
	10		Gyro activity	
	11		Drive CDU S	
	12		Drive CDU T	
	13		Drive CDU Z	
	14		Drive CDU Y	
	15		Drive CDU X	
15	5	Main DSKY	This channel consists of 5 bit positions.	
	1		KEY 1M	Whenever a key on the
	2		KEY 2M	DSKY is pressed, a
	3		KEY 3M	unique 5 bit code is
	4		KEY 4M	generated and entered
	5		KEY 5M	into this channel. The RUPT 5 interrupt routine is also developed whenever a key is depressed.
16	7	Nav DSKY	This channel consists of 7 bit positions. The	
	1		KEY 1N	function of the first
	2		KEY 2N	5 positions are the
	3		KEY 3N	same as those in
	4		KEY 4N	channel 15.
	5		KEY 5N	

(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Designation	References
16	6 7		MARK MARK REJECT If the mark pushbutton is depressed, a 1 is put in bit position 6 and would cause a KEYRUPT 2 (RUPT6) interrupt routine. If the MARK REJECT pushbutton is depressed, a logic is entered in bit 7 and would cause a KEYRUPT 2 interrupt routine.	
30	15	GN&C		
	1		Ullage thrust present	
	2		SM separate	
	3		SPS ready	
	4		SIVB separate, abort	
	5		Lift off	
	6		Guidance reference release	
	7		Optics CDU fail	
	8		Spare	
	9		IMU Operate	
	10		S/C control of SAT	
	11		IMU cage	
	12		ICDU fail	
	13		IMU fail	
	14		ISS trunnion request	
	15		Temp in limits	
31	15	* Trans. and Rot.	Consists of 15 bit positions	
	1		MANR+P	
	2		MANR-P	
	3		MANR+Y	
	4		MANR-Y	
	5		MANR+R	
	6		MANR-R	
	7		+X TRANS	
	8		-X TRANS	
	9		+Y TRANS	
	10		-Y TRANS	
	11		+Z TRANS	
	12		-Z TRANS	
	13		HOLD FUNCTION	
	14		FRE FUNCTION	
	15		S/C AUTO CONTROL	

(Cont)

Table 10-10. Input/Output Designation and Reference

Channel	Bit Pos	Name	Designation	Reference
32	15	*IMPULSE	Consists of 15 bit positions.	
	1		MNIM+P	
	2		MNIM-P	
	3		MNIM+Y	
	4		MNIM-Y	
	5		MNIM+R	
	6		MNIM-R	
	7		Spare	
	8		Spare	
	9		Spare	
	10		Spare	
	11		LM attached	
	12		Spare	
	13		Spare	
	14		Spare	
	15		Spare	
33	15	*Optics CMC		
	1		Spare	
	2		Spare	
	3		Spare	
	4		Zero optics	
	5		CMC control	
	6		Spare	
	7		Spare	
	8		Spare	
	9		Spare	
	10		Block uplink	
	11		Uplink too fast	
	12		Dnlink too fast	
	13		PIPA fail	
	14		Warning	
	15		OSC alarm	
34	15	DNLNK1	First of two, 15 bit words	
35	15	DNLNK2	Second of two, 15 bit words	

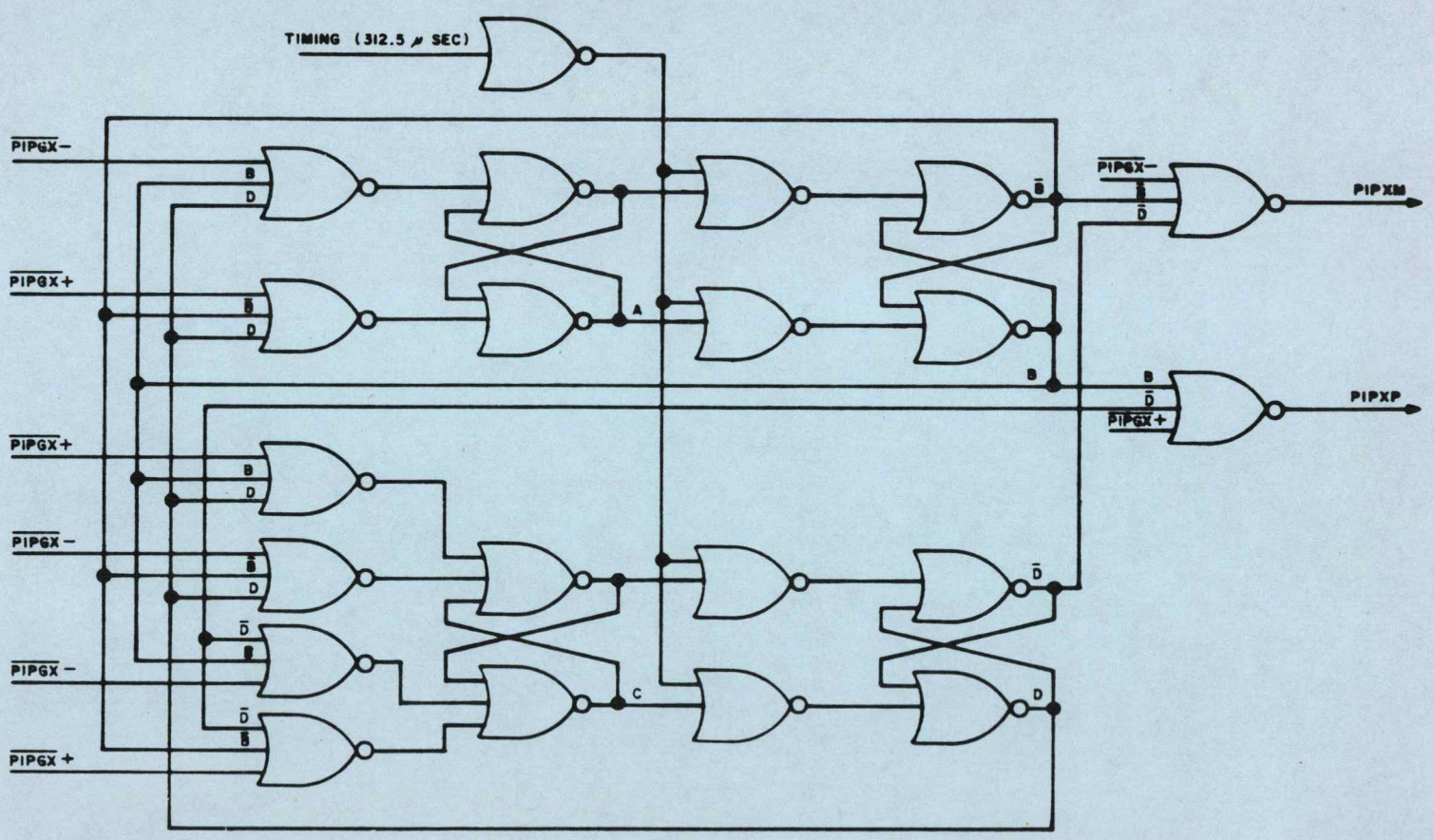


Figure 10-52. PIPA Forward-Backward Counter

Table 10-11. PIPAX Counter Truth Table

Initial Conditions		Input Signal	Resulting Conditions		
Signal B	Signal D		Signal B	Signal D	Output Signal
1	1	PIPGX+	1	0	-
1	0	PIPGX+	0	0	-
0	0	PIPGX+	0	1	-
0	1	PIPGX+	0	1	PIPXP
0	1	PIPGX-	0	0	-
0	0	PIPGX-	1	0	-
1	0	PIPGX-	1	1	-
1	1	PIPGX-	1	1	PIPXM

The PIPA failure detection circuitry monitors for the following conditions:

a. That each PIPA have output pulses (plus and minus) within a given period of time.

b. That no PIPA has both plus and minus pulses at the same time.

c. That each PIPA has a plus or a minus pulse within a given time.

If any of these three conditions exist, a PIPA fail (PIPAFL) signal is generated. This signal is applied to channel 33 bit position 13 and is used internal to the computer.

The circuit that monitors for plus and minus pulses within a given time period is illustrated in figure 10-53. When a PIPA pulse is generated, the associated input flip-flop is reset and generates signal NOXP, NOXM, NOYP, NOYM, NOZP or NOZM equal to logic zero. All six NO__ signals are applied to an "NOR" gate and if all inputs are logic "ZERO" the output of the NOR gate will be a logic "ONE". A logic "ONE" applied to the next NOR gate will force its output to be a logic "ZERO". If all inputs to the output flip-flop are logic "ZERO", the flip-flop will remain reset (signal PIPAFL = 0). At time F18AX, the input flip-flops are all set (signals NO__ = 1). If any PIPA does not produce both a plus and a minus pulse within the following 1.3 seconds, the particular input flip-flop will not be reset; therefore, the next NOR gate will have a logic "ZERO" output. This logic "ZERO" output is applied to the next NOR gate and at time $\overline{\text{F18B}}$ the gate will produce a logic "ONE" which sets the output flip-flop and generates signal PIPAFL.

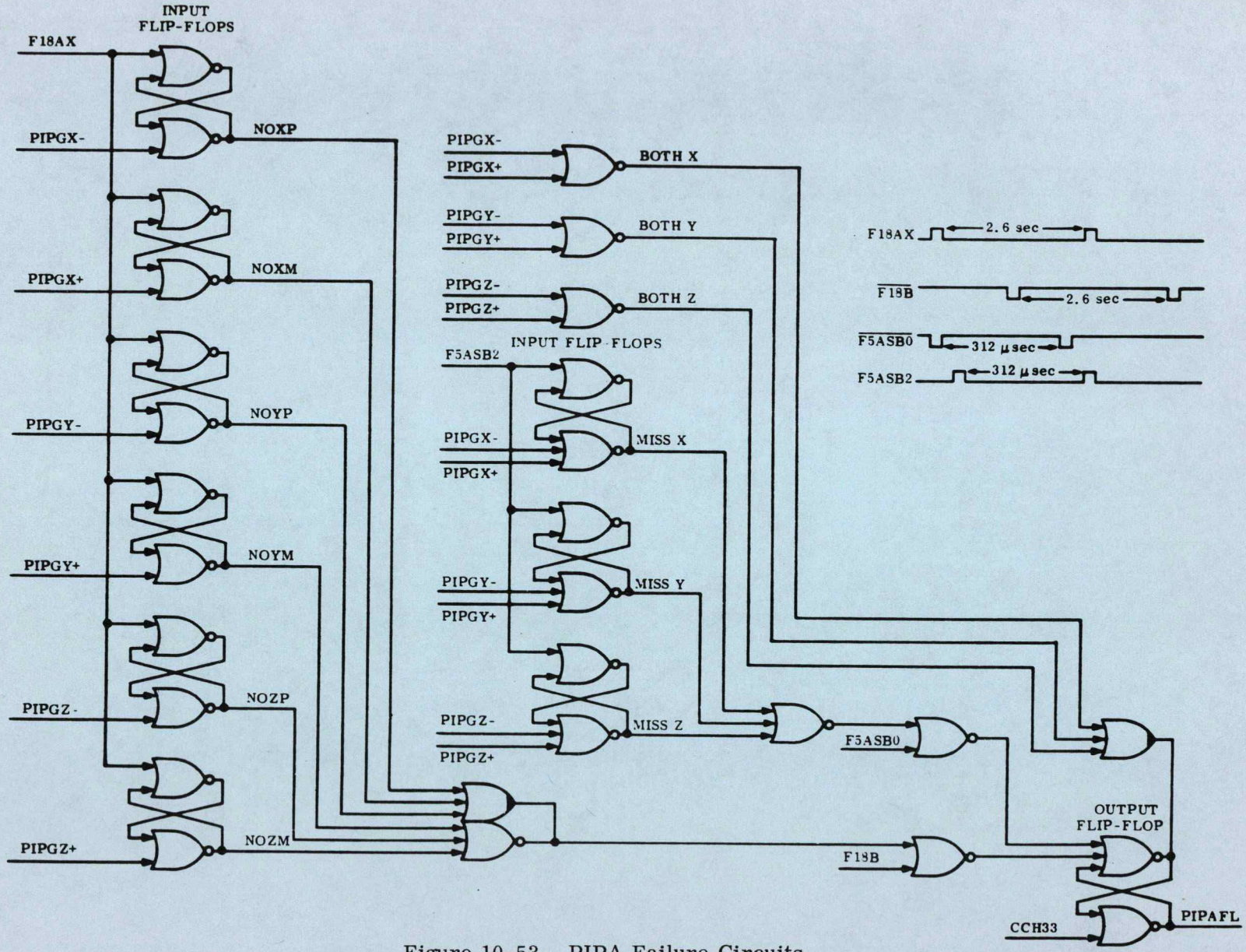


Figure 10-53. PIPA Failure Circuits

The circuit that monitors for a plus or a minus PIPA pulse within a given period of time will generate the PIPA fail signal (PIPAFL) if each PIPA does not generate either a plus or a minus pulse for every PIPA data pulse generated. Timing signal F5ASBZ sets the input flip-flops associated with this circuitry every time that a PIPA data pulse is applied to the PIPA binary current switches. Each PIPA loop must produce a plus or a minus pulse for every PIPA data pulse. The plus or minus pulses reset the input flip-flops prior to timing signal F5ASBO. If all PIPA loops generate a plus or a minus pulse. All three of the input flip-flops will be reset (MISSX, MISSY and MISSZ = 0). The next NOR gate will generate a logic "ONE" and prevent the setting of the output flip-flop. If one of the PIPA loops fails to produce a plus or a minus pulse prior to time F5ASBO, the output flip-flop will be set (PIPAFL = 1).

The circuit that monitors for both plus and minus PIPA pulses occurring at the same time will generate the PIPAFL signal be setting the output flip-flop through the extended NOR gate. Signal Both X, Both Y, or Both Z will set the output flip-flop.

10.10.7.3 Interface Circuits. The interface circuits provide interfacing between the computer and the DSKY's, the spacecraft, and the remainder of the PGNCS. All input to and output from the computer are routed through these circuits. See figure 10-54.

There are seven types of interface circuits that provide the proper voltage levels and impedance matching between the computer and other spacecraft systems. These seven circuit types are designated circuits A, C, D, P, XT, R, and Y.

The A type circuit is an analog to digital converter which is used in the LGC only in conjunction with propulsion rate commands.

The C type circuit is a transistor driver circuit which buffers discrete type output from the computer to the DSKY's and the reaction control system.

The D type circuit consists of an RC filter, the output of which is applied directly to the computer logic circuits. The input signals involved are discrete type signals from the DSKY, other PGNCS subsystems, and the other spacecraft systems.

The P type circuit filters the +14 vdc input to the XT circuits.

The R type circuit is a series resistor and is used to provide short circuit protection for output from the power supply.

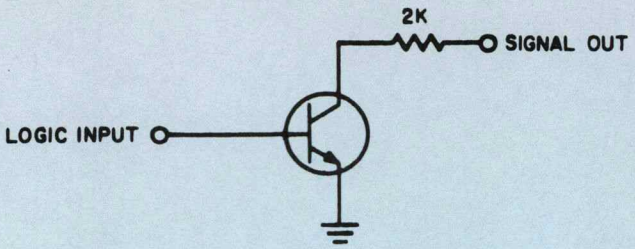
The XT type circuit consists of a pulse transformer driven by an input transistor circuit. It provides the required output impedance to match spacecraft circuits and other subsystem circuits. It also is used as an input interface circuit to provide impedance matching and the voltage level necessary to operate the logic in the computer.

All signals interfacing with the computer have an alphanumeric code rather than the functional name when routed outside of any particular subsystem. This code is used in the interface drawings and designates the interface circuits type, signal type and number (for example, DE 040). The first letter designates the interface circuit type:

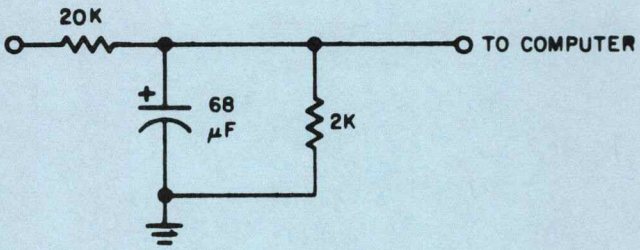
A analog-to-digital converter

C discrete type output circuit

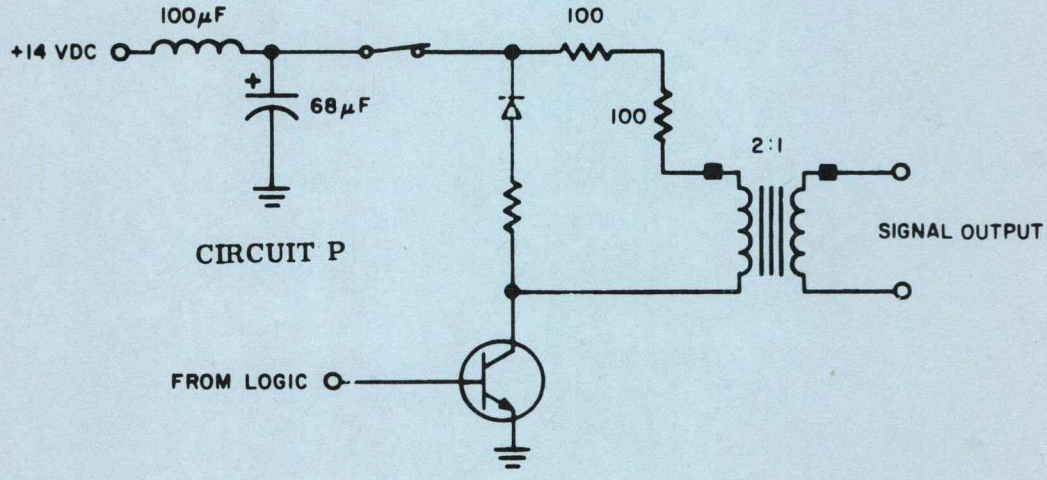
D discrete type input circuit



CIRCUIT C

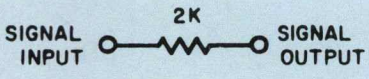


CIRCUIT D

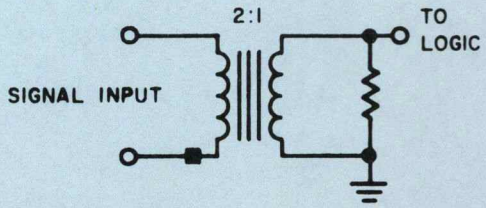


CIRCUIT P

CIRCUIT XT



CIRCUIT R



CIRCUIT Y

Figure 10-54. Interface Circuit Types

R resistor in series

S switch closure

W connecting wire

X transformer coupled output circuit (XT)

Y transformer coupled input circuit

The second letter designates the type of signal:

A indicates the signal is under counter control (each output pulse counted)

B indicates the signal is under program control

C indicates the signal is continuous

D indicates the signal is a dc level

E indicates the signal goes to an IN bit or comes from an OUT bit

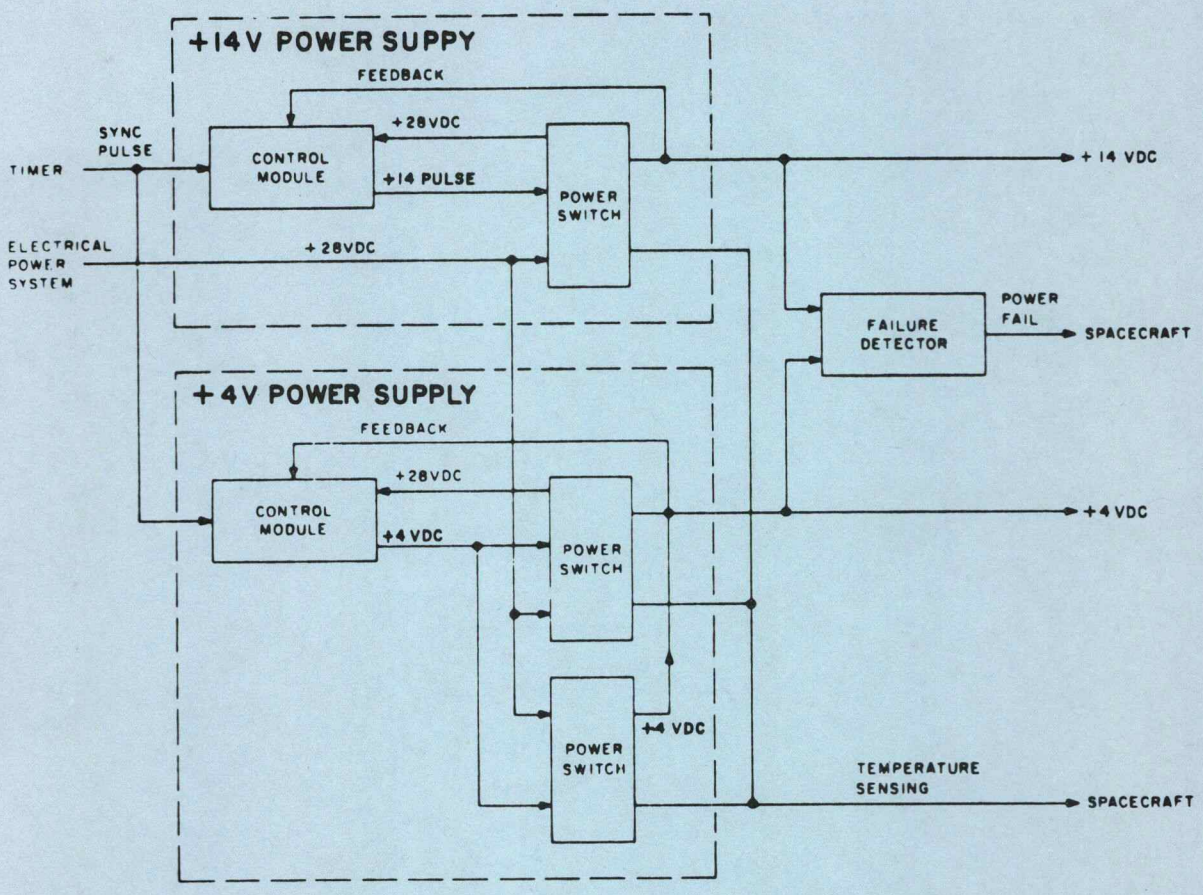
G indicates the signal goes to a counter

The digits indicate interface signals between specific systems:

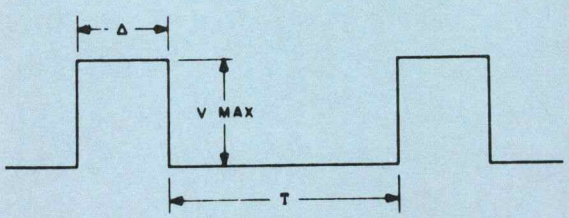
001 - 100	computer/spacecraft
100 - 200	computer/PGNCS
200 - 300	computer/DSKY
300 - 400	DSKY/PGNCS
400 - 500	DSKY/spacecraft
600 - 700	computer/GSE
700 - 800	computer/GSE
800 - 900	computer/spacecraft
900 - 1000	computer/PGNCS

10.10.8 POWER. LGC power (figure 10-55) is furnished by two switching-regulator power supplies: a +4 volt and a +14 volt power supply which are energized by fuel cells in the Electrical Power System.

Input voltage from the Electrical Power System is chopped at a variable duty cycle and then filtered to produce the required voltages. Chopping is accomplished by varying the pulse width of a signal having a fixed repetition rate and known amplitude. Referring to figure 10-55, V_{out} can be stated as $V_{out} = V_{max} \frac{\Delta}{A}$ Where: A is the fixed repetition rate, Δ is the pulse width, V_{max} is the known input amplitude. Therefore, V_{out} can be varied by changing the pulse width, Δ. Operation of the +14 volt power supply, which is typical of both, is described.



(a)



(b)

Figure 10-55. Computer Power Supply

Source voltage, +28 vdc, is supplied from the Electrical Power System through the power switch to the control module. The control module, essentially a pulse generator, detects the difference between the primary feedback output of the power supply and a reference voltage. (A secondary feedback path is connected to the CTS for marginal-voltage test operations.) A differential amplifier detects any change in the output voltage from the desired level. The output of the differential amplifier and a 51.2 kilocycle sync pulse from the timer drive a one-shot multivibrator in the control module. The differential amplifier output determines the multivibrator pulse width. The resultant +14 volt pulse is supplied to the power switch.

The power switch filters the control module output to produce the desired dc voltage. Additional filtering action protects the Electrical Power System from the wide load variations caused by the chopping action of the power supply. The power switch also contains a temperature sensing circuit. The +4 volt power supply requires two power switches due to load requirements.

The power supply outputs are monitored by a failure detector consisting of four differential amplifiers. There are two amplifiers for each power supply, one for overvoltage and one for undervoltage detection. If an overvoltage or undervoltage condition exists, a relay closure signal indicating a power fail is supplied to the spacecraft.

10.11 DSKY FUNCTIONAL OPERATION

The DSKY (figures 10-56 and 10-57) consist of a keyboard, power supply, decoder relay matrix, status and cuation circuits and displays.

The keyboard contains the key controls with which the astronaut operates the DSKY. Each of the key controls is lighted by 115 vac, 400 cps. Inputs to the CMC initiated from the keyboard are processed by the program. The results are suppled to either the decoder and relay matrix or to the status and caution circuits for display. Each key when depressed, with the exception of standby, will produce a 5 bit code. The keycode enters into the CMC and initiates an interrupt to allow the data to be accepted. The key reset signal (+28 vdc) is generated each time a key is released, and conditions the CMC to accept another keycode. The reset code and signal (+28 vdc) is used when the astronaut wishes certain display indicators to go out. It also checks on whether a particular indicator is transient or permanent. The clear code is used when the astronaut wishes to clear displayed sign and digit information. Key release turns the control of displaying information on the DSKY over to the CMC. The standby signal (+28 vdc) initiates putting the CMC into the standby mode. It also initiates putting the CMC into operate mode when pressed a second time.

The power supply utilizes +28 vdc and +14 vdc from the CMC power supply and an 800 cps sync signal from the timer to generate a 250 volt, 800 cps display voltage. The display voltage is applied to the displays through the relay matrix and status and caution circuits.

The decoder receives a four bit relay word (bits 12 through 15) from channel 10 in the CMC. The decoded relay word, in conjunction with relay bits 1 through 11 from channel 10, energizes specific relays in the matrix. The relays are energized by the coincidence of a selection signal from the diode matrix in the decoder which produces a row selection signal, and relay bits which produce column selection signals. Relay selection allows the display voltage (250 vac) from the power supply to be routed to the proper sign and digit indicators. Relay selection also allows the alarm common (0 vdc) or +5 vac from the PGNCS, or from the CM, to be routed through the relay to the PGNCS or to the CM (caution signals) or to the proper status and caution indicators respectively. The PGNCS caution signals from the relay matrix, represented by 0 vdc, are PROG CAUTION and GIMBAL LOCK. The status and caution indicators, lit by the +5 vac are: PROG, GIMBAL LOCK and NO ATT. All relays associated with the relay matrix are the latching type.

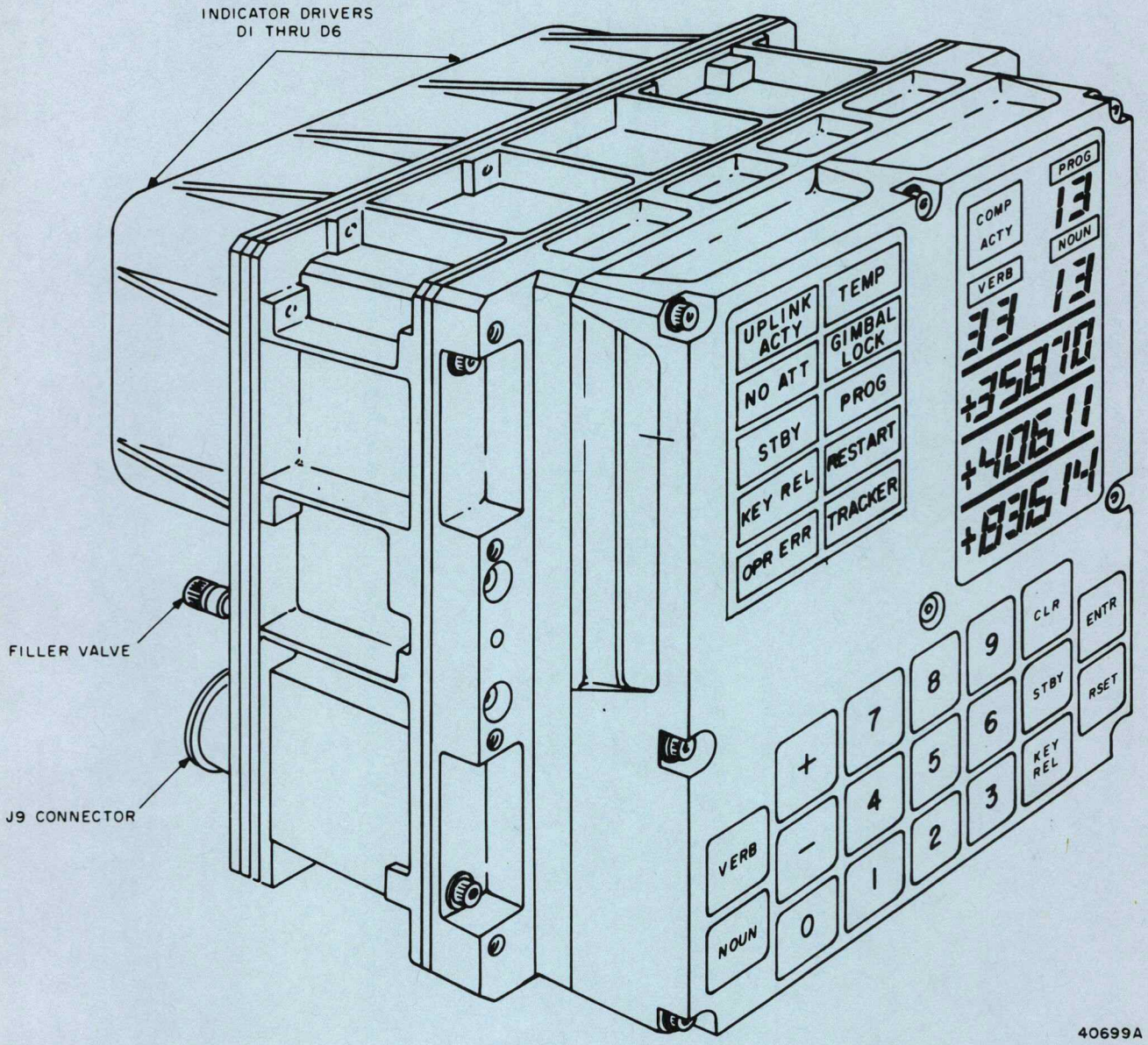


Figure 10-56. Main Panel and Navigation Panel DSKY

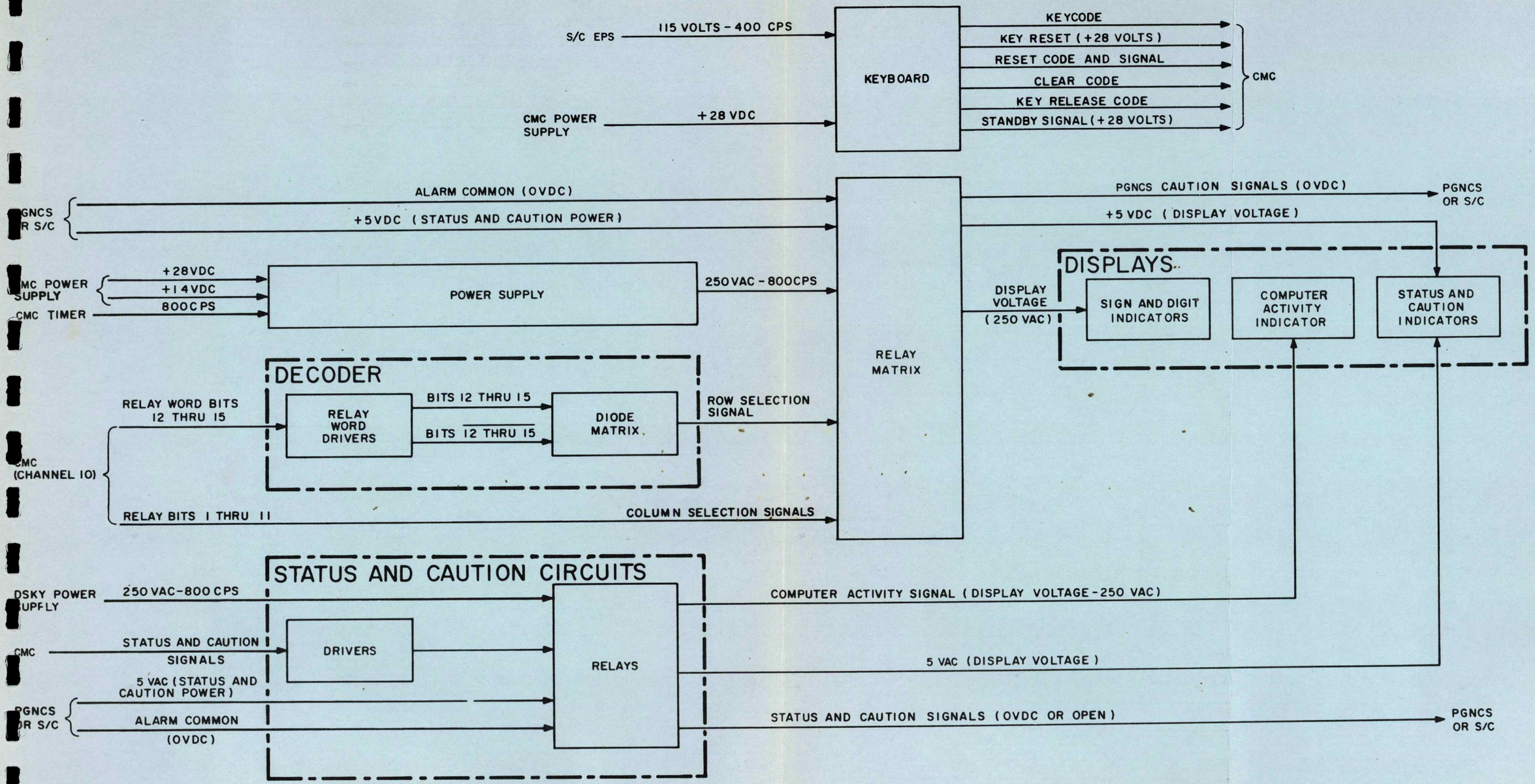


Figure 10-57. DSKY Functional Diagram

The status and caution circuits receive all CMC status and caution signals. Each signal is applied to a driver circuit and to an associated relay. When a relay is energized, it allows the voltage from the DSKY power supply (250 vac), or +5 vac or 0 vdc from the PGNCS or CM to be routed to the proper display indicators or equipment. The voltage from the power supply is routed through a relay to the computer activity indicator (COMP ACTY). The +5 vac is routed through relays to the following status and caution indicators: UPLINK ACTY, RESTART, OPR ERR, KEY REL, and TEMP. The status and caution signals, represented by 0 vdc or an open circuit, are ISS WARNING, STBY, CMCWAR, TEMP CAUTION, and RESTART. All relays associated with the status and caution circuits are the non-latching type.

The displays consist of sign and digital (operational and data display) and status and caution indicators. The sign and digital indicators allow the astronaut to observe the data entered or requested from the keyboard. The status and caution indicators present an indication of any variance from certain normal operations.

10.12 KEYBOARD

The keyboard consists of ten numerical keys (pushbuttons) labeled 0 through 9, two sign keys (+ or -) and seven instruction keys: VERB, NOUN, CLR (clear), STBY (standby), KEY REL (key release), ENTR (enter) and RSET (reset). Table 10-12 lists these keys (pushbuttons) and their functions.

Whenever a key is depressed, +14 vdc is applied to a diode encoder which generates a unique five bit code associated with that key. There is, however, no five bit code associated with the STBY key. These keys and their respective codes are shown in figure 10-58. If a key on the main panel DSKY is pressed, the five bit code associated with that key is entered into bit positions 1 through 5 of Input Channel 15 of the CMC. Note that this input will cause a request for the KEYRUPT 1 program interrupt. If a key on the navigation panel DSKY is pressed, the five bit code associated with that key is entered into bit position 1 through 5 of Input Channel 16 of the CMC. Note that this input will cause a request for the KEYRUPT 2 program interrupt.

The switches for the keys are wired in series to insure that only one input at a time is presented to the diode encoder and, consequently, only one code at a time to the appropriate input channel. Trap reset signals are associated with each DSKY. When a key is released on this main panel DSKY, signal TRAP 15 RESET is sent to trap circuitry in the CMC associated with the KEYRUPT 1 program priority interrupt; when a key is released on the navigation panel DSKY, signal TRAP 16B RESET is sent to the trap circuitry in the CMC assocated with the KEYRUPT 2 program priority interrupt.

10.13 DISPLAY INDICATORS

There are 24 display indicators on the DSKY; 21 digit display indicators and three sign display indicators. The locations of the digit display indicators are shown on figure 10-59. The indicators and their functions are described in table 10-13.

Table 10-12. DSKY Pushbuttons

Pushbutton	Function
0 through 9 pushbuttons	Enter numerical data, noun codes and verb codes into the CMC.
+ and - pushbuttons	Inform the CMC that the following numerical data is decimal and indicate the sign of the data.
NOUN pushbutton	Conditions the CMC to interpret the next two numerical characters as a noun code and causes the noun display to be blanked.
CLEAR pushbutton	Clears data contained in the data displays. Depressing this key clears the data display currently being used. Successive depressions clear the other two data displays.
STBY pushbutton	Commands the CMC to the standby mode when depressed the first time. An additional depression commands the CMC to resume regular operation.
KEY REL pushbutton	Releases the DSKY displays initiated by keyboard action so that information supplied by the CMC program may be displayed.
ENTR pushbutton	Informs the CMC that the assembled data is complete and that the requested function is to be executed.
RSET pushbutton	Extinguishes the lamps that are controlled by the CMC.
VERB pushbutton	Conditions the CMC to interpret the next two numerical characters as a verb code and causes the verb display to be blanked.

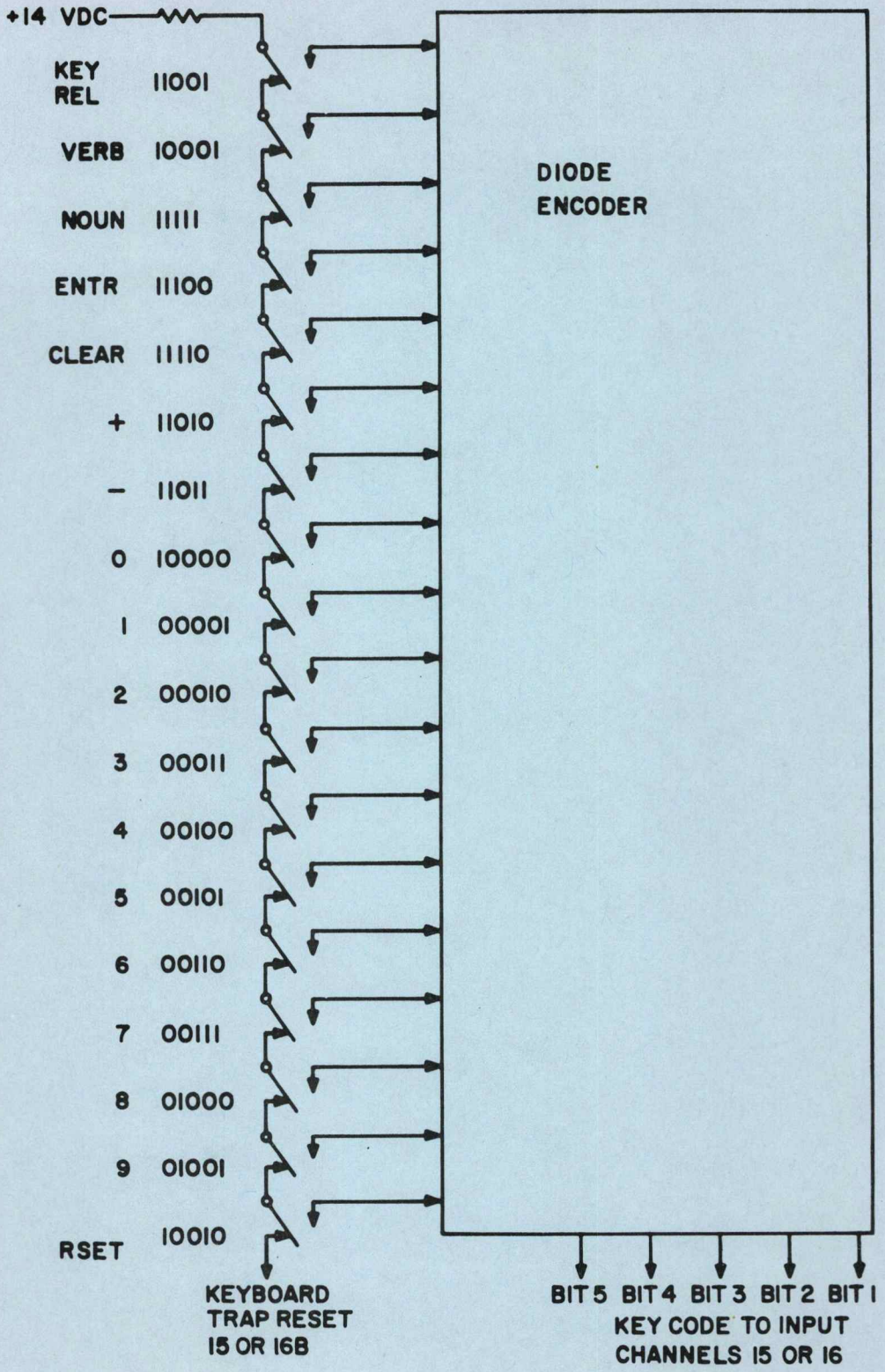


Figure 10-58. Diode Encoder and Associated Codes

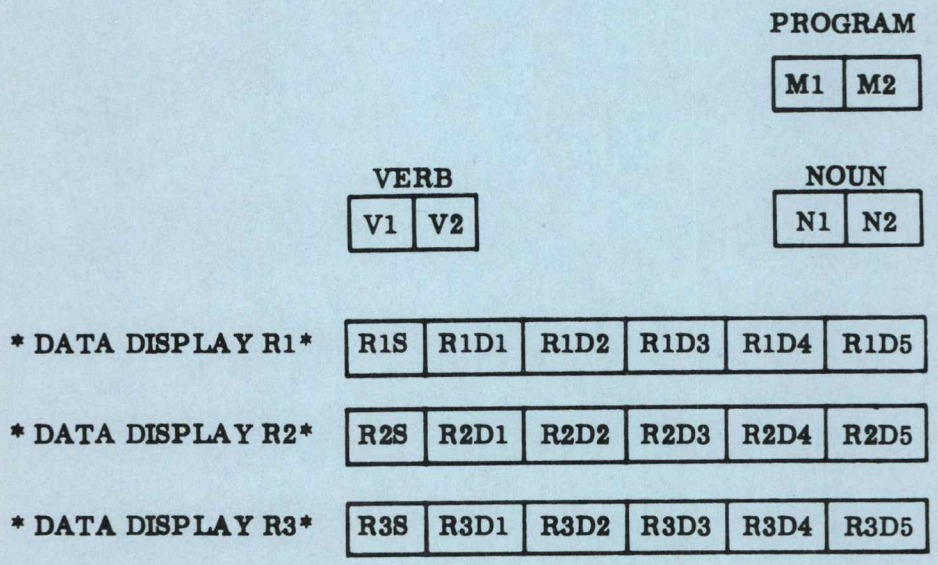


Figure 10-59. Display Indicators

Table 10-13. Display Indicators and Functions

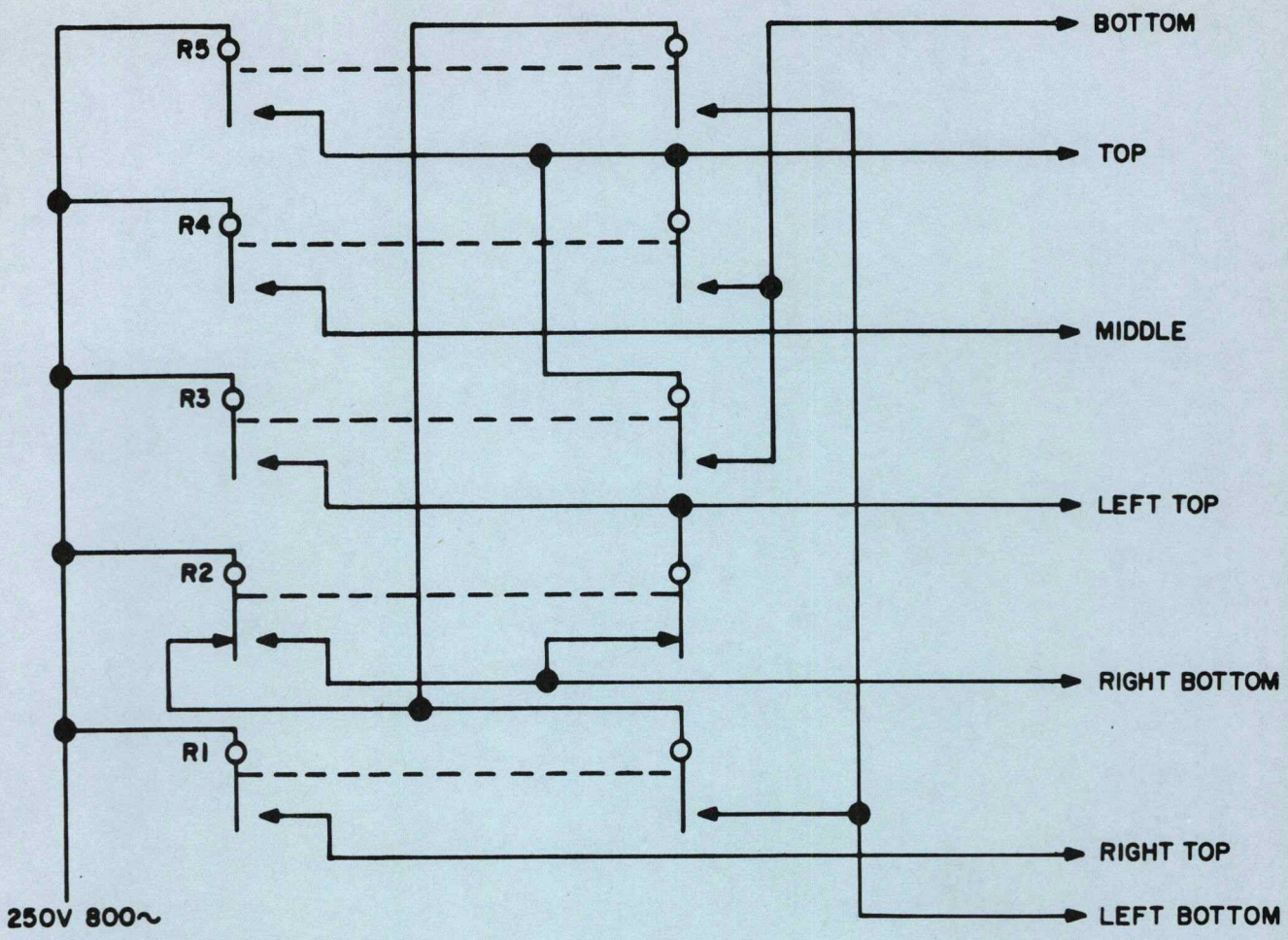
Display Indicator	Function
PROGRAM indicators	Indicate program being processed by CMC.
VERB indicators	Indicate verb code entered at keyboard or commanded by CMC.
NOUN indicators	Indicate noun code entered at keyboard or commanded by CMC.
DATA DISPLAY indicators	Indicate numerical data entered at keyboard or commanded by CMC and sign associated with this numerical data if it is in decimal.

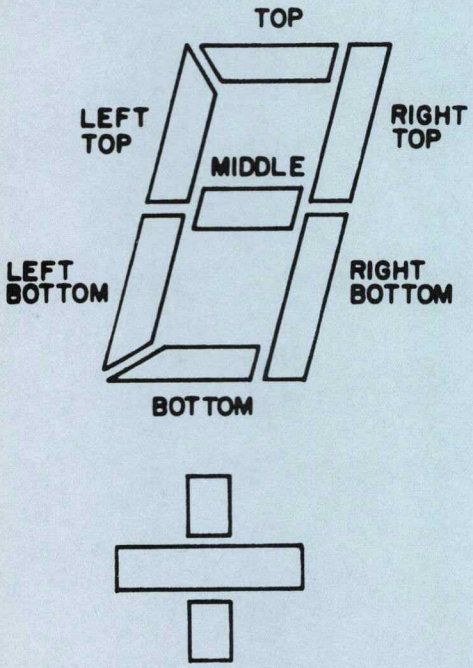
Any digit can be formed on a digit display indicator by lighting a proper combination of electro-luminescent lamps. There are seven of these lamps associated with each digit display indicator and each set of seven lamps is controlled by a set of five bistable relays (figure 10-60). Each sign display is controlled by a pair of bistable relays (one for +, one for -). Setting the proper bistable relays lights the proper sign.

The relays mentioned in the preceding paragraph are controlled by the CMC through output channel 10 (figures 10-61 and 10-62). There are other bistable relays in the DSKY in addition to those mentioned above. These relays are used for various command functions.

The relay matrix in figure 10-61 consists of 14 banks of 11 relays. Bits 15 through 12 of output channel 10 form a four bit code which is sent to a bank of four relay drivers. Each relay driver then generates two logic level outputs for its particular input: (1) the logic level of the input and (2) the complement of the logic level of the input. This eight bit code is sent to a diode decoder when it then supplies a ground to one of the fourteen banks of 11 bistable relays. This bank is uniquely specified by the eight bit code; consequently, the other 13 banks receive no ground. The outputs of the relay drivers associated with bits 11 through 1 of output channel 10 are tied to the set and reset coils of the relays in each of the 14 banks. Therefore, the outputs of the relay drivers associated with bits 11 through 1 of output channel 10 will set or reset those bistable relays in that bank to which ground has been applied.

The relays shown in figure 10-61 are divided into R relays and A relays. The R relays are used in conjunction with the display indicators and condition indicators. The A relays are used in conjunction with the condition indicators on the DSKY and switching associated with downline spacecraft warning and mode indications. Some of R and A relays can be enabled by inputs from other sources than the diode decoder and output channel 10.





RELAYS					DIGIT
R5	R4	R3	R2	R1	DISPLAYED
1	0	1	0	1	0
0	0	0	1	1	1
1	1	0	0	1	2
1	1	0	1	1	3
0	1	1	1	1	4
1	1	1	1	0	5
1	1	1	0	0	6
1	0	0	1	1	7
1	1	1	0	1	8
1	1	1	1	1	9

Figure 10-60. **Digit and Sign Displays**

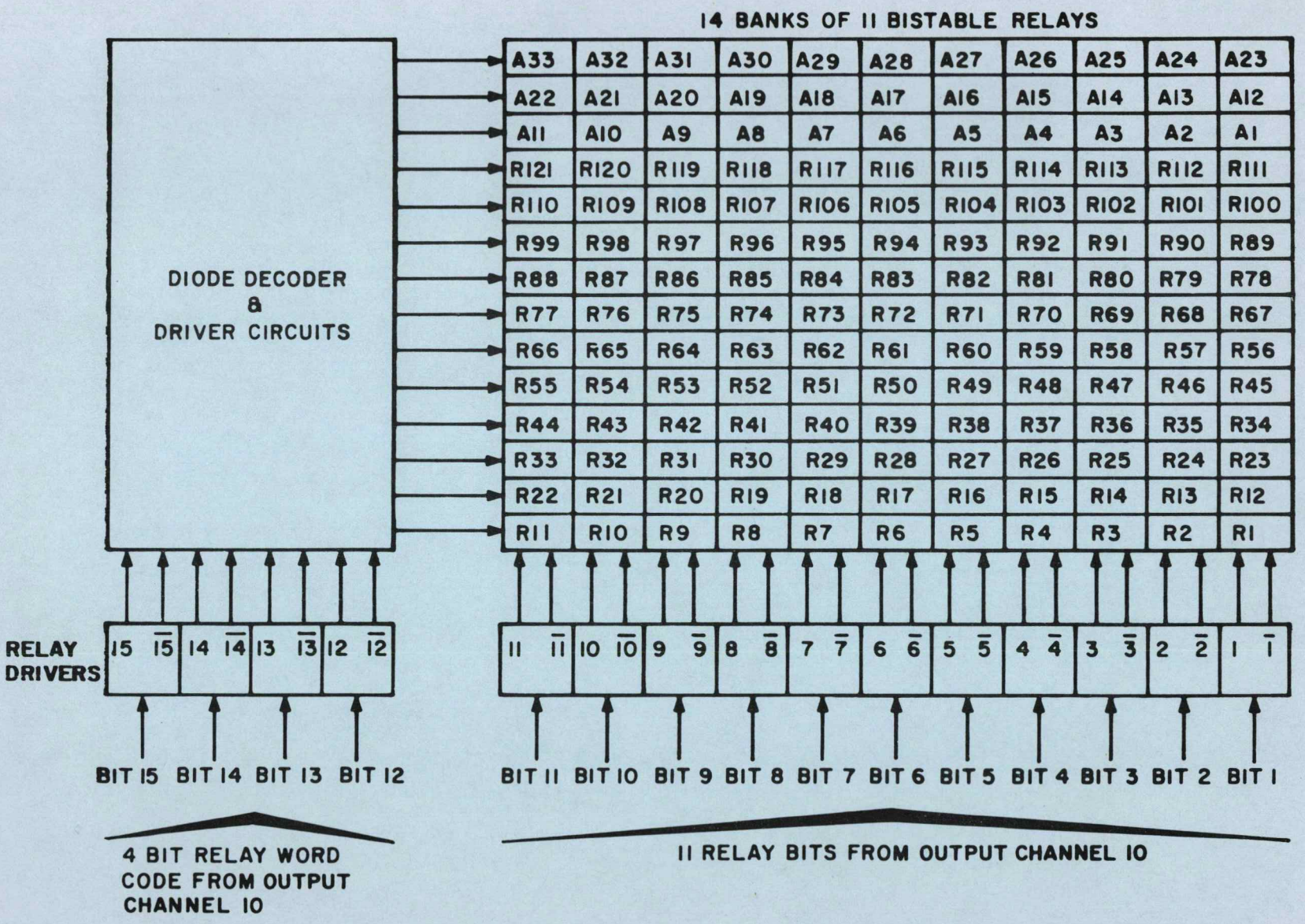


Figure 10-61. DSKY Display and Command Relay Circuitry

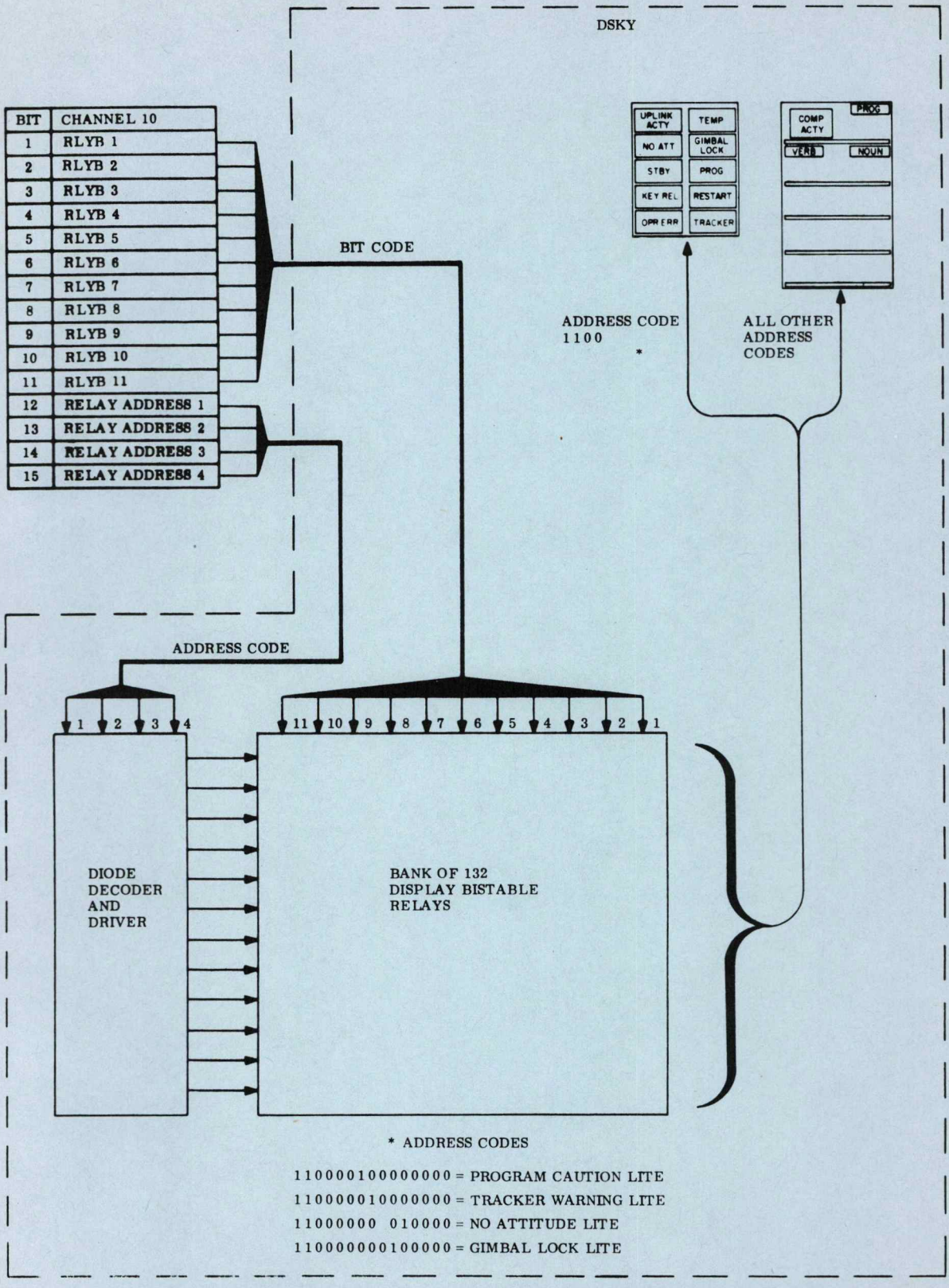


Figure 10-62. Channel 10 Interface

The following is a list of the R relays which are associated with the various display indicators.

R98 - R94	: M1	R82 - R78	: V1	R71 - R67	: N1
R93 - R89	: M2	R87 - R83	: V2	R76 - R72	: N2
R110	: R1S +	R55	: R2S +	R22	: R3S +
R66	: R1S -	R44	: R2S -	R11	: R3S -
R60 - R56	: R1D1	R32 - R28	: R2D1	R5 - R1	: R3D1
R65 - R61	: R1D2	R38 - R34	: R2D2	R10 - R6	: R3D2
R104 - R100	: R1D3	R43 - R39	: R2D3	R16 - R12	: R3D3
R110 - R105	: R1D4	R49 - R45	: R2D4	R21 - R17	: R3D4
R115 - R111	: R1D5	R54 - R50	: R2D5	R27 - R23	: R3D5

10.14 DSKY CONDITION INDICATORS

There are ten condition indications displayed on the DSKY. (Figure 10-63 and 10-64). Table 10-14 lists the indicators and their functions.

The UPLINK ACTY indicator will light if bit position 3 of Output Channel 11 contains a logic 1.

The TEMP indicator will light if:

(1) Bit position 4 of Output channel 11 contains a logic 1, or

(2) Bit position 15 of Output channel 30 contains a logic 0.

The GIMBAL LOCK indicator will light if bit position 6 of Output channel 10 contains a logic 1 and bit positions 15 through 12 of the same channel are 1, 1, 0, 0 respectively.

The PROG indicator will light if bit position 9 of Output channel 10 contains a logic 1 and bit positions 15 through 12 of the same channel are 1, 1, 0, 0 respectively.

The RESTART indicator will light if a GOJAM signal is generated.

The NO ATT indicator will light if bit position 4 of Output channel 10 contains a logic 1 and bit positions 15 through 12 of the same channel are 1, 1, 0, 0 respectively.

The STANDBY indicator will light if the STANDBY circuit is enabled. The indicator will also light if a light test is performed.

The KEY REL indicator will light if bit position 5 of Output channel 11 is a logic 1. This indicator is modulated by the flash signal.

The OPR ERR indicator will light if bit position 7 of Output channel 11 is a logic 1. This indicator is also modulated by the flash signal.

The COMP ACTY indicator will light if bit position 2 of Output channel 11 is a logic 1.

The TRACKER indicator will light if bit position 7 of channel 30 contains a logic 1.

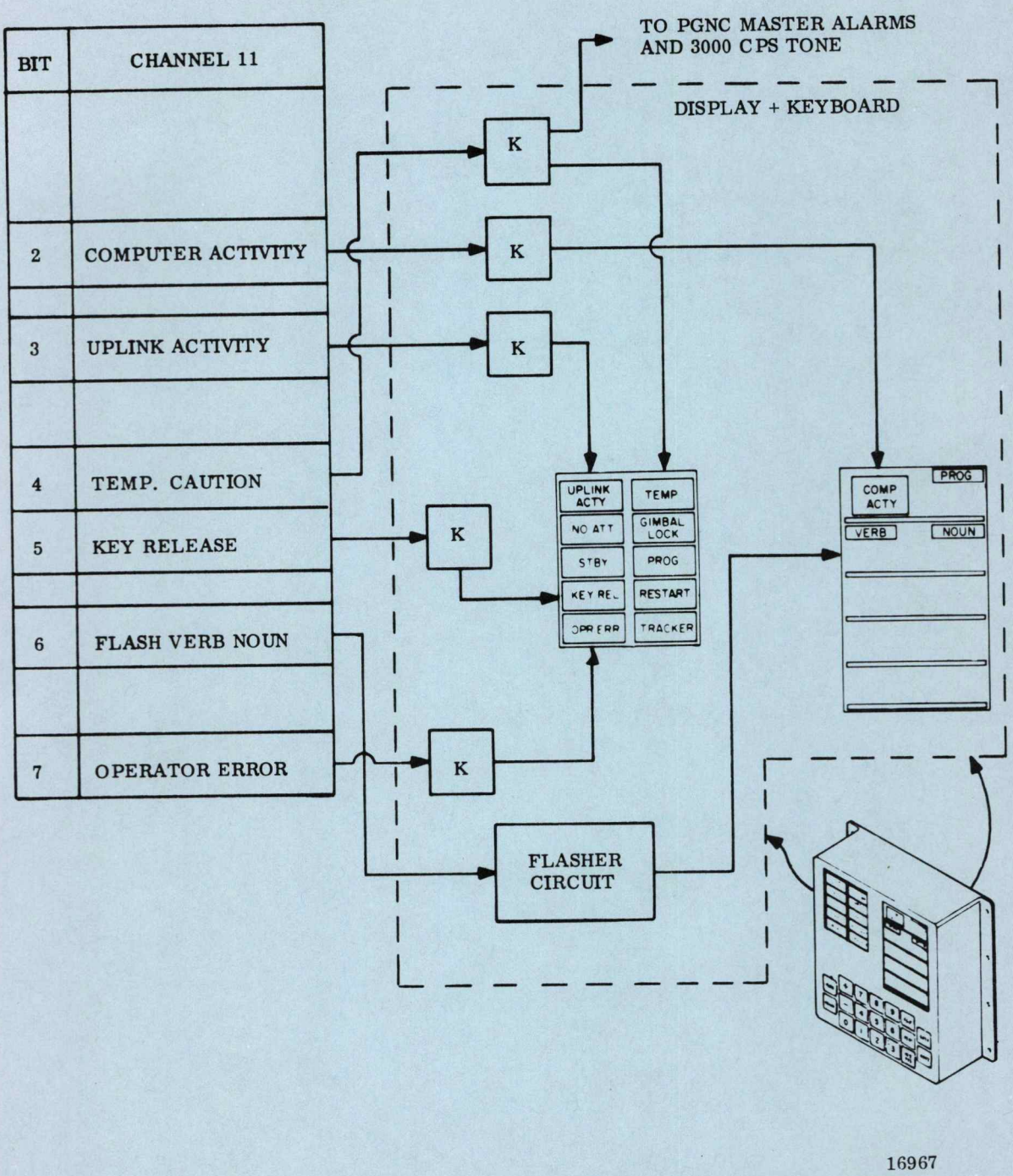


Figure 10-63. Channel 11, Bits 2 through 7 Interface

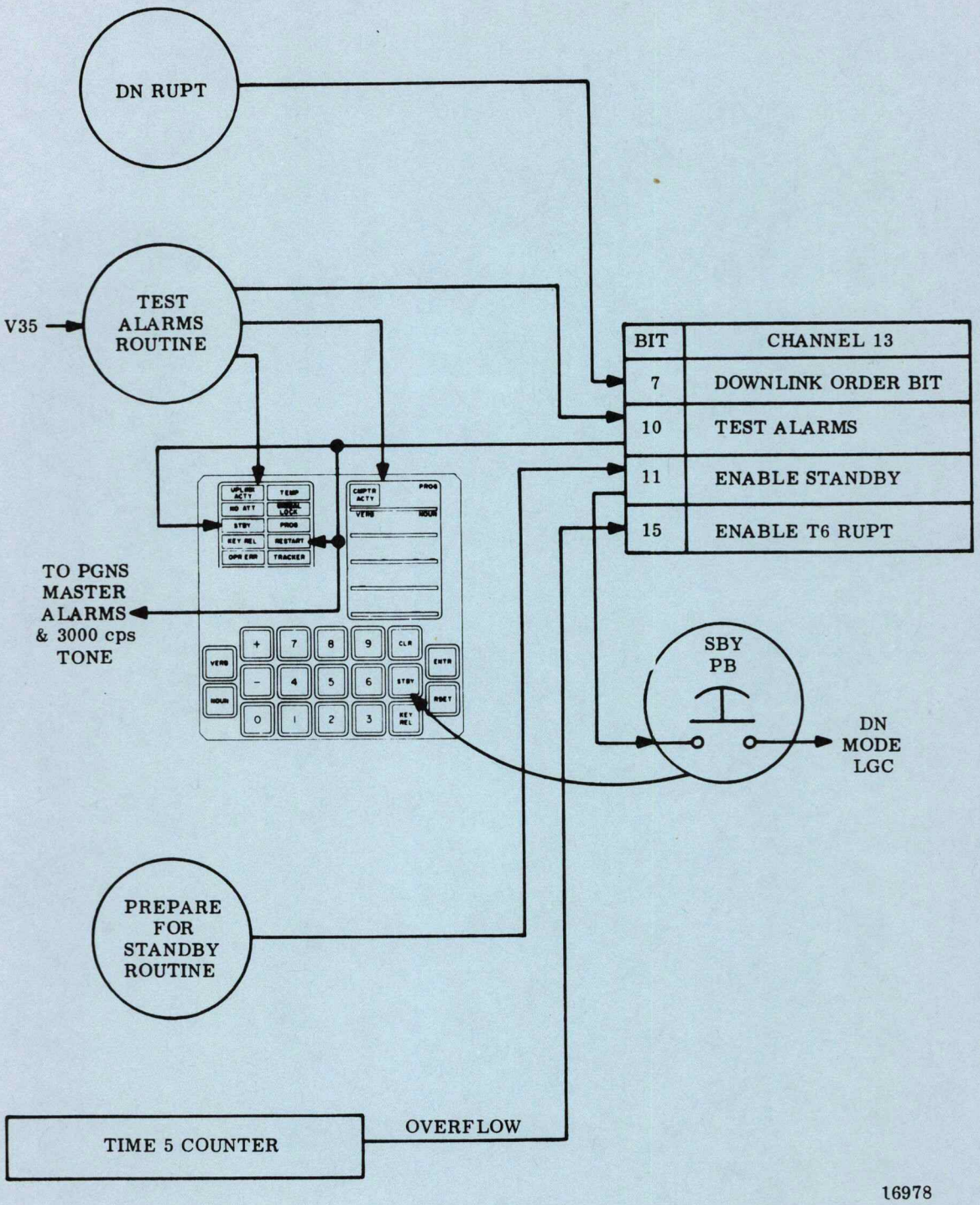


Figure 10-64. Channel 13, Bits 7, 10, 11 and 15 Interface

Table 10-14. DSKY Condition Indicators

Indicator	Function
UPLINK ACTY indicator	Indicates that information is being received via UPLINK.
TEMP indicator	Indicates that the stable member temperature has exceeded its design limit by $+5^{o}F$.
GIMBAL LOCK indicator	Indicates that the middle gimbal has driven greater than $\pm 75^{o}$ from its zero position.
PROG indicator	Indicates that a program check has failed.
RESTART indicator	Indicates: 1. That a word has been incorrectly transferred from memory - Parity Fail. 2. That (a) too many consecutive TC or TCF instructions have occurred or (b) TC or TCF instructions have occurred too infrequently. 3. That interrupts are too long or too infrequent - RUPT Lock. 4. That the CMC has not accomplished a new job within a period whose duration is program dependent and various from .64 to 1.92 seconds - Night Watchman. 5. That a test alarm has been generated by program control.
NO ATT indicator	Indicates that the ISS is not suitable as an attitude reference.
TRACKER indicator	Indicates an optics CDU failure.
STBY indicator	Indicates that the computer is in the standby condition.
KEY REL indicator	Indicates that the CMC program has attempted to use the DSKY and found it busy.
OPR ERR indicator	Indicates that an illegal keyboard operation has been performed.
COMP ACTY indicator	Indicates that the CMC is in a program other than dummy job and that the CMC is not in the standby mode.

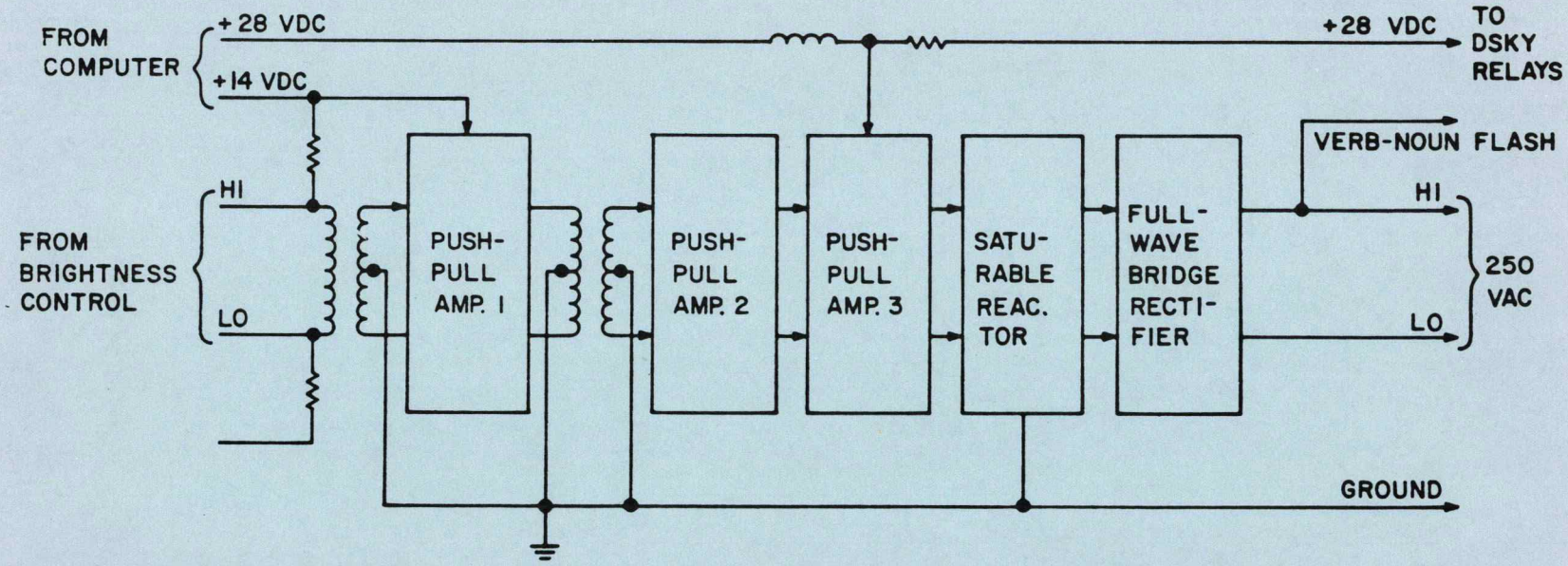


Figure 10-65. DSKY Power Supply

10.15 DSKY POWER SUPPLY

The DSKY power supply inputs are +28 vdc and +14 vdc from the CMC power supply and 800 cps from the CMC timer. The output of 250 volts, 800 cps, is used to light the DSKY display registers.

The power supply (figure 10-65) contains three transformer-coupled, push-pull amplifiers; a saturable reactor; and a full-wave bridge rectifier. The input to the first stage is an 800 cps square wave which varies about a +14 vdc level. The dc level is controlled by the brightness control on the astronauts' control panel. The two transformers step up the voltage applied to their primaries. The three amplifiers also increase the amplitude of the input voltage. The output from the third push-pull amplifier is applied to the saturable reactor.

The saturable reactor and its associated circuitry regulate the voltage applied to the display registers. The displays act as a variable capacitive load which varies as a function of the number of register indicators which are lighted. Changes in the capacitive load are reflected back to the control winding of the reactor through the full-wave rectifier bridge. As the number of lighted indicators increases, the voltage applied to the reactor control winding increases. This increased control winding voltage drives the reactor further into saturation and keeps the output relatively constant. If the load decreases, the control winding voltage decreases and the reactor becomes less saturated.

Computer 28 vdc is filtered and used to operate the DSKY relays.

10.16 SUMMARY

The CMC is a core memory, digital computer which serves as the central processing element of the PGNCS. It permanently stores all the navigation tables, trajectory parameters, programs and constants necessary to solve the guidance and navigation problems. The CMC processes data and issues discrete control signals, both for the PGNCS and other spacecraft systems. It is a control computer with many features of a general purpose computer. As a control computer, the CMC aligns the stable platform of the IMU, positions the optical unit and issues commands to the spacecraft. As a general purpose computer, the CMC solves the PGNCS calculations required for the Apollo mission. In addition, the CMC also monitors the operation of the PGNCS.

The CMC can be functionally divided into a timer, sequence generator, central processor, memory and priority control. The timer provides all of the necessary synchronization pulses to insure a logical flow of data from one area to another inside the CMC. The sequence generator combines basic timing pulses defining action times with the order codes to produce a set of sequential control pulses. The central processor performs the necessary arithmetic and logical data manipulations. The memory area provides a storage capacity of 38,912 (16 bit) words. The priority control time shares the computer to process the different input and output requirements.

The DSKY consists of a keyboard, power supply, decoder, relay matrix, status and caution circuits, and displays.

The keyboard consists of ten numerical keys, two sign keys and seven instruction keys. When a key is pressed, a five bit keycode is entered into input channel 15 of the CMC.

The displays consist of 21 digit displays, three sign displays, and ten condition displays. Any digit can be formed by the lighting of the proper combination of electroluminescent panels. The lighting of these panels is controlled by CMC output channel 10.