This is different Info. from that received on the phone from Mike C.
JCH3

To: Geo. Silver

Please return to L. Larson

MEMORANDUM

11 December 1970
AP70-00826

RECEIVED
DEC 22 1970
GEORGE SILVER

TO: W. Gahan, W. Nelson

CC: T. Hanley, M. Cavalier, J. Wachholz, M. Lynn, S. Sudman, W. Farley, D. Grassell, H. Elingsen, C. Gigstead, W. Schwantes, J. Barker (MIT)

SUBJECT: G&N EFFECTS OF "A" HARNESS SHORT, S/C 110

REFERENCE: DSE-Apollo(P)-78, AFR 23251

During testing of Apollo G&N System 214 in Spacecraft 110 at KSC on November 9 an anomaly occurred which manifested itself in gimbal motion with the application of 28VDC to the OSS buss. The +28VDC ISS buss was off during this period, yet monitoring equipment measured a DC level of 6.1 volts on the ISS buss.

The cause was later isolated to a short between pins 40 and 41 of connector 96-P1 in the "A" Harness. This resulted in the OSS 28 volt 1% 800 cycle supply being connected in parallel with the ISS 28 volt 1% 800 cycle supply.

Since ISS power was off, power from the OSS 800 cycle supply was being delivered to the ISS 800 cycle load and also to the output of the ISS 800 cycle amplifier. Part of this energy was converted to a DC voltage and applied to the +28 volt DC ISS buss via the output transformer and rectifying action of the output transistors. The circuit is as shown in Figure 1.

In failure isolation tests G&N 214 was actually operated for two conditions for several minutes each where OSS was "ON" and ISS "OFF" and with OSS "OFF" and ISS "ON". Total power dissipation would be approximately the same in each case. The circuit of Figure 3 would however have the largest short circuit current flow.

Simulated failure tests were made using a breadboard amplifier of the 800 cycle 1% supply. These tests aided in substantiating the failure and in analyzing the short circuit effects on the "driven" 800 cycle 1% amplifier and also on the "driver" 800 cycle 1% amplifier.

It was determined that the output transistors in the driven amplifier were acting as Zener switches when the emitter-to-base voltage exceeded the break down level of approximately 16 volts. With 14 volts RMS across each half of the primary, each transistor was "ON" (conducting) about 20% of each cycle. Figure 2 shows the equivalent circuit.

This "ON" time can be calculated as follows:

Peak voltage = 2 (14) = 20 volts

20 Cos θ = 15 Cos θ = 16/20 = 0.8

θ = 37° 2 θ = 74°

74/360 = 20.5% "ON" Time

Since each transistor is "ON" for 20% of each cycle the total "ON" time for both transistors is 40%. Peaked current waveform observed through an induced short circuit test on C&N 207 are shown in Figure 3a. Voltage waveforms tend to be flattened slightly at their peaks because of the additional loading effects during this period.

Figure 3 shows the power dissipation levels that occur under the shorted condition. The values shown were obtained from empirical and analytical sources and should closely represent the actual case.

Power dissipation will be most severe in the driving 800 cycle power amplifier since it must supply the two parallel loads plus that required to drive the output of the driven 800 cycle amplifier as detailed in Figure 3. Total load power under the conditions shown is approximately 24 watts. Power input to this amplifier is approximately 50 watts resulting in 26 watts of internal amplifier dissipation. Of this, 2 watts is dissipated in the output transformer and 12 watts in each output transistor Q4 and Q5.

The transformer has a secondary resistance of 0.8 ohms and 0.5 ohms in each half of the primary. Secondary and primary currents were measured at 0.86 amperes and 1.7 amperes respectively. Therefore $P_{SEC} = I^2R = (.86)^2 (.8) = 0.6$ watts $P_{PRI} = (1.7)^2 (0.5) = 1.4$ watts or 2 watts total. Because of the size and construction of this transformer, no appreciable temperature rise and consequently no overstress occurred.

Power dissipated by the output transistors is as follows:

P = IE X 50% duty cycle

= (1.7 amp) (14 volts) X 0.5 = 11.9 watts

These levels of current and power are considerably less than their rated capabilities. A potential overstress analysis was made by Dept. 32-37. (Ref. DSE-Apollo(P)-78) on these transistors at power level dissipations of 20 watts each which allows a 60% margin.

The results of their analysis indicate no overstress occurred and that devices submitted to these conditions are flightworthy.

G. Hamren

Approved by: R. Kraemer

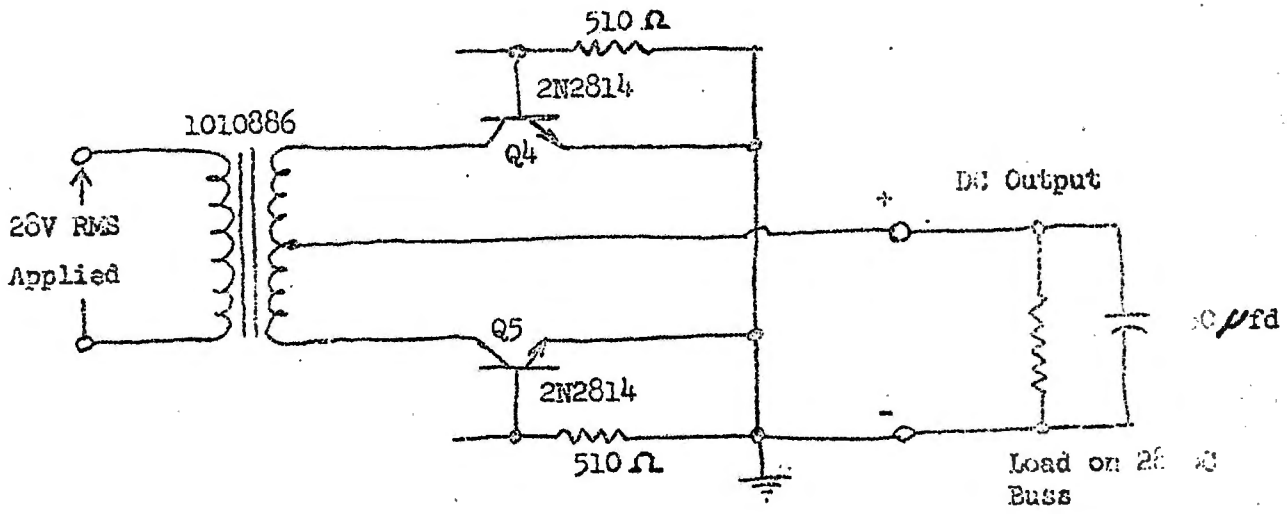


Figure 1

800HZ 1% Amplifier Output Stage

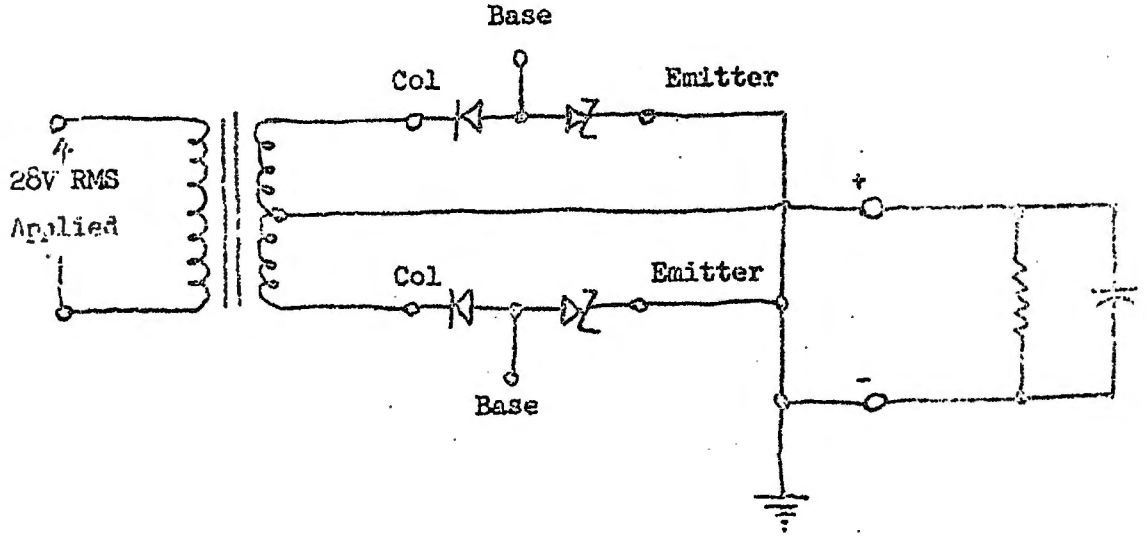


Figure 2

800HZ 1% Amplifier Equivalent Effect of Output Stage

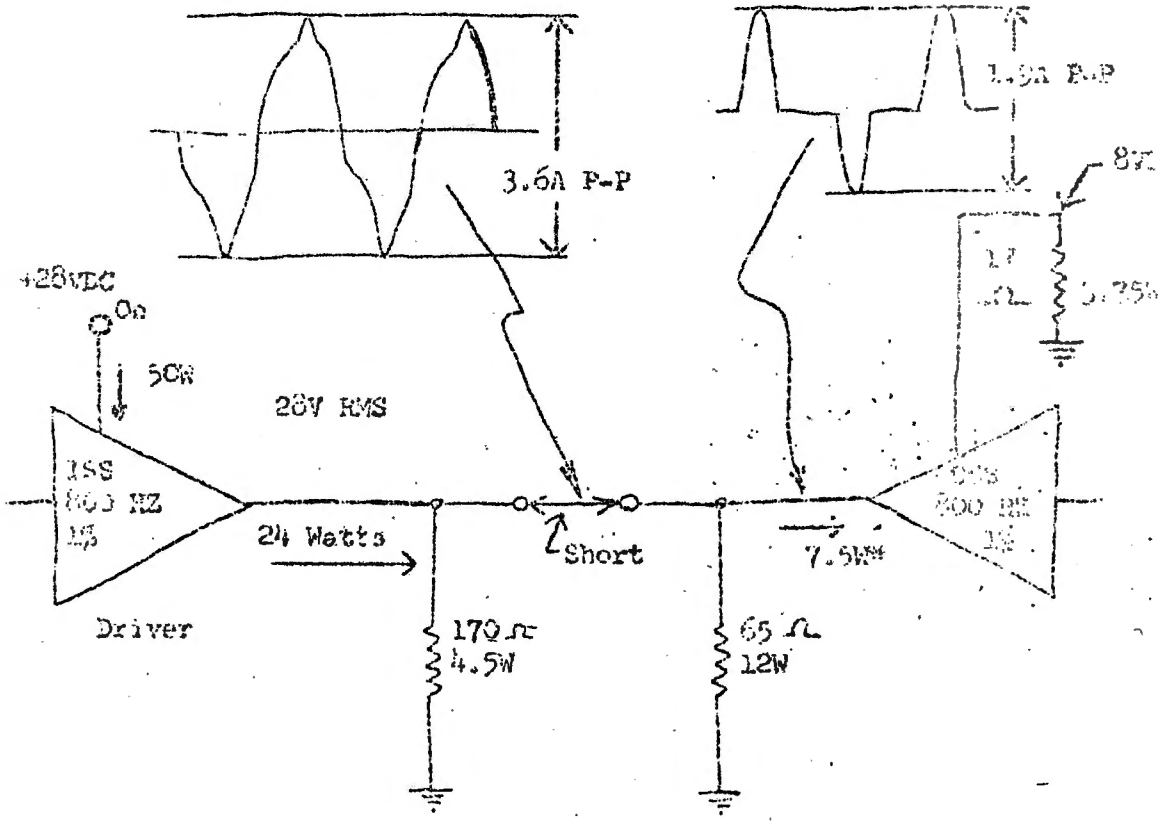
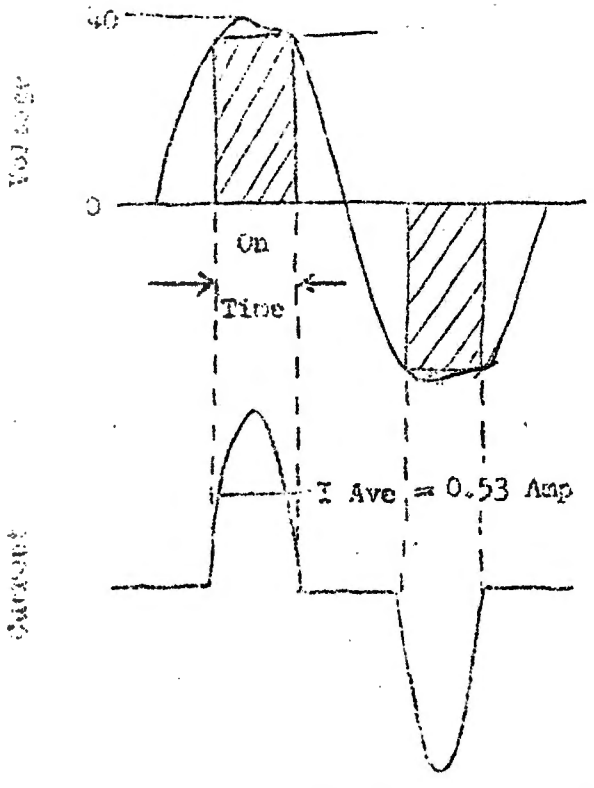


Figure 3a. Power Distribution During Shorted Condition of ISS Supplying the OSS 800HZ Amplifier



* P = 35V X .53 Amp X 40% On Time

= 7.5 Watts

Figure 3b. Voltage and Current at Input to OSS 800HZ Output