

LUMINARY Development Note #54

To: Distribution
From: Dave Moore
Date: 1 July 1970
Subject: Odd Things in a "Simple" Test of Coding Paths in P66

Summary:

The events in the simulation test which prompted further questions and analysis have been resolved. It has been seen that no undue or excess changes in guidance or throttle commands occur. Justification of the sequence of events is based on the enclosed time chart. Therefore all questions are answered and events explained within this memo.

History:

When Luminary 173 was made and before 23B wanted to be confident in the assembly a test of P66 coding paths was submitted. On the surface, paths taken were correct as advertised in coding design purposes. Digging deeper it was found that odd messages were printed at seemingly unlikely times in the simulation. To track down the cause of these oddities clocks, traces and dumps were inserted (with TLOSS variations) into the simulation.

Sequence of Events:

The test began to be interesting in P64 just before switching to P66 (via SCSMODE ATTHOLD and ROD) at about 600 ft. The events are listed below and a discussion of each event follows.

List of Events to be Questioned:

- A) 31201s in P64 (is there a hung P64 job?)
- B) 1410 alarm in P66 and what it allows (any hung P64 job to start up again?)
- C) P66 omission at T=373379 - why? (what happens after omission?)
- D) DCMCL clock without FINDCDUW or TCQCDUW (is this part of hung P64 job?)

- E) N82CDUSP & TCQCDUW (is this also part of hung P64 job?)
(where does job go via Q?)
- F) P66 omission (why?) (what about Servicer's coming on .5 sec after one another?)
- G) P66 omission - 1466 (did hung Servicer job cause this?)
- H) P66 omission - 1466 (why only 1 Rodcomp since last omission?)
- I) P66 omission at T=373399.25
- J) P66 omission at T=373405.27
- K) P66 omission at T=373453.24

Discussion of Events:

A) 31201's in P64 (FINDCDUW jobs hung at 20% TLOSS): Note that 5 FINDCDUW's are missed before 31201 cleans up VAC areas and lets a FINDCDUW get through. However, only 2 get through after first 31201 before 4 more are missed (+1 restarted via group 3 in restart logic = 5 total) and then the second 31201 comes along. Two are begun in P64 before the first FINDCDUW is missed and before the job test can back up any further, P66 is entered. Thus, a FINDCDUW from P64 is hung when P66 is entered. Given a chance (through TLOSS reduction or omission of P66 jobs) this P64 job will crank on through to finish.

B) 1410 ALM allows FINDCDUW -2 from P64 (see (A)) to be accessed but is hung before completion by Servicer + P66's coming up. (Also, TLOSS went from 20% to 18% just before FINDCDUW -2 accessed.)

C) P66 omission (T=373379.414): TLOSS of 18% + FINDCDUW being accessed at T=373375.6. Evidently time left was less than 2LATE466 would allow. In fact time from Servicer to P66 = 1.7 seconds, .2 seconds greater than 2LATE466. (This will open door for any hung up jobs.)

D) DCMCL accessed (continuation of hung P64 FINDCDUW job) as a result of the P66 omission discussed in (C). Hung from finishing by Servicer & P66 job coming in. Will finish later.

E) N82CDUSP & TCQCDUW accessed to finish P64 (hung FINDCDUW) job. Evidently return from FINDCDUW is to P66VERT which sets up another RODCOMP only .6 sec since last RODCOMP. This RODCOMP goes to VERTDISP. Then the RODCOMP set up by P66 at (373380) (before

P64 hung job finished) comes on .24 seconds late and .6 secs after RODCOMP set up by TCQCDUW (finish of hung P64). Then the RODCOMP set up by P66VERT (return address of TCQCDUW) comes on .5 seconds after the late RODCOMP (late by .2). Finally this madness is straightened out but the timing is such that at 373389 a P66 is omitted.

F) P66 omission (T=373389): Timing off so that 2LATE466 time not enough due to 2 extra RODCOMPs from TCQCDUW in (E). This is compounded by a Servicer being late stemming from 2 Servicer calls from 373379.723 to 373383 and only 1 Servicer accessed in this time. The late Servicer comes in at 373383.233 (2 secs late). In the meantime another Servicer is requested at 373383.723 but does not come on until 373385.269 whereupon another Servicer is requested and comes on at 373385.746. This means a Servicer is hung up. The P66 omission allows this Servicer (hung from 373385.269) to get through after only 1 P66 job done. Also TLOSS = 16% at 373390 (from 18%).

G) P66 omission - 1466 ALM at 373391.65 only 1 throttle (1 P66 complete) between 373389.437 (P66 omission w/o alarm) to 373391.6 so that TOOFEW criteria is enough for 1466. Note COPYCYC at 373391.573. The COPYCYC returned to P66 so P66 clocked 2 times between 373390.62 and 373391.654. Only 1 P66 (RODCOMP) actually done in that time, however. The P66 at 373390.62 called a RODCOMP which comes in late at 373392.048 (1.4 secs). This will cause another 1466 ALM because that RODCOMP did the only throttle job and was 1.4 secs late.

H) P66 omission - 1466 alarm at 373393.247 caused by late Servicer calling P66 which set up RODCOMP which subsequently was late and did only 1 throttle job since last omission.

I) P66 omission at T=373399.247. After the 2 1466 alarm madness finished, still had 16% TLOSS. Timing such that from Servicer call at 373397.723 to P66 at 373399.242, time = 1.52 secs so that 2LATE466 criterion just met ($1.52 \approx 1.5$ sec). This allows P66 omission without alarm.

J) P66 omission at T=373405.272. Still have 16% TLOSS after P66 omission at T=373399.247. Timing again such that from Servicer call at 373403.723 to P66 at 373405.266 time = 1.54 secs so that 2LATE466 criteria just satisfied again ($1.54 \approx 1.5$). So have P66 omission without alarm.

**Note: Cases (I) and (J) are from timing problems due to TLOSS - making P66 omissions. The timing is getting close to 1.5 secs (another omission) 4 P66 (RODCOMP) vertical passes later at 373410.3 but at 373410 TLOSS changed to 14% from 16%. A simulation has been submitted on 6/26/70 to see if 16% TLOSS is that TLOSS which will cause a P66 omission after every 4 throttle jobs (so TOOFEW criteria not met even though 2LATE466 criteria is).

K) P66 omission at T=373453.243. TLOSS = 14% from T=373410 to T=373430. TLOSS = 12% from T=373430 to 373460. TLOSS = 10% from T=373460 to end of run. So still have TLOSS = 12% (after timing O.K. from last P66 omission at 373405). Timing built up so that noticing Servicer vs. P66 clocks just before P66 omission: Servicer at T=373451.723; P66 at 373453.237 Time = 1.51 so that 2LATE466 criterion just satisfied ($1.51 \approx 1.5$).

**Note: After case (K) timing such that no more P66 omissions occur.

Conclusions:

All events (odd and otherwise) to be questioned are justified by timing chart and late Servicers, etc. Questions answered and events explained.

To Be Done:

Answer if TLOSS = 16% is TLOSS so that P66 omitted every 4 throttle jobs.

SEQUENCE OF EVENTS
TIME CHART

It may prove necessary to refer to this table when reading the discussion of the events.

Notation: For the following time chart the following abbreviations are used:

S - Servicer

C - COPYCYC

F - FINDCDUW -2

N - N82CDUSP

T TCQCDUW +2

SP66 - STARTP66

P66 - P66

R - RODCOMP

V - VERTDISP

OMIT66 - P66 OMISSION

Also, the actual AGC time in the AGC time column is $373000.000 + T$
where T is that number in the time column.

TLOSS	MODE	REQUEST	EVENT	TIME
0	64	S		341.5725
			S	341.5789
			F	342.817
			T	343.038
		S		343.5725
			S	343.5789
			F	344.806
.20			T	345.041
		S		345.573
			S	345.589
			F	347.01
			T	(missed)
		S		347.573
			S	347.61
			F	349.43
			T	(missed)
		S		349.573
			S	349.61
			F	351.49
			T	(missed)
		S		351.574
			S	351.61
			F	353.504
			T	(missed)
		S		353.583
			S	353.593
			F	355.443
			T	(missed)
		S		355.593
			31201	355.594
		F		355.613
		S		355.624
			S	355.691

TLOSS	MODE	REQUEST	EVENT	TIME
.20	64		F	357.229
			T	357.636
		S		357.639
			S	357.833
			F	359.529
		S		359.643
			T	359.945
			S	360.130
			F	(missed)
		S		361.643
			S	361.658
			F	363.553
		S		363.657
			S	363.671
			F	365.554
		S		365.663
			S	365.688
			F	367.571
		S		367.673
			31201	367.675
		F		367.697
		S		367.704
			S	367.768
			F	369.313
			T	369.698
		S		369.713
			S	369.901
			F	371.576
		S		371.715
			T	371.933
			S	372.118
			C	372.989
			F	(missed)
		S		373.723
			S	373.782
			C	373.606
			SP66	373.698

TLOSS	MODE	REQUEST	EVENT	TIME
.20	66		P66	374.799
			1410	374.828
			R	374.832
.18				375.000
			V	375.184
			F	375.609
		S		375.723
			S	375.736
			R	375.848
			V	376.249
			C	377.035
			P66	377.114
			R	377.506
		S		377.723
			V	377.846
			S	378.030
			R	378.521
			V	378.831
			C	379.33
			P66	379.409
			OMIT66	379.414
			V	379.416
			DCMCL	379.656
		S		379.723
			S	379.735
			C	380.529
			P66	380.647
			R	381.034
			V	381.339
			N	381.643
			T	381.654
			P66VERT	381.656
			R	381.659
		S		381.723
			V	382.057
			R	382.237

TLOSS	MODE	REQUEST	EVENT	TIME
.18	66		V	382.556
			R	382.742
			V	383.055
			S	383.233
		S		383.723
			C	384.383
			P66	384.413
			R	384.779
			V	385.084
			S	385.269
		S		385.723
			S	385.746
			R	385.779
			V	386.131
			C	387.047
			P66	387.122
			R	387.485
		S		387.723
			V	387.850
			S	388.039
			R	388.526
			V	388.842
			C	389.346
			P66	389.432
			OMIT66	389.437
			V	389.439
		S		389.723
			S	389.739
.16			C	390.000
			P66	390.476
			R	390.623
			V	390.957
			C	391.261
			P66	391.573
			OMIT66	391.654
			1466	391.664
			V	391.668

TLOSS	MODE	REQUEST	EVENT	TIME
.16	66	S		391.723
			S	391.849
			R	392.048
			V	392.354
			C	393.083
			P66	393.241
			OMIT66	393.247
			1466	393.249
			V	393.250
		S		393.723
			S	393.735
			C	393.474
			P66	394.584
			R	394.956
			V	395.263
		S		395.723
			S	395.738
			R	395.957
			V	396.279
			C	396.956
			P66	397.041
			R	397.371
		S		397.723
			V	397.749
			S	397.874
			R	398.375
			V	398.737
			C	399.143
			P66	399.242
			OMIT66	399.247
			V	399.249
		S		399.723
			S	399.739
			C	400.533
			P66	400.650
			R	401.03
			V	401.345

TLOSS	MODE	REQUEST	EVENT	TIME
.16	66	S		401.723
			S	401.742
			R	402.037
			V	402.346
			C	403.049
			P66	403.125
			R	403.479
		S		403.723
			V	403.834
			S	403.978
			R	404.478
			V	404.719
			C	405.185
			P66	405.266
			OMIT66	405.272
			V	405.274
		S		405.723
			S	405.735
			C	406.319
			P66	406.438
			R	406.776
			V	407.076
		S		407.723
			S	407.736
			R	407.779
			V	408.146
			C	408.757
			P66	408.830
			R	409.158
			V	409.515
		S		409.724
.14				410

TLOSS	MODE	REQUEST	EVENT	TIME
.12	66			430
			P66	451.169
			R	451.554
		S		451.723
			V	451.884
			S	452.049
			R	452.555
			V	452.859
			C	453.146
			P66	453.237
			OMIT66	453.243
			V	453.245
		S		453.723
			S	453.733
			C	454.473
			P66	454.572
			R	454.945
			V	455.246