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LVDC Preflight Program Descriptions

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PREFACE

The LVDC Preflight Program Descriptions manual provides a functional breakdown of the Preflight Program by routine and subroutine.

The document is effective for the Preflight program effectivities 512/513/206. All changes to the document will be incorporated by updating the existing descriptions and flowcharts.

Appendix B contains the Regular Status Codes, Special Status Codes, Vehicle Dependent Parameters, Linkages, Flags and Constants, and Preflight PIO Tags. These items are common to Saturn V, Saturn IB and Skylab I missions. Exceptions are noted.

Appendix C contains the status of the Discrete Input Register, Discrete Input Spares Register, and Interrupt Storage Register by program series.

SECTION 1

INTRODUCTION

The LVDC Preflight Program performs the following functions under control of the SLCC:

1. Load and/or verify the LVDC memory.
2. Exercise, monitor, and verify internal functions of the LVDC and LVDA.
3. Exercise and/or monitor selected Instrument Unit subsystems.
4. Participate in overall guidance and control system tests.
5. Perform limited data processing for the Launch Computer Complex.

These preflight routines are versatile and flexible in that they are adaptable to pre-launch conditions for the entire Saturn series of missions as presently conceived.

In conjunction with the launch computer, these routines provide the following subsystem checkout capabilities:

1. Operational checkout of the LVDC.
2. Operational checkout of the LVDA.
3. Operational checkout of the Switch Selector - LVDA Interface.
4. Operational checkout of the accelerometer and gimbal angle processing features.
5. Operational checkout of the vehicle discretes and interrupts.
6. Operational checkout of the LVDA-PCM Interface.

SECTION 2

GENERAL DESCRIPTION

In defining the preflight routines, certain assumptions have been made, and ground rules followed, concerning:

- The RCA-110A Communication Link.
- The prelaunch checkout philosophy.

Those aspects of the interface between the Launch Vehicle Data Adapter (LVDA) and the RCA-110A (and its ESE) which are utilized extensively by the preflight routines are illustrated in Figure 2-1. The interrupt line to the LVDA/LVDC from the ESE forces a program recycle in the LVDC. The interrupt for the LVDA/LVDC going to the ESE forces the RCA-110A to read the hardwired LVDA Telemetry Buffer Register. The interrupt is issued by the LVDC/LVDA whenever information is sent to the Telemetry Buffer Register. The SYNC signal to the LVDC serves two purposes:

- Notifies the LVDC that the launch computer is about to send information to the LVDC.
- Serves as a "data received" indication from the launch computer. The signal must be acknowledged before the LVDC continues on the next program function.

The SYNC Reset signal indicates to the launch computer that the LVDC has recognized the SYNC signal and is proceeding to honor it. The fourteen mode/data lines are used by the launch computer to load information (mode commands or data) into the LVDC. The 6 Mode Register lines indicate to the launch computer the routine currently executing in the LVDC. The hardwire lines are the means by which the LVDC/LVDA outputs data to the launch computer without requiring it to process PCM/DDAS data.

During preflight checkout the launch computer sequentially commands the LVDC into various routines; not more than one routine can be commanded at a time. During normal operation, when the LVDC is not executing a commanded routine, the preflight program is "idling" in a Self-Check loop in the Mode Sort Routine. In this routine the LVDC periodically searches for the Sync Signal. Upon receipt of the Sync Signal, the LVDC reads the mode/data lines and proceeds to execute the commanded routine. Upon entering the commanded routine, the Mode Register is loaded with the appropriate mode indication (refer to Appendix B) for ground display purposes. The same information which is loaded into the Mode Register is sent to the PCM/DDAS Assembly

and to the launch computer via the hardwires. The launch computer monitors this mode information to verify that the LVDC actually entered the commanded routine. When the mode is verified, the launch computer may provide data to the routine. The pertinent data from the commanded routines, if any, is then telemetered and the LVDC returns to its "idling" condition.

In order to insure that the launch computer recognizes each individual data transmission from the LVDC/LVDA to the ESE, the LVDC capability to interrupt the RCA-110A on level 4, line 7 is provided. The interrupt is energized by the LVDC immediately after each telemetry operation, except as noted below:

- Following the data transmitted during the Mode Sort Routine.
- Following the data transmitted during the Prepare to Launch Routine.
- Following the status code words of the Power Up and Initialize Routine.

Should the LVDC recognize an error condition, a special error status code is issued to the launch computer, and any error message associated with the error condition is telemetered. The LVDC then waits for the Sync Signal before continuing. After processing the error, the LVDC will continue the commanded routine or return to the Mode Sort Routine. In the event that the launch computer desires to terminate an LVDC routine prematurely, it can do so with an RCA-110A interrupt signal (INT 3) which forces a program recycle to Forced Begin Routine and then to Mode Sort.

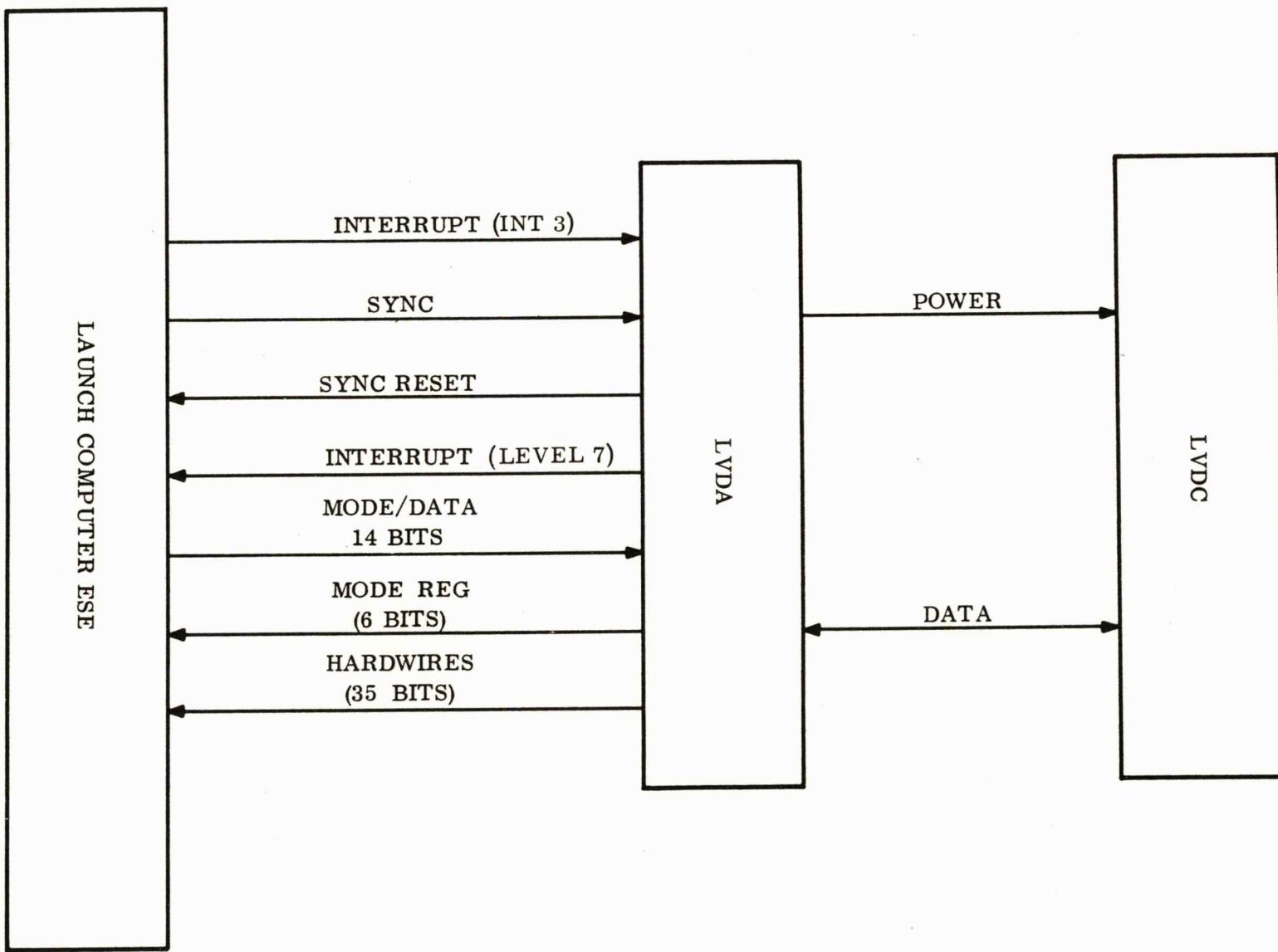


Figure 2-1. LVDA/RCA-110A Interface

SECTION 3

DETAILED DESCRIPTION

3.1 ROUTINES

3.1.1 Power Up Initialize Routine (Figure 3-1)

This routine performs the necessary initialization after power has been applied to the LVDA and LVDC. The routine is automatically entered upon the release of the Halt Signal and performs the following sequence of operations:

1. Perform a divide to block any initial interrupt from being honored.
2. Test a program indicator to determine if Power Up was entered from the Orbital phase of the Flight Program.
 - a. If not, proceed to step 3.
 - b. Test the RCA Register and Discrete Input Register to determine if Special Loader has been commanded.
 - (1) If not, the program waits until Halt is set and released.
 - (2) If so, perform another divide to block any initial interrupt from being honored.
3. Reset all Initial Interrupts.
4. Inhibit all interrupts.
5. After enabling Ground Computer Control, place the COD/PS error word in the DOM while a channel is available.
6. Test a program indicator to determine if Power Up was entered from the Orbital phase of the Flight Program.
 - a. If it was, proceed to step 7.
 - b. Test a program indicator to determine if Halt had been issued while executing the Memory Error Test Routine.

- (1) If not, proceed to step 7.
 - (2) Restore Memory Error Test memory locations.
7. Inhibit all interrupts except TLC.
 8. Test the RCA Register and the Discrete Input Register to determine if the Special Loader has been commanded.
 - a. If not, proceed to step 9.
 - b. Execute the Register Initialize Subroutine, and exit to Special Loader.
 9. Initialize proper data sector selection.
 10. Telemeter status code 40 and load the Mode Register with 40.
 11. Execute the Register Initialize Subroutine.
 12. Initialize the "interrupt HOP 400" address in every module present.
 13. Execute Dummy EMR read to discard initial bits in the Error Monitor Register.
 14. Inhibit all interrupts, using the Inhibit Register, except TLC and RCA-110A.
 15. Initialize all necessary program constants.
 16. Exit to Forced Begin Routine.

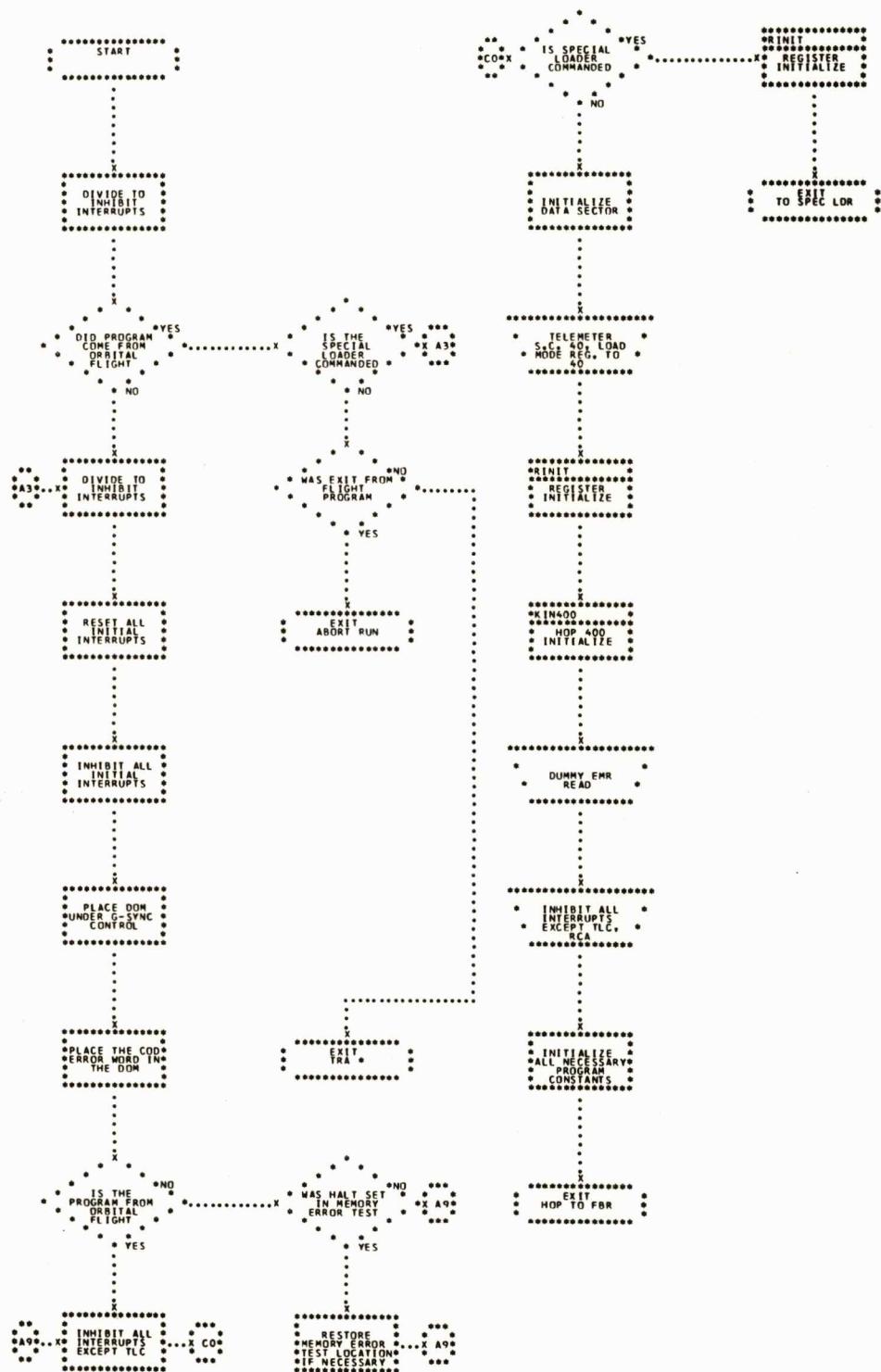


Figure 3-1. Power Up Initialize Routine

3.1.2 Forced Begin and Initialize Routine (Figure 3-2)

The purpose of this routine is to initialize certain program constants and LVDA registers prior to executing any preflight routine. This routine shall be entered only from the Power Up Routine, or as the result of an RCA-110A interrupt. This interrupt is used when the launch computer terminates an LVDC routine prior to completion, or re-initializes program constants and certain LVDA registers. The following sequence of operations is performed:

1. Read Error Monitor Register (EMR); mask disagreement detectors EM 8, EM 3, and two spare bits if entered by the RCA-110A interrupt. If the normal Power Up entry is used, read and save raw EMR.
2. Execute HOP 400 Initialize Subroutine.
3. Set ICRs 1 and 9 (block "T" SYNC and reset OCRB).
4. Reset all ICRs except 1 and 9.
5. Issue the Forced Begin status code (265252260).
6. HOP to the Register Initialize Subroutine.
7. Initialize EMCON.
8. Test GCO Test indicator to determine if the RCA-110A is checking the Telemetry Buffer lines.
 - a. If not, proceed to set 9.
 - b. Test GCO Test indicator to determine if the RCA-110A desires a 512525510 pattern.
 - c. If not, proceed to step 11.
 - d. If the desired pattern is 512525510, proceed to step 10c.
9. Issue a dummy Group 5 PIO to stop the COD counters.
10. Check the saved EMR reading from step 1.
 - a. If an error exists, load a special status code into the Mode Register and telemeter the contents of the EMR. Both of the above outputs will

be done with an interrupt being set to the launch computer. Proceed to step 10c.

- b. If no error exists, proceed to step 9.
 - c. Issue special status code, set Mode Register, and issue interrupt to launch computer.
11. Wait for a Sync signal from the launch computer.
 12. When the Sync signal is detected, reset it.
 13. Reset the RCA-110A interrupt. This is done in the event that this routine was entered via an RCA-110A interrupt.
 14. Exit to the Mode Sort Routine.

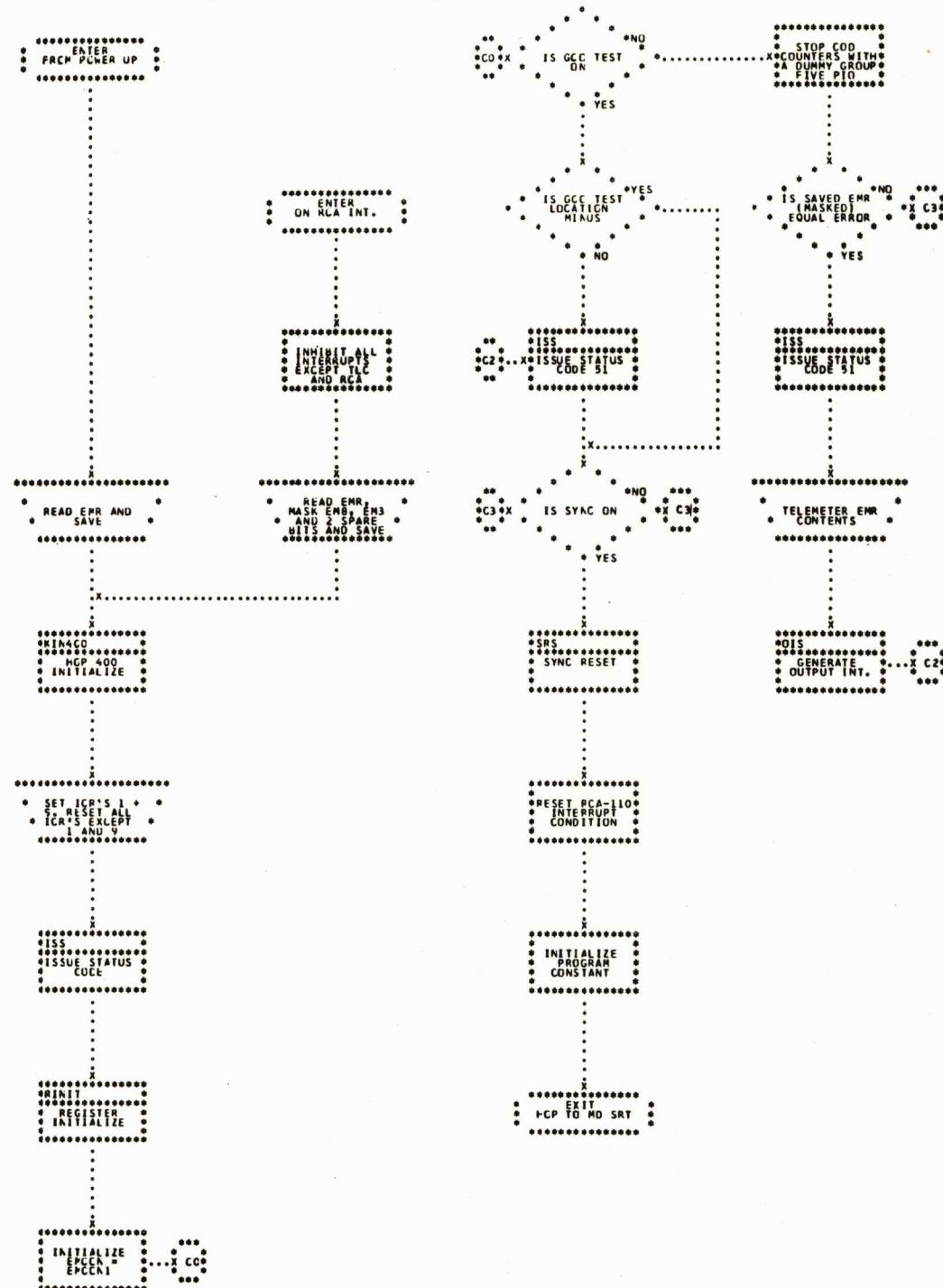


Figure 3-2. Forced Begin and Initialize Routine

3.1.3 Mode Sort Routine (Figure 3-3)

The purpose of this routine is to accept an input word from the launch computer and interpret it as a mode command. This routine shall be entered directly from the Forced Begin Routine and all other routines shall automatically exit to this routine upon their completion.

Once the Mode Sort Loop has been entered and the Sync signal is recognized, the LVDC shall read the fourteen (14) bit RCA 110A input word. It shall then issue Sync Reset, wait for Sync to go off, then reset the Sync Reset signal.

The LVDC shall then examine the Mode/Data bit of the fourteen (14) bit input word which must indicate mode information. It shall then HOP to the commanded routine specified by the mode bits of the RCA input word. If the Mode/Data bit indicates data information, the LVDC shall indicate an error condition by loading the special status code in the Mode Register. It shall then exit to the Error Monitor Subroutine from which it will return to the beginning of this routine.

When no Sync signal is present this routine shall continuously cycle through a self-check loop which shall include the LVDC Self Test Subroutine, LVDA Timing and Counter Test Subroutine, the Error Monitor Subroutine, and the Accelerometer Monitor Subroutine.

During each loop of the Mode Sort Routine (206 and Subs and 513 and Subs), data is telemetered from: Discrete Input Register, Discrete Input Spares Register, Interrupt Storage Register, Downrange Accelerometer, Crossrange Accelerometer, and Vertical Accelerometer. The Telemetry PIO codes are indicated in Appendix B. Accelerometer off level indications are telemetered for all vehicles.

The RCA-110A Input Word format required by this routine is shown below.

Mode Word format for S 1 2 3 4 5 6 7 8 9 10 11 12 13

Pre-flight Operation: $\frac{M}{D} \quad 0 \quad M \quad M \quad M \quad M \quad M \quad M \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0$

$\frac{M}{D}$ MODE/DATA Bit

M Mode Information

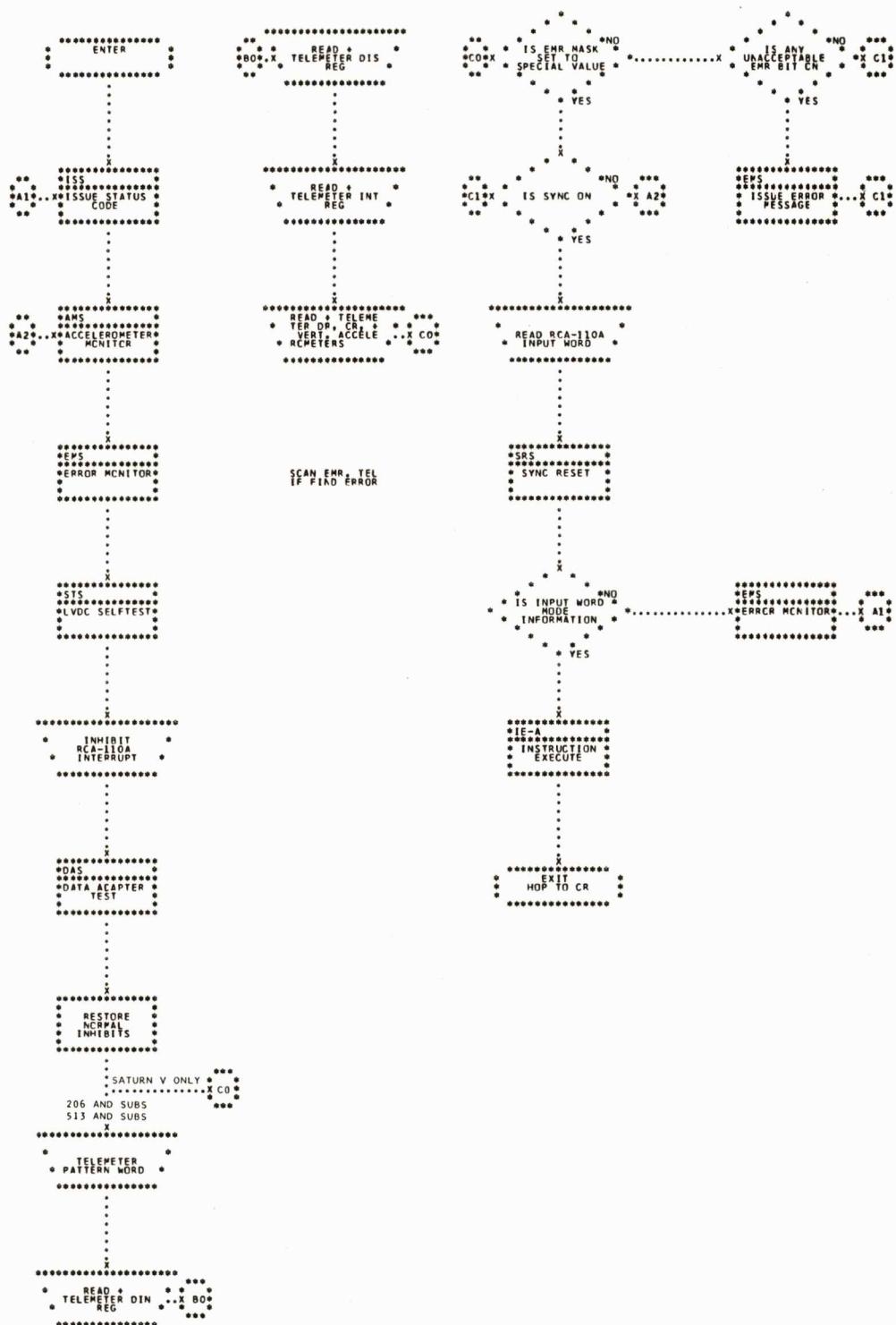


Figure 3-3. Mode Sort Routine

3.1.4 Verify and Prepare to Load Routine (Figure 3-4)

This routine has two distinct modes. The purpose of Mode 1 (Verify) is to allow the launch computer to examine the contents of any LVDC memory location.

Mode 1 (Verify) requires the launch computer to load two words for each memory location to be verified:

	S	1	2	3	4	5	6	7	8	9	10	11	12	13
Word 1	<u>M</u> D	S	S	S	S	M	M	M	D	D	D	D	O	O
Word 2	<u>M</u> D	W	W	W	W	W	W	W	W	L	V	<u>S</u> D	0	1

M
D Mode/Data Bit

S Sector Bit

M Module Bit

D Data Bit (These bits are used only during Prepare to Load Mode).

W Word Address Bit

L 0-last group of RCA words has not been read into LVDC.
1-last group of RCA words has been read into LVDC.

V 0-Prepare to Load Mode
1-Verify only Mode

S
D Set equal 0 for a verify
Set equal to 0 to 1 for prepare to load depending upon whether a simplex or duplex load is desired.

Bits 12, 13 - Character counters

The LVDC decodes these two words to form a control word made up of a CDS instruction and a CLA instruction. The control word is used to extract the desired data word from the specified location. Both the LVDC data word and the control word are then stored in a sequential table in temporary storage. When all groups of two input words have been accepted by the LVDC and the corresponding control and data words have

been stored (i.e., when the L bit is a 1), both the control and the corresponding data words are telemetered to the launch computer. The LVDC then returns to the Mode Sort Routine or the Prepare to Launch Routine, depending upon the origin of the Mode Command.

Mode 2 (Prepare to Load) requires the RCA-110A to supply four input words for each LVDC memory location which it wishes to load. The format of the four words required is shown as follows:

	S	1	2	3	4	5	6	7	8	9	10	11	12	13
Word 1	<u>M</u> D	S	S	S	S	M	M	M	D	D	D	D	0	0
Word 2	<u>M</u> D	W	W	W	W	W	W	W	W	L	V	<u>S</u> D	0	1
Word 3	<u>M</u> D	D	D	D	D	D	D	D	D	D	D	D	1	0
Word 4	<u>M</u> D	D	D	D	D	D	D	D	D	D	D	D	1	1

The LVDC decodes these four words to form a program-built control word made up of a CDS instruction and a STO instruction, and a data word 26 bits in length. The control word and data word are stored sequentially in temporary storage. When all groups of four input words have been read by the LVDC (i.e., when the L bit is a 1), and the corresponding control and data words stored, both the control words and the data words are telemetered to the launch computer. The LVDC then returns to the Mode Sort Routine or the Prepare to Launch Routine, depending upon the origin of the Mode Command. The data assembled in this routine remains in temporary storage until the launch computer verifies that the proper loading instructions and corresponding data words have been assembled, at which time the Load Routine is commanded.

For either mode, the TLC interrupt is inhibited during execution. After each LVDC memory location is accessed, the EMR is checked for TLC, EAM, and EBM errors. Upon occurrence of any of these bits in the EMR, an error message and EMR contents are telemetered by the Error Monitor Subroutine.

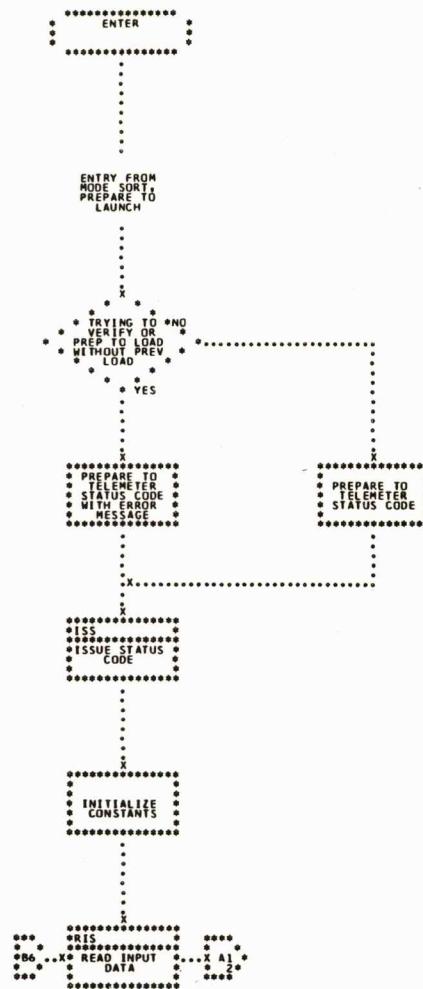


Figure 3-4. (Sheet 1 of 3) Verify and Prepare to Load Routine

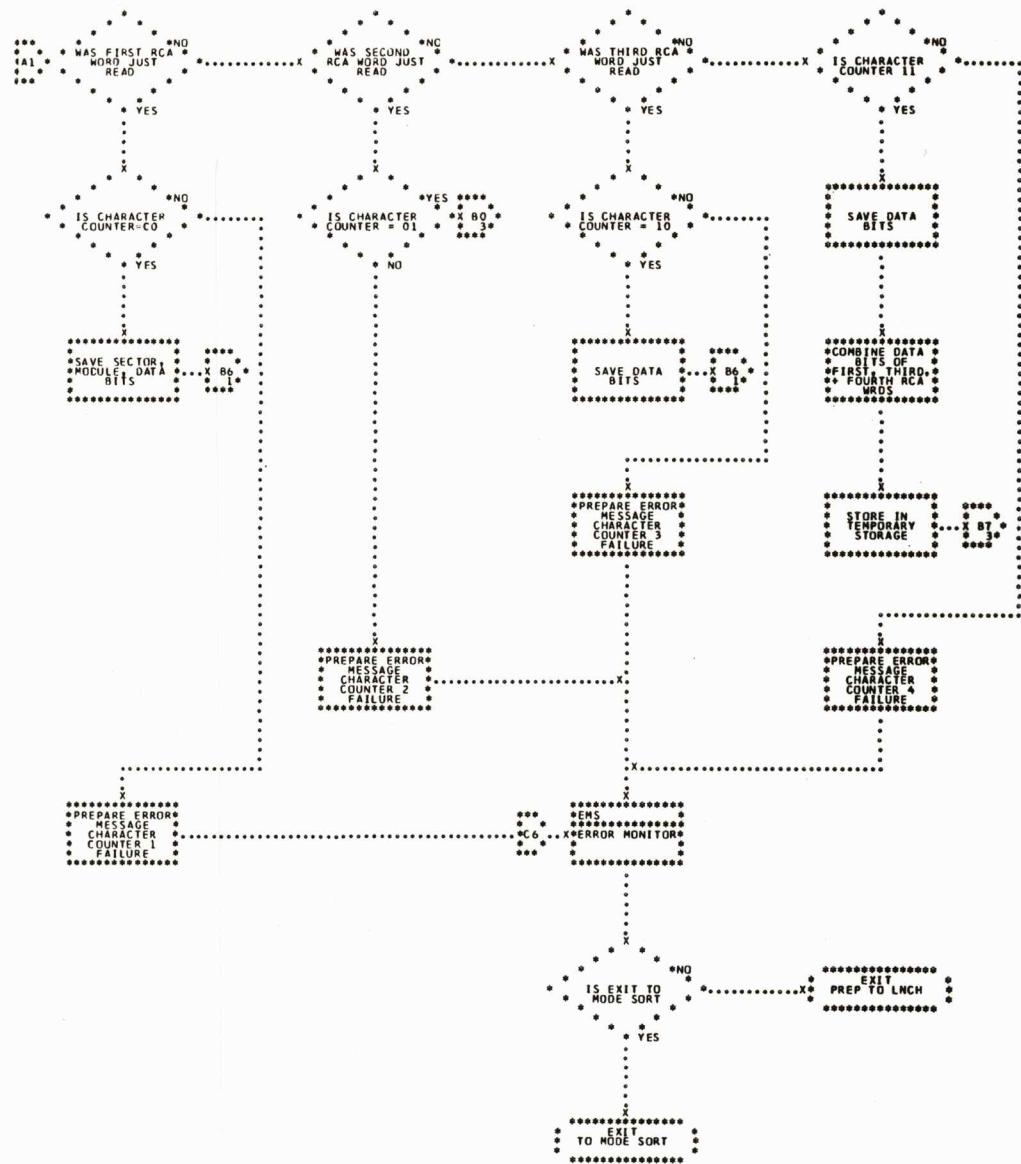


Figure 3-4. (Sheet 2 of 3) Verify and Prepare to Load Routine

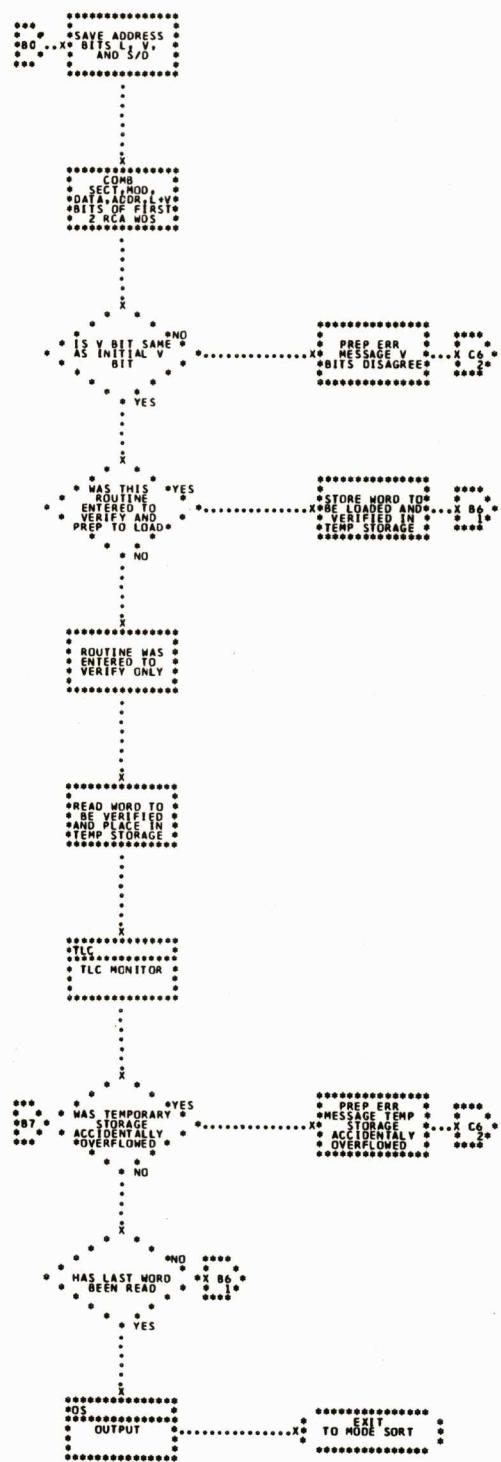


Figure 3-4. (Sheet 3 of 3) Verify and Prepare to Load Routine

3.1.5 Load Routine (Figure 3-5)

This routine allows the information previously placed in temporary storage by the Verify and Prepare to Load Routine to be transferred to the permanent memory locations specified. Upon entering this routine, the LVDC verifies that the Prepare to Load Routine has been executed to be sure that the temporary storage block contains valid information. If a Prepare to Load has been executed, a test is made to determine if this routine was commanded from Prepare to Launch. If it was, the contents of the temporary storage block are checked to insure the data is loaded into a special parameter block of 16 locations. A coded error message is issued if any of the data is loaded outside this block. If all conditions have been satisfied, the contents of the temporary storage block are transferred to the specified locations utilizing the program-built control words. If Prepare to Load Routine has not been executed, the LVDC issues a coded error message and returns to the Mode Sort Routine or the Prepare to Launch Routine, depending upon the origin of the mode command.

Figure 3-5. Load Routine

3.1.6 Sector Sumcheck Routine (Figure 3-6)

The purpose of this routine is to allow the RCA-110A launch computer to verify that the instructions and/or data (constants) stored in a given sector have not been affected by LVDC operations. One input word is required from the launch computer specifying the module and the sectors within it that are to be sumchecked. This word specifies the starting and ending sectors, and the routine sequentially sumchecks all sectors between the two. The input word format is:

S	1	2	3	4	5	6	7	8	9	10	11	12	13
<u>M</u>	S _E	S _E	S _E	S _E	S _S	S _S	S _S	S _S	M	M	M	0	0
<u>D</u>													

M Mode/Data Bit
D

S_E Sector End Bits (last sector to be sumchecked)

S_S Sector Start Bits (first sector to be sumchecked)

M Module (module containing sectors to be sumchecked)

The TLC interrupt is inhibited during execution of the routine. After each LVDC memory location is accessed, the EMR is checked for TLC, EAM, and EBM errors. If an error bit is found, an error message and EMR contents are telemetered to the launch computer by the Error Monitor Subroutine.

This routine selects the specified module by forcing simplex data module operation. It is the responsibility of the launch computer to command a sumcheck of both modules (and the specified sectors within) of a duplexed pair. The routine sums the memory words in the starting sector and saves the value. The routine performs the same operation in the next sequential sector until all requested sectors have been summed. The Output Subroutine is entered and two words are telemetered for each requested sector. The words indicate:

- The sector that has been sumchecked.
- The sumcheck value.

The routine then exits to Mode Sort.

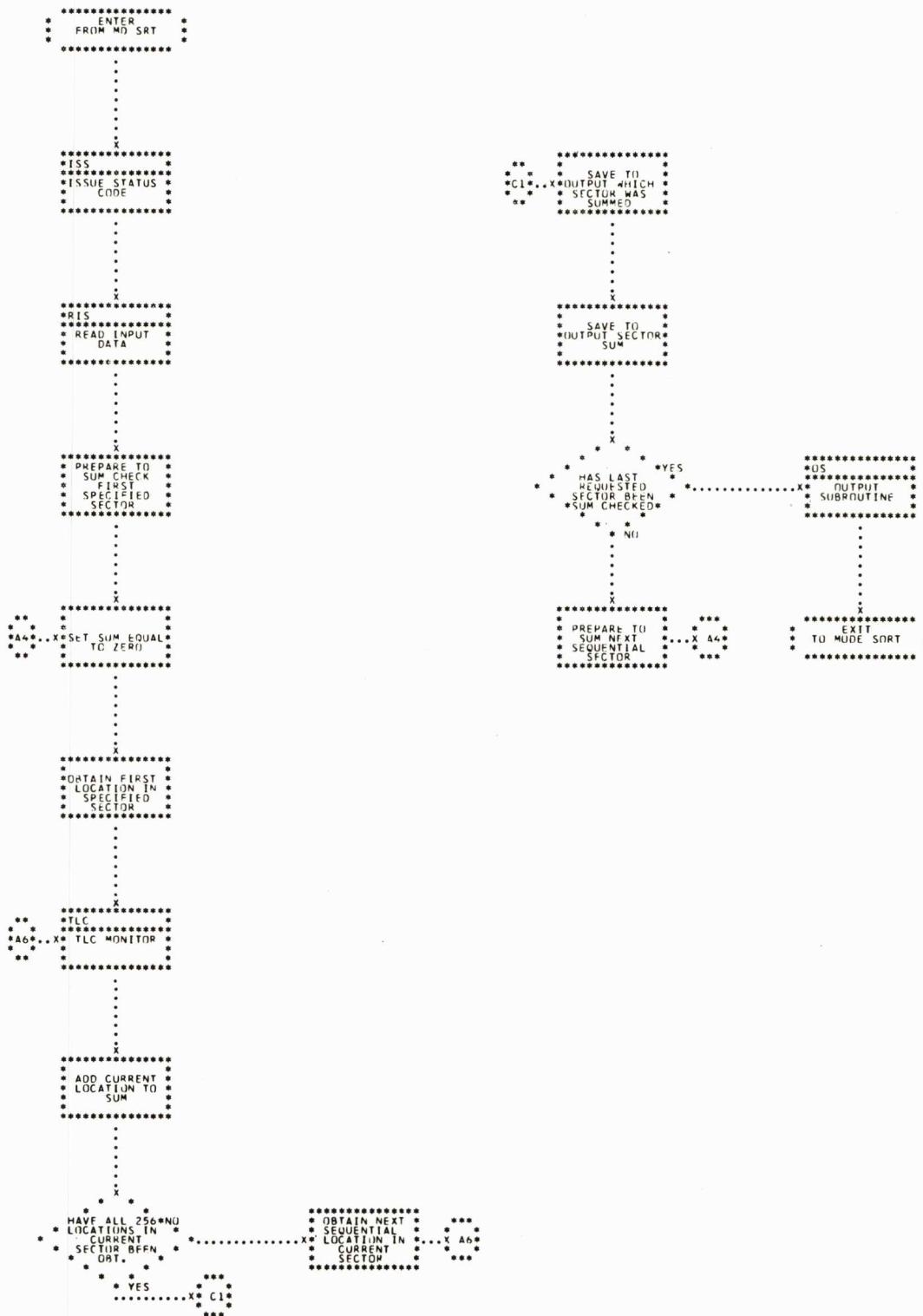


Figure 3-6. Sector Sumcheck Routine

3.1.7 Sector Dump Routine (Figure 3-7)

The purpose of this routine is to allow the RCA-110A launch computer to verify that all 256 locations within a given sector contain the correct instructions and/or data. One input word is required from the RCA-110A specifying a module and the sequential sectors within that module which are to be dumped.

The input word format is:

S	1	2	3	4	5	6	7	8	9	10	11	12	13
$\frac{M}{D}$	S_E	S_E	S_E	S_E	S_S	S_S	S_S	S_S	M	M	M	0	0
Mode/Data													
$\frac{D}{M}$													
S_E Sector End (last sector to be dumped)													
S_S Sector Start (first sector to be dumped)													
M Module (module containing sectors to be dumped)													

The TLC interrupt will be inhibited during execution of the Routine. After each LVDC memory location is accessed, the EMR is checked for TLC, EAM, and EBM errors. If an error bit is found, an error message and EMR contents are telemetered to the launch computer by the Error Monitor Subroutine.

The routine telemeters the sector locations sequentially, in 32 groups, 8 groups per sector, and then performs the same operation on the next sector if it is to be dumped. The LVDC does no verification of its own in this routine.

The telemetry output contains 5 bits which are used as Telemetry Counter Bits. These bits (A3 to A7 of the telemetry PIO Instruction) cycle from 31 to 0, eight times per second. Upon completion of the required dumps, the LVDC returns to the Mode Sort Routine

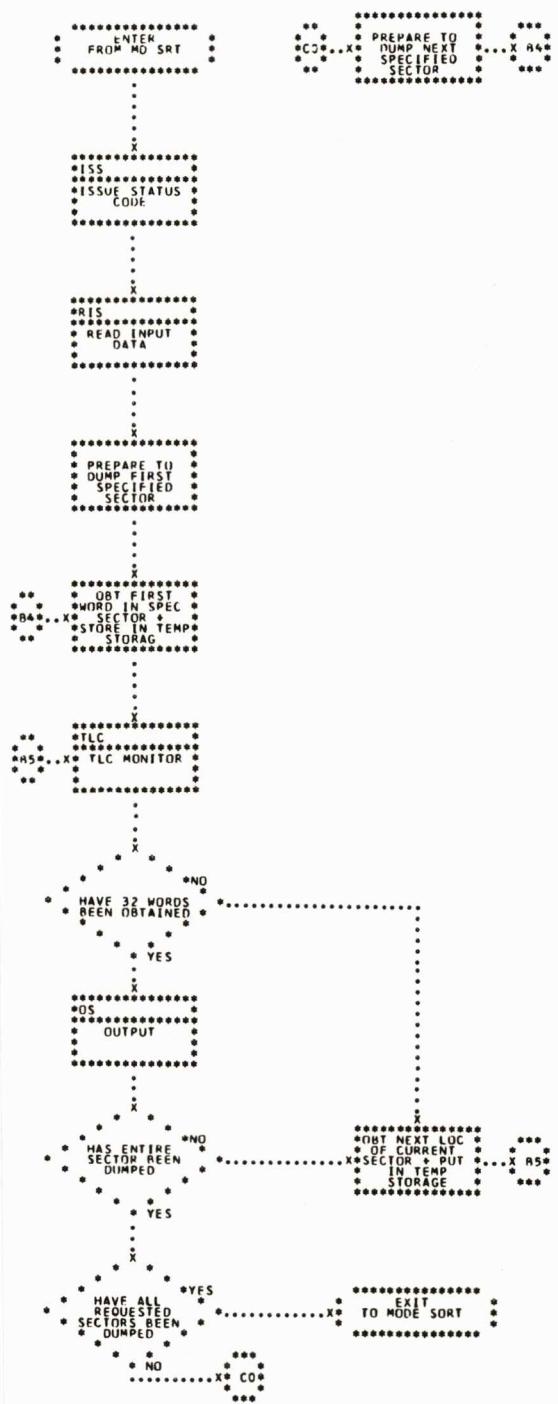


Figure 3-7. Sector Dump Routine

3.1.8 Gimbal Angle Monitor Routine (Figure 3-8)

The purpose of this routine is to accurately read platform attitude utilizing the multi-speed resolvers and the LVDC analog to digital converters.

The routine can be entered from Mode Sort or as a subroutine entry from Prepare to Launch. Both entries require one input data word, the format of which is shown below:

S	1	2	3	4	5	6	7	8	9	10	11	12	13
---	---	---	---	---	---	---	---	---	---	----	----	----	----

$\frac{M}{D}$	Y	C ₁	C ₂	C ₃	F ₁	F ₂	F ₃	B ₁	B ₂	B ₃	1	0	0
---------------	---	----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------	---	---	---

$\frac{M}{D}$ Mode/Data Bit

Y 1-Read resolvers; 0 - Read and correct resolver values

C Coarse gimbal angles 1, 2, 3

F Fine gimbal angles 1, 2, 3

B Backup gimbal angles 1, 2, 3

This routine reads the specified resolvers sequentially, makes the necessary correction (if requested) to both duplexed counter values, and at the end of the routine, telemeters the uncorrected counter readings and both corrected values to the launch computer. The uncorrected readings contain the status of the disagreement bit.

If the disagreement bit is detected On upon entry from Mode Sort and was not caused by the COD counters passing through zero, the Resolver Error Subroutine is entered to isolate the error source. The result of the Resolver Error Subroutine is used as the error message input word for the Error Monitor Subroutine. The Error Monitor Subroutine telemeters both the error message and the contents of the Error Monitor Register and then waits for the occurrence of Sync. Upon receiving a Sync signal, the subroutine returns to the Gimbal Angle Monitor Routine, which telemeters the accumulated output data, and then returns control to the Mode Sort Routine.

If the disagreement bit is detected On upon entry from Prepare To Launch, a maximum of two consecutive gimbal reads are performed to insure that a transient condition has not occurred. If the disagreement bit remains On for all three reads, the Resolver Error Subroutine is entered and the results are used as input to the Error Monitor Subroutine. The Error Monitor Subroutine telemeters the error message, the EMR, and sets DO 13 (Firing Commit Inhibit).

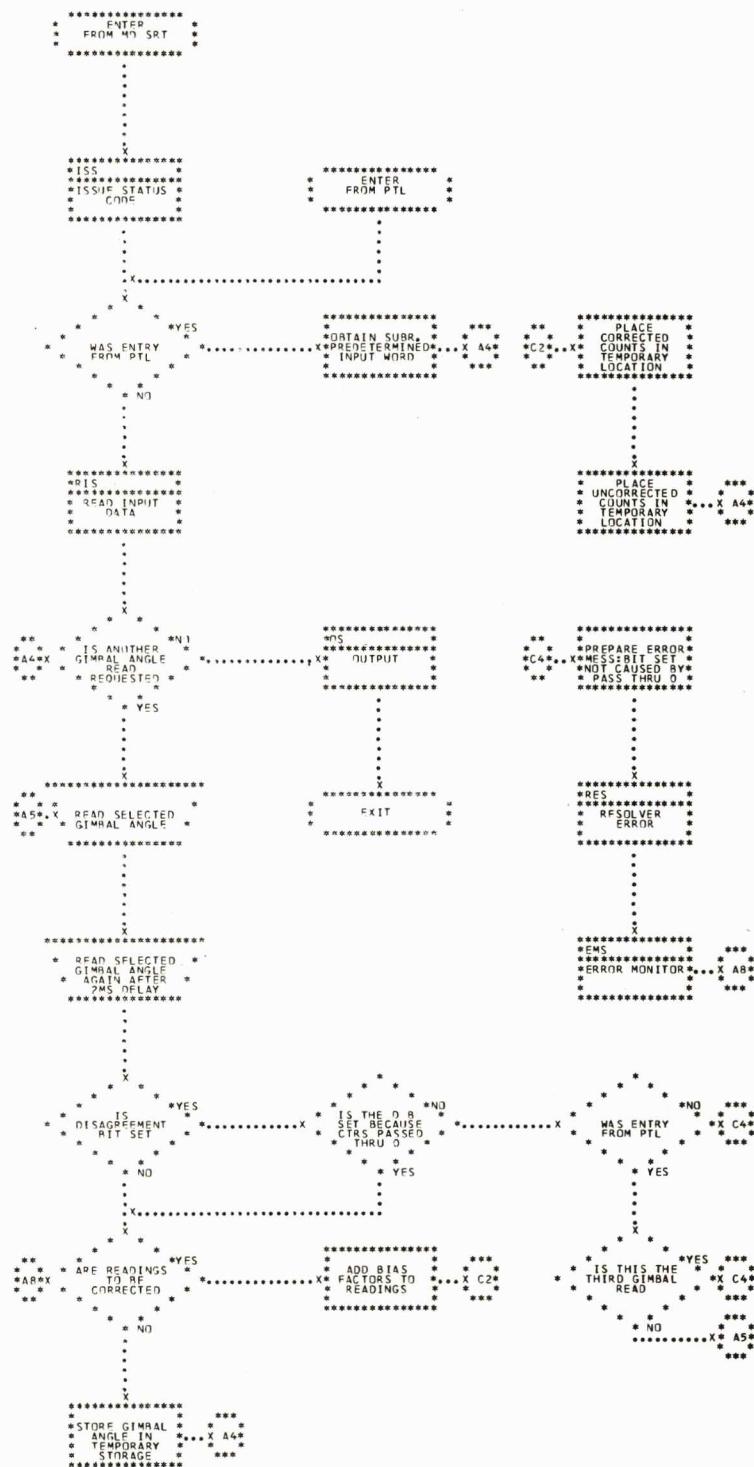


Figure 3-8. Gimbal Angle Routine

3.1.9 Accelerometer Pulse Count Routine (Figure 3-9)

It is the purpose of this routine to simultaneously accumulate accelerometer data on all three platform axes to verify that the LVDC/LVDA can properly sense coordinate velocity changes. The routine also provides data to the launch computer while serving in the capacity of platform monitor.

This routine requires three data input words from the launch computer.

	S	1	2	3	4	5	6	7	8	9	10	11	12	13
Word 1	0	N	N	0	0	A	A	B	B	C	C	S	0	0
Word 2	0	D ₁₃	D ₁₄	D ₁₅	D ₁₆	D ₁₇	D ₁₈	D ₁₉	D ₂₀	D ₂₁	D ₂₂	D ₂₃	D ₂₄	D ₂₅
Word 3	0	D _S	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂

Where: S = 0, Time interval referenced to syllable 0 accumulations.

S = 1, Time interval referenced to syllable 1 accumulations.

AA = First Accelerometer to be interrogated.

BB = Second Accelerometer to be interrogated.

CC = Third Accelerometer to be interrogated.

NN = 1, the delta-count specified applies to the first accelerometer specified and the corresponding time accumulation is accurate to 410 microseconds. The second and third accelerometer pulse accumulations are not started or stopped on cross-over occurrences; thus, they represent gross accumulations on their respective axes during the time interval that the specified count is accumulated on the first axis.

NN = 2, the delta-count applies to the second accelerometer specified. The first and second accumulations are accurate to 410 microseconds - the third is only a gross accumulation.

NN = 3, the delta-count applies to the third accelerometer specified. All three time accumulations are accurate to 410 microseconds.

D = Sign through Bit 25 are the delta-count bits.

If, for example, three axes are specified ($NN = 3$) , all three accumulations are started sequentially on cross-over occurrences. When the specified number of pulses have been accumulated on the third axis, that accumulation stops on the next velocity change detected (or as near to it as possible) , and the first and second accumulations are stopped sequentially on velocity change occurrences.

Therefore, in all cases there is an accumulated velocity change and corresponding time interval for each axis. When the accumulations are completed the LVDC teleimeters the Syllable 1 and Syllable 0 values, and the associated delta-time values. The time values are referenced to the syllable accumulation specified in the first input data word.

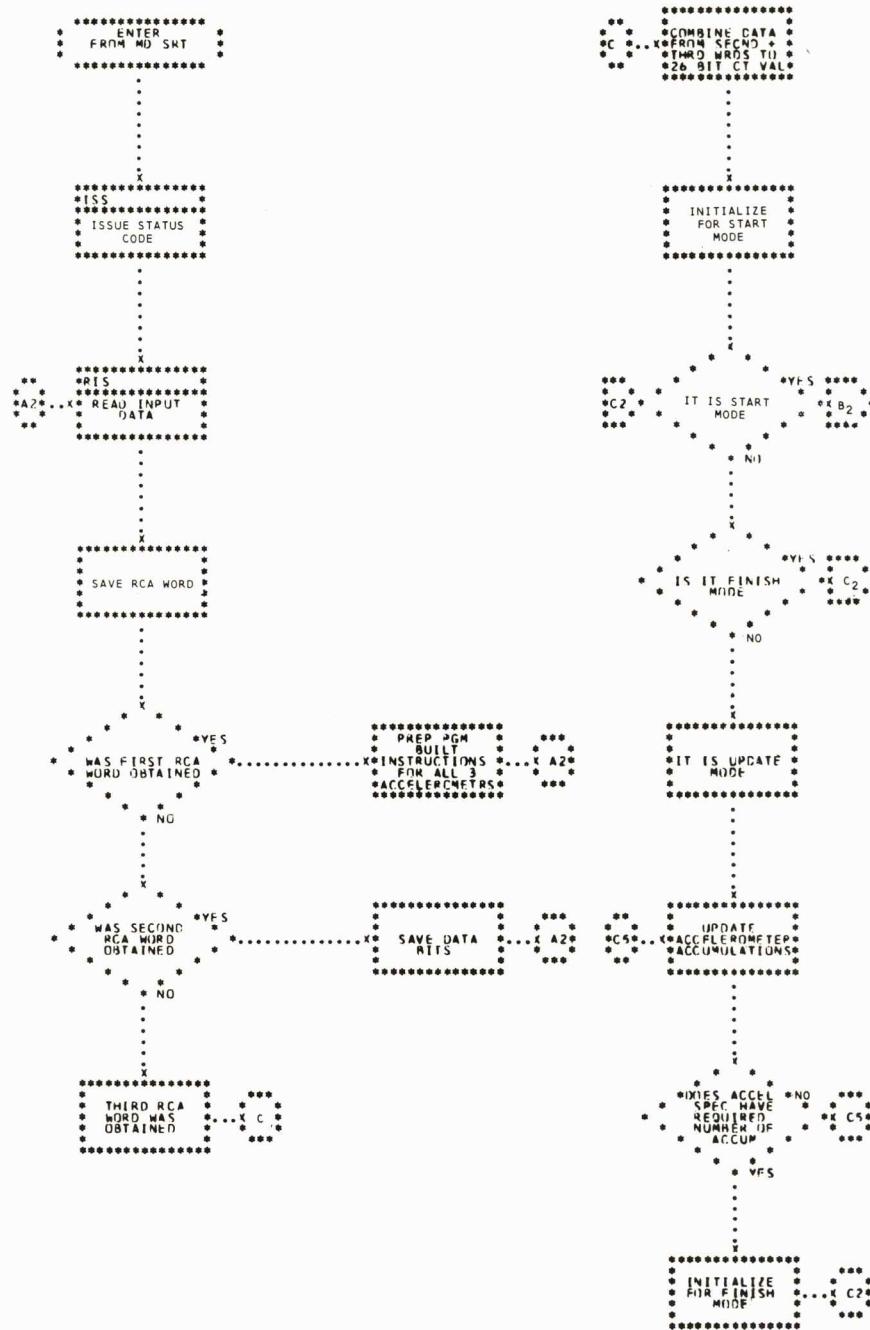


Figure 3-9. (Sheet 1 of 2) Accelerometer Pulse Count Routine

```
***** START *****  
R * X ACCELEROMETER  
* IN A  
CROSSOVER  
***** STOP *****  
C * X ACCELEROMETER  
* SPECIFIED TO  
START ON  
CROSSOVER  
  
***** START THE *****  
* OTHER TWO *  
* SEQUENTIALLY *  
* AFTER HF *  
* FIRST *  
***** PUT TIME INCH *****  
* X VEL CHNG *  
* FOR ALL 3 *  
* AXES & U TEMP *  
* X STR *  
***** INITIALIZE *****  
* OS *****  
* FOR UPDATE * C2 *  
* MODE *  
***** OUTPUT *****  
***** EXIT *****  
* X TO PRINT SORT *  
*****
```

Figure 3-9. (Sheet 2 of 2) Accelerometer Pulse Count Routine

3.1.10 Switch Selector Routine (Figure 3-10)

The purpose of this routine is to provide the capability of exercising the vehicle Switch Selector Drivers in the LVDA. The Switch Selectors are capable of being operated by the LVDC/LVDA, the Launch Computer, and a Manual Exerciser; thus, the LVDC must be prohibited from using any routine during preflight checkout that would exercise any Switch Selector independent of launch computer control.

This routine requires two data words from the launch computer; the first word specifies the switch selector and address to be used, and the second word specifies four status bits. The first status bit indicates whether the CIU is operational or not; if not, the CIU checks within this routine are bypassed. The second status bit indicates whether the Switch Selector specified is active or not. If not, the feedback is expected to be zero. The third and fourth status bits indicate desired channel. Switch selector read status is indicated by the Z bit. The RCA-110A input word formats are:

	S	1	2	3	4	5	6	7	8	9	10	11	12	13
Word 1	$\frac{M}{D}$	S	S	S	S	A	A	A	A	A	A	A	A	A
Word 2	$\frac{M}{D}$	X	Y	C	Z	0	0	0	0	0	0	0	0	0

Where: $\frac{M}{D}$ = Mode/Data

X = 1 - CIU is connected
= 0 - CIU is not connected

Y = 1 - Switch Selector present
= 0 - Switch Selector not present

C = 1 - Use Channel A
= 0 - Use Channel B

Z = 1 - Issue a Read Command
= 0 - Do not issue a Read Command

S = Stage Select Bits

A = Address Select Bits

This routine tests the stage select bits of the input data word to insure that the routine is not being requested to exercise more than two switch selectors at one time. The routine verifies that all switch selectors are in a reset condition before addressing any

of them. The verification is done by reading the feedback bits directly, and then through the CIU (if present); and by reading the stage select bits, the read bit, and the reset bit through the CIU (if present).

All readings must be zero to verify a reset condition; otherwise, the routine shall indicate an error condition (with an error message), by means of the Error Monitor Subroutine, in which case the input data word, the direct feedback data, and CIU data shall be telemetered, and the LVDC shall return to the Mode Sort Routine.

If the above tests are passed, the routine shall then issue the requested address to the proper switch selector and then delay for 20 milliseconds. The routine will then verify the switch selector feedback directly and through the CIU, if present.

After passing (or bypassing) the above test, the routine will reset the address and stage selects, and set the read command. The read command will be held on for 28 ms. then verified through the CIU, if present. The read command shall then be reset and the switch selector reset command issued. The reset command will be held on for 15 ms. and then reset after being verified through the CIU.

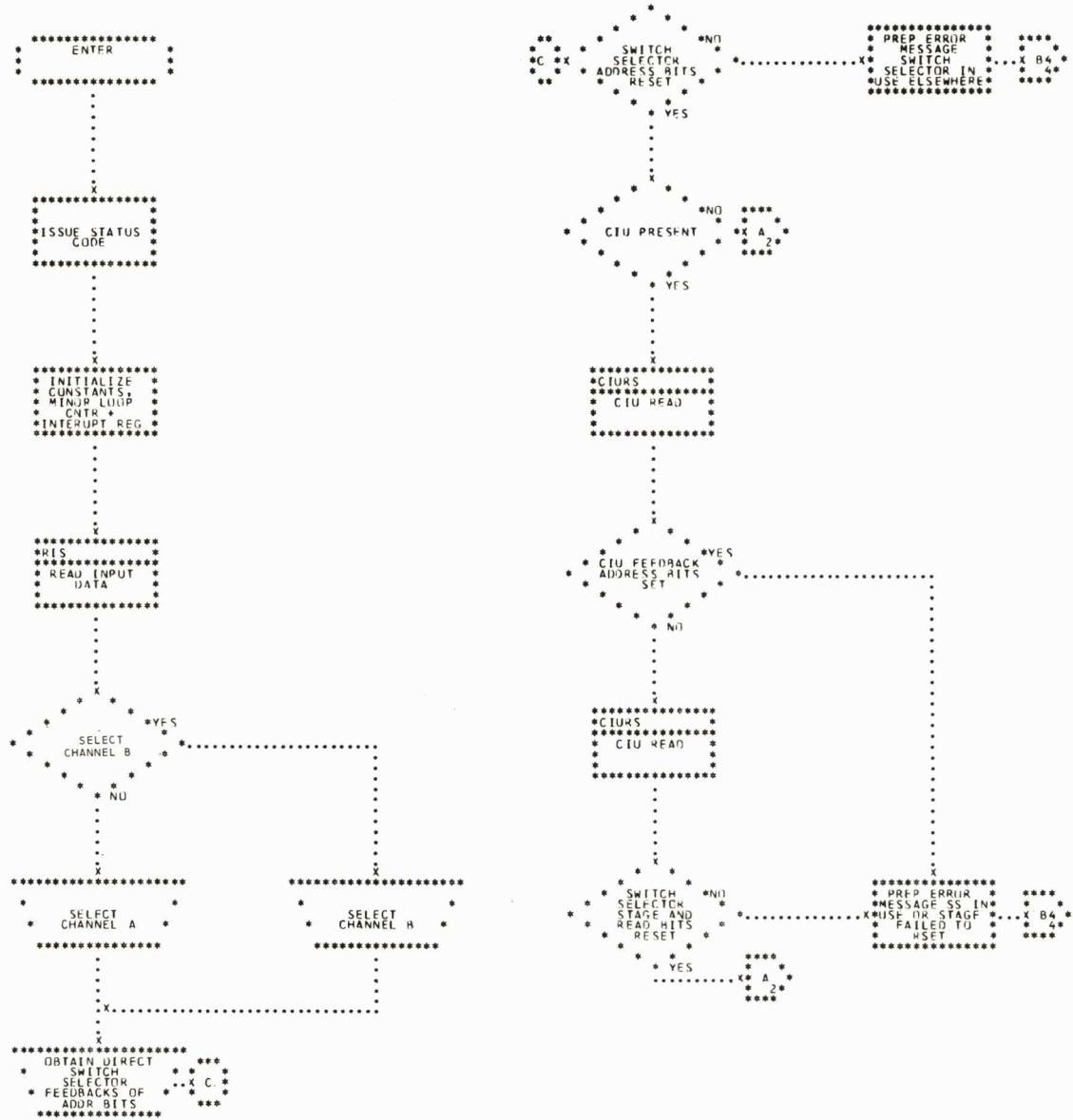


Figure 3-10. (Sheet 1 of 4) Switch Selector Routine

Figure 3-10. (Sheet 2 of 4) Switch Selector Routine

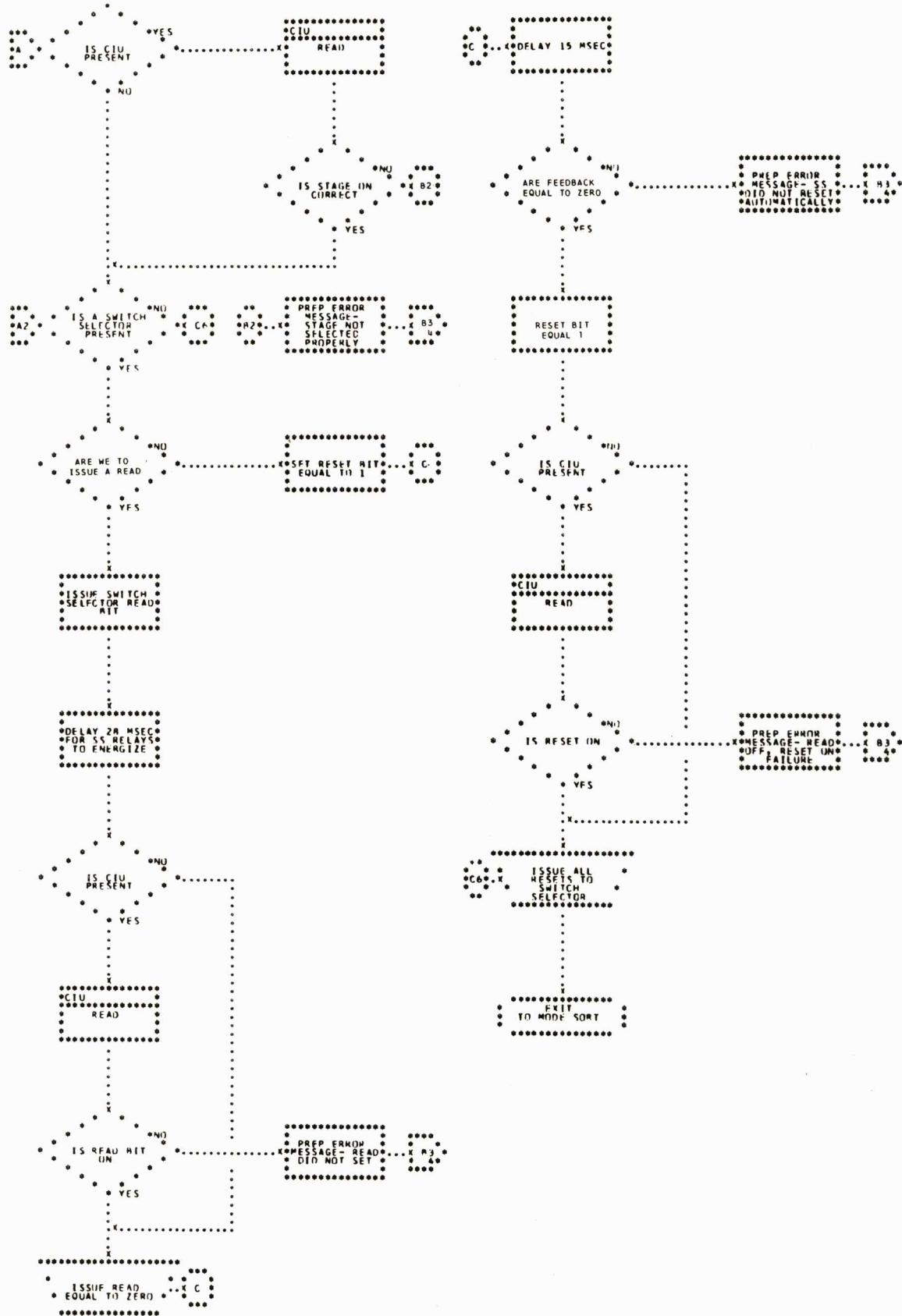


Figure 3-10. (Sheet 3 of 4) Switch Selector Routine

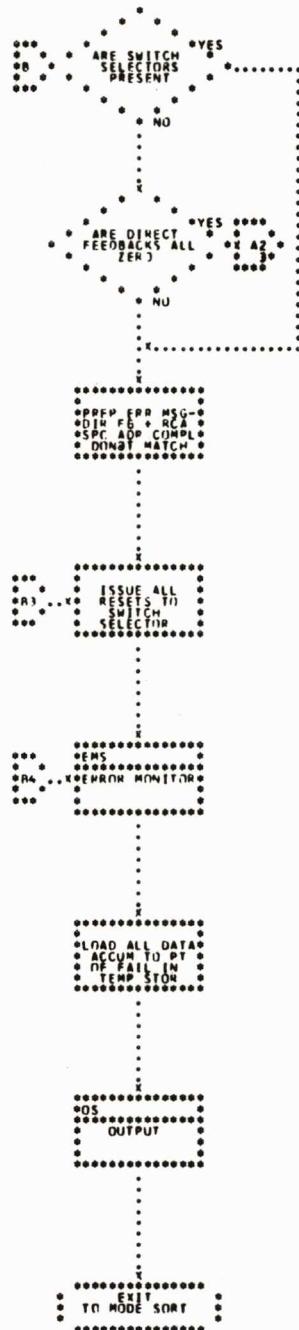


Figure 3-10. (Sheet 4 of 4) Switch Selector Routine

3.1.11 CIU Read Routine (Figure 3-11)

The purpose of this routine is to provide the launch computer with a means to verify LVDA Computer Interface Unit (CIU) operation and to provide the launch computer with an additional means of securing DDAS information. The routine is also used to obtain DDAS feedback data for the Switch Selector Routine.

The routine requires one input data word having the format shown:

S	1	2	3	4	5	6	7	8	9	10	11	12	13
<u>M</u>	A	A	A	A	A	A	A	A	A	A	A	A	0
D													

$\frac{M}{D}$ Mode/Data Bit

A CIU Telemetry Scan address of parameter to be sampled.

If this program is called by the launch computer, the input word will be furnished by that computer. When the Switch Selector Routine calls the CIU Read Routine, the CIU address bits are supplied as an input parameter.

This routine resets the CIU interrupt inhibit, and then sends the twelve bit address and data request bit to the CIU. The routine then waits 260 ms. or until the CIU interrupt is received. When the interrupt occurs, the routine reads the requested data from the Digital Input Multiplexer. If this routine was entered as a subroutine the LVDC returns control to the Switch Selector Routine. If this routine was commanded from the launch computer the LVDC exists to the Output Subroutine to telemeter the required data and then returns to the Mode Sort Routine. If the CIU interrupt does not occur, the routine transfers to the Error Monitor Subroutine with an error message. Upon leaving the Error Monitor Subroutine a decision is made concerning the mode of entry into the CIU Read Routine. If entry was made from the Switch Selector Routine, the Switch Selectors are reset and the LVDC returns to the Mode Sort Routine. If the entry was commanded the routine returns immediately to the Mode Sort Routine.

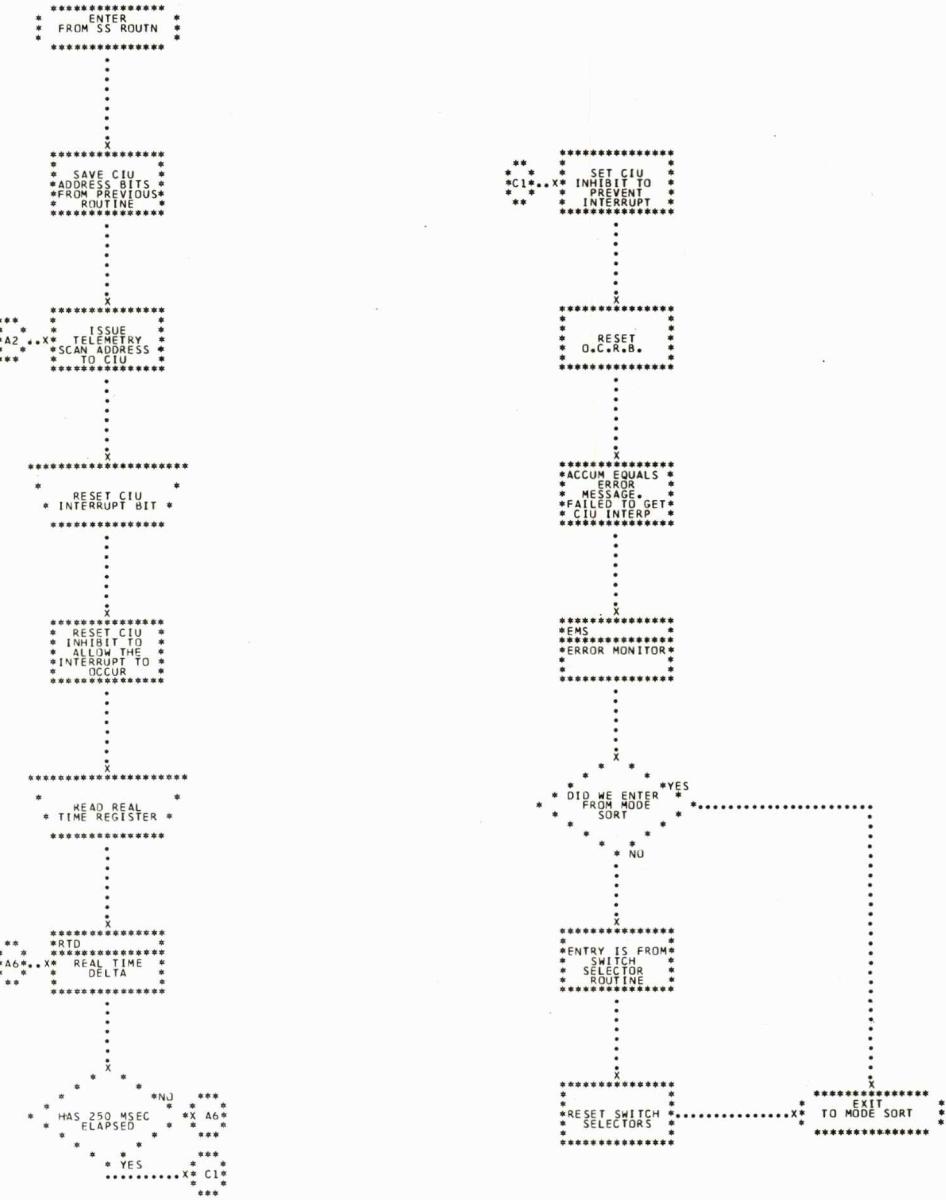


Figure 3-11. (Sheet 1 of 2) CIU Read Routine

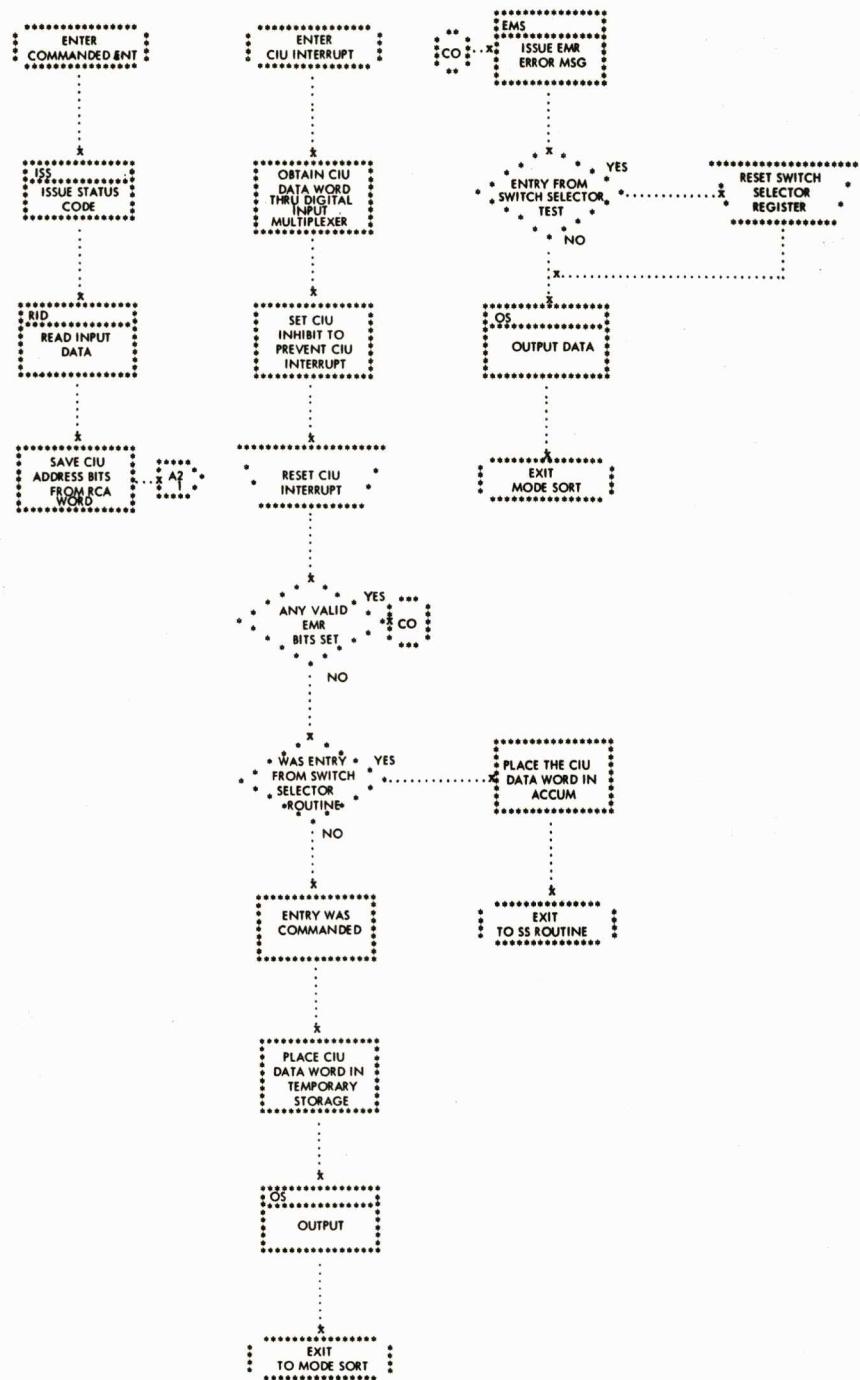


Figure 3-11. (Sheet 2 of 2) CIU Read Routine

3.1.12 Exercise Attitude Command Test Routine (Figure 3-12)

The function of this routine is to exercise the digital-to-analog LVDA ladder circuitry and to provide steering signal inputs to the control computer for testing purposes. The routine has two modes of operation.

Mode 1 provides control signals to the ladders that result in a steering command pattern of the form shown in Figure 3-13. The routine sequentially increments the pitch ladder from 0° to plus 2° in increments of 0.06° . After holding the ladder at plus 2° for 3 seconds, the routine decrements the ladder back to 0° in the same 0.06° steps. The ladder is held at 0° for 3 seconds and then incremented to minus 2° ; it is held there for 3 seconds and then decremented to 0° . The yaw ladder is then stepped in the same manner. The roll ladder is then stepped in similar manner, only the amplitude is 5° instead of 2° .

Mode 2 allows individual or simultaneous exercising of the three active ladders (Pitch, Roll, Yaw) under control of the launch computer. This mode uses an input data word (which may be changed through the Verify and Prepare to Load, and Load Routines) specifying the polarity and magnitude of the increment to be used for each ladder. The memory word format is:

S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
C	0	0	0	0	0	0	0	0	0	0	R	R	R	S _Y	S _R	S _P	0	Y	Y	Y	P	P	P		

Where: C = 0 Select Converter A

 C = 1 Select Converter B

 R, Y, P = Incremental changes in ladder output

 S, S, S = Sign of above changes

The maximum increment allowed is 0.42° (1 bit is equal to $.06^\circ$). The input data word specifies whether converter A or converter B is to be selected. Initially, all ladder output voltages are driven to zero, the specified converter is selected, and an initial increment is issued to all three ladders. Upon the occurrence of a Sync signal, each ladder output voltage will be changed by an additional increment. The ladders can be stepped to any desired value under control of the launch computer. However, the routine will automatically prevent the ladder outputs from exceeding a maximum permissible value. The routine keeps the ladders updated at 40 ms. intervals and increments them only on the occurrence of the Sync signal. The Sync discrete is honored only after a minimum time interval of one second has elapsed between each incremental change of the ladder outputs. When the launch computer decrements the ladders to

zero, it issues a special "change-direction mode" command to the LVDC which then steps the ladders to zero in the same manner they were stepped away from zero.

After each set of increments are issued, the routine monitors the SCB (Select Converter B) bit of the Error Monitor Register and the two ladder selection bits of the Discrete Input Spares Register. If the ladders have switched from the initially selected converter, the LVDC issues a unique error status code and then proceeds with the test. All ladder output voltages are driven to zero and Converter A is selected when the routine exits to Mode Sort.

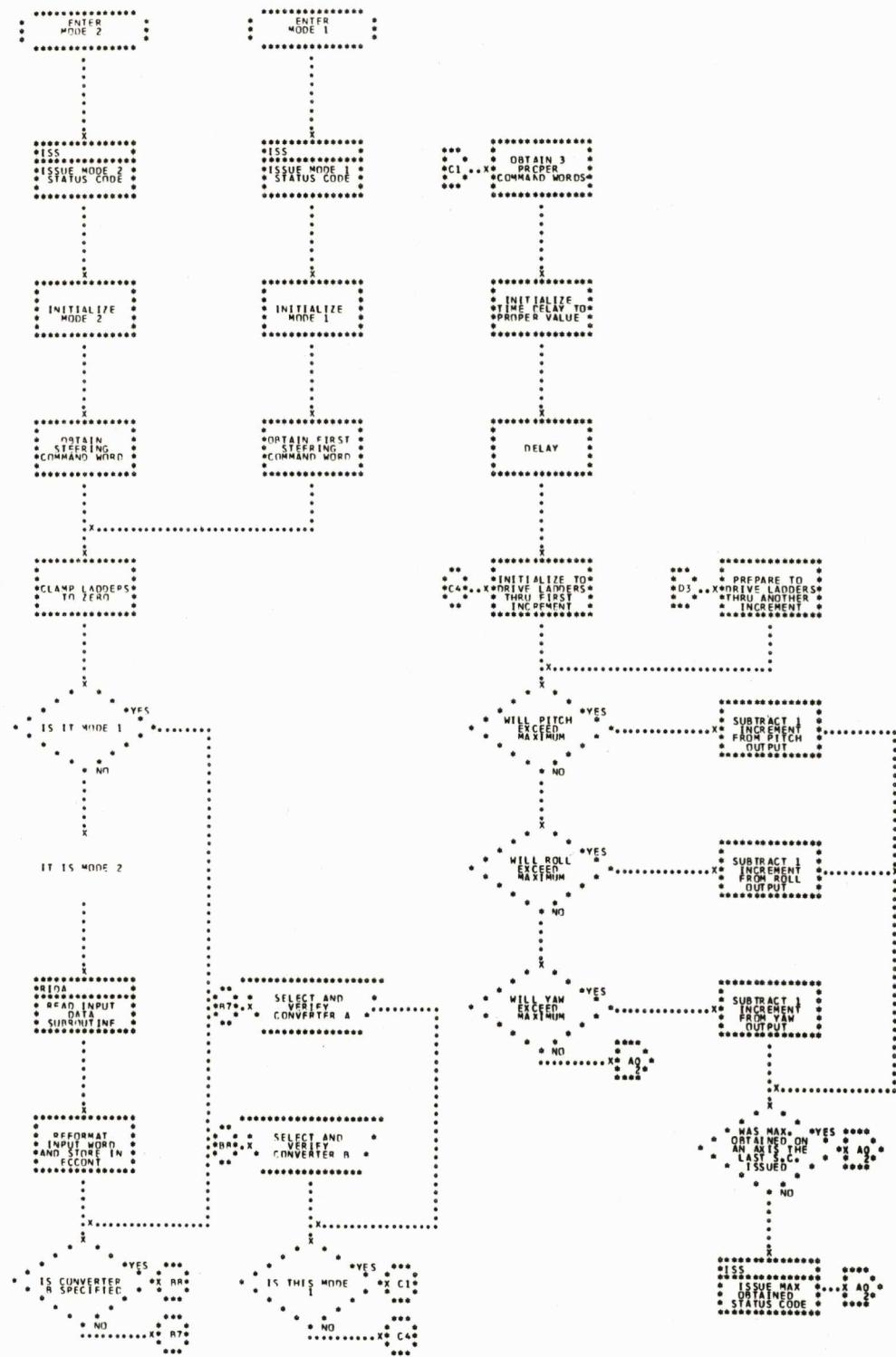


Figure 3-12. (Sheet 1 of 3) Exercise Attitude Command Test Routine

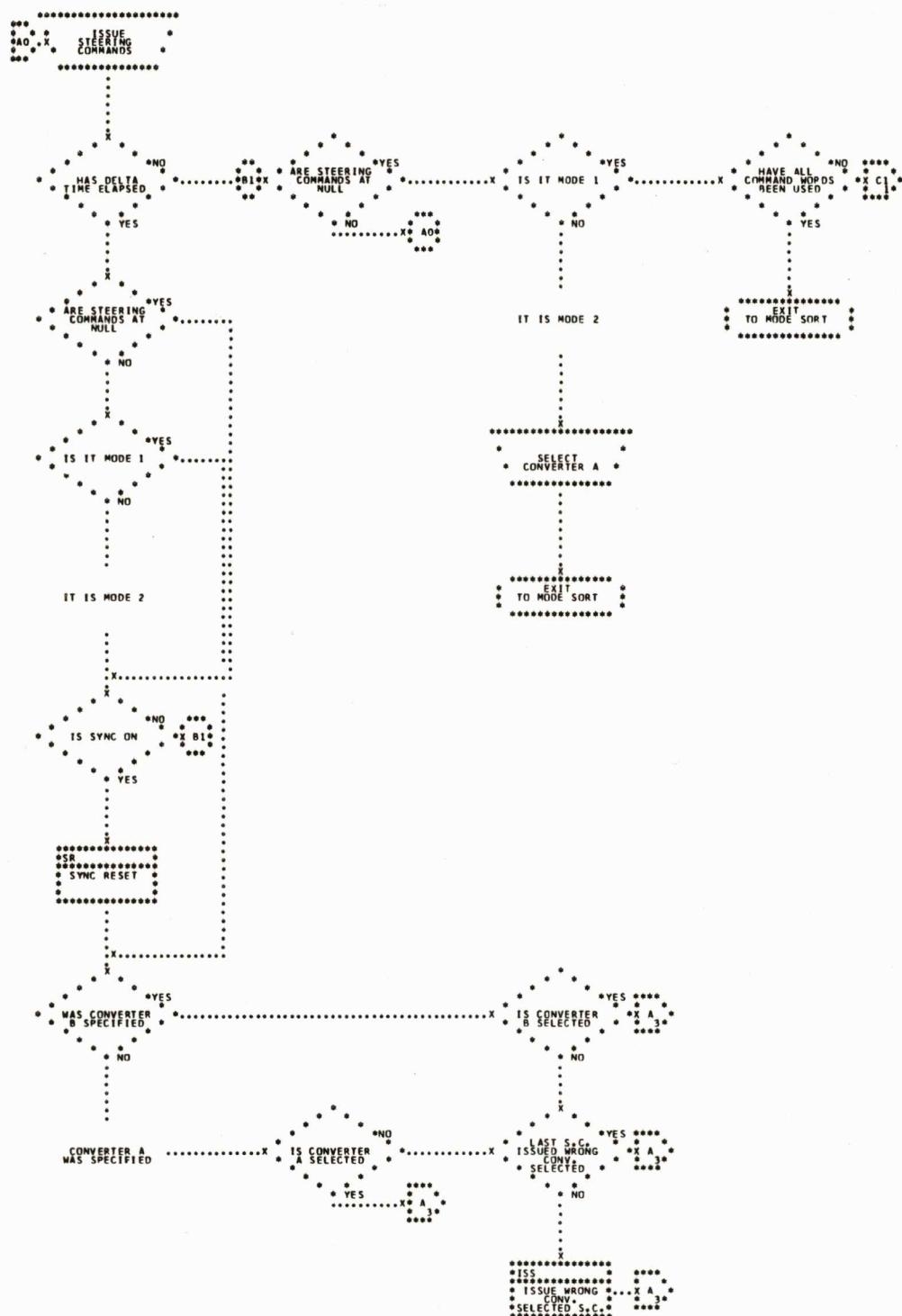


Figure 3-12. (Sheet 2 of 3) Exercise Attitude Command Test Routine

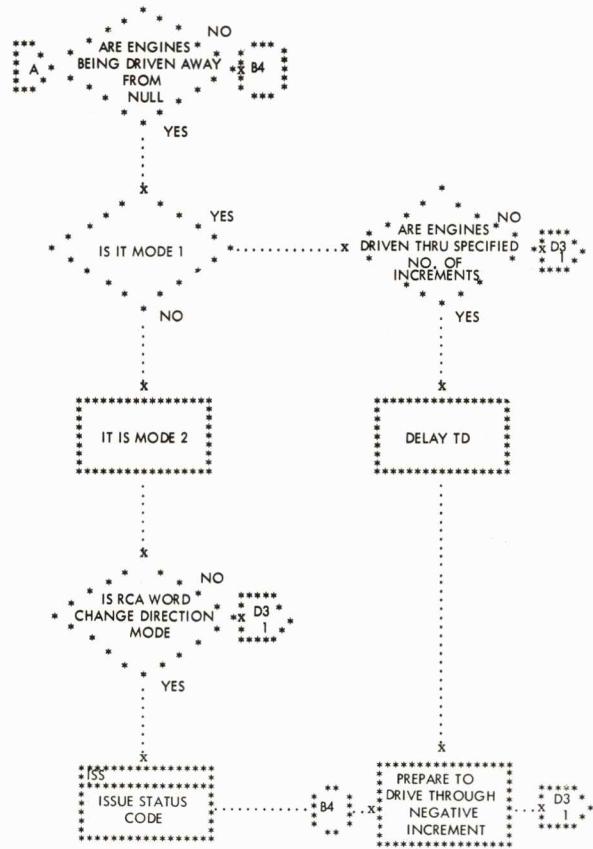


Figure 3-12. (Sheet 3 of 3) Exercise Attitude Command Test Routine

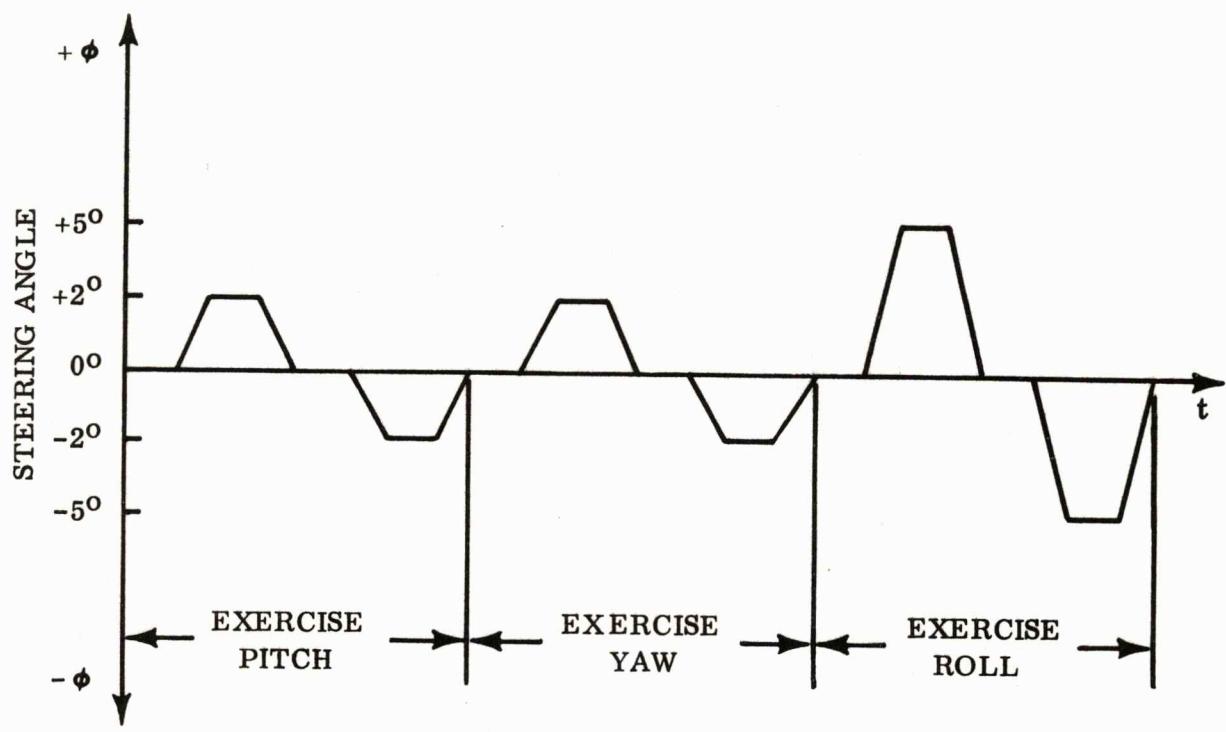


Figure 3-13. Mode 1 Steering Profile

3.1.13 G & C Steering Test Routine (Figure 3-14)

It is the purpose of this test to verify the phasing of the attitude control system by requiring the Guidance Computer to recognize deviations in platform attitude and generate steering signals to the control system of such polarity and magnitude as to correct for the attitude deviations.

The method of test is for the launch computer to control the platform attitude by sequentially deviating the pitch, roll, and yaw gimbals from their reference values. During this time, the flight computer is executing the minor loop portion of the flight routine, which generates steering commands that are a function of the difference between desired attitude and actual attitude. This routine enters the Flight Initialize Subroutine of the LVDC Flight Program to initialize the variables used in the minor loop equations, prior to actually executing the minor loop operation 25 times a second. There is no telemetered output from this routine and this routine can be terminated only by application of the Halt signal.

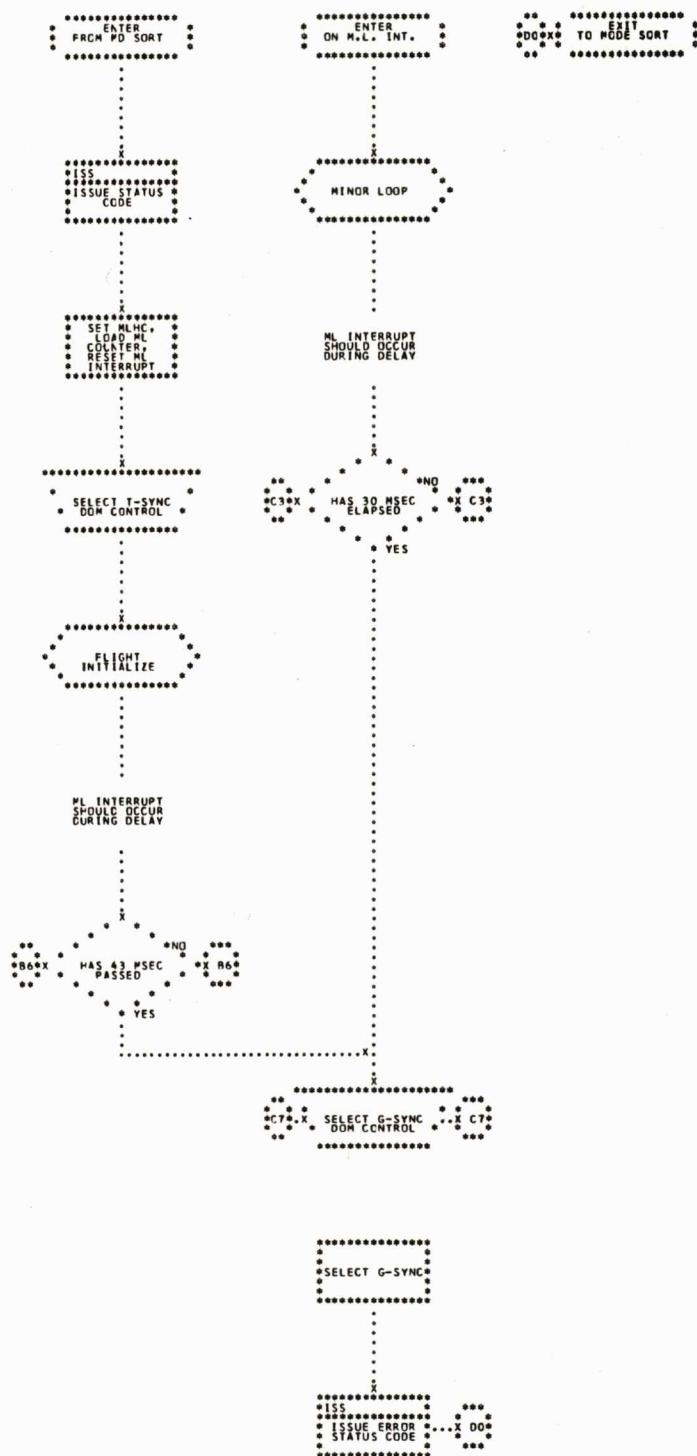


Figure 3-14. G & C Steering Test Routine

3.1.14 Discrete Input Monitor Routine (Figure 3-15)

The purpose of this routine is to allow the launch computer to verify that the LVDC can recognize the desired discrete inputs. The launch computer must simulate the desired vehicle discretes and then command the LVDC to this routine. The LVDC shall then read the discrete input and discrete input spare registers, and the Interrupt Storage Register and telemeter their contents to the launch computer. This routine shall then inhibit all interrupts except TLC, and wait for Sync. Upon receiving Sync, the LVDC shall repeat this routine, and keep repeating it on every Sync signal. This type of operation allows the LVDC to repetitively monitor the discrete inputs and Interrupts with a minimum of communication with the launch computer. The only exit from this routine is by the Halt signal.

```

***** ENTEK ****
* FROM MD SRT *
***** *****

.
.
.
X

*****
*ISS
*AL...x*ISSUE STATUS
*   * CODE
*****
***** *****

X
***** DBT DISCR.
* INPT REG. *
* DISCR INPT *
* SPRS,+ INT *
* STIM,CONT *
*****
***** *****

X
***** *****

* PLACE THEM IN *
* TEMPORARY *
* STORAGE *
*****
***** *****

X
***** OS
***** OUTPUT
*****
***** *****

***** TFL CONTENTS
* OF DISC INPUT
* DISC STORES +
* INT STIM REGS

***** *****

X
***** LIMIT ALL INT
* STORAGE
* EXCEPT TLC
*****
***** *****

X
* * * * * YES
* * * * * NO
* * * * * NU
* * * * * A7
* * * * * IS SYNC ON
* * * * * A7
* * * * * ***

* * * * * YES
* * * * * NU
* * * * * A7
* * * * * IS SYNC ON
* * * * * A7
* * * * * ***

* * * * * YES
* * * * * NU
* * * * * A7
* * * * * IS SYNC ON
* * * * * A7
* * * * * ***

***** EXIT
* TO MODE SORT
***** *****

A7x
RSS
* RESET SYNC *...x A1*
*   *   *   *

```

Figure 3-15. Discrete Input Monitor Routine

3.1.15 Discrete Output Monitor Routine (Figure 3-16)

The purpose of this routine is to allow the launch computer to verify that the LVDC can issue all discrete outputs and switch selector outputs. This routine shall read two input data words from the launch computer specifying the discretes and switch selector outputs to be affected. The first word shall specify whether the Discrete Output Register is to be set or reset and which DO's are affected. The second word specifies the Switch Selector Register outputs (read, reset, and stage selects) to be set. The word formats are:

	S	1	2	3	4	5	6	7	8	9	10	11	12	13
1.	M/D	D	D	D	D	D	D	D	D	D	D	X	D	
2.	M/D	R	R	S	S	S	S	S	0	0	0	0	N	

M/D Mode/Data Bit

D A 1-bit in this area signifies that particular discrete output register latch is to be set or reset, depending on the value of the X-bit.

X ON/OFF bit that determines set or reset PIO to discrete output register; 1 = set, 0 = reset.

R Switch Selector Read Bit

R Switch Selector Reset Bit

S Switch Selector Stage Select Bits

N Causes Switch Selector Load PIO to be bypassed when equal to "1".

The desired discretes and/or switch selector outputs are set (or reset) and the routine exits to Mode Sort. In this manner the launch computer can command the setting or resetting of any LVDC discrete output or switch selector output for any length of time. It shall be the responsibility of the launch computer to reinitialize the Discrete Output Register and Switch Selector Register using this routine at the completion of their test program.

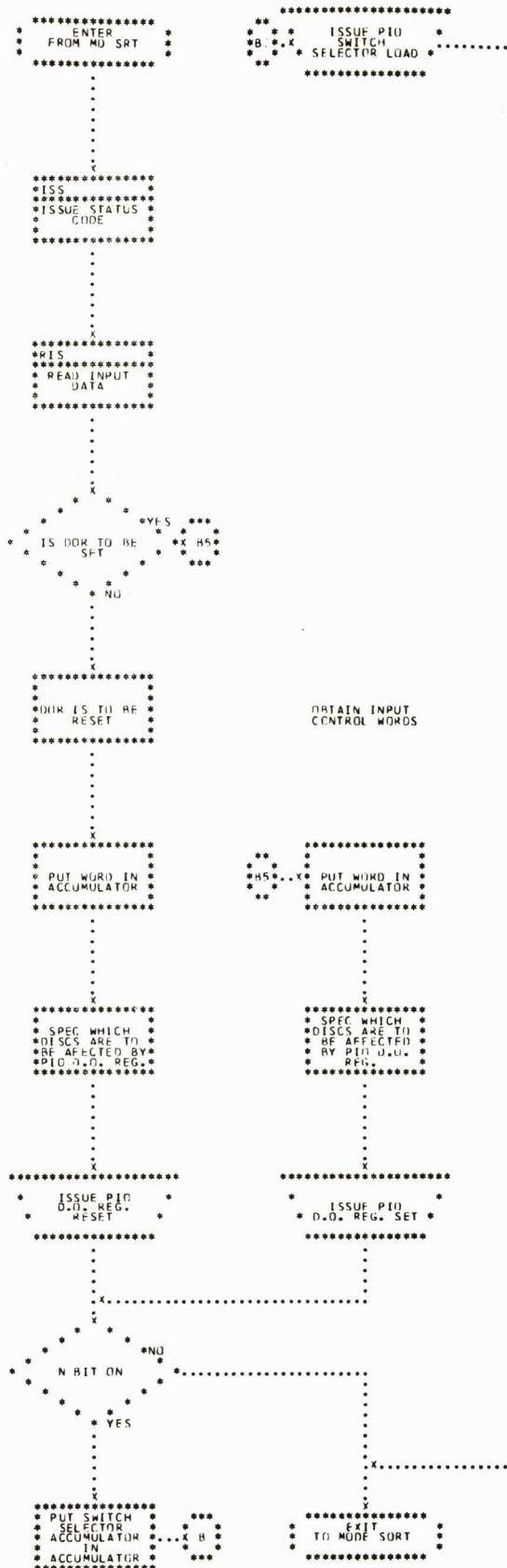


Figure 3-16. Discrete Output Monitor Routine

3.1.16 DOM Test Routine (Figure 3-17)

The purpose of this routine is to exercise the LVDA Data Output Multiplexer (DOM). It is the responsibility of the launch computer to verify proper operation of the DOM by analysis of the telemetered data. This routine exercises the following features of the DOM.

1. Loading of all pertinent PIO addresses into the DOM disregarding the associated data.
2. The LVDC telemetry word override capability.
3. Rejection of new data if all four channels are loaded.
4. The "half-valid" feature associated with the minor loop operation.

The successful execution of this routine depends on the ability of the launch computer to obtain valid DOM data in a predefined sequence. The routine delays 22 ms. after loading the DOM. The delay allows the launch computer to step the data out of the DOM.

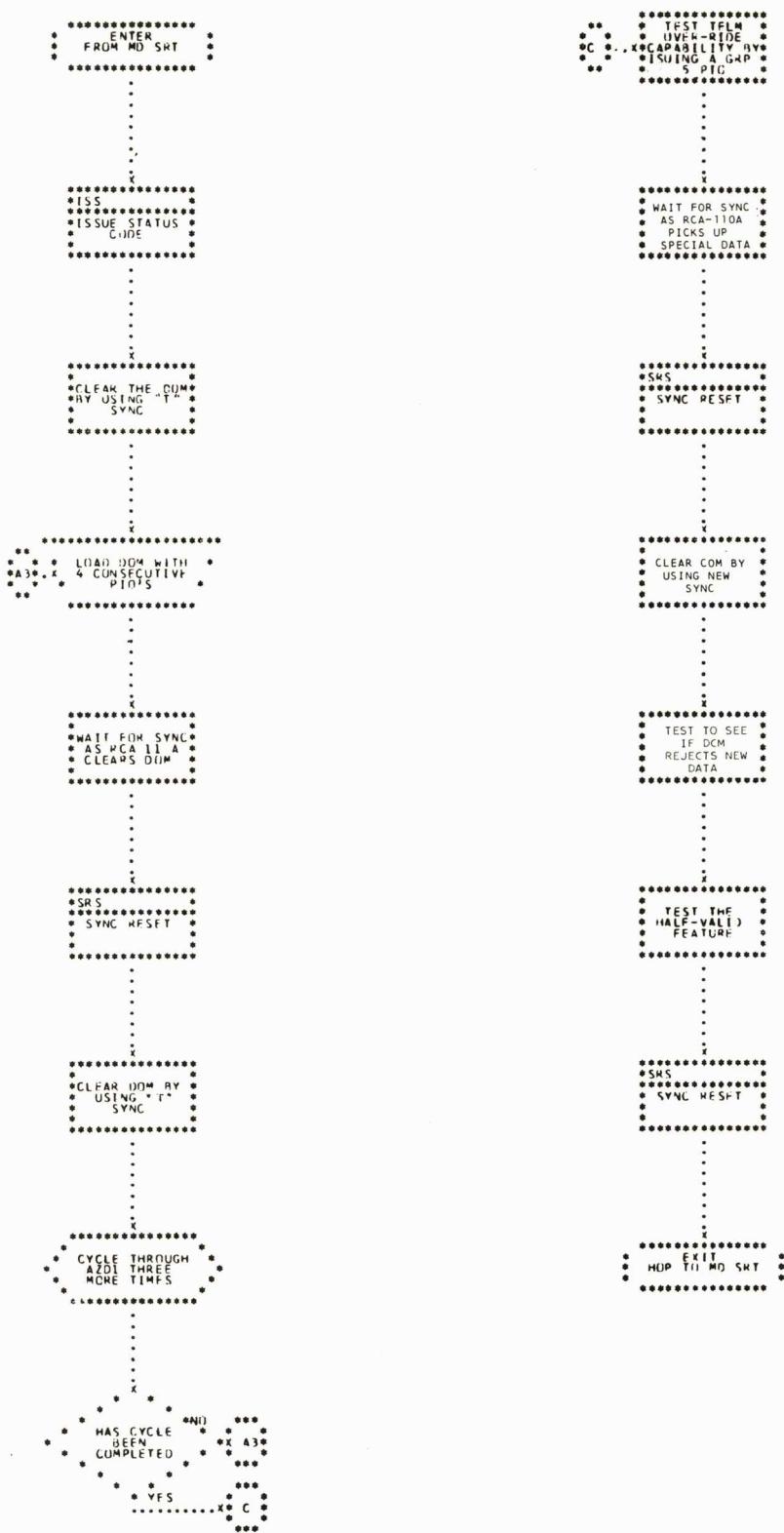


Figure 3-17. DOM Test Routine

3.1.17 Ladder Error Test Routine (Figure 3-18)

The purpose of this routine is to exercise the ladder error detection circuits. In this routine all ladder commands are held for a minimum of 2.5 ms. to allow full charging of the Sample and Hold capacitors.

This routine initially zeros all ladder voltages, selects Converter A (and verifies its selection), and then performs the following functions on the first ladder (pitch):

1. Issues a zero command to the pitch ladder output.
2. Sets ICR 2 which inhibits Converter A from being changed.
3. Issues a ladder command of plus 0.192 volts (4 bits).
4. Determine if Converter A is still selected, if not, indicate an error condition.
5. Reselects Converter A if necessary and verifies the selection.
6. Issues a ladder command of plus 0.384 volts (8 bits).
7. Determine if Converter A is still selected, if so, indicate an error condition.
8. Resets ICR 2.
9. Issues a zero command to the ladder.
10. Reselects Converter A and verifies its selection.
11. Sets ICR 2.
12. Issues a ladder command of minus 0.192 volts.
13. Determine if Converter A is still selected, if not, indicate an error condition.
14. Reselects Converter A if necessary.
15. Issues a ladder command of minus 0.384 volts.
16. Determine if Converter B has been selected, if not, indicate an error condition.

17. Resets ICR 2.
18. Issues a zero command to the ladder.
19. Reselects Converter A and verifies its selection.

The above procedure exercises and verifies the coarse comparator. The fine comparator is exercised and verified as follows:

1. Sets ICR 11.
2. Issues a zero command to the pitch ladder.
3. Delay six instructions.
4. Determine if Converter A is still selected, if not, indicate an error condition.
5. On the tenth instruction following Step 2, determine if Converter B has been selected. If not, indicate an error condition.
6. Reselects Converter A and verifies its selection.

If an error condition is recognized at any time in this routine, the LVDC enters the Error Monitor Subroutine, issues the Error Monitor status code, and telemeters the error message and the contents of the EMR Register. The LVDC then loops waiting for Sync. Upon recognizing the Sync signal, the LVDC returns to the Ladder Error Test. After the return, the ladders are clamped to zero and Converter A is reselected.

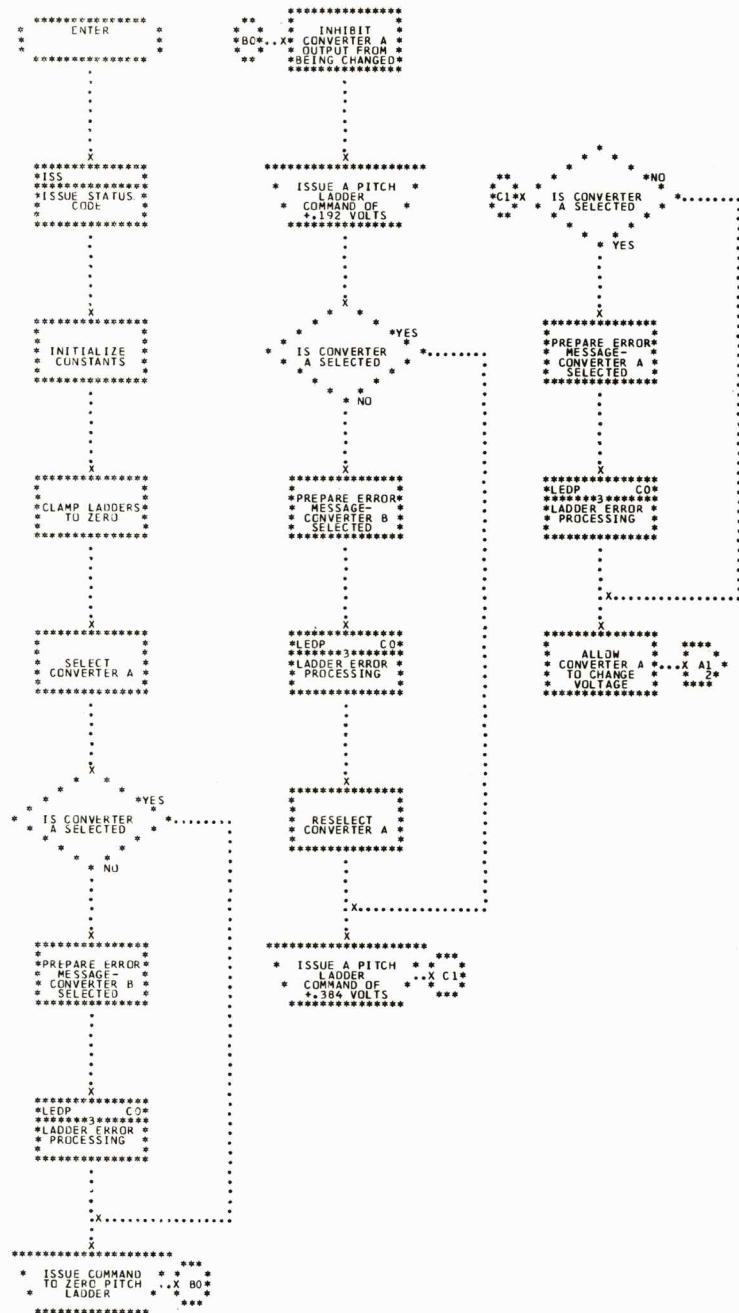


Figure 3-18. (Sheet 1 of 3) Ladder Error Test Routine

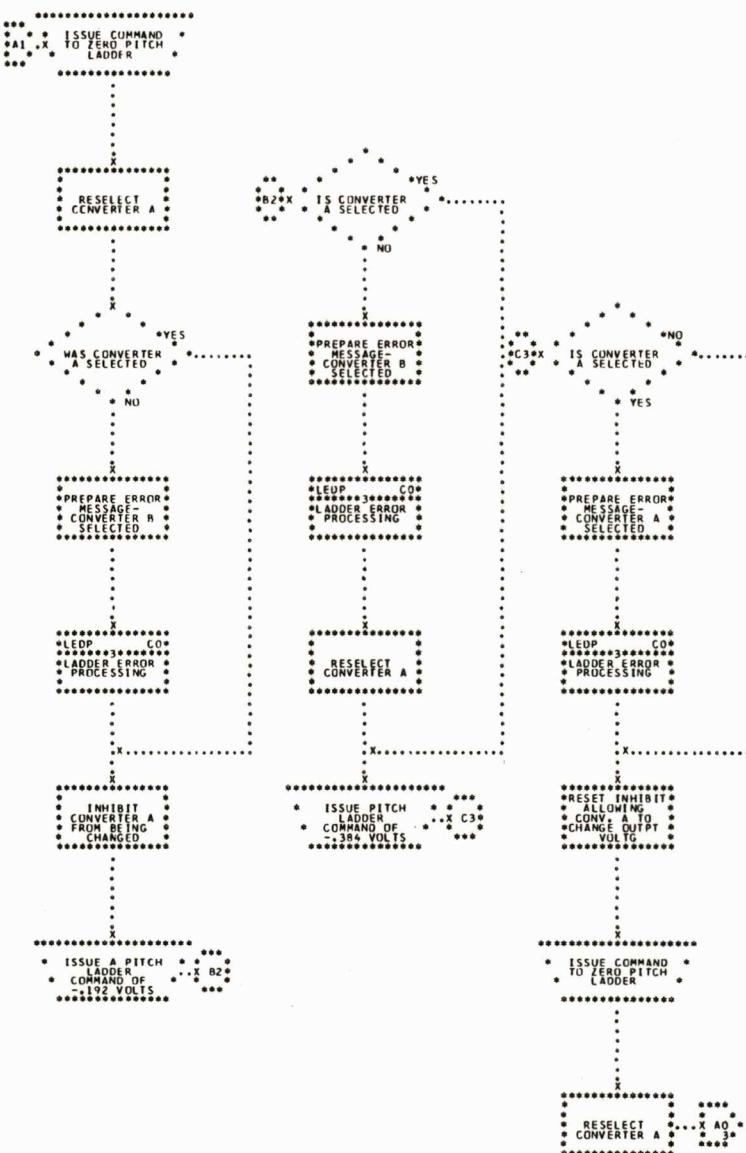


Figure 3-18. (Sheet 2 of 3) Ladder Error Test Routine

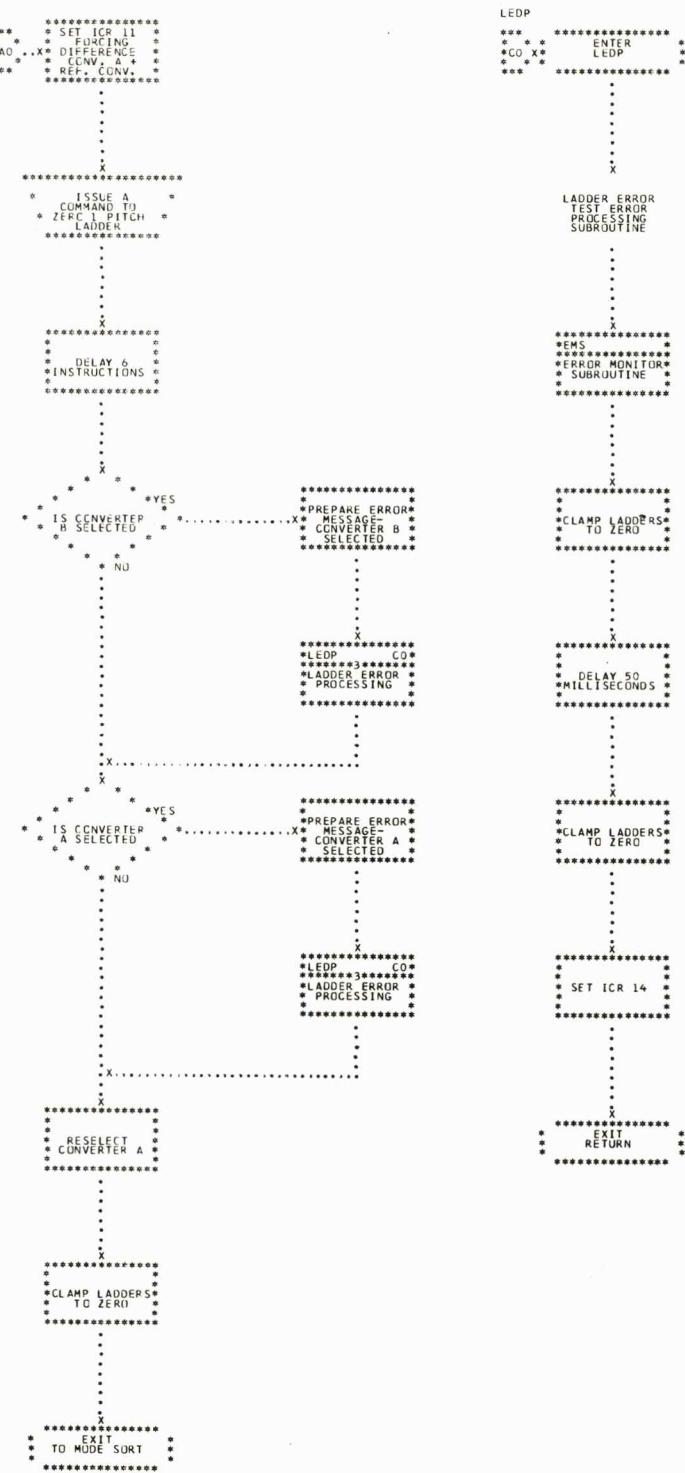


Figure 3-18. (Sheet 3 of 3) Ladder Error Test Routine

3.1.18 Minor Loop, Switch Selector, and Real Time Counter Tests (Figure 3-19)

The purpose of this routine is to insure that all of the logic of the minor loop, switch selector and real time counters is fully exercised and checked.

The Minor Loop counter is loaded with 1.28 seconds. Following a 4.8 ms. delay the Switch Selector counter is loaded with 1.28 seconds. The test on these counters follows immediately.

The program tests the counter functions in the following manner:

1. The Real Time Counter is exercised to insure the counter increments by 1 count every 3 instruction times.
2. The Minor Loop Counter is exercised to insure that the minor loop interrupt (INT 12) occurs 1.28 seconds after the counter is loaded.
3. The Switch Selector Counter is exercised to insure that the switch selector interrupt (INT 11) occurs 1.28 seconds after the counter is loaded.

If this routine executes without detecting an error condition, a return is made to the Mode Sort Routine. If an error is discovered, an error message is telemetered by the Error Monitor Subroutine, and then the routine returns to Mode Sort.

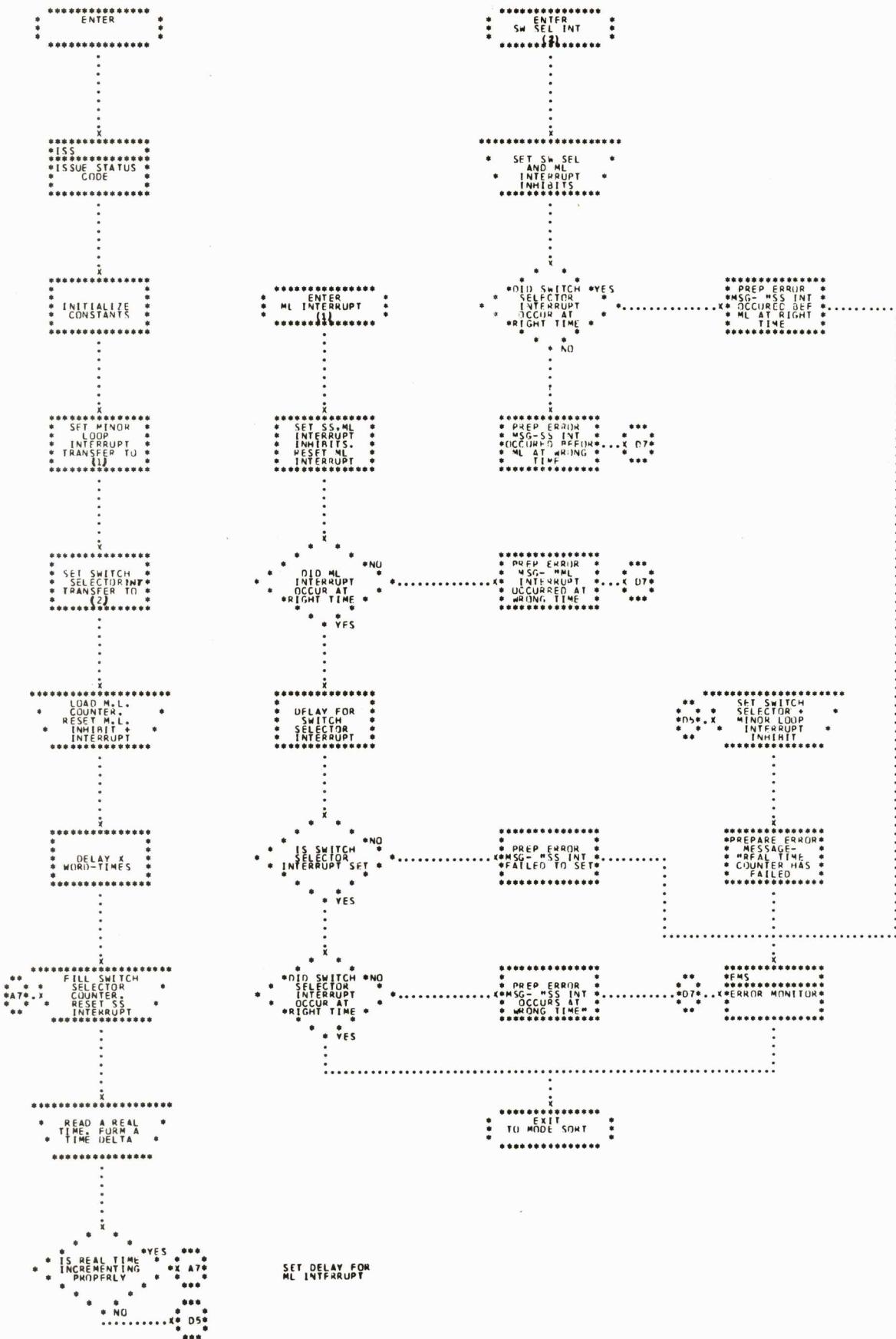


Figure 3-19 Minor Loop, Switch Selector and Real Time Counter Tests

3.1.19 Memory Error Test (Figure 3-20)

The purpose of the Memory Error Test Routine is to perform the testing of the memory error detection circuitry and logic. This check is divided into the following two categories:

1. Tests initiated with the SHF instruction.
2. Tests initiated with the PIO instruction.

The SHF instruction, with address bits A7 and A3 set equal to a 1, generates a Memory Sync Pulse when the error detect logic is testing for no memory current.

The SHF test is implemented as follows:

1. Select simplex even data module.
2. Execute SHF.
3. Check for EAM and TLC.
4. Read location addressed by SHF.
5. Check for EAM and TLC.
6. Select simplex odd data module.
7. Execute SHF.
8. Check for EBM and TLC.
9. Read location addressed by SHF.
10. Check for EBM and TLC.
11. Restore odd memory location.
12. Select duplex data modules.
13. Read location addressed by SHF.
14. Check for EAM and that even module data was restored by odd module data.
15. Select simplex odd data module.

16. Execute SHF.
17. Select duplex data modules.
18. Read location addressed by SHF.
19. Check for EBM and that odd module data was restored by even module data.
20. Execute SHF.
21. Check for TLC, EBM, and EAM.
22. Restore destroyed locations.

The second category of tests is initiated with a PIO instruction with address 775. This PIO instruction is then followed by a MPH, SUB, XOR, or CLA. This combination of instructions test the current error detect circuitry by multiple memory address selection during the following times:

1. MPH, during restore pulse of Syllable 1.
2. SUB, during read pulse of Syllable 1.
3. XOR, during restore pulse of Syllable 0.
4. CLA, during read pulse of Syllable 0.

The PIO test is implemented as follows:

1. Address each of the HI Y tests locations.
2. Test each location, with the four instructions, insuring that EAM and EBM occur correctly.
3. Address each of the HI Y, LO X, AND LO Y test locations in the same manner.
4. Restore all test locations.

The above tests are repeated for all available modules. At the completion of the routine, the exit is to Mode Sort.

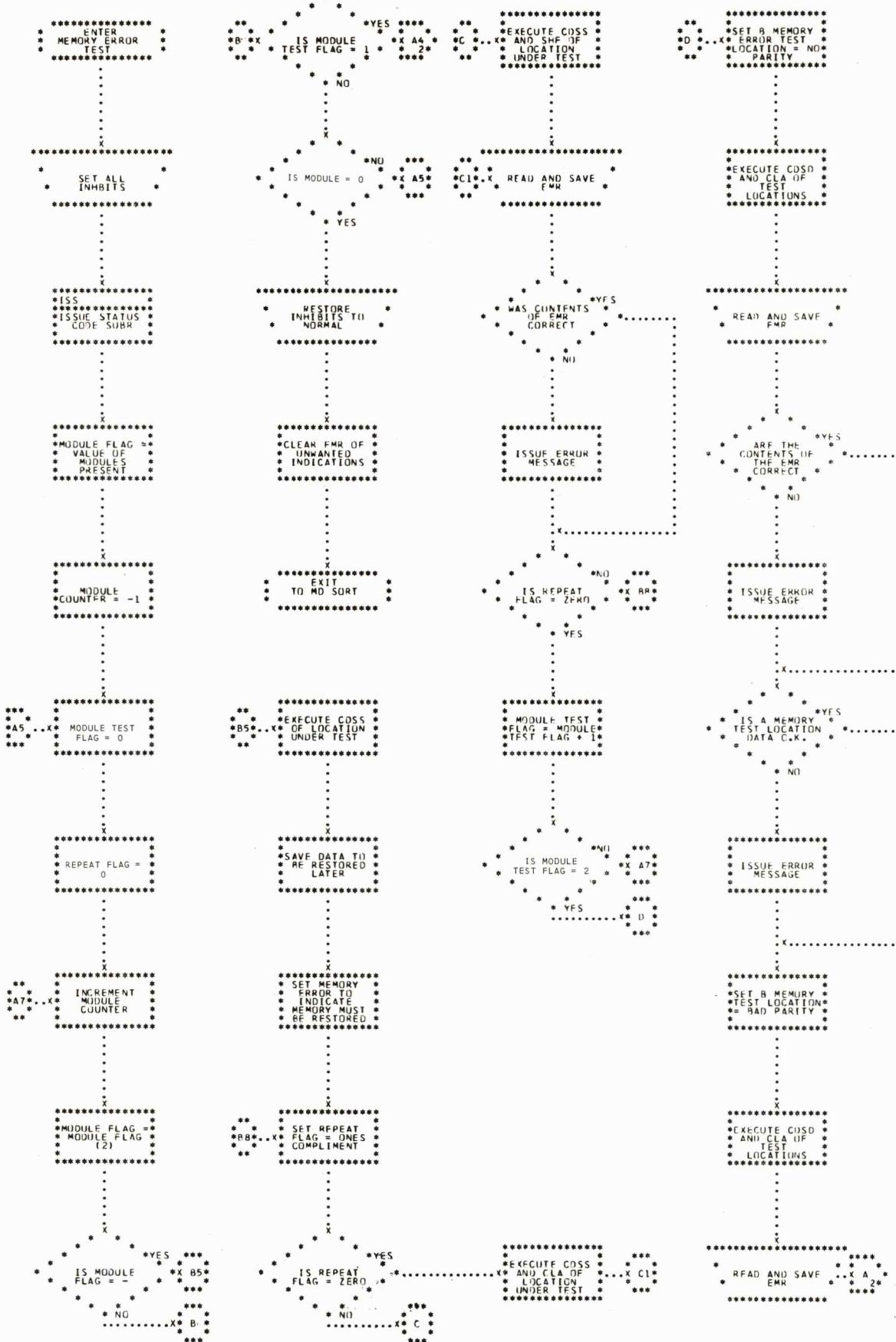


Figure 3-20. (Sheet 1 of 3) Memory Error Test

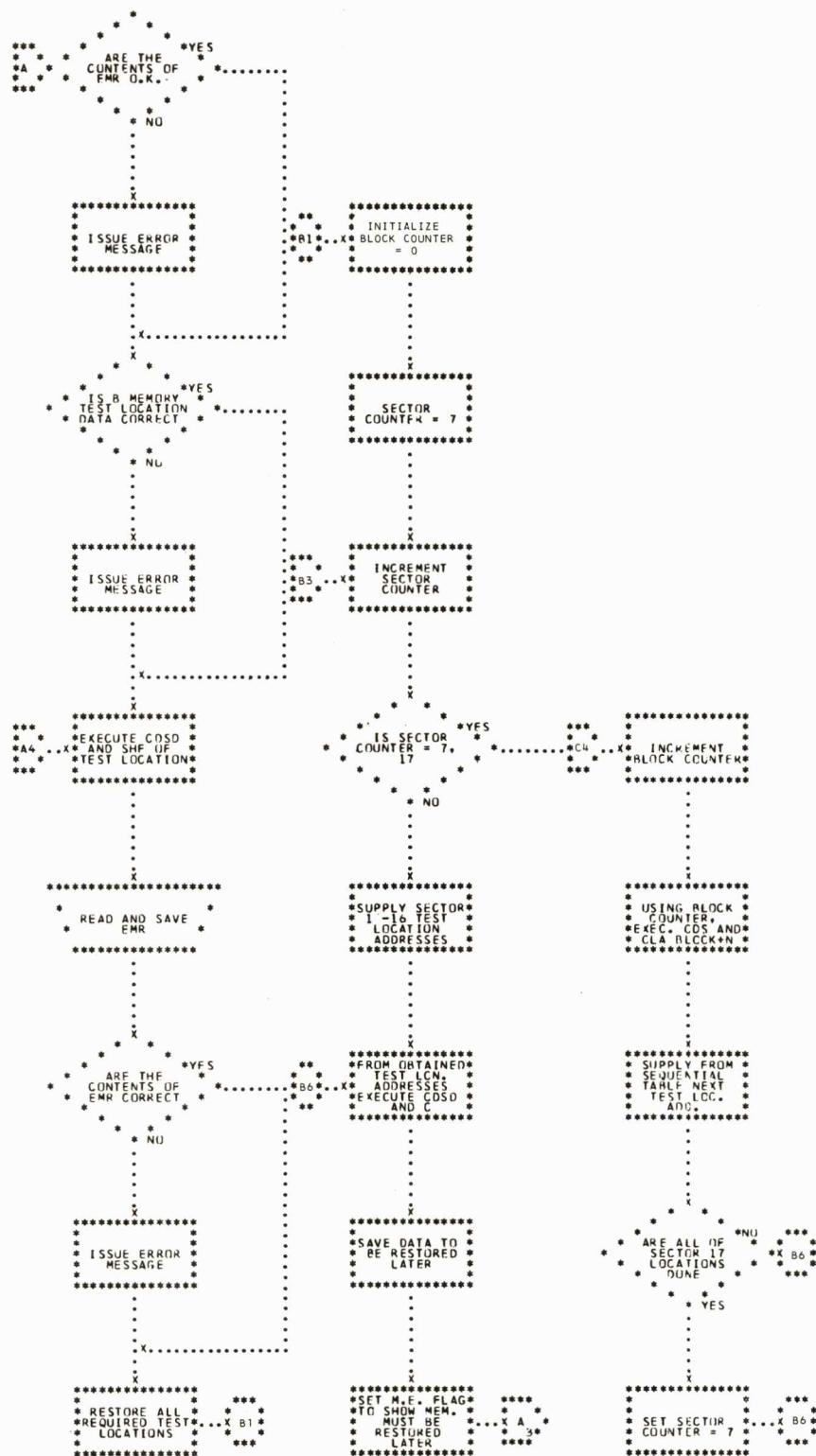


Figure 3-20. (Sheet 2 of 3) Memory Error Test

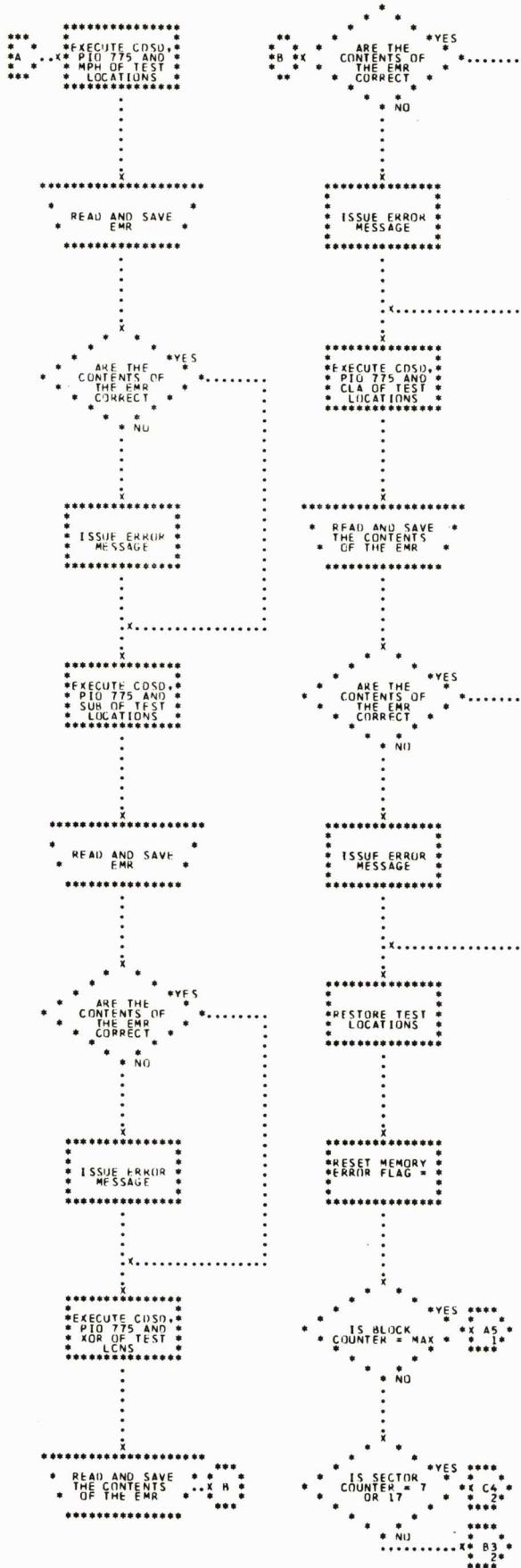


Figure 3-20. (Sheet 3 of 3) Memory Error Test

3.1.20 Interrupt Processing Routine (Figure 3-21)

The purpose of the Interrupt Processing Routine is to determine which interrupt occurred and to direct the LVDC to the corresponding processing routine. This routine is entered automatically every time an interrupt HOP 400 is generated. The contents of the accumulator and PQ register, which represent partial results from the program wherein the interrupt occurred, will be saved at the beginning of the Interrupt Processing Routine and restored to their respective locations when the interrupt has been processed. Determination of which interrupt occurred is done by repeatedly shifting the Interrupt Storage Register contents to the left and executing a HOP to the indicated processing routine when a one-bit is discovered in the sign position. One-bits representing interrupts whose inhibits are set will be eliminated from the word before the shifting and testing process begins. This is to insure that interrupts whose inhibits are set will not be mistaken as the true cause of the current interrupt. If no one-bit is found in interrupt storage, even though an interrupt did occur, the Interrupt Processing Routine will transfer to the Error Monitor Subroutine. Transfer to the Mode Sort Routine will then occur (with the exception of a TLC interrupt). The location to which a particular interrupt branch transfers program control is dependent upon the particular program using that interrupt; therefore, the generalized Interrupt Processing Routine flow shows no specific exit except for the error branch.

All interrupts except TLC will be inhibited while a TLC interrupt is being processed. After TLC processing is completed, the normal inhibits will be restored.

Upon occurrence of the GRR interrupt T-Sync is selected before entering the Flight Program.

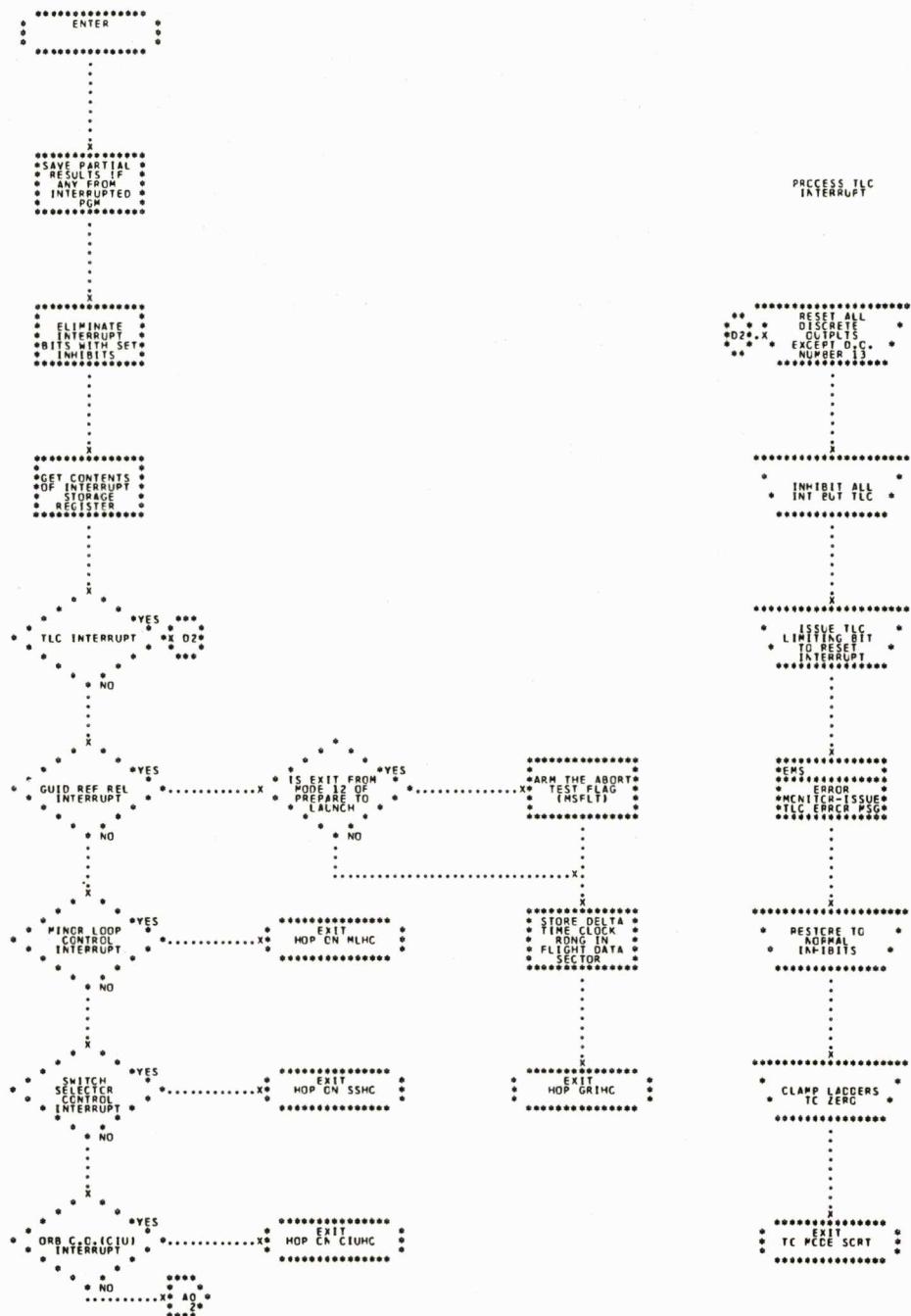


Figure 3-21. (Sheet 1 of 2) Interrupt Processing Routine

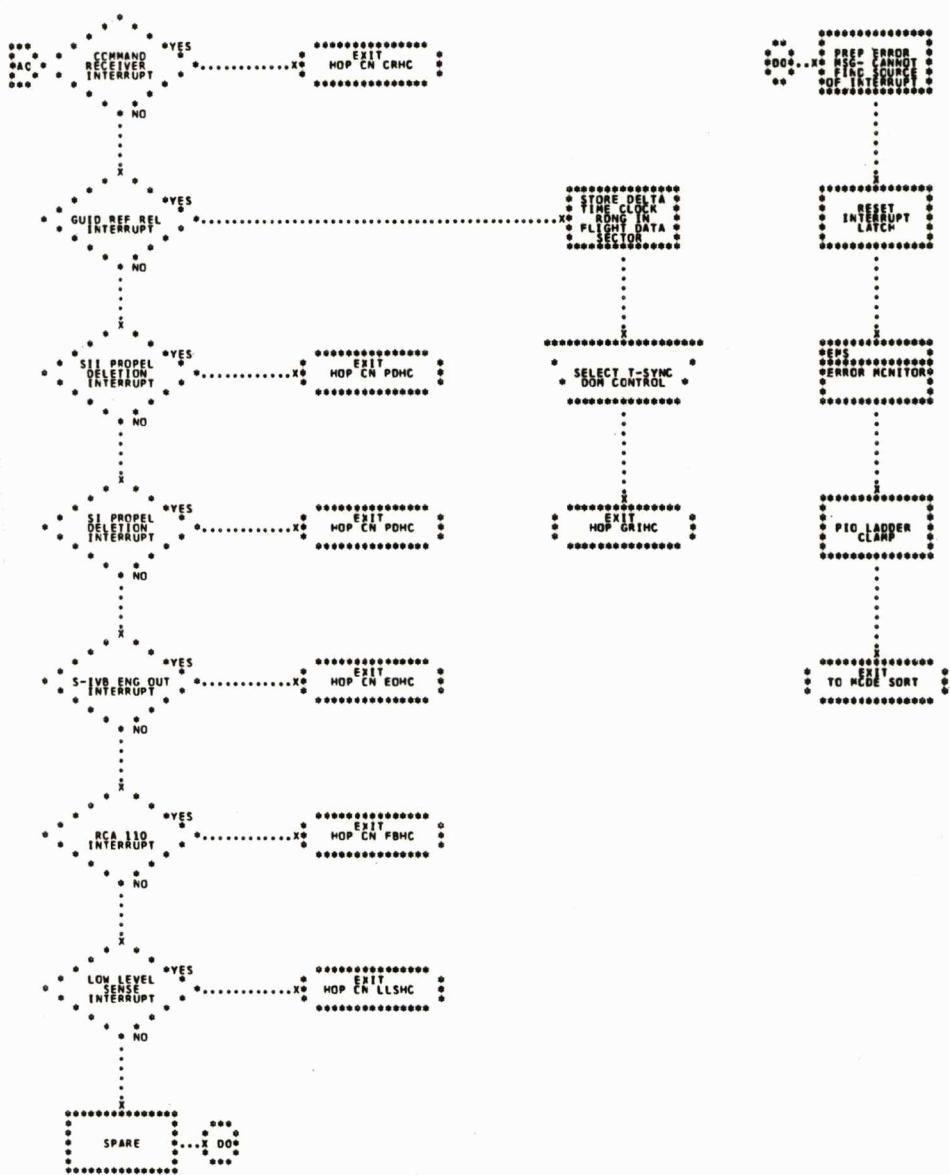


Figure 3-21. (Sheet 2 of 2) Interrupt Processing Routine

3.1.21 Prepare to Launch Routine (Figure 3-22)

The purpose of this routine is to prepare the LVDC for entering the Flight Program. It is the last commanded preflight routine prior to launch. This routine is made up of three basic sections:

1. Entry and Initialization
2. Slow Loop
3. Fast Loop

There are three commandable entries to this routine as described below:

1. For expected entry into Flight Simulation with no inertial platform.
2. For expected entry into Flight Program with an inertial platform.
3. For expected entry into Flight Simulation with the inertial platform.

The initialization is performed on program flags, the Interrupt Inhibit Register, the Internal Control Register, the Discrete Output Register, and the ladder outputs. Expected Gimbal Angle Reasonableness constants are computed from the Firing Azimuth and Position 1 Azimuth.

The slow loop performs the following functions:

1. Check for all active interrupts to be in the "off" state.
2. Check for correct status of active discrete inputs.
3. Check to see if the Sim Flight Indicator indicates the Flight or Sim Flight with Platform. If so, perform the following sequence. If not, go to step 4.
 - a. Check to see if GRRA has been issued without PLOT and GMT being loaded, and the platform not aligned to the correct azimuth. If these conditions exist, issue an error message and go to step 4. If GRRA is set with all conditions met, go to step 4.
 - b. Check to see if one minute has elapsed since entry without PLOT or GMT being loaded. If so, issue an error message and go to step 4.
 - c. Check to see if PLOT has been loaded initially or changed since last pass through the program.

- d. Check to see if this is a variable launch mission; if not, go to step f.
 - e. Check to see if PLOT is within the launch window. If not, issue an error message and proceed to step 4. The PLOT launch window test is not performed on Skylab I vehicles.
 - f. Compute the correct firing azimuth after PLOT and ETPTL have been loaded. On Saturn IB vehicles, the firing azimuth is calculated by the S-IB Azimuth Calculate Subroutine. Saturn V firing azimuth is calculated by the Flight Program.
 - g. Check to see if the firing azimuth is within range safety limits. If not, issue an error message and proceed to step 4. If azimuth is correct, telemeter its true and complement form along with a DO 2 interrupt to the RCA-110A.
 - h. Compute the expected Gimbal Angle Reasonableness constants using the new firing azimuth. Omit Gimbal Angle Reasonableness Test until RCA-110A interrupt (used as a discrete) is received. If Platform Aligned indication is not received by T-152 seconds, an error message is telemetered.
4. Check to see if Gimbal Angle Reasonableness test is to be bypassed. If so, test for the RCA-110A interrupt set condition. If set, start performing a reasonableness test on the fine and backup gimbal angle inputs from the inertial platform, if the platform is present.
 5. Telemeter the fine and backup gimbal angle readings, the values in the LVDA real time counter and velocity accumulation counters, and an alternating bit pattern as a special telemetry test.
 6. Execute the Accelerometer Monitor Subroutine if the platform is present. This subroutine is bypassed while the platform is being positioned.
 7. Execute the Error Monitor Subroutine to check for valid EMR bits.
 8. Execute the LVDC Self-Test Subroutine.
 9. Execute the LVDA Timing and Counter Test Subroutine.
 10. Telemeter status of Discrete Input Register, Discrete Input Spares Register, Interrupt Storage Register and Error Monitor Register. This telemetry applies only to 206 and subs and 513 and subs.

In addition, the slow loop is capable of commanding the Verify and Prepare to Load Routine, or the Load Routine to allow loading a block of 16 words by the RCA-110A.

Upon recognizing the Guidance Reference Release Alert signal (GRRA), this routine enters the fast loop which deletes the following from the above sequence:

1. Accelerometer Monitor Subroutine.
2. LVDA Timing and Counter Test Subroutine.
3. The loading capability.
4. The Variable Azimuth computation capability.

Any program-detected error in the Prepare to Launch Routine causes transfer to the Error Monitor Subroutine where DO 13 is set and the normal notification of error is made to the launch computer. Resetting of DO 13 can be accomplished by application of the Halt signal, or by allowing Prepare to Launch to proceed to the next LVDA initialize subroutine section.

The only exits from this program are:

1. The Guidance Reference Release Interrupt which transfers control to the Flight Initialize Routine of the LVDC Flight Program.
2. Application of the Halt signal.

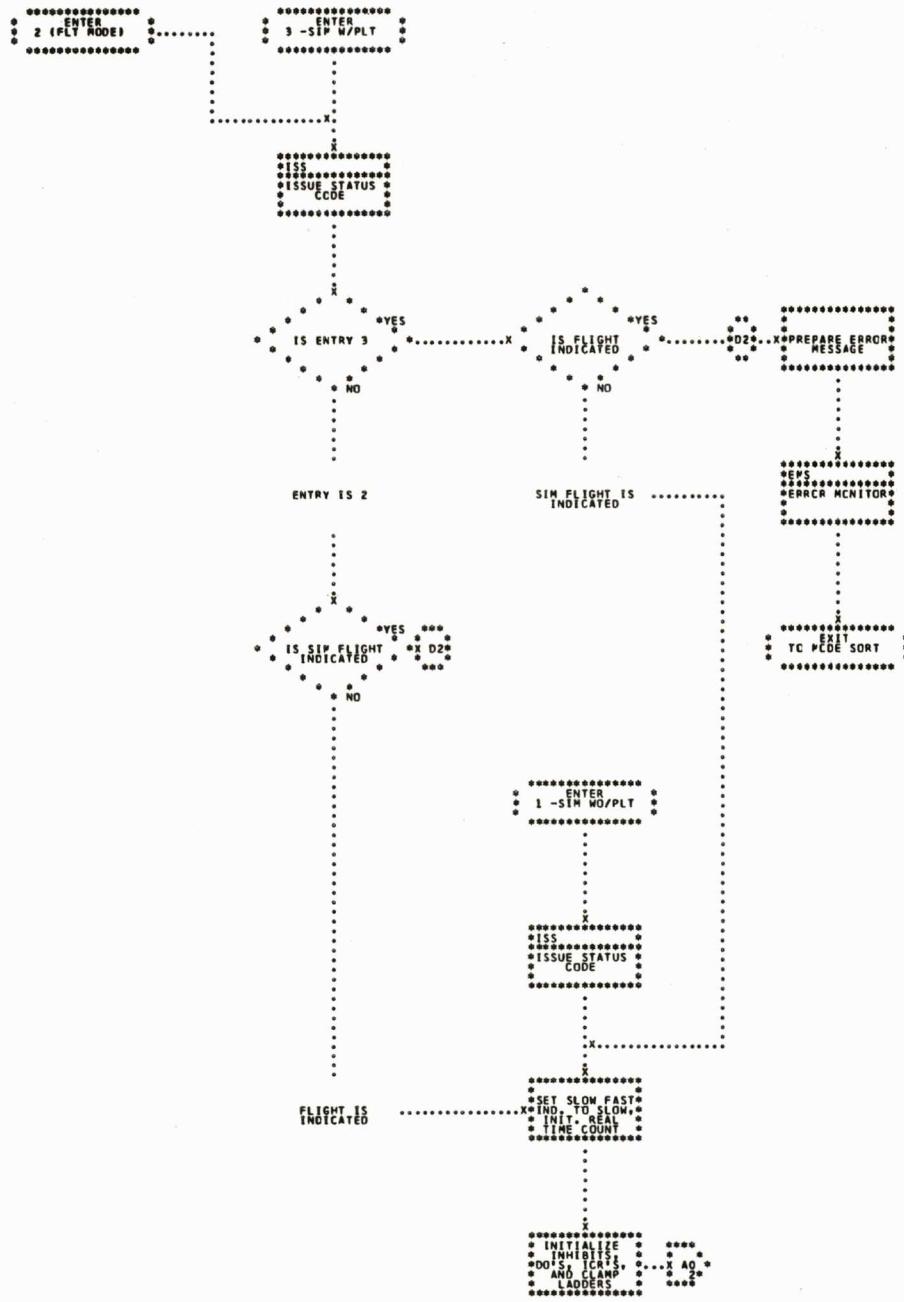


Figure 3-22. (Sheet 1 of 5) Prepare to Launch Routine

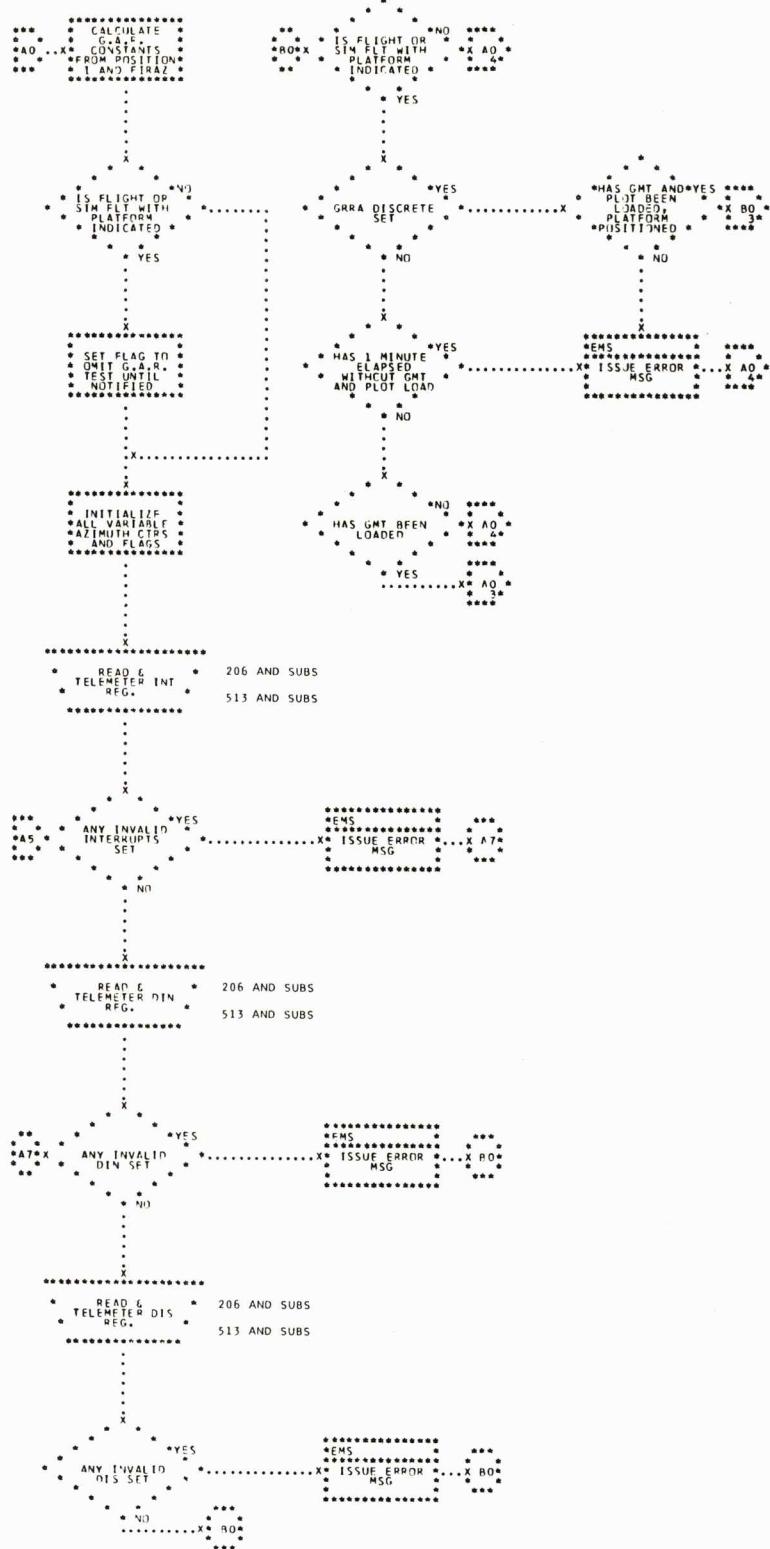


Figure 3-22. (Sheet 2 of 5) Prepare to Launch Routine

Change 1

Changed 1 September 1972

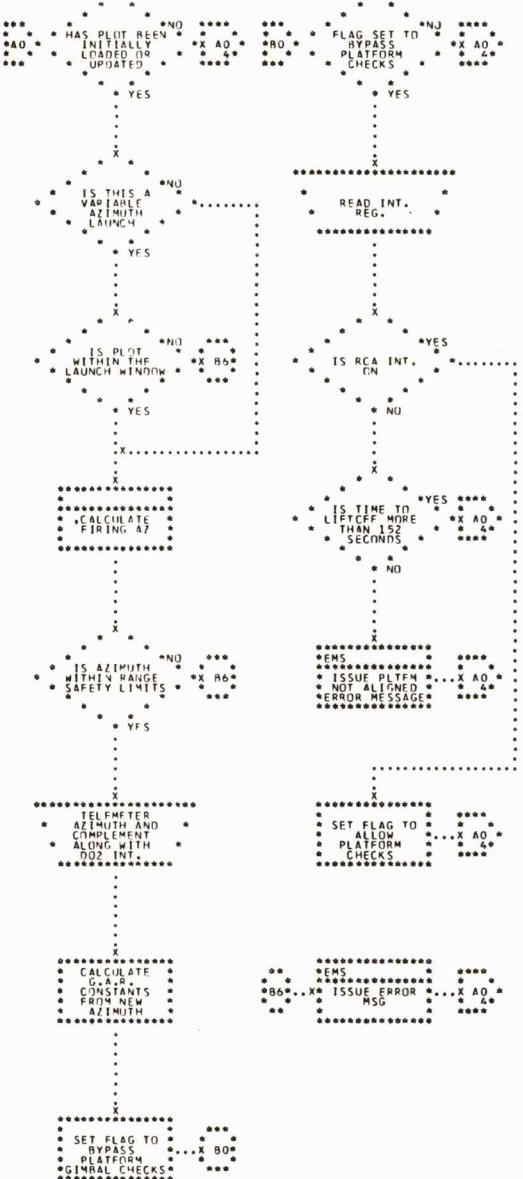


Figure 3-22. (Sheet 3 of 5) Prepare to Launch Routine

Change 1

Changed 1 September 1972

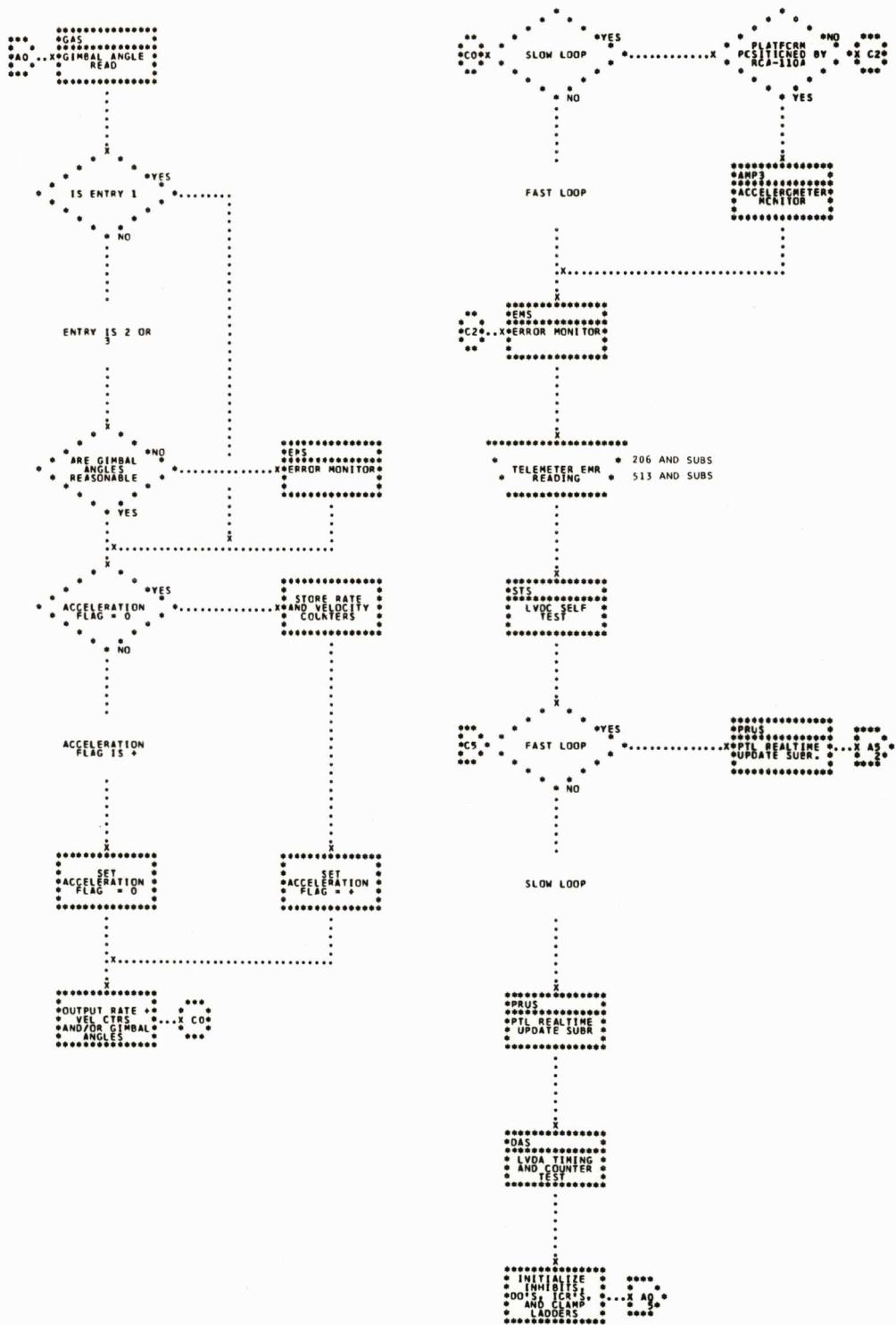


Figure 3-22. (Sheet 4 of 5) Prepare to Launch Routine

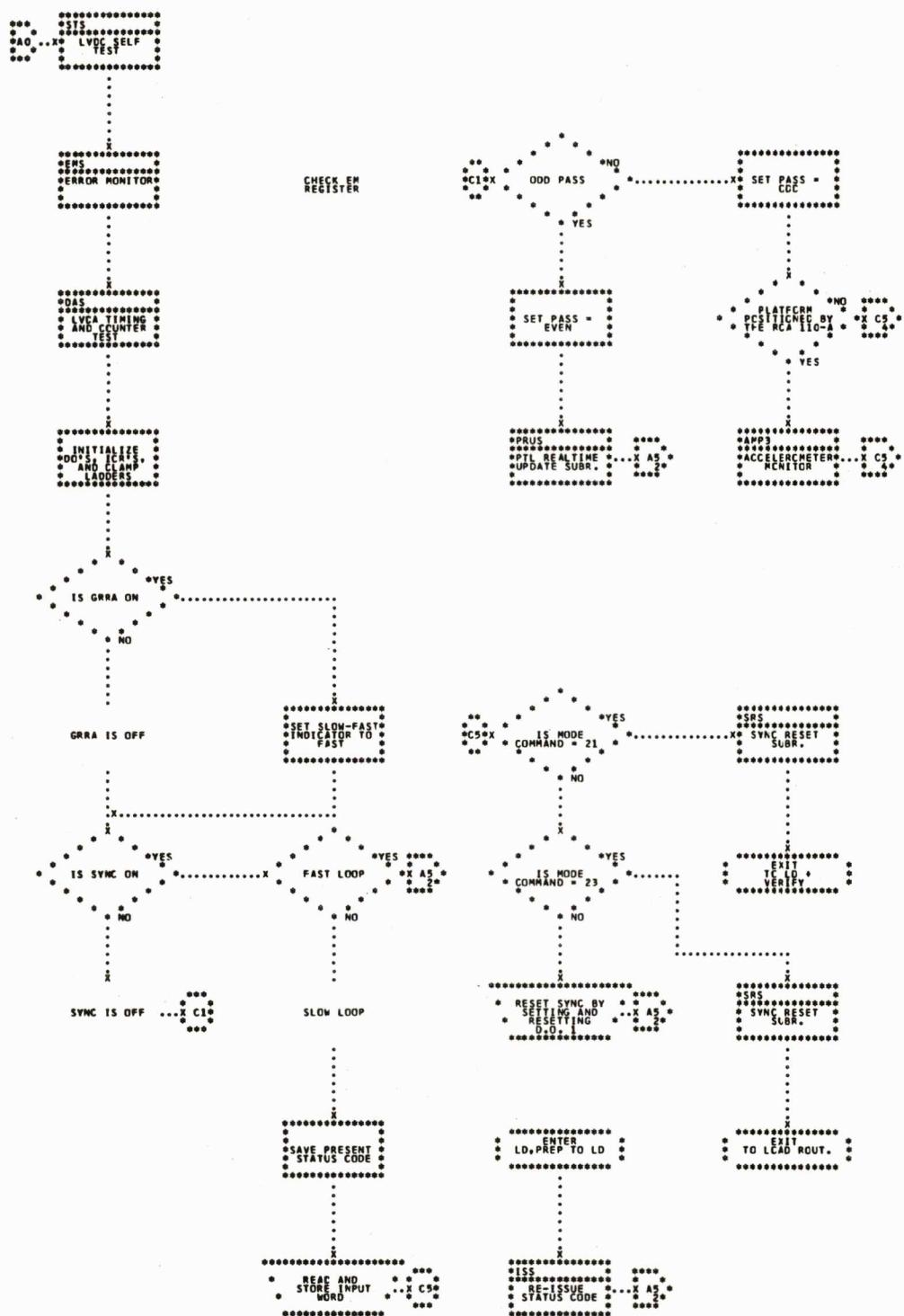


Figure 3-22. (Sheet 5 of 5) Prepare to Launch Routine

3.1.22 Special Loader (Program Restore Routine) (Figure 3-23)

It is the purpose of this routine to provide the overall LVDC/RCA-110A computer system with the capability to:

1. Allow the RCA-110A to restore LVDC Preflight memory after exercising a Simulated Flight with compressed data storage.
2. Provide the RCA-110A with the ability to load advanced LVDC program configurations.

Without the Special Loader's ability to reload memory after running Simulated Flight, it would be necessary to remove the LVDC from the vehicle in order to restore the LVDC Preflight Program.

In order to reduce the RCA-110A programming effort, the Special Loader was specifically designed to be indistinguishable from the normal preflight load and verify routines as far as the RCA-110A was concerned. However, the Special Loader lacks a number of the internal safety checks incorporated in the normal Preflight Load Routine.

The Special Loader is comprised of the following routines:

1. Pseudo Mode Sort
2. Pseudo Verify and Prepare to Load
3. Pseudo Load
4. Pseudo Sector Dump
5. TLC Processor
6. Required Pseudo Subroutines

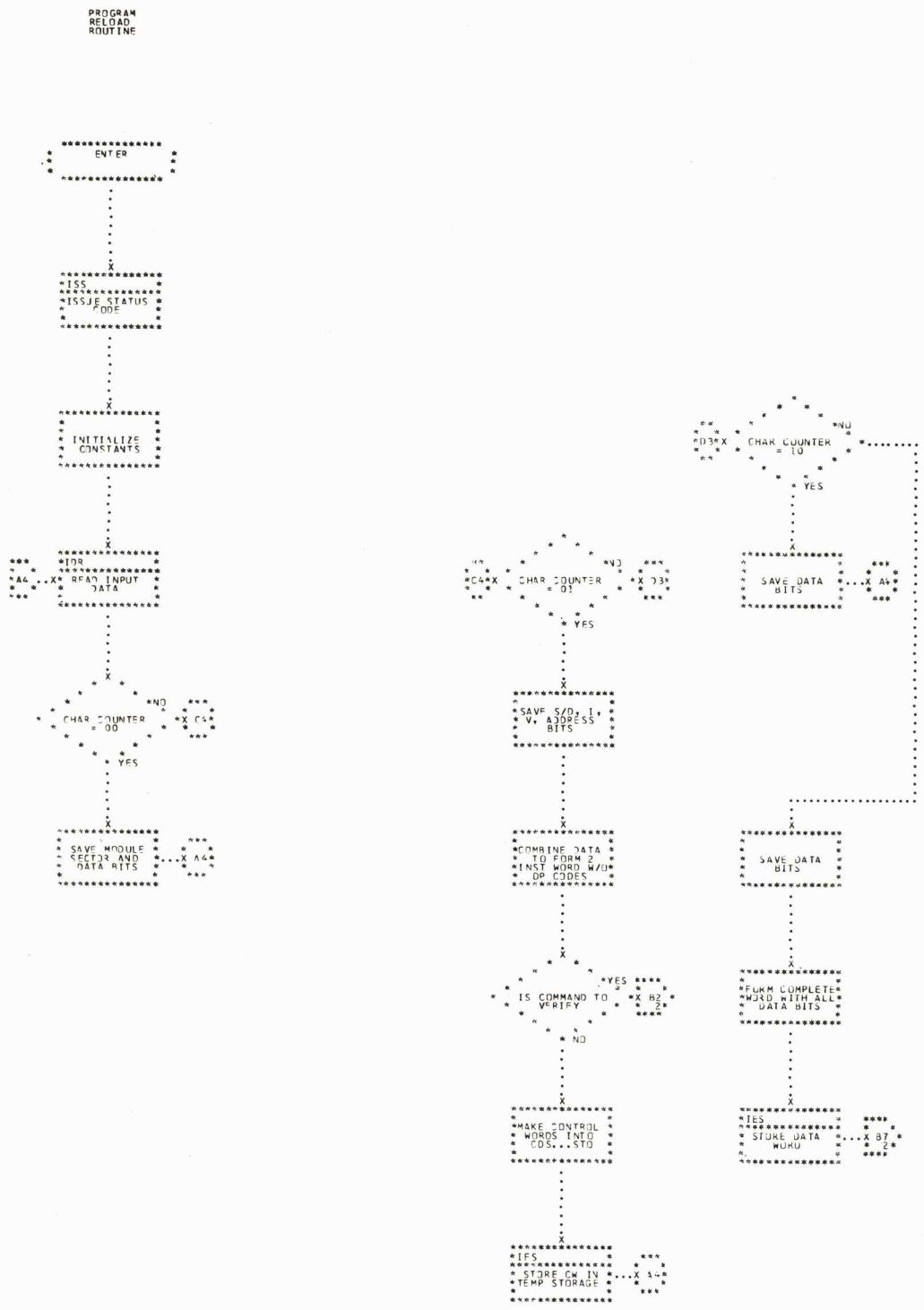


Figure 3-23. (Sheet 1 of 12) Special Loader

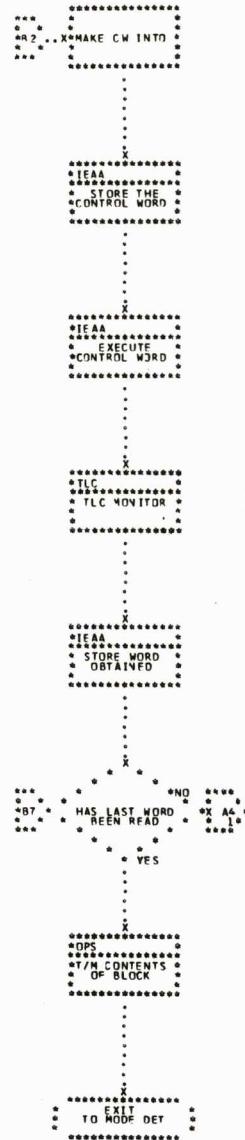


Figure 3-23. (Sheet 2 of 12) Special Loader

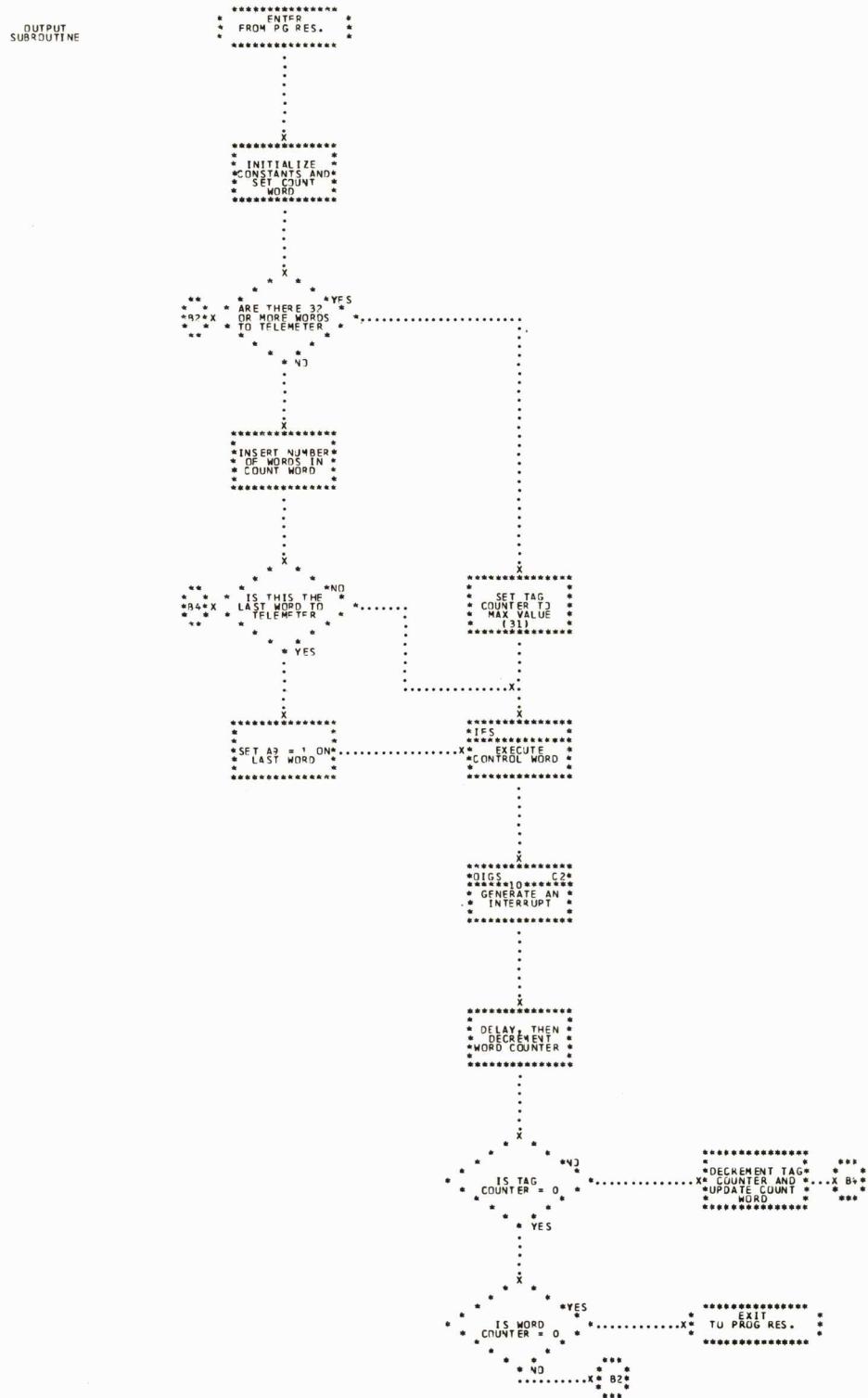


Figure 3-23. (Sheet 3 of 12) Special Loader

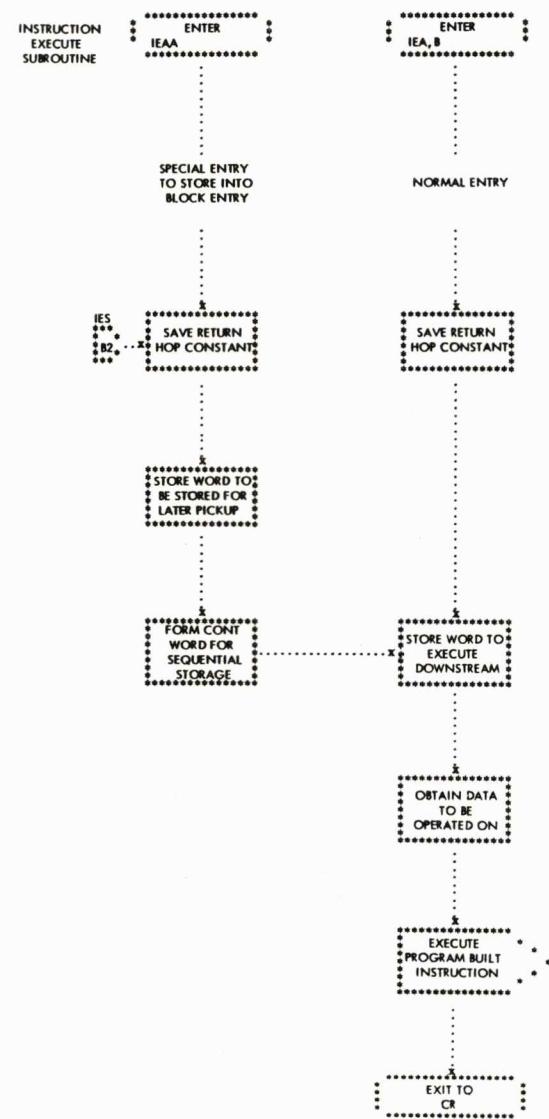


Figure 3-23. (Sheet 4 of 12) Special Loader

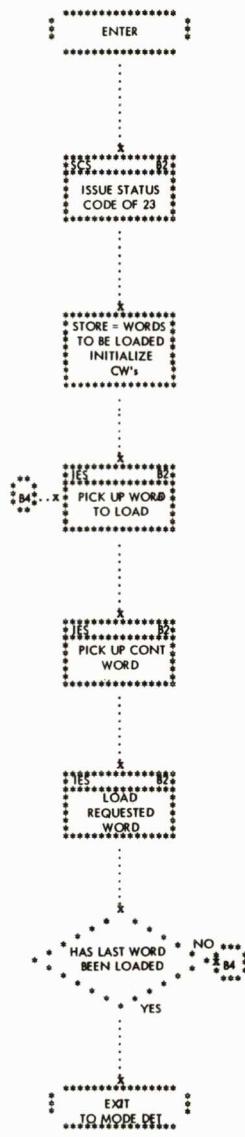


Figure 3-23. (Sheet 5 of 12) Special Loader

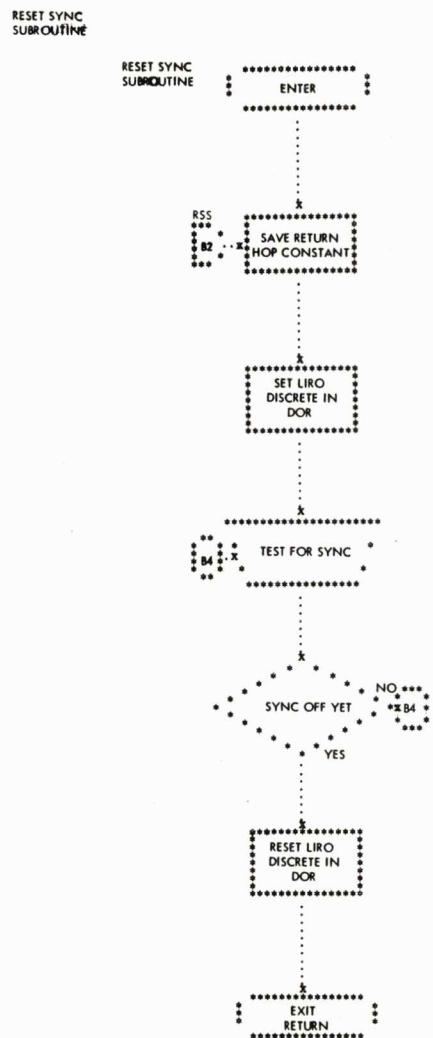


Figure 3-23. (Sheet 6 of 12) Special Loader

STATUS CODE
SUBROUTINE



Figure 3-23. (Sheet 7 of 12) Special Loader

INPUT DATA
READ
SUBROUTINE

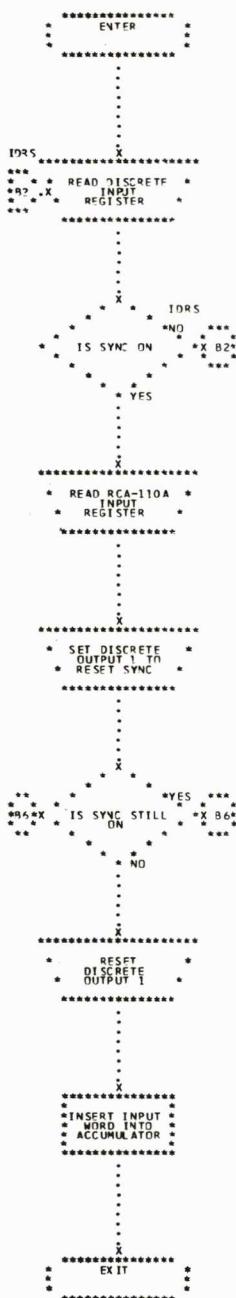


Figure 3-23. (Sheet 8 of 12) Special Loader

MODE
DETERMINING
ROUTINE

```

***** * ENTRY * ****
***** * NORMAL ENTRY * ****
***** * X *****

***** * INHIBIT ALL * ****
***** * INTERRUPTS * ****
***** * EXCEPT TLC * ****
***** * X *****

***** * ISS * ****
***** * ISSUE STATUS * ****
***** * CODE 00 * ****
***** * X *****

***** * SFT MODE * ****
***** * REGISTER = 77 * ****
***** * X *****

***** * INRS R2* ****
***** * INP DATA * ****
***** * READ SURR * ****
***** * X *****

***** * WAIT FOR * ****
***** * SYNC READ * ****
***** * REG, * ****
***** * RESET SYNC * ****
***** * X *****

***** * IS MODE V3 * ****
***** * COMMAND A 20, * ****
***** * 21, OP 23 * ****
***** * X B3 * ****
***** * YES * ****
***** * X *****

***** * EXIT * ****
***** * TO ROSTO PROG * ****

```

Figure 3-23. (Sheet 9 of 12) Special Loader

OUTPUT
INTERRUPT
GENERATE
SUBROUTINE

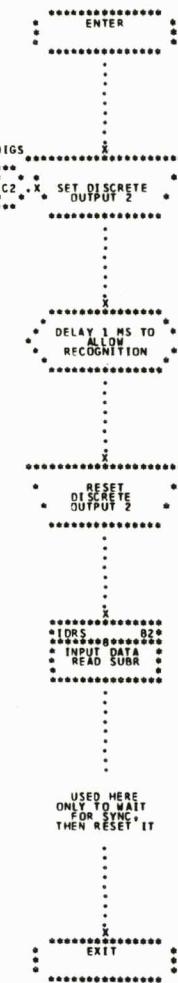


Figure 3-23. (Sheet 10 of 12) Special Loader

```

    * ***** ENTER ***** *  

    * FRONT 400D. *  

    * DATA *  

    * ***** *  

    .  

    .  

    .  

    .  

    X  

    * CCS C2*  

    * ISSUF STATUS *  

    * CODE *  

    * ***** *  

    .  

    .  

    .  

    X  

    * INR *  

    * READ INP JT *  

    * DATA *  

    * ***** *  

    .  

    .  

    .  

    X  

    * PREPARE TO *  

    * DUMP *  

    * SPECIFIED *  

    * SECTOR *  

    * ***** *  

    .  

    .  

    .  

    X  

    * DRT FIRST *  

    * WORD IN SEC *  

    * SECT STORE *  

    * IN TEMP LOC *  

    * ***** *  

    .  

    .  

    .  

    X  

    * TTY *  

    RS X TLC MONITOR  

    * ***** *  

    .  

    .  

    .  

    X  

    * YES *  

    * HAS ENTIRE *  

    * SECTOR BEEN *  

    * DUMPED *  

    * NO *  

    * YES *  

    * HAVE 32 WORDS *  

    * BEEN OBTAINED *  

    * NO *  

    * ***** *  

    * CHANGE FLAG *  

    * TO CAUSE 1941 *  

    * ON LAST *  

    * OUTPUT T/M *  

    * FLAG *  

    * ***** *  

    .  

    .  

    X  

    * DS *  

    * OUTPUT *  

    * SUBROUTINE *  

    * ***** *  

    .  

    .  

    X  

    * DRT NEXT LOC *  

    * OF SEC * PUT *  

    * IN TEMP STOR *  

    * ***** *  

    * X 85 *  

    * ***** *  

    .  

    .  

    .  

    X  

    * D/P SURR *  

    * REFURNS *  

    * DIRECTLY TO *  

    * M.D. WHEN *  

    * DUMP THRU *  

    * ***** *
  
```

Figure 3-23. (Sheet 11 of 12) Special Loader

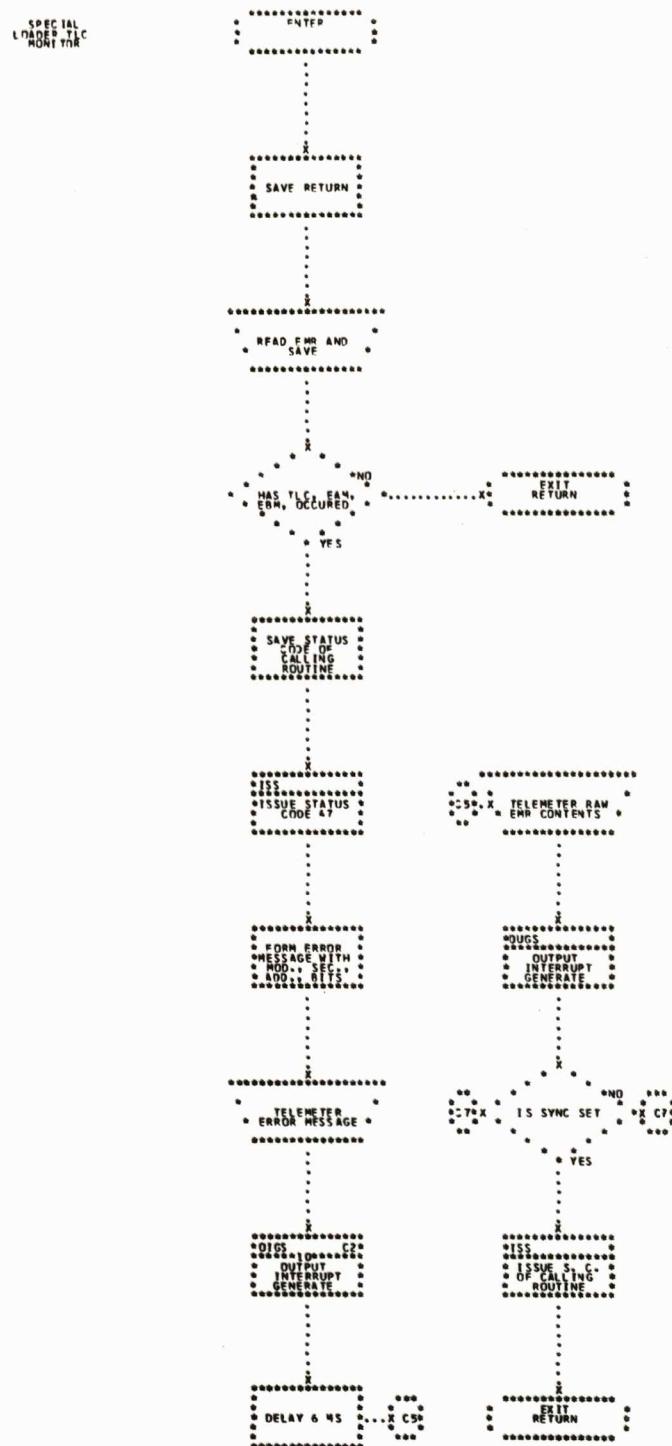


Figure 3-23. (Sheet 12 of 12) Special Loader

3.1.23 Telemetry Test Routine (Figure 3-24)

The purpose of the Telemetry Test Routine is to provide the capability to check the telemetry system by outputting LVDC and DOM telemetry using computer telemetry rates specified in the routine input word.

The entry to this routine is commanded through the Mode Sort Routine. This routine requires one input data word, having the following format:

S	1	2	3	4	5	6	7	8	9	10	11	12	13
M/D													
	M	A	B	C	D	E	F	0	0	0	0	0	0

where

M/D = mode / data bit (=0 for data)

M = 0, run the specified rate until terminated by
an RCA-110A interrupt

= 1, run rates A through E for a period of three
minutes each

and if M=0, the following bits will cause delays of:

A - 4.183 milliseconds between computer telemetry PIO's

B - 4.347 milliseconds between computer telemetry PIO's

C - 4.511 milliseconds between computer telemetry PIO's

D - 8.285 milliseconds between computer telemetry PIO's

E - 8.94 milliseconds between computer telemetry PIO's

F - this rate is not fixed and may be loaded by means of
Verify and Prepare to Load Routine prior to the
commanding of this routine

If the input bit M is set =1, the routine will exit to the Mode Sort Routine upon completion. If the input bit M is set = 0, as when only one rate is to be used, the only exit from the routine is from the RCA-110A interrupt, which causes an exit to the Forced Begin Routine.

Also, if the M bit is set =1, the rate word will be telemetered at the beginning of each rate change and at the start of the first rate generation period.

Refer to Appendix B for PIO Tags used in this routine.

The DOM PIO data is the Switch Selector Registers' Feedback contents, which provides the desired pattern. The DOM is filled at the start of the test, at the start of each rate change, and one DOM word is issued with each computer telemetry word generated.

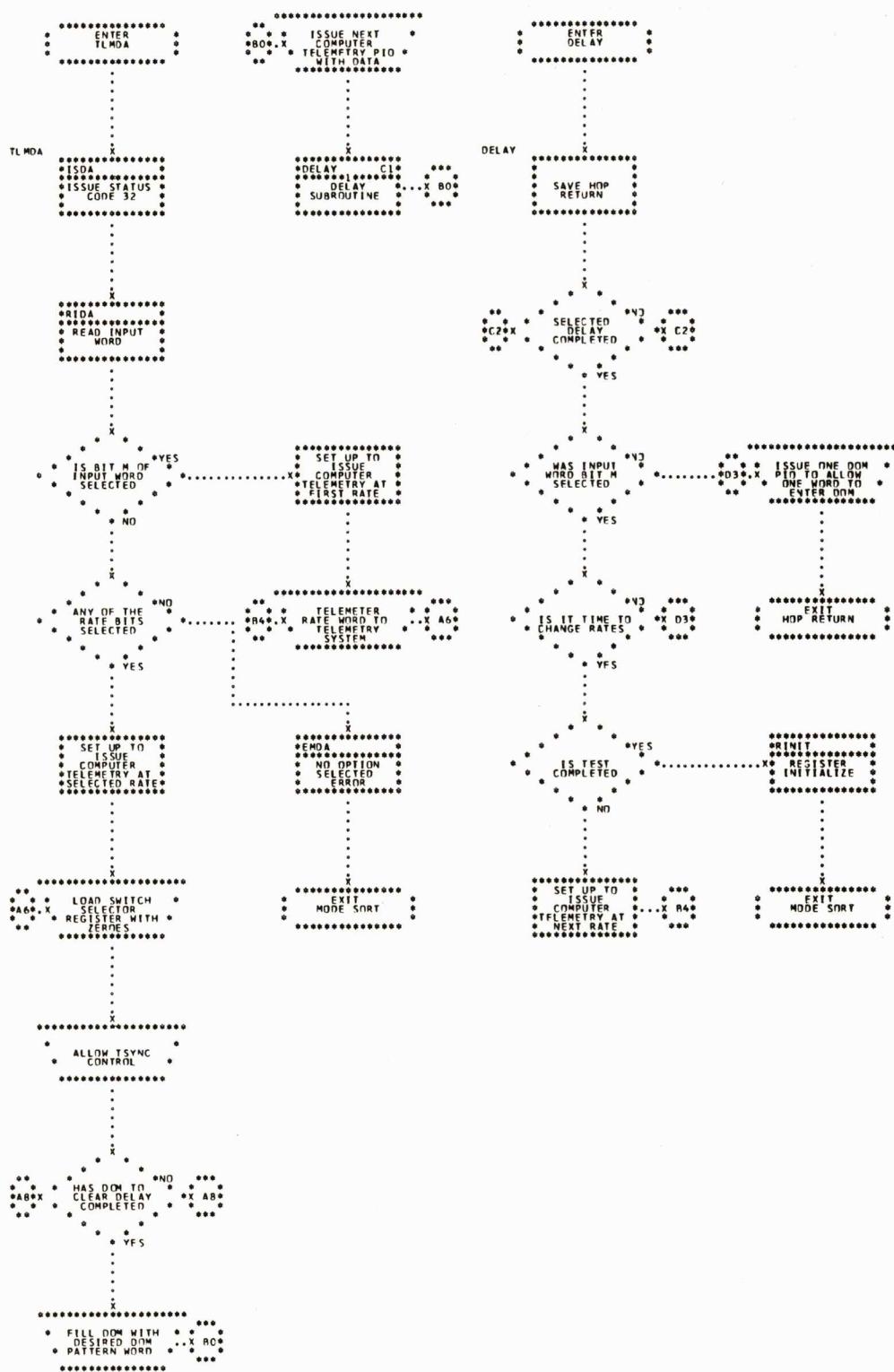


Figure 3-24. Telemetry Test Routine

3.1.24 Command Receiver Linkage (Figure 3-25)

The purpose of this routine is to provide the necessary program linkage for direct access to the Flight Program's Command Receiver Program during prelaunch testing.

When the program is called by the launch computer, necessary Preflight communications are established, T-SYNC DOM control is selected, the Command Receiver Interrupt is reset, and the Flight Program is entered.



Figure 3-25. Command Receiver Linkage Routine

3.1.25 Repeatable Flight Sim Linkage Routine (Figure 3-26)

The purpose of this routine is to provide the capability to execute the Flight Program in its Repeatable Flight Sim Mode.

When the program is called by the launch computer, the program will supply the necessary Preflight communications to allow control, select T-SYNC DOM control, and then exit directly to the Flight Program.

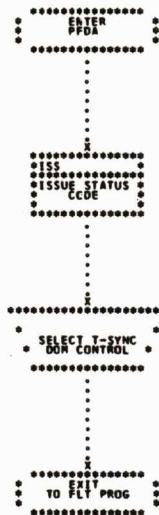


Figure 3-26. Repeatable Flight Sim Linkage Routine

3.1.26 S-IB Targeting Dump Routine (Figure 3-27)

The purpose of this routine is to provide the necessary program linkage to allow direct access to the S-IB Flight Program during Prelaunch testing. When this program is called by the launch computer in a Saturn IB environment, necessary Preflight communications are established, T-Sync DOM control is selected, command receiver interrupt is reset, the Flight program is entered, and an automatic dump of targeting parameters is performed. After the dump is completed, control is returned to the Preflight program where ICRs 1 and 9 are set, and the routine exits to Mode Sort.

```
*****  
*      ENTER      *  
*      SIBTDA     *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*ISSUE      *  
*****  
*ISSUE STATUS *  
*      CODE      *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*      RESET ICR 1    *  
*          TO ALLOW   *  
*      TSYNC ROM    *  
*          CONTROL   *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*      RESET ORBITAL  *  
*          LINKAGE   *  
*      INTERRUPT    *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*FLTPGM      *  
*****  
*TARGETING    *  
*      DUMP      *  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*      SET ICR'S 1    *  
*          AND 9      *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*      RESTORE      *  
*      NORMAL       *  
*      INTERRUPT    *  
*      INHIBITS     *  
*****  
*          .  
*          .  
*          .  
*          .  
*          .  
*          .  
*          X  
*****  
*      EXIT        *  
*      TO MODE SORT *  
*          .
```

Figure 3-27. S-IB Targeting Dump Routine

Change 2

3.2 SUBROUTINES

3.2.1 Read Input Data Subroutine (Figure 3-28)

It is the purpose of the Read Input Data Subroutine to handle data sent to the LVDC/LVDA via the fourteen RCA-110A input lines.

When program control is transferred to the Read Input Data Subroutine, the LVDC examines the Sync discrete; if Sync is off (0), the LVDC loops through the Real Time Delta Subroutine. If the Sync bit is not set within 256 seconds of entry, the LVDC issues an overtime status code and continues cycling. When the Sync bit is set (1), the LVDC reads the fourteen input lines, resets Sync, and examines the Mode/Data Bit. If the Mode/Data Bit indicates mode information, an error has occurred and the LVDC transfers to the Error Monitor Subroutine and then to either the Prepare to Launch Routine, or to the Mode Sort Routine. If the Mode/Data Bit indicates data information, the LVDC transfers control to the calling program with the fourteen bit data word in the accumulator. If necessary, the status code of the calling program is re-established before the return is made.

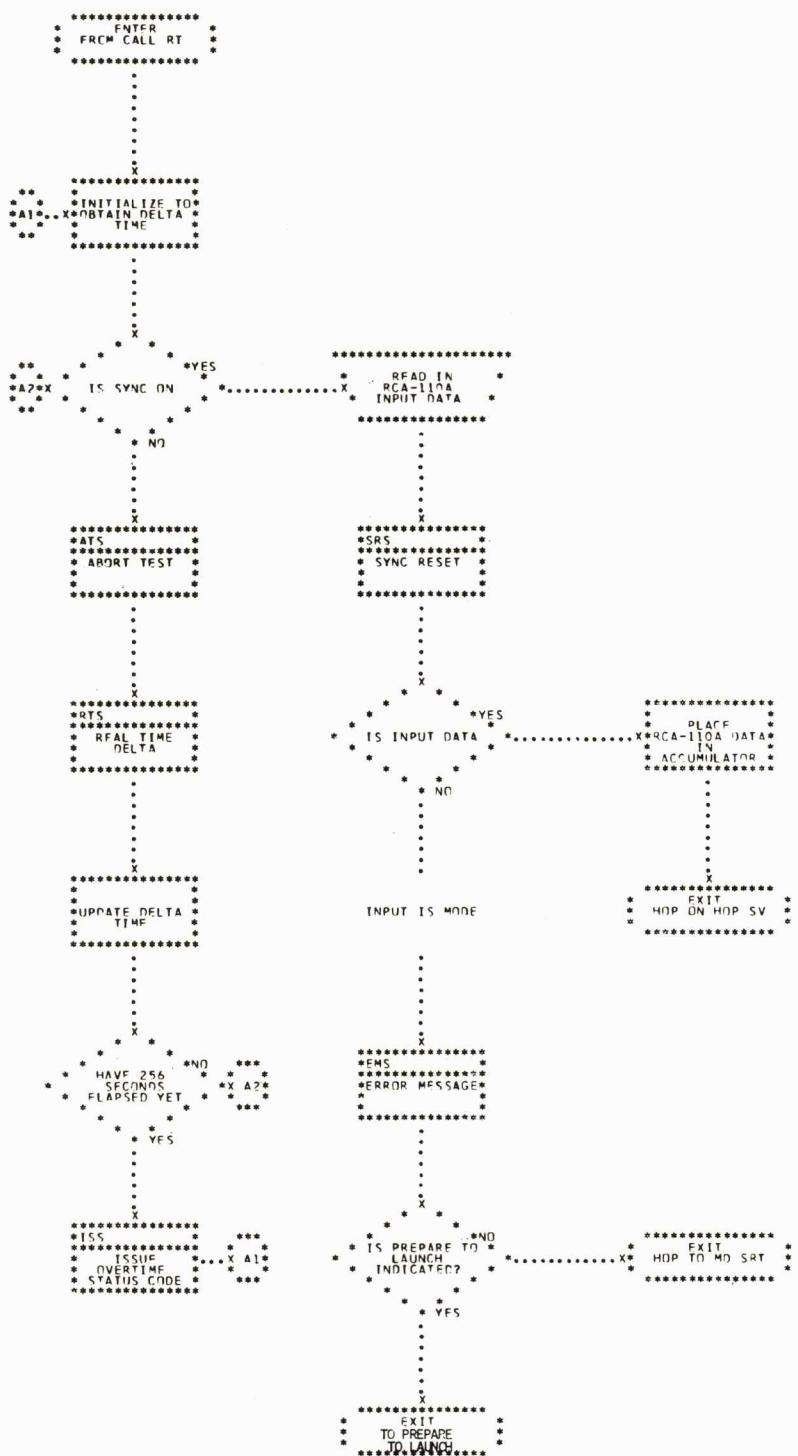


Figure 3-28. Read Input Data Subroutine (RIS)

3.2.2 Sync Reset Subroutine (Figure 3-29)

The purpose of this subroutine is to turn off the RCA-110A SYNC signals to the LVDC. This will be accomplished by setting Discrete Output 1, which causes the SYNC logic to be reset. The LVDC will then cycle waiting for the SYNC input to reset. When SYNC is reset and found off, the LVDC will return to the calling routine.

```
*-----*  
*      ENTER      *  
*-----*  
  
*-----*  
*      SET DISCRETE    *  
*      OUTPUT 1       *  
*-----*  
  
*-----*  
*      IS SYNC OFF    *  
*      YES           *  
*      NO            *  
*-----*  
*-----*  
*      RESET          *  
*      DISCRETE        *  
*      OUTPUT 1       *  
*-----*  
  
*-----*  
*      PRUS           *  
*-----*  
*      RET TO CAL RT  *  
*-----*
```

Figure 3-29. Sync Reset Subroutine

3.2.3 Error Monitor Subroutine (Figure 3-30)

The purpose of this subroutine is to interrogate the contents of the Error Monitor Register, and to output error messages when an error is detected during the performance of a Preflight routine. This subroutine has two modes of operation.

First, the subroutine is entered periodically as part of the Mode Sort self-test loop and the Prepare to Launch self-test loop. The Error Monitor Register and Discrete Input Spares Register are tested for the occurrence of a Switch to Converter B (SCB). The Error Monitor Register is also checked for unexpected bits. If either test detects an unexpected condition: the Error Monitor status code is telemetered, DO 13 is set (if entry was from Prepare to Launch), the contents of the EMR is telemetered, and the LVDC enters a loop to wait for Sync.

The second mode of operation is used when an error is found during the performance of a commanded routine. When such an error is detected, this subroutine: selects G-Sync DOM control; sets DO 13 (if entry was from Prepare to Launch); telemeters the error message without the usual RCA-110A communications (if there is no error message and the EMR is non-zero, the EMR is telemetered instead of an error message); issues the Error Monitor status code; telemeters the error message from the specific routine wherein the error occurred; telemeters the contents of the Error Monitor Register; and then loops to wait for Sync. The error message provides a means of determining the exact nature of the error.

On detection of any of the following errors, the contents of the register which indicates the error condition is telemetered along with the EMW, in lieu of the normal EMR telemetry. This data is sent, using the EMR telemetry PIO 701, by the Error Monitor Subroutine. If a valid EMR bit is set, the contents of the EMR are telemetered on the next pass through the Error Monitor Subroutine.

<u>Error Message Word (EMW)</u>	<u>Routine</u>	<u>Error Description</u>
001	Mode Sort	Incorrect mode command - data rather than mode in the RCA-110 A input register.
451	Read Input Data Subroutine	Incorrect data word - mode rather than data in the RCA input register.
121	Prepare to Launch	Unacceptable bit(s) in the Interrupt Register.

<u>Error Message Word (EMW)</u>	<u>Routine</u>	<u>Error Description</u>
122	Prepare to Launch	Unacceptable bit(s) in the Discrete Input Register.
123	Prepare to Launch	Unacceptable bit(s) in the Discrete Input Spares Register.

Recognition of the Error Monitor status code causes the launch computer to issue Sync after it has analyzed the telemetered outputs. When the LVDC recognizes Sync, a check is made to determine if the subroutine was entered from Prepare to Launch. If so, Sync is reset and the exit is to Prepare to Launch. Otherwise, it will read the RCA-110A Input Register and reset Sync. If the Input Register is not equal to either a zero or a mode word of 77, the LVDC returns to Mode Sort, and waits for Sync. If the Input Register is equal to zero, the LVDC re-establishes the proper status code, and executes a return to the calling routine. If the Input Register is equal to the 77 mode word, the LVDC sets its Error Monitor Register mask word to ignore all errors except EAM, EBM, and TLC, and exits to the Forced Begin Routine.

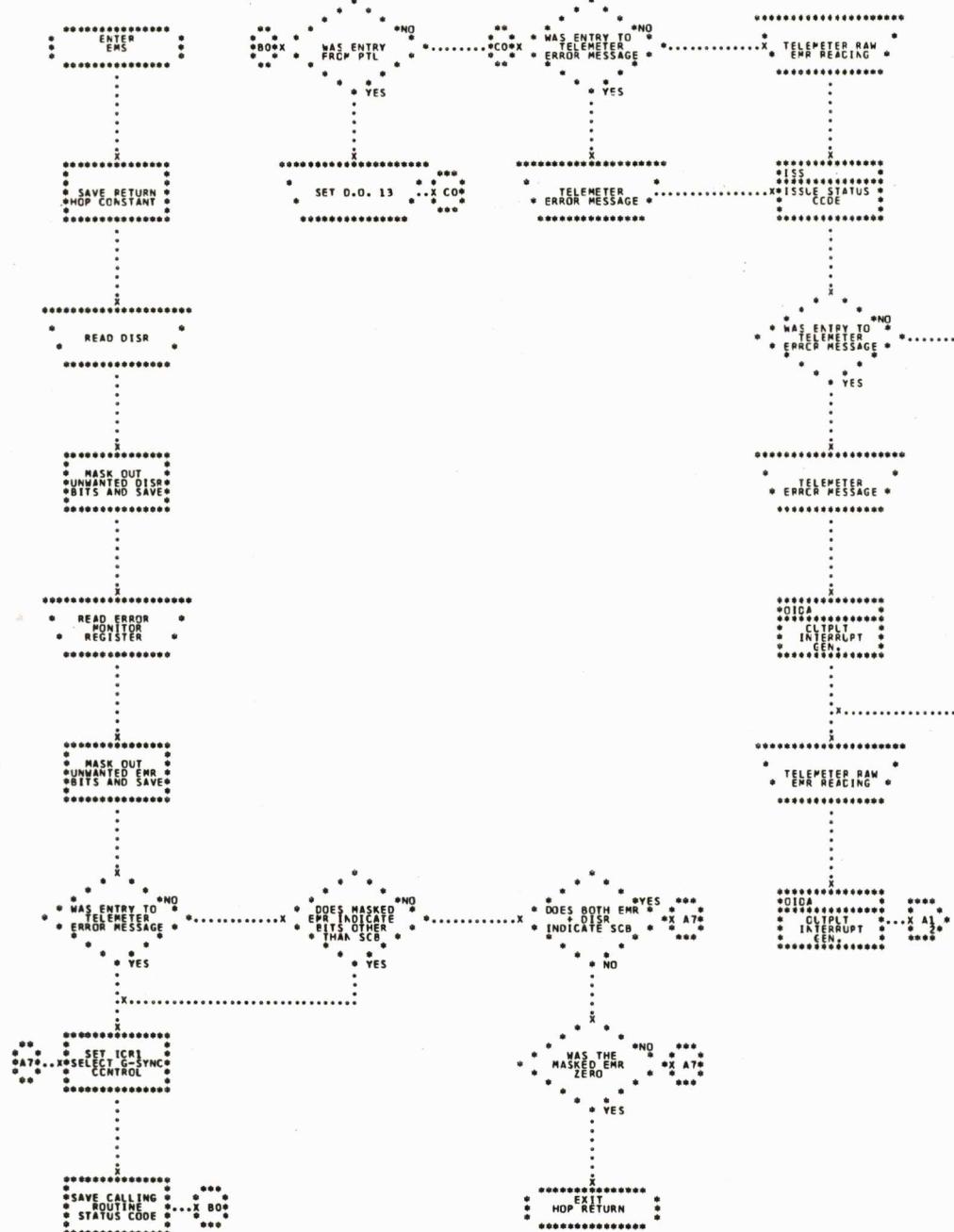


Figure 3-30. (Sheet 1 of 2) Error Monitor Subroutine

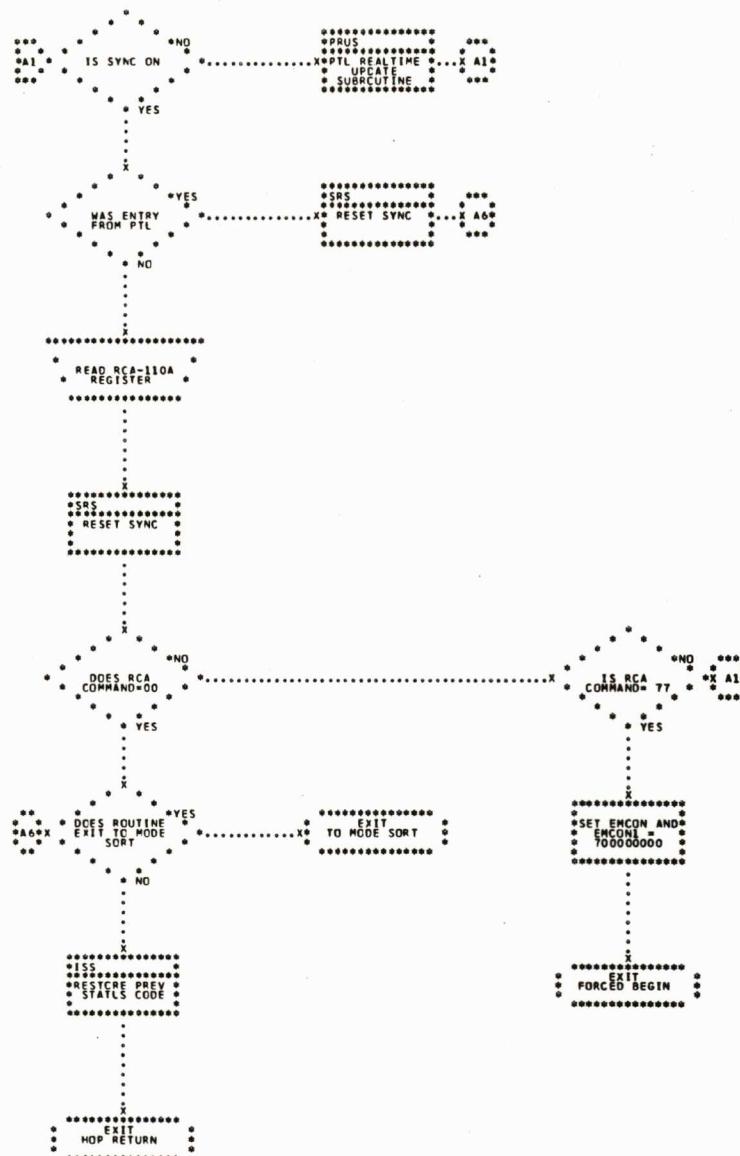


Figure 3-30. (Sheet 2 of 2) Error Monitor Subroutine

3.2.4 Issue Status Code Subroutine (Figure 3-31)

The function of this subroutine is to telemeter the Status Code of the current routine, load the Mode Register, and interrupt the RCA-110A by issuing DO 2. SYNC is then received from the RCA-110A and reset by the Sync Reset subroutine. A delay of 6 ms. is utilized to insure the Sync signal has been reset and control is returned to the calling routine.

```
ISSUE STATUS
CODE
SUBROUTINE

*****+
*   ENTER    *
* FROM CAL ROUT    *
*****+
.
.
.
ISS X *****
*   TELEMETED    *
* PRESENT    *
* STATUS CODE    *
*****+
.
.
.
X *****
*   PRESENT    *
* STATUS CODE    *
* IN THE MODE    *
* REGISTER    *
*****+
.
.
.
X *****
ENTGS +
*   GENERATE    *
*   OUTPUT    *
*   INTERRUPT    *
*****+
.
.
.
X
+-----+
| EXIT      |
| RET TO CAL RT |
+-----+
```

Figure 3-31. Issue Status Code Subroutine

3.2.5 Output-Interrupt Generate Subroutine (Figure 3-32)

The purpose of this subroutine is to provide an interrupt after certain computer telemetry operations. The computer telemetry operations which do not result in an interrupt are identified in Section 2.

After issuing the interrupt (DO 2) to the launch computer, this subroutine waits 1 ms. for the SYNC signal from the launch computer. When SYNC is detected, the subroutine issues SYNC reset and returns to calling routine.

OUTPUT
INTERRUPT
GENERATE
SUBROUTINE

```
***** ENTER ****
* FROM CAL ROUT *
*****
*
*
*
***** PRUS ****
* DTL REALTIME *
* UPDATE SUBR. *
*****
*
*
*****
* SET DISCRETE *
* OUTPUT NUMBER *
* 2 *
*****
*
*
X
*****
* NO *
* HAS 1 MS *
* ELAPSED *
* R4 *
*****
* YES *
*****
X
*****
* PESY *
* DISCRETE *
* OUTPUT NUMBER *
* 2 *
*****
*
*
X
*****
* NO *
* IS SYNC ON *
* DISCRETE ON *
* X HAS *
*****
* YES *
*****
X
*****
SRS
SYNCH RESET
SUBROUTINE
*****
*
*
*****
* EXIT *
* RET TO CAL RT *
*****

```

Figure 3-32. Output-Interrupt Generate Subroutine

3.2.6 Instruction Execute Subroutine (Figure 3-33)

LVDC programming standards require that the instructions for a given routine and the accompanying data words be stored in different sectors. It is, therefore, impossible to execute program-built and modified instructions without first changing the current data sector to the current instruction sector. The Instruction Execute Subroutine provides a quick and efficient means to execute these program-built instructions.

This program has the capability of executing one or two program-built instructions and operating upon one data word. To execute two instructions, the input format is:

1. First instruction to be executed in accumulator Syllable 1.
2. Second instruction to be executed in accumulator Syllable 0.
3. Data word, if any, in the PQ register.

To execute a single instruction, the input format is:

1. Instruction to be executed in accumulator Syllable 0.
2. Data word, if any, in the PQ register.

The subroutine returns to the calling program after the instruction(s) is executed.

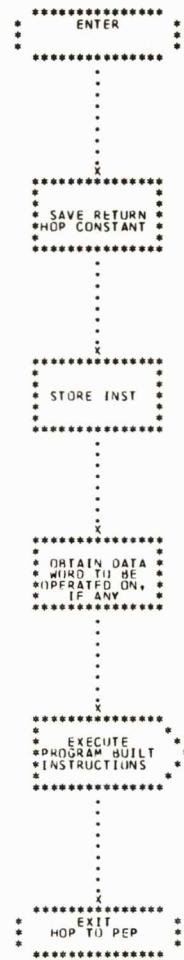


Figure 3-33. Instruction Execute Subroutine

3.2.7 CW Execute Subroutine (Figure 3-34)

The CW Execute Subroutine is called by the Load Routine and by the verify mode of the Verify and Prepare to Load Routine.

When used by the Load Routine, this subroutine loads the data prepared by the Verify and Prepare to Load Routine, into the memory locations specified by the control words what were also prepared in that program.

When called by the verify portion of the Verify and Prepare to Load Routine, the CW Execute Subroutine uses the previously prepared control words to obtain the required information from memory. This subroutine utilizes the Instruction Execute Subroutine, to verify or load LVDC memory.

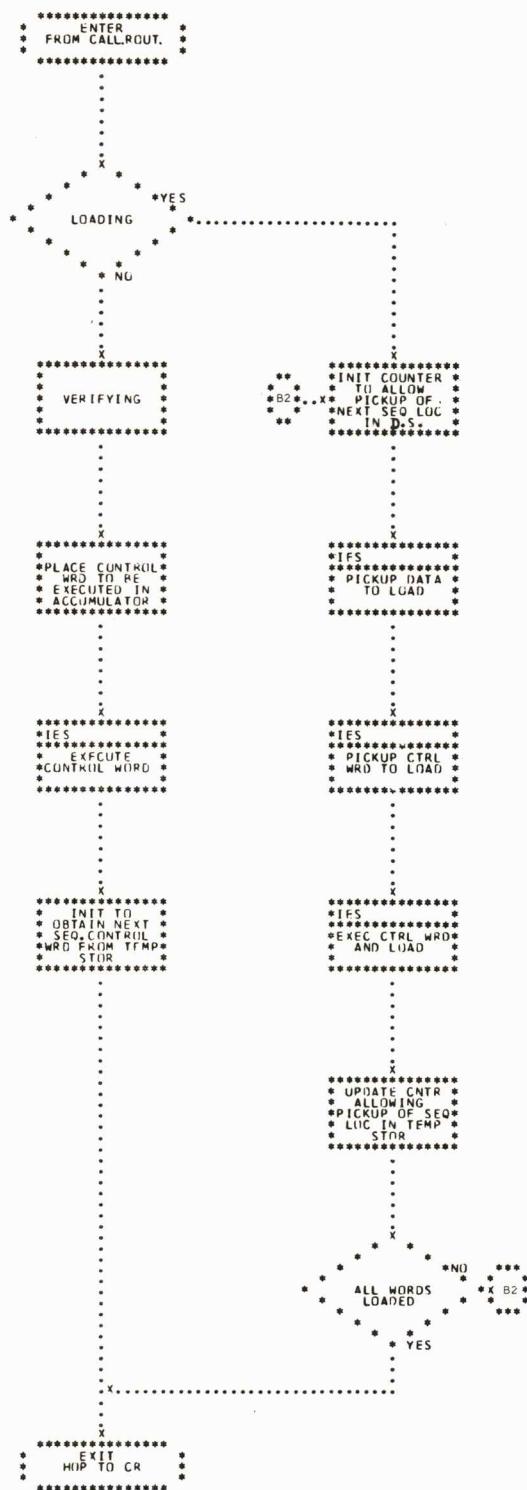


Figure 3-34. CW Execute Subroutine

3.2.8 Accelerometer Monitor Subroutine (Figure 3-35)

This subroutine provides a continual monitor of the output of the three platform accelerometers. A time interval accuracy of one second is required for the downrange and crossrange accelerometers and a time interval accuracy within 410 microseconds per pulse is required for the vertical accelerometer. This data (time and pulse count) will be used to calculate the percentage error for the vertical accelerometer and the degrees off level for the downrange and crossrange accelerometers. The information must be processed, displayed, and updated by the SLCC Monitor Program frequently enough to provide a realistic indication of platform accelerometer performance. In order to provide this facility, the Accelerometer Monitor Subroutine is incorporated into the Mode Sort test loop.

The monitor of all accelerometers will be performed once each time through this loop at a nominal interval of one second, or less, up to the detection of Guidance Reference Release Alert discrete. The basic equations solved by the LVDC are the following:

$$\frac{Vd, v, c - Kd, v, c}{Td, v, c} . Cd, v, c = Ed, v, c$$

Where: $Vd, v, c = [Vd, v, c \text{ (present)} - Vd, v, c \text{ (previous)}]$ accumulated velocity in pulses

$T = [T \text{ (present)} - T \text{ (previous)}]$ accumulated time

$Kd, Kc = F \text{ (Earth's Rate, Latitude, Scale Factor and Azimuth)}$

$Kv = F \text{ (Earth's Rate, Scale Factor, and Gravity)}$

$Cd, Cc = F \text{ (Gravity and Scale Factor)}$

$Cv = F \text{ (Earth's Rate, Gravity and Scale Factor)}$

$d, v, c = \text{downrange, vertical, crossrange}$

The monitor function will not be performed while executing commanded programs. Upon returning to the Mode Sort Routine, the Accelerometer Monitor function will be reinitialized and accelerometer updating will be resumed.

A data word will be telemetered on every pass through the Mode Sort loop whether or not there has been an update of the data. This will allow the RCA-110A monitor program to operate asynchronously with the output from the LVDC.

The single uniquely-identified data word will contain the off-level information for all three axes. The downrange and crossrange axis terms will be composed of nine bits each (one polarity, eight magnitude), and the vertical axis term of eight bits (one polarity, seven magnitude).

S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
S	d	d	d	d	d	d	d	d	S	c	c	c	c	c	c	c	S	v	v	v	v	v	v	v	

Where: S = Sign of error term

 d, v, c = Magnitude of error

This LVDC telemetry word is not accompanied by an interrupt to the RCA-110A computer. The initial message from the LVDC will be all "ones" in the magnitude bits, and will remain in this condition until sufficient data are gathered to make the first computations. In this case, the ground monitor program will indicate that the data are invalid when the all "ones" message exists in any (or all) axes. The following are special codes employed in the telemetry word:

- 376 - (vertical) initial message
- 374 - (vertical) accelerometer is inoperative
- 372 - (vertical) scaling limit was exceeded
- 370 - (vertical) this is the maximum valid error count
- 377 - (downrange, crossrange) initial message
- 376 - (downrange, crossrange) this is the maximum valid error count

A capability exists to allow the launch computer to completely bypass the monitor function.

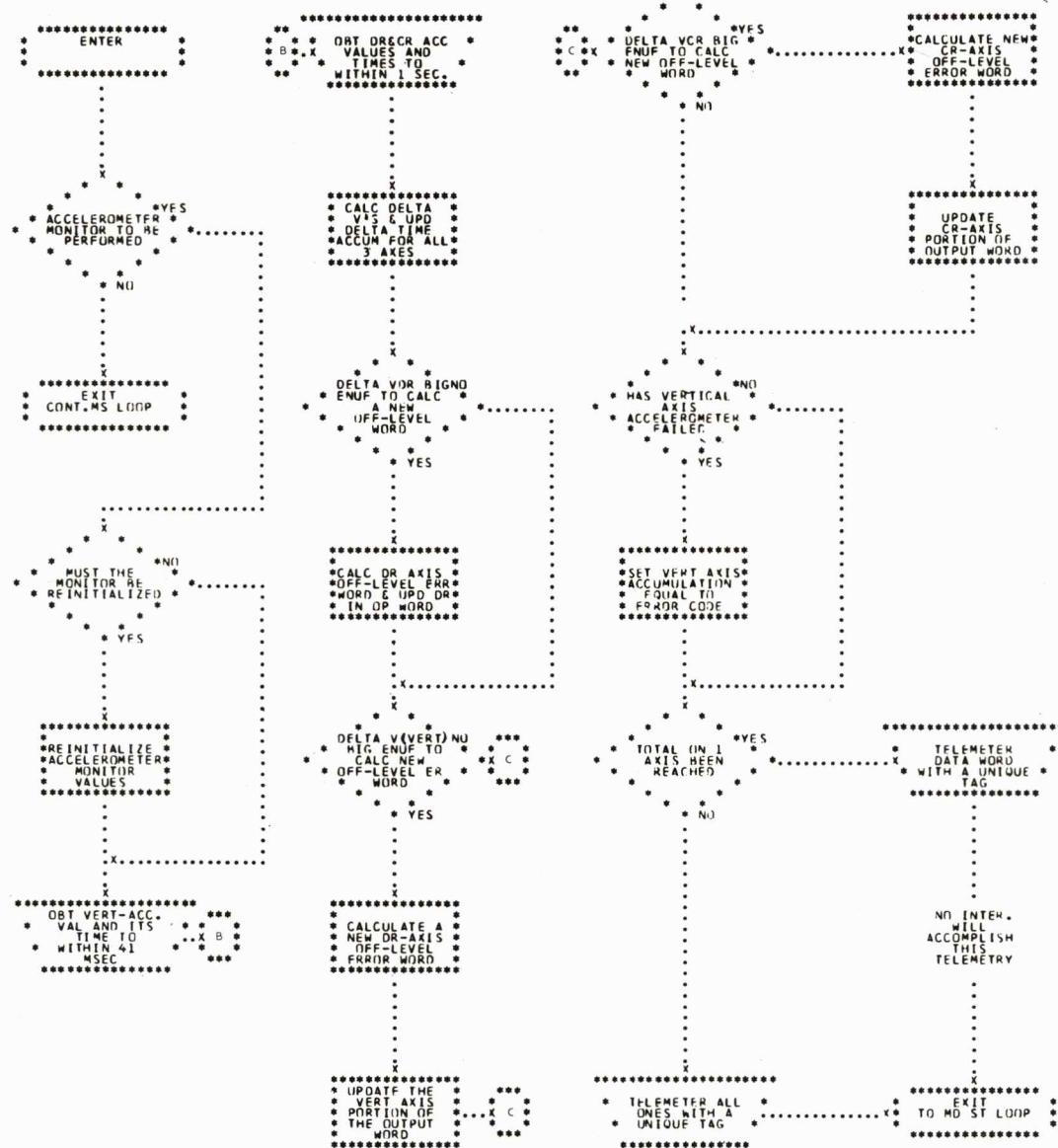


Figure 3-35. Accelerometer Monitor Subroutine

3.2.9 Resolver Error Subroutine (Figure 3-36)

The purpose of this subroutine is: (a) to determine the reason for the occurrence of the disagreement bit in the duplexed gimbal angle resolver reading if it has not been caused by the counters passing through zero and (b) to place one of eight possible coded error messages in temporary storage to be telemetered at a later time by the Error Monitor Subroutine.

The subroutine is called by the Gimbal Angle Monitor Routine. The routine starts the COD counters (PIO 217), delays for 7.5 ms., then stops the COD counters (PIO 377) and tests the A and B counters against a predetermined expected value. If the difference between the counters is within ± 5 bits, the counter reading is considered valid. The format of the duplexed COD values brought into the accumulator is as follows:

S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	0	0	0	B	B	B	B	B	B	B	B
<u>B</u>																									

D Bit position of the disagreement bit.
B

A Position of the values in the A Counter.

B Position of the values in the B Counter.

The condition of the A Counter, the B Counter, and the disagreement bit, as determined in the test, are placed in temporary storage and the subroutine returns to the Gimbal Angle Monitor Routine which uses that message to prepare an error word for transmission in the Error Monitor Subroutine.

The eight possible error messages are:

- | | | | |
|----|----------------|----------------|--------------------------|
| 1. | Counter A good | Counter B good | Disagreement bit set |
| 2. | Counter A good | Counter B good | Disagreement bit not set |
| 3. | Counter A good | Counter B bad | Disagreement bit set |
| 4. | Counter A good | Counter B bad | Disagreement bit not set |
| 5. | Counter A bad | Counter B good | Disagreement bit set |
| 6. | Counter A bad | Counter B good | Disagreement bit not set |
| 7. | Counter A bad | Counter B bad | Disagreement bit set |
| 8. | Counter A bad | Counter B bad | Disagreement bit not set |

```

***** ENTER *****  

* FROM GAMR *
*****  

*****  

* START CUD *  

* COUNTERS *  

*****  

*****  

* DELAY A KNOWN *  

* TIME *  

*****  

*****  

* STOP CUD *  

* COUNTERS *  

*****  

*****  

* SAVE *  

* CONDITION OF *  

* DISAGREEMENT *  

* R *  

*****  

*****  

* SAVE COUNTER *  

* A VALUE *  

*****  

*****  

* SAVE COUNTER *  

* B VALUE *  

*****  

*****  

* DETERMINE *  

* CONDITION OF *  

* A COUNTERS A *  

* COUNTER, D.H. *  

*****  

*****  

* PLACE ERROR *  

* MESSAGE IN *  

* TEMPORARY *  

* STORAGE *  

*****  

*****  

* FIX *  

* RET TO GAMR *  

*****

```

Figure 3-36. Resolver Error Subroutine

3.2.10 Real Time Update Subroutine (Figure 3-37)

It is the purpose of this subroutine to provide a means to accumulate elapsed time for the LVDC Prepare To Launch Routine. If entry is from any other Routine, no time will be accumulated.

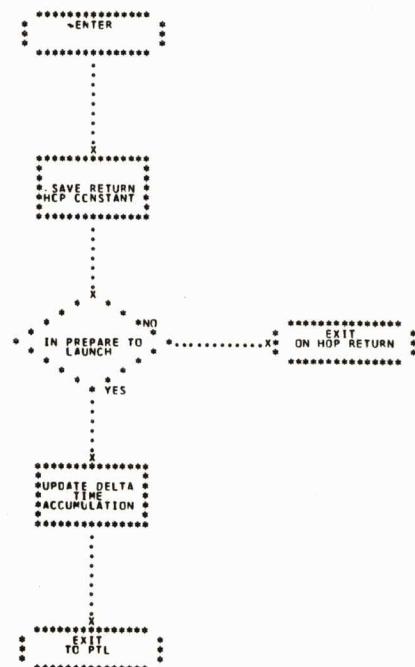


Figure 3-37. Real Time Update Subroutine

3.2.11 Register Initialize Subroutine (Figure 3-38)

The purpose of the Register Initialize Subroutine is to guarantee that the Switch Selector Register, Discrete Output Register, Internal Control Register, Ladder Output Register, and the ladder converter are at their proper condition during either Power Up, or a commanded recycle through Forced Begin from an RCA-110A Interrupt.

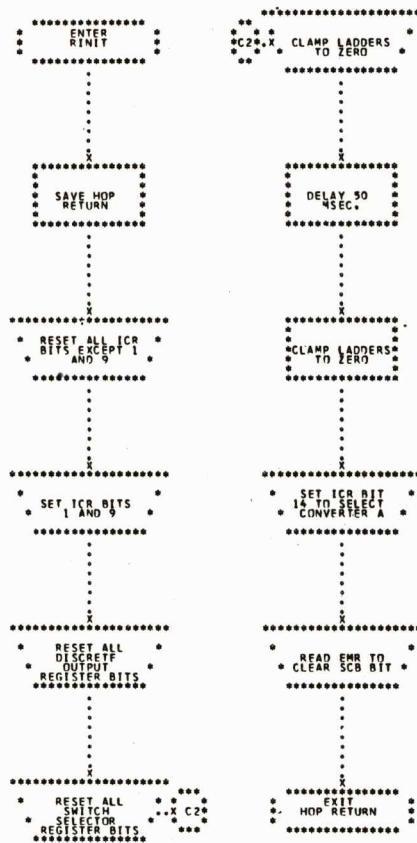


Figure 3-38. Register Initialize Subroutine

3.2.12 Real Time Delta Subroutine (Figure 3-39)

The purpose of the Real Time Delta Subroutine is to provide a current value of real time and a delta time value. The delta time is the difference between the current time and the last value of real time that was read in this subroutine. Upon entry, the last reading of real time is present in the PQ Register. Upon return to the calling program, the current real time reading is in the PQ register, and the delta value is in the accumulator.

```

***** ENTER ****
*
*          X
*
***** SAVE RETURN ****
***** HOP CONSTANT ****
*
*          X
*
***** SORT PREV DET ****
***** VALUE OF REAL ****
***** TIME FRM PQ ****
***** VALUE ****
*
*          X
*
***** OBTAIN ****
***** CURRENT VALUE ****
***** OF REAL TIME ****
***** AND FORM ****
***** DELTA TR. ****
*
*          X
*
***** PUT CURRENT ****
***** REAL TIME IN ****
***** PQ REGISTER ****
*
*          X
*
***** PUT DELTA ****
***** TIME IN ****
***** ACCUMULATOR ****
*
*          X
*
***** EXIT ****
***** HOP TO CR ****

```

Figure 3-39. Real Time Delta Subroutine

3.2.13 LVDC Self Test Subroutine

The LVDC Self Test Subroutine consists of the internal verification of the LVDC control and arithmetic logic through the comparison of test solutions with known results. The subroutine verifies the following:

1. Transfer operations, the transfer register and address register, and syllable, address, sector, and module selection.
2. Arithmetic operations including CLA, ADD, SUB, RSU, XOR, SHF, STO and their associated logic.
3. Multiply and divide operations with various combinations of multipliers, multiplicands, divisors, and dividends.
4. The X and Y memory addressing in each module.
5. Execute modified operations with various combinations of object instruction locations, data sectors, syllables, A4 and A3 bits, and A2 and A1 bits. This step is executed for all vehicles except AS-512.

The flow chart of this subroutine is not included in this document, since it would require an instruction-by-instruction format.

3.2.14 LVDA Timing and Counter Test Subroutine (Figure 3-40)

It is the purpose of this subroutine to allow the LVDC to perform an internal check on certain specific areas of the LVDA. It is required that this routine have a relatively fast cycle time, since it will be executed periodically throughout the preflight sequence. One of the main objectives of this program is to operate without requiring inputs or affecting outputs to any equipment other than the LVDC. The main functions performed are:

1. Verification that the Real Time Counter increments every three word times for at least two consecutive increments.
2. Verification that the Minor Loop Counter functions properly, including the limiting and inhibit features.
3. Verification that the Switch Selector Counter functions properly, including the limiting and inhibit features.
4. Verification that the optisyn delay lines are functioning properly and execute reasonableness test on all axis, both syllables.
5. Verification that the COD counters and their associated ICR controls are functioning properly and to verify the operation of the following:
 - a. Duplex COD counters.
 - b. Subtract and limit feature associated with COD counters.
 - c. Disagreement bit inhibit feature.
 - d. Reversal of COD counter reading order.

If an error condition is recognized at any time during the execution of this routine, the LVDC obtains an appropriate error message and transfers control to the Error Monitor Subroutine. Once the error condition has been recognized by the launch computer, the LVDC continues with the program.

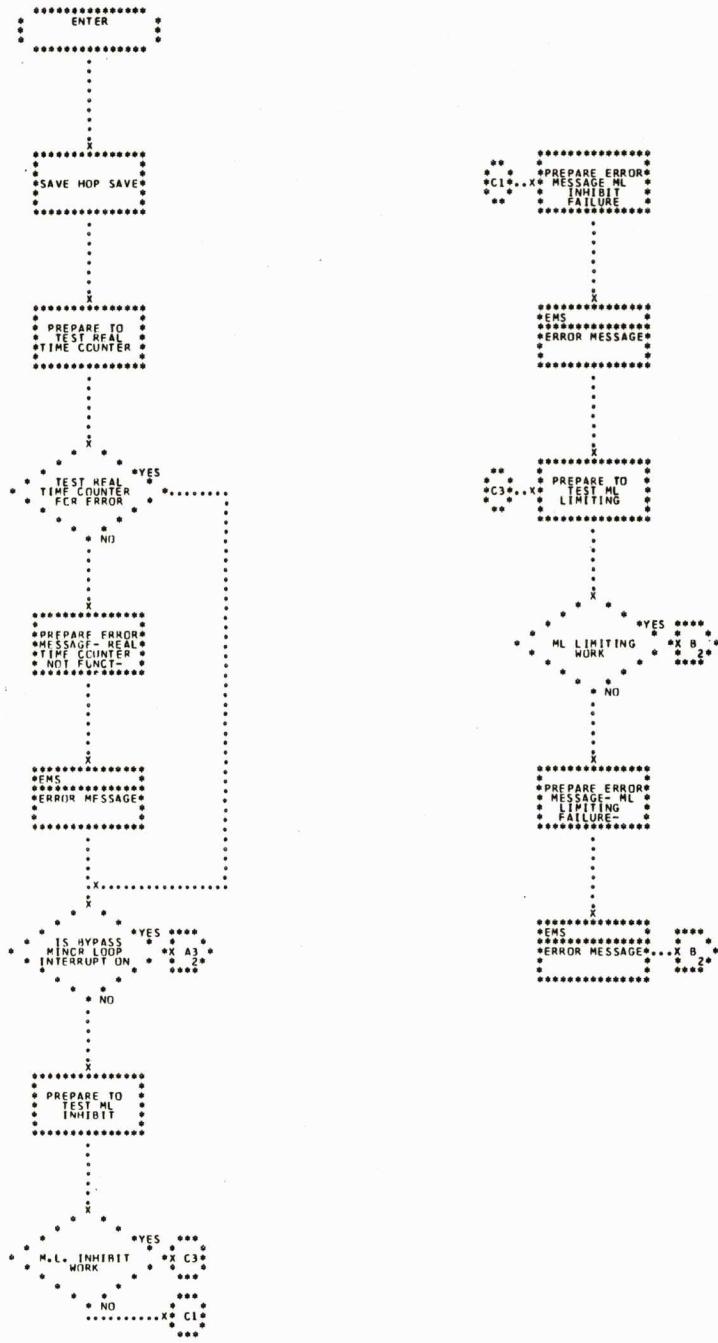


Figure 3-40. (Sheet 1 of 4) LVDA Timing and Counter Test Subroutine

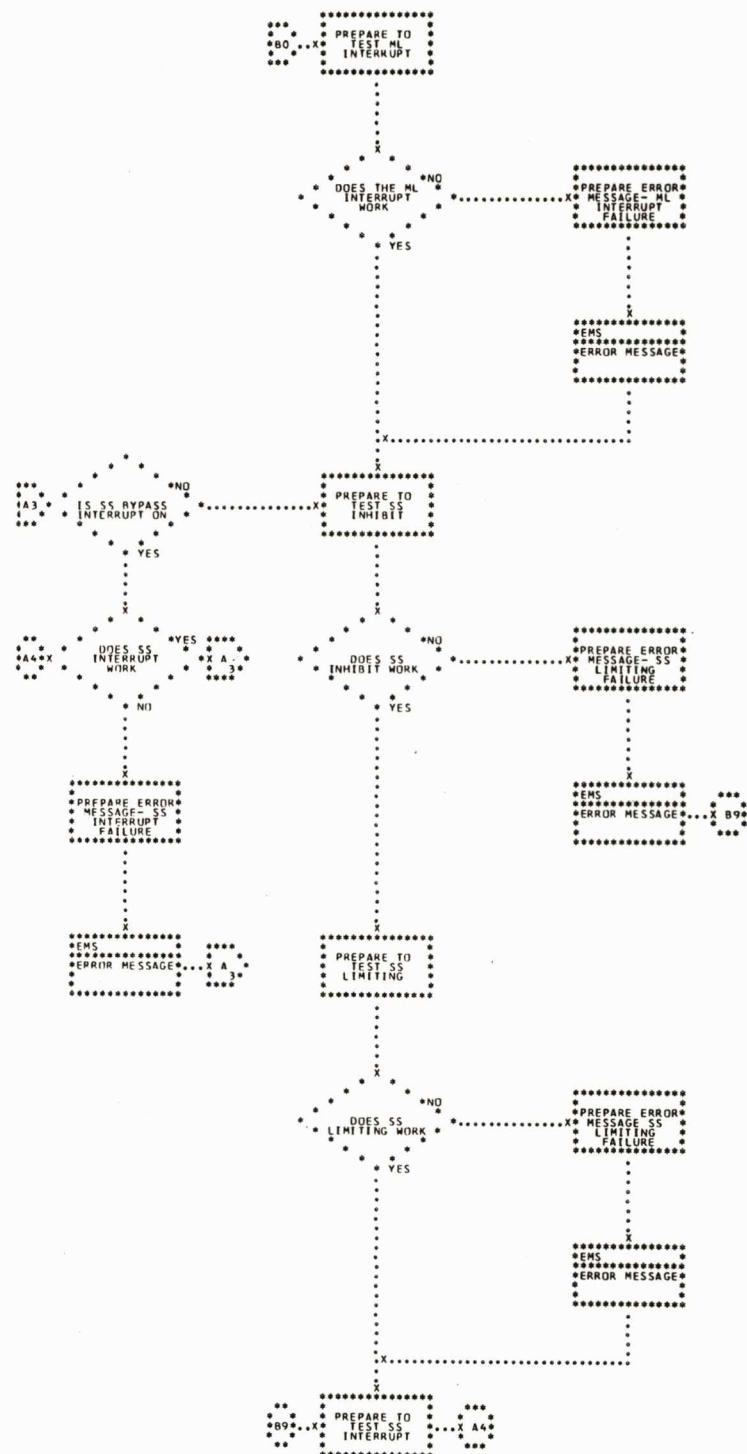


Figure 3-40. (Sheet 2 of 4) LVDA Timing and Counter Test Subroutine

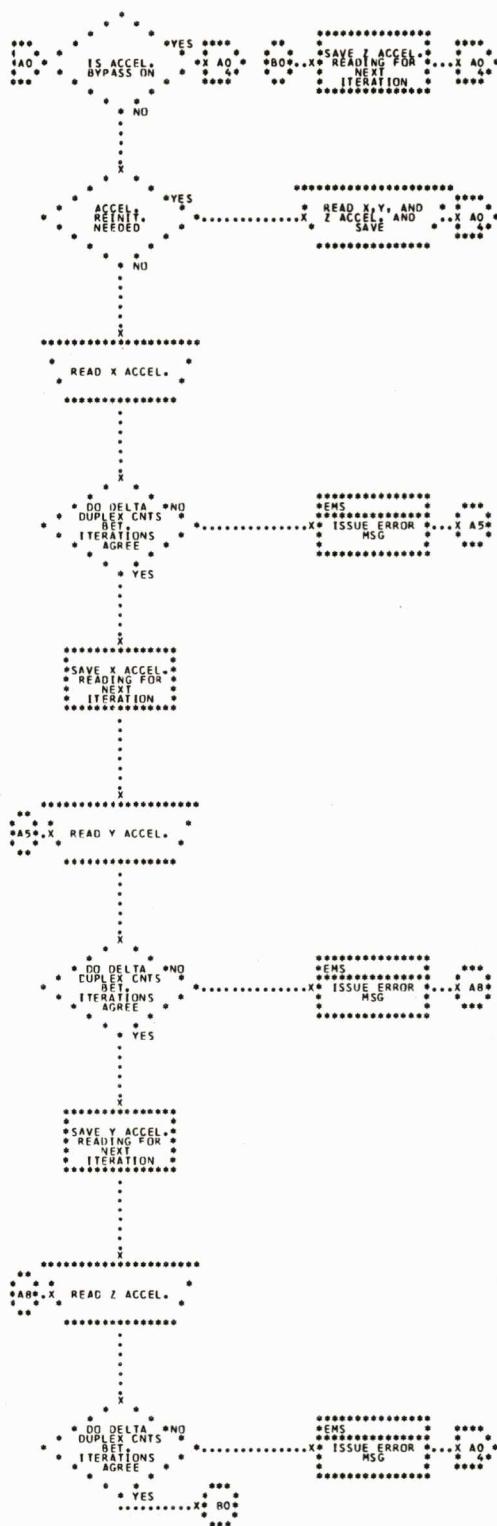


Figure 3-40. (Sheet 3 of 4) LVDA Timing and Counter Test Subroutine

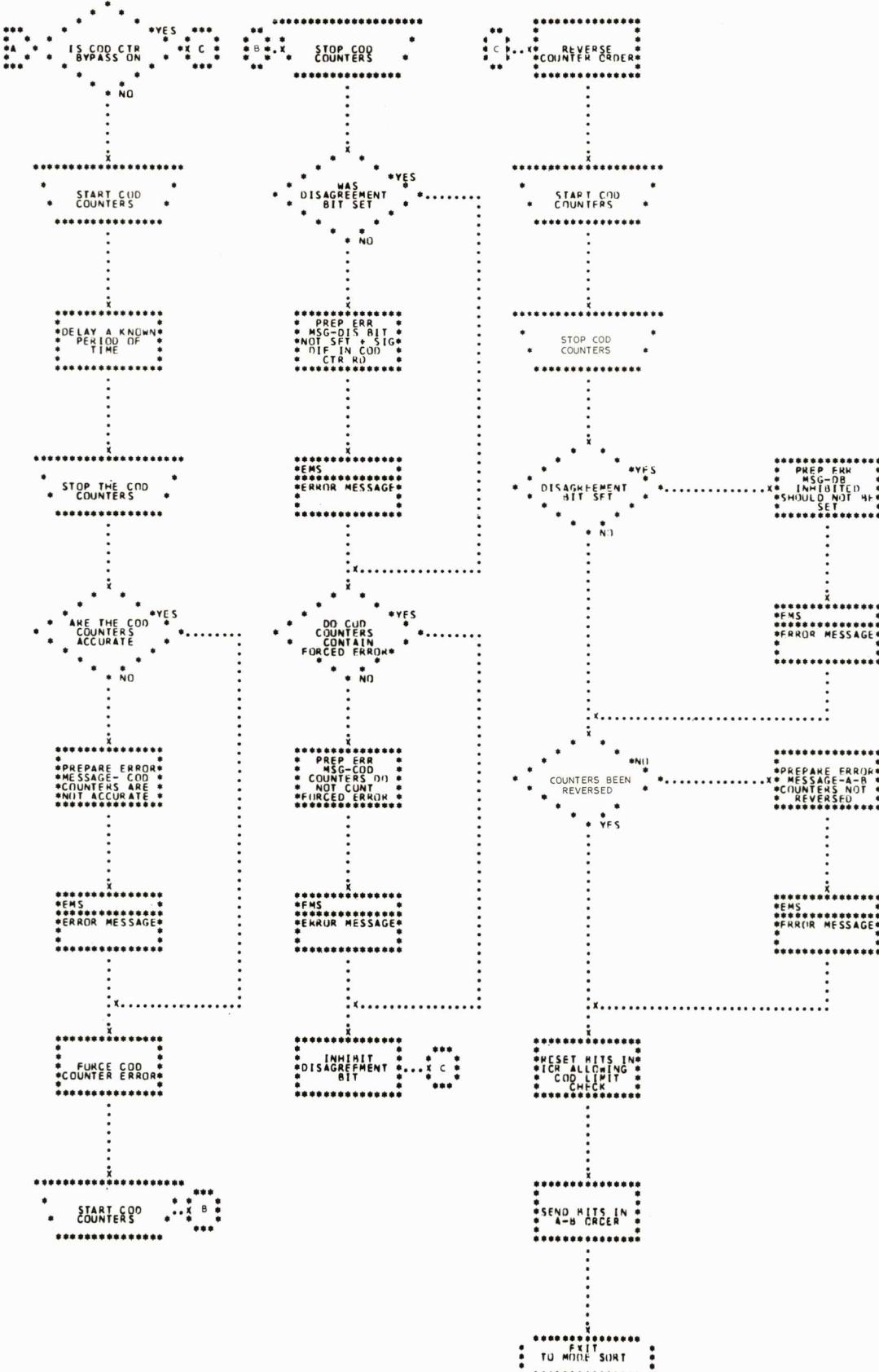


Figure 3-40. (Sheet 4 of 4) LVDA Timing and Counter Test Subroutine

3.2.15 Output Subroutine (Figure 3-41)

The purpose of this subroutine is to telemeter words placed in temporary storage. Upon entering this subroutine, a telemetry counter (bits A3 to A7 in the telemetry PIO instruction) is initialized and instructions are built to telemeter the first word. The counter is set to the number of words to be telemetered if this number is less than 32 and is decremented after every telemetry operation until zero is reached. If the number of words is greater than or equal to 32, the counter is initialized to 31 (to telemeter the 32 words), decremented to zero, and re-initialized if necessary until all words have been telemetered. The last word telemetered will have A9 = 1. All other words telemetered by this subroutine will have A9 = 0.

The Instruction Execute Subroutine accomplishes the telemetry. The program-built instructions are then indexed so that the next word in temporary storage can be telemetered. This program continues until all temporarily stored locations are telemetered.

There are two entries to this subroutine: One is from the Verify and Prepare to Load Routine, wherein this subroutine is used to telemeter data and addresses to be verified, or verified and loaded; the other entry is from any commanded routine which must output information. The reason for having two entry points is that each requires a different block of temporary storage locations.

Figure 3-41. Output Subroutine

3.2.16 S-IB Azimuth Calculate Subroutine (Figure 3-42)

The purpose of the S-IB Azimuth Calculate Subroutine is to utilize targeting parameters and predefined azimuth coefficients to calculate the firing azimuth for S-IB flights.

This subroutine is entered only from Prepare to Launch.

The following targeting parameters are used in the Azimuth equation calculations:

INC - Inclination
LAMBDA - Descending Node
LDOT - Rate of Change of Descending Node
TNGRR - Time of Nominal GRR

```
S-IB AZIMUTH
CALCULATE
SUBR.

*****
*      ENTER      *
*      FROM PTL   *
*****
.
.
.
X
*****
*      CALCULATE  *
*      DGRR       *
*****
.
.
.
X
*****
*      CALCULATE  *
*      LAMBDA    *
*****
.
.
.
X
*****
*      CALCULATE  *
*      INC        *
*****
.
.
.
X
*****
*      CALCULATE  *
*      AZIMUTH   *
*****
.
.
.
X
*****
*      EXIT      *
*      TO PTL    *
*****
.
```

Figure 3-42 S-IB Azimuth Calculate Subroutine

3.2.17 HOP 400 Initialize Subroutine (Figure 3-43)

The HOP 400 Initialize Subroutine initializes the Interrupt HOP 400 address in every module present in the LVDC.

When an interrupt is encountered during Prelaunch, the HOP 400 address is utilized in reaching the Preflight Interrupt Processor Routine.

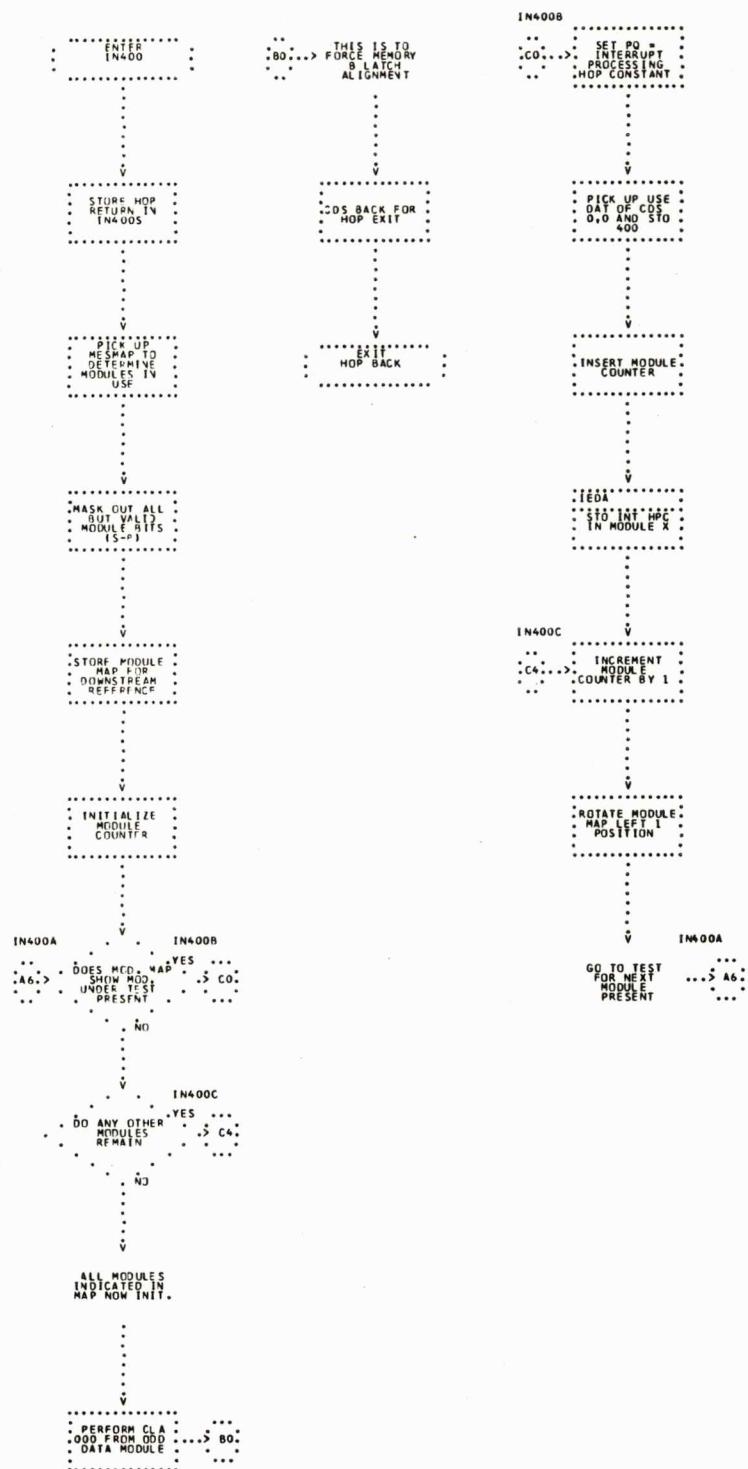


Figure 3-43. HOP 400 Initialize Subroutine

3.2.18 TLC Monitor Subroutine (Figure 3-44)

The TLC Monitor subroutine is entered each time core is accessed. This subroutine tests the EMR for occurrence of a TLC, EAM or EBM. If any of these bits are detected "ON", the module, sector and address bits of the calling routine are inserted into an Error Message. This Error Message is then telemetered.

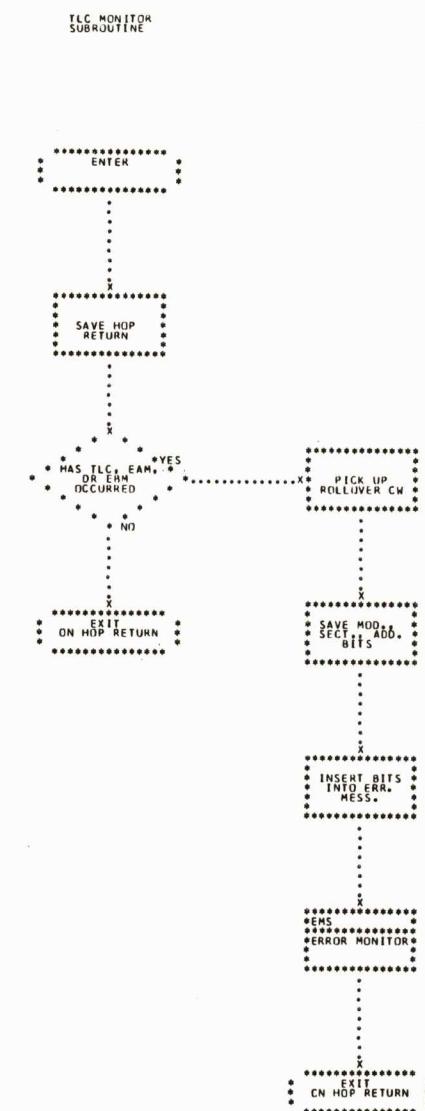


Figure 3-44. TLC Monitor Subroutine

APPENDICES

APPENDIX A

ABBREVIATIONS

CIU	Computer Interface Unit
COD	Cross-over Detector
COD/PS	Cross-over Detector and Power Supplies
DDAS	Digital Data Acquisition System
DO	Discrete Output
DOM	Data Output Multiplexer
EAM	Signal Indicating an Error in an Even Memory Module
EBM	Signal Indicating an Error in an Odd Memory Module
EMR	Error Monitor Register
ESE	Electrical Support Equipment
GR	Guidance Release Signal
GRRA	Guidance Reference Release Alert
ICR	Internal Control Register
LTE	Laboratory Test Equipment
LVDA	Launch Vehicle Data Adapter
LVDC	Launch Vehicle Digital Computer
ms.	Milliseconds
OCR	Orbital Checkout Request
PCM	Pulse Code Modulation
PIO	Input/Output Instruction in LVDC
PEGR	Prepare for Guidance Release
SLCC	Saturn Launch Computer Complex

APPENDIX B

This appendix contains data items which are common to all LVDC Preflight Programs.
The data items included are:

- Regular Status Codes
- Special Status Codes
- Vehicle Dependent Parameters
- Linkages
- Flags and Constants
- Telemetry PIO Tags

REGULAR STATUS CODES

Note that each routine is assigned two codes — complements. Either code will command the routine. Where parentheses appear around the name of the routine, the complement status code will be issued on entry.

- 00 MODE SORT ROUTINE - COMMANDS SPECIAL LOADER MODE SORT
- 02 ACCELEROMETER PULSE COUNT ROUTINE ENTRY
- 03 GIMBAL ANGLE MONITOR ROUTINE ENTRY
- 04 DISCRETE INPUT ROUTINE ENTRY
- 05 DISCRETE OUTPUT ROUTINE ENTRY
- 06 G & C STEERING TEST ENTRY
- 07 DOM TEST ROUTINE ENTRY
- 10 LADDER ERROR TEST ROUTINE ENTRY
- 11 PREPARE TO LAUNCH SIM FLT WITHOUT A PLATFORM
- 12 PREPARE TO LAUNCH FLIGHT WITH A PLATFORM
- 13 EXERCISE ATTITUDE COMMAND ROUTINE MODE 1 ENTRY
- 14 COMPUTER INTERFACE UNIT READ ROUTINE ENTRY
- 15 SWITCH SELECTOR ROUTINE ENTRY
- 16 SECTOR SUMCHECK ROUTINE ENTRY
- 17 EXERCISE ATTITUDE COMMAND ROUTINE MODE 2 ENTRY
- 20 SECTOR DUMP ROUTINE ENTRY
- 21 VERIFY AND PREPARE TO LOAD ROUTINE ENTRY
- 22 MEMORY ERROR TEST
- 23 LOAD ROUTINE ENTRY
- 24 MINOR LOOP, SWITCH SELECTOR AND REAL TIME COUNTER TESTS ENTRY
- 27 SIB TARGET DUMP ROUTINE
- 30 PREPARE TO LAUNCH SIM FLIGHT WITH PLATFORM
- 31 REPEATABLE FLIGHT SIM ROUTINE
- 32 TELEMETRY TEST ROUTINE
- 35 COMMAND RECEIVER LINKAGE ROUTINE
- 40 POWER UP AND INITIALIZE
- 50 (SIB TARGET DUMP ROUTINE)
- 53 (MINOR LOOP, SWITCH SELECTOR, REAL TIME COUNTER TEST ROUTINE)
- 54 (LOAD ROUTINE)
- 55 (MEMORY ERROR TEST ROUTINE)
- 57 (SECTOR DUMP ROUTINE)
- 60 (EXERCISE ATTITUDE COMMAND ROUTINE MODE 2)
- 62 (SWITCH SELECTOR ROUTINE)
- 63 (COMPUTER INTERFACE UNIT READ ROUTINE)

REGULAR STATUS CODES (Continued)

64 (EXERCISE ATTITUDE COMMAND ROUTINE MODE 1)
65 (PREPARE TO LAUNCH ROUTINE)
67 (LADDER ERROR TEST ROUTINE)
71 (G & C STEERING TEST ROUTINE)
72 (DISCRETE OUTPUT ROUTINE)
73 (DISCRETE INPUT ROUTINE)
74 (GIMBAL ANGLE MONITOR ROUTINE)
75 (ACCELEROMETER PULSE COUNT ROUTINE)

SPECIAL STATUS CODES

Status codes enclosed in parentheses are issued by the routine, but not commanded. Status codes not enclosed in parentheses are used to command indicated functions within the indicated routine.

- (26) FORCED BEGIN AND INITIALIZE ROUTINE ENTRY
- (34) EXERCISE ATTITUDE COMMAND ROUTINE ERROR '' INITIAL
CONVERTER NOT STILL SELECTED
- (37) RESERVED FOR SIM FLT
- (42) RESERVED FOR FLIGHT
- (43) EXERCISE ATTITUDE COMMAND TEST MAXIMUM ATTAINED ON 1 OR
MORE AXES
- (45) READ INPUT DATA SUBROUTINE OVERTIME MESSAGE
- (46) EXERCISE ATTITUDE COMMAND TEST DRIVING TOWARDS NULL
- (47) ERROR MONITOR SUBROUTINE ENTRY
- (51) FORCED BEGIN ROUTINE ERROR -- EMR NON-ZERO
- (56) VERIFY AND PREPARE TO LOAD ROUTINE TRYING TO LOAD WITHOUT
FIRST LOADING PREVIOUS INFORMATION (IF ANY)
- (66) ISSUED ON COMPLETION OF REPEATABLE FLT-SIM RUN
- (70) RESERVED FOR SIM FLIGHT
- 77 FORCES THE EMR SUBROUTINE TO RETURN TO FORCED BEGIN FBDA
- (77) ISSUED TO MODE REGISTER ONLY WHEN IN SPECIAL LOADER MODE
SORT

DESCRIPTION OF VEHICLE DEPENDENT PARAMETERS

Vehicle dependent parameters are classified as those constants which are affected by the size of LVDC core (6 or 8 modules), CIU addresses, active discretes, active interrupts, latitude, local gravity, firing azimuth, earth's rate, and platform misalignment.

The following list reflects those vehicle dependent parameters.

1. MESMAP (Memory Status Map) Used by the Memory Error Test Routine and HOP 400 Initialize Subroutine to identify which modules are present in the LVDC.
2. PLDIN1 (Prepare to Launch Discrete Input 1) Used by the Prepare to Launch Routine, and identifies the active discretes to be examined for the proper state.
3. PLDIN2 (Prepare to Launch Discrete Input 2) Used by the Prepare to Launch Routine, and examines the active discrete inputs for the proper state.
4. PLDIS1 (Prepare to Launch Discrete Input Spares 1) Used by the Prepare to Launch Routine, and identifies the active discrete input spares and ladder converter selection to be examined.
5. PLDIS2 (Prepare to Launch Discrete Input Spares 2) Used by the Prepare to Launch Routine and examines the active discrete input spares and ladder converter selection for the proper state.
6. PLISR1 (Prepare to Launch Interrupt Storage Register 1) Used by the Prepare to Launch Routine and examines the active interrupts.
7. PSNLAT (SIN of Geodetic Latitude) Used in Calculating (AMP 3) platform constants.
8. PCSLAT (COS of Geodetic Latitude) Used in calculating (AMP 3) platform constants.

DESCRIPTION OF VEHICLE DEPENDENT PARAMETERS (Continued)

- | | |
|--|---|
| 9. RANGE1 and RANGE2 (Azimuth Safety Limits) | Used by PTL to test the azimuth value. |
| 10. Memory Module Status (MOD Constants) | Used to define MESMAP and core map module status words. |
| 11. PLTGRR (Difference Between PLOT and GRR) | Used by Prepare to Launch to calculate predicted GRR. |
| 12. PSNFAV (SIN of the Medium Variable Firing Azimuth) | Used by Accelerometer Monitor |
| 13. PCSFAV (COS of the Medium Variable Firing Azimuth) | Used by Accelerometer Monitor |

LINKAGES

A. Linkages from Preflight to Flight and Orbital Routines.

B. Linkages for return to Preflight.

<u>SYMBOL</u>	<u>LOCATION</u>	<u>LINKAGE POINT</u>	<u>DESCRIPTION</u>
PF SCHC	0, 4, 227	0, 11, 0, 005, 2, 17 (D)	Used to exit from Preflight Sector Sum Check Routine.
GCFIHC	0, 7, 006	0, 11, 0, 002, 2, 17 (D)	Used by G and C Steering Test to enter Flight Initialize.
GRIHC	0, 17, 157	0, 11, 0, 000, 2, 17 (D)	Used by preflight interrupt processing to enter Flight Initialize upon Guidance Reference Release Interrupt.
OCRLHC	0, 7, 253,	4, 17, 0, 274, 4, 17 (D)	Used to exit from Preflight Orbital Command Receiver Test.
AZCHC	0, 5, 371	0, 11, 0, 012, 2, 13 (D)	Used by Variable Azimuth Prepare to Launch to enter Azimuth Calculate Subroutine.
IBOLHC	0, 5, 372	0, 11, 0, 005, 2, 16 (D)	Used to SIB Target Load Linkage Routine to enter the Flight Program.

FLAGS AND CONSTANTS

<u>SYMBOL</u>	<u>DESCRIPTION</u>
EMCON	Used in Error Monitor Subroutine to mask out EMR bits which are to be disregarded.
EMCON1	Used to initialize EMCON in Forced Begin.
BYPASS	Used by Prepare to Launch and LVDA Test, and provides the capability to bypass undesired functions of the programs.
OBFLAG	Must be set non-zero by any Orbital Routine writing into Preflight Routines.
INTH	Always contains present image of Inhibit Register.
INHOPC	Assembled HOP constant to Interrupt Processing Routine. Is used to initialize location 400 of each module while running Preflight Routines.
CRAIHC	HOP constant used upon Command Receiver Interrupt. Orbital Initialize stores its own value here.
INHC	Storage location for the return HOP constant stored upon entry to INT processing.
INACC	Storage location for contents of accumulator upon entry to INT processing.
INPQ	Storage location for contents of PQ Register upon entry to INT processing.
MPLC1	Flag used to control whether the Accelerometer Monitor Program (AMP 3) will be executed or not. 0 = Run + = Do Not Run
PTLTA	Preflight stores delta time from start of Prepare to Launch until GRR Interrupt. Scaled B25 in RT clock pulses.

FLAGS AND CONSTANTS (Continued)

<u>SYMBOL</u>	<u>DESCRIPTION</u>
PTL103	Preflight stores last RT clock reading used to compute PTLTA.
FPARAM	Start of 16 word table for storage of FLT parameters, azimuth, GMT.
SIMIND	This location is referenced in the core map to be used by the RCA-110A. Is defined as 2 locations to include the SIM indicator and FIN 1 Azimuth. Prepare to Launch uses both of these data words.
TVRATE	Flag used to indicate a fixed azimuth for Skylab I and variable azimuth for Saturn V.

PREFLIGHT TELEMETRY PIO TAGS

<u>PIO TAGS</u>	<u>DESCRIPTION</u>
001	TELEMETRY TEST PATTERN WORD (707070706)
025	TELEMETRY TEST PATTERN WORD (252525252)
040	BIT PATTERN WORD FROM MODE SORT
061	BIT PATTERN WORD FROM MODE SORT OR PREPARE TO LAUNCH
171	BACKUP 3 GIMBAL ANGLE
174	REAL TIME CLOCK READ
175	BACKUP 1 GIMBAL ANGLE
371	ERROR MESSAGE WORD
401	FINE 1 GIMBAL ANGLE
405	FINE 2 GIMBAL ANGLE
411	FINE 3 GIMBAL ANGLE
445	DISCRETE INPUT REGISTER
470	AZIMUTH IN PIRADS
471	AZIMUTH COMPLEMENT IN PIRADS
501	DOWNRANGE ACCELEROMETER
505	VERTICAL ACCELEROMETER
511	CROSSRANGE ACCELEROMETER
521	TELEMETRY TEST PATTERN WORD (525252524)
545	DISCRETE INPUT SPARES REGISTER
565	INTERRUPT STORAGE REGISTER
635	BACKUP 2 GIMBAL ANGLE
671	STATUS CODE
675	ACCELEROMETER OFF-LEVEL INDICATION
701	RAW EMR CONTENTS
714	BIT PATTERN WORD FROM PREPARE TO LAUNCH

PREFLIGHT TELEMETRY PIO TAGS (Continued)

<u>PIO TAGS</u>	<u>DESCRIPTION</u>
735	BIT PATTERN WORD FROM MODE SORT AND PREPARE TO LAUNCH
741	BIT PATTERN WORD FROM MODE SORT ONLY
771	TELEMETRY TEST PATTERN WORD (77777776)
174 to 000 and 400	TAGS 400 AND TAGS 174 TO 000 BY DECREMENTS OF 4 ARE USED BY THE OUTPUT SUBROUTINE

APPENDIX C

This Appendix contains data items (Interrupts, Discrete Inputs, and Discrete Input Spares) unique to a vehicle or series. The data is divided into three categories by tabs:

- Saturn V
- Saturn IB
- Skylab I

The Saturn V data items are effective for AS-512 and subsequent. The Saturn IB data items are effective for AS-206 and subsequent. The Skylab I data items are effective for AS-513 and AS-515.

OFF

JT 'B'

D

TOFF 'A'

ES

F

ANCE REFERENCE

LEASE

COMMAND RECEIVER

TEMPORARY LOSS OF

CONTROL (TLC)

SPARE

TIMER 2 (SWITCH

SELECTOR)

TIMER 1 (MINOR LOOP)

SATURN V DATA ITEMS

INTERRUPTS

The Interrupts are tested during Prepare to Launch to insure that all interrupts, being checked, are in the "off" state. The interrupts and their descriptions are as follows:

<u>INTERRUPT</u>	<u>STATE OF INTERRUPT DURING PREPARE TO LAUNCH</u>	<u>INTERRUPT DESCRIPTION</u>
INT1	IGNORED	RCA
INT2	OFF	S/C INIT of SII/SIVB SEP 'A', SIVB CUTOFF
INT3	IGNORED	RCA
INT4	OFF	SIVB ENGINE OUT 'B'
INT5	OFF	SIC OUTBOARD ENGINE CUTOFF 'A'
INT6	OFF	SII ENGINES CUTOFF
INT7	OFF	GUIDANCE REFERENCE RELEASE
INT8	OFF	COMMAND RECEIVER
INT9	OFF	TEMPORARY LOSS OF CONTROL (TLC)
INT10	IGNORED	SPARE
INT11	IGNORED	TIMER 2 (SWITCH SELECTOR)
INT12	IGNORED	TIMER 1 (MINOR LOOP)

DISCRETE INPUTS

The Discrete Inputs are tested in Prepare to Launch to insure that all Discretes are in their proper state. The Discretes and their descriptions are as follows:

<u>DINs</u>	<u>EXPECTED STATE DURING PREPARE TO LAUNCH</u>	<u>DESCRIPTION</u>
DIN1	IGNORED	RCA
DIN2	OFF	COMMAND RECEIVER
DIN3	OFF	O2-H2 BURNER MALFUNCTION
DIN4	OFF	S/C CONTROL OF SATURN
DIN5	ON	SIVB ENGINE OUT 'A'
DIN6	OFF	TLI INHIBIT
DIN7	OFF	LIFTOFF 'B'
DIN8	IGNORED	SPARE
DIN9	OFF	SPACECRAFT CONTROL OF SATURN
DIN10	ON	SII/SIVB SEPARATION
DIN11	ON	SIC INBOARD ENGINE OUT 'B'
DIN12	ON	SIC/SII SEPARATION
DIN13	ON	SII INBOARD ENGINE OUT
DIN14	OFF	SIC OUTBOARD ENGINE OUT
■ DIN15	IGNORED	SII AFT INTERSTAGE SEPARATION
■ DIN16	IGNORED	GUIDANCE REFERENCE RELEASE ALERT
DIN17	OFF	UPPER OUTBOARD ENGINE OUT
DIN18	OFF	SIC OUTBOARD ENGINE CUTOFF 'B'
DIN19	OFF	SII ENGINE OUT
DIN20	OFF	SIVB ENGINE SEQUENCE START
DIN21	ON	SII OUTBOARD ENGINE OUT

DISCRETE INPUTS (Continued)

<u>DINs</u>	<u>EXPECTED STATE DURING PREPARE TO LAUNCH</u>	<u>DESCRIPTION</u>
DIN22	OFF	S/C INIT OF SII/SIVB SEP 'B', SIVB CUTOFF
DIN23	OFF	S/C INIT OF SIVB ENGINE CUTOFF
DIN24	OFF	LIFTOFF

DISCRETE INPUT SPARES

The Discrete Input Spares are tested during Prepare to Launch to insure that all Discrete Spares are in the proper state. At the present time none of the Discrete Spares are tested in the PTL Register Test. Discrete Spares A & B (Switch to Converter A, Switch to Converter B) are tested separately in Error Monitor Subroutine.

<u>DISCRETE SPARES</u>	<u>EXPECTED STATE</u>	<u>DESCRIPTION</u>
DIS1	IGNORED	COOLANT THERMAL SWITCH NO. 1
DIS2	IGNORED	COOLANT THERMAL SWITCH NO. 2
DIS3	IGNORED	SPARE
DIS4	IGNORED	SPARE
DIS5	IGNORED	SPARE
DIS6	IGNORED	SPARE
DIS7	IGNORED	SPARE
DIS8	IGNORED	SPARE
DISA	IGNORED	
DISB	IGNORED	

L_R
SS OF
L_C)

L (SWITCH
LCTOR)
MER 1 (MINOR
LOOP)

SATURN IB DATA ITEMS

INTERRUPTS

The Interrupts are tested during Prepare to Launch to insure that all interrupts, being checked, are in the "off" state. The interrupts and their descriptions are as follows:

<u>INTERRUPT</u>	<u>STATE OF INTERRUPT DURING PREPARE TO LAUNCH</u>	<u>INTERRUPT DESCRIPTION</u>
INT1	IGNORED	RCA
INT2	OFF	SIB LOW LEVEL SENSORS DRY 'A'
INT3	IGNORED	RCA
INT4	OFF	SIVB ENGINE OUT 'B'
INT5	OFF	SIB OUTBOARD ENGINE CUTOFF 'A'
INT6	OFF	SIB LOW LEVEL SENSORS DRY 'B'
INT7	OFF	GUIDANCE REFERENCE RELEASE
INT8	OFF	COMMAND RECEIVER
INT9	OFF	TEMPORARY LOSS OF CONTROL (TLC)
INT10	IGNORED	SPARE
INT11	IGNORED	TIMER 2 (SWITCH SELECTOR)
INT12	IGNORED	TIMER 1 (MINOR LOOP)

DISCRETE INPUTS

The Discrete Inputs are tested in Prepare to Launch to insure that all Discretes are in their proper state. The Discretes and their descriptions are as follows:

<u>DINs</u>	<u>EXPECTED STATE DURING PREPARE TO LAUNCH</u>	<u>DESCRIPTION</u>
DIN1	IGNORED	RCA
DIN2	IGNORED	COMMAND RECEIVER
DIN3	IGNORED	SPARE
DIN4	IGNORED	SPARE
DIN5	ON	SIVB ENGINE OUT 'A'
DIN6	IGNORED	SPARE
DIN7	OFF	LIFTOFF 'B'
DIN8	IGNORED	SPARE
DIN9	OFF	SPACECRAFT CONTROL OF SATURN
DIN10	IGNORED	COOLANT THERMAL SWITCH NO. 1
DIN11	IGNORED	COOLANT THERMAL SWITCH NO. 2
DIN12	ON	SIB/SIVB SEPARATION
DIN13	IGNORED	SPARE
DIN14	OFF	SIB OUTBOARD ENGINE OUT
DIN15	OFF	SIB INBOARD ENGINE OUT
DIN16	IGNORED	GUIDANCE REFERENCE RELEASE ALERT
DIN17	IGNORED	SPARE
DIN18	IGNORED	SPARE
DIN19	IGNORED	SPARE
DIN20	IGNORED	SPARE
DIN21	IGNORED	SPARE
DIN22	IGNORED	SPARE CUTOFF 'B'
DIN23	OFF	SIB OUTBOARD ENGINES CUTOFF 'B'
DIN24	OFF	LIFTOFF

Change 2

Changed 15 October 1972

DISCRETE INPUT SPARES

The Discrete Input Spares are tested during Prepare to Launch to insure that all Discrete Spares are in the proper state. At the present time none of the Discrete Spares are tested in the PTL Register Test. Discrete Spares A & B (Switch to Converter A, Switch to Converter B) are tested separately in Error Monitor Subroutine.

<u>DISCRETE SPARES</u>	<u>EXPECTED STATE</u>	<u>DESCRIPTION</u>
DIS1	IGNORED	SPARE
DIS2	IGNORED	SPARE
DIS3	IGNORED	SPARE
DIS4	IGNORED	SPARE
DIS5	IGNORED	SPARE
DIS6	IGNORED	SPARE
DIS7	IGNORED	SPARE
DIS8	IGNORED	SPARE
DISA	IGNORED	
DISB	IGNORED	

INTURPTS

To ensure that all interrupts, being
descriptions are as follows:

INTRODUCTION

SKYLAB I

SKYLAB I DATA ITEMS

INTERRUPTS

The Interrupts are tested during Prepare to Launch to ensure that all interrupts, being checked, are in the "off" state. The interrupts and their descriptions are as follows:

<u>INTERRUPT</u>	<u>STATE OF INTERRUPT DURING PREPARE TO LAUNCH</u>	<u>DESCRIPTION</u>
INT1	IGNORE	RCA INTERRUPT
INT2	IGNORE	SPARE
INT3	IGNORE	RCA INTERRUPT
INT4	OFF	SII ENGINES OUT 'B'
INT5	OFF	SIC OUTBOARD ENGINES CUTOFF 'A'
INT6	IGNORE	SPARE
INT7	OFF	GRR
INT8	OFF	COMMAND RECEIVER
INT9	OFF	TEMPORARY LOSS OF CONTROL (TLC)
INT10	IGNORE	SPARE
INT11	IGNORE	TIMER 2 (SWITCH SELECTOR)
INT12	IGNORE	TIMER 1 (MINOR LOOP)

DISCRETE INPUTS

The Discrete Inputs are tested in Prepare to Launch to ensure that all Discretes are in their proper state. The Discretes and their descriptions are as follows:

<u>DINs</u>	<u>EXPECTED STATE DURING PREPARE TO LAUNCH</u>	<u>DESCRIPTION</u>
DIN1	IGNORE	RCA
DIN2	RESET	COMMAND RECEIVER
DIN3	IGNORE	SPARE
DIN4	IGNORE	SPARE
DIN5	IGNORE	SPARE
DIN6	IGNORE	SPARE
DIN7	RESET	LIFTOFF 'B'
DIN8	IGNORE	SPARE
DIN9	IGNORE	SPARE
DIN10	ON	SII/SWS SEPARATION
DIN11	ON	SIC INBOARD ENGINE OUT 'B'
DIN12	ON	SIC/SII SEPARATION
DIN13	ON	SII INBOARD ENGINE OUT
DIN14	OFF	SIC OUTBOARD ENGINE OUT
DIN15	IGNORE	SII AFT INTERSTAGE SEPARATION
DIN16	IGNORE	GRRA
DIN17	OFF	SIC INBOARD ENGINE OUT 'A'
DIN18	OFF	SIC OUTBOARD ENGINE CUT OFF 'B'
DIN19	OFF	SII ENGINE OUT
DIN20	IGNORE	SPARE
DIN21	ON	SII OUTBOARD ENGINE OUT
DIN22	IGNORE	SPARE
DIN23	IGNORE	SPARE
DIN24	OFF	LIFTOFF

DISCRETE INPUT SPARES

The Discrete Input Spares are tested during Prepare to Launch to ensure that all Discrete Spares are in the proper state. At the present time none of the Discrete Spares are tested in the PTL Register Test. Discrete Spares A & B (Switch to Converter A, Switch to Converter B) are tested separately in Error Monitor Subroutine.

<u>DISCRETE SPARES</u>	<u>EXPECTED STATE</u>	<u>DESCRIPTION</u>
DIS1	IGNORED	SPARE
DIS2	IGNORED	SPARE
DIS3	IGNORED	SPARE
DIS4	IGNORED	SPARE
DIS5	IGNORED	SPARE
DIS6	IGNORED	SPARE
DIS7	IGNORED	SPARE
DIS8	IGNORED	SPARE
DISA	IGNORED	
DISB	IGNORED	

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August 4, 1972

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B. R. Huckabee, Manager
Flight Programming II

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Title Page Preface	Title Page Preface
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3-71 and 3-72 3-75 and 3-76	3-71 and 3-72 3-75 and 3-76
Appendices	
B-7 through B-10 C-1/C-2 Skylab II Tab C-11/C-12	B-7 through B-10 C-1/C-2 Skylab I Tab C-11 through C-13/C-14

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Table of Contents (iii, iv)	Table of Contents (iii, iv)
List of illustrations (v, vi)	List of illustrations (v, vi)
Section 3	
3-99/3-100	3-99, 3-100
Appendices	
B-3, B-4	B-3, B-4
B-7, B-8	B-7, B-8
C-3, C-4	C-3, C-4
C-7, C-8	C-7, C-8

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