## **TECHNICAL DESCRIPTION**



# MICRO PCM TELEMETRY SYSTEM



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PCM

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## SECTION 1.0

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INTRODUCTION

#### 1.0 INTRODUCTION

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The Micro PCM Telemetry System was designed and produced by Radiation Incorporated for the National Aeronautics and Space Administration, Manned Spacecraft Center. The design was initiated in October 1964, and the system was qualified to the launch and flight environments of the Apollo mission, in July 1965.

The system samples, in sequence, 98 single-ended, high level (0 to +5 volts) analog channels and converts each sample to an eight bit binary coded word. These 98 analog data words are combined with 2 sync code words to form a serial non-return-to-zero PCM output at any one of seven programmable bit rates in the range from 800 to 51,200 bits per second. The power consumption is approximately 1.7 watts.

The system is packaged in a sealed aluminum housing with a volume of 33 cubic inches. The total weight of the system is 1.4 pounds.

A picture of the Micro PCM Telemetry System is shown in Figure 1.0.

Appendix A-1 and A-2 contain the pin assignments for the six connectors Appendix B provides the output format of the PCM system. Appendix C gives the theoretical analog voltage corresponding to the switching point for each of the 255 digital output codes of the PCM system.





Figure 1.0. Micro PCM Telemetry System

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## SECTION 2.0

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## ELECTRICAL DESCRIPTION

#### 2.0 ELECTRICAL DESCRIPTION

The Micro PCM Telemetry System represents the state-of-the-art with respect to size, weight, power, and performance. The design has been thoroughly proven by outstanding performance during a very stringent qualification test program. The unit is now flight qualified for any mission which does not exceed the severe environments (detailed in subsequent paragraphs) imposed during this series of tests.

The electrical performance of the PCM system was well within the specification limits during the qualification test program. In fact, results during the temperature tests show that the system qualified to an accuracy better than  $\pm 0.05\%$ . This performance is unsurpassed by conventional discrete component systems and certainly represents the state-of-the-art for micro PCM systems.

#### 2.1 System Operation

As shown in the system block diagram in Figure 2.1, analog data are received at the input to the analog multiplexer where the data are sequentially sampled. Ninety-eight single-ended, high-level analog inputs are processed by the analog multiplexer. The multiplexer utilizes P-channel metal oxide semiconductor (MOS) field effect transistors (FET) to perform the gating function.

The analog-to-digital converter (coder) effectively buffers the sampled analog voltage PAM wavetrain to provide a high input impedance. The coder converts the sampled analog voltage to a parallel 8-bit digital word with 255 possible levels.

The output register provides serial readout for 98 coded analog words as well as two 8-bit sync words for a total of 100 words per frame.

The programmer provides system timing by successive binary counters triggered from a crystal oscillator. Logic circuits decode the binary counter status to provide any required timing. The block diagram shows how the programmer controls all block functions. The bit rate may be externally selected in binary steps from 51,200 to 800 cycles per second. Any six of the seven possible rates may be wired to the patch connector for programming.

The PCM signal conditioner serves to provide the two electrically independent signal outputs at the proper voltage and impedance levels which are required for the serial output data. Data rate timing and frame rate timing are also provided externally. Two independent buffers for each digital signal out are used to provide a dual set of outputs with the required output characteristics.



#### Figure 2.1. Block Diagram. Micro PCM Telemetry System

The power supply converts the nominal 28 vdc power input to the various voltages required by the PCM system and also isolates the power and signal grounds.

#### 2.2 Analog Multiplexer

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The analog multiplexer sequentially samples 98 signal inputs and provides a PAM wavetrain to the coder. The sample rate and sample period are controlled by the programmer. All gate drive circuitry is located in the multiplexer and it interfaces directly with the counter stages of the programmer.

The multiplexer was designed using four integrated circuit flat-pack building blocks. These are:

- 1. A monolithic MOS FET gate package which contains five separate gate circuits.
- 2. A monolithic high voltage NPN gate driver package which contains six independent gate driver circuits.
- 3. A monolithic high voltage NPN logic package, two circuit elements per flat-pack, which provides part of the multiplexer sequencer drive circuitry.
- 4. A high voltage PNP logic package, six circuit elements, which interfaces directly with the counter stages of the programmer.

The 98 analog channels are processed in 20 groups of five channels each. Each group of five channel gates, or first tier gates are processed by one MOS FET flat pack. Thus, 20 flat packs for the channel gates and four flat packs for the sequencer, or second tier gates are required for the analog gating function. These analog channel-flat pack allocations are illustrated by Figure 2.2-1.

A total of 22 command pulses are required to operate the multiplexer. These 22 command lines, which consist of 10 column drives, 10 row drives, and 2 sequencer drives, are shown in matrix form in Figure 2.2–2.





			$\overline{}$	$7  \stackrel{4}{\searrow}$	$\sim$				7 5		7
sequencer drive A	$\geq$	1-5	11-15	21-25	31-35	41-45	51-55	61-65	71-75	81-85	91-95
ROW DRIVES		1	11	21	31	41	51	61	71	81	91
ROW 1		2	12	22	32	42	52	62	72	82	92
ROW 2		2	12		02	72	52	02			
ROW 3		3	13	23	33	43	53	63	73	83	93
ROW 4		4	14	24	34	44	54	64	74	84	94
ROW 5	$\triangleright$	5	15	25	35	45	55	65	75	85	95
ROW 6	$\triangleright$	6	16	26	36	46	56	66	76	86	96
ROW 7		7	17	27	37	47	57	67	77	87	97
ROW 8	$\triangleright$	8	18	28	38	48	58	68	78	88	98
ROW 9	$\triangleright$	9	19	29	39	49	59	69	79	89	99
ROW 10	$\succ$	10	20	30	40	50	60	70	80	90	100
SEQUENCER DRIVE B	$\triangleright$	6-10	16-20	26-30	36-40	46-50	56-60	66-70	76-80	86-90	96-100



#### 2.2.1 Multiplexer Switch Circuit

At any particular multiplexer sample time, one row, one column, and one sequencer logic input is driven by a saturated NPN transistor in the programmer logic. The switch circuit shown in Figure 2.2.1 only allows one (of 100) input gates and one (of 20) sequencer gates to conduct.

A description of conducting input and sequencer gates as shown in Figure 2.2.1 follows. If transistors Q1, Q2, and Q3 bases are at ground potential and the +4V duty cycle pulse is present, current determined by R1 will flow into each resistor R2. The column drive current causes transistor Q4 to saturate which clamps the common column drive line with the emitters of transistors Q5 and Q6 to -20V. The row drive current can now flow into the common row drive line and will then flow into the base of transistor Q5 since its emitter is at -20V. When transistor Q5 saturates the gate of the input P-channel enhancement mode MOS FET is driven to -20V which causes it to conduct. The sequencer driver current into the base of transistor Q6, similarly causes conduction of the sequencer gate. Without the row or column drive the gate could not conduct. Resistor R3 connected to -15V prevents emitter base breakdown of Q5 when Q4 is not conducting. Resistors R4, R5, and R6 provide failure isolation short circuit protection to the remainder of the system and the input transducer in case of any catastrophic failure (short circuit) in any input tier MOS FET.

When system power is off the most positive input sample voltage in any tier of five channels will flow through R5 from the source body diode of the input MOS FET to bias the now common five MOS FET gates off to prevent the input from conducting. D1 allows this circuit to be biased positive since the +20V line is now near ground potential.

#### 2.3 Analog-to-Digital Converter

The analog-to-digital converter (ADC or coder) provides the highest accuracy possible commensurate with minimum size and power consumption. The A/D converter utilizes integrated circuits for all active circuit devices and discrete components for the resistance ladder and bias networks. A feedback correction loop compensates for offset and drift produced by the tolerances and temperature coefficients and integrated circuit resistors. The gain control circuitry utilizing discrete components combined with a precision resistance ladder network acts to stabilize performance for temperature changes.



Figure 2.2.1. Analog Gating Circuitry

The A/D converter design performed with a total error of less than  $\pm 0.05\%$  (2.5 mv) over the temperature range of  $-35^{\circ}$ C to  $+71^{\circ}$ C and a temperature transient to  $+100^{\circ}$ C during the Qualification Test Program. The A/D converter consumes 550 milliwatts of power and is packaged in a module less than two cubic inches in volume.

Five basic microelectric building blocks are used in the A/D converter. The primary unit is a general purpose single-ended operational type amplifier. Six of these amplifiers are used in the design. The remaining microelectronic units are: dual analog type PNP transistors with various collector and emitter resistances available for each transistor, the complement with NPN transistors, PNP choppers, and NPN choppers. Four dual PNP flat packs and seven dual NPN flat packs are used in the A/D converter. These are to be used primarily for constructing differential amplifiers and for MOS gate drivers. Two flat packs each containing four NPN and PNP chopper transistors are used. These units switch the reference voltage across the precision resistance ladder.

#### 2.3.1 Analog-to-Digital Converter Operation

The A/D converter consists of five functional circuits as shown in Figure 2.3.1. These circuits are: input, error amplifier and clamp, output amplifier and clamp, precision reference generator and ladder and switches circuitry.

The operating cycle is divided into three intervals. They are: the clamp interval, the multiplexer settling interval, and the coding interval. During the clamp interval, the input is shorted to -19.6 mv, allowing the feedback correction loop to null to this voltage. During the settling interval, the desired analog channel voltage is switched to the input and allowed to rise to its full value. This voltage is converted to an 8-bit binary code during the coding interval.

Regardless of the selected bit rate, the first two bit periods of each word are used for the clamp interval. At the start of "bit 1", switch S1 closes and connects the input to -19.6 millivolts. Five microseconds later, switch S2 closes and connects the error amplifier output to the clamp amplifier input starting the action of nulling offset. This state is held until microseconds before the end of "bit 2" (30 microseconds at the 51.2 kc bit rate), then switch S2 opens followed 5 microseconds later by switch S1.

The desired channel gate is closed applying an input voltage and half scale current to the summing bus. This current is held for 25 microseconds allowing the analog input to rise and the summing bus to reach its proper net current. At the end of the 25 microsecond period, the current on the bus equals the converted analog current minus half scale current. The polarity of this converted current determines



Figure 2.3.1. Analog-To-Digital Converter. Block Diagram

the polarity of the error amplifier output voltage depending upon whether the input voltage is greater or less than half scale. In addition, the polarity of the converted current determines the state of the steer inputs to the error amplifier flip-flop.

At the end of settling time, a coder clock transition occurs setting the error amplifier flip-flop to the previously determined state. If the analog input is greater than half scale, the flip-flop output goes negative. Two and one-half microseconds later, the programmer removes the half-scale current from the bus if it is greater than the converted analog current or leaves it on if it is less. Simultaneously, the quarter-scale current is commanded onto the bus. The error amplifier is then allowed 7.5 microseconds to decide the polarity of the new net current on the summing bus before another coder clock transition occurs. Again, 2.5 microseconds later, the programmer acts upon the decision either removing or leaving the quarter scale current and commanding the 1/8 scale current onto the bus. The decision-action cycle is repeated at 10 microsecond intervals for the 1/16, 1/32, 1/64, 1/128, and 1/256 scale currents. The time between the 1/2 scale current decision and the 1/256 scale current decision is 70 microseconds. At the end of this 70 microsecond period, by observing which currents were retained on the bus and which were rejected, the value of the applied analog signal is determined to within the accuracy limits of the system.

Seven and one-half microseconds after the last decision is made, the channel gate opens removing the analog input. During the last half of "bit 8", the code representing the channel voltage is read into the output register. Five micro-seconds later, switch S1 is closed starting the cycle for another channel.

As the bit rate is reduced from 51.2 kilocycles, the settling period and coding period remain constant at 25 microseconds and 70 microseconds, respectively. The clamp period and period between the final decision and coder read out expands to cover the longer word times. Concurrently, the clamp interval is maintained at 25% of the word length.

#### 2.3.2 ADC Circuit Description

#### 2.3.2.1 Input Circuitry

Referring again to Figure 2.3.1, the input circuitry consists of two amplifiers, A1 and A2, and the gain adjust resistor. A1 and A2 are general purpose amplifiers (GPA) connected for unity voltage gain. The input circuitry presents a high input impedance to the analog signal and converts the input analog voltage to a precision analog current. The high input impedance is accomplished through use of a constant current source in the emitter circuit and boot strapping the collector of the input transistor. As shown in Figure 2.3.2.1, the voltage-to-current conversion is accomplished as follows:

- a. A voltage present between the input terminals (analog PAM and analog signal ground) is impressed directly across the gain resistor resulting in a current flow through the resistor.
- b. This current flows plus to minus into the output terminal of A2. There is a 1-milliampere current sink at the output terminal of A2.
- c. Therefore, the current flowing through the gain resitor (11) and the collector current of Q1 and Q2 (12) totals 1 milliampere.

Note that any incremental increase in 11 results in the same increment of decrease in 12 and that this change in 12 is a direct function of the analog input voltage. Current 12 is the analog input current to the summing bus.

#### 2.3.2.2 Error Amplifier

The error amplifier is composed of amplifiers A3 and A4 and associated feedback circuitry. The clamp circuitry consists of amplifier A7, switches S1 and S2 and the capacitor and two resistors associated with amplifier A7. General purpose amplifier, A3, and associated feedback circuitry forms an inverting current-to-volt-age converter with a transfer function of  $-10^4$  volts per ampere. Amplifier A4 is connected as an inverting voltage gain amplifier with a gain of -10. These amplifiers measure any net current on the summing bus and transfer it to a proportional voltage at the output of amplifier A4. The diodes in the feedback circuits of the two amplifiers limit the output voltage swing to  $\pm 0.6$  volts and provide a path for excess input current preventing the amplifiers from saturating, therefore, maintaining high switching speed.

General purpose amplifier A7, in conjunction with the input resistor and feedback capacitor, forms an integrator. Switches S1 and S2 are analog MOS gate switches. Their drivers are built with the dual NPN and dual PNP units. With switches S1 and S2 closed, amplifier A7 senses the output of amplifier A4 and feeds a current back to the summing bus until the difference between amplifier A4 output voltage and Analog Common (+10V) is zero, thereby nulling the net current on the



Figure 2.3.2.1. Voltage to Current Conversion

summing bus to zero. When switches S1 and S2 open, the null current is retained by the memory capability of A7 and the feedback capacitor. This operation essentially nulls out any voltage offset in the input buffers and the error amplifier. Offsets beyond this point are desensitized by the gain factor of the error amplifier.

#### 2.3.2.3 Output Amplifiers and Clamp

The output amplifier and clamp consists of amplifiers A5, A6 and the error amplifier flip-flop. Amplifiers A5 and A6 are differential voltage amplifiers with gains of 150 and 50 respectively. They are formed with the dual PNP micro-electronic unit.

Amplifiers A5 and A6 amplify a differential voltage between the output of amplifier A4 and Analog Common (+10V) to a sufficient level to effectively steer the flip-flop. Upon receipt of a clock pulse, the flip-flop assumes the output dictated by the steers and supplies this output to the programmer for use in the digital feedback loop.

#### 2.3.2.4 Precision Reference Generator

This block is composed of the reference voltage generator and amplifier A8. The primary reference voltage element is a 6.4 volts zener diode temperature compensated to 0.0005% change per  $^{\circ}$ C. The purpose of the other circuitry involved in the generation is to maintain a precision current of 500 microamps through the diode. General purpose amplifier A8 is connected for unity voltage gain and buffers the reference voltage, effectively reducing the output impedance to a point where the bit currents supplied from this source have no effect on gain. The resulting reference voltage is a nominal +3.6 volts.

#### 2.3.2.5 Ladder and Switches

The ladder and switches circuitry consists of the eight ladder switches and the 17 resistor ladder network. The switches contain a digital driver and two complementary NPN and PNP chopper transistors. Upon command, a switch connects its ladder resistor to the reference voltage or to Analog Common. Low resistance, low offset choppers transistors are used to make the connection. The ladder resistors are .01%, 5 parts per million bulk film types. They are arranged so that connecting the resistor controlled by the 128 command to the reference voltage generates a current change on the summing bus equal to half scale (approximately 320 microamperes), and the resistor controlled by the 64 command generates a current change equal to one-quarter scale, etc. The offset adjust resistors connected to switch S1 are used to set the "zero" level of the coders so that the first bit switches in at zero volts input. This is done by setting the junction of the resistors to -19.6 millivolts and allowing the clamp to null to this value.

#### 2.4 Programmer

The programmer timing, as illustrated by Figure 2.4, is generated by two counter systems. The first counter system provides a fixed timing sequence for the coder operation. The second system provides a timing sequence for the analog multiplexer and output register at programmed bit rates from 51,200 to 800 cps. The prime timing reference is a crystal-controlled oscillator operating at 409.6 kilocycles per second. An eight stage binary counter divides the oscillator frequency to provide timing for the external bit rate program. In addition, these counters provide a fixed timing sequence for the analog-to-digital conversion; thus, the signal sample period is independent of the programmed bit rate.

The programmed bit rate timing is divided by a one stage buffer counter which provides the data rate timing; followed by a three stage 8-to-1 counter which generates the eight bit timing for each word. Three operations are performed during each eight bit word:

- 1. The coder correction cycle is performed during the first two bits of each word.
- The correction cycle is followed by an analog-to-digital conversion fixed time period of approximately 100 microseconds (30 microseconds MSD settle time and 70 microseconds for the eight conversion decisions).
- 3. The coder word is read into the output register by the digital multiplexer gates during the last half of bit eight.

Since the conversion period is constant, independent of bit rate, the eight stage counters providing this sequence are synchronized with the bit counters to begin a conversion cycle with the beginning of bit three of each word.

After the last conversion decision, all half-split weighted currents are gated OFF to reduce power while the digital code remains stored until the required parallel readout during bit eight. Since power is dissipated in the coder weighted currents and analog gates only during the fixed time conversion cycle, system power

![](_page_21_Figure_0.jpeg)

Figure 2.4. Programmer. Block Diagram

is actually reduced as bit rate is reduced. The one hundred word frame is generated by two ten stage shift registers which have feedback from output to input. These registers actually perform the functions of frequency division and a decoding matrix, thus, the analog gate row and column drivers may be driven directly from the register outputs. Each analog gate is energized by the coincidence of:

- 1. Row drive
- 2. Column drive
- 3. Analog gate duty cycle

The analog gate duty cycle energizes each gate for the required conversion time only.

The digital multiplexer gates the 8-bit encoded word into the output register by parallel read-in for each of the 98 analog words, and gates the preset sync code during the first two words of each data frame for frame synchronization.

The output register provides the parallel-to-serial conversion of each 8-bit encoded word and the frame sync code words. The NRZ serial output is shifted out of the register one-half bit delayed from all bit counter and word counter transitions. This allows accurate phasing of output transitions of data rate timing, NRZ serial data, and frame sync without introducing the delay of the word counters. The total delay between a data sample period and the serial output representing this data (including the time required to shift the word out of the register) is eight and one-half bits.

Output buffers provide independent outputs with low driving impedance and small propagation delay. These complementary output circuits provide low driving impedance in both the high and low states.

As mentioned previously, the bit rate may be externally programmed in the range from 800 to 51,200 cps. Any six of the following seven rates may be selected for wiring to the seven pin patch connector.

800 cps	12,800 cps
1,600 cps	25,600 cps
3,200 cps	51,200 cps
6,400 cps	

As the bit rate is changed from 800 to 51,200 cps, the sampling rates for the individual analog channels changes from 1 to 64 sps.

#### 2.5 Power Supply

The block diagram for the power supply is shown in Figure 2.5. The input LC filter provides filtering to minimize the input current ripple and to provide attenuation for conducted electromagnetic interference. The series switch is alternately opened and closed to the output LC filter. When the switch is not conducting, a diode provides a path for continuous current through the inductor. Thus, the input voltage is transformed to a continuous 16-volt output to the dc-to-dc converter input without the resulting losses of a series regulator. Higher efficiency and lower power dissipation within the power supply are obtained for the 24- to 32-volt input range. A preregulator consisting of a half-shot (RC circuit) controlled by the sampled input voltage controls the input series switch. Additional feedback is provided from the 16-volt output. This 16-volt output is compared to a reference diode and then amplified to control a free running multivibrator. The multivibrator provides an input to the half-shot circuit. Additional circuitry assures a 16-volt output within 5 milliseconds from power turn on to provide system power by enabling the multivibrator.

A dc-to-dc converter provides constant power to the output rectifiers. The dc-to-dc converter is synchronized with the basic 160-microsecond high-speed word rate to ensure noise-free operation during the analog-to-digital conversion process.

The output rectifiers provide system power to filter capacitors. A transistor rectifier is used on the 3.2-volt line to increase efficiency.

The power consumed by the PCM system is typically 1.7 volts at 28 vdc. The high efficiency of the sampling type preregulator maintains the power consumption essentially constant over the +24 to +32 vdc voltage range. As the bit rate is reduced from 51,200 to 800 cps the power consumption reduces from 1.7 to 1.4 watts.

![](_page_24_Figure_0.jpeg)

#### Figure 2.5. Power Supply. Block Diagram

## SECTION 3.0

## MECHANICAL DESCRIPTION

#### 3.0 MECHANICAL DESCRIPTION

The design approach for the packaging of the Micro PCM Telemetry System was developed giving careful consideration to the following criteria:

1. Maximum protection for the electronics during dynamic environments of vibration, shock, acoustic noise, etc.

2. Packaging techniques compatible with both discrete components and integrated circuits.

3. Efficient solution to the internal wiring problem normally present in this type equipment.

4. Minimum size and weight structure.

The selected design approach, which provided excellent performance during the extensive qualification test program, utilizes the compression packaging technique to achieve maximum protection for the electronics with a minimum size and weight housing. The integrated circuits in the system are mounted in a planar configuration to multilayer printed circuits for the multiplexer and programmer junctions, and in a cordwood configuration for the analog-to-digital-converter function. An epoxy molding process, which was developed and proved on a previous program, was used to encapsulate the integrated circuit flat packs for the cordwood configuration. This provides subassemblies with handling and fabrication characteristics equivalent to discrete components. In addition, a card-to-card interconnection technique was developed to efficiently fulfill the internal wiring function.

#### 3.1 Physical Description

Refereing again to Figure 1.0, the electronics of the PCM system are packaged in an aluminum-polyurethane foam housing. The physical details are shown in Figure 3.1, PCM Envelope dimensions. The volume of the system is 33 cubic inches and the weight is slightly less than 1.4 pounds.

The external finish of the box is a black, wrinkle finish, baked enamel. This finish was chosen for its high emissivity characteristics and for its excellent durability.

All external connectors are Cannon Micro-K series. Two 55-pin and four seven-pin connectors are used. The connectors are discretely keyed by the selective blocking and/or removal of pins and sockets. Electromagnetic interference

shielding is accomplished by modification of the clamping barrel nuts of the mating connectors of the cable harness. The barrel nuts are lengthened in both directions in order to provide wiping action against the PCM housing on one end and to permit the attachment of a metallic braid termination on the other.

The system is mounted from underneath by inserting four 6-32 screws through a mounting plate into the inserts provided for this purpose (see figure 3.1).

#### 3.2 Housing Design

The basic mechanical housing for the PCM Telemetry System consists of a thin-walled, one piece reinforced aluminum machining. The entire housing is machined from solid stock in order to eliminate the tolerance and sealing problems normally associated with minimum weight structures.

The top and bottom panels are filled with polyurethane foam to provide both structural and thermal advantages. Structurally, the area moments of inertia of each panel are increased without increasing the weight of aluminum. This raises the fundamental resonant frequency of the panels and consequently lowers the displacement amplitude of the panels at resonance. Thermally, the insulating qualities of the polyurethane foam help protect the circuitry from rapid temperature transients as experienced during the specification requirement of a ten minute excursion to 230°F.

Sealing of the package for humidity protection is accomplished by use of the cover gasket and by the application of RTV silastic around each connector and connector screw at assembly. The package is not hermetically sealed but has a leak rate of approximately 1 pound per square inch per hour at a pressure differential of 5 pounds per square inch.

Electromagnetic interference radiation is also reduced by a metal-tometal contact at the housing-cover interface of the package.

#### 3.3 Compression Packaging

The successful use of the compression packaging technique on many Radiation PCM systems including Nimbus, OAO, Telstar, Titan III Airframe, Apollo, LEM and Lunar Orbiter contributed strongly to the decision to use this basic packaging technique for the Micro PCM Telemetry System.

A key feature of this technique is that the entire module stack is placed under a compressive load of 8 to 10 psi at the final system assembly. This compression yields a semi-rigit, "solid-mass" structure which possess excellent shock and vibration attenuation characteristics. Resonant amplifications of input vibrations NOTES:

1. ALL TOL TO BE  $\pm$ .005.

#### CONNECTOR ALLOCATION

![](_page_28_Figure_3.jpeg)

5|54|

![](_page_28_Figure_5.jpeg)

as low as 4 or 5 can be expected in a properly designed "compression package". This compares most favorably with amplifications of twenty or more usually encountered with more standard packaging methods.

The compressive force is applied by the top and bottom panels which, as discussed previously, are designed to provide this compression loading.

#### 3.4 Electronics Packaging

The system's electronics consists of three PC card subassemblies: a programmer assembly, an analog multiplexer assembly and a power supply/ analog-to-digital converter (ADC) assembly.

#### 3.4.1 Programmer Assembly

The programmer assembly, shown in Figure 3.4.1 installed in a checkfixture, consists of a multilayer board (6 layers), integrated circuit flat packs, bit rate connector and the card-mounted individual connector sockets. The multilayer card, designed and produced by Radiation Incorporated contains the complex wiring pattern required to interconnect the logic elements. The 98 monolithic integrated circuit flat packs attached to the PC card by the resistance soldering technique. Individual AMP connector sockets are attached to the card at its perimeter and the bit rate connector is hard wired to solder pads located at the front edge of the card.

This assembly provides the complete programming function for the PCM system with the exception of the crystal oscillator and six output buffer circuits.

#### 3.4.2 Analog Multiplexer Assembly

The analog multiplexer assembly shown in its completed form in Figure 3.4.2 is similar in design and construction to the programmer assembly. Sixty integrated circuit flat packs are attached to a six layer PC card. Two 55 pin connectors supply the analog input signals and the AMP connector sockets provide the necessary card-to-card connections.

This assembly provides the complete analog multiplexing function including the row and column drivers and MOS gate drivers.

![](_page_30_Picture_0.jpeg)

1064-8

![](_page_30_Figure_2.jpeg)

![](_page_31_Picture_0.jpeg)

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![](_page_31_Figure_2.jpeg)

#### 3.4.3 Power Supply/ADC Assembly

The power supply/ADC assembly is shown in Figure 3.4.3. Four welded modules are attached to a two-sided PC card. Three 7 pin connectors, one for the 28 volt power input and two for the PCM system outputs, are hard wired to the PC card. The individual connector sockets provide the necessary card-to-card connections.

The welded modules are fabricated by arranging electronic components in a cordwood fashion between thin Mylar sheets. Interconnections are made by welding nickel ribbon between component leads according to the ribbon routing paths printed on the Mylar sheets. The welded assembly is then encapsulated in a semirigid polyurethane foam.

The power supply comprises two of the four welded modules. These two modules were designed using conventional components

A buffer and oscillator module, using conventional components, provides a stable crystal-controlled clock to the programmer and six special buffer circuits for the PCM and timing outputs.

The last module, the analog-to-digital converter (ADC) consists of both integrated circuits and discrete components. Twenty-four integrated circuit flat packs, which includes all active circuits of the ADC, and 54 discrete components are packaged in the module. As discussed previously, all flat packs have nickel wires attached and special interconnections made on each device by the welding process. The units are then encapsulated in a hard epoxy to provide a subassembly which is more suitable for the cordwood packaging technique. The encapsulated subassemblies are then installed in the welded modules.

#### 3.4.4 Final Assembly Process

As shown in Figure 3.4.4 the three card assemblies are properly aligned and then interconected by installing the solid conductor feed-through wires in the individual card-mounted connectors. In addition to providing an efficient internal wiring function, these feed-through interconnection wires may be readily removed to expedite maintenance or troubleshooting, should this be necessary.

In order to provide access to as many electrical terminations as possible after the three cards are assembled, the bottom card (power supply/ADC) is oriented with the module solder pads on the outside facing down. The top card (programmer) has its planar flat packaged integrated circuits on the outside facing up. The center card (analog multiplexer) contains the analog gates and the gate driver functions

![](_page_33_Picture_0.jpeg)

![](_page_33_Figure_1.jpeg)

![](_page_34_Picture_0.jpeg)

1064-12

![](_page_34_Figure_2.jpeg)

which are available at the solder point wiring entries to the center card. Therefore, rapid and accurate isolation of malfunctions is possible during check-out prior to installation of the card stack within the housing.

The final assembly process is completed by installing this electronic card stack assembly in the housing and applying the compression loading by attaching the top cover.

## SECTION 4.0

## SPECIFICATIONS AND PERFORMANCE

#### 4.0 SPECIFICATIONS AND PERFORMANCE

The significant specifications which were used as the basis for the design of the MICRO PCM Telemetry System are listed in paragraph 4.1. As discussed previously, the performance of the system meets, and in most, cases exceeds all specifications. Typical performance data are presented in paragraph 4.2. Of particular importance are the size, weight, power consumption, accuracy and dynamic environment characteristics.

#### 4.1 Significant Specifications Number of Analog Input Channels 98 Signal Source 0 to 5 volts full scale 10,000 ohms or less Source Impedance Sampling Rate (Programmable) 1 to 64 samples per second Encoding 8-bit binary word **Output Format** NRZ type "C" 8-bits per word 100 words per frame Output Bit Rate Programmable at 800, 1600, 3200, 6400, 12,800,25,600 and 51,200 bits per second Output Impedance 100 ohms maximum Binary "1" = +5 volts +0.0 -0.5<sup>volts</sup> **Output Levels** Binary "0" = 0 volts +0.5 -0.0<sup>volts</sup> Accuracy $\pm 0.6\%$ , three sigma limits Weight 3.1 pounds Size 52 cubic inches Power Consumption 2.5 watts @ 28 VDC

4-1

Reliability	P <sub>s</sub> = 0.999 for 10-hour mission
Service Life	2000 hours with no maintenance or adjustments
Storage Life	36 months
Environmental	
Temperature	-30 <sup>o</sup> F to 230 <sup>o</sup> F
Altitude	10 <sup>-5</sup> mm Hg.
Acceleration	20 g's
Shock	50 g's for 11 milliseconds, half sine
Acoustic Noise	165 db random noise referenced to .0002 dynes/cm <sup>2</sup>
Vibration	15 g's RMS
O <sub>2</sub> Atmosphere	100% at 7 psia for 1 hour
Salt Spray	5% for 24 hours per MIL-STD-810
Humidity	97.5% <u>+</u> 2.5% RH at 80 <sup>0</sup> F to 160 <sup>0</sup> F for 24 hours

#### 4.2 Typical Performance Including Environmental Conditions

Output Bit Rate

Frequency Stability

Duty Cycle

Programmable at 800, 1600, 3200, 6400, 12,800, 25,600, 51,200 bits per second

+ 10 CPS @ 51.2 KC

50% + ,5%

No effect upon format, performance, or accuracy

#### Digital Outputs

Digital Output Impedance

70 ohms

Digital Output Levels

Binary One Binary Zero

Amplitude Stability

Rise Time Fall Time < 0.1 volt + 1%

+ 0.2%

4.8 volts

0.2 microsecond 0.1 microsecond

Analog Characteristics

Accuracy

Imput Impedance

During Sampling Non-Sampling System "OFF" > 3 Meg ohms > 600 Meg ohms > 600 Meg ohms

Fault Voltage with No Effect on Performance

Weight

Size

Power

Reliability

Service Life

Storage Life

Environmental

-1.0 volt to +16 volts

1.4 pounds

33 cubic inches

1.7 watts @28 VDC

P<sub>c</sub> = 0,999 for 10 hour missions (predicted)

No periodic maintenance or adjustments required

36 months (predicted)

The Micro PCM Telemetry System was qualified to the environments of paragraph 4.1 during a formal – customer approved Qualification Test Program

#### 4.3 Electromagnetic Interference Characteristics

The Micro PCM Telemetry System was designed to meet the requirements of MIL-I-26600, MIL-I-6181 and the 50 volt power source transient requirement of the MSC-ASPO-EMI-10A addendum to MIL-I-26600. During the Qualification Test Program the system was tested to the above requirements and met or exceeded all specifications. After the completion of the Qualification Test Program the system was tested to all the requirements of the MSC-ASPO-EMI-10A Addendum to MIL-I-26600. The unit met or exceeded all requirements of this specification. Detailed electromagnetic interference performance characteristics are available in a separate report.

4-4

## APPENDIX A-1

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### INTERFACE REQUIREMENTS

BY

## CONNECTOR - PIN - FUNCTION

Power	Connector	

Brown Color Dot

Pin	Function
1	NC – Keying Pin
2	Power Ground
3	Signal Ground Point
4	Power Ground
5	+28V Input
6	Chassis Ground
7	NC

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#### Analog Input Connector

Red Color Dot

Pin	Function	Pin	Function
	NC - Keying Pin	29	Channel 73
2	Analog Ground	30	Channel 31
3	Analog Ground	31	Channel 33
4	Channel 75	32	Channel 65
5	Channel 91	33	Channel 85
6	Channel 93	34	Channel 82
7	Channel 94	35	Channel 34
8	Analog Ground	36	Channel 95
9	Analog Ground	37	Channel 54
10	Channel 22	38	Channel 52
11	Channel 21	39	Analog Ground
12	Channel 5	40	Channel 63
13	Channel 4	41	Channel 61
14	Channel 72	42	Channel 43
15	Channel 14	43	Channel 41
16	Channel 74	44	Channel 3
17	Channel 45	45	Channel 71
18	Channel 25	46	Channel 11
19	Channel 24	47	Channel 13
20	Channel 23	48	Channel 15
21	Channel 81	49	Channel 32
22	Channel 83	50	Channel 92
23	Channel 84	51	Channel 35
24	Channel 64	52	Channel 55
25	Channel 62	53	Channel 53
26	Channel 44	54	Channel 51
27	Channel 42	55	Channel 49
28	Channel 12		

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## Data Rate Select

Orange Color Dot

Pin	Function
1	Data Rate Select Return
2	800 cps
3	1.6 KC
4	3.2 KC
5	6.4 KC
6	12.8 KC
7	25.6 KC

J3

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J4	Analog I	nput Connector	Yellow Color D
Pin	Function	Pin	Function
	Channel 48	29	Channel 46
2	Analog Ground	30	Channel 17
3	Analog Ground	31	Channel 19
4	Keying Pin NC	37	Channel 79
5	Channel 67	33	Channel 59
6	Channel 68	34	Channel 100
7	Analog Ground	35	Channel 98
8	Analog Ground	36	Channel 96
9	Channel 66	32	Channel 36
10	Channel 86	38	Channel 77
11	Channel 57	39	Channel 76
12	Channel 56	40	Channel 37
13	Channel 40	41	Channel 60
14	Channel 39	42	Channel 58
15	Channel 38	43	Channel 99
16	Analog Ground	44	Channel 97
17	Channel 29	45	Channel 80
18	Channel 50	46	Channel 78
19	Channel 69	47	Channel 9
20	Channel 70	48	Channel 7
21	Channel 90	49	Channel 47
22	Channel 89	50	Channel 16
23	Channel 88	51	Channel 18
24	Channel 87	52	Channel 20
25	Channel 27	53	Channel 30
26	Channel 10	54	Channel 28
27	Channel 8	55	Channel 26
28	Channel 6		

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Dot

15	#1 Digita	l Outputs Green Color Dot
Pin		Function
1		NC
2		NC - Keying Pin
3		Serial Data No. 1 Output
4		Frame Rate Timing No. 1 Output
5		Data Rate Timing No. 1 Output
6		PCM Grd. No. 1
7		NC

A1-5

J6	#2 Dig	ital Outputs	Blue Color Do
Pin		Function	
1		NC	
2		NC	
3		Serial Data No.	2 Output
4		Frame Rate Timin	g No. 2 Output
5		Data Rate Timing	No. 2 Output
6		PCM Grd. No. 2	2
7		NC - Keying Pir	1

## APPENDIX A-2

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#### INTERFACE REQUIREMENTS

BY

## FUNCTION - CONNECTOR - PIN

## POWER

Function

+ 28V Input

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Connector	Pin
JI	5

## GROUNDS

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Function	Connector	Pin
Power Grd.	JI	2
Signal Grd. Pt.	JI	3
Power Grd	٦١	4
Chassis Grd	JI	6
Data Grd	J2	2
Data Grd	J2	3
Data Grd	J2	8
Data Grd	J2	9
Data Grd	J2	39
Data Grd	J4	2
Data Grd	J4	3
Data Grd	J4	7
Data Grd	J4	8
Data Grd	J4	16
PCM Grd #1	J5	6
PCM Grd #2	J6	6

## DIGITAL SIGNALS

Function	Connector	Pin
Serial Data No. 1 Output	J5	3
Frame Rate Timing No. 1 Output	J5	4
Data Rate Timing No. 1 Output	J5	5
Serial Data No. 2 Output	J6	3
Frame Rate Timing No. 2 Output	J6	4
Data Rate Timing No. 2 Output	J6	5
Data Rate Select Ret.	J3	1
800 cps	J3	2
1.6 KC	J3	3
3.2 KC	J3	4
6.4 KC	J3	5
12.8 KC	J3	6
25.6 KC	J3	7

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## ANALOG INPUTS

Function	Connector	Pin
Channel 3	J2	44
Channel 4	J2	13
Channel 5	J2	12
Channel 6	J4	28
Channel 7	J4	48
Channel 8	J4	27
Channel 9	14	47
Channel 10	14	26
Channel 11	.12	46
Channel 12	J2	28
Channel 13	J2	47
Channel 14	J2	15
Channel 15	J2	48
Channel 16	J4	50
Channel 17	J4	30
Channel 18	J4	51
Channel 19	J4	31
Channel 20	J4	52
Channel 21	J2	11
Channel 22	J2	10
Channel 23	J2	20
Channel 24	J2	19
Channel 25	J2	18
Channel 26	J4	55
Channel 27	J4	25
Channel 28	14	54
Channel 29	J4	17
Channel 30	J4	53
Channel 31	J2	30
Channel 32	J2	49
Channel 33	J2	31
Channel 34	J2	35
Channel 35	J2	51
Channel 36	J4	32
Channel 37	J4	40
Channel 38	J4	15
Channel 39	J4	14
Channel 40	J4	13
Channel 41	J2	43
Channel 42	J2	27
Channel 43	J2	42
Channel 44	J2	26
Channel 45	J2	17

## ANALOG INPUTS (Continued)

Function	Connector	Pin
Channel 46	J4	29
Channel 47	4ر	49
Channel 48	4ل	1
Channel 49	J2	55
Channel 50	4ل	18
Channel 51	J2	54
Channel 52	J2	38
Channel 53	J2	53
Channel 54	J2	37
Channel 55	J2	52
Channel 56	J4	12
Channel 57	4ل	11
Channel 58	٦4	42
Channel 59	4ل	33
Channel 60	4ل	41
Channel 61	J2	41
Channel 62	J2	25
Channel 63	J2	40
Channel 64	J2	24
Channel 65	J2	32
Channel 66	4ل	9
Channel 67	J4	5
Channel 68	4ل	6
Channel 69	4ل	19
Channel 70	4ل	20
Channel 71	J2	45
Channel 72	J2	14
Channel 73	J2	29
Channel 74	J2	16
Channel 75	J2	4
Channel 76	J4	39
Channel 77	J4	38
Channel 78	J4	46
Channel /9	J4	37
Channel 80	J4	45
	JZ	21
Channel 82	JZ	34
Channel 83	JZ	22
Channel 84	JZ	23
Channel 83	JZ	33
Channel 80	J4	10
Ungnnel 0/	4	24

## ANALOG INPUTS (Continued)

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Function	Connector	Pi	n
Channel 88	J4		23
Channel 89	J4		22
Channel 90	J4		21
Channel 91	J2		5
Channel 92	J2		50
Channel 93	J2		6
Channel 94	J2		7
Channel 95	J2		36
Channel 96	J4		36
Channel 97	J4		44
Channel 98	J4		35
Channel 99	J4		43
Channel 100	J4		34

## NO CONNECTIONS

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Function	Connector	Pin
Keying Pin	JI	1
NĆ	J	7
Keying Pin	J2	1
Keying Pin	J4	4
NC	J5	1
Keying Pin	J5	2
NC	J5	7
NC	J6	1
NC	J6	2
Keying Pin	JG	7

OUTPUT FORMAT

APPENDIX B

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## APPENDIX B

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## OUTPUT FORMAT

Word No.	Input		Word No.	Input	
1	Sync Code		42	Analog Channel	42
2	Sync Code		43	Analog Channel	43
3	Analog Channel	3	44	Analog Channel	44
4	Analog Channel	4	45	Analog Channel	45
5	Analog Channel	5	46	Analog Channel	46
6	Analog Channel	6	47	Analog Channel	47
7	Analog Channel	7	48	Analog Channel	48
8	Analog Channel	8	49	Analog Channel	49
9	Analog Channel	9	50	Analog Channel	50
10	Analog Channel	10	51	Analog Channel	51
11	Analog Channel	11	52	Analog Channel	52
12	Analog Channel	12	53	Analog Channel	53
13	Analog Channel	13	54	Analog Channel	54
14	Analog Channel	14	55	Analog Channel	55
15	Analog Channel	15	56	Analog Channel	56
16	Analog Channel	16	57	Analog Channel	57
17	Analog Channel	17	58	Analog Channel	58
18	Analog Channel	18	59	Analog Channel	59
19	Analog Channel	19	60	Analog Channel	60
20	Analog Channel	20	61	Analog Channel	61
21	Analog Channel	21	62	Analog Channel	62
22	Analog Channel	22	63	Analog Channel	63
23	Analog Channel	23	64	Analog Channel	64
24	Analog Channel	24	65	Analog Channel	65
25	Analog Channel	25	66	Analog Channel	66
26	Analog Channel	26	67	Analog Channel	67
27	Analog Channel	27	68	Analog Channel	68
28	Analog Channel	28	69	Analog Channel	69
29	Analog Channel	29	70	Analog Channel	70
30	Analog Channel	30	71	Analog Channel	71
31	Analog Channel	31	72	Analog Channel	72
32	Analog Channel	32	73	Analog Channel	73
33	Analog Channel	33	74	Analog Channel	74
34	Analog Channel	34	75	Analog Channel	75
35	Analog Channel	35	76	Analog Channel	76
36	Analog Channel	36	77	Analog Channel	77
3/	Analog Channel	37	78	Analog Channel	78
38	Analog Channel	38	79	Analog Channel	79
39	Analog Channel	39	80	Analog Channel	80
40	Analog Channel	40	81	Analog Channel	81
41	Analog Channel	41	82	Analog Channel	82

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## APPENDIX B

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## OUTPUT FORMAT (Continued)

Word No.	Input		Word No.	Input	
83	Analoa Channel	83	92	Analog Channel	92
84	Analog Channel	84	93	Analog Channel	93
85	Analog Channel	85	94	Analog Channel	94
86	Analog Channel	86	95	Analog Channel	95
87	Analog Channel	87	96	Analog Channel	96
88	Analog Channel	88	97	Analog Channel	97
89	Analog Channel	89	98	Analog Channel	98
90	Analog Channel	90	99	Analog Channel	99
91	Analog Channel	91	100	Analog Channel	100

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#### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART

#### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART

INPUT ANALOG (MV)

#### LOWER SWITCHING POINT OF DIGITAL CODE

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	Decimal	Binary
0.000	1	0000001
19.685	2	00000010
39.370	3	00000011
59.055	4	00000100
78.740	5	00000101
98.425	6	00000110
118.110	7	00000111
137.795	8	00001000
157.480	9	00001001
177.165	10	00001010
196.850	11	00001011
216.535	12	00001100
236.220	13	00001101
255.905	14	00001110
275.590	15	00001111
295.275	16	00010000
314,960	17	00010001
334,645	18	00010010
354,330	19	00010011
374.015	20	00010100
393.700	21	00010101
413.385	22	00010110
433.070	23	00010111
452.755	24	00011000
472.440	25	00011001
492.125	26	00011010
511.810	27	00011011
531.495	28	00011100
551,180	29	00011101
5/0.865	30	00011110
370,550	31	00011111
010.233	32	0010000
029,920	33	00100001
047.005	34	00100010

## THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MV)	LOWER SWITCHING POINT	OF DIGITAL CODE
	Decimal	Binary
669.291	35	00100011
688.976	36	00100100
708.661	37	00100101
728.346	38	00100110
748.031	39	00100111
767.716	<sup>*</sup> 40	00101000
787.401	41	00101001
807.086	42	00101010
826.771	43	00101011
846.456	44	00101100
866.141	45	00101101
885.826	46	00101110
905.511	47	00101111
925.196	48	00110000
944.881	49 -	00110001
964.566	50	00110010
984.251	51	00110011
1003.936	52	00110100
1023.621	53	00110101
1043.306	54	00110110
1062.991	55	00110111
1082.676	56	00111000
1102.361	57	00111001
1122.046	58	00111010
1141.731	59	00111011
1161.416	60	00111100
1181.101	61	00111101
1200.786	62	00111110
1220.471	63	00111111
1240.156	64	0100000
1259.841	65	0100001
1279.526	66	01000010
1299.211	67	01000011
1318.897	68	01000100
1338.582	69	01000101
1358.267	70	01000110

## THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

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INPUT ANALOG (MV)	LOWER SWITCHIN	NG POINT OF DIGITAL CODE
	Decimal	Binary
1377.952	71	01000111
1397.637	72	01001000
1417.322	73	01001001
1437.007	74	01001010
1456.692	75	01001011
1476.377	76	01001100
1496.062	77	01001101
1515.747	78	01001110
1535.432	79	01001111
1555.117	80	01010000
1574.802	81	01010001
1594.487	82	01010010
1614.172	83	01010011
1633.857	84	01010100
1653.542	85	01010101
1673.227	86	01010110
<b>16</b> 92.912	87	01010111
1712.597	88	01011000
1732.282	89	01011001
1751.967	90	01011010
1771.652	91	01011011
1791.337	92	01011100
1811.022	93	01011101
1830.707	94	01011110
1850.392	95	01011111
1870.077	96	01100000
1889.762	97	01100001
1909.447	98	01100010
1929.132	99	01100011
1948.817	100	01100100
1968.503	101	01100101
1 <b>98</b> 8.188	102	01100110
2007.873	103	01100111
2027.558	104	01101000
2047.243	105	01101001

## THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MV)	LOWER SWITCHING	LOWER SWITCHING POINT OF DIGITAL CODE		
	Decimal	Binary		
2066.928	106	01101010		
2086.613	107	01101011		
2106.298	108	01101100		
2125.983	109	01101101		
2145.668	110	01101110		
2165.353	111	01101111		
2185.038	112	01110000		
2204.723	113	01110001		
2224.408	114	01110010		
2244.093	115	01110011		
2263.778	116	01110100		
2283.463	117	01110101		
2303.148	118	01110110		
2322.833	119	01110111		
2342.518	120	01111000		
2362.203	121	01111001		
2381.888	122	01111010		
2401.573	123	01111011		
2421.258	124	01111100		
2440.943	125	01111101		
2460.628	126	0111110		
2480.313	127	0111111		
2499.998	128	1000000		
2519.683	129	1000001		
2539.368	130	10000010		
2559.053	131	10000011		
2578.738	132	10000100		
2598.423	133	10000101		
2618.108	134	10000110		
2637.794	135	10000111		
2657.479	136	10001000		
2677.164	137	10001001		
2696.849	138	10001010		
2716.534	139	10001011		
2736.219	140	10001100		

#### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MV)

#### LOWER SWITCHING POINT OF DIGITAL CODE

	Decimal	Binary
2755.904	141	10001101
2775.589	142	10001110
2795.274	143	10001111
2814.959	144	10010000
2834.644	145	10010001
2854.329	146	10010010
2874.014	147	10010011
2893.699	148	10010100
2913.384	149	10010101
2933.069	150	10010110
2952.754	151	10010111
2972.439	152	10011000
2992.124	153	10011001
3011.809	154	10011010
3031.494	155	10011011
3051.179	156	10011100
3070.864	157	10011101
3090.549	158	10011110
3110.234	159	10011111
3129.919	160	10100000
3149.604	161	10100001
3169.289	162	10100010
3188.974	163 =	10100011
3208.659	164	10100100
3228.344	165	10100101
3248.029	166	10100110
3267.714	167	10100111
3287.400	168	10101000
3307.085	169	10101001
3326.770	170	10101010
3346.455	171	10101011
3366.140	172	10101100
3385.825	173	10101101
3405.510	174	10101110
3425.195	175	10101111
3444.880	176	10110000

#### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MV)	LOWER SWITCHING POIN	T OF DIGITAL CODE
	Decimal	Binary
3464, 565	177	10110001
3484, 250	178	10110010
3503,935	179	10110011
3523,620	180	10110100
3543, 305	181	10110101
3562,990	182	10110110
3582,675	183	10110111
3602, 360	184	10111000
3622,045	185	10111001
3641,730	186	10111010
3661.415	187	10111011
3681,100	188	10111100
3700, 785	189	10111101
3720.470	190	10111110
3740.155	191	10111111
3759.840	192	11000000
3779.525	193	11000001
3799.210	194	11000010
3818.895	195	11000011
3838.580	196	11000100
3858.265	197	11000101
3877.950	198	11000110
3897.635	199	11000111
3917.320	200	11001000
3937.006	201	11001001
3956.691	202	11001010
3976.376	203	11001011
3996.061	204	11001100
4015.746	205	11001101
4035.431	206	11001110
4055.116	207	11001111
4074.801	208	11010000
4094.486	209	11010001
4114.171	210	11010010
4133.856	211	11010011
4153 541	212	11010100

### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MV)	LOWER SWITCHIN	IG POINT OF DIGITAL CODE
	Decimal	Binary
4173.226	213	11010101
4192.911	214	11010110
4212.596	215	11010111
4232.281	216	11011000
4251.966	217	11011001
4271.651	218	11011010
4291.336	219	11011111
4311.021	220	11011100
4330.706	221	11011101
4350.391	222	11011110
4370.076	223	11011011
4389.761	224	11100000
4409.446	225	11100001
4429.131	226	11100010
4448.816	227	11100011
4468.501	228	11100100
4488.186	229	11100101
4507.871	230	11100110
4527.556	231	11100111
4547.241	232	11101000
4566.926	233	11101001
4586.611	234	11101010
4606.296	235	11101011
4625.982	236	11101100
4645.667	237	11101101
4665.352	238	11101110
4685.037	239	11101111
4704.722	240	11110000
4724.407	241	11110001
4744.092	242	11110010
4763.777	243	11110011
4783.462	244	11110100
4803.147	245	11110101
4822.832	246	11110110

#### THEORETICAL INPUT ANALOG TO OUTPUT CODE CONVERSION CHART (Continued)

INPUT ANALOG (MC)	LOWER SWITCHING POINT OF DIGITAL CODE		
	Decimal	Binary	
4842.517	247	11110111	
4862.202	248	11111000	
4881.887	249	11111001	
4901.572	250	11111010	
4921.257	251	11111011	
4940.942	252	11111100	
4960.627	253	11111101	
4980.312	254	1111110	
4999.997	255	1111111	

![](_page_68_Picture_0.jpeg)