

# Saturn Preflight Program Verification Plan

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## Saturn Preflight Program Verification Plan

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PART I

BASELINE PROGRAM VERIFICATION REQUIREMENTS

PART I  
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## SECTION 1

### GENERAL PREFLIGHT VERIFICATION

#### 1.1 INTRODUCTION

The LVDC Preflight Verification Plan outlines the procedures which require the LVDC Preflight Program to use all of its program logic. An LVDC preflight routine performs its function by executing a set of program logic.

The only variations from a fixed logic path are determined by:

- RCA-110A input word options
- Error conditions

Verification of the LVDC Preflight Program is divided into two parts:

- General Preflight Routines
- Prepare to Launch

The first part is divided into Nominal Conditions and Error Conditions. In the Nominal Conditions verification, variations introduced by RCA-110A input word options are exercised. The combination of options selected for input to the preflight routine requires the routine to perform all of its functions.

In the Error Conditions verification, variations introduced by anomalies are exercised. The LVDC preflight routines which respond to error conditions are exercised. Each RCA-110A input word error or each hardware performance error tested by the routine is generated by the control program.

In the Prepare to Launch verification, the same requirements apply to the input as in the nominal and error conditions verification of the General

Preflight Routines. That is, the input exercises the functions of the routine for both nominal and error conditions. However, the launch criticality of the monitor functions of the Prepare to Launch routine necessitates an emphasis on the test status of external inputs to the routine. Thus, the plan details the contents of external inputs such as discrete inputs, discrete input spares, staging interrupts, accelerometers, and gimbals.

## 1.2 GENERAL REQUIREMENTS

### 1.2.1 Program Functional Requirements

#### 1.2.1.1 General Preflight Routines

The LVDC Preflight Program performs the following functions under control of the SLCC:

- Load and/or verify the LVDC memory.
- Exercise, monitor, and verify internal functions of the LVDC and LVDA.
- Exercise and/or monitor selected Instrument Unit subsystems.
- Participate in overall guidance and control system tests.
- Perform limited data processing for the Launch Computer Complex.

These preflight routines are versatile and flexible in that they are adaptable to prelaunch conditions for the entire Saturn series of missions as presently conceived.

In conjunction with the launch complex computer, these routines provide the following subsystem checkout capabilities.

- Operational checkout of the LVDC.
- Operational checkout of the LVDA.
- Operational checkout of the Switch Selector - LVDA interface.
- Operational checkout of the accelerometer and gimbal angle processing features.
- Operational checkout of the vehicle discretes.
- Operational checkout of the LVDA/PCM interface.

#### 1.2.1.2 Prepare to Launch

The PTL program's primary functions during prelaunch testing and launch countdown are:

- Checks active interrupt and discrete input status.
- Checks Sim Flight Indicator status.
- Checks validity of input data used to compute azimuth.
- Computes azimuth and checks to see if it is within limits.
- Checks platform output data for validity.
- Checks LVDC/LVDA internal hardware status.

### 1.2.2 Verification Requirements

#### 1.2.2.1 General Preflight Routines

The functions of these routines are verified by exercising variations introduced through the RCA-110A input word option. The combination of options selected for input to each routine requires the routine to perform all of its functions. Correct error detection logic of the routines is confirmed by simulating error conditions and verifying the proper error telemetry.



#### 1.2.2.2 Prepare to Launch

The PTL verification effort is directed toward verifying the adequacy of the PTL program to perform the sequence of events which occur before Guidance Reference Release (GRR). Correct sequencing of the RCA-110A ground routine/flight program interface, proper GMT synchronization and azimuth management will be verified. Errors will be simulated during PTL to insure that all error detection logic is functioning correctly.

The PTL functions will be verified through analysis of logic tests designed to detect any implementation errors. Both nominal and perturbed configurations will be tested to exercise all logic paths and check for possible program interactions. Assurance that Discrete Output (DO) 13 (LVDC/LVDA Firing Commit Inhibit) will be set upon detection of errors in a subroutine entered from Prepare-to-Launch is obtained.

Assurance that program module interaction will not degrade the performance of the overall PTL program will be obtained through analysis of cases specifically designed to test both nominal and perturbed configurations of the program operating as a complete system.

#### 1.2.3 Applicable Document List

The specification documents used in the process of PTL program verification (see Appendix A) are the LVDC Preflight Program Descriptions document and the approved Program Change Requests (PCR's) for the mission. The Astrionics System Handbook is used for interpretation of requirements, and the Programmer's Operating Manual is used to interpret programming techniques.

## SECTION 2

### DETAILED VERIFICATION REQUIREMENTS

#### 2.1 INTRODUCTION

This section describes the verification requirements for the Preflight Program in detail. In many sections of this document, reference is made to the applicable sections of the Preflight Program Descriptions Document (Reference 1, Appendix A). This approach facilitates a cross reference between verification requirements and program specifications while, at the same time, providing a verification plan format suitable for conducting a verification effort.

#### 2.2 GENERAL PREFLIGHT ROUTINES

##### 2.2.1 Nominal Conditions

The Nominal Conditions section of General Preflight Verification requires the routines to execute all of their program logic. Successful execution under nominal conditions is indicated through the absence of any preflight error message. Also, the preflight routines which produce an output are verified by checking their output against expected values.

##### 2.2.1.1 Memory Load and Verification Programs

The following paragraphs illustrate how the various memory load and verifications techniques of the Preflight Program are verified.

#### 2.2.1.1.1 Sector Dump/Sector Sum Check

The functions of these routines are verified by forcing dumps and sum checks through the RCA-110A input word option and checking the results against dumps and sum checks performed by the the preflight simulator. Refer to paragraphs 3.1.6 and 3.1.7 of Reference 1, Appendix A for the specific requirements of these routines.

#### 2.2.1.1.2 Verify & Prepare to Load & Load Routines

These routines are verified by loading data into the LVDC and verifying the change. The contents of the telemetered control word is verified by the control program, and any failure is reported. Refer to paragraphs 3.1.4 and 3.1.5 of Refence 1, Appendix A.

#### 2.2.1.1.3 Special Loader

All the functions of the Special Loader routine are verified by exercising the routine and performing the same tests outlined in the two previous sections. Refer to paragraph 3.1.23 or Reference 1, Appendix A.

#### 2.2.1.1.4 Power Up Initialize Routine

This routine is verified by commanding its execution. Output is received only if there is an error. Refer to paragraph 3.1.1 of Reference 1, Appendix A.

#### 2.2.1.2 Guidance & Control System Test & Monitor Program

The following paragraphs present the methods used to verify the Guidance & control system test and monitor capabilities of the Preflight Program.

#### 2.2.1.2.1 Accelerometer Pulse Count Routine

Different pulse counts are specified, and all three axes are interrogated. The computed accelerometer rates are then verified to be within tolerance. Refer to paragraph 3.1.9 of Reference 1, Appendix A.

#### 2.2.1.2.2 CIU Read Routine

Twelve bit CIU addresses are input to the CIU Read Routine, and ten CIU data bits are supplied by the preflight simulator to the LVDC for each input. The corresponding data output by the routine is checked against expected output. Refer to paragraph 3.1.11 of Reference 1, Appendix A.

#### 2.2.1.2.3 Command Receiver Linkage and Commanded Flight Linkage Tests

The Command Receiver Linkage Routine is verified as follows. All preflight-flight interfaces are exercised through execution of DCS commands, and the control program verifies the Flight DCS Processor output data. It is assured that the Preflight Program does not interfere with the execution of repeatable flight simulation by commanding the Repeatable Flight Sim Linkage Routine and taking sum checks after repeatable flight simulation has completed. Refer to paragraphs 3.1.25 and 3.1.26 of Reference 1, Appendix A.

#### 2.2.1.2.4 Discrete Input and Discrete Output Monitor Routines

The Discrete Input Monitor Routine is verified by setting different bit patterns in the DIN, DIS, and ISR registers and checking for the expected output. The Discrete Output Monitor Routine is verified by setting bit patterns in the DOR and by specifying different Switch Selector Register outputs. Refer to paragraphs 3.1.14 and 3.1.15 of Reference 1, Appendix A.



#### 2.2.1.2.5 Exercise Attitude Command and G&C Steering Test Routines

The functions of these routines are verified by exercising the routines and comparing their pitch, roll, and yaw ladder outputs against expected values. Refer to paragraphs 3.1.12 and 3.1.13 of Reference 1, Appendix A.

#### 2.2.1.2.6 Gimbal Angle Monitor Routine

Simulated platform gimbal angle values are input to the Gimbal Angle Monitor Routine by the preflight simulator, and the corresponding data telemetered by the routine is verified by the simulator. Refer to paragraph 3.1.8 of Reference 1, Appendix A.

#### 2.2.1.2.7 Switch Selector Test Routine

The Switch Selector Routine is verified by specifying switch selectors to be driven by way of the RCA-110A input words of the routine. If the routine does not complete execution completely, an error message will be issued by the Preflight Program. Refer to paragraph 3.1.10 of Reference 1, Appendix A.

#### 2.2.1.2.8 Telemetry Test Routine

The functions of this routine are verified by exercising valid telemetry rates of the routine. Refer to paragraph 3.1.24 of Reference 1, Appendix A.

#### 2.2.1.3 LVDC/LVDA Test Programs

The following paragraphs illustrate the methods used in verifying the preflight routines designed to test specific functions of the LVDC/LVDA.



#### 2.2.1.3.1 DOM Test Routine

The functions of the DOM Test Routine are verified by executing the routine and monitoring DOM telemetry. Refer to paragraph 3.1.16 of Reference 1, Appendix A.

#### 2.2.1.3.2 Ladder Error Test Routine

The Ladder Error Test Routine is verified by commanding execution of the routine. Output is received only if there is an error. Refer to paragraph 3.1.1.17 of Reference 1, Appendix A.

#### 2.2.1.3.3 Memory Error Test Routine

The Memory Error Test routine is verified by commanding execution of the routine. Output is received only if there is an error present. Refer to paragraph 3.1.19 of Reference 1, Appendix A.

#### 2.2.1.3.4 Minor Loop Switch Selector and Real Time Counter Test Routine

The functions of this routine are verified by exercising the routine. Output is received only if there is an error. Refer to paragraph 3.1.18 of Reference 1, Appendix A.

#### 2.2.1.4 Automatically Called Routines and Subroutines

All other General Preflight Routines and Subroutines not previously specified in this document are automatically called from the routines listed in the verification procedures above or are called from the PTL program and are therefore verified when the requirements of these procedures are satisfied. Those routines or subroutines that are called from the PTL program are also tested, as described in the Prepare to Launch section of

this document. A cross reference table of preflight called routines and calling routines is presented in Appendix D.

The routines and subroutines automatically called from the General Preflight Routines are listed below. Refer to Reference 1, Appendix A for the specific functions of these routines.

- Accelerometer Monitor\*
- Control Word Execute\*
- Forced Begin
- Error Monitor\*
- HOP 400 Initialize
- Instruction Execute\*
- Interrupt Processing\*
- Issue Status Code\*
- LVDA Timing & Counter\*
- LVDC Self Test\*
- Mode Sort
- Output Interrupt Generate\*
- Output\*
- PTL Real Time Output\*
- Read Input Data\*
- Real Time Delta\*
- Resolver Error\*
- Sync Reset\*

\*Additional testing and verification are performed on these routines when the Prepare to Launch Routine is verified.

### 2.2.2 Error Conditions

The LVDC Preflight Error Conditions verification exercises all Preflight Program variations caused by recognition of error conditions. The preflight routines report the error conditions by the telemetry of error messages. The Error Conditions verification, therefore, exercises each routine of the LVDC Preflight Program which can telemeter error messages. The control program, used to perform the verification, forces the RCA-110A input word error or the hardware performance error tested for by each routine. The preflight routine telemetry is compared against expected, and any deviations are reported by the control program. Upon successful completion of the tests for a preflight routine, the error message telemetry received is printed.

Certain control program capabilities and limitations are pertinent to the error test definition. These include:

- The contents of COD counter 1 and 2 for any axis and any resolver may be specified in failure control counter 'A' and 'B'.
- Timing functions within the LVDA may be stopped while LVDC continues operation (DST discrete control). This control stops real time clock from incrementing and simultaneously stops timer 1 and 2 counters from decrementing.
- The rate at which accelerometers increment by channel and axis may be specified.
- The contents and operation of most registers internal to the LVDA can not be directly controlled. These include interrupt inhibit, interrupt limit, ladder error circuitry, and memory error circuitry functions.

- The preflight simulator control program can, however, identify execution of any PIO by the LVDC Preflight Program. The control program can stop execution, specify results of PIO by loading the LVDC accumulator and then restarting the LVDC Preflight Program. In this operation the LVDC Preflight Program timing is unaffected. Thus, the effect is a real time operation of the preflight routines where error conditions are supplied by a control program.

Appendix C lists the error message telemetry by routine and by sequence executed within the routine.

### 2.3 PREPARE TO LAUNCH

This section contains a detailed description of the methods applied to verify that the baseline Prepare to Launch program meets all functional requirements.

Nominal and error conditions verification of PTL are combined and described in the following paragraphs.

#### 2.3.1 LVDC/LVDA Internal Error Detection Verification

The PTL program's ability to correctly detect internal hardware malfunctions and perform the defined program action for a malfunction are verified as described in the following paragraphs.

##### 2.3.1.1 LVDA Timer and Counter Test

Verification that correct implementation of the LVDA timer and counter test (see Appendix A, Reference 1, 3.2.14) has been accomplished will be done through analysis of the perturbation cases described below. These cases are



designed to intentionally force execution of each error detection logic path. PTL program error telemetry analysis will be the primary instrument used to accomplish verification.

#### 2.3.1.1.1 Real Time Clock (RTC) Accuracy Test

Changes will be made to the clock read instructions (because the clock hardware can only be stopped) used to test the RTC accuracy. This method will enable verification of the error detection capability under all realistic error conditions. Positive and negative clock count bias and runaway errors will be simulated to demonstrate proper error detection.

#### 2.3.1.1.2 Timer 1 and Timer 2 Test

Analysis of the program listing is required to establish that the values used to test the timer 1 and timer 2 interrupt generating counters are of sufficient magnitude to fully exercise the hardware (numbers greater than  $2048_{10}$  must be used). Modification of these values will perturb the comparison between expected and actual interrupt receipt time, forcing positive and negative comparison error configurations. These tests will be run for both timers along with a test series created to checkout correct detection of a malfunction in the interrupt limit and inhibit registers. This test series will consist of forcing the presence of interrupt bits in the storage register, when the program flow requires that the interrupts should not be present. All possible error paths will be simulated to verify correct program action upon hardware malfunction detection.

#### 2.3.1.1.3 Accelerometer Optisyn Delay Line Test

Assurance that the PTL program can detect errors in the vertical, downrange, and crossrange accelerometer optisyn delay lines will be obtained through



analysis of a series of perturbations forcing reading errors above and below the specified two count tolerance. Both positive and negative differences in the A and B channel readings will be simulated for each platform axis.

#### 2.3.1.1.4 Crossover Detector (COD) Counter Test

All of the COD hardware logic tests and controlling Internal Control Register (ICR) bits will be exercised under nominal and perturbed conditions to verify the program's capability to correctly detect malfunctions. The counters will be configured such that the difference between the duplex counter readings will lie on each side of the specified tolerance of +3, -4 counts. It will be shown that differences outside the tolerance are treated as an error, and the proper action is executed and that the values within the tolerance are acceptable. Assurance that the subtract and limit circuitry checkout logic is functioning correctly will be obtained by disagreement bit monitoring with proper ICR setting. The disagreement bit inhibit feature will be exercised with the bit forced on to verify correct implementation of the associated error test. COD reading order reversal will be perturbed to cause the reading to appear not reversed with the required ICR setting to force this error path.

#### 2.3.1.2 LVDC Instruction Execution Test

The self test capability will be verified by using the instruction substitution method of testing to force execution of each error path. Further assurance that the logic implemented to test the correct execution of each instruction will be attained through analysis of the program listing. PTL program error telemetry will be analyzed in verification of the following functions. Requirements for this section are given in paragraph 3.2.13 of Appendix A.

#### 2.3.1.2.1 Transfer Operations

All conditional transfer instruction tests will be verified by forcing the accumulator to contain the required error condition. This will demonstrate both the validity of the test and proper execution of the associated error paths.

#### 2.3.1.2.2 Arithmetic Operations

Perturbations to the arithmetic tests will be accomplished by modifying the bit patterns within the constants used to verify the operation of the arithmetic logic circuits. All error paths will be exercised to verify the validity of test implementation.

#### 2.3.1.2.3 Multiply and Divide Operations

These functional checkout routines will be verified in the same manner as is described in 2.3.1.2.2.

#### 2.3.1.2.4 Memory Addressing

An analysis of the program listing will be required to verify that the memory addressing scheme complies with the desired objective of this part of the Selftest Routine. Assurance that the TLC interrupt is not inhibited during execution of a series of "CLA" instructions will be obtained during this analysis.

#### 2.3.1.3 Error Monitor Register (EMR) Test

Verification that the EMR is periodically telemetered during execution of the PTL program will be accomplished through analysis of real time telemetry. Verification of proper telemetry of error messages from specific routines and

setting of DO 13 is also accomplished by telemetry analysis. Paragraph 3.2.3 of Reference 1, Appendix A gives requirements for this routine.

#### 2.3.2 LVDA Digital Input Error Detection

These paragraphs describe how digital input error detection verification is accomplished. Digital input routines include the Interrupt Processing Routine and the Discrete Input Routine. The Discrete Input Routine reads both discrete inputs and discrete input spares. Inputs will be perturbed to verify all paths of error detection resulting from these inputs.

##### 2.3.2.1 Interrupt Detection

The following paragraphs describe the verification of interrupt detection which includes both interrupt processing (requirements given in paragraph 3.1.20 in Reference 1 of Appendix A) and interrupt storage register testing.

##### 2.3.2.1.1 Interrupt Processing

The Interrupt Processing Routine determines which interrupt occurred and directs the LVDC to the corresponding processing routine. Error messages will be forced by simulating an interrupt with no bit set in the interrupt storage register. Also, the TLC bit will be set in the accumulator with all interrupts inhibited, and the resulting interrupt error message will be verified.

##### 2.3.2.1.2 Interrupt Storage Register Testing

The interrupt storage register will be checked by setting all possible external interrupt bits and combinations of valid and invalid bits to insure no invalid bit is accepted. Any program error messages resulting from these tests will be verified.

#### 2.3.2.2 Discrete Input Detection

Discrete input detection is verified as described in the following paragraphs. The discrete inputs and discrete input spares are checked periodically by the Prepare to Launch Routine. The purpose of this check is to allow the launch computer to monitor the detection of discrete inputs and discrete input spares by the LVDC.

Verification of discrete settings is accomplished by setting all bits on in the discrete input register and also various combinations of bits. In addition, the routine is exercised with a single bit loaded in the discrete input register. This is done for each bit position in the register. Valid and non-valid bit positions are verified along with all error messages.

These tests are also performed using the discrete input spares register to verify correct detection of discrete input spares.

#### 2.3.3 Analog Input Error Detection

These paragraphs describe how the analog input error detection verification will be accomplished. The two analog inputs to the routines are the accelerometer data and the gimbal angle data. These data will be perturbed to verify all methods of error detection resulting from these inputs.

##### 2.3.3.1 Accelerometer Error Detection

The purpose of the Accelerometer Monitor Subroutine is to monitor the ST-124-M inertial platform accelerometers. The requirements for this subroutine are given in paragraph 3.2.8 in Reference 1 of Appendix A.



Accelerometer error detection will be verified by perturbations to the accelerometer readings by (1) initial accelerometer misalignments, (2) accelerometer constant bias errors, and (3) accelerometer scale factor errors. These perturbations will be used individually and in combinations to exercise all accelerometer error detection logic.

Program reaction will be verified through analysis of the error words resulting from detection of the accelerometer errors. Accelerometer off-level data will be included in these error words.

#### 2.3.3.2 Gimbal Angle Monitor

The purpose of the gimbal angle monitor routine is to accurately read platform attitude utilizing the multi-speed resolvers and the LVDA analog to digital converters. The requirements for this routine are given in paragraph 3.1.8 of Reference 1 of Appendix A.

Perturbations to gimbal angle readings are accomplished by (1) constant drift rate simulation and (2) constant bias simulation. Correct program reaction is verified by introducing all combinations of these perturbations and monitoring all error messages resulting from these perturbations. Both uncorrected gimbal angle readings and corrected gimbal angle readings are perturbed for fine, coarse, and backup gimbal resolver readings.

#### 2.3.4 Flight Ground Computer Interface

During the Prepare to Launch routine, the Verify and Prepare to Load routine is used to allow the RCA-110A ground checkout computer to load data into the LVDC memory or examine a memory location in the LVDC. The



subroutines used by the Verify and Prepare to Load routines are the Read Input Data, Issue Status Code, Output Interrupt Generate, and Sync Reset subroutines.

#### 2.3.4.1 Verify and Prepare to Load Routine

During the Prepare to Launch Routine, the Verify and Prepare to Load routine is issued to allow the RCA-110A ground checkout computer to load data into the LVDC memory or examine a memory location in the LVDC. The subroutines used by the Verify and Prepare to Load Routine are the Read Input Data, Issue Status Code, Output Interrupt Generate, and Sync Reset subroutines.

The Verify and Prepare to Load Routine has two distinct modes - the verify mode and prepare to load mode. The verify mode allows the launch computer to examine the contents of any LVDC memory location. The prepare to load mode allows the launch computer to load any LVDC memory location. The requirements for the Verify and Prepare to Load Routine are found in paragraph 3.1.4 of Reference 1, Appendix A.

The following paragraphs describe the method of verifying the Verify and Prepare to Load Routine.

##### 2.3.4.1.1 Issue Status Code Subroutine

Each commanded LVDC routine issues a status code indicating the present mode of operation to the launch computer. This subroutine is verified by checking telemetry for proper issuance of the status code after commanding

a known routine. The required 6 ms. delay in telemetry after issuing a status code will be verified. Paragraph 3.2.4 of Reference 1, Appendix A gives requirements for this subroutine.

#### 2.3.4.1.2 Read Input Data Subroutine

The purpose of this subroutine is to read the data input to the LVDC/LVDA via the 14 data lines from the RCA-110A. Program control will be transferred to the Read Input Data Subroutine with the sync bit off to force the overtime error status code. Control will be transferred to the subroutine with the sync bit on and the mode/data bit indicating mode to force this error message. It will be verified that the data bits are used only during the prepare to load mode. The prepare to load mode will be exercised with the last word bit set in the second word and in the third word. The verify mode will be used in attempt to verify 51 (50 is maximum storage capacity) locations to force an error message. The telemetry from the LVDC will be compared with known input words which were loaded to insure correct formation of the control word by the LVDC. The input mode (verify or prepare to load) will be changed during execution of the subroutine to force an error condition. It will be verified that the input words are received in correct sequence. Requirements for this subroutine are found in paragraph 3.2.1 of Reference 1, Appendix A.

#### 2.3.4.1.3 Output Interrupt Generate Subroutine

The purpose of this subroutine is to generate an RCA-110A interrupt (Discrete Output 2) after certain computer telemetry operations. This subroutine is verified by observing that the interrupt is correctly issued after the specified telemetry operation. Requirements of this subroutine are found in paragraph 3.2.5 of Reference 1, Appendix A.

#### 2.3.4.1.4 Sync Reset Subroutine

The purpose of this subroutine is to turn off the RCA-110A sync signal to the LVDC. The sync reset line is Discrete Output 1 (D01). Demonstrating that the sync is reset verifies this subroutine.

#### 2.3.4.2 PTL Telemetry Cycle

All telemetry from the PTL routine will be printed by the preflight simulator program and checked against expected values. Verification of telemetered data will include that data telemetered every pass through PTL, every other pass through PTL, and the data telemetered after the platform is aligned.

#### 2.3.5 Utility Routines

##### 2.3.5.1 Instruction Rollover Subroutine

The instructions and data used in the Preflight Program are stored in different sectors. To execute program-built and modified instructions, a roll-over routine is used to execute both syllables of a data word containing two instructions. Correct program operation implies the routine is correctly implemented and properly used. Paragraph 3.2.6 of Reference 1, Appendix A gives the requirements of this subroutine.

##### 2.3.5.2 PTL LVDA Initialize Subroutine

The function of this routine is to inhibit all interrupts except GRR and TLC, to set and reset specified ICR and DOR bits, and to dump all ladders to zero. The routine is verified by checking the interrupt inhibit register contents in PTL and by checking and manipulating the contents of the ICR and DOR set and reset constants in core.

PART II

VEHICLE AND MISSION DEPENDENT VERIFICATION  
REQUIREMENTS



PART II  
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SECTION 1  
AS-200 SERIES VEHICLES

1.1 INTRODUCTION

This section contains the verification requirements that are applicable to Saturn IB Launch vehicles. Any changes made to the Prepare to Launch program to satisfy the functional requirements of a specific mission must be verified, and the test required to accomplish this effort are outlined herein. This document was originated for the AS-206 mission, thus, all previous vehicles are not included. Updates for future vehicles will be distributed in a periodic manner for inclusion in the verification plan.

1.2 GENERAL PREFLIGHT

1.2.1 Program Change Requests

All program changes will be verified as received for each subsequent mission. Program Change Requests (PCR) and methods of verification will be described in the Preflight Verification Results document.

1.2.2 Tape Compare Program

A tape compare program will be used to compare all future Preflight Programs to the previous mission program. This comparison will be an added check on changes to the Preflight Program and will also insure that no redundant or unnecessary changes are made.

1.3 AS-206 PREPARE TO LAUNCH VERIFICATION REQUIREMENTS

The primary area of change for the AS-206 mission is in the DCS targeting load capability. This function is required to provide an accurate

targeting for linkup with the previously launched orbiting Workshop based on tracking data. Verification of the implementation of this scheme will be accomplished as outlined in the following paragraphs.

#### 1.3.1 DCS Command Verification

Assurance that the program is capable of accepting the target load data sequence and properly formatting each of the eight parameters required to target the launch vehicle will be obtained through analysis of a test series designed to exercise the following requirements:

- Command and data only accepted during the defined time frames.
- Program manipulation with respect to scaling is correct.
- Data overflow conditions are properly handled.
- Negative data quantities (two's complement) are formatted properly.
- Formatted quantities are stored in the right locations for subsequent program use.

All realistic input error configurations will be simulated to insure that only valid data will be accepted and used by the program.

#### 1.3.2 Azimuth Calculation Verification

A test series designed to demonstrate the PTL program's ability to compute and telemeter the required platform azimuth as a function of the difference (TD) between the predicted time of GRR ( $T_L'$ ) and the nominal time of GRR ( $T_{GRR0}$ ) will be used to verify correct azimuth calculations. Azimuths for values of TD in increments of five seconds will be tested throughout the launch window limits specified for the AS-206 mission.

### 1.3.3 Backup Target Load Verification

The backup method of target data loading (should the DCS fail) will be verified by demonstrating that the LVDC/LVDA/RCA-110A interface is enabled and functional after three DCS load attempts have been made and that the capability is disabled at the correct time during the launch vehicle count-down sequence.



SECTION 2  
AS-500 SERIES VEHICLES

2.1 INTRODUCTION

This section contains the verification requirements that are applicable to Saturn V launch vehicles. Any changes made to the Prepare to Launch program to satisfy the functional requirements of a specific mission must be verified, and the tests required to accomplish this effort are outlined herein. This document was originated for the AS-511 mission, thus, all previous vehicles are not included. Updates for future vehicles will be distributed in a periodic manner for inclusion in the verification plan.

2.2 GENERAL PREFLIGHT

All program changes will be verified as received for each subsequent mission. The Program Change Requests (PCR) and methods of verification will be described in the Preflight Verification Results document.

2.2.1 Program Change Requests

All program changes will be verified as received for each subsequent mission. Program Change Requests (PCR) and methods of verification will be described in the Preflight Verification Results document.

2.2.2 Tape Compare Program

A tape compare program will be used to compare all future Preflight Programs to the previous mission program. This comparison will be an added check on changes to the Preflight Program and will also insure that no redundant or unnecessary changes are made.

## 2.3 AS-511 PREPARE TO LAUNCH VERIFICATION REQUIREMENTS

The primary functional requirements needed in the Prepare to Launch programs for AS-500 series lunar missions is the variable launch azimuth capability. This requirement has been nominally verified in the course of previous flight program verification efforts, i.e., the PTL program has been cycled under nominal conditions to verify the PTL/flight program interface. A thorough verification is required with perturbed inputs to the program to validate error detection implementation. This verification effort will be accomplished as outlined in the following paragraphs.

### 2.3.1 GMT and PLOT Synchronization and Azimuth Management

Verification of proper program usage and testing of these input functions (from RCA-110A) will be obtained through analysis of a series of tests designed to exercise the following checks.

- The requirement to receive GMT and PLOT within 60 seconds of entry into PTL will be violated to check this error path.
- PLOT values outside the launch window opening and close times will be tested to check error detection.
- The RCA-110A interrupt (handled as a discrete input) will be inhibited indicating no platform alignment and GRRA issued to test for program response.
- Perturbed fine and backup roll gimbal angle readings will be used to check the gimbal angle reasonableness test (a function of computed azimuth).

In all error conditions forced, proper D013 setting will be demonstrated.

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## APPENDIX A

### REFERENCES

1. LVDC Preflight Program Descriptions, MSFC No. DRL-008A, IBM No. 67-F11-0011.
2. LVDC Equation Defining Document for the Saturn V Flight Programs Revision I, MSFC III-4-423-15, IBM No. 69-207-0001.
3. Astrionics System Handbook - Saturn Launch Vehicles, MSFC No. IV-4-401-1, IBM No. 68-966-0002.
4. Programmers Operating Manual - Saturn Launch Vehicle Digital Computer, Launch Vehicle Data Adapter and Programmable Test Controller, Contracts NAS8-11561 and NAS8-11562.
5. Program Verification Plan for Saturn Launch Vehicle Prepare to Launch Programs, IBM No. 71W-00143.
6. IBM Memo K96-70-048, Determination of AMP3 Error Equations



APPENDIX B  
VERIFICATION TEST CASE DESCRIPTION

The verification cases which are described in this Appendix constitute the minimum tests to be performed for verification of the Preflight Program.

GENERAL PREFLIGHT NOMINAL CONDITIONS TEST CASES

<u>Case</u>	<u>Description</u>
1.0	<u>Memory Load, Verification, and Initialization Programs</u>
1.1	Command sector dumps from modules 0, 2, 5.
1.2	Command sector sum checks of modules 0, 2, 5.
1.3	Load various core locations, and verify the data loaded through the Verify & Prepare to Load Routine.
2.0	<u>Guidance and Control System Test and Monitor Programs</u>
2.1	Command sector dumps of modules 0, 1, 2, 4 through the Special Loader Routine.
2.2	Load various core locations, and verify the data loaded through the Special Loader Routine.
2.3	Specify various pulse counts and order of axis interrogation to the Accelerometer Pulse Count Routine.
2.4	Input twelve-bit CIU addresses to the CIU Read Routine.
2.5	Command execution of the Command Receiver Linkage Routine.
2.6	Command execution of the Commanded Flight Linkage Routine, and sum check all sectors, when Repeatable Flight Simulation has completed.

<u>Case</u>	<u>Description</u>
2.7	Command execution of the Discrete Input Monitor Routine with various patterns set in the DIN, DIS, and ISR registers.
2.8	Input different pitch, roll, and yaw increments to the Exercise Attitude Command Routine.
2.9	Command execution of the G&C Steering Test Routine.
2.10	Specify different combinations of fine, backup, and coarse resolvers to be monitored, and command execution of the Gimbal Angle Monitor Routine.
2.11	Specify different switch selectors to be driven, and command execution of the Switch Selector Test Routine.
2.12	Specify each rate in both modes of the Telemetry Test Routine.
3.0	<u>LVDC/LVDA Test Programs</u>
3.1	Command execution of the DOM Test Routine, and monitor the resulting DOM telemetry.
3.2	Command execution of the Ladder Error Test Routine.
3.3	Command execution of the Memory Error Test Routine.
3.4	Command execution of the Minor Loop Switch Selector and Real Time Counter Test Routine.

## PREPARE TO LAUNCH TEST CASES

<u>Case</u>	<u>Description</u>
1.0	<u>LVDA Real Time Counter Tests</u>
1.1	Simulate a positive one count clock bias by adding a low order bit to the latest clock reading.
1.2	Simulate a negative one count clock bias as in 1.1 above.
1.3	Simulate clock readings close to the overflow value, and test the following configurations: <ul style="list-style-type: none"><li>• Just prior to counter overflow</li><li>• Just after counter overflow</li></ul>
1.4	Simulate a counter running 1/3 faster than nominal (runaway configuration).
2.0	<u>Timer 1 and Timer 2 Tests</u>
2.1	Modify the constants loaded into each counter to force an interrupt time in error by 3 (equivalent to 1 RTC count) LVDC word times.
2.2	Same as 2.1 with a -3 LVDC word time error.
3.0	<u>Accelerometer Optisyn Delay Line Tests</u>
3.1	One count difference in A and B channel readings; all three axes.
3.2	Two count difference in A and B channel readings; all three axes.
3.3	Three count difference in A and B channel readings; all three axes.

<u>Case</u>	<u>Description</u>
4.0	<u>Crossover Detector Counter Tests</u>
4.1	Positive three count difference between duplex counter readings.
4.2	Positive four count difference between duplex counter readings.
4.3	Negative four count difference between duplex counter readings.
4.4	Negative five count difference between duplex counter readings.
4.5	ICR and disagreement bit combinations to check subtract and limit circuitry and disagreement bit inhibit logic.
5.0	<u>LVDC Instruction Execution Tests</u>
5.1	Execute each conditional transfer by forcing the accumulator to contain the required error condition.
5.2	Execute all arithmetic tests with perturbations to the comparison constants.
5.3	Program listing analysis to verify the memory addressing scheme.
6.0	<u>Error Monitor Register (EMR) Tests</u>
6.1	Real Time telemetry analysis to verify EMR telemetry.
6.2	Set the EAM bit and the EBM bit in the EMR.
6.3	Simulate all possible set/reset combinations of the SCA and SCB bits in the EMR and the DISR.



<u>Case</u>	<u>Description</u>
7.0	<u>Interrupt and Discrete Cases</u>
7.1	Forced interrupt with no bit set in ISR.
7.2	TLC bit set in ISR with all interrupt inhibited.
7.3	Verify ISR ANDing constant.
7.4	Set (one at a time) all external interrupts.
7.5	Verify DIN ANDing and XORing constants.
7.6	Set all discrete inputs.
7.7	Set (one at a time) all discrete inputs.
7.8	Verify DIS ANDing and XORing constants.
7.9	Set all discrete input spares.
7.10	Set (one at a time) all discrete input spares.
7.11	Set bit combinations of discrete inputs (both valid and non-valid bits).
7.12	Set bit combinations of discrete input spares (both valid and non-valid bits).
8.0	<u>Accelerometer and Gimbal Angle Perturbation Cases</u>
8.1	Initial accelerometer misalignment test cases.
8.2	Accelerometer constant bias error test cases.
8.3	Accelerometer scale factor error test cases.
8.4	Initial accelerometer misalignment and constant bias error test cases.
8.5	Initial accelerometer misalignment and scale factor error test cases.
8.6	Accelerometer constant bias and scale factor error test cases.
8.7	Initial accelerometer misalignment, constant bias, and scale factor error test cases.

<u>Case</u>	<u>Description</u>
8.8	Gimbal angle constant drift rate test cases.
8.9	Gimbal angle constant bias test cases.
8.10	Gimbal angle constant drift rate and constant bias test cases.
9.0	<u>Verify and Prepare to Load Test Cases</u>
9.1	Real time telemetry analysis to verify status code issuance.
9.2	Force overtime subroutine status code from read input data.
9.3	Force mode bit set error message.
9.4	Test non-read of data bits in verify mode.
9.5	Check table storage capacity in verify mode.
9.6	Input Prepare to Launch control words with last bit set in second word and in third word.
9.7	Change input mode during execution.
9.8	Input word sequence tests.
9.9	Real time telemetry analysis to check output interrupt generation.
9.10	Real time telemetry analysis to check sync reset.
10.0	<u>PTL LVDA Initialize Test Cases</u>
10.1	Verify contents of Interrupt Inhibit Register.
10.2	Verify ICR and DOR set and reset constants.
10.3	Modify DOR and ICR set and reset constants and execute PTL.

# APPENDIX C

The following table lists the error message telemetry for the preflight routines. For each routine the error name, the error message number in octal, and the sequence that the error occurs within the routine is outlined. The model 44, unlike the LVDC, also possesses a description of each error message number. The decimal number is assigned in the model 44 to each error message description.

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
1. LVDA Timing & Counter	1	DAEM1	111000000	51
		DAEM2	112000000	59
		DAEM4	114000000	70
		DAEM7	117000000	34
		DAEM9	112000000	53
		DAEM12	111500000	56
		DAEM13	111600000	57
		DAEM14	111700000	58
		DAEM15	112100000	60
		DAEM16	112200000	61
		DAEM33	114500000	63
		DAEM18	112400000	64
		DAEM19	112500000	66
		DAEM21	112700000	68
		DAEM22	113100000	69

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
	2	DAEM23	113200000	71
		DAEM5	115000000	72
	3	DAEM10	111300000	54
	4	DAEM3	113000000	67
	5	DAEM8	111100000	52
	6	DAEM6	116000000	73
	7	DAEM11	111400000	55
	8	DAEM20	112600000	65
	9	DAEM17	112300000	62
	10	NONE		
2. Minor Loop, Switch	1	CTEM1	130000000	11
Selector, and Real	2	CTEM2	131000000	12
Time Counter	3	CTEM3	132000000	13
	4	CTEM4	133000000	14
	5	CTEM5	134000000	15
	6	CTEM6	135000000	16
	7	NONE		
3. Mode Sort Routine	1	MSEM0	000000000	21
		MSEM1	001000000	23
		MSEM3	001200000	141
	2	MSEM2	001100000	22
	3	NONE		
4. Telemetry Test	1	TLEM1	327000000	136
	2	NONE		
5. Read Input Data	1	RIEM1	451000000	138
Subroutine	2	NONE		

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
6. CIU Read Routine	1	CIUEM1	141000000	103
	2	CIUEM2	142000000	104
	3	NONE		
7. G&C Steering	1	GCEM1	061000000	25
	2	NONE		
8. DOM Test	1	DIEM1	071000000	26
	2	NONE		
9. Ladder Error Test	1	LEEM1	101000000	27
	2	LEEM2	102000000	35
		LEEM4	104000000	47
		LEEM5	105000000	48
		LEEM7	107000000	50
		LEEM9	101200000	29
		LEEM11	101400000	31
		LEEM23	103100000	44
		LEEM12	101500000	32
		LEEM14	101700000	34
		LEEM16	102200000	37
		LEEM20	102600000	41
	3	LEEM3	103000000	43
		LEEM8	101100000	38
		LEEM10	101300000	30
		LEEM22	103300000	46
		LEEM13	101600000	33
		LEEM15	102100000	36



LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
		LEEM17	102300000	38
		LEEM21	102700000	42
	4	LEEM4	104000000	47
		LEEM6	106000000	49
	5	LEEM18	102400000	39
	6	LEEM19	102500000	40
	7	LEEM11	101400000	31
		LEEM24	103200000	45
	8	NONE		
10. Interrupt	1	INEM1	331000000	1
Processor	2	INEM2	332000000	137
	3	NONE		
11. Verify & Prepare	1	LVEM1	211000000	122
to Load	2	LVEM2	212000000	123
	3	LVEM3	213000000	124
	4	LVEM4	214000000	125
	5	LVEM5	215000000	126
	6	LVEM6	216000000	127
	7	LVEM7	217000000	0
	8	NONE		
12. Exercise Attitude	1	ECEM1	171000000	118
Command	2	ECEM2	172000000	119
	3	ECEM3	173000000	120
	4	ECEM4	174000000	121
	5	NONE		

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
13. Load Routine	1	LDEM1	231000000	128
	2	LDEM2	231200000	129
	3	NONE		
14. Resolver Error	1	REEM1	441000000	2
Subroutine	2	NONE		
15. Switch Selector	1	SSEM1	151000000	105
Test	2	SSEM2	152000000	112
	3	SSEM3	153000000	113
	4	SSEM4	154000000	114
	5	SSEM5	155000000	115
	6	SSEM7	157000000	116
	7	SSEM11	151400000	109
	8	SSEM7	157100000	117
		PASS2		
	9	SSEM11	151410000	110
		PASS2		
	10	SSEM8	151100000	106
	11	SSEM9	151200000	107
	12	SSEM12	151500000	111
	13	SSEM10	151300000	108
	14	NONE		
16. Self Test	1 - 35	STEM1	002000000	24
Subroutine				
17. Memory Error	1	MEM1	220000000	3
Test	2	MEM2	220000010	4
		MEM3	220000020	5

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
		MEM4	220000030	6
		MEM5	220000040	7
		MEM6	220000050	8
		MEM7	220000060	9
		MEM8	220000070	10
		MEM9	220000100	11
		MEM10	220000110	12
		MEM11	220000120	13
		MEM12	220000130	15
		MEM13	220000140	17
		MEM14	220000150	19
	3	NONE		
18. Prepare to	1	PLEM1	121000000	87
Launch		PLEM2	122000000	88
		PLEM3	123000000	92
	2	PLEM52	125200000	93
		PLEM54	125400000	94
	3	PLEM5	125000000	90
		PLEM51	125100000	91
	4	PLEM6	126000000	98
	5	PLEM61	126100000	99
	6	PLEM62	126200000	100
	7	PLEM63	126300000	101
	8	PLEM56	125600000	96
	9	PLEM57	125700000	97
	10	PLEM7	127000000	140

LVDC Preflight Routine	Test Sequence	Preflight Error Name	Octal Error Telemetry	Decimal Assigned Number
	11	PLEM4	124000000	139
	12	PLEM00	120000000	75
		PLEM01	120040000	76
		PLEM02	120100000	77
		PLEM03	120140000	78
		PLEM04	120200000	79
		PLEM05	120240000	80
		PLEM06	120300000	81
		PLEM07	120340000	82
		PLEM08	120400000	83
		PLEM09	120440000	84
		PLEM0A	120500000	85
		PLEM0B	120540000	86

## APPENDIX D

The following table presents a cross reference between Preflight calling routines and called routines. The column on the left of the table lists and numbers all Preflight routines and subroutines. The top row of the table lists the routines and subroutines by the numbers corresponding to the routines listed in the left hand column. The left hand column lists all Preflight routines whether or not they call other routines, but the row at the top of the table lists only those routines which are called automatically, when another Preflight routine is executed. It should be noted that this table depicts a cross reference for Preflight only under nominal conditions. Logic paths for error conditions or interrupt processing are not included.



# PREFLIGHT PROGRAM CALLING ROUTINES VS. CALLED ROUTINES

Calling Routines		Called Routines																				
		1	3	6	10	12	13	15	16	18	21	22	25	26	27	30	31	34	35	41	44	45
1.	Accelerometer Monitor																					
2.	Accelerometer Pulse Count*								X	X					X	X		X	X			
3.	CIU Read*									X					X			X	X			
4.	Command Receiver Linkage*									X												
5.	Commanded Flight Linkage*									X												
6.	Control Word Execute								X													
7.	Discrete Input Monitor*									X					X					X		
8.	Discrete Output Monitor*									X								X				
9.	DOM Test*									X										X		
10.	Error Monitor																					
11.	Exercise Attitude Command*									X								X	X	X		
12.	Forced Begin							X		X			X	X						X		X
13.	Gimbal Angle Monitor*								X	X					X	X		X				
14.	G&C Steering*									X												
15.	HOP 400 Initialize								X													

PREFLIGHT PROGRAM CALLING ROUTINES VS. CALLED ROUTINES (CONTINUED)

Calling Routines	Called Routines																	
	1	3	6	10	12	13	15	16	18	21	22	25	26	27	30	31	34	35
16. Instruction Execute																		
17. Interrupt Processing****																		
18. Issue Status Code														X				
19. Ladder Error Test*									X								X	
20. Load**			X						X									
21. LVDA Timing and Counter Test																		
22. LVDC Self Test																		
23. Memory Error Test*									X									
24. Minor Loop, Switch Selector, & Real Time Counter*									X									
25. Mode Sort		X		X					X	X	X							X
26. Output Interrupt Generate															X			X
27. Output														X				
28. Power Up Initialize					X		X											X
29. Prepare to Launch*	X		X		X			X	X	X	X		X		X	X		X
30. PTL Real Time Update																		X

PREFLIGHT PROGRAM CALLING ROUTINES VS. CALLED ROUTINES (CONTINUED)

Calling Routines	Called Routines																					
	1	3	6	10	12	13	15	16	18	21	22	25	26	27	30	31	34	35	41	44	45	
31. PTL LVDA Initialize																						
32. Program Continue*									X													
33. Program HOP																						
34. Read Input Data									X						X				X	X		
35. Real Time Delta																						
36. Resolver Error																						
37. Sector Dump*									X	X					X				X		X	
38. Sector Sum Check*									X	X					X				X		X	
39. Special Loader***																						
40. Switch Selector Test*				X						X									X			
41. Sync Reset																X						
42. Telemetry Test*									X	X												
43. Verify and Prepare to Load**				X						X					X				X			

PREFLIGHT PROGRAM CALLING ROUTINES VS. CALLED ROUTINES (CONTINUED)

Calling Routines	Called Routines																				
	1	3	6	10	12	13	15	16	18	21	22	25	26	27	30	31	34	35	41	44	45
44. TLC Monitor																					
45. Register Initialize																					

\*Commanded only through Mode Sort.

\*\*Commanded through Mode Sort and/or PTL.

\*\*\*Commanded through Mode Sort and/or Power Up Initialize.

\*\*\*\*Can be entered during any routine or subroutine, when an interrupt allowed by that routine or subroutine is received.