

# IBM

Saturn Instrument Unit

## Saturn Preflight Program Verification Plan

Oxley, B. G.  
K99/5-1

1 May 1971

MSFC-DRL-008A

Line Item 92

IBM No. 71W-00141



Contract No. NAS 8-14000

MSFC-DRL-008A

Line Item 282

IBM No. 71W-00141

Prepared for the  
GEORGE C. MARSHALL  
SPACE FLIGHT CENTER  
Huntsville, Alabama

## Saturn Preflight Program Verification Plan

1 May 1971

Classification and Content Approval

*G. V. Doolittle*

Data Manager Approval

*DM Cooklin*

Program Office Approval

*RT Smith*

**IBM**

Space Systems Center/Huntsville/Alabama

## PREFACE

The Saturn Preflight Program Verification Plan for the Saturn Launch Vehicle Preflight Program describes the methods which will be used to insure that the Preflight program meets all functional requirements and is operational for use in Saturn mission countdowns and preflight testing.

The Saturn Preflight Program Verification Plan combines the objectives formerly covered by the Program Verification Plan for Saturn Launch Vehicle Prepare to Launch Programs, MSFC-DRL-008A, Line Item 293, IBM No. 71W-00143 and the Saturn Preflight Program Verification Plan, MSFC-DRL-008A, Line Item 292, IBM No. 71W-00141. This document supersedes the two documents formerly directed towards Preflight verification and should, therefore, be the only reference for Preflight verification.

The objective of this plan is to specify the verification requirements for the baseline Preflight Program and the verification requirements for the changes implemented as a function of specific mission and/or vehicle operational requirements. Since the Preflight Program as defined applies to all mission configurations, any corrections to deviations or changes implemented to satisfy specific mission requirements will be reflected in periodic updates to this document. Program configuration control is maintained through use of a digital symbolic program comparison routine executed for each program revision to identify all the differences in the new configuration. This method insures that only those areas specified to change are different.

Part I contains the requirements for verifying the baseline Preflight program common to all Saturn launch vehicles. Part II defines the verification

required to validate specific mission and vehicle dependent Preflight program changes to the baseline. Part II will be updated for each vehicle and will contain the methods to be used to verify changed areas of the Preflight program.

The 360/44 simulator will be used as the major tool for the PTL verification effort. This simulation contains a mathematically modeled platform, flight type LVDC/LVDA hardware and simulated LVDA interfacing equipment (DCS, switch selector, CIU, etc.).

# TABLE OF CONTENTS

Paragraph	Title	Page
Section 1:	GENERAL PREFLIGHT PROGRAM VERIFICATION	--
1.1	Introduction	1-1
1.2	General Preflight Program Requirements	1-2
1.2.1	Program Functional Requirements	1-2
1.2.2	Applicable Document List	1-3
1.3	Ground Rules for Preflight Programming	1-3
1.3.1	RCA-110A Communication Link	1-3
1.3.2	Prelaunch Checkout Philosophy	1-4
Section 2:	LVDC NOMINAL CONDITIONS VERIFICATION	--
2.1	Introduction	2-1
2.2	Accelerometer Pulse Count	2-2
2.3	CIU Read	2-4
2.4	Command Receiver Linkage	2-4
2.5	Commanded Flight Linkage	2-5
2.6	Discrete Input Monitor	2-6
2.7	Discrete Output Monitor	2-7
2.8	Data Output Multiplexer Test	2-10
2.9	Exercise Attitude Command Test	2-12
2.10	Gimbal Angle Monitor	2-19
2.11	G&C Steering Test	2-22
2.12	Ladder Error Test	2-22
2.13	Load Routine	2-24
2.14	Memory Error Test	2-24
2.15	Minor Loop, Switch Selector, and Real Time Counter Test	2-25
2.16	Sector Dump	2-26

## SECTION 1

### GENERAL PREFLIGHT PROGRAM VERIFICATION

#### 1.1 Introduction

The LVDC Preflight Verification Plan provides a procedure which requires the LVDC Preflight Program to use all of its program logic. An LVDC preflight routine performs its function by executing a set of program logic. The only variations from a fixed logic path are determined by:

- RCA-110A input word options
- Error conditions

The LVDC Preflight Verification Plan contains three verification sections:

- LVDC Preflight Nominal Conditions Verification
- LVDC Preflight Error Conditions Verification
- LVDC Preflight Prepare to Launch Verification

In the Nominal Conditions Verification, variations introduced by RCA-110A input word options are exercised. The combination of options selected for input to the preflight routine requires the routine to perform all of its functions.

In the Error Conditions Verification, variations introduced by anomalies are exercised. The LVDC preflight routines which respond to error conditions are exercised. Each RCA-110A input word error or each hardware performance error tested by the routine is generated by the control programs.

For both Nominal and Error Conditions Verification, the plan provides the results expected when the preflight routine is executed with the specified input.

In the LVDC Preflight Prepare to Launch Verification, the same requirements apply to the input as in the Nominal and Error Conditions Verification. That is, the input exercises the functions of the routine for both nominal and error conditions. However, the launch criticality of the monitor functions of the Prepare to Launch routine necessitates an emphasis on the test status of external inputs to the routine. Thus, the plan details the contents of external inputs such as discrete inputs, discrete input spares, staging interrupts, accelerometers, gimbals, and variable azimuth quantities. These external inputs are neither RCA-110A input word options nor necessarily error conditions, yet they can significantly affect program logic path.

## 1.2 General Preflight Program Requirements

### 1.2.1 Program Functional Requirements

The LVDC Preflight Program performs the following functions under control of the SLCC:

- Load and/or verify the LVDC memory.
- Exercise, monitor, and verify internal functions of the LVDC and LVDA.
- Exercise and/or monitor selected Instrument Unit subsystems.
- Participate in overall guidance and control system tests.
- Perform limited data processing for the Launch Computer Complex.

These preflight routines are versatile and flexible in that they are adaptable to prelaunch conditions for the entire Saturn series of missions as presently conceived.

In conjunction with the launch computer, these routines provide the following subsystem checkout capabilities:

- Operational checkout of the LVDC.
- Operational checkout of the LVDA.
- Operational checkout of the Switch Selector - LVDA interface.
- Operational checkout of the accelerometer and gimbal angle processing features.
- Operational checkout of the vehicle discretes.
- Operational checkout of the LVDA-PCM interface.

#### 1.2.2 Applicable Document List

All documents used in verification of the preflight program are listed in Appendix A. All preflight routines, tested in verification described herein, are described in detail in the "LVDC Preflight Description" document (Reference 1).

#### 1.3 Ground Rules for Preflight Programming

In defining the preflight routines, certain assumptions were made and ground rules were followed concerning the RCA-110A communication link and the prelaunch checkout philosophy.

##### 1.3.1 RCA-110A Communication Link

Those aspects of the interface between the Launch Vehicle Data Adapter and the RCA-110A, which are extensively utilized by the preflight routines, are described in this section.

One aspect of the interface between the RCA-110A and the LVDA/LVDC is the interrupts between them. In preflight, an interrupt to the LVDA/LVDC from the

RCA-110A will force a program recycle in the LVDC. Whereas, an interrupt from the LVDC to the RCA-110A electrical support equipment (ESE) forces the RCA-110A to read the telemetry buffer register.

Another aspect of the interface is the synchronization signals. The SYNC discrete to the LVDC serves two purposes:

- It notifies the LVDC that the launch computer is about to send information to the LVDC.
- It serves as a "data received" indication from the launch computer after the LVDC has sent out data, accompanied by an interrupt, to the launch computer and must be acknowledged before the LVDC continues on to the next program function.

The SYNC RESET signal indicates to the RCA-110A launch computer that the LVDC has recognized the SYNC signal and is proceeding to honor it.

Other preflight communication bridges between the RCA-110A and the LVDA/LVDC are 14 mode/data lines, six mode register lines, and 35 hardwire lines. The mode/data lines provide a means for the RCA-110A launch computer to relay mode commands or data to the LVDC. The mode register lines indicate to the launch computer the preflight routine currently being executed in the LVDC, and the hardwire lines are the means by which the LVDC/LVDA transmits data to the launch computer without requiring the processing of PCM/DDAS data.

### 1.3.2 Pre-Launch Checkout Philosophy

During preflight checkout, the launch computer sequentially commands the LVDC into various routines. Only one routine can be commanded at a time. When the

LVDC is not executing a commanded routine, it is "idling" in a self-check loop in the Mode Sort Routine, periodically searching for the SYNC signal.

Upon receipt of the SYNC signal, the LVDC reads the 14 mode/data lines and proceeds to execute the commanded routine. Upon entering the commanded routine, the appropriate mode indication is loaded into the mode register, sent to the PCM/DDAS assembly, and sent to the launch computer via the hardwires. Pertinent data, if any, from the commanded routine is telemetered during execution of the routine, and the LVDC returns to its "idling" conditions when execution is completed.

Should the LVDC recognize an error condition, it will issue a special error status code to the launch computer, telemeter any error messages associated with the error condition, and wait for the SYNC signal before continuing. After processing the error, the LVDC will continue with the routine it was executing before the error condition arose or return to the Mode Sort Routine.

In the event that the launch computer desires to terminate an LVDC routine prematurely, it can do so with an RCA-110A interrupt signal which forces a program recycle.

## SECTION 2

### LVDC NOMINAL CONDITIONS VERIFICATION

#### 2.1 Introduction

The LVDC Preflight Nominal Conditions Verification requires the preflight routines to exercise logic variations determined by the RCA-110A input word options. The procedure for each preflight routine is defined in five sections:

- Function
- Options
- Input
- Comments
- Expected Output

The Function section provides a description of the purpose of the preflight routine.

The Options section details the items which are specified by the RCA-110A input word(s).

The Input section prescribes the combination(s) of input word options to select in exercising the preflight routine.

The Comments section contains any explanations which relate to selection of input and/or operation of the control program.

The Expected Output reports the results which must be obtained from the routine to indicate successful execution of the preflight routine.

The LVDC Preflight Nominal Conditions Verification plan does not select all possible combinations of input word options in exercising the preflight routines. However, the combination of options selected for input do verify that the preflight routine can respond to all combinations by selecting combinations which force the preflight routine to process each bit of the input word options in both an ON and an OFF state.

## 2.2 Accelerometer Pulse Count

### 2.2.1 Function

The Accelerometer Pulse Count Routine accumulates delta pulse counts and the associated time intervals for the accelerometers.

### 2.2.2 Options

Specify the first, second, and third accelerometer to be interrogated.

Specify syllable selection for pulse count accumulations.

Specify number of pulses to accumulate.

Specify mode 1, 2, or 3. (The mode determines the axis for the specified count and the time interval accuracy.)

### 2.2.3 Input

Input	Mode	Axis 1st	Axis 2nd	Axis 3rd	Syl	Count
1	1	X	Y	Z	0	1958
2	2	Z	Y	X	1	0002
3	3	Y	X	Z	0	0001
4	3	X	Z	Y	1	0001

#### 2.2.4 Comments

Each mode is selected.

Each axis is selected for interrogation first, second, and third.

Syllable 0 and 1 are each selected.

Counts specified are multiples of the output rates for the axis to which they correspond.

Platform Simulation Rates:

<u>Axis</u>	<u>Rate</u>
X	195.8125 pulses every second
Y	1 pulse every 16 seconds
Z	1 pulse every 32 seconds

#### 2.2.5 Expected Output

<u>Input</u>	<u>Axis</u>	<u>Count</u>	<u>Max Deviation</u>	<u>Time Delta Seconds</u>
1	X	1958	+3	10.0
	Y	0	+1	9.0
	Z	0	+1	9.0

For combinations 2, 3, and 4, the counts for the X, Y, and Z axes should be equal to the product of the platform simulated output rate specified in section 2.2.4, and the respective associated time interval. The X axis count should be within a +5 counts tolerance. The Y and Z axes counts should be within a zero (0) count tolerance.

In all cases, the B Channel count should be within +1 count of the A Channel count.

### 2.3 CIU Read

#### 2.3.1 Function

The CIU Read Routine telemeters the data received for the CIU address requested.

#### 2.3.2 Options

Specify 12 CIU data address bits.

#### 2.3.3 Input

<u>12 bit CIU address</u>	<u>10 bit CIU data</u>
5252 <sub>8</sub>	1252 <sub>8</sub>
2525	0525

#### 2.3.4 Comments

Each CIU address bit is requested in both states. The data bits specified are supplied to the LVDC by the model 44 preflight simulator control program and are requested in both states.

#### 2.3.5 Expected Output

<u>Addr</u>	<u>PIO Tag</u>	<u>Data</u>
5252 <sub>8</sub>	400 <sub>8</sub>	525377776 <sub>8</sub>
2525	400	252777776

### 2.4 Command Receiver Linkage

#### 2.4.1 Function

The Command Receiver Linkage Routine provides direct access to the DCS Processor of the LVDC Flight Program for preflight.

#### 2.4.2 Options

None.

#### 2.4.3 Input

Verify Linkages - Entry to LVDC flight at location 4,17,0,274,4,17.

Verify Interrupt Processor interfaces by requesting telemeter single memory location and sector dump.

#### 2.4.4 Comments

The preflight simulator control program requires that T-SYNC be allowed and that the command receiver interrupt be limited before entry to flight from preflight. The DCS commands executed exercise all preflight-flight interfaces.

#### 2.4.5 Expected Output

Flight DCS Processor output data. The control program verifies this data and indicates status completion.

### 2.5 Commanded Flight Linkage

#### 2.5.1 Function

Commanded Flight Linkage enters the flight program to run repeatable flight simulation.

#### 2.5.2 Options

None.

### 2.5.3 Input

Command Repeatable Flight Simulation. Upon completion, sum checks are taken. These sum checks must correspond to those received in flight program verification.

### 2.5.4 Comments

The sum checks assure that LVDC preflight does not interfere with the execution of repeatable flight simulation.

### 2.5.5 Expected Output

None.

## 2.6 Discrete Input Monitor

### 2.6.1 Functions

The Preflight Discrete Input Monitor routine performs these functions sequentially:

- Inhibit all interrupts except TLC.
- Read Discrete Input, Discrete Input Spares, and Interrupt Storage Registers.
- Limit all interrupts except TLC.
- Telemeter register readings.
- Recycle upon receipt of SYNC.

### 2.6.2 Options

None.

### 2.6.3 Input

#### Set Pattern for Registers

<u>Pattern</u>	<u>DIN</u>	<u>DIS</u>	<u>INT</u>
1	3,5,7,9,11,...,23	1,3,5,7	1,5,7
2	4,6,8,10,...,24	2,4,6,8	2,3,4,6,8,10

Command routine with first pattern set. Reset first pattern, set second pattern, and recycle routine.

### 2.6.4 Comments

All functions are verified. The status of interrupt storage bits 12 and 11 are undeterminable. These bits are indicated off in expected output.

Information which is not telemetered is available to the control program through the FCDD registers. This information can then be presented to the user.

### 2.6.5 Expected Output

Register bits must be set as in the input pattern. The inhibit register must indicate all interrupts are inhibited. The limiting register must indicate limiting bits for each interrupt set. See Table 2.6.

## 2.7 Discrete Output Monitor

### 2.7.1 Functions

The Discrete Output Monitor Routine allows for the set or reset of all discrete output register bits (except D.O.2) and the execution of a switch selector command.

# PATTERN 1

## DIN REGISTER

1 = SET

2 2 2 2 2 1 1 1 1 1 1 1 1 1 1  
4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1 1 1 1 1 1 1 1

## DIS REGISTER

8 7 6 5 4 3 2 1  
1 1 1

## INT REGISTER

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1

## INHIBIT REGISTER (Not Telemetered)

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1 1 1 1 1 1 1 1

## LIMIT REGISTER (Not Telemetered)

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1

# PATTERN 2

## DIN REGISTER

2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1  
4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1 1 1 1 1 1 1 1 1 1

## DIS REGISTER

8 7 6 5 4 3 2 1  
1 1 1 1

## INT REGISTER

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1 1 1

## INHIBIT REGISTER (Not Telemetered)

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1 1 1 1 1 1 1 1

## LIMIT REGISTER (Not Telemetered)

1 1 1  
2 1 0 9 8 7 6 5 4 3 2 1  
1 1 1 1

Table 2.6

### 2.7.2 Options

Set or reset of discrete output register.

D.O. register bits.

Switch Selector Load.

- Read bit.
- Reset bit.
- Stage bits (5).

### 2.7.3 Input

	<u>Set/Reset</u>	<u>D.O.</u>	<u>SW-SEL.</u>	<u>READ</u>	<u>RESET</u>	<u>STAGES</u>
1)	Set	3-13	No	0	0	None
2)	Reset	1	Yes	0	0	IU,S1
3)	Reset	3-13	No	1	1	All
4)	Set	0	Yes	1	0	IU,S1
5)	Reset	1	Yes	0	1	None
6)	Set	1	Yes	N	N	None

### 2.7.4 Comments

The setting of D.O.1 in the last verification combination prohibits any further commands to preflight. Halt must be applied and power-up performed to clear the D.O.1 bit, since D.O.1 resets SYNC.

Information not telemetered is available to the control program through the FCDD registers.

## 2.7.5 Expected Output (none telemetered)

1 = SET

	<u>Discrete Output Register</u>	<u>Switch Selector Feedbacks</u>	<u>Switch Selector Register</u>
	1 1 1 1 3 2 1 0 9 8 7 6 5 4 3 2 1		
1)	1 1 1 1 1 1 1 1 1 1 1 1	000 <sub>8</sub>	00000 <sub>8</sub>
2)	1 1 1 1 1 1 1 1 1 1 1 1	377	10400
3)		377	10400
4)		377	50400
5)		000	20000
6)		1      000	00000

## 2.8 Data Output Multiplexer Test Routine

### 2.18.1 Function

The Preflight DOM Test Routine exercises features of the DOM by issuing telemetry in a specified sequence.

### 2.8.2 Options

None.

### 2.8.3 Input

Command execution of DOM Test Routine and monitor DOM telemetry.

### 2.8.4 Comments

The telemetry contents correspond to those for conditions using the control program.

## 2.8.5 Expected Output

### DOM TEST

Expected output is based on known inputs to the preflight simulator control program.

<u>TAG</u>	<u>DATA</u>	<u>ITEM DESCRIPTION</u>
022 <sub>8</sub>	020040002 <sub>8</sub>	ICR SET
057	000000006	DIN READ
053	001777576	DIS READ
077	774007776	SSFB READ
022	020040002	ICR SET
023	000000000	EMR READ
067	000377776	CIU READ
043	000017776	RCA INPUT REG. READ
022	020040002	ICR SET
107	XXXXXXXXXX	X ACCELEROMETER READ
127	XXXXXXXXXX	Y ACCELEROMETER READ
117	XXXXXXXXXX	Z ACCELEROMETER READ
022	020040002	ICR SET
236	000000000	S.S. REG. LOAD
012	000000000	D.O. REG. LOAD
052	000000000	S.S./D.O.
000	070707070	TELEMETRY OUTPUT
022	020040002	ICR SET
103	7777XXXXX	REAL TIME CLOCK READ
057	000000006	DIN READ
022	020040002	ICR SET
023	000002000	FG1 AND LAD 1
163	000004000	FG2 AND LAD 2
153	000014000	FG3 AND LAD 3

## 2.9 Exercise Attitude Command Test Routine

### 2.9.1 Function

This routine has two modes of operation. Mode 1 provides for automatic sequential driving of the pitch, roll, and yaw ladders. Mode 2 allows individual or simultaneous driving of the three ladders through predetermined increments at a rate determined by the frequency of SYNC discretes, issued by the launch computer.

### 2.9.2 Options

Mode 1 (automatic):

- None.

Mode 2:

- Ladder converter to select.
- Roll increment.
- Yaw increment.
- Pitch increment.
- Sign of increments.

### 2.9.3 Input

<u>Converter</u>	<u>Pitch Increment</u>	<u>Roll Increment</u>	<u>Yaw Increment</u>	<u>Number of Increments</u>
B	+ .12°	+ .06°	+ .24°	64
B	- .24°	+ .12°	+ .12°	64
A	+ .06°	- .24°	- .18°	64
A	0	0	0	4
A	+ .42°	+ .42°	- .42°	35

#### 2.9.4 Comments

Each option is requested in both states. SYNC will be issued by the control program at the fastest allowed rate and will be issued in such a manner as to drive each axis past maximum ladder output. This will test the issuance of special status codes.

#### 2.9.5 Expected Output

None telemetered.

Ladder strip charts.

Status code history.

##### 2.9.5.1 Status Code History

<u>MODE 1</u>	<u>STATUS CODE HISTORY</u>
---------------	----------------------------

00 <sub>8</sub>	Mode Sort
13	Exer. Att. Com. Test
00	Mode Sort

<u>MODE 2</u>	<u>STATUS CODE HISTORY INPUTS 1, 2, and 3</u>
---------------	---

00 <sub>8</sub>	Mode Sort
17	Exer. Att. Com. Test
43	Exer. Att. Com. Error (Driving past max)
46	Exer. Att. Com. Test (Returning to null)
00	Mode Sort

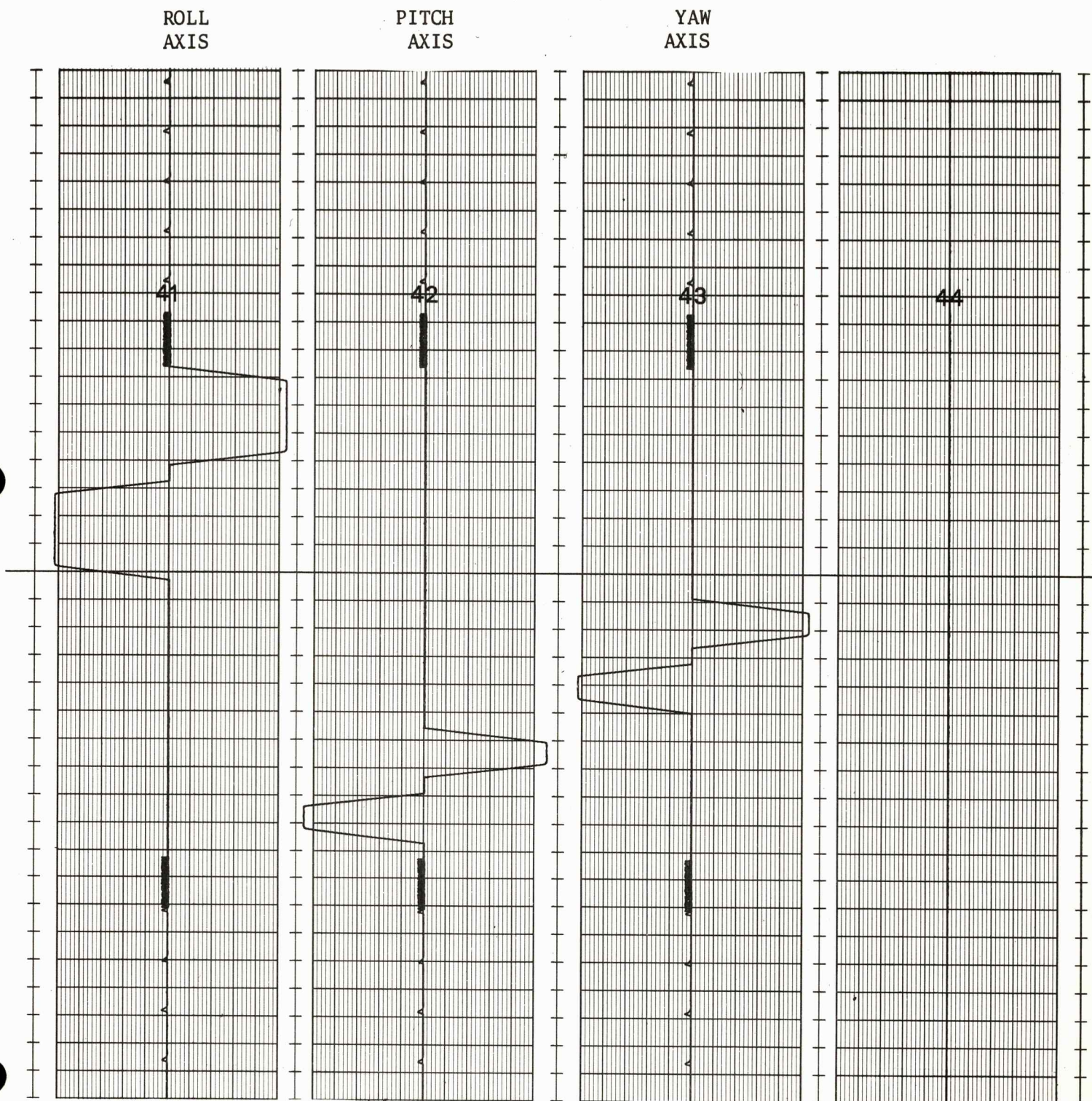
<u>MODE 2</u>	<u>STATUS CODE HISTORY INPUTS 4 and 5</u>
---------------	---

00 <sub>8</sub>	Mode Sort
17	Exer. Att. Com. Test
46	Exer. Att. Com. (Returning to null)
00	Mode Sort

## 2.9.5.2 Ladder Strip Charts

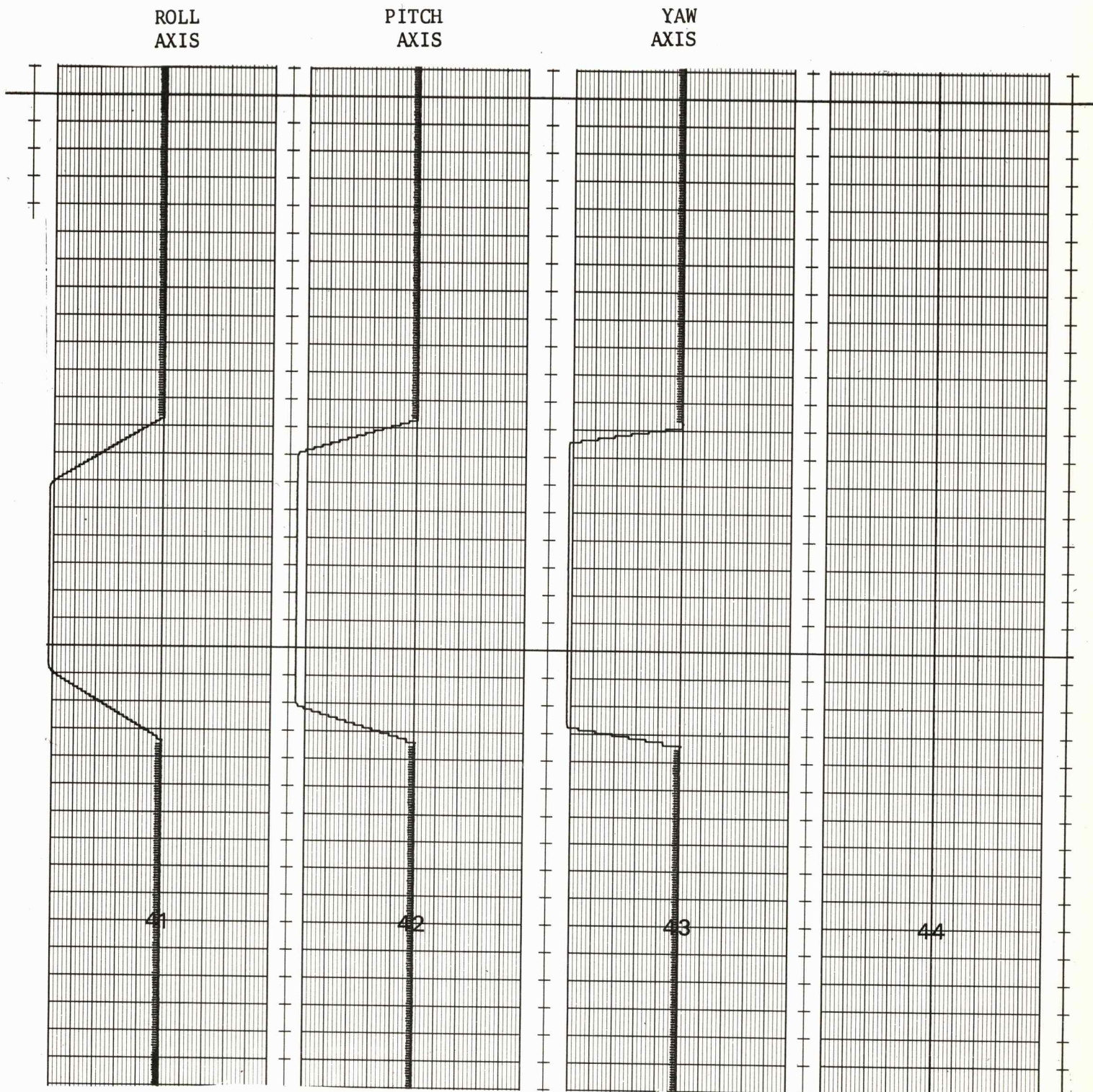
EXERCISE ATTITUDE  
COMMAND TEST  
MODE 1

ladder sensitivity = 50  
rate = 100, power 100



EXERCISE ATTITUDE  
COMMAND TEST  
MODE 2  
(INPUT 1)

ladder sensitivity = 50  
rate = 5



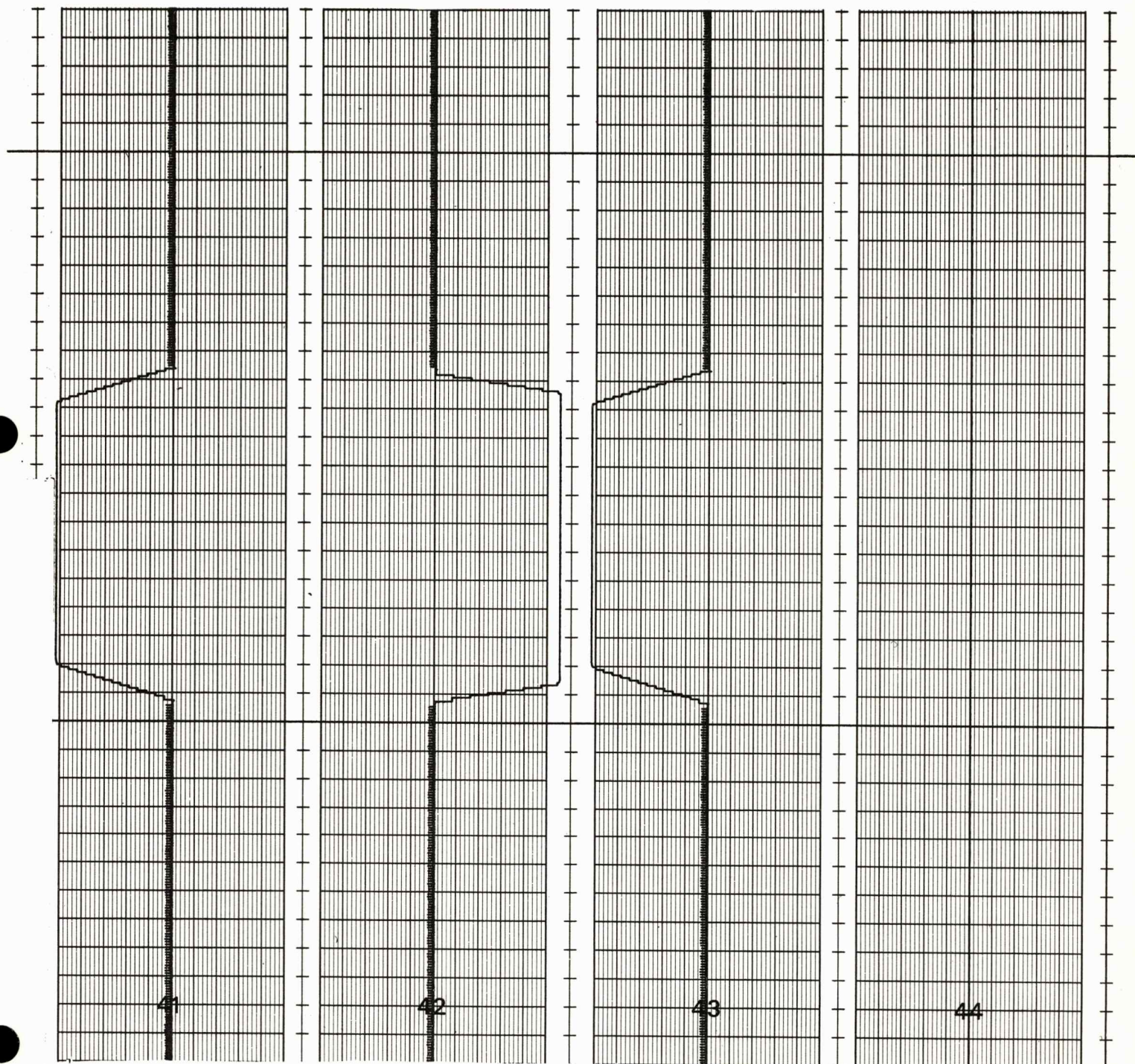
EXERCISE ATTITUDE  
COMMAND TEST  
MODE 2  
(INPUT 2)

ladder sensitivity = 50  
rate = 5

ROLL  
AXIS

PITCH  
AXIS

YAW  
AXIS



EXERCISE ATTITUDE  
COMMAND TEST  
MODE 2  
(INPUT 3)

ladder sensitivity = 50  
rate = 5

ROLL  
AXIS

PITCH  
AXIS

YAW  
AXIS

44

43

42

41

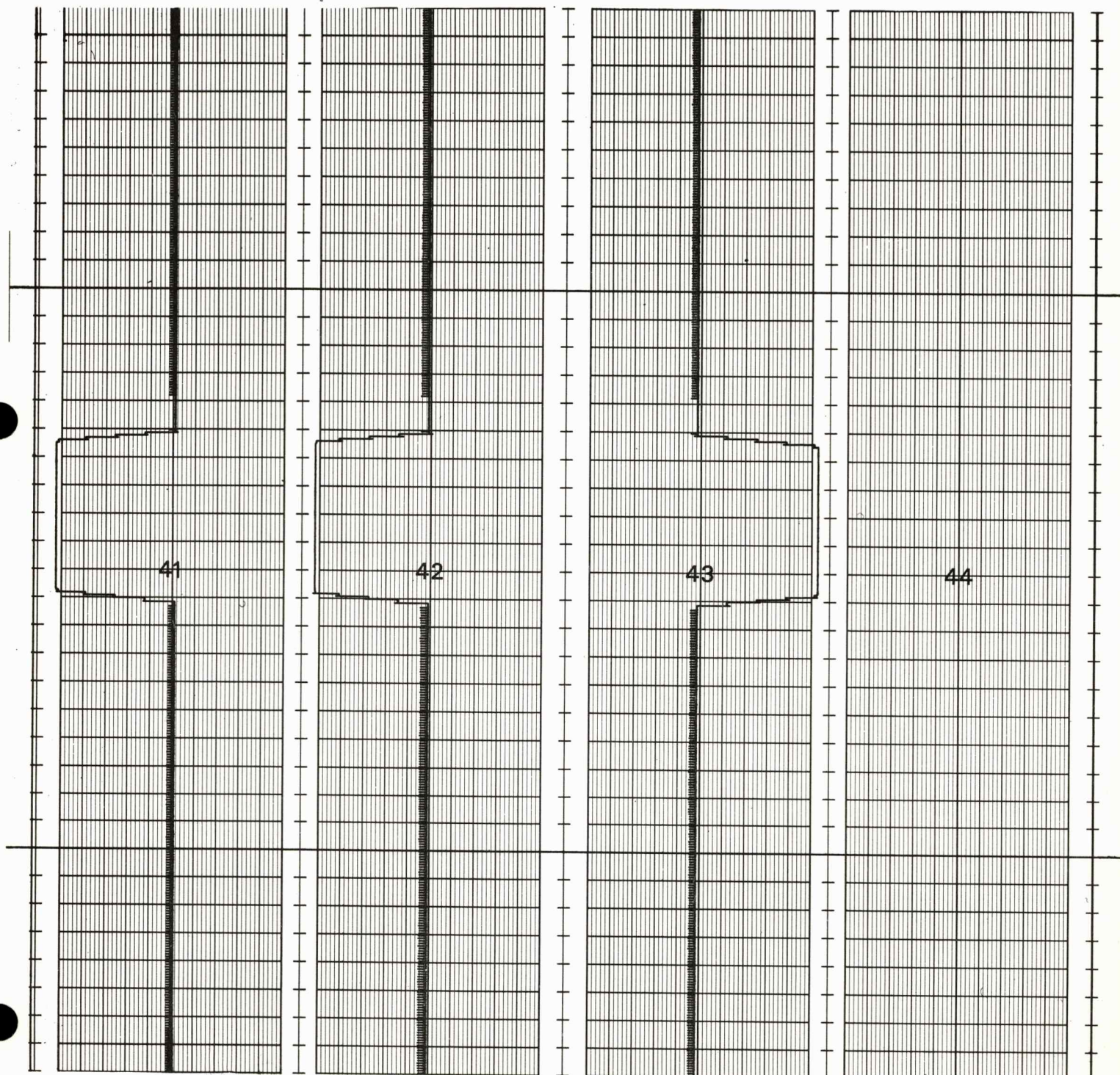
EXERCISE ATTITUDE  
COMMAND TEST  
MODE 2  
(INPUT 5)

ladder sensitivity = 50  
rate = 5

ROLL  
AXIS

PITCH  
AXIS

YAW  
AXIS



## 2.10 Gimbal Angle Monitor Routine

### 2.10.1 Function

The Gimbal Angle Monitor routine determines platform attitude utilizing the gimbals. Sequentially, the routine will:

- Read the gimbals.
- Monitor disagreement bit.
- Compute corrected readings.
- Telemetry results.

### 2.10.2 Options

Specify resolvers to monitor.

Select computation of corrected readings.

### 2.10.3 Input

	Resolvers									Corrected Readings
	C1	C2	C3	F1	F2	F3	B1	B2	B3	
1)	Y	N	Y	N	Y	N	Y	N	Y	N
2)	N	Y	N	Y	N	Y	N	Y	N	Y
3)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

### 2.10.4 Comments

Each resolver is requested in both states. Corrected readings are computed for all gimbals. The disagreement bit is monitored in a non-failure condition.

## 2.10.5 Expected Output

### GIMBAL ANGLE MONITOR

(INPUT 1)

<u>TAG</u>	<u>DATA</u>	<u>TYPE</u>
020 <sub>8</sub>	000100002 <sub>8</sub>	COARSE G.A. 1
014	000000000	COARSE G.A. 3
010	311506232	FINE G.A. 2
004	000000000	BACKUP G.A. 1
400	000000000	BACKUP G.A. 3

(INPUT 2)

<u>TAG</u>	<u>DATA</u>	<u>TYPE</u>
054 <sub>8</sub>	000000000 <sub>8</sub>	COARSE G.A. 2
050	000003642	COUNTER B CORRECTION
044	000003642	COUNTER A CORRECTION
040	000000000	FINE G.A. 1
034	000000000	COUNTER B CORRECTION
030	000000000	COUNTER A CORRECTION
024	000000000	FINE G.A. 3
020	000000000	COUNTER B CORRECTION
014	000000000	COUNTER A CORRECTION
010	342607054	BACKUP G.A. 2
004	000007054	COUNTER B CORRECTION
400	000007054	COUNTER A CORRECTION

## GIMBAL ANGLE MONITOR

(INPUT 3)

<u>TAG</u>	<u>DATA</u>	<u>TYPE</u>
150 <sub>8</sub>	000100002 <sub>8</sub>	COARSE G.A. 1
144	000003644	COUNTER B CORRECTION
140	000003644	COUNTER A CORRECTION
134	000000000	COARSE G.A. 2
130	000003642	COUNTER B CORRECTION
124	000003642	COUNTER A CORRECTION
120	000000000	COARSE G.A. 3
114	000003642	COUNTER B CORRECTION
110	000003642	COUNTER A CORRECTION
104	000000000	FINE G.A. 1
100	000000000	COUNTER B CORRECTION
074	000000000	COUNTER A CORRECTION
070	311506232	FINE G.A. 2
064	000006232	COUNTER B CORRECTION
060	000006232	COUNTER A CORRECTION
054	000000000	FINE G.A. 3
050	000000000	COUNTER B CORRECTION
044	000000000	COUNTER A CORRECTION
040	000000000	BACKUP G.A. 1
034	000000000	COUNTER B CORRECTION
030	000000000	COUNTER A CORRECTION
024	342607054	BACKUP G.A. 2
020	000007054	COUNTER B CORRECTION
014	000007054	COUNTER A CORRECTION
010	000000000	BACKUP G.A. 3
004	000000000	COUNTER B CORRECTION
400	000000000	COUNTER A CORRECTION

## 2.11 G&C Steering Test Routine

### 2.11.1 Function

The G&C Steering Routine provides linkage to the Flight Initialize routine and to the Minor Loop of the flight routine.

### 2.11.2 Options

None.

### 2.11.3 Input

Command execution of the routine.

### 2.11.4 Comments

Output is handled by the Minor Loop. The only exit from this routine is by an executed halt.

### 2.11.5 Expected Output (none telemetered)

See Figure 2.11.

## 2.12 Ladder Error Test

### 2.12.1 Function

The purpose of this routine is to exercise the ladder error detection circuitry.

### 2.12.2 Options

None.

### 2.12.3 Input

Command execution of Ladder Error Test routine.

# G&C STEERING LADDER STRIP CHART

PLATFORM INITIALLY LEVEL, DEVIATE 5 degrees

ladder sensitivity = 50

rate = 5

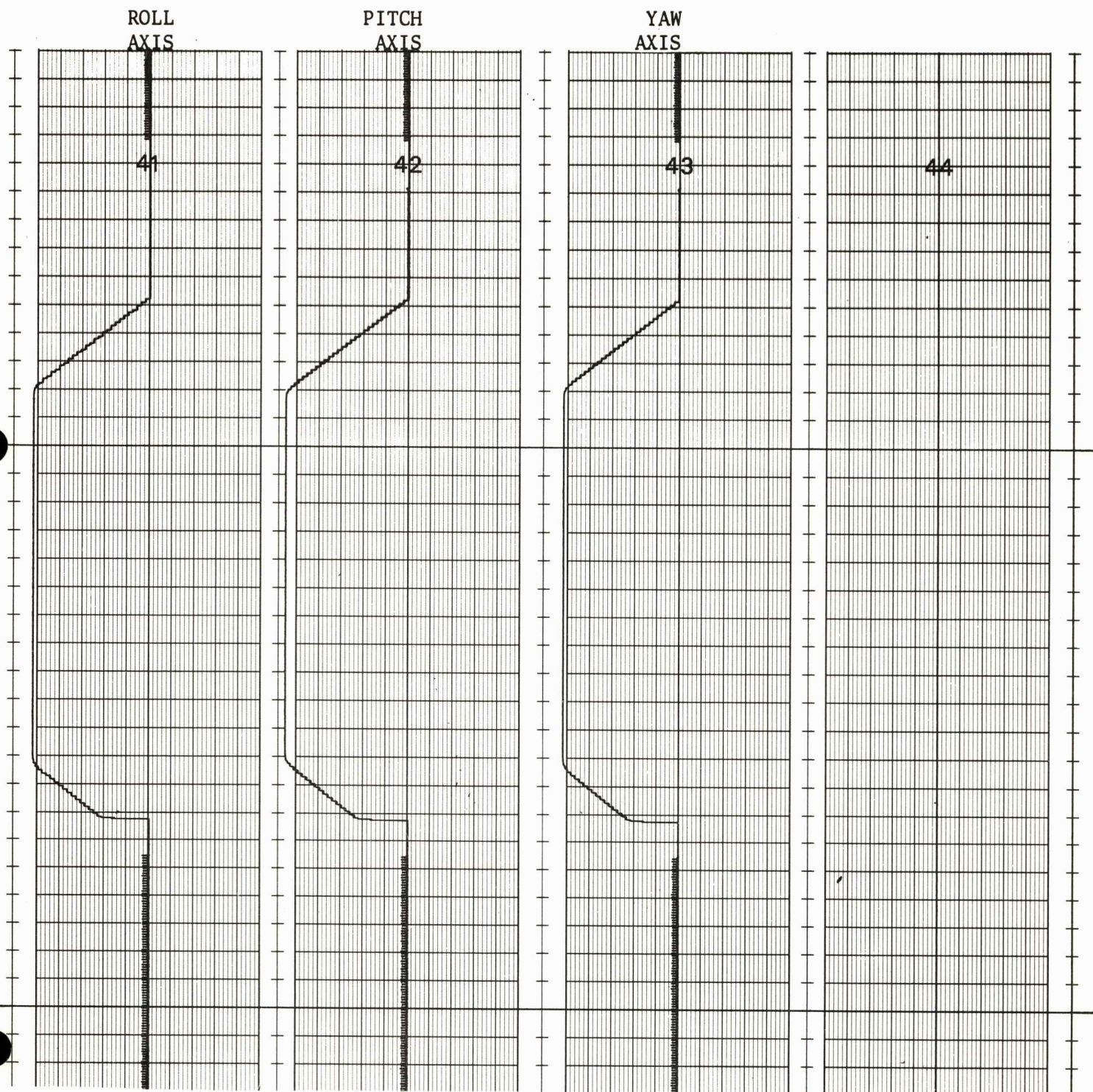


Figure 2.11

#### 2.12.4 Expected Output

None.

#### 2.12.5 Comments

Output received only on error

### 2.13 Load Routine

#### 2.13.1 Function

This routine allows the information previously placed in temporary storage by the Verify and Prepare to Load Routine to be transferred to the permanent memory locations specified.

#### 2.13.2 Options

None.

#### 2.13.3 Input

The Load Routine verification is executed in the verification of Verify and Prepare to Load.

#### 2.13.4 Expected Output

None telemetered.

#### 2.13.5 Comments

Proper verification is obtained in the Verify and Prepare to Load Routine procedure.

## 2.14 Memory Error Test

### 2.14.1 Function

This routine performs the testing of the memory error detection circuitry and logic. This check is divided into the following two categories:

- Tests initiated with the shift instruction. The shift instruction generates a memory SYNC pulse when the error detect logic is testing for no memory current.
- Tests initiated with the PIO instruction. The PIO instruction followed by a CLA, XOR, SUB, or MPH will select multiple address memory lines.

The above tests are repeated for all available modules.

### 2.14.2 Options

None.

### 2.14.3 Input

Request execution of memory error test routine.

### 2.14.4 Expected Output

None.

## 2.15 Minor Loop, Switch Selector, and Real Time Counter Test Routine

### 2.15.1 Function

This routine tests the Real Time Counter (it must increment by 1 every 3 instructions), the Minor Loop Counter (must generate an interrupt 1.28 seconds after the minor loop counter is loaded), and the Switch Selector Counter (bit 1 in the Interrupt Storage Register must be set 1.28 seconds after the Switch Selector Counter is loaded).

#### 2.15.2 Options

None.

#### 2.15.3 Input

Command execution of the program.

#### 2.15.4 Expected Output

None.

#### 2.15.5 Comments

The LVDC Error Detection Program has the capability of simulating an error condition in the Minor Loop, Switch Selector & Real Time Counter routine. If the routine functions properly without an error, it will return to Mode Sort upon completion.

### 2.16 Sector Dump Routine

#### 2.16.1 Function

The purpose of this routine is to allow the RCA-110A launch computer to verify that all 256 locations within a given sector contain the correct instructions and/or data. The RCA-110A specifies the module and the sector(s) within that module which are to be dumped.

#### 2.16.2 Options

Module.

Starting Sector.

Ending Sector.

### 2.16.3 Input

<u>Module</u>	<u>Starting Sector</u>	<u>Ending Sector</u>
2	00 <sub>8</sub>	17 <sub>8</sub>
5	12	05
0	00	00

### 2.16.4 Expected Output

A sequential dump of sectors 0-17 of module 2.

A sequential dump of sectors 12-17 and 0-5 of module 5.

A dump of sector 0 of module 0.

NOTE: Sector locations are telemetered in groups of 32 words, 8 groups per sector.

### 2.16.5 Comments

Output from a Sector Dump can be checked against that received by doing a forced memory module dump (control program option).

Module and sector bits have been chosen such that the starting sector is less than the ending sector, starting sector is greater than the ending sector, and the starting sector is equal the ending sector.

## 2.17 Sector Sum Check Routine

### 2.17.1 Function

The purpose of this routine is to allow the RCA-110A launch computer to verify that the instructions and/or data (constants) in a given sector have not been affected by LVDC operations. The Launch Computer specifies the module and the sector(s) within that module to be sum-checked.

### 2.17.2 Options

Module.

Starting Sector.

Ending Sector.

### 2.17.3 Input

<u>Module</u>	<u>Starting Sector</u>	<u>Ending Sector</u>
2	00 <sub>8</sub>	17 <sub>8</sub>
5	12	05
0	00	00

### 2.17.4 Expected Output

Sector sum-check of sectors 0-17 of module 2.

Sector sum-check of sectors 12-17 and 0-5 of module 5.

Sector sum-check of sector 0 of module 0.

### 2.17.5 Comments

The LVDC sector sum checks should equal the sum checks calculated by the preflight simulator control program.

Module and sector bits have been chosen such that the starting sector is less than the ending sector, starting sector is greater than the ending sector, and the starting sector is equal the ending sector.

## 2.18 Special Loader

### 2.18.1 Function

The Preflight Special Loader is a package which performs the same functions as these routines:

- Verify and Prepare to Load Routine.
- Load Routine.
- Sector Dump Routine.

This package is contained in module 1, sector 17. The Special Loader Mode Determine routine may be entered from the preflight Power Up and Initialize routine or Mode Sort routine.

### 2.18.2 Options

The options and input word formats for the Special Loader routines are the same as those of the Verify and Prepare to Load, Load, and Sector Dump routines, however, the ending sector bits of the Sector Dump routine input word are ignored. Only one sector is dumped per command.

### 2.18.3 Input

#### 2.18.3.1 Verify Fixed Linkages

Entry to special loader is 1,17,0,001. All routines and subroutines are contained in 1,17.

Tables of 100 locations each must start at 0,04,234 and 0,06,234.

#### 2.18.3.2 Sector Dump

<u>Module</u>	<u>Starting Sector</u>	<u>Ending Sector</u>
0	00 <sub>8</sub>	00 <sub>8</sub>
1	00	00
2	07	07
4	10	12

### 2.18.3.3 Prepare to Load

<u>Module</u>	<u>Sector</u>	<u>Address</u>	<u>Data</u>
5	00 <sub>8</sub>	000 <sub>8</sub>	000000000 <sub>8</sub>
5	00	007	777777776
2	07	070	252525252
4	10	300	525252524

### 2.18.3.4 Load

Perform modifications indicated in Prepare to Load .

### 2.18.3 Verify

<u>Module</u>	<u>Sector</u>	<u>Address</u>	<u>Data Expected</u>
5	00 <sub>8</sub>	000 <sub>8</sub>	000000000 <sub>8</sub>
5	00	007	777777776
2	07	070	252525252
4	10	300	525252524

### 2.18.4 Comments

Restore altered core locations. Output from sector dump can be checked against that received by doing a forced dump (control program option). Verification requests select all input bits in each state.

### 2.18.5 Expected Output

#### 2.18.5.1 Sector Dump

<u>Module</u>	<u>Sector</u>	
0	00 <sub>8</sub>	
1	00	
2	07	
4	10	2-30

#### 2.18.5.2 Prepare to Load

<u>Control Word</u>	<u>Data</u>
(The control	000000000 <sub>8</sub>
program verifies	777777776
contents of	252525252
telemetry	525252524

#### 2.18.5.3 Load

None telemetered.

#### 2.18.3.4 Verify

<u>Control Word</u>	<u>Data</u>
(The control	000000000 <sub>8</sub>
program verifies	777777776
contents of	252525252
telemetry)	525252524

#### 2.19 Switch Selector Test

##### 2.19.1 Function

The Switch Selector Routine provides the capability of exercising the vehicle switch selector drivers in the LVDA. The routine tests all readings in the reset condition for zero, and tests stage select bits of the input word to prevent exercising more than two switch selectors at one time. It then issues the requested address to the selected switch selector, delays 20 milliseconds, and verifies switch selector feedbacks directly through the CIU (if present). It also verifies the stage select bit through the CIU (if present).

### 2.19.2 Options

Specify stage bits (maximum of 2).

Specify address bits.

Specify CIU present.

Specify switch selector relay present.

Specify a switch selector read command.

Specify switch selector channel A or B.

### 2.19.3 Input

<u>Stage Bit(s)</u>	<u>Address</u>	<u>CIU</u>	<u>Relay</u>	<u>Read</u>	<u>Channel</u>
S2,IU	370 <sub>8</sub>	Y	N	Y	A
S1,S4	007	N	Y	N	B
IU,Spare	377	Y	Y	Y	A

### 2.19.4 Comments

All options will be exercised in both on and off state. The switch selector feedback shall be delayed in relationship to the issuance of the options in order to simulate the actual hardware.

### 2.19.5 Expected Output

No output expected.

## 2.20 Telemetry Test Routine

### 2.20.1 Function

The Telemetry Test Routine provides the capability to check the telemetry system for proper operation by providing computer telemetry and DOM telemetry at a selectable rate.

## 2.20.2 Options

Select mode 0 (indefinite length loop):

- 4.183 ms. telemetry rate (A).
- 4.347 ms. telemetry rate (B).
- 4.511 ms. telemetry rate (C).
- 8.285 ms. telemetry rate (D).
- 8.941 ms. telemetry rate (E).
- Rate supplied by previous load.

Select mode 1 (run each rate (A-E) 3 minutes)

## 2.20.3 Input

<u>Mode</u>	<u>4.183</u>	<u>4.347</u>	<u>4.511</u>	<u>8.285</u>	<u>8.941</u>	<u>Rate Supplied By Previous Load</u>
0	Yes	No	No	No	No	No
0	No	Yes	No	No	No	No
0	No	No	Yes	No	No	No
0	No	No	No	Yes	No	No
0	No	No	No	No	Yes	No
0	No	No	No	No	No	Yes
1	Run rates (A-E) for a period of three minutes each					

## 2.20.4 Comments

All telemetry rates will be exercised in the verification procedure. The routine will exit to Mode Sort if the mode = 1 upon completion. If the mode = 0, the only exit from the routine is via the RCA-110A interrupt, which causes an exit to Forced Begin.

## 2.20.5 Expected Output

Telemetry Data		
<u>PIO</u>	<u>DATA</u>	<u>TYPE</u>
001 <sub>8</sub>	707070706 <sub>8</sub>	LVDC
771	777777776	LVDC
521	525252524	LVDC
025	252525252	LVDC
077	774007776	DOM

The control program verifies the telemetry and indicates the telemetry rate issued.

## 2.21 Verify and Prepare to Load

### 2.21.1 Function

This routine has two distinct modes. Mode 1 (Verify) allows the launch computer to obtain the contents of any LVDC memory location. Mode 2 (Prepare to Load) allows the launch computer to specify the desired contents of any LVDC memory location. (The actual core modification occurs upon execution of the Load Routine subsequent to the Prepare to Load).

### 2.21.2 Options

Mode (Verify, Prepare to Load).

Last group.

Simplex or duplex (Prepare to Load only).

Module.

Sector.

Address.

Data to load (Prepare to Load only).

### 2.21.3 Input

	<u>Mode</u>	<u>Module</u>	<u>Sector</u>	<u>Address</u>	<u>S/D</u>	<u>Last Group</u>	<u>Data</u>
1)	Prep. to Load	5	01 <sub>8</sub>	125 <sub>8</sub>	0	1	525252524 <sub>8</sub>
2)			Perform Load				
3)	Verify	5	01	125	0	1	
4)	Prep. to Load	2	10	252	1	0	252525252
	Prep. to Load	4	06	377	1	1	777777776
5)			Perform Load				
6)	Verify	2	10	252	0	0	
	Verify	4	06	377	0	1	

### 2.21.4 Comments

The contents of the telemetered control word are verified by the control program and any failure is reported. The data word contents are displayed.

After a Prepare to Load, the successful execution of the Load Routine provides verification of the Load Routine.

### 2.21.5 Expected Output

	<u>Control Word</u>	<u>Data</u>
1)	(The control	525252524 <sub>8</sub>
2)	program	----
3)	verifies	525252524
4)	contents of	252525252
	telemetry)	777777776
5)		----
6)		252525252
		777777776

## SECTION 3

### LVDC PREFLIGHT ERROR CONDITIONS VERIFICATION

#### 3.1 Introduction

The LVDC Preflight Error Conditions Verification exercises those preflight program variations caused by recognition of error conditions. The preflight routines report the error conditions by the telemetry of error messages. The Error Conditions Verification, therefore, exercises each routine of the LVDC Preflight Program which can telemeter error messages. The control program used to perform the verification plan forces the RCA-110A input word error or the hardware performance error tested for by each routine. The preflight routine telemetry is compared against expected, and any deviations are reported by the control program. Upon successful completion of the tests for a preflight routine, the error message telemetry received is printed.

This section contains two parts for each preflight routine tested:

- Preflight Function
- Error Test Organization

The Preflight Function describes the purpose of the routine, emphasizing the routines relation to the error conditions tested. The number of error messages which can be telemetered by the routine is indicated. Appendix B lists the error messages by routine.

The Error Test Organization defines the method the control program employs in indicating the error conditions to the preflight routine. Certain error conditions are mutually exclusive. For example, the error condition which states that COD counter 1 is greater than COD counter 2, and the error condition which

states that COD counter 2 is greater than COD counter 1 are mutually exclusive conditions. Thus, the Error Test is sub-divided into sequences, where a sequence defines the error condition(s) generated for a single execution of the preflight routine. When the control program completes a sequence, all conditions are reset to normal and the next sequence is performed.

Certain control program capabilities and limitations are pertinent to the Error Test definition. These include:

- The contents of COD counter 1 and 2 for any axis and any resolver may be specified in failure control counter 'A' and 'B'.
- Timing functions within LVDA may be stopped while LVDC continues operation (DST discrete control). This control stops real time clock from incrementing and simultaneously stops timer 1 and 2 counters from decrementing.
- The rate at which accelerometers increment by channel and axis may be specified.
- The contents and operation of most registers internal to the LVDA can not be directly controlled. These include interrupt inhibit, interrupt limit, ladder error circuitry, and memory error circuitry functions.
- The preflight simulator control program can, however, identify execution of any PIO by the LVDC Preflight Program. The control program can stop execution, specify results of PIO by loading the LVDC accumulator and then restarting the LVDC Preflight Program. In this operation the LVDC Preflight Program timing is unaffected. Thus, the effect is a real time operation of the preflight routines where error conditions are supplied by a control program.

Appendix B lists the error message telemetry by routine and by sequence within the routine.

### 3.2 LVDC Timing and Counter Subroutine

#### 3.2.1 Preflight Function

The LVDA Timing and Counter subroutine is executed in the Mode Sort loop. This subroutine monitors:

- Real time clock.
- Minor Loop timer.
- Switch Selector timer.
- Duplex COD counters.
- Duplex accelerometers.

Twenty-four error messages can be telemetered by this subroutine (see Appendix B).

#### 3.2.2 Error Test Organization

##### 3.2.2.1 First Sequence

- a) Stop LVDC on a read error monitor register instruction (PIO 023), guaranteeing that execution is not in LVDA Timing and Counter Subroutine.
- b) Drive 'A' accelerometers X, Y, Z at max. rate.  
Drive 'B' accelerometers X, Y, Z at 0 rate.  
This will result in  $\Delta A \neq \Delta B$ .

- c) Set for failure control of COD counters A and B.

Set for counter 'A' to be  $6024_8$ .

Set for counter 'B' to be  $6040_8$ .

This will cause errors in A - B order.

- d) Load BYPASS word to make subroutine run accelerometer tests.

- e) Set FCDD bit which stops timing functions in LVDA (FCDD discrete control bit DST). This stops real time clock from counting and stops timers from counting down.

- f) Reset ICR 11 bit when subroutine sets it. (single step function)

#### 3.2.2.2 Second Sequence

- a) See step a) above

- b) Set for failure control COD counters A & B

- c) Set counter 'A' =  $6020_8$ .

Set counter 'B' =  $6006_8$ .

This will generate disagreement bit and failure in B - A order.

- d) Single step to set minor loop inhibit and reset inhibit causing failure indication on inhibit function.

#### 3.2.2.3 Third Sequence

- a) See step a) above.

- b) Single step to set switch selector inhibit, reset inhibit, causing failure indication on inhibit function.

#### 3.2.2.4 Fourth Sequence

- a) See step a) above.

- b) Single step to read interrupt storage register, and advance two instructions.

- c) Set accumulator = 0, causing reset of interrupt control latch but not minor loop bit.

This indicates failure of limiting function.

#### 3.2.2.5 Fifth Sequence

- a) See step a) above.
- b) Set single step to reset switch selector interrupt bit in the interrupt storage register, advance two instructions to read the ISR, and put switch selector bit into the accumulator, indicating a limit function failure.
- c) Load BYPASS to prevent running of minor loop test. This makes the sequence of PIO's correct for step b).

#### 3.2.2.6 Sixth Sequence

- a) See step a) above.
- b) Single step past first minor loop test (inhibit set) to second load of minor loop counter. Go to reset of minor loop bit when the interrupt is received. Advance two instructions to read ISR, and put minor loop bit in the accumulator.  
This indicates failure of reset logic.
- c) Load BYPASS to cancel effects of step c) above.

#### 3.2.2.7 Seventh Sequence

- a) See step a) above.
- b) As for minor loop, single step past first switch selector test (inhibit set) to second load of switch selector counter. Go to reset of switch selector interrupt, and advance two instructions to read ISR. Put switch selector bit into accumulator.  
This indicates failure of limiting function.

- c) Load BYPASS to prevent running of minor loop test. This makes the sequence of PIO's for step b) correct.

#### 3.2.2.8 Eighth Sequence

- a) See step a) above.
- b) Set to fail COD counters A.  
Set counter 'A' =  $6010_8$ .  
Set counter 'B' =  $6016_8$ .  
This sets disagreement bit on, but difference tests will pass.
- c) Reset ICR 8 when test sets it. This causes disagreement bit to occur when it is not expected.
- d) Load BYPASS to cancel effects of step c) above.

#### 3.2.2.9 Ninth Sequence

- a) See step a) above.
- b) Set to fail COD counter.  
Set counter 'A' =  $6010_8$ .  
Set counter 'B' =  $6016_8$ .
- c) Single step to set internal control register bit 8 during test of disagreement bit logic, i.e., when ICR 11 first set. ICR 8 will disable disagreement bit when it is expected.

#### 3.2.2.10 Tenth Sequence

- a) Reset ERROR mode flag.
- b) Display completed message.

### 3.3 Minor Loop, Switch Selector, Real Time Counter Routine

#### 3.3.1 Preflight Function

The Minor Loop, Switch Selector, Real Time Counter routine is a commanded preflight routine. This routine verifies the operation of the real time clock and the two timers. The minor loop timer and the switch selector timer are checked by calculating the time interval between the load of the counter and receipt of the interrupt.

Six error messages can be telemetered from the routine (see Appendix B).

#### 3.3.2 Error Test Organization

##### 3.3.2.1 First Sequence

- a) Command Preflight to the Minor Loop, Switch Selector, Real Time Counter routine.
- b) Set FCDD bit which stops LVDA timing functions (FCDD discrete control bit DST). This causes a real time clock failure.

##### 3.3.2.2 Second Sequence

- a) See step a) above.
- b) Single step to load minor loop counters. Load counters with a 0. This will cause minor loop interrupt to occur early.

##### 3.3.2.3 Third Sequence

- a) See step a) above.
- b) Single step to check for Switch Selector bit after minor loop occurred properly (second read of ISR). Put Switch Selector bit into accumulator indicating switch selector occurred early.

#### 3.3.2.4 Fourth Sequence

- a) See step a) above.
- b) Single step to load switch selector counter. Reload counter with full counter. This will cause no switch selector interrupt to occur.

#### 3.3.2.5 Fifth Sequence

- a) See step a) above.
- b) Single step to load switch selector counter. Reload with 1 bit. This will cause no minor loop operation and an early switch selector interrupt.

#### 3.3.2.6 Sixth Sequence

- a) See step a) above.
- b) Single step to release minor loop inhibit. Inhibit minor loop interrupt. This will cause no minor loop interrupt and a switch selector interrupt at the correct time.

#### 3.3.2.7 Seventh Sequence

- a) Reset error mode flag.
- b) Display completed message.

### 3.4 Mode Sort Routine

#### 3.4.1 Preflight Function

The Mode Sort routine is executed as a minor loop. The routine monitors the EMR register and accepts mode commands from the ground. There are other functions performed in the loop; however, they are discussed in each subroutine.

There are four error messages in the Mode Sort routine (see Appendix B).

### 3.4.2 Error Test Organization

#### 3.4.2.1 First Sequence

- a) Single step to EMR read in the Error Monitor subroutine of the mode sort loop. Put a  $600_8$  into the accumulator. These are TLC bits which cannot be accepted. From this point, single step to next error read (second read in mode sort loop), and set EM8 bit in the accumulator. This will cause an error, since EM8 is not accepted on second read of EMR.

#### 3.4.2.2 Second Sequence

- a) Load command receiver/RCA register with zeros. This is an error, as only mode commands (mode bit = 1) are accepted in Mode Sort.

#### 3.4.2.3 Third Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

#### 3.4.2.4 Fourth Sequence

- a) Set the SCB bit and reset the SCA bit in the DIS register.

### 3.5 Telemetry Test

#### 3.5.1 Preflight Function

The Telemetry Test routine is a commanded preflight program. This routine accepts an input word which defines the rate at which to telemeter data. The routine then telemeters data bit patterns to test the system.

There is one error message in the telemetry test (see Appendix B).

### 3.5.2 Error Test Organization

#### 3.5.2.1 First Sequence

- a) Command Telemetry Test and issue an input word of 0. An input word of 0 is unacceptable to the telemetry test.

#### 3.5.2.2 Second Sequence

- a) Reset error flag.
- b) Display 'completed' message.

### 3.6 Read Input Data Subroutine

#### 3.6.1 Preflight Function

The Read Input Data Subroutine is a preflight utility subroutine which handles ground/LVDC interface in accepting data words.

There is one error message issued from the read input data subroutine (see Appendix B).

#### 3.6.2 Error Test Organization

##### 3.6.2.1 First Sequence

- a) Command the Telemetry Test routine. Issue an input word with the mode bit = 1. This is an error.

##### 3.6.2.2 Second Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.7 CIU Data Read Routine

#### 3.7.1 Preflight Function

The CIU Read Data routine is a preflight commanded routine. This routine requests data from the CIU by loading the CIU register with an address in the CIU. When the requested address is found in the strobe of the CIU, the data is loaded into the data register and an interrupt is generated.

There are two messages issued by the routine (see Appendix B).

#### 3.7.2 Error Test Organization

##### 3.7.2.1 First Sequence

- a) Command the CIU data read routine and issue the required input word.
- b) Do not respond to CIU data request. This will cause routine to time out and issue an error message.

##### 3.7.2.2 Second Sequence

- a) As step a) above, except single step from load of CIU address bits (PIO 042<sub>8</sub>) to the EMR read (PIO 023<sub>8</sub>) made by the routine when the data register is read. Supply unacceptable EMR bits.

##### 3.7.2.3 Third Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.8 G and C Steering Routine

#### 3.8.1 Preflight Function

The G and C Steering routine is a commanded preflight routine. This routine will call the flight program minor loop processor upon receipt of a minor loop interrupt. The routine times out, if a delay of more than 30 milliseconds occurs before receiving an interrupt.

There is one error message issued from this routine (see Appendix B).

#### 3.8.2 Error Test Organization

##### 3.8.2.1 First Sequence

- a) Command G and C Steering routine.
- b) Set the FCDD control (DST), which stops timing functions in the LVDA so no minor loop will occur.

##### 3.8.2.2 Second Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.9 DOM Test

#### 3.9.1 Preflight Function

The DOM test is a commanded preflight routine. The functions of the DOM are verified by telemetering data bit patterns. One specific function of the DOM is performed when minor loop interrupt occurs.

There is one error message issued by this routine (see Appendix B).

#### 3.9.2.1 First Sequence

- a) Command preflight DOM test.
- b) Set FCDD control (DST) which stops timing functions in the LVDA so no minor loop interrupt will occur.

#### 3.9.2.2 Second Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.10 Ladder Error Test

#### 3.10.1 Preflight Function

The Ladder Error test is a commanded preflight routine. This routine exercises the converter switching logic of the ladders. Under the specifications of the analog converters, this test verifies that the converters will or will not switch and that such a switch is recorded in the EMR bit 17 and DIS ladder bits.

#### 3.10.2 Error Test Organization

##### 3.10.2.1 First Sequence - Test Select Converter A in EMR

Error test indicating failure by setting SCB in EMR.

- a) Command Ladder Error Test, clamp ladders to zero, and set ICR function to select converter A.
- b) Single step to first read of DIS. Advance two instructions to read of EMR where bit 17 should be zero. Put 17 into the accumulator to indicate SCB where no SCB is expected.

If the following sequences are performed as listed, the errors may be generated without commanding the ladder routine after each error.

### 3.10.2.2 Second Sequence

This error test indicates failure by setting SCB in the DIS.

- a) Same as a) above.
- b) Test Select Converter A in DIS - Single step to set read of DIS.  
Indicate converter B selected by putting bits 18 and 19 in the accumulator.

From this point, the sequence generates errors on tests of the EMR.

### ICR 2 TESTS

- c) +.192V (4 bits) Ladder Command Test - Indicate SCB on issuance of +.192V (4 bits) ladder command by single stepping from PIO 146<sub>8</sub> to read of EMR (PIO 023<sub>8</sub>) and putting bit 17 into the accumulator.
- d) Test to Reselect Converter A on EMR Error from c) - On attempt to reselect converter A, single step from issuance of 0 pitch (PIO 146<sub>8</sub>) command to read of DIS (PIO 053<sub>8</sub>), which is after dummy EMR read. Advance computer 2 instructions to second read of EMR, and indicate converter B still selected by putting bit 17 into accumulator.
- e) +.384V (8 bits) Ladder Command Test - Single step from issuance of +.384V pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Advance two instructions to read of EMR, and indicate no SCB by putting a zero into the accumulator.
- f) Test to Reselect Converter A before Negative Ladder Command Tests - On attempt to reselect converter A, single step from issuance of 0 pitch ladder command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>), which is

past the dummy EMR read. Advance two instructions to second read of EMR (PIO 023), and put bit 17 into the accumulator indicating SCB.

- g) -.192V (4 bits) Ladder Command Test - Single step from issuance of -.192V pitch command (PIO 146<sub>g</sub>) to the read of EMR (PIO 023<sub>g</sub>).

Indicate SCB by putting bit 17 into the accumulator.

- h) Test to Reselect Converter A on Error from g) - On attempt to reselect converter A, single step from issuance of 0 pitch command (PIO 146<sub>g</sub>) to read of DIS (PIO 053<sub>g</sub>), which is past dummy EMR read.

- i) -.384V (8 bits) Ladder Command Test - Single step from issuance of -.384V (8 bits) command to read of DIS (PIO 053<sub>g</sub>), which is past dummy EMR read. Advance 2 instructions to second EMR read, and put 0 into accumulator to indicate converter A still selected.

- j) Test to Reselect Converter A before Legal PIO Test (ICR 11) - On attempt to reselect converter A, single step from 0 pitch command (PIO 146<sub>g</sub>) to read of DIS (PIO 053<sub>g</sub>), which is past dummy EMR read. Advance 2 instructions to EMR read, and put bit 17 into accumulator to indicate SCB.

#### LEGAL PIO (ICR 11) TEST

- k) Forced SCB (ICR 11) Test (First EMR read) - Advance from step j) to next read of DIS. This read of DIS is executed 4 instruction times past the SCB which is forced by setting ICR 11. Advance 2 instructions to read of EMR and put bit 17 into accumulator to indicate SCB. The bit should not appear in EMR until the eleventh instruction past forced SCB.

- l) Reselect Converter A Test (before mode sort exit) - Single step from issuance of 0 pitch command (PIO 146<sub>g</sub>) to read of DIS (PIO 053<sub>g</sub>),

which is past dummy EMR read. Advance 2 instructions to read of EMR.

Put bit 17 into accumulator to indicate SCB.

### 3.10.2.3 Third Sequence

As in the previous sequence a chain is performed. This chain forces an error of DIS status bits in each test.

- a) See step a) above.
- b) +.192V (4 bits) Ladder Command Test - Single step from issuance of +.192V ladder command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.
- c) +.384V (8 bits) Ladder Command Test - Single step from issuance of +.384V pitch ladder command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.
- d) Test to Reselect Converter A - Single step from issuance of 0 pitch ladder command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.
- e) -.192V (4 bits) Ladder Command Test - Single step from issuance of -.192V pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.
- f) -.384V (4 bits) Ladder Command Test - Single step from issuance of -.384V pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.
- g) Test to Reselect Converter A - Single step from issuance of 0 pitch command (PIO 146<sub>8</sub>) to read of DIS. Put bits 18 & 19 into accumulator.

### LEGAL PIO TEST

- h) Forced SCB Test (First DIS read) - Advance to issuance of pitch command (PIO 146<sub>8</sub>). Advance to read of EMR (PIO 023<sub>8</sub>). The advance

to EMR read allowed enough time for SCB to occur. The test of the first read of DIS will fail. Put 0 into accumulator to allow test of first EMR read to pass.

- i) Reselect Converter A Test (before mode sort exit) - Single step from issuance of 0 pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.

#### 3.10.2.4 Fourth Sequence

- a) See step a) above.
- b) +.192V (4 bits) Ladder Command Test - Single step from issuance of +.192V pitch command (PIO 146<sub>8</sub>) to read of EMR (PIO 023<sub>8</sub>). Put bit 17 into accumulator to show SCB. [same as step c) of sequence 2].
- c) Test to Reselect Converter A on EMR Error from b) - Single step from issuance of 0 pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.

#### 3.10.2.5 Fifth Sequence

##### LEGAL PIO TEST

Error test indicating failure of EMR test on second read.

- a) See step a) above.
- b) Second EMR Read Test - Using compares on setting of the ICR (PIO 022<sub>8</sub>), single step to last read of DIS before Legal PIO test. Advance 10 instructions to point where bit 14 is in the accumulator. Put bit 12 into accumulator (ICR 14 set instead of ICR 11). SCB will not occur.

#### 3.10.2.6 Sixth Sequence

Error test indicating failure of DIS test on second DIS read.

- a) See step a) above.

- b) Second DIS Read Test - Using compares on the setting of the ICR (PIO 022<sub>8</sub>), single step to the last read of the DIS before legal PIO test. Advance 10 instructions to point where bit 15 is put into accumulator for setting of ICR 11. Put 12 in accumulator (ICR 14 selects converter A). Advance to first read of EMR (PIO 023<sub>8</sub>) and then to second read of EMR (PIO 023<sub>8</sub>). Put bit 17 into accumulator indicating SCB as expected. Test on second read of DIS will fail, since true SCB occurred.

### 3.10.2.7 Seventh Sequence

Error test indicating failure of the EMR on - .192V (4 bits) ladder command and a DIS failure on attempt to reselect converter A.

- a) See step a) above.
- b) Using compare on pitch ladder command, single step to read of EMR in -.192V test. Put 17 into accumulator to show SCB.
- c) Test to reselect converter A on EMR error from b).
- d) Single step from issuance of 0 pitch command (PIO 146<sub>8</sub>) to read of DIS (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.

### 3.10.2.8 Eighth Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

## 3.11 Interrupt Processor

### 3.11.1 Preflight Function

The Interrupt Processor is a preflight utility subroutine which determines the cause of any HOP 400<sub>8</sub>.

There are two error messages issued directly from Interrupt Processor (see Appendix B).

### 3.11.2 Error Test Organization

#### 3.11.2.1 First Sequence

- a) Single step from one EMR read (PIO 023<sub>8</sub>) in Mode Sort to next EMR read (PIO 023<sub>8</sub>). This guarantees that execution is not in the LVDA Timing & Counter test.
- b) Reset minor loop inhibit and load minor loop counter with one bit. Interrupt will occur and preflight mask will show minor loop as inhibited.

#### 3.11.2.2 Second Sequence

- a) See step a) above.
- b) Single step to read interrupt storage register (PIO 137<sub>8</sub>). Put TLC interrupt bit into accumulator and set all inhibits.

#### 3.11.2.3 Third Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.12 Verify and Prepare to Load

#### 3.12.1 Preflight Function

This preflight commanded routine accepts input words from which it generates two control words that are telemetered to the ground. For a verify, the first control word contains a CLA instruction, and the second control word contains the

26 data bit result of CLA. For a prepare to load, the first control word is a store instruction (STO), and the second is the 26 data bits that are stored.

There are seven error messages issued by this routine (see Appendix B).

### 3.12.2 Error Test Organization

#### 3.12.2.1 First Sequence

- a) Command Verify and Prepare to Load. Set word count  $\neq 00_2$  on first input word.

#### 3.12.2.2 Second Sequence

- a) Command as before. On second input word set word count  $\neq 01_2$ .

#### 3.12.2.3 Third Sequence

- a) Command as before. Set third word count  $\neq 10_2$ .

#### 3.12.2.4 Fourth Sequence

- a) Command as before. Set fourth word count  $\neq 11_2$ .

#### 3.12.2.5 Fifth Sequence

- a) Command as before. On second set of input words switch from verify mode to prepare to load mode.

#### 3.12.2.6 Sixth Sequence

- a) Command as before. Attempt to verify 51 locations. This should exceed allowed space for verify operations.

#### 3.12.2.7 Seventh Sequence

- a) Command as before. Attempt to verify a location. Single step from read of input word (PIO 043<sub>8</sub>) to read of EMR (PIO 023<sub>8</sub>). Put bits S-2 into accumulator to indicate TLC occurred when verify was done.

#### 3.12.2.8 Eighth Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.13 Exercise Attitude Command Test

#### 3.13.1 Preflight Function

This commanded preflight routine drives the ladders using the rate, converter, direction, and magnitude specified by the user or a pre-determined profile.

There are four error messages issued by this routine (see Appendix B).

#### 3.13.2 Error Test Organization

##### 3.13.2.1 First Sequence

- a) Select user specified mode and request converter B. Single step from the ladder clamp (PIO 172<sub>8</sub>) to reset of ICR 11 function (PIO 026<sub>8</sub>). Advance two instructions to point where EMR contents are in accumulator, and put 0 into accumulator to show no SCB.

##### 3.13.2.2 Second Sequence

- a) Select user specified mode and request converter B. Single step from the ladder clamp (PIO 172<sub>8</sub>) to DIS read (PIO 053<sub>8</sub>). Put bits 18 & 19 in accumulator for DIS error.

#### 3.13.2.3 Third Sequence

- a) Select user specified mode and request converter A. Single step from the ladder clamp (PIO 172<sub>8</sub>) to read DIS (PIO 053<sub>8</sub>). Advance three instructions to EMR test, and put bit 17 in accumulator to show SCB.

#### 3.13.2.4 Fourth Sequence

- a) Select user specified mode and request converter A. Single step from the ladder clamp (PIO 172<sub>8</sub>) to DIS read (PIO 053<sub>8</sub>). Put bits 18 & 19 into accumulator.

#### 3.13.2.5 Fifth Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.14 Load Routine

#### 3.14.1 Preflight Function

This commanded preflight routine performs the load of LVDC core locations using the control words accepted by the Verify and Prepare to Load routine.

There are two error messages issued by this routine (see Appendix B).

#### 3.14.2 Error Test Organization

##### 3.14.2.1 First Sequence

- a) Command Load routine. No previous prepare to load commanded.

#### 3.14.2.2 Second Sequence

- a) Command "Sim Flight without a platform" mode of Prepare to Launch.
- b) Load Bypass to prevent running tests.
- c) Use S/360/44 routine to call Verify & Prepare to Load for a prepare to load location (0,16,300). The command the load routine. (This address is not in the allowed range of load locations when in Prepare to Launch.)

#### 3.14.2.3 Third Sequence

- a) Reset Bypass = 0.
- b) Reset error mode flag.
- c) Display 'completed' message.

### 3.15 Resolver Error Subroutine

#### 3.15.1 Preflight Function

The Resolver Error Subroutine is used by gimbal angle routines to determine the cause of a disagreement bit resulting from a duplex gimbal read. The subroutine performs start and stop COD counter PIO's. If the COD counters fail, this subroutine will issue an error message; otherwise, control is returned to the caller immediately.

There is one error message issued by this subroutine (see Appendix B).

#### 3.15.2 Error Test Organization

##### 3.15.2.1 First Sequence

- a) Command preflight to the Gimbal Angle Monitor routine, and request that a read of the coarse gimbal angles be performed.

- b) Force the COD counters and the coarse gimbal angles to fail.

#### 3.15.2.2 Second Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

### 3.16 Switch Selector Test

#### 3.16.1 Preflight Function

The commanded preflight Switch Selector Test exercises and verifies the switch selector system. The routine accepts two input words which define the switch selector stage and address, presence of the CIU, switch selector relay, whether a read should be done, and selection of channel A or B. The proper functioning of feedback readings are tested in the reset condition and after issuing requested stage and address. The functions are verified through the CIU, if it is present.

#### 3.16.2 Error Test Organization

A generalized control program routine handles the command of the preflight Switch Selector Test and supplies input as demanded by a parameter list. The parameters specify:

- 1) Switch selector stage and address bits.
- 2) CIU, switch selector relay, read, and channel bits.
- 3) Current error mode sequence number.
- 4) Flag to specify allowing automatic switch selector feedbacks or feedbacks specified by the control program.
- 5) Address of switch selector feedback (SSFB), if supplied to the control program.

- 6) Address of CIU data to supply if the simulator specifies that the CIU is present.

There are three feedback states associated with the switch selector which are tested as follows:

- 1) Initial SSFB.
- 2) SSFB after issuance of stage and address.
- 3) SSFB after reset issuance.

There are six feedback states associated with the switch selector, if the presence of the CIU is indicated in the control program parameter input. The six states are tested as follows:

- 1) CIU initial address feedback.
- 2) CIU initial stage, read and reset bits feedbacks.
- 3) CIU address feedback complement after switch selector stage & address is issued.
- 4) CIU stage feedback.
- 5) CIU read/reset bit feedback after read switch selector command is issued.
- 6) CIU read/reset bit feedback after reset switch selector command is issued.

#### 3.16.2.1 First Sequence

##### Initial Switch Selector Address Selection Feedback Test

- a) Supply SSFB data word:

- 1) 003770000<sub>8</sub>

### 3.16.2.2 Second Sequence

#### Initial CIU Switch Selector Address Selection Feedback Test

- a) The CIU is present. Allow automatic SSFB.

Supply CIU data word:

- 1) 776000000<sub>8</sub>

### 3.16.2.3 Third Sequence

#### Initial CIU Switch Selector Stage Selection Feedback Test

- a) The CIU is present. Allow automatic SSFB.

Supply CIU data words:

- 1) 0  
2) 740000000<sub>8</sub>

### 3.16.2.4 Fourth Sequence

#### Initial CIU Switch Selector Read and/or Reset Feedback Test

- a) The CIU is present. Allow automatic SSFB.

Supply CIU data words:

- 1) 0  
2) 014000000<sub>8</sub>

### 3.16.2.5 Fifth Sequence

#### Switch Selector Commanded Stages Selected Test

- a) No CIU is present. Allow automatic SSFB and select more than two stages in RCA input word.

### 3.16.2.6 Sixth Sequence

#### CIU/Direct Switch Selector Address Selection Feedbacks Test

- a) The CIU is present. Allow automatic SSFB.

Supply CIU data words:

- 1) 0
- 2) 0
- 3) 0

#### 3.16.2.7 Seventh Sequence

##### Direct Switch Selector Feedback/Complement Test

- a) No CIU is present. Inhibit the automatic SSFB.

Supply SSFB data words:

- 1) 0
- 2) 0

#### 3.16.2.8 Eighth Sequence

##### CIU/Direct Switch Selector Address Selection Feedback Test (2nd Pass)

- a) The CIU is present. Allow automatic SSFB and request switch selector address 01001001.

Supply CIU data words:

- 1) 0
- 2) 0
- 3) 332000000<sub>8</sub>
- 4) 0

#### 3.16.2.9 Ninth Sequence

##### Direct Switch Selector Feedback/Complement Test (2nd Pass)

- a) No CIU is present. Inhibit the automatic SSFB and request switch selector address 01001001.

Supply data words:

- 1) 0
- 2) 002600000<sub>8</sub>
- 3) 0

### 3.16.2.10 Tenth Sequence

#### CIU Stage Selection/Requested Stage Selection Feedback Test

- a) The CIU is present. Allow automatic SSFB and request switch selector address 01001001.

- 1) 0
- 2) 0
- 3) 332000000<sub>8</sub>
- 4) 332000000<sub>8</sub>
- 5) 0

### 3.16.2.11 Eleventh Sequence

#### CIU Read Bit Test

- a) The CIU is present. Allow the automatic SSFB and request switch selector address 01001001.

Supply CIU data words:

- 1) 0
- 2) 0
- 3) 332000000<sub>8</sub>
- 4) 332000000<sub>8</sub>
- 5) 040000000<sub>8</sub>
- 6) 0

### 3.16.2.12 Twelfth Sequence

#### Switch Selector Reset Bit Test

- a) No CIU is present. Inhibit the automatic SSFB and request the IU stage and address 01001001.

### 3.16.2.13 Thirteenth Sequence

#### CIU Reset Bit Test

- a) The CIU is present. Allow automatic SSFB and request address 01001001.

Supply CIU data words:

- 1) 0
- 2) 0
- 3) 332000000<sub>8</sub>
- 4) 332000000<sub>8</sub>
- 5) 040000000<sub>8</sub>
- 6) 010000000<sub>8</sub>
- 7) 0

### 3.16.2.14 Fourteenth Sequence

- a) Reset error mode flag.
- b) Display 'completed' message.

## 3.17 Self Test Subroutine

### 3.17.1 Preflight Function

This subroutine is executed in the mode sort loop. The subroutine tests the LVDC instructions by performing each instruction with predictable results and then verifying the results.

### 3.17.2 Error Test Organization

The error detection test package is based on hardware perturbations through the FCDD; however, the Self Test Subroutine tests the LVDC instructions, none of which are controllable through the FCDD. The error test, therefore, resorts to modifying the assembled constants used by the Self Test program. Since there

is only one Self Test error message, the error test reads the Self Test HOP constant which is unique for each failure. This HOP constant replaces the contents of the EMR in the documentation of the Self Test Subroutine.

One error test routine is repeatedly executed to generate the Self Test failures. Upon each execution, this routine increments the error test current sequence, starting at one proceeding through 35 (see Appendix B). The LVDC constant(s) required for the next failure are loaded, and the constant(s) from the prior failure was restored.

The following defines those constants by name and location for each sequence:

<u>Error Test Sequence</u>	<u>LVDC Label</u>	<u>LVDC Location</u>	<u>Contents</u>
1	STZERO	1,07,235	400000000 <sub>8</sub>
2	STZERO	1,07,235	200000000
3	STZERO	1,07,235	000000000
4	STBT6	1,07,243	400000000
4	STBT6	1,07,243	0
5	STBT6	1,07,243	004000000
	STBT9	1,07,244	400000000
6	STBT9	1,07,244	000400000
	STBT23	1,07,246	0
7	STBT23	1,07,246	000000004
8	STBT23	1,07,246	000000014
9	STBT23	1,07,246	000000010
	STBT14	1,07,245	400000000
10	STBT14	1,07,245	000010000
	STK5	1,07,253	0
11	STK5	1,07,253	645645646

	STK7	1,07,255	0
12	STK7	1,07,255	600000000
	STONES	1,07,237	0
13	STONES	1,07,237	777777776
	STK11	1,07,261	0
14	STK11	1,07,261	504664700
	STK13	1,07,263	000000020
15	STK13	1,07,263	041012000
	STBT1	1,07,241	0
	STBT2	1,07,242	0
16	STK12	1,07,262	0
	STK13	1,07,263	0
17	STBT1	1,07,241	200000000
	STBT2	1,07,242	100000000
	STMINS	1,07,236	0
18	STK12	1,07,262	204050030
	STK13	1,07,263	041012000
	STMINS	1,07,236	400000000
	STB1B2	1,07,240	0
19	STB1B2	1,07,240	300000000
	STK16	1,07,266	0
20	STK16	1,07,266	0
	STK18	1,07,270	777777776
21	STK18	1,07,270	006074000
	STK21	1,07,273	0
22	STK21	1,07,273	567107650
	STK23	1,07,275	0

23	STK23	1,07,275	150460674
	STK26	1,07,300	
24	STK26	1,07,300	232314570
	STK29	1,07,303	0
25	STK29	1,07,303	021477510
	STK32	1,07,306	0
26	STK32	1,07,306	217171710 <sub>8</sub>
	STK35	1,07,311	0
27	STK35	1,07,311	440000000
	STK37	1,07,313	0
28	STK37	1,07,313	733606410
	STK39	1,07,315	0
29	STK39	1,07,315	400000400
	STK42	1,07,320	0
30	STK42	1,07,320	337777770
	STK44	1,07,322	100000000
31	STK44	1,07,322	377777776
	STK46	1,07,324	0
32	STK46	1,07,324	137777770
	STK48	1,07,326	0
33	STK48	1,07,326	726654556
	STK51	1,07,331	0
34	STK51	1,07,331	377777770
	STK53	1,07,333	0
35	STK53	1,07,333	046733156

### 3.18 Memory Error Test

#### 3.18.1 Preflight Function

This commanded preflight routine tests the error detection circuitry of the LVDC/LVDA. Using an illegal shift instruction and an illegal PIO instruction, this routine forces TLC, EAM, and EBM failures.

Though 336 error messages can be telemetered from this routine, only 13 unique conditions are tested. Four of these 13 failures can be detected in various combinations of modules and sectors, thus the large total number.

#### 3.18.2 Error Test Organization

The Memory Error Test routine uses a subroutine labeled MESEMR to read and save the contents of the EMR register after generating a failure. The error detection test must modify core to change the PIO 023<sub>8</sub>, which reads the EMR, to a PIO 053<sub>8</sub> in order to read the DIS registers.

##### 3.18.2.1 First Sequence

- a) Read location containing EMR read instruction.
- b) Modify that syllable to perform read of DIS.
- c) Restore location.
- d) Set DIS to 576<sub>8</sub>. This will cause TLC, EAM bits to appear as expected, and unacceptable EMR bits will be present.
- e) Command Memory Error Test.

##### 3.18.2.2 Second Sequence

- a) Set DIS to 400<sub>8</sub>. This will indicate TLC only, which is never acceptable, as either EAM or EBM bit must accompany the TLC.

- b) Command Memory Error Test.
- c) After the seventh error message is telemetered, set location 0,00,504 to 0. Likewise, after the ninth error message is telemetered, set location 1,00,504 to 0. This will indicate a failure of duplex CLA to restore other memory on a TLC. These test locations are restored by Memory Error Test.

#### 3.18.2.3 Third Sequence

- a) Restore the location to read EMR rather than DIS.
- b) Reset error mode flag.
- c) Display 'completed' message.

## SECTION 4

### LVDC PREFLIGHT PREPARE TO LAUNCH VERIFICATION

#### 4.1 Introduction

This section describes the methods used to verify the functions of the preflight Prepare to Launch routine.

#### 4.2 PTL Functional Requirements

The Prepare to Launch routine performs the following functions, when entered at approximately 12 minutes prior to lift-off:

- Executes the LVDC/LVDA self-test program and telemeters the results.
- Monitors accelerometer inputs and calculates the platform off-level indications. Telemeters accelerometer outputs and time.
- Performs reasonableness checks on particular discrete inputs and alerts.
- Interrogates the error monitor register.
- Keeps all ladder outputs zeroed.
- Processes a GRR interrupt and transfers LVDC control to the flight program.
- Samples platform gimbal angles.

#### 4.3 PTL Verification

The Prepare to Launch Verification combines the tasks of nominal and error conditions verification for the Prepare to Launch routine. This section defines the procedures for verification of each functional area of the Prepare to Launch routine. The procedures contain six sections for each functional area:

- Function
- Option

- Input (Nominal)
- Expected Output
- Input (Error)
- Expected Output

The Function describes the particular task performed by a specific portion of the routine.

The Option defines any RCA-110A input or any LVDC constant that is pertinent to the function of the area.

The Input indicates the nominal and error conditions for exercising the function.

The Expected Output specifies the results that must be obtained when exercising Prepare to Launch with the indicated inputs. The indicated error message numbers are in octal.

#### 4.3.1 Sim-Indicator Test (SIMIND)

##### 4.3.1.1 Function

The Sim-Indicator test is required to verify that the mode selected in Prepare to Launch equals the status selected in SIMIND.

##### 4.3.1.2 Option

- Sign bit of SIMIND word equal 1 (flight mode).
- Sign bit of SIMIND word equal 0 (sim flight mode).

#### 4.3.1.3 Nominal Input Test

##### 4.3.1.3.1 Input

- Specify sign bit of SIMIND word equal 1. (Enter PTL on flight mode).
- Specify bit of SIMIND word equal 0. (Enter PTL on sim flight mode).

##### 4.3.1.3.2 Expected Output

- None

#### 4.3.1.4 Error Input Tests

##### 4.3.1.4.1 Input

- Specify sign bit of SIMIND word equal 0. (Enter PTL routine on flight mode, status code 12).

##### 4.3.1.4.2 Expected Output

- Error Message Number 126 - Status code 12 entry was used (flight). However, the sim flight indicator says sim flight. D013 = Reset.

##### 4.3.1.4.3 Input

- Specify sign bit of SIMIND word equal 1. (Enter PTL routine on sim flight mode, status code 30).

##### 4.3.1.4.4 Expected Output

- Error Message Number 1261 - Status code 30 entry was used (sim flight). However, the sim flight indicator says flight. D013 = Reset.

#### 4.3.2 Interrupt Storage Register Test (ISR)

##### 4.3.2.1 Function

The Interrupt Storage Register is required to indicate any invalid interrupts in the ISR.

##### 4.3.2.2 Option

- The ISR ANDing constant.

##### 4.3.2.3 Nominal Input Test

###### 4.3.2.3.1 Input

- Access the LVDC ISR ANDing constant from core.

###### 4.3.2.3.2 Expected Output

- See Table 4.3.2.

##### 4.3.2.4 Error Input Test

###### 4.3.2.4.1 Input

- Set ISR 5.

###### 4.3.2.4.2 Expected Output

- Error Message Number 121 - Interrupt storage register contains bit other than those acceptable. DO13 = Set.

#### 4.3.3 Discrete Input Register (DIN)

##### 4.3.3.1 Function

The Discrete Input Register test is required to indicate any invalid DIN's from the discrete input register.

# INTERRUPT STORAGE REGISTER (ISR) ANDING CONSTANT

PLISR1 = 077200000 (ANDing constant)

The ANDing constant must indicate the following status:

ISR Bit	LVDC Data Word Bit Position	Test Status	Function
12	Sign	IGNORE	Timer 1 (Minor Loop)
11	1	IGNORE	Timer 2 (Switch Selector)
			Internal to the LVDC
10	2	IGNORE	CIU
9	3	OFF	Temporary Loss of Control (TLC)
8a	4	OFF	Command Decoder Interrupt "A"
8b	4	OFF	Command Decoder Interrupt "B"
7	5	OFF	Guidance Reference Release
6	6	OFF	S-II Engines Cutoff
5	7	OFF	S-IC Outboard Engines Cutoff "A"
4	8	OFF	S-IVB Engine Out "B"
3	9	IGNORE	RCA-110A Interrupt
2	10	OFF	S/C Initiation of S-II/S-IVB Separation
			"A" and S/C Initiation of S-IVB Cutoff "A"
1	11	IGNORE	RCA-110A Interrupt
	12	IGNORE	UNUSED BIT
	•	•	•
	•	•	•
	25	IGNORE	UNUSED BIT

NOTE: All functions that are monitored are indicated by a set bit in the corresponding LVDC bit position of the ANDing constant.

Table 4.3.2

#### 4.3.3.2 Options

- DIN ANDing and XORing constants.

#### 4.3.3.3 Nominal Input Test

##### 4.3.3.3.1 Input

- Access the LVDC DIN constants from core.

##### 4.3.3.3.2 Expected Output

- See Table 4.3.3.

#### 4.3.3.4 Error Input Test

##### 4.3.3.4.1 Input

- Set DIN 2.
- Set DIN 4.
- Set DIN 23.

##### 4.3.3.4.2 Expected Output

- Error Message Number 122 - Discrete input bit or bits present other than those acceptable. D013 = Set.

#### 4.3.4 Discrete Input Spares Register (DIS)

##### 4.3.4.1 Function

The Discrete Input Spares Register test is required to indicate any invalid discretes from the discrete input spares register.

# DISCRETE INPUT REGISTER (DIN) ANDING AND XORING CONSTANTS

PLDIN1 = 776774760<sub>8</sub> (ANDing constant)      PLDIN2 = 040570200<sub>8</sub> (XORing constant)

NOTE: All functions that are monitored (ON or OFF) are indicated by a set bit in the corresponding LVDC bit position of the ANDing constant. The test status of a monitored function specified ON is indicated by a set bit in the XORing constant.

The results of the ANDing and XORing constants must indicate the following status.

DIN No.	LVDC Bit Position	Test Status	Function
24	Sign	OFF	Liftoff
23	1	OFF	S/C Initiation of S-IVB Engine Cutoff
22	2	OFF	S/C Initiation of S-II/S-IVB Separation "B" and S/C Initiation of S-IVB Cutoff "B"
21	3	ON	S-II Outboard Engine Out
20	4	OFF	S-IVB Ignition Sequence Start
19	5	OFF	S-II Engine Out
18	6	OFF	S-IC Outboard Engine Cutoff "B"
17	7	OFF	S-IC Inboard Engine Out "A"
16	8	IGNORE	Prepare for Guidance Reference Release
15	9	ON	S-II Aft Interstage Separation
14	10	OFF	S-IC Outboard Engine Out
13	11	ON	S-II Inboard Engine Out
12	12	ON	S-IC/S-II Separation
11	13	ON	S-IC Inboard Engine Out "B"
10	14	ON	S-II/S-IVB Separation
9	15	OFF	Spacecraft Control of Saturn

# DISCRETE INPUT REGISTER (DIN) ANDING AND XORING CONSTANTS (CONTINUED)

8	16	IGNORE	Spare (Wired to ESE)
7	17	IGNORE	Spare (Wired to ESE)
6	18	OFF	Translunar Injection Inhibit
5	19	ON	S-IVB Engine Out "A"
4	20	OFF	Spare (Wired to Control Distributor)
3	21	OFF	O <sub>2</sub> -H <sub>2</sub> Burner Malfunction
2a	22	OFF	Command Decoder OM/D "A"
2b	22	OFF	Command Decoder OM/D "B"
1	23	IGNORE	RCA-110A SYNC
	24	IGNORE	UNUSED
	25	IGNORE	UNUSED

Table 4.3.3

#### 4.3.4.2 Options

- DIS ANDing and XORing constants.

#### 4.3.4.3 Nominal Input Test

##### 4.3.4.3.1 Input

- Access the LVDC DIS constants from core.

##### 4.3.4.3.2 Expected Output

- See Table 4.3.4.

#### 4.3.4.4 Error Input Test

##### 4.3.4.4.1 Input

- Set DIS on.

##### 4.3.4.4.2 Expected Output

- None.

#### 4.3.5 Entry Time in Prepare to Launch

##### 4.3.5.1 Function

Entry Time in Prepare to Launch (ETPTL) is used to establish an initial real time reading.

##### 4.3.5.2 Options

- None.

# DISCRETE INPUT SPARES REGISTER (DIS) ANDING AND XORING CONSTANTS

PLDIS1 = 000000000 (ANDing constant)<sup>1</sup>      PLDIS2 = 000000000 (XORing constant)<sup>1</sup>

The results of the ANDing and XORing constants must indicate the following status.

DIS No.	LVDC Bit Position	Test Status	Function
DIS 8	5	IGNORE	Spare (not wired)
DIS 7	1	IGNORE	Spare (not wired)
DIS 6	2	IGNORE	Spare (not wired)
DIS 5	3	IGNORE	Spare (not wired)
DIS 4	4	IGNORE	Spare (not wired)
DIS 3	5	IGNORE	Spare (not wired)
DIS 2	6	IGNORE	Coolant Thermal Switch 2
DIS 1	7	IGNORE	Coolant Thermal Switch 1
	8	IGNORE	UNUSED
	•	•	•
	•	•	•
	17	IGNORE	UNUSED
X	18	IGNORE	Ladder Channel A selected
X	19	IGNORE	Ladder Channel B selected
	20	IGNORE	UNUSED
	•	•	•
	•	•	•
	25	IGNORE	UNUSED

Table 4.3.4

<sup>1</sup>See Note, p. 4-7

#### 4.3.5.3 Nominal Input Test

##### 4.3.5.3.1 Input

- Load ETPTL within one minute from entry into Prepare to Launch.

##### 4.3.5.3.2 Output

- None.

#### 4.3.5.4 Error Input Test

##### 4.3.5.4.1 Input

- Inhibit load of ETPTL.

##### 4.3.5.4.2 Output

- Error Message Number 125 - ETPTL (GMT) not loaded within 60 seconds of entry to Prepare to Launch. D013 = Set.

#### 4.3.6 Guidance Reference Release Alert (GRR)

##### 4.3.6.1 Function

The Guidance Reference Release Alert test is required to alert the LVDC preflight program of the issuance of GRR.

##### 4.3.6.2 Options

- Entry time to Prepare to Launch (ETPTL).
- Predicted time of lift off (PLOT).
- Platform aligned indicator (ISR bit 3).

#### 4.3.6.3 Nominal Input Test

##### 4.3.6.3.1 Input

- Enter PTL.
- Set DIN 16 = ON, 60 seconds after entering PTL.
- Load nominal PLOT and ETPTL.
- Set ISR bit 3 = ON.

##### 4.3.6.3.2 Expected Output

- None.

#### 4.3.6.4 Error Input Tests

##### 4.3.6.4.1 Input

- Enter PTL.
- Inhibit load of ETPTL.
- Load nominal PLOT.
- Set DIN 16 = ON, 30 seconds after entering PTL.

##### 4.3.6.4.2 Expected Output

- Error Message Number 1252 - GRRA discrete was set before ETPTL was loaded. DO13 = Set.

##### 4.3.6.4.3 Input

- Enter PTL.
- Load nominal ETPTL.
- Inhibit load of PLOT.
- Set DIN 16 = ON, 30 seconds after entering PTL.

#### 4.3.6.4.4 Expected Output

- Error Message Number 1253 - GRRRA discrete was set before PLOT was loaded. DO13 = Set.

#### 4.3.6.4.5 Input

- Enter PTL.
- Load nominal ETPTL.
- Load nominal PLOT.
- Inhibit platform aligned indicator (ISR3).
- Set DIN 16 = ON, 60 seconds after entering PTL.

#### 4.3.6.4.6 Expected Output

- Error Message Number 124 - GRRRA discrete was set before RCA-110A indicated to LVDC that platform had been aligned to correct azimuth. DO13 = Set.

#### 4.3.7 PLOT: Old PLOT

##### 4.3.7.1 Function

Predicted lift-off time (PLOT) is used in calculating a new mission azimuth. The old PLOT (PLOT1) is used as a means of determining when a new PLOT is loaded. PLOT must be loaded before one minute elapses in PTL.

##### 4.3.7.2 Options

- None.

#### 4.3.7.3 Nominal Input Test

##### 4.3.7.3.1 Input

- Load PLOT within one minute of entry to Prepare to Launch.

##### 4.3.7.3.2 Output

- None.

#### 4.3.7.4 Error Input Test

##### 4.3.7.4.1 Input

- Load a new PLOT that will cause a difference greater than 30 seconds.
- Load a new PLOT less than the old PLOT.
- Inhibit load of PLOT.

##### 4.3.7.4.2 Output

- No error message expected per PCR #C082.
- No error message expected per PCR #C082.
- Error Message Number 1251 - PLOT not loaded within 60 seconds of entry to Prepare to Launch. D013 = Set.

#### 4.3.8 Target Vector Rate

##### 4.3.8.1 Function

The LVDC location which contains the target vector rate (TVRATE) designates either a fixed or a variable azimuth launch. If TVRATE is non-zero, a variable azimuth launch is indicated. If TVRATE is zero, a fixed azimuth launch is

indicated. PLOT window tests are not performed in a fixed azimuth launch since the window is nonexistent. The fixed azimuth is equal to the value of H10.<sup>1</sup>

#### 4.3.8.2 Options

- None.

#### 4.3.8.3 Nominal Input Test

##### 4.3.8.3.1 Input

- Load TVRATE = 0, PLOT = LWOP + TDS1.
- Load TVRATE = 0, PLOT less than LWOP.

NOTE: Variable azimuth tests are performed in the PLOT Window Test, section 4.3.9.

##### 4.3.8.3.2 Output

- Azimuth = H10.<sup>1</sup> (No error telemetry).

#### 4.3.9 PLOT Window Test

##### 4.3.9.1 Function

The launch window is a time interval in which launch may occur in a variable azimuth mission. The PLOT loaded by the RCA-110A must fall within this time interval.

##### 4.3.9.2 Options

- TVRATE = Variable Azimuth.

<sup>1</sup> REF. 1, TABLE 15-2.

#### 4.3.9.3 Nominal Input Test

##### 4.3.9.3.1 Input

- Load PLOT = LWOP + 17 seconds + TDS(I) (where I = 0,1,2,3).

##### 4.3.9.3.2 Expected Output

- Azimuth + complement.

#### 4.3.9.4 Error Input Test

##### 4.3.9.4.1 Input

- Load PLOT = LWOP + 16 seconds.
- Load PLOT = LWOP + 17 seconds + TDS3 + 1 second.

##### 4.3.9.4.2 Expected Output

- Error Message Number 1262 - PLOT value loaded indicates lift-off is to occur before launch window opens. D013 = Set.
- Error Message Number 1263 - PLOT value loaded indicates lift-off is to occur after launch window closes. D013 = Set.

#### 4.3.10 Calculate Azimuth

##### 4.3.10.1 Function

Azimuth is calculated in the flight program by using the latest PLOT supplied by the Prepare to Launch routine and expanding it in a fifth order polynomial.

##### 4.3.10.2 Options

- None.

#### 4.3.10.3 Nominal Input Test

##### 4.3.10.3 Input

- Supply a PLOT equal to the launch window open time + 17 seconds.

This should give an azimuth equal to the value of H10.

##### 4.3.10.3.2 Output

- Azimuth telemetry and complement.

#### 4.3.10.4 Error Input Test

##### 4.3.10.4.1 Input

- Load H10 =  $79^\circ$  and PLOT equal launch window open time + 17 seconds.
- Load H10 =  $101^\circ$  and PLOT equal launch window open time + 17 seconds.

##### 4.3.10.4.2 Output

- Error Message Number 1256 - Calculated azimuth less than  $79.5^\circ$  range safety limit. D013 = Set.
- Error Message Number 1257 - Calculated azimuth greater than  $100.5^\circ$  range safety limit. D013 = Set.

#### 4.3.11 Platform Aligned

##### 4.3.11.1 Function

The alignment of the platform will confirm that the accelerometer and gimbal angle readings are valid for the calculated azimuth.

#### 4.3.11.2 Options

- None.

#### 4.3.11.3 Nominal Input Test

##### 4.3.11.3.1 Input

- $PLOT = LWOP + 17 \text{ seconds.}$
- $ETPTL = PLOT - 200 \text{ seconds.}$
- Set Interrupt 3.

##### 4.3.11.3.2 Expected Output

- None.

#### 4.3.11.4 Error Input Test

##### 4.3.11.4.1 Input

- $PLOT = LWOP + 17 \text{ seconds.}$
- $ETPTL = PLOT - 200 \text{ seconds.}$
- Inhibit platform aligned indicator (ISR 3).

##### 4.3.11.4.2 Expected Output

- Error Message Number 124 - Platform was not aligned at 2 minutes and 32 seconds before liftoff. DO13 = Set.

#### 4.3.12 Gimbal Angle Monitor - Gimbal Angle Reasonableness Test

##### 4.3.12.1 Function

Each time a new azimuth is calculated in the Prepare to Launch routine new gimbal angle reasonableness constants are calculated. These are the ideal gimbal angles which correspond to the computed azimuth. The Gimbal Angle Monitor routine then reads the actual gimbal angles. These readings are examined by the PTL routine to insure that the fine readings are within  $1^\circ$  of the ideal and that the back-up readings are within  $2.5^\circ$  of the expected.

##### 4.3.12.2 Options

- None.

##### 4.3.12.3 Nominal Input Test

###### 4.3.12.3.1 Input

- The simulated fine gimbal will be biased by  $1.00167^\circ$  and the simulated back-up gimbal will be biased by  $2.5^\circ$ .

###### 4.3.12.3.2 Output

- None.

##### 4.3.12.4 Error Input Test

###### 4.3.12.4.1 Input

- The simulated fine gimbal will be biased on all three axes by  $1.00167^\circ$  plus 1 bit, and the simulated back-up gimbal will be biased on all three axes by  $2.5^\circ$  plus 1 bit.

#### 4.3.12.4.2 Output

##### Fine Gimbal Errors

Error Message 12000	COD	FINE 1	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12004	COD	FINE 1	SYL 1	FAILED THE REASONABLENESS TEST
Error Message 12010	COD	FINE 2	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12014	COD	FINE 2	SYL 1	FAILED THE REASONABLENESS TEST
Error Message 12020	COD	FINE 3	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12024	COD	FINE 3	SYL 1	FAILED THE REASONABLENESS TEST

##### Backup Gimbal Errors

Error Message 12030	BACKUP 1	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12034	BACKUP 1	SYL 1	FAILED THE REASONABLENESS TEST
Error Message 12040	BACKUP 2	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12044	BACKUP 2	SYL 1	FAILED THE REASONABLENESS TEST
Error Message 12050	BACKUP 3	SYL 0	FAILED THE REASONABLENESS TEST
Error Message 12054	BACKUP 3	SYL 1	FAILED THE REASONABLENESS TEST

D013 is set with each error message.

#### 4.3.13 Telemetry Cycle

##### 4.3.13.1 Description

The telemetry from the Prepare to Launch routine provides information for real time and post-flight analysis. This telemetry does not interrupt the SLCC, and D013 is not set. The information is included here for completeness.

#### 4.3.13.2 Telemetry from PTL

##### 4.3.13.2.1 Data Telemetered at Least One Per Pass

<u>LVDC Computer Telemetry Tag</u>	<u>Data Description</u>
401 <sub>8</sub>	Fine 1 Gimbal Reading
405	Fine 2 Gimbal Reading
411	Fine 3 Gimbal Reading
175	Backup 1 Gimbal Reading
171	Backup 3 Gimbal Reading
635	Backup 2 Gimbal Reading

##### 4.3.13.2.2 Data Telemetered Every Other Pass (before the gimbal readings).

<u>LVDC Computer Telemetry Tag</u>	<u>Data Description</u>
174 <sub>8</sub>	Real Time Clock
061      25252525252 <sub>8</sub>	Pattern Word
or 714      52525252524	
501	Down Range Accelerometer
505	Vertical Accelerometer
511	Cross Range Accelerometer

##### 4.3.13.3.3 Telemetry Occurring When Platform Aligned (before GRRA).

<u>LVDC Computer Telemetry Tag</u>	<u>Data Description</u>
675 <sub>8</sub>	AMP3 Off-Level Word

#### 4.3.14 Accelerometer Monitor Subroutine (AMP3)

##### 4.3.14.1 Function

The AMP3 subroutine monitors the duplex accelerometers. A single word telemetry contains the platform off-level indications calculated by comparing received acceleration to that predicted for a level platform on PAD 39A.

#### 4.3.14.2 Options

- None.

#### 4.3.14.3 Error Input Tests

##### 4.3.14.3.1 Input

The accuracy of the AMP3 calculations is verified for each axis over a range of predicted values. (see Table 4.3.14.)

##### 4.3.14.4 Expected Output

- See Table 4.3.14.

#### 4.3.15 Error Monitor Subroutine

##### 4.3.15.1 Function

The function of this subroutine is to test the bit status of the LVDA Error Monitor Register (EMR).

##### 4.3.15.2 Options

- PLEMR1 is the EMR ANDing mask for PTL. This mask contains the bits for SCB, EAM, EBM, and TDI.

##### 4.3.15.3 Nominal Input Test

###### 4.3.15.3.1 Input

- Access the EMR ANDing mask for PTL from core.

###### 4.3.15.3.2 Output

- PLEMR1 = 300001040<sub>8</sub>.

AMP3 SUBROUTINE  
PERTURBATIONS

Data supplied for firing azimuth = 80 degrees.

<u>VERTICAL (X) AXIS</u>	
<u>Scale Factor/Bias</u>	<u>% Off-Level</u>
<u>Input</u>	<u>Output</u>
SF +0.00005	+0.005
B +0.001	+0.010
SF +0.0004	*372* Vertical Axis Exceeds Scale
SF -0.00005	-0.005
B -0.001	-0.010
SF -0.0004	*372* Vertical Axis Exceeds Scale
SF -1.0000	*374* Vertical Axis Failure

<u>CROSS-RANGE (Y) AXIS</u>	
<u>Scale Factor/Bias</u>	<u>deg. Off-Level</u>
<u>Input</u>	<u>Output</u>
SF +0.5000	+0.0078
B +0.0020	+0.0107
SF +5.000	+0.0878
B +0.0420	*376* C-Range Axis Exceeds Scale
SF -0.5000	-0.00879
SF -5.0000	-0.08789
B -0.0420	*376* C-Range Axis Exceeds Scale

<u>DOWN-RANGE (Z) AXIS</u>	
<u>Scale Factor/Bias</u>	<u>deg. Off-Level</u>
<u>Input</u>	<u>Output</u>
SF +1.0000	-0.0059
B -0.0026	-0.0176
SF +5.0000	-0.0176
B -0.0420	*376* D-Range Axis Exceeds Scale
B +0.0026	+0.01172
SF -5.0000	+0.01172
B +0.0318	+0.1885
B +0.0500	*376* D-Range Axis Exceeds Scale

NOTE: Output in the form \*XXX\* represents special error telemetry codes, defined for the magnitude bits in the AMP telemetry word.

Table 4.3.14

#### 4.3.15.3.3 Input

- Reset the SCA bit in the discrete input spares register (DISR).
- Set the SCB bit in the DISR.
- Set the SCB bit in the Error Monitor Register (EMR).

#### 4.3.15.3.4 Output

- None.

#### 4.3.15.4 Error Input Test

##### 4.3.15.4.1 Input

- Set the EAM bit in the EMR.
- Set the EBM bit in the EMR.

##### 4.3.15.4.2 Output

- Error Message Number 000 - A valid failure has been detected by the EMR check in the Error Monitor Subroutine. There is no error message telemetry. However, SLCC will see all zeros as error message and the telemetered contents of the EMR.

##### 4.3.15.4.3 Input

- Reset the SCA bit and set the SCB bit in the DISR.
- Reset the SCA bit in the DISR and set the SCB bit in the EMR.
- Reset the SCA bit and set the SCB bit in the DISR and set the SCB bit in the EMR.
- Set the SCB in the DISR and in the EMR.

#### 4.3.15.4.4 Output

- Error Message Number 127 - The state of the SCA and SCB bits in the Discrete Input Spares Register and the SCB bit in the EMR indicate a switch to converter B.

#### 4.3.16 LVDC Self-Test Subroutine

##### 4.3.16.1 Function

This subroutine performs internal verification of LVDC control and arithmetic logic.

##### 4.3.16.2 Options

- None.

##### 4.3.16.3 Error Input Test

###### 4.3.16.3.1 Input

- Load STZERO = + (Set assembled 0 constant equal to non-zero.)

###### 4.3.16.3.2 Expected Output

- Error Message Number 2 - An LVDC Self-Test error has occurred. Verify the three word LVDC Self-Test error table to determine the nature and location of the failure. D013 = Set

#### 4.3.17 PTL Real Time Update Subroutine

##### 4.3.17.1 Function

This subroutine accumulates real time from entry to Prepare to Launch.

#### 4.3.17.2 Options

- None.

#### 4.3.17.3 Nominal Input

##### 4.3.17.3.1 Input

- None.

##### 4.3.17.3.2 Expected Output

- None.

#### 4.3.17.4 Comments

The function of this subroutine is verified in these time tests:

- One minute elapsed in PTL.
- Platform aligned at 2 minutes 32 seconds.
- Accumulate GMT, supplied to flight program.

#### 4.3.18 LVDA Timing and Counter Subroutine

##### 4.3.18.1 Function

This subroutine verifies the operations of the LVDA timers, cross-over detectors, and duplex accelerometers.

##### 4.3.18.2 Options

- None.

#### 4.3.18.3 Error Input

##### 4.3.18.3.1 Input

- Stop B channel vertical accelerometer from incrementing.

##### 4.3.18.3.2 Output

- Error Message Number 1116 - Vertical accelerometer duplex counts differed by more than plus or minus two counts when compared with readings taken on last iteration. D013 = Set.

#### 4.3.19 PTL LVDA Initialize Subroutine

##### 4.3.19.1 Function

The function of this routine is to inhibit all interrupts except GRR and TLC, to set and reset specified ICR and DOR bits, and to clamp all ladders to zero.

##### 4.3.19.2 Options

- ICR set constant.
- ICR reset constant.
- DOR set constant.
- DOR reset constant.

##### 4.3.19.3 Nominal Input Test

###### 4.3.19.3.1 Input

- Obtain the Interrupt Inhibit register contents in PTL.
- Obtain LVDC ICR and DOR set and reset constants from core.

###### 4.3.19.3.2 Expected Output

- See Tables 4.3.19A-C

# INTERRUPT INHIBIT REGISTER

The Inhibit Register must indicate the following status.

Interrupt Bit	Inhibit Status	Function
12	YES	Timer 1 (Minor Loop)
11	YES	Timer 2 (Switch Selector)
10	YES	CIU
9	NO	Temporary Loss of Control (TLC)
8	YES	Command Decoder Interrupt "A" and "B"
7	NO	Guidance Reference Release
6	YES	S-II Engines Cutoff
5	YES	S-IC Outboard Engines Cutoff "A"
4	YES	S-IVB Engine Out "B"
3	YES	RCA-110A Interrupt
2	YES	S/C Initiation of S-II/S-IVB Separation "A" and S/C Initiation of S-IVB Cutoff "A"
1	YES	RCA-110A Interrupt

Table 4.3.19A

# INTERNAL CONTROL REGISTER (ICR) SET AND RESET CONSTANTS

PLICRS = 000010002<sub>8</sub> (Specifies ICR bits to be set)

PLICRR = 000027774<sub>8</sub> (Specifies ICR bits to be reset)

The set and reset constants must indicate the following status.

ICR Bit	LVDC Bit Position	Status		Function
		Reset	Set	
	S	NO	NO	UNUSED
	•	•	•	•
	•	•	•	•
	11	NO	NO	UNUSED
14	12	NO	NO	Reselect ladder converter A
13	13	YES	NO	Not assigned
12	14	NO	YES	Switch Selector Channel
11	15	YES	NO	Forces SCB, COD test errors
10	16	YES	NO	COD A-B
9	17	YES	NO	ICR bit
8	18	YES	NO	Inhibit disagreement bit
7	19	YES	NO	Not assigned
6	20	YES	NO	Not assigned
5	21	YES	NO	Not assigned
4	22	YES	NO	Gimbal 1
3	23	YES	NO	Not assigned
2	24	YES	NO	Hold converter A
1	25	NO	YES	T SYNC, G SYNC

Table 4.3.19B

# DISCRETE OUTPUT REGISTER (DOR) SET AND RESET CONSTANTS

PLDORR = 777740000 (Specifies DOR bits to be reset)

PLDORS = 000000000 (Specifies DOR bits to be set)

The set and reset constants must indicate the following status.

DOR Bit	LVDC Bit Position	Status		Function
		Reset	Set	
13	5	YES	NO	Firing Commit Inhibit
12	1	YES	NO	Firing Enable Signal
11	2	YES	NO	Control Distributor (Not Used)
10	3	YES	NO	Control Distributor (Not Used)
9	4	YES	NO	Control Distributor (Not Used)
8	5	YES	NO	Control Distributor (Not Used)
7	6	YES	NO	Control Distributor (Not Used)
6	7	YES	NO	IU Guidance Reference Failure
5	8	YES	NO	Control Distributor (Not Used)
4	9	YES	NO	IU Guidance Reference Failure
3	10	YES	NO	Control Distributor (Not Used)
2	11	YES	NO	RCA-110A Line 7 Interrupt
1	12	YES	NO	SYNC Reset
	13	NO	NO	
	•	•	•	
	•	•	•	
	•	•	•	
	25	NO	NO	

Table 4.3.19C

#### 4.3.19.3.3 Input

- Modify DOR and ICR set constants so that D06, D07, and ICR1, ICR7 and ICR12 are set.
- Modify DOR and ICR reset constants so that only D07 and ICR7 are reset.

#### 4.3.19.3.4 Expected Output

- D06, ICR1, and ICR12 set.

### 4.3.20 Verify and Prepare to Load and Load Routine

#### 4.3.20.1 Function

These routines allow the launch computer to verify any LYDC memory location and to load variable azimuth data (locations 0,16,360-377).

#### 4.3.20.2 Options

- Command Verify and Prepare to Load.
- Command Load.

#### 4.3.20.3 Nominal Input Test

##### 4.3.20.3.1 Input

- Load ETPTL and PLOT.

##### 4.3.20.3.2 Expected Output

- Communication with the commanded routine is verified by the simulator.

#### 4.3.20.4 Error Input Test

##### 4.3.20.4.1 Input

- Load location 0,16,357 with any value.

##### 4.3.20.4.2 Expected Output

- Error Message Number 2312 - Load routine was called from PTL to load location(s) other than 0,16,360-377. No load will be executed.  
DO13 = Set.

#### 4.3.21 Interrupt Processor

##### 4.3.21.1 Function

The function of this routine is to determine which interrupt occurred and to process the interrupts according to the prescribed priority. A TLC interrupt has highest priority, and a GRR interrupt has second highest. In PTL all other interrupts are inhibited.

##### 4.3.21.2 Options

- None.

##### 4.3.21.3 Nominal Input Test

###### 4.3.21.3.1 Input

- Set the ISR to force several interrupts including GRR and excluding TLC.
- Issue "GRR Immediately" from PTL.

###### 4.3.21.3.2 Expected Output

- Exit to flight program

#### 4.3.21.4 Error Input Test

##### 4.3.21.4.1 Input

- Set the ISR to force all interrupts.

##### 4.3.21.4.2 Expected Output

- Error Message Number 332 - A TLC interrupt has occurred. The HOP save value is telemetered. D013 = Set.

## APPENDIX A

### REFERENCES

1. LVDC Equation Defining Document for the Saturn V Flight Programs  
Revision H, MSFC III-4-423-15, IBM No. 69-207-0001.
2. LVDC Preflight Program Descriptions, MSFC No. DRL-008A, IBM No.  
67-F11-0011.
3. Astrionics System Handbook - Saturn Launch Vehicles, MSFC No.  
IV-4-401-1, IBM No. 68-966-0002.
4. Programmers Operating Manual - Saturn Launch Vehicle Digital  
Computer, Launch Vehicle Data Adapter and Programmable Test  
Controller, Contracts NAS8-11561 and NAS8-11562.
5. Program Verification Plan for Saturn Launch Vehicle Prepare-to-Launch  
Programs, IBM No. 71W-00143.

# APPENDIX B

The following table lists the error message telemetry for the preflight routines. For each routine the error name, the error message number in octal, and the sequence that the error occurs within the routine is outlined. The model 44, unlike the LVDC, also possesses a description of each error message number. The decimal number is assigned in the model 44 to each error message description

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
1. LVDA TIMING & COUNTER	1	DAEM1	111000000	51
		DAEM2	112000000	59
		DAEM4	114000000	70
		DAEM7	117000000	34
		DAEM9	111200000	53
		DAEM12	111500000	56
		DAEM13	111600000	57
		DAEM14	111700000	58
		DAEM15	112100000	60
		DAEM16	112200000	61
		DAEM33	114500000	63
		DAEM18	112400000	64
		DAEM19	112500000	66
		DAEM21	112700000	68
		DAEM22	113100000	69
	2	DAEM23	113200000	71
		DAEM5	115000000	72
	3	DAEM10	111300000	54

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

(CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
	4	DAEM3	113000000	67
	5	DAEM8	111100000	52
	6	DAEM6	116000000	73
	7	DAEM11	111400000	55
	8	DAEM20	112600000	65
	9	DAEM17	112300000	62
	10	NONE		
2. MINOR LOOP, SW. SEL.				
REAL TIME	1	CTEM1	130000000	11
	2	CTEM2	131000000	12
	3	CTEM3	132000000	13
	4	CTEM4	133000000	14
	5	CTEM5	134000000	15
	6	CTEM6	135000000	16
	7	NONE		
3. MODE SORT ROUTINE				
	1	MSEM0	000000000	21
		MSEM1	001000000	23
	2	MSEM2	001100000	22
	3	NONE		
	4		001200000	95
4. TELEMETRY TEST				
	1	TLEM1	327000000	136
	2	NONE		
5. READ INPUT DATA SUBR				
	1	RIEM1	451000000	138
	2	NONE		

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

(CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
6. CIU READ ROUTINE				
	1	CIUEM1	141000000	103
	2	CIUEM2	142000000	104
	3	NONE		
7. G&C STEERING				
	1	GCEM1	061000000	25
	2	NONE		
8. DOM TEST				
	1	DIEM1	071000000	26
	2	NONE		
9. LADDER ERROR TEST				
	1	LEEM1	101000000	27
	2	LEEM2	102000000	35
		LEEM4	104000000	47
		LEEM5	105000000	48
		LEEM7	107000000	50
		LEEM9	101200000	29
		LEEM11	101400000	31
		LEEM23	103100000	44
		LEEM12	101500000	32
		LEEM14	101700000	34
		LEEM16	102200000	37
		LEEM20	102600000	41
	3	LEEM3	103000000	43
		LEEM8	101100000	38
		LEEM10	101300000	30

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

(CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
		LEEM22	103300000	46
		LEEM13	101600000	33
		LEEM15	102100000	36
		LEEM17	102300000	38
		LEEM21	102700000	42
	4	LEEM4	104000000	47
		LEEM6	106000000	49
	5	LEEM18	102400000	39
	6	LEEM19	102500000	40
	7	LEEM11	101400000	31
		LEEM24	103200000	45
	8	NONE		
10. INTERRUPT PROCESSOR				
	1	INEM1	331000000	1
	2	INEM2	332000000	137
	3	NONE		
11. VERIFY & PRÉPARE TO LOAD				
	1	LVEM1	211000000	122
	2	LVEM2	212000000	123
	3	LVEM3	213000000	124
	4	LVEM4	214000000	125
	5	LVEM5	215000000	126
	6	LVEM6	216000000	127
	7	LVEM7	217000000	0
	8	NONE		
12. EXERCISE ATTITUDE COMMAND				
	1	ECEM1	171000000	118

ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE (CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
	2	ECEM2	172000000	119
	3	ECEM3	173000000	120
	4	ECEM4	174000000	121
	5	NONE		
13. LOAD ROUTINE				
	1	LDEM1	231000000	128
	2	LDEM2	231200000	129
	3	NONE		
14. RESOLVER ERROR				
SUBROUTINE	1	REEM1	441000000	2
	2	NONE		
15. SWITCH SELECTOR TEST				
	1	SSEM1	151000000	105
	2	SSEM2	152000000	112
	3	SSEM3	153000000	113
	4	SSEM4	154000000	114
	5	SSEM5	155000000	115
	6	SSEM7	157000000	116
	7	SSEM11	151400000	109
	8	SSEM7	157100000	117
		PASS2		
	9	SSEM11	151410000	110
		PASS2		
	10	SSEM8	151100000	106
	11	SSEM9	151200000	107
	12	SSEM12	151500000	111

## ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE

(CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
	13	SSEM10	151300000	108
	14	NONE		
16. SELF-TEST SUBROUTINE	1 - 35	STEM1	002000000	24
17. MEMORY ERROR TEST				
	1	MEM1	220000000	3
	2	MEM2	220000010	4
		MEM3	220000020	5
		MEM4	220000030	6
		MEM5	220000040	7
		MEM6	220000050	8
		MEM7	220000060	9
		MEM8	220000070	10
		MEM9	220000100	11
		MEM10	220000110	12
		MEM11	220000120	13
		MEM12	220000130	15
		MEM13	220000140	17
		MEM14	220000150	19
	3	NONE		
18. PREPARE TO LAUNCH				
	1	PLEM1	121000000	87
		PLEM2	122000000	88
		PLEM3	123000000	89
	2	PLEM52	125200000	92
		PLEM53	125300000	93
		PLEM54	125400000	94

ERROR MESSAGE TELEMETRY VS. PREFLIGHT ROUTINE (CONTINUED)

LVDC PREFLIGHT ROUTINE	TEST SEQUENCE	PREFLIGHT ERROR NAME	OCTAL ERROR TELEMETRY	DECIMAL ASSIGNED NUMBER
	3	PLEM5	125000000	90
		PLEM51	125100000	91
	4	PLEM6	126000000	98
	5	PLEM61	126100000	99
	6	PLEM62	126200000	100
	7	PLEM63	126300000	101
	8	PLEM56	125600000	96
	9	PLEM57	125700000	97
	10	PLEM4	124000000	139
	11	PLEM00	120000000	75
		PLEM01	120040000	76
		PLEM02	120100000	77
		PLEM03	120140000	78
		PLEM04	120200000	79
		PLEM05	120240000	80
		PLEM06	120300000	81
		PLEM07	120340000	82
		PLEM08	120400000	83
		PLEM09	120440000	84
		PLEM0A	120500000	85
		PLEM0B	120540000	86
	12	PLEM7	127000000	102

APPENDIX C  
ABBREVIATIONS

AMP3	Accelerometer Monitor Subroutine	INTC	Interface Output Latch
B	Bias	ISR	Interrupt Storage Register
CIU	Computer Interface Unit	LAD	Ladder
COD	Crossover Detector	LVDA	Launch Vehicle Data Adapter
DCS	Digital Command System	LVDC	Launch Vehicle Digital
DDAS	Digital Data Acquisition System		Computer
DIN	Discrete Input	LWOP	Launch Window Opening Time
DIS	Discrete Input Spares	ms.	Milliseconds
D.O.	Discrete Output	OCR	Orbital Check-out Ready
DOM	Data Output Multiplexor	PCM	Pulse Coded Modulation
DOR	Discrete Output Register	PCR	Program Change Request
DST	Discrete Control Bit of the LVDA Timing Function	PIO	Process Input Output
EAM	Memory A Error	PLOT	Predicted Liftoff Time
EBM	Memory B Error	PTL	Prepare to Launch
EMR	Error Monitor Register	PTR	Program Trouble Report
ESE	Electrical Support Equipment	REG	Register
ETPTL	Entry Time to Prepare to Launch	SCA	Switch to Converter A
FCDD	Flight Computer Data Device	SCB	Switch to Converter B
FG	Fine Gimbal	SF	Scale Factor
G.A.	Gimbal Angle	SIMIND	Simulated Flight Indicator
G&C	Guidance and Control	SLCC	Saturn Launch Computer Complex
GMT	Greenwich Mean Time	S.S.	Switch Selector
GRR	Guidance Reference Release	SSFB	Switch Selector Feedback
GRRA	Guidance Reference Release Alert	TDI	Transient & Low Voltage Detector
ICR	Internal Control Register		
INT	Interrupt		

## ABBREVIATIONS

TDS(I) Partition Times for Azimuth

Polynomials

TLC Simultaneous Memory Error

TVRATE Target Vector Rate



Space Systems Center  
Huntsville, Alabama

Printed in USA



Apollo/Saturn Team