

AC SPARK PLUG DIVISION
 General Motors Corporation
 Milwaukee, Wisconsin

XDE 34-S-504 A

**ENGINEERING
 DESIGN INFORMATION
 EXHIBIT**

PRELIMINARY AGC INTERFACE SPECIFICATION

By T. W. DeSwarte
 J. E. Kernan Date 1/31/63

I. PURPOSE

This document is intended to be a basis for developing the complete functional, timing and electrical specification for the AGC interface with Apollo equipments or subsystems with which ACSP is, or may be, concerned. Since this is the first comprehensive attempt at internal documentation of this particular interface, the interface described is necessarily quite incomplete; hence, an important result of issuing this document will be the answering of the many specific questions herein contained. Many revisions of this XDE will be forthcoming based on information to be supplied by personnel working with the various design groups. It is, therefore, requested that corrections and additions to this document be communicated to any of the following personnel associated with the Digital Techniques Group:

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III. List of Abbreviations

ACSP	AC Spark Plug
AGANI	Apollo Guidance and Navigation Information
AGC	Apollo Guidance Computer
AGE	Apollo Guidance Equipment
A/P	Autopilot
CDU	Coupling Display Unit
D/A	Digital to Analog Converter
D & C	Displays and Controls
DSKY	Display and Keyboard of AGC
G & N	Guidance and Navigation
GMT	Greenwich Mean Time
GSE	Ground Support Equipment
IMU	Inertial Measurement Unit
IN	INput Register
IRIG	Inertial Reference Integrating Gyro
IUA	Inertial Unit Assembly
LEM	Lunar Excursion Module
MCT	Memory Cycle Time
MIT	Massachusetts Institute of Technology
mr/sec	Milliradians per second
OUT	OUTput Register

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III. List of Abbreviations Cont'd.

PCM	Pulse Code Modulation
PIPA	Pulsed Integrating Pendulous Accelerometer
pps	Pulses per second
PSA	Power and Servo Assembly
SA	Shaft Axis
S/C	Spacecraft
SCT	Scanning Telescope
SPACE	Spacecraft Prelaunch Automatic Checkout Equipment
SXT	Sextant
TA	Trunnion Axis
T/M	Telemetry

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IV. INTRODUCTION

It is the purpose of this section to briefly describe the method of presenting the interface material in this document.

In addition to the general AGC interface considerations presented in Section VI, Sections VII through XI present as much detail as is presently internally known concerning the AGC interface with five particular areas.

Each of these five particular interfaces is introduced by a simple data flow block diagram which merely identifies the interface. This is followed by one or more detailed interface charts, each a 3-4 page foldout, which summarizes in considerable detail yet in convenient form and minimum space, the particular interface area being considered. When interface changes or corrections are made, it is intended that these charts will be the handiest medium of updating the interface.

A textual explanation of the details of the interface follows the interface chart. This detailed explanation is not intended to merely elaborate upon what has already been more simply and briefly described by the chart, but rather to explain fine points and special interface considerations which do not lend themselves to presentation in chart form. The explanation is followed by a listing of interface questions which must be answered in order to complete the chart or to enable a better understanding of the interface requirements.

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V. INTERPRETATION OF INTERFACE CHARTS

The interface charts presented in this document represent the best internal ACSP knowledge at this time concerning the particular AGC interface areas. It is intended that documentation of the increasingly better defined interface will be largely implemented by timely review of these charts by appropriate ACSP, MIT and Raytheon personnel.

Areas of missing or incomplete knowledge may rapidly be ascertained by noting the many blank spaces on the charts. If enough charts are placed in the hands of enough knowledgeable people, it should be a simple matter for these people to take red pencil in hand and make corrections right on the charts themselves. Co-ordination of these corrections will be accomplished by the Digital Techniques Group.

However, in order to efficiently update the charts, it is necessary to have a pretty good understanding of what was intended to be included under the various chart headings. In some cases, the headings are self-explanatory in themselves; in other cases, further explanation is necessary to what is intended. The main purpose of this section is to present this explanation, which will be implemented by a discussion of the readings and information on the first interface chart in this document (refer to Chart 1, AGC Interface with CDU, Page VII-3).

Signal Designation (Name and Abbreviation)

This column lists by name all the signals of which the particular interface consists. It is hoped that the terminology employed in designating the signals will be standardized between MIT, Raytheon and ACSP. Where standard abbreviations have been accepted, these should also be listed.

Input (I) or Output (O)

By using capital letters I or O this column shows whether the signal is an input to or an output from the AGC.

Origin or Destination

This column briefly describes the origin or source of AGC inputs or the destination of AGC outputs.

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Initiated How, When and How Often

This column is the first which contains significant information. It and the next six columns to the right contain information which should be available in order to thoroughly understand the system implications of the AGC interface. (The succeeding 14 columns, starting with "Physical Form", contain information of more interest to those responsible for implementing the physical interface between the AGC and the rest of the system).

Information to be included in this column might consist of:

1. What action in the AGC initiates this signal?
 (A certain instruction, the setting of a particular control flip-flop, etc.).
2. Which bits in which AGC registers contain the information to be output or receive the information to be accepted?
3. When (at what time) is this signal initiated?
 (After a sequence of prior events or the fulfillment of certain conditions during a certain loop or program phase, etc.).
4. How often is the signal likely to occur?
 (In terms of time or events).

Available (up) How Long

When the signal is on high or up, how long will it remain in that condition in order that the AGC may accept it as input or that other equipment may receive it as output?

Usage of Input or Response Caused by Output

This column should contain a brief verbal description of the function of the signal. If an input, what action does it cause the AGC to take? If an output, what response will be forthcoming from the receiving equipment?

Effect of Failure to Accept Input or Supply Output at Required Rate

It is quite likely that this column will be the last, in point of time, to be completed. Before the bugs are worked out of any system, it is usual that

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many interface signals--through an unknown sequence of events--are not accepted or issued at the proper time or rate. This type of system interface difficulty will be much easier to pinpoint if the effect of such trouble on the system can first be described. (As an oversimplified example, if CDU loop control is not issued at the required time or rate, the CDU will be in the wrong loop or mode).

Quantity Represented (Accuracy, Resolution, Range)

These three columns contain quantitative information about the abstract mathematical or non-physical corollary of the physical signal in question. For example, a signal which is physically measured in terms of volts might represent milliradians per second.

The accuracy of the quantity represented differs from its resolution or precision. Resolution (precision) is simply how closely the hardware involved is capable of measuring the signal presented to it. The resolution of the quantity represented would be the resolution of the physical quantization times the scale factor necessary to convert from say, pulses per sec to milliradians per sec. The accuracy of the quantity represented is related to system error considerations and is usually not as good as the resolution or precision to which the physical representation of that quantity can be measured. The range of values of the quantity represented is self-explanatory.

Physical Form

This is a very brief description of the physical form of the signal, such as DC voltage level, pulse, continuous square wave, analog, etc. It is important, however, to state the form of the signal as it must appear at the input to the AGC (or immediately after output from the AGC) rather than merely giving the form of the signal as it is sent from or received by the sending or receiving equipment. Only in this manner will interface discrepancies be efficiently covered.

It is simpler to accomplish this for AGC outputs than for AGC inputs. An AGC interface man usually knows pretty definitely the exact physical form of the output signals from the AGC. He should, however, give this form and not the form in which that someone else responsible for some other piece of equipment wants to see. If any discrepancy exists, it can be readily resolved later by mutual discussion, but unless the existence of the discrepancy is made obviously apparent, it may take considerably more time to resolve the problem.

In the case of inputs to the AGC from other equipment, the AGC interface man is much more dependent for information upon the person who specifies the form of the output from that equipment.

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The AGC interface should, however, still be given in terms of the type of signal which the AGC input circuitry expects to see. Any discrepancy which exists can be resolved by a simple comparison of the separate AGC and CDU interface charts.

Physical Quantization (Accuracy, Resolution, Range)

These three columns contain quantitative information about the particular signal as it appears in its true physical form, the form in which it is actually measured by hardware. The units used might typically be volts, pulses per second (pps), etc. If the quantity is sent to or delivered from a binary register, it might be described in bits.

All comments as to differentiation between accuracy, resolution and range are analogous to those made under the heading, "Quantity Represented".

Number of Lines

This column lists the number of lines (data, control, ground, etc.) actually required to implement the interface for each signal. Where each line is the output of a transformer, the two lines are simply called a "pair".

Signal Characteristics

Eight columns (Type Element, Z, Amplitude, I, Pulse Width, Rise Time, Full Time, f) are included under this category of interface data. These are all of interest to the circuit or logical designer who must implement the interface. For each signal these columns should be filled out twice, using the upper line of the chart for the characteristics of the signal at the transmitting end of the line and immediately beneath the corresponding characteristics of the signal at the receiving end of the line.

Type Element

The type of circuit or logic element used to form or accept the signal.

Z

The impedance seen by the load when looking at the source and vice versa.

Amplitude

The voltage level, or voltage swing, etc., necessary at each end of the line to properly actuate the signal-handling element.

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I The current put out by the transmitting device or that necessary to actuate or actually drained by the receiving device.

Rise Time For pulse signals, the time it takes for the signal to rise from 10 percent of its peak amplitude to 90 percent of its "up" peak amplitude.

Fall Time For pulse signals, the time it takes for the signal to drop from 90 to 10 percent of its peak "up" amplitude. (Usually of significance only in those circuits which depend upon the trailing edge of the pulse for their operation).

f Applicable only where the signal has a cycle nature, such as a sinusoidal or a repetitive square wave. The cyclic frequency.

Line Delay

The amount of time it is estimated it will take the signal to traverse the line between the transmitting and receiving elements, or the upper time limit which can be allowed for such traversal (clearly differentiate between these two numbers).

Since this is the first internal attempt at designing an Apollo digital interface chart, it may very well be that some columns may not be too useful and that other significant categories or headings have been inadvertently omitted. Any suggestions as to improvements in the format of these charts or comments regarding their utility will be welcomed by the Digital Techniques Group.

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B. General Characteristics

1. Logical

- | | |
|--|-----------------|
| 1. Word length and format | 16 bits |
| Data: Sign, 14 bits, parity.
One's complement | |
| Instructions: Order Code (3 bits)
Address (12 bits), parity | |
| 2. Parallel transfer of words | |
| 3. Memory Cycle Time (MCT) | 11.72 μ sec |
| 4. Normal Order Codes | 11 instructions |
| 5. Involuntary instructions (Interrupt, Increment, Load, Start) | 8 instructions |
| 6. Add instruction time | 2 MCT |
| 7. Double precision add (subroutine) | 20 MCT |
| 8. Multiply instruction time | 10 MCT |
| 9. Divide instruction time | 18 MCT |
| 10. Counter incrementing time | 1 MCT |
| 11. Aggregate input rate at which instructions are executed at half speed. | 43 K pps |
| 12. Storage | |
| Flip-flop registers | 14 |
| +0 (Inhint and Relint - no hardware for these words) | 2 addresses |
| Erasable core memory | 1008 words |
| Fixed rope core memory | 12,288 words |

2. Electrical

(To be supplied)

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3. Counter Incrementing Feature

Certain erasable registers addressable by program, can act as counters. Upon receipt of an input pulse, the contents of the counter register are read into the arithmetic units' adder, incremented by + 1 (or -1) and placed back into the counter register. These registers are otherwise normal ones and may be written into. In this way, a counter may be set to overflow after any number of pulses.

The overflow or underflow of a counter may be used as an output, as the input to another counter and as the input to the Program Interrupt circuit. No time is spent on the incrementing operation unless there is a non-zero increment.

4. Program Interrupting Feature

Once during each instruction time the interrupt circuit is scanned and if an input has been received, the computer puts away the contents of relevant central register in the arithmetic unit and proceeds to execute some other program. There are eight possible interrupt inputs and each results in a different program being executed. Upon completion of the interrupt program, the original contents of the central registers are restored and the original task resumed exactly where it was interrupted.

An interrupt program may not itself be interrupted. Inputs to the interrupt circuits are not lost; however, should they occur during an interrupt program, they are stored and processed according to some predetermined priority.

The interrupt reaction time is one instruction time; i.e., the interruption occurs at the end of the instruction presently executed.

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4.1 List of Interrupts

Rupt 1 - T3 RUPT

This is a general scheme for generating waits and delays. It is caused by an overflow of counter TIME 3; entry is to the WAITLIST programs. This interrupt can be caused to occur at some specific time by initializing the contents of TIME 3.

Rupt 2 - ERRUPT

Certain error signals from external sources cause automatic entrance to alarm, abort or PIPA scale factor change programs. At present, these signals are defined as: Bad Boost, Abort, AGC Power Fail, IMU Fail, CDU Fail, OPT Fail, TRKR Fail, and ACCEL Fail.

Rupt 3 - DSRUPT

The "End Pulse" from NAA's telemetry programmer and overflows of TIME 4 cause this interrupt. Programs entered are DOWNLINK for loading of OUT 4 and display programs.

Rupt 4 - KEYRUPT

Activity signals from the MARK button, keyboards, or the tape reader cause interrupt which results in entry to the keyboard input programs.

Rupt 5 - UPRUPT

An overflow of the UPLINK counter causes this interrupt. It cause entry to keyboard input programs to process GSE originated information. Also, it is possible that LEM range data for TRACKER programs will be processed via this interrupt.

Rupt 6, 7 and 8 - Spare

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5. Input bit assignments and functions

<u>Register</u>	<u>Bit Assignment</u>	<u>Function</u>
IN 0 (VO)	Bit 1 Key 1	All bit of this register are normally zero.
	2 Key 2	
	3 Key 3	
	4 Key 4	
	5 Key 5	
	6 Key Active (KEYRUPT)	
	7 Spare	
	8 Spare	
	9 Spare	
	10 Spare	
	11 Spare	
	12 Spare	
	13 Spare	
	14 St'by Allowed SW	
	15 MARK (KEYRUPT)	
IN 1 (V1)	Bit 1 1600 pps	Time vernier
	2 800 pps	
	3 400 pps	
	4 200 pps	
	5 OR of C1, 2, 3, 4, 10	IMU Relay Drivers
	6 OR of C5, 6, 7, 8, 9	S/C Alarm Lights
	7 OR of C11, 12	OPT Relay Drivers
	8 Spare	
	9 Spare	
	10 Spare	
	11 Parity	
	12 CROSSPOINT FAIL	AGC Alarms
	13 SR INACTIVE (GO)	
	14 RUPT LOCK (GO)	
	15 TCA TRAP (GO)	

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(Input bit assignments and functions, cont'd)

<u>Register</u>	<u>Bit Assignment</u>	<u>Function</u>
IN 2 (V2)	Bit 1 or CDU <u>ZERO</u>	
	2 or OPT <u>ZERO</u>	
	3 or TRKR <u>ZERO</u>	
	4 Photocell -	
	5 Photocell +	
	6 Spare	
	7 Spare	
	8 TRKR Fail	} ERRUPT
	9 OPT Fail	
	10 CDU Fail	
	11 ACCEL Fail	
	12 IMU Fail	
	13 ABORT	
	14 BAD BOOST	
	15 AGC POWER Fail	
IN 3 (V3)	Bit 1 K1 Zero CDU	
	2 K2 Coarse Align	
	3 K3 Manual CDU	
	4 K4 Fine Align	
	5 ATTSW	
	6 TRNSW	
	7 ZERO OPT	
	8 OPT MODE SW	
	9 OPT MODE SW	
	10 OPT MODE SW	
	11 Spare	
	12 Spare	
	13 S/C MODE SW	
	14 S/C MODE SW	
	15 Lift-off	

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6. Counter Assignments

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<u>ADDRESS</u>	<u>NAME</u>	<u>INPUTS</u>	<u>OUTPUT</u>	<u>OUTPUT GOES TO</u>
0034	OVCTR	+, -		
35	TIME 1	+, 100 pps	OVFLOW	TIME 2
36	TIME 2	+, TIME 1		
37	TIME 3	+, 100 pps	OVFLOW	T3 RUPT
40	TIME 4	+, 100 pps	OVFLOW	DSRUPT
41	UPRUPT	+, Shift	OVFLOW	UPRUPT
42	OUTCR I	+	OVFLOW	Block Rate I
43	OUTCR II	+	OVFLOW	Block Rate II
44	Δ V X PIPA	+, -		
45	Y PIPA	+, -		
46	Z PIPA	+, -		
47	I CDU	+, -	} No sign correction upon overflow or underflow. Overflows not used.	
50	M CDU	+, -		
51	O CDU	+, -		
52	OPT T	+, -		
53	OPT S	+, -		
54	TRKR X	+, -		
55	TRKR Y	+, -		
56	TRKR R	+, Shift		

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6.1 NOTES ON COUNTERS

The Overflow Counter (OVCTR) stores the overflows and underflows resulting from additions. When an overflow occurs, the counter is incremented, for an underflow, it is decremented. Interrupting programs which do ADD's must take care to leave this register in its original state, either by preserving its contents or by guaranteeing no overflows.

The Time 1 and Time 2 counters count time for some arbitrary starting point. Time 2 accumulates the overflows of Time 1; units of which are 10 msec.

Time 3 is used as a general purpose timer, its units are 10 msec. Overflows cause interrupt to the WAITLIST program.

Time 4 has essentially the same function as Time 3 except it is concerned only with the display programs. Units of Time 4 are worth 10 msec.

The UPLINK counter is used as a serial to parallel converter of information coming from the outside world. The counter is shifted and incremented until a word has been accumulated (15 bits). The first bit is always a 1 so the counter will overflow when 16 bits have been sent in. This overflow is used to detect the end of a loading operation. It is possible that UPLINK may be used in the LEM for accepting a serial transmission of range data from a tracking device (radar or laser).

The OUTCR I counts the OR of all the set pulses which go to the CDU's and the IRIG's. An overflow of OUTCR I knocks down all the output latches of RATE I and thus, a prespecified number of pulses can be sent to each device.

OUTCR II counts the OR of all set pulses which go to OPT and THRUST control. An overflow knocks down RATE II.

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7. Output Bit Assignments and Functions

<u>Register</u>	<u>Bit Assignment</u>	<u>Function</u>
OUT 0 (W0)	Bit 1 Rlybit 1	Operates the following 1. Two digital display panels in parallel 2. IMU, CDU, OPT & TRKR switching 3. Alarm lights
	2 Rlybit 2	
	3 Rlybit 3	
	4 Rlybit 4	
	5 Rlybit 5	
	6 Rlybit 6	
	7 Rlybit 7	
	8 Rlybit 8	
	9 Rlybit 9	
	10 Rlybit 10	
	11 Rlybit 11	
	12 Rlybit 12	
	13 Rlywd 1	
	14 Rlywd 2	
	15 Rlywd 3	
OUT 1 (W1)	Bit 1 Rlysys 1	
	2 Rlysys 2	
	3 Rlysys 3	
	4 Spare	
	5 Spare	
	6 Block UPLINK	
	7 Spare	
	8 Slow Speed, STANDBY	
	9 Word Order T/M	
	10 Block End Pulse	
	11 Scale PIPA Fine	
	12 Scale PIPA Emerg.	
	13 Engine Start	
	14 Engine Sequence Start	
	15 Engine Cutoff	
OUT 2 (W2)	Bit 1 OPT T	Rate II
	2 OPT S	
	3 THRUST	
	4 +	
	5 -	
	6 Spare	

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(Output bit assignments and functions, cont'd)

<u>Register</u>	<u>Bit Assignment</u>	<u>Function</u>
	Bit 7 Spare	
	8 X GYRO	} Rate I
	9 Y GYRO	
	10 Z GYRO	
	11 I CDU	
	12 M CDU	
	13 O CDU	
	14 +	
	15 -	
OUT 3 (W3)	15 Spare Bits	
OUT 4 (W4)	16 Bits	Word to be sent via DOWNLINK, including parity.

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PRELIMINARY AGC INTERFACE SPECIFICATION

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8. Input Signal Summary

<u>ORIGIN</u>	<u>N WIRES</u>	<u>DEVICE</u>	<u>COMMENTS</u>
CDU J BOX	6 Pair	Encoders	3 + Δ A Counters
	7	Controls	K ₁ , K ₂ K ₃ K ₄ Relays, ATTSW, TRN SW, Relay Common
PSA	6 Pair	PIPA	3 + Δ V Counters
	1 Pair	PIPA	OR of PIPA FAILURE BITS
	1 Pair	IMU	OR of IMU FAILURE BITS
	1 Pair	Encoder	OR of CDU Not Zeros
	1 Pair	CDU	OR of CDU FAILURE BITS
	5	OPT CONTROLS	Zero Encoder Ind., 3 Mode Select, Mark
	4 Pair	OPT	2 Counters, +
	6 Pair	TRKR	3 Counters, +
	2 Pair	Error Detectors	OR of ZEROS, OPT, TRKR
	2 Pair	Servos	Failure Bits, OPT, TRKR
2 Pair	Photo Detector Controls		
D & C or Test	6	Key or Tape	5 Code, 1 Activity
	3	Controls	3 OR of C Relays
	1	Controls	Standby Allowed SW
LINK	3 Pair	T/M Programmer	START, END and BITSYNC
	2 Pair	Receiver	UPSYNC, DATA TO UPLINK CNTR.
S/C	3 Pair	XFMR	LIFTOFF, ABORT, BAD BOOST
	3	CONTROLS	2 Mode Select, Common
	2	AGC "ON" SW	+28 VDC Prime Power
	2	PWR GND	0 VDC

AGC DSKY'S INTERFACE WITH OTHER SUBSYSTEMS

CDU J BOX	2	PSA	6 v 400 cps Lamp Power 6 v 400 cps Press to Test
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9. Output Signal Summary

<u>DESTINATION</u>	<u>NO. WIRES</u>	<u>DEVICE</u>	<u>COMMENTS</u>
CDU J BOX	7 Pair	D/A Converters	3 + Set Rates, 1.6 KC, Time Modulated. 1 Reset, 1.6 KC 512 KC Master Clock
	1 Pair	Clock	
PSA	3 Pair	PIPA	Set, Reset, Clock 3 + Set, 1.6 KC Time Modulated. 1 Reset, 1.6 KC 0.8 KC, 3.2 KC, 25.6 KC Set, Reset. 12.8 KC
	7 Pair	IRIG	
	7 Pair	Power Supplies	
	5 Pair	OPT or TRKR in LEM	
D & C	2	Thermistor	2 + Set Rates, 1.6 KC Time Modulated 1 Reset, 1.6 KC AGC Temp. Hi & Low
	18	Relay System	
	3	Timing Signals	
	2	AGC Power	
	2	POWER	
	10	Alarm Lights	
LNK	1 Pair	PCM	Output Bits for DOWN T/M
S/C	3 Pair	Engine Controls	Pulse Rates for Engine Sequence Start, Engine Start, Cutoff
	3 Pair	Thrust (LEM)	
			1 + Set Rate, 1.6 KC Time Modulated 1 Reset Rate, 1.6 KC

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PRELIMINARY AGC INTERFACE SPECIFICATION

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(Output Signal Summary, Cont'd.)

AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

<u>DESTINATION</u>	<u>NO. WIRES</u>	<u>DEVICE</u>	<u>COMMENTS</u>
PSA	3 2	Optics Mode Relays "OR" Circuit	C11, C12, GND +13v or +3v Loss Signal GND
Flight PCM	7	Word Assembler in Flight PCM	6 one-bit, non-program controlled failures, GND
CDU J BOX	5 1	Relays in CDU IMU Control Panel	C1-C4, GND Attitude Control Light Command
Map & Data Viewer	6 2	Caution Lights on M & D.V. Panel +13v or +3v Loss Indicator	C5-C9, GND Contact B of P1, GND

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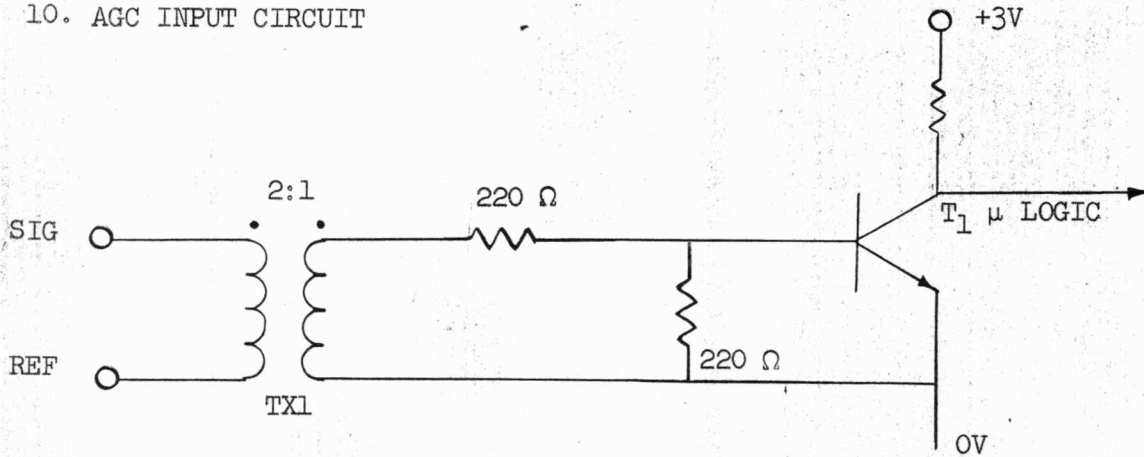
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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Des:

10. AGC INPUT CIRCUIT



INPUT SPECIFICATION

INPUT

SPECIFICATIONS

Amplitude	10 + 4 volts pp with respect to ref.
Impedance	Approx. 1600 ohms at 3 volts in 1400 ohms at 6 volts in 1100 ohms at 14 volts in
Pulse Width	0.5 to 8 μsec measured at 90% amplitude
Duty Cycle	Max. of .3 at 6 volts
Rise and Fall Time	Less than 20% of pulse width, 10-90% of amplitude
Noise	Less than +2 volts pp

Ref. Tx1 - NASA # 1006762

T1 - NASA # 1006771

Figure VI-2

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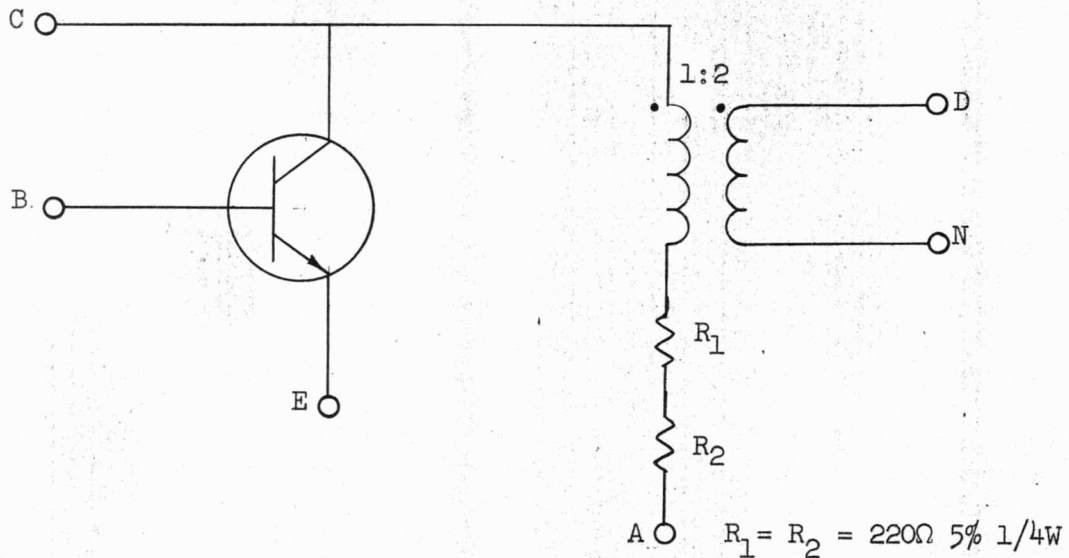
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11. PULSE OUTPUT CIRCUIT



Output Signal Characteristics

Pulse Width: $3 \mu s \pm 0.3 \mu s$
 Rise Time: $\leq 0.2 \mu s$ into 500Ω
 V_{out} , no load: $\geq 20 V$ pp
 V_{out} , 500Ω load: $\geq 5 v$ pp
 Source Impedance: $1.6 K$
 Sync with SBII

Exceptions:

1. Master Clock to S/C: Square wave output.
2. Data to LINK: Pulse width determined by width of BITSYNC pulse.

Figure VI-3

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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

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VII. A. AGC INTERFACE WITH CDU JUNCTION BOX

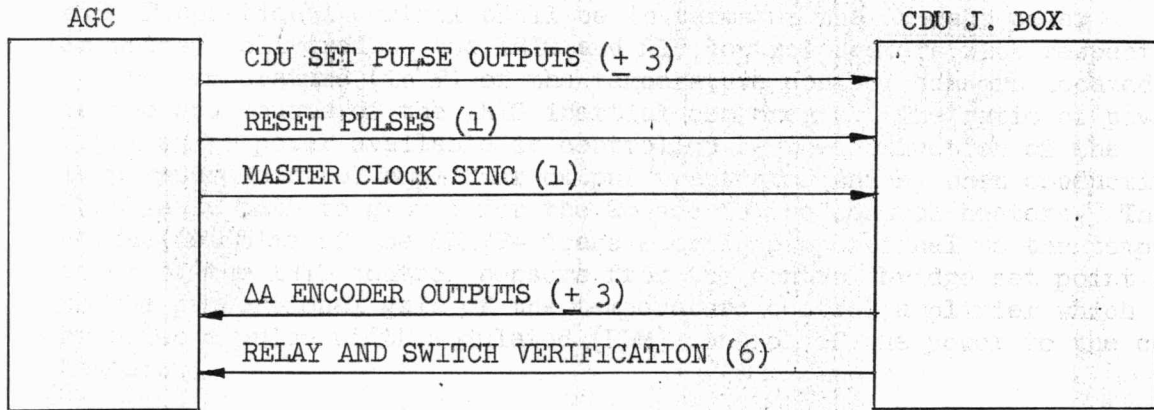


Figure VII-1
 PRELIMINARY AGC-CDU J. BOX INTERFACE BLOCK DIAGRAM

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AGC-CDU J. BOX INTERFACE SCHEMATIC INPUTS

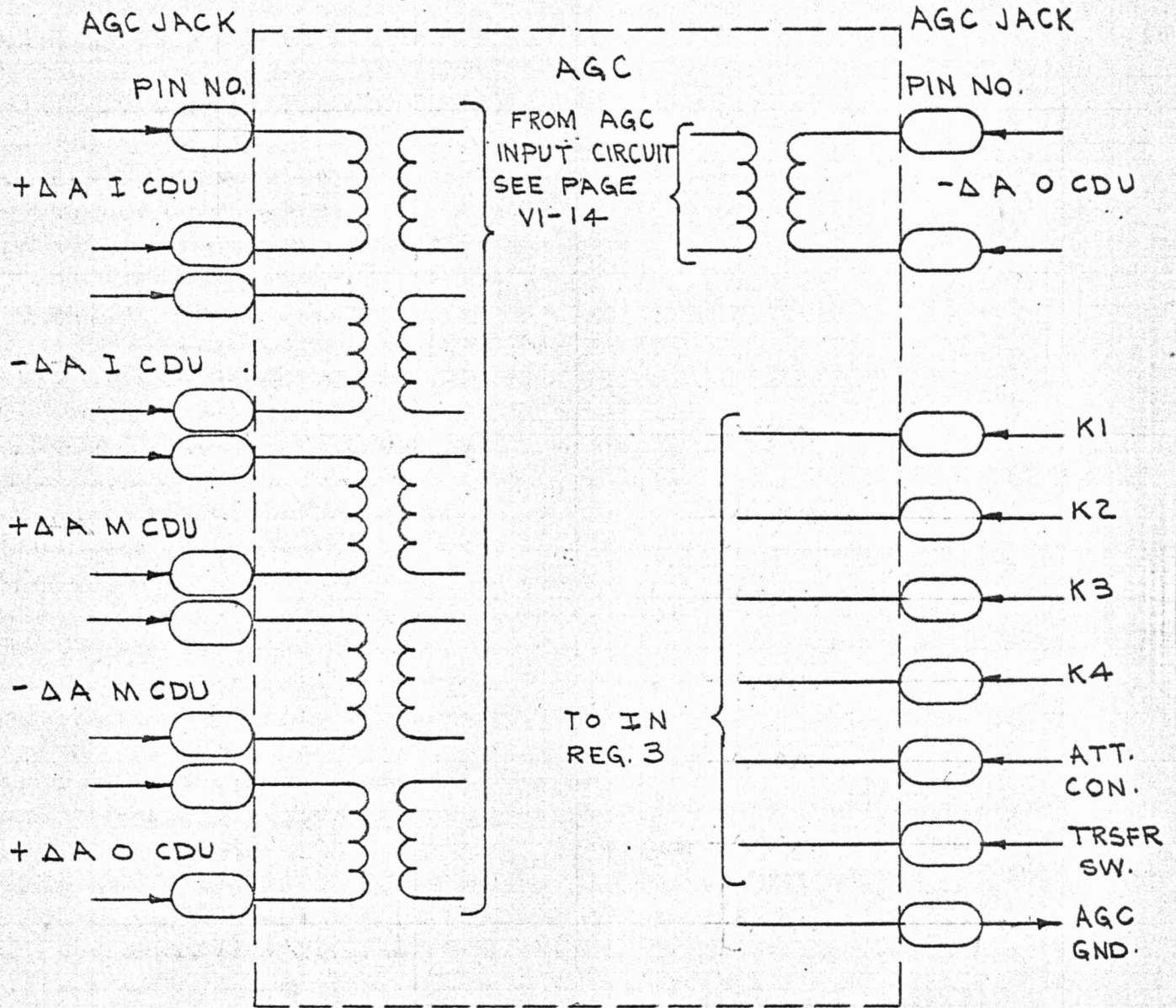


FIGURE VII-2

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AGC - CDU J. BOX INTERFACE SCHEMATIC OUTPUTS

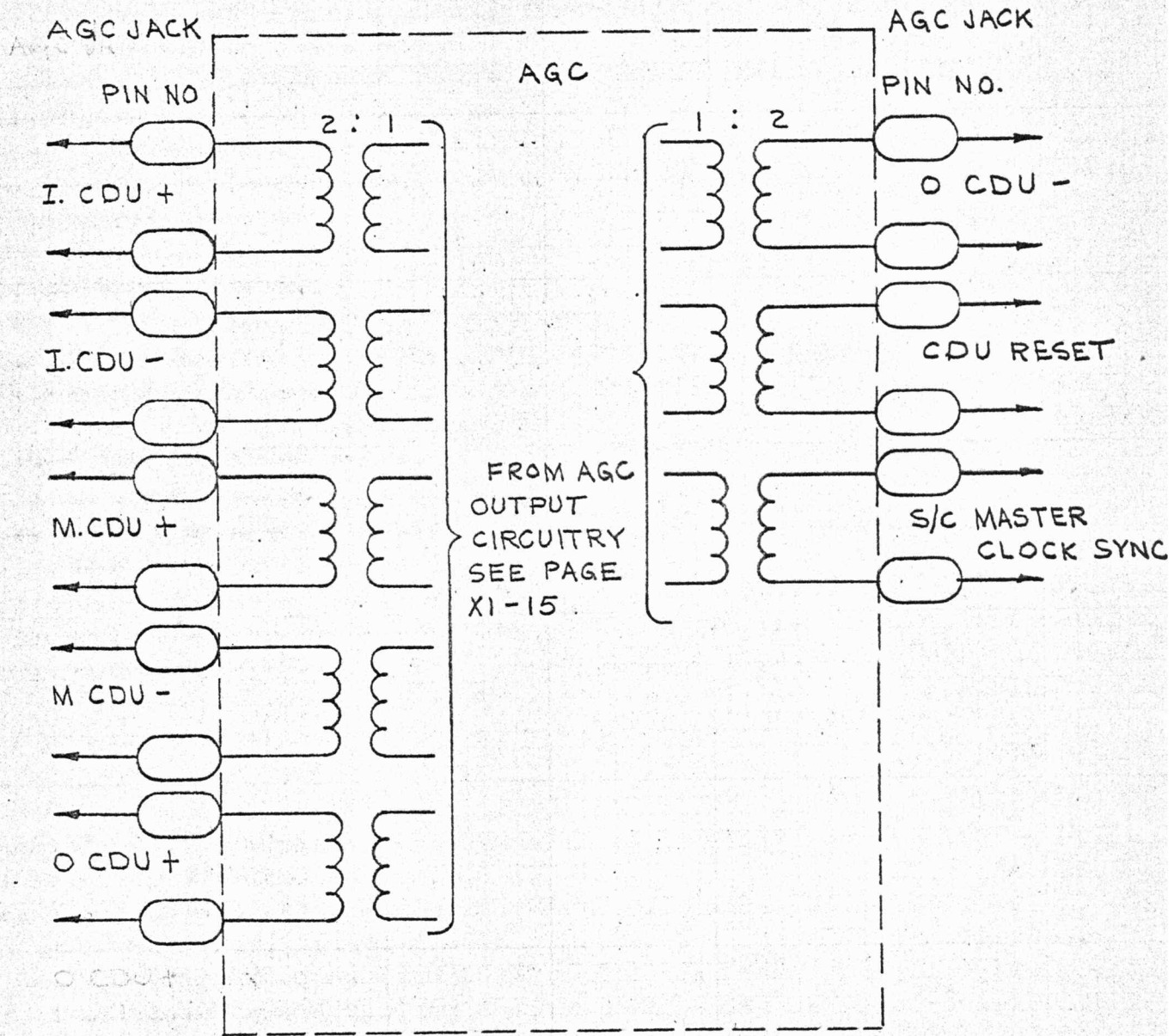


FIGURE VII-3

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AGC INTERFACE WITH CDU J. BOX

AGC INTERFACE WITH CDU J. BOX

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT OR OUTPUT (I/O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (U/P) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS						LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLITUDE	I	PULSE WIDTH	RISE TIME		FALL TIME	f
Δ A ENCODER OUTPUTS	I	3 CDU encoder circuits	By rotation of CDU shaft		Determine CDU Angles Pulses cause counters to be incremented or decremented			39.56 SEC		pulse			6 pair	XFMR	11 to 1.6K	1014 V PP	.5 to 3 sec. ± 3%	< 20% of Pul	< 20% of Pul				
3 CDU GET PULSE OUTPUTS	O	1 D/A converter in each CDU	When torquing of CDU shaft by AGC is desired. Initiated by a one in OUT Z, bit 5 or 4		only one CDU may be torqued at a time. The specified number of pulses in each burst time modulates the pulse train.			39.56 SEC	0 or 17.6 deg	pulse train			0 or 1600pps	6 pair	XFMR	1.6K	25 Vpp	3.4 sec ± 0.345	± 0.245	1.6 KC			
									25 pulses per new								500						
CDU RESET PULSE RATE	O	3 D/A converters	continuous		In conjunction with the set pulses, time modulates the D/A converter outputs								1 pair	XFMR	1.6K	25 Vpp	3.45 ± 0.345	± 0.245	1.6 KC				
																						500	
RELAY AND SWITCH VERIFICATION	I	K ₁ , K ₂ , K ₃ , K ₄ TRNSW ATTSW AGC GND	When contacts close		Informs AGC of relay states					dc level				0-28V dc	7								
MASTER CLOCK SYNC.	O	Master clock on IMU control panel	continuous		synchronizes the spacecraft master clock with the AGC.					square wave			1 pair	XFMR	1.6K	25 Vpp		± 0.245	512 KC				
																						500	

CHART 1 AGC Interface with CDU J. Box		AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN
SCALE NONE	T. W. D.	

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By J. Kerman Date

AGC OUTPUTS TO CDU J BOX

1. CDU SET PULSE OUTPUTS

Ref: AGC 4 Memo #5, NASA Dwg. 1010134

The AGC 4 torques the CDU shafts by means of bursts of pulses at a fixed rate of 1600 pps. To generate a rate-like output, it is necessary to repeat these bursts at fixed intervals. Typically, bursts lasting up to .08 seconds can be repeated every .24 seconds. The three CDU's must be pulsed sequentially with such a schedule.

Out bits 8-15 of Register OUT 2 (=W2) are reserved for generating Rate I and Outbits 1-5 of OUT 2 are used to generate Rate II. The outbit assignments for Rate I are as follows:

W2	Bit 15	-Rate I OUT
	14	+Rate I OUT
	13	1600 pps to O CDU
	12	1600 pps to M CDU
	11	1600 pps to I CDU
	10	1600 pps to Z GYRO
	9	1600 pps to Y GYRO
	8	1600 pps to X GYRO

To send a positive rate to the Inner CDU, a one is required in both Outbits 14 and 11. The reason for requiring two outbits to be set is to minimize the risk of accidentally sending unintended pulses due to program malfunction.

Prior to sending pulses to CDU Inner, a number 1-K is placed in Counter OUTCR I. 1-K is such that OUTCR I will overflow after K pulses have been sent. When OUTCR I overflows, all outbits associated with Rate I are knocked down to zero, preventing further pulses from being sent out.

The three CDU's may be controlled in sequence by using the display routine, which is entered every 80 msec. This process results in sending bursts of pulses to all three CDU's twelve times each second, or four times each second for each CDU.

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Rate II is controlled by Outbits 1-5 of OUT 2. Bit assignments are -

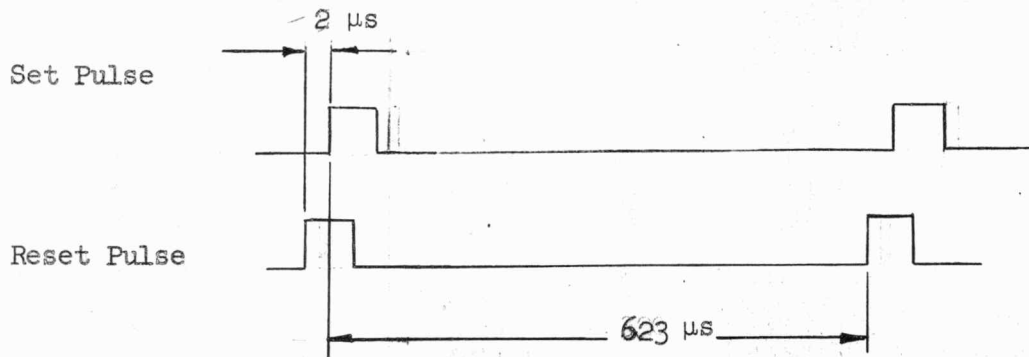
W2 B 5 - Rate II Out
 4 + Rate II Out
 3 Thrust. Reset is at 1600 pps
 2 Optics Y (1600 pps) Reset is at 1600 pps
 1 Optics X (1600 pps)

Rates I and II may be used simultaneously and independently.

2. CDU Reset Pulse Rate

Ref: AGC 4 Memo #5, NASA 1010134

The CDU reset pulse rate goes to the D/A converters in the inner, middle and outer CDU's. The 1600 pps rate is continuous and leads the set pulse rate by 2 microseconds. The following figure shows the phase relationship.



When the set pulse rate is on, the flip-flop of the D/A Converter is turned on for 623 μs and off for 2 μs of the 625 μs period. The CDU shafts are torqued at a rate of 17.6 degrees per second.

AGC Inputs from the CDU J Box

1. Δ A, CDU Encoder Outputs

Ref: AGC Memo #5, NASA 1010134

These are pulse waveforms from the CDU encoders to the AGC 4 input priority circuits. The priority circuits generate the address of the counter to be updated and also cause the interrupt to the program which will perform the updating. The scale factor equals 40 sac per pulse (approximately).

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VIII. AGC INTERFACE WITH PSA

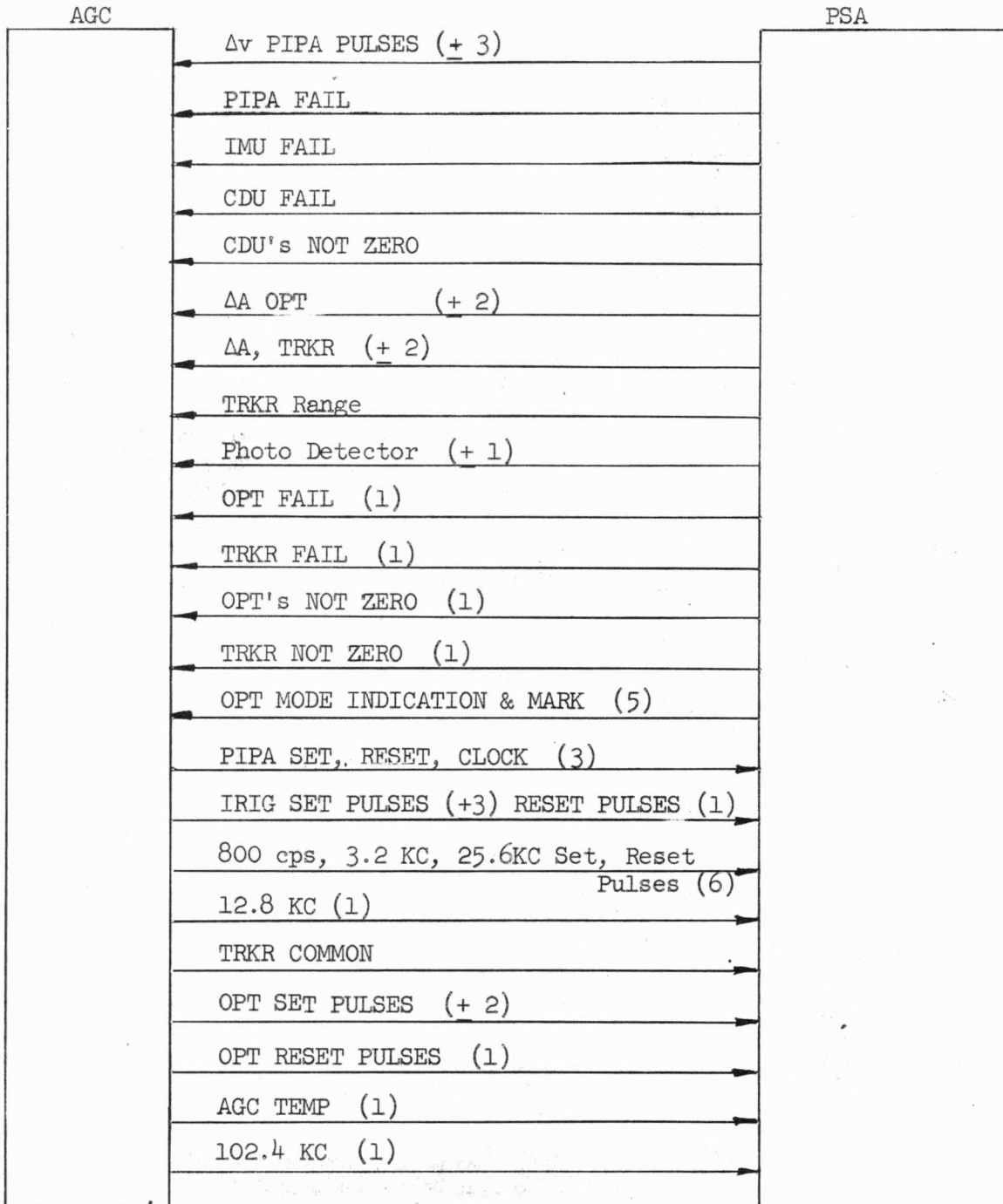
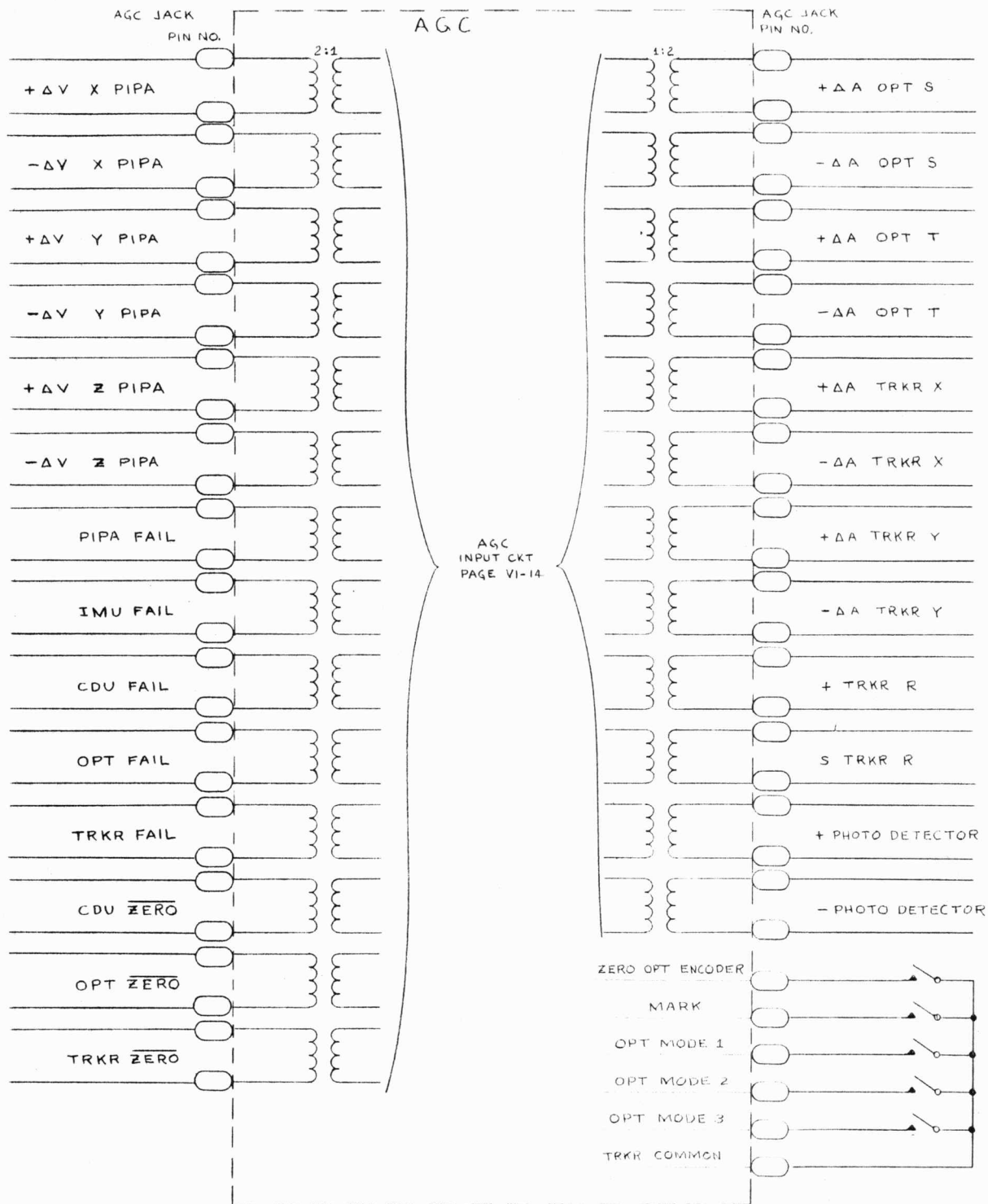


FIGURE VIII-1 AGC-PSA INTERFACE BLOCK DIAGRAM

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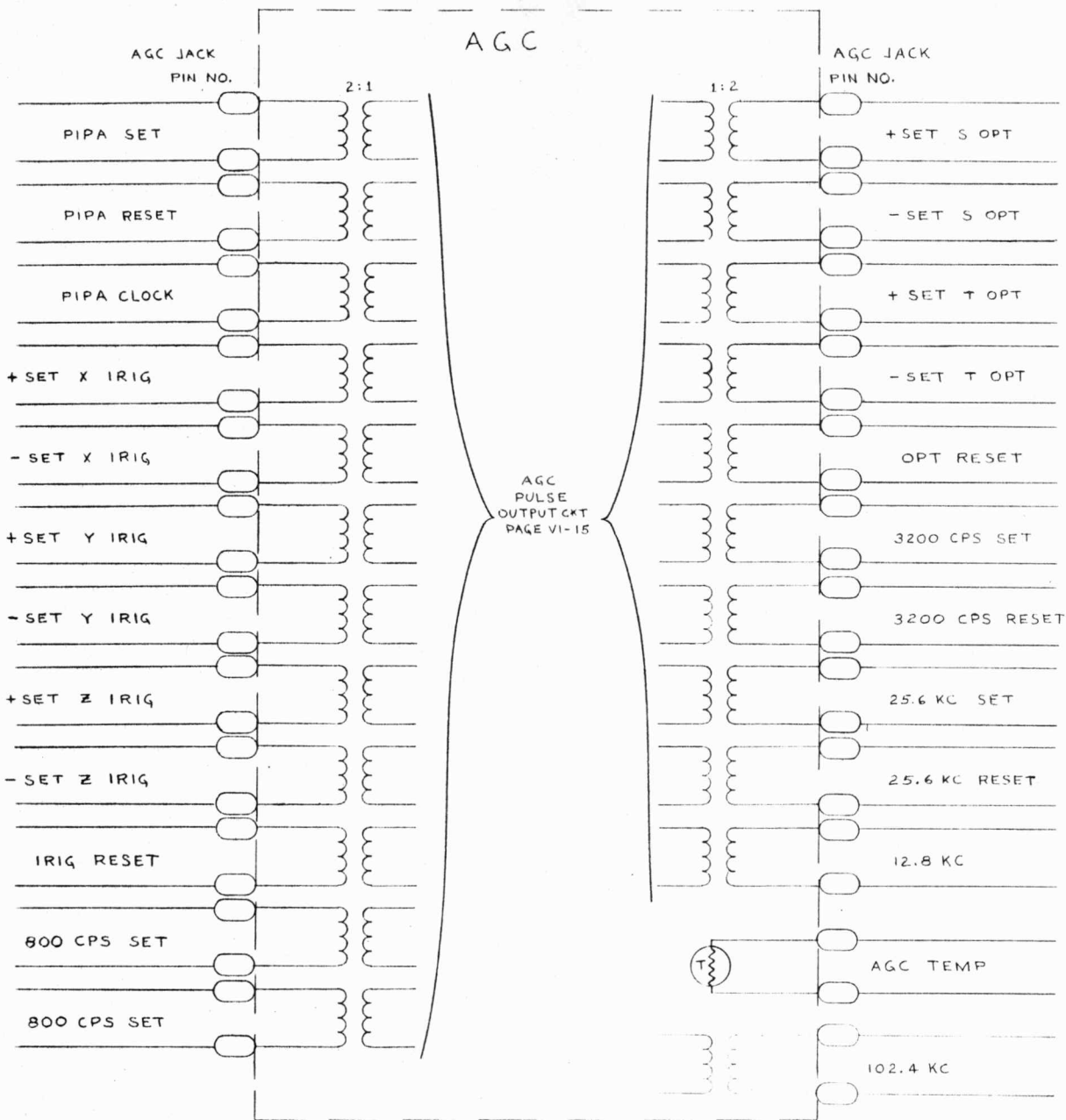
AGC-PSA INTERFACE SCHEMATIC

AGC INPUTS

FIGURE VIII-2 PAGE 1 of 2

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AGC-PSA INTERFACE SCHEMATIC

AGC OUTPUTS

FIGURE VIII-2 PAGE 2 of 2

AGC INTERFACE WITH PSA

AGC INTERFACE WITH PSA

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (U) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	PULSE WIDTH	RISE TIME	FALL TIME	UPPER LINE FOR TRANSMITTING END LOWER LINE FOR RECEIVING END.			
± ΔV PIPA PULSES	I	PIPA Current Switch	From differentiated rise of PIPA SET pulse when respective PIPA is torqued.		Increments (recement) X, Y, Z PIPA counters.	AGC will not know S/C velocity, be able to calibrate PIPA's, or to fine align the IMU.				Pulse				6 pair	Capacitor Compied	10V pp	5 μs	2 μs						
PIPA FAIL	I	OR in PSA	OR of 3 peak detected Signal Generator out- puts and 120Vdc		Used to change torquing scale factor and detect PIPA failure. INTERRUPT	AGC would not change scale factor and velocity integration may be in error.				Pulse				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW						
IMU FAIL	I	OR in PSA	OR of IG, MG and OG Error, 3200cps, Wheel Supply, RSVR Supply, and -28V Power loss.		Lights IMU FAIL and commands Coarse Align. INTERRUPT					Pulse				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW						
CDU FAIL	I	OR in PSA	OR of I, M, and O CDU errors, CDU Motor exci., and 25.6 KC Supply loss.		Light CDU FAIL and stops accel. integration INTERRUPT					Pulse train				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW					0.24 KC	
OPTICS FAIL	I									Pulse				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW						
TRACKER FAIL	I									Pulse				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW						
CDU'S NOT ZERO	I	Zero Detector	When I, M, & O CDU Resolvers are not all zeroed		Used to clear CDU counters.					Pulse train				1 pair	XFMR	1.1 to 10±4 1.4 K v pp	0.5 to 8 μs	< 20% of PW					0.24 KC	

<p>CHART 2 AGC - PSA INTERFACE</p>		<p>AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN</p>
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AGC INTERFACE WITH PSA

AGC INTERFACE WITH PSA

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME		φ	
OPTICS NOT ZERO	I	Zero Detector	When SXT and SCT Shaft and Trunnion RSVR's are not all zeroed.		Used to clear Optics counters.	OPT's angle readings will be in error.				Pulse				1 pair	XFMR	1.1 to 10 ± 4 1.4 K v pp				0.5 to 8 μs	< 20% of PW	< 20% of PW		
TRACKER NOT ZERO	I	Zero Detector	When TRKR angles are not all zeroed.		Used to clear TRKR counters.	TRKR angle readings will be in error.				Pulse				1 pair	XFMR	1.1 to 10 ± 4 1.4 K v pp				0.5 to 8 μs	< 20% of PW	< 20% of PW		
± ΔA OPTICS	I	Encoder	When rotation about respective axis occurs.		To compute Shaft and Trunnion angles. Increments (Decrements) counters.	OPT's angle readings will be in error.		Trunnion: 9.8 sec per bit. Shaft: 39.55 sec per bit.	Trunnion: 0° to +90° Shaft: ± 270°	Pulses	1 bit	1 bit	2 ¹⁵ pulses	4 pair	XFMR	1.1 to 10 ± 4 1.4 K v pp				0.5 to 8 μs	< 20% of PW	< 20% of PW		
± ΔA TRACKER	I	Encoder	When rotation about respective axis occurs.		To compute TRKR angles. Increments (Decrements) counters.	TRKR angle readings will be in error.				Pulses	1 bit	1 bit	2 ¹⁵ pulses	4 pair	XFMR	1.1 to 10 ± 4 1.4 K v pp				0.5 to 8 μs	< 20% of PW	< 20% of PW		
TRACKER RANGE	I				Increments or Shifts counter.					Pulses	1 bit	1 bit	2 ¹⁴ pulses	2 pair	XFMR	1.1 to 10 ± 4 1.4 K v pp				0.5 to 8 μs	< 20% of PW	< 20% of PW		
± PHOTO DETECTOR	I													2 pair										
ZERO OPTICS ENCODER INDICATION	I	FUNCTION SELECTOR SW 1	When SW 1 is in ZERO OPTICS position		Informs AGC that Optics function is zero encoder.					DC level				1	Switch Contact									
COMPUTER OPTICS MODE	I	OPTICS MODE SWITCH SW 3	When SW 3 is in COMPUTER position.		Informs AGC that Optics is in COMPUTER Mode.					DC level				1	Switch Contact									

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AGC INTERFACE WITH PSA

AGC INTERFACE WITH PSA

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TUDE	PULSE WIDTH	RISE TIME	FALL TIME	φ			
TRACKER OPTICS MODE	I	OPTICS MODE SWITCH SW 3	When SW 3 is in TRKR Mode position		Informs AGC that OPT is under TRKR control.					DC level				1	Switch Contact									
MARK	I	MARK BUTTON	When MARK BUTTON is depressed.		Commands AGC to read Optics, TRKR & CDU angles. INTERRUPT					DC level				1	Switch Contact									
TRACKER COMMON	O	SW 1, SW 3 and MARK BUTTON	Continuous							DC level				1	Contacts on Switches									
OPTICS SET PULSES	O	D/A CONVERTER	Rate II is controlled through OUT 2.		Torques OPT about Swit and Trunnion axes.					Time modulated pulse Train			0 or 1600pps	4 pair	XFMR 500	1.6K	5v pp	3 μs ± 0.3 μs	0.2 μs			1.6 KC		
OPTICS RESET PULSES	O	D/A CONVERTER	Continuous		Resets torque to Optics					Pulse train			1600pps	1 pair	XFMR 500	1.6K	5v pp	3 μs ± .3	0.2 μs			1.6 KC		
PIPA SET PULSES	O	PIPA Interrogator	Continuous		Interrogates phase and magnitude of Signal Generator output.	Gross failure or erratic behavior of PIPA loops.				Pulse train			1600pps	1 pair	XFMR 500	1.6K	5v pp	3 μs ± .3	0.2 μs			1.6 KC		
PIPA RESET PULSES	O	PIPA Torquing Circuits	Follows Set pulse by 78.1 μs in Sensitive, 312.5 μs in Normal. Off in Emergency		ANDed with Clock pulse to reset plus and minus Flip-Flops. This turns torquing current off.	Abnormal behavior of PIPA loops.				Pulse train			1600pps (SEN) 0 pps (E)	1 pair	XFMR 500	1.6K	5v pp	3 μs ± .3	0.2 μs			1.6 KC		

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SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME	
PIPA CLOCK PULSES	O	PIPA Torquing Circuits	Continuous		AND'ED with Inter- rogator output to set plus or minus Flip-flop. This turns torquing current on.	Faulty behavior of PIPA loops.				Pulse Train			12.8 K PPS	1 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	12.8 KC	
GYRO TORQUING SET PULSES $\pm X, Y, Z$	O	GYRO Torquing electronics	During Fine Erect and Calibrate. Controlled via OUT 2.		Turns plus or minus torquing current on.	Faulty behavior of Fine Erect loop.		1.1 deg/sec 2.7 sec per pulse	Time modulated 1600pps		2 ¹⁹ pulses per rev.	0 or 1600pps	6 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	1.6 KC		
GYRO TORQUING RESET PULSES	O	GYRO Torquing electronics	Continuous		Turns torquing current off.	Faulty behavior of Fine Erect loop.			pulse train		1600pps	1 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	1.6 KC			
800 PPS SET AND RESET	O	800 CPS Power Supplies	Continuous		Phase and Frequency reference to 800cps Power Supplies. Set leads Reset by 180°	Power Supply will free- run at 800 CPS $\pm 10\%$			pulse trains		800pps	2 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	800 PPS			
3200 PPS SET AND RESET	O	3200 CPS Power Supplies	Continuous		Phase and Frequency reference to 3200cps power supplies. Set leads Reset by 180°	Power Supply will free- run at 3200 CPS $\pm 10\%$			Pulse trains		3200 pps	2 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	3.2 KC			
25.6 K PPS SET AND RESET	O	25.6 KC Encoder Excitation Supplies	Continuous		Phase and Frequency reference to Encoder Excitation Supplies. Set leads Reset by 180°				Pulse Trains		25.6 KC	2 pair	XFMR	1.6 K	5v pp		3 μ s $\pm .3$	0.2 μ s	25.6 KC			

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AGC INTERFACE WITH PSA

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT OR OUTPUT (I/O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME		f	
12.8 K PPS	O	PSA DC/DC Converters	Continuous		Sync pulses to +120v and -28v DC/DC Converters. Sync frequency is 6.4 KC	DC/DC Converters will free-run at 6.0 to 6.2 KC.				Pulse train			12.8 K PPS	1 pair	XFMR	1.6 K	5v pp			3.45 ±.3	0.245			2.8 KC
AGC TEMPERATURE	O	PSA T/M Conditioning Circuit	Continuous		Indicates crystal clock temperature.					DC				2										
102.4 KC	O	Error & Failure Detectors	Continuous		Switches back to AGC by Detectors for ZERO and Failure indications					Pulse train			102.4 K PPS		XFMR	1.6 K	5v pp			3.45 ±0.345	0.245			2.8 KC

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PRELIMINARY AGC INTERFACE SPECIFICATION

By

J. Kernan

Date

AGC Inputs from PSA

1. $\pm \Delta V (X_{sm}, Y_{sm}, Z_{sm})$

Ref: Project Memo 194

These pulses originate in the PIPA current switch as a result of an AND or the appropriate torquing flip-flop, which must be set, and the differentiated inverted PIPA Set Pulse. Therefore, the ΔV pulse is dependent on the trailing edge of the Set Pulse.

The velocity scale factors for these pulses can be determined by referring to Page 312 of AGANI.

2. PIPA Fail

Ref: AGANI p. 465

The PIPA Fail signal is generated by comparing the signal generator outputs to a reference. If the S.G. output exceeds the reference, the PIPA Fail signal is issued. A loss of +120 VDC also results in PIPA Fail. The AGC responds to PIPA Fail by switching to a higher torquing mode. If this signal occurs during the Emergency mode, the AGC will light the Accelerometer Fail indicator and stop integrating the PIPA ΔV outputs.

This is an automatic interrupt (RUPT 2) to bit 11 of IN 2.

3. IMU FAIL, CDU FAIL, OPTICS FAIL, AND TRACKER FAIL

These are all interrupts (Rupt 2) to Bits 12, 10, 9 and 8 respectively of IN 2.

QUESTIONS

What are the electrical characteristics of these signals? What criteria is used to initiate these signals and how are they generated?

4. CDU's NOT ZERO, OPTICS NOT ZERO, AND TRACKER NOT ZERO

These signals are inputs to Bits 1,2, and 3 of IN 2 respectively.

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By

J. Kernan

Date

1/14/68

QUESTIONS

What are the electrical characteristics of these signals?

5. + ΔA OPTICS

These inputs to AGC counters enable the AGC to read the shaft and trunnion angles of the OPTICS.

It appears that there will be no SXT in the LEM, but a radar or Laser tracker instead.

6. TRACKER RANGE

Ref: AGC-4 MEMO #6

It appears that this information will be received in bit bursts of one word length. This follows from the fact that the counter inputs are + and shift only.

7. + PHOTO DETECTOR

This signal will presumably be generated by a photosensitive device attached to the OPTICS eyepiece. Its purpose is evidently star or horizon seeking and tracking. The torquing loop would be closed through the computer.

8. OPTICS MODE SWITCH

Ref: NASA Dwg. 1015100 and 1006060

Sheet 7 of 1006060, AGC Interface, shows three inputs from the Optics Mode Switch. The Optical System Functional Diagram, 1015100, shows only two inputs from this switch. For the purpose of this document, the latter is assumed to be correct.

9. MARK

Ref: NASA Dwg. 1006060 and 1015100

MARK is an interrupt (Rupt 4) to Bit 15 of IN 0. This signal commands the AGC to read the OPTICS encoder angles by storing the present counter value. The AGC also records the CDU counter values and the time.

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By J. Kernan

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AGC Outputs to PSA

1. TRACKER Common

This line is connected to the wiper arm of the MARK button, Optics Mode Switch and the Optics Function Selector. It is switched back to the AGC by these switches to indicate the wiper arm position.

QUESTION: What value of voltage is maintained on this line?

2. OPTICS Set Pulses

Ref: AGC In-Out Book

These are plus or minus set pulses, controlled through OUT 3 and sent to the Optics D/A converter. The pulse rate is 1600 pps, time modulated to control the average torquing rate. Only one output can be active at any one time. The scaling of these pulses has not been determined as yet.

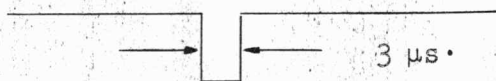
The set pulses will be delayed from the reset pulses by 2μ seconds.

3. PIPA Set Pulses

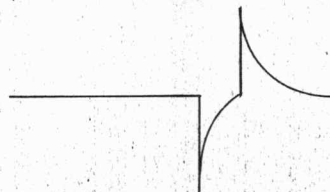
Ref: Project Memo 194
NASA Dwg. 1006501

This is a continuous 1600 pps signal used to interrogate the phase and magnitude of the signal generator output. In addition, this pulse is inverted and differentiated; the resulting waveform is summed with the torquing flip-flop to generate the ΔV pulse.

INVERTED SET PULSE



Differentiated Set Pulse



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By J. Kernan

Date 11/14/61

Since it is the positive portion of the differentiated pulse that is used to trigger the ΔV pulse, the ΔV pulse will be dependent upon the fall time of the original set pulse.

The PIPA Set Pulse leads every eighth clock pulse by 2μ sec.

The scaling of the Set Pulses for the three PIPA modes of operation is as follows:

Sensitive: 1.68 cm/sec/pulse
Normal: 5.22 cm/sec/pulse
Emergency: 9.34 cm/sec/pulse

4. PIPA Reset Pulses

Ref: NASA Dwg. 1006501

The PIPA Reset Pulse is a 1600 pps waveform which is used to control the torquing mode of the PIPA loop. The length of time that the torque current is applied is determined by the time between a PIPA Set Pulse and the following PIPA Reset Pulse. During the Sensitive mode the Reset Pulse is delayed by 78.1μ s from the set pulse; during Normal it is delayed by 312.5μ sec. During Emergency mode, there is no Reset Pulse.

The AGC controls the Reset Pulse signal through Bit 11 (Scale PIPA fine) and Bit 12 (Scale PIPA Emerg) of OUT 4.

These waveforms are shown in Figure VIII-3.

5. GYRO Set Pulses

The Gyro Set Pulse signal is a time modulated 1600 pps waveform. The time modulation allows the AGC to vary the average torquing rate. Only one Gyro Set Pulse Output will be ON at one time - the gyros will be scanned. The set pulse lags the reset by 2μ seconds.

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PRELIMINARY AGC INTERFACE SPECIFICATION

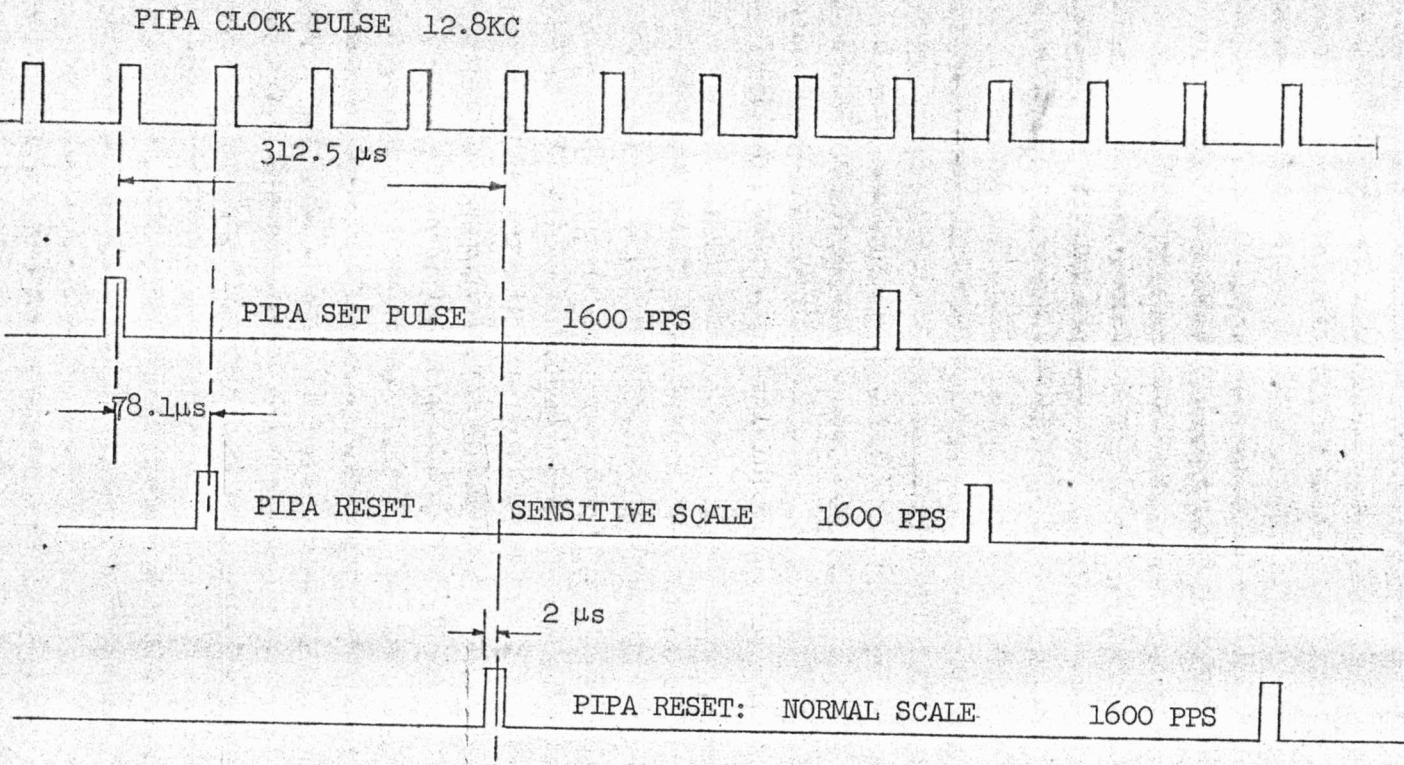
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NOTES:

1. No reset pulse for emergency scaling
2. All pulse widths: $3 \pm 0.3 \mu s$

PIPA PULSE TIMING

FIGURE VIII-3

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By J. Kernan

Date 1/29/63

IX. AGC INTERFACE WITH DISPLAYS AND CONTROLS

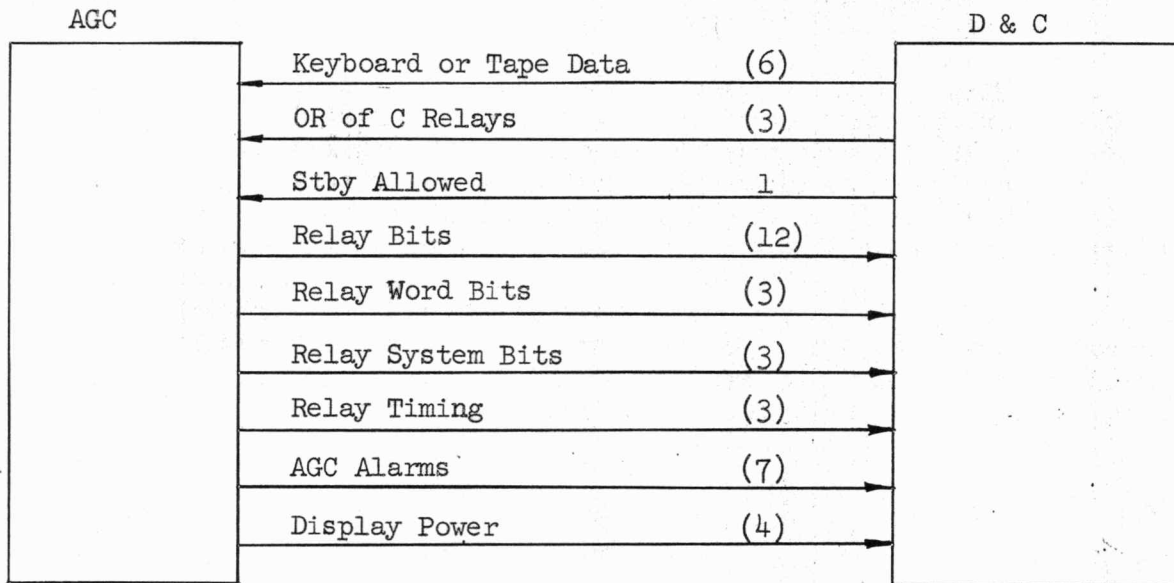


FIGURE IX-1 AGC- D & C INTERFACE BLOCK DIAGRAM

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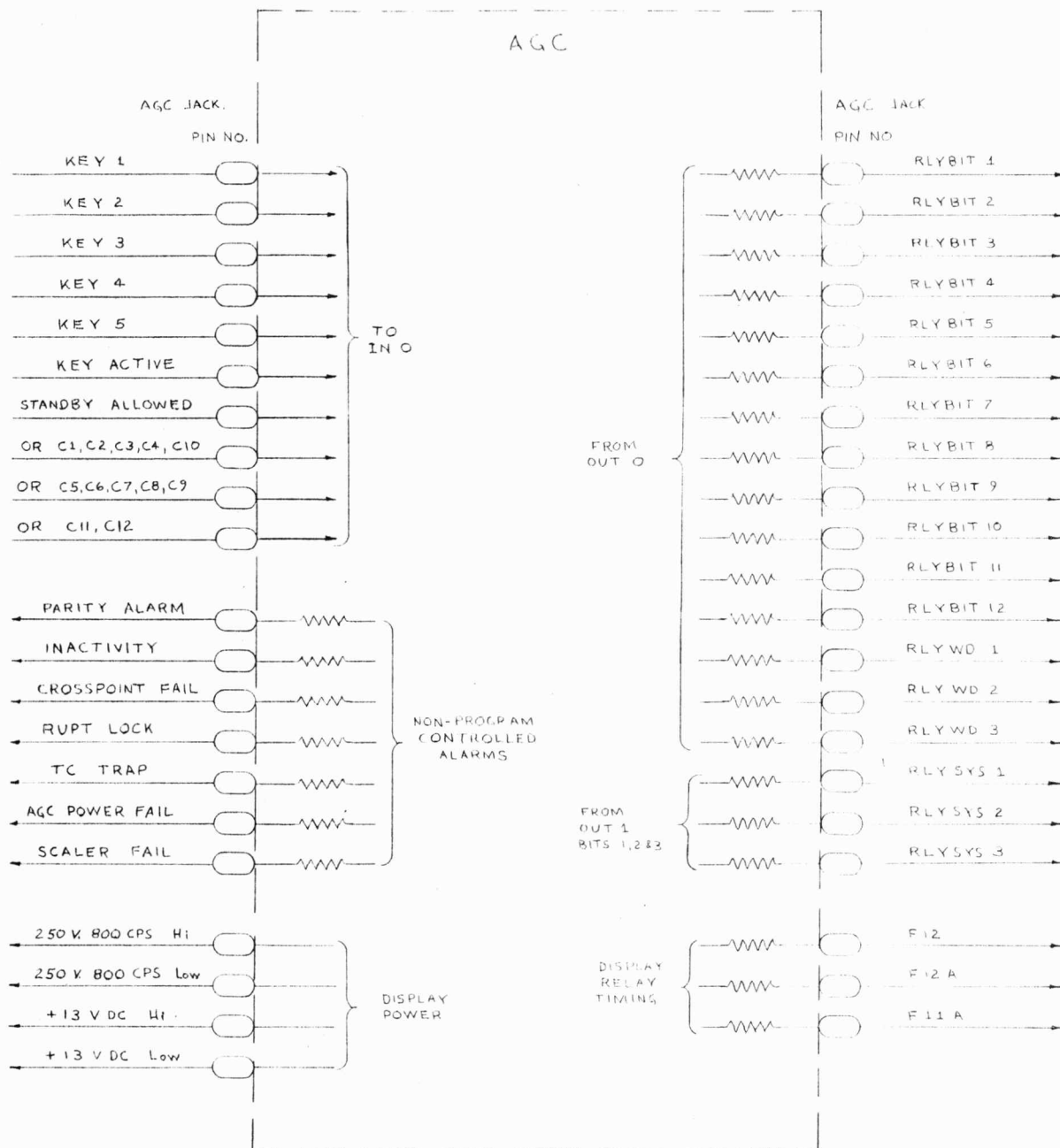


FIGURE IX-2

AGC-D&C INTERFACE SCHEMATIC

AGC INTERFACE WITH AGC D&C

AGC INTERFACE WITH AGC D&C

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS								LINE DELAY			
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME	f				
KEYBOARD OR TAPE READER INPUTS	I	2 S/C Keyboards or Factory Tape Reader	By key depression		To enter data and commands - 5 lines. Keyboard Active (KEYRPT) - 1 line.					DC level				6	Switch Contacts											
OR OF C1,C2,C3,C4,C10 OR OF C5,C6,C7,C8,C9 OR OF C11,C12	I	C Relays												3	Relay Contacts											
DISPLAY POWER	O		Continuous		Used to light electroluminescent displays.					Sine wave				2			250 RMS								800 KPS	
DISPLAY LOGIC POWER	O		Continuous							DC				2 Hi and Low			+13V								0	
FLY BIT FLY WD FLYSYS	O	RYWORD and ELWORD Decoding Matrix	Through OUT 0 and bits 1,2,3 of OUT 1.		Operates: 1. Two S/C AGC Display Panels 2. IMULC DU, OPT & TRKR SWITCH- ING. 3. Alarm and Condition lights.					DC level				18	NPN Collector											

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AGC INTERFACE WITH AGC D&C

AGC INTERFACE WITH AGC D&C

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME		f	
RELAY TIMING	F12	O			Continuous					Square Wave				1	NPN Collector						50.245	25 PPS		
	F12A	O			Continuous					Pulse Train				1	NPN Collector					10.45	50.245	25 PPS		
	F11A	O			Continuous					Pulse Train				1	NPN Collector					10.45	50.245	50 PPS		
NON-PROGRAM CONTROLLED ALARMS	O	Display Lamps	When internal AGC failures occur.		Lights: PARITY ALARM INACTIVITY AGC PWR FAIL CROSSPOINT FAIL RUPT LOCK TC TRAP SCALAR FAIL 3 Spares					DC level				7	NPN Collector									
STANDBY ALLOWED	I	STANDBY ALLOWED SWITCH	Whenever no maj AGC function is needed.		Requests AGC to enter Standby if no interrupt is present.					DC level				1	Switch Contact									

CHART 3
AGC - AGC D&C
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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kerman Date

AGC Inputs from D & C

1. Keyboard Codes and Key Active

Ref: AGC 4 Memo #5

Each of the keyboard keys when depressed presents a particular 5 bit code to bits 1-5 of IN 0. At present, there are 16 keys: 0 through 9, +, -, Noun, Verb, Clear and Enter-Execute.

Every key energizes the Keyboard Active line, bit 6 of IN 0. This is an interrupt (KEYRUPT) which transfers control to a program which examines the contents of IN 0.

The Keyboard allows only one key depression during an adjustable hold-in time. This hold-in time must be long enough to allow for contact bounce, interrupt reaction and IN 0 examination time.

These same lines provide tape reader inputs during factory and lab tests.

2. STANDBY Allowed

Ref: AGC 4 Memo #5

This signal, from a two-position manual switch, allows the AGC to enter the Standby mode. In Standby, the high current +3 VDC supply is turned off and the AGC is relegated to keeping time.

When Standby allowed is a one, a program entered which sets all output bits to zero, synchronizes counter TIME 1 to the scaler, sets bit 8 of OUT 1 (Standby) to one and turns the high current +3V supply off.

The AGC will not enter Standby until all interrupts have been processed.

While in Standby, the AGC turns itself on for a 10 msec interval every 1.28 seconds. Upon turn on, it initiates the sequence described above, incrementing TIME 1 by 2¹. It will return to Standby if no other action is requested.

3. OR of C Relays

Ref: AGC In-Out Book, NASA Dwg. 1006060

These are three signals to INPUT Register 1. The OR of C1, C2, C3, C4 and C10, which control the IMU relay drivers, is the input to Bit 5. The OR of C5, C6, C7, C8 and C9, which control the alarm lights, is the input to Bit 6.

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**ENGINEERING
DESIGN INFORMATION
EXHIBIT**

PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan Date 1/13/63

(3. OR of C Relays Cont'd.)

The OR of C11 and C12, which control the OPTICS relays, is the input to bit 7.

It appears that these are feedback signals which inform the AGC on which C relays are being switched.

QUESTIONS:

Is the purpose of these signals as described above, correct?

Is the meaningful signal a pulse or a steady DC value?

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AC SPARK PLUG DIVISION
General Motors Corporation
Milwaukee, Wisconsin

XDE 34-S-504A

ENGINEERING
DESIGN INFORMATION
EXHIBIT

PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Date

AGC Outputs to D & C

1. Non-Program Controlled Alarms

Ref: AGC 4 Memo #5, NASA Dwg. 1006060

The alarms which indicate an AGC failure are Parity, Inactivity, Crosspoint Fail, TC Trap, Ruptlock, Scaler Fail, and AGC Power Fail.

The Parity Alarm is issued if a word with an even number of ones is detected. This check is performed on all data transfers to and from fixed and erasable memory.

The Inactivity alarm indicates a fault in the crystal oscillator or 512 KC reference frequency.

Crosspoint Fail indicates a malfunction of the Sequence Generator.

The TC Trap will be issued if the instruction in location L is TCL. This occurrence would prevent the program from advancing, however, the alarm triggers the GO sequence. This alarm will also be issued if the counter priority circuit fails so as to cause endless counting.

The Ruptlock alarm is issued and the GO sequence triggered if an interrupt state persists for 20 m sec.

The Scaler is checked by verifying that one of its low frequencies has occurred within the last second.

The AGC Power Fail alarm if one of the three power supplies fails. These three are the +13V, the +3V (A) and the switchable +3V (B) supplies.

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X. AGC INTERFACE WITH LINK

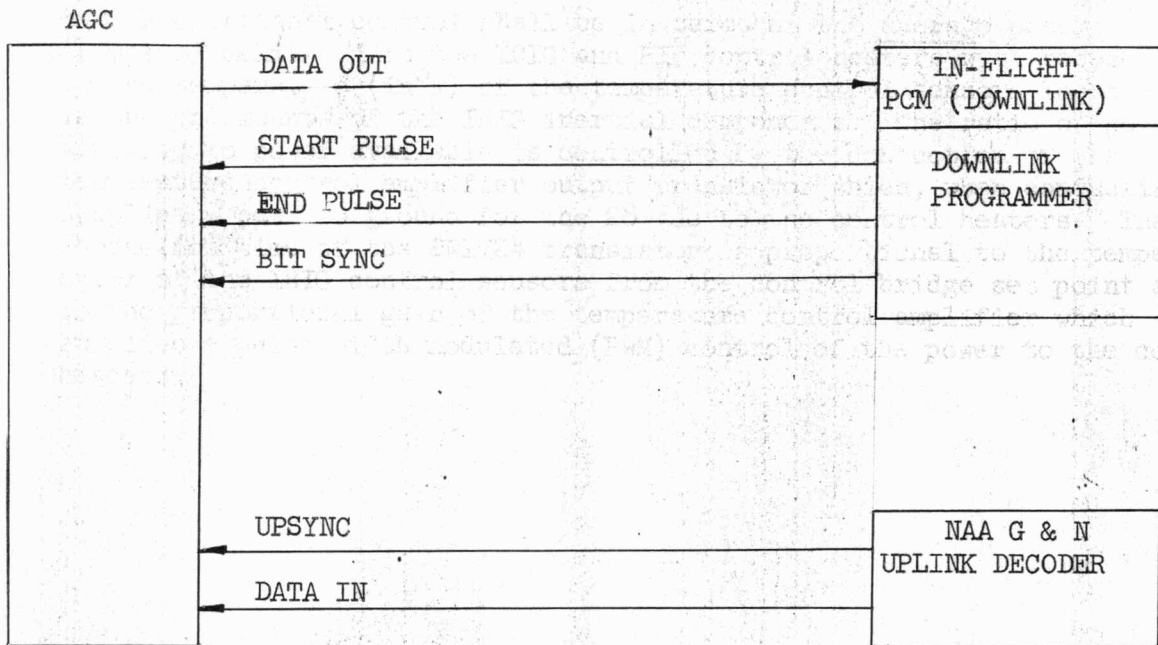


FIGURE X-1 AGC-LINK INTERFACE BLOCK DIAGRAM

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AGC - LINK INTERFACE SCHEMATIC

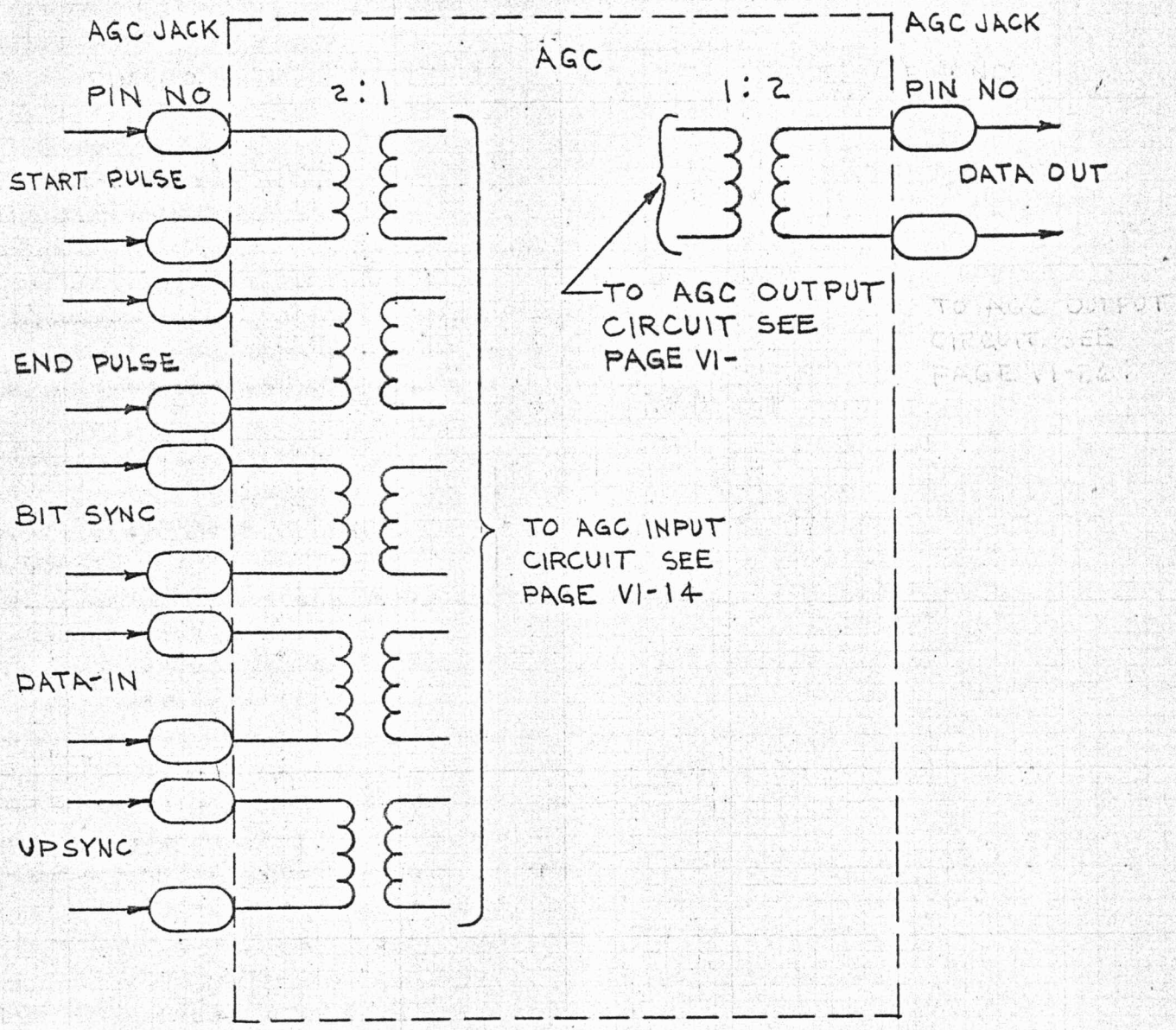


FIGURE X-2

AGC INTERFACE WITH LINK

AGC INTERFACE WITH LINK

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (1) OR OUTPUT (0)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME		f	
UPSYNC	I	SPACE carry-on transceiver	By transmission of "zero" to UPLINK counter in AGC. Max rate: UPSYNC + DATA-IN = 80pps		Shift the UPLINK counter one bit to left	UPLINK is cleared by transmitting 16 con- secutive "zeros" to AGC before further data transmissions				pulse				1 pair	XFMR	1:1 to 1:6 K	10V± 4Vpp		0.5 to 8μs @ 90% amp.	<20% of pul width	<20% of pul width			
DATA-IN	I	SPACE carry-on transceiver	By transmission of "one" to UPLINK counter in AGC. Max rate: UPSYNC + DATA-IN = 80pps		Shift and increment the UPLINK counter	same as above				pulse				1 pair	XFMR	1:1 to 1:6 K	10V± 4Vpp		0.5 to 8μs @ 90% amp.	<20% of pul width	<20% of pul width			
START PULSE	I	Downline programmer	Signal to AGC that transfer of word to PCM is to begin. Occurs at beginning of every data transmission to PCM. Rate = 25 pps (50 pps optional). Must precede bit sync by at least 2μs		Used to initiate the unloading of OUT 4 under control of bit sync pulses.					pulse train				1 pair	XFMR	1:1 to 1:6 K	10V± 4Vpp		0.5 to 8μs @ 90% amp.	<20% of pul width	<20% of pul width		25 pps	
BIT SYNC PULSE	I	Downline programmer	Initiated by down- line programmer when a data bit is transferred from AGC to PCM 40 pulses per AGC transmission AGC word twice = 8 bit code		Used to sync the transfer of data from the OUT 4 register to the PCM					pulse train				1 pair	XFMR	1:1 to 1:6 K	10V± 4Vpp		0.5 to 3μs @ 90% amp.	<20% of pul width	<20% of pul width			64 μs

CHART 4 AGC INTERFACE WITH LINK		AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN
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SCALE	T.W.D.	XDE-3A-S-304A PAGE X-3

AGC INTERFACE WITH LINK

AGC INTERFACE WITH LINK

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS							LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TUDE	I	PULSE WIDTH	RISE TIME	FALL TIME		f	
END PULSE	I	Downtel programmer	Initiated by downtel prog. at end of tran- mission (Rate = 25 pps - 50 pps optional)		Used to signal end of transmission. Initiates the inter- rupt DSRUPT for routine to load OUT 4 for next transmission.					pulse train				1 pair	XFMR	1.1 to 1.6 K	10% 4V pp		.5 to 8 45 @ 90% of amp	<20% 0+ p.w. 10 to 30 % of amp	<20% of p.w. to 30 % of amp	25 pps		
DATA OUT	O	INFLIGHT PCM	INITIATED by bit sync pulses @ a 64 KC rate							pulse train				1 pair	XFMR	1.6 K	25% pp		3 us 0.3 us	≤ 0.2 us				

<p>CHART 4 AGC INTERFACE WITH LINK</p>		<p>AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN</p>
SCALE None	T.W.D.	

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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Date

Uplink Inputs to AGC

Ref: AGC 4 Memo #5, A.P.M. #230

There are two lines which transmit information to the AGC from the "SPACE" carry-on transmitter. These are the upsync and the data-in lines..

1. Upsync Line

The upsync line transmits "zeros" to the AGC. When a "zero" is being sent, a pulse appears on the upsync line. This input causes the Uplink counter to be shifted left one bit (called SHINC).

2. Data-in Line

The data-in line transmits "ones" to the AGC. When a "one" is being sent, a pulse appears on the data-in line. This input causes the Uplink Counter to be shifted left one bit and then incremented (SHINC, PINC).

Sixteen bit transmissions to the AGC constitute one word of data. The first bit sent is always a one. Because the UPLINK counter is fifteen bits long, the sixteenth transmission forces the counter to overflow. This action initiates the interrupt UPRUPT which processes the contents of UPLINK and clears it for the next transmission.

The inputs to uplink may be asynchronous with a repetition rate of at least 12 msec between pulses. This allows a maximum of 5 words per second to be accepted by the AGC.

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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Date

AGC Interface with Downlink

Ref: AGC 4 Memo #5

For transmission of data to the SPACE Checkout System, a single PCM channel with a bit frequency of 64 KC will be used. The following defines the format for the telemetry system.

Group: One second's worth of pulses ($=64 \times 10^3$ bits)

Frame: 20 ms worth of pulses (= 1280 bits)
One group = 50 frames

Word: 125 ms worth of pulses (= 8 bits)
One frame = 160 words

Bit: 1 pulse
1 word = 8 bits

The transmission period allotted to the AGC is five consecutive telemetry words per alternate frame (every frame as an option). Each five words constitute a transmission and corresponds to a single 16 bit AGC word sent twice (for error detection and correction) and an 8 bit identifying code. This identifying code tells if the transmitted AGC word is a data word or an address.

The interface consists of three transformer coupled lines from the down-telemetry programmer to the AGC and one transformer coupled output from the AGC to the PCM. The three inputs to the AGC are start pulses, bit sync and end pulse and the output is called data out.

The down-telemetry programmer sends a start pulse to the AGC every other frame (or every frame as a second choice). The AGC word which is stored in output Register 4 (OUT 4) is then scanned by the bit sync pulses. This continues for 32 bit sync pulses after which an 8 bit code is sent as explained above. After the 40th bit sync pulse, the transmission is terminated. The start and end pulses precede the bit sync pulses by a slight amount to insure that the first pulse sent to the PCM is not delayed relative to the leading edge of the bit sync pulse. The format is shown in the diagram below.

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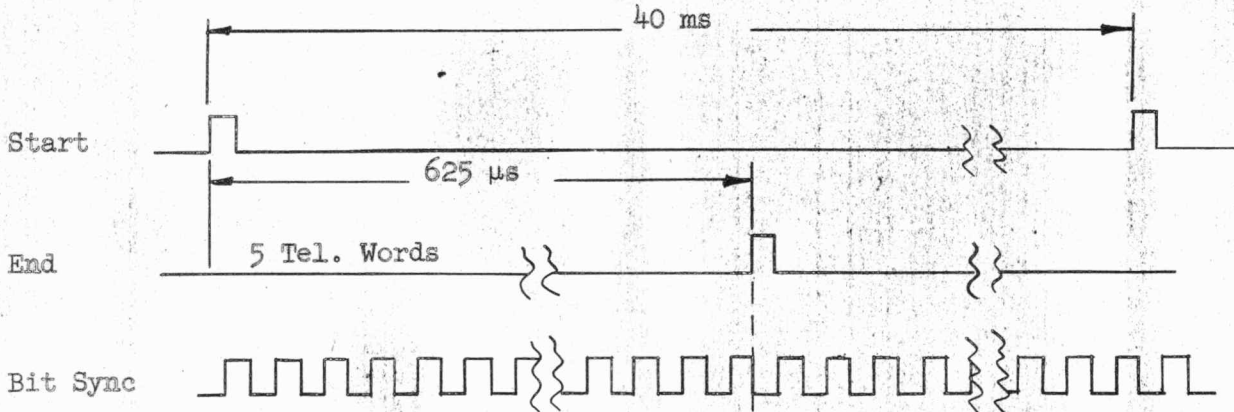
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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Date 2/14/58



The end pulse performs two functions. It terminates the transmission period and also initiates the interrupt DSRUPT. This program loads the next word to be transmitted into OUT 4.

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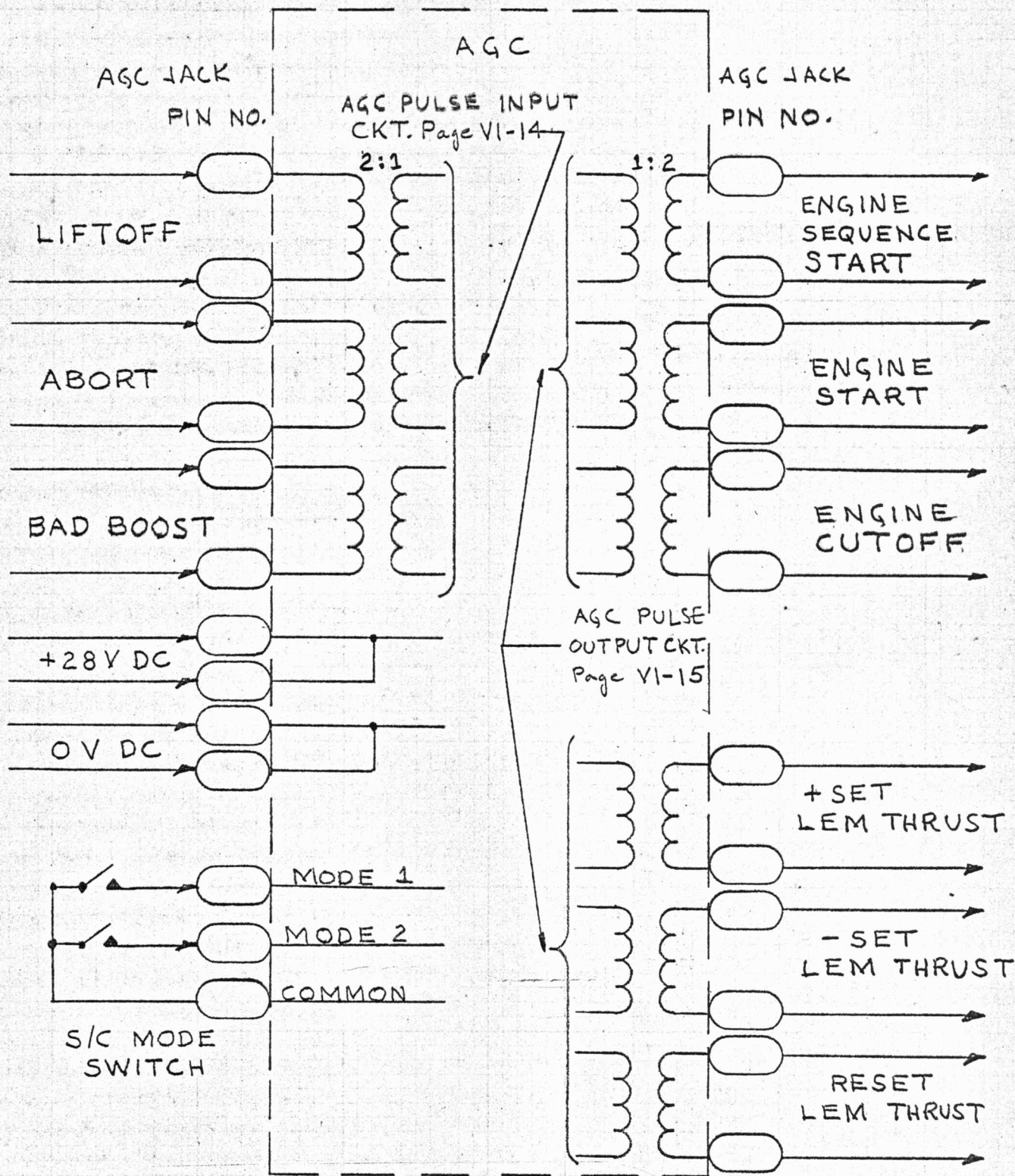


FIGURE XI-2
AGC-S/C INTERFACE SCHEMATIC

AGC INTERFACE WITH S/C

AGC INTERFACE WITH S/C

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO. OF LINES	SIGNAL CHARACTERISTICS <small>UPPER LINE FOR TRANSMITTING END LOWER LINE FOR RECEIVING END</small>							LINE DELAY					
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	PULSE WIDTH	RISE TIME	FALL TIME	f						
+ 28 V DC PRIME POWER	I		Continuous for AGC operation		Used to generate +3vdc (A&B) and +13vdc AGC power.	Marginal operation of AGC if supply is low.				DC Hi & Low				4			28 ± 3 -2vdc									0	
S/C MODE 1 S/C MODE 2	I	S/C MODE SWITCH			To bits 13 & 14 of IN 3.					DC level				3													
LIFTOFF	I				To bit 15 of IN 3. Informs AGC of either Booster or LEM liftoff.					Pulse				1 pair	XFMR												
BAD BOOST	I		When boost phase is bad.		To bit 14 of IN 2. INTERRUPT					Pulse				1 pair	XFMR												
ABORT	I		When an abort condition exists		To bit 13 of IN 2. Causes INTERRUPT to Abort Program.					Pulse				1 pair	XFMR												
ENGINE SEQUENCE START	O	Engine Control System	During Mid-course for ΔV correction. When bit 14 of OUT 1 is a 1.		Starts Engine Clock.					Pulse train				1 pair	XFMR	1.6K 500	$\geq 5v_{pp}$	$3 \mu s$ $\pm .3$	502,45								102.4 KC
ENGINE START	O	Engine Control System	During Midcourse for ΔV correction. When bit 13 of OUT 1 is a 1.		Starts Engine					Pulse train				1 pair	XFMR	1.6K 500	$\geq 5v_{pp}$	$3 \mu s$ $\pm .3$	502,45								102.4 KC
ENGINE CUTOFF	O	Engine Control System	When bit 15 of OUT 1 is a 1		Turns Engine Off.					Pulse train				1 pair	XFMR	1.6K 500	$25v_{pp}$	$3 \mu s$ $\pm .3$	502,45								102.4 KC

CHART 5
AGC - S/C
INTERFACE

AC SPARK PLUG DIVISION
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AGC INTERFACE WITH S/C

AGC INTERFACE WITH S/C

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (1) OR OUTPUT (0)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (UP) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS						LINE DELAY		
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TUDE	I	PULSE WIDTH	RISE TIME		FALL TIME	f
LEM THRUST SET PULSE RATE(±)	0	LEM	When bit 3 and bit 4 (+) or bit 5 (-) of OUT 2 are 1's.		Controls the thrust magnitude of the LEM engine.					Time modulated pulse train				2 pair	XFMR	1.6K	≥5v _{pp}		3.45 ±.3	50.245		1/6 KC	
LEM THRUST RESET PULSE RATE	0	LEM	Continuous		Controls the thrust magnitude of the LEM engine.					Pulse train				1 pair	XFMR	1.6K	≥5v _{pp}		3.45 ±.3	50.245		1/6 KC	

<p>CHART 5 AGC - S/C INTERFACE</p>		<p>AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN</p>
<p>SCALE</p>	<p>J.E.K.</p>	

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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

Date

AGC Inputs from S/C

1. 28 VDC Hi and Low

Ref: NASA Dwg. 1006060, AGC 4 Memo #5

This power supplies prime AGC operating power. Each level is brought in on two lines for either reliability or loading reasons, or both.

QUESTIONS:

What is the allowable variation of voltage level of the supply?

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XII. AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

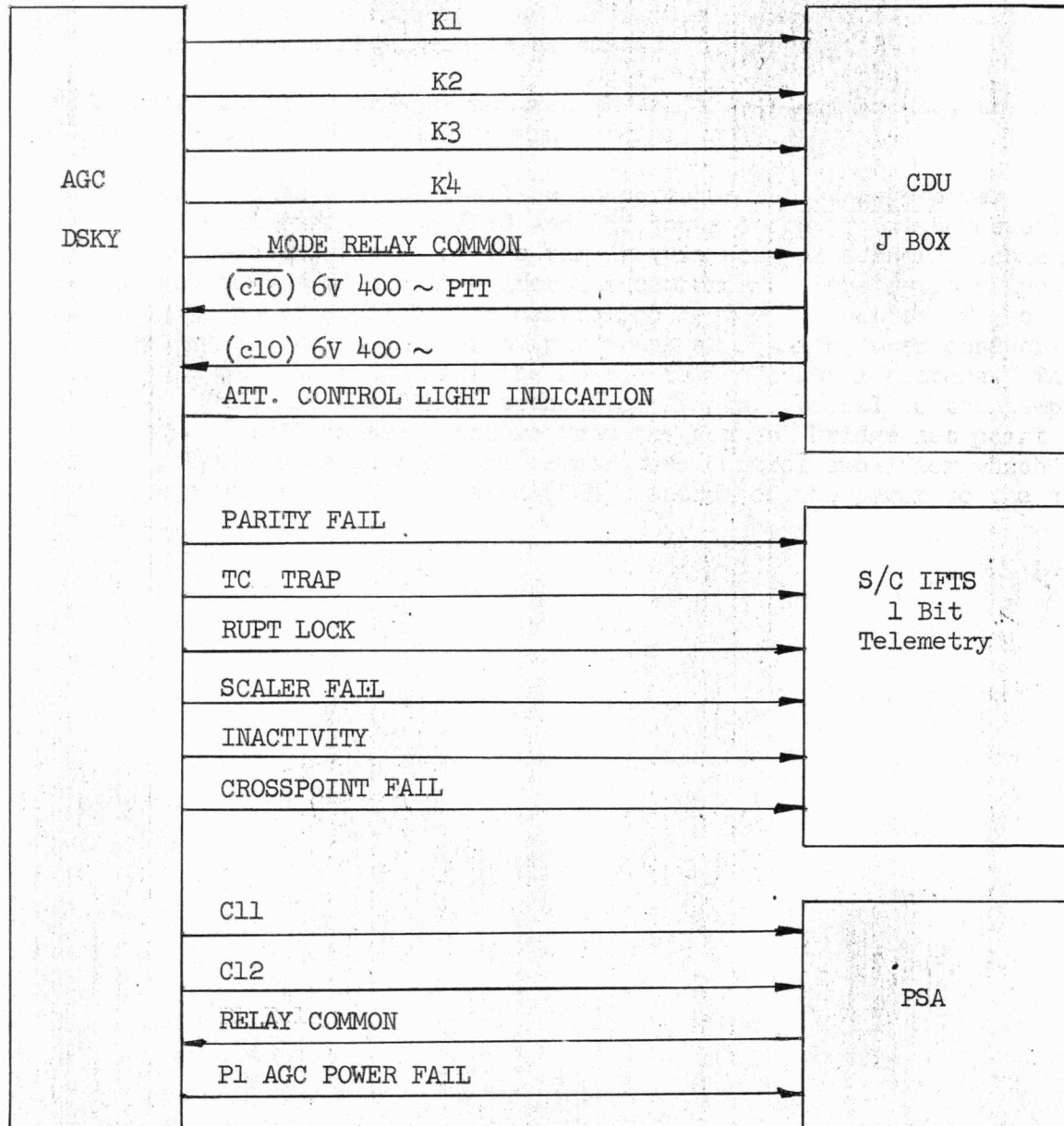


Figure XII-1

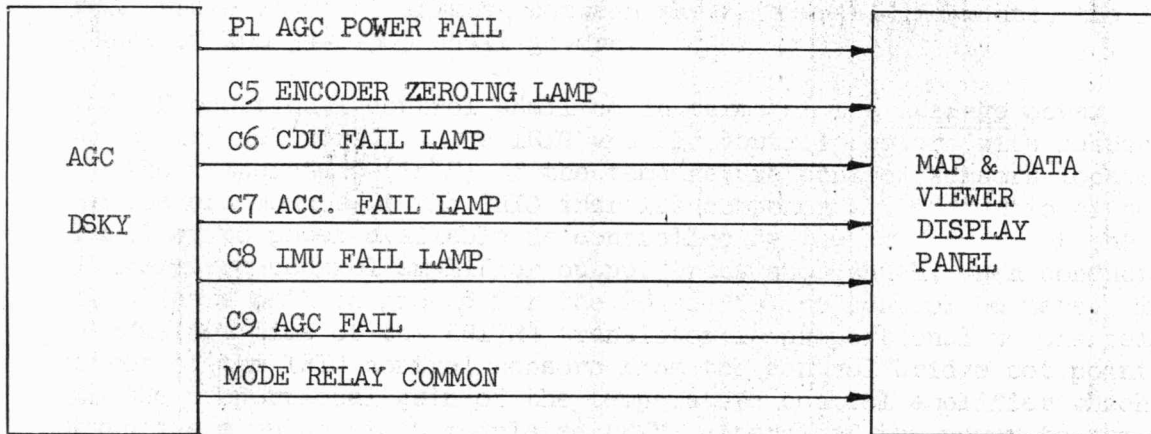
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PRELIMINARY AGC INTERFACE SPECIFICATION

By J. Kernan

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XII. (AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS, CONT'D.)



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AGC DSKY - OTHER SUBSYSTEMS INTERFACE SCHEMATIC

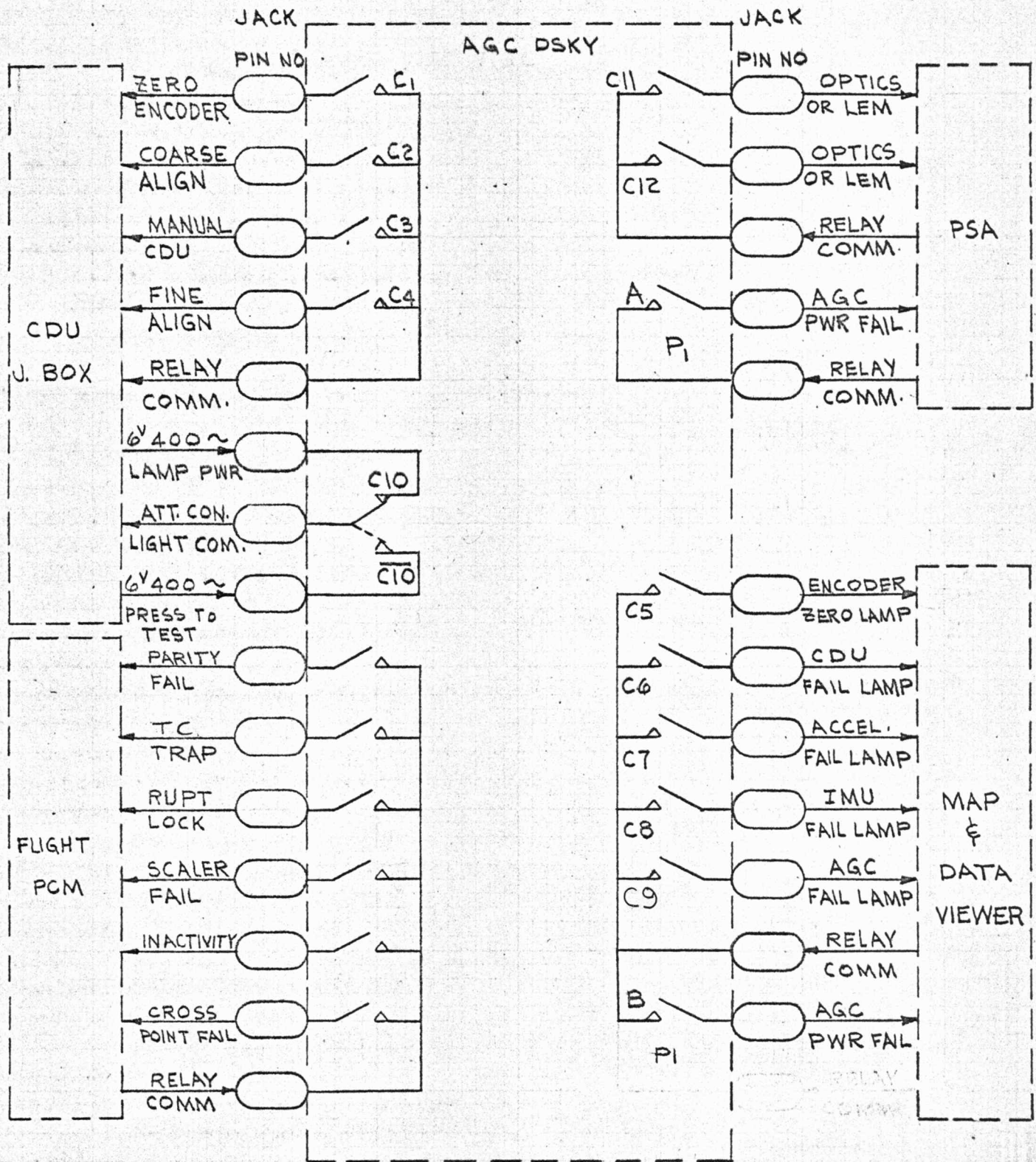


FIGURE XII-2

AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN, AND HOW OFTEN	AVAILABLE (U) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS								LINE DELAY			
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TUDE	I	PULSE WIDTH	RISE TIME	FALL TIME	f				
<u>CDU J. BOX</u> 1. IMU MODE COMMANDS (C1-C4) + RELAY COMM.	O	mode relays in CDU	initiated by AGC program thru relay bit out- puts to DSKY		Command guidance system: C1 - zero encoder C2 - Coarse Align C3 - manual CDU C4 - Fine align				0 OR 28 ^v dc	dc level				5				28 ^v dc								
2. ATTITUDE CONTROL LIGHT COMMAND	O	Attitude control light in IMU control panel	1) when in atti- tude control mode 2) when "press to test" switch is activated		1) Indicate attitude control mode 2) Test lamp opera- tion			0 OR 6V	ac level				1				6V rms								400 cps	
3. 6V 400 cps LAMP POWER	I	PSA	continuous		indicator lamp power			6V ac	ac level				1				6V rms								400 cps	
4. 6V 400 cps PRESS TO TEST	I	PSA	continuous		test indicator lamp operation			6V ac	ac level				1				6V rms								400 cps	
<u>FLIGHT PCM</u> AGC ALARMS + RELAY COMM.	O	word assembler in FLIGHT PCM	When one of failures listed in the inter- face diagram is present		Display alarm on main panel and telemetry failure bit to ground station			0 OR 28 ^v dc	dc level				7				28 ^v dc									
<u>PSA</u> 1. OPTICS (OR LEM) CONTROL RELAYS C1 AND C2 + RELAY COMM.	O	ops cs electronics in PSA	When mode is commanded by AGC		Command optics (OR LEM) to modes (Not defined as yet)			0 OR 28 ^v dc	dc level				3				28V ac									
2. CONTACT "A" OF "D" RELAY + RELAY COMM.	O	"OR" circuit in PSA	Loss of +13V or +3V power or AGC 28 ^v dc		To generate "ERROR DETECT" indication on g/n. and main panel								2													

CHART 6 AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS		AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN
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AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS

SIGNAL DESIGNATION (NAME & ABBREVIATION)	INPUT (I) OR OUTPUT (O)	ORIGIN OR DESTINATION	INITIATED HOW, WHEN AND HOW OFTEN	AVAILABLE (U) HOW LONG	USAGE OF INPUT OR RESPONSE CAUSED BY OUTPUT	EFFECT OF FAILURE TO ACCEPT INPUT OR SUPPLY OUTPUT AT REQUIRED RATE	QUANTITY REPRESENTED			PHYSICAL FORM	PHYSICAL QUANTIZATION			NO OF LINES	SIGNAL CHARACTERISTICS										
							ACCURACY	RESOLUTION	RANGE		ACCURACY	RESOLUTION	RANGE		TYPE ELEMENT	Z	AMPLI- TITUDE	I	PULSE WIDTH	RISE TIME	FALL TIME	LINE DELAY			
MAP AND DATA VIEWER 1. PROGRAM INITIATED ALARMS (5-5) + RELAY COMM	0	Caution lights in map and data viewer panel	When one of the failures listed in interface diagram occurs		display failure indication on map and data viewer panel					dc level			0 0E 28Vdc	6			28V dc								
	2. CONTACT "B" OF PI RELAY + common	0	"+3V or +13V FAILURE" indication in m.f.d.v. panel "AGC Power FAILER" indi- cation on MAIN PANEL	Loss of +3V or +13V AGC POWER		Indicate loss of +3V or +13V as listed in column 3				dc level			0 0E 28Vdc	2			28V dc								

CHART 6 AGC DSKY INTERFACE WITH OTHER SUBSYSTEMS		AC SPARK PLUG DIVISION GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN
SCALE	T.W.D.	

PRELIMINARY AGC SPECIFICATION

By
J. Kernan

Date

1.) AGC DSKY INTERFACE WITH THE CDU J-BOX

Ref: AGC4 In-Out Appendix

The AGC DSKY interface with the CDU J-Box consists of the IMU mode commands K1, K2, K3, K4 and the attitude control light command. The K1 through K4 relays are controlled by C1 through C4 contacts in the DSKY. The attitude control light command is controlled by the C10 contact. When the attitude control mode is commanded, the C10 output is connected to the 6V 400 cps lamp power input. When the attitude control mode is not commanded, the 6V 400 cps press to test input (C10) is connected to the attitude control light command.

2.) AGC DSKY INTERFACE WITH FLIGHT PCM

Ref: AGC4 Memo #5

The AGC DSKY displays the six failure indications shown on the interface diagram and also sends them to the flight PCM where they are sampled once per second.

A description of the failure modes is given in Section IX which covers the Display and Control interface:

3.) AGC DSKY INTERFACE WITH THE MAP AND DATA VIEWER PANEL

The C5 through C9 contacts in the AGC DSKY transmit the program generated failure indications as shown in the interface diagram. These failure indications are displayed as caution lights in the map and data viewer panel.

The B contact of the power failure relay in the AGC DSKY (P1), send an AGC +3V or +13V failure indication at the map and data viewer panel and the computer power supply failure at the main panel.

4.) AGC DSKY INTERFACE WITH PSA

Ref: AGC 4 Memo #5

The AGC DSKY interface with the PSA consists of the C11 and C12 mode relays for the optics or LEM control and contact A of P1. The mode contacts are sufficiently explained by the interface chart.

Contact A of P1 indicates to the "or" circuitry in the PSA that a failure is present. This input is used to generate an "error detect" at the map and data viewer panel and at the main panel.

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