1. GENERAL:
A. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED
BY MIL-D-70327.
B. UNITS SHALL MEET THE REQUIREMENTS OF MIL-S-19500 EXCEPT AS,
AND IN ADDITION TO THE REQUIREMENTS SPECIFIED HEREIN.
C. SUPPLIER SHALL CONFORM TO THE QUALITY ASSURANCE PROVISIONS
CONTAINED IN ND 1002248, CLMRS 2
D. MARKING: UNITS SHALL BE MARKED IN ACCORDANCE WITH
ND 100219 WITH THE MANUFACTURER'S IDENTIFICATION, DATE
CODE, DIFFUSION SUB-Lot CODE, KEYING STRIPE, *COLOR OPTION*,
BLACK OR WHITE. THE NUMBER 321. THE BACK OF THE PACKAGE MAY BE
UTILIZED FOR THE DIFFUSION SUB-Lot NUMBER.
E. PREPARATION FOR DELIVERY SHALL BE IN ACCORDANCE WITH
ND 1002215, CLASS 2, CODE 2.
1. MARKING OF SHIPPING CONTAINERS SHALL CONFORM TO THE
MARKING OF UNIT AND INTERMEDIATE PACKAGES AND THE
METHODS OF MARKING AS SPECIFIED IN ND 1002215.
F. THE SHIPMENT LOTS, MADE UP OF UNITS AS SPECIFIED BY THIS
DRAWING, MUST MEET THE REQUIREMENTS OF ND 1002248, WHEN
PROCESSED AS SPECIFIED IN ND 1003248, PERFORMED AT THE
BUYERS PLANT. LOTS OR SUBLOTS REJECTED BY THE CRITERIA OF PARA.4.3
OF ND 1015404, NEGOTIATION MAY BE CHANGED DURING THE
IMPLEMENTATION OF ND 1015404. ON =
2. ACCEPTANCE AND INSPECTION: QUALITY DEMONSTRATION PER TABLES | AND II
A. DEFINITIONS:
1. A SHIPMENT LOT IS DEFINED AS A GROUP OF PARTS
ASSEMBLED FROM DIFFUSION SUB-LOTS AND DATE CODES WHICH
ARE SHIPPED AT ONE TIME WHICH HAVE BEEN FABRICATED IN
A SINGLE CONTINUOUS PRODUCTION RUN USING LIKE
MATERIALS WHICH ARE CONTROLLED USING A CONTROLLED
PROCESS. NO PROCESS CHANGES ARE AS CRITICAL BY
ND 1005404, NEGOTIATION MAY BE CHANGED DURING THE
FABRICATION OF A SHIPMENT LOT. MAXIMUM NUMBER OF UNITS SHIPPED IN A LOT SHALL BE 5,000. A MAXIMUM OF
100 DIFFUSION SUB-LOTS MAY BE USED TO ASSEMBLE ONE
SHIPMENT LOT. A SHIPMENT LOT MAY INCLUDE MORE THAN
ONE DATE CODE LOT.
2. A DIFFUSION SUB-Lot IS DEFINED AS A GROUP OF PARTS
FABRICATED FROM MATERIALS WHICH WERE PROCESSED THROUGH
DIFFUSION MIGRATION, ETCHING AND METALLIZATION AT ONE
TIME (A SINGLE BATCH). THIS SUB-Lot IDENTIFICATION
MUST BE MAINTAINED THROUGH SUBSEQUENT STAGES OF
ASSEMBLY AND TEST. A DIFFUSION SUB-Lot SHALL BE
SEALED WITH ONLY ONE DATE CODE.
3. A DATE CODE LOT IS DEFINED AS THOSE UNITS SEALED DURING
ONE WEEK.
B. TEST CONDITIONS:
1. THE TESTS AS DEFINED IN TABLES I & II SHALL BE PERFORMED BY
THE QUALITY CONTROL DEPARTMENT OF THE VENDOR.
2. UNLESS OTHERWISE SPECIFIED HEREIN ALL ELECTRICAL TESTS
MUST BE REFERENCED TO AN REFERENCE TEMPERATURE PLUS
0 DEGREES CENTIGRADE.
3. THE PRE-SEAL TEST PER TABLE I SHALL BE PERFORMED AFTER
THE FINAL PRODUCTION, INTERNAL INSPECTION AND
PRIOR TO SEALING.
PROCURE ONLY FROM APPROVED SOURCES LISTED IN ND 1002248 FOR THIS DRAWING.
2. LEAD DIMENSIONS: THE PARTS SUPPLIED IN ANY SHIPMENT LOT MUST BE UNIFORM WITH RESPECT TO LEAD DIMENSIONS. THE LEAD THICKNESS SHALL BE WITHIN ±0.0005 INCHES OF A NOMINAL VALUE TO BE SPECIFIED BY THE VENDOR. THE LEAD WIDTH SHALL BE WITHIN ±0.001 INCHES OF A NOMINAL VALUE ALSO TO BE SUPPLIED. THE NOMINAL VALUES FOR EACH SHIPMENT LOT WILL BE SUPPLIED WITH THE APPLICABLE SHIPMENT.

3. DESIGN:
   A. ABSOLUTE MAXIMUM RATINGS AT 25°C AMBIENT:
      1) VOLTAGE TO PIN 10: PLUS 10.0 VOLTS WITH RESPECT TO PIN 5.
      2) VOLTAGE APPLIED TO ANY INPUT PIN PLUS OR MINUS 4 VOLTS WITH RESPECT TO PIN 5.
      3) THERMAL RESISTANCE, JUNCTION-CASE: (\(\theta_{jc}\)): 200°C/WATT.
      4) THERMAL RESISTANCE, JUNCTION-AMBIENT: (\(\theta_{ja}\)): 500°C/WATT.
   B. TEMPERATURE:
      1) TEMPERATURE RANGE, JUNCTION, OPERATING: -55°C TO +125°C.
      2) TEMPERATURE RANGE, JUNCTION, STORAGE: -65°C TO +150°C.
      3) TEMPERATURE, SOLDERING LEADS: +250°C (1 MINUTE MAX).
   C. CONSTRUCTION:
      1) SEMICONDUCTOR: SILICON, NPN.
      2) ENCLOSURE: A HERMETICALLY SEALED PACKAGE ELECTRICALLY ISOLATED FROM POWER OR GROUND, THE DIMENSIONS OF WHICH MEET THE REQUIREMENTS OF FIGURE 1 AND PARAGRAPH 2.E.
      3) LEADS:
         LEAD MATERIAL SHALL BE IN ACCORDANCE WITH NASA DOCUMENT PS 105402 WITH THE FOLLOWING EXCEPTIONS:
         GOLD PLATE SHALL BE A MINIMUM OF 100 AND A MAXIMUM OF 200 MICRO INCHES. THE NICKEL STRIKE UNDER THE GOLD SHALL BE OPTIONAL BUT IF USED SHALL BE A MAXIMUM OF 100 MICRO INCHES. CERTIFICATE OF COMPLIANCE FOR LEAD MATERIAL SHALL ACCOMPANY EACH LOT SHIPPED.
      4) TEST METHODS: (REF. MIL-STD-750 WITH EXCEPTIONS NOTED BELOW).
   A. AVERAGE PROPAGATION DELAY (\(\tau_{p}\)): MEASUREMENTS SHALL BE PERFORMED ON EACH INPUT USING TEST CIRCUIT SPECIFIED IN FIGURE 2 MADE UP OF ACCEPTABLE UNITS WHERE \(\tau_{p} = \left(\tau_{1} + \tau_{2}\right)/2\). VOLTAGE V, A 10% DURING TEST. ALL UNUSED BASES SHALL BE GROUNDED.

**REPLACES REV(C) WITH CHANGES**
B. VISUAL AND MECHANICAL EXTERNAL EXAMINATION UNDER 10X AND 80X MAGNIFICATION:

Markings shall be legible. The case finish shall have no flaking, spattering, chipping or holes. The glass or ceramic shall have no seal impairing cracks. Re-entrance at the glass, ceramic or solder seal shall not extend to over 60% of the seal width. No foreign matter shall be in or on the seal interface. Leads shall be free from kinks and nicks and shall maintain a uniform thickness within lead specifications. The units shall comply with the specified lead material requirement. Lead section (a) may be cut from the lead preform and shall not be subjected to physical examination. No body paint shall be on the leads or package seal area.

C. PRE SEAL VISUAL INSPECTION: The preseal visual inspection shall be performed using the rejection criteria of [ISO 1002257].

The diffusion sublot shall be utilized for sampling specified in Table I. Data shall accompany each shipment covering the number of sub-lots tested, the number of units that failed from each sub-lot, the cause of failure, and the number of times each sub-lot was resubmitted to Table I test.

<table>
<thead>
<tr>
<th>TEST</th>
<th>TEST CONDITIONS</th>
<th>DIFFUSION SUB-LOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VISUAL INTERNAL INSPECTION</td>
<td>SEE NOTE 2.C.(4) AND A.C.</td>
<td>LTIP* = 7 MAX ACC NO. = 1</td>
</tr>
</tbody>
</table>

Note: See Table I for details.

### Table I

<table>
<thead>
<tr>
<th>Visual Internal Inspection Test</th>
<th>Test Conditions</th>
<th>Diffusion Sub-Lot</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX BODY DIMENSIONS INCLUDE ALL GLASS CLING, BODY SWL. TO BE SYMMETRICAL ABOUT 1/2 IN. AND 1/2 OF LEADS TO BE SYMMETRICAL WITHIN .005 OF 1/2 IN. OF LEADS TO BE MEASURED WITHIN .005 OF PACKAGE BODY.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEE PARAGRAPH 2.C.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table II

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Conditions</th>
<th>Diffusion Sub-Lot</th>
</tr>
</thead>
<tbody>
<tr>
<td>VISUAL INTERNAL INSPECTION</td>
<td>SEE NOTE 2.C.(4) AND A.C.</td>
<td>LTIP* = 7 MAX ACC NO. = 1</td>
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</table>

Note: See Table II for details.

### Table III

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Conditions</th>
<th>Diffusion Sub-Lot</th>
</tr>
</thead>
<tbody>
<tr>
<td>VISUAL INTERNAL INSPECTION</td>
<td>SEE NOTE 2.C.(4) AND A.C.</td>
<td>LTIP* = 7 MAX ACC NO. = 1</td>
</tr>
</tbody>
</table>

Note: See Table III for details.
### Table II

**ACCESSION INSPECTION**

<table>
<thead>
<tr>
<th>TEST NUMBER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUBGROUP 1</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VISUAL AND MECHANICAL EXAMINATION</td>
<td>METHOD 2079</td>
<td>SEE PARAGRAPH (4.B)</td>
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</tr>
<tr>
<td><strong>SUBGROUP 2</strong></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>BASE CURRENT</td>
<td>PIN 2.6</td>
<td>PIN 5.7</td>
<td>PIN 5</td>
<td>PIN 6.8</td>
</tr>
<tr>
<td></td>
<td>$I_B$</td>
<td>+870.2mV</td>
<td>+1800.2mV</td>
<td>+870.2mV</td>
</tr>
<tr>
<td>BASE CURRENT</td>
<td>PIN 2.6</td>
<td>PIN 5.7</td>
<td>PIN 5</td>
<td>PIN 6.8</td>
</tr>
<tr>
<td></td>
<td>$I_B$</td>
<td>+1800.1mV</td>
<td>+1800.1mV</td>
<td>+1800.1mV</td>
</tr>
<tr>
<td>OUTPUT VOLT PIN 1.9</td>
<td>$V_O$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>OUTPUT VOLT PIN 1.9</td>
<td>$V_O$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>SAT VOLT PIN 1.9</td>
<td>$V_S$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>SAT VOLT PIN 1.9</td>
<td>$V_S$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>COLLECTOR-EMITTER</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>THRESHOLD CURRENT</td>
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<tr>
<td><strong>SUBGROUP 3</strong></td>
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<td></td>
</tr>
<tr>
<td>COLLECT CUTOFF CURRENT</td>
<td>$I_{cut}$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>EMITTER CUTOFF CURRENT</td>
<td>$I_{em}$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>COLLECT CUTOFF CURRENT</td>
<td>$I_{cut}$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>INTERFACE TEST</td>
<td>$I_T$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>50V TO +10V</td>
</tr>
<tr>
<td>INTERFACE TEST</td>
<td>$I_T$</td>
<td>OPEN</td>
<td>OPEN</td>
<td>50V TO +10V</td>
</tr>
<tr>
<td>COLLECTOR RESISTANCE</td>
<td>$R_C$</td>
<td>BETWEEN PINS 10 AND 1.9</td>
<td>MEASUREMENT CURRENT = 1 mA</td>
<td>2.7</td>
</tr>
<tr>
<td>D.C. CURRENT GAIN</td>
<td>D.C.</td>
<td>1 mA</td>
<td>NCE = 0.5V ALL TRANSISTORS</td>
<td>30</td>
</tr>
</tbody>
</table>

* LTDP PER MIL-S-19500C, TABLE IV

**DIMENSIONS ARE IN INCHES**

<table>
<thead>
<tr>
<th>MATERIAL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAPACITOR VALUES ARE IN µF</td>
<td></td>
</tr>
<tr>
<td>RESISTOR VALUES ARE IN OHMS</td>
<td></td>
</tr>
<tr>
<td>TOLERANCES ON FRACTIONS DECADES ANGLES</td>
<td></td>
</tr>
<tr>
<td>DO NOT SCALE THIS DRAWING</td>
<td></td>
</tr>
</tbody>
</table>

**MATERIALS LIST**

- UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- CAPACITOR VALUES ARE IN µF
- RESISTOR VALUES ARE IN OHMS
- TOLERANCES ON FRACTIONS DECADES ANGLES
- DO NOT SCALE THIS DRAWING

**DUAL NOR GATE**

**FLAT PACK**

**INSTRUMENTATION LAB**

**MANNEED SPACECRAFT CENTER**

**HOUSTON, TEXAS**

**CODE IDENT No.

**SPECIFICATION CONTROL DRAWING**

**DRAWING NO.**

**MATERIAL**

**APPROVED**

**SHEET 4 OF 5**

---

**NOTICE**

- WHEN GOVERNMENT DRAWINGS, SPECIFICATIONS, OR OTHER DATA RELATED TO FEDERAL PROCUREMENT OPERATIONS FOR UNITED STATES GOVERNMENT
- REVISIONS ARE AUTHORIZED ONLY PER TORR 2540
- ANY PATENTED INVENTION THAT MAY IN ANY WAY BE RELATED THERETO
- REVISED PER T00 2087
- REVISED PER TORR 27100

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**REPLACES REV(C) WITH CHANGES**

**NEXT ASSY USED ON**

**APPLICATION**

---

**MASTER**

---

**D**

---

**E**

---

**F**

---
**FIGURE 2**

AVERAGE PROPAGATION DELAY

**FIGURE 3**

TEST CIRCUIT - POWER BURN IN

D. REPLACES REV(C) WITH CHANGES