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LIT-77-1001

**Space Shuttle  
Advanced System/4 Pi  
Prototype Input/Output Processor (IOP)**

**Functional Description**

IBM

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# Space Shuttle Advanced System/4 Pi Prototype Input/Output Processor (IOP)

## Functional Description

Prepared for

Rockwell International Corporation  
Space Division  
12214 Lakewood Blvd.  
Downey, CA 90241

25 October 1974

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# TABLE OF CONTENTS

Section		Page
1	INTRODUCTION.....	1-1
1.1	OVERVIEW.....	1-1
1.1.1	Instructions .....	1-3
1.1.2	Data Bus Operating Modes .....	1-3
1.1.3	Fault Detection .....	1-4
1.1.4	Packaging.....	1-5
1.2	OPERATING PRINCIPLES.....	1-5
2	FUNCTIONAL IMPLEMENTATION .....	2-1
2.1	INTRODUCTION.....	2-1
2.1.1	Time Sharing .....	2-1
2.1.2	Operation of Processor Elements .....	2-1
2.1.3	Example Program Execution .....	2-5
2.2	PROGRAM CONTROL INPUTS AND OUTPUTS .....	2-5
2.2.1	PCI/PCO Command Word Format .....	2-5
2.2.2	PCO Data Words .....	2-9
2.2.3	PCI Data Words .....	2-13
2.3	STATUS AND INTERRUPT REGISTERS .....	2-17
2.4	MASTER SEQUENCE CONTROLLER (MSC) .....	2-20
2.4.1	MSC Programmable Registers .....	2-21
2.4.2	MSC Operation .....	2-21
2.4.3	MSC Instructions .....	2-24
2.4.4	MSC Local Store and Status Register .....	2-27
2.5	BUS CONTROL ELEMENT .....	2-28
2.5.1	Programmable Registers .....	2-29
2.5.2	BCE Operation .....	2-29

# Table of Contents (cont)

Section		Page
2.5.3	BCE Instructions .....	2-30
2.5.4	BCE Local Store and Status Register .....	2-33
2.6	FAULT HANDLING .....	2-33
2.6.1	Fault Detection .....	2-34
2.6.2	Fault Identification .....	2-41
2.6.3	Reconfiguration .....	2-41
2.7	INITIAL PROGRAM LOADING .....	2-43
2.7.1	GPC Mode Control .....	2-40
2.7.2	Computer Initial Program Load .....	2-40
3	SYSTEM ELEMENTS .....	3-1
3.1	INTRODUCTION .....	3-1
3.2	MIA AND BUFFER .....	3-4
3.2.1	Serial Data Bus Modulation Scheme .....	3-5
3.2.2	Overview of MIA Operations .....	3-6
3.2.3	IOP/MIA Interface and Timing .....	3-9
3.2.4	Individual Circuits .....	3-9
3.2.5	MIA Buffer .....	3-16
3.3	CONTROL MONITOR .....	3-17
3.4	CHANNEL CONTROL .....	3-22
3.4.1	Channel Control Elements .....	3-22
3.4.2	PCI/PCO Sequence .....	3-25
3.4.3	DMA Sequence .....	3-27
3.5	DMA QUEUE .....	3-32
3.5.1	Queue Format .....	3-32
3.5.2	Queue Operation .....	3-34
3.5.3	Queue Control Field .....	3-35
3.5.4	Queue Microdecode .....	3-35

# Table of Contents (cont)

Section		Page
3.6	PROCESSOR ELEMENTS. ....	3-37
3.6.1	Microstore and Timing . . . . .	3-39
3.6.2	Local Store . . . . .	3-44
3.6.3	Data Flow Element . . . . .	3-47
3.7	REDUNDANCY MANAGEMENT (RM) HARDWARE LOGIC . . . .	3-49
3.7.1	Noncooperative Elements . . . . .	3-49
3.7.2	Cooperative Hardware/Firmware Elements . . . . .	3-53
3.8	POWER SUPPLIES . . . . .	3-55
3.8.1	General . . . . .	3-55
3.8.2	Functional Description . . . . .	3-57
3.8.3	Power Supply Sequencing . . . . .	3-62
3.9	IOP MEMORY . . . . .	3-66
4	IOP PACKAGING (PROTOTYPE) . . . . .	4-1
4.1	IOP HOUSING . . . . .	4-1
4.2	MULTILAYER INTERCONNECTION BOARDS . . . . .	4-1
4.2.1	Tape Cable Assembly Page . . . . .	4-3
4.2.2	IOP Backpanel . . . . .	4-3
4.2.3	Core Storage Page . . . . .	4-4
4.3	PAGE NOMENCLATURE, LOCATION, AND CIRCUIT POPULATION . . . . .	4-5
4.4	ASSEMBLY PACKAGING . . . . .	4-5
4.4.1	IOP Assembly . . . . .	4-5
4.4.2	Main Memory Assembly . . . . .	4-5
4.4.3	Power Supply Assembly . . . . .	4-5
4.5	STRUCTURE DESIGN . . . . .	4-7
4.6	IOP/CPU INTERCONNECTIONS . . . . .	4-7

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# Table of Contents (cont)

Section		Page
5	IOP TEST EQUIPMENT.....	5-1
5.1	COMPUTER/COMPUTER TESTER.....	5-1
5.1.1	Panel Layout.....	5-7
5.1.2	Display Indicators.....	5-8
5.1.3	CPU Controls.....	5-8
5.1.4	Mode Select.....	5-9
5.1.5	Operation.....	5-10
5.1.6	Error Indicators.....	5-11
5.1.7	Inhibit Switches.....	5-11
5.1.8	Status Indicators.....	5-12
5.1.9	Discrete Inputs.....	5-13
5.2	IOP TESTER.....	5-13
5.2.1	AP-101 Tester Interface.....	5-13
5.2.2	MIA Box Interface.....	5-13
5.2.3	Tester-to-IOP Interface.....	5-13
5.2.4	Tester - IOP Controls.....	5-17
5.3	MAGNETIC TAPE TRANSPORT.....	5-18
5.4	LINE PRINTER.....	5-18
6	DIFFERENCES BETWEEN IOP DEVELOPMENT AND PROTOTYPE MODELS.....	6-1

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# LIST OF ILLUSTRATIONS

Figure		Page
1-1	Basic Five GPC Shuttle Data Processing System . . . . .	1-2
1-2	Example of Command and Listen Modes . . . . .	1-4
1-3	Input/Output Processor Functional Block Diagram . . . . .	1-6
2-1	IOP Functional Block Diagram . . . . .	2-2
2-2	Simplified IOP Organization . . . . .	2-3
2-3	Microcycle Information Flow . . . . .	2-3
2-4	Typical IOP Instruction Timing . . . . .	2-6
2-5	Basic MSC Instructions Formats . . . . .	2-26
2-6	BCE Instruction Formats . . . . .	2-31
2-7	Functional Summary of Fault Detection . . . . .	2-36
2-8	Cockpit/GPC/MMU/MCDS Functional Interface Summary . . . . .	2-44
2-9	IPL Power-On Sequencing . . . . .	2-47
3-1	IOP Elements . . . . .	3-2
3-2	Detailed System Diagram . . . . .	3-3
3-3	Biphase-Level Manchester II Code Modulation Scheme . . . . .	3-5
3-4	Sample Manchester II Code Bit Combinations . . . . .	3-6
3-5	Command and Data Word Sync . . . . .	3-7
3-6	MIA Block Functional Block Diagram . . . . .	3-8
3-7	IOP/MIA Interface and Timing Signals . . . . .	3-12
3-8	MIA Receiving Circuits Functional Block Diagram . . . . .	3-14
3-9	MIA Receiver Timing . . . . .	3-15
3-10	MIA Buffer Functional Block Diagram . . . . .	3-18
3-11	Control Monitor Element Functional Diagram . . . . .	3-20
3-12	Channel Control and Interfaces . . . . .	3-24
3-13	PCI/PCO Sequence . . . . .	3-26
3-14	DMA Input Sequence . . . . .	3-28
3-15	DMA Output Sequence . . . . .	3-29
3-16	Channel Control Timing . . . . .	3-30
3-17	DMA Queue Functional Diagram . . . . .	3-34
3-18	Processor Elements Data Paths . . . . .	3-38
3-19	IOP Timing Diagram . . . . .	3-40
3-20	Microstore and Timing . . . . .	3-41
3-21	Microprogram Control of Data Flow . . . . .	3-43
3-22	Microprogram Control of Actions and Micro Branching . . . . .	3-43
3-23	Local Store Data Paths . . . . .	3-45

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# List of Illustrations (cont)

Figure		Page
3-24	Local Store Timing .....	3-46
3-25	Data Flow Timing .....	3-48
3-26	Redundancy Management Hardware Logic Diagram.....	3-50
3-27	IOP Power Supply Block Diagram .....	3-56
3-28	Input Filter and Converter .....	3-57
3-29	Converter Driver Circuit .....	3-59
3-30	+5-V Controller Block Diagram .....	3-60
3-31	Internal Voltage Block Diagram .....	3-61
3-32	Power Supply On/Off Timing Diagram .....	3-63
3-33	Power Up/Down Controls.....	3-65
3-34	IOP Memory Block Diagram 24K x 36 Bits .....	3-67
4-1	Exploded View of IOP .....	4-2
4-2	Basic IOP Page .....	4-2
4-3	Tape Cable Assembly .....	4-4
4-4	Main Memory Assembly — 24K, 36-Bit .....	4-7
4-5	GPC Prototype Model Interface Configuration .....	4-8
5-1	IOP and Test Equipment Interface .....	5-2
5-2	IOP Tester Interface Data Bus .....	5-2
5-3	AP-101 Test Set.....	5-4
5-4	IOP Test Set .....	5-4
5-5	Computer Tester Block Diagram.....	5-5
5-6	CPU Tester Lower Panel.....	5-6
5-7	CPU Tester Upper Panel.....	5-6
5-8	IOP Tester Block Diagram.....	5-14
5-9	IOP/AGE Interface .....	5-15
5-10	IOP Controls.....	5-17
5-11	IOP Tester Upper Panel .....	5-17
5-12	IOP Tester Lower Panel .....	5-18
6-1	IOP Development Model Packaging .....	6-1
6-2	Logic Allocation for IOP Development Model .....	6-2

# LIST OF TABLES

Table		Page
1-1	IOP Slot Timing . . . . .	1-7
2-1	Example MSC Program . . . . .	2-8
2-2	Example BCE Programs . . . . .	2-9
2-3	PCI and PCO Instructions . . . . .	2-10
2-4	Redundancy Management Status Register . . . . .	2-18
2-5	MSC Characteristics . . . . .	2-20
2-6	MSC Instructions . . . . .	2-25
2-7	MSC Local Store Usage . . . . .	2-27
2-8	MSC Status Register . . . . .	2-27
2-9	BCE Characteristics . . . . .	2-28
2-10	BCE Instruction Summary . . . . .	2-32
2-11	BCE Local Store Register Allocations . . . . .	2-34
2-12	BCE Status Register . . . . .	2-35
2-13	IOP Interrupt Detected Errors . . . . .	2-37
2-14	MSC Firmware Detected Errors . . . . .	2-38
2-15	BCE Firmware Detected Errors . . . . .	2-39
2-16	GCP and DEU Load Procedure . . . . .	2-45
2-17	IOP/IPL Microroutine Sequence . . . . .	2-46
3-1	Processor Elements to MIA Signals . . . . .	3-10
3-2	MIA to Processor Elements Signals . . . . .	3-11
3-3	Control Monitor Reset Logic Summary . . . . .	3-23
3-4	IOP/CPU Interface Signal Descriptions . . . . .	3-31
3-5	Queue Register Format . . . . .	3-33
3-6	Micro Decoding by DMA Queue . . . . .	3-36
3-7	Micro Instruction Field Description . . . . .	3-42
3-8	IOP Memory Performance Characteristics . . . . .	3-68
4-1	Page Nomenclature, Location and Circuit Population . . . . .	4-6
4-2	CPU/IOP Connector Pin Functions . . . . .	4-9
5-1	Computer Tester Characteristics . . . . .	5-3
5-2	Mode Select Switch Functions . . . . .	5-9
5-3	Data Format for AGE Data B00-53 (54 Lines) IOP→AGE . . . . .	5-15
6-1	Packaging Differences Between IOP Configurations . . . . .	6-3
6-2	Hardware Limitations of Development Model IOP . . . . .	6-3

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# GLOSSARY

ACC	Accumulator
AGE	Aerospace Ground Equipment
ALU	Arithmetic Logical Unit
BA	Boundary Alignment
BASE	Base Register
BCE	Bus Control Element
BITE	Built-In Test Equipment
BTO	Block Timeout
BU	Branch Unconditional
C	Control
CC	Channel Control
CC	Cross-Couple
CCR	Cross-Couple Register
CM	Control Monitor
CMD	Command
CP	Clock Pulse
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DC	Direct Current
DEU	Display Electronics Unit
DF	Data Flow
DI	Discrete Input
DIN	Direct-In Instruction
DIP	Dual In-Line Package
DISP	Displacement
DLY	Delay

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DMA	Direct Memory Access
DO	Discrete Output
DU	Display Unit
ECR	External Call Register
EIU	Engine Interface Unit
EMI	Electromagnetic Interference
EP/MCM	Extended Performance/Modular Core Memory
EMU	Extended Memory Unit
ETI	Elapsed Time Indicator
FCOS	Flight Control Operations System
FIFO	First-In/First-Out
ft	Foot or Feet
FTP	Functional Test Program
FW	Fullword
GPC	General-Purpose Computer
GSE	Ground Support Equipment
HW	Halfword
IMM	Immediate
IMS	Inhibit Main Store
IMU	Inertial Measurement Unit
in	Inch or Inches
I/O	Input/Output
IOP	Input/Output Processor
IOPIMS	Input/Output Processor Inhibit Main Store
IPL	Initial Program Load
IPLC	Initial Program Load Complete
ITO	Initial Timeout
IUAR	Interface Unit Address Register
K	1024
KB	Keyboard
lb	Pound(s)

LBR	Load Base Register
LC	Inductor-Capacitor
LCC	Load Cross-Couple Register
LRU	Line-Replaceable Unit
LS	Local Store
LSB	Least Significant Bit
LSI	Large-Scale Integration
LTOR	Load Timeout Register
MA	Micro Architecture
MAL	Malfunction
MCDS	Multipurpose CRD Display Subsystem
MDM	Modulator Demodulator
MHz	MegaHertz ( $1 \times 10^6$ cycles)
MIA	Multiplexer Interface Adapter
MB	Multilayer Interconnection Board
MM	Mass Memory
MMU	Mass Memory Unit
MPOR	Master Power-On Reset
ms	Millisecond(s)
MSB	Most Significant Bit
MSC	Master Sequence Controller
MSI	Medium Scale Integration
MTO	Maximum Timeout Register
MTS	Microprogram Test System
NOP	No Operation
OCC	Overcurrent Comparator
OP	Operation
OVC	Overvoltage Comparator
PC	Program Counter
PCI	Program Control Input
PCO	Program Control Output



pF	Pico Farad(s)
POI	Power On/Off Interrupt
POR	Power On/Off Reset
PROM	Programmable Read-Only Memory
PS	Power Supply
PSW	Program Status Word
RAW	Repeat until All BCEs are Waiting
RC	Resistor-capacitor
RDL	Receive Data Long (Format)
RDS	Receive Data Short (Format)
RFI	Radio Frequency Interference
RIB	Reset Indicator Bit
RM	Redundancy Management
ROM	Read-Only Memory
ROS	Read-Only Storage
ROSAR	Read-Only Storage Address Register
ROSDR	Read-Only Storage Data Register
SAR	Storage Address Register
SC	Store Complete
S/D	Skeleton/Dynamic
SDR	Series Dissipating Regulator
SIB	Set Indicator Bit
SQ	Super Queue
SSC	Store Status and Clear
SSW	Store Status and Wait
STP	Self-Test Program

SVC .....	Supervisor Call
TDL .....	Transmit Data Long (Format)
TDS .....	Transmit Data Short (Format)
T/F .....	True/False
TO .....	Timeout
T/R .....	Transmit/Receive
TTL .....	Transistor-Transistor Logic
V .....	Volt(s)
W .....	Watt(s)
WAT .....	Wait
WR .....	Working Register
XMT .....	Transmitter
$\Omega$ .....	Ohm(s)
$\mu$ PC .....	Microprogram Counter

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## Section 1

### INTRODUCTION

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## Section 1

### INTRODUCTION

This manual describes the Input/Output Processor (IOP) Subsystem design. It provides functional hardware and software information. A programmer reference manual entitled "IOP Principles of Operation" is available. The IOP and Central Processing Unit (CPU) use IBM System/4 Pi components manufactured and packaged at IBM Owego, New York.

This manual is organized in five sections as follows:

1. Introduction
2. Functional Implementation — Describes the software-to-hardware relationship
3. System Elements — Describes hardware, timing, and signal flow details of the IOP design
4. IOP Packaging — Provides line-replaceable unit (LRU) packaging descriptions, and identifies replaceable subassemblies and connector pin assignments
5. Test Equipment — Provides interface and test and checkout capability information and summarizes test procedures

The IOP is an all-digital, programmable, time-shared processor that transmits and receives Shuttle Orbiter subsystems data under control of the CPU. The CPU processing functions are guidance, navigation and control, performance monitoring, and payload control management. The data processing involved is accomplished by five identical general-purpose computer (GPC) subsystems. Each GPC subsystem is comprised of a CPU and an IOP (Figure 1-1).

#### 1.1 OVERVIEW

The Shuttle Orbiter subsystems are connected to the IOP by 24 serial, 1-MHz data buses. Data bus-to-IOP interface is accomplished by 24 multiplexer interface adapters (MIA) located in each IOP. The MIAs convert Manchester II coded serial data words, received by the IOP, to the parallel format required by the CPU/IOP.



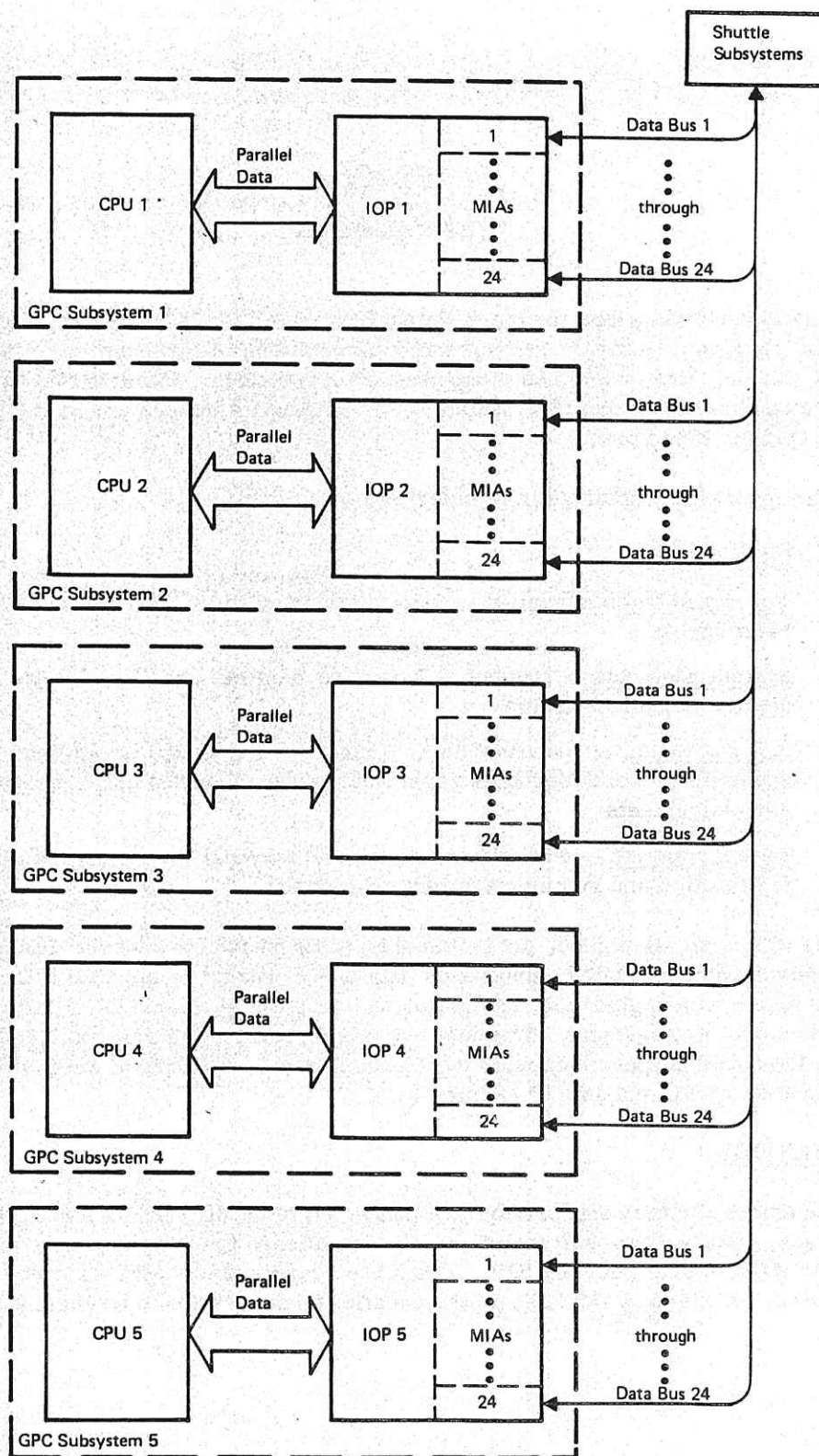


Figure 1-1. Basic Five GPC Shuttle Data Processing System



Conversely, the MIAs convert the CPU/IOP parallel word format (to be transmitted over the data buses) to the Manchester II coded serial data format. Also, the MIAs generate and check data parity used for transmission error detection.

The IOP handles the processing required to service the 24 data buses. An IOP buffers and controls input/output (I/O) operations for the CPU. The IOP is time-shared by the 24 data buses as determined by a fixed sequence timer. Data processing programs for the IOP (stored in main memory) are independent of CPU programs and have their own unique instruction set.

Functionally, the CPU and IOP share main memory. After an IOP program has been initiated by the CPU, a direct memory access (DMA) channel between the IOP and main memory is used to obtain the IOP program instructions required to fetch the output data or put away input data. This DMA technique provides common data storage to eliminate CPU-to-IOP I/O data transfers. However, the DMA technique produces CPU/IOP contention for main memory, thereby reducing CPU processing capacity.

### 1.1.1 INSTRUCTIONS

IOP and CPU instructions are defined by microcoding techniques. A read-only storage (ROS) is employed for controlling a fixed sequence of operations and internal data paths to be executed for each instruction. This provides an efficient and flexible technique to define the exact processing requirements for each IOP instruction.

### 1.1.2 DATA BUS OPERATING MODES

IOP data bus channel operating modes are

- Command
- Listen

In the Command mode, I/O data (to or from an interfacing Shuttle subsystem) will be processed. In the Listen mode, only input data will be processed. A Master Sequence Controller (MSC) is used to control all of the Bus Control Elements (BCEs) and to route data from one MIA channel to another through the IOP. Each MIA channel is controlled by its BCE.

Use of typical Command and Listen modes are illustrated in Figure 1-2. Note that avionics functions are triple redundant; i.e., three completely independent subsystems are designated. For example, redundant information received from each of three inertial measuring units (IMU) by each GPC should be the same. IMU 1 is assigned to and controlled by GPC 1; IMU 2 with GPC 2, etc. GPC 1 provides all command functions on the data bus associated with IMU 1, while GPC 2 and 3 monitor (listen).

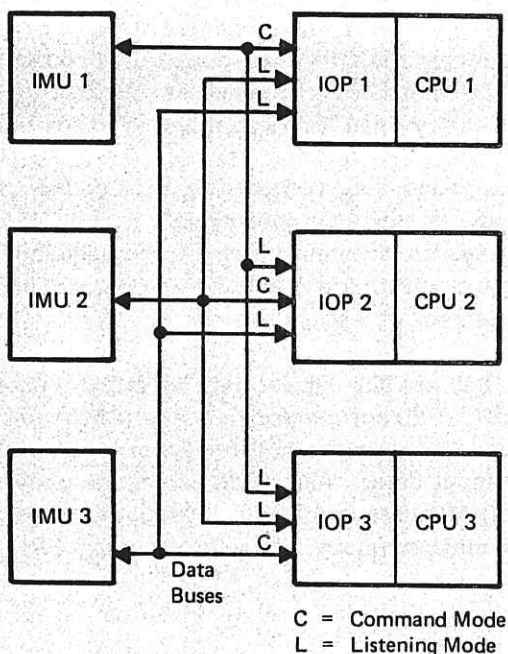


Figure 1-2. Example of Command and Listen Modes

GPCs 2 and 3 are connected in a similar manner with their respective systems. A malfunction in one system will be detected by the other two, and corrective action will be taken to eliminate the faulty unit from control.

### 1.1.3 FAULT DETECTION

Fault detection in the IOP is achieved by redundancy management (RM) software, programmed self-test, and built-in test equipment (BITE). These methods provide fail-safe data transfers on the MIA data channels. Since all critical functions are at least triple redundant at the subsystem level, an individual IOP failure will not affect the operation of the Shuttle Orbiter systems.

A Watchdog timer (BITE functional) is located in the RM hard logic. This timer is set and reset under program control. Should program control be lost, the Watchdog timer will time out, producing an IOP transmission termination, thereby failsafing the GPC subsystem. RM hard logic contains voting logic, so that good computers can force recognition of a failed computer. RM hard logic in each IOP receives four individual votes from the other computers while transmitting up to four votes of its own. An IOP RM hard logic that receives two or more votes, indicating that its operation is incorrect, actuates a failure latch, and any further MIA transmission is terminated. All transmission termination is under CPM software control via the termination control latches.

An IOP Self-Test program may be executed along with the background data processing program to detect IOP failures. Corrective action is taken by the program as required. Crew notification and Watchdog timer Time-Out are possible program actions.

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- CONCLUSIONS**

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## 1





**Figure 1-3. Input/Output Processor Block Diagram**

A single processor element is contained in the IOP. Except for local storage the IOP hardware is time-shared and functionally provides the 24 data bus control elements (BCE) and the master sequence controller (MSC). The MSC and BCE execute programs located in main memory to perform the desired I/O operations. (MSC and BCE instruction sets are summarized in Section 2.) The MSC controls the BCE, which in turn controls one of the 24 data buses. Time sharing of the IOP processor element is defined by the slot timer as defined in Table 1-1. Slot timing sequence for one IOP processor element is BCE test, MSC, BCE 1, BCE 2, BCE 3 MSC . . . . BCE 22, BCE 23, BCE 24 and repeat. The BCE test slot initiates individual self-test programs, which verify that the processor and BCE data flow are operating correctly.

Table 1-1

IOP SLOT TIMING

• Design Restriction	1 MSC every 3 slots preceded by odd BCE slot
• Slot Layout	24 BCE 1 BCE Test 8 MSC 33 Total
• Slot Time	0.500 $\mu$ s
• Cycle Time	$33 \times 0.500 = 16.5 \mu$ s
• MIA Word Transfer	28 bits at 1 MHz = 28 $\mu$ s
• Interword Gap	5 $\mu$ s
• MIA Slaved to 1-MHz Timing	
Interword Gap is set by IOP Cycle Time for Data Bus Outputs	

Figure 1-3, a simplified functional diagram of the IOP, shows the I/O data flow and major system elements. The primary functions of the major IOP elements are as follows:

- Control Monitor — Interfaces with the CPU to provide power on/off, master reset functions, MIA enable/inhibit, decode the PCI and PCO commands, control the I/O channel interface, handle system discretes, IOP interrupt to CPU, and controls the initial program load (IPL) sequence.
- Channel Control — Receives and transmits data over the main I/O channel
- Local Store — Contains the general registers associated with the MSC and with each BCE



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- The following example of IOP operation is a simplified description of how the IOP functions for an input data request from the CPU. This example uses MIA input processor BCE 1 with its transmitter and receiver enabled.

- 1-8

8. BCE 1 executes first instruction, which commands a system device to supply a data word over the MIA 1 data bus.
9. BCE 1's next instruction from main memory is to receive the data word. If more than one data word was required, the word count is part of the receive instruction.
10. MIA signals BCE 1 that data have been received.
11. BCE loads data in the main memory address specified in Step 4.
12. BCE 1's next instruction is to store its status register in main memory and enter the Wait state. Any error conditions are resolved by MSC and CPU programming.
13. MSC detects BCE Program completion and checks for errors. If no errors are present, the CPU is informed via MSC specified interrupt.
14. CPU accepts interrupt and processor input data.

1-9/1-10

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## Section 2.

### FUNCTIONAL IMPLEMENTATION

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## Section 2

### FUNCTIONAL IMPLEMENTATION

This section delineates the IOP system capabilities and describes the relationship between IOP system design and I/O programming. The topics covered in this section are:

- IOP program execution
- CPU control of the IOP by PCI/PCO commands
- MSC processor
- BCE processors
- IOP fault-detection capabilities
- Initial program loading.

#### 2.1 INTRODUCTION

##### 2.1.1 TIME SHARING

The functional components comprising the IOP are shown in Figure 2-1. Basic IOP operation centers around a fixed time sequence of operations determined by the slot timer, or "wheel," as shown in Figure 2-2. All BCEs and the MSC have dedicated general registers assigned in local store and share a common data flow. The MIA channels and the MSC are serviced in a very methodical fixed sequence using the local store. The IOP communicates with the CPU main memory (to fetch instructions and transfer data) in a completely asynchronous manner. The BCEs or MSC issue memory requests required from data flow during their slot times. These requests are stacked in DMA queue and are serviced in sequence by the channel control independent of the basic IOP processing operation.

##### 2.1.2 OPERATION OF PROCESSOR ELEMENTS

The major IOP processor elements, shown in Figure 2-3, are local store, micro-program, data flow, and timing. A standard phrase, "processor elements," will be used in reference to the actual IOP hardware elements to distinguish them from the general term, "processor," which refers to the MSC or a BCE program execution.

A processor's (MSC or BCE) operation is controlled by a series of instructions executed from main memory. A set of general registers in local store is maintained for each processor. A basic IOP instruction cycle consists of extracting an instruction from main memory, performing the instruction, and storing the results.

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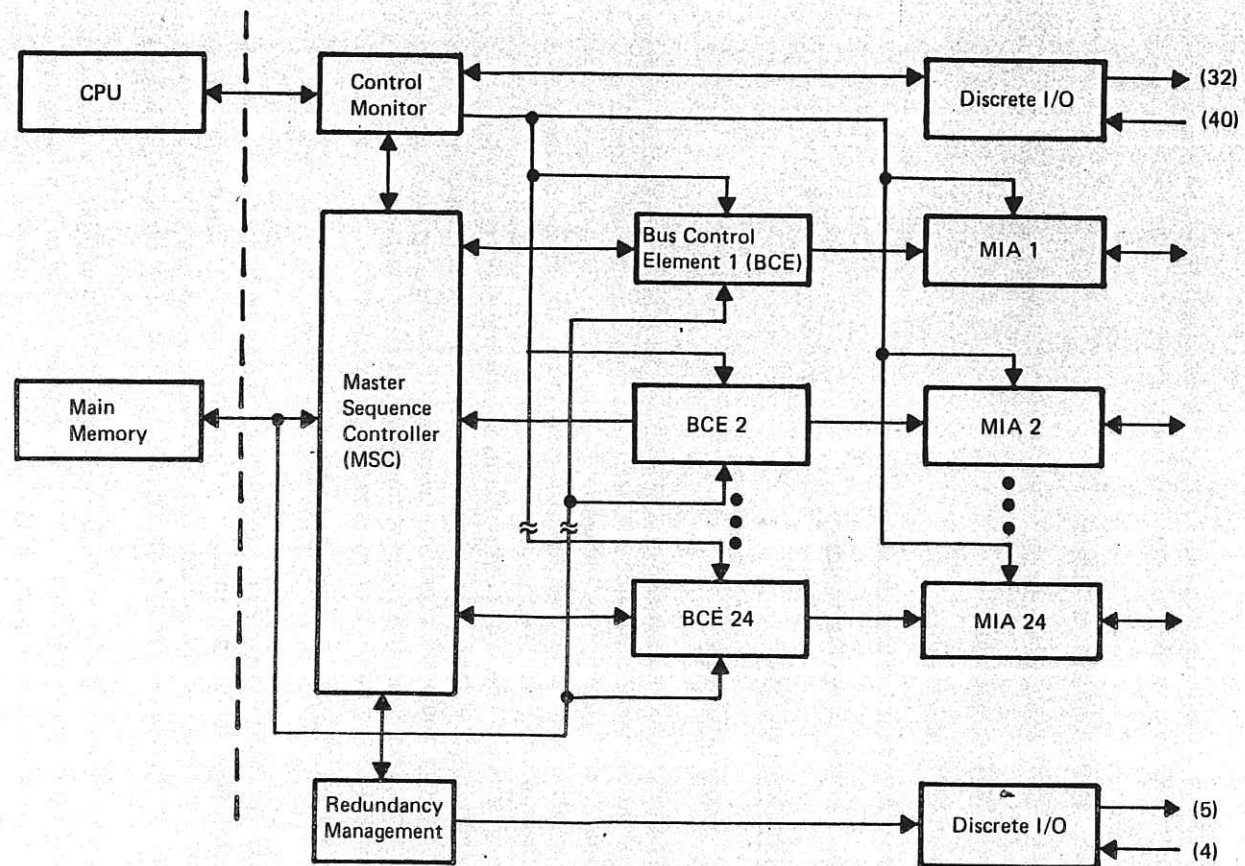


Figure 2-1. IOP Functional Block Diagram

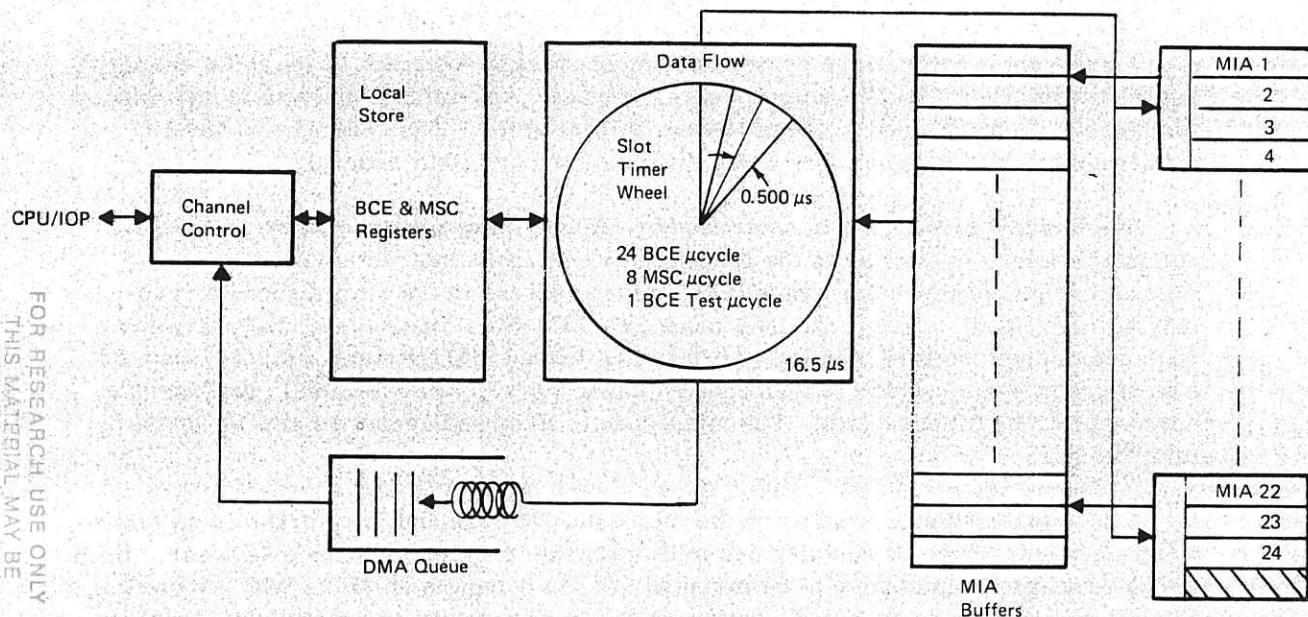


Figure 2-2. Simplified IOP Organization

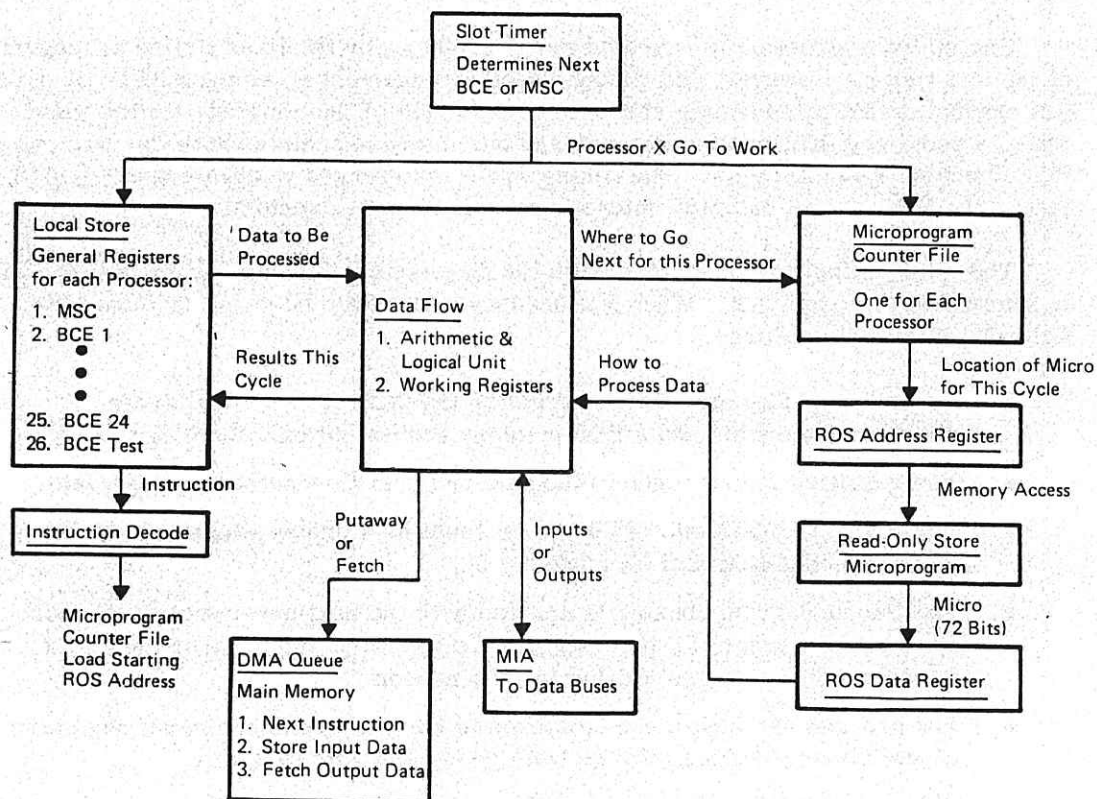


Figure 2-3. Microcycle Information Flow

A program counter in the processor's local store keeps track of the main memory address from where the program is being executed. Any related main memory address for I/O data is maintained in the processor's local store. The instructions and I/O data transfers are accomplished using the main memory DMA channel.

Internal IOP processing is controlled by micros (micro instructions). The execution of a micro is similar to the execution of MSC/BCE instructions in that a microprogram counter keeps track of the micro address in the microprogram read-only storage (ROS). During the first phase of a MSC/BCE instruction, the operation code determines the ROS starting address to be loaded into the microprogram counter. The microprogram counter is then updated as the micros are executed to perform the desired MSC/BCE instruction. The microcode is fixed and cannot be altered by the programmer.

A hardware register resides on the micro decode page and is referred to as microprogram counter file. It contains one microprogram counter for each processor. Each micro requires one slot time to be executed and, to complete an MSC/BCE instruction, several micros will be executed, depending on the complexity of the MSC/BCE instruction. A simple MSC instruction, such as Store Accumulator, requires five micros. One of the more complex instructions, BCE Receive Data, requires 60 micros to define the required processing.

One micro instruction is executed every  $0.500 \mu s$  by the fixed timing arrangement of the slot timer. However, the timing wheel arrangement gives each BCE (or data bus channel) a dedicated timing slot once every cycle of the complete timing wheel. Thus, a dedicated BCE can be serviced and one micro associated with this dedicated BCE executed every  $16.5 \mu s$ . The timing wheel is arranged to devote every fourth slot to the MSC so that one MSC micro instruction can be executed every  $2.0 \mu s$ .

The information flow associated with the processor elements for one microcycle is illustrated in Figure 2-3. When a processor's slot time becomes current, the following microcycle occurs:

- A Read-Only Storage Address register (ROSAR) is loaded from the microprogram file, and a ROS memory access obtains the micro.
- The resulting micro controls the data and data flow paths for this cycle.
- The micro is executed. Each micro contains a processing step, and a test for a condition may be made.
- The microprogram counter is updated with the next sequential micro, or a branch can occur if a test condition is specified and met, or the same micro may be repeated waiting for a condition.
- The processing results can be stored in the processor's general registers (Local Store), written into the DMA queue, or sent to a MIA.
- This completes a slot time, and the next micro is executed.

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MSC/BCE instructions are defined by a microprogram and are defined in the Micro-program Principles of Operation manual. MSC and BCE instruction lists can be found in Subsections 2.4 and 2.5, respectively.

### 2.1.3 EXAMPLE PROGRAM EXECUTION

The timing chart shown in Figure 2-4 is the sequence of micros needed to implement example MSC and BCE programs. The MSC program is listed in Table 2-1, and the BCE programs are listed in Table 2-2. This example shows the relationship between slot timing, I/O channel use, and MIA activity and briefly describes what occurs during a microcycle (one slot time). The MSC micro labeled RAW (repeat until all BCEs are waiting) is continually testing the status of BCE 3 and 15 in the example to determine when they have finished. The remarks column in Tables 2-1 and 2-2 briefly describe each instruction.

MSC programs are initiated by the CPU; the MSC starting sequence follows:

- PCI to test MSC status. If MSC is in the Wait state, proceed.
- PCO to load MSC program counter (100 in this example).
- PCO to place MSC in the Busy state.

## 2.2 PROGRAM CONTROL INPUTS AND OUTPUTS

The CPU controls the IOP by PCI and PCO instructions issued over the I/O channel data bus. PCI and PCO instruction formats are summarized in Table 2-3. PCI/PCO transmissions involve a PCI/PCO command word immediately followed by a data word. For a PCO instruction, both a command word and a data word are issued by the CPU. For a PCI instruction, the CPU issues the command word, and the IOP responds with the data word. The CPU maintains a timeout check on IOP response to PCI/PCO commands. For timeout check details, see Subsection 3.4.

### 2.2.1 PCI/PCO COMMAND WORD FORMAT

The 5-bit Device-Select field must contain only the bit specified in the format description for the desired device selected. Additional bits will cause the PCI/PCO data word to be written to all the devices designated, with associated loss of IOP control. No attempts to use the hardware configuration should be made, since driving circuits are not sized to drive multiple loads and will not operate reliably.

Handshaking for a PCI/PCO is required for several operations to allow the device selected to complete an operation before the PCI/PCO command function is implemented. The handshaking operation prevents loss of control of the IOP software because of possible configuration changes during the PCI/PCO implementation.

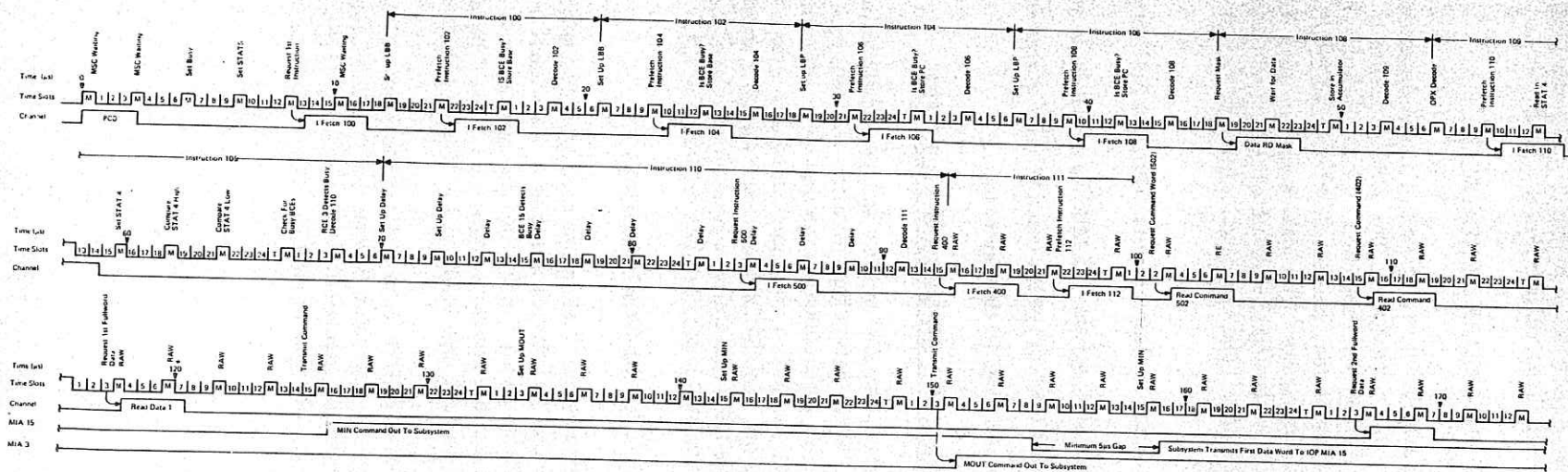
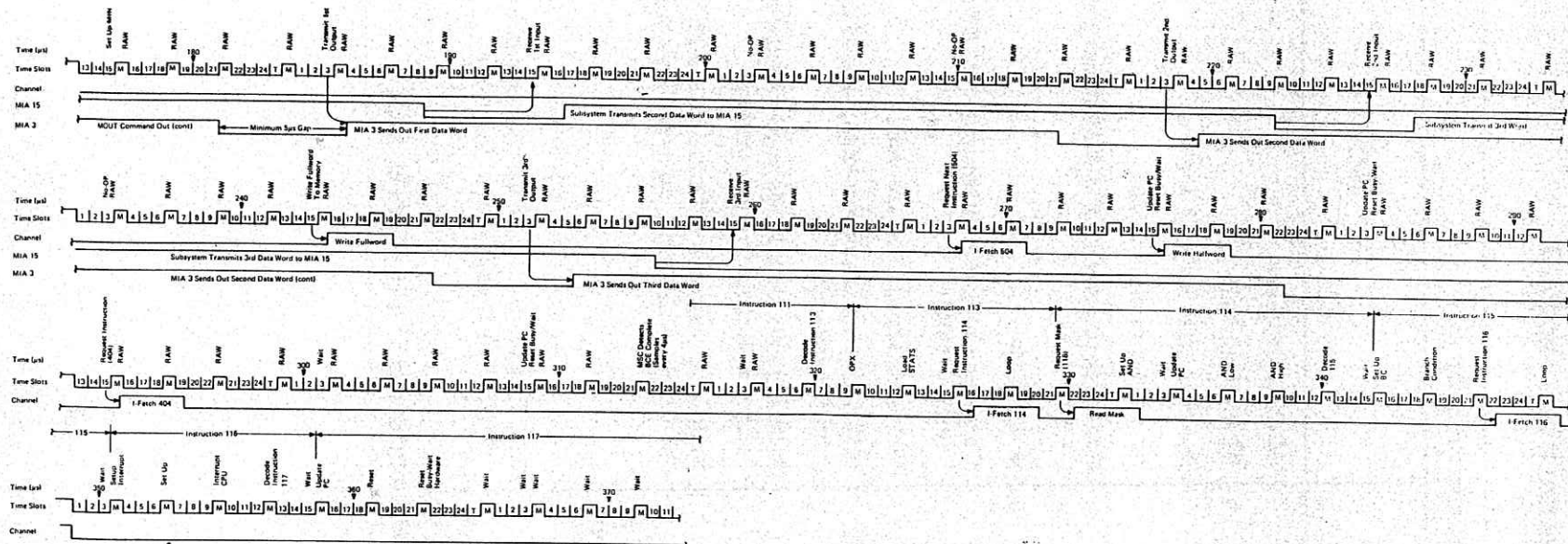


Figure 2-4. Typical IOP Instruction Timing



**Figure 2-4. Typical IOP Instruction Timing (cont)**



Table 2-1  
EXAMPLE MSC PROGRAM

MSC: Start BCEs 15 to Receive, 3 to Transmit			
Main Memory Location	OP Code	Operand	Remarks
100	LBB	15,300	BCE 15 load base
102	LBB	3,200	BCE 3 load base
104	LBP	15,400	Set BCE 15 to start at 400
106	LBP	3,500	Set BCE 3 to start at 500
108	L	10	Get mask to start BCE 3 & 15 (from cell 108 + 10 = 118)
109	SIO		Start BCEs
110	DLY	8	Wait one wheel revolution to get BCES started (8 MSC slots)
111	RAW	10	Now wait until BCEs are done
112	BC	TIMEOUT	If this instruction is executed, one of the BCEs did not turn off
113	LAR	3	At this point, both BCEs have completed. Will now check if there were errors
114	N	4	And error register (STAT1) with BCE mask. If result is nonzero, an error occurred.
115	BC	NOT ZERO, ERROR	
116	INT		Interrupt the GPC with an "All Operations Completed Successfully" interrupt
117	WAT		
118		000100000000000100..0 BCE mask. 1 in positions 3 & 15	

Table 2-2

## EXAMPLE BCE PROGRAMS

BSE 15 - Receive 3 Words of Data			
Main Memory Location	OP Code	Operand	Remarks
400	MIN	2*, 2, CMD	Transmit command to subsystem device telling it to transmit 3 words. Receive data word count = 3, displacement from base = 2
404	WAT	-	Enter Wait state
BCE 3 - Transmit 3 Words			
500	MOUT	2*, 0, CMD	Similar to receive program, transmit 3 words with displacement of data from base = 0
504	WAT	-	Enter Wait state
*One less than actual count			

## 2.2.2 PCO DATA WORDS

The following data present the information contained in the data words associated with each of the PCO instructions. These 32-bit data words may be correlated with the command words through the title and/or the octal or hexadecimal bit configuration. The positions within the data word are referenced by bit positions 0 through 31. Further details are available in the PCI/PCO Principal of Operation. The PCO data word descriptions follow:

- |           |         |                |             |
|-----------|---------|----------------|-------------|
| DMA Burst | Inhibit | 60002000000(8) | C0040000(H) |
|           | Enable  | 60202000000(8) | C1040000(H) |

The data word transferred with this command contains no information and is ignored.

Table 2-3  
PCI AND PCO INSTRUCTIONS

PCIO Command Word Format																																		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 = PCO Command 0 = PCI Command																Command ID Field																		
0	0	0	0	0	1	Select CM										Device Select Field																		
0	0	0	0	1	0	RM										DF																		
0	0	1	0	0	0	LS										CC																		
0	1	0	0	0	0	0 = No Handshake with Device 1 = Handshake with Device										Handshake Control Field																		
																Data Select Field																		
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Load																		
																CC																		
																Disable Burst DMA Mode Enable Burst DMA Mode Enable Bad Parity MIA Add Disable Bad Parity Data In Enable Bad Parity Data In Disable Bad Parity Add Disable Bad Parity DMA Add Disable Bad Parity Data In																		
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Load																		
																CM																		
																Disable MIA Transmitter Enable MIA Transmitter Disable MIA Receiver Enable MIA Receiver Reset Discrete Output Set Discrete Output Halt Processor Enable Processor MIA Transmitter Enable Register MIA Receiver Enable Register Discrete Output Register Halt Register (Stat 5) Master Reset																		
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Read																		
																RM																		
																Watchdog Timer Termination Control Latches Voter Test Register Watchdog Timer for Test No Test All Interrupts Test All Interrupts Interrupt Register A Interrupt Register B Interrupt Register C Interrupt Register D Interrupt Register E Status Register Discrete Input A (High 32) Discrete Input B (Low 8)																		
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Load																		
																DF																		
																Stat 1 (Reset) Stat 4 (Set MSC to Busy) Stat 1 Stat 4																		
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Read																		
																DF																		
																Stat 1 Stat 4																		
1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																Load																		
																LS																		
																Read																		
																LS																		
																MSC Region BCE 1 : BCE 24 Proc 25 (Self-Test) Bank A Bank B Bank C Location 0 : Location 7																		



- MIA Transmitter      Disable      41002000000(8)      84040000(H)  
                                  Enable      41202000000(8)      85040000(H)

Positions 0, <sup>25 through</sup>28, 29, 30, 31 = not used and should be "0"s.

Positions 1 through <sup>27</sup>27 = channels 1 through <sup>27</sup>27 of MIA transmitters, respectively.

If "0" = no change of status.

If "1" = Enable or Disable, depending on command word.

- MIA Receiver      Disable      41004000000(8)      84080000(H)  
                                  Enable      41204000000(8)      85090000(H)

Positions 0, <sup>25 through</sup>28, 29, 30, 31 = not used and should be "0"s.

Positions 1 through <sup>27</sup>27 = channel 1 through <sup>27</sup>27 of MIA transmitters, respectively.

If "0" = no change of status.

If "1" = Enable or Disable, depending on command word.

- Discrete Output      Reset      41010000000(8)      84100000(H)  
                                  Set      41210000000(8)      85100000(H)

Positions 1 through 31 = Discrete Outputs (DO) 1 through 31, respectively.

If "0" = no change of status.

If "1" = set or reset the DO, depending on command word.

- Processor      Halt      41020000000(8)      84200000(H)  
                                  Enable      41220000000(8)      85200000(H)

Positions 0, <sup>25 through</sup>28, 29, 30, 31 = not used and should be "0"s.

Position 0 = MSC.

Position 1 through <sup>27</sup>27 = BCE processors 1 through <sup>27</sup>27, respectively.

If "0" = no change of status.

If "1" = Processor Halt or Enable, depending on command word.

- Master      Reset      41040000000(8)      84400000(H)

The data word transferred with this command word is ignored.

- Load    Go/No-Go    Timer    42002000000(8)    88040000(H)  
              Go/No-Go    Timer Test    42002200000(8)    88048000(H)

Positions 0 through 19 = not used and should be "0"s.

Positions 20 through 31 = weighted binary data representing the value to be loaded.

Position 20 = MSB.

Position 31 = LSB = 0.768 ms.

- Termination    Latch Control    42004000000(8)    88080000(H)

Positions 0 through 29 = not used and should be "0"s.

Position 30 = Timeout Termination latch.

Position 31 = Voter Termination Latch.

If "0" = reset.

If "1" = set.

- Load Test Register    42010000000(8)    88100000(H)

Positions 0 through 26 = not used and should be "0"s.

Position 27 = voter test control.

If "0" = permit normal RM operation.

If "1" = inhibit normal RM operation to perform test.

Positions 28 through 31 = voter inputs 1 through 4 for test inputs.

If "0" = simulation of nonfail case.

If "1" = simulation of failed input.

- Reset Program Exception    44400000000(8)    92000000(H)

Positions ~~28, 29, 30~~, 31 = not used and should be "0"s.

Position 0 = MSC.

Positions 1 through <sup>27</sup>~~27~~ = BCE numbers 1 through <sup>27</sup>~~27~~, respectively.

If "0" = do not alter Go or No-Go status as presented.

If "1" = reset the position to a normal or Go status.

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- Load MSC Busy 44402000000(8) 92020000(H)

The data word associated with the transfer of this command word is not used. The command word will force the MSC to the Busy state.

- Load Local Store (Command word specifies address.)

Positions 0 through 13 = not used and should be "0"s.

Positions 14 through 31 = positions 0 through 17 of the specified Local Store word.

### 2.2.3 PCI DATA WORDS

The PCI data word descriptions follow:

- MIA Transmitter Status 01000000000(8) 04000000(H)  
Receiver Status 01002000000(8) 04020000(H)

Positions 0 through <sup>23</sup>26 = MIA channels 1 through <sup>24</sup>27, respectively.

If "0" = transmitter (or receiver) disabled.

If "1" = transmitter (or receiver) enabled.

Positions 27 through 31 = not used and should be "0"s.

- Read Discrete Outputs 01004000000(8) 04080000(H)

Positions 0 through 31 = DOs 1 through 32, respectively.

If "0" = DO is off.

If "1" = DO is on.

- Processor Halt Status 01006000000(8) 040C0000(H)

Position 0 = MSC.

Positions 1 through 27 = BCEs 1 through 27, respectively.

If "0" = processor is disabled.

If "1" = processor is enabled.

Positions 28 through 31 = not used and should be "0"s.

- Read Interrupt Register 1 02000000000(8) 08000000(H)

Position 0 = Watchdog timer.

If "0" = timer has not timed out.

If "1" = timer has timed out.

Position 1 = IOP Fail latch.

If "0" = not failed.

If "1" = IOP failed.



Position 2 = CM IDLE.

If "0" = control monitor logic is operating.

If "1" = control monitor is in Idle mode and is available.

Position 3 = ROS parity error.

If "0" = no error.

If "1" = parity error for IOP ROS has been detected.

Position 4 = IOP fault.

If "0" = no fault detected.

If "1" = IOP oscillator has stopped.

Position 5 = spare.

Positions 6 through 31 = not used and should be "0"s.

**READ**

- Interrupt Register 2 02002000000(8) 08040000(H)

Position 0 = PCI/PCO parity error.

If "0" = no error.

If "1" = parity error detected during PCI/PCO transfer on one of the words data or command.

Position 1 = DMA instruction parity error.

If "0" = no errors.

If "1" = parity error on instruction word during DMA operation.

Position 2 = DMA data parity error.

If "0" = no errors.

If "1" = parity error detected during data word transfer during DMA operation.

Position 3 = Burst DMA error.

If "0" = no errors.

If "1" = more than 63 (10) words have been transferred in sequence.

Position 4 = DMA Queue Full indicator.

Position 5 = spares.

Positions 6 through 31 = not used and should be "0"s.

- Interrupt Register 3 02004000000(8) 08080000(H)

Positions 0 through 11 = MSC program interrupts 1 through 12, respectively.

If "0" = no interrupt.

If "1" = interrupt received.

Positions 12 through 31 = not used and should be "0"s.

• Interrupt Register 4 02010000000(8) 08100000(H)  
Positions 0 through 3 = spares.  
Positions 4 through 31 are not used and should be "0"s.

• Interrupt Register E 02010000000(8) 08100000(H)  
Positions 0 through 3 = spares.  
Positions 4 through 31 = not used and should be "0"s.

• RM Status Register 02010000000(8) 08100000(H)  
Position 0 = Fail or Timeout latch.  
If "0" = no failure.  
If "1" = IOP failure or simulated failure if in Self-Test mode.  
Position 1 = PCO Inhibit Fail Vote inputs for test.  
If "0" = RM voter configured for normal operations.  
If "1" = RM voter configured for self-test; normal operations inhibited  
Position 2 = MSC inhibit Fail Vote outputs for test.  
If "0" = normal operation.  
If "1" = RM Vote output inhibit for self-testing.  
Positions 3 through 6 = Failure Vote inputs 1 through 4.  
If "0" = no failures.  
If "1" = Failure Votes being received from other IOPs.  
Positions 7 through 10 = Failure Vote outputs 1 through 4.  
If "0" = no failure detected (good vote).  
If "1" = Failure Vote to other IOPs.  
Positions 11 through 14 = Test Failure Vote inputs 1 through 4.  
If "0" = no failures simulated.  
If "1" = failures simulated for self-testing.  
Position 15 = Voter Fail latch.  
If "0" = no failure indicated.  
If "1" = failure indicated for Normal or Test modes.  
Position 16 = Timeout latch.  
If "0" = no Go/No-Go timeout indicated.  
If "1" = Go/No-Go time out reached.  
Position 17 = Voter Termination Control latch.



Position 18 = Timer Termination Control latch.

If "0" = latch is reset indicating Go.

If "1" = latch is set indicating No-Go.

Position 19 = IOP transmission termination.

If "0" = normal operation, Go.

If "1" = terminate operations, No-Go.

Positions 20 through 31 = Go/No-Go timer data value in weighted binary.  
Bit 31 is LSB and equals 0.768 ms. All "1"s  
represent an excess of 3 seconds.

- Discrete Input Register A 02014000000(8) 08180000(H)

Positions 0 through 31 = DIs 1 through 32, respectively.

- Discrete Input Register B 02016000000(8) 081C0000(H)

Positions 0 through 7 = DIs 33 through 40, respectively.

- Read Program Exception 04000000000(8) 10000000(H)

Position 0 = MSC.

If "0" = No-Go.

If "1" = Go.

Positions 1 through 27 = BCEs 1 through 27, respectively.

If "0" = No-Go.

If "1" = Go.

Positions 28 through 31 = not used and should be "0"s.

- Read Busy/Wait 04002000000(8) 10040000(H)

Position 0 = MSC.

If "0" = Wait.

If "1" = Busy.

Positions 1 through 27 = BCEs 1 through 27, respectively.

If "0" = Wait.

If "1" = Busy.

Positions 28 through 31 = not used and should be "0"s.

- Read Local Store (Command word specifies address.)

Positions 0 through 13 = not used and should be "0"s.

Positions 14 through 31 = bits 0 through 18 from local store, respectively.



### 2.3 STATUS AND INTERRUPT REGISTERS

IOP data processing state is maintained by status and interrupt registers. The IOP contains the following types of status registers:

- Processor Hardware Status registers
- Processor Software Status registers
- Redundancy Management Status register.

The hardware and RM status registers are described in the following paragraphs. The software status registers are maintained in the processor's local store and are described in Subsections 2.4 (MSC) and 2.5 (BCE).

IOP interrupts to the CPU are generated by IOP error conditions or as a result of program execution. Basically, programmed interrupts are used by the MSC to communicate with the CPU program. The CPU has mask/unmask (off/on) control of all IOP interrupts except the IOP Power-Off interrupt.

Hardware status registers contain 25 or 26 bits, which summarizes how a hardware status register is controlled. Status register functions are as follows:

- Halt Register — Is a 25-bit register which provides individual control of the processors to stop program execution. If a processor is halted, a PCO command must be issued to re-enable the processor. If the RM transmission termination is activated, all processors are halted.
- Program Exception Register — This register contains 25 bits, one for the MSC and one for each BCE. When a bit in this register is reset (No-Go), it indicates that a processor has encountered some problem in the execution of a program. The MSC's or BCE's software status register, maintained in the processors local store, will contain the cause of the exception.
- Busy/Wait Register — For the MSC and each BCE this 25-bit register provides an indication that a processor is executing a program.
- Indicator Register — Provides a communication path between processors. For example, a BCE channel can signal the MSC that MSC processing is required to resolve an error condition.
- MIA Transmit Enable Register — Controls MIA transmitters. If the RM transmission termination is activated, all channels are inhibited.
- MIA Receive Enable Register — Controls MIA receivers. If the RM transmission termination is activated, all channels are inhibited.
- RM Status Register — Provides the status of the various functions associated with RM hardware logic. Register contents are listed in Table 2-4. A PCI instruction is used to read the RM status register.

Table 2-4  
REDUNDANCY MANAGEMENT STATUS REGISTER

Bit	Description
0	Fail or Timeout Latch "0" = Normal, "1" = Fail
1	PCO Inhibit for Test
2	MSC Inhibit for Test
3	Failure Vote 1 In
4	Failure Vote 2 In
5	Failure Vote 3 In
6	Failure Vote 4 In
7	Failure Vote 1 Out
8	Failure Vote 2 Out
9	Failure Vote 3 Out
10	Failure Vote 4 Out
11	Test Failure Vote 1 In
12	Test Failure Vote 2 In
13	Test Failure Vote 3 In
14	Test Failure Vote 4 In
15	Voter Fail Latch "0" = Normal
16	Timeout Latch "1" = Fail
17	Voter Termination Control Latch "0" = Reset
18	Timer Termination Control Latch "1" = Set
19	IOP Transmission Termination "0" = Normal, "1" = Terminate
20	Timer Bit 0 (MSB)
21	Timer Bit 1
22	Timer Bit 2
23	Timer Bit 3
24	Timer Bit 4
25	Timer Bit 5
26	Timer Bit 6
27	Timer Bit 7
28	Timer Bit 8
29	Timer Bit 9
30	Timer Bit 10
31	Timer Bit 11 (LSB)

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- Interrupt Register — One associated with each of the five interrupt lines from the IOP to the CPU. Two of the interrupt lines (and registers) are spares. Each bit in a register is ORed together to produce an interrupt when any bit is set. If an interrupt is enabled (unmasked) in the CPU, it will cause the CPU to interrupt the program being executed, and the CPU will service the IOP interrupt. The Interrupt register will be read (and reset) by a PCI instruction to determine which bit in the register was set. If the interrupt is inhibited (masked), the interrupt will remain pending until unmasked. The ~~three~~ active Interrupt register groups are as follows:

- Interrupt Register Group 1 (16A to 16F)

Bit 0 — Set when the Watchdog timer has timed out.

Bit 1 — Set when the ~~RM Hardware~~ Voter latch is activated.

Bit 2 — Set during power turn-on and turn-off sequencing, set if Master Reset command is issued, and set if IOP Failure signal is generated. Indicates to CPU that IOP is in Reset state when active.

Bit 3 — Set if a ROS parity error is detected.

Bit 4 — Set if the timing stop detector (oscillator failure) occurs.

Bit 5 — Spare.

Bits 6 through 31 — Not used.

- Interrupt Register Group 2 (17A to 17F)

Bit 0 — Set if a parity error is detected on the PCI/PCO channel data bus.

Bit 1 — Set if a parity error is detected for a DMA instruction request.

Bit 2 — Set if a parity error is detected for a DMA data request.

Bit 3 — Set when more than 64 consecutive Burst mode DMA requests have been issued. IOP will inhibit Burst mode until enabled by PCO command.

Bit 4 — Set if the DMA queue overflows. IOP processing will continue.

Bit 5 — DMA Timeout. Individual DMA transfers are timed, channel is cleared and reset if Timeout occurs.

- Interrupt Register Group 3 (18A to 18L)

Bits 1 through 12 — Programmable interrupts generated by the MSC processor.

Bits 13 through 31 — Not used.

- Interrupt Register Group 4 (19A to 19D)

Four interrupts

- Interrupt Register Group 5 (20A to 20D)

Four interrupts



## 2.4 MASTER SEQUENCE CONTROLLER (MSC)

The MSC executive type processor controls the BCEs. The major functions of the MSC are listed:

- Supervise the IOP data processing by execution of programs from main memory
- Control and monitor the BCE status and aid in error handling
- Communicate with the CPU through IOP interrupts
- Perform redundancy management processing.

MSC characteristics are summarized in Table 2-5.

Table 2-5  
MSC CHARACTERISTICS

Characteristic	Description
Type Processor	Single Accumulator I/O Management Computer
Control Structure	Microprogrammed
Programmable Registers	32-Bit Accumulator (ACC) 18-Bit Index Register (X) 18-Bit Program Counter (PC)
Program Visible Registers	18-Bit Status Register 25-Bit Program Exception Register 25-Bit Busy/Wait Register 24-Bit BCE-MSC Indicators 5-Bit RM Fail Discretes 12-Bit IOP Programmable Interrupt Register 18-Bit External Call Register
Instruction Formats	16-Bit Short/32-Bit Long
Instruction Repertoire	47 Short Format/10 Long Format (not counting Addressing Modes)
Addressing Space	131,072 32-Bit Fullwords/262,144 16-Bit Halfwords
Addressing Modes	Absolute, Indexed, PC Relative, Immediate
Data Format	Signed, Two's Complement Integer

#### 2.4.1 MSC PROGRAMMABLE REGISTERS (See Table 2-11 and Figure 2-7).

The ACC is a 32-bit register capable of accumulating a fullword of data from memory. MSC instructions are available to load, modify, test, and store this register. The ACC also contains bit masks for status and polling applications.

Data representation of numbers held by the ACC is a signed, two's-complement, 32-bit integer, with the sign bit in bit 0 and the binary point to the right of bit 31.

The Index register may be used both in generating 18-bit main memory addresses and as a holding register for signed two's-complement, 18-bit integers.

The Program Counter is an 18-bit register that indicates the main memory halfword or fullword location of the MSC instruction presently being executed.

#### 2.4.2 MSC OPERATION

During normal operation the MSC can be in one of three states: Halt, Wait, and Busy. In the Halt state, the MSC is physically restrained from performing any operations; in the Wait state, the MSC is awaiting a command to execute a program; and in the Busy state, the MSC is executing MSC programs from main store.

Typical state transitions are as follows:

- During any system or CPU-directed MSC reset, the MSC is in the Halt state.
- Upon release from the Halt state, the MSC enters the Wait state (with perhaps intermediate execution of an Initial Program Load (IPL) sequence).
- A sequence of PCOs from the CPU initializes the MSC and places it in the Busy state.
- In the Busy state, the MSC is executing a program located in main memory. It exits the Busy state only upon execution of a Wait instruction, detection of an invalid instruction, or some MSC reset signal. In all but the latter case, the MSC re-enters the Wait state; in the latter case, it is forced to the Halt state.

The two bits that indicate the current state of the MSC are its Halt bit (bit 0 of the IOP Halt register) and its Busy/Wait bit (bit 0 of the IOP Busy/Wait register). In addition, the MSC Program Exception bit indicates if the MSC has found an error during its last period of time in the Busy state. If it has found an error, the MSC Status register contains a record of the exact error.

The following paragraphs describe each state in detail.

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#### 2.4.2.1 Halt State

The primary purpose of the Halt state is twofold:

- Allow the external world to reset MSC operation to a known condition
- Upon the detection of very serious IOP faults (such as failure in the microstore), to isolate the MSC and prevent it from performing potentially erroneous operations.

Entry and exit from the Halt state are controlled by the value of a single MSC Halt status bit, which is part of the IOP Halt register. As long as this bit is set, the MSC microprogram counter is forced to point to a microinstruction that performs no operation other than clear the MSC Busy/Wait bit. The Halt bit may be set at any time, and effectively terminates anything that the MSC is doing.

The signals that set the MSC Halt bit include

- ~~BCE~~ ~~Discrete~~
- Master-Reset discrete from the CPU
- Power-Up/Down signal
- Setting of the Fail latch for this GPC by either the Redundancy Management voting logic or IOP-detected serious errors such as ROM parity error
- A Halt Processor PCO from the CPU with a "1" in bit position 0.

The first three signal classes also halt all BCEs. Exit from this state to the Wait state occurs only when

- Master-Reset discrete is reset
- Power-up sequence is complete
- Fail latch is reset

and a CPU Enable Processors PCO with bit 0 = "1" is present. Existence of the IPL signal causes the microcode supporting the MSC to run through an IPL sequence before entering Wait.

Upon any exit from the Halt state, the MSC Program Exception bit and MSC Status register are cleared. The MSC also clears its External Call register at this time.

#### 2.4.2.2 Wait State

In the Wait state, the MSC is prepared to be told to perform an MSC program. This Wait loop is implemented by a microroutine that monitors the status of the MSC Busy/Wait bit. The MSC remains in the Wait state as long as this bit is reset to the Wait value. Setting this bit to a Busy condition causes the MSC to enter the Busy state. This transition consists of using the present value of the MSC's Program Counter as the starting address of an MSC program in Main Store.



Entry to the Wait state occurs either upon exit from the Halt state, as described, or by a transition from the Busy state. The MSC performs this latter transition when

- A WAIT instruction is executed
- An instruction with an illegal OP code is encountered
- A valid long format instruction is found starting on an odd halfword boundary.

In the latter two cases, the following actions are performed prior to entering the Wait state:

- The MSC Program Exception bit is set to 0 (error).
- The MSC Status register is set to indicate the exact cause of the error.
- The MSC Program Counter is left pointing to the offending instruction.

The Program Exception bit and Status registers may also be set when other errors are detected while the MSC is in the Busy state. In these cases, however, the MSC continues execution of the program.

Exit from the Wait state is normally to the Busy state. This is done by the CPU via a sequence of PCOs, which typically include

- A Load Local Store PCO to clear the MSC Status register (if set)
- A Reset Program Exception Register PCO with a "1" in bit 0 (again used only when MSC has indicated an error)
- A Load Local Store PCO to point to the start of the desired MSC program in main store
- A Start MSC PCO to set the MSC Busy/Wait bit.

Note that the first two are needed only to recover from an MSC error, and the third is needed only if the MSC Program Counter must be reset. They may not always be necessary, since the Wait instruction (WAT), when executed, leaves the PC pointing to the next sequential instruction, which in turn may be programmed as a simple jump back to the beginning of the MSC program. In this case, the CPU needs only to issue the "Start MSC" PCO to restart the MSC program.

#### 2.4.2.3 Busy State

In the Busy state, the MSC is in the process of executing a program out of main store. A value of "1" in the 0 bit of the IOP Busy/Wait register indicates this condition.

The Busy state may be entered only from the Wait state, as just described. When the transition occurs, the MSC uses whatever value is presently in its Program Counter to fetch the first instruction from memory and start executing it. The MSC continues executing instructions until either a Wait instruction or some kind of invalid instruction is encountered. In either case, the MSC transitions back to the Wait state, as described previously.

While the MSC is in the Busy state, the CPU may execute any PCI without problem. However, all PCOs that write into MSC local store should be carefully controlled, since the MSC is not aware that this action has occurred, and the resulting MSC program execution may be unpredictable.

#### 2.4.2.3.1 Busy State — External Calls

Once the CPU has set the MSC busy, it has no direct control over the program that the MSC executes. Consequently, if the CPU finds some task that it wishes the MSC to execute, it must somehow signal this to the MSC without destroying the status of the MSC program currently being executed. The MSC allows such signalling to occur through the use of "External Calls."

If the CPU wishes the MSC to perform some function while the MSC is busy with another function, it may load the starting address of the relevant MSC program into the MSC's External Call register (ECR). Each time the MSC executes a "Sample for External Call" instruction, it samples this register. As long as it is zero, the MSC continues with the current program. A nonzero value, however, causes the MSC to store in memory copies of its Accumulator, Index register, Status register, and Program Counter, and to clear the Status register of all error indicators. The MSC then loads its Program Counter with the value found in the ECR, zeros the ECR, and begins execution of the CPU-specified routine. At the end of this routine a "Return from External Call" instruction reloads all the above MSC registers to their original state, and resumes execution of the original program just as if it had never been interrupted.

#### 2.4.3 MSC INSTRUCTIONS

MSC instruction formats are shown in Figure 2-5 and are listed in Table 2-6.

Short format 1 is used primarily by instructions dealing with memory and the MSC accumulator. It has the following fields:

<u>Field</u>	<u>Field Description</u>
OP	This 4-bit field defines the basic operation to be performed by the MSC.
I	This bit serves either as an OP code extension or as an index mode specification in address generation.
DISP	This 11-bit field serves either as immediate data or as a PC relative address displacement.

Short format 2 is used by the register operation, register immediate, repeat, and conditional branching instruction classes. It has the following fields:

<u>Field</u>	<u>Field Description</u>
OP	This 4-bit field defines the basic operation class to be performed by the MSC.
I	This bit serves either as an OP code extension or as an index mode specification in address generation.



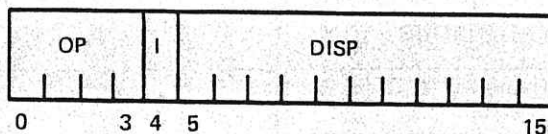
Table 2-6  
MSC INSTRUCTIONS

OP Code I OPX	Instruction	Mnemonic	Assembler Format	Notes
<b>ACCUMULATOR/MEMORY INSTRUCTIONS</b>				
0100	Load ACC	@L	Label (X)	1, 2, 17
0101	Add to ACC	@A	Label (X)	1, 2, 17
0110	And to ACC	@N	Label (X)	1, 2, 17
0111	XOR to ACC	@X	Label (X)	1, 2, 17
1000	Store ACC	@ST	Label (X)	1, 2, 17
1111-100	Load ACC Fullword	@LF	Label (X)	1, 12, 15, 19
1111-100	Load ACC with Halfword	@LH	Label (X)	1, 12, 16, 19
1111-101	Store ACC Full	@STF	Label (X)	1, 12, 15, 19
1111-101	Store ACC Half	@STH	Label (X)	1, 12, 16, 19
<b>BRANCH INSTRUCTIONS</b>				
00100	Branch On Acc	@BC	COND., Label	6, 7, 17
00101	Branch On Index	@BXC	COND., Label	6, 7, 17
1111-000	Branch Unconditional	@BU	Label (X)	1, 10, 12, 19
1111-001	Subroutine Call	@CALL	Delta, Label (X)	1, 10, 12, 13, 19
1010	Return from External Call	@REC	Label (X)	1, 2, 17
<b>CONDITIONAL SKIPS</b>				
1001	Tally & Skip Zero	@TSZ	Label (X)	1, 2, 17
1111-110	Compare	@C, CI	Label (X)	1, 10, 14, 19
1111-111	Test Under Mask	@TM, TMI	Label (X)	1, 10, 14, 19
<b>BCE REGISTER LOADS</b>				
1111-010	Load BCE Base	@LBB	BCE, Label (X)	1, 10, 11, 12, 19
1111-011	Load BCE PC	@LBP	BCE, Label (X)	1, 10, 11, 12, 19
<b>REGISTER OPERATIONS</b>				
1110-0000	Load ACC with an IOP Status Register	@LAR	REG	8, 18
1110-0001	Set Fail Discretes	@SFD		18
1110-0010	Reset Fail Discretes	@RFD		18
1110-0011	Load ACC with MSC Status	@LMS		18
1110-0100	Start BCEs	@SIO		18
1110-0101	Exchange ACC And/X	@XAX		18
1110-0110	Sample for External Call	@SEC	Label	7, 18
1110-0111	Reset BCE Indicator	@RBI	BCE	11, 18
<b>REGISTER IMMEDIATES</b>				
1110-1000	Normalize & Increment X	@NIX	IMM	9, 18
1110-1001	Tally ACC to X	@TAX	IMM	9, 18
1110-1010	Tally X	@TXI	IMM	9, 18
1110-1011	Load X Immediate	@LXI	IMM	9, 18
1110-1100	Tally X to ACC	@TXA	IMM	9, 18
1110-1101	Tally ACC Immediate	@TI	IMM	9, 18
1110-1110	Subtract ACC from IMM	@SAI	IMM	9, 18
1110-1111	Load ACC Immediate	@LI	IMM	9, 18
<b>REPEAT INSTRUCTIONS</b>				
1101-000	Repeat Until All Waiting	@RAW	Count (X)	1, 5, 18
1101-001	Repeat Until Any Waiting	@RNW	Count (X)	1, 5, 18
1101-100	Repeat Until All Indicators	@RAI	Count (X)	1, 5, 18
1101-101	Repeat Until Any Indicators	@RNI	Count (X)	1, 5, 18
<b>SPECIAL INSTRUCTIONS</b>				
0000	Wait	@WAT		17
0001	Self-Test	@STP		17
1100	Delay	@DLY	Count (X)	1, 3, 17
0011	Interrupt GPC	@INT	INTLIST (X)	1, 4, 17

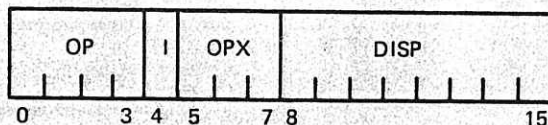
Notes:

- (X) specifies indexing mode bit 4 (0) — No index, (1) — index
- Label is translated into updated PC relative address, -1024 to +1023
- Count has range 0 to 2047 (11 bits)
- INT LIST is an 11-bit interrupt designator
- Count has range 0 to 255
- COND has value from 0 to 7 to specify branch condition
- Label is translated into updated PC relative address, -128 to +127
- REG has value 0-3
- IMM (Immediate) has value -128 to +127 (8 bit)
- Following OP code mnemonic by @ specifies M=1, direct addressing
- BCE is BCE number -0 to 24
- Label is absolute 18-bit address
- Delta is positive constant between 0 and 31
- Label can be 18 bit immediate or 18-bit address if direct specified
- Bit 12 = 0
- Bit 12 = 1
- Short Format 1
- Short Format 2
- Long Format

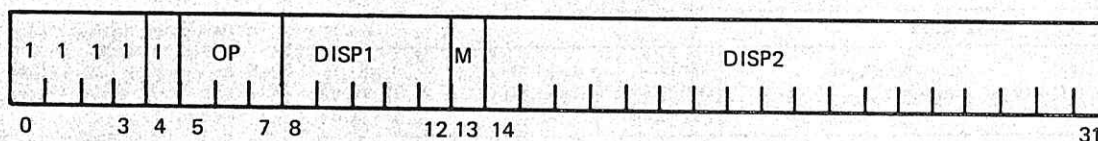




Short Format 1



Short Format 2



Long Format

Figure 2-5. Basic MSC Instructions Formats

- OPX This field is an extension of OP.
- DISP This field serves as either immediate data or as a PC relative address displacement.

Format 3, used for all long 32-bit instructions and has the following fields:

Field	Field Description
OP	This 3-bit field defines the basic operation to be performed by the MSC.
DISP1	This 5-bit field defines such things as BCE numbers, short displacements, etc.
DISP2	This 18-bit field is used in conjunction with I and M to generate both 18-bit main memory addresses and immediate data
I, M	These two bits define the way that DISP2 forms values used by the instruction for main memory addresses and immediate data.

#### 2.4.4 MSC LOCAL STORE AND STATUS REGISTER

MSC general registers are maintained in Local Store. Table 2-7 lists the MSC Local Store register assignments.

The information contained in the MSC Status register (Local Store bank C, word 7) is listed in Table 2-8.

Table 2-7

#### MSC LOCAL STORE USAGE

Bank A	Bank B	Bank C	Word
WR	WR	WR	0
WR	WR	WR	1
PC	IH	IL	2
X	AH	AL	3
		WR	4
		WR	5
		ECR	6
		ST	7

Notes:

WR - working registers used for temporary storage. Major items are: DMA address and data high, low, test constants, and address assembly

PC = MSC Program Counter

X = MSC Index register

IH - upper 16 bits of present MSC instructions (right-justified with bits 0 and 1 ignored)

IL - lower 18 bits of last instruction word that was read from memory

AH - bits 0 through 15 of MSC accumulator (right-justified with local store bits 0, 1 ignored).

AL - bits 16 through 31 of MSC accumulator (right-justified as for AH)

ECR - External Call register

ST - bits 0 through 17 of MSC Status register

Table 2-8

#### MSC STATUS REGISTER

Bit	Use	Description
17-B/W	Busy/Wait	A copy of bit 0 of the Busy/Wait register
16-E	Program Exception	An inverted copy of bit 0 of the Program Exception register. If set to 1, an error was detected during MSC program execution. Bits 15 through 11 give exact errors
15-I	Illegal OP Code	The MSC encountered an illegal instruction in the execution of a program
14-BA	Boundary Alignment	The MSC encountered a long format instruction on an odd halfword boundary
13-LBB	LBB Error	An LBB instruction attempted to load a busy BCE
12-LBP	LBP Error	An LBP instruction attempted to load a busy BCE
11-SIO	SIO Error	An SIO instruction attempted to start a busy BCE

## 2.5 BUS CONTROL ELEMENT

The BCE processors execute programs from main memory to service the 24 MIA data buses. BCE functions are to

- Receive MIA data
- Transmit MIA data and commands
- Check incoming data for errors
- Read or write I/O data into main memory via DMA
- Receive Listen commands from other IOPs.

BCE characteristics are summarized in Table 2-9.

Table 2-9

### BCE CHARACTERISTICS

Type — Programmable I/O traffic controller

Number — One per bus, 24 BCEs per IOP

Control Structure — Microprogrammed

Programmable Registers (per BCE)

18-Bit Base Register (BASE)

18-Bit Program Counter (PC)

18-Bit Maximum Time Out Register (MTO)

5-Bit Interface Unit Address Register (IUAR)

1-Bit BCE/MSI Indicator Bit

Other BCE Registers (per BCE)

32-Bit Status Register

1-Bit Program Exception Register (part of STAT 1)

1-Bit Busy/Wait Bit (part of STAT 4)

1-Bit MIA Transmitter Enable

1-Bit MIA Receiver Enable

6-Bit Identity Register

Instruction Formats: 16-Bit Short/32-Bit Long

Instruction Repertoire: 11 Short/7 Long

Addressing Space: 131,072 32-Bit Fullwords/262,144 16-Bit Halfwords

Addressing Modes: Immediate, PC Relative, Base Relative, Absolute

Special Operating Modes: Command, Listen

Bus Data Format: 25 + Sync Bit Serial



### 2.5.1 PROGRAMMABLE REGISTERS

Each BCE processor has a set of programmable registers in local store. The major BCE registers include:

- Program Counter (18 bits) — Specifies the main memory address where the next BCE instruction is located. BCE instructions are executed sequentially unless a branch instruction is encountered.
- Base Register (18 bits) — Specifies the main memory address where I/O data is located.
- Maximum Timeout (18 bits) — Controls the maximum time that a BCE will wait for the first data word for a receive data instruction.
- Interface Unit Address (5 bits) — Contains the 5-bit bus address of the subsystem presently in communication with this BCE.
- Status Register (32 bits) — Used to record any error conditions encountered during program execution.
- Indicator Register (1 bit) — Set and reset by a BCE to communicate with MSC.

### 2.5.2 BCE OPERATION

The BCE can be in one of three states: Halt, Wait, or Busy. In the Halt state, the BCE is inhibited from performing any operations. In the Wait state, the BCE is waiting for a signal from the MSC to execute a program. In the Busy state, the BCE is executing BCE programs from main memory. Typical state transitions are similar to those for the MSC, except that

- Either the MSC or CPU may initialize BCE Base and Program Counter registers
- Only the MSC may set a BCE busy.

The BCE enters the Busy state to perform one of the following I/O sequences:

- Command and Receive Data
- Command and Transmit Data
- Listen and Receive Data
- Wait for Listen Command.

The receive and transmit sequences are triggered by either execution of the BCE Instruction Transmit command (CMD), followed by a BCE Receive or Transmit instruction, or by a Message In or Message Out instruction. The CMD informs a data bus device that data are required from it or that data will be sent to it. The Receive or Transmit instruction controls the operation of the BCE during the actual data transfer, and indicates how many bus words are to be received/transmitted, and where in memory the data is destined for or originates. All data buffer addresses are Base relative.

#### 2.5.2.1 BCE Command and Listen Mode

When a BCE is in the Busy state, the status of the associated MIAs transmitter and receiver affects the way various BCE instructions are executed.

MIA transmitters and receivers are enabled or inhibited by hardware registers. The CPU controls these Enable/Inhibit registers by PCO instructions. This gives the Flight Control Operating System (FCOS) software control of data bus transmissions.

In command mode (Transmitter and Receiver enabled) the BCE is master of its bus and is free to transmit both commands and data and receive incoming data. In Listen mode (only receiver enabled) the BCE is not allowed to transmit either commands or data, but may receive data and "Listen Commands." A BCE in Listen mode relies on other IOPs to command subsystems to return data, and uses the presence of these commands on its bus as signals to start receiving data (when the BCE is executing a Receive Data instruction). Additionally when a BCE in Listen mode executes a Wait-for-Index instruction, it monitors its bus for a command from another IOP (termed a "Listen Command"). This command contains an index into a table of branch addresses (located in memory), and is used by the BCE to branch to the start of a new BCE program. This allows one IOP to tell another IOP when it is time to execute certain BCE programs and accept data from various subsystems.

#### 2.5.3 BCE INSTRUCTIONS

BCE instruction formats are shown in Figure 2-6 and are listed in Table 2-10.

Short Format 1 is used primarily by instructions dealing with BCE registers. It has the following fields:

<u>Field</u>	<u>Field description</u>
OP	This 4-bit field defines the basic operation to be performed by the BCE.
M	This bit serves either as an opcode extension, or as an address mode specification in address generation.
DISP	This 11-bit field serves either as immediate data or as a PC relative address displacement.



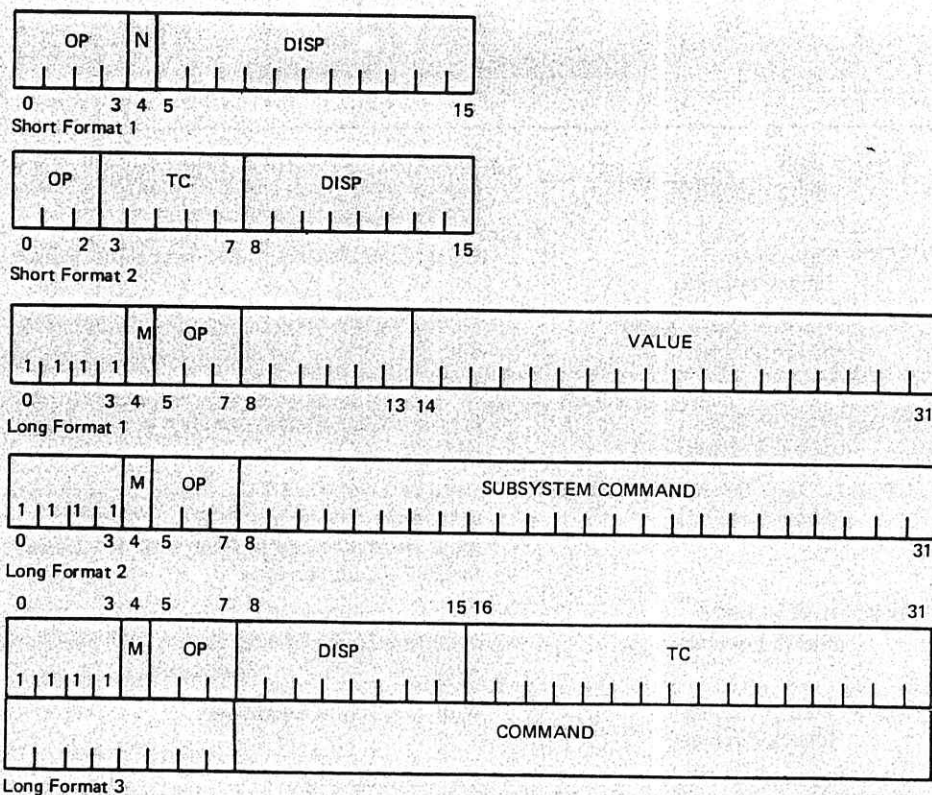


Figure 2-6. BCE Instruction Formats

Short format 2 is used by instructions that transmit and receive data. It has the following fields:

Field	Field description
OP	This 3-bit field defines the basic operation to be performed (data read or write).
TC	Transfer Count. This field defines the number of inputs or outputs to be handled.
DISP	This 8-bit field serves as a displacement off of the BCE's base register in the computation of the main memory buffer addresses associated with the I/O data.



Table 2-10  
BCE INSTRUCTION SUMMARY

WAT — Wait (Short Format)	Causes the BCE to set Busy/Wait bit to zero and enters Wait state. BCE is placed in Busy state by the MSC @ SIO instruction
STP — Self-Test (Short Format)	Initiates execution of self-test microprogram
SSC — Store Status & Clear (Short Format)	Stores BCE's Status register in a fullword address, clears its Status register, and resets Program Exception bit
SST — Store Status (Short Format)	Stores BCE's Status register in a fullword address
LTO, LTOI — Load Timeout Register (Short Format)	Used to Load Maximum Timeout register to determine how long a BCE will wait for first input word. Range is from 0 to 4.1 seconds in 16.5 $\mu$ s increments
DLY, DLYI — Delay (Short Format)	Delays execution of next instruction. DLYI specifies range of 0 to 32 ms. DLY specifies range of 0 to 4.1 s. Increment is 16.5 $\mu$ s
WIX — Wait for Index (Short Format)	Wait for Listen command
SIB — Set Indicator Bit (Short Format)	Sets Indicator bit.
IIB — Reset Indicator Bit (Short Format)	Indicator bit associated with BCE is reset
RDS — Receive Data Short (Short Format)	Directs BCE to accept the specified number of input words from its MIA
RDL, RDLI — Receive Data Long (Long Format)	Details of Receive Data instruction are given in BCE Principles of Operation Manual
MIN — Message In (Long Format)	Transmit command and then accept data
TDS — Transmit Data Short (Short Format)	Directs BCE to transmit the specified number of output words from its MIA
TDL, TDLI — Transmit Data Long (Long Format)	Details of Transmit Data instruction are given in BCE Principles of Operation Manual
MOUT — Message Out (Long Format)	Transmit command and data
BU — Branch Unconditional (Long Format)	Next instruction is executed from main memory address specified by the effective address
LBR — Load Base Register (Long Format)	BCE's Base register is loaded with main memory address as specified by effective address
CMD, CMDI — Transmit Command (Long Format)	Used to send 24-bit commands to MIA data bus-connected device. The device number is saved for future use by the Receive or Transmit Data instruction. The command will not be issued unless BCE is in Command mode

Most long format instructions use long format 1. This format provides the following fields:

<u>Field</u>	<u>Field description</u>
OP	This 3-bit field defines the basic operation to be performed by the BCE.
VALUE	This 18-bit address is used either for immediate data or as an address.
M	This bit influences how the Value field is used.

Long Format 2 is used by the Transmit Command instruction to provide 24 bits to be given to the MIA for command transmission.

Long Format 3 is used by the Message In/Out instruction to specify displacement, transfer counter, and commands.

In many BCE instructions the direct addressing mode includes automatic indexing by twice the BCE's number. This allows BCE programs to be written in a table-driven fashion, where the same BCE program can be used by many different BCEs, and yet each BCE will use a separate set of parameters in the program's execution.

#### 2.5.4 BCE LOCAL STORE AND STATUS REGISTER

BCE general registers are located in Local Store. There is a separate set of registers for each BCE. Table 2-11 lists BCE Local Store register assignments.

The information contained in each BCE Status register is listed in Table 2-12.

#### 2.6 FAULT HANDLING

GPC fault handling consists of:

- Detecting failures which can cause incorrect GPC outputs
- Identifying such failures to the appropriate GPC
- Reconfiguring the identified GPC from the redundant set; (1) automatically using hardware, (2) upon manual command or, (3) if enabled by the crew, automatically using software.

The IOP contains hardware and firmware elements to support GPC fault handling, based on status derived internal to the GPC (noncooperative) and from other GPCs or manual inputs (cooperative) (Figure 2-7).

Table 2-11

## BCE LOCAL STORE REGISTER ALLOCATIONS

Bank A	Bank B	Bank C	
WR	WR	WR	0
WR	WR	WR	1
PC	I <sub>H</sub>	I <sub>L</sub>	2
ID	MTO	Base	3
		IUAR	4
		WR	5
		Status High	6
		Status Low	7

Notes:

WR = Working registers, temporary storage for:

a) DMA address and data high, low

b) Word Count normally A1

I<sub>H</sub> = Instruction Register High

I<sub>L</sub> = Instruction Register Low

ID = BCE Identity Register =  $2 \times \text{BCE \#}$

MTO = Maximum Timeout Register

Base = Base Register

IUAR = Interface Unit Address Register

Status High, Low = Status Register

## 2.6.1 FAULT DETECTION

The following IOP elements are used to support GPC fault detection.

2.6.1.1 Error Interrupts

Error conditions detected by the IOP which result in the generation of an interrupt to the CPU are described in Table 2-13.

2.6.1.2 MSC Status Indicators

Error conditions detected by the MSC which result in the setting of an MSC status indicator are described in Table 2-14.



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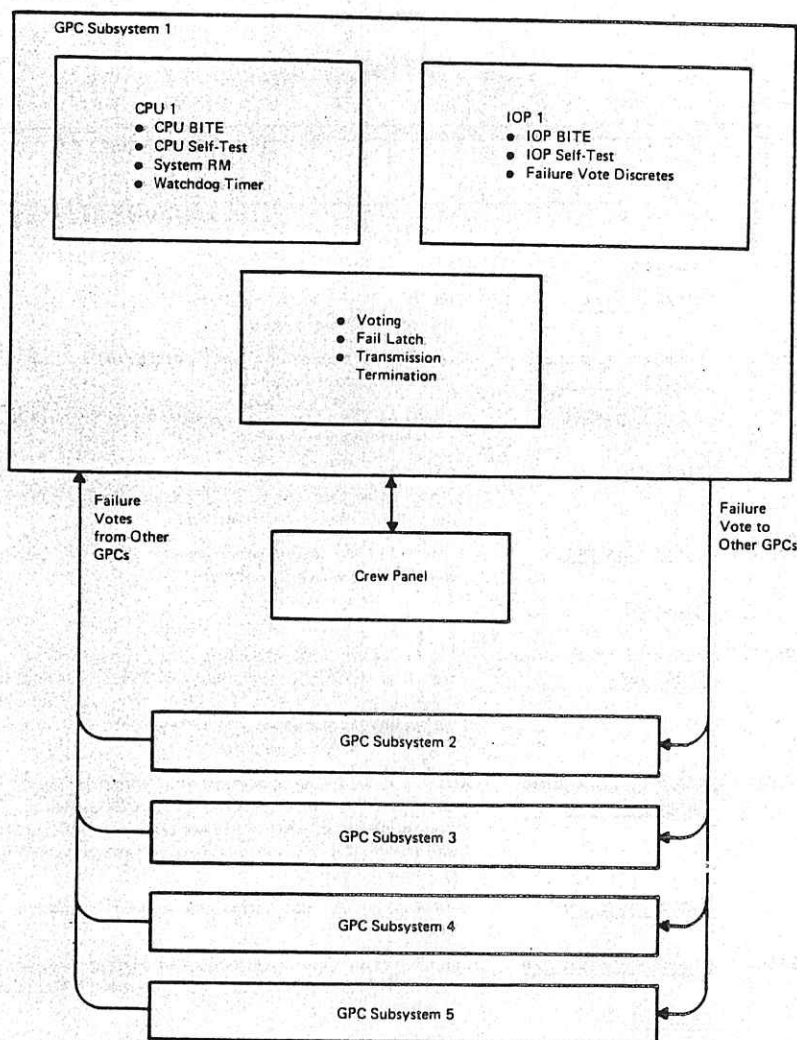


Figure 2-7. Functional Summary of Fault Detection

### 2.6.1.3 BCE Status Indicators

Error conditions detected by the BCE which result in setting a BCE status indicator are described in Table 2-15. Note that, should a BCE receive an invalid listen command while executing a wait for index instruction, no status bit is set, and the command is ignored. (An invalid listen command is one which does not have an IOP address, incorrect parity/bit count/data sync, or a nonvalid Manchester code.)

Table 2-13

## IOP INTERRUPT DETECTED ERRORS

Error	Detected by	Action
Microstore Parity Error	Microdecode Logic	Set Interrupt 16D IOP resets and sets C/M Idle Interrupt 16C
Clock Failure	Timing Detect Logic	Set Interrupt 16E IOP resets and sets C/M Idle Interrupt 16C
Watchdog Timer Timeout	R/M Logic	Set Interrupt 16A If Term Control is "ON"; IOP resets and sets C/M Idle Interrupt 16C
Voter Fail Latch	R/M Logic	Set Interrupt 16B If Term Control is "ON"; IOP resets and sets C/M Idle Interrupt 16C
DMA Parity Error PCI/PCO	Channel Control Logic	Set Interrupt 17A Aborts transfer within IOP and clears channel IOP continues with the next request
DMA Parity Error Instruction Read	Channel Control Logic	Set Interrupt 17B Force illegal OP Code 0 IOP continues with the next request
DMA Parity Error Data Read	Channel Control Logic	Set Interrupt 17C Abort transfer to Local Store IOP continues with the next request (MSC and BCE may loop indefinitely)
Burst DMA Excess (greater than 64)	Channel Control Logic	Set Interrupt 17D Disable Burst mode IOP continues with the next request (burst enabled by PCO)
Queue Overflow	Channel Control Logic	Set Interrupt 17E IOP continues with the next request (new requests are lost if queue is full)
DMA Cycle Timeout	Channel Control Logic	Set Interrupt 17F Clear DMA channel IOP continues with the next request (information will be lost)

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Table 2-14

## MSC FIRMWARE DETECTED ERRORS

Error	Detected By	Action
Illegal instruction opcode	Microcode	Set MSC program exception bit. Set status bits 15 and 16. Enter Wait state.
32-bit instruction starting on odd boundary	Microcode	Set MSC program exception bit. Set status bits 14 and 16. Enter Wait state.
Attempt to start busy BCE	Microcode	Set MSC program exception bit. Set status bits 11 and 16. Continue instruction.
Attempt to load PC of busy BCF	Microcode	Set MSC program exception bit. Set status bits 12 and 16. Continue instruction.
Attempt to load base of busy BCE	Microcode	Set MSC program exception bit. Set status bits 13 and 16. Continue instruction
Attempt @SIO with ACC [0] = 1 (See @SIO)	Microcode	Set MSC program exception bit. Set status bit 11. Continue execution

2.6.1.4 Redundancy Management (RM) Status Indicators

A register in the IOP is used to store the status of the IOP hardware dedicated to fault detection and identification (Subsection 3.7). This register, in conjunction with other IOP test registers and logic, is under PCO and PCI control and is used to validate the RM hardware logic shown in Figure 3-26.

2.6.1.5 Watchdog Timer

A watchdog timer, loaded by PCO, is used, (1) to detect failures which affect cyclic program execution in the CPU, and (2) as a means of indicating the GPC has failed after fault detection by the CPU. Whenever time loaded into the timer elapses; a timeout latch is set to identify the failure to that GPC (see Subsection 3.7 for hardware description of timer).

Table 2-15

## BCE FIRMWARE DETECTED ERRORS

Error	Detected by	Action		
		Status Bit Set?	Wait State Entered?	Other
Illegal instruction	Microcode	Bit 29	Yes	Write all 0's into Instruction register (illegal opcode) CPU interrupt
Long Format instruction on odd boundary	Microcode	Bit 28	Yes	
DMA channel parity error on instruction read	Channel Logic	(See Illegal instruction)		
DMA channel parity error on data read for transmit data instruction	Channel Logic Microcode Time-Out	21	Yes	CPU interrupt
Excessive concurrency resulting in $\leq 20 \mu s$ gap in transmit data	Microcode Time-Out	21	Yes	(Note: MOUT = Error Detected for GAP > 5 $\mu s$ )
Transmitter disabled during transmit data	Microcode Test	23	Yes	Save IUA from data. Data is not stored
Transmitter busy at wrong time during transmit data	Microcode Test	23	Yes	
Parity error on input data	MIA	4	Yes	
Wrong SEV bits	Microcode/ Hardware	5, 6, 7	Yes	Data is not stored
Command sync in receive data (except for first word)	Microcode	15	Yes	Data is not stored (See #RDS)
Wrong IUA in incoming data	Microcode/ Hardware	3	Yes	(See #RDS)
Failure of subsystem to respond with data	Microcode Time-Out	25	Yes	Data is not stored
Excessive interword gap in incoming data	Microcode Time-Out	26	Yes	
Wrong bit encoding, too short, too long word on bus (bit count errors)	MIA/Microcode Time-Out	26	Yes	

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#### 2.6.1.6 MSC Timeout

The MSC instruction set includes an instruction termed "Repeat Until All Waiting" which can be used to detect GPC faults, on a cooperative or noncooperative basis. If all of a set of specified BCEs have set their busy/wait bits to wait before a specified timeout (set under BCE software control), the MSC skips the next halfword instruction and continues. If a timeout occurs, the MSC begins execution of the next instruction. If a timeout occurs because a BCE in the Command mode is still busy after it executes its transmit program, that condition represents a GPC failure which can cause incorrect output. If a timeout occurs because a BCE in the Listen mode is still busy after expecting a listen command or a subsequent subsystem command from another GPC, that condition represents a failure in a GPC or bus.

#### 2.6.1.7 MSC Self-Test

Microcode exists in the IOP which is dedicated to detecting MSC failures. This microcode is executed with an MSC instruction (@ STP) and consists of testing the following hardware:

- MSC local store
- ALU 1 and 2 operations/MSD data flow
- MSC/Main store data flow
- MSC/RM hardware control
- ROS parity circuit.

When an error is detected, the MSC No-Go and MSC status bit 9 is set, and the MSC continues to the next instruction.

#### 2.6.1.8 BCE Self-Test

Microcode exists in the IOP which is dedicated to detecting BCE failures. This microcode is executed with one of two BCE instructions (#STP0 and #STP1). BCEs in the Command mode can be tested using #STP1, which tests the following hardware:

- BCE local store
- ALU 1 and 2 operations/BCE data flow
- BCE/Main store data flow
- MIA data flow and MIA buffer (using wrap test).



BCEs in the Listen mode can be tested using #STP0, which is the same as #STP1 but does not include testing the associated MIA data flow and buffer. When an error is detected, the BCE No-Go and BCE status bit 22 is set and the BCE goes to the Wait state.

#### 2.6.1.9 Compare Word Test

The MSC is capable of making a comparison of "compare" words received from other GPCs with a compare word transmitted to them, counting the number of noncompares associated with a particular GPC, and interrupting the CPU should a GPC be determined as failed using this technique.

#### 2.6.2 FAULT IDENTIFICATION

The IOP elements which support GPC fault identification are contained in the hardware which is described in Subsection 3.7. This hardware makes use of status internal to the GPC and status going to and coming from other IOPs. The hardware automatically identifies a computer as failed by setting a GPC fail discrete. In addition, the hardware is used to transmit fail vote (discrete) status to the other GPCs under control of the MSC. A GPC fail discrete is set by hardware when, (1) the GPS receives two or more fail votes, or (2) its watchdog timer times out.

#### 2.6.3 RECONFIGURATION

The IOP provides both automatic and manual reconfiguration of a GPC when a critical failure is detected and identified. Reconfiguration involves removal of a GPC from functioning as a member in a redundant set. The following IOP elements are used to support GPC reconfiguration.

##### 2.6.3.1 Transmission Termination Control

The IOP contains hardware whose status determines whether automatic reconfiguration under software control has been enabled. The logical output of two latches, both under PCO control, are used to control automatic IOP bus transmission termination and resetting of all discrettes under PCO control, should a GPC failure be identified by the watchdog timer or voter.

##### 2.6.3.2 IOP Fail Reset

Whenever an IOP clock failure, an IOP ROS parity is detected, a timeout occurs with the timer control latch set, or a voter latch is set with the voter control latch set, an IOP fail reset is generated. The IOP fail reset signal will reset the IOP hardware in accordance with Table 3-3.

#### 2.6.3.3 Failure Vote Inhibit

When a GPC is identified as failed by either cooperative or noncooperative means, its failure votes to the other GPCs are automatically inhibited.

#### 2.6.3.4 Halt Discrete

A Computer Mode switch (one for each GPC) is provided to the crew as one method for manual control of the redundant GPC set. Position 1 (presently Halt) forces the GPC system reset to be raised and causes a power-on reset of the GPC without power cycling. When the Computer Mode switch located on D&C Panel 07, is set to Position 1, a discrete input is generated to the dedicated GPC and all latches in the RM hardware (including the timeout latch and timer termination control latch) will be reset. All output discrettes from the GPC will also be reset. The watchdog timer will be set to zero and not be counting while the halt discrete is set.

#### 2.6.3.5 IOP Terminate Commands

Additional switches are available on a D&C Panel 07 for manual control of data transmission over specific (critical) data buses.

##### 2.6.3.5.1 IOP Terminate Cmd A

When the Computer Output switch on D&C Panel 07 is in the TERMINATE position, a discrete input is generated to the GPC to terminate data transmission over data buses FC1 through FC4 (GPC data bus ports 10 through 13). When the switch is in the NORMAL position, the IOP will initiate/continue normal data transmission of these buses.

##### 2.6.3.5.2 IOP Terminate Cmd B

If the Computer Output switch is in the TERMINATE position or if the Backup Flight Control System (BFCS) Engage Switch/Indicator, located on D&C Panel F6, is on, a discrete is sent to the GPC to terminate data transmission over data buses FC5 through FC8, PL1 and PL2, and LB1 and LB2 (GPC data bus ports 14-16, 20-21 and 22-23). When the Computer Output switch is in the NORMAL position and the BFCS Engage Switch/Indicator is OFF, the IOP is to initiate/continue normal data transmission over the indicated data buses.

#### 2.6.3.6 Power-Off Interrupt (POI)

A signal is generated from the IOP to the CPU when either 28 VDC primary power falls below the specified minimum steady state value; or a power transient, having a duration greater than 2 ms, occurs on its primary power lines. One-hundred microseconds after receipt of this signal, (1) the mainstore operations are inhibited, (2) the CPC discrete interfaces are reset, and (3) all IOP data bus transmission and reception is terminated. (Once the power down sequence has started, the sequence will continue to completion regardless of the subsequent power line status.)



## 2.7 INITIAL PROGRAM LOADING

Initial Program Loading (IPL) is used to write valid programs into the main memory when invalid programs, or no programs, are resident in core storage. A normal turn-on sequence does not require IPL, since main memory is a core storage device (non-volatile). Programs are not lost by power transients or power removal. IPL is required when main memory must be reloaded. The following paragraphs briefly describe the GPC sequencing and interfaces to perform IPL.

Figure 2-8 summarizes the cockpit controls and subsystems involved with IPL. The programs are written into main memory from the mass memory unit (MMU). Program loading is specified by keyboard entries through the Multipurpose CRT Display Subsystem (MCDS). Table 2-16 lists the basic procedure required for each subsystem.

### 2.7.1 GPC MODE CONTROL

As shown in Figure 2-8, a mode switch is used to place a GPC into the following states:

- Halt — The CPU and IOP are held in a Reset state. All I/O operations are inhibited and program execution is inhibited.
- Standby — Limited processing is allowed by software control to communicate with MM and MCDS over nonflight-critical data buses. The operation of a GPC can be monitored to determine its condition.
- Run — Full operational capabilities are conducted in this mode.

### 2.7.2 COMPUTER INITIAL PROGRAM LOAD

The sequence of IPL operations (Figure 2-9) internal to the GPC are discussed here. Also described are the elements which perform each step (IOP hardware, IOP microroutine, or CPU microroutine).

The IOP hardware detects the IPL signal while in the Halt mode to initiate the IPL process. This hardware resets the IOP, and sets the IPL STATUS indicator on the panel. The reset hardware stops the CPU, resets all discrete outputs, disables the MIA transmitters and receivers, resets internal IOP timers, and forces all MSC and BCE to the Halt state. The CPU is stopped by raising the System Reset line (Figure 2-14). Concurrently, the Lockout signal is also raised. At the completion of this step System Reset is dropped, allowing the CPU microroutine to execute.

The IOP microroutine samples the IPL discretes from the mass memories to determine which mass memory to use for loading the main memory. If neither discrete is set, the IOP microroutine will continue to sample the discretes until at least one is set. If only one discrete is set, the corresponding mass memory will be selected as the load source. If both discretes are set, the IOP microroutine will select mass memory 1 as the load source. The MSC and the appropriate BCE communicate as outlined in Table 2-17.



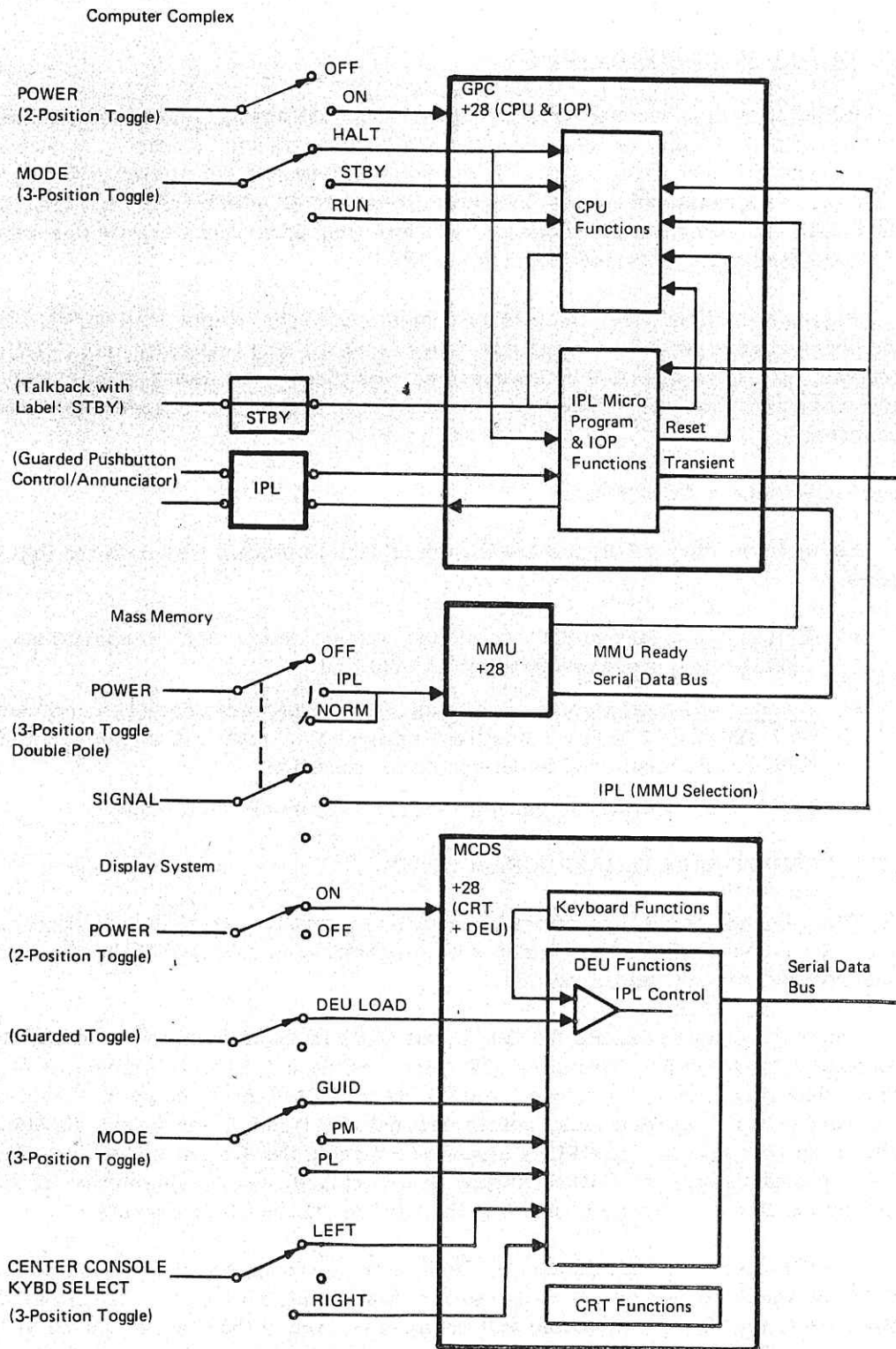


Figure 2-8. Cockpit/GPC/MMU/MCDS Functional Interface Summary

Table 2-16

GCP AND DEU LOAD PROCEDURE

Mass Memory

Mode to IPL

GPC

Mode to HALT

Power On

IPL (Momentary)

Load\*

IPL Status Light OFF\*

Mode to STBY

Standby Status Light ON\*

Mass Memory

Mode to NORM

DEU

Power On

Mode to DEU LOAD

Depress Enter Key

Load\*

LOAD COMPLETE Message on CRT\*

Mode to NORM

Load Complete — Ready for Initialization

\*Automatic Response

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Table 2-17  
IOP IPL MICROROUTINE SEQUENCE

MSC	BCE
<ol style="list-style-type: none"> <li>1. After release from Halt, if IPL is true write SPV call to all locations in Main Store</li> <li>2. Start the BCE not in the Halt mode</li> <li>3. Wait for the BCE doing IPL to turn on its indicator</li> <li>4. Read first IPL word from Main Store to determine block size</li> <li>5. Store in BCE Local Store and wait for BCE indicator to go off.</li> <li>6. Start BCE for verify sequence</li> <li>7. Read first word of IPL block from Main Store and wait for indicator on</li> <li>8. Compare word read above with word in location N+1</li> <li>9. If OK not last word send BCE to Step 5 and delay until indicator off</li> <li>10. When indicator on, go to Step 7 next word, or if last word write SPV call in N+1, set IPLC and BCE to Halt.</li> </ol>	<ol style="list-style-type: none"> <li>1. Begin reading mass memory and storing in Main/Store when MMR is activated. Compare word count to a pseudo block size number</li> <li>2. When first word is stored, turn the indicator on</li> <li>3. Continue reading and storing data until stored block is equal to block size with no errors</li> <li>4. Turn off indicator</li> <li>5. Reset indicator. Read first IPL word and load in location N+1</li> <li>6. When word is stored in N+1 set indicator</li> </ol>

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To verify that the IPL program has been successfully stored, the IOP micro-routine again initializes the BCE to repeat the data transfer from mass memory. This time, an MSC program is also initiated to compare the incoming data with that from main memory, rather than storing into main memory. Successful completion of this step verifies that the data were properly received and stored.

The IOP then issues a signal that the IPL sequence is complete (IPLC) and enters the Halt state. The IOP hardware disables the BCE transmitter and receiver on the selected mass memory channel. The storage protect control is set to the No Protect state. The IPL STATUS indicator on the panel resets to indicate successful completion of the IPL process. The System Reset line is raised to disable the CPU, followed by dropping the Lockout line.

The IPL process is now ended. The current GPC state results from applying power to the GPC with the mode switch at Halt, without using the IPL switch. All subsequent operations are controlled by the GPC software when the Standby or Run mode is selected. The crew must remove the mass memory from the IPL status.

If any error is detected during the IPL process, the process is stopped without resetting the IPL STATUS indicator. The crew is alerted to an error in the IPL process by failure of this indicator to reset after a reasonable time. The crew is responsible for all error recovery or retry procedures by cycling power to the GPC.

Moving the GPC mode control to STBY following IPL causes the System Reset line to fall, with the Lockout line in the Off state. The CPU, therefore, always begins operation at the location specified by the System Reset PSW following an IPL operation. The information stored into this location from mass memory during the IPL process must direct the software to an IPL Cleanup program.

During the IPL process, all memory locations were loaded as store-protected. The Cleanup program must remove the store protection from selected memory locations before any store operation is attempted. The exact locations will depend on the programs in memory. However, as a minimum, it will be necessary to enable writing into all interrupted old PSW locations. The Cleanup routine must also change the System Reset PSW to point to a true System Reset routine instead of the IPL Cleanup routine.

The IPL process does not load the application programs into memory, although all of FCOS may be loaded. The crew must communicate with the program via the DEU to complete the load process.

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SYSTEM ELEMENTS

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## Section 3

### SYSTEM ELEMENTS

#### 3.1 INTRODUCTION

The IOP subsystem design is described in this section. Figure 3-1 is an overall IOP block diagram showing the major hardware elements and the major signal flow paths. Figure 3-2 gives more detail and relates the block diagram to the system elements described later in this section. IOP subsystem elements are

- Channel Control - Controls the communication between the IOP and the CPU over the 32-bit, bidirectional I/O channel. It routes the information from the CPU to the control monitor, the processor element, and redundancy management hard logic as required. Requests by the IOP for access to main memory are also handled by the channel control element over the 18-bit memory address channel and I/O channel.
- Control Monitor - Performs many of the miscellaneous control functions. These include control of power-on/power-off sequencing, control of MIA transmit and receive enables, and the processing of discrete inputs and outputs.
- Processor Element - The microprogrammed device which performs the processing and data handling for the MSC and BCE processors. The processor element includes microstore and decode, local store, and data flow elements.
- Direct Memory Access Queue - A 64-word deep first-in-first-out (FIFO) buffering device for holding stacked requests for information from main store.
- Multiplex Interface Adapters and MIA Buffers - Interface between the IOP and the 24 1-MHz serial data buses. The 24 separate MIAs convert the parallel IOP data into the serial data bus formats, add the sync pattern, a parity bit, and encode the data for the bus. Conversely, the MIAs also receive the data from the bus; decode it; check the sync pattern, number of bits, and parity; and convert it into parallel data for the IOP. The MIA one-word buffers for the 24 MIAs assure that information is not lost because of timing interference.
- Redundancy Management Hard Logic Element - Has two functions. The watchdog time-out timer must be updated periodically or it indicates a failure. The failure vote logic distributes failure indicators to the other IOPs and votes the inputs from the other IOPs.

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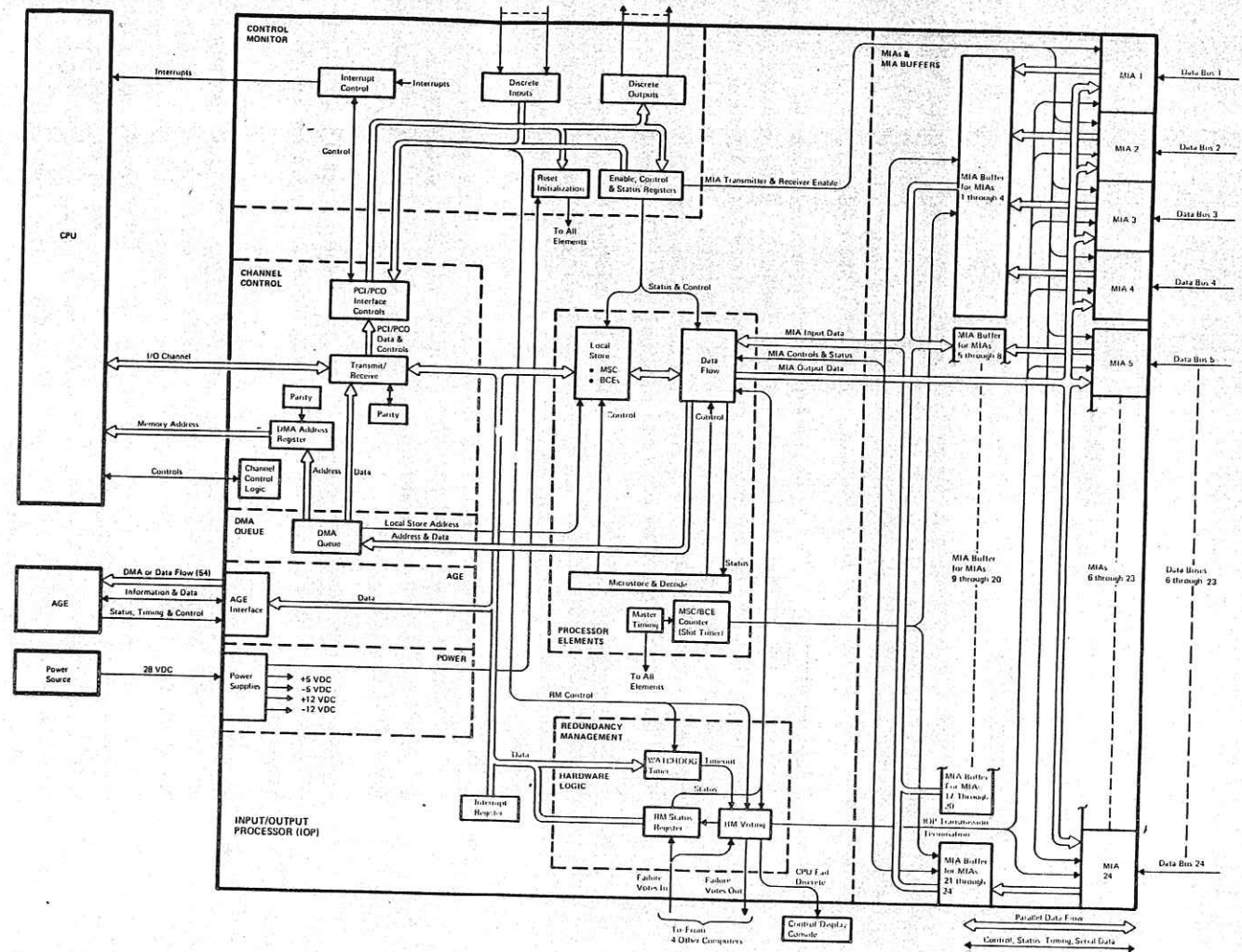


Figure 3-1. IOP Elements



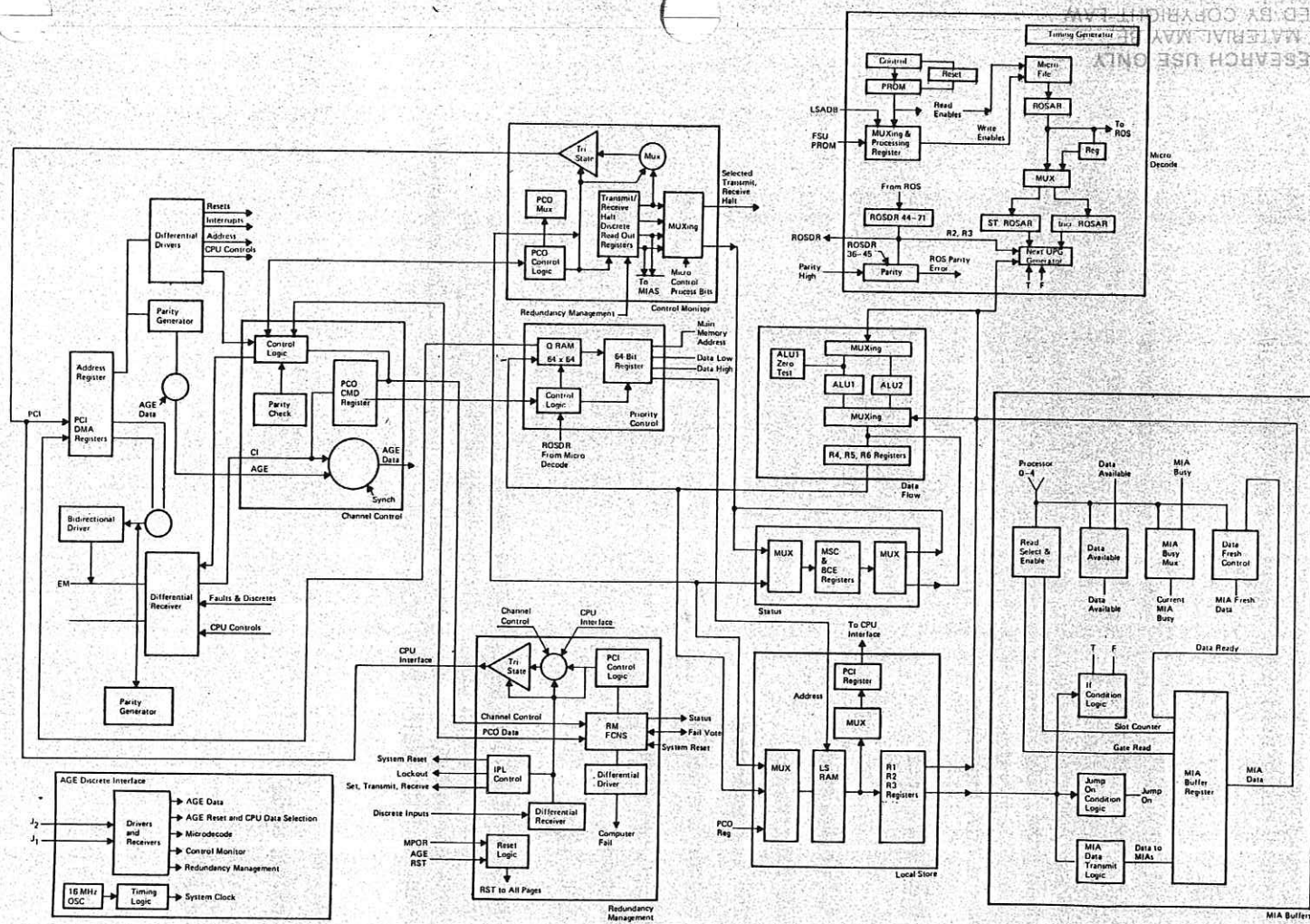


Figure 3-2. Detailed System Diagram



- Power Supply — A standard IBM System/4 Pi modular power supply identical to that used in the AP-101 Computer. It contains DC-to-DC converters, controllers, etc., to generate -12 VDC, +12 VDC and +5 VDC.
- AGE Interface — A common interface with test equipment. This allows the IOP to be exercised under controlled conditions and the results monitored.

### 3.2 MIA AND BUFFER

A network of twisted, shielded-pair data buses, each terminated with multiple parallel connections, provides communication paths within the Shuttle subsystems. Subsystem data flow over these buses in 1-MHz serial Manchester II code (described later). The MIAs interface between these buses and the IOP elements. An IBM-designed MIA, described here, will service the development and prototype IOPs. IBM's device is functionally equivalent to other MIAs but will be packaged for IOP installation. The general MIA functions are as follows:

- Transmit and receive data
- DC isolation
- Parallel/serial conversion
- Serial/parallel conversion
- Sync generation and detection
- Manchester encode and decode
- Parity generation and detection
- Bit count detection
- Provide status to BCE.

Each IOP is interfaced with 24 data buses and therefore will contain 24 MIAs. The MIA circuits are packaged four to a page. All functions in these all-hardware MIAs are handled by logic (no software). Each MIA operates completely asynchronously from the others and from the IOP itself. Each MIA can be functionally subdivided into several parts:

- 24 bit data register
- Timing and control logic
- Transmitting circuits
- Receiving circuits.

### 3.2.1 SERIAL DATA BUS MODULATION SCHEME

The Shuttle data buses information appears in Manchester II code. In this biphas-level code, the value of a bit is represented by a polarity shift at the mid-point of the bit time. A "1" is represented by a + to - ( $1 \rightarrow 0$ ) shift, while a "0" is represented by a - to + ( $0 \rightarrow 1$ ) shift, as shown in Figure 3-3.

With this code, polarity always changes at the bit time mid-point. However, there may not be a change at the bit time boundaries. If adjacent bits are the same, there is a polarity change, but if adjacent bits are different, there is no polarity change. Other features of Manchester II code include

- DC Balance - Each bit is DC balanced, which prevents build up of DC bias and makes data easily transmitted via AC coupling circuits.
- Self-Clocking - When polarity changes at the middle of a bit time, a separate clock or reference signal is not required. Self-clocking also relieves the problem of skew due to unequal delays.

Some sample bit combinations are shown in Figure 3-4.

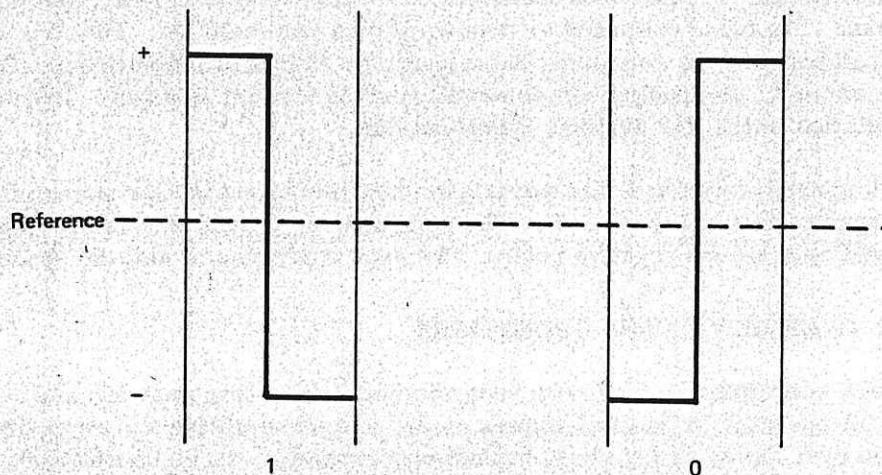


Figure 3-3. Biphas-Level Manchester II Code Modulation Scheme

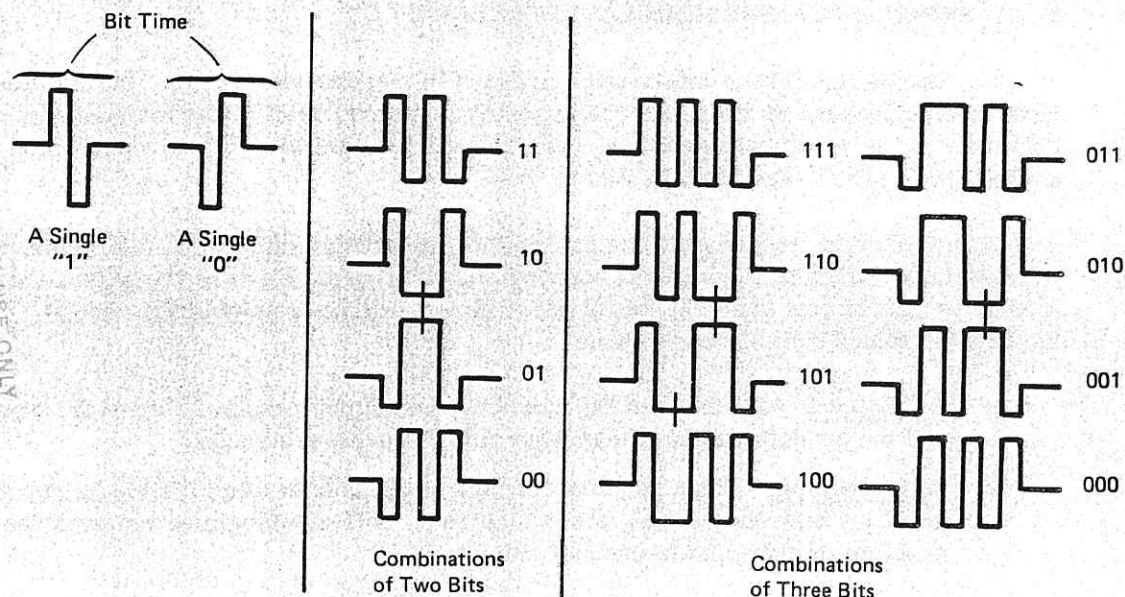


Figure 3-4. Sample Manchester II Code Bit Combinations

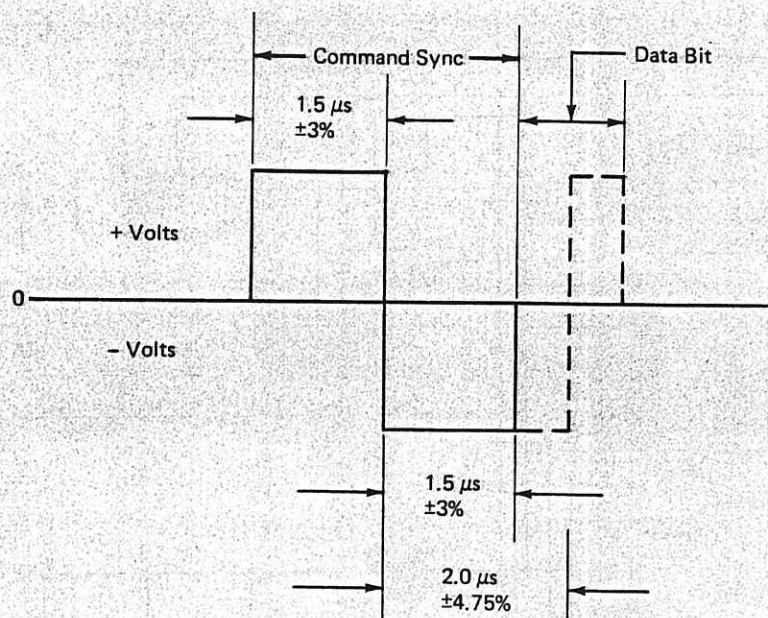
The Shuttle avionics data buses use a 1-MHz serial data rate, which give a 1- $\mu$ s bit time. The basic command or data word on a bus is 28  $\mu$ s. The first 3  $\mu$ s are a sync pattern, and the remaining 25  $\mu$ s contains 25 bits of information. There is a minimum of 5  $\mu$ s spacing between each word on a given data bus. The various formats are detailed in the IOP Systems Specifications.

Command words and data words are identified by their 3- $\mu$ s nonvalid Manchester code sync patterns (Figure 3-5). The command word sync is a 1.5- $\mu$ s positive pulse followed by a 1.5- $\mu$ s negative pulse. The data word sync is just the opposite.

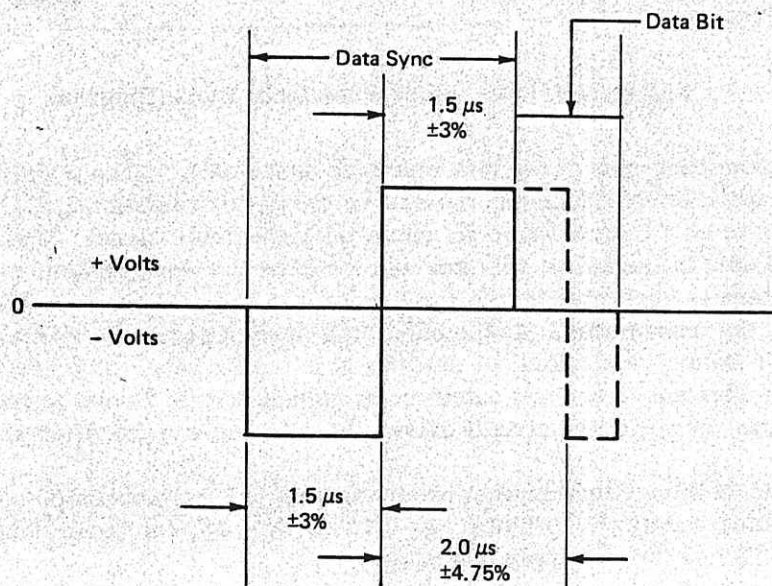
### 3.2.2 OVERVIEW OF MIA OPERATIONS

MIA operations occur in two separate activities: transmission and receiving. The MIA operates in the Half-Duplex mode, and transmitting and receiving are performed over the same data bus, but not concurrently. To be operational, each MIA must have its particular Transmit Enable or Receive Enable bit set in the Enable registers located in the control monitor. A simplified block diagram is shown in Figure 3-6. Note that all MIA words are formatted in the BCE except for the sync pattern and the parity bit. Bits 4 through 27 are transmitted between the MIAs and BCEs.





a. Command Word Sync



b. Data Word Sync

Figure 3-5. Command and Data Word Sync

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The MIA receiver (assuming it is enabled) continuously monitors the associated bus. Input threshold detectors look for either a positive or negative signal exceeding 0.5 V (noise threshold). When a signal (either positive or negative) arrives, it starts a timer that monitors the signal state for 1313 ns. If the state does not change, the signal is probably a sync pattern, and the testing continues. The circuit then checks whether the input changes polarity between 1313 and 2125 ns. If so, the input is considered a valid sync pattern, and the data are shifted in through a Manchester decoding circuit.

The decoded data are serially clocked into the 24-bit register. The parity bit is checked against the actual received parity, and the received bits are counted. If the count of received bits is not exactly 25, the information output is inhibited by the 24-bit register. For a parity error, the information is outputted, but the BCE is notified of a parity error.

### 3.2.3 IOP/MIA INTERFACE AND TIMING

Interface signals between the IOP processor elements and each MIA are described in Tables 3-1 and 3-2. The MIA signals are illustrated in Figure 3-7. Certain of these signals are common to all MIAs, and some are unique to each MIA. There are also MIA-to-BCE signals common to the four MIAs on an MIA page; the status of these signals is also given in the two tables.

Interface signal timing is shown in Figure 3-7, along with some of the internal MIA signals. Signal generation is discussed in Subsection 3.1.5.

### 3.2.4 INDIVIDUAL CIRCUITS

#### 3.2.4.1 24-Bit Register

The 24-bit shift register provides parallel-to-serial conversion for IOP output data and the serial-to-parallel conversion for IOP inputs from the data buses. When the MIA is to transmit a word, 24 bits of parallel data are transferred over the MIA data bus and placed in the register. The Data Available signal sets the register and starts the timing for the word transmission. Following the transmission of the correct sync pattern, a register clock signal shifts the data out of the register, most significant bit (MSB) first, at a 1-MHz serial data rate to the Manchester converter.

When receiving data, the serial data stream, after the Manchester code is removed, is shifted into the register at the 1-MHz rate. After the last bit is received, and all receiver data checks are satisfied, the data are ready to be transferred in parallel to the IOP data flow element. The 24-bit register is a tri-state device with a "1", "0", or high-impedance output state for each bit. The register's parallel output is normally left in the high-impedance state to reduce loading on the other MIA registers paralleled together. When data are to be transferred, the register output is enabled and the "1" and "0" levels are transferred to the MIA buffer. The MIA Data Ready signal notifies the buffer that the data are ready. Since four MIAs per page are bussed together, the data will be transferred during the time slot allocated to the individual MIA. This time slot is entirely independent of the MSC/BCE time slots.



Table 3-1

## PROCESSOR ELEMENTS TO MIA SIGNALS

Signal	Description	Status
MIA Data Out Bus	24-bit parallel bus to be used to transfer 24-bit words from the data flow element to the MIA	Common
Data Available	Inform the MIA that a word has been placed on the MIA Data Out bus which should be accepted into the MIA and transmitted over the Serial Data bus. The word on the MIA Data Out bus must be valid any time this signal is active	Unique
Command	Inform the MIA that the current word transferred to the MIA for transmission is a command word. The MIA will prefix this word with a command sync for serial transmission. This signal must be active for exactly the same time as its associated word bits on the MIA Data Out bus	Common
Transmit Enable	This signal enables serial transmission by the MIA. This signal must be active a minimum of 100 ns prior to the Data Available signal and remain active as long as serial transmission is desirable	Unique
Receive Enable	This signal in the active state allows the MIA receiver to operate normally. When this signal is inactive, the MIA will not transfer received words from the MIA to the IOP.	Unique
Clock	A 16-MHz clock signal is used in the MIA for control purposes	Common
Reset MIA	This signal resets all registers, flip-flops, and latches in the MIA to a fixed state. The MIA will operate normally upon removal of this signal	Unique
+5 V to MIA	Input voltage to MIA. +5 VDC ±5% at TBD W	Common
-5 V to MIA	Input voltage to MIA. -5 VDC ±5% at TBD W	Common
+12 V to MIA	Input voltage to MIA. +12 VDC ±5% at TBD W	Common
-12 V to MIA	Input voltage to MIA. -12 VDC ±5% at TBD W	Common

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Table 3-2  
MIA TO PROCESSOR ELEMENTS SIGNALS

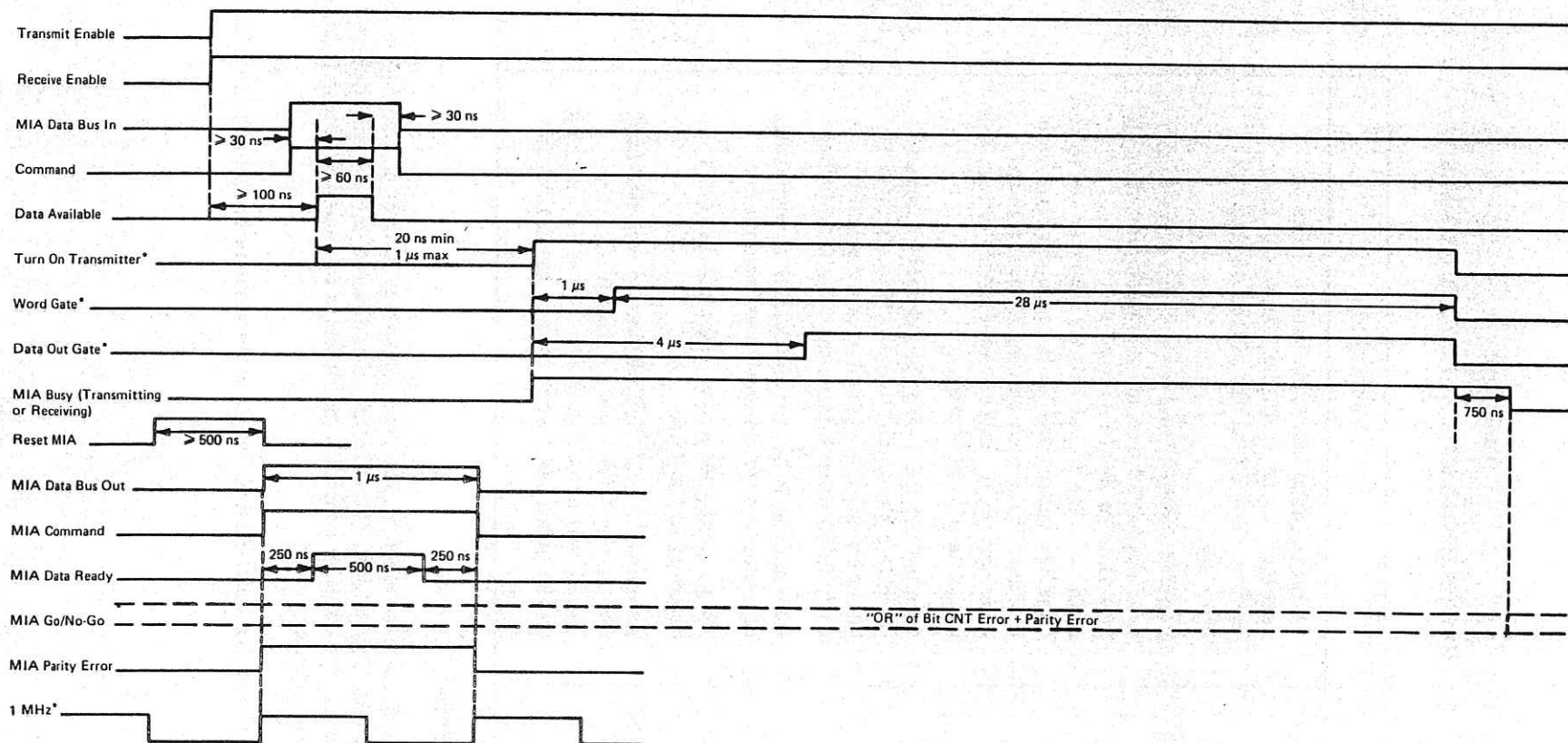
Signal	Description	Status
MIA Data In Bus	24-bit parallel bus to be used to transfer received words from the MIA to the MIA Buffer. Word bits are placed on this bus for 1 $\mu$ s	Common to page
MIA Data Ready	Informs the BCE that a word has been received over the Serial bus and has been placed on the MIA Data In Bus to be accepted by the MIA Buffer. This signal will be a 500-ns pulse and signifies valid word bit time on the MIA Data In Bus. If the MIA senses an error in the received word, other than a parity error, this signal is not generated.	Unique
MIA Command	Informs the BCE that the current received word is a Command word. This signal will be active for the same 1- $\mu$ s time as the associated word bits on the MIA Data In bus	Common to page
MIA Busy	Informs the BCE that the MIA is transmitting or receiving words on the serial data bus	Unique
MIA Go/No-Go	This signal goes active when any error is detected in the MIA	Unique
MIA Parity Error	Informs the BCE that bad parity was detected for the word received on data bus. This signal will be active for the same 1- $\mu$ s, time as the associated word bits on the MIA Data In Bus	Unique

#### 3.2.4.2 MIA Clocks

The basic IOP 16-MHz clock signals are frequency divided to provide 8-, 4-, 2-, and 1-MHz MIA clocking pulses. In addition, there is a 1-MHz signal delayed 0.25- $\mu$ s. These clock signals are used by control logic circuits to generate gating pulses and specialized clock signals.

Figure 3-7 shows the relationship between the various MIA clock signals.

3-12



Note: Times are not to scale.  
All times are nominal.

\* — MIA Internal Signals.

Figure 3-7. IOP/MIA Interface and Timing Signals

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### 3.2.4.3 MIA Transmitting Circuits

The MIA provides the following functions to transmit a word:

- Generate the timing signals
- Generate the sync pattern
- Convert the data to Manchester II code
- Generate the correct parity bit.

The transmit timing generator is a 32-bit shift register that is enabled by the Transmit Enable signal, started by the Data Available signal, and is shifted at a 1-MHz rate. Output pulses are used at T0, T2 (2  $\mu$ s), T4 (4  $\mu$ s, etc.), T27, T28, and T29. In addition, the internal signals; i.e., word gate, Turn On Transmitter, and Data Gate; are supplied by the transmit timing generator (Figure 3-8).

The first step in outputting a word to the data bus is generating the sync pattern. At T1 time, the sync generator starts outputting the sync pattern. If a command word is desired, a flip-flop is preset to a "1" state. If a data word is desired, the flip-flop is left at "0". At time T2.5, the flip-flop is clocked, changing its state to the opposite value. At T4, the sync-generator is disabled and the 24-bit data register starts clocking out data serially to the Manchester converter.

Each data bit, as it enters the Manchester converter, sets a flip-flop at the beginning of its bit time. A "1" sets the flip-flop equivalent to an up level; a "0" sets it to a down level. At the midpoint of the bit time, the flip-flop is forced to the opposite state. At the next bit time, the flip-flop is set or reset and the cycle repeated.

The Manchester-coded serial bit stream is coupled to the transmitter line driver of the MIA. This stage is independently enabled and disabled by the Turn-On Transmitter gate (Figure 3-8), which prevents spurious signals from being outputted onto the data bus. The Turn-On Transmitter gate is controlled by the Transmit Enable signal from the Transmit Enable register in the control monitor.

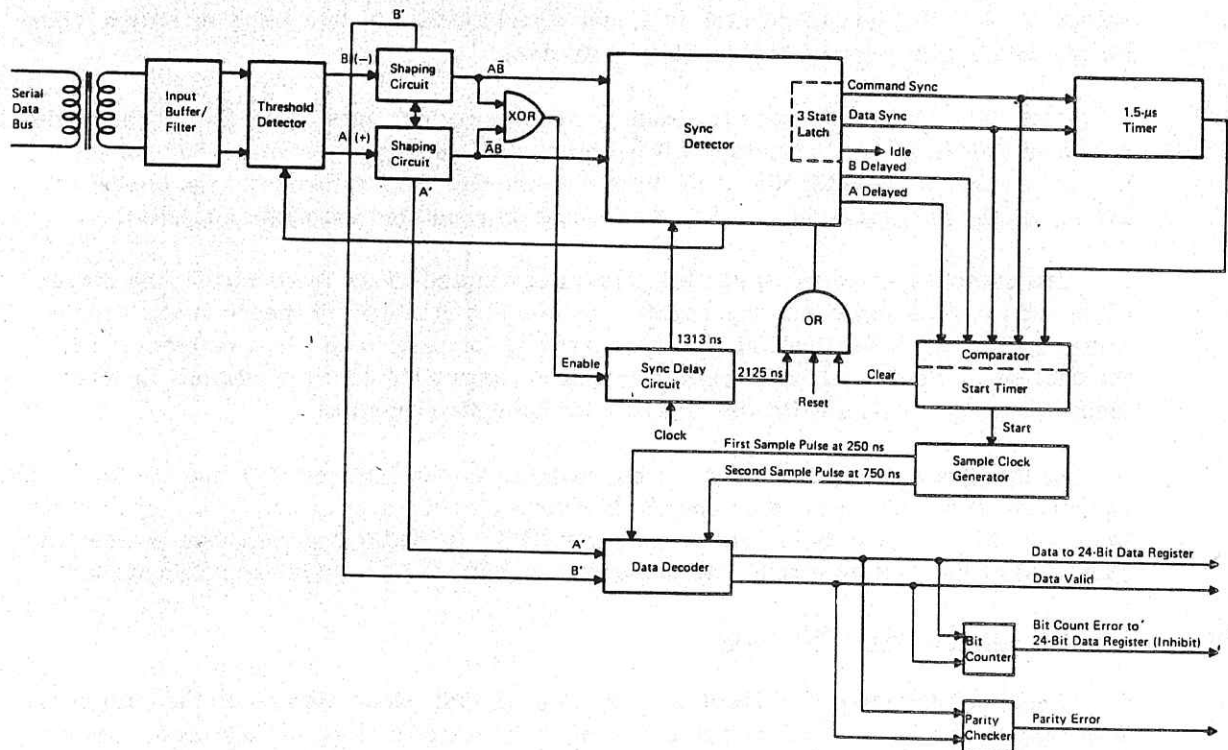
As the data are being clocked out between the 24-bit data register and the Manchester converter, the parity generator counts the number of "1" bits in the word. Following the last data bit, a parity bit will be output at T28. If the bit accumulation is even, a parity bit of "1" will be output. With an odd number, the parity bit remains at "0."

### 3.2.4.4 MIA Receiving Circuits

The receiving operation involves receiving asynchronous signals on the data bus, detecting when a valid sync pattern is received, locking the internal timing to the incoming pattern, and sampling the data to extract the encoded information. Next, the receiving circuits check the total bit count and received parity.

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- Input Buffer/Filter — This circuit consists of an operational amplifier that converts the differential transformer signal to a single, ground referenced signal. The amplifier drives an L-C filter.
- Threshold Detectors— Two comparators which detect input signals greater than 0.5 V either positive (A), or negative (B). (A and B in this discussion indicate positive or negative waveforms prior to establishing any informational value from the waveforms). After sync is detected, the threshold is changed to 0 V and remains at that threshold until the end of the word.
- Shaping Circuits — Shape the signals prior to sync detection and ensure that both positive and negative signals cannot co-exist.



3-14



- **Sync Delay Circuit** — Is enabled by the exclusive OR of either the positive AB or negative AB waveform. This shift register starts with the first clock pulse after enabling, and continues to shift as long as enabled. The first output occurs at 1313 ns after starting, which should mark a point on a valid sync pattern, just prior to the polarity change. Figure 3-9 provides an overall view of sync detection timing.

When the polarity changes at the sync midpoint, the delay register is stopped and reset to zero time. The new polarity signal starts the delay timer again, and the earlier operation is repeated.

The output at 2125 ns is used to reset the sync detector in the case where the signal was too long to be a valid sync.

- **Sync Detector** — Consists of two separate channels of delaying latches (375 ns), comparing logic, and a combined three-state latch set for command sync, data sync, or neither. At the 1313-ns signal, the exclusive A or B signal is started into a 375-ns delay. During this period, a valid received sync pattern will change polarity, at which time, the delayed signal is compared to the opposite polarity current signal and, if opposite, the three-state sync latch is set as follows. A positive-to-negative change sets the Command Sync latch while a negative-to-positive change sets the Data Sync latch. The new (second half) polarity input signal also starts into the 375-ns delay. This signal will be used by the start timer test. If the received signal did not change state during the delay interval, and the opposite signal comparison fails, the latch remains idle.

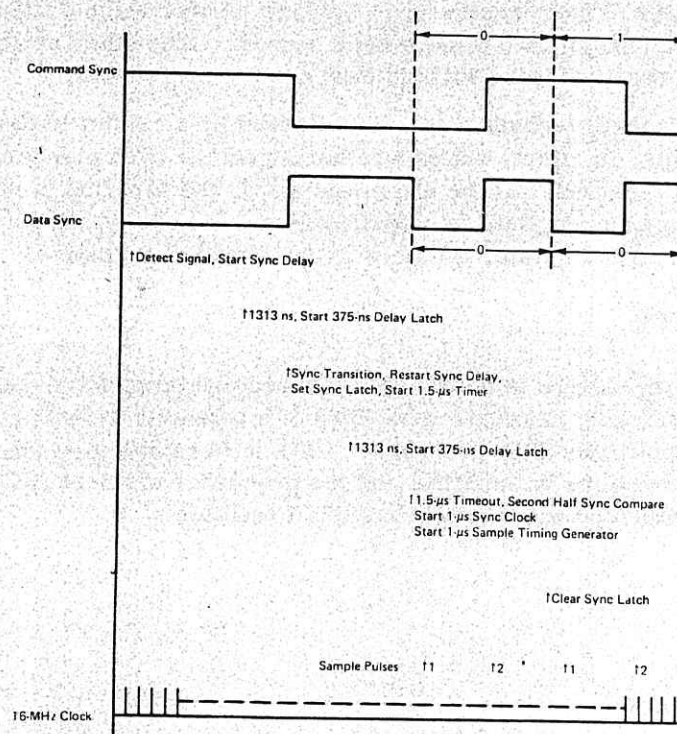


Figure 3-9. MIA Receiver Timing



- 1.5- $\mu$ s Timer — Consists of a divide-by-six ring counter and a divide-by-four binary counter, all clocked by 16 MHz. The setting of either sync latch starts this timer, and the resultant delay marks the end of the second half of the sync pattern.
- Start Timer — Consists of a compare circuit and a 1- $\mu$ s timer. At the end of the 1.5- $\mu$ s delay, the 375-ns delayed input signal of the second half polarity is compared to the set sync latch (positive input compared to data sync, negative input compared to command sync). If the comparison is good, the Start Timer latch is set (the Start signal is issued) and a 1- $\mu$ s timer to reset the Sync latch is started.
- Sample Clock Generator — Is a counter started by the Start Signal and clocked with the 16-MHz clock. The counter outputs are combined to form sampling pulses that are generated at 250 ns and 750 ns after the start of each bit. These points are midway in the stable periods for each serial bit.
- Data Decoder — Using the sampling pulses, the decoder samples the positive (A') and negative (B') signals out of the shaping circuits. The two samples (first half bit and second half bit) are compared, and if unequal, the corresponding data is outputted to the 24-bit register. As indicated in Subsection 3.2.1, a positive-to-negative change indicates a "1" output and a negative-to-positive change indicates a "0" output. The Data Valid circuit monitors for a bi-polar signal during each bit time, and outputs a "1" while this is true. Following the last bit of data received, the data decoder checks for data at both sample periods and the Data Valid signal is dropped. For this reason the Data Valid signal lags the loss of data by 750 ns.
- Bit Counter — Is a counter-and-compare circuit which gives a "go" output only when exactly 25 bits have been counted. Any other number of valid bits in a received word will indicate a bit count failure.
- Parity-Checker — Uses a flip-flop clocked by a "1" bit in the received data. This, in effect, states whether an odd or even number of "1" bits has been received. At the end of the word, the flip-flop is stopped and tested, and an odd state is outputted as a valid parity check. If the flip-flop is in an even state, a Parity Error signal is outputted.

### 3.2.5 MIA BUFFER

These one-word buffers temporarily store received data for each of the 24 MIA channels. This buffering is required because of a potential timing problem between the MIA and the applicable BCE processor. MIA buffers are functionally located between the 24-bit registers in the MIAs and the processor element (BCE processors). Buffers have no interface with the MIA transmit function.

As shown in Figure 3-10, MIA buffers are organized into six 28-bit 4-word registers. Each buffer temporarily stores a 28-bit word, which includes the following items:

- 24 bits — MIA information
- 1 bit — Received Command/Data word
- 1 bit — MIA parity error
- 2 bits — Spares.

When an MIA receives a valid word, loads the 24-bit register, and completes the required tests, it issues a Data Ready signal to the MIA buffer and simultaneously sets a bit in the Fresh Data Status register. Note that the Data Ready signals and the bits in the Fresh Data Status register are unique to each MIA. When the MIA sample period corresponds to the MIA position in its group of four, the Data Ready signal addresses the desired word in the four-word register connected to the active MIA page, and the data from the MIA are stored into the buffer register. The set bit in the Fresh Data Status register causes the BCE to fetch the buffer data at its next opportunity.

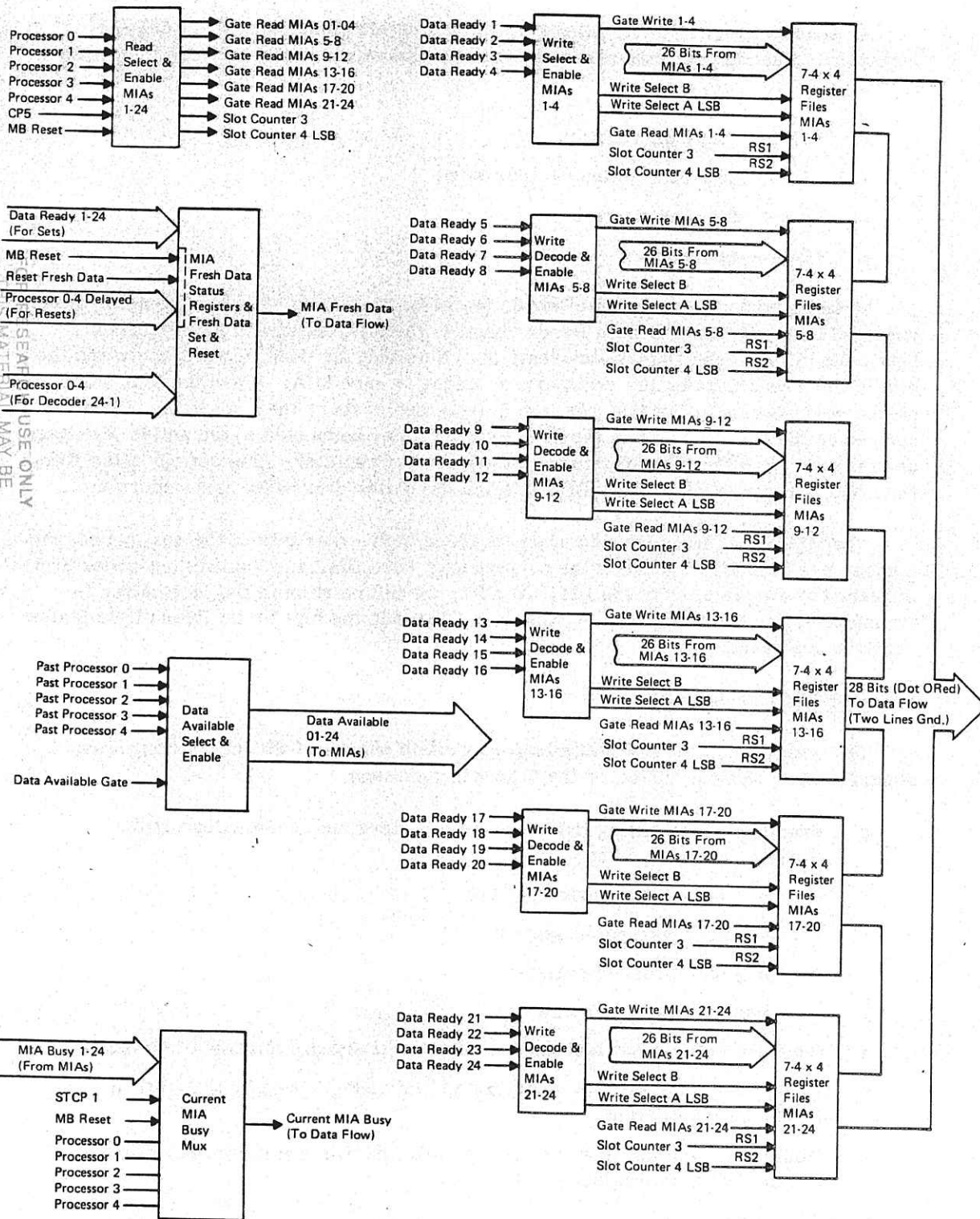
The MIA buffer is addressed when the three high-order bits of the next processor number are decoded to address the correct four word file, and the two low-order bits address the proper word in the file. At CP7, the information in the MIA buffer is transferred into the data flow. As the data are read, the bits in the Fresh Data Status register are reset.

### 3.3 CONTROL MONITOR

The control monitor element monitors certain phases of the IOP operation and controls other phases, including the following functions:

- Enabling and disabling the following registers and communicating the status to other elements
  - MIA Transmit Enable register
  - MIA Receive Enable register
  - BCE halt/proceed register
  - Discrete Output register
- Controlling the reset logic and issuing reset signals to all IOP elements
- Monitoring the interrupt registers and initiating action by the CPU to process the interrupt
- Monitoring and multiplexing for the CPU, the Discrete Input registers and the Interrupt registers
- IPL Initialization.





\* Processor Number is the upcoming current processor number prior to that slot.

Figure 3-10. MIA Buffer Functional Block Diagram



The control monitor element is functionally divided into four segments.

- The control registers and their related circuits
- The Discrete Input and Interrupt registers
- The PCI multiplexers
- The reset logic circuits.

The control monitor element is controlled by the CPU through PCO and PCI commands. The processor element has no authority over the control monitor.

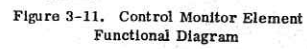
An overall block diagram of the control monitor element is shown in Figure 3-11. The detailed interfaces with other elements are also illustrated. The control monitor interfaces with the channel controller for all communication with the CPU including the PCI/PCO instructions and data and the requested data from the Discrete Input registers, interrupt registers, and others. The interface with the processor element consists of providing status of the MIA registers and the Halt/Proceed register, as well as receiving the processor-generated interrupts. The MIA interface consists of the 24 MIA transmit/receive Enable discretes. External interfaces are for 40 discrete inputs and 32 discrete outputs. The reset logic provides reset signals to all elements in the IOP.

The control registers specify the enable/disable status of the MIAs, the BCE processors and the discrete outputs. These four registers, each with independent latch circuits for each bit in each word, operate as follows:

- MIA Transmitter Enable Register (24 bits) — Contains an independent bit for each MIA transmitter, which when set, enables the corresponding MIA transmitter.
- MIA Receiver Enable Register (24 bits) — Contains an independent bit for each MIA receiver, which when set, enables the corresponding MIA receiver.
- Halt/Proceed Register (25 bits) — Contains a bit for the MSC and each BCE processor, and either enables or halts the corresponding processor.
- Discrete Output Register (32 bits) — Defines the IOP discrete output configuration. This register provides the data to the DO drivers which set the external interfaces.

Setting and resetting the bits in the control registers requires the assistance of the PCI/PCO control logic and the PCO multiplexer circuit. The PCI/PCO control logic is a decoding circuit which interprets the individual bits in the PCO Command word and sets up the PCO multiplexer and addressed control register. The PCI/PCO control logic is also used by the PCI multiplexer.

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The PCO multiplexer is a 32-bit gating circuit which sets and resets the addressed Control register as directed by the PCO Command word through the PCI/PCO control logic and the PCO Data word following the Command word.

As an example of Control register operation, assume MIA receiver 3 is to be enabled. The CPU issues a PCO command word with bits set for enabling the MIA receiving register. The channel controller routes the information to the PCI/PCO control logic for decoding. Following the PCO command word, the CPU outputs a Data word which the channel controller routes directly into the PCO multiplexer. This Data word is a mask word that specifies the bit(s) associated with the control element. In this case, only the bit corresponding to MIA 3 is set. The PCI multiplexer now reads out the current information in the MIA receiver register when a PCI command is received from the channel controller.

The control monitor also contains the Discrete input and Interrupt registers. There is capability for 40 discretes, 32 in one register and eight in another. The discrete inputs are processed through discrete input receivers and made available to the RM PCI multiplexer. The discrete output drivers are also located in the control monitor and supply external signals to the avionics subsystems.

There are five separate Interrupt registers corresponding to different interrupt priority levels. Interrupt signals for registers A, B, and C are presently defined. Registers D and E (lower priorities) are spares.

The Interrupt registers contain latching circuits for storing the Interrupt signals until they are processed. The latch outputs from each interrupt are logic ORed together by register, and the five Interrupt signals are supplied to the CPU via the channel controller circuitry. The CPU, detecting an interrupt, reads the Interrupt register via the RM PCI multiplexer, as soon as possible, depending on the interrupt level. The interrupts are reset as they are read.

The PCI multiplexers are divided into two parts, the control monitor PCI multiplexer which reads the Control Register data and the RM PCI multiplexer which handles the Interrupt registers, discrete inputs, and RM discretes. The RM PCI multiplexer is somewhat mislabeled, since RM is only a small part of its function. It acquired the name because it is located with the RM circuitry.

When information is requested by the CPU from the IOP, the CPU outputs a PCI word which is decoded by the PCI/PCO control logic. This decoded signal is supplied to the two PCI multiplexers. The signal indicates what data are to be read out of the IOP into the CPU. The control monitor PCI multiplexer consists of a series of gating circuits for each bit of the four inputs to the control monitor PCI multiplexer, MIA Transmit register, MIA Receive register, halt/proceed register, and Discrete Output register. The selection signal determines which register is to be read, and this information is gated by the multiplexer to the tri-state driver. This, three-state output device has the normal "1" or "0" output status when enabled, but when not enabled supplies a high-impedance output to reduce loading on other circuits when the driver is not in use.

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The RM PCI multiplexer operates like the CM PCI register, but with different inputs; i.e., the five Interrupt registers, the two Discrete Input registers, and the RM Status registers. The selected input is gated through the multiplexer to a tri-state driver which outputs the information to the channel controller and thereby to the CPU.

The control monitor contains the IOP reset logic and issues reset signals to all IOP elements, as required. Table 3-3 summarizes the control monitor reset logic.

### 3.4 CHANNEL CONTROL

Information transfers between the IOP and CPU are handled by the channel control. Two types of I/O operations are used:

- Direct I/O operations controlled by the CPU
- Main memory accesses requested, then controlled by the IOP

CPU-directed I/O is achieved by PCI and PCO instructions (commands), and IOP-directed I/O is achieved by direct memory access (DMA).

The IOP uses the DMA capability to acquire MSC and BCE programs, to read MIA output data, and to write MIA input data. PCI/PCO and DMA activity share a common bidirectional, 32-bit parallel data bus (I/O channel) between the CPU and IOP. The channel control interfaces the IOP with the I/O channel. Figure 3-12 diagrams the channel control and interfaces.

#### 3.4.1 CHANNEL CONTROL ELEMENTS

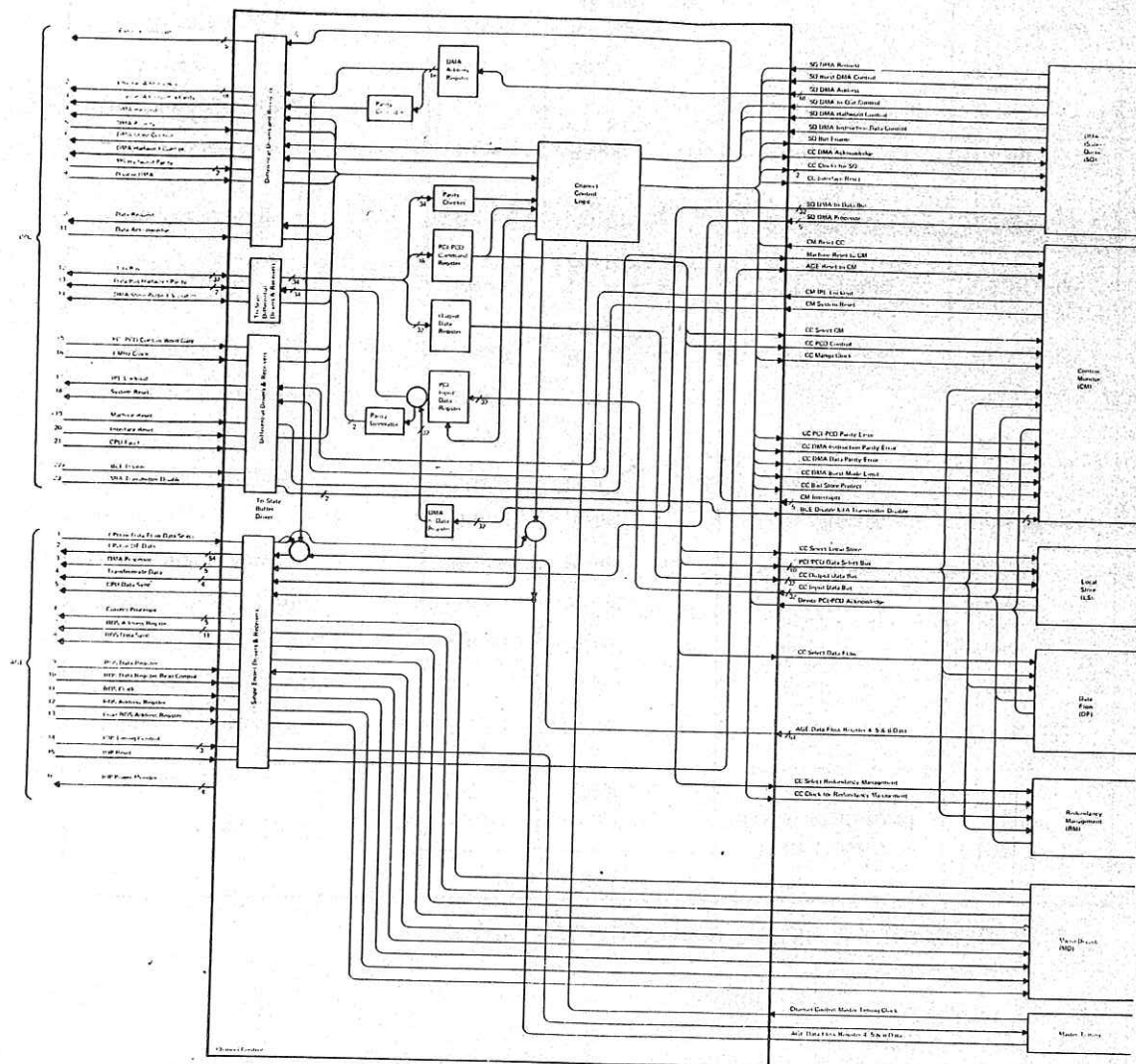
The major elements contained in the channel control are as follows:

- Differential Drivers and Receivers — These transfer control signals between the IOP and CPU. These differential circuits provide a high common mode rejection path. Signal flow is one way, with a logic level state of 5 V for high and 0 V for low.
- Tri-State Differential Drivers and Receivers — These are used for the I/O channel. This bidirectional data channel consists of 32 bits of parallel data, a Parity bit for each halfword, and a Storage Protect bit. Since these are bidirectional signals, a high-impedance state is entered when the driver is not active to relieve data bus loading. The tri-states are 5 V (high), 0 V (low) and high impedance.
- DMA Address Register — The address of the main memory word is transferred to the CPU by this 18-bit register.

Table 3-3

## CONTROL MONITOR RESET LOGIC SUMMARY

Function	Power Reset		PCO Master Reset Command	IOP Fail Reset	
	On or Halt	CPU or IOP Off			
Status 1 (Go/No-Go)	Reset	Reset	Reset	No Change	Reset = Go
Status 4 (Busy/Wait)	Reset	Reset	Reset	Reset	Reset = Wait
Status 5 (Halt/No Halt)	Reset	Reset	Reset	Reset	Reset = Halt MSC/BCE
Transmitter Enable	Reset	Reset	Reset	Reset	Reset = Disable
Receiver Enable	Reset	Reset	Reset	Reset	Reset = Disable
Channel	Reset	Reset	No Change	No Change	
Fail Vote Register	Reset	Reset	Reset	Reset	Reset = No Fail
Voter Test Register	Reset	Reset	Reset	Reset	Reset = Operation Data
Terminate Control Latches	Reset	Reset	Reset	Reset	Reset = Inhibit Termination
Fail Latch	Reset	No Change On CPU PD	No Change	No Change	Reset = No Fail
Timeout Latch	Reset	No Change On CPU PD	No Change	No Change	Reset = Inhibit Timer Clock
Watchdog Timer	Reset	No Change	Reset	Reset	Reset = Zero Timer and Inhibit Counting
Discrete Outputs	Reset	Reset	Reset	Reset	Reset = Inactive
Interrupt Register					
CM Idle	Set	Set	Set	Set	Set = Interrupt Pending
Fail Latch	Reset	No Reset On CPU PD	No Change	No Change	Set = Interrupt Pending
Timeout Latch	Reset	No Reset On CPU PD	No Change	No Change	Set = Interrupt Pending
ROS Parity Error	Reset	Reset	Reset	No Change	Set = Interrupt Pending
IOP Fault	Reset	Reset	Reset	No Change	Set = Interrupt Pending
All Others	Reset	Reset	Reset	Reset	Set = Interrupt Pending



**Figure 3-12. Channel Control and Interfaces**



- DMA Address Register Parity Generator — This provides odd parity bit to the CPU for transmission error detection.
- PCI/O Command Register — This 18-bit register holds the PCI or PCO command. PCI/PCO command decoding is accomplished and the required response is handled by the appropriate IOP element. PCI/PCO command decoding was described in Subsection 2.2.
- Output Data Register — This 32-bit register holds the PCO Data word or DMA Output word. The output of this register is the main output data bus within the IOP.
- Parity Checker — All PCI/PCO Command words and DMA Output words are checked for valid parity. Each halfword is assigned odd parity by the CPU for transmission error detection by the IOP. Also, main memory parity is received and checked.
- PCI Data Register — This 32-bit register holds the PCI Data word.
- DMA Input Data Register — This 32-bit register holds the DMA input word.
- Parity Generator — Each halfword of the appropriate PCI or DMA input data register is assigned odd parity for transmission to the CPU.
- Channel Control Logic — This unit performs the control functions associated with the DMA and PCI/PCO interface between the CPU and IOP. It establishes the necessary links between the various IOP elements and the I/O channel, and controls PCI/PCO or DMA activity.
- AGE Interface — The AGE interface is shown on Figure 3-12 and is described in Section 5.

### 3.4.2 PCI/PCO SEQUENCE

The CPU can initiate a PCI or PCO command when the I/O channel is not busy (see Figure 3-13). When the Data Request and Data Acknowledge lines are deactivated, the I/O channel is not busy. The following PCI/PCO Command word sequence can occur:

- The PCI/PCO Command word is placed on the I/O channel, and the CPU activates the PCI/PCO Control Word Gate Line.
- When the IOP accepts the PCI/PCO Command word, the IOP channel control activates the Data Request line.
- The CPU acknowledges receipt of the PCI/PCO by the IOP and activates the Data Acknowledge line.
- The IOP responds by deactivating the Data Request line after the IOP has processed the PCI/PCO Command word.
- The CPU then deactivates the Data Acknowledge line, drops the PCI/PCO control word gate line, and removes the PCI/PCO Command word from the I/O channel.

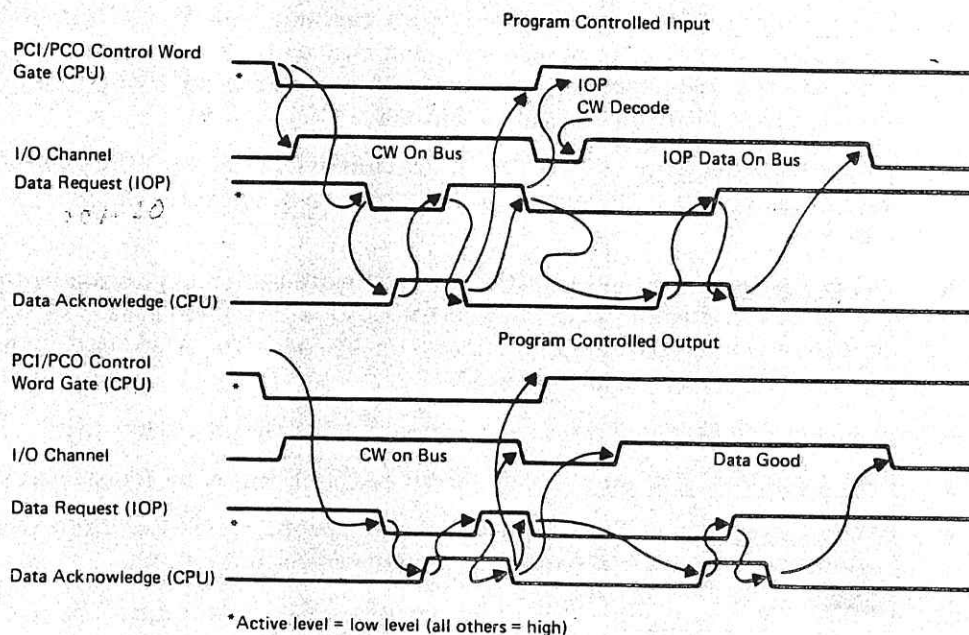


Figure 3-13. PCI/PCO Sequence

This completes the first half of a PCI/PCO sequence. A Data word always accompanies a PCI/PCO command. For some commands the Data word is not used but it is always issued.

#### 3.4.2.1 PCI Data Word Sequence

To complete a PCI command sequence, the IOP must respond by supplying a Data word. See Figure 3-14 for the timing diagram. The following sequence occurs:

- The IOP channel control places a Data word on the I/O channel and activates the Data Request line.
- After the Data word is accepted by the CPU, the CPU activates the Data Acknowledge line.
- In response, the IOP deactivates the Data Request line, and the IOP removes the data from the I/O channel.
- The sequence is completed by the CPU deactivating the Data Acknowledge line.

#### 3.4.2.2 PCO Data Word Sequence

To complete a PCO command sequence, the CPU must supply a Data word. See Figure 3-13 for the timing diagram. The following sequence occurs:

- The IOP signals the CPU that it is ready for the PCO Data word by activating the Data Request line.
- The CPU sends data to the IOP by placing a Data word on the I/O channel and activating the Data Acknowledge line.
- When the Data word is accepted by the IOP, the Data Request line is deactivated.
- The CPU finishes the sequence by deactivating the Data Acknowledge line and removing the Data word from the I/O channel.

#### 3.4.2.3 PCI/PCO Timeout

The CPU maintains timeout checks on PCI/PCO command response from the IOP. Timeout periods are as follows:

- For a PCI/PCO Command word transfer, the CPU will time out if the period from the leading edge of PCI/PCO Control Word gate to the trailing edge of the first Data Request signal exceeds  $5.75 \mu s$  at the computer terminals.
- For PCOs, the CPU will time out if the period from the trailing edge of the first Data Acknowledge to the trailing edge of the second Data Request exceeds  $6.15 \mu s$ .
- For PCIs, the CPU will time out if the period from the trailing edge of the first Data acknowledge to the leading edge of the second Data Request exceeds  $6.15 \mu s$ .

#### 3.4.3 DMA SEQUENCE

##### 3.4.3.1 DMA Input Sequence

Figure 3-14 shows the DMA input sequence, which is described below:

- IOP activates the DMA request line.
- CPU responds, when main memory is available, by activating the DMA priority line.
- Then, IOP activates the DMA Store Control line, which causes main memory to store input data.

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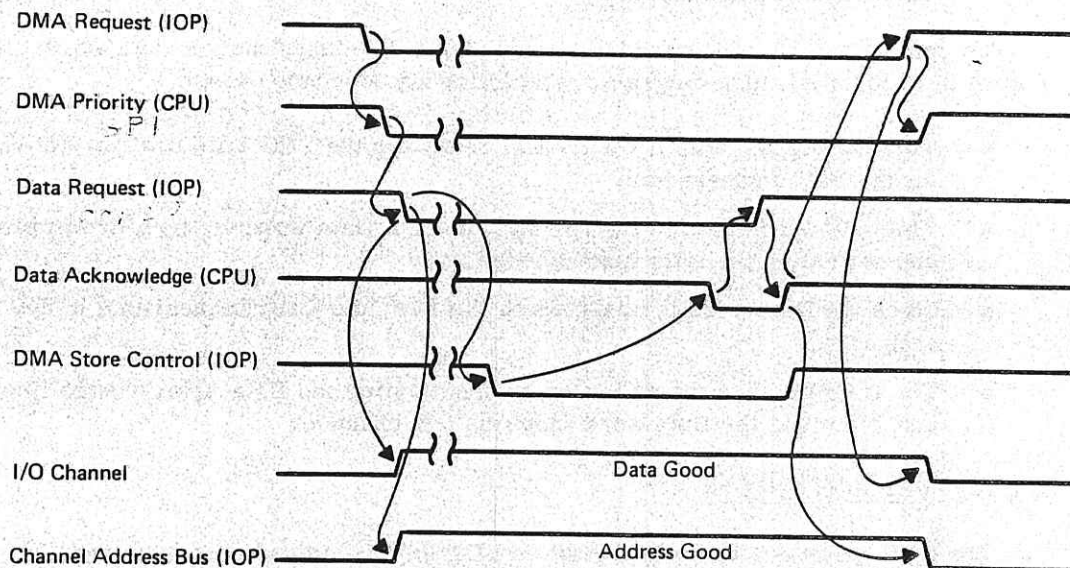


Figure 3-14. DMA Input Sequence

- With the activation of DMA priority the IOP places input data on I/O channel, places the main memory address (where the data will be written) on the channel address bus, and activates the Data Request.
- CPU acknowledges receipt of input by activation of Data Acknowledge.
- IOP deactivates the Data Request line.
- CPU deactivates Data Acknowledge.
- IOP removes address from channel address bus, removes data from I/O channel, and if DMA Burst mode is not active, deactivates DMA Request. If Burst mode is required, the sequence is repeated, starting at the third step.
- The sequence is completed by CPU deactivating DMA priority.

#### 3.4.3.2 DMA Output Sequence

Figure 3-15 shows the DMA output sequence, which is described below:

- IOP activates the DMA Request line.
- When main memory is available, CPU responds by activating DMA Priority.

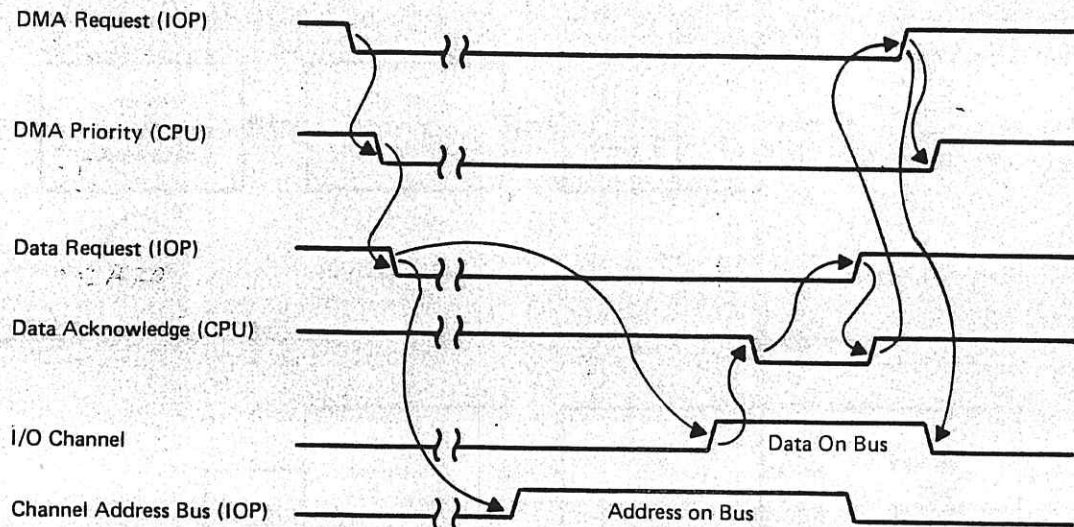


Figure 3-15. DMA Output Sequence

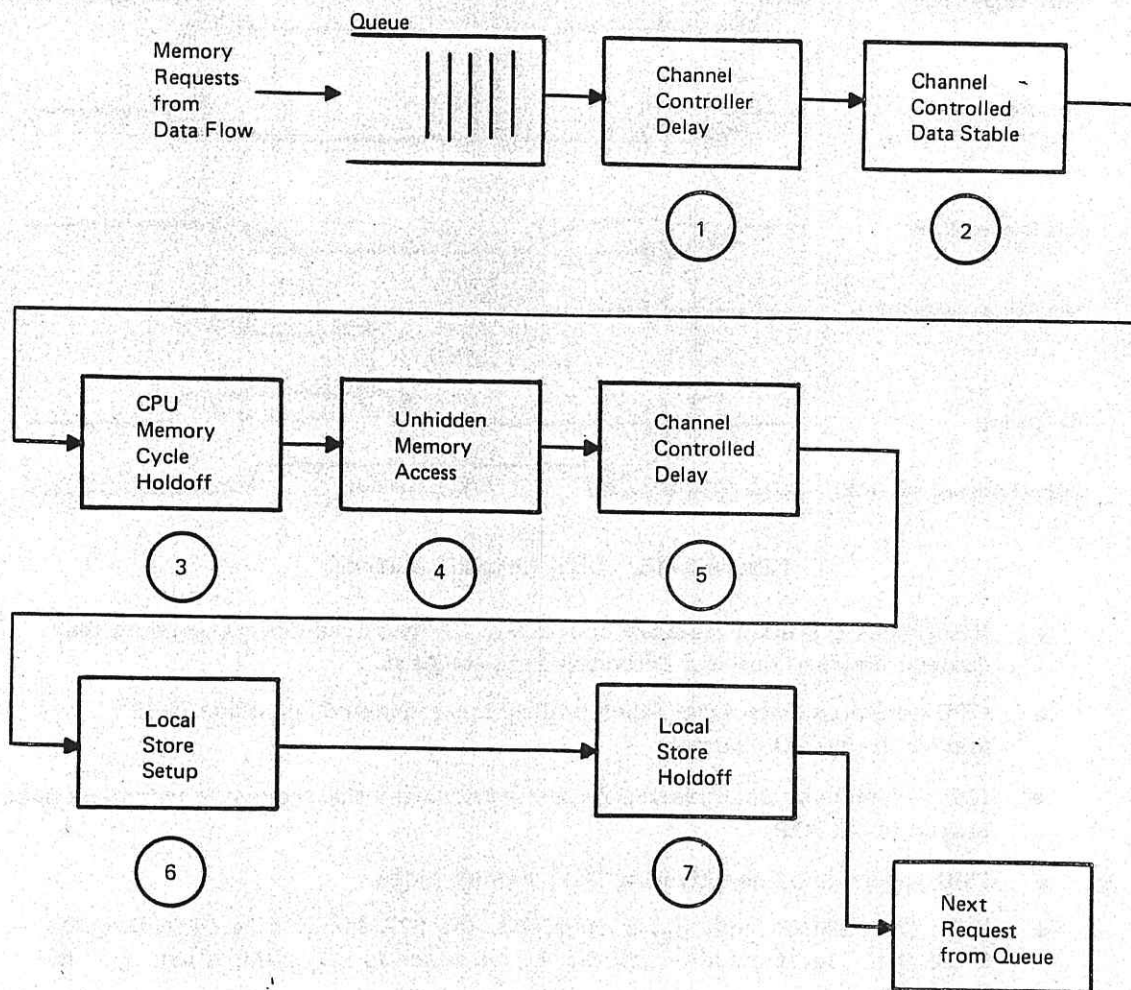
- IOP places the main memory address of the required Output word on the channel address bus and activates Data Request.
- CPU activates Data Acknowledge after the requested word has been placed on the I/O channel.
- IOP responds by deactivating Data Request after the requested word has been stored in the IOP.
- CPU responds by deactivating Data Acknowledge.
- If the DMA Burst mode is not required, the IOP deactivates DMA Request. If the DMA Burst mode is active, the sequence is repeated, starting at the third step.
- The sequence is completed by the CPU deactivating DMA priority.

#### 3.4.3.3 DMA Channel Access Time

DMA channel access time varies, depending on the CPU processor state and IOP timing. The timing delays encountered in performing a main memory access are shown and listed in Figure 3-16.

#### 3.4.3.4 IOP Interfaces

The IOP-to-CPU connector interface is shown in Figure 3-12; the interface signals are briefly described in Table 3-4.



No.	Delay	Read from Main Store				Write into Main Store			
		Normal		Burst		Normal		Burst	
		Max.	Avg.	Max.	Avg.	Max.	Avg.	Max.	Avg.
1	Channel Controller	0.312	0.312	0.312	0.312	0.312	0.312	0.312	0.312
2	Channel Controlled Data	0.300	0.300	—	—	0.300	0.300	—	—
3	CPU Memory Cycle	2.000	1.250	—	—	2.000	1.250	—	—
4	Memory Access	0.825	0.825	0.825	0.825	1.075	1.075	1.075	1.075
5	Channel Controller	0.375	0.375	0.375	0.375	0.187	0.187	0.187	0.187
6	Local Store Setup	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
7	Local Store Access	0.761	0.761	0.761	0.761	—	—	—	—
—	Sum (Less 7)	4.112	3.362	1.948	1.948	4.174	3.424	1.874	1.874

Figure 3-16. Channel Control Timing



Table 3-4  
IOP/CPU INTERFACE SIGNAL DESCRIPTIONS

CPU/IOP Interface	Description
External Interrupt (to CPU)	Five interrupt lines. Informs CPU of error condition or programmable interrupts in IOP
Channel Address Bus (to CPU)	Main memory address, 18-bits parallel
Channel Address Bus Parity (to CPU)	Main memory address parity
DMA Request (to CPU)	IOP request to use main memory
DMA Priority (from CPU)	Informs IOP that main memory is available for DMA request.
DMA Store Control (to CPU)	Causes main memory store. Must be gated after DMA priority received from CPU
DMA Halfword Control (to CPU)	Specifies that a halfword will be written into main memory
MS Halfword parity (from CPU)	Parity read from (2 bits) main memory
Disable DMA (from CPU)	Used by CPU when an error condition exists
Data Request (to CPU)	Primary signal used by IOP to establish communication on I/O channel. It indicates to CPU that output data are needed or input data are available
Data Acknowledge (from CPU)	Response signal to IOP. It indicates that output data are available or input data are accepted
Data Bus (Bidirectional)	Major I/O channel between CPU and IOP, 32-bit parallel
Data Bus Halfword Parity (Bidirectional)	Two bits containing parity information for each halfword for I/O channel
DMA Store Protect/Violation (Bidirectional)	Specifies Main Memory Protection Bit state
PCI/PCO Control Word Gate (from CPU)	Informs IOP that a PCI or PCO command is on the I/O channel
IPL Lockout (to CPU)	Used during initial program load to enable control of main memory storage protection bit
System Reset (to CPU)	External signal from crew station to place GPC in Standby mode
Machine Reset (from CPU)	From CPU power supply to indicate a power-off condition
Interface Reset (from CPU)	Used during error recovery to reset I/O channel logic
CPU Fault (from CPU)	Not used by the IOP
BCE Disable (from CPU)	Used by CM to force all BCEs to the HALT state
MIA Transmitter Disable (from CPU)	Used by CM to inhibit all MIA transmissions

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### 3.5 DMA QUEUE

IOP main memory accesses are used to transfer the following types of information:

- MSC and BCE instructions for program execution
- Data for MIA output
- Data from MIA input.

A transfer is initiated when an IOP main memory access is generated and stacked in the queue, which can hold up to 64 main memory word requests. The queue memory device subsequently acts on the requests on a first-in, first-out (FIFO) basis.

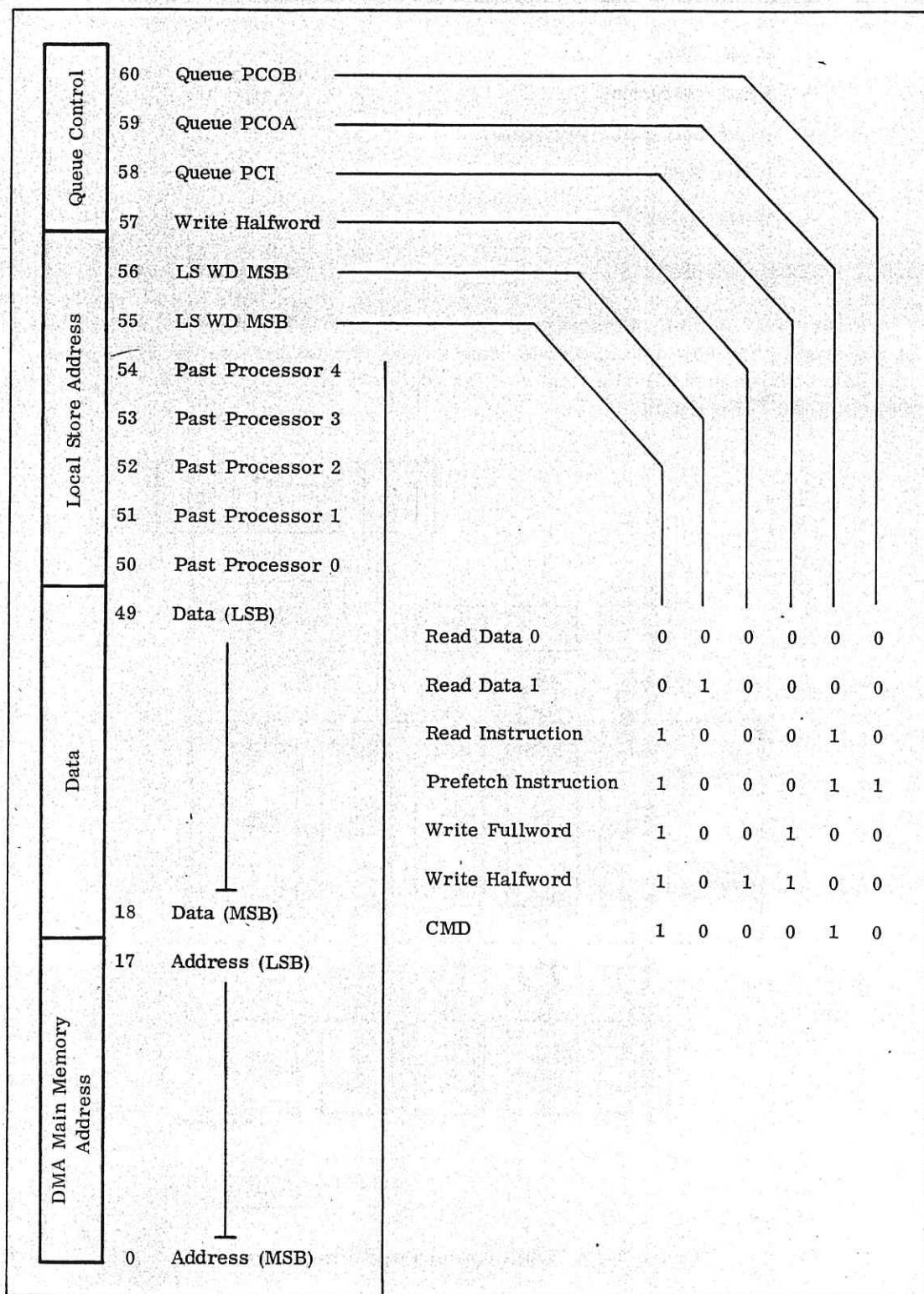
A single request from the queue requires an average main memory access time of 3.4  $\mu$ s (see Figure 3-16). When more than 8 requests have been stacked, the DMA Burst mode of operation occurs, which has average main memory access time of 1.9  $\mu$ s. In Burst mode, the Main Memory is dedicated to the IOP. Burst mode will continue until less than 8 requests are stacked in the FIFO or 64 DMAs have occurred. But if the queue does become full, an IOP error condition will be flagged by setting an interrupt to the CPU. IOP processing will continue.

#### 3.5.1 QUEUE FORMAT

The queue register format is listed in Table 3- 5. The queue register bits are described here:

- DMA Main Memory Address (18 bits) — Specifies any halfword in main memory. For main memory read operations, a full 32-bit Main Memory word is received. For write operations, a halfword or a fullword can be written into main memory. A Storage Protect bit for each halfword in main memory will prevent a processing error from writing over critical main memory locations.
- Data (32 bits) — Used for a write operation, but not for read operations. One MIA Input Data word requires a main memory halfword. If only one MIA Input word is being written into main memory, a Halfword Write operation is specified in the queue control field, and only the first 16 bits will be transferred to the main memory address specified by DMA address. A Fullword Write will transfer 32 bits to main memory (two MIA input words).
- Local Store Address (7 bits) — Contains the processor and general register address (bank and word number). This field is not used for a Write operation. For a Read operation, this field is used to store the I/O channel information, when it arrives, into the specified processor local store. A processors' slot time is not associated with the I/O channel access to local store.

Table 3-5  
QUEUE REGISTER FORMAT





- Queue Control (4 bits) — Specifies the type operation as follows:

- Read Data
- Read Instruction
- Read Instruction Prefetch
- Write Fullword
- Write Halfword.

### 3.5.2 QUEUE OPERATION

Figure 3-17 is a block diagram of the DMA queue. When a main memory access is required by the IOP the microcode controls the data loaded into the FIFO queue. The figure shows how the data flow working registers (R4, R5, and R6) are gated into the top of the FIFO stack.

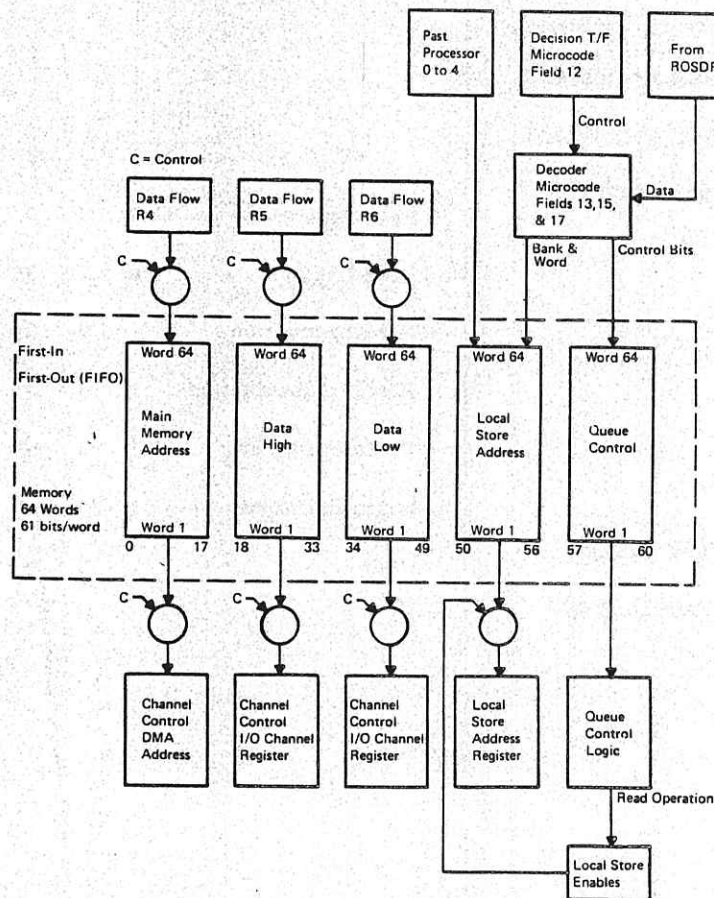


Figure 3-17. DMA Queue Functional Diagram

After a DMA request has been loaded into the FIFO, the queue control logic establishes communications with the channel control and the channel control requests a DMA access. The DMA channel control sequence is described in Subsection 3.4.

When the main memory access is a Write operation, the main memory address (FIFO bits 0 through 17), data high (FIFO bits 18 through 33), and (if this is a Fullword Write operation) data low (FIFO bits 34 through 49) are gated into the channel control registers. Any subsequent DMA request is issued when the reception of the previous DMA request is acknowledged by the CPU.

For a Read operation, the FIFO main memory address is passed to channel control, and when the main memory word arrives, the FIFO local store address (bits 50-59) is used to control the put-away into local store. The timing associated with local store is covered in Subsection 3.6. The maximum access time associated with local store put-away is 0.761  $\mu$ s. After the FIFO local store address information has been gated into the Local Store Address register, any remaining DMA request in the FIFO is propagated to initiate the next DMA cycle.

### 3.5.3 QUEUE CONTROL FIELD

The queue control field (bits 57 through 60) is placed into the Queue register during the microcycle. These control bits are used during the main memory access cycle as follows:

- Write Operation — The channel control logic is informed that the Write operation will be halfword or fullword operation. Since this is a write into main memory, the local store will not be involved.
- Read Operation — The channel control logic is informed that the information received over the I/O channel will be sent to local store. The local store address is obtained from the Queue register (bits 50 through 56).

### 3.5.4 QUEUE MICRODECODE

Table 3-6 summarizes the different types of DMA requests specified by the micro-code. When MSC or BCE instructions are requested, the instruction OP code is used to load the microprogram counter. The instruction OP code is the starting address in ROS where the microprogram is located. The microprogram counter is loaded two ways:

- For an Instruction Prefetch operation, the new instruction OP code is 56), written into local store.
- For an Instruction Read operation, the new instruction OP code is written directly into the microprogram counter file. The processor number (microprogram counter file address) is obtained from the queue, and the new OP code is obtained from the channel control data register.

The microprogram counter file is described in Subsection 3.6.

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Table 3-6

MICRO DECODING BY DMA QUEUE

No.	Operation	(Microcode)	Microfield Field	Local Store Bank/Word	Microprogram Counter Load
1	Write Fullword	(DWR)	Field 12 True & Field 13 = 1	N/A	N/A
2	Write Halfword	(HDWR)	Field 12 True & Field 13 = 2	N/A	N/A
3	Read Data	(DRD0)	Field 12 True & Field 13 = 3	High → B0 Low → C0	N/A
4	Read Data	(DRD1)	Field 12 True & Field 13 = 4	High → B1 Low → C1	N/A
5	Prefetch Instruction Read	(PFCH)	Field 12 True & Field 13 = 5	High → B2 Low → C2	OP Code from Local Store
6	Prefetch Instruction Read	(PFCH A)	Field 12 False & Field 15 = 3	High → B2 Low → C2	OP Code from Local Store
7	Prefetch Instruction Read	(PFCH B)	Field 17 = 2	High → B2 Low → C2	OP Code from Local Store
8	Instruction Read	(RIR)	Field 12 True & Field 13 = 6	High → B2 Low → C2	OP Code from CC Data Register
9	Instruction Read	(RIRA)	Field 12 False & Field 15 = 4	High → B2 Low → C2	OP Code from CC Data Register
10	Instruction Read	(RIRB)	Field 17 = 1	High → B2 Low → C2	OP Code from CC Data Register
11	MIA Output Read	(CMD)	Field 12 True & Field 13 = 10	High → B2 Low → C2	OP Code from CC Data Register



### 3.6 PROCESSOR ELEMENTS

IOP data processing is accomplished by the MSC and BCE programs, which are executed from main memory by the IOP processor elements. The processor elements, described below, were shown in Figure 3-1:

- Local store
- Data flow
- Microstore and decode
- Master timing.

Functionally, the MSC and BCE processors can be thought of as a set of general registers (one set for the MSC, one set for each of the 24 BCEs, and one set for BCE test) maintained in the local store. Data flow is through the arithmetic logical unit (ALU) time-shared by the MSC/BCEs. Microstore and decode contains the detailed information (microprogram) that defines how to execute a MSC/BCE instruction, and the master timer determines how the processor elements will be time-shared.

Figure 3-19 diagrams the IOP processor elements. Information flows through the processor elements under the control of the microcode. The basic data paths and interfaces are as follows:

- I/O channel information from channel control is gated into local store, as shown at the top of Figure 3-18.
- Microcode specifies the words from Banks A, B, and C of local store to be gated into their respective working registers R1, R2, and R3.
- Microcode determines how R1, R2, and R3 are to be sent to a MIA Transmit register for outputting data, or processed by ALU 1 or 2.
- ALU 1 and 2 perform all the arithmetic and logical functions.
- The results of ALU processing are gated into working registers R4, R5, and R6.
- For MIA input data, microcode determines where the input data will be placed in register R4, R5, or R6.
- To complete a microcycle, registers R4, R5, and R6 are stored either in microcode-specified words of local store banks A, B, and C, respectively, or gated into the DMA queue to perform a main memory access.

3-38

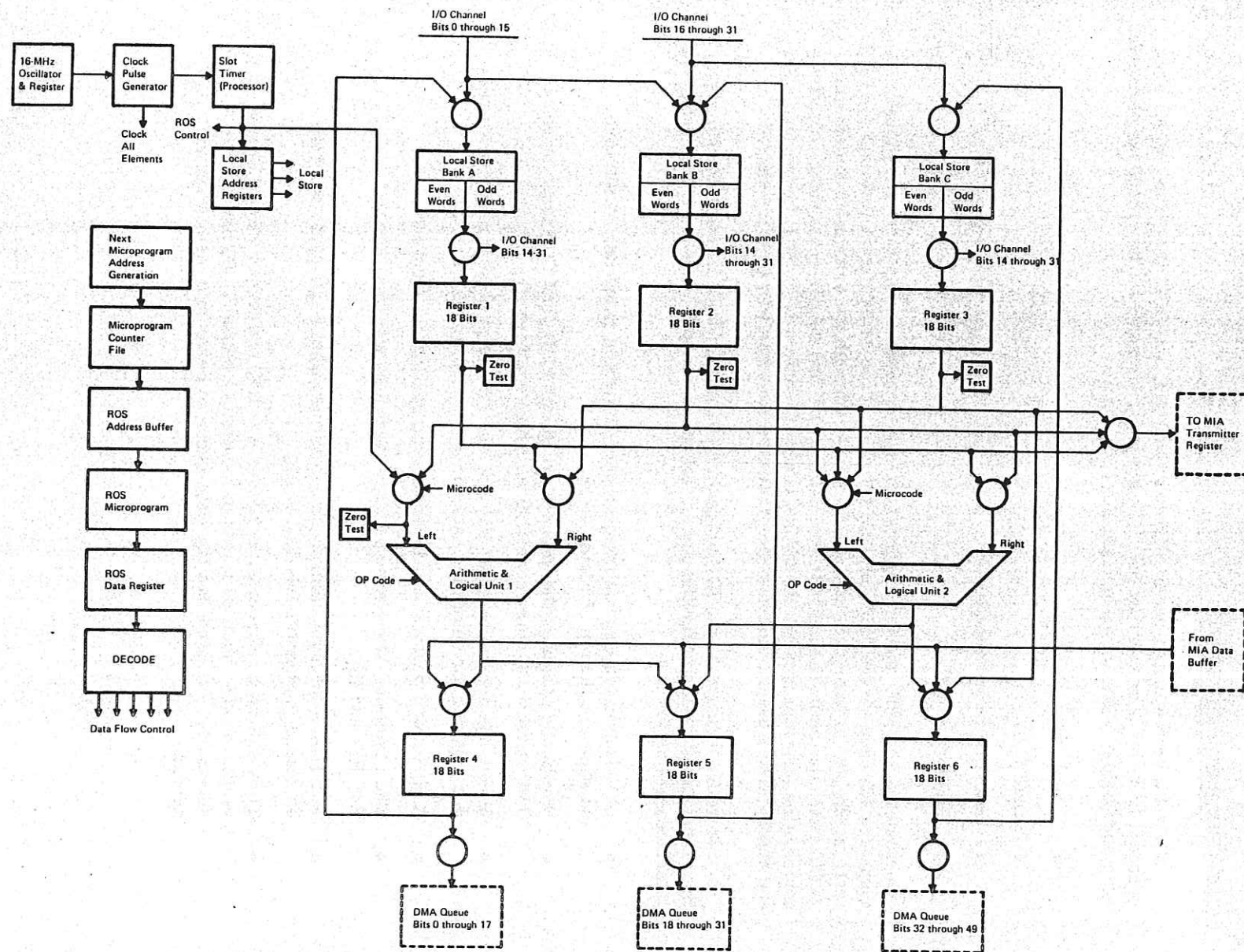


Figure 3-18. Processor Elements Data Paths



### 3.6.1 MICROSTORE AND TIMING

This section of the IOP contains (1) the oscillator, timing circuits, and counters for controlling each active MSC/BCE/BCE Test program, and (2) the stored microprograms to control the processor elements. Since timing is basic to the rest of the processor, it is described first.

#### 3.6.1.1 Timing

The basic oscillator for the IOP is a 16-MHz crystal-controlled square-wave generator. The 16 MHz output is distributed through several drivers to the numerous user circuits in the IOP.

The 16 MHz is counted down with an 8-bit shift register arranged as a ring counter to provide eight clock pulses, labeled CP1 through CP8, each pulse 62.5 ns wide. The clock pulses time the various steps in the processor element operation. The 8-clock pulse times constitute one slot time 500 ns wide. The slot time is started by the CP1 leading edge.

The basic IOP cycle time is generated from 33 slot times, giving a cycle time of 16.5  $\mu$ s. Slot timer functions are described in Section 2. Basically, the slot time determines which BCE, the MSC or BCE Test program, is active at a given time.

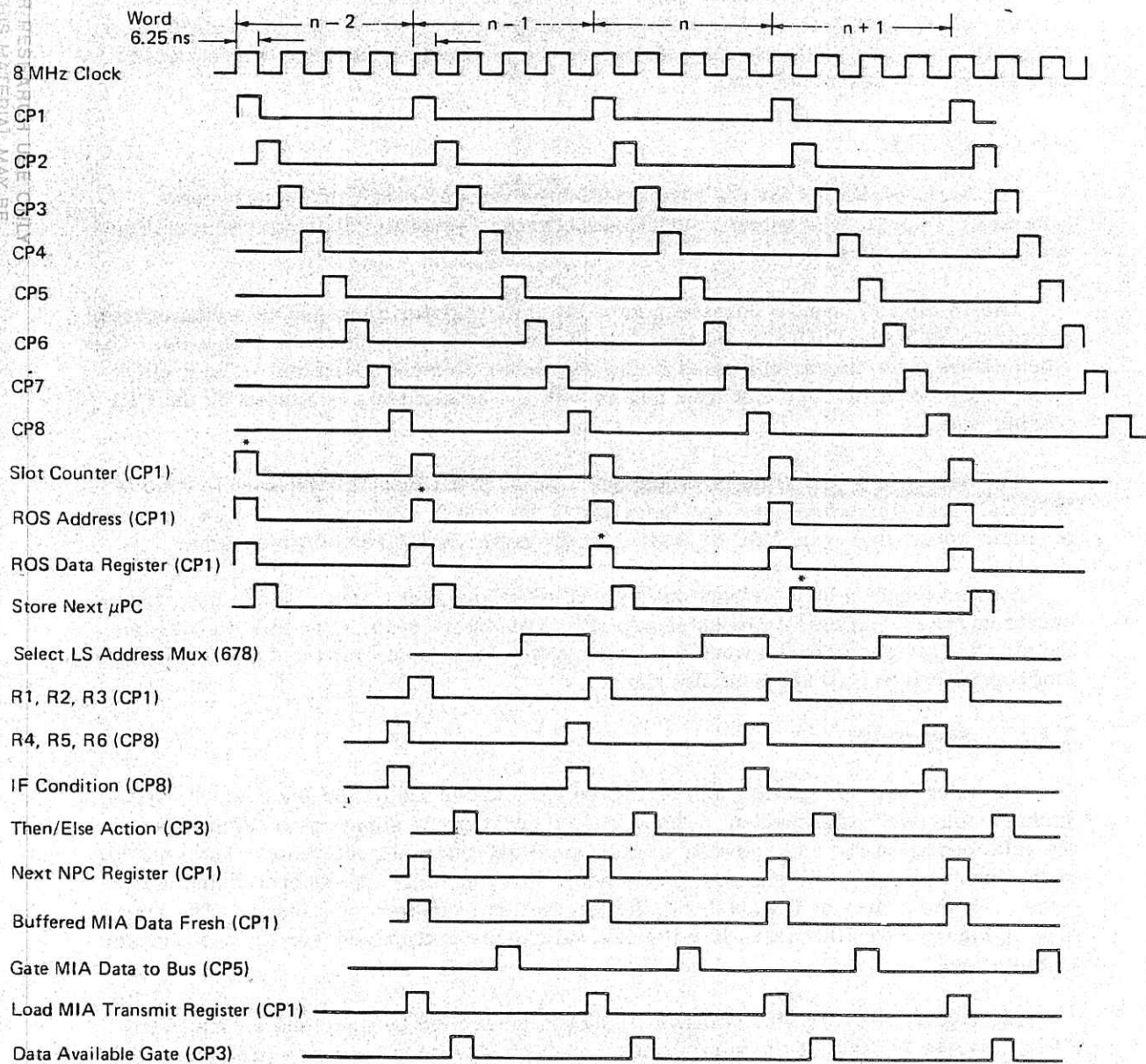
A given single micro instruction is timed over four slot times. Micro instruction events and their timing relationships are shown in Figure 3-19. For this discussion, the slot time is designated  $n$  when the instruction is active,  $n-1$  and  $n-2$  for the previous slot times, and  $n+1$  for the next slot time.

#### 3.6.1.2 Microstore

The microstore block diagram of Figure 3-20 shows the major microstore events during a four-slot time period. The slot time chart in the same figure illustrates the relationship of the major events in relation to the current processor. The left side of the figure shows how the processor numbers ( $n+1$ ,  $n$ ,  $n-1$ ) are generated and maintained. In the center of Figure 3-20, the microstore registers are shown. The right side of Figure 3-20 illustrates how the next micro-instruction address for a processor is generated.

The register-to-register transfer of data is controlled by the clock pulses (CP1, CP7). Basically, at CP1 the state of microstore is advanced from one processor to the next processor, the current micro instruction is executed, a prefetch for the next processor's micro instruction is started, and the previous processors next microprogram counter is loaded with the results of its execution cycle.





\*Denotes occurrence of signal pertinent to processor n.

Figure 3-19. IOP Timing Diagram

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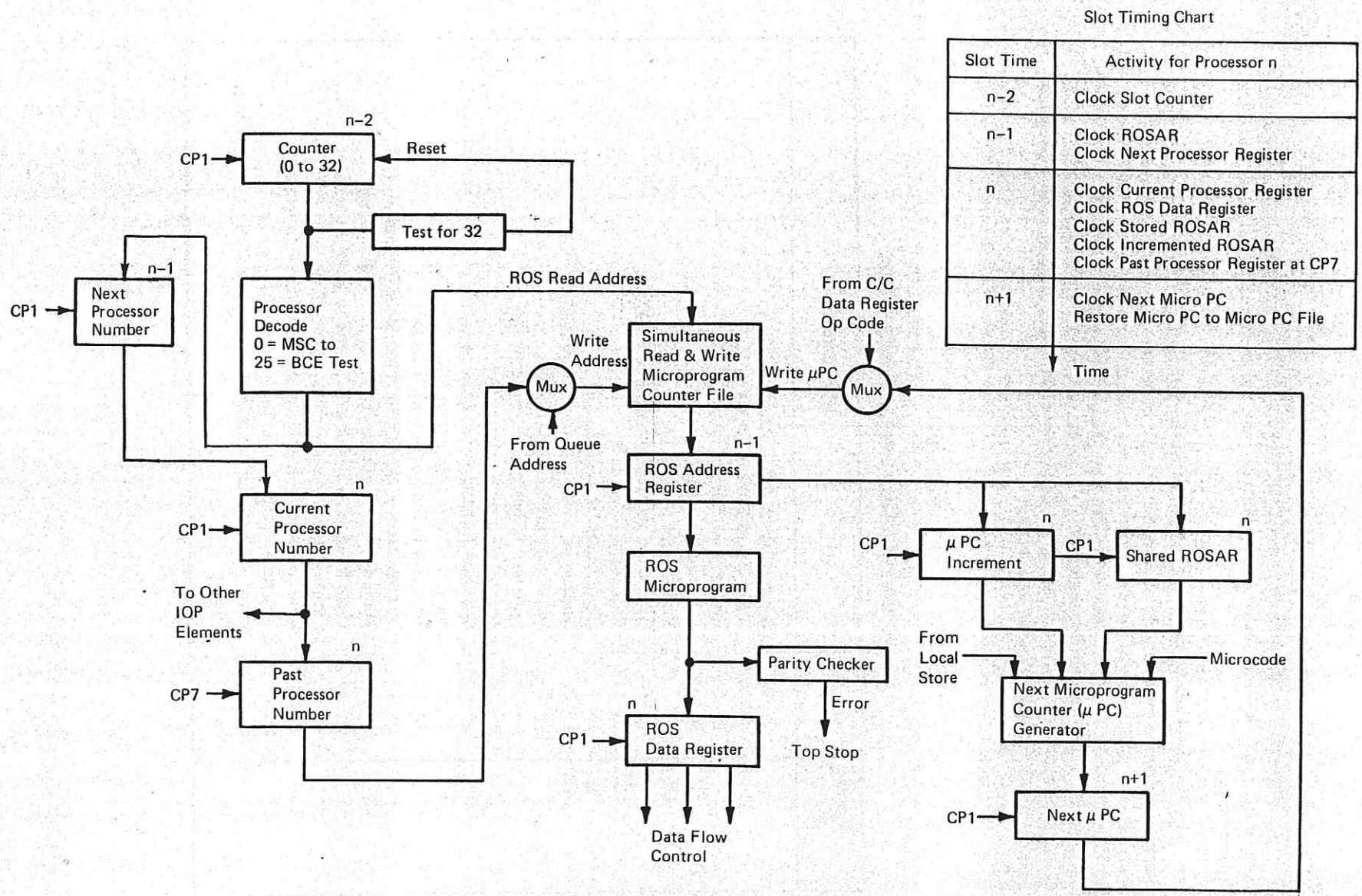


Figure 3-20. Microstore and Timing

The microprogram memory is a 1.5K word  $\times$  72-bit, fuseable link, ROS device containing the complete set of micro instructions for performing all MSC and BCE instructions.

The output of the microstore is stored in the Microstore Data register, which distributes the various fields of micro instruction data to the various users; i.e. local store, ALUs, multiplexers, and the next microprogram counter generator. The 72 bits of the Microstore Data registers are utilized as shown in Table 3-7. The individual bit patterns and corresponding functions for each field are described in a Microprogram Principles of Operation document. The use of each of the fields is diagrammed in Figures 3-21 and 3-22.

Table 3-7

MICRO INSTRUCTION FIELD DESCRIPTION

Field No.	Bits	Information
1	00-01	Address in Bank A to go to R1
2	02-03	Address in Bank B to go to R2
3	04-06	Address in Bank C to go to R3
4L	07-09	Left input to ALU 1
4R	10	Right input to ALU1
4OP	11-14	Operation to be performed by ALU 1
5L	15-17	Left input to ALU 2
5R	18	Right input to ALU 2
5OP	19-22	Operation to be performed by ALU 2
6	23-24	Source of information to R4
7	25-26	Address in bank A for data in R4
8	27-28	Source of information to R5
9	29-30	Address in bank B for data in R5
10	31-32	Source of information to R6
11	33-35	Address in bank C for data in R6
12	36-40	IF condition — What condition is to be tested
13	41-45	Then action — Action to be taken if IF is true
14	46-48	Then branch — Branch to be taken if IF is true
15	49-51	Else action — Action to be taken if IF is false
16	52-54	Else branch — Branch to be taken if IF is false
17	55-58	Action — Action to be taken regardless of IF
18	59-70	Emit — Contains constants to be used by microprogram
19	71	Parity



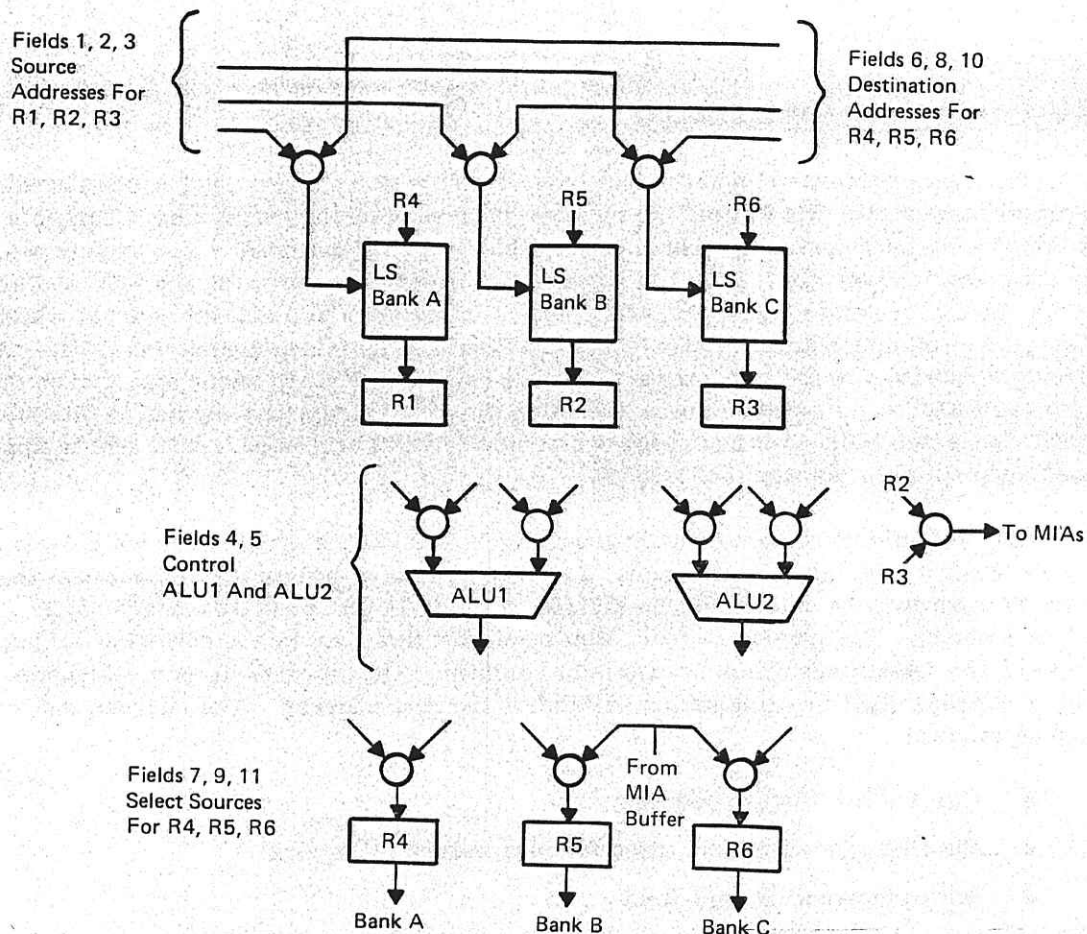


Figure 3-21. Microprogram Control of Data Flow

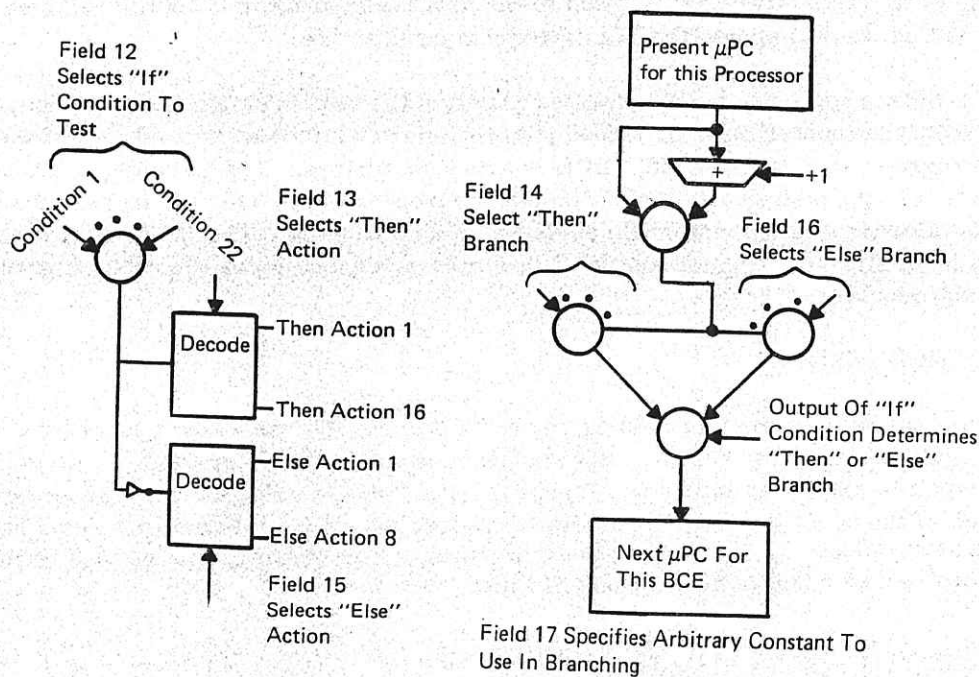


Figure 3-22. Microprogram Control of Actions and Micro Branching

### 3.6.1.3 Microprogram Addressing

The next processor number output from the Processor Decode addresses the microprogram counter file to prefetch the next processor micro instruction. This is a 26 word  $\times$  11-bit register file which can address and read one word while another word is addressed and written. This file contains the program counter for the MSC and each of the BCE processors. The program count is in the form of an 11-bit address which designates the microstore location containing the desired micro instruction. This address is outputted to the microstore through a register (ROSAR) which also drives the stored ROSAR register and a second register which is incremented by one to provide a next instruction address if no branches or other changes are made. AGE addressing is also accomplished through this ROSAR.

The next microprogram counter generator is basically a multiplexer which selects a processor's next micro instruction. The current micro instruction defines how the next address is to be determined as defined by fields 14 and 16 (THEN branch and ELSE branch). The true/false indication from data flow, set by the condition defined in field 12, determines which branch is to be made. The selected branch designates which address input or combination will define the next address. The address inputs are as follows:

- Current microstore address
- Current address plus 1 (used for next sequential micro)
- Micro instruction emit field
- Register 2, bits 2 through 9 and 13, and Register 3, bits 2 through 6. (branch conditions).

The output of this multiplexer is gated to the next Microprogram Counter register, which will be used to update the microprogram counter file.

If a DMA access has been requested to obtain the next MSC/BCE instruction, the microprogram counter must be loaded with the appropriate starting address of the new microprogram when the new MSC/BCE instruction arrives. The OP code of the new instruction is the address in ROS of the new microprogram. This OP code is loaded into the microprogram counter file as shown in Figure 3-20. The OP code is obtained from a local store or channel control data register, depending on the type of instruction fetch that occurred.

### 3.6.2 LOCAL STORE

Local store is a group of holding registers for the MSC and BCE processors. These registers hold information between each stop of the MSC or BCE programs. Local store is organized into three "banks", 1, 2, and 3. For the MSC processor and each of the 24 BCE processors, there are four words each in banks 1 and 2 and eight words in bank 3. Each word is 18 bits long. The organization and use of the registers is described in Subsections 2.4 and 2.5.

Each bank also contains an input multiplexer and a register (R1, R2, R3) for data flow interface. There is also an output register for outputting data to the CPU data bus. This register has a multiplexer for reading from any of the three banks of local store.

The local store interfaces with data flow, as shown in Figure 3-23. Inputs to local store are from either the CPU I/O bus through channel control, or from Data Flow registers R4, R5, and R6. Inputs are gated by the local store input multiplexer or controlled by the microprogram.

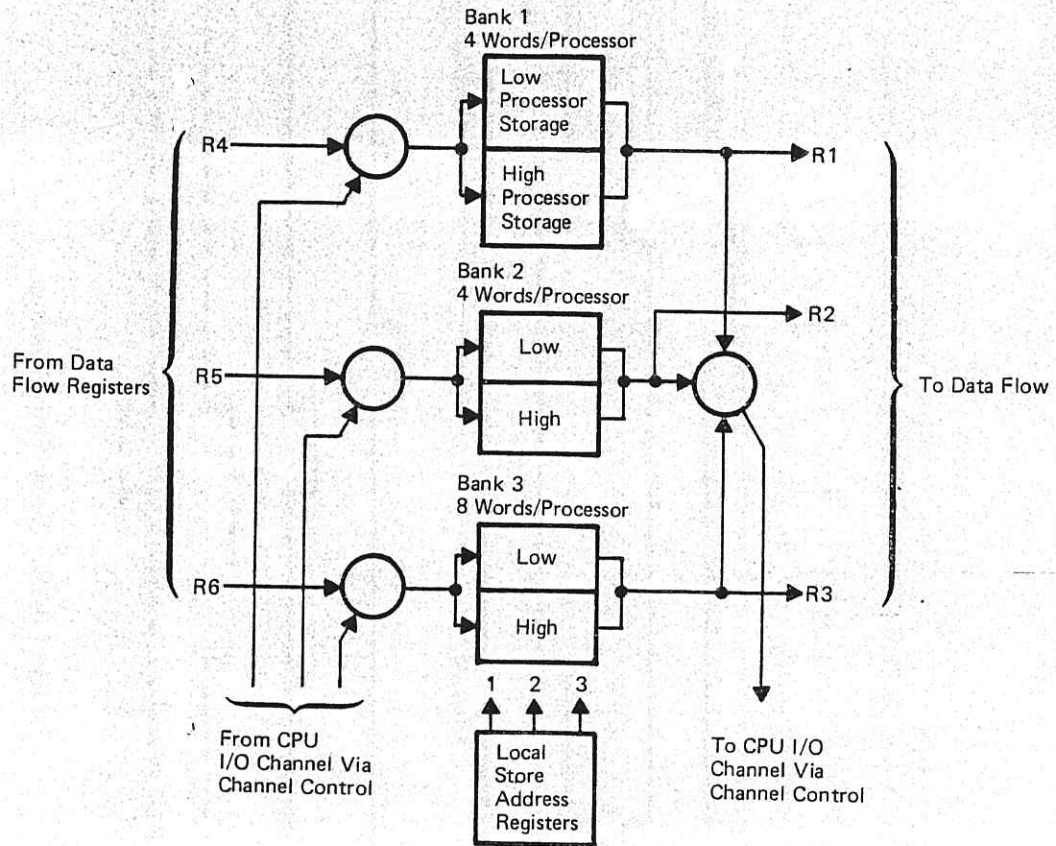


Figure 3-23. Local Store Data Paths

The local store for each bank is further divided into Low and High segments with separate addressing capabilities. High and Low refer to the current processor number. The separation of the store segments allows information to be read from one side, while the information out of the previous data flow cycle is being read back to the other side of local store. Figure 3-24 shows the local store timing sequence.

During the read time the current processor and ROS source bits are selected and the appropriate RAMs are addressed. At clock R1, 2, 3, the data is stored in the data flow registers (R1, R2, R3).



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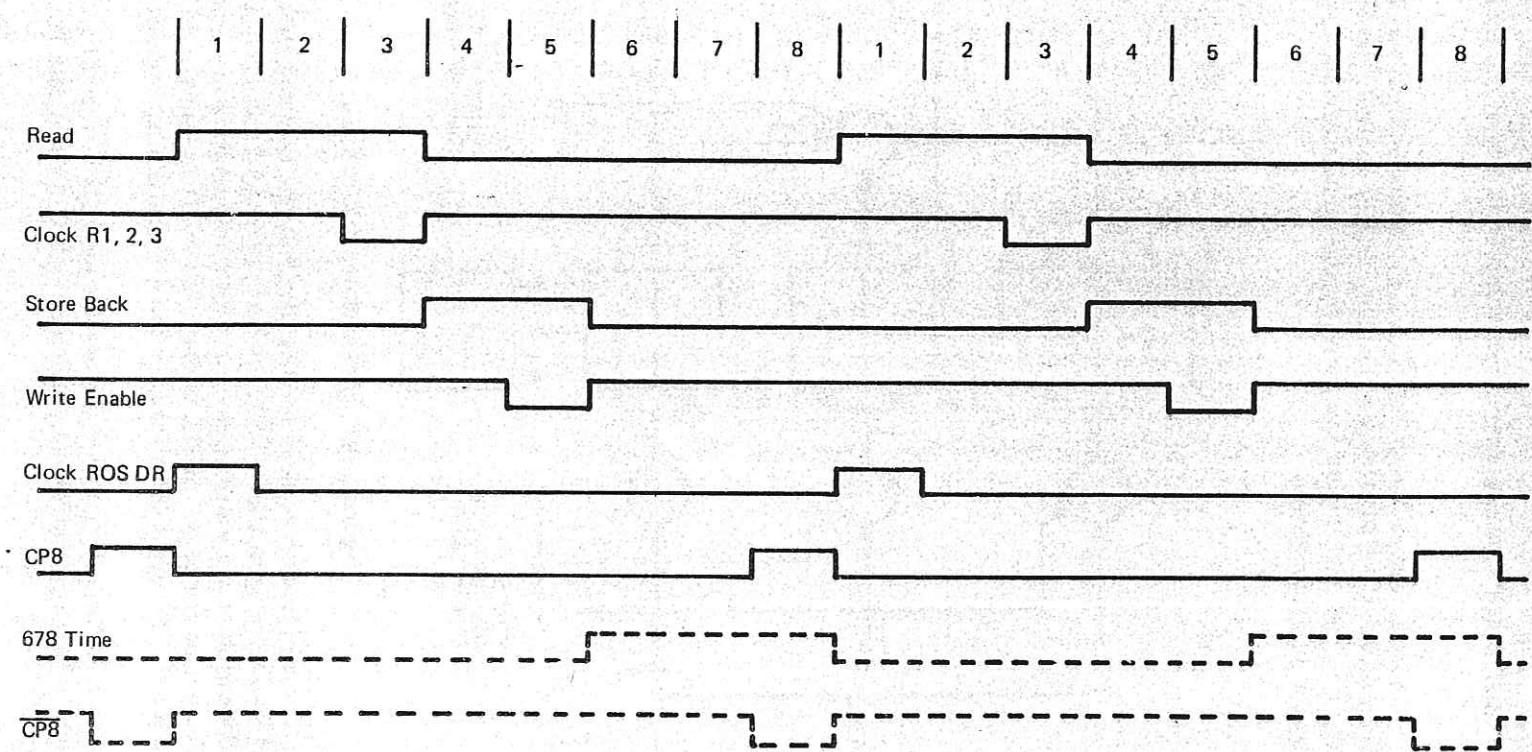


Figure 3-24. Local Store Timing

During Store Back (45 time) the past processor or cross couple and destination bits are selected, the appropriate data bank is enabled, and a selection is made between storing the high or low order bits in the designated bank. During Write Enable time, data is written into Local Store. The read and store back pulses are generated in the timing logic.

Clock ROS DR occurs at CP1 time and generates the current processor data bits. At CP8 time the ROS DR destination bits are clocked and "no store" circuitry determines if store back will occur on the next process cycle. PCO inputs to Local Store are multiplexed at 678 time. A Write Enable occurs at CP8 time.

During a read cycle, data is available to the I/O channel. PCIO data is multiplexed under control of PCIO select address bits and clocked into PCI registers at CP8 time. The PCI/PCO is determined by the CPU command ID field.

For a DMA read cycle, data is written into Local Store from the I/O channel while the Local Store address is carried through the queue. This data is clocked into Local Store at CP8 time. For a DMA write cycle, the data in registers R1, R2, R3 is clocked into R4, R5, R6 at CP8 time. Using the R4 data as the main memory address, the data flows through the queue and I/O channel into main memory.

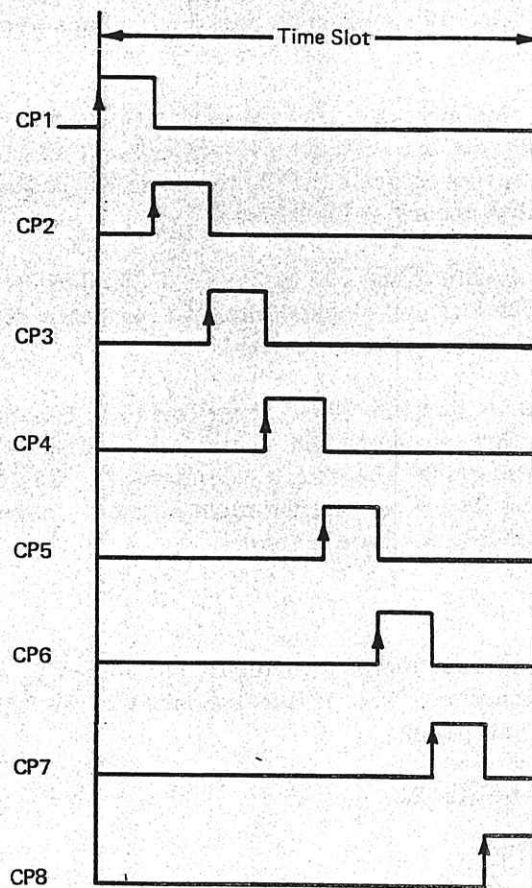
### 3.6.3 DATA FLOW ELEMENT

The data flow portion of the processor element manipulates, formats, and tests the data specified by the micro instruction. This is accomplished in the following circuitry under control of the microprogram:

- Two parallel operation 18-bit ALUs
- Data flow control multiplexers
- Working registers (R1 through R6)
- MIA Transmit Data register.

The data flow element operates as follows. The required input data determined by the microprogram is clocked from registers R1, R2, and R3 at CP4 time. The data (three parallel 18-bit words) are routed to the ALUs through the input multiplexers. Inputs to ALUs are specified as right or left as shown in Figure 3-18.

Figure 3-25, the timing diagram for local store accesses, shows the correlation between slot times and the current processor and the Read/Write activity in local store. When local store is not busy at CP4 time, an Enable gate is sent to the channel control to allow it access to the local store.



CP1 Start "If" operations not dependent on local store information; fetch data from local store

CP3 Clock local store data into R1, R2, R3 and start "If" operations that are dependent on local store Clock ROSDR into another register (ROSDR → ROSDR Buffer) to allow "ACTIONS" and "BRANCHES" to be set up properly.

CP8 "If" condition register (true/false) clocked; clock data flow into R4, R5, R6

CP1 "Actions" and "Branches" enabled; write R4, R5, R6 into local store

Figure 3-25. Data Flow Timing



The ALU combines the left argument and right argument inputs in one of 16 logical or arithmetic formats. These operations are defined in the Micro instruction Principles of Operation.

The outputs of the ALUs are routed through the multiplexer and clocked into registers R4, R5, and R6 at the leading edge of CP8. These outputs will be reloaded into local store at CP6 through CP2 time. All of the actions following clocking at the rise of CP3 time must occur prior to clocking at the rise of CP6 time. Registers R4, R5, and R6 are also used to load the DMA queue for DMA requests.

### 3.7 REDUNDANCY MANAGEMENT (RM) HARDWARE LOGIC

Fault detection, identification, and subsequent reconfiguration of the GPC redundant set is accomplished by using elements within the computer, as well as elements cooperating between computers and the crew panels.

Dedicated RM hardware/firmware/software is used to detect, identify, and reconfigure because of GPC critical failures, based on; (1) internal GPC status (noncooperative), or (2) status information derived external to the GPC (cooperative) i.e., from other GPCs or manual inputs). A functional block diagram of the dedicated redundancy management hardware logic is given in Figure 3-26.

#### 3.7.1 NONCOOPERATIVE ELEMENTS

The following elements are concerned with GPC fault detection, identification, and reconfiguration without the use of information external to the GPC.

##### 3.7.1.1 Detection

The following logic is used to detect GPC failures which can cause incorrect critical output.

##### 3.7.1.1.1 IOP BITE - RM Status Register

A 32-bit register contained in the IOP is used to store RM hardware status data. The contents of the register may be read by a CPU PCI command during CPU self-test and RM hardware self-test. Each position of the register is dedicated to status of a particular RM hardware element to continuously monitor the state of the logic.

##### 3.7.1.1.2 Watchdog Timer

The watchdog timer consists of a 12-bit incrementing counter with a resolution of 0.768 ms and a total capacity of 3.144960 seconds. The timer is used primarily to detect GPC cyclic failures but can also be used to indicate a failure detected by GPC self-test/BITE.

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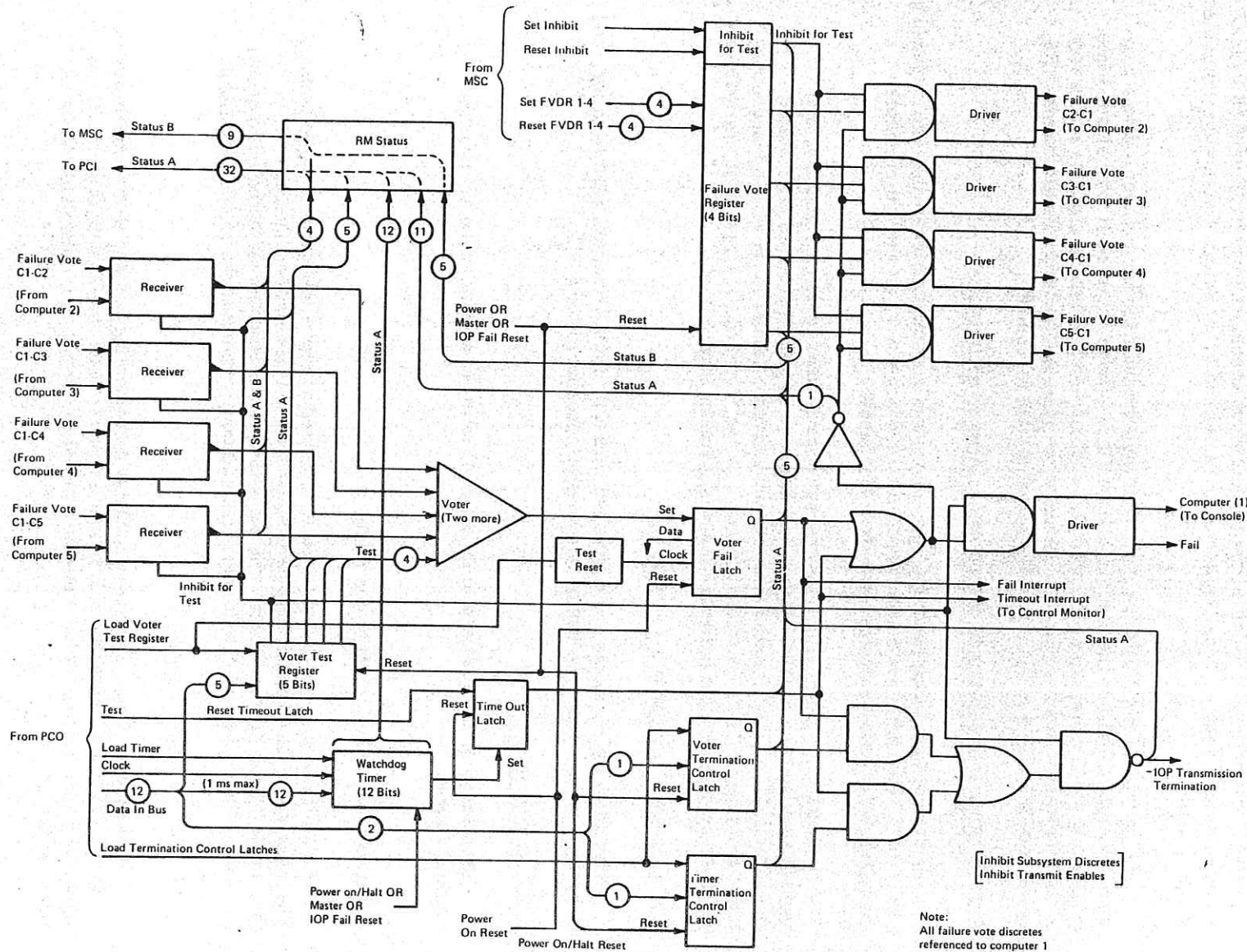


Figure 3-26. Redundancy Management Hardware Logic Diagram



At specific intervals, the timer is loaded by the CPU (PCO) to a predetermined timeout value. A correctly cycling CPU will result in a periodic reload of the timer prior to a timeout. Upon detection of an error during self-test, the CPU can also load the timer to its maximum value to generate an immediate timeout. Whenever a timeout occurs, a timeout latch is set to identify a failure in the GPC. A timeout occurs whenever the timer is allowed to count up to its maximum value and overflow.

The watchdog timer is reset for any IOP reset signal. After a reset, as defined in Table 3-3, the timer will not set the timeout latch unless it is loaded by the CPU and subsequently times out (overflows). Once loaded, the timer begins counting immediately.

#### 3.7.1.2 Identification

The following RM hardware is used for noncooperative identification of GPC failures.

##### 3.7.1.2.1 Timeout Latch

The timeout latch is initially reset (logical zero) by an IOP Power Reset or Halt discrete input from the mode switch. It is subsequently set by the watchdog timer whenever a timeout occurs. The output of this latch is transmitted to the computer fail driver, failure vote inhibit, and transmission termination control logic. When set, the latch also generates a timeout interrupt to the control monitor.

##### 3.7.1.2.2 Computer Fail Driver (Fail Discrete)

The computer fail driver is used to transmit a GPC critical failure indication to the Control and Display Console for both noncooperative and cooperative GPC failure identification. When a noncooperative critical failure is detected by timeout of the watchdog timer and the timeout latch is subsequently set, the computer fail driver transmits a logical one output discrete for distribution to appropriate annunciators on the crew panel. A logical zero output from the driver indicates that the GPC is powered on and operating normally, powered off, or the mode switch for the GPC is in Halt (position 1).

##### 3.7.1.3 Reconfiguration

The GPC redundancy management provides for both automatic and manual modes for reconfiguration of the GPC operating set when a critical failure in a GPC is detected and identified. Reconfiguration involves removal of a GPC from functioning as a member of the redundant set.

##### 3.7.1.3.1 Watchdog Timer Timeout Interrupt

If the timeout latch is set, by a timeout of the watchdog timer, a watchdog timer timeout interrupt is generated to the control monitor in the IOP. Subsequent CPU action



when a timeout interrupt occurs is dependent upon the existing GPC redundant configuration and the hardware status of IOP transmission termination control logic.

### 3.7.1.3.2 Transmission Termination Control

Status of the transmission termination control logic determines whether the automatic or manual mode for reconfiguration has been enabled in the IOP. Manually-operated switches on the Controls and Display (C&D) Console generate input discretes to each GPC to provide manual reconfiguration for 12 critical channels in two groups of 8 and 4. Manual reconfiguration may also be effected via keyboard inputs.

**3.7.1.3.2.1 Timer Termination Control Latch (TTCL)** – The logical output of the timer termination control latch is used to control automatic IOP transmission termination and reconfiguration in the noncooperative failure identification mode using the watchdog timer. If the TTCL has been enabled and a timeout of the watchdog timer subsequently occurs (to set the timeout latch), an IOP Fail Reset signal is generated to reset IOP hardware except for the voter fail latch and timeout latch. If the TTCL was not set prior to the timeout, a Fail Reset signal is not generated when the timeout occurs.

**3.7.1.3.2.2 Transmission Control Output Logic** – The TTCL control of the automatic transmission termination mode is implemented by a logical AND of the TTCL output and the timeout latch output. Whenever both latches are set a (logical one) is generated and transmitted to a subsequent logical OR invert circuit in the control logic which generates a transmission termination signal for both noncooperative and cooperative automatic IOP transmission termination modes. During normal operation, the output of this circuit is a logical one. A logical zero output generates the signal for termination.

**3.7.1.3.2.3 IOP Fail Reset** – Whenever timeout occurs with the timer termination control latch set, an IOP Fail Reset is generated. The IOP Fail Reset signal will reset IOP hardware as indicated in Subsection 3.7.1.3.2.1.

### 3.7.1.3.3 Failure Vote Inhibit

When a GPC is identified as failed by either cooperative or noncooperative RM hardware, its failure votes to other GPCs are inhibited by this circuit. In noncooperative RM failure detection and identification, set of the timeout latch will activate this circuit to prevent outputs of the Failure Vote Register (FVR) from propagating to the Fail Vote discrete drivers. The inhibit circuit provides one input to each logical AND associated with a fail vote discrete driver. An RM failure indication generates a logical zero (inverter) output to the respective logical AND gates to provide the inhibit signal. During normal operation, the output of the inhibit circuit is a logical one. Any IOP reset which resets the timeout latch and the voter latch will remove the failure vote inhibit function.

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### 3.7.2 COOPERATIVE HARDWARE/FIRMWARE ELEMENTS

The following elements are concerned with GPC fault detection, identification, and reconfiguration using information external to the GPC.

#### 3.7.2.1 Detection

Cooperative detection of GPC faults is performed in software by a compare and test.

#### 3.7.2.2 Identification

The following elements are involved in cooperative identification of GPC failures.

##### 3.7.2.2.1 Failure Vote Generation/Transmission

The results of the compare word test are used to set dedicated discretes to other GPCs in the GPC redundant set and to the D&C Console.

3.7.2.2.1.1 Failure Vote Register (FVR) - Each IOP contains a 4-bit register which is used to identify a noncompare with another GPC as a result of the compare word test. When a noncompare is detected, a bit is set in this register (FVR). Each position of the FVR is associated with another GPC within the DPS. The outputs of the FVR are used to set dedicated discretes to any GPC whose compare word, as received, does not agree with the corresponding word generated by the computer performing the compare. The FVR is set and reset under control of the MSC and is automatically reset (to logical zeros) for any reset of the IOP.

3.7.2.2.1.2 Fail Vote Discrete Drivers - Each output of the FVR is logically connected to an independent discrete driver. Each fail vote discrete driver has two dedicated outputs. One output is routed to indicators on the crew panel. The other output is wired to a discrete receiver in the IOP of one of the other GPCs (the one corresponding to the dedicated FVR position). Thus, each GPC contains four fail vote discrete drivers for transmission of the results of the compare word test to other GPCs (and to the crew panel). Whenever a GPC detects a noncompare with another specific GPC and the corresponding bit is set in its FVR, a noncompare indication (fail vote) is transmitted to a fail vote discrete receiver in the other GPC.

3.7.2.2.1.3 Fail Vote Discrete Receiver - Each IOP contains four discrete receivers to receive dedicated vote discretes from other GPCs. The outputs of the receivers are transmitted to voting logic to evaluate the GPC operating status as detected by other computers in the operating redundant set.



#### 3.7.2.2.2 Voter Logic

Voter logic accepts the outputs of the fail vote discrete receivers and generates an output to set a voter fail latch whenever two or more fail vote discretely are received from other GPCs.

#### 3.7.2.2.3 Voter Fail Latch

The voter fail latch is reset to a logical zero by an IOP Power Reset or a Halt Discrete Input from the Computer Mode switch. It is set by voter logic whenever two or more fail vote discretely are received. The output of the latch is transmitted to the computer fail driver, failure vote inhibit, and transmission termination control logic. When the latch is set, it also generates a fail interrupt to the control monitor.

#### 3.7.2.2.4 Computer Fail Driver (Fail Discrete)

The computer fail driver is used to transmit a GPC critical failure indication to the Controls and Display Console for both noncooperative and cooperative GPC failure identification. When the voter fail latch is set to a logical one, the computer fail driver will transmit an output discrete to the crew panel. Transmission of a logical zero output corresponds to a GPC that is powered on and operating normally, powered off, or has received a Halt discrete input (Computer Mode switch is in position 1).

#### 3.7.2.3 Reconfiguration

Reconfiguration involves termination of the role of a GPC as a functioning member of the redundant GPC set. Both manual and automatic reconfiguration modes are implemented by redundancy management when a critically-failed GPC is detected and identified.

##### 3.7.2.3.1 Fail Interrupt

Whenever the voter fail latch is set by voter logic, an interrupt is generated to the control monitor in the IOP. The CPU is informed of the interrupt by a PCI. Subsequent CPU action when a Fail interrupt occurs is dependent on GPC redundant configuration and IOP hardware status.

##### 3.7.2.3.2 Transmission Termination Control

Activation of the automatic mode for reconfiguration is determined by the status of the transmission control logic in the IOP. Manually-operated switches located on the Control and Display Console are used to generate input discretely to each GPC during manual reconfiguration.

3.7.2.3.2.1 Voter Terminal Control Latch (VTCL) - Automatic IOP transmission termination and subsequent reconfiguration is controlled by the output of the VTCL when a critical failure is detected and identified by cooperative RM hardware. The VTCL may be set (enabled) or reset (disabled) under software control of the CPU, or by manual inputs from the crew. The latch is automatically reset when any IOP



reset is generated. If the VTCL is enabled and the voter fail latch is subsequently set, an IOP Fail Reset signal is generated to reset IOP hardware except for the voter fail latch and timeout latch. If the VTCL is not enabled when the voter fail latch is set, the IOP Fail Reset signal will not be generated.

3.7.2.3.2.2 Transmission Control Output Logic - VTCL control of automatic reconfiguration is achieved by a logical AND of the outputs of the voter fail latch and the VTCL. Set of the VTCL acts as a gate to transmit a signal to the output inhibit circuit (logical OR-invert) which generates a transmission termination signal. The output of the logical OR-invert is held at a logical one during normal operation. This output transmits a logical zero to generate transmission termination.

#### 3.7.2.3.3 Failure Vote Inhibit

When any GPC is identified as critically failed by either cooperative or noncooperative RM hardware, transmission of its failure votes to other GPCs (and the crew panel) are inhibited. During cooperative critical failure detection and identification, the failure vote inhibit is activated when the voter fail latch is set. When the voter fail latch is set, the inhibit generates a logical zero (inhibit) input to each logical input AND circuit associated with a fail vote discrete driver to prevent propagation of the FVR contents to the discrete drivers. At any time the voter fail latch is reset (logical zero output) the failure vote inhibit circuit will gate the FVR contents to the fail vote discrete drivers. The circuit operates to prevent a critically-failed GPC from further participation in cooperative critical failure detection.

### 3.8 POWER SUPPLIES

#### 3.8.1 GENERAL

Power supplies convert the 28 VDC input power into the required IOP operating voltages (+12 VDC, +5 VDC, and -5 VDC, -12 VDC). The IOP power supply unit is identical to the AP-101 CPU unit and operates in conjunction with it in regard to power on/off sequencing. At power up or power down (or loss of power), the power supply is sequenced on or off in an orderly fashion to assure that no stored data or program is affected by transient signals. A block diagram of the power supply is given in Figure 3-27.

The power supply consists of the following functional blocks:

- Electromagnetic Interference (EMI) Filters
- DC/DC converters
- Transformers
- Rectifiers and Filters (mounted on backpanel)
- Series dissipative regulator (SDR)
- Internal voltage module
- Controller assemblies
- Built-in-Test equipment.

Each of these blocks is subsequently described.

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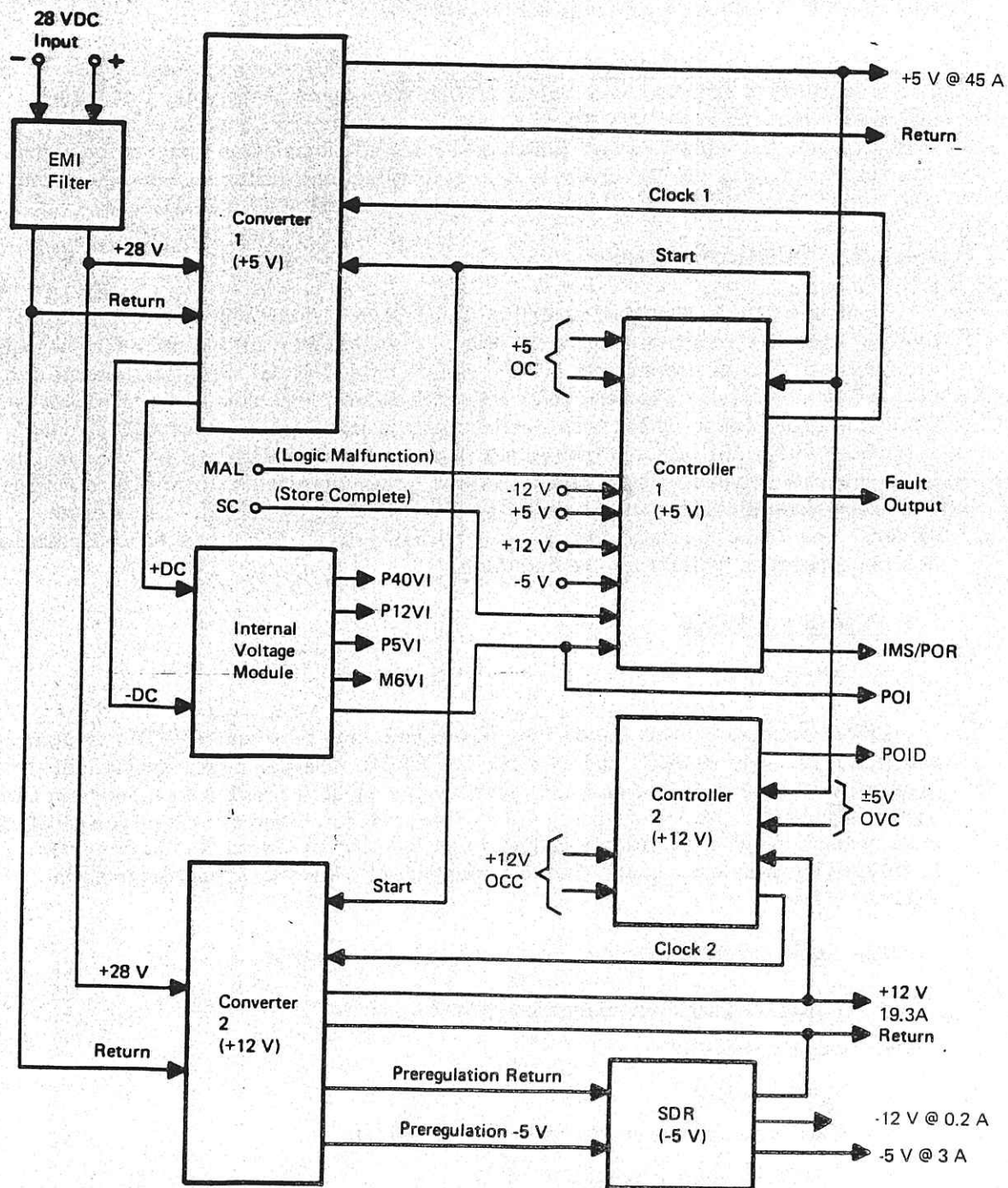


Figure 3-27. IOP Power Supply Block Diagram



### 3.8.2 FUNCTIONAL DESCRIPTION

#### 3.8.2.1 Converter

The converter-regulator section contains an input ripple/energy storage filter, converter driver circuits, and a pulsewidth-modulated DC-to-DC converter operating in the 25-kHz region. Figure 3-28 is the schematic diagram for the input filter and converter that provides a single output voltage (+5 VDC). Power transistors Q1 and Q3 or Q2 and Q4 conduct simultaneously, in a standard push-pull (pulsewidth modulated) configuration.

The separate primary and secondary circuits on transformer T1 provide a definable degree of load share imbalance between simultaneously conducting transistors, with a combined worst-case peak current of less than 30 A. For example, differences in the storage times between Q1 and Q3 cannot result in full-load transfer to the last conducting transistor, because T1 presents a substantial leakage inductance component between the two loosely coupled primary windings. The load transfer rate is limited to a maximum of  $1\text{A}/\mu\text{s}$  of storage time differential. In contrast, very tight coupling between a given primary and its associated secondary results in low stress levels on the converter power transistors rated at 15 A.

The voltages impressed across the transformer primary windings by alternate switching of the converter transistors also appear across the respective secondary windings (modified by the turns ratio). The voltage waveform is fullwave-rectified by diodes CR1, CR2, CR3, and CR4, and the rectified voltage is applied to the input of a low-pass filter comprised of L1, L2, and  $C_{out}$ . The filter output is DC with a small AC ripple component at twice the operating frequency of the converter.

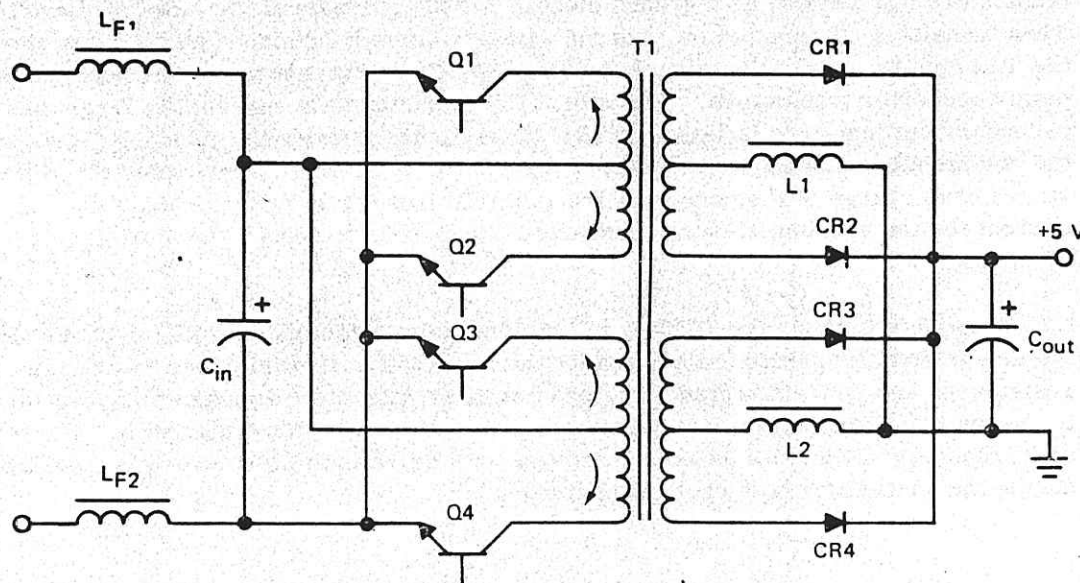


Figure 3-28. Input Filter and Converter



A variable frequency, variable pulsewidth controller (described in Subsection 3.8.2.3) monitors the output voltage and adjusts the duty ratio (ratio of converter transistor "on" time to period of converter operation) to maintain constant DC output voltage. The steady-state duty ratio required to maintain a regulated output voltage is a direct function of the input voltage and is related to the output current only through second-order effects, such as changes in efficiency in the circuit. The duty ratio does, however, change significantly in response to load current transients.

Additional secondary windings, each having its own rectifiers and filters, are added to the transformer to obtain additional output voltages. While only the main output (the one sensed by the controller) is closely regulated (+1%), other outputs are effectively preregulated (+5%) during steady-state operation by the control loop to compensate for changes in input voltage. Voltage transients on the preregulated outputs may occur when the control loop is compensating for changes in main output load current, but these transients will be limited to approximately  $\pm 5\%$  of the nominal DC output voltage by the output filters. Further regulation of the preregulated outputs is provided by series dissipative regulators.

### 3.8.2.2 Converter Driver Operation

The schematic for the power converter current drivers and control logic is shown in Figure 3-29. The Start input to the control logic is provided by the controller module as an Inhibit signal during power system start-up and shutdown. The Clock input logic signal from the controller module contains the variable rate and variable pulsewidth information required for proper control of the power converter.

The push-pull logic alternately connects the Clock data to the two current sink transistors (Q3 and Q4) as a ground closure for the duration of the clock pulsewidth. Then transistor Q3 is gated on, and the constant current furnished by Q3 flows through the T1 primary (predominately), providing base drive current to the two odd-numbered power converter transistors. The value of T1 inductance is sufficiently large that the secondary current drop is less than 15% at maximum pulsewidth. When Q3 is gated off, the voltage stored on C3 (as a result of the preceding drive current), plus the reflected stored base charge of the converter transistor, turns Q1 on and provides turn-off current for the associated power converter transistors to reduce the storage and turn-off times.

The +40-V bias source (P40VI) in conjunction with zener diode VR1 assures that the driver circuit operates in a Constant Current mode. Transformer secondary resistances and converter transistor base-emitter saturation voltages are controlled to assure a 20% (or better) match between power transistor drive currents. Current sink transistor Q4 and its associated components drive the power converter transistors during the succeeding half-cycle of operation.

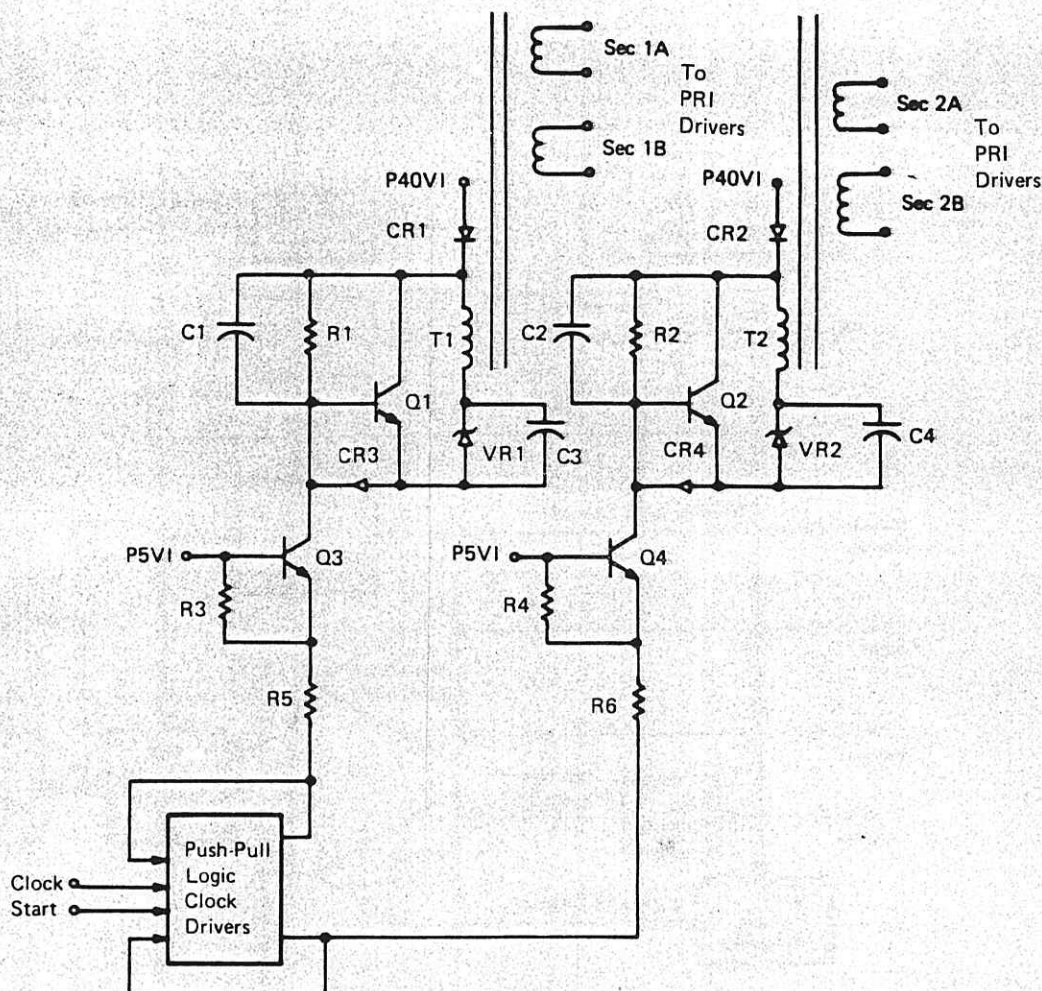


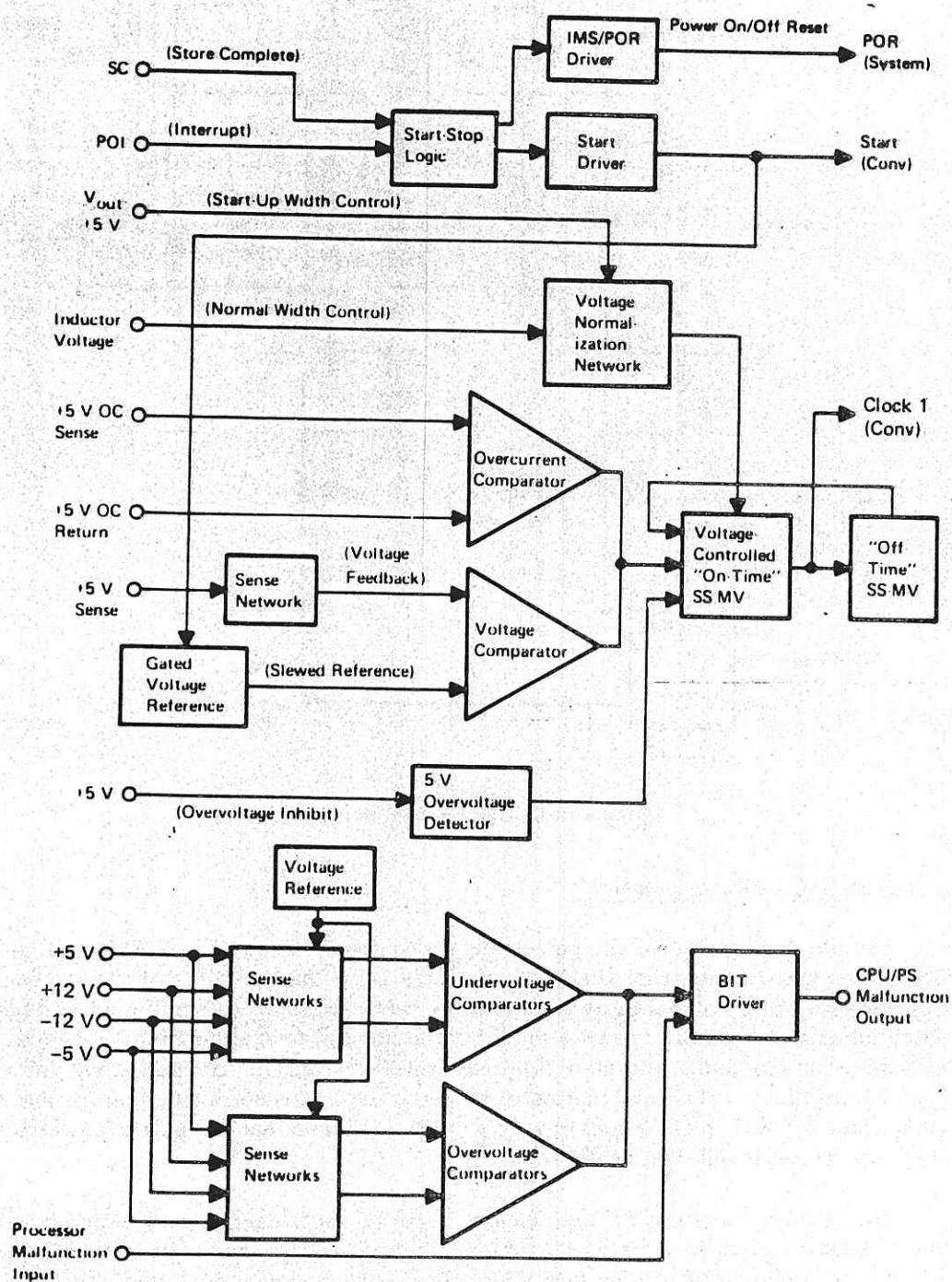
Figure 3-29. Converter Driver Circuit

### 3.8.2.3 Controller Operation

The block diagram for the power supply controller module is shown in Figure 3-30. The power On/Off Interrupt (POI) signal, input from the internal voltage module, permits the converter Start signal to go to an enable level, after all internal bias voltages are established and the power source is within the normal operating range. The Start signal also gates on the controlled rise-time reference voltage for the main-loop voltage feedback comparator. The combination of a controlled reference voltage slope and start-up pulsewidth control, proportional to  $V_{out}$  (+5V), assures that the power converter start-up stress levels are controlled.

The remainder of the voltage feedback control loop comprises a variable-width multivibrator (width inversely proportional to line voltage) and a fixed-width multivibrator which establishes the minimum time between successive half-cycles of converter switching. The overcurrent comparator output is ORed into the main loop voltage comparator output to provide overcurrent protection.







#### 3.8.2.4 Internal Voltage Operation

The block diagram for the internal voltage circuit is shown in Figure 3-31. The central part of the circuit is a stored-energy, single-ended, DC-to-DC converter operating at 35 kHz. This circuit provides four ground-isolated, regulated, bias voltages for operating the control circuits of the power supply.

The switch transistor (Q1) operates directly from the filtered 28-VDC input source. Q1 is driven from a pulse transformer and gated current sink in a manner similar to that of the power converter drivers.

An isolated secondary winding provides operating power for the internal voltage controller and drive circuits, while maintaining isolation from the main power supply output return. This same secondary is voltage-sensed to provide regulation for all five output voltages. Controller power is temporarily provided by a low-current regulator during the start-up interval of approximately 3 ms.

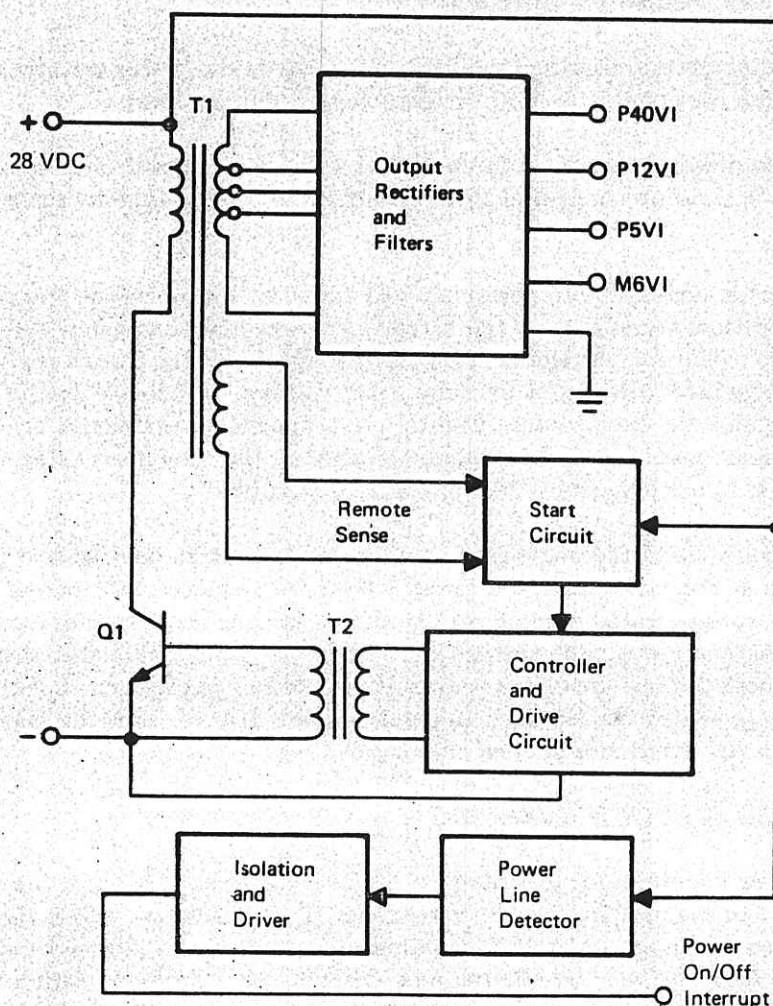


Figure 3-31. Internal Voltage Block Diagram

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The internal voltage controller consists of a voltage comparator, an RC timing network, a threshold comparator, and pulse drivers. Timing is accomplished by alternately charging and discharging the timing capacitor between the hysteresis points of the threshold comparator. The capacitor charge time (output on time) is set by the input line voltage magnitude to provide a fixed voltage-time product for the power transformer. The capacitor discharge time (output off time) is set by the feedback voltage comparator error signal.

The internal voltage module also contains a voltage detector circuit which monitors both the input line voltage (DC equivalent) and its own sense voltage. The combined voltage status signal is transformer isolated via a 1-MHz oscillator to provide a Power On/Off Interrupt (POI) logic output. The POI signal initiates power converter operation during start-up and inhibits converter operation during interruption of either power source or internal bias voltage.

#### 3.8.2.5 Series Dissipative Regulators

Series dissipative regulators (SDRs) are used in the power system to provide voltages which have small (6 ADC or less) load requirements.

Since the power dissipation in an SDR is proportional to the voltage across the series pass transistor, it is desirable to minimize this voltage to achieve reasonable efficiency.

The voltage necessary to power an SDR for a specified output voltage is provided by adding additional windings on the already present high-frequency (25-kHz) power transformer. This AC voltage is fullwave-rectified and LC filtered (as in the main converter-regulator voltage) to produce a DC voltage. Since the duty-cycle factor required to maintain steady-state regulation is dependent primarily on line voltage rather than load conditions, the voltage obtained in this manner varies very little, even though it is not sensed by the converter controller.

The turns ratio of the converter power transformer is designed to place the SDR input voltage at approximately 2 V greater than the required SDR output voltage. The SDR utilizes an integrated circuit voltage amplifier and a current driver in conjunction with a Darlington series pass transistor. Gain and frequency stabilization networks are used in both the low-level and power stages of the regulator. Local overcurrent protection is provided via foldback limiting of each SDR to limit the maximum SDR dissipation in the event of a severe overload.

#### 3.8.3 POWER SUPPLY SEQUENCING

The power supply internal voltage circuit is the first section of the power supply that responds to the application or restoration of input power. When the filtered 28-V power reaches a voltage level of approximately 12 VDC, the internal voltage circuit starts (see Figure 3-32). Regulated bias voltages are developed with a controlled rise



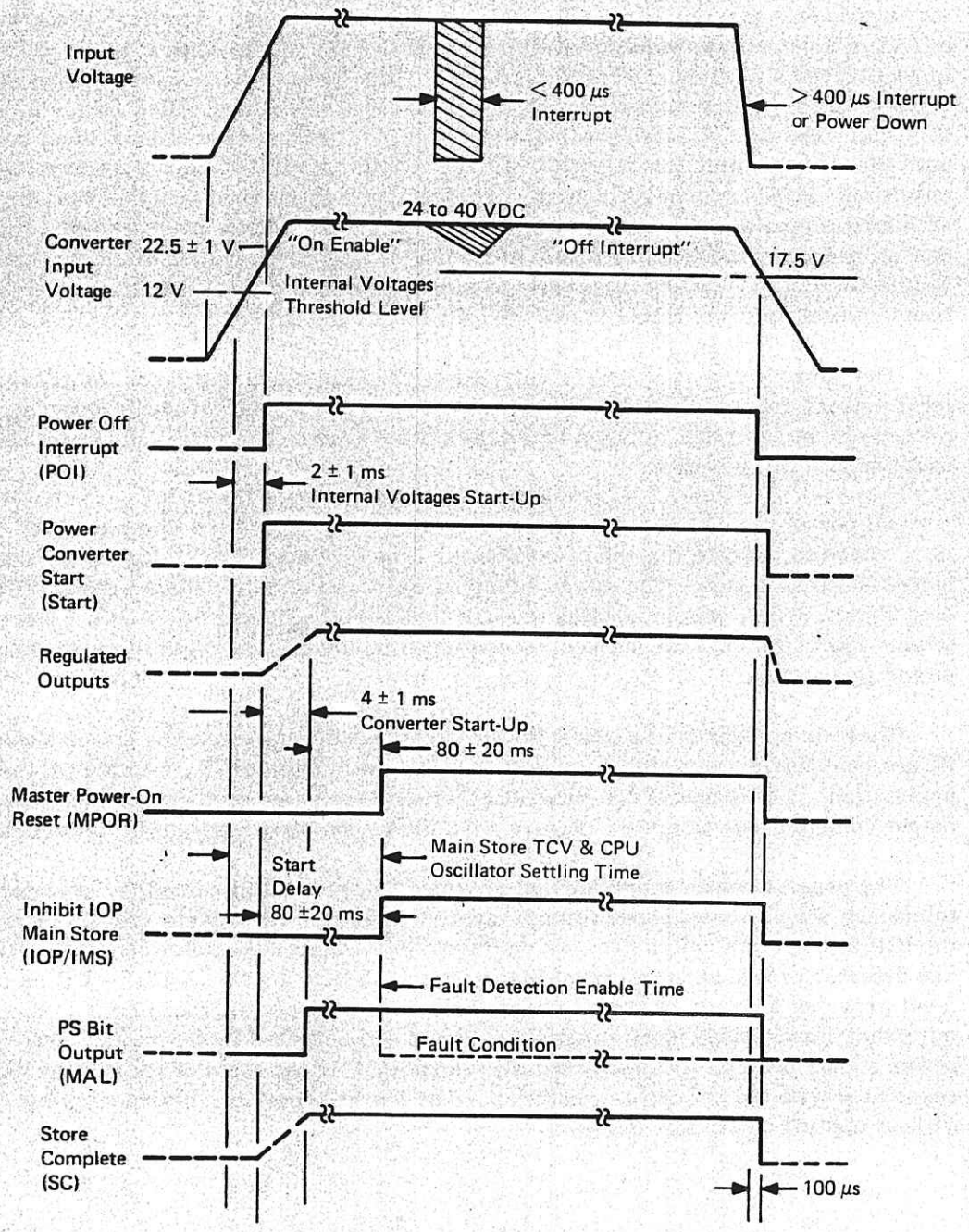


Figure 3-32. Power Supply On/Off Timing Diagram



time of  $2 \pm 1$  ms, during which time a continuously clamped Power Off Interrupt (POI) signal prevents main power supply functions from beginning. A voltage detector set at 95% of nominal bias voltage levels releases the POI clamp when the filtered 28-V input reaches a minimum level of 21.5 VDC. The main converter-regulators are then enabled and regulated output voltages are generated with a controlled rise time of  $4 \pm 1$  ms. The IOP Master Power-On Reset (MPOR) signal is at a down level condition until  $80 \pm 20$  ms after the regulated voltage monitor circuits indicate an in tolerance condition. MPOR is available at the interface and will be used in the power supply as an Inhibit signal to the inhibit clamp. The signal is at a down level condition to inhibit operation from sensed power application until  $80 \pm 20$  ms to ensure stabilization of the timing oscillator. During the power-on sequence, all interrupts will be reset and will remain reset until the signal rises. These events are illustrated in the timing diagram.

The power-down sequence is initiated by the POI signal whenever the filtered 28-V input voltage decreases to a level of 17.5 VDC. Upon receipt of the POI signal, the IOP processes the interrupt to begin terminating operation. The POI is also sent to the CPU to terminate its operation.

All power supply functions continue normally until the Store Complete (SC) signal is received to indicate the end of operation. The issuance of SC initiates the actual power-down sequence. The power supply control signal Start inhibits the MPOR signal (see Figure 3-28), which initiates the IOP Inhibit Main Memory (IOPIMS). Once the power-down sequence has started, it continues to completion regardless of subsequent power line status.

There is no danger of a power-down "race" condition, since the power supply output filters can sustain regulated voltage levels for a minimum of  $25 \mu s$  following the Inhibit application. The status of the general system clamp is assured during the power system output voltage decay interval. Figure 3-33 shows the power-up/power-down controls.

The present power supply design provides an operational capability (all outputs in tolerance) down to a net input voltage level of 15 VDC. To provide adequate time for the IOP to complete any in process operation following a POI indication, the POI voltage detector provides an interrupt signal at a 17.5 VDC level. A 17.5 VDC interrupt level provides adequate margin to permit the power supply to ignore combinations of minimum steady-state input voltage and ripple or conducted interference. The IOP power supply has built-in energy storage capability, in the form of input filter capacitors, associated with the converter regulator. The power supply can continue to function without applied power for  $400 \mu s$ .

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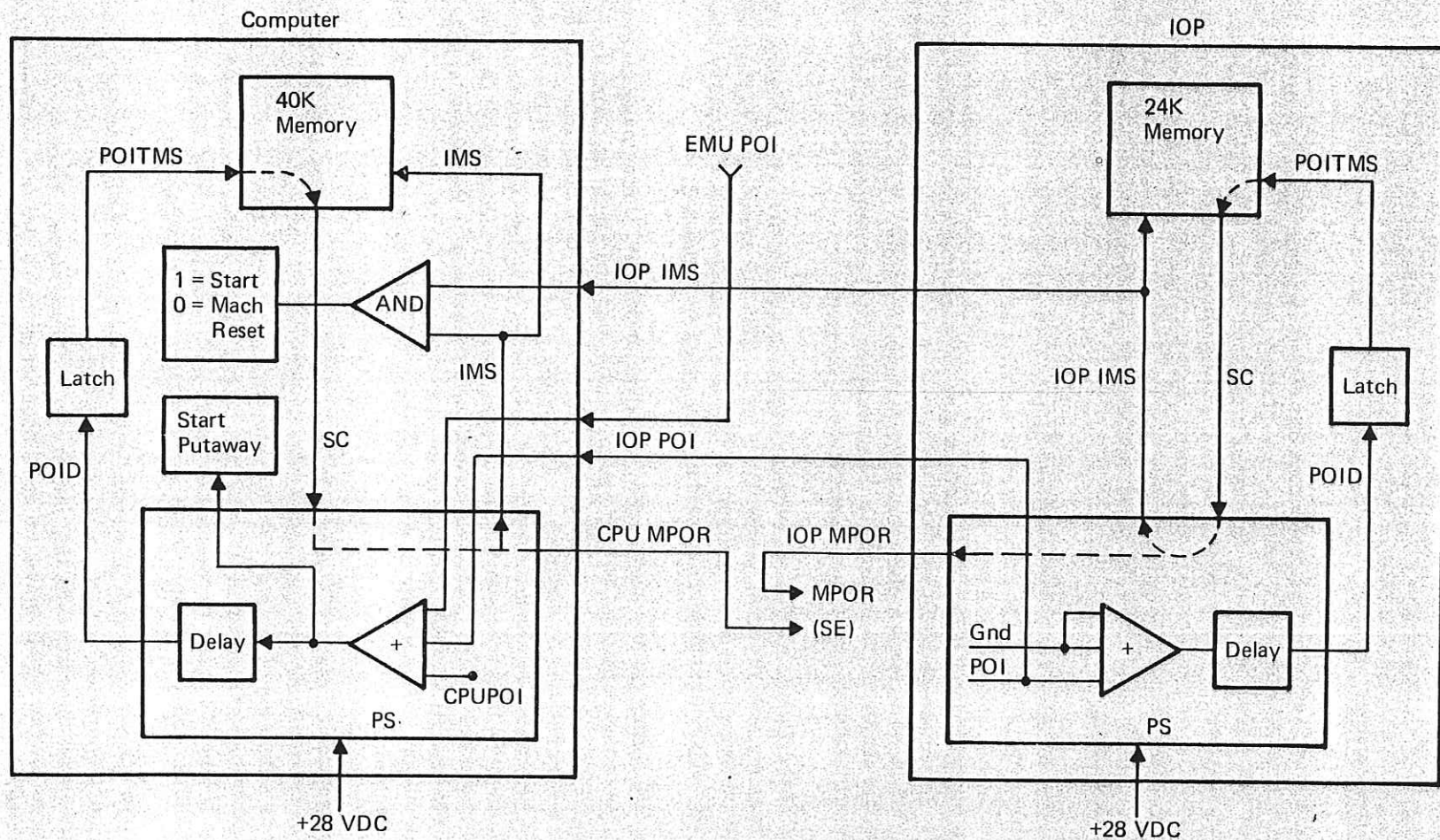


Figure 3-33. Power Up/Down Controls



### 3.9 IOP MEMORY

The Space Shuttle main storage consists of two separate Extended Performance/Modular Core Memories (EP/MCM). One of these memories, having a storage capacity of 40K words by 36 bits, is located in the CPU LRU. The other memory, with a storage capacity of 24K words by 36 bits is located in the IOP LRU (Figure 3-34). Both memories communicate directly with the CPU; the IOP memory via a differential interface. This subsection briefly describes the IOP memory. A more detailed functional description of the EP/MCM can be found in the memory section of the CPU functional description.

The EP/MCM is a 2-1/2D organized ferrite core memory having a basic modularity of 8K words by 18 bits. The core array is a planar structure of 8 mil (ID), 14 mil (OD) cores on 15-mil centers in a 256 by 576 matrix. This array is attached to two multi-layer interconnection boards (MIBs) which are, in turn, bonded to separate heat sink frames. These two sections are folded together about flex tapes connecting the top parts of the MIBs to form a pluggable storage page assembly. The core array is contained on the inside of the page while medium scale integration (MSI) drive and sense modules are mounted to the outside surfaces of the page.

Two of the 18-bit, 8192-word storage pages, in conjunction with a timing page, yield a memory capacity of 8K words by 36 bits. The IOP memory is expandable in 8K by 36-bit increments up to a maximum of 24K words within the IOP memory backpanel. A summary of performance characteristics is given in Table 3-8.

The IOP timing page is structurally identical to the CPU timing page. These pages are similar to the standard 4 Pi logic page, except that the height has been increased to allow space for mounting a delay line, and two connectors have been added to the top of the page for increased I/O capability. The timing page interfaces with the storage pages via the bottom two connectors on the page which plug into the memory backpanel. All CPU/memory interface signals are through the top two connectors of the timing page. For the IOP timing page, this interface is differential. Receivers are the standard 9615FM type (IBM 6088602) while drivers are the S/N 55113 (IBM 6088856-1) with Tri-State outputs. These outputs remain in the high impedance state until the IOP memory is selected.

A bidirectional data bus is employed at the IOP memory interface to conserve I/O pins. The transmitting and receiving times for this bus are controlled within the IOP memory as a function of the store (STR) input signal from the CPU which defines the type of operation to be performed. The IOP timing page contains an address bit parity checker. If a parity error is detected on the 19-bit CAB bus, a load operation would be inhibited and an Address Parity Error signal will be issued to the CPU.

The IOP memory operates at a cycle time of 900 ns for a read operation, and 1.1  $\mu$ s for a store operation. Read access time is 475 ns. These times are referenced to the differential interface with the memory in a standby state. When the memory is in a quiescent or low power state, an additional 500 ns is required to power up to the standby state.



3-67

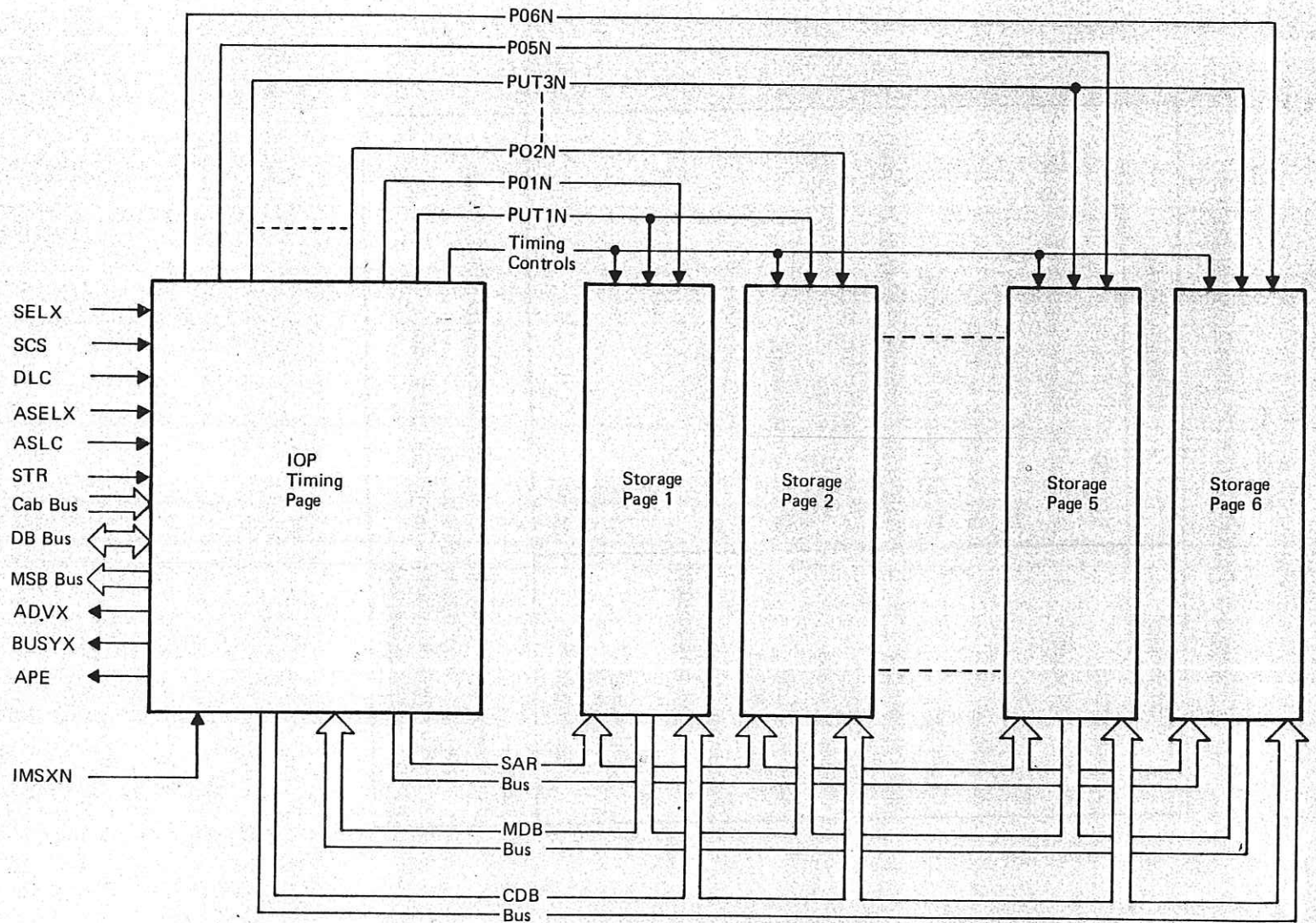


Figure 3-34. IOP Memory Block Diagram 24K x 36 Bits



Section 4  
IOP PACKAGING (PROTOTYPE)

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## Section 4

### IOP PACKAGING (PROTOTYPE)

This section describes the IOP packaging techniques, which include the following:

- IOP housing
- Multilayer interconnection boards (MIBs)
- Individual MIB nomenclature, quantity, location, and circuit population
- Assembly packaging
- Interconnections and interface configuration.

#### 4.1 IOP HOUSING

The IOP (Figure 4-1) housing conforms to standard ATR case dimensions 10.12 w × 7.62 h × 19.56 inches. With the 24K core memory, the unit weighs approximately 59 lb.

Top and bottom covers use captive, quick-release fasteners to provide access to subassemblies inside. A top cover provides access to the IOP logic, three MIA pages, the memory timing page, and the six memory pages. A bottom cover provides access to the IOP and memory backpanels, four MIA pages, power supply, and input power RFI filter. The front panel provides a mounting surface for seven circular connectors, elapsed-time indicator, fault indicator, handles, and unit installation mounting hardware. The prototype external connectors are not the same as flight configuration connectors.

#### 4.2 MULTILAYER INTERCONNECTION BOARDS

The basic electronic module is a pluggable subassembly called a "page," Figure 4-2. A page consists of two multilayer interconnection boards (MIBs) bonded to a metal frame. Insulators separate the boards from the frame. Electronic components are attached to the outer surface of each board. Heat generated by the components is conducted through the MIB to the metal page frame.

The MIBs are made of several layers of etched, copper-clad, epoxy-glass laminates bonded together under heat and pressure. Connections between conductor layers are made through plated holes. Integrated circuit flatpacks are soldered to the etched patterns on the surface of the MIBs. Discrete components are soldered in the plated holes or on the board surface, depending on terminal configuration. A conformal coating, which can be easily removed with a soldering iron to repair components underneath, is applied for environmental protection.

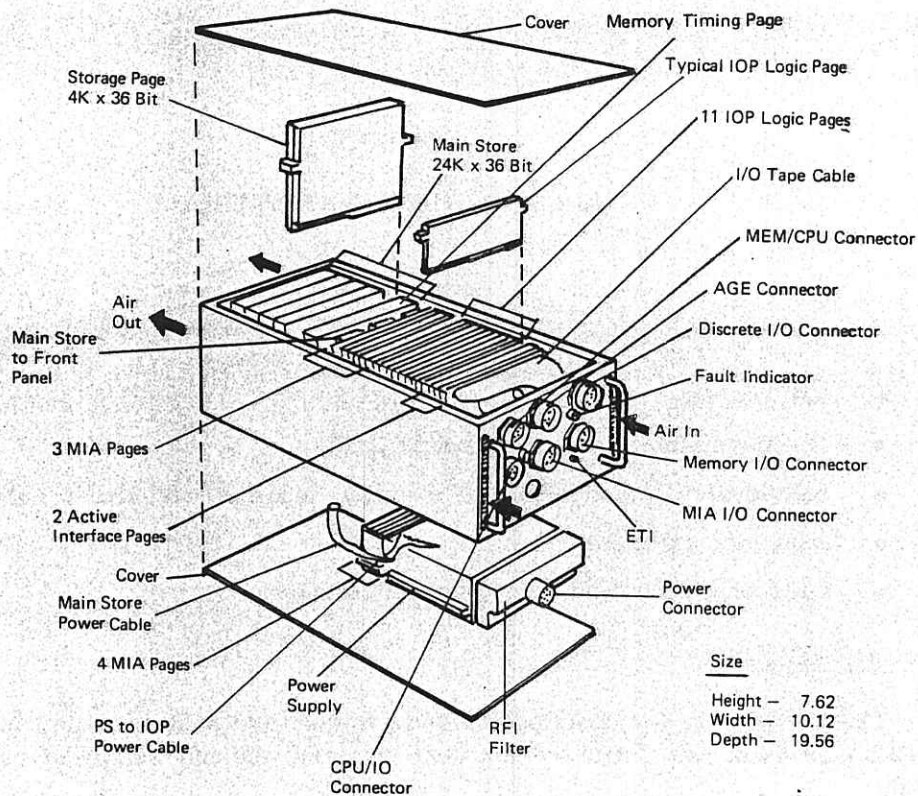


Figure 4-1. Exploded View of IOP

- Standard 4 Pi Page Extended by
  - Width Change from 8 to 9 inches
  - New Standard 120 Pin Connector

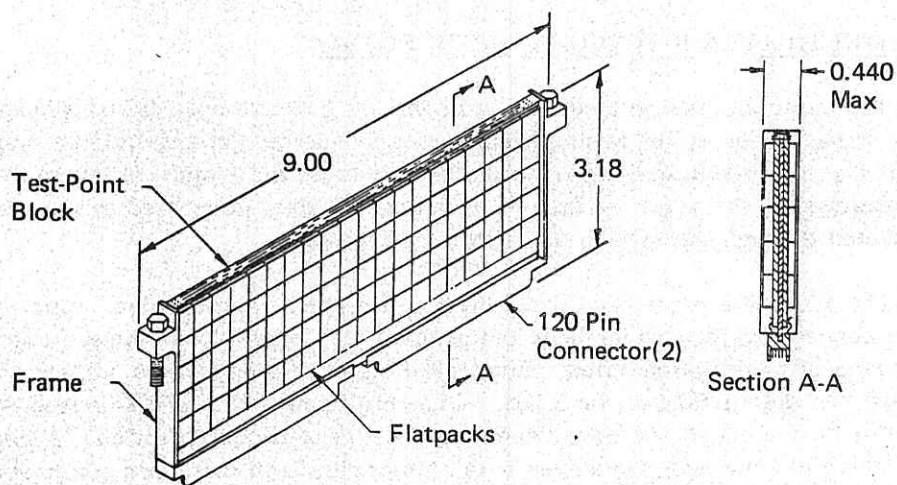


Figure 4-2. Basic IOP Page



Two 120-pin connectors are fastened along the lower edge of the page frame. The blade-and-fork contacts provide redundant current paths for each circuit. -

Sixty-four feedthrough connections and 128 test points are along the upper edge of the frame. The page is fastened to a supporting structure at the two mounting flanges (ears), with additional support provided by the connectors. The page is cooled by thermal conduction through the frame and mounting flange thermal interface. Keyed guide pins project from the lower edge of the page to guide the page during insertion, to prevent mislocation, and to ensure that the correct page is installed in the proper location. Jackscrews on the mounting flanges permit installation and removal without special tools.

Most of the pages in the IOP are packaged in this manner. The few exceptions are described in the following paragraphs.

#### 4.2.1 TAPE CABLE ASSEMBLY PAGE

The tape cable assembly (Figure 4-3) is essentially a standard page with 3/5 high MIBs on each side. A flexible, integral, polyimide-layer flat cable is located at the top edge of the MIB and terminates at a connector. The basic page design is as described in the previous paragraph, along with the following modifications:

- MIBs — In the fabrication process, an inner layer of glass epoxy in the laminated MIB is replaced by a flexible polyimide layer containing etched copper circuitry on each side.
- Page Frame — The standard page frame is modified to provide a strain relief for the exiting flexible layer at the top of the page. This design eliminates the contact blocks, containing feed-through connections and test points, along the upper edge. However, each signal line is available at plated-through holes along the top of each cable assembly MIB to permit software rework.

#### 4.2.2 IOP BACKPANEL

The backpanel is a single MIB on which IOP page connectors are mounted. One short wiring harness, using discrete wiring, is attached and strain-relieved at one end of the backpanel, for regulated DC power distribution. The harness terminates with pluggable connectors for interface with the power supply. An aluminum support plate is bonded to the backpanel to provide rigidity and mounting facilities.



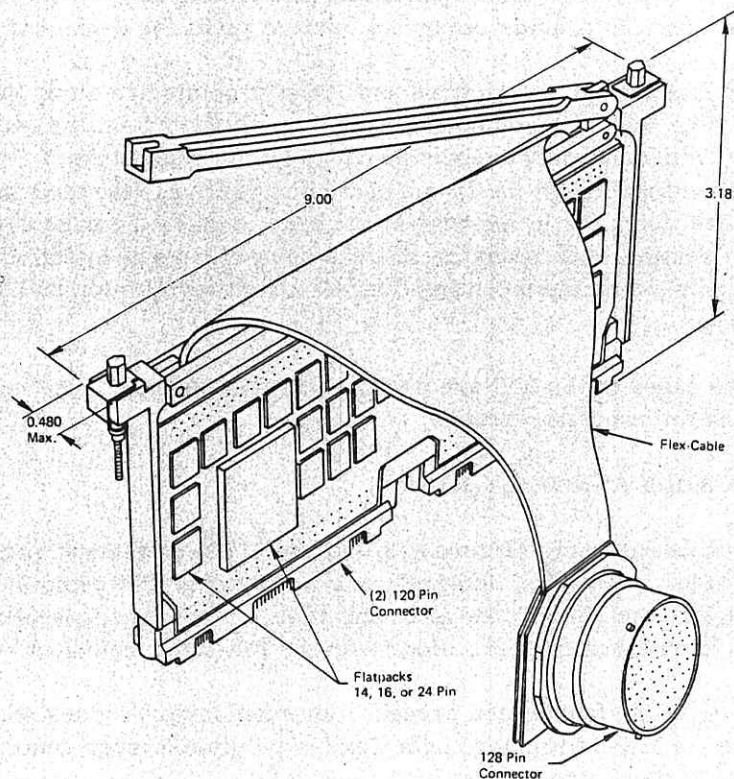


Figure 4-3. Tape Cable Assembly

#### 4.2.3 CORE STORAGE PAGE

The core storage page consists of two multilayer circuit boards, each bonded to separate heat-sink frames. The core mat is soldered to a pattern on the back of the two circuit boards, which are then folded and fastened together. By positioning the core mat between the two separable boards, the outside faces and portions of the inside faces of the circuit boards are left free for component mounting. This configuration allows sufficient mounting area for 8192, 18-bit halfwords per page.

The core mat is an array of 0.008-inch inside diameter, 0.013-inch outside diameter cores on 0.015-inch centers, in a  $256 \times 576$  matrix. The wires are continuous between the two circuit boards, with no interference with the cores where the fold is made. A Burndy UPC 92-pin right-angle connector is soldered to each circuit board along the bottom edge, one connector on each end of the assembly. These connectors interconnect the pages through the backpanel multilayer board, which is bonded to a metal support plate.

The page is fastened to the IOP supporting structure, through mounting flanges extending from each side of the page. Additional support is provided by the connectors and the backpanel support plate. Rigid aluminum support plates provide stiffness for maintaining low page deflections under vibration.

#### 4.3 PAGE NOMENCLATURE, LOCATION, AND CIRCUIT POPULATION

Table 4-1 lists each page by name and includes the page locations in the IOP and the type of circuits found on each page.

#### 4.4 ASSEMBLY PACKAGING

##### 4.4.1 IOP ASSEMBLY

The IOP logic backpanel is mounted with 14 socket-head cap screws to two rails which are brazed to the heat exchanger wall. The following pages are then plugged into the backpanel and secured to the tray rails with captive mounting hardware:

- Two interface pages
- Eleven IOP logic pages
- Three MIA pages (top)
- Four MIA pages (bottom).

##### 4.4.2 MAIN MEMORY ASSEMBLY

The main memory assembly, Figure 4-4, consists of seven pluggable pages interconnected by a multilayer circuit backpanel. Six of the pages are core storage pages, and the seventh is a timing/interface page. The storage pages measure approximately  $9.00 \times 6.42 \times 0.87$  inches. All of the core storage pages are identical and interchangeable.

The main memory backpanel is mounted directly to the structure rails with socket-head cap screws. The memory timing/interface page cable assembly is plugged into the backpanel. One memory timing/interface and six storage pages are then plugged into the backpanel and secured with captive mounting hardware.

##### 4.4.3 POWER SUPPLY ASSEMBLY

The input power circular connector attached to the RFI filter is inserted through an opening in the front panel. The filter is then secured to the structure mounting rails with captive fasteners.



Table 4-1

## PAGE NOMENCLATURE, LOCATION AND CIRCUIT POPULATION

Page	Quantity	Location	Circuit Population	Weight (lb)
AGE/Discrete I/O 6246521-1	1	A01		1.00
CPU I/O 6246520-1	1	A02		1.00
Control Monitor 6246518-1	1	A04		0.60
DMA Channel 6246514-1	1	A05		0.60
Redundancy Management 6246519-1	1	A06		0.60
Control Page 6246554-1	1	A07		TBD
Priority Control 6246513-1	1	A08		0.60
Local Store 6246516-1	1	A09		0.75
Data Flow 6246511-1	1	A10		0.60
Status Register 6246522-1	1	A11		0.66
Micro Decode 6246512-1	1	A12		0.60
MIA Buffer 2 6246555-1	1	A13		TBD
MIA Buffer 1 6246517-1	1	A14		0.60
MIA 6246523-1	6	A15-A20		5.00
Timing Interface 6246559-1	1	A21		1.50
MCM 6246079-1	6	A22-A27		11.76
Micro Store (ROM) 6104848-1	1	A31		TBD
Micro Store Page 6104844-1	1	A32		TBD

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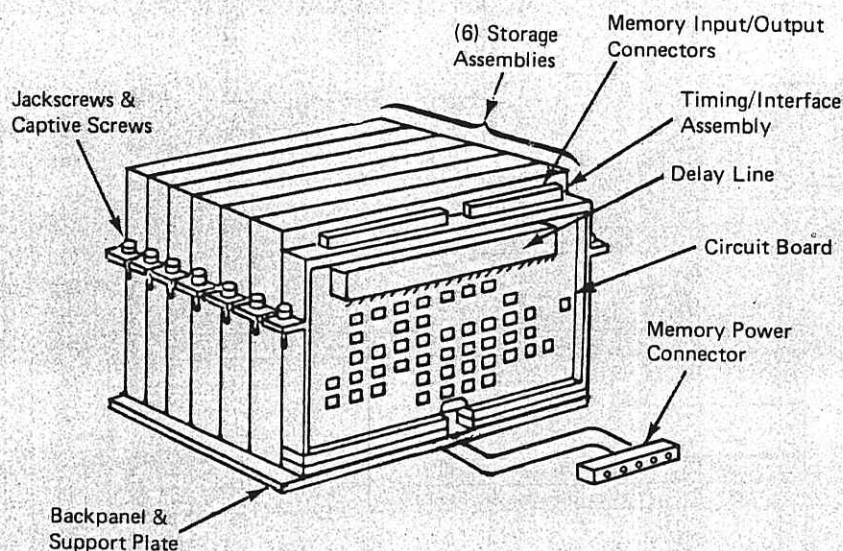


Figure 4-4. Main Memory Assembly — 24K, 36-Bit

The power supply is mounted directly to the structure rails with captive fasteners. Regulated DC power distribution cables from the IOP backpanel and memory backpanel assembly are then plugged into the power supply.

#### 4.5 STRUCTURE DESIGN

A dip-brazed, aluminum alloy housing with finned heat exchangers on the side walls is the main structural member. Cooling air is forced through, and contained within, the heat exchanger, thus preventing direct impingement of air on subassemblies and components. Aluminum rails, brazed to the heat exchanger, provide mounting surfaces and thermal conduction paths for all pages and assemblies.

#### 4.6 IOP/CPU INTERCONNECTIONS

Refer to Figure 4-5 for the GPC prototype model interface configuration and Table 4-2 for connector J1 through J7 pin functions. The interconnecting external cables are shielded, twisted pairs having a nominal line-to-line characteristic impedance of  $68\Omega$ , a nominal line-to-line distributed capacitance of 25 pF per foot and a nominal line to shield capacitance of 45 pF/ft.

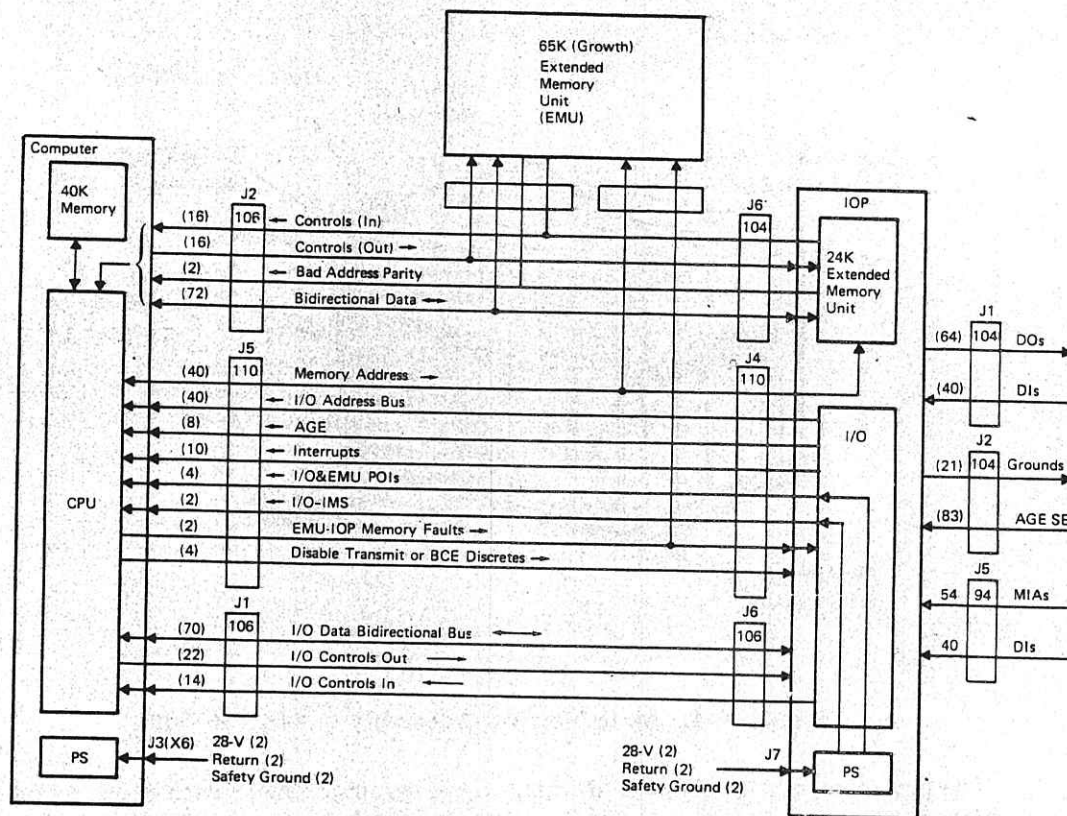


Figure 4-5. GPC Prototype Model Interface Configuration

The maximum drivable cable length is a function of the maximum I/O data transfer rate. The maximum cable length consistent with the 900,000 halfwords per second achievable is 33 ft. This distance may be lengthened if necessary by connecting a 130- $\Omega$  termination resistor, built into the receiver, from line-to-line.

A circular connector attached to the RFI filter and protruding through the front panel provides the external power interface to the IOP. Insulated wiring attached to threaded stud terminals interconnect the RFI filter output and power supply input.

Three connectors distribute regulated DC voltages on the power supply output. Two of these connectors mate with the wiring harnesses attached to the IOP backpanel; the third mates with a discrete wiring harness on the memory backpanel assembly for distribution of power to the main store.

Table 4-2

## CPU/IOP CONNECTOR PIN FUNCTIONS

CPU		IOP		Signal Description
Con- nector	Pin	Con- nector	Pin	
				(To be supplied)

4-9/4-10

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Section 5

IOP TEST EQUIPMENT

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## Section 5

### IOP TEST EQUIPMENT

The system configuration for IOP testing is shown in Figure 5-1. The computer interfacing with the IOP is an AP-101 previously tested for proper operation. The basic testing software and IOP tester control is within the AP-101, having been loaded by the computer tester. The AP-101 tester then provides 32-bit parallel data bus interface between the AP-101 and the IOP tester, as indicated in Figure 5-2. This interface provides access to the IOP input/output data through the MIA box portion of the IOP tester for the Function Test program (FTP) operating in the AP-101. The tester data bus traffic is two way, so that the AP-101 may control the IOP tester to feed back the appropriate data or to provide the IOP tester with data on IOP input simulations. The computer tester is also used with the AP-101 alone to perform the required tests to verify proper AP-101 operation.

The following test equipment is required to functionally test the IOP as follows:

- AP-101 computer
- AP-101 tester (MTS/AP-101)
- IOP tester (MTS-IOP)
- IOP MIA interface box
- Tape unit
- Printer.

#### 5.1 COMPUTER/COMPUTER TESTER

The computer tester is used to load the test program and control the computer during hardware and software testing. This equipment consists of a control and display unit, a magnetic tape transport, a line printer, and power and cooling units. The computer, under control of the computer test equipment, is tested using the FTP which iterates continuously in a sequence that verifies the proper operation of all portions of the computer. Computer tester characteristics are listed in Table 5-1.

The tester is microprogrammed and contains logic, switches, and displays for functionally testing the computer. It provides capability for memory load and verify,

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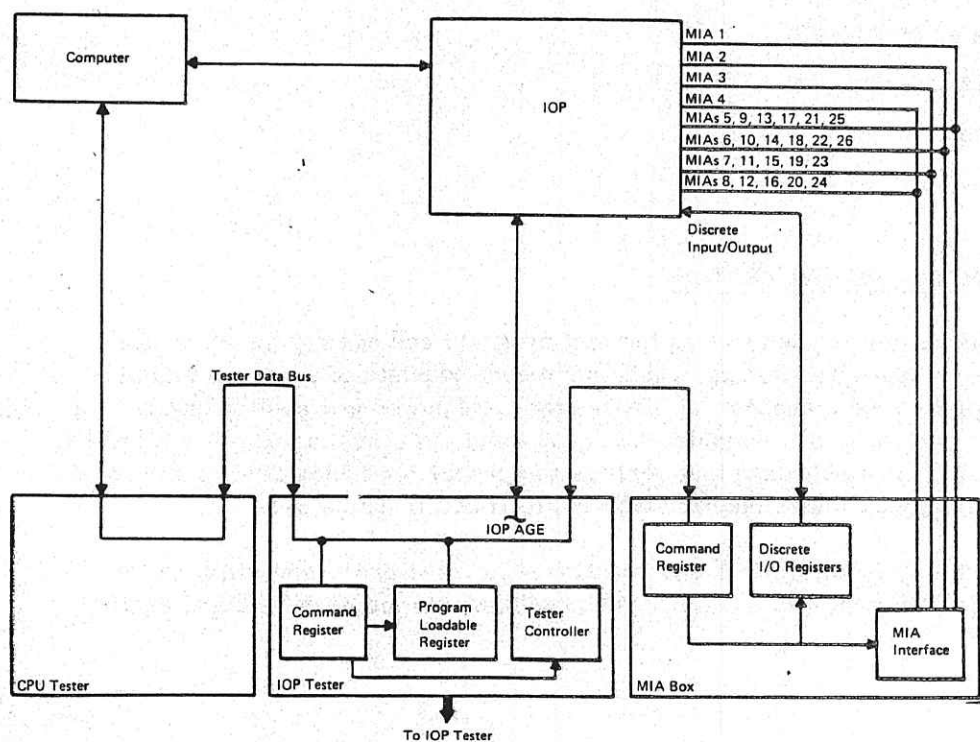
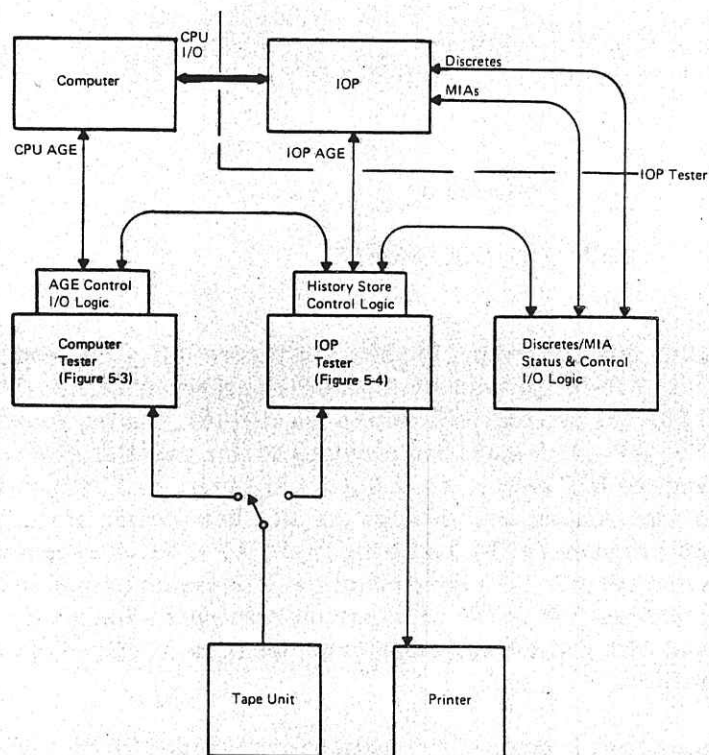




Table 5-1

# COMPUTER TESTER CHARACTERISTICS

## Supports

1. Loading and verification of software
2. General checkout and maintenance of the computer
3. Software checkout and verification
4. Functional testing of the computer and software

## Control Functions

1. Enter data into data and control registers
2. Start execution from operator preset address
3. Stop instruction at preset address
4. System reset
5. Memory load of single word
6. Halt execution
7. Single step execution
8. Single cycle execution
9. Address compare (instruction, operand, I/O, ROS)
10. History storage

ROS Address

Instruction Address

I/O Address

## Testing and Maintenance Functions

1. Clock sequence control (single cycle execution)
2. Display registers
3. Display fault status
4. Initiate memory read and write (manual main storage load and/or display)
5. Set mode control (scan code register set)
6. Initiate interrupts
7. Initiate self-test
8. Perform memory load and verify from test set magnetic tape
9. Hardware memory dump from operator preset addresses (block or total dump)
10. Stop on error (memory data compare or parity)
11. I/O test

## Control and Display Unit Characteristics

1. Dimensions — 17 × 20 × 26 inches
2. Weight — 100 lb

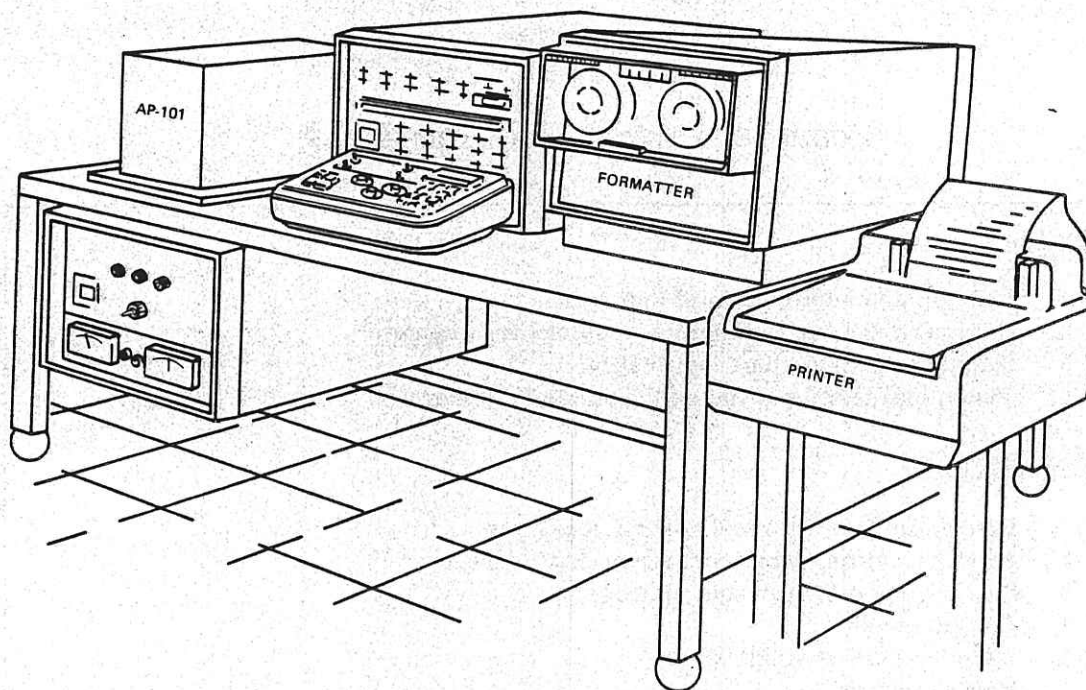


Figure 5-3. AP-101 Test Set

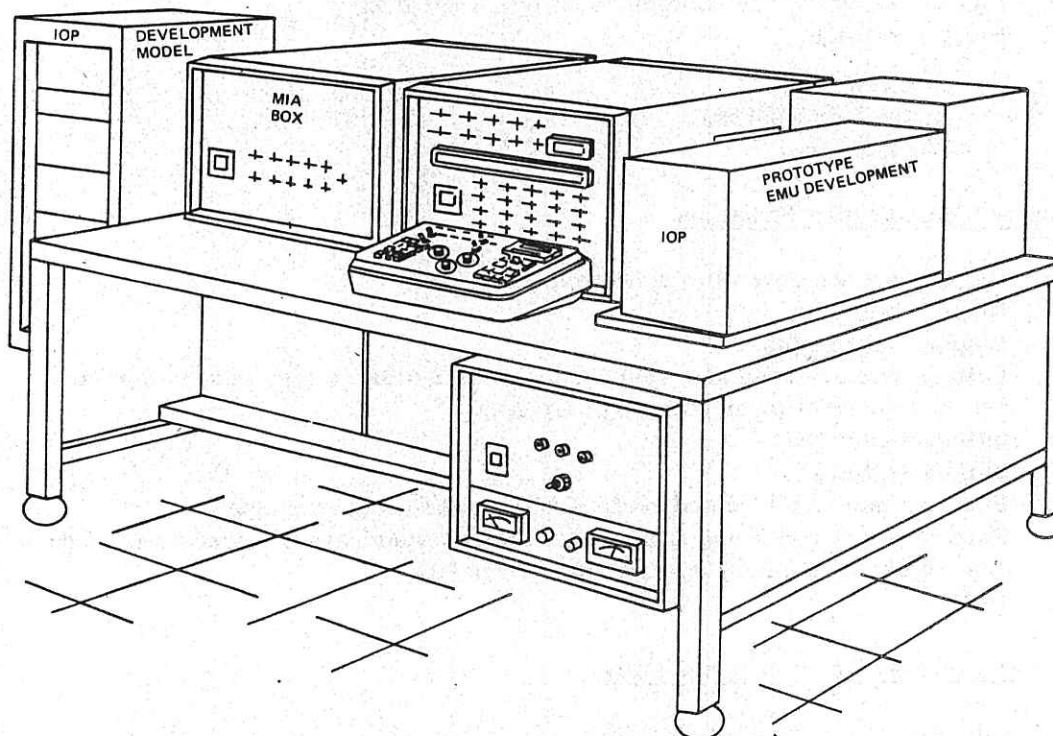


Figure 5-4. IOP Test Set



display of registers, manual insertion of data, single step, repeat, and other functions necessary for central processor checkout and operational and test program debugging. The test set is manually controlled, with free run, or dynamic operation, of some functions.

Displays are provided for data in comparators, registers, local storage, error, and status indicators of the computer. The computer is primarily controlled through AGE connector interface lines which are buffered as required. The system configuration also provides external I/O wrap-around. Wrap-around connects output to input lines and provides signal conditioning and buffering as required. In this mode, the computer passes signals out through the interface and back to itself for comparison. A block diagram of the computer tester is shown in Figure 5-5.

The following descriptive material separates the two tester panels into functional groups. The total layout of the two panels is shown in Figures 5-6 and 5-7.

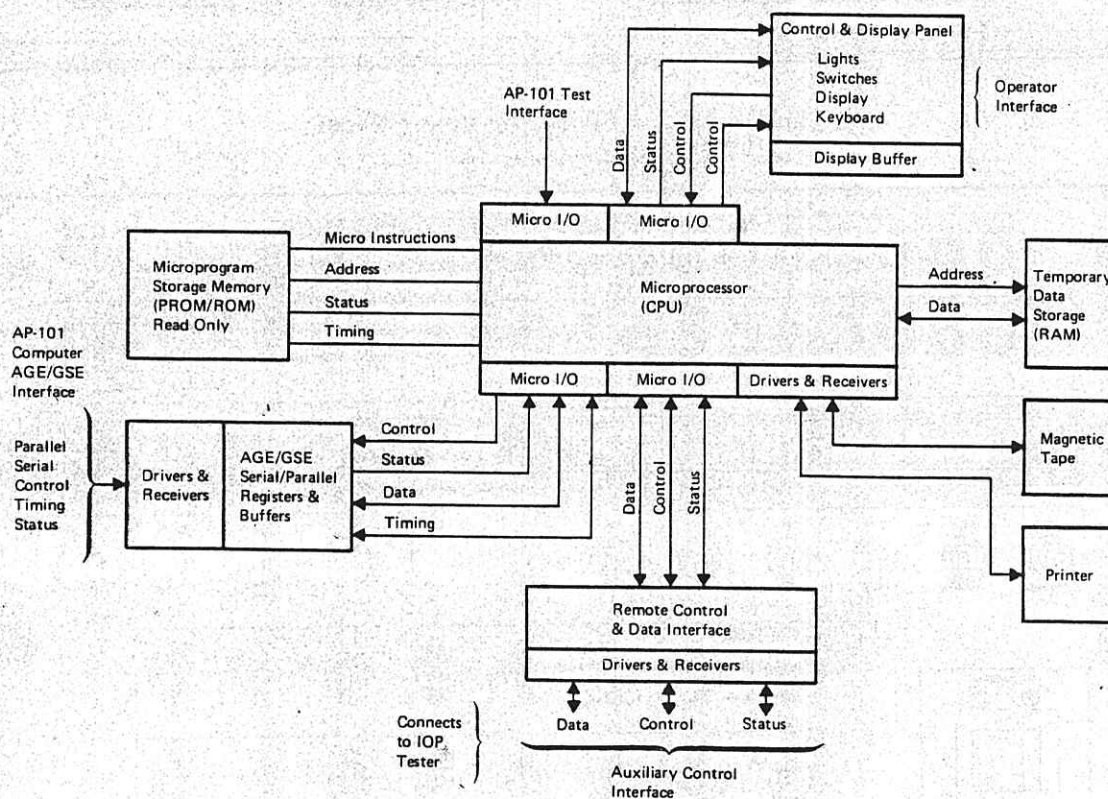


Figure 5-5. Computer Tester Block Diagram

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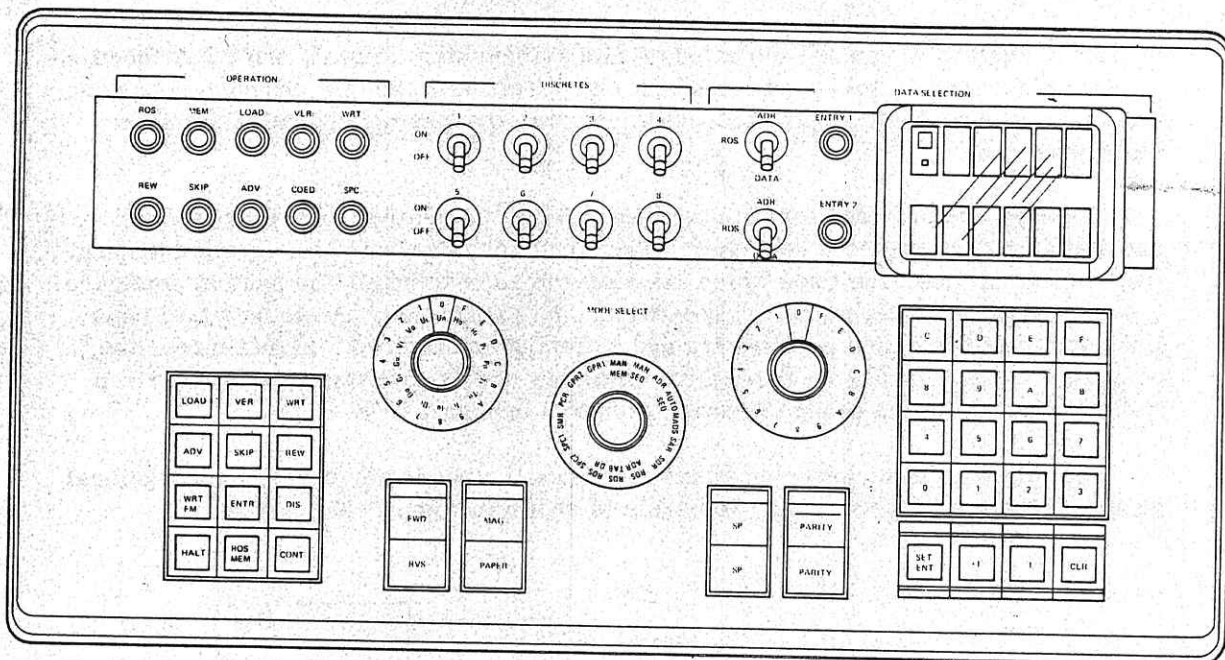


Figure 5-6. CPU Tester Lower Panel

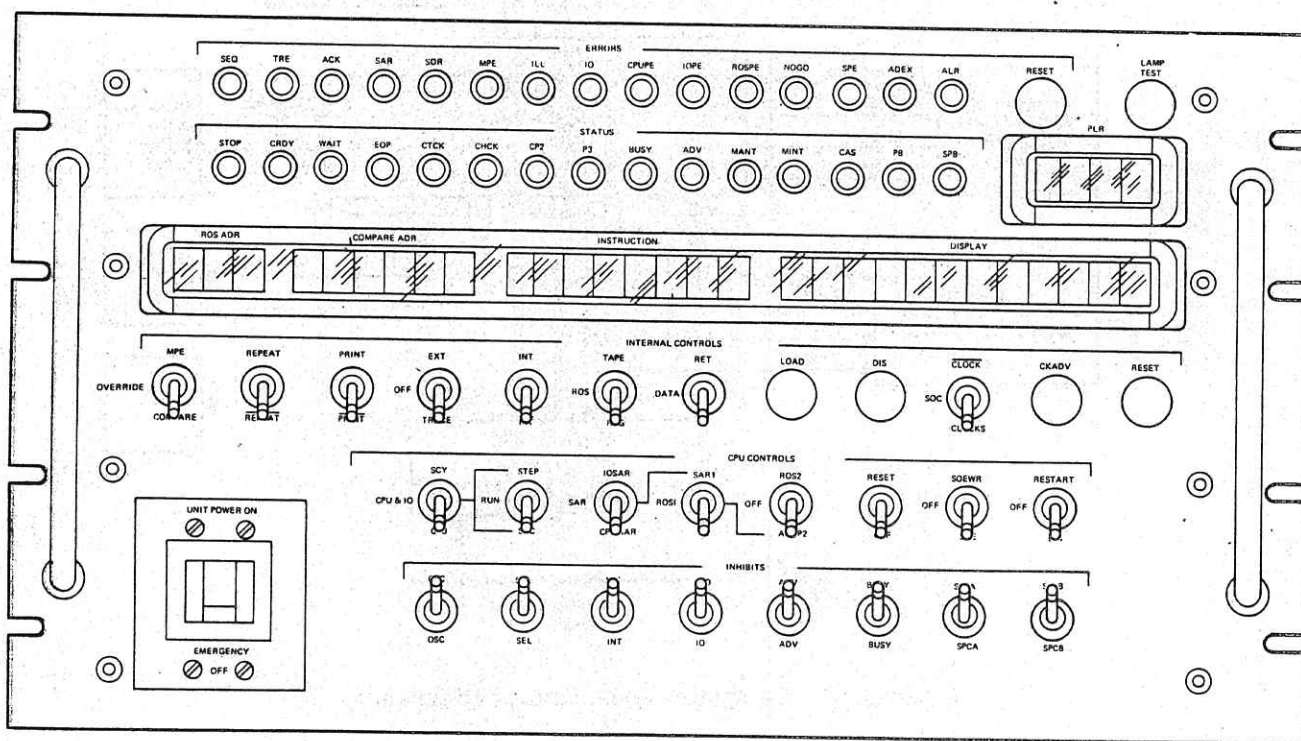


Figure 5-7. CPU Tester Upper Panel

### 5.1.1 PANEL LAYOUT

DATA SELECTION is the mechanism by which the operator selects the data to be entered into the CPU registers for display of CPU memory and CPU addresses for address compare. DATA SELECTION consists of two three-position toggle switches, two binary indicators, 12 hex indicators a 16-position keyboard, four pushbuttons, and two rocker switches (see Figure 5-6).

DATA SELECTION is divided into two entries denoted an ENTRY 1 and ENTRY 2. When the binary indicator ENTRY 1 is illuminated, ENTRY 1 is selected; when the binary indicator ENTRY 2 is illuminated, ENTRY 2 is selected. Operation of the SET ENT pushbutton changes the data entry selection. For example, if indicator ENTRY 1 is illuminated, operation of SET ENT switches from ENTRY 1 to ENTRY 2 (ENTRY 1 indicator is extinguished and ENTRY 2 indicator is illuminated). Operation of SET ENT does not alter the contents of ENTRY 1 or ENTRY 2.

Each data entry contains six hex digits to indicate the contents of each data entry. For AP-101, only five hex digits are required for each data entry so the left-most digit for each data entry is always blanked (no character is displayed). Associated with each set of hex indicators is a three-position toggle switch, whose positions are denoted as ADR, ROS, DATA, respectively. Each switch controls the blanking of its set of hex indicators. When in the DATA position, the left two digits are blanked; when in the ROS position, the left three digits are blanked; when in the ADR position the left-most digit is blanked.

The keyboard consists of 20 keys, each key representing a hex digit or function. Operation of a key causes the contents of the selected DATA ENTRY to be updated by entering the contents of the operated key into the right-most digit in the DATA ENTRY selected. All other hex digits are shifted left one. For example, suppose DATA ENTRY 1 is selected and DATA ENTRY 1 indicators indicate the hex number 5AC92. The operation of the B key will result in the updating of DATA ENTRY 1, with the result shown in DATA ENTRY 1 indicators as AC92B.

The operation of the +1 key adds plus one to the contents of DATA ENTRY 1. DATA ENTRY 1 is updated independent of the DATA ENTRY selected.

The operation of the -1 key subtracts one from the contents of DATA ENTRY 1. DATA ENTRY 1 is updated independent of the DATA ENTRY selected.

The Operation of the CLR key clears the selected DATA ENTRY. Clear is defined as all "0"s.

The two rocker switches denoted as SP/ $\overline{\text{SP}}$  and  $\overline{\text{PARITY}}$ /PARITY are used only for AP-101 manual memory operations. The SP/ $\overline{\text{SP}}$  switch in the  $\overline{\text{SP}}$  position indicates a Storage Protect bit equal to a "1" and in SP position indicates a Storage Protect bit equal to a "0".



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The PARITY/PARITY switch indicates the state of the parity bit to be stored in the the CPU memory. For any manual memory load operation, a parity bit is automatically generated and stored in the CPU memory. When the PARITY/PARITY switch is in the PARITY position, the proper value of the CPU parity bit is stored in the CPU memory, and when in the PARITY position the complement of the proper value is stored in the CPU memory. The switch allows the operator to store bad parity in memory.

#### 5.1.2 DISPLAY INDICATORS

There are four sections of display indicators: ROS address, COMPARE address, INSTRUCTION, and DISPLAY. The three ROS address indicators always display current ROS address. Compare indicators consist of six hex digits which indicate the memory address you compared. INSTRUCTION indicators are eight hex digits which indicate the current CPU instruction.

The 12 hex digits for display sections show the results of memory load, memory verify, and memory display operation.

#### 5.1.3 CPU CONTROLS

These paragraphs describe the controls shown in Figure 5-7.

- IA1/ROS1/SAR1 — This switch defines address compares. When in the IA1 position, we are comparing instruction addresses. When in the ROS1 position, we are comparing ROS addresses. When in the SAR1 position, we are comparing a memory address as defined by IOSAR/SAR/CPSAR. When that switch is in the IOSAR position, we are comparing only IO memory addresses.

When in the CPUSAR position, we are comparing only CPU memory addresses. When in the SAR, we are comparing all memory addresses. The addresses for all these operations are compared in DATA ENTRY 1.

- ROS2/OFF/ACMP2 — This switch is used with two others. When the switch is in the ACMP2 position, the contents of DATA ENTRY 1 or DATA ENTRY 2 are used as the compare address. When IA1/SAR1/ROS1 is in the IA1 position, and the ROS2/OFF/ACMP2 switch is in the ROS2 position, DATA ENTRY 1 is used as an instruction address compare, and DATA ENTRY 2 is used as a ROS compare.

When IA1/SAR1/ROS1 is in the ROS1 position, and ROS2/OFF/ACMP2 is in the ROS2 position, DATA ENTRY 1 or DATA ENTRY 2 are the compare addresses.

- STEP/RUN/SOC — When in the RUN position, the CPU can execute programs. When in the SOC position, the CPU is halted when an address compare occurs. When in the STEP position, the CPU is either single step or single cycle, as defined by the SCY/CPU & IO/CPU switch.



#### 5.1.4 MODE SELECT

The MODE SELECT consists of three rotary switches which define the operation to be performed when the display pushbuttons are activated (see Figure 5-6). Table 5-2 lists the switch functions.

Table 5-2

MODE SELECT SWITCH FUNCTIONS

Switch Position	Function
<u>First Switch</u>	
MM	Manual Memory
MSM	Manual Sequential Memory
ASME	Auto Sequential Memory Stop on No Compare
ASMC	Auto Sequential Memory Stop on Compare
MAP	Memory Address Pattern
SSA	Start/Stop Address
MHS	Memory History Storage
RHS	ROS History Storage
RAB	ROS Address Bus
LNDI	Low NDI Bus
MAB	Memory Address Bus
ALUL	ALU Left Bus
ROST	ROS Table
RDR	ROS Data Register
RP	Read PROMs
REG	CPU Register
<u>Second Switch</u>	
A	CPU A Register
B	CPU B Register
C	CPU C Register
D	CPU D Register

Table 5-2. Mode Select Switch Functions (cont)

Switch Position	Function
NROA	New ROS Address
GPR	CPU General Purpose Registers
FPR	CPU Floating Point Registers
ROSBP	CPU ROS Backup Register
NIR	CPU Next Instruction Register
S015	CPU STATS 0-15
OP	CPU OP Code Register
CTR0	CPU Counter 0
CTR1	CPU Counter 1
CTR2	CPU Counter 2
P	CPU P Register

The third rotary switch, which is hexadecimally encoded, is used when the rotary switch A is in the REG and when rotary switch C is either in the GPR or FPR position and is used to define which general-purpose register or which floating point register is to be loaded or displayed.

#### 5.1.5 OPERATION

This section consists of a 12-position keyboard and 10 indicators. The keyboard defines operations to be executed. The indicator designates which operation is being executed. The 12 positions of the keyboard are defined as follows (see Figure 5-6):

- ROS/MEM Switch — In conjunction with the tape reader, defines whether we are going to load or verify CPU main memory or verify CPU ROS memory. The indicators denoted as ROS and MEM indicate which memory is to be loaded or verified. The switch changes the status of the indicators.
- Load Key — Starts the loading process of the CPU memory/verify magnetic tape. The load indicator will be illuminated until the operation is completed. This switch can only be used for CPU main memory operations.
- VER Key — Initiates the verify process of either ROS memory or CPU main memory via the magnetic tape read. The VER indicator is illuminated as long as the verifying process is being completed.



- WRT Key — Initiates the recording of the CPU main memory or CPU ROS memory contents onto the magnetic tape. The WRT indicator will be illuminated until the process is completed.
- ADV — Is undefined.
- SKIP Key — Causes the tape to skip one record.
- REW Key — Causes the tape reader to rewind.
- WRM Key — Writes a file mark.
- ENTR Key — Initiates entry operations.
- DIS Key — Initiates display operations.
- CONT Key — Is used to start the computer if the CPU is halted.
- HALT Key — Is used to stop the computer if it is running.

#### 5.1.6 ERROR INDICATORS

The following error indicators are available:

- SAR — Indicates that the contents of the CPU storage address register does not agree with the address transmitted to it.
- SDR — Indicates that the contents of the CPU storage data register does not agree with the DATA switches or in case of a tape reader operation, the data read off the tape.
- MPE — Indicates a memory parity error has been detected.
- SEQ — Indicates the tape is out of sequence.
- TPE — Indicates a tape parity error has been detected.
- ACK — Indicates the last memory address does not agree with the check address read from the tape.
- ILL — Indicates the operator has done an illegal panel operation.
- ALR — Indicates action by the CPU.
- NOGO — Indicates the NOGO counter overflowed.
- CPUPE — Indicates a CPU memory parity error has been detected while the CPU is executing a program.
- IOPE — Indicates an I/O parity error has been detected.
- IO — Indicates the I/O option test logic has detected an I/O error.

#### 5.1.7 INHIBIT SWITCHES

Two inhibit switches denoted as  $\text{INT}/\overline{\text{INT}}$  and  $\text{OSC}/\overline{\text{OSC}}$  inhibit the CPU interrupts or the CPU oscillator. When the  $\text{INT}/\overline{\text{INT}}$  switch is in the  $\overline{\text{INT}}$  position, interrupts are



inhibited. The OSC/ $\overline{\text{OSC}}$  switch in the  $\overline{\text{OSC}}$  inhibits the oscillator. With this switch in the  $\overline{\text{OSC}}$  position, an external oscillator can be jumpered to the EXT OSC test point to simulate the CPU oscillator. Both switches are latched, and the state of the latches will only change when the CPU is halted. The normal states of the two switches are INT and OSC (see Figure 5-5). Other inhibit switches include the following:

- $\text{SEL}/\overline{\text{SEL}}$  — Inhibits CPU select signals in  $\overline{\text{SEL}}$  position.
- $\text{IO}/\overline{\text{IO}}$  — Inhibits all I/O in  $\overline{\text{IO}}$  position.
- $\text{ADV}/\overline{\text{ADV}}$  — Inhibits advance signal to computer in the  $\overline{\text{ADV}}$  position.
- $\text{BUSY}/\overline{\text{BUSY}}$  — Inhibits the busy signal to computer in the  $\overline{\text{BUSY}}$  position.
- $\text{SPCA}/\overline{\text{SPCA}}$  and  $\text{SPCB}/\overline{\text{SPCB}}$  — Are spare switches.

#### 5.1.8 STATUS INDICATORS

Status indicators are as follows (see Figure 5-7):

- STOP — Indicates the CPU clocks are halted.
- CRDY — Indicates the CPU is halted and the CCSE panel is ready for use. The CCSE panel operations are inhibited as long as this indicator is off.
- EOP — Indicates when the next CPU time level to be executed is I-FETCH. When the CPU is executing a program, the intensity of the indicator varies. When the CPU is halted at the end of an instruction, the indicator may or may not be lit. If it is illuminated when the CPU is started, the first CPU time level executed is I-FETCH. If it is not lit, it means an interrupt is pending.
- WAIT — Indicates the CPU is in the Wait state.
- CTCK — Is undefined.
- CHCK — Is undefined.
- CP2 — Is connected to the AP-101 CPU clock pulse 2. When the CPU is executing a program, this indicator is normally lit with a varying intensity. When the CPU is halted, this indicator must always be off. If it is not off, then the CPU clock generator is halted in the wrong state.
- P3 — Indicates the CPU memory priority latch is set. When the CPU is halted at the end of an instruction, the indicator must be off; otherwise, the CPU is hung under a memory cycle.
- BUSY — Indicates CPU Memory Busy when lit.
- ADV — Indicates CPU Advance signal (lit-"1" state)
- MANT and MINT — Are undefined.
- CAS — Indicates tester clocks stopped
- PB — Indicates CPU parity bit
- SPB — Indicates CPU Store Protect bit.

#### 5.1.9 DISCRETE INPUTS

The AP-101 reads the discrete input switches via the I/O interface by issuing a Direct-In instruction (DIN). For the AP-101 to read the discrete input switches, the AP-101/IO test option logic board must be in the MTS.

#### 5.2 IOP TESTER

The basic unit of the IOP tester is identical to the AP-101 tester, but the I/O portion of an AP-101 tester is modified to provide the following functions:

- AP-101 tester interface
- MIA box interface
- Tester-to-IOP interface (AGE).

The modifications are provided by logic board exchange in a basic MTS.

##### 5.2.1 AP-101 TESTER INTERFACE

The data bus concept used by this equipment is illustrated in Figure 5-2. The logic in the IOP tester provides the required decoding of command and data words on the data bus. It also permits two-way data transfers to the AP-101 AGE interface, which allows the AP-101 to configure the IOP input/output MIAs (in the MIA box) and the IOP tester as required to support the Functional Test program (FTP). The bus also provides the path to set an alarm lamp on the tester, inhibit/control history storage, and reset the tester.

##### 5.2.2 MIA BOX INTERFACE

This interface controls the four MIAs in the MIA box and the Discrete Input and Output registers. The DI/DO interface registers, also located in the MIA box, provide selection and data transfer capability.

The MIAs are connected as shown in Figure 5-2 to provide up to four-channel operations. Under AP-101 (FTP) control, the IOP MIAs may all be checked sequentially. Test points on the MIA box permit continuous monitoring of the MIA channels if required. The IOP tester block diagram of Figure 5-8 shows the interfaces.

##### 5.2.3 TESTER-TO-IOP INTERFACE

This interface provides the data required from the IOP to identify the function the IOP is performing. It also permits access to data internal to the IOP; i.e., data not available at the IOP interface. Figure 5-9 summarizes the interface lines.

The interface permits the operator to specify conditions within the IOP for tester comparison and test sequence control. A compare capability within the tester monitors the IOP/AGE data. When the data are available and compares, the IOP may be stopped (for single stepping), or the data may be routed to the tester display for operator evaluation.

The IOP/AGE interface circuitry also provides a 1K word  $\times$  80-bit history storage area for the IOP data that is to be printed out on the system printer.



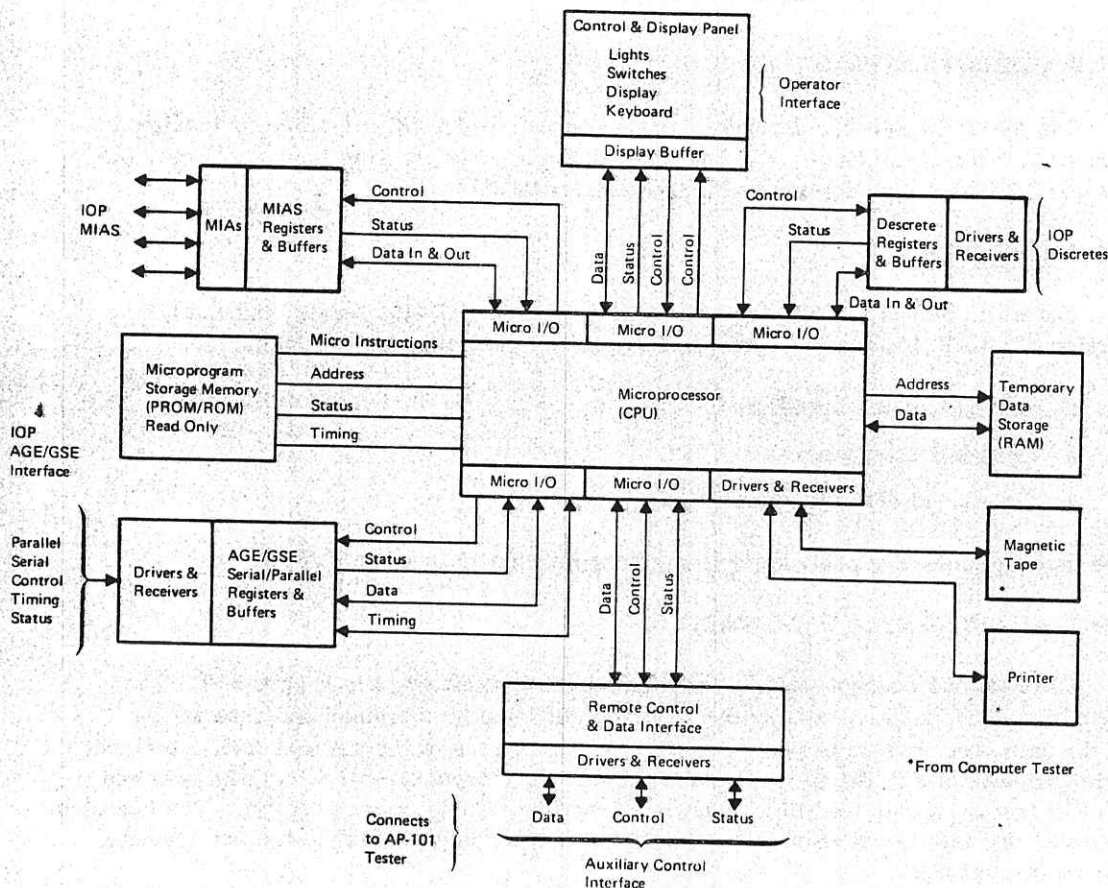
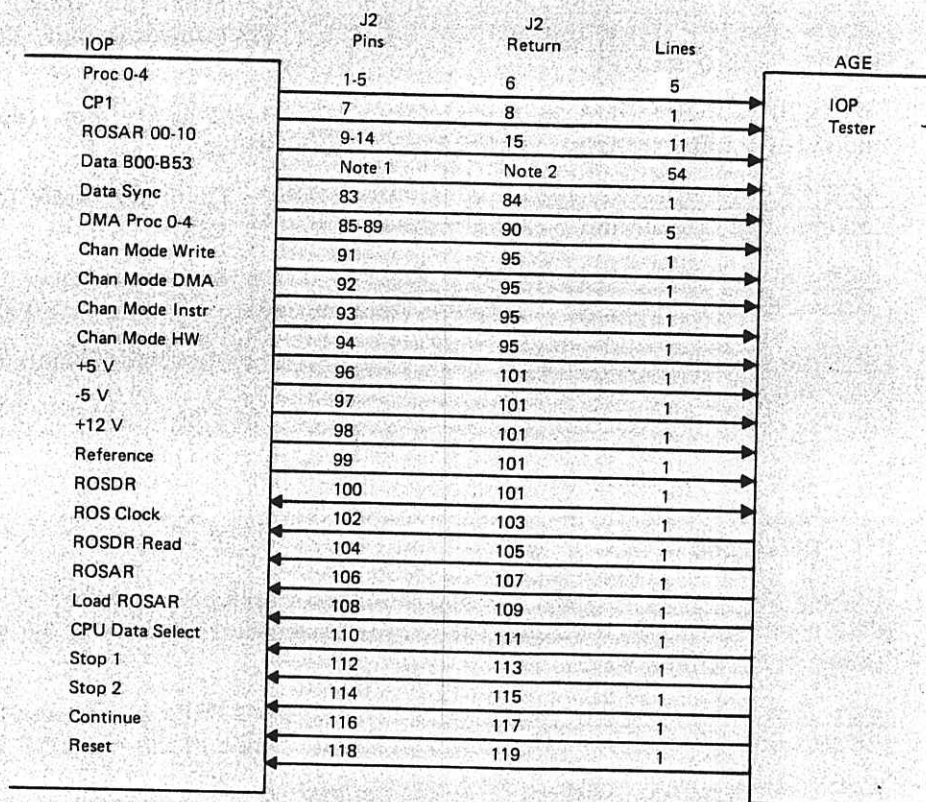


Figure 5-8. IOP Tester Block Diagram

The following defines the IOP/AGE interface; all signals are single-ended:

- AGE PROC 0-4 (5 Lines) IOP → AGE — The output of slot counter, when decoded, describes the identity of the element (BCE, MSC, T) currently in process. The highest order bit (MSB) is AGE PROC 0. The lowest order bit (LSB) is AGE PROC 4. Sense of the signal is negative.
- AGE CP1 (1 Line) IOP → AGE — This is clock CP1 of IOP timing ring. Sense of the signal is negative.
- AGE ROSAR 00-10 (11 Lines) IOP → AGE — This is output of ROS Address Register. Sense of the signal is negative.
- AGE DATA B00-B53 (54 Lines) IOP → AGE — AGE DATA bits 00-53 will represent either DMA data or internal registers R4, R5, and R6 data. Selection of data is dependent upon AGE CPU DATA SEL signal. Data format is shown in Table 5-3.
- AGE DATA SYNC (1 Line) IOP → AGE — This signal gates AGE DATA B00-53 to interface after data has settled down. Sense of the signal is negative.
- AGE DMA PROC 0-4 (5 Lines) IOP → AGE — These signals identify the processor associated with data transfer on "AGE DATA B00-53" bus. They have meaning only when IOP is in a DMA mode. Sense of signal is negative.





Notes:

- 22-29, 31-38, 40-47, 49-56, 58-65, 67-74, 76-81
- 30, 39, 48, 57, 66, 75, 82

Figure 5-9. IOP/AGE Interface

Table 5-3

DATA FORMAT FOR AGE DATA B00-53 (54 Lines) IOP-AGE

AGE Data	DMA Mode	Internal Regs
B00	Address Bit 0	R4 Bit 0
B17	Address Bit 17	R4 Bit 17
B18	Address Bit Parity	R5 Bit 0
B19	Data Bit 0	
B35		R5 Bit 17
B36		R6 Bit 0
B50	Data Bit 31	
B51	High Halfword Parity	
B52	Low Halfword Parity	
B53	Storage Protect (Fullword Only)	R6 Bit 17

- AGE CHAN MODE WRITE (+ READ) IOP → AGE — When this signal is active (down), the IOP is writing data into the CPU. When inactive (up), the IOP is reading data from CPU.
- AGE CHAN MODE DMA (+ PCIO) IOP → AGE — The active state (down level) indicates a DMA transfer. Otherwise, it is a PCIO.
- AGE CHAN MODE INSTR (+ DATA) IOP → AGE — The active state (down level) indicates an instruction transfer. Otherwise it is data.
- AGE CHAN MODE HW (+ FW) IOP → AGE — The active state (down level) indicates a halfword transfer. Inactive state (up level) is a fullword transfer.
- POWER STATUS IOP → AGE — The four power status lines consists of the following:
  - +5 V
  - 5 V
  - +12 V
  - Reference

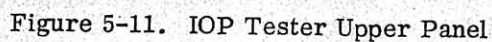
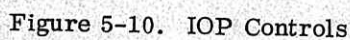
- ROSDR IOP ↔ AGE — This is a bidirectional interface consisting of serial data read from or written into the ROS Data register. Sense of the signal is negative, either way.
- AGE ROS CLOCK AGE → IOP — This signal is a 1-MHz clock used to gate ROSDR or ROSAR across the AGE interface. Sense of the signal is negative.
- AGE ROSDR READ AGE → IOP — This signal controls direction of ROSDR data. The active state (down level) gates serial data from the ROSDR. The inactive state gates data to the ROSDR.
- ROSAR AGE → IOP — This signal represents serialized data into the ROS Address register. Sense of the signal is negative.
- AGE LOAD ROSAR AGE → IOP — This line gates ROSAR. Sense of the signal is negative (load with AGE ROS clock). When positive, it gates ROSDR.
- AGE CPU DATA SEL (+ R4, R5, R6) AGE → IOP — The active state (down level) of this signal gates the CPU channel data. The inactive state (up level) gates internal IOP registers R4, R5, and R6.
- STOP 1 AGE → IOP — This stops timing ring after completion of CP6 time. It places IOP into the Halt state at that time. Sense of signal is negative.
  - (Stop 1) • (Continue) = 1 slot time = 375 ns
- STOP 2 AGE → IOP — This inhibits IOP clock oscillator. Sense of the signal is negative.
  - (Stop 2) • (Continue) = 1 clock pulse  
(CP1 or CP2 or CP3, etc.)
- CONTINUE AGE → IOP — This restarts timing ring. Sense of the signal is negative.
- RESET AGE → IOP — Resets the IOP logic.

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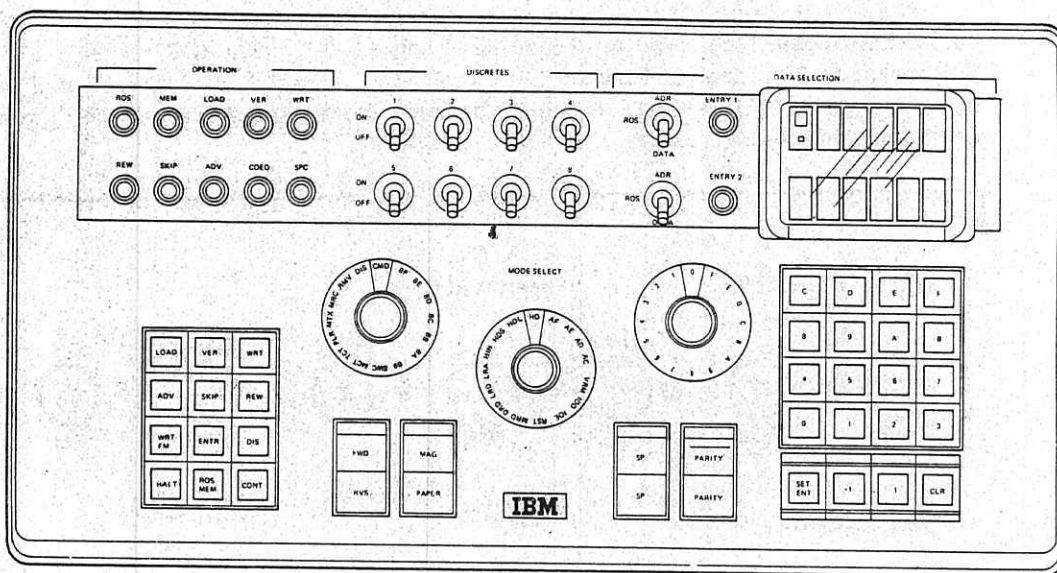


Figure 5-12. IOP Tester Lower Panel

#### 5.2.4.1 Upper Panel Controls

The IOP Tester Upper Control Panel is shown on Figure 5-11.

#### 5.2.4.1.1 Internal Controls

- MPE/Override/Compare — Not Used.
- REPEAT/REPEAT — Used to REPEAT ENTER mode microprogram instruction as stated in the operating procedure.
- PRINT/PRINT — Enables printer for hard copy of data during display functions.
- EXT/OFF/TRACE — Place in "OFF" position (not used for operational programs)
- INT/INT — Controls display and tape transport for internal tester operations. INT is normal operating position.
- TAPE/ROS/REG — Place in "TAPE" for magnetic tape operations. Normal position is "ROS". The "REG" position is used for internal microprogram control only.
- RET/DATA/ADR — Used for internal microprogram control only.

- CLOCK/SOC/CLOCKS — "CLOCKS" is the normal operating position. "CLOCK" is used for internal operations — Tape Load or Write as stated in the operating procedure. Tester clocks are stopped in this position. "SOC" — Internal Stop on Compare for microprogram control.
- LOAD (Pushbutton) — Not used for normal operating conditions, for internal microprogram control only.
- DIS (Pushbutton) —
- CKADV (Pushbutton) —
- RESET — Provides Reset-to-Tester logic.

#### 5.2.4.1.2 Internal Controls — Other

- ERROR RESET (Pushbutton) — Resets Error Register
- LAMP TEST (Pushbutton) — Lights all indicators except SPC, P3, BUSY, EOP, MINT and all Hex LED displays.

#### 5.2.4.1.3 IOP Controls

The IOP tester main panel and controls are identical to those on the AP-101 tester but with different labels and microcoding. The IOP controls area of the IOP tester is identified in Figure 5-8. Many of the control panel functions are not used for IOP testing. Some of the lamp identifiers and all of the displayed data are unique to the IOP tester.

- Switch (A)
  - SCY — This position forces the IOP to single-step operation, with the unit of stepping being one MSC/BCE slot time.
  - CLK — This position permits single-stepping at one of six IOP clock times.
  - IOP — The stepping cycle in this position is identified by switch D.
- Switch (B) — When in the RUN position, the IOP is allowed to execute programs. When in the SOC position, the IOP is halted when an address compare occurs. When in the STEP position, the IOP uses either single step or single cycle, as defined by switch A.
- Switch (C) — This switch identifies the source of data for stop-on-compare operations or data display operations. The data depend on SWITCH G settings and therefore IOP/AGE output data. AD, PN, and MODE imply channel mode of operation. The data are used with switches D and E as a set.



- Switch (D) — This switch defines address compares. When in the PSN position, we are comparing processor slot numbers. When in the ROS1 position, we are comparing ROS addresses. When in the CH/REG position, we are comparing an address as defined by AD/R4 - Pn/R5 - MODE/R6. When switch C is in the AD/R4 position, we are comparing on memory addresses or register 4 data.

When switch C is in the MODE/R6 position, we are comparing mode identifiers or register 6 data. When switch C is in the PN/R5 position, we are comparing channel processor number or register 5 data. The compare addresses for all these operations are compared in data entry 1.

- Switch (E) — This switch is used in conjunction with switches C and D. When the switch is in the ACMP2 position, the contents of data entry 1 or data entry 2 are used as the compare address. When switch D is in the PSN position and switch E is in the ROS2 position, data entry 1 is used as a PSN compare and data entry 2 is used as a ROS compare.
- Switch (G) — This switch provides the DATA SEL signal to the IOP to force one of the two data sets and reconfigure the IOP tester logic to support data reduction of the new format. CH indicates Channel mode while REG indicates the IOP Internal Register mode for R4, R5, and R6. IHS position inhibits History Storage while maintaining channel mode data operation.

#### 5.2.4.1.4 Inhibit Switches

The Inhibit switches are not used for IOP testing. Place all in the down position.

#### 5.2.4.1.5 Error Indicators

- SEQ — Tape sequence error
  - Tape drive malfunction
  - Tape formatter malfunction
  - Tape improperly positioned for FWD/REV operation
- TPE — Tape parity error
  - Tape has detected a parity error
- ACK — N/A
- SAR — ROSAR error
  - Read back of ROSAR does not match verify ADR from tape
- SDR — ROSDR error
  - ROSDR contents do not match data from tape
- MPE — N/A
- ILL — Operator error
- ALR — The FTP lights this indicator to notify the operator that it has detected an error.

All other error indicators are not used.



#### 5.2.4.1.6 Status Indicators

- STOP — The IOP is in a HALT state.
- CRDY — The IOP is halted and the control panel is ready for manual intervention.
- WAIT — When "ON" the MTS microprogram is waiting for an entry on the operation keyboard.

When "OFF" the program is busy and will not accept inputs.

When the IOP is operating — "STOP" is "OFF" only a "HALT" will be acceptable by the microprogram.

- CP2 — Will be lit with varying intensity when the CPU is running. It will be off when the CPU is halted.
- CAS — Will be lit when the tester internal clocks are stopped.

All other status indicators are not used.

#### 5.2.4.2 Lower Panel Controls

The IOP Tester Lower Control Panel is shown on Figure 5-12.

##### 5.2.4.2.1 Panel Layout (Lower)

DATA SELECTION is the mechanism by which the operator selects the data to be entered into the IOP Tester registers for display or modification of IOP Memory Registers and addresses for mode as well as address compare functions. DATA SELECTION consists of two three-position toggle switches, two binary indicators, 12 hex indicators, a 16-position keyboard, four pushbuttons, and two rocker switches.

DATA SELECTION is divided into two entries denoted an ENTRY 1 and ENTRY 2. When the binary indicator ENTRY 1 is illuminated, ENTRY 1 is selected; when the binary indicator ENTRY 2 is illuminated, ENTRY 2 is selected. Operation of the SET ENT pushbutton changes the data entry selection. For example, if indicator ENTRY 1 is illuminated, operation of SET ENT switches from ENTRY 1 to ENTRY 2 (ENTRY 1 indicator is extinguished and ENTRY 2 indicator is illuminated). Operation of SET ENT does not alter the contents of ENTRY 1 or ENTRY 2.

Each data entry contains six hex digits to indicate the contents of each data entry. Associated with each set of hex indicators is a three-position toggle switch, whose positions are denoted as ADR, ROS, DATA, respectively. Each switch controls the blanking of its set of hex indicators. When in the DATA position, the left two digits are blanked; when in the ROS position, the left three digits are blanked; when in the ADR position the left-most digit is blanked. Place the switch in the DATA position for all IOP operations.

The keyboard consists of 20 keys, each key representing a hex digit or function. Operation of a key causes the contents of the selected DATA ENTRY to be updated by entering the contents of the operated key into the right-most digit in the DATA ENTRY selected. All other hex digits are shifted left one. For example, suppose DATA ENTRY 1 is selected and DATA ENTRY 1 indicators indicate the hex number 5AC92. The operation of the B key will result in the updating of DATA ENTRY 1, with the result shown in DATA ENTRY 1 indicators as AC92B.

The operation of the +1 key adds plus one to the contents of DATA ENTRY 1. DATA ENTRY 1 is updated independent of the DATA ENTRY selected.

The operation of the -1 key subtracts one from the contents of DATA ENTRY 1. DATA ENTRY 1 is updated independent of the DATA ENTRY selected.

The Operation of the CLR key clears the selected DATA ENTRY. Clear is defined as all "0"s.

The two rocker switches denoted as SP/ $\overline{SP}$  and  $\overline{PARITY}$ /PARITY are not used.

- IOP Tester Discretes — The eight discrete switches will provide the only operator-controlled inputs to the FTP operating in the AP-101. They permit reconfiguration of the FTP (preplanned sequence) to support operator-desired test configurations. Data are transferred via the tester data bus through AP-101 AGE interface (not IOP interface).

#### 5.2.4.2.2 Operation Keyboard

This section consists of a 12-position keyboard and 10 indicators. The keyboard defines operations to be executed. The indicator designates which operation is being executed. The 12 positions of the keyboard are defined as follows:

- ROS/MEM Switch — In conjunction with the tape reader. The indicators denoted as ROS and MEM indicate which memory is to be loaded or verified. The switch changes the status of the indicators. Place in ROS condition for all IOP operations.
- Load Key — Starts the loading process of the magnetic tape. The load indicator will be illuminated until the operation is completed.
- VER Key — Initiates the verify process of either ROS memory or tester memory via the magnetic tape read. The VER indicator is illuminated as long as the verifying process is being completed.
- WRT Key — Initiates the recording of the tester memory or IOP ROS memory contents onto the magnetic tape. The WRT indicator will be illuminated until the process is completed.
- ADV — Advances the IOP one cycle if IOP is halted



- SKIP Key — Causes the tape to skip one record
- REW Key — Causes the tape reader to rewind
- WRM Key — Writes a file mark
- ENTR Key — Initiates entry operations
- DIS Key — Initiates display operations
- CONT Key — Used to start the IOP if the IOP is halted
- HALT Key — Used to stop the IOP if it is running.

#### 5.2.4.2.3 Tape Control Rocker Switches

- FWD/RVS — Leave in "FWD" position
- MAG/PAPER — Leave in "MAG" position.

The Mode Rotary Switches A, B, and C shown in Figure 5-12 are used to configure the various operating and testing modes of the tester and is defined as follows.

#### Switch A

<u>Position</u>	<u>Function</u>
HD	History Dump [continue to 3FF (1024 addresses) or <u>PRINT</u> ]
HDL	History Disp/Dump Last Entry
HDS	History Disp/Dump Sequential
HIN	History Input DISP/DUMP (AGE Signals to History)
LRA	Load ROS Address Register
LRD	Load ROS Data Register
DRD	Display ROS Data Register
MRD	Modify ROS Data Register
RST	IOP Reset
IOE	Entry Registers Selector by Switch B
IOD	Display Registers Selected by Switch B
VRM	Verify IOP ROS Memory
AC	DRAM (Internal RAM Display-Program Debug Aid) (not used for test)
AD	Not Assigned
AE	Not Assigned
AF	Not Assigned



## Switch B

<u>Position</u>	<u>Function</u>
CMD	Command Register I/O Box
DIS	*Discrete In/Out Selected by Switches C — 1, 2, 3, A, B
RMV	Redundancy Management Vote Discretes
MRC	*MIA Receive Register Data Selected by Switches C — 1, 2, 3, 4
MTX	*MIA Transmit Register Data Selected by Switches C — 1, 2, 3, 4
PLR	Program Loadable Register Display (AGE 101 Program)
TCT	Tester Control Register (AGE 102 Program)
MCT	MIA Control Register
SWC	Not Assigned
B9	Not Assigned
BA	Not Assigned
BB	Not Assigned
BC	Not Assigned
BD	Not Assigned
BE	Not Assigned
BF	Not Assigned

## Switch C — HEX 0 → F

\*Used with positions noted on Switch B

### 5.2.4.2.3 Test Points

Located on the left side of the lower panel of the MTS/IOP Tester and the following test points:

- IOP Power Monitor
  - +5 V
  - 5 V
  - +12 V
  - Common Voltage Reference
- R SYNC — A sync pulse is provided each time the IOP ROS address reaches a compare as defined by the IOP compare controls.
- M SYNC — A sync pulse is provided each time the main comparator sees a compare on any function other than ROS Address.
- I SYNC — Provides a sync pulse at selected addresses in the microprogram of the MTS. Used to troubleshoot tester problems.

#### 5.2.4.3 Magnetic Tape Transport

The magnetic tape transport is used with the IOP test configuration to load and verify the AP-101 memory via the Computer Tester. When attached to the IOP Tester it is used to verify IOP ROS memory and the tester microprogram.

The magnetic tape transport is IBM System/360 compatible. The tape unit formatter can convert between IBM System/360 nine-track format and computer information. The tape unit uses a 7-inch reel (600 ft) of 0.5-inch tape, recording nine-track data at 800 bits/in density at 12.5 in/s, and has a rewind time of 1 minute.

#### 5.2.4.4 Line Printer

The line printer is used to obtain a hard copy of History Storage, the AGE Interface signals, and the IOP ROS Data Register.

Printer characteristics:

- Printing rate
  - 100 characters/s
  - 60 full lines/min (80 characters)
  - 150 short lines/min
- Character structure
  - 5 × 7 dot matrix
  - 10-point equivalent
- Input language
  - USACH — 64 characters
- Character buffer
  - 80 characters
- Printing structure
  - 80 characters/line
  - 6 lines/in.