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PROGRESS REPORT
ON ATTAINABLE RELIABILITY
OF INTEGRATED CIRCUITS FOR
SYSTEMS APPLICATION
by
Jayne Partridge, L. David Hanley,
Eldon C. Hall
November 1964



**INSTRUMENTATION
LABORATORY**

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PROGRESS REPORT ON ATTAINABLE RELIABILITY
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ABSTRACT

An approach to reliable systems design through standardization is given. The approach which allows systems to use predominantly the same simple integrated circuit also allows the development and maintainability of the high reliability of integrated circuits. The approach will be justified by the presentation of integrated circuit failure modes detected to date. The integrated circuit failure modes will indicate present reliability problems, the need for detection, monitoring, and elimination of the problems, and the necessity of reliability evaluation among suppliers. The success of the approach will be demonstrated by extended use failure rate data made available through the Apollo program.

By
Jayne Partridge
L. David Hanley
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PROGRESS REPORT ON ATTAINABLE RELIABILITY OF INTEGRATED CIRCUITS FOR SYSTEMS APPLICATION

I INTRODUCTION

In the design of any system, the end goal must be considered in the associated constraints. For military and space application, high reliability is an extremely important goal which is often overlooked during the initial design of the system. The selection of components, producibility, circuit packaging and thermal design must all be included in the initial design of a reliable system. In addition, proving the high reliability prior to field use has become a major problem. By proven reliability we mean actual demonstration of reliability. To prove the high reliability objectives of space and military applications, many tens of millions of element operating hours with no operating failures are required. If large samples are not available, the accumulated time required to prove high reliability exceeds the time after which the system parts or processing of parts become obsolete. There have been methods proposed and used to circumvent these problems. They are

A Use of Mathematical Models for Reliability Prediction

Mathematical models have been developed by fitting a failure frequency distribution to past failure experience and so determine future failure rates as a function of time. Examples of fitted failure frequency distributions are the exponential function, gaussian and Weibull distributions. If the failure frequency distribution is assumed for a new system without prior knowledge of how parts assembly of parts and therefore systems fail and under what conditions they fail, the technique is highly questionable. If one considers the multitude of time and stress dependencies of various failure modes occurring in various parts or assembly of parts and the fact that these failure modes must be weighted in order of frequency of occurrence, a general mathematical model does not appear promising. Should a potentially applicable mathematical model be developed, the

applicability of the model must be still demonstrated by extended life tests.

B. Step Stressing

This is also a prediction technique, but unlike the mathematical model approach, step stressing attempts to incorporate rapidly accumulated data generated by small samples. This technique has been employed to accelerate failure modes and then extrapolate the results to normal stresses. Although accelerated stressing can be useful, the prediction of normal failure rates can be erroneous and has been so demonstrated.¹ In any event, both the failure rates and failure modes generated during step stressing must be correlated with normal use life tests. Therefore extended life tests must still be performed.

C. Redundancy Techniques

Von Neumann² introduced the concept of synthesizing reliable systems from unreliable components. This technique depends upon the use of failure analysis since knowledge of the dominance of open and short circuits and the dominance of input or output failures is required. Also, knowledge of failure "randomness" and failure correlation is necessary. If the designer of a system is working with parts where all the failure modes have been detected, and the variation of failure modes and frequency of failure modes among suppliers and among the different lots of a supplier are predictable, then redundancy techniques can be successful. However, redundancy techniques sacrifice weight, power, size, and increase the complexity of the system.

Too often the designer of the redundant system is working with new components and new assembly techniques. Generally when new components and new assembly techniques are introduced all the failure modes and their variations with time are not known. In this case a large gamble is being taken

since the chance is extremely probable that failure modes will appear which make erroneous the basic assumptions on which the redundancy is based.

D. Reliability through Standardization

An approach which will help assure end reliability is the design of the system with minimization of the number of different components. This approach has several advantages. First, an aspect of reliability which is often overlooked is the fabrication of parts into a system. Standardization minimizes the number of different components which **greatly simplifies** the process control for production lines. For example, the use of one packaged integrated circuit with no components external to it allows for ease of fabrication and handling which in turn decreases errors and damage during fabrication. Second, no assumptions as to how parts fail have to be made, since proven reliability can be developed and maintained if a **large volume of a relatively simple** device can be produced. The development of a reliable device must be stressed. Even if at the start of a program a device is not sufficiently reliable or its reliability has not been demonstrated, large volumes allow both reliability improvement and demonstration.

II. RELIABILITY THROUGH STANDARDIZATION

Military and space objectives require the very latest in technological development coupled with reliability goals that require successful operation for several years. A compromise must often be made between the use of new technology and high reliability objectives. With judicious planning this compromise can be instituted effectively. For example, integrated circuits using planar technology have made new objectives possible by reducing the size and weight of a system while introducing an important future reliability gain. Because of very similar processing, the development of the inherent planar integrated circuit reliability to the levels of the already proven high reliability of planar transistors appeared inevitable*. This exciting concept meant that one planar integrated circuit, with a combination of active and passive components, using a potentially carefully controlled interconnect process, packaged in a hermetically sealed enclosure, could achieve the failure rates of a single planar transistor. Therefore, the integrated circuit could exceed the reliability of a circuit consisting of several transistors with associated diodes or resistors plus all the external interconnects.

Once the component part has been selected, reliability can be developed by determining techniques to detect all possible failures by studying the failure modes of the part, and by determining contributing factors to failures thus correcting faults originating in the production of the part. Reliability can be maintained by determining vendor qualification lists which allow parts to be purchased from a selected group of vendors with proven history of quality and reliability. Reliability is further maintained by developing lot rejection criteria following predetermined testing procedures for known failure modes such that the entire lot can be returned to the vendor when a certain percentage of failures is detected. Lot rejection by failure modes

and percentages of failures institutes a continuous monitoring procedure. Since reliability is built into a device, testing and screening cannot create a more reliable device, but testing and screening can eliminate a poor device or suspected troublesome lots of devices. Reliability depends on vendor control over proven processes with rapid feedback to the vendor when new failure modes are detected.

Purchasing of large volumes of a part aids in the development and maintenance of high reliability. Purchasing of large quantities results in lower prices which allow funds to be allocated into evaluation, testing and monitoring. Large volumes allow a continuous production flow where manufacturing control is facilitated. Large samples become available for rapid extended life testing and provide extensive vendor history.

The standardization approach, which is particularly adaptable to computers, has been demonstrated with the Polaris flight computer and extended with integrated circuits to the Apollo Guidance Computer. Both computers were designed to use a three input Nor gate as the only logic element. All logic functions are generated by interconnecting the three input Nor gate with no additional logic blocks, resistors, or capacitors. At first glance, it appears that using only one type of logic block greatly increases the number of blocks required for the computer. But by judiciously selecting and organizing the logic functions it is quickly apparent that few additional blocks are necessary. The few additional units required are greatly counter balanced by the increased reliability gain during both the manufacturing of components and fabrication of the components into modules.

The integrated circuit for which all of the following data is to be presented is the three input Nor gate as shown in Fig. 1. This circuit is used at 3V and 15 mw, but is rated at 8V and 100 mw. Unpowered temperature rating is 150°C. The basic simplicity of the three input gate aids an effective screening process. All trans-

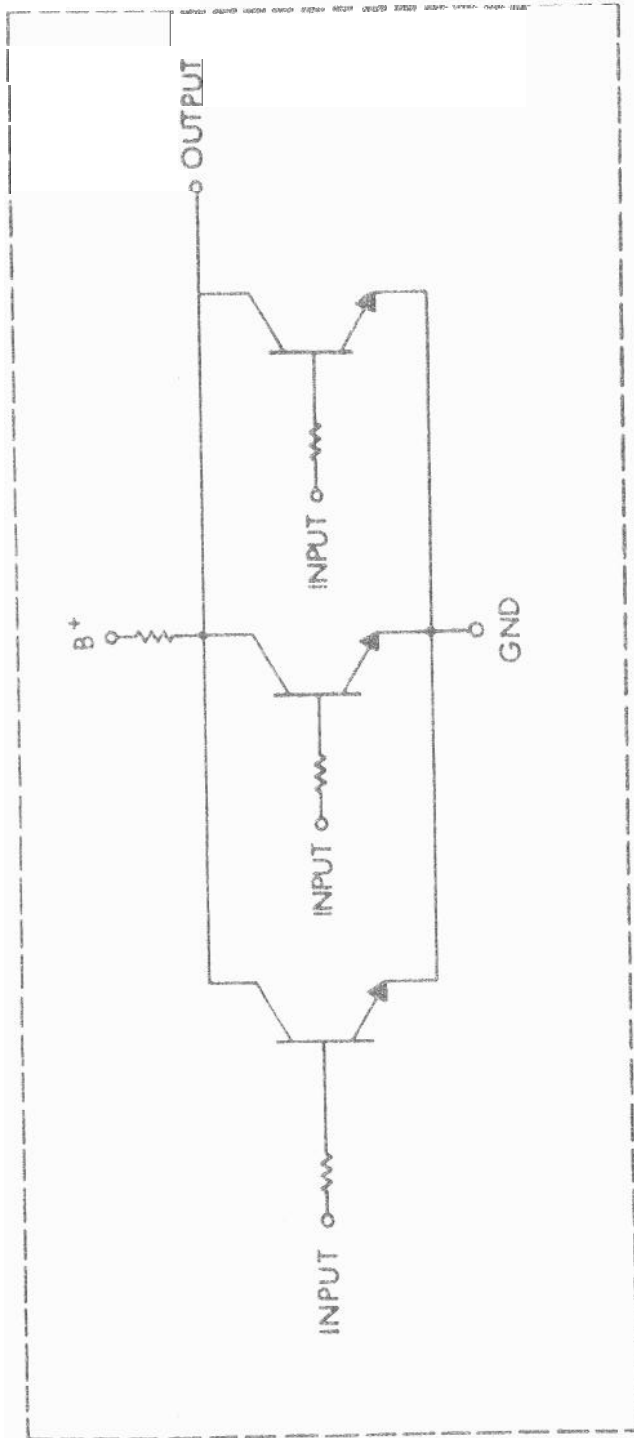


Fig Schematic drawing of the three input Nor gate

sistors and resistors can be tested to insure product uniformity. The simplicity of the circuit also aids in the quick detection and diagnosing of insidious failures without extensive probing as required with more complicated circuits.

III. INTEGRATED CIRCUIT FAILURE MODES

Since the standardization approach depends on failure detection and failure elimination or minimizing of failures, knowledge of integrated circuit failure modes is required. The following is a summary of integrated circuit failure modes detected to date. The devices of any given vendor do not necessarily exhibit all of the following failure modes. The frequency of occurrence of any of the following failure modes is variable among the vendors and among the lots shipped from a vendor. It is not the purpose of this report to discuss the details of the various failure mechanisms, but contributing factors to failures will be given when they are known and can be simply stated.

A. Open Nail Head Bonds (sometimes referred to as a Ball Bond) Using Gold Wires Making Contact to Aluminum Pads.

1. An example of open bonds due to the gold-aluminum eutectic formation ("purple plague") is shown in Fig. 2. In most cases, failures due to "purple plague" have been traced back to uncontrolled bonding procedures. The failures may be triggered by mechanical shock, thermal shock, acceleration, or vibration testing. "Purple plague" does not appear to be created during extended bakes at 200°C or less. This tentative conclusion is based on the fact that when a population of integrated circuits exhibits plague problems after baking, the plague problems are also detected after mechanical stresses prior to baking. Visual internal inspection accompanied by bond probing of integrated circuits from the population prior to any stressing has indicated that a weakened bond already exists.

2. An example of open bonds due to poor aluminum adhesion to the silicon dioxide is shown in Fig. 3. This failure type has always been found to be triggered by

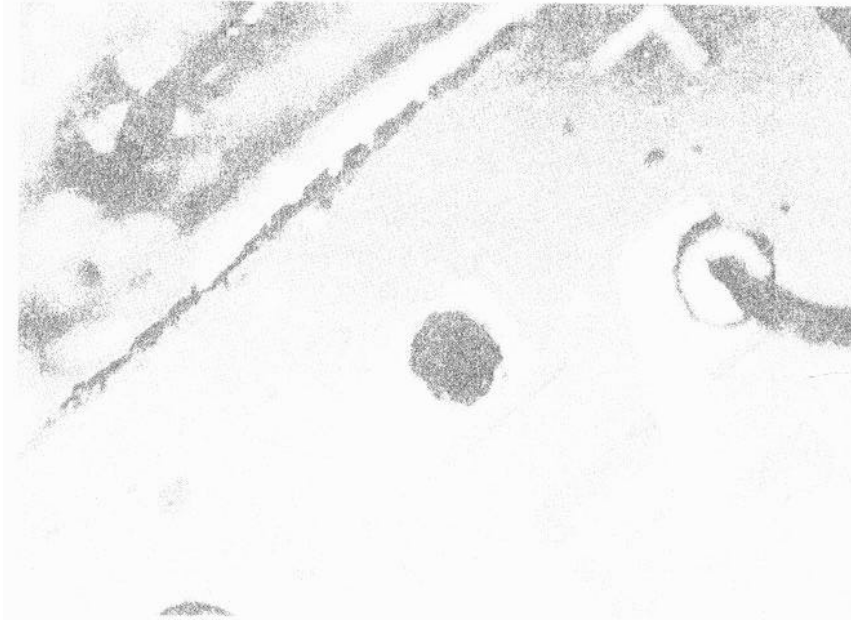


Fig. 2 An example of the gold-aluminum eutectid formation ("purple plague").

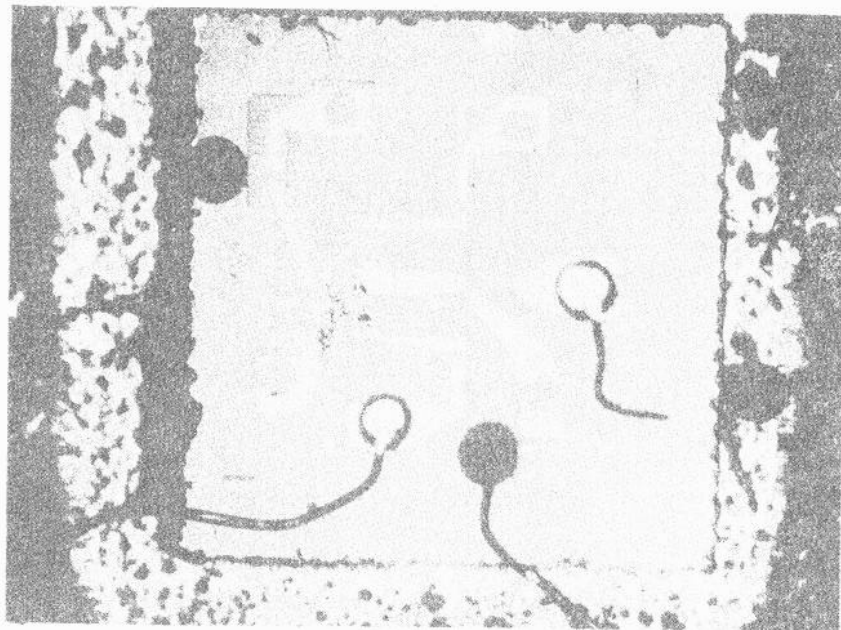


Fig. 3 An example of poor aluminum adhesion to the silicon dioxide.

mechanical stresses. Generally when this failure mode is prevalent in a lot, probing or pulling at the bond prior to mechanical stressing has shown that the bonds are easily opened. Examination of the underside of the bond has shown that the missing aluminum has adhered to the gold with no signs of "purple plague."

3. An example of open bonds due to underbonding (insufficient pressure and/or temperature) is shown in Fig. 4. This failure mode has always been found to be triggered by mechanical stressing. Although signs of plague are observed at intervals around the periphery, evidence of no metallurgical union of the gold with the aluminum is observed on most of the bond area.

4. Figure 4 may also serve as an example of electrically open bonds due to a periphery plague only, even if the bond were mechanically strong and most of the bond area had no plague. This failure mode usually occurs when the aluminum pad area is too small for the nail head bond area, or the nail head bond is misplaced such that the bond is made in the thinner region of the aluminum interconnect. Under these conditions, if the type of gold-aluminum eutectic formed is electrically insulating,³ the periphery plague is sufficient to cause an electrical open.

5. Figure 5 displays an electrically open bond attributed to overbonding (excessive temperature and/or pressure). Figure 5 pictures the only example of this failure mode shown with the bond intact to date. Normally open bonds due to overbonding pull up the silicon dioxide exposing raw silicon. The failure shown in Fig. 5 was detected after baking at 150°C for 168 hours. The baking may have contributed to the electrical failure by causing some of the aluminum

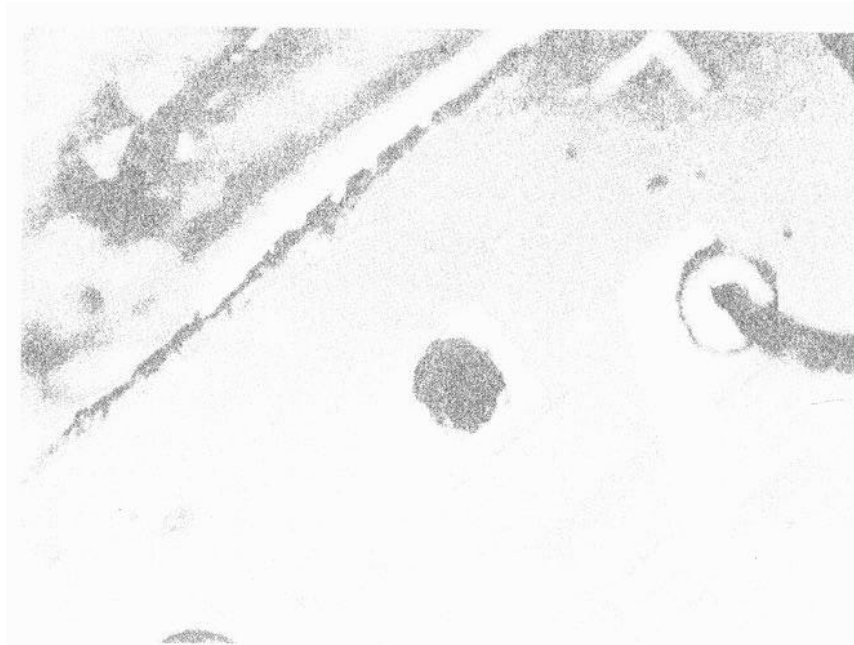


Fig. 2 An example of the gold-aluminum eutectic formation ('purple plague').

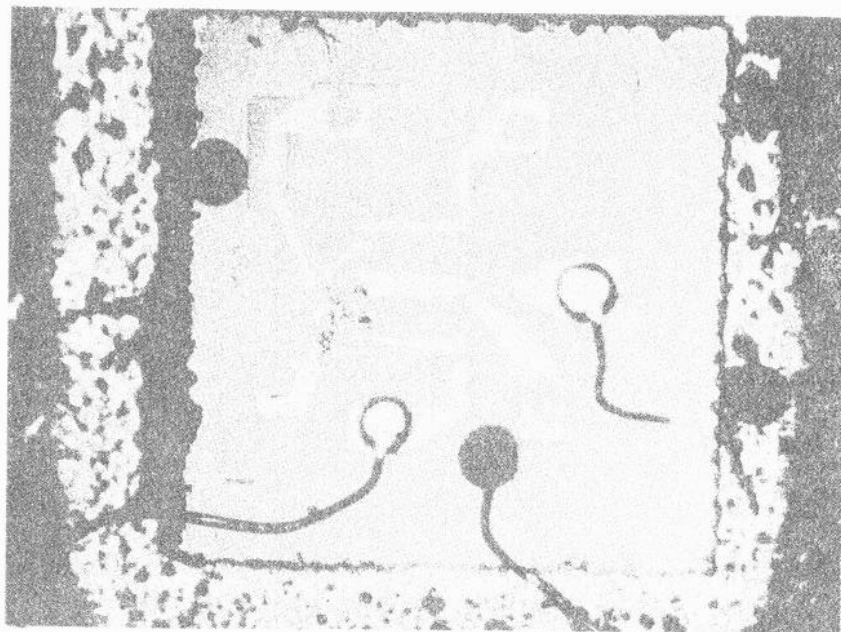


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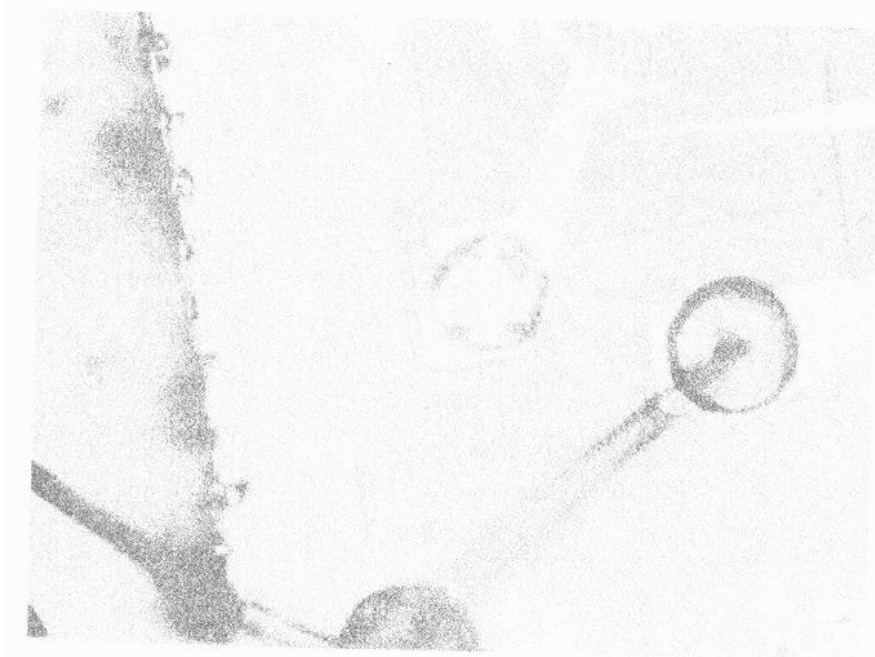


Fig. 4 An example of underbonding and periphery plaque.

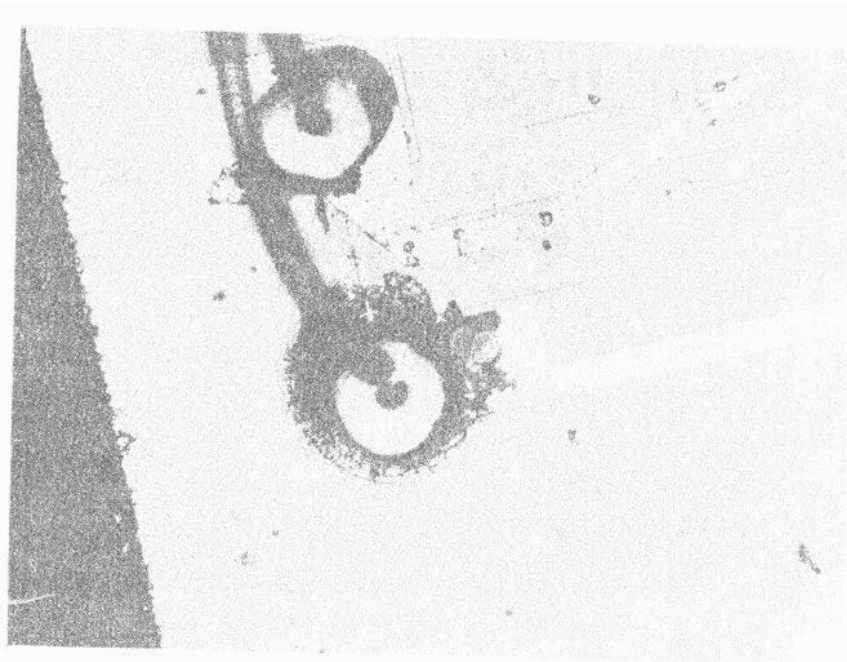


Fig. 5 An example of overbonding.

corrosion (to be discussed later). However, aluminum peeling or lifting is also evident and the baking could not have caused the fracture and discoloration of the silicon dioxide surrounding the bond.

B. Opens In Aluminum Interconnects

1. Figure 6a is an example of a hydrated alumina* which has formed at the dissimilar metal contacts in the presence of excessive moisture. Figure 6b shows a similar formation on the aluminum interconnect away from the gold. Although this electrically insulating compound may be formed at room temperature with time, the failure mode appears to be accelerated by power operating or baking. Figure 6a and 6b are examples of early in time failures.

2. Figure 7 is an example of an electrical open which occurred in an aluminum interconnect after over 6000 hours of operation at elevated temperature. By appearance, the open appears to be due to the formation of the hydrated alumina aided by a scratch. Although the scratch is a contributing factor to the failure, the failure was more basically attributed to faulty wash and dry techniques.

3. Another long in time operating failure, at room temperature, is shown in Fig. 8. Here, an open occurred in the base interconnect at a scratch such that the oxide beneath the aluminum is visible. Microscopic examination revealed no aluminum flaking or peeling, and it has been hypothesized that a transparent corrosion has been produced. The "disappearing" aluminum with no evidence of flaking or peeling has also been observed

* Identification of the hydrated Al_2O_3 was performed by Westinghouse, Molecular Electronics Division.

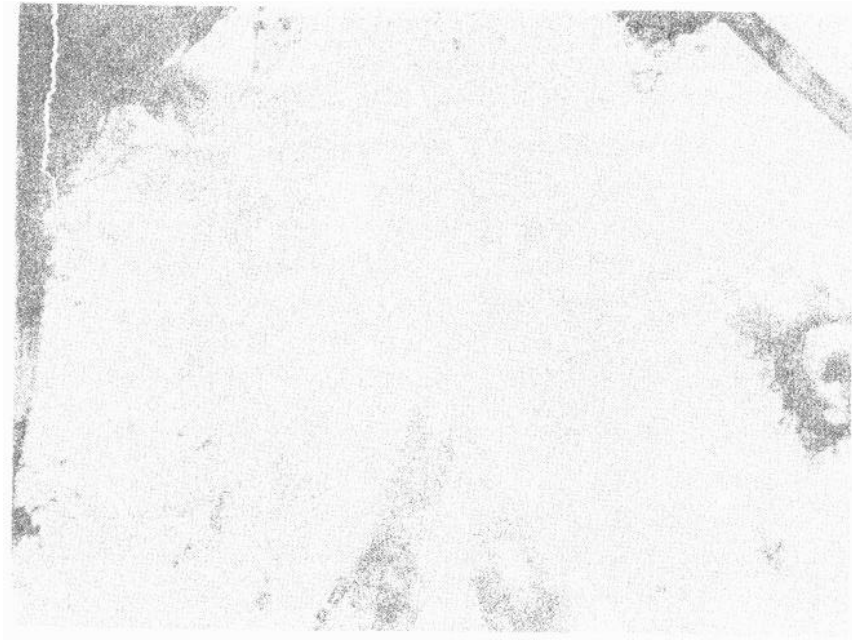


Fig. 6a An example of hydrated alumina emanating from dissimilar metal contacts,

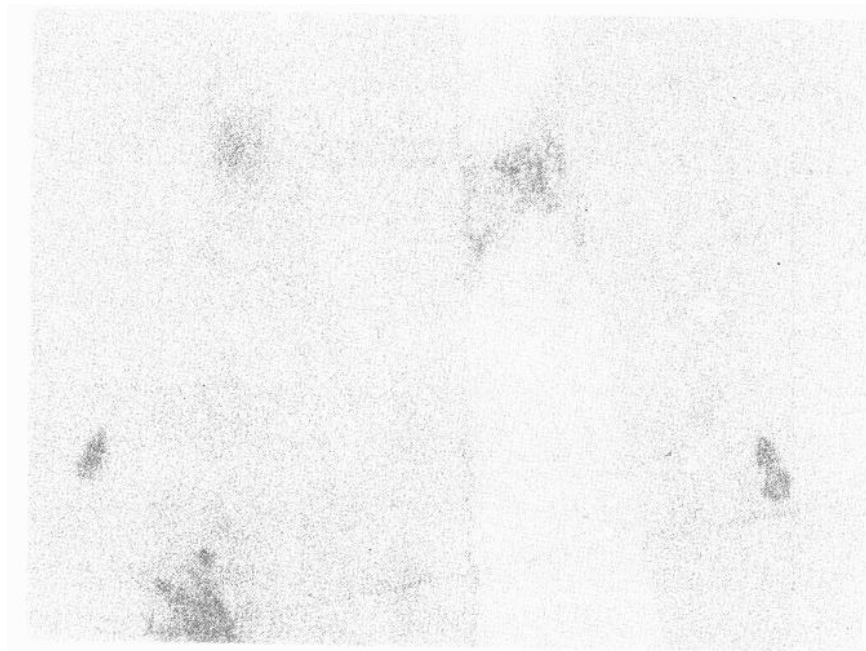


Fig. 6b An example of hydrated alumina forming in the center of an aluminum interconnect



Fig. 7 An example of an open created at a scratch after long time operation because of suspected hydrated alumina formation.



Fig. 8 An example of an open and melting created at a scratch after long time operation because of a suspected aluminum corrosion.

on devices where it was known that the aluminum was present initially. The regions of aluminum absence are usually found emanating from bonds and they are often detected after baking.

It is interesting to note that Fig. 8 shows a very localized aluminum melting such that the melt ran downhill at the oxide step. Preliminary studies using a thermal plotter have indicated that extreme localized heating, even in the base interconnects, can occur at scratches and at oxide steps in the interconnects of a powered device. For the type of failure shown in Fig. 8, it is suspected that the localized heating has accelerated a corrosion mechanism which in turn generates more localized heating as the resistance increases. Electrical overstressing for this failure type is improbable since the melting of a base interconnect without melting of a collector or emitter interconnect has never been detected after overstress conditions. Also for this failure, circuit operation was continuously maintained until time of failure,

It is interesting to note that unless excessive moisture (in the order of vapor pressures which allow condensation) is present within the package ambient, any corrosion phenomena seem to occur only at scratches or oxide steps for at least a year's operation at normal conditions. It should also be mentioned that several corrosion phenomena have also been observed on thin film powered and unpowered circuits using other than aluminum metal systems.

4. Figure 9 indicates that scratches contribute to opens even when the corrosion phenomena is not observed. In this case overstressing was possible although not certain, and it can be argued that severe scratching can markedly decrease the tolerance of a

circuit to overstress pulses which it could otherwise handle.

C. A non-photographable failure mode is the forming of electrically insulating layers between the aluminum and silicon where the two materials form an interface at the window in the oxide. The failure appears to be more rapidly detected after baking or operation, although it has been observed during shelf life. The electrically insulating layer is easily broken through with microprobe pressures or voltage. The latter is most troublesome since verification of the failure may heal the device. However, if spot alloying has not occurred, the failure may be recreated by baking. Several independent sources have attributed this failure mode to faulty oxide removal at the windows. Since this failure mode is time dependent one might speculate if a mechanism such as described by Wortman and Burger is occurring.⁴

D. Bulk shorts due to secondary breakdown⁵ occasionally occur in these low power devices. Also, bulk shorts caused by uncontrolled PNP switching may be found when the design of the integrated circuit is such as to allow floating internal junctions (i. e., not grounding isolation regions). These anomalous characteristics can generally be eliminated by proper specification of electrical characteristics.

E. An interesting type of shorting can be created by the always troublesome scratching of the chip surface as shown in Fig. 10. Because Fig. 10 shows a base-to-base short this unit will pass most functional electrical tests and will operate in a ring oscillating circuit. However, when logic operations are required, this circuit would appear as a failure.

F. Shorts have been detected from the aluminum interconnect to the silicon through the silicon dioxide. This is a voltage dependent failure mode and is attributed to the poor dielectric strength of the silicon dioxide. Poor oxide dielectric

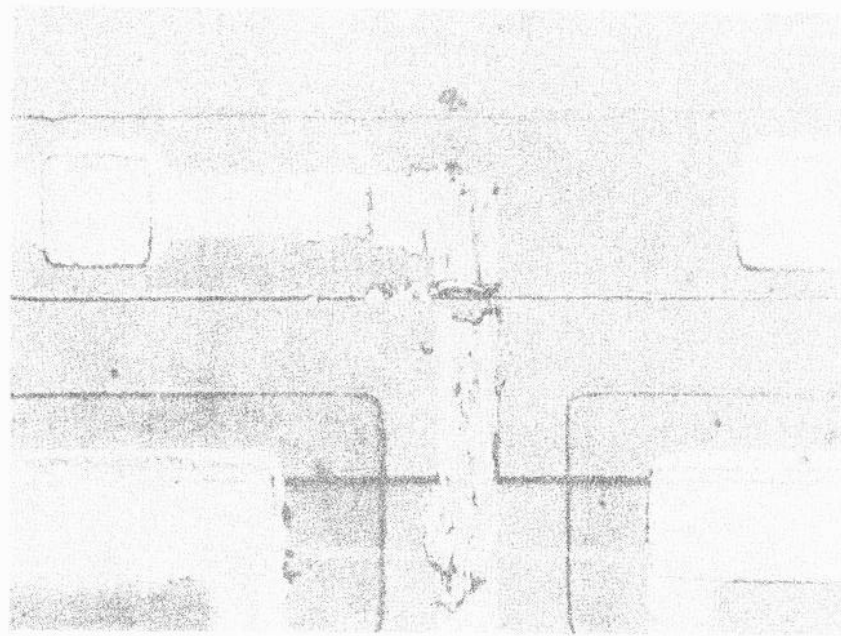


Fig. 9 An example of an open at a scratch over an oxide step due to aluminum melting.

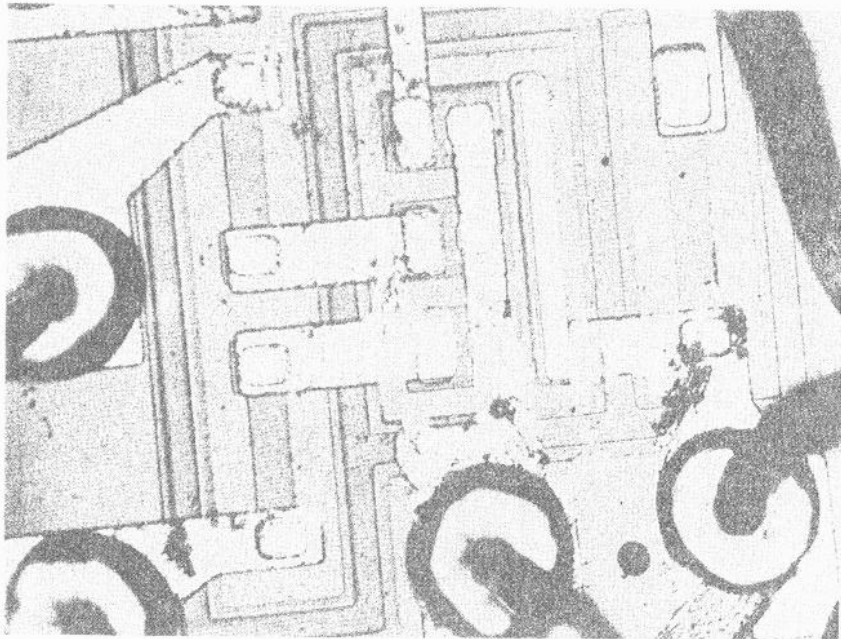


Fig. 10 An example of shorting due to aluminum scratching and smearing.

strength has been known to be created by oxide faults such as pin holes, entrapped impurities, and coating the silicon oxide with substances of poor dielectric strength. Generally this failure mode is detected during parameter testing or after purposely applying over voltage to the various diodes while stringently limiting current. Unfortunately complete shorting through the oxide may not always result. If partial oxide damage occurs without deteriorating the electrical characteristics of the device, a fault has been created which could be troublesome later in time.

G. Shorts have been created during parameter testing because bonds have been made too close to an oxide edge on the surface of the chip (poor pattern layout). Examples are given below:

1) Figure 11. shows that even though the bond appears to make contact to the silicon from the surface view the devices exhibiting this failure type are known not to have shorts to the silicon at one time during the testing procedure. Figure 12 depicts a cross-sectional representation where the oxide step is shown tapering. Shorting could occur by expansion of the gold through the distance, a. Perhaps equally possible is shorting through the silicon dioxide (distance b). Since the oxide thickness at b is capable of being much thinner, a decreased dielectric strength is possible, or added strains could result such that eventual rupture with or without applied voltage may occur. This particular failure type may be eliminated by not allowing pattern layouts which will potentially cause the described failures,

2. Figure 13 shows how poor scribing and dicing can cause a failure mode similar to that described in 7a above. This problem is caused not only by a poor pattern layout but also by poor alignment during



Fig. 11 An example of a bond made too close to unthermally oxidized silicon.

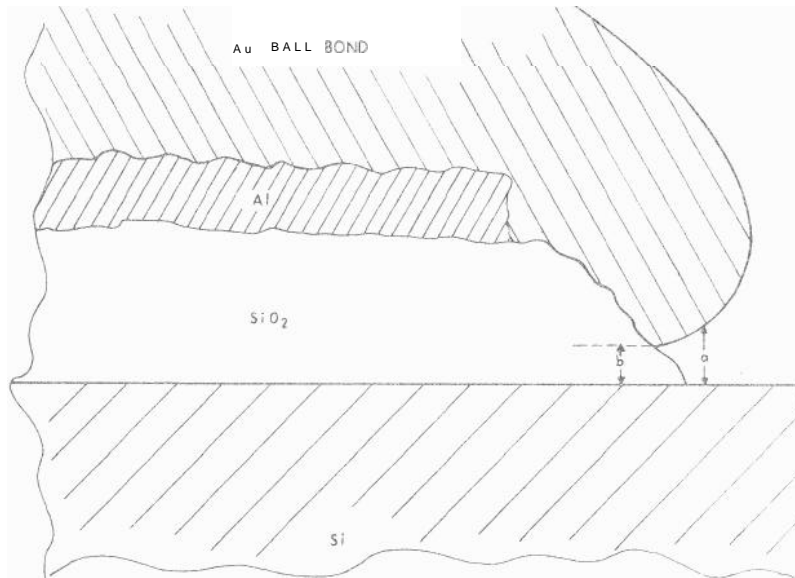


Fig. 12 A schematic cross-sectional representation of Fig. 11.

dicing and additionally creating excess chipping of the silicon dioxide.

H. Surface problems even with the "passivated" semiconductor occasionally cause failures although they are usually not of a catastrophic nature. Any impurities at the silicon-silicon dioxide interface in or on the silicon dioxide which have any translational or rotational freedom may become mobile in the impressed electrical field at the surface of a Junction, or during variations in thermal stressing. This then causes corresponding changes in the electrical characteristics. This has been the subject of many papers a few of which are referenced ⁶⁻⁹ and will not be covered in detail here. Specifically for the integrated circuits under study the predominant surface failure mode is the degradation of the gain and leakage currents under reverse bias. The degradation under reverse bias is aided by the application of elevated temperatures. The electrical characteristics may be recovered by baking without voltage stressing. This degradation is minimized or eliminated through changes in surface preparation. Some of the techniques are discussed in reference 6-9.

I. Figure 14 indicates an occasional failure due to cracks in the silicon die. Most of the chips which are susceptible to cracking during mechanical stressing or thermal shocking are those where strains have been set up during die attach procedures. Most notable are poor die attach procedures not using the silicon-gold eutectic although good die attaching has been observed using other than the standard technique.

J. Many types of shorts have been caused by internal lead wires and the method of making contact from the aluminum pads on the chip surface to the posts of the package.

1) Figure 15 shows the shorting of a gold lead to the edge of the silicon chip. The possibility of this type of shorting is enhanced by the fact that the contact to



Fig. 13 An example of excessive chipping and breaking exposing raw silicon.

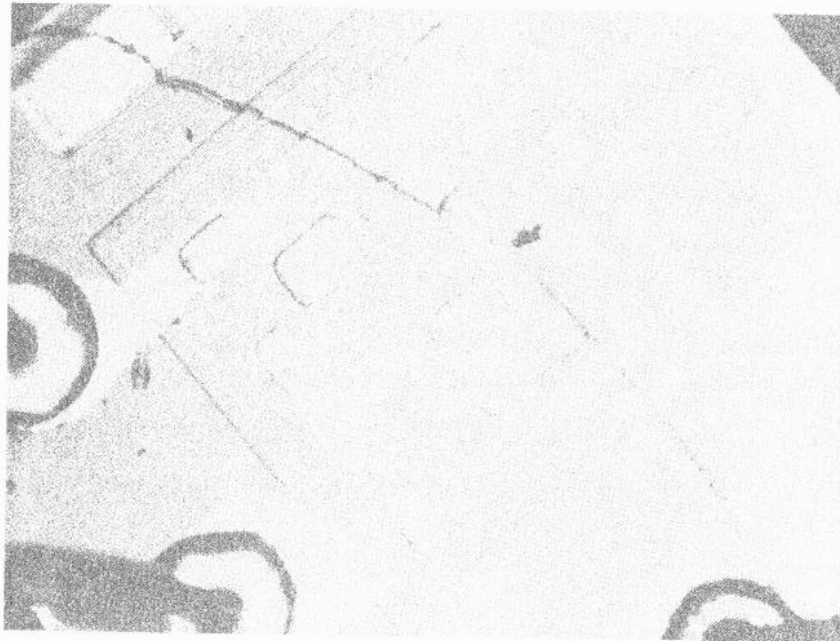


Fig. 14 An example of chip cracking.

the post of the package has to be made at a lower level than the contact to the surface of the chip. This failure mode can usually be detected after centrifuge testing. Note that this may be eliminated by using packages where the posts are higher relative to chip height.

2. Extra long lead wires may short to the lid of the package, the bottom of the package, the surface on edge of the chip, or to one another. Examples are given in Figs. 16 and 17. Note that Fig. 17 also shows the rotation of the chip such that connection to the post necessitates long looping leads.

3. Intermittent shorts have been found because of poor pattern layout and improper mounting in a package causing leads to come too close to one another. Although the leads are not overly long, mechanical stressing or the application of voltage may temporarily short the leads because they are too close. An example is given in Fig. 18.

K) Opens can occur in lead wires because of faulty handling, bonding and subsequent processing. Nicks and cuts in lead wires have been known to break open during mechanical stressing. If bonds are made such that an extreme thinning of the wire is forced, or the wire constricted, the wire is extremely susceptible to breaking open during the slightest of mechanical stressing such as handling. The latter failure type has been observed at the post of the package where wedge or capillar bonds rather than nail head bonds are made,

L) Loose material and particles within a package are always a potential cause of failures. Excessive "pigtailed" excess of a lead after the lead is broken off when a bond is made have created shorts. The presence of free conducting materials (metallic or otherwise) within a package is a most troublesome cause of failure. Non conducting free particles can cause mechanical



Fig. 15 An example of a lead shorting to the edge of the chip.

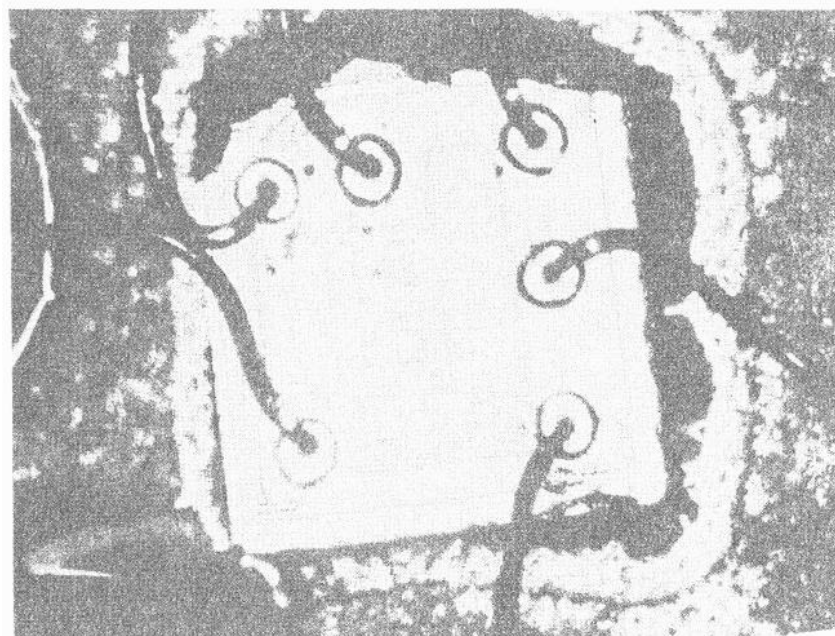


Fig. 16 An example of leads shorting to one another due to excessive lead length.

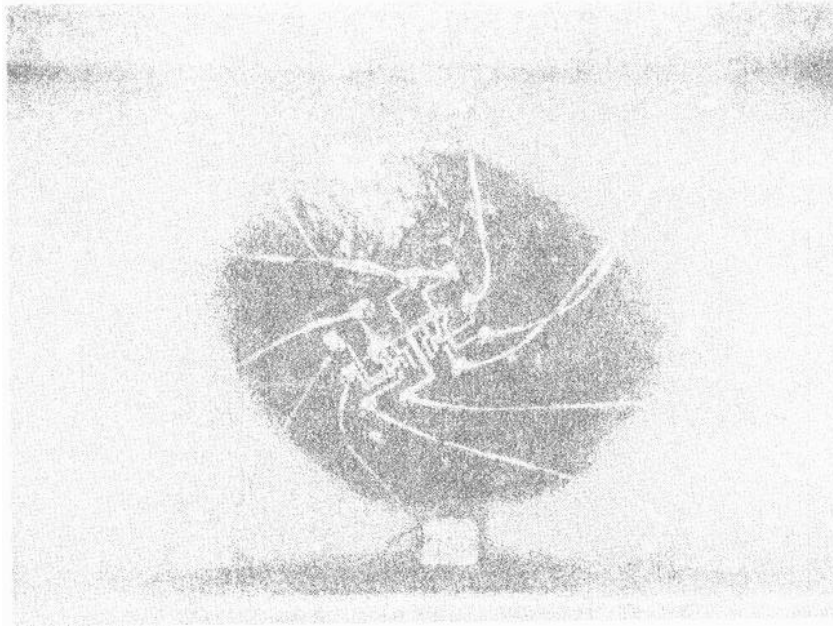


Fig. 17 An example of excessive lead length and improper chip orientation.

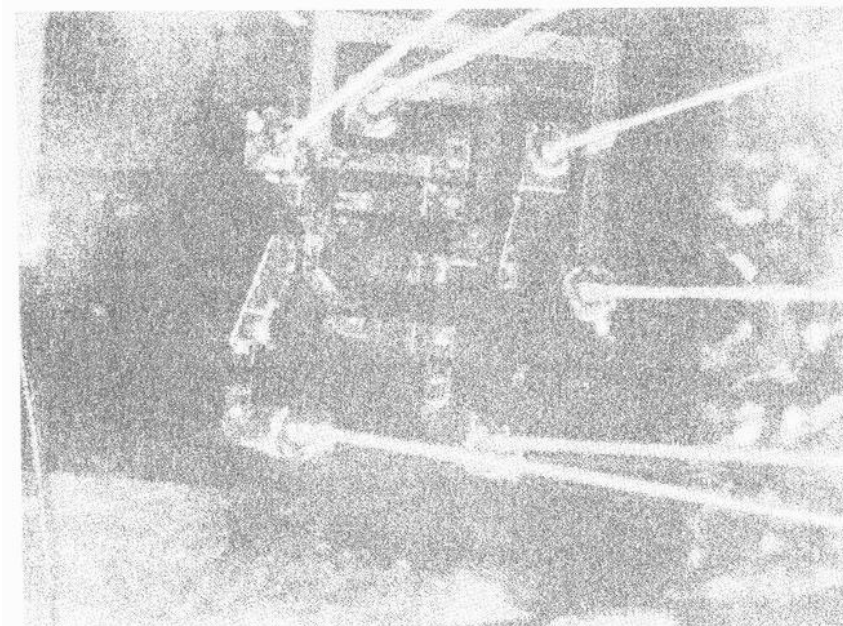


Fig. 18 An example of proper length leads shorting due to poor pattern layout and poor chip orientation.

ical damage.

The packaging of a semiconductor device will not be discussed in this report even though the package plays an important role in the reliability of the device. The failure or success of a package to meet the hermetic and mechanically strong enclosure of an electrical component is subject to study and testing as are integrated circuits and is the subject of another report.

IV. DETECTION, ELIMINATION, AND MONITORING OF FAILURE MODES

The list of failure modes given in the previous section might make appear impossible the task of developing a highly reliable integrated circuit. It must be noted that excluding poor design, all the indicated failure modes are the result of poor process control or the vendor's lack of complete technical knowledge of his process. A "dynamic state-of-the-art" process will be subject to Inadvertent process changes. As a result, attempts to legislate reliability through fixed processing documents are by themselves, ineffective. A program must be established to detect new failure modes, determine contributing causes and finally eliminate or minimize failures. Eliminating or minimizing failure modes implies controlled process changes. Continuous effective monitoring must be performed to assure that no process changes occur other than for reliability improvement and that the vendor can maintain a high degree of quality and reliability from lot to lot throughout the entire program. The functional aspects of the reliability program for the Apollo Guidance and Navigational system are the prequalification tests, the screen and burn-in testing, and extended life tests at use conditions.

The following is a brief description of the approach used for detecting, eliminating, and monitoring of failures.

The vendor prequalification tests consist of small samples of devices which are subjected to a combination of mechanical, thermal, and power stressing at normal and accelerated stresses. These tests are performed to detect many of the existing failure modes, and must be backed up by thorough failure analysis particularly when accelerated stressing is performed. The prequalification studies are coupled with thorough visual inspection of submitted samples and complete electrical characteristic studies. Knowledge of the device processing and any reliability history accumulated by the vendor is also incorporated. Although

all of the described information sources and testing procedures may not detect all of the future modes, insight into the quality and reliability of the device can be developed and non-destructive stress testing can be initiated.

Failure modes may now generally be classified as those which can be eliminated through specification; those which lend themselves to being eliminated through a series of mechanical, thermal, voltage and power stressing; and those which can be detected only occasionally after varied stressing. The latter comprise the group of so called troublesome or long time dependent failure modes. The easiest failure modes to eliminate are those which may be specified out. For example, any designing, processing, or packaging of devices which is found to create or aggravate known or new failure modes can be eliminated through specification. Electrical anomalies may be removed by electrical characteristic specification. Many of the failure modes given in the previous section fall into this category. Next, failure modes which occur early in time or are mechanically stress dependent (time independent and mechanical fatigue failures) are easily removed through a 100% non-destructive combination of stresses commonly referred to as screen and burn-in. Additionally, a properly designed screen and burn-in procedure allows for further detection of failure modes at realistic stress conditions, particularly those which are not easily "weeded out" (troublesome failure modes).

The screen and burn-in procedure if properly designed establishes a continuous vendor qualification and monitoring procedure. Once most if not all of the failure modes have been determined, vendor evaluation on large samples at realistic stress conditions can be maintained. Vendors can be rated with respect to

1. Number of failure modes,
2. Frequency of failure modes; i.e., how often a given failure mode appears.

3. Seriousness of failure modes. The seriousness of a failure mode depends upon how difficult it is to weed out or detect a given failure mode. Failure modes which are easily weeded out or detected can be tolerated in reasonable number but indicate a measure of the vendor's quality control. The more serious (long time dependent) failure modes are intolerable and indicate that a vendor does not fully understand his process .
4. How rapidly a vendor can eliminate or minimize failure modes. Feedback information is provided to the vendor such that vendor action for corrective procedures can be established and contributing factors to failure modes be determined and reported.

The screen and burn-in procedure then provides extensive vendor history from several points of view and provides continuous monitoring of lots from a given vendor. The monitoring assures that quality and reliability be maintained. If an unrealistic number of failures or failure modes is detected or if non "specoutable" or "weedoutable" failure modes occur, the lot can be rejected for use in critical high reliability systems.

Any test or qualification procedures which are designed to eliminate failures must be self correcting. If failures occur after a screen procedure, the complete screening and qualification procedures must be scrutinized. The failures and the lot from which they come must be studied. Simultaneously, as data is accumulated, failure mode and mechanism studies continue. Modifications may then occur in vendor qualification, the screen and burn-in procedure, and/or lot rejection criteria.

V. DATA AND ANALYSIS

The success of the standardization approach can only be demonstrated by its effectiveness. Table I provides a summary of the data, by vendors, accumulated up to 10 October, 1964. The following gives sample sizes, failure definitions, and further explanations as needed:

1. The prequalification tests were performed with samples of 100 to 200 devices for each vendor. The failure definition is an inoperable device in our computer circuits.

2. The screen and burn-in tests were performed with sample sizes ranging from 20,000 to 60,000 devices for each vendor. The screen and burn-in results are divided into two sections; the total fallout, and the fallout after baking, centrifuge, and power operating at room temperature. The latter is referred to as the second and third electrical results. The failure definitions for the second and third electrical results are: inoperable devices, any devices drifting out of the electrical specification, and any device exhibiting a maximum allowable percentage drift. The total fallout results include the same failure definitions as the second and third electrical results and also include incoming visual and electrical inspection fallouts, lead stressing, and hermeticity fallouts.

3. The failure rates at use conditions were determined with sample sizes ranging from 6,000 to 18,000 devices for each vendor. The failure definition is an inoperable device.

The data of Table I presents extremely interesting results, not only in showing the achievable reliability and the variation among vendors, but also in showing how the vendor maintains his respective position throughout the entire evaluation procedure. At the outset, the prequalification testing indicated an order of magnitude difference in the extremes. Just as significant were the failure types generated among vendors. Vendor A exhibited no serious failure modes

VENDOR	PRE QUALIFICATION % FAILURES	SCREEN & BURN-IN % FAILURES		FAILURE RATES AT USE CONDITIONS 90% CONFIDENCE
		TOTAL	2nd & 3rd ELECTRICAL	
A	5	1.8	0.3	0.005% / 10^3 hrs (0 FAILURES)
B	26	3.8	1.7	0.3% / 10^3 hrs (2 FAILURES)
C	58	5.0	2.5	1.8% / 10^3 hrs (26 FAILURES)

Table I A summary of vendor reliability evaluation

while Vendor B exhibited one of the very troublesome failure modes and some mechanical problems. Vendor C exhibited most of the more serious failure modes and many general quality control problems.

The correlation of the prequalification results to the screen and burn-in results is amazing. Comparing the prequalification percentage failures to the second and third electrical percentage failures, it is seen that in both cases there is a factor of 3 difference between Vendor A and B while there is approximately a factor of 10 difference between Vendor A and C. Again Vendor A did not exhibit the serious failure modes throughout the extensive screen and burn-in testing. Vendors B and C exhibited the same failure modes detected during prequalification testing with some additional ones.

The most interesting and applicable comparison is that of the failure rates during computer use. It is interesting to note that although a small percentage fallout for the best vendor occurs during the stress testing of screen and burn-in, over 50×10^4 element hours were accumulated with no operational failures. The lower failure rates of Vendors B and C are partly reflected in the fewer accumulated element hours ($\sim 2,000,000$). However, the failure modes detected at use conditions are an indication of things to come. The chance that Vendor B will accumulate another 98×10^4 element hours for the same population without an additional failure is improbable. These additional element hours are needed for Vendor B to compete with Vendor A. The serious time dependent failure mode described in Section III, C, constitutes the two failures of Vendor B. As far as Vendor C is concerned, the situation appears hopeless for the same population of devices. It does not appear that Vendor C will ever accumulate sufficient device hours to be competitive with Vendor A. The detected failure modes at use conditions for Vendor C were a combination of interconnect corrosion, oxide breakdown, and failure modes due to generally poor quality control.

The data of Table I does not necessarily indicate that future populations of devices of Vendors B and C will not have their failure modes under control.

VI. EFFECT OF COMPONENT RELIABILITY ON SYSTEMS DESIGN

Without the demonstrated high reliability of integrated circuits other methods of achieving the reliability goal through design would be required to satisfy the Apollo mission. Since failures are not random but are always based on cause and effect principles, passive redundancy would not have efficiently achieved the required mission life time. The alternative was to consider forms of active redundancy.¹⁰ One solution was inflight sparing and maintenance. The maintenance would be accomplished by interchanging modules with the aid of the computer system and self test procedures. With respect to any redundancy technique, the inflight sparing concept minimized the system weight, power, and volume. The disadvantages were a requirement for additional crew tasks in case of failure and the possibility of a time critical failure which could not be repaired. Also packaging to allow for inflight repair was a serious restriction on the design and in itself introduced reliability risks. Alternatively, at a higher cost in weight, power, and volume, two active computers could be provided. This concept allowed for computer switching via the operator at any time during the flight, thus reducing the possibility of the time critical failures when there would be no time for repair. Both computers were required to be operating only during the time critical phase of the mission and switch over would be accomplished by electronically gating out the output commands of one of the two computers. Because of the proven reliability of the integrated circuits, redundancy becomes unnecessary with the resultant use of a single computer and no inflight repair.

VII. SUMMARY

An approach which designs in and builds in reliability through standardization of parts has been presented. The standardization approach has been exemplified through the choice of a simple planar process integrated circuit, the high reliability of which has not been heretofore extensively demonstrated.

Unlike the redundancy approach which also attempts to design in reliability, the standardization approach has a major advantage in that no assumptions need to be made concerning how parts fail. The list of detected planar process integrated circuit failure modes again shows that failures are not random but that failures have causes which are always traceable to misuse and handling, vendor control, or insufficient vendor process understanding. The variation of failure modes and frequency of failures among vendors, the variations among lots of a vendor, and non-randomness of failures make redundancy design expensive and unwieldy. On the other hand, the standardization of parts approach lends itself economically to thorough testing procedures, failure detection and elimination through failure analysis, and vendor evaluation and monitoring. Purchasing of large volumes of a simple part causes vendor incentive and experience which also aids reliability improvement. Through standardization, large samples become available for reliability demonstration prior to field use at realistic use conditions.

The achievable reliability of integrated circuits has finally been demonstrated.

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