

E-2402 PORTAFAM SYSTEM OPERATIONAL DESCRIPTION by Jonathan Leavitt July 1969

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PORTAFAM SYSTEM OPERATIONAL DESCRIPTION

ABSTRACT

The purpose of this report is to provide an operational description of the Portafam system. Special attention is paid to the master control logic and front panel controls.

Portafam is designed to provide a compact electrically alterable core rope simulator to replace the fixed memory or rope memory in the Apollo guidance computer (AGC). The construction and operation of this system is described on a subsystem level.

The master control logic controls the operation of all subsystems in Portafam and therefore an understanding of this subsystem logic is necessary to operate the complete system. This logic is described in detail including a description of the interfacing pulses to other Portafam subsystems.

Front panel operation procedures are also analyzed in order to further explain the proper operation of the complete system.

> by Jonathan Leavitt July 1969

ACKNOWLEDGMENT

Allen Harano designed the AGC Interface, Master Control Logic, and major portions of the Display and Control Panel.

Phillip Ward specified the Tape Transport and designed the Tape Control Logic, Remote Test Unit, and major portions of the Display and Control Panel.

Bruce Barrett, Thomas Donegan and Robert Tove designed major portions of the core memory.

Eldon Hall made many helpful suggestions for organizing the material in this report.

The aid of the above individuals in the understanding and organization of the material presented in this report is herewith acknowledged with gratitude.

This report was prepared under DSR Project 55-38625 sponsored by the Manned Spacecraft Center of the National Aeronautics and Space Administration through Contract NAS 9-4065 with the Instrumentation Laboratory of Massachusetts Institute of Technology in Cambridge, Massachusetts.

The publication of this report does not constitute approval by the National Aeronautics and Space Administration of the findings or the conclusions contained therein. It is published only for the exchange and stimulation of ideas.

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PORTAFAM SYSTEM

CHAPTER 1

PHYSICAL CHARACTERISTICS

1

The Portafam System is a compact, electrically-alterable core rope simulator designed to be installed into the spacecraft. The System consists of four subsystems described below. These are Interface Electronics; Tape Transport; Portafam Assembly; and finally the Power Supply which, in the present design, should be external to the spacecraft. The System is designed to simulate the programs of a complete set of rope modules and to provide a program trace capability for software diagnostic analysis following a hardware restart.

Portafam will accomplish the following operation objectives:

- 1. The AGC fixed memory is simulated with an erasable memory which can be loaded from a magnetic tape.
- 2. A portion of the Portafam erasable memory, called Trace Memory, is designed for use as a recirculating push-down list for storing the contents of recently AGC-fixed memory locations. In case of a restart this list of addresses is transferred to the magnetic tape for later processing.

1.1 <u>Interface Electronics</u>

As shown in Fig. 1.1, the AGC Portafam interface circuitry replaces both physically and electronically six modules which comprise the fixed memory of the AGC. There are two large interface boxes each of which replaces three of the smaller rope modules. The interface electronics is located in one of the two boxes and consists of five two-sided etch plated-through hole printed circuit boards which are hinged to permit access to all components. Communication between interface circuitry and Portafam is effected by means of a cable which connects to the front of the box containing electronics. In addition a short cable between the two boxes supplies the interface with needed signals which are available





only from the plug in the back of the box which does not contain the electronics. Each of these boxes receives the interface signals for three ropes while one of the boxes supplies the AGC with the output signals for all six ropes.

1.2 <u>Tape Transport Assembly</u>

Figure 1.2 illustrates the tape transport for this system purchased from Data Science Corporation, San Diego, California. It may be mounted as shown in Dwg. 166458 in an external chassis and connected by a cable to the tape control electronics which is located in the main Portafam assembly.

1.3 Portafam Assembly

An enclosure which will be referred to as Portafam (Fig. 1.3 and Dwg. 166565) contains various components of the system. This chassis contains three separate trays which are designed to accept modules in various configurations.

1.3.1 Memory Subsystem

The lower tray or tray C of this chassis (Fig. 1.4 and Dwg. 166545), contains a core memory subsystem. The electronics of this system is similar in construction to that used in AGC itself. Three core stacks which are purchased from RCA are each organized into coincident current 16, 384, 16-bit word capacity stacks. Figure 1.5 shows the selector board designed by MIT/IL attached to the top of each of these stacks. These boards contain the address and decoding logic required to access these stacks. Sense and digit drivers are located in external modules similar in construction to AGC cordwood assemblies and connected to the stack separately. Input and output signal and power access is accomplished by a cable running from tray C to tray A, the master control tray. Special power generation is accomplished by means of power cubes located in this memory chassis. This will be covered in Section 1.4.1. Timing and other memory subsystem logic is assembled in cordwood construction or its equivalent for the handling of integrated circuits.

1.3.2 Tape-Control Logic

Above tray C is located tray B (Dwg. 166547) which contains the tapecontrol logic. This logic uses NAFI card construction which consists of a printed circuit card with a 40-pin connecter which will accept circuitry of various types. The cards in this subsystem utilize Texas Instruments



Fig. 1.2 Portafam tape transport.

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Fig. 1.3 Portafam assembly.



Fig. 1.4 Portafam core memory subsystem.





series 74 logic in most cases. Dual in-line packages of 14 to 16 pins are mounted three per NAFI card, with the cards plugged into wireup connectors. The wire wrapping was accomplished automatically through the use of a computer program to generate a card deck which was used to operate a computer controlled wire wrapping machine. Note that the interconnections for the memory tray C were also wire wrapped but because of the nonstandard design of the connectors, this was accomplished by hand. Input-output signals for this tray are accomodated by means of hand wired leads from tray B to tray A.

1.3.3 Master Control Logic

The master-control electronics (which is the main topic of this report) is contained in tray A (Dwg. 166548) of the Portafam chassis, located at the top of the chassis. The construction of this tray is similar to tray B in that NAFI cards are used for logic (Fig. 1.6). In addition NAFI connectors are used torun cables from the front panel to this master-control unit. Thus all input-output signals from this Portafam chassis are fed through the connectors in a single row of tray A. The wire wrapping of tray A (Fig. 1.7) was done by a computer-controlled wire-wrap machine as was that of tray B.

1.3.4 Display and Control Panel

The front panel of the Portafam chassis (Dwg. 166541 and Fig. 1.8) contains switches, dials, and displays which permit operator access into the Portafam system. Trays A, B, and C previously mentioned are bolted to each other and to the front panel. All connectors to the front panel fit into tray A. Service loops are provided so that the front panel may be removed a distance from the logic trays to permit servicing either in an operating or non-operating mode. In addition, as previously discussed, feed-through connectors are mounted on the front panel to permit connection to the tape transport of the interface assembly, the rope interface assembly, the power supply, and a test box. See Section 4.3 for a detailed discussion of front-panel operation.

1.4 <u>Power Supply System</u>

The power supply system consists of internal power cubes and an external supplies assembly.



Fig. 1.6 Portafam master control logic, card side view.



Fig. 1.7 Portafam master control logic, connector side view.



Fig. 1.8 Portafam display and control panel.

1.4.1 Power Cubes

Power cubes in tray C (Section 1.3.1) supply the power for the memory electronics. The power cubes receive 28 volts, $\pm 15\%$ and generate ± 23 vdc, ± 5.250 vdc, and -5.250 vdc, all with a $\pm 0.5\%$ tolerance. The 28 vdc input to the power cubes is isolated from the chassis. The low sides of the outputs are all connected to chassis.

1.4.2 External Supplies Assembly

External supplies (Fig. 1.9) consist of +28 vdc, + 10 vdc, and +5 vdc supplies. The 28-vdc supply feeds the power cubes in the memory and the tape transport through the front panel. The 10-vdc supply is used for indicators on the front panel and the projected remote test unit. The 5-vdc supply activates the master-control, tape-control, front-panel and test-box logic.

1.5 <u>Remote Test Unit</u>

A remote test unit (Fig. 1.10) has been constructed to permit easier testing of this system. This unit consists of an 85-pin connector with a four-foot cable connected to a chassis which contains two rows of nine transistorized indicator lamps; a single-pole, five-position, rotary switch; two single-pole double-throw switches; and associated resistors and capacitors for interfacing of input signals. The rotary switch is used to select the various banks in the tape-control logic in four groups of nine banks each. The indicator lamps are labeled as primary indicators (P) and verify-error indicators (V). At the initiation of the test all lamps are on. After the first load the P lamps go off. After the second load the V lamps go off. After the third load P lamps turn on again. Therefore, a perfect load is all V lamps off and all P lamps on. An acceptable load is all V lamps off; all P lamps either on or off. Perfect loads are indicated in the banks where the P lamps are on. A bad load has occured in any bank where a V lamp is on. The fifth position of the bank-selector switch is used as a lamp test for the chassis. The two single-pole, double-throw switches are labeled reset-trace address, and inhibit no-cycle timing. These switches perform the logic indicated in the master-control logic sections of the Portafam assembly.



Fig. 1.9 Portafam external supplies assembly.



Fig. 1.10 Portafam remote test unit.

CHAPTER 2

2

GENERAL SYSTEM OPERATION

MIT Block II AGC contains a destructive readout core memory of 2K × 16 bits and a core rope memory of 36K × 16 bits capacity. The cycle time of both of these memories has been established at 11.7 microseconds. Information in the core rope memory must be calculated for each particular mission and then wired into this memory. The use of this electrically unalterable program memory or fixed memory in the AGC has delayed spacecraft checkout with mission programs until a few months before launch date. Portafam is intended to alleviate some of the delay in checkout of mission programs by providing simulation of the rope memory with any program easily loaded into this fixed-memory simulator by means of a program tape. In addition special program and trace capability is also provided.

2.1 Rope Interface Assembly

This subsystem consists of two boxes which mate with the AGC rope connectors, convert digital signals from the Portafam interface to simulate rope signals and then convert AGC signals to the rope connector into digital signals which the Portafam digital logic may interpret.

2.1.1 Theory of AGC Rope Memory Operation

The Apollo Block II rope memory is organized into six modules of 512 cores each. Each of these 512 cores contains 12×16 wires. These 16 wires in each core consist of one of the 16 bits of a single word. Selection is made at two different times. During the first selection period nine binary bits select one of the 512 cores in each module. During the second selection period the AGC performs one of two functions. The AGC aborts the previous nine address bits selected if it is not operating on the rope memory during that period, or, if rope memory selection is required, it generates an additional seven address bits which then select one of 12 sets of 16 wires in one of the six modules. Thus at this selection time a single word of 16 bits is read out to the memory. In addition to the above activities the AGC may not even activate the first nine bits, and thus AGC cycles may occur at periods greater than the standard 11.7 microseconds between normal AGC cycles. All of the above AGC options are considered in the Portafam logic.

2.1.2 Interface Timing

Refer to Fig. 2.1, AGC and interface timing. The AGC cycle begins with an IHENV pulse (inhibit pulse) and SET pulse (set line pulse). During this period of memory fetch, one of two set lines sets one core per 512 core module, other cores being inhibited by 7 inhibit lines and a parity line plus their complements. The AGC interface generates a SETOR/ pulse which is generated by a delay from the leading edge of the SET pulse. This SETOR/ pulse is sent to the Portafam by the interface module. It indicates that the first nine bits of the rope memory address (fixed-memory address) have been selected and will be on the address lines from the interface to the Portafam system. There are 16 fixed-memory address (FMA) lines between the interface and Portafam. This first decoding generates data which will appear shortly on the nine least significant bits of these lines. Note that after the IHENV and SET pulses have turned off that either a STRGAT pulse which decodes the additional seven bits of information, or a CLROPE pulse, which resets the ropes and does not decode the additional bits of information, is generated by the AGC to the interface circuitry. The interface circuitry then generates STR116/ pulse or a CLR19/ pulse to Portafam. These pulses are derived from the leading edge of the STRGAT and CLROPE pulses respectively. The STR116/ pulse indicates that a full 16-bit address is present on the FMA lines, while the CLR19/ pulse indicates only nine low-order bits are present on the FMA lines because an abort cycle of the AGC has occurred. If a normal cycle has occured (STRGAT pulse generated) then the AGC will also send a RESET pulse to the interface. The reset pulses reset the ropes and thus readout the information. SBF is a strobe-memory pulse and strobes the sense amplifiers of the rope signals into the memory buffers of the AGC. The Portafam must present data to the rope interface of the AGC at this time. Note also that the TPGF pulse is a test-parity signal and occurs at a time when the information is settled in the buffer register of the AGC. The interface circuitry generates a STROBF/ pulse derived from the leading edge of the



Fig. 2.1 AGC and interface timing.

reset signal. This pulse is intended to coincide with the SBF signal in the AGC and gates the contents of the data lines from Portafam into the sense amplifiers of the AGC. In addition Portafam must send information to the interface circuitry. This is accomplished through the 16 AGCD01/ to 16/ lines which are connected to the interface through the Portafam data bus. The end of the STROBF/ pulse also signals to Portafam that the data are no longer required by the AGC. This will be discussed in detail later.

2.2 Tape Transport Assembly

The Portafam system requires a tape recorder and reproducer subsystem in order that the programs to be stored in the core memory may be easily entered into the system. In addition the tape unit is utilized to store malfunction data and thus permits analysis by external means, such as large computer systems. A brief investigation of this subsystem with emphasis on how it relates to the Portafam master control follows.

The tape subsystem consists of a tape transport purchased from Data Science Corporation of California plus tape-control logic to permit the use of this tape transport in the Portafam system. A detailed discussion of the tape transport and control logic is beyond the scope of this report. See Specification 171039 for more information.

2.3 Portafam Assembly

2.3.1 Core Memory Subsystem

In order to replace the fixed AGC memory with an erasable memory subsystem, a core memory is required since random access is necessary and the subsystem must operate somewhat faster than the 11.7 microsecond cycle time of the AGC memory. The Portafam's erasable memory system consists of three nearly identical modules, each having a capacity of 16K by 16 bit words. The memory is organized in a conventional coincident current arrangement. Each memory module is equipped with its own address decoding system and its own digit and sense systems. Each module shares (with two other modules) a memory address register (MAR), the memory buffer register(MBR), a control pulse generator (sequence generator), and power supplies. Note that the total capacity is 48K words, while the rope memory used in the AGC has only a 36K capacity. The additional 12K are therefore unassigned and in the Portafam system are utilized as a pushdown trace memory which records, in order, the fixed memory addresses (FMA) as they are received from the AGC interface

circuitry. It should be noted that since 16 bits of information are required for a full FMA and since parity generation is also required in this information that a single fixed -memory address may fill two locations of trace memory. This will be discussed in detail later.

Refer to Fig. 2.2, Master control:memory cycle timing. Note the following wave shapes. When a cycle type is first established, the RDREST line is either positive for the read/restore mode or at ground for the clear/ write mode of memory system operation. Coincident with the establishment of the mode request, the ADDRSG signal is generated. This is used to strobe address data onto the 16 data input lines (MBRI01-16) between the Portafam master control and the Portafam core memory subsystem. Coincident with the address strobe pulse generation a CYCREQ (cycle request) pulse is also transmitted to the Portafam memory from the master control. This cycle request pulse is followed internally in the core memory by a MARGATE pulse which strobes the address line data into the MAR of the memory. After the address strobe pulse has returned to ground a DATOUTG (data-out strobe) pulse is generated by the master control which strobes the bit data information onto the same 16 lines as the address information. Coincident with a portion of the DATOUTG pulse a WMBR (write memory buffer register) pulse is internally generated in the memory which strobes this data information into the MBR of the memory. Note that this pulse only occurs during a clear/write cycle since during a read/restore cycle the data to be accepted by the MBR is stored in the cores of the memory. At the conclusion of the DATOUTG pulse the master control internally generates a DATING signal which, in read/restore cycles only, initiates a RMBR (read memory buffer register) pulse to the Portafam memory. This signal strobes out the data from the MBR which was written by the addressed cores. Note that in all except the AGC modes the RMBR pulse turns off at 3 microseconds after the start of the CYCREQ pulse. In the AGC modes this line remains active until after a STROBF/ pulse is received from the AGC interface which indicates that the AGC no longer requires data on the data lines. Note also the TSTPTIM pulse which occurs toward the end of the DATING function. TSTPTIM is used to time parity testing among various logic functions in the master control. At the end of the DATING pulse a CYLEND (cycle end) pulse is generated during all operations except the AGC modes. This pulse is used in most cases to reset the mode logic that has determined in which mode the master control has been operating. The various manipulations of these timing pulses by the master control will be discussed in detail in Chapter 3 when the master control logic is analyzed.





2.3.2 Tape Transport Control Subsystem

Various modes of tape subsystem operation interact with the Portafam master control.

Refer to Fig. 2.3 (Data flow tape commands). This logic flow diagram shows how the Portafam master control transmits front panel and AGC interface signals to the tape control logic to permit entrance to various tape modes. The basic modes of operation are: load mission program, in which a mission program is read into the core memory; load special program, in which a special type of program is written into the core memory; and dump trace mode, in which the trace portion of the core memory subsystem is read out to the tape subsystem. These modes may be entered either from the AGC interface through event sequences or the front panel. See Section 3.6.1 for a detailed explanation of this logic.

Figure 2.4 is a state diagram of the Portafam master control during various tape modes. The master control performs the various functions after a load request is received from the tape unit. The state of the function depends on parity checks and other information from the logic. This will be discussed in more detail in Sections 3.6.2 to 3.6.7 and illustrated in Figs 3.5 to 3.10.

2.3.3 Master Control Electronics Functions

The major functions of the master control electronics outline the modes in which the whole Portafam system may be used.

2.3.3.1 AGC Data Fetch

The purpose of the AGC data fetch operation is to retrieve from the Portafam core memory data corresponding to an AGC fixed address. These data, because of the interface electronics, appear to the AGC as the equivalent of a rope memory core signal.

2.3.3.2 Trace Cycles of AGC Address

As previously mentioned a section of the Portafam core memory subsystem is used to record the address of the AGC cycles in the order requested of Portafam. This should be helpful in diagnosing problems if errors occur. To record an AGC address requires one or two trace memory cycles.



Fig. 2.3 Data flow tape commands.



Fig. 2.4 Tape mode states.

2.3.3.3 Tape Load into Core Memory

The purpose of this operation is to load either a predetermined mission program or predetermined special program into the fixed portion of the Portafam core memory from the tape subsection. Note that AGC program data are never loaded into the trace memory. Even if an AGC or Portafam failure occurs only the address of the AGC program into which the fixed data were loaded is recorded in the trace memory.

2.3.3.4 Trace Memory Dump to Tape

This operation permits the recording of trace memory information on a tape reel. The tape reel may then easily be analyzed by an external computer system if required because of system malfunction.

2.3.3.5 Manual Operations

Various manual operating modes are designed into this system to permit easier troubleshooting if errors do occur.

In the manual read mode the Portafam core memory may be manually addressed by the means of the thumb wheels located on the front panel which displays the data at that address on the front panel. This mode is used to read program or trace memory.

Data may also be loaded into a manually selected core memory address by means of thumb wheels on the front panel. Utilization of this manual load mode and the manual read mode should permit easy analysis of the core memory subsystem if trouble is suspected in that section. In addition, mission program data may be easily modified during software checkout.

This read trace address mode permits the reading of the trace address without incrementing the trace address counter. This should prove useful if an AGC or Portafam error is suspected in a particular trace address of the core memory. This address can then be selected and studied utilizing the other manual modes.

If a restart occurs the trace memory can be manually read to determine the events which led to the restart.

2.3.4 Display and Control Panel

The display and control panel is the interface to the operator for this system.

Drawing 166565 contains the best illustration of the front-panel system. Drawing 166541 also shows this chassis but does not include the labels on the switches or display information. Drawing 171011 illustrates the various connections to the front-panel control switches and display drivers. It does not show the connections to the various feedthrough connectors for the test box, the power supplies, the tape transport, and the AGC interface. As illustrated in these drawings and Fig. 1.8, this display panel permits manual operation of the Portafam system as well as interpretation and display of address and data information. Front-panel operation will be discussed in detail in Chapter 5.

CHAPTER 3

MASTER CONTROL LOGIC ANALYSIS

3.1 Logic Drawings

3

See Table 3.1 (Logic schematic list). This table lists the logic flow diagrams of all the logic located in tray A. The drawings were generated by the same computer program which automatically generated the card deck and wire list, Dwg. 171036, for wire wrapping the tray. These drawings will be studied in various logic groupings. Detailed discussion of this hardware by mode data flow follows in Sections 3.4 to 3.7.

3.1.1 Timing

Drawing 171053 (Master control: memory cycle timing) contains a buffer toggle stage plus a five-stage shift register which is used to generate the various memory cycle timings as illustrated in Fig. 2.2 and described in Section 2.3.1. In addition, Dwg. 171043 (Master control: no cycle timing) shows the input from a 5.3376 megahertz oscillator which is used to generate the \approx 2 megahertz clock and, in addition, times the AGC signals such that if an AGC pulse does not appear in the normal AGC-cycle time a NOCYCL (no cycle timing) signal will be generated. This will be discussed further in Section 3.1.3.

3.1.2 Cycle Type Decoding

Drawings 171048 and 171049 (Master control: cycle request primaries I and II) contain various buffer flip-flops to store mode information received from external sources. Drawing 171050 (Master control: cycle type decoding) contains the logic necessary to decode not only the various mode signals, but also to assign priorities to these signals. That is, one signal will not be generated until those of higher priority have been processed. This will be discussed in more detail in Section 4.2.

TABLE 3,1

Logic schematic list.

DWG NO.	TITLE	DISCUSSION IN SECTION
171040	Master Control: FCADR Register	3 1 3
171041	Master Control: Front Panel Switches	3.1.7
171042	Master Control: Bank Register	3.1.3
171043	Master Control: No Cycle Timing	3.1.1.3.1.3
171044	Master Control: Write Lines 01-08	3.1.7
171045	Master Control: Write Lines 09-16	3.1.7
171046	Master Control: Event Detector	3.1.3
171047	Master Control: Memory Parity Tree	3.1.8
171048	Master Control: Cycle Request Primaries I	3.1.2
171049	Master Control: Cycle Request Primaries II	3.1.2
171050	Master Control: Cycle Type Decoding	3.1.2
171051	Master Control: Tape V/L Control I	3.1.4
171052	Master Control: Tape V/L Control II	3.1.4
171053	Master Control: Memory Cycle Timing	3.1.1
171054	Master Control: Trace Dump Counter	3.1.6
171055	Master Control: Stop Trace	3.1.6
171056	Master Control: Trace Address Counter	3.1.6
171057	Master Control: Tape Compare Register	3.1.5
171058	Master Control: Tape Commands	3.1.4
1,71059	Master Control: Control Pulses	3.1.3
3.1.3 AGC Modes Control

Various registers are required to process the AGC modes. Drawing 171040 (Master control: FCADR register) contains a 16-bit latching register which stores the fixed complete address from the AGC interface as received. Drawing 171042 (Master control: bank register) contains a 6-bit register with comparison circuitry which determines if the six most significant bits of the AGC address have changed since the previous address or remained the same. This drawing also illustrates a buffer flip-flop which is used to read the trace address. Drawing 171043 (Master control: no cycle timing) contains the buffer gates which accept the signals from the AGC and indicate if the operation to follow will be a true or aborted cycle. In addition, as previously described, a no-cycle timer is also included to generate no cycle-pulses when AGC pulses are not present. Drawing 171046 (Master control: event detector) contains logic to determine if an event has occurred as defined by a combination of various AGC addresses. This will be discussed in more detail in Section 3.3. Drawing 171059 (Master control: control pulses) contains additional gates to perform various logic operations required in the various system modes including AGC modes.

3.1.4 Tape Mode Control

Drawings 171051 and 171052 (Master control: tape V/L control I and II) and Dwg. 171058 (Master control: tape commands) contain most of the logic to implement the logic of Fig. 2.3 (Data flow tape commands) and the state diagram of Fig. 2.4 (Tape mode states).

3.1.5 Tape Compare Register

Refer to Dwg. 171057 (Master control: tape compare register). The tape compare register is a 16-bit latching register which accepts 16 bus lines and stores the information presented on command. The main function of this register is to store and thus to permit comparison of tape data with memory data during the analysis of the tape system performance. The output of this register is displayed on the front panel and serves as a monitor of the data being generated during various modes including AGC modes, which will use this register when tape modes are not in process.

3.1.6 Trace Address and Dump Control

Refer to Dwg. 171056 (Master control: trace address counter). The 14stage trace-address counter is pre-wired to count from 4K to 16K. At the same time the counter is activated, bit 16 of the data bus is set to a 1, which is equivalent to 32K. This means that this counter will always count from 36K to 48K total count as far as the data bus is concerned, which is the address range of the trace section of the core memory subsystem. This function is transferred to the data bus, by either INCTRAD/ or TRAD1/ signals. INCTRAD/ is active in all modes which interrogate the trace memory except for the manual read trace address mode which utilizes the TRAD1/ function. Refer to Dwg. 171054 (Master control: trace dump counter). Note the 14-stage counter which is preset by the RESTRCTR/ signal and generates a CTR 12K signal when stages 13 and 14 are in the one state, a count of 12K. Note also that the INCTRCT signal toggles the first counter stage and generates the counts to be recorded. Note that the first stage switch is an OR function which transfers two signals which are gated by a flip-flop. These signals are PCADR and INCTRAD. A PCADR signal occurs every time a partial complete address of an AGC is recorded. INCTRAD occurs every time a trace cycle of any sort is recorded. This logic will be discussed in further detail when we look at the various mode configurations. Refer to Dwg. 171055 (Master control: stop trace). This consists of comparison logic which compares an input from the front panel with the trace counter and generates a STPTRAS signal when coincidence occurs. This signal is used to transfer the system out of trace mode into other activities a predetermined number of cycles following a restart.

3.1.7 Interface

Refer to Dwg. 171041 (Master control: front panel switches). This logic shows how the signals from the front panel are gated into the master-control data bus. It also shows how data are combined before transfer to the front panel. Refer to Dwg. 171044 (Master control: write lines 01-08) and Dwg. 171045 (Master control: write lines 09-16). These drawings show the 16stage data bus which consists of OR gates which transfer signals from the various signal-generating sources (such as the front-panel signals previously described) to the various internal and external electronics such as the tape interface and core-memory subsystem.

3.1.8 Parity Logic

Refer to Dwg. 171047 (Master control: memory parity tree). This logic is connected to 15 of the write lines previously described and from this information generates odd parity on bit 16. It also is used to detect if a parity error has occurred in data that have already been generated, in this case also noting the state of write line 16.

3.2 Memory Cycle Priorities

Refer to Table 3.2, Memory cycle priority list. Priorities are necessary since two or more mode-operation requests may be presented to the master control at the same time. This priority assignment occurs mainly in the logic of Dwg. 171050, but is also present in the logic of some other sections. Note that priorities 4 to 9 are tape cycles and occur when the tape logic is activated. Note also that all these cycles activate the core memory in either read/restore or clear/write operation except for manual read trace which does not utilize the memory but is still assigned a priority rating. Note that Fig. 3.1 to 3.14 which illustrate the various data-flow configurations for these various modes also show a mode abbreviation and a priority rating which are tabulated on this chart.

3.3 <u>Events Definitions</u>

Refer to Table 3.3, Events definitions. This table lists various sequences which the AGC can generate starting at address 4000 followed by address 4001 to 4007. Each one of these address combinations indicates to the master control that a certain function should be performed. Table 3.3 lists these functions.

3.4 <u>AGC Data Fetch Modes</u>

The following modes are used to retrieve data stored in the Portafam core memory either in the fixed-address portion or the trace portion of the memory.

Refer to Fig. 3.1 which illustrates the data flow in the AGC normal datafetch mode. The following conventions are used in this and subsequent data-flow diagrams. The rectangle is used as an indication of a section of logic which performs a particular function. An example in this drawing is the AGC interface which is actually outside of the Portafam chassis. Signals in or out of this logic are shown with an arrow such as FMA01-16. Signals that gate this logic in or out are shown as perpendicular arrows such as the WFCADR signal which gates the FMA01 to 16 into the FCADR logic. In some cases more than one signal is required to gate logic such as the WTCOMP output which requires three signals to be activated, in addition to its source which is loosely defined as the mode-control logic. OR signal functions such as the sum of NOCYCLE or AGC for WFCADR in Fig. 3.3 are shown as arrows perpendicular to a line. Inhibit functions are shown as slanted intersecting lines. Flip-flops and inverters are illustrated by conventional notation. Signal delays are shown by a D in a square. In some cases, where logic flow is similar in various modes, it may be





Fig. 3.1 Data flow AGC data fetch mode (normal).

TABLE 3.2

Memory cycle priorities list.

PRIORITY	MEMORY MODE	FUNCTIONS PERFORMED	MODE ABBREVIATION
1	R/R	AGC Normal Data Fetch AGC	
1	R/R	AGC Downlink Trace Dump Data Fetch AGC. DLNK	
2	C/W	AGC Bank Change	TRACE
3	C/W	Aborted Cycle, No Cycle, AGC Switched	TRACE
		Fixed, AGC Fixed - Fixed, or AGC	
		Fixed - Fixed with Special Event	
4	R/R	Tape Verify 1	TAPE, TVFY1
5	C/W	Tape Load	TAPE, TLOAD
6	* R/R	Tapĕ Verify 2	TAPE, TVFY2
7	C/W	Verify Fail 1	TAPE, PFAIL1
8	C/W	Verify Fail 2	TAPE, PFAIL2
9	C/W	Verify Fail 3	TAPE, PFAIL3
10	R/R	Trace Dump To Tape	DUMP
11	R/R	Manual Read AGC	MREAD
12	C/W	Manual Load AGC	MLOAD
13	NONE	Manual Read Trace	MTRAD

TABLE 3.3

Events definitions.

EVENT NO	ADDRESS AFTER ADDRESS 4000	ACTION REQUIRED
1	4001	Restart, Verify/ Load Mission Program:
		Freeze and Dump Trace or Load Special
		Program if Unconditional DLNK or Start
		Trace if Unconditional Start, Wait for
		Event 2 or 6 if Conditional
2	4002	Freeze Trace and Load Special Program
3	4003	Load Mission Program
4	4004	Read Trace Memory only if Proceeded by
		Event 2, Event 3
5	4005	Freeze and Dump Trace Memory
6	4006	Start Trace
7	4007	Unassigned

shown in detail in one figure or with a brief shorthand notation in others. Signals such as INCTRAD which are generated in many modes are normally illustrated only as they pertain to the mode under investigation. Note how this is listed in the Fig. 3.2 where the ETC for INCTRAD refers to other modes that are bussed in by the ADDRSG signal.

3.4.1 Normal Data Fetch

Refer again to Fig. 3.1. As described in Section 2.1, the AGC interface first generates a SETOR/ pulse which indicates that an AGC data fetch may be required shortly. Tape cycles are inhibited until receipt of a CLR19/ or STR116/ signal. If the STR116/ pulse appears, data lines 1 to 16 contain the FCADR requested by the AGC. If the CLR19/ pulse is generated however, then only the low-order 9 bits are presented and the AGC has generated an abort cycle. This will be discussed in more detail in Section 3.5.2. Assume, however, that a normal AGC data fetch mode has occurred. Then, as illustrated, the STR116/ pulse sets the AGCP flip-flop which in turn generates additional mode requirements for this data flow. The STR116/ pulse generates the WFCADR/ pulse which gates the FMA into the FCADR (fixed complete address register). Note how the RFCADR pulse links the FCADR data to the data bus which is labeled with a (1). The (1) indicates that the data bus is used more than once in this mode, in this case whenever the ADDRSG pulse is activated. Note that the mode control logic has activated the memory cycle timing which generates this addressgating pulse. This memory-cycle timing also generates RDREST pulse and a CYCREQ pulse which activates the core memory subsystem in the read/restore mode. Note that the MBRO01-16 line address data from the data bus are fed to the memory at this time. See Fig. 2.2 for the timing of these pulses. Thus the core memory has been requested to read outthe data at a particular address. This is accomplished by a RMBR pulse which reads out this data through MBRO01-16 to the data bus at time (2). At TSTPTIM the parity logic checks parity and if even parity is detected stores this information in the PORTPAR flip-flop to be read into bit 14 during the next partial complete address trace mode which will be discussed in Section 4.5.2. These data bus data are then gated by the WTCOMP signal to the tape-compare register which, if the tape mode is not activated and the trace not frozen, will accept and display this data on the front panel. Thus the tape compare register is used to display data in AGC fetch modes. This should prove useful to indicate that the AGC is fetching data normally. Thus, if the data display stops changing



Fig. 3.2 Data flow AGC data fetch mode (downlink trace dump).

it may be assumed that a malfunction has occurred. There is also the parity line signal and a display which is active if a parity error has occurred. Also note that the address display is stored from the first 10 least significant bits of the FCADR and the 6 bits of the bank register which correspond to the 6 most significant bits of the FCADR. Some logic buffering is required as discussed in Section 5.3. Note that the STROBF/ pulse from the AGC interface resets the AGC mode. This is the end of the mode from AGC point of view, and data from Portafam are no longer required. Note also that the data from the data bus (2) also flow as read out by the WAGC signal to the AGC interface along the AGCD01/ to 16/ lines. Thus the AGC interface has received data back from Portafam after generating the appropriate address information.

3.4.2 AGC Downlink-Fetch

Figure 3.2 illustrates the data flow when an AGC data fetch is requested of the trace-memory portion of Portafam rather than the fixed-address portion. The data flow in this mode is identical to the mode previously described except that the memory address information is derived not from the data supplied by the AGC but instead from the trace address counter. Note that the DLNK signal is generated by the event detector as a result of event 4 which, according to Table 3.3, can only occur if preceded by events requiring freeze trace and load special program without a load mission program. This signal generates an INCTRAD pulse which reads out the 14-bit trace address counter to the data bus and sets bit 16 to the one-state during the first portion of the cycle, advancing the counter at the end of the pulse time. The remaining portion of the data flow is identical to that shown in the previous paragraph. The AGCP flip-flop is not shown as a simplification of the logic diagram. The AGC modes described in this and the previous paragraph have been assigned first priority according to Table 3.2. That is, these modes will be processed before other operations are requested of the memory.

3.5 <u>Trace Modes</u>

Trace cycles store AGC address information in the trace portion of Portafam memory. If the trace is enabled (NABTRAS = "1"), information is written into trace memory every AGC memory cycle time. The information stored is:

a. The AGC FMA just accessed - if a normal AGC rope cycle has just occurred.

- b. The nine low-order bits of the AGC's S register if an aborted cycle has just occurred.
- c. A "no cycle" code if no fixed memory activity occurred during the last AGC memory cycle time.

The trace can be enabled (set TRASFF) from three sources:

- a. The "START TRACE" push button (STRTR-0) on the front panel.
- b. Event 6 (detection of the address sequence 04000, xxxxx, 04006).
- c. The front-panel rotary switch labeled "AFTER RESTART" is set to the "LOAD MISSION PROGRAM" position (signal S-TRAS = "1") and a mission program load has just been completed.

The trace can be disabled (reset TRASFF) by:

- a. The "STOP TRACE" pushbutton (STPTR-0) on the front panel
- b. Event 2
- c. Event 5
- After a delay of X AGC memory cycle times following a restart.
 X is determined by the position of the "STOP TRACE CYCLES" front-panel rotary switch.

The trace is temporarily disabled whenever load mission program, load special program or trace dump activity is in progress.

Since sixteen bits are required to completely specify an FMA and only fifteen bits are available for data in the trace memory (the sixteenth bit is parity), two types of trace cycles can be executed - bank change and PCADR.

Figures 3.3 and 3.4 illustrate the data flow during trace cycles. If trace is enabled (NABTRAS = 1), the trace primary flip-flop (TRASP) is set (request a trace cycle) each time data are copied from the FMA lines, coming from the interface electronics, into the FCADR register. Signal WFCFFB is required to write into the FCADR register and is caused by STR116 (the AGC is requesting a normal cycle), CLR19 (the AGC is aborting this fixed-memory cycle), or NOCYCL (generated by the no-cycle timing in Portafam).

If STR116 caused the WFCFFB, an AGC cycle will be performed. During this cycle the 6 high-order bits of the FCADR register are compared to the bank register. If there is disagreement and the current contents of the FCADR register do not correspond to the fixed-fixed portion of AGC memory the PCADFF is reset (PCADFF = 0).



Fig. 3.3 Data flow AGC bank change mode.



A.A.

Fig. 3.4 Data flow trace partial complete address modes.

When the trace cycle is initiated a cycle request (CYCREQ) in the clear/ write mode (RDREST = 0) is sent to the memory subsystem. At ADDRSG time an INCTRAD pulse is generated; this pulse places the contents of the trace-address counter (TRAD01 - TRAD14) onto the data bus and forces bit 16 of the data bus to "1". This causes the address supplied to fall in the range of 110000 - 137777, since the trace address counter counts between 10000 - 37777.

3.5.1 Bank Change Mode

The bank change trace cycle is executed when the six most significant bits of the current FMA differ from the corresponding bits of the last FMA. This is equivalent to changing the FBANK register in the AGC. It should be noted that changing from switched-fixed to fixed-fixed memory in the AGC does not require changing the FBANK register. Likewise , changes in the six most significant bits of the FMA from switched - fixed to fixed - fixed (or aborted or no-cycle codes) are not considered bank changes. The FMA must change from one switched-fixed bank to another switched-fixed bank in order to cause a bank change cycle. See discussion of PCADFF in Section 3.5.7. Figure 3.3 illustrates the data flow during a bank change cycle.

Note that the memory data are read in after the address data are read into the core memory along the same lines (MBRIOL to 16). Note that the leading edge of the NABTRAS signal generates the STTRC signal which sets the bank register to 1 which indicates in storage the last FMA bits 16 - 11 were all 1's. This illegal state is used to indicate initialization of the trace formats.

3.5.2 Partial Address Modes

Figure 3.4 illustrates the data flow for trace memory loading during partial complete address modes. These modes occur when the PCADFF (partial complete address flip-flop) has been set. Note that the bank change resets the PCADFF during the AGC cycle, and the trailing edge of the trace cycle sets it so that when the PCADR is set, a trace cycle for the bank change has already occurred. Thus these partial complete address modes occur one Portafam core memory cycle after the AGC mode has been initiated or two cycles after, if a bank change cycle was processed. The cycle is started with a \overrightarrow{RDREST} (clear/write) mode cycle-request pulse to the core memory. As with the bank change mode, the address is determined from the trace-address counter through

the data bus as processed by the INCTRAD signal. The DATAOUTG signal then gates bits 1 to 10 of the FCADR to the ten corresponding data bus lines. Bit 10 becomes a one if this is a no-cycle format (bits 01-09 of FCADR are zero); bit 11 is set to one if this turns out to be a switched-fixed address; bit 13 is set to a one if an event as determined by the event detector has occurred; bit 14 is set to one if there was a Portafam parity failure during the previous AGC data-fetch cycle. The AGC cycles utilize the Portafam core memory in the read/restore mode; trace cycles utilize the clear/write mode. Parity errors can occur only during read/restore cycles but can only be recorded in a clear/write cycle to follow. In all modes, bit 16 is determined by parity, generated in C/W cycles, and measured in R/R cycles. As tabulated in Fig. 3.4, bits 10-15 identify the type of cycle. Note the octal identifier code which is determined from the binary bits listed. The other possible combinations of bits 10-15 not covered in Fig. 3.4 are identifier codes 10-13 and 60-67 which are unused; a combination of special event and a parity failure which is identified by code 37; identifier codes 40-47 which cover verify-fail formats used in tape cycles; and the bank constant format discussed in Section 3.5.1 which is 50 to 57.

3.6 Tape Modes

The tape control logic is operated in various mode sequences by the master control logic.

3.6.1 Command Logic

Figure 2.3 (Data flow tape commands) illustrates the various data flows that occur when the tape-control unit is instructed to load mission program, load special program or receive information dumped into it from the Portafam trace memory. Each one of these modes may be requested in one of three ways. The mode may be initiated by a detection of an AGC event as defined in Table 3.3; it may occur during a restart procedure which would enter into the mode either automatically or through a manual override instruction; or it may be initiated by a direct manual instruction from the front panel. The load mission program flip-flop is set either by an EVENT3/ signal which is a load mission program request from the AGC event detector, EVNT1D/ which is a restart procedure, or LDMPG-0/ which is load mission program request manually entered from the front panel. These signals will set the load mission program flip-flop if the RDYALTP/ (tape is ready at the load point) signal is received from the tape-control logic. Similarly the load special program flip-flop will be set either by an EVENT2/ signal from the event detector, a S-DLNK-0/

restart front-panel signal if gated in by the EVNT1D/ signal or by LDSPG-0/ which is a manual load special program request. As before these signals must be gated in by the RDYALTP/ signal. The dump trace flip-flop is set by either the EVENT5/ signal from the event detector, the EVNT1D/ signal after restart or the manual DMPTR-0/ signal from the front panel. These signals do not require a tape ready at the load-point signal since other logic initiates this dumping as described later. Note that during a restart procedure the mission program is first loaded and then the trace memory is dumped onto tape. Load mission program is a tape mode while the dump trace procedure is a dump mode, and the trace cycles are of higher priority than the dump cycle (Table 3.2). The data flow during load mission program proceeds as follows. After the LDMPFFB flip-flop is set as previously described, the buffered output of this flip-flop is fed to the tape control logic as CLDMSPG/. This signal in tape-control logic generates a T2MREQ/ signal which sets the tape mode flip-flop as it requests acceptance of the tape of the register word in the fixed-memory location specified by the tape-address register. Portafam then goes into the various tape modes as illustrated in Fig. 2.4, which are to be described in more detail later. The only time that the trace memory records any information is in the various PFAIL modes which are activated if errors are detected. At the completion of the mission program load the tape-control logic generates an EMPL/ signal which indicates that the mission-program loading is finished, resets the load mission program flip-flop, and gates the S-TRAS/ signal from the front panel to set the start trace flip-flop. LDSPFFB cannot be set unless RDYATLP = 1. Since EMPL cannot occur if you are at the load point, the trace memory will be dumped if requested before the tape is rewound to the load point. When the load point is reached, the tape logic will then begin the load special program sequence. We are now ready to dump the contents of Portafam trace memory to the tape unit. Let us assume that the dump trace flip-flop has been set by the signals previously described. When the DMPTRFF signal is true, a CDMPTRC/ signal to the tape-control logic indicates + that tape data will be forthcoming shortly. The tape-control logic in turn generates an M2TREQ/ pulse which requests transfer of the trace memory words specified by the trace-memory address register to the tapebuffer register setting the dump trace flip-flop in the process. Then as shown in Fig. 2.3, the Portafam core memory is read out with an INCTRAD signal generated every cycle. Assuming the trace dump counter input flip-flop has been previously set to the proper state by the STPRAS signal, the dump trace counter will count every cycle until the counter logic sends a CTR12K / pulse to the tape-control logic. This indicates that 12,288

cycles have occurred since the start of the trace dump and the full trace information is on the tape. The load special program flip-flop is set in the the manner previously described, provided the load mission program flipflop is not set, and generates the CLDSPPG/ signal to the tape-control logic which requests the loading of the special program which may be stored on the same tape as the mission program, appearing after an indicator mark which permits the tape-control logic to detect the special program tape location. As previously, the T2MREQ signal is generated and the previously described procedure for the mission program is followed. As before, the tape-control logic generates an ESPL/ signal which indicates the special program load is finished and resets the load special program flip-flop. Restart may also initiate the above modes. The start trace flip-flop is set either by an EVENT6/ signal from the event detector, a STRTR-0/ start trace signal from the front panel or a S-TRAS/ load mission program after restart signal from the front panel which is gated by EVNT1FF signal and the EMPL/ signal. This starttrace signal will generate a NABTRAS signal provided that the logic is not either loading or dumping the trace. NABTRAS permits transfer from the AGC to trace cycles. In addition the EVENT1/ signal from the event detector will reset the trace dump counter and set the input flip-flop to the trace dump counter to the state which will permit recording of PCADR signals by the trace dump counter. These PCADR signals will be counted until a coincidence occurs between the trace dump counter and stop-trace logic. This coincidence is determined by the S-(x)WDS/ signal which is established at the front panel. This signal determines how many cycles delay before STPRTAS is generated by the stop trace logic. STPRTAS tells how many trace (clear/write memory cycles) are written over the old trace data. This signal also initiates a resetting of the load mission program through the EVENT1 flip-flop which in turn loads the mission program into the 36K bits reserved for fixed-memory simulation. Conclusion of the load mission program mode as previously described then permits the dump trace cycle to occur as before. Thus the trace memory is overwritten by the number of trace cycles perdetermined by the switch on the front panel, then dumps 12K bits to the tape, mostly information that occurred before the restart event. These data may then be analyzed in an external computer if required.

3.6.2 Parity Check and Tape Verify 1 Modes

Refer to Fig. 3.5 (Data flow check parity of tape data mode to tape verify 1 mode). As described in the previous section, the tape mode flip-flop





is met by a T2MREQ/ pulse from the tape-control logic. The setting of the TAPEP flip-flop is indicated to the tape control logic by the TREQRST/ line fed back to the tape-control logic. The TAPEP signal performs two immediate functions. It resets the tape mode control register to the \overline{ABC} state and initiates the tape signal from the mode control logic. The tape signal gates \overline{ABC} state of the tape mode control register through to the tape control logic the RTAPBF/ signal which places the data in the tape buffer register on the RL01TB-16TB lines. This data word is transferred to the data bus and from there to the parity logic where a PAR signal is generated into goodword logic. In the goodword logic the UNUSED signal from the tape-control logic is compared with PAR and GOODWRD is generated, the exclusive OR of UNUSED and PAR. The UNUSED signal indicates that the current word in the tape-buffer register is associated with an unused fixed-memory location and will therefore fail odd parity since all zeros are even parity. Thus a good word is exclusively either good parity or an unused word from the tape buffer. As shown in the tape mode state diagram of Fig. 2.4, the generation of GOODWRD changes the tape mode control register from \overline{ABC} to $A\overline{BC}$, or into the TVFY1 (tape verify 1) mode. A good word failure sets the tape mode control register into the PFAIL1 mode, which is to be discussed later. The data flow during the TVFY1 is as follows. Memory-cycle timing is activated, and a CYCREQ pulse with a RDREST signal is sent to the core memory. The ADDRSG strobe activates the RTAPAD/ signal to the tape-control logic which reads the tape-address register onto RL01TA-16TA. The core memory is therefore addressed to the address specified by the tape unit and reads out data at RMBR time back to the data bus. This data information is then strobed by the TSTPTIM signal to the tape-compare register which in turn displays the data on the front panel. If the TBFNEWL signal from the tape-control logic is in the zero state, the tape buffer register is equal to the Portafam data lines, and a proper load has occurred. The combination of TBFNEWL/, TVFY1, and CYLEND from the memory timing establishes the RSTAPEP signal which resets TAPEP and steers the Portafam logic out of TVFY/ and back to the CKTPAR state. If, however, the TBFNEWL is in the true state, then the tape-buffer register is not equal to the write lines and the logic proceeds along one of two paths. If the Pxx line from the tape-control logic is true this indicates that the bank presently being loaded has completed at least one pass without any tape reading errors, and therefore errors are not due to the fact that the system has not been loaded. If, however, the Pxx signal is zero, then the errors that occur will most likely be because the system has not been loaded and the TLOAD mode is established. The TLOAD mode will be discussed in Section 3.6.3 and the PFAIL1 mode in Section 3.6.5. Note how the TVFY1 mode signal is strobed back to the

tape-control logic at CYLEND time as VERFAL1/ which indicates that TBFNEWL is still true at the end of the cycle. Note also the logic condition under which the parity alarm on the front panel is set. There are two tape-verify modes, the second type is discussed in Section 3.6.4. When Portafam is not in one of these tape-verify modes, then the parity light will be lit if a parity failure occurs during a read/restore cycle. If it is in a tapeverify mode then the parity light will be lit if the parity failure is detected and GOODWRD is zero. Note that a good word situation must occur before entering the tape-verify modes. This logic blocks TVFY from the parity error indication in a good word situation which can indicate that parity is zero because the word is unused. This means that the parity error light will only be lit when a true parity error has occurred, which can happen in a TVFY mode if GOODWRD has returned to zero after the modes were established.

3.6.3 Tape Load Mode

Refer to Fig. 3.6 (Data flow tape load mode). As previously described this mode is entered when, after the tape mode control register is in the TVFY1 mode, a TBFNEWL one signal and Pxx zero signal are received from the tape-control logic. After entering the tape-load mode, the memory cycle timing initiates a CYCREQ pulse and a RDREST/ signal to the core memory. It strobes the tape address register data onto the data bus by generating RTAPAD/ at ADDRSG time to establish the proper core address and reads the tape buffer with RTAPBUF/ at DATOUTG time to establish the tape-buffer data on the data bus so that these data may be written into the core memory at the address specified.

3.6.4 Tape Verify 2 Mode

Refer to Fig. 3.7 (Data flow tape verify 2 mode). In this mode the data flow read restores the memory and compares the tape data buffer with the data bus (WL01-16). If this comparison fails it is then known that the trouble is in the core memory and the memory data are copied into the tape compare register. This procedure is accomplished in the following manner. The memory-cycle timing generates a CYCREQ pulse and RDREST mode signal to the core memory. An RTAPAD/ signal generated at ADDRSG time reads the tape-address register onto data bus lines RL01TA - RL16TA. The memory-buffer register is readout to the data bus with the RMBR signal where the data are fed back to the tape control logic which determines if the tape-word buffer register is unequal to WL01-16. This test deter-



Fig. 3.6 Data flow tape load mode.



Fig. 3.7 Data flow tape verify 2 mode.

mines the TBFNEWL signal level which is fed back to Portafam to generate the VERFAL2/ signal. VERFAL2/ at TSTPTIM becomes WTCOMP which writes the data bus contents into the tape-compare register for future analysis.

3.6.5 Verify Fail 1 Mode

Refer to Fig. 3.8 (Data flow verify fail mode from tape verify 2 mode). The entrance into the tape verify fail 1 mode from the check-parity mode is illustrated in Fig. 3.5, and the entry from the tape verify 1 mode is illustrated in Fig. 3.6. This mode is used as a means of recording previous data for analysis. Tape address register bits 11 - 16 are written on write lines 1 to 6. Strobing TCOMP16 of the tape-compare register on write line 7, and a status word on write lines 8 to 12 explaining the reason for the failure. In addition the strobe pulse (RTVCODE) is written into line 15 as a cycle indicator. This generates the verify-fail code mentioned in Section 3.5.2. The data flow to accomplish this is as follows. The finish of the TVFY2 mode automatically sets the tapecontrol register to the PFAIL 1 mode. Note that the two other possibilities for entering this mode depend on external conditions to enter from the other states. The data flow begins with a CYCREQ pulse and RDREST/ mode level from the memory-cycle timing to the core memory. During ADDRSG time the INCTRAD signal is generated which reads the traceaddress counter onto the data bus as described in other modes which use this counter for the address source. The data bus then generates a trace address to the core memory. At DATOUTG time RTVCODE is generated which strobes bits 11 - 16 of the tape-address register to data bus lines 1 to 6. Bit 7 comes from bit 16 of the tape-compare register which records the parity bit of the last time this register was loaded. Bit 8 records the state of the VFAL1FF flip-flop. This flip-flop is set during an earlier TVFY1 mode and reset by TPCKDN which occurs during the CKTPAR mode, which may or may not have occurred earlier than TVFY1. Thus this bit indicates if PFAIL1 was entered into from either CKTPAR or TVFY2 route. Bit 9 records the state of the VFAL2FF flip-flop and is set by the VERFAL2 signal which occurs during the TVFY2 mode, reset by the TPCKDN signal of CKTPAR mode. Thus the combination of bits 8 and 9 indicates from which mode the TFAIL1 mode was derived. The PFALFF flip-flop which generates the data for bit 10 is set by the GOODWRD signal and reset by the later PFAIL3 logic. This will tell us if GOODWRD has been generated during the CKTPAR cycle. Bit 11 is strobed in from the tape-control logic and is determined by the



Fig. 3.8 Data flow verify fail 1 mode from tape verify 2 mode.

state of the Pxx line. Bit 12 comes from the event detector and is determined by the state of EVNT1FF flip-flop which is set by the restart operation. Bit 15 is the RTV code itself and is used as a marker with bits 13 and 14 always zero. In all clear/write cycles, bit 16 is determined by the parity logic.

3.6.6 Verify Fail 2 Mode

Refer to Fig. 3.9 (Data flow verify fail 2 mode). This mode is entered into automatically at the completion of the verify fail 1 mode discussed in the previous section. In this mode bits 1 to 12 of the tape-address register are written into the trace memory. In PFAIL1 mode bits 11 to 16 of the address were recorded corresponding to the bank register portion of an AGC FMA. In this mode bits 1 to 12, which correspond to the PCADR of the AGC address, are recorded. In addition bit 14 is activated if GOODWRD/ was present during a previous tape-verify-mode cycle. Since the tape-verify mode will be entered if GOODWRD originally was present then GOODWRD/ during a tape-verify mode indicates parity failure during a tape-verify mode. These functions are accomplished by an initiation of a CYCREQ with RDREST/ signal from the memory-cycle timing to the core memory. As previously the address of the core memory is determined by the trace address counter. The PFAIL2 state of the tape mode control register is initiated by the CYLEND pulse at the end of the PFAIL1 analyzed. The PFAIL2 signal then generates RTPAD12/ at DATOUTG time which is fed back to the tape-control logic and instructs the logic to read the 12 bits of the tape-address register onto lines 01 - 12 of the data bus. The TVFYPAR flip-flop is set if, as previously described, GOODWRD/ and TVFY signals are coincidently present. TVFYPAR is strobed to the data bus bit 14 by the DATOUTG signal of the memory-cycle timing, as is the RTPAD12/ signal. Also at DATOUTG time the parity logic is activated to generate the correct parity bit for the information written into the core memory.

3.6.7 Verify Fail 3 Mode

Refer to Fig. 3.10 (Data flow verify fail 3 mode). Like the verify fail 2 mode, verify fail 3 (PFAIL3) automatically follows from the previous verify fail 2 mode. In this mode the contents of the tape compare register are written into the trace memory at the address following that used for the PFAIL2 mode. The first 15 bits plus parity are the contents of the fixed-memory address for the tape word stored if it were stored at all. Note that in the tape verify 2 mode, the tape-compare register is loaded with the core memory information if the tape word is unequal to



Fig. 3.9 Data flow verify fail 2 mode.



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Fig. 3.10 Data flow verify fail 3 mode.

the memory word after tape word was stored (VERFAL2/). The implementation of PFAIL3 is accomplished by a CYCREQ pulse and RDREST/ signal from the memory-cycle timing to the core memory. As previously described the address for this core memory is taken from the trace-address counter. The data bits 1 to 15 are generated from the tape-compare register at DATOUTG time with the bit 16 parity bit also generated at this time. The tape-compare register date as previously mentioned are displayed on the front panel. At the completion of the PFAIL3 mode, the combination of PFAIL3 and CYLEND pulses generate a PFLSEND/ signal which resets the tape-mode control register to the ABC state or CKTPAR state ready for the next tape command and also resets the TAPEP flip-flop back to the zero state to end the tape modes.

3.6.8 Trace Dump to Tape Modes

Refer to Fig. 3.11 (Data flow trace dump to tape mode). In this mode which is initiated as described in Section 3.6.1, the information in the trace portion of the Portafam core memory is transfered to the tape recorder. As is illustrated in Fig. 2.3, the mode is initiated by the M2TREQ/ signal and continues for 12,288 cycles which is the complete trace-memory capacity. In Fig. 3.11 the M2TREQ/ pulse is shown setting the DUMPP flip-flop. This sets the mode-control logic to the dump mode which institutes a CYCREQ pulse to the core memory with a RDREST mode level signal. The address data are read from the trace address counter at ADDRSG time and then the RMBR signal is sent to the core memory which transfers the MBR data to the data bus. After generation on the write lines it is written into the tape-control logic-buffer register during TSTPTIM time by the WTAPBUF/ signal which permits transfer of WL01-16 into the tape buffer lines 1 to 16. At this time also the DUMPP flip-flop is reset to wait the next M2TREQ/ pulse from the tape-control logic. The tape-compare register will also accept the data bus lines provided that the REL DISPLAY button is pushed on the front panel to strobe this data in. The release-display signal is necessary in order to view a line: otherwise the display would change rapidly so that it would be impractical to read. Note also that the parity alarm signal may be generated during this mode as with all read/restore operations.

3.7 Manual Modes

All the modes that Portafam may perform without direct intervention by the operator through the front panel have now been analyzed. Some of these modes may be initiated by the operator in addition to the automatic method of implementing these operations. The following sections look at the various operations which may only be initiated by operator control.



Fig. 3.11 Data flow trace dump to tape mode.

3.7.1 Manual Read Mode

Refer to Fig. 3.12 (Data flow manual read mode). This mode is used to manually read the memory information at an address specified by thumb-wheel positions on the front panel. Fig. 3.12 shows the data flow to accomplish this objective. The mode is initiated by depressing the MANUAL READ MEMORY button on the front panel which sends an MREAD-0/ signal to the MREADP flip-flop. This establishes the MREAD mode in the mode-control logic which in turn resets the MREADP flip-flop. The mode information is stored in the cycle type flip-flops until completion of the manual read operations. The memory cycle is initiated with CYCREQ pulse and RDREST mode level to the core memory. The address information is the data preset by the address thumb-wheels on the front panel and strobed through the data bys by the RPNLADR signal at ADDRSG time. The bit data in the memory buffer register are then readout to the data bus by the RMBR signal. The data bus data are then written into the tape-compare register by the WTCOMP signal at TSTPTIM time. The parity logic detects parity errors if they occur and records this on the front panel. Note also that the freeze display flip-flop which serves to block AGC and DUMP mode actions from disturbing the tape compare register, is set by the RPNLADR signal. This flip-flop does not, however, block further manual read modes but only serves to prevent other automatic modes from interfering with the display. It may be reset by the release-display signal from the front panel. Note that the tapecompare register data are displayed on the front panel.

3.7.2 Manual Load Mode

Refer to Fig. 3.13 (Data flow manual load mode). This mode is used to manually load the Portafam core memory. It should prove useful if malfunctions are suspected in the core memory since this mode permits testing of the core memory manually. Analysis is combined with the manual-read mode just described. Figure 3.13 illustrates the data flow to accomplish the load operation. The mode is initiated by pressing the MANUAL LOAD MEMORY button on the front panel which sends the MLOAD-0/ signal to the MLOADP flip-flop. This flip-flop initiates MLOAD in the mode-control logic which in turn resets the MLOAD flipflop. The memory timing is initiated and sends the cycle-request pulse combined with a clear/write mode level to the core memory. As before the address data are determined by the thumb-wheel positions on the front panel, and the RPNLADR signal strobes these data onto the data



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Fig. 3.12 Data flow manual read mode.



Fig. 3.13 Data flow manual load mode.

bus where they are in turn transferred to the core memory. As before, the freeze-display flip-flop is set by this signal. At DATOUTG time the bit data are transferred from the front-panel manual data switches through the data bus to the core memory, with a parity bit generated by the parity logic. At TSTPTIM time WTCOMP transfers the data line signals to the tape-compare register from which they are displayed on the front panel. Since the memory buffer register is not enabled, the tape-compare register will display all zeroes because no register is being read. To check if the memory has loaded correctly, follow with a manual read mode (Section 3.7.1).

3.7.3 Manual Read Trace Address Mode

Refer to Fig. 3.14 (Data flow manual read trace address mode). The purpose of this mode is to interrogate the trace address counter and determine at what address the counter is established. This mode is initiated by depressing the READ TRACE ADDR button on the front panel. This generates an M-TRAD-0/ signal which sets the MTRADP flip-flop. As before the MTRAD mode is established in the mode-control logic which in turn resets the MTRADP flip-flop. As before, the cycle-type flipflops in the mode-control logic store this information until the cycle is completed. The MTRAD signal also sets the TRAD1 flip-flop which, in turn, sets the freeze-display flip-flop. The TRAD1 also transfers the address-counter outputs to bits 14 to 1 of the data bus and generates a one in bit 16 of the data bus, similar to the function of the INCTRAD signal. Simultaneous to this transfer, WTCOMP transfers the data bus outputs into the tape-compare register from where they are displayed on the front panel. Note that the trace address is displayed in the data-display section of the front panel and also that bit 16 which is the parity bit is indicated by the parity light. The data display shows five octal numbers (15 binary figures), and the sixteenth figure corresponds to the parity bit. Note since bit 15 is always zero, the highest value of the most significant octal display is three. Note also that since the address of the first trace location is octal 10,000, then the most significant display has the value 1, 2, or 3 only. Any other value for this display indicates a malfunction in the system.



Fig. 3.14 Data flow manual read trace address mode.

CHAPTER 4

FRONT PANEL OPERATION

Drawing 166565 (Portafam assembly) shows the complete assembly of the Portafam chassis including the front panel with labels on the various switches and push buttons.

4.1 <u>Cable Connections</u>

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Drawing 171011 (Schematic display panel) shows all the wiring from tray A to the front panel switches and thumb wheels. It does not show the connections to the connectors labeled TAPE, AGC, POWER, and TEST. These connections are listed in assembly Dwg. 171030 to 171033 respectively. These documents and the logic drawings referred to in Section 3.1 contain most of the information required for tracing this system. Various analysis procedures useful in utilizing this system will be discussed briefly, since the descriptions of the various modeoperations presented most of this information.

4.2 Automatic Procedure

As previously emphasized all of the modes discussed except those described in Section 3. 7 may be initiated without the requirement of operator control by programing the proper events definitions as illustrated in Table 3. 3. Thus automatic checkout procedures may be initiated with the proper programing. The load special-program operation may aid in the implementation of these procedures.

4.3 Manual Procedure

The various switches, dials, and displays on the front panel perform the following functions. The two groups of seven-segment decoders along the top of the panel are used to display address and data information which is obtained from various sources. In most modes this information is obtained directly from the core-memory address and data

registers. In the read trace address mode which is initiated by the READ TRACE ADDR button, the data display displays the trace address counter address as explained in more detail in Section 3.7.3. The MANUAL LOAD MEMORY button initiates the manual-load cycle; the MANUAL READ MEMORY button initiates the manual-read memorycycle mode, and the REL DISPLAY button releases the display registers so that new information may be presented in the data-display portion. The two sets of thumb wheels located to the left and right of these switches are used to set up manual address and data information to be loaded into the memory. The LOAD MP/ACTIVE switch indicates that mission program is being loaded by the tape transport. The LOAD SP/ ACTIVE switch indicates that the special program is being loaded by the tape unit. The DUMP TRACE/ACTIVE pushbutton indicates that the information in the trace memory is being dumped to the tape unit. The PORTAFAM PARITY ERROR switch indicates that a parity error has occurred and also may be used to reset the error flip-flop. The PARITY BIT light indicates the state of the sixteenth bit of data (parity bit), since the five octal data displays do not fully cover the 16 bits of a word. The START/TRACING switch is used to initiate the trace memory and when lit also indicates that the trace memory is operative. The FREEZE TRACE switch is used to stop the trace memory from operating.

The switches over the TAPE CONTROL label are utilized as follows for controlling the tape unit. When power is first supplied to the tape unit, it enters the automatic mode and automatically rewinds. During this time the REWIND light is lit. When the tape is at the load point, the READY light goes on. Before this time the REWIND light is lit, the unit is not ready and is proceeding to the load point and alignment. When the tape unit is at the load-point and ready, that is, the READY light is lit, depressing the STOP/MANUAL pushbutton lights the MAN-UAL light, and the READY light is off. Depressing the START/READY button keeps the tape unit in the ready position and the READY light remains lit. Depressing the LOAD/REWIND button does nothing since the unit is already at the load point. When the FILE PROTECT light is lit, this means that the file-protect ring in the tape is not installed, the file is protected, and no writing can occur. In order to write the fileprotect ring must be inserted in the tape spool.

The EOT light indicates that the tape is at or beyond the EOT mark. This can only occur during a write operation, since any read operation will be terminated at the EOT marker. There is no danger of writing

off the end of the tape since an entire Trace Dump will not use up the extra four feet (plus a ten-foot leader) of tape beyond the EOT marker. If a write operation has taken the unit past the EOT marker, no further write operations will be permitted by the system until a new reel of tape is installed (The system finds the EOT marker before it finds any blank tape.). The NO TAPE light indicates that there is no tape in the machine. If the unit is not at the load point and ready this means the system is in operation. Depressing the STOP/MANUAL pushbutton at this point causes the tape unit to stop, and a tape error light of some type will appear depending on which mode the system was operating at the time this button was depressed. Depressing the START/READY button at this time will have no effect since the unit is in the manual mode. Depressing the LOAD/REWIND button will cause the unit to start to rewind.

Seven tape error lights are shown: VRC ERROR/LRC ERROR, WORD ERROR/VERIFY FAIL, MP FAIL/SP FAIL, and TRACE DUMP ERROR. These are located on four light buttons above the TAPE ERRORS label on the front panel. Some of these lights will be reset automatically when various modes are requested, and/or may also be reset by the ERROR RESET pushbutton. If any of the error lights are lit, the ERROR RESET button will also be lit.

Two convenience pushbuttons are also supplied in this panel. These are the LAMP TEST button which turns on all the lights in the system including the seven segment displays setting these all to the number eight (8). The ILLUM PANEL button turns off the light bus so that the lights that are normally always on may be turned off, and just lights that are activated by various signals are shown. The STOP TRACE Cycles After Restart switch determines how many cycles of trace information will occur after restarting and before proceeding to the dumping of the trace memory. The AFTER RESTART switch determines what the system will do after the restart procedure; either LOAD MISSION PROGRAM, LOAD SPECIAL PROGRAM, or some function as determined by the OPERATOR CONTROL.

4.4 Display Interpretation

Figure 4.1 (Display connections) illustrates the sources of the address and data-display light information and also the destination of the address and data thumb wheels. Note that the address display consists of six octal displays which is 18 binary bits to display a 16 binary bit fixed-



Fig. 4.1 Display connections.
memory address. Note that fixed-memory address bits 1 to 10 are directed directly to display least significant bits. Note that the bits 11 to 16 of the fixed complete address are coupled directly to the most significant bits of the display through the bank register. Bit 11 of the fixed-memory address is also connected through logic to the eleventh least significant bit of the display and also directly to the least significant bank bit. Note that the twelfth most significant bit of the display is a one when the fixed-complete-address bits 16 to 13 are zero, and bit 12 is a one. This expansion of information is reversed when going from the six octal thumb wheels of 18 binary bits down to the 16 address in lines through the data bus. The address in bit 11 corresponds to (BANK 1)(ADDRESS 12) + (ADDRESS 11)(ADDRESS 12). If address 12 is a one then bit 11 will always be a function of the address 11 thumb wheel. If address 12 is zero, however, then bits 11 and 12 will always be a function of the bank 1 and bank 2 thumb wheel functions. The data display is less complicated in that 15 bits of TCOMP register are coupled directly to the displays with the sixteenth bit being indicated by the parity display function. When writing in the 5 thumb wheels for data go directly into the 15 lines of the data bus. Remember that during clear/write modes the sixteenth bit is always parity.

CHAPTER 5

FURTHER REFERENCES

In addition to the drawings and articles cited, a detailed description of other areas of this system is available in the various Portafam monthly progress reports. Especially useful may be the report of 11 June 1968, AG254-68. This article has sections entitled AGC-Portafam Interface (Operational Description); Portafam Erasable Memory System; Portafam Magnetic Tape Recorder, Reproducer; Magnetic Tape Organization and Recording Format; and Portafam Memory Word Formats. In addition Digital Development Memos 219 and 239 should prove useful in analysis of the rope memory and interface. Any reports on the Apollo Guidance Computer itself should also prove useful.

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