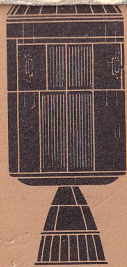


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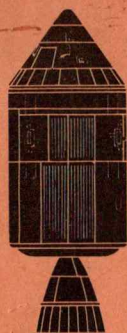
TELECOMMUNICATION
SYSTEMS
STUDY GUIDE
COURSE NUMBER A-624

FOR TRAINING PURPOSES ONLY

OCTOBER 1, 1965



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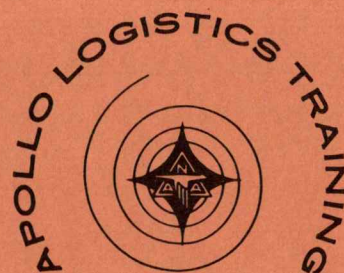


APOLLO TRAINING

TELECOMMUNICATION
SYSTEMS
STUDY GUIDE
COURSE NUMBER A-624

FOR TRAINING PURPOSES ONLY

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Preface

This study guide was prepared to augment the oral presentation of the Communication Systems courses.

The guide is organized to correspond to the instructor's procedure in presenting the concept of the system's operation and mechanization. This text arrangement affords the user the advantage of review, with printed material. Consequently, the format contributes directly to recall memory and is therefore conducive to prolonged retention, and increased course efficiency.

The study guide enhances the course and facilitates further learning by providing the physical convenience of having immediately before the user the same illustrations and documentation in the form of graphs, charts, and tables that are being explained by the instructor. The necessity for making notes is minimized as is the possibility of missing portions of the explanation because of difficulty in distinguishing distant visual aids.

The information in the study guide is accurate as of the publication date. This document is intended for training purposes only and is not subject to scheduled revision.

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SECTION I

INTRODUCTION

The Communications System is the only link between the spacecraft and the Manned Space Flight Network (MSFN). In this capacity the Communications System provides the MSFN flight controllers with data through the Pulse Code Modulated (PCM) Telemetry System for monitoring Spacecraft parameters, subsystem status, crew bio-medical data, event occurrence, and scientific data. As a voice link the Communications System gives the crew the added capability of comparing and evaluating data with MSFN computations. The Communications System, through its MSFN link, serves as a complete backup to the Guidance and Navigation (G&N) System for determination of Spacecraft attitude, position in space, and rate of change in position. Through the use of the Television Camera, vital crew observations and public information can be transmitted in real time to MSFN. A means by which data can be stored in the Spacecraft to avoid loss because of an interrupted communications link is provided by the Communications System in the form of the Data Storage System. Aids are provided for tracking the Spacecraft in a near earth condition, for trajectory and orbit analysis. Direction finding aids are provided for post landing location and rescue by ground personnel.

1.1 GENERAL

The communications System provides the following basic functions:

1. Voice Communication

- a. Within the spacecraft between astronauts

- b. From the spacecraft to and from the MSFN
- c. From the spacecraft to and from the LEM (Lunar Excursion Module)
- d. From the spacecraft to and from an extra vehicular astronaut (EVA)
- e. From the spacecraft to and from recovery aircraft and ships.

2. Data Transmission

- a. Of spacecraft systems and astronaut status to the MSFN
- b. Of extra vehicular astronaut status by relaying to the MSFN
- c. Of real time video pictures taken from inside the C/M to the MSFN

3. Up Data Reception

- a. From the MSFN to update the (Command Module) time reference
- b. From the MSFN to the C/M Guidance & Navigation System to update or provide basic navigational data.
- c. From the MSFN to the C/M systems to perform 64 real time commands

4. Tracking Information

- a. Through the JPL Pseudo Random Noise Ranging technique for a precise and fast distance measurement
- b. Through the Double Doppler tracking for an accurate radial velocity measurement
- c. Through a conventional radar transponder during near earth operations

5. Beacon Transmission

- a. At HF frequencies from C/M to recovery forces beyond line of sight after splash down
- b. At VHF frequency from C/M to recovery forces at line of sight distances after main chute deployment

1.2 SYSTEM FUNCTION/SYSTEM COMPONENT/MISSION PHASE

Figure 1-1 is a matrix showing what component of the telecommunication system is performing the designated function during the particular mission phase.

1.2.1 Pre-Launch

During the pre-launch phase of the mission voice, data, up-data, TV, and bio-med communications are handled by hardline. Tracking and Beacon functions are naturally not needed during this phase.

1.2.2 Launch, Earth Orbit, and Lunar Injection

During this near earth phase the VHF/AM transceiver will be the prime mode for voice communication. The Unified S-Band Equipment, (USBE) would serve as backup.

Data would be transmitted to the MSFN by the VHF/FM transmitter with the S-Band acting again as backup.

The Up Data information from the MSFN would be received on the UHF/FM receiver during this near earth phase with S-Band acting as backup.

Tracking would be facilitated by the C-Band transponder with S-Band acting as backup.

Any TV transmission would be limited to only those times the CSM was over an S-Band tracking station since the video information can only be transmitted via the USBE.

1.2.3 Trans Lunar and Trans Earth

The Unified S-Band Equipment, (USBE), will now be responsible for handling all communications between the spacecraft and the MSFN. Any extra vehicular astronauts or astronauts in the LEM would communicate with the C/M via the VHF/AM transceiver. Biomedical information would also be transmitted by this means. The C/M could then relay the voice or biomed information to the MSFN via the USBE.

1.2.4 Lunar Orbiting LEM Descent, Lunar Explore LEM Ascent

As in the trans lunar and trans earth mission phases, the Unified S-Band Equipment, (USBE) carries the responsibility of providing the communications link to the Manned Space Flight

COMM EQUIPMENT / MISSION PHASE

1

	PRE - LAUNCH	LAUNCH EARTH ORBIT LUNAR INJECT.	TRANS- LUNAR FLIGHT >4000 MI.	LUNAR ORBIT	LEM DESCENT LUNAR EXPLORE LEM ASCENT	EARTH INJECT TRANS EARTH FLIGHT	LANDING RECOVERY
VOICE	HARDLINE VHF/AM*	VHF/AM S-BAND*	S-BAND	S-BAND	S-BAND VHF/AM+	S-BAND	HF VHF/AM*
TV	HARDLINE	S-BAND	S-BAND	S-BAND	S-BAND	S-BAND	
BIO MED	HARD LINE VHF/FM*	VHF/FM S-BAND	S-BAND VHF/AM+	S-BAND	S-BAND VHF/AM+	S-BAND	
UP-DATA	HARD LINE UHF/FM*	UHF/FM S-BAND	S-BAND	S-BAND	S-BAND	S-BAND	
DWN- DATA	HARD LINE VHF/FM*	VHF/FM S-BAND*	S-BAND	S-BAND	S-BAND	S-BAND	
RANGING		C-BAND S-BAND*	S-BAND	S-BAND	S-BAND	S-BAND	
BEACON							HF VHF-BCN*

* BACKUP MODE

+ LEM-E. V. A. COMMUNICATIONS

figure 1-1

Network, (MFSN). Voice and Biomed information from the LEM astronauts or an extra vehicular astronaut, (EVA), is received via the VHF/AM receiver in the C/M and then can be relayed to earth using the USBE. The LEM telecommunications system will allow it to communicate directly to the MFSN via S-Band and also perform the relaying of EVA information.

1.2.5 Landing and Recovery

After reentry and landing, the telecommunications system will be providing two prime functions, voice communications and beacon. The HF transceiver will be the prime unit in providing these functions due to its beyond line of sight operational capabilities. The VHF/AM will be a backup for voice communications and the VHF/BCN will be backup for the HF Beacon.

1.2.6 Summary

Since the inter relationships between mission phase, function to be performed, and component is some what confusing a matrix, figure 1-1, is provided as a quick reference.

1.3 EQUIPMENT LOCATION

The telecommunications system equipment is mainly clustered in the lower equipment bay as shown in figure 1-2. The controls and displays are located on panels 19, 20, 13, 26, and 23 of the control panel. The power supplied to the telecommunications system is current limited by the circuit breakers on panels 22 and 25. The specific function of the controls and displays is discussed in section 2 of this book.

The antennas used by the telecommunications system and their locations, are discussed at length in sections 6 and 14 of this book.

1.4 AUDIO EQUIPMENT INTERFACES

At the left side of figure 1-3 are the inputs and outputs for the audio equipment. These are the microphone and earphone of each astronaut. Several types of microphones and earphones are utilized by the astronauts. Each has a constant-wear helmet, figure 1-3, and a suit helmet. These provide the stimulae for the Audio Center. Located on the umbilical cord, called the cobra cable, figure 1-4, is a push-to-talk (PTT) button. An additional PTT button is located on the translation Controller. This PTT button is used by the astronaut to turn on the selected transmitter for voice communication. Each astronaut has an audio control panel at his particular station. Each panel controls a separate Audio Center. These centers are used to distribute the voice signals from the astronaut to the selected transmitters in the Spacecraft. The Audio Centers also isolate the voice signals coming from various receivers in the Spacecraft. The VHF/AM Transmitter Receiver is utilized to transmit voice signals between the Spacecraft and ground in near earth phases of the mission. It is also utilized to communicate between the LEM and the C/M. The VHF/AM Transmitter-Receiver feeds the VHF Multiplexer. The Multiplexer is used to isolate the various receivers and transmitters from one another. The Multiplexer output is sent to the antenna switch, where either the SCIN antennas or the recovery antennas are selected to receive the transmitter signals.

In the recovery phase, the HF Transceiver is used for long range voice communications. The VHF/AM Transmitter-Receiver can be utilized as a backup to the HF system for recovery communications. For deep space communications, the audio signal is placed on a subcarrier in the Premodulation Processor (PMP) and transmitted to earth via the Unified S-Band Equipment (USBE). The signal from the USBE can either be amplified in the S-Band Power Amplifier or

LOWER EQUIPMENT BAY

COMMUNICATIONS

1

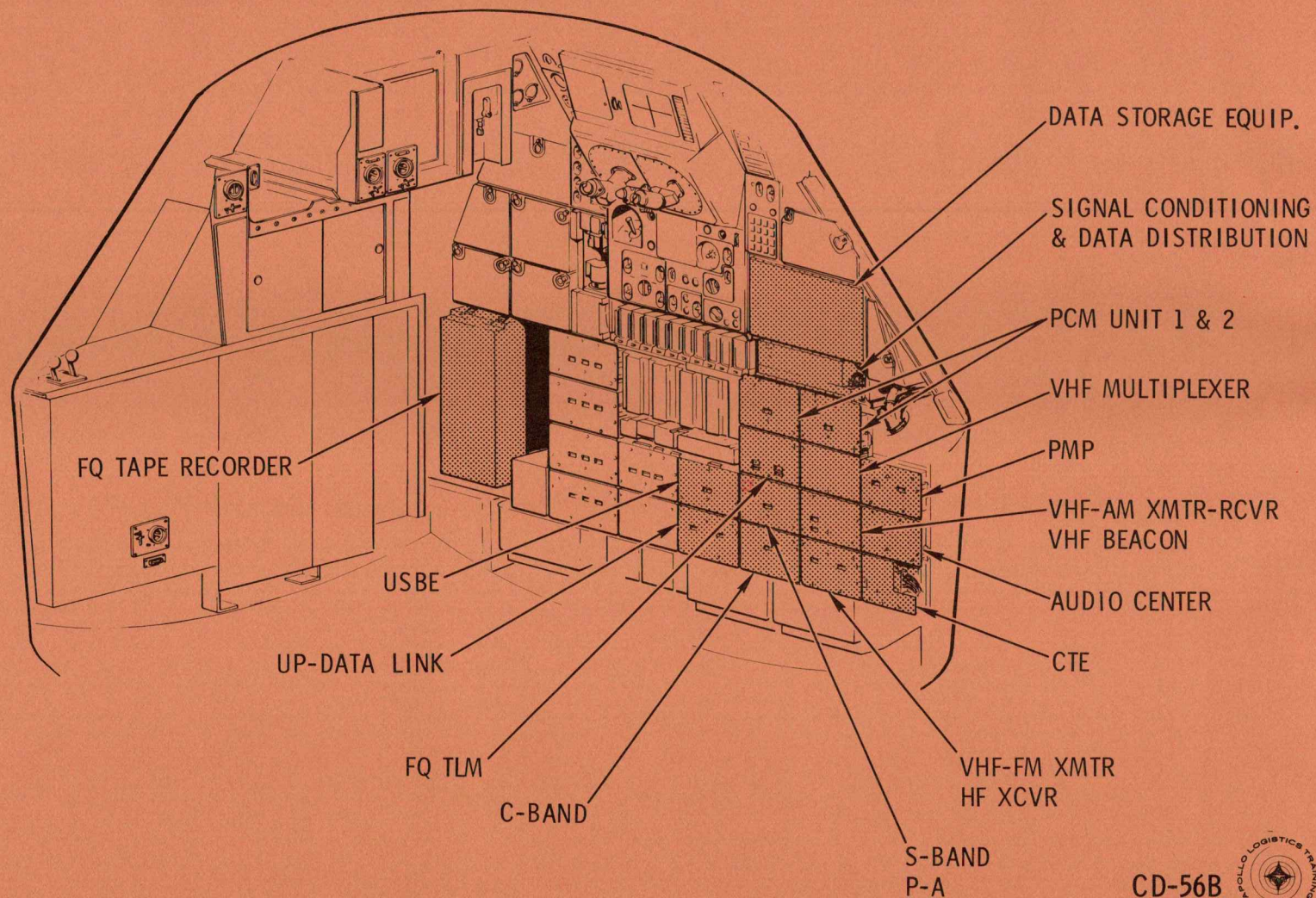


figure 1-2

CD-56B



CONSTANT WEAR PERSONAL COMMUNICATIONS ASSY (BUMP HAT)

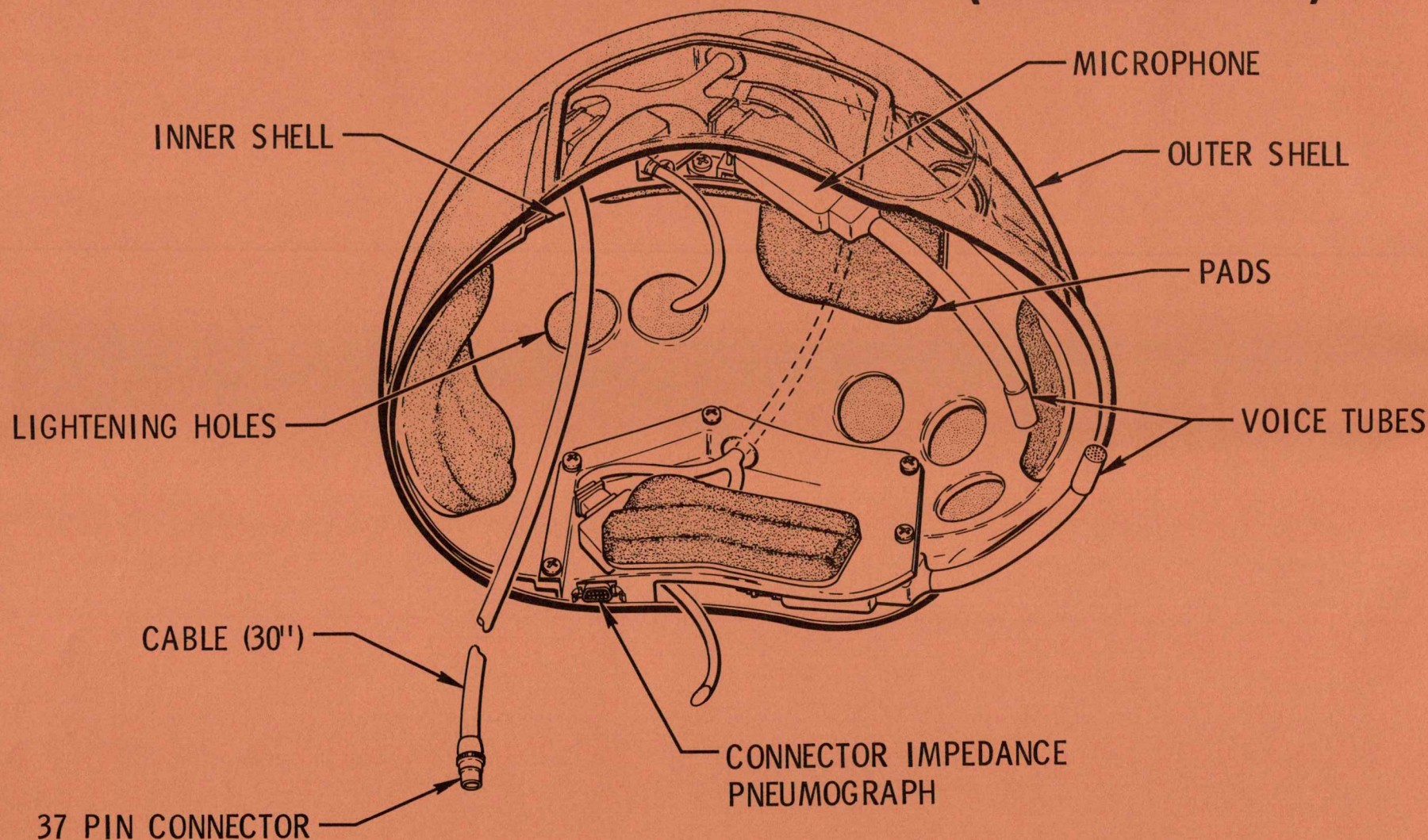


figure 1-3

CS-1017



PERSONAL COMMUNICATIONS EQUIPMENT CONNECTIONS (SHIRTSLEEVE ENVIRONMENT)

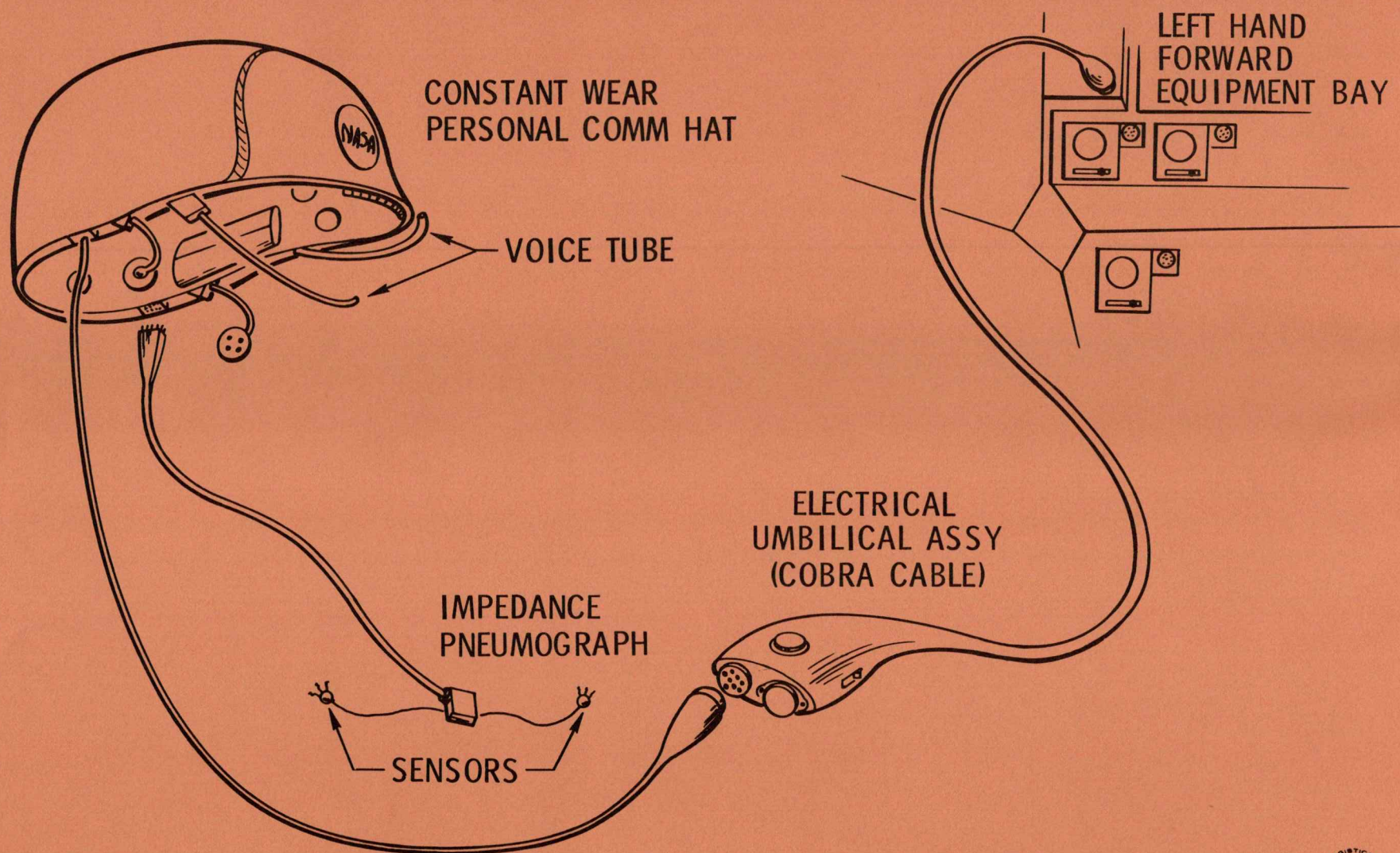


figure 1-4

CS-1016



AUDIO EQUIPMENT INTERFACES

1

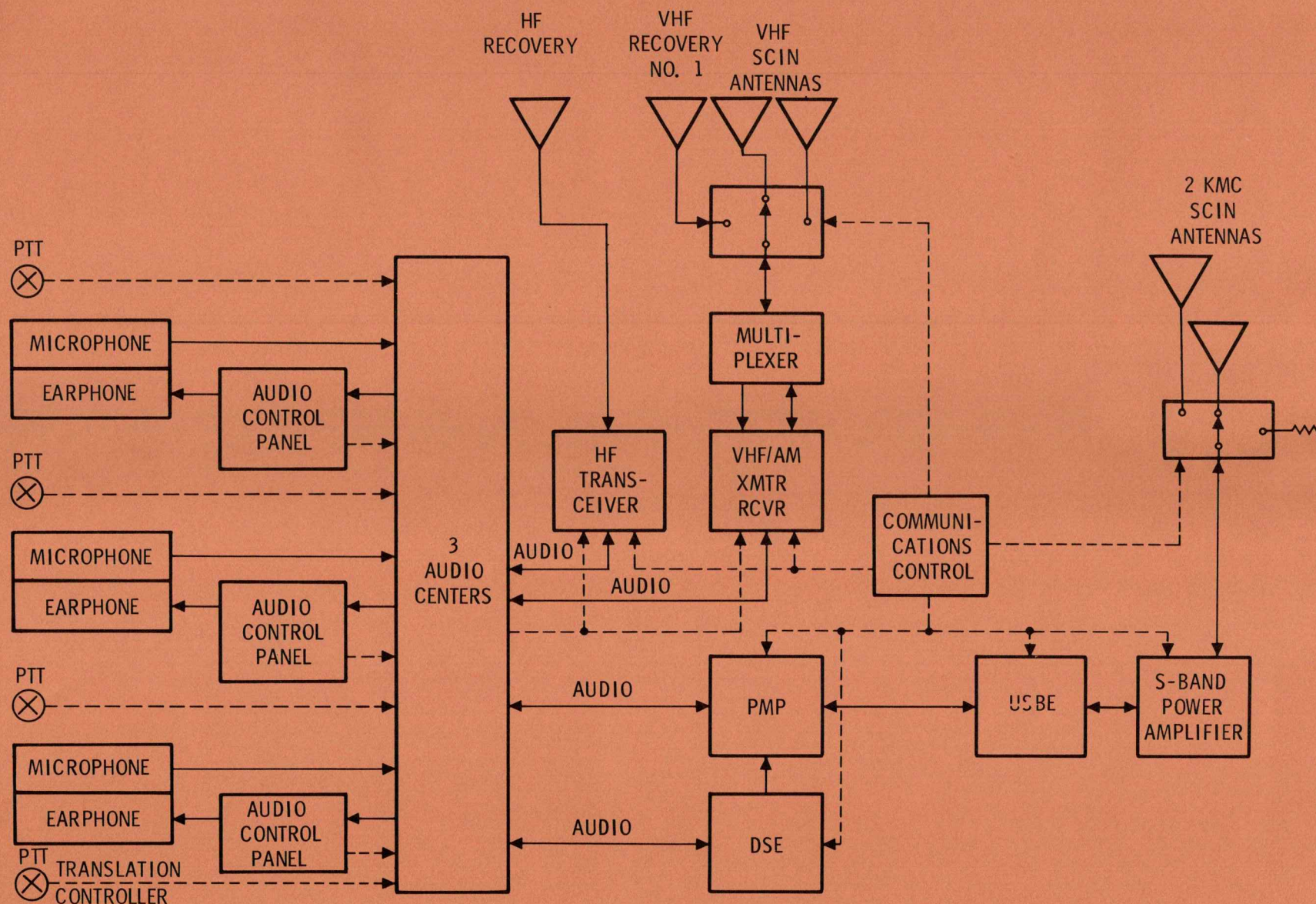


figure 1-5

CD-51 C



passed directly through the amplifier to the antennas, dependant upon mission requirements. The antenna system consists of the 2 KMC portion of the SCIN antennas.

The voice transmissions can be recorded on the Data Storage Equipment (DSE) if there is a possibility that the transmitted signal will not reach earth, such as when the S/C is behind the moon or during powered flight. The recorded voice signals may be played back through the PMP and the USBE to earth at a later time.

1.5 DATA SYSTEM INTERFACES

The data distribution panel, center-right figure 1-6, serves as a point of interface between the telemetry, displays, and GSE. The unconditioned analog inputs are conditioned to a compatible range in the Signal Conditioners. Conditioned analog and digital inputs interface with the data distribution panel. The signals are then sent to the three places listed above. In the telemetry equipment the analog signals are converted to a digital format for transmission to earth. Besides the analog signals coming from the distribution panel, there are low level analog signals coming directly into the telemetry. These low level signals are amplified and converted to the same digital format as the other analog signals. The Central Timing Equipment (CTE) interfaces with the telemetry equipment, supplying it with 512 kc and 1 cps. The CTE also supplies time information to the telemetry in the form of 26 parallel bits. Biomedical data is also encoded into the telemetry format. G&N information is supplied through the data distribution panel to the telemetry where it is encoded for transmission to earth.

The output of the telemetry interfaces with the PMP, sending it data in nrz digital bit form. In the PMP, the signal is routed to the VHF/FM or USBE transmitter for transmission to earth. The signal is sent to the VHF/FM Transmitter during the near earth phases of the mission. The VHF/FM Transmitter interfaces, through the Multiplexer, with the SCIN antennas. In deep space, telemetry data is transmitted via the USBE. From USBE, the signal can be sent directly to the antenna system or amplified in the S-Band Power Amplifier. Telemetry data can be sent to the Data Storage Equipment for recording at times when communications may be interrupted. Besides digital information being transmitted, high frequency analog signals are transmitted directly to earth by way of the USBE.

1.6 UP-DATA INTERFACES

Up-data is required to provide information to the Apollo Guidance Computer (AGC) and the time accumulator in the CTE. Also the up-data link can be used to command 64 different events in the Spacecraft. The up-data link system is divided into two parts and is shown in figure 1-7. The first part consists of a UHF/FM Receiver which is used in the near earth mission phases to receive up-data. The UHF/FM Receiver interfaces through the Multiplexer, with the SCIN antenna. The second, and main, part of the up-data link system is the decoder unit. The decoder unit processes the up-data from the receiver and feeds it to the appropriate system; the AGC, the CTE or one of 64 locations programmed for real time commands. Every up-data link message is validated or rechecked, and this information is sent back to earth through the PCM Telemetry. In deep space, the up-data link information is received by the USBE, detected in the PMP, and sent to the decoder portion of the up-data link system for distribution.

DATA SYSTEM INTERFACES

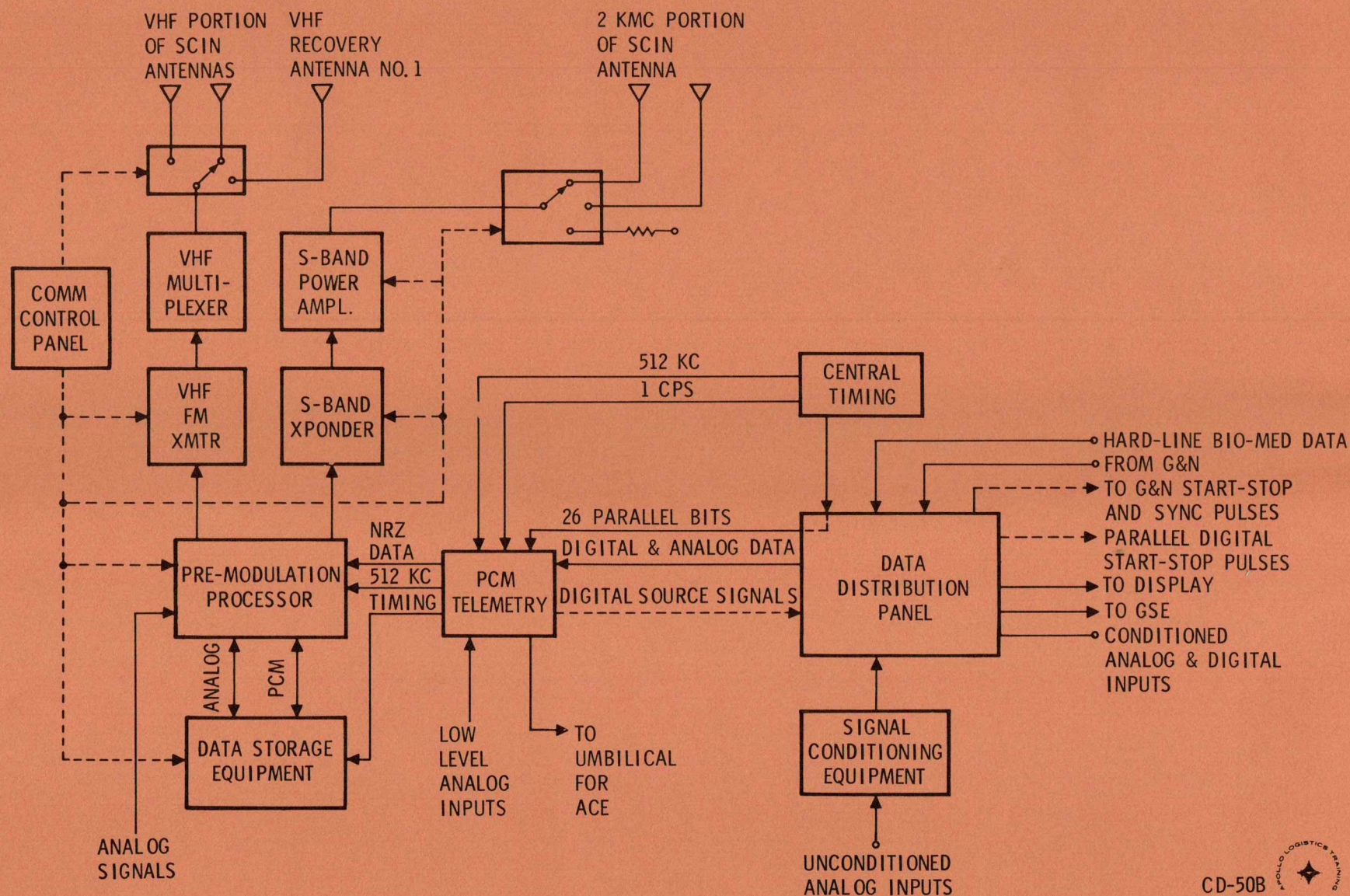


figure 1-6

CD-50B



UP-DATA INTERFACES

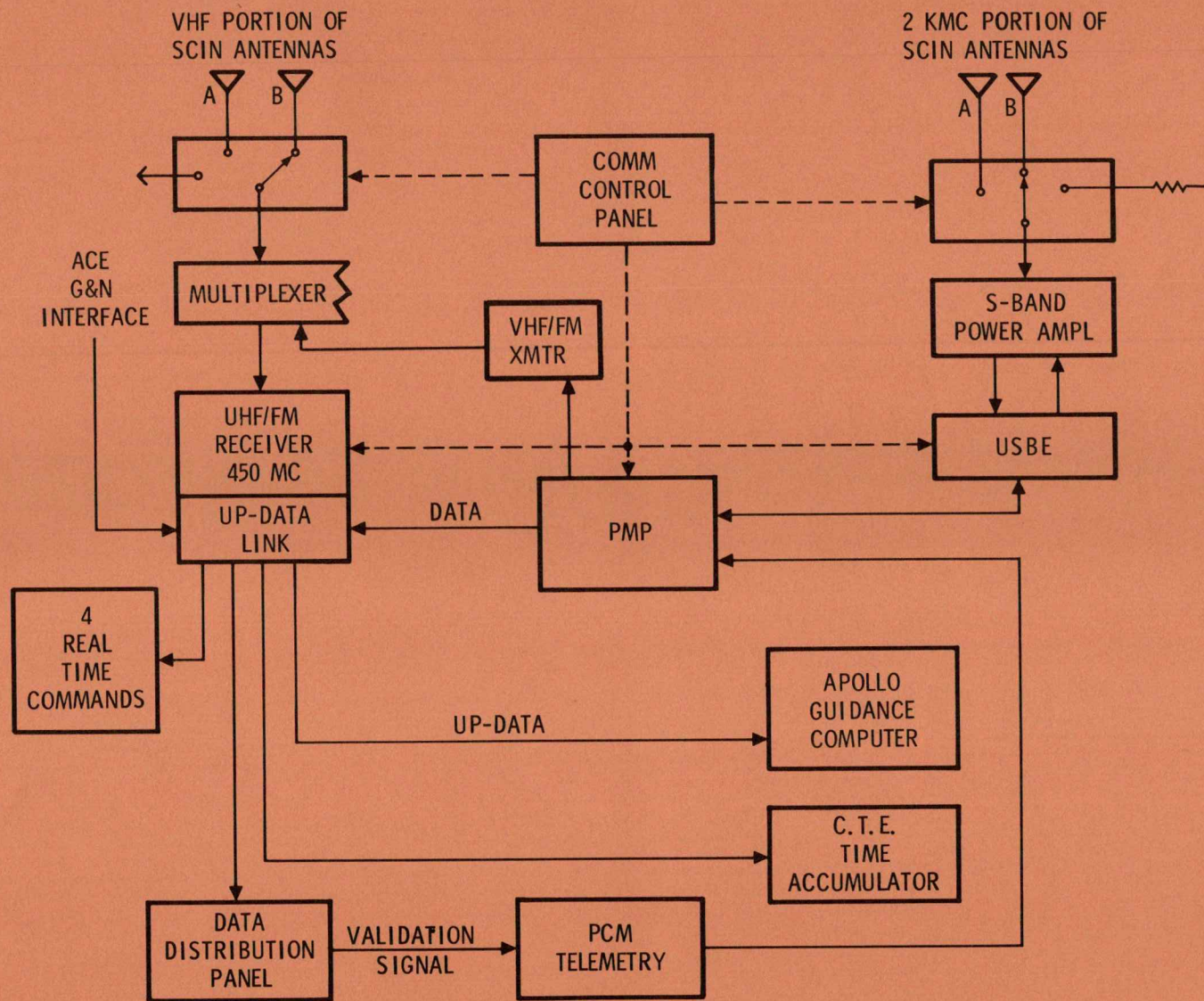


figure 1-7

1.7 PRE-MODULATION PROCESSOR INTERFACES

The Pre-Modulation Processor (PMP) interfaces equipments and processes signals prior to their distribution. The following signals are processed through the PMP shown in figure 1-8. Bio-medical data from the LEM via the VHF/AM Receiver and the PMP is sent to the USBE for transmission to earth. Voice signals are sent from the Audio Centers to the PMP where they are placed on a subcarrier and then sent to the USBE for transmission to earth. Voice signals from earth, received by the USBE, are processed in the PMP and sent to the Audio Centers. High frequency analog signals are placed on subcarriers in the PMP prior to transmission by the USBE. The PMP serves as an interface between the Data Storage Equipment (DSE) and the signals that are recorded. The various recorded signals are later played back through the PMP to the USBE for transmission to earth. The television signals pass through the PMP as they are sent to the USBE for transmission to earth. Telemetry signals are sent to the PMP to be placed on subcarriers for transmission to earth by either the FM Transmitter or the USBE. The CTE supplies 512 kc to the PMP for use as subcarriers and for timing. In an emergency condition, the astronaut's PTT button can be used as a telegrapher's key and Morse code can be sent to earth by interrupting the 512 kc signal in the PMP and transmitting this through the USBE.

1.8 TELECOMMUNICATIONS SYSTEMS

The Telecommunications System figure 1-9 overall block diagram is an integration of the audio, Data, PMP, and up-data interface diagrams. The equipment not discussed on the other diagrams are the C-Band Transponder which is used for near earth tracking of the Spacecraft and the VHF Beacon

which is used for location of the spacecraft in the recovery phase of the mission.

1.9 COMMUNICATION SYSTEM POWER DISTRIBUTION

The circuit breakers and DC switches for the Communication System are located on panel 22 and 21.

1.9.1 DC Power Distribution

The dc power for distribution to the Communication System is provided by the Flight and Post Landing bus. This bus may receive power from Main busses A and B, Entry busses A and B, or from the Post Landing battery through circuit breakers. Normally the Flight and Post Landing bus, through three circuit breakers, feeds dc power to the various sections of the Communications System.

The group 3 circuit breakers feeds dc power to the up-data link equipment.

The group 4 circuit breaker provides primary dc power to the Audio Center keying relay circuit, Engineers Audio Center and microphone amplifier, the VHF/AM Transmitter and receivers, the HF transceiver and the VHF Recovery Beacon.

The group 5 circuit breaker provides dc power to several components and a switch. The Commanders and navigators Audio Centers and microphone amplifier, the VHF/AM Transmitter and receivers, the HF transceiver and the VHF Recovery Beacon.

The Main Bus A circuit breaker on panel #25 provides dc power to the Pre-modulation processor, Data Storage Relay and the Signal conditioning Power relay.

PRE-MODULATION PROCESSOR INTERFACES

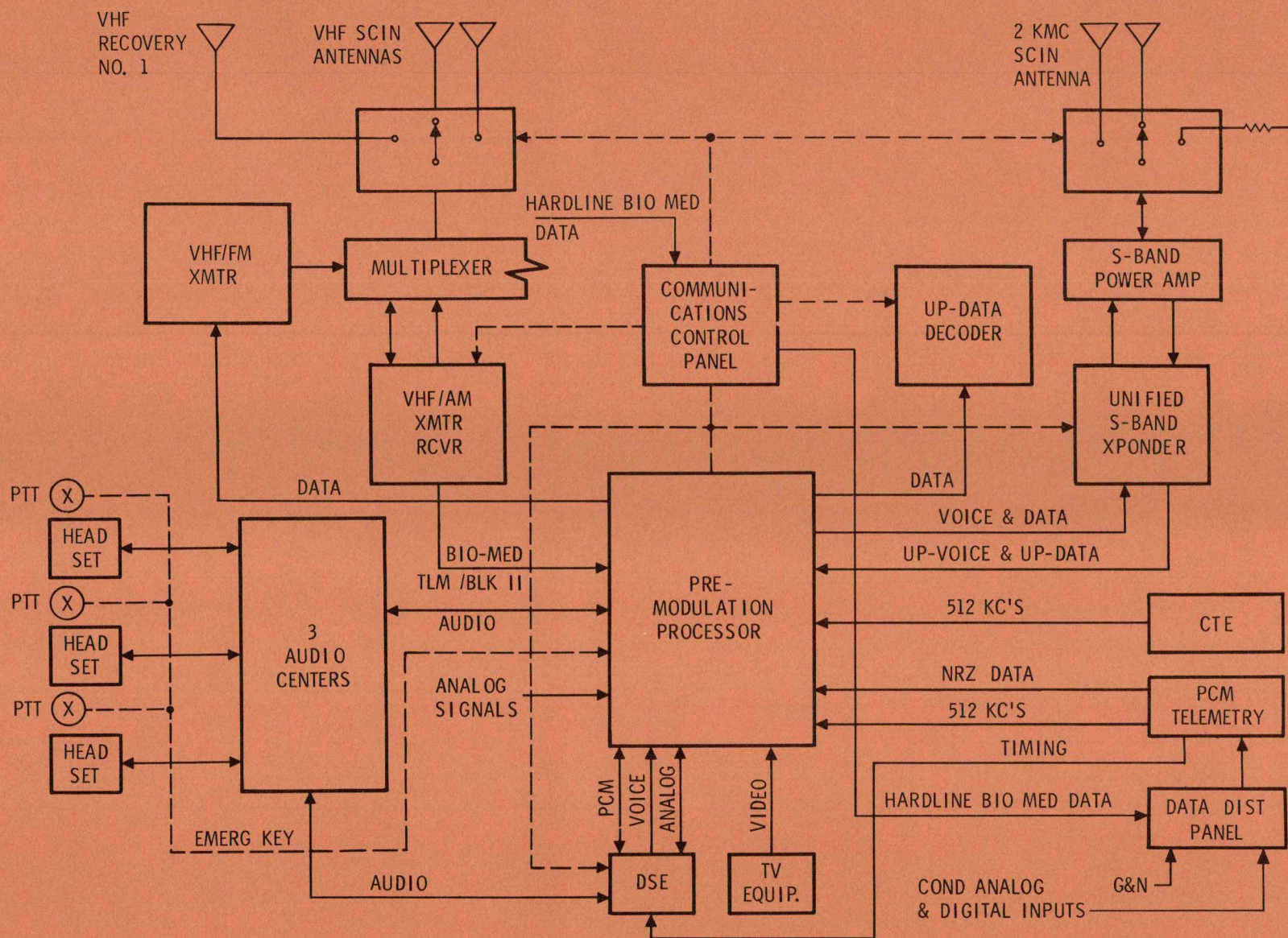


figure 1-8

CD-55B



TELECOMMUNICATIONS SYSTEM

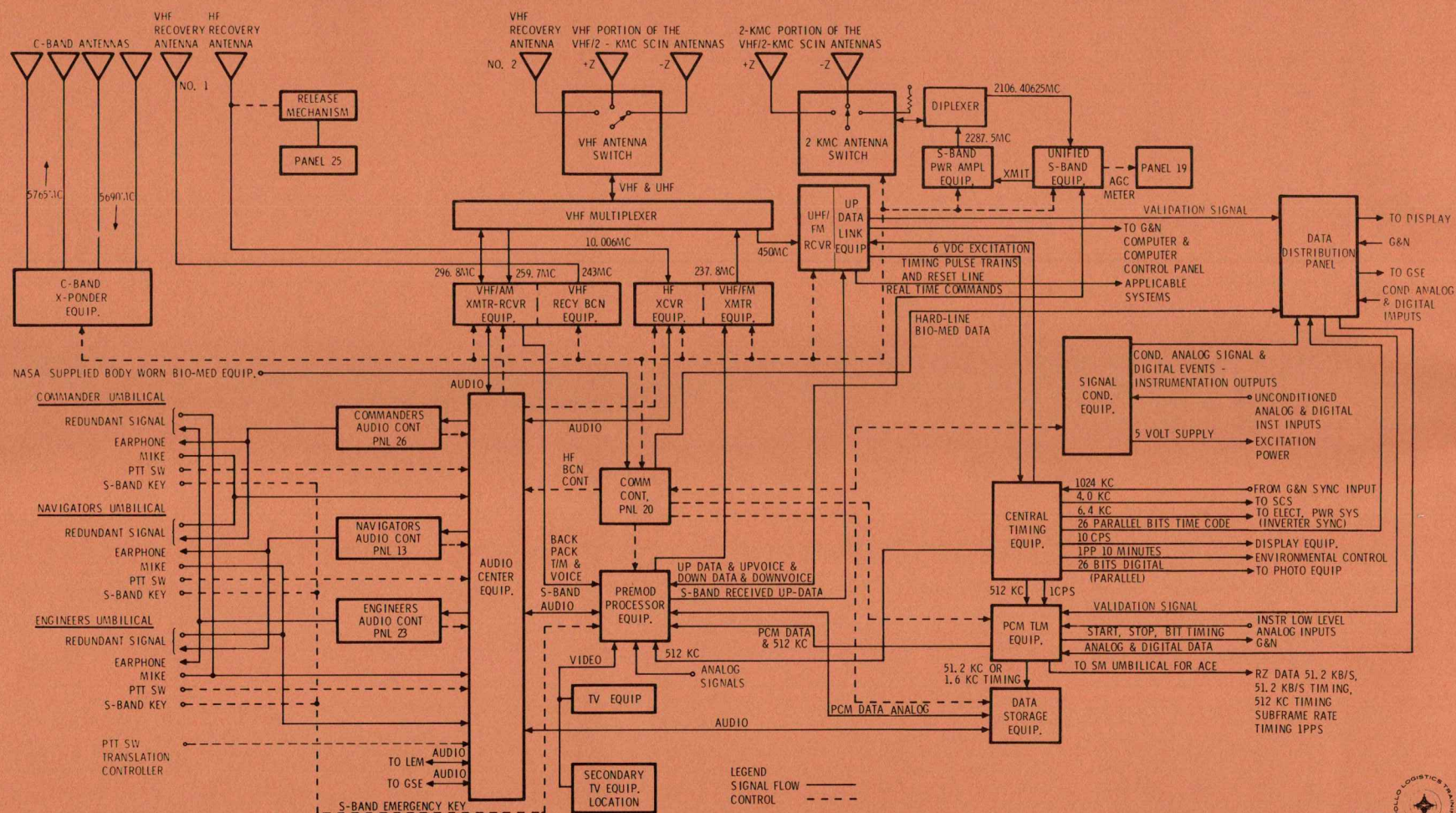


figure 1-9

The Main Bus B circuit breaker on panel #25 provides power to the S-Band power amplifier and relay, the up voice and up-data discriminators, the S-Band antenna switch and power amplifier relay, plus the biomed amplifier.

The Main Bus circuit breaker on panel #22 provides dc power to the VHF/FM transmitter relay and the central timing equipment. Main Bus B on the same panel also provides power to the CTE.

The PAM transmitter and non essential circuit breakers provide dc power to the flight qualification transmitter and recorder respectively.

The scientific circuit breaker provides dc power to the C-Band transponder relay.

The essential A & B circuit breakers provide dc power to the essential instrumentation system.

1.9.2 AC Power Distribution

Located on the lower left-hand corner of figure 1-10 are AC busses number 1 and number 2. Through two toggle switches on panel 22, labeled "NON ESS T/C" and "ESS T/C" switches 5 and 6. AC Bus 1 or Bus 2 power can be selected or removed. The 400 cps ac is sent through circuit breakers into the basic equipment groups. The PCM-TLM circuit breaker provides 400 cps, 115v, 3 phase, ac power to the signal conditioning equipment, PCM telemetry equipment, and data storage unit.

The S-Band PA - signal conditioner circuit breakers provide ac power to the USBE and the the S-Band Power Amplifier.

NOTE: At this point we must be aware of the discrepancies between the circuit breaker nomenclature and their actual functions.

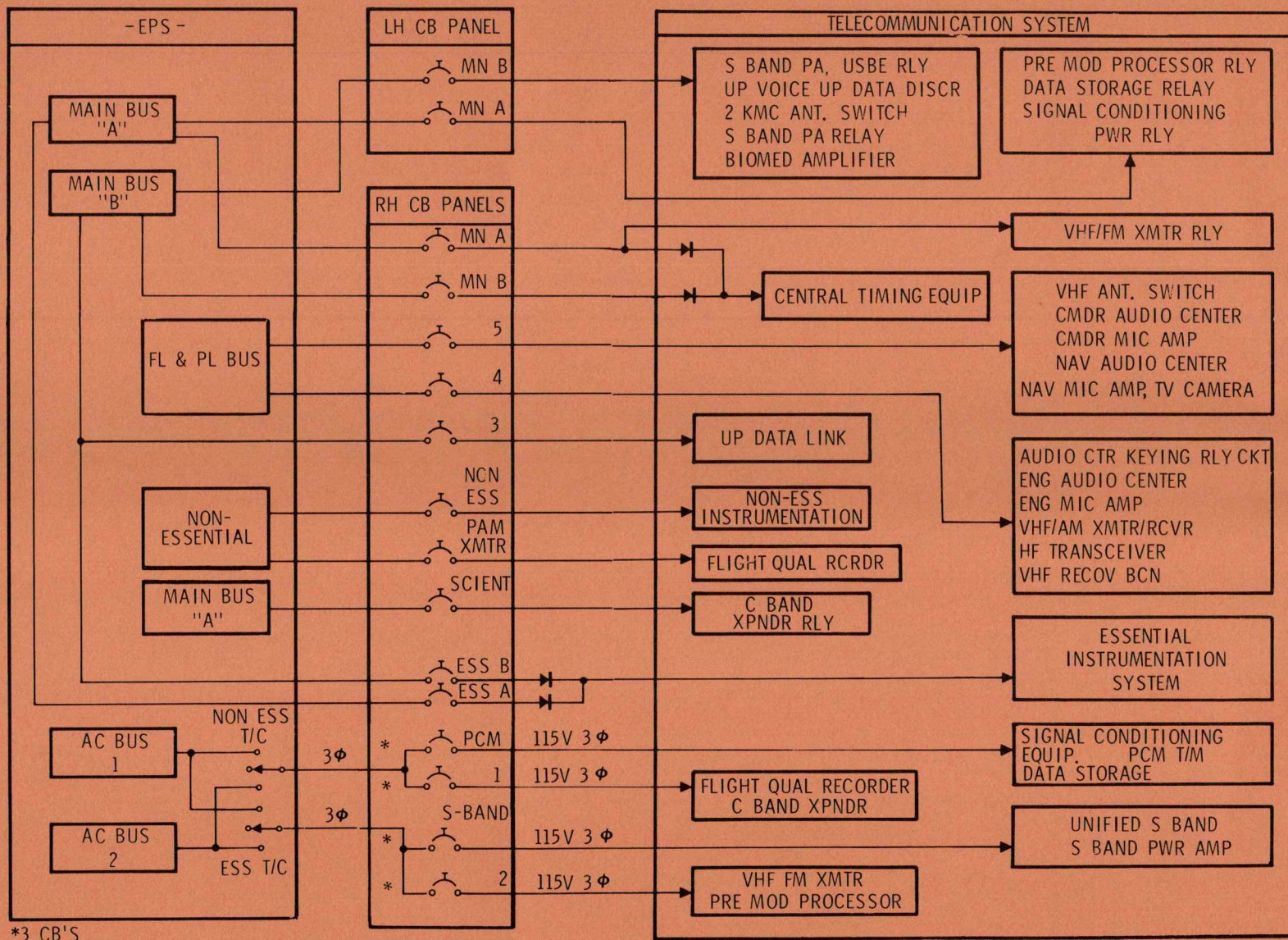
This is being changed but as of September, 1965 no change has been processed.

Group #1 circuit breaker provides ac power to the Flight Qualification Recorder and the C-Band transponder.

Group #2 circuit breaker provides ac power to the VHF/FM transmitter and the Pre-modulation processor.

INSTRUMENTATION & COMMUNICATION

POWER DISTRIBUTION



*3 CB'S

figure 1-10

EP-208C



SECTION II

CONTROLS AND DISPLAYS

The controls and displays for the telecommunications equipment are located on eight of the main display panels in the Command Module. Control panel 20 contains the switches which determine the operating modes of the various pieces of telecommunications equipment. Control panel 19 contains a display which deals with the S-Bands System. There are three identical Audio Control Centers, one for each astronaut. They are located on control panels 13, 23, and 26. These control panels are not, themselves, identical.

In the following text each control panel is given a major heading and general sections of the panels will have minor headings. Each switch has a sub-heading.

2.1 COMMUNICATIONS CONTROL PANEL NUMBER 20

2.1.1 S-Band General

The first group of switches that will be discussed are those which control the S-Band equipment. These switches are shown on figure 2-1 & 2-2. S-Band equipment is used for all modes of data transmission from the spacecraft to ground and from the ground to spacecraft while in deep space. The S-band equipment is also used as a backup to the communications equipment used in earth orbit when the S/C is near the earth. S-band controls consist of eight switches.

2.1.1.1 Power Amplifier Switch

The "PWR AMP" switch is a three-position, center off, switch. The TRANSPONDER position turns

on the S-band transponder in the Unified S-Band Equipment (USBE), leaving the power amplifier off. This gives a power output of 250-400 mw. The PWR AMP position turns on both the S-Band Power Amplifier and the USBE transponder. This removes the power amplifier from the by-pass mode and enables the "POWER MODE" switch to determine the power output. The off position removes all power from the USBE and S-Band Power Amplifier.

2.1.1.2 Power Mode Switch

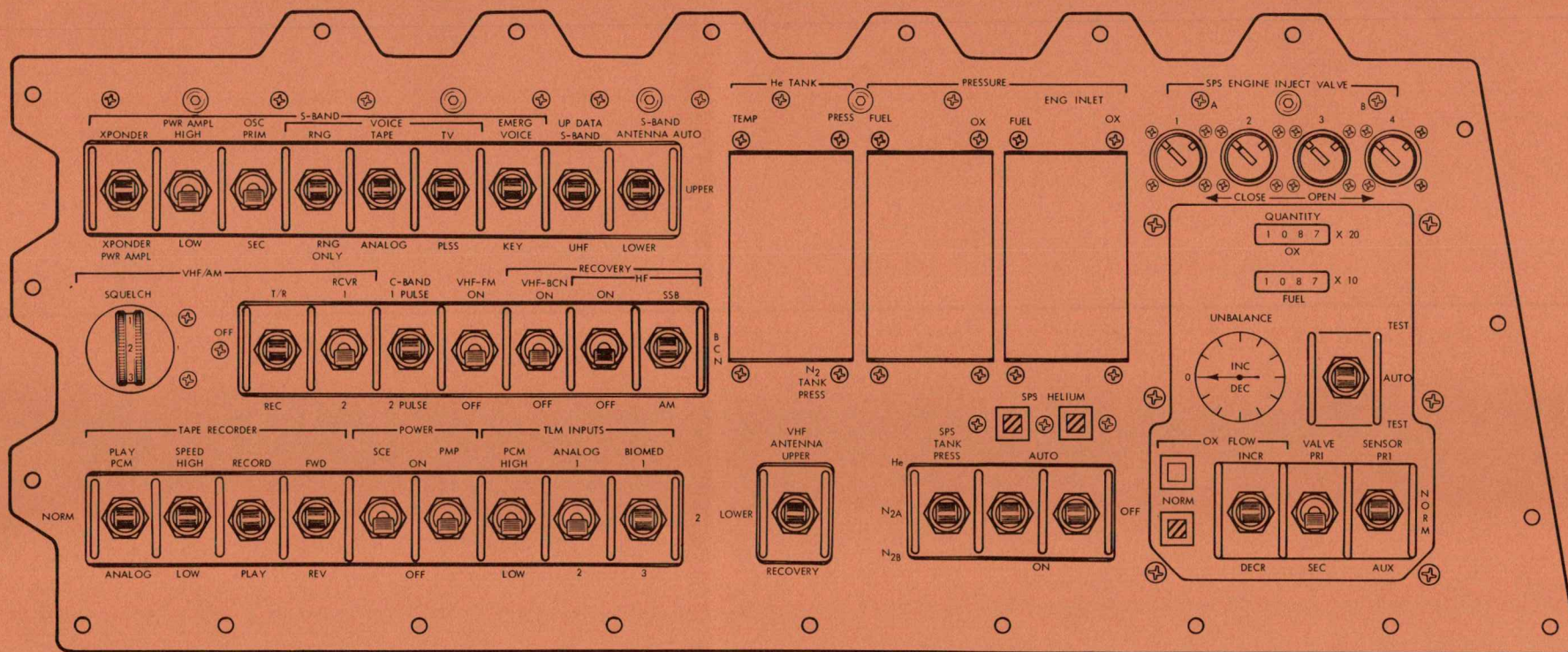
The HI position selects a 20 watt mode of operation in the S-Band Power Amplifier while the LOW position selects a 5 watt mode.

2.1.1.3 Oscillator

The "OSC" switch is a two-position switch for control of the voltage control oscillator (VCO) and Aux oscillator for the USBE. The PRI position selects the VCO operation of the receiver and transmitter. The SEC position selects the auxiliary crystal oscillator for use as a reference in the USBE transmitter.

2.1.1.4 Normal Switches

These three switches are for normal mode of operation of the S-band equipment. When these three switches are in the center position, information from the PCM Telemetry and Audio Centers will be transmitted via the S-band. The top position of the first switch in a normal mode is labeled RNG/PCM. This mode provides a simultaneous ranging function in conjunction with voice and PCM Telemetry transmission. The



20

figure 2-1

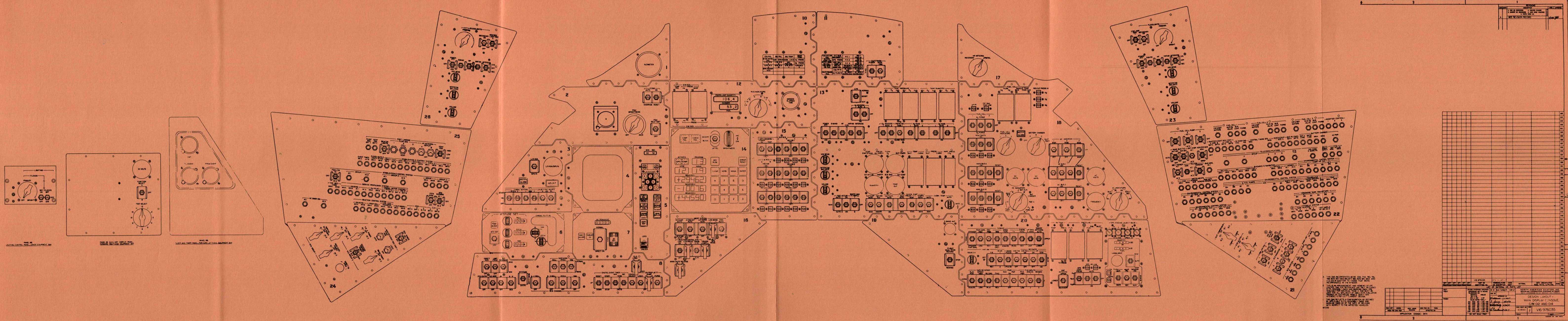


figure 2-2

lower, or RNG, position will allow only voice transmission and simultaneous ranging. The second switch has the upper position labeled TAPE/PCM. In this position data to be transmitted by the S-band equipment is controlled by the tape recorder switches. These are located in the lower left hand corner of the panel. The bottom position of the switch is labeled ANLG/PCM. In this mode of operation real time analog, PCM Telemetry data and voice signals will be transmitted. The next switch has its upper position labeled TV/PCM. In this position PCM Telemetry, voice, and television will be transmitted. The lower, or PLSS/PCM, position will enable transmission of PCM Telemetry and voice information and will also relay bio-medical information concerning extra vehicular astronauts.

2.1.1.5 Emergency Switch

This switch is used to control the emergency communications modes of operation of the S-band equipment. The VOICE position is used for emergency voice transmission. The KEY position is used for transmission of emergency key information.

2.1.1.6 Up-Data Switch

This switch is used whenever up-data link information is needed or required. It is a three-position, center off switch. The S-BAND position is used when the Communication system is in deep space and up data link information is to be received via the USBE. The UHF position will be used for receiving up data information when the S/C is near the earth.

2.1.2 VHF/AM General

The VHF/AM Transmitter-Receiver provides a two way voice link between the Spacecraft and GOSS

when the S/C is near the earth. The VHF/AM equipment is also used to provide a two way voice link between the S/C and the LEM or an extravehicular astronaut and can relay to GOSS bio-medical data from either of them. The next row of switches, shown on figure 2-1, are used to control the VHF/AM system.

2.1.2.1 Squelch

This thumbwheel controls the quieting level in the VHF/AM Receiver.

2.1.2.2 VHF/AM Transmitter Switch

This switch is a three-position, center-off, switch. The upper position, T/R, is used when transmission and reception via the VHF/AM equipment is desired. The REC position will be used when only the VHF/AM Receiver is to be activated.

2.1.2.3 Receiver Switch

This is a two-position switch that will select the frequency at which VHF/AM equipment will receive data. The NORM position will enable communication with an extravehicular astronaut or with the ground station. The LEM position will be utilized when communicating with the Lunar Excursion Module and may also be used when communicating with the ground stations.

2.1.3 C-Band Switch

The C-band equipment provides near earth tracking data to GOSS. The C-band transponder is independent of all other equipment with the exception of power. One switch is provided for its control.

The 1-PULSE position of the "C-BAND" switch selects an operation in the C-Band Transponder whereby ground based radars having either 1 or 2 pulse transmitters can interrogate the S/C transponder. This is a secondary mode of operation. The 2-PULSE position selects an operation in the C-Band Transponder whereby only those ground based radars which have a correctly coded 2 pulse transmitter can interrogate the S/C transponder. This is a primary mode of operation.

2.1.4 VHF/FM Switch

This is a two-position switch. The VHF/FM equipment is utilized when the S/C is near the earth to transmit PCM telemetry data to the ground. The ON position applies power to the VHF/FM Transmitter. The lower position is OFF.

2.1.5 Recovery General

The recovery equipment provides aids for the location of the spacecraft and for long range voice communications. The controls consist of three switches with one for VHF Beacon and two for the HF Transceiver.

2.1.5.1 VHF Beacon Switch

This is a two-position switch labeled ON and OFF. The ON position applies power to the VHF Beacon.

2.1.5.2 HF Power Switch

This is a two-position switch labeled ON and OFF. The ON position applies power to the HF Transceiver.

2.1.5.3 HF Mode Switch

The HF MODE switch has three positions. The SSB position selects the single side-band mode of operation for the HF Transceiver. The center BCN position selects the beacon mode of operation. The lower or AM position selects the amplitude modulation mode of operation for the HF Transceiver.

2.1.6 Tape Recorder General

The tape recorder is used to store both digital PCM telemetry, and analog information (including voice) which might otherwise be lost due to a break in the communications link. The first four switches at the lower left of Control Panel 20 (figure 2-1) control the tape recorder. An input to the tape recorder is also required from the "PCM HI-LO" switch to control speed.

2.1.6.1 Tape Recorder Switch

This switch selects the mode of operation of the tape recorder. The RECORD position selects a record function for the tape recorder. The center position is OFF. The PLAY position selects a playback mode of operation for the tape recorder. Power application is controlled by this switch. Data to be either recorded or played back is selected by the "PLAY" switch.

2.1.6.2 Play Switch

This switch works in conjunction with two others, the "S-BAND NORMAL" switch in the TAPE/PCM position and the "TAPE RECORDER" switch in the PLAY position. The positions of the "PLAY" switch

determine the input to the Pre-Modulation Processor. In the NORMAL position both recorded analog and PCM data with real time voice information is fed to the S-band equipment for transmission. In the PCM position, recorded PCM telemetry data is transmitted along with voice information. In the ANALOG position recorded analog data is transmitted along with real time PCM and voice information.

2.1.6.3 Speed Switch

This is a three-position switch which selects the speed of operation of the tape recorder. The HIGH position selects 120 inch per second which is the dump or rewind speed. The center position selects a 15 inches per second (ips) speed. This is the normal speed of the tape recorder. The LOW position selects a 3.75 inch per second speed for the tape recorder.

2.1.6.4 Tape Direction Switch

The FWD position of this switch commands the direction of tape travel through the recorder to be left to right. The center position is STOP. The REV position commands tape travel from right to left.

2.1.7 Power Switches General

One switch is used to supply power for the signal conditioning equipment (SCE) and one for the pre-modulation processor (PMP). These are two-position switches labeled ON and OFF.

2.1.8 TLM General

The telemetry switches are used to select the type of analog signals to be transmitted or

recorded and the rate of PCM inputs to be sampled. They are located in the lower right section of control panel 20.

2.1.8.1 PCM Switch

The "PCM" switch is a two-position switch. In the HI position, the high bit rate of 51.2 kilobits per second is selected as the telemetry system output. Also, when this position is selected, the tape recorder speed will be locked at 15 ips. The LOW position will select the low bit rate of operation for the telemetry equipment, or 1.6 kilobits per second. This position also locks the tape recorder speed to 3.75 inches per second.

2.1.8.2 Analog Switch

This is a two-position switch which will select either set of nine analogs signals, to be transmitted or recorded. There is a total of 18 analog channels.

2.1.8.3 Biomed Switch

This switch will select the astronaut, or the position, from which biomedical data will be transmitted. Bio-medical data will be transmitted in the high bit rate mode of the PCM telemetry data only. The upper position, labeled 1, will select bio-medical data from the commander's station. The center position, labeled 2, will select bio-medical data from the navigator or from the sleep station. The lower position, labeled 3, will select bio-medical data from the systems engineer station.

2.1.9 S-Band Antenna

The S-Band antenna switch is used to select the antenna or the automatic selection of the

S-band antenna to be used in conjunction with USBE. The S-band antenna switch is a three-position switch.

2.1.9.1 Auto

The auto position activates the circuit inside the USBE which selects the appropriate antenna based on received signal strength.

2.1.9.2 Upper

This position selects the S-band antenna located on the -Z axis.

2.1.9.3 Lower

This position selects the S-band antenna located on the +Z axis.

2.2 AUDIO CENTER CONTROLS

There are three Audio Center Control panels, one panel for each of the astronaut couch positions. The Commander's audio center is located at panel 26, the navigator's audio center is on panel 13, and the engineer's audio center control is on panel 23 as shown in figure 2-2. All three Audio Center Control panels are identical, and each controls audio for its particular astronaut station. Therefore, only one of the three panels, #13, will be explained. Each panel consists of five switches and three thumbwheel controls which are explained below. Refer to figure 2-3 for a detailed picture of panel #13.

2.2.1 Switches

2.2.1.1 S-Band Control Switch

The "S-BAND" switch, when set to the T/R position, allows the astronaut to communicate with

GOSS via the USBE if the appropriate controls on the Communication Control panel have been selected. The center off position removes the audio input from the S-band voice section of the Audio Center. The RECEIVE position allows the astronaut to only receive information via the S-band equipment.

2.2.1.2 HF Switch

With the three-position HF switch in the T/R position, the astronaut is able to communicate with the recovery forces via HF if the appropriate controls on the Communication Control panel have been selected. The center off position removes power from the HF channel of the audio center and the RECEIVE position enables reception by the HF Transceiver if the appropriate controls have been selected on the Communications Control panel.

2.2.1.3 VHF-AM Switch

This is a three position switch. With the "VHF-AM" switch in the T/R position, two way voice communication via the VHF-AM Transmitter-Receiver is enabled if the appropriate controls have also been selected on the Communication Control panel. The center position removes power from the audio center channel for VHF-AM. The bottom position, RECEIVE, allows the astronaut to receive voice transmission by the VHF-AM receiver if the receiver is activated by switches on the Communication Control panel.

2.2.1.4 Intercom

This three position toggle switch has its upper position labeled T/R. This allows the astronaut to transmit to, and receive from, the other stations in the spacecraft, the Lunar Excursion Module via a hard line connection, ground personnel

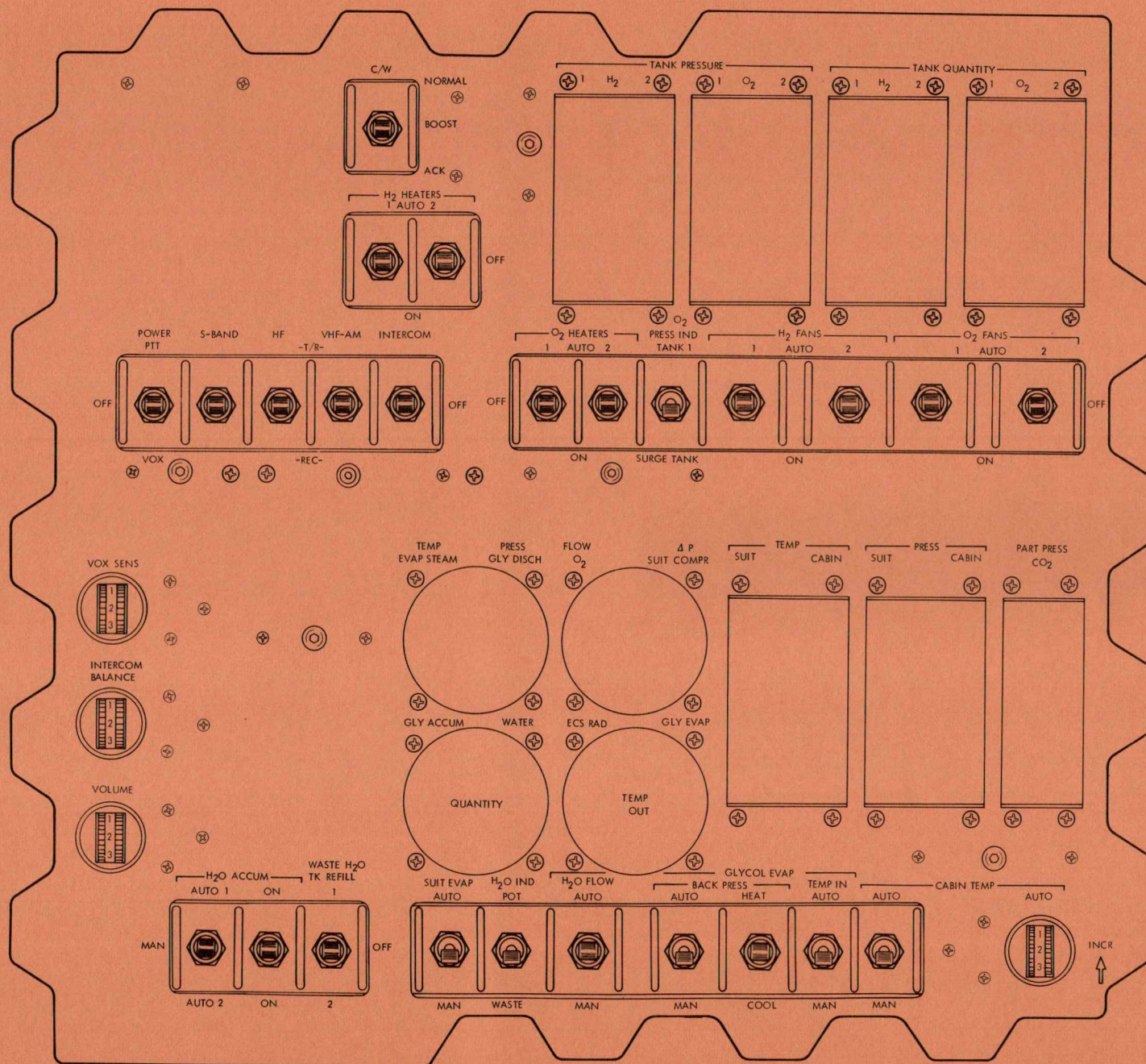


figure 2-3

prior to lift off, and to transmit voice to the Data Storage Equipment. The center off position removes power from this astronaut's intercom channel of his audio center. The lower position, RECEIVE, allows the astronaut to receive intercom voice only.

2.2.1.5 Power

The top position of this three position switch is labeled PTT, (Push-to-Talk). With the switch in this position, the audio center equipment and the particular transmitter selected is activated by the push-to-talk button, located on the cobra connection of his umbilical cord. The center, off, position removes power from the audio center and the selected transmitter to be activated by a voice operated switch.

2.2.2 Thumb Wheel Controls

2.2.2.1 Volume

This control is a master volume control for the audio center. It will vary the audio center's output volume into the earphones.

2.2.2.2 Intercom Balance

This control allows the astronaut to lower the transmitted intercom signal below the incoming audio signal from other sources or make it equal to these signals.

2.2.2.3 VOX Sensitivity

This control allows the astronaut to select the level of volume with which he will have to speak in order to trigger the appropriate transmitter.

2.3 ANTENNA DEPLOY CONTROLS

The antenna deploy controls are located on the left hand circuit breaker panel No. 25. There are two switches under the general heading of Post Landing, Antenna. They are the "A", (Pyro Arm, safe) switch and the B, (deploy) switch. These two switches are in series and are used to deploy the HF recovery antenna and can be seen in figure 2-4.

2.4 ANTENNA SELECT SWITCH

The antenna select switch is located on panel No. 17. This rotary switch selects which antenna will be utilized in conjunction with the VHF equipment. Recovery position selects the Recovery antenna which is automatically deployed after the main chutes. Upper selects the "SCIN" antenna located on the -Z axis, lower selects the "SCIN" antenna on the +Z axis.

2.5 AGC METER

Located on panel No. 19 is an AGC meter which is used in conjunction with the USBE. This meter gives the relative signal strength of the received S-band signal.

2.6 TELECOMMUNICATIONS POWER DISTRIBUTION

Located on panel No. 22 are the circuit breakers for the Telecommunication system, figure 2-5.

2.6.1 A-C Power

A-C Power for the T/C system is furnished by a-c bus No. 1 and bus No. 2. All T/C equipment which requires a-c power has been divided into two

groups, termed essential T/C and nonessential T/C. If necessary, either a-c bus No. 1 or bus No. 2 will provide sufficient power for both groups of T/C and non ESS T/C, provide a means for selecting either a-c bus No. 1 or bus No. 2 to provide power for either or both groups of T/C equipment.

2.6.2 D.C. Power

All d-c power for the T/C system, except for the central timing equipment (CTE), is supplied by the flight and postlanding bus. This includes equipment which operates solely on d-c and power control relays for equipment which operates primarily on ac. The CTE is supplied directly, through diodes and circuit breakers, by d-c main bus A and main bus B.

SECTION III

AUDIO CENTER EQUIPMENT

INTRODUCTION

Aboard the spacecraft, each astronaut has a headset consisting of two independent earphones and two independent microphones. Each headset is connected to an individual Audio Center and audio control sub panel. The audio system amplifies voice signals, then reduces these signals to their original condition in order to provide isolation. It also provides amplification of incoming signals. The audio equipment is located in a space electronics package and consists of three identical, replaceable Audio Center modules. Each module is a complete and independent unit operated by one astronaut. It contains a microphone amplifier, an earphone voice operated switch circuitry, isolation pads, and diode switches. The three Audio Centers operate with complementary audio control sub panels to provide selection, isolation and amplification of all spacecraft audio to and from the transmitters and receivers in the Communications System.

The Audio Center Equipment carries voice signals from the astronauts' microphones to the HF Transmitter, the VHF/AM Transmitter, or the S-Band Transmitter. The signals to the S-Band Transmitter are routed through the Pre-Modulation Processor. Voice signals are selected from the HF Receiver, the VHF/AM Receiver and the S-Band Receiver. The incoming voice signals from the S-Band Receiver are processed through the Pre-Modulation Processor. The voice signals are selected from the audio control sub panel, amplified in the Audio Center, and fed to the astronauts' earphones. Each Audio Center is

independently capable of selecting any transmitter or receiver or any combination of transmitters and receivers. A keying voltage is provided from the Audio Center for the operation of the keying relays in the HF Transmitter and the VHF/AM Transmitter.

The intercom bus provides communications between the Data Storage Equipment, the GSE intercom system (prior to launch), and the LEM intercom system. The Data Storage Equipment has the capability of recording voice signals from the intercom bus and playing back the recorded voice into the intercom bus.

The equipment is located in the Lower Equipment Bay and weighs 6.75 pounds with a volume of 252 cubic inches. The voltage input is 28 volts dc at a maximum power input of 12.8 watts.

AUDIO EQUIPMENT CONTROLS. Three audio control sub panels form part of the controls and displays. The Commander's and Engineer's audio control sub panel are located on either side of the Main Display Console. The Navigator's audio control sub panel is located in the Main Console Panel. Each audio control sub panel contains five toggle assemblies which actuate hermetically sealed switches, two 25 k ohm potentiometers, and a 1 megohm potentiometer with each potentiometer controlled by a thumbwheel mechanism. For more information on the Audio Equipment Controls see Section II, Controls and Displays.

BLOCK DIAGRAM DESCRIPTION

EARPHONE AMPLIFIER. Audio input signals from the receiver portion of the VHF/AM Transmitter-Receiver, the receiver portion of the HF Transceiver, and the receiver portion of the USBE after it has been processed in the Pre-Modulation Processor, along with an input from the intercom bus, enter diode switching circuits which are controlled from the audio control sub panel. Isolation is provided at each audio input to prevent the astronaut from hearing a signal from an unselected source, if and when the diode switches are turned on in the other two Audio Center modules. The audio signal passes through an isolation amplifier and then through a preamplifier stage. The signal is developed further in a push-pull driver stage and fed to a push-pull output stage for final amplification. The output signal is then coupled to the "VOLUME" control and to the earphones of the astronaut.

A portion of the signal is taken from the push-pull output stage for use in the automatic volume control circuitry. This signal is rectified and amplified in the dc amplifier. The output of the dc amplifier is fed to an attenuating network which helps to maintain a constant signal level to the input amplifier stage. This helps to maintain a constant signal level out of the amplifier.

MICROPHONE AMPLIFIER. A signal from the astronaut's microphone is fed into the microphone amplifier input. During standby, the amplifier is inoperative. It is turned on when a ground is completed through an external Push-To-Talk switch or through a transistor switch in the circuitry. When operating, the amplifier increases the signal level enough to modulate the transmitters and the intercom bus through the isolation pads and the diode switches. The signal passes through an input amplifier and through the second

stage which is a preamplifier. The signal is developed further in a push-pull driver stage and fed to a push-pull output stage for final amplification. The output signal is fed through isolation pads to the diode switches. The signal is switched to a transmitter or to the intercom bus when the corresponding diode switches. The signal is switched to a transmitter or to the intercom bus when the corresponding diode switch is turned on from the audio control sub panel. Isolation is provided between the amplifier and the various outputs to prevent any appreciable signal from reaching an unselected output. The audio signal appearing at the intercom bus provides communication between the astronauts and between the Command Module and the GSE intercom, LEM intercom, and Data Storage Equipment input, and the Data Storage Equipment output. Audio sidetone is fed back to the input diode switching circuits to enable the astronaut to hear his own transmission.

A portion of the signal is taken from the push-pull output stage for use in the automatic volume control circuitry. This signal is rectified and amplified in a dc amplifier. The output of the dc amplifier controls an attenuating network which helps to maintain a constant signal level to the input amplifier stage and so maintain a constant output level.

VOX CIRCUITRY. This circuitry receives the same voice input signal that goes to the microphone amplifier as shown in figure 3-1. A remote "VOX SENS" control varies the input signal amplitude. Changing the position of this control determines

AUDIO CENTER

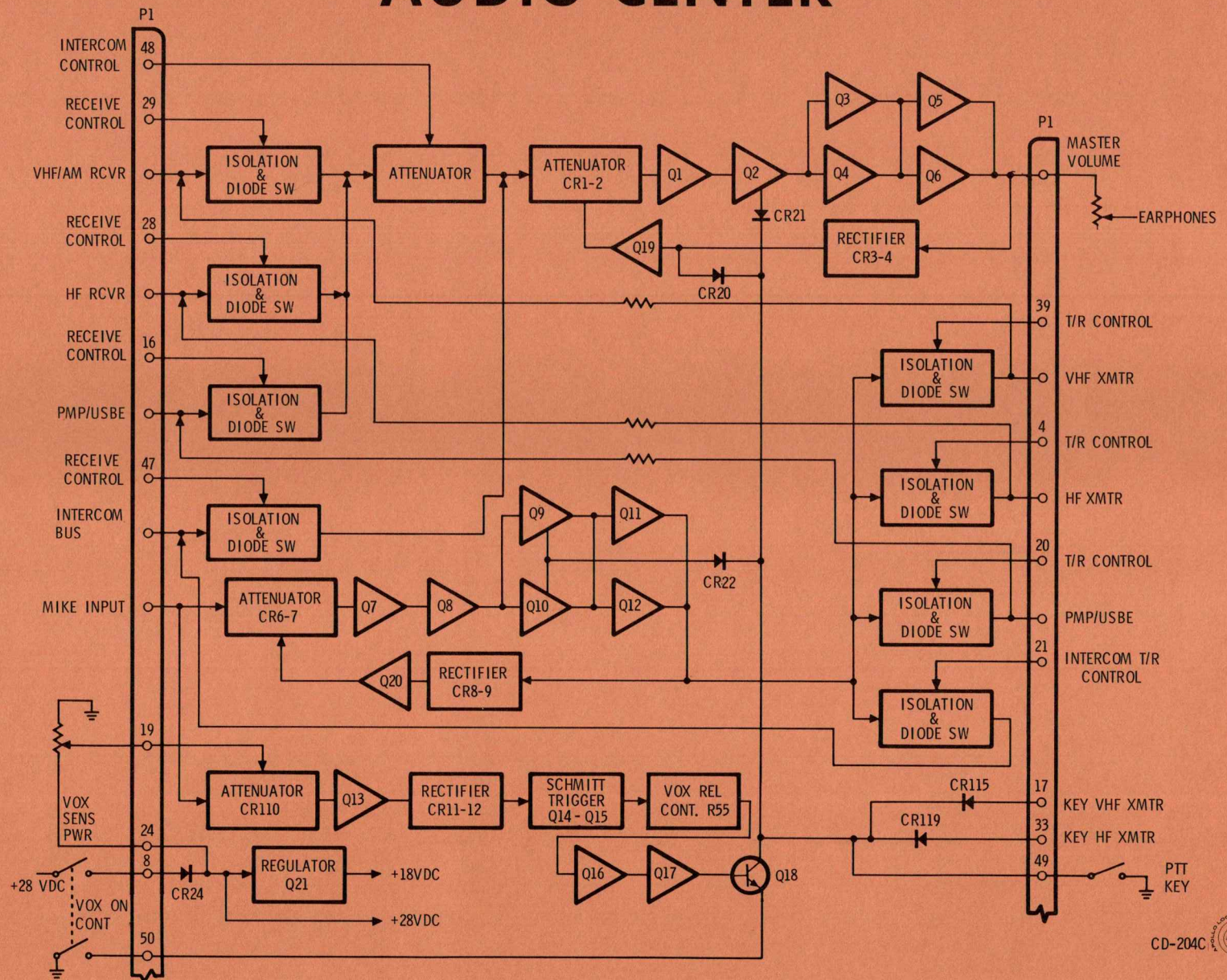


figure 3-1

CD-2040

the level of voice input signal needed to operate the circuitry. The signal is fed through an input amplifier and rectifier circuit before it is processed in a schmitt trigger circuit. The release time of the circuit is varied by an internal adjustment in the VOX release amplifier. The output from the schmitt trigger is fed through three dc amplifiers. When a sufficient signal is fed through the circuit, the final stage conducts, supplying a ground to key the HF and VHF Transmitters.

The final stage also supplies a ground to the microphone amplifier circuit, turning it on. A ground is also supplied to the earphone amplifier input stages which changes the bias condition of the preamplifier so that the sidetone is reduced below the normal level in the earphone amplifier. A ground is also supplied to the avc amplifier in the earphone amplifier circuit to prevent it from compensating for the drop in signal level in the earphone amplifier.

ELECTRICAL EQUIPMENT CHASSIS. The Electrical Equipment Chassis serves as a mounting for the three Audio Center assemblies, as well as a terminal board for the input and output lines to the unit. The three Audio Center assemblies, when mounted on the chassis, plug into three separate jacks. There are three plugs mounted on the back of the panel. One of these plugs is used to connect the unit to the spacecraft power distribution system. Signal lines are connected through another plug, and control lines from the audio control sub panels enter the unit through the third plug.

Lines requiring multiple connections are tied together on a central terminal board on the chassis. Also connected to this board and to the power lines

is an Elapsed Time meter. This meter operates at all times when power is applied to any one or all of the Audio Center assemblies. The electrical equipment chassis also contains isolation pads for LEM intercom, tape record, tape playback and GSE intercom.

DETAILED BLOCK DIAGRAM DESCRIPTION

RECEIVE AUDIO INPUTS. During normal operation, the audio inputs from the VHF/AM Receiver, the HF Receiver, the USBE Receiver and the intercom bus, enter the Audio Center at an input level of 0 dbm, which is about 10 db above the threshold signal. The input impedance seen by each receiver line is 18 k ohms at 1000 cps. Selection of the signal to be fed to the input stage of the earphone amplifier is controlled in the diode switching circuits, in turn, controlled from the audio control sub panel. Input circuits provide approximately 70 dbm of isolation between any two receiver inputs and also attenuate the earphone amplifier input to a -35 dbm level.

The input audio signal is transformer coupled to the base of the input amplifier. This is an isolation amplifier in a common-collector, or emitter follower, configuration which matches the high impedance input to the low impedance required in the preamplifier stage. The signal is taken from the emitter of the isolation amplifier stage and fed to the base of the preamplifier stage. A common-emitter preamplifier stage amplifies the signal and passes it to the coupling transformer. In turn, the transformer feeds a class A push-pull driver stage which consists of two common-emitter amplifiers. Its output is transformer coupled to the final output stage. This common-emitter, class B, push-pull

stage is transformer coupled to the "VOLUME" control on the audio control sub panel. Output level to the "VOLUME" control is +20 dbm.

AVC Circuitry

A portion of the output from the final push-pull stage is processed through the automatic volume control (avc) circuitry. This signal is coupled to a diode rectifier circuit. After rectification, the signal is applied to the dc avc amplifier whose output is processed in a diode attenuator circuit consisting of two diodes. Its purpose is to reduce the level of the signal applied to the input isolation amplifier stage. As the output from the avc amplifier increases due to an increase in the input signal level, the current through the diode attenuator increases. This increase in current reduces the impedance of the diodes and attenuates the signal at the base of the input amplifier, maintaining a fairly constant output level at the earphones over a wide range of input levels. Operation of the avc is such that the output will increase not more than 4 db when the input signal is increased 20 db from the threshold level. Approximately 50 milliseconds is required for the avc to recover its original state after an instantaneous increase in the input signal (attack time). Release time, or recovery from an instantaneous decrease in the input signal, is one second or greater. Output distortion of the audio channel with an input signal level 20 db above avc threshold is less than 6% from 300 to 3000 cps. Internal noise of the audio amplifier is at least 50 db below the output level at avc threshold.

TRANSMIT FUNCTION. After selecting the transmitter or the intercom desired, via the Audio Center controls,

the astronaut initiates communications by speaking into his microphone. The microphone output is applied to the primary of the Audio Center input transformer. During normal operation, this signal is 0 dbm, which is at least 10 db above the threshold signal. The input impedance of the microphone amplifier is 600 ohms, balanced and center tapped.

The input audio is attenuated to approximately -35 dbm and transformer coupled to the input amplifier. This is an isolation amplifier in a common-collector configuration which matches the high impedance input to the low impedance required in the preamplifier stage which follows. Here the signal is amplified and passed to the coupling transformer. The transformer couples the signal from the preamplifier to the class A, push-pull driver stage. Both common emitter push-pull stages are normally disabled, and are only turned on when keyed from either the vox circuitry or the "PTT" switch. The output of this push-pull driver stage is transformer coupled to a second stage. This stage is a common-emitter, class B amplifier, which applies its output through isolation pads and diode switches to the desired transmitter or the intercom bus. The +20 dbm signal from the final push-pull stage is attenuated in the isolation stage to a 0 dbm level and gives approximately 40 dbm of isolation between any two channels. Selection of outputs is accomplished at the Audio Center and enables the modulation signal to be fed to the VHF/AM Transmitter, HF Transmitter or the S-Band Transmitter, through the Pre-Modulation Processor. Part of the output to the transmit intercom line is fed back internally to the receive intercom line. The microphone output is connected to the intercom bus for distribution to the Audio Centers of the other astronauts. A sidetone line is connected to each of the other output circuits, except the HF

Transceiver. This line is connected to the receive audio input circuits and permits the astronaut to hear his own output signal. Also the output of the intercom bus is fed through a diode bridge attenuating network (controlled by the intercomm balance control) before it is presented to the input of the earphone amplifier. The balance control permits the astronauts to attenuate the sidetone level as well as the audio level from the other astronauts to about 9db below the level of the receiver audio.

AVC Circuitry

The action of the avc circuitry is the same as previously discussed under Receive Audio Inputs heading.

VOX CIRCUITRY. The vox function makes it possible for the astronaut to transmit without the use of a push-to-talk switch. A control on the audio control sub panel gives the astronaut the option of Push-To-Talk or vox operation. This control provides a ground to the emitter of Q18 when the vox mode of operation is desired. In either case, operation is achieved by providing a ground to the keying circuits of the transmitter and the driver stage of the microphone amplifier.

The microphone output is fed through the input transformer into the microphone amplifier. Through a diode attenuator, the input signal is fed into the vox amplifier. Variation of the "VOX SENS" control on the audio control sub panel changes the amount of current flowing through the diode attenuator and reduces the signal level passed to the vox input amplifier. Thus a decrease in sensitivity setting will cause more input signal current to be drawn by the diode attenuator, and less to be passed to the amplifier. A large voice signal then will be required to operate the amplifier. The signal level

required to energize the vox circuitry is adjustable between +10 and -10 dbm. The attack time of the vox circuitry is 50 milliseconds or less; the release time of the vox circuitry is adjustable from 1.2 to 6 seconds. The input signal, after the desired attenuation, is passed to a common-emitter vox amplifier, and it is then rectified in a diode rectifier. The output of the rectifier is applied to a schmitt trigger circuit. After the signal has reached a required level it causes the schmitt trigger circuit to turn on. When the schmitt trigger conducts, its output rises very rapidly and is applied to the base of the next stage which is a dc amplifier. In rapid succession, the following two dc amplifiers conduct. When the last stage conducts, it supplies a ground to the key lines of the transmitters, triggering them into the transmit mode of operation.

When the voice signal applied to the vox circuit ends, the schmitt trigger turns off. The vox release circuit, whose delay time is adjustable from 1.2 to 6 seconds, prevents the final dc amplifiers from turning off until an RC time constant circuit has discharged sufficiently. When the dc amplifiers are turned off, the ground is removed from the keying relays in the transmitters.

When the external Push-To-Talk switch is actuated, a ground from the push-to-talk circuit is applied to the transmitter enabling operation.

DIODE SWITCH OPERATION. The astronaut is able to control the inputs to, and the outputs from, his Audio Center assembly by using the controls on the audio control sub panel. The transmitter and receiver inputs to the Audio Center assembly are connected to diode switches controlled from the audio control sub panel. A control ground is provided at the panel for use in these circuits.

The simplified schematic, figure 3-2, shows the equipment in the off mode. A bias voltage of +18 volts dc is applied to the center tap of two transformers, T-1 and T-2, and +28 volts dc bias is applied through R-9 to the switch circuitry. Diodes CR-1, CR-3, CR-4 and CR-5 are back-biased by the application of the bias voltages. The switch will provide the ground required to forward bias the diodes allowing them to pass the audio signals from the receiver, or to the transmitter.

When the switch is placed in the T/R position, a ground is furnished to both transmit and receive control circuits. Signals may pass through diodes CR-1, CR-3, CR-4 and CR-5, as they are now forward biased through resistors R-3, R-4, and also CR-2, R-5, and R-6, to ground.

When the switch is in the REC position, a ground is furnished to only the diodes in the receive diode switch, CR-4 and CR-5. Operation of the diode switch in the transmit circuit is prevented by the diode CR-2, which is biased in the reverse direction. Thus, only the receiver will pass audio signals to the Audio Center assembly, while the output of the microphone amplifier will be off.

Resistors R-7 and R-8 attenuate the input signal from 0 dbm to the desired level for input to the earphone amplifier. Resistors R-2 and R-12 reduce the +20 dbm output level from the microphone amplifier to the 0 dbm level which is required by the transmitter. Capacitors C-1, C-2, C-3, and C-4 prevent actuation of the control circuitry by the dc voltage when the switch is in the off position. A sidetone line connects the transmit switch back to the receive switch through resistors R-10 and R-11, which act to attenuate the signal in the same manner

as R-7 and R-8. The low level of the receiver output, plus the attenuation provided by R-10 and R-11, will keep the received signal from activating the transmitter circuits.

DIODE SWITCHING, AUDIO CENTER

SIMPLIFIED SCHEMATIC

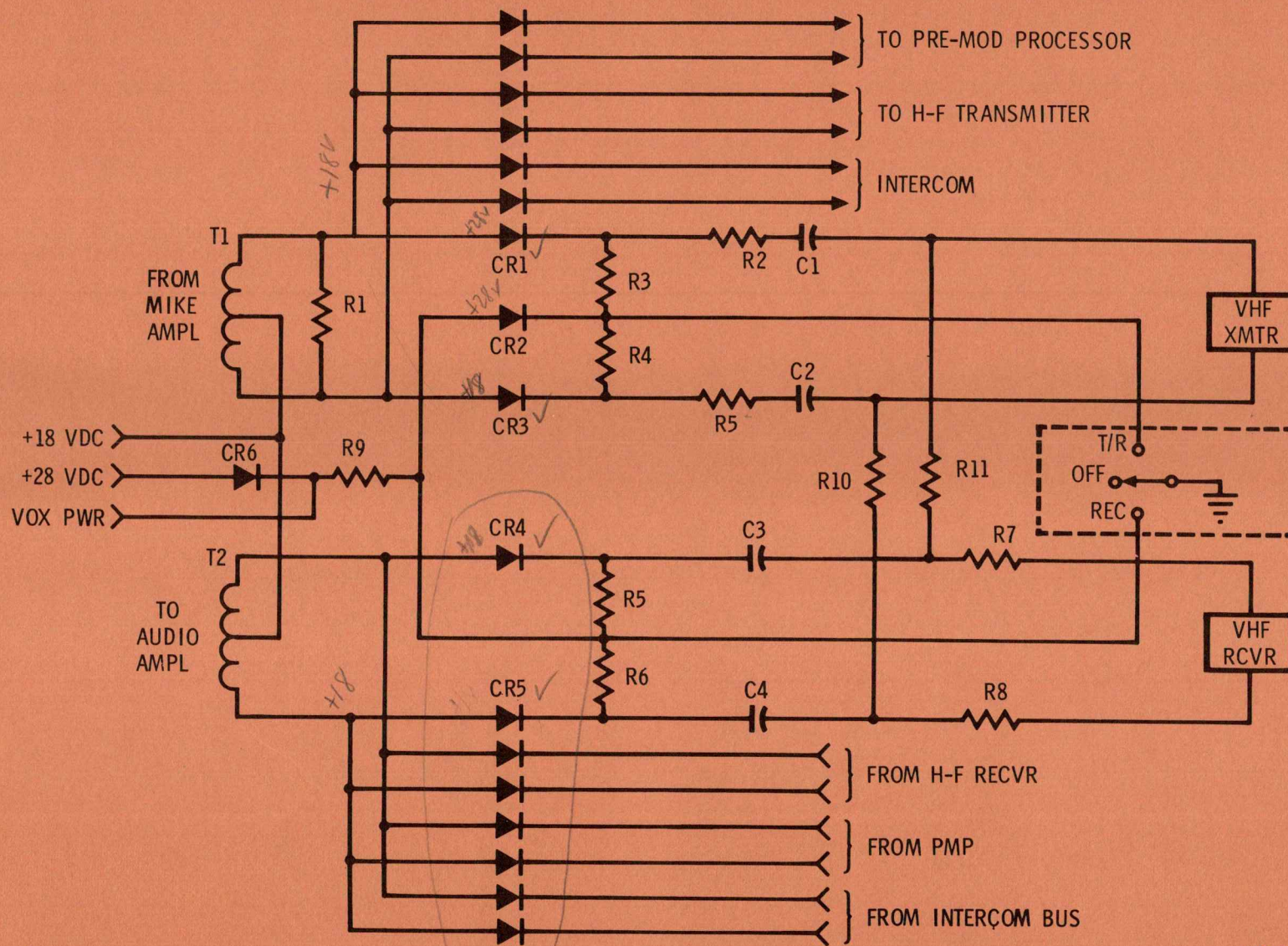


figure 3-2

SECTION IV

VHF/AM TRANSMITTER-RECEIVER

INTRODUCTION

The VHF/AM Transmitter-Receiver provides voice communications between the Spacecraft and external equipment. The equipment is capable of simplex and duplex operation. In simplex operation, the equipment transmits and receives on 296.8 mc. In duplex operation, the equipment transmits on 296.8 mc and receives on 259.7 mc. The duplex mode of operation is used for communications with the LEM.

The VHF/AM Transmitter-Receiver consists of three modules that are mounted on a common chassis with the VHF Recovery Beacon. The weight of the VHF/AM Transmitter-Receiver is 7.4 pounds with a volume of 205 cubic inches. The power input is 16.5 watts in standby, 1.5 watts in receive, and 50 watts in transmit and receive. The transmitter output is 5 watts into a nominal 50 ohm resistive load. The equipment is located in the Lower Equipment Bay of the Command Module. The controls are located on the communications Control panel, number 20.

BLOCK DIAGRAM DESCRIPTION

The functional flow diagram depicted on figure 4-1 illustrates the VHF/AM Transmitter-Receiver. This diagram will be referenced in the discussion of the operation of the equipment.

RECEIVER OPERATION. The receiver (upper portion of figure 4-1) consists of two modules, an amplifier module and a power supply module. Operation of the receiver is controlled by two switches on the

communications control panel. Placing the "VHF/AM MODE" switch to either the REC or T/R position applies 28 volts dc to the receiver power supply. The position of the "VHF/AM RCVR" switch selects the receiver frequency to be employed. The NORM position selects the simplex mode of operation and uses the primary communications frequency of 296.8 mc. The front end of receiver number one is connected to the VHF Multiplexer through the ptt relay in the transmitter module. The LEM position selects the receiver frequency of 259.7 mc that is used in duplex operation. The front end of receiver number two is connected directly to the VHF Multiplexer. The "VHF/AM" switch on the Audio control sub panel must also be in either the REC or T/R position. The switches on the audio control sub panel are independent of the switches on control panel number 20. They only control switching within the Audio Center.

The receiver frequency chosen through operation of the "VHF/AM RCVR" switch is passed from either the SCIN or the Recovery antenna, through antenna switching and the VHF Multiplexer, to the VHF/AM Transmitter-Receiver. The simplex signal is fed through the ptt relay in the transmitter; the duplex signal is fed directly to the receiver front end. The signal is amplified in two amplifier stages and applied to a mixer stage with the output of the oscillator-tripler. The oscillator-tripler, Q-5, for receiver no. 1 consists of a crystal oscillator operating at 108.9333 mc and a tuner that passes the third harmonic of the oscillator, providing an output of 326.8 mc. The crystal oscillator in receiver no. 2 operates at 96.5666 mc, and

VHF/AM RECEIVER

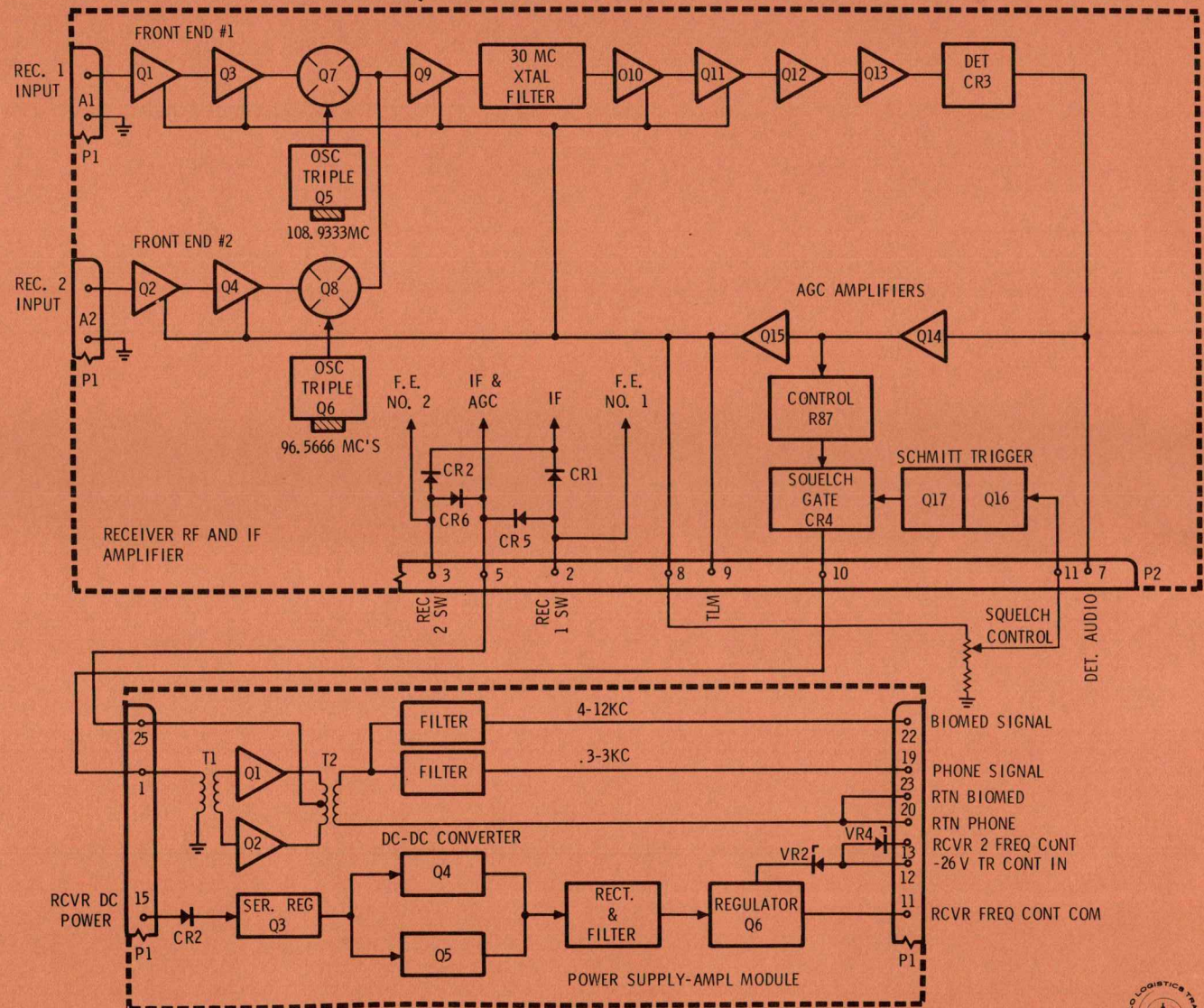


figure 4-1

VHF/AM TRANSMITTER

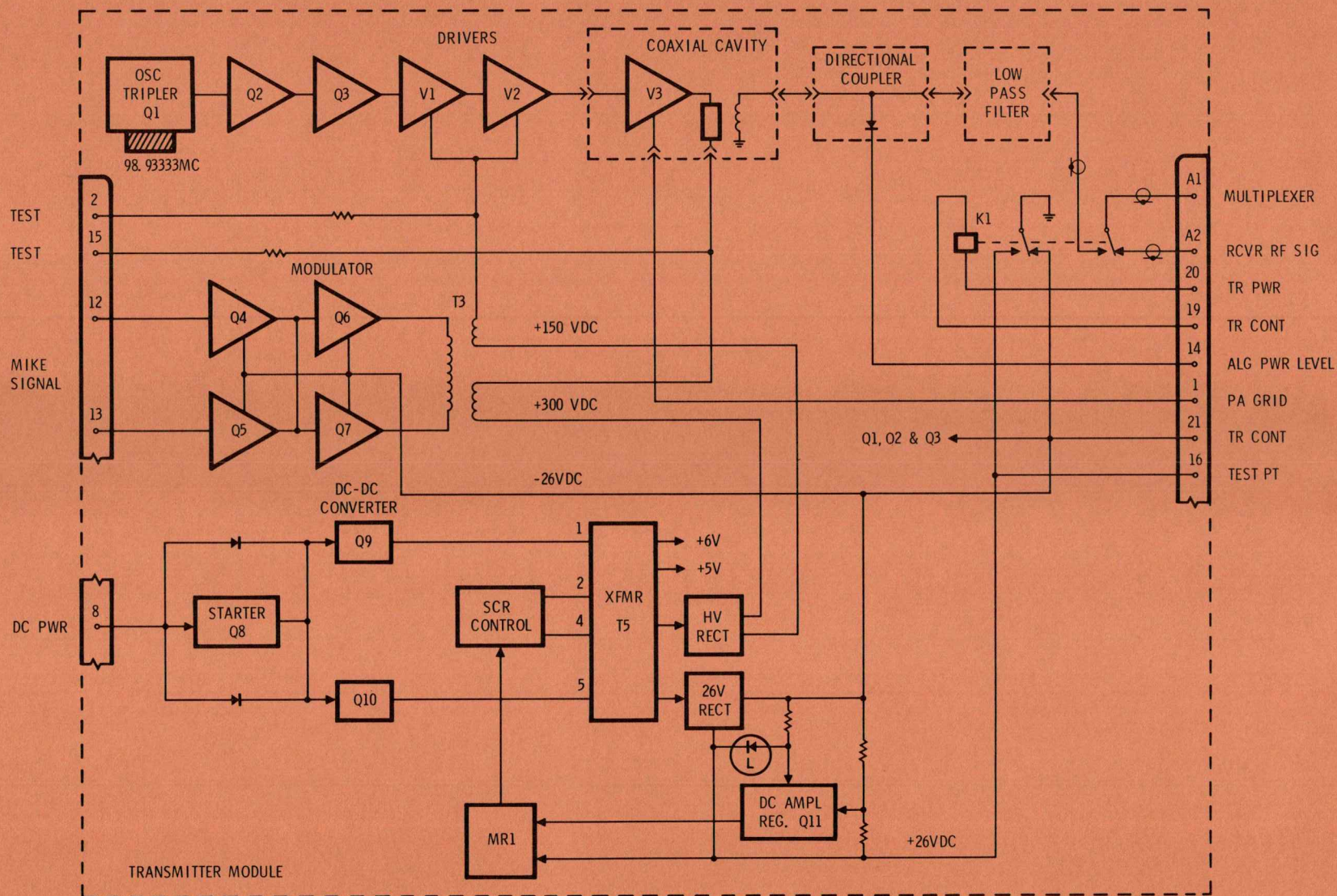


figure 4-1A

CD-114B



provides a multiplied 289.7 mc output from the oscillator-tripler, Q-6. The output of the oscillator-tripler in either receiver injects a frequency into the mixer that is 30 mc higher than the received frequency. The mixer output of 30 mc is then fed to the first stage common to both receiver front ends, i-f amplifier Q-9, and passed through a 30 mc crystal filter. The filter allows further selectivity. The signal is again amplified and filtered in four amplifier stages Q-10, Q-11, Q-12, and Q-13 before it is presented to the detector, CR-3. This stage demodulates the 30 mc signal and applies the audio output to a squelch gate, Q-18. The squelch gate is normally turned off, but when the level of the signal becomes great enough, the squelch gate will conduct and pass the audio signal to the push-pull amplifiers Q-1 and Q-2, in the power supply module. The audio output from the push-pull amplifier is then routed to the Audio Center for amplification and switching. Audio outputs are taken from the detector stage and the push-pull amplifier for routing to test connectors.

Squelch Control

A "VHF/AM SQUELCH" control is mounted on control panel number 20 and is used to vary the squelch setting of the receiver. The squelch circuitry is carrier-operated, and controlled by the level of the agc signal at the output of agc amplifier, Q-15. When minimum squelch is used, amplifier Q-17 of the schmitt trigger circuit is operating, and the squelch gate, Q-18, is conducting, permitting the audio to pass to the output. When the squelch is increased, the base bias on Q-16 increases, causing Q-16 to conduct and Q-17 to cut-off. When Q-17 cuts off, Q-18 will no longer conduct, and the audio is not passed to the output.

In order for the audio to be heard, the carrier level must be high enough to change the state of the schmitt trigger circuit. This is achieved when the agc output voltage goes down. This decrease reduces the voltage on the base of Q-16, cutting it off, and causing Q-17 to conduct. This again turns on the squelch gate, and allows the audio signal to pass to the output.

An agc voltage is taken from the detector stage and amplified in two agc amplifiers Q-14 and Q-15. This action reduces the voltage output from Q-15 which is then fed back to the indicated stages (figure 4-1) of the receiver to help achieve a constant level output for the receiver. A portion of this voltage is also used to feed the squelch circuitry.

Power Source

Power for the receiver is provided by the EPS Flight and Post Landing bus through circuit breakers. The +28 volts dc input is fed to a series regulator and transient suppressor stage, Q-3, in the power supply module, where a regulated input to the dc to dc switcher is obtained. The switcher stage, Q-4 and Q-5, is a saturable reactor that is used to transform the input +28 volts dc to +15 volts dc. The output square wave of the dc to dc switcher is passed through a full-wave rectifier and a filter, providing 15 volts dc at the output terminals of the module.

This power is applied to the "VHF/AM RCVR" switch. At this switch, the selection of receiver front ends is made. Selection of the LEM (receiver number two) position applies +15 volts dc to switch Q-7 as shown on figure 4-2. Transistor Q-7 conducts

VHF/AM RECEIVER SWITCHING 'D' MODEL

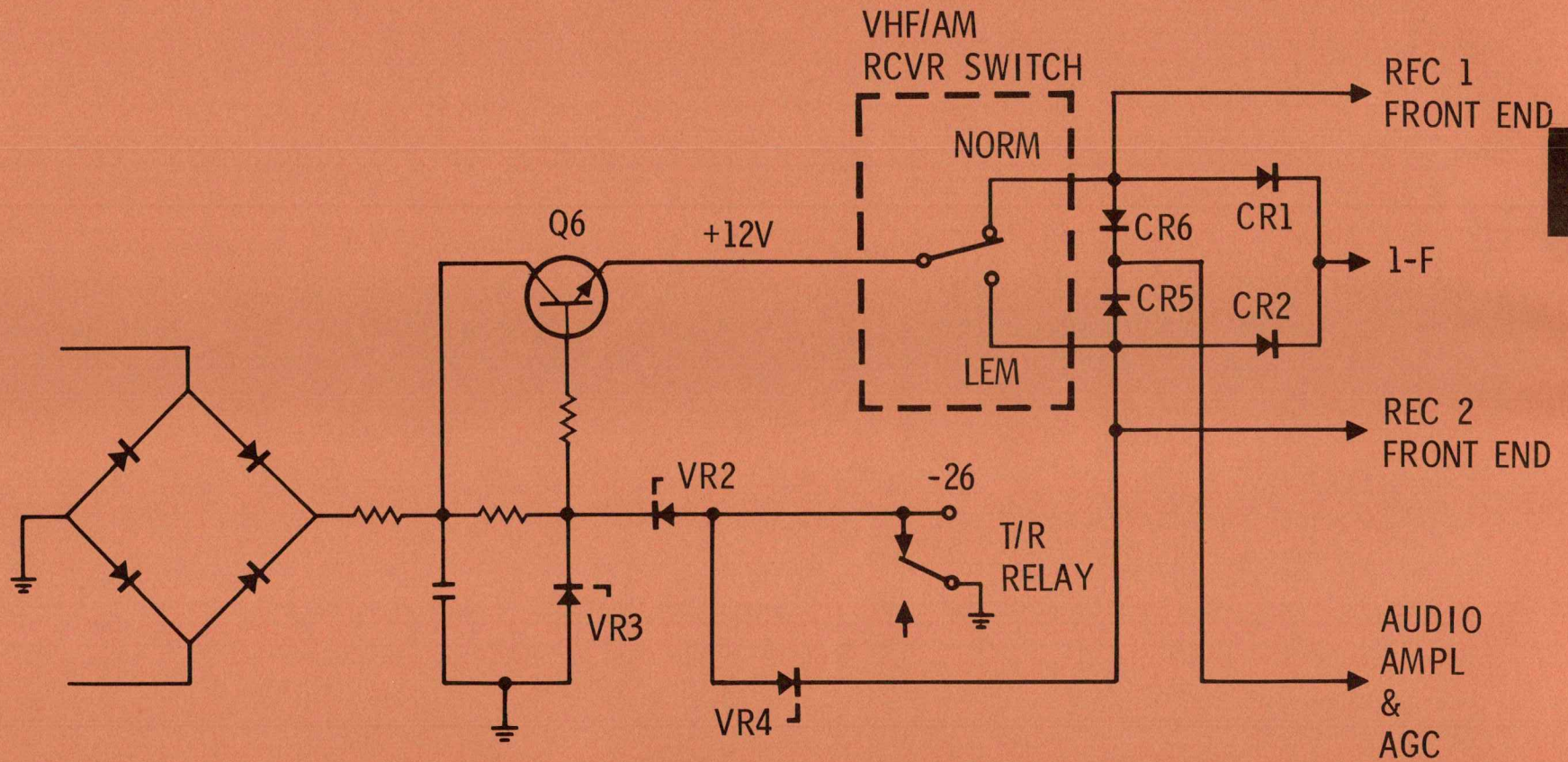


figure 4-2

CD-134B



and applies a regulated +12 volts dc to the receiver bias circuits. When the switch is in the NORM position, the bias circuits of receiver number one will be similarly activated through Q-6. This switch also has the capability of being turned off when the transmit ptt relay is actuated. In this case, +26 volts dc from the transmitter power supply causes Q-6 to turn off, disabling the receiver circuits. When the ptt relay is deactivated, the +12 volts dc is again applied to the receive number one circuits, making reception on 296.8 mc possible.

TRANSMITTER OPERATION. Referring again to figure 4-1, it can be seen that in the transmitter module an audio signal is obtained from the using astronaut's Audio Center assembly. The audio input to the transmitter is gated on by positioning the "VHF/AM" switch on the audio control sub panel to the T/R position. Power is applied to the transmitter when the "VHF/AM MODE" switch on control panel number 20 is placed in the T/R position. The audio signal, entering the transmitter module at a 0 dbm level, is applied to a push-pull amplifier stage, Q-4 and Q-5, and then coupled to a push-pull modulator, Q-6 and Q-7, for further amplification. The modulator output is applied in series with the plate supply voltages to driver V-2 and power amplifier, V-3.

The rf signal in the transmitter is generated by a crystal oscillator operating at 98.9333 mc in a resonant base-emitter circuit. The collector circuit of the oscillator is tuned to pass the third harmonic, 296.8 mc, while rejecting other frequencies. The output of this stage is amplified in a grounded emitter rf amplifier, Q-2, and a grounded-base rf amplifier, Q-3. The signal is further amplified by drivers V-1 and V-2 to the level necessary to drive the power amplifier, V-3. Each of these stages

is a grounded-grid amplifier that is tuned to pass the 296.8 mc transmitting frequency. Power amplifier, V-3, uses a coaxial cavity for the plate tank circuit.

Amplitude modulation of the rf signal is accomplished by plate modulating driver V-2 and power amplifier V-3.

The signal from the tuned cavity is passed to a directional coupler that measures the forward power from the transmitter. Its output signal is fed through a low-pass filter to the T/R relay and then to the VHF Multiplexer. The output of the VHF Multiplexer is fed to the selected antennas.

Power Source

The transmitter operates from the +28 volts dc provided by the EPS Flight and Post Landing us. The power supply circuit has a constant efficiency, and accomplishes regulation by, in effect, changing the transformer turns ratio. In the transmitter module the converter starter, Q-8, initiates operation of the converter and then becomes an inactive portion of the circuit during normal operation. The dc to dc converter, a saturable reactor, takes the input voltage and provides the required output voltage through transformer, T-5. Outputs from the transformer include:

1. 5 volt square wave for the filaments of V-3
2. 6 volt square wave for the filaments of V-1 and V-2
3. +150 volts dc driver plate voltage
4. +300 volts dc final power amplifier plate voltage

5. ± 26 volts dc for modulator power, power amplifier bias and transistor amplifier supply voltage.

These voltages are regulated for power input variations between 24 and 30 volts dc.

The +26 volt dc output is also used in the regulation of the power supply. The output of this line is sensed by the dc amplifier regulator, Q-11. If the voltage is not +26 volts dc, the regulator circuitry acts to alter the silicon controlled rectifiers, thus maintaining the output at +26 volts dc. If this voltage is properly adjusted, the other outputs from transformer T-5 will also be correctly regulated.

The transmitter operating mode is determined by the operation of the transmitter ptt relay, K-1. In receive operations, the line to the antenna, through the VHF Multiplexer, is connected to the receiver by K-1. K-1 also removes the applied power from the exciter and modulator stages. When the ptt relay is actuated, the antenna line is switched to connect the transmitter to the VHF Multiplexer. The relay removes the ground from the -26 volt dc line, providing power to the exciter and modulator stages, and to the receiver switch in the amplifier module of the receiver. This enables the transmitter, and prevents reception unless the equipment is in the duplex mode.

Several test parameters may be measured at the test connector. These include points for monitoring the +300 volts dc, +150 volts dc, -26 volts dc and +26 volts dc supply voltages. Test points are also available for power amplifier grid tests and transmitter power output monitoring.

SECTION V

VHF MULTIPLEXER

The compact design of the spacecraft requires that all vhf communications and data channels be operated in conjunction with a single vhf antenna. The VHF Multiplexer is utilized to allow simultaneous connection and operation of six vhf transmitters and receivers with a single antenna system.

INTRODUCTION

The VHF Multiplexer 635Q-1E (figure 5-1) is an airtight, rigid box of dipbrazed aluminum construction. The sides and top of the box chassis are further stiffened and thermally insulated by the use of integral, sandwiched aluminum-honeycomb panels. The top and bottom covers and a rear connector panel can be removed for parts installation and tuning. The covers and rear panel are each gasket-sealed along all edges to make the chassis airtight. The multiplexer is purged and charged with nitrogen gas. The interior and exterior of the chassis are gold plated, allowing increased conductivity and resistance to corrosion. The weight of the unit is 12 pounds and it is located in the Lower Equipment Bay.

The interior of the multiplexer chassis is divided into 15 tuned cavities. Each cavity contains an adjustable pedestal assembly. A tuning disc at the top of each pedestal allows tuning of the cavity for resonance at the desired frequency. The 15 cavities are grouped to operate as 6 bandpass filters, one filter for each channel. Either two or three of the tuned cavities are needed for each channel filter, depending upon the desired shape of the passband. An input or output connection for

each cavity is provided by capacitive coupling between the inner post of the pedestal assembly and a coupling disc mounted in the top cover of the chassis. Coupling between two cavities of the same channel filter is provided by a semi-circular opening (aperture) in the common cavity wall, at floor level.

FUNCTIONAL DESCRIPTION

The VHF Multiplexer is a six channel filter device. The multiplexer contains no active components and requires no power supply. Adjustments are provided for tuning each channel filter to resonance and for obtaining optimum values of insertion loss and voltage standing wave ratio (vswr). The multiplexer is tuned at the factory and then sealed. No tuning adjustments are required for installation or operation.

Figure 5-2 is a schematic diagram of the multiplexer. The six bandpass filters shown are an integral part of the mechanical construction of the multiplexer chassis. Each filter is tuned to a different channel frequency. Six different vhf/uhf equipment items are connected to the inputs of the channel filters. The common output of the filters is connected to a broadband vhf antenna. All equipment connected to the input of the multiplexer may operate simultaneously, either transmitting or receiving, over the common antenna. The frequency range of the multiplexer is 225 to 450 mc and the operating frequency of each channel is as listed below.

TYPE 635Q-IE EXPLODED VIEW



5-2

VHF MULTIPLEXER, SCHEMATIC DIAGRAM

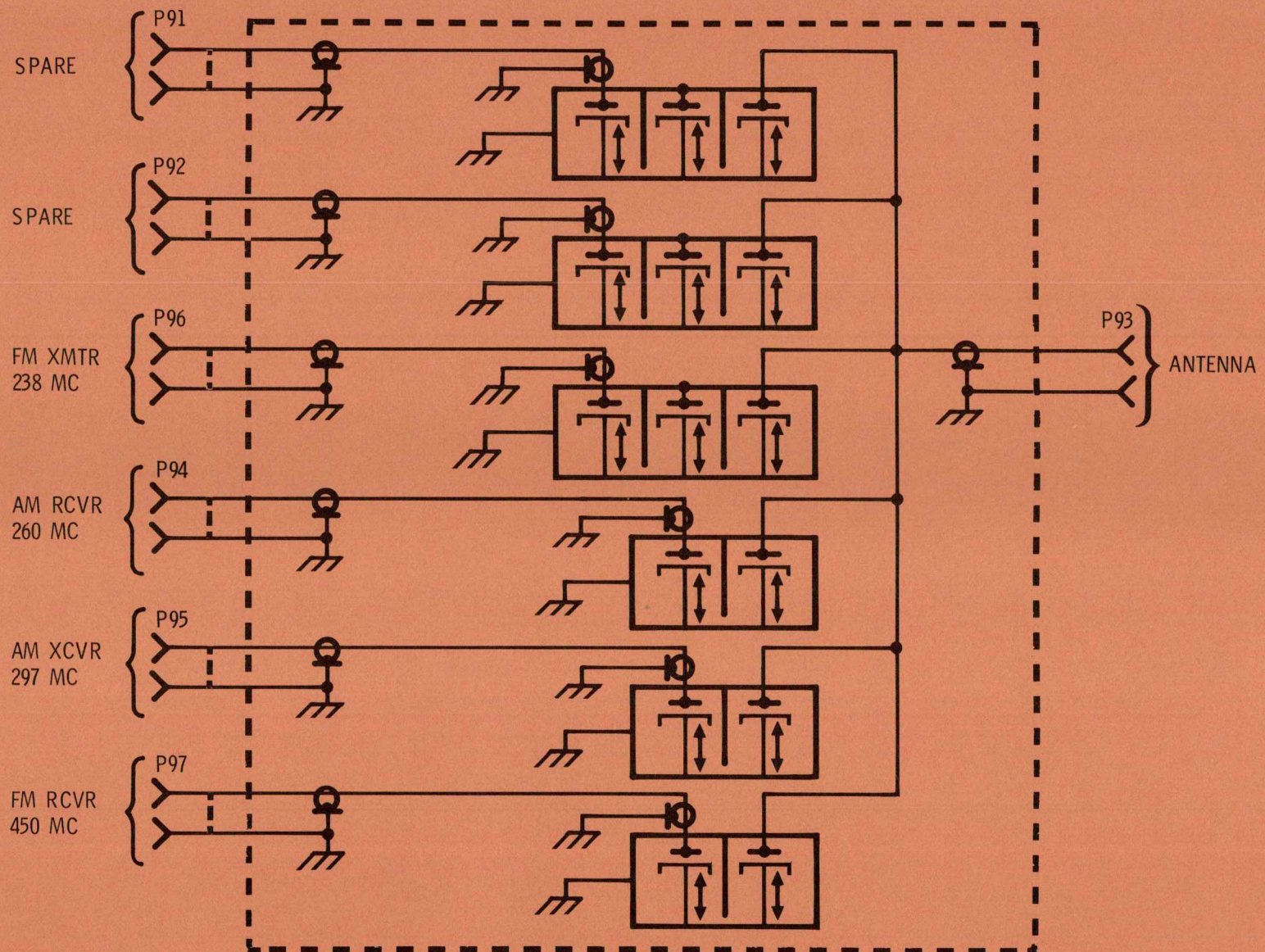


figure 5-2

Channel	Equipment	Frequency
1.	VHF/AM Transmitter-Receiver	296.8 mc
2.	VHF/FM Receiver	259.7 mc
3.	VHF/FM Transmitter	237.8 mc
4.	SPARE	
5.	NASA R&D Transmitter	247.3 mc
6.	UHF/FM Receiver	450.0 mc

With the output connections terminated in a matched 50 ohm load, the vswr is a maximum of 1.5:1. The 3db band-width of each of the six channels is a minimum of 1 mc. The isolation between channels is proportional to their frequency separation. The passband insertion loss of each channel, measured at the center frequency of the pass band, is a maximum of 1.5db. The multiplexer is capable of simultaneously carrying 15 watts continuous power on channels 3 and 5, 10 watts on channel 1, and 100 watts of peak pulse power on channel 4.

OPERATION

In the multiplexer each channel filter, composed of two or three tuned cavities, functions as a shorted coaxial transmission line, approximately one-tenth of a wave-length long. The outer conductor is represented by the square walls of the cavity. The floor of the cavity shorts the coaxial section. The inner conductor is terminated on the open-circuited end and an adjustable tuning disc.

Figure 5-3 shows a simplified cross-sectional view of a typical cavity in the multiplexer chassis. The dotted lines and symbols indicate the equivalent electrical circuit of the cavity. These equivalent circuit elements will be used to explain the operation of the cavity as a parallel resonant circuit. Cavity inductance is resonated by disc capacitance,

and to a lesser extent, by the coaxial capacitance. Disc capacitance can be varied by adjusting the spacing between the tuning disc and the top cover. Coaxial capacitance is relatively fixed for various positions of the inner post, and it is therefore represented as a fixed capacitance. Input and output coupling for the cavity is provided by post capacitance. This coupling can be varied by adjusting the spacing between the inner post and a fixed, insulated, copper disc in the top cover of the multiplexer. Coupling to an adjacent cavity is provided by a semi-circular aperture in the common cavity wall. Coupling bullets of different sizes are used to adjust the coefficient of aperture coupling to the desired value. Figure 5-4 shows the equivalent circuit for a typical three cavity, channel filter. The dotted lines on figure 5-4 represent energy transferred between sections of the channel filter by intercavity aperture coupling. Input and output coupling for the filter is changed by adjusting post capacitance in the first and last filter sections. In the center section, the post and disc capacitances are paralleled by shorting the coupling disc to the top of the cavity. Disc capacitance is adjusted to tune the filter section to parallel resonance at the assigned channel frequency. The complete three section filter has a 3db passband of 1 megacycle or more, for an assigned channel frequency in the range from 225 to 450 mc.

EQUIVALENT CIRCUIT FOR TUNED CAVITY OF MULTIPLEXER

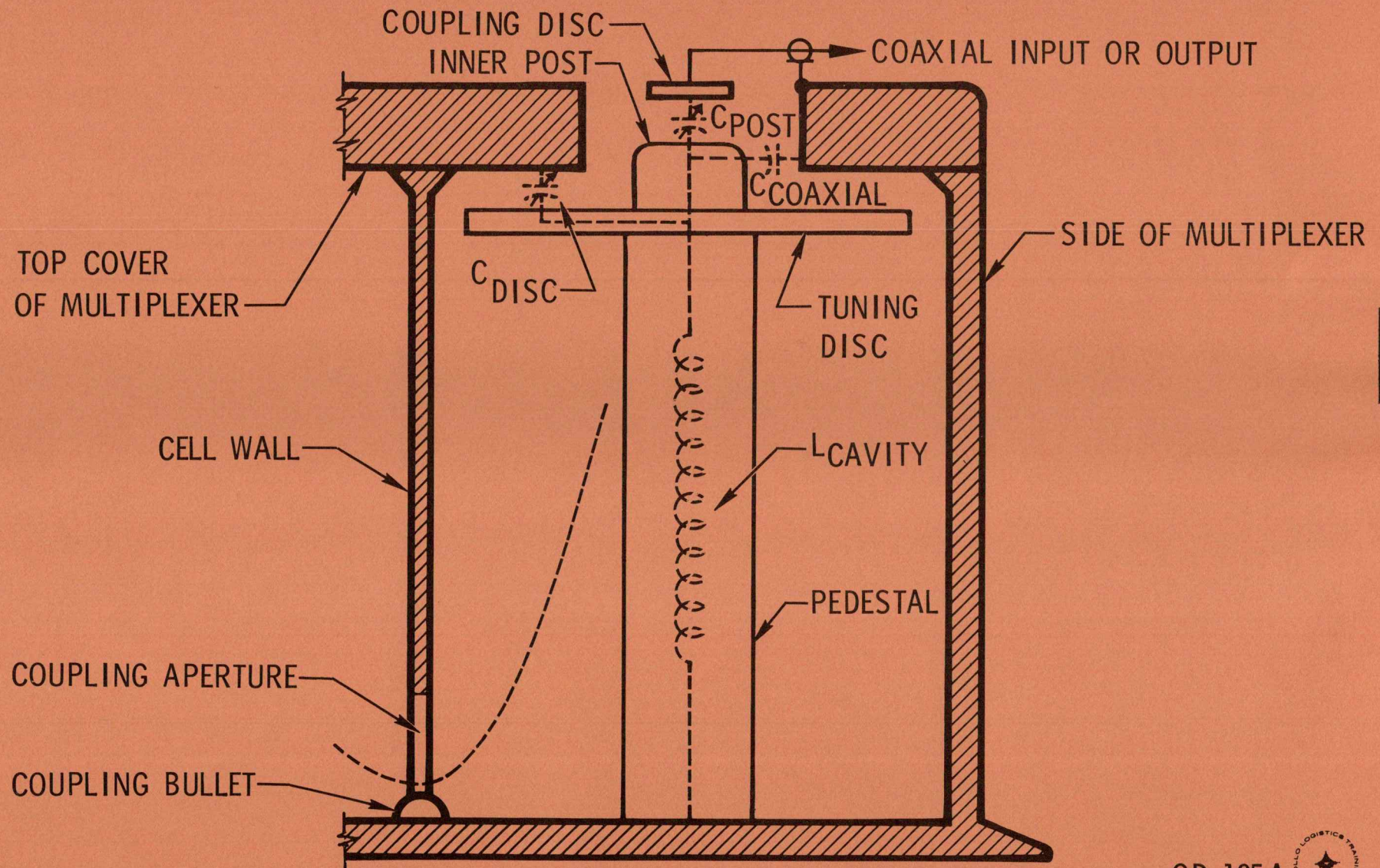


figure 5-3

EQUIVALENT CIRCUIT FOR THREE-SECTION CHANNEL FILTER OF MULTIPLEXER

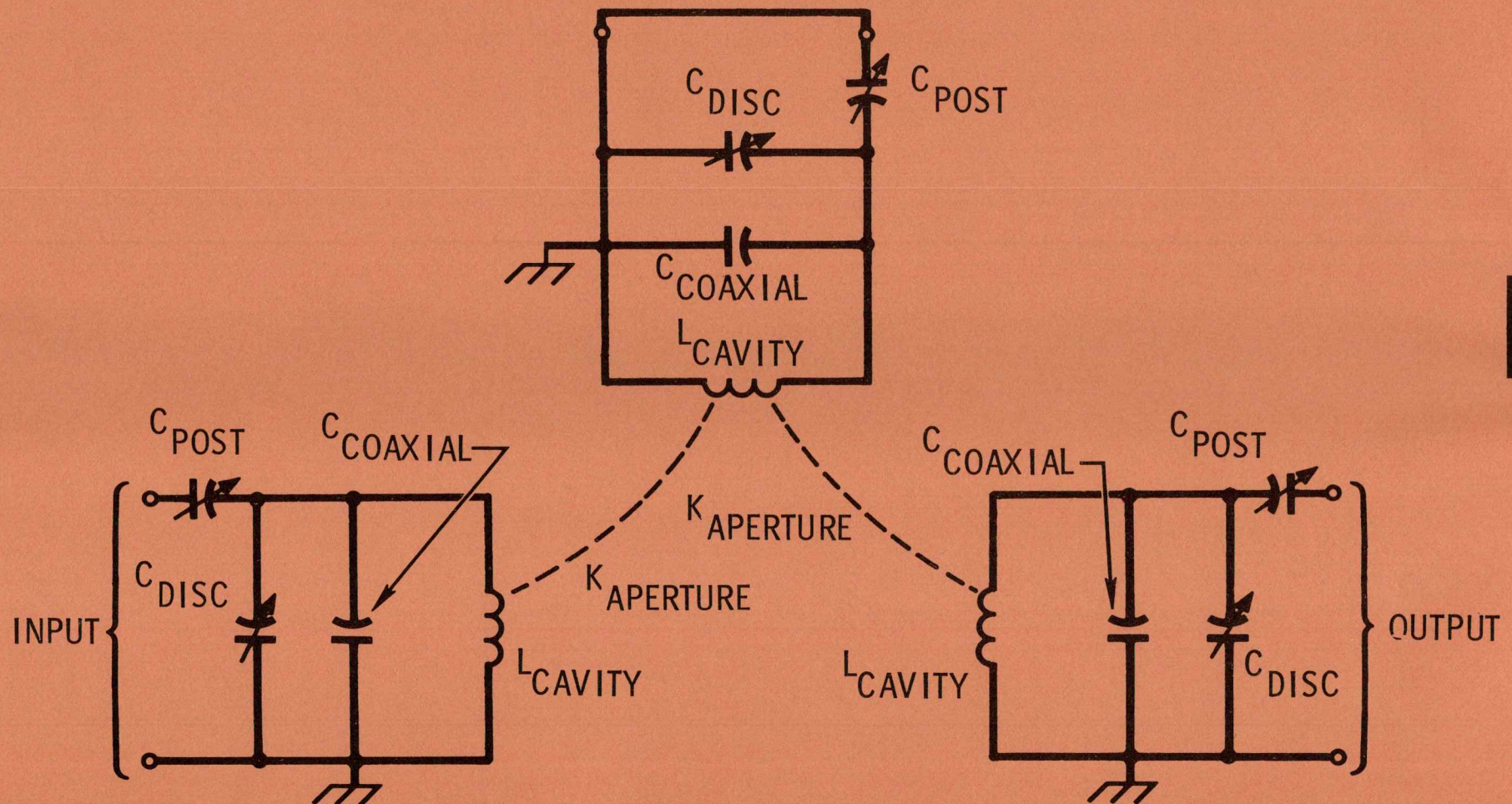


figure 5-4

SECTION VI

OMNI ANTENNAS

6.1 INTRODUCTION

Omni antenna refers to the characteristic of an antenna to radiate energy in all directions. The antennas can be of different construction and physical appearance and still be classified omni because of their radiation patterns. Therefore, when the term omni is used, it refers to radiation patterns and not construction.

6.2 SCIMITAR ANTENNA

The scimitar antenna derives its name from the characteristic shape of the antenna, as shown in figure 6-1. This type of antenna was chosen for its broad band radiation ability. The antennas protrude from the side of the C/M. There are two of these antennas located on the Z axis as seen in figure 6-2. The antenna on the -Z axis will survive entry as it is located at a minimum heat point. The antenna located on the -Z axis is referred to as the upper antenna; the one on the +Z axis is referred to as the lower antenna. Antenna selection is made from a switch located on control panel 17. Each antenna radiates in a hemisphere about the axis on which it is located.

The scimitar antenna has two distinct functional sections, a VHF section and a 2 kmc section. The 2 kmc section is the notch portion of the scimitar. Because of this distinct feature, an acronym is used to describe the antenna. SCIN, pronounced "sin", is a combination of SCimitar and Notch.

The VHF portion of the SCIN has a band width of 225 to 450 mc. This is possible because of the shape of the antenna. The antenna is 0.02 inches thick and is covered with fiberglass for protection. The 2 kmc portion is a notch which exhibits the characteristics of a half wave dipole and has a band width of 2100 to 2300 mc.

6.3 RECOVERY ANTENNAS

There are three recovery antennas, two VHF and one HF. The antennas are located as shown in figure 6.2. The VHF antennas are automatically deployed after main chute deployment. The HF antenna is deployed after landing.

6.3.1 VHF Recovery

The VHF recovery antennas are 9 inch blade type antennas which act as quarter wave length stubs. They are located, as shown in figure 6-2, in the forward equipment compartment. Upon deployment of the main parachutes, two time delayed, pyrotechnic line cutters are activated. After 8 seconds the line cutters sever a restraining cord and the spring loaded antenna assemblies swing up to their up-right position.

The antenna located next to longeron #2 is connected to the VHF Recovery Beacon and is designated antenna #1. Antenna #2 is located next to longeron #1 and is connected via a switch to the VHF multiplexer.

VHF/2KMC SCIN ANTENNA

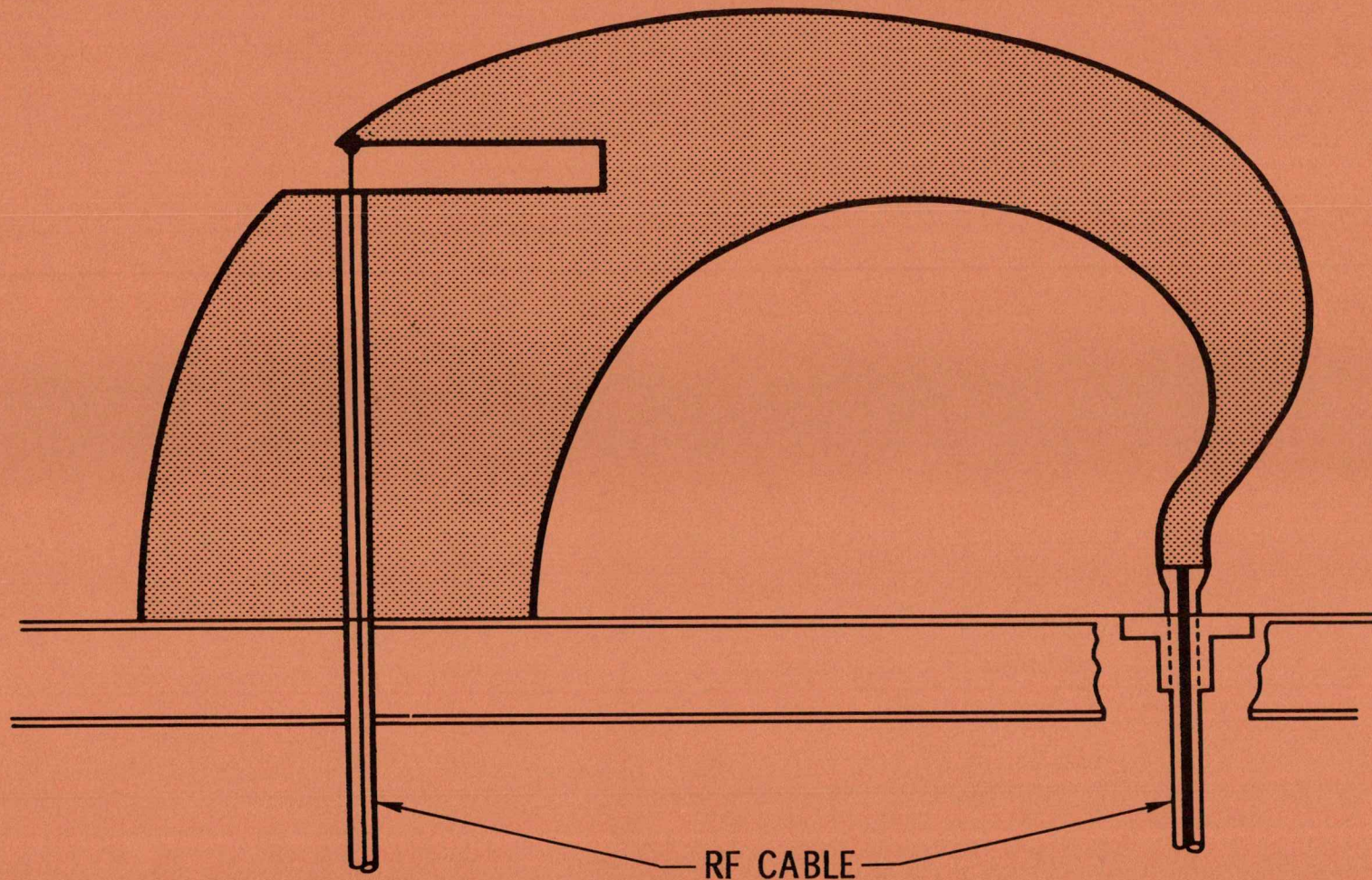


figure 6-1

CD-117A



COMMUNICATIONS SYSTEM

ANTENNA EQUIPMENT GROUP

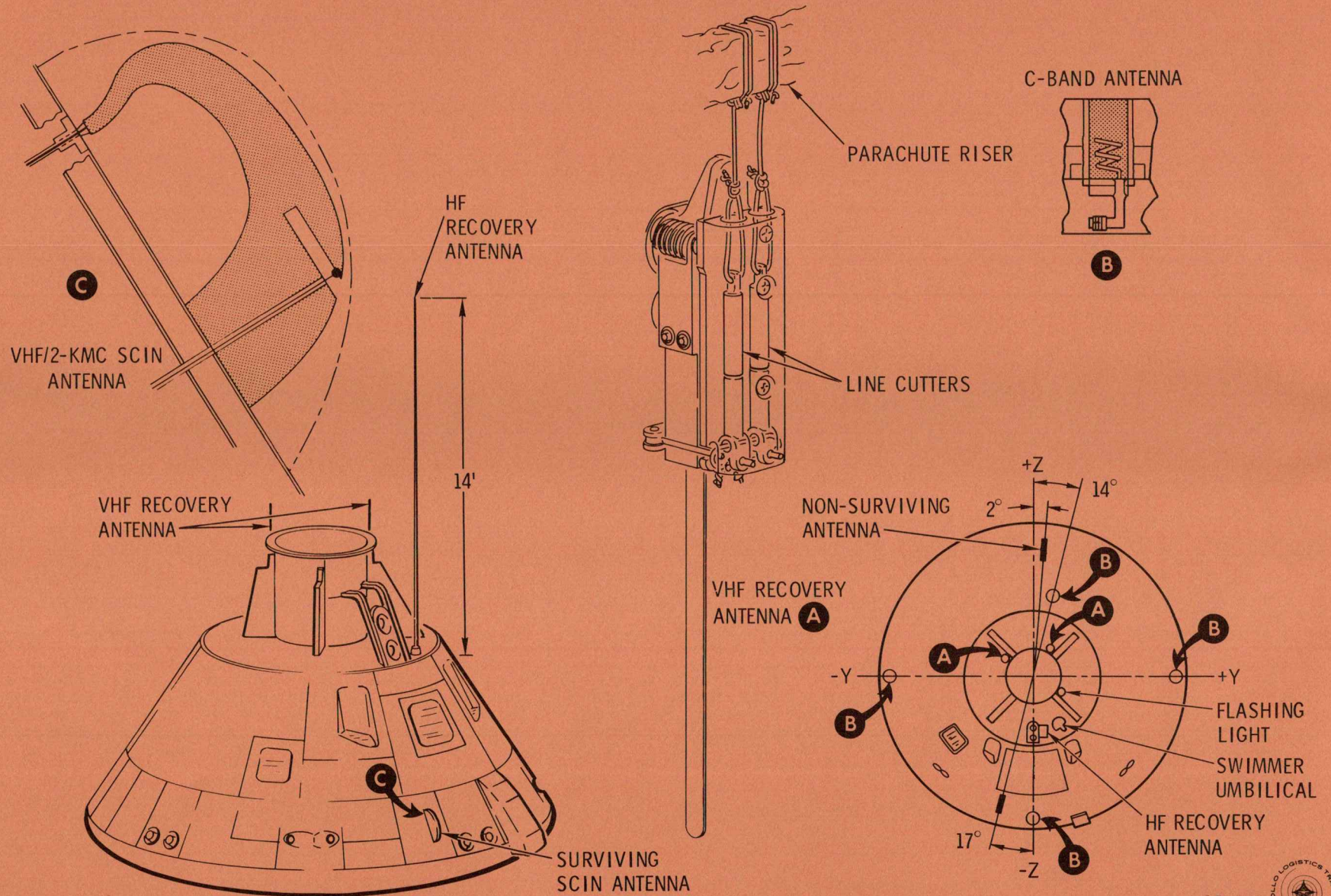


figure 6-2

CD-17B



6.3.2 HF Recovery

The HF recovery antenna is a one-eighth wave length whip antenna 12.75 feet long. Located next to the tip is a curved portion; this is for stowage purposes. The antenna is located between the +Y and -Z axis just off of the -Z axis.

SECTION VII

SIGNAL CONDITIONING EQUIPMENT

The function of the telemetry system is to receive data from a multitude of sources and convert these data into a time-shared, serial-digital output. The telemetry system is comprised basically of a measuring system, signal conditioning equipment and the PCM Telemetry Equipment. The measuring system consists of those various sensors and transducers that measure the physical status of the spacecraft structures and systems. These are eleven major divisions or types of measurements in the Apollo spacecraft: strain; vibration; flow; acceleration; acoustic; char; ablation; pressure; heat flux; leak detection, and temperature. The proper evaluation of data provided by the measuring system can indicate correct functioning of spacecraft systems and structures or, more important, can give warning of malfunction and possible failure of the various systems and structures under observation, so that timely corrective procedures might eliminate what would otherwise be a mandatory abort or failure situation. The function of the Signal Conditioning Equipment is to accept signals from a variety of sensors and convert these signals to a zero to 5 volts dc level. The Signal Conditioner Equipment consist of d-c amplifiers; attenuators; frequency-to-dc converters; variable resistance-to-dc converters; phase sensitive demodulators; dc-to-dc converters, and a power supply. Refer to Figure 7-1.

The Signal Conditioning Equipment of the Apollo Communications and Data Subsystem, is designed to process inputs from spacecraft sensors and produce analog outputs ranging from 0 to +5.0 volts dc. These outputs are routed to the PCM Telemetry Equipment via a distribution panel for processing.

The Signal Conditioning Equipment can consist of up to 45 modules, 14 different types, mounted on a common electrical equipment chassis. The equipment weighs 33 pounds and is 4.0 x 14.0 x 14.5 in size. The equipment operates from the 115/200 volt 3 phase, 400 cps bus and uses 90 watts of power. The unit is controlled from the communications control panel by an "on-off" toggle switch.

The Signal Conditioning Equipment contains a limited number of interchangeable modules. To ease interchangeability identification, the Signal Conditioning Equipment package is divided into five zones. This limited interchangeability provides a capability of up to 154 channels of sensor input-analog output information depending upon the type and number of modules used. The modules and their associated positions on the chassis are color coded to aid in module placement. Since the modules are designed to have limited interchangeability, the code is such that any module may be placed in any position that has the same color indicator as the module has.

All of the positions in Zone 1 have two violet color dots adjacent to the jack number. The positions in Zone 2 have two color dots, a blue and yellow dot, adjacent to the jack number. The positions in Zone 3 have the same color arrangement as that of Zone 2. The positions in Zone 4 have two yellow color dots adjacent to the jack number. The Power Supply and Regulator modules are color coded separately since they can only be placed in one position. The +20 and -20 volt Regulator module position has two green color dots. The +10 and +5.0 volt Regulator position has two orange color dots. The Power Supply module position has two black color dots.

TELECOMM SIGNAL CONDITIONER

BLOCK DIAGRAM

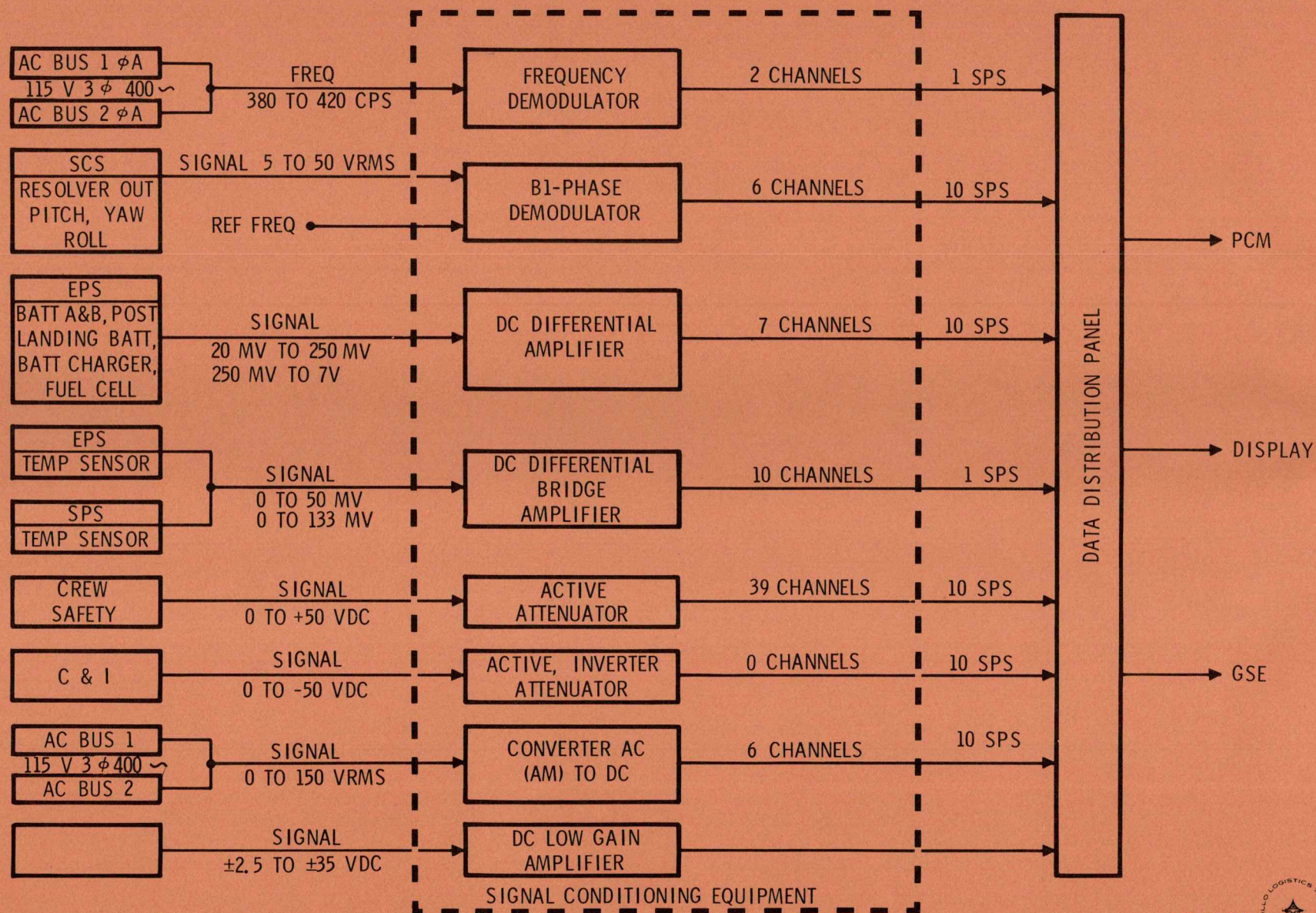


figure 7-1

CD-199 A



The electrical equipment chassis contains five connectors to provide the external power and signal connections. The chassis also contains forty-five connectors to route power to and from the forty-five modules in the equipment.

The Signal Conditioning Equipment is activated by positioning SCE "ON-OFF" switch to the "ON" position. This activation applies +28 volts dc to a latching relay that enables input power to be applied to the Power Supply module. This is the only control needed to operate the Signal Conditioning Equipment. When signals are applied to the individual modules, the output is automatically present, provided that operating power is supplied to the module. The Signal Conditioning Equipment is turned off by positioning SCE "ON-OFF" switch to the "OFF" position. This applies +28 volts dc to disable the latching relay that applies power to the Signal Conditioner Equipment.

DC ACTIVE ATTENUATOR MODULE

The dc active attenuator module is a signal conditioning device used to attenuate dc inputs to the level of 0 to +5.0 volts dc. The input voltage range is 0 to +7.0 volts dc thru +18.7 volts dc on range No. 1 and 0 to +18.7 volts dc thru +50 volts dc on range No. 2.

In the present configuration there are 8 modules with 7 circuits per module, packaged in a standard size module of $4 \frac{3}{4} \times 3 \times 3 \frac{3}{4}$ ". Each module weighs 0.64 pounds with a total combined weight of 5.12 pounds. The input impedance is 20,000 ohms and the output impedance is less than 500 ohms.

Power to operate the dc active attenuator is obtained from the +20 volt dc and -20 volt dc supplies. Input to the signal conditioner is a

single ended type and is fed into a selecting circuit for the purpose of choosing the various ranges. Refer to block diagram, Figure 7-2. The signal is fed thru gain adjust potentiometer R-1 and into the base of Q-1, the active attenuator. The output of the active attenuator is taken from the emitter of Q-1 and fed thru a blocking diode CR-1 and to the output of the module. Zener diode VR-1 is connected across the output of the circuit to limit the output voltage from rising above +6.2 volts dc and from falling below -0.8 volts dc. The output voltage varies from 0 to +5.0 volts dc linearly with respect to the input voltage. Output is of the single ended type. The attenuator has a frequency response of from dc to 200 cps. The input voltage range is by a simple bench maintenance operation.

DC ACTIVE INVERTER ATTENUATOR

The dc active inverter attenuator module is a signal conditioning device used to attenuate dc inputs to the level of 0 to +5.0 volts dc and inverts the input from a minus dc voltage to a plus dc voltage. The input voltage range is 0 to -7.0 volts dc thru -18.7 volts dc on range No. 1 and 0 to -18.7 volts dc thru -50 volts dc on range No. 2. In the present configuration there is one module with 7 circuits per module.

Refer to the block diagram Figure 7-3. Power to operate the dc active inverter attenuator is obtained from the +20 volts dc and -20 volts dc supplies. Input to the conditioner is of the single ended type and into the selecting circuit for the purpose of choosing the various operational ranges. The signal is fed into the base of the inverter stage Q-1. The signal is taken from the collector and is fed into the active filter stage Q-2. The output of Q-2 is the output of the circuit and is of the single ended type. The emitter of Q-2 is connected thru the gain adjust potentiometer R-1 and into the base of Q-1. Zener diode VR-1 is connected across the output of the

DC ACTIVE ATTENUATOR MODULE

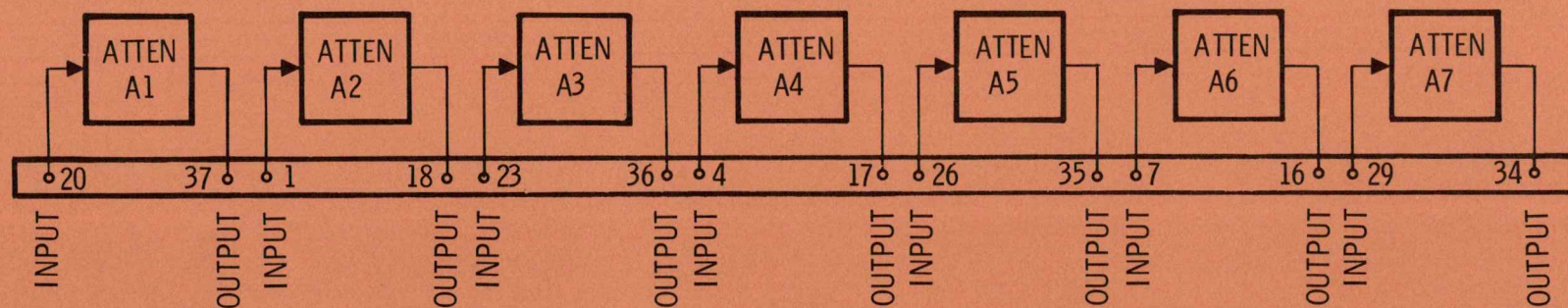
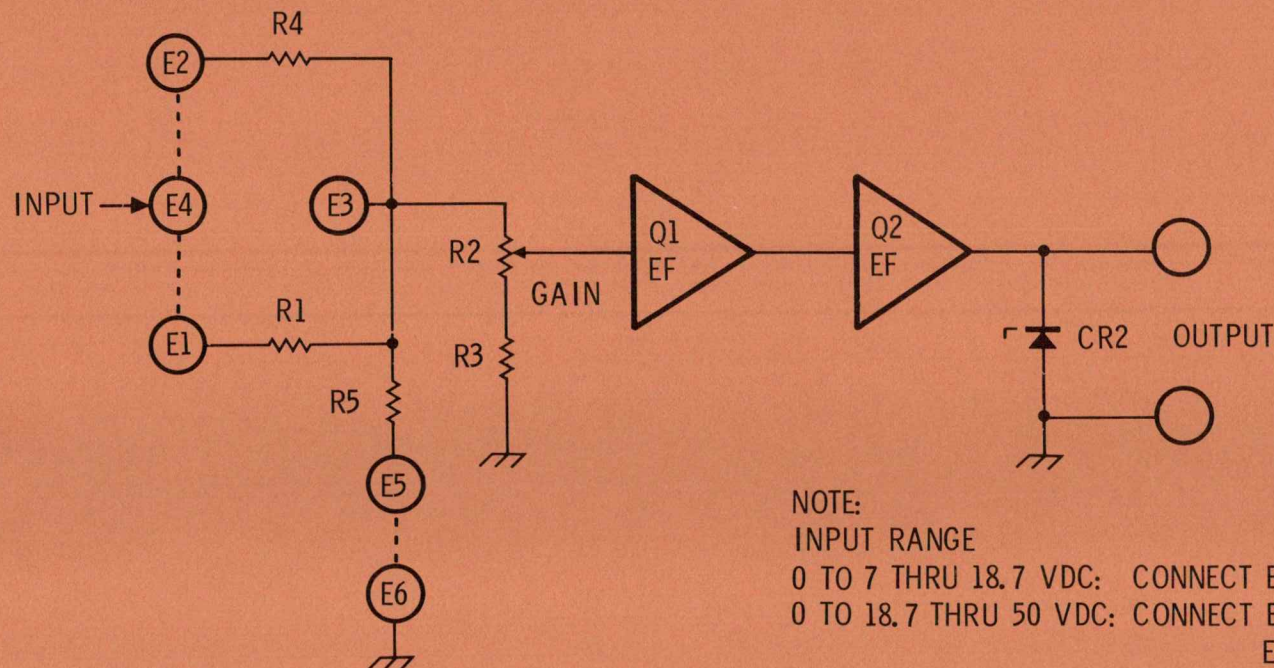


figure 7-2

CD-173C



DC ACTIVE INVERTER ATTENUATOR

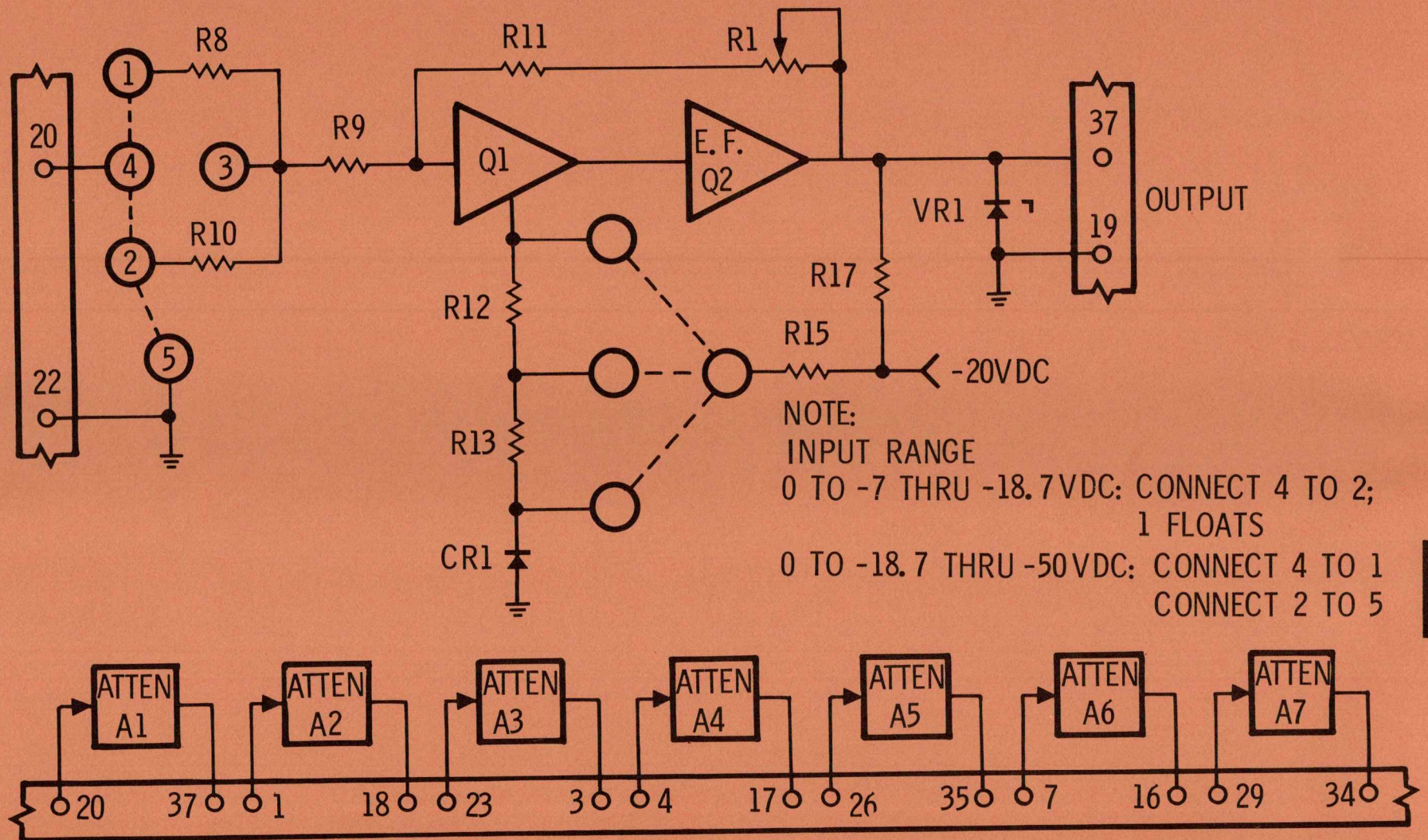


figure 7-3

CD-174C

circuit to limit the output voltage from rising above +6.2 volts dc and from falling below -0.8 volts dc. The output voltage varies from 0 to +5.0 volts dc linearly with respect to the input voltage. The input impedance is 20 K and the output is less than 500 ohms.

AC (AM) TO DC CONVERTER MODULE

The ac (am) to dc converter module signal conditioner device is used to monitor ac amplitude variations. The input signal amplitude is from 0 volts RMS to 150 volts RMS. The ac (am) to dc converter module is used to transform the ac signal amplitude variations to an analog output of 0 volts to +5.0 volts dc.

In the present configuration there are three modules with two circuits per module, packaged in a standard module size of $4 \frac{3}{4} \times 3 \times \frac{3}{4}$ ". Each module weighs 0.39 pounds with a total combined weight of 1.17 pounds. The current required from the power supply is 30 ma per module. The input impedance is greater than 500,000 ohms and the output impedance is less than 500 ohms. The input source is from the ac buses 1 and 2, each leg of the three phase supply. The output is to the data distribution panel and then to the pcm telemetry equipment.

Refer to the block diagram, Figure 7-4. Power to operate the ac (am) to dc converter module is obtained from the +20 volt dc and -20 volt dc supplies. The input ac signal is fed into an operational voltage divider select circuit that reduces the input voltage to the desired level. The choice of three ranges of input are chosen by selecting resistance values: (a) 0 to 150 mv; (b) 100 mv to 20 volts; (c) 15 volts to 150 volts. The output of this input voltage select network is fed into Q1A and Q1B an ac differential amplifier that operates class A. A constant current source Q7 is connected

to the emitters of Q1A and Q1B. Q1A and Q1B is also used as a common mode rejection amplifier. The gain of the module is accomplished by R43 (coarse) and R40 (fine). The output of the differential amplifier is fed thru the coarse control R43 to the operational amplifier Q2. Q2 is operated as a common emitter Class A amplifier. The output of Q2 is fed into another class A amplifier Q3. The output of Q3 is fed into Q4. Q4 operates as an emitter follower and is used as an impedance matching stage to the active filters that follow. The output of Q4 is fed into a rectifier circuit composed of CR2 and CR3. The rectified output of the rectifier network is fed into Q5. The output stage Q6 is operated as an emitter follower. Also on the output line is a Zener diode VR1 to limit the output voltage from rising above +6.2 volts dc or from falling below -0.8 volts dc. The output will vary between 0 and +5.0 volts dc with a minimum to maximum change in input. For example, with the input range of 15 volts to 150 volts RMS, 15 volts input would give 0 volts dc at the output and 150 volts input would give +5.0 volts dc in the output.

DC DIFFERENTIAL AMPLIFIER

The dc differential amplifier is used to monitor either single ended inputs or differential signal inputs. The input signal for differential input is 0 to +20 mv dc and all intermediate ranges thru 250 mv dc. The full scale range consists of 2 ranges; 20 mv to 200 mv, and 200 mv to 250 mv. The single ended input is 0 to +250 mv thru +7.0 volts dc. The full scale range consists of 4 ranges; +250 mv to +320 mv, +320 mv to +410 mv, +410 mv to +4.46 volts, and +4.46 volts to +7.0 volts dc.

In the present configuration there are 9 modules with 2 circuits per module, packaged in a standard module size. The input impedance is greater than 500,000 ohms and the output impedance is less than 500 ohms. The frequency response of the differential amplifier is dc to 200 cps.

AC(AM) TO DC CONVERTER,

BLOCK DIAGRAM

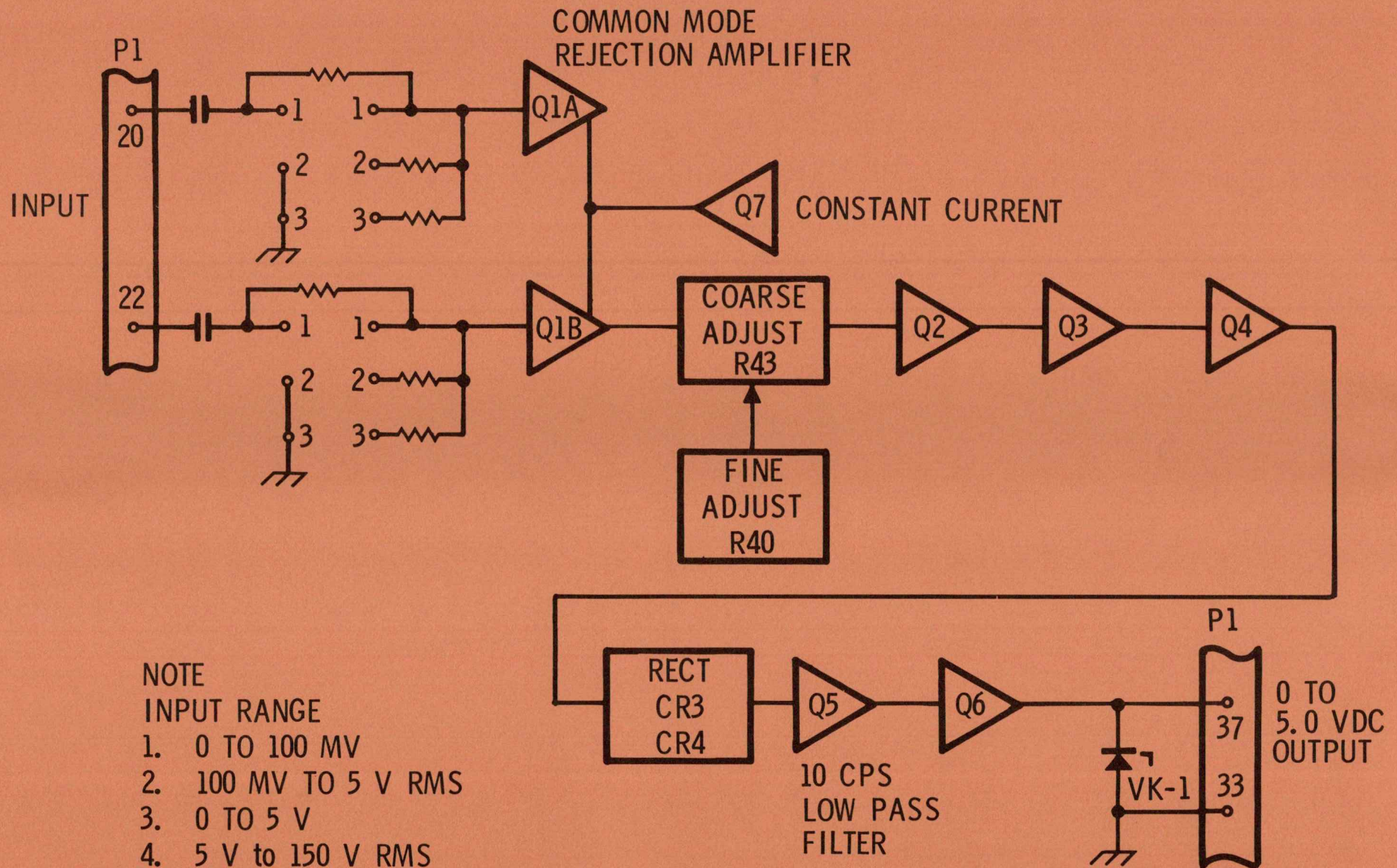


Figure 7-4

CD-176B



Power to operate the dc differential amplifier is obtained from the +20 volt and -20 volt supplies. Input ranges either differential or single ended is by a simple bench maintenance operation. Various combinations on the input terminal board are available, dependent upon the desired input range and as to whether it is to be a differential input or a single ended input. Refer to Figure 7-5. For a differential input, the input signal is fed directly into the bases of Q1A and Q1B. Q2 is used to provide a constant current source for the differential amplifier. Potentiometer R17 is a zero adjust and is connected to the emitters of Q1A and Q1B. The output of the first stage of the differential amplifier is taken from the collectors of Q1A and Q1B and is fed into the bases of Q3A and Q3B, the second stage of differential amplification. Potentiometer R12 is used to balance the amplifier and is connected to Q4, the constant current source associated with this differential amplifier. The outputs from the collectors of Q3A and Q3B are fed into the bases of Q5 and Q6, the third stage of differential amplification. The output of this stage is taken from the collectors of Q5 and Q6 and is fed into the fourth stage of differential amplification Q7 and Q8. The output at the collector of Q7 is fed through a 200 cps low pass filter and to the output of the module. The feedback network controls and gain of the circuit within a range through the adjustment of potentiometer R35. Zener diode CR3 is connected across the collectors of Q7 and Q8, the fourth stage of differential amplification. This will limit the output voltage to +6.2 v dc and -0.8 volts dc. The output of this conditioner is variable from 0 volts to +5.0 volts dc, linearly with the minimum to maximum input voltage. For example on the 20 mv to 200 mv range, an input of 20 mv will give an output of 0 volts and an input of 200 mv will give an output of 5.0 volts dc.

DC DIFFERENTIAL BRIDGE AMPLIFIERS

The dc differential bridge amplifier is a signal conditioning device that is used to monitor input signals which require a bridge type input circuit. The passive elements of the bridge circuit are in the dc differential bridge amplifier module and the variable element of the bridge is installed at the measuring location.

Refer to the block diagram, Figure 7-6. The dc differential bridge amplifier has the capability to balance the following sensors for zero output of the bridge:

(a) Sensor 1	270 ohms
(b) Sensor 2	328 ohms
(c) Sensor 3	455 ohms
(d) Sensor 4	2.8 k ohms

The bridge circuit also contains a gain control to adjust the delta R for full scale output of the amplifier:

(a) Sensor 1	R = 255 ohms
(b) Sensor 2	R = 27 ohms
(c) Sensor 3	R = 195 ohms
(d) Sensor 4	R = 2.9 k ohms

The bridge ranges are changed by a simple bench maintenance procedure.

Power to operate the dc differential bridge amplifier is obtained from the +20 and -20 volt dc supplies. The resistive type input is fed into a bridge circuit that is excited from the +10 volt dc power supply. Output of the bridge circuit is fed into the bases of Q1A and Q1B, the first stage of a differential amplifier. R37 is used to adjust the gain of the amplifier and R34 is used to balance the

DC DIFFERENTIAL AMPLIFIER

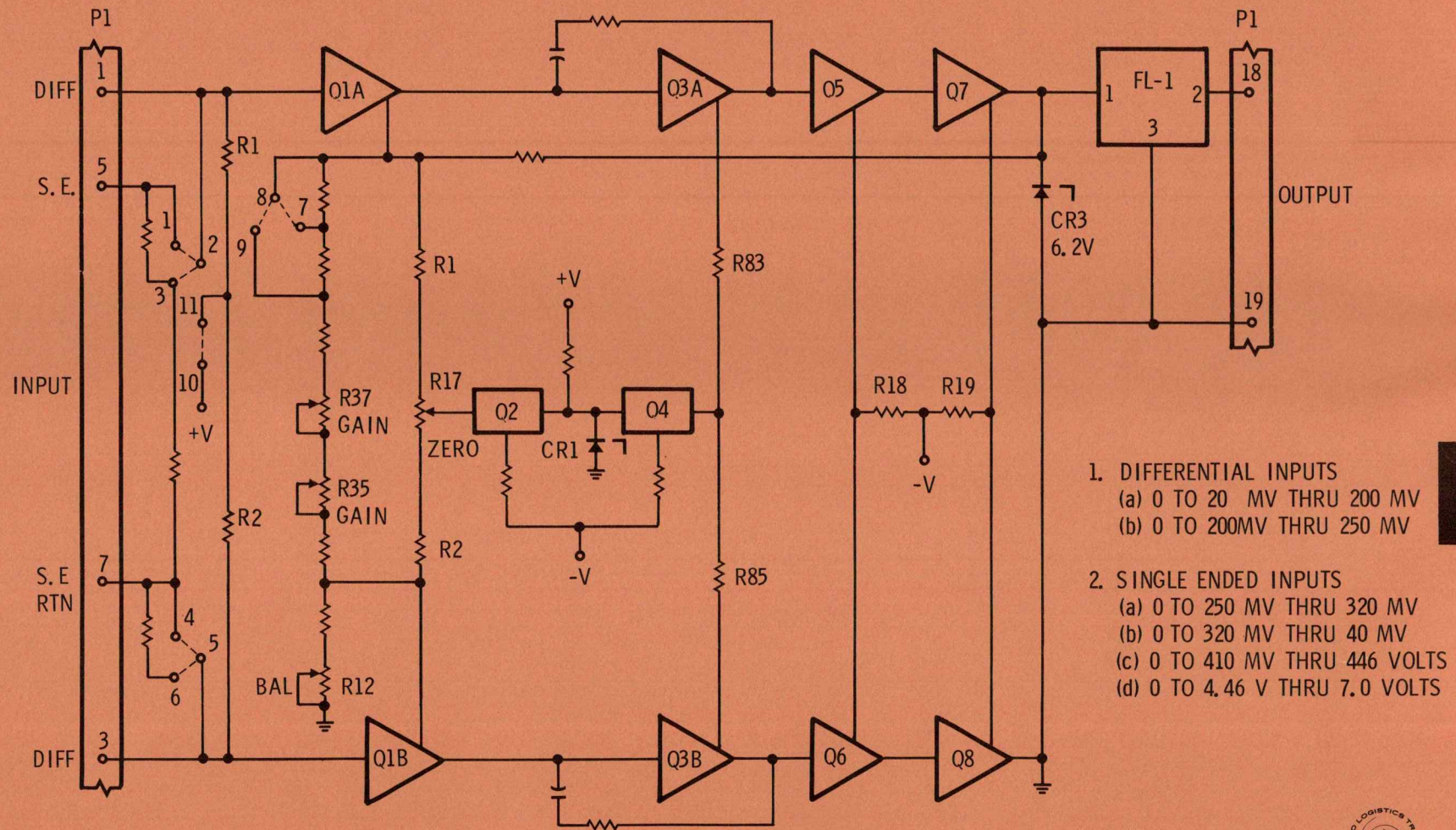


figure 7-5

CD-177D



DC DIFFERENTIAL BRIDGE AMPLIFIER

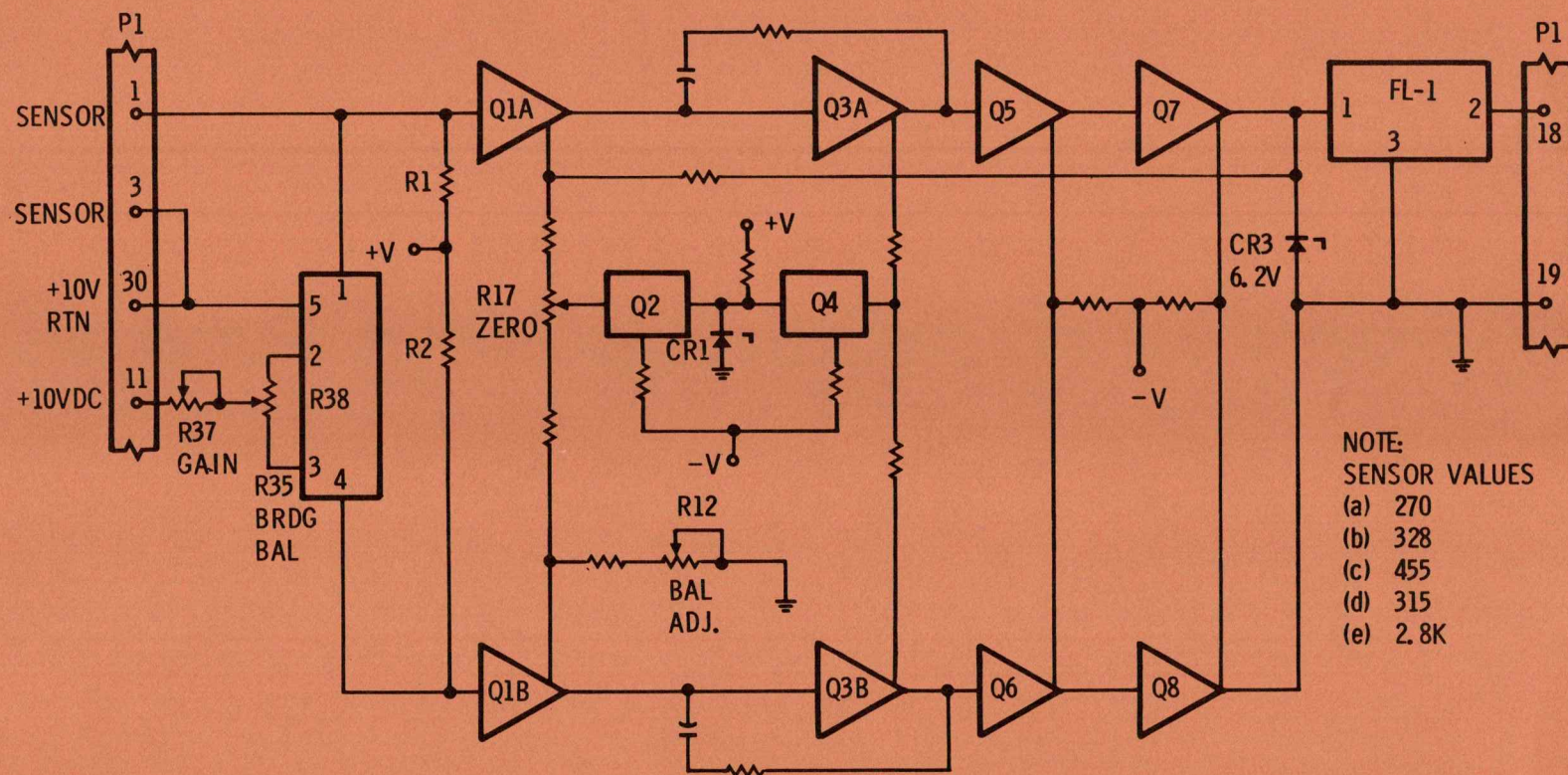


figure 7-6

input bridge circuit. Q2 is used to provide a constant current source for the differential amplifier. The collector of Q2 is connected to the zero adjust potentiometer R17, which is in turn connected to the emitter of Q1A and Q1B, the input differential amplifier. The output of the first stage of differential amplification is taken from the collectors of Q1A and Q1B and is fed into the bases of Q3A and Q3B, the second stage of differential amplification. Potentiometer R12 is used to balance the differential amplifier and is connected to Q4, the constant current source associated with this amplifier. The outputs from the collectors of Q3A and Q3B are fed into the bases of Q5 and Q6, the third stage of differential amplification. The output of this stage is taken from the emitters of Q5 and Q6 and is fed into the fourth stage of differential amplification Q7 and Q8. Output at the collector of Q7 is fed through a 200cps low pass filter and to the output of the signal conditioner. A feedback circuit is connected between the collector of Q7 and the emitter of Q1B. Zener diode CR3 is connected across the collectors of Q7 and Q8, the fourth stage of differential amplification. This zener diode will limit the output voltage to +6.2 volts dc and -0.8 volts dc. The output of this conditioner is variable from 0 volts to +5.0 volts dc, with the minimum to maximum change in input resistance. The output is of the single ended type.

BI-PHASE AC (AM) DEMODULATOR

The bi-phase ac (am) demodulator is a signal conditioning device used to monitor phase inputs of 0 and 180 degrees with respect to a reference signal over a frequency range of 400 cps to 1600 cps. The output of the demodulator is a dc signal of 0 volts when the maximum input signal is 180 degrees out of phase with the reference signal, +5.0 volts dc output when the maximum signal input is in phase with the reference signal, and +2.5 volts dc when there is no signal present at the input.

In the present configuration there are six modules with one circuit per module, packaged in a standard module size of $4 \frac{3}{4} \times 3 \times \frac{3}{4}$ ". Each module weighs 0.38 pounds for a total combined weight of 2.28 pounds. The input impedance is greater than 500 k ohms and the output impedance is less than 500 ohms. The input source is from the SCS resolver; pitch; yaw; and roll. The input signal amplitude is from 5.0 to 50 volts RMS, using a balanced input to the signal conditioner. The output of the modules is to the Data Distribution Panel and then to the PCM Telemetry Equipment. The reference signal input impedance is greater than 250 k ohms.

Refer to the block diagram, Figure 7-7. Power to operate the bi-phase demodulator is obtained from the +20 and -20 volts dc supplies. The signal input is fed into terminals 20 and 22, thru dc isolation capacitors and into a compound connected amplifier of Q8B and Q2B, and Q8A and Q2A, the input signal amplifiers. The output of the input signal amplifier is taken from the collector of Q2A, a 2 volt peak-to-peak sine wave for maximum input. The output from the collector of Q2B is fed into an ac feedback amplifier, Q6. AC feedback amplifier Q6 with the Gain control R23 is used to control the gain of the amplifier. A reference input at terminals 13 and 32 at the same frequency as the signal input, is fed into the bi-phase demodulator. Three levels of amplitude from the reference signal are available: (a) 26 volts, (b) 50 volts, or (c) 120 volts RMS. The reference input is fed thru dc isolation capacitors and into the reference clipping amplifiers. The reference clipping amplifier is an ac differential amplifier operating in saturation, or cutoff, with the output taken from the collector of Q1B. The output signal is a 2 volt square wave between the levels of -18 volts and -20 volts. The sine wave output of the input signal amplifier and the square wave output of the reference clipping amplifier are combined and fed into the summing amplifier, Q3A. The summing amplifier operates class A when the collector of Q1B is

BI-PHASE AC (AM) DEMODULATOR, "D" MODEL

BLOCK DIAGRAM

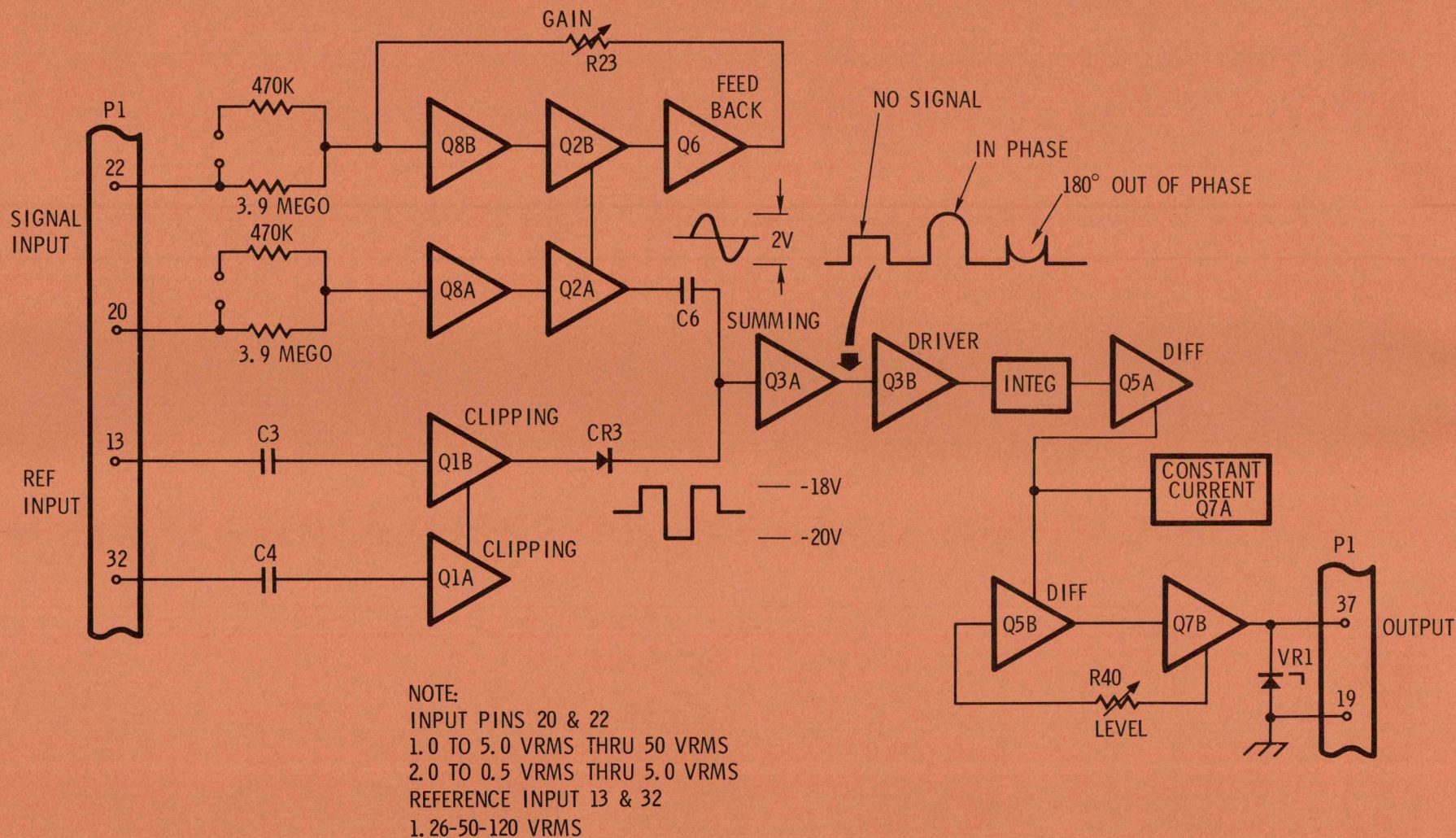


figure 7-7

-20 volts and operates in saturation when the collector of Q1B is -18 volts. The level of the output of Q3A varies with three possibilities; (a) in-phase; (b) 180 degrees out of phase; or (c) no signal at the input. The output of the summing amplifier is fed into a driver stage Q3B. The driver stage is used to reduce the impedance of the previous stages to provide a more desirable input to the dc differential amplifier and filter Q5A and Q5B. The base circuit of Q5A is used as an active filter circuit. A reference signal is fed into the base of Q5b thru the level adjust R40. Q7A is used as a constant current source for the differential amplifier. The output from the differential amplifier Q5A and Q5B is fed into the output amplifier and filter Q7B. The output of Q7B is of the single ended type with a zener diode, VR1, connected across the output to limit the voltages from rising above +6.2 volts dc and from falling below -0.8 volts dc. A portion of the output from Q7B is fed back into the base of Q5B for negative feedback.

The level adjust, R40, and the gain adjust R23, controls provide for external calibration of the demodulator to enable the output to be set at 0 volts, +2.5 volts, and +5.0 volts dc for the three input conditions described above. It is noted that the input signal will either be 180 degrees out of phase or it will be in phase with the reference. Intermediate values of output are analogs of the two phase relationships at the input with reduced signal amplitudes.

FREQUENCY (FM) DEMODULATOR

The frequency (FM) demodulator signal conditioning module is used to transform a varying frequency input of 380 to 420 cps to an analog output of 0 volts dc to +5.0 volts dc.

In the present configuration there are two modules with one circuit per module, packaged in a standard module of 4 3/4 x 3 3/4". Each module weighs 0.39 pounds and the current required from the power supply is approximately 30 ma. The input impedance is greater than 500 k ohms and the output impedance is less than 500 ohms. The input signal amplitude is from 105 volts RMS to 150 volts RMS, 400 cps. The input source is from the spacecraft a-c buses 1 and 2 phase A of each bus. The output of the module is to the data distribution panel and then to the pcm telemetry equipment.

Refer to the block diagram, Figure 7-8. Power to operate the frequency demodulator is obtained from the +20 volts dc and the -20 volts dc power supply. The frequency demodulator is capable of operation in either a balanced or unbalanced mode. The input ac signal at an amplitude of 105 to 150 volts RMS is fed thru an attenuating network to the input stage which operates as a two section ac differential buffer amplifier. The ac buffer amplifier partially clips the input ac signal so as to form a wave between a sine wave and a square wave. The input buffer amplifier also isolates the input from the effects of load impedance variation in subsequent stages of the frequency demodulator. Complete dc isolation is accomplished with the use of capacitors at the input. The outputs of the two sections of the ac buffer amplifiers are two modified sine waves of approximately 10 volts peak-to-peak and 180 degrees out of phase with each other. The output of the ac buffer amplifiers are fed into two clipping amplifiers Q2A and Q2B. Both Q2A and Q2B operate in saturation so as to form two square waves 180 degrees out of phase with respect to each other. The output of the clipping amplifiers are passed thru a differentiator composed of CR5 and CR6. The output of the differentiator is a single pulse train at a rate of twice the input frequency. This pulse train is used

FREQUENCY (FM) DEMODULATOR, "D" MODEL

BLOCK DIAGRAM

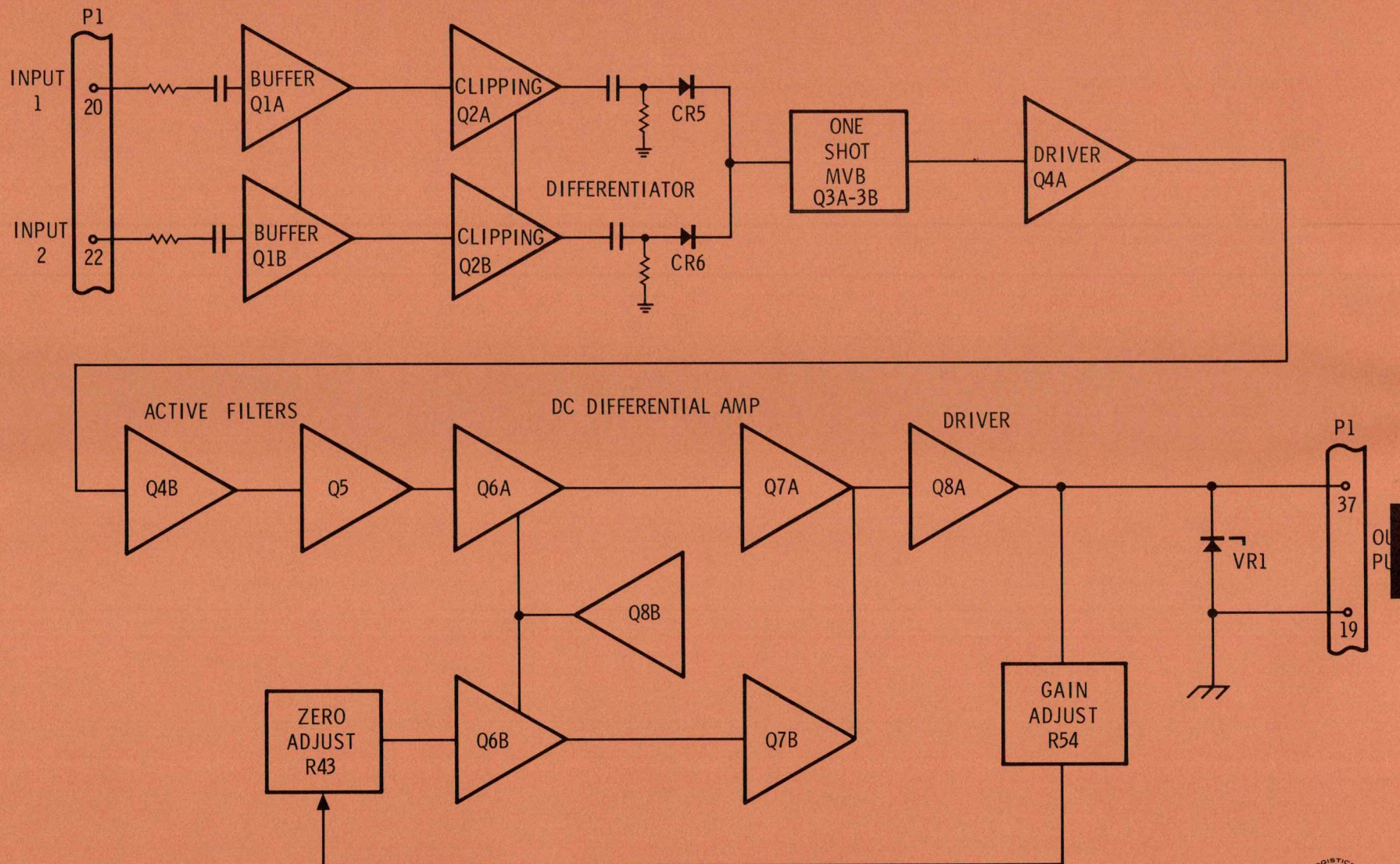


figure 7-8

CD-181C



to drive a monostable one shot multivibrator. The output of the multivibrator is a square wave. The pulse width of the output is constant since it is dependent upon the RC time constant of the multivibrator and not upon the input frequency. A change in input frequency will change the frequency of the output pulses from the multivibrator. The square wave output of the multivibrator is fed into a square wave driver, Q4A. The square wave driver acts as a switch with the output being a square wave of approximately 17 volts. The output square wave is fed thru two stages of an active filter, Q4B and Q5. The output of the active filter is an average dc voltage, the average dc voltage is dependent upon the frequency output of the multivibrator, which is fed into a differential amplifier, Q6A and Q6B. The reference for the differential amplifier is the ZERO ADJUST R43. The output from the differential Q6A and Q6B is fed into another differential Q7A and Q7B. The output from the second differential of Q7A and Q7B is fed into the output driver Q8A. The output driver Q8A is in a common emitter configuration. R54 the GAIN ADJUST is variable to enable nominal adjustments to be made on the gain of the module. A zener diod VR1 is connected across the output to limit the output from rising above +6.2 volts and from falling below -0.8 volts dc. The output is of the single ended type. An output of 0 volts dc corresponds to an input frequency of 380 cps. An output of +2.5 volts dc corresponds to an input of 400 cps and an output of +5.0 volts dc corresponds to an input of 420 cps. Any other frequencies between 380 and 420 cps are represented by values linearly between 0 and +5.0 volts dc. The signal conditioner ZERO ADJUST and GAIN ADJUST are used for high end, center and low end scale calibration of the output. The overall response of the demodulator is flat from 0 to 15 cps with respect to rate of change of the

input frequency. This as well as the output ripple and noise levels are determined by the active filter stages, Q4B and Q5.

POWER SUPPLY AND REGULATOR MODULES

The power supply module in conjunction with the regulator modules converts three phase 115/200 volt, 400 cps ac input power into dc operating voltages for the signal conditioner modules and the spacecraft sensors. One regulator module supplies +20 volts dc and -20 volts dc to all the signal conditioner modules. One regulator module supplies regulated +5.0 volts dc and +10 volts dc to the spacecraft sensors that require a regulated dc voltage for operation and also +10 volts dc to the dc differential bridge amplifier modules. The power supply module contains a test connector that, when the module is in place in the chassis, is accessible through the signal contitioning equipment front panel. The power supply voltages can be measured at this test connector.

Refer to the block diagram, Figure 7-9. Input power, three phase 400 cps, is fed into the primary of transformer T1. The secondary windings of T1 are fed into the +10 volt rectifier, +5.0 volt rectifier, +20 volt rectifier, and the -20 volts rectifier. Each one of these supplies is electrically isolated from each other and each supply operates identically, Since all four regulators are identical only one will be discussed. The output from the transformer T1 is fed thru a bridge rectifier, and into a regulator stage. The bridge output is also fed into a pre-regulator stage. The pre-regulator is used to reduce ripple in the output. This is accomplished by using a constant current type pre-regulator. Regulation is provided through a feedback loop from the supply back into the regulator. The output voltage is sampled and fed into the differ-

POWER SUPPLY & REGULATORS

BLOCK DIAGRAM

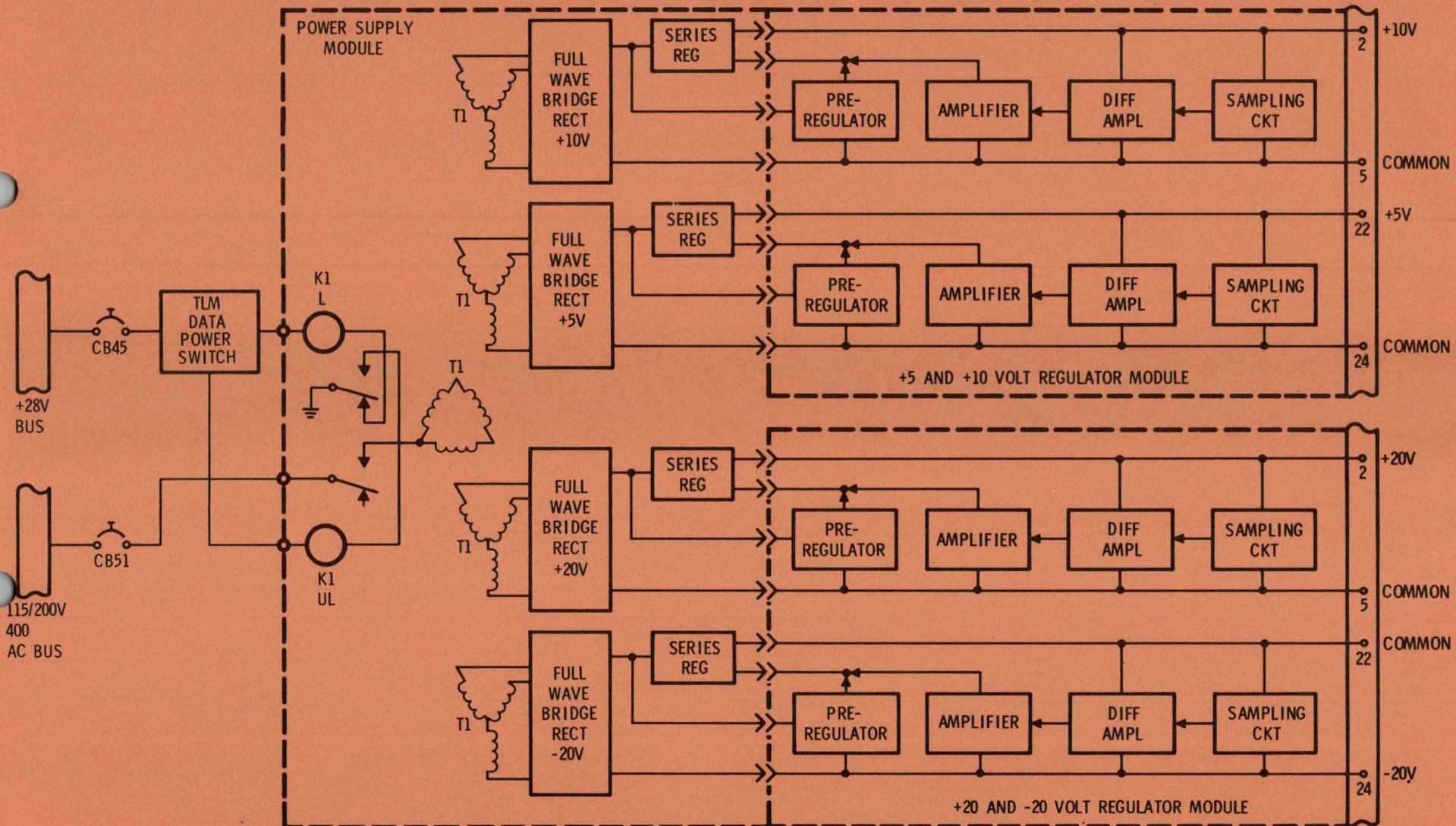


Figure 7-9

ential amplifier. A reference voltage is established in the differential amplifier. A change in the differential amplifier will in turn cause a change in the driver amplifier. The driver amplifier is held at a constant level by the use of zener diodes. Any changes in the differential amplifier output will cause a corresponding change in the driver amplifier which provides negative feedback to the series regulator, which in turn will either increase or decrease the output voltage of the regulator. Total input power for the signal conditioning equipment is approximately 90 watts. The efficiency of the power supply is 61% and the power factor is 0.85 - inductive. All the circuits are designed so that maximum overload or short circuit current equals 150%. The maximum ripple is less than 3 mv p-p. and the regulation is $\pm 0.25\%$. The power supply is the largest module in the signal conditioning equipment and is $4\frac{1}{2} \times 4\frac{3}{4} \times 3$ ", and along with the regulator modules weighs 7.05 pounds.

AC TO DC EXPANDED SCALE CONVERTER

All sensors which offer 105 volts rms to 125 volts rms feed into the ac to dc expanded scale converter for processing to the 0 to +5 volt dc range.

In Figure 7-10, Q1A and Q1B form a differential amplifier which provides high gain and also common mode rejection. The output of the differential amplifier is fed to common-emitter amplifier, Q2. This amplifiers' output feeds an amplitude detection circuit made up of CR1 and CR2. These two diodes form the same type of amplitude detection circuit as CR1 and CR2 in the ac to dc converter. The negative half cycle output is applied to the base of Q3 and the positive half cycle is isolated. Degenerative feedback is coupled to the base of Q1A for stability.

Transistors Q3 and Q4 form a single input differential amplifier. The +5 volt dc output level is set by R23, and R11 sets the 0 volt dc output level.

The output of Q3 is applied to Q5, which is an emitter-follower. Further current amplification is accomplished by a second emitter follower, Q6.

CR3 is put across the output to keep the failure mode voltage within the range of -1 to +7 volts dc.

DC EXPANDED SCALE ATTENUATOR

Refer to block diagram, Figure 7-12. The dc expanded scale attenuator module is a signal conditioning device used to attenuate dc inputs to the level of 0 to +5.0 volts dc. The input range is 24 to 32 volts dc. Each module contains two identical circuits. Power to operate the dc expanded scale attenuator is obtained from the +20 and -20 volts dc supplies. Input to the signal conditioner is of the single ended type. The signal is fed into the base of the first stage, Q2, which is one half of a differential amplifier. The other half of the differential amplifier, Q1, has a reference dc signal applied to the base which is determined by R6 and the zener diode VR1. Q3 is a constant current source connected to the emitters of the differential amplifier pair, Q1 and Q2. The gain of the amplifier is controlled by the gain adjust pot R1 which is also in the emitter circuit of the differential amplifier pair. The output of Q1 is used to drive Q4 which is an emitter follower output stage. The output of Q4 is also fed back thru the zero adjust pot R2 to the reference half of the differential amplifier Q1. The zero adjust pot is adjusted for 0 volts dc output with 24 volts dc input. The gain adjust pot is adjusted for +5.0 volts dc output with 32 volts dc input.

EXPANDED SCALE AC AM TO DC CONVERTER

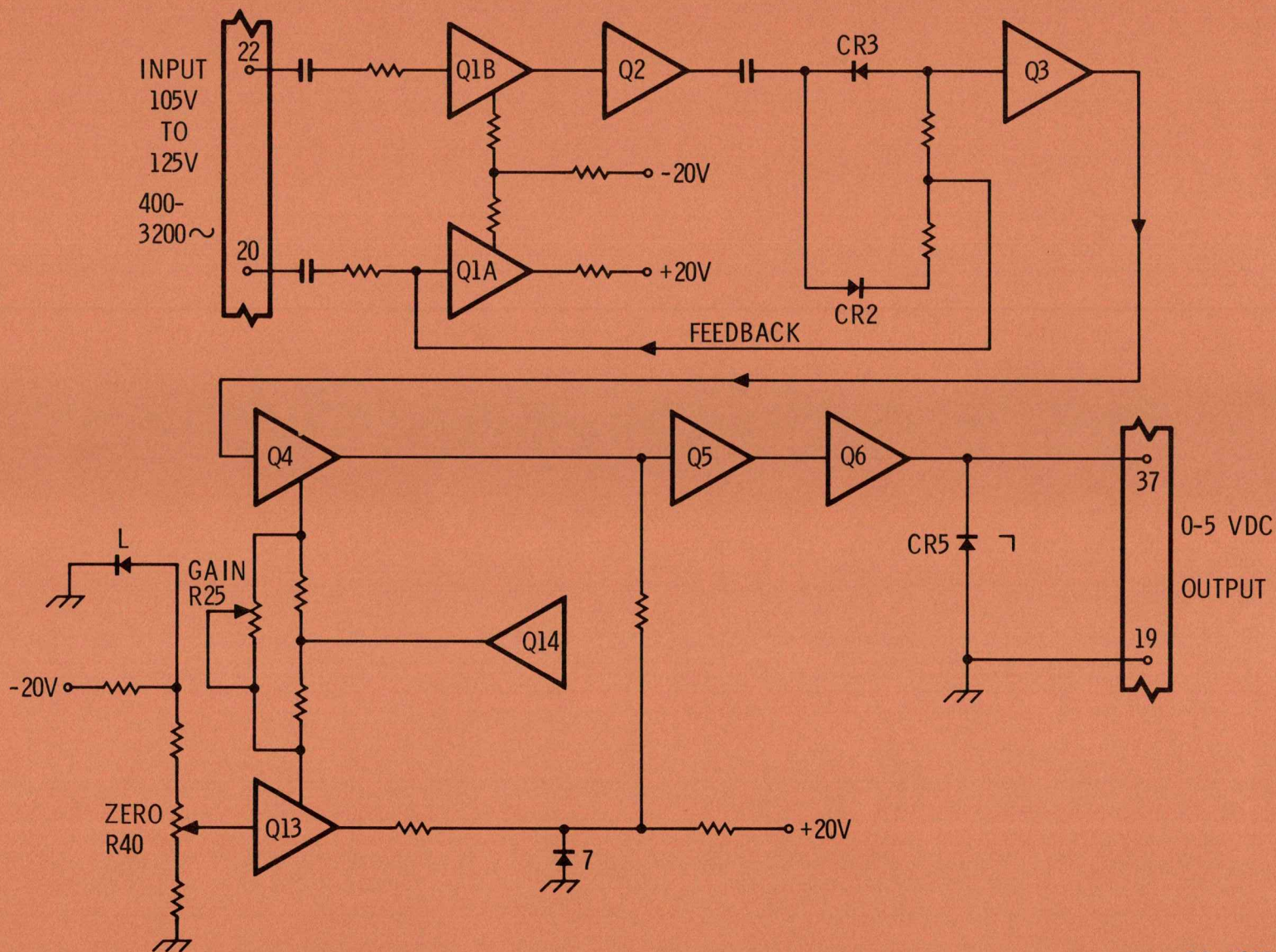


Figure 7-10

CD-182B



DC EXPANDED SCALE ATTENUATOR MODULE

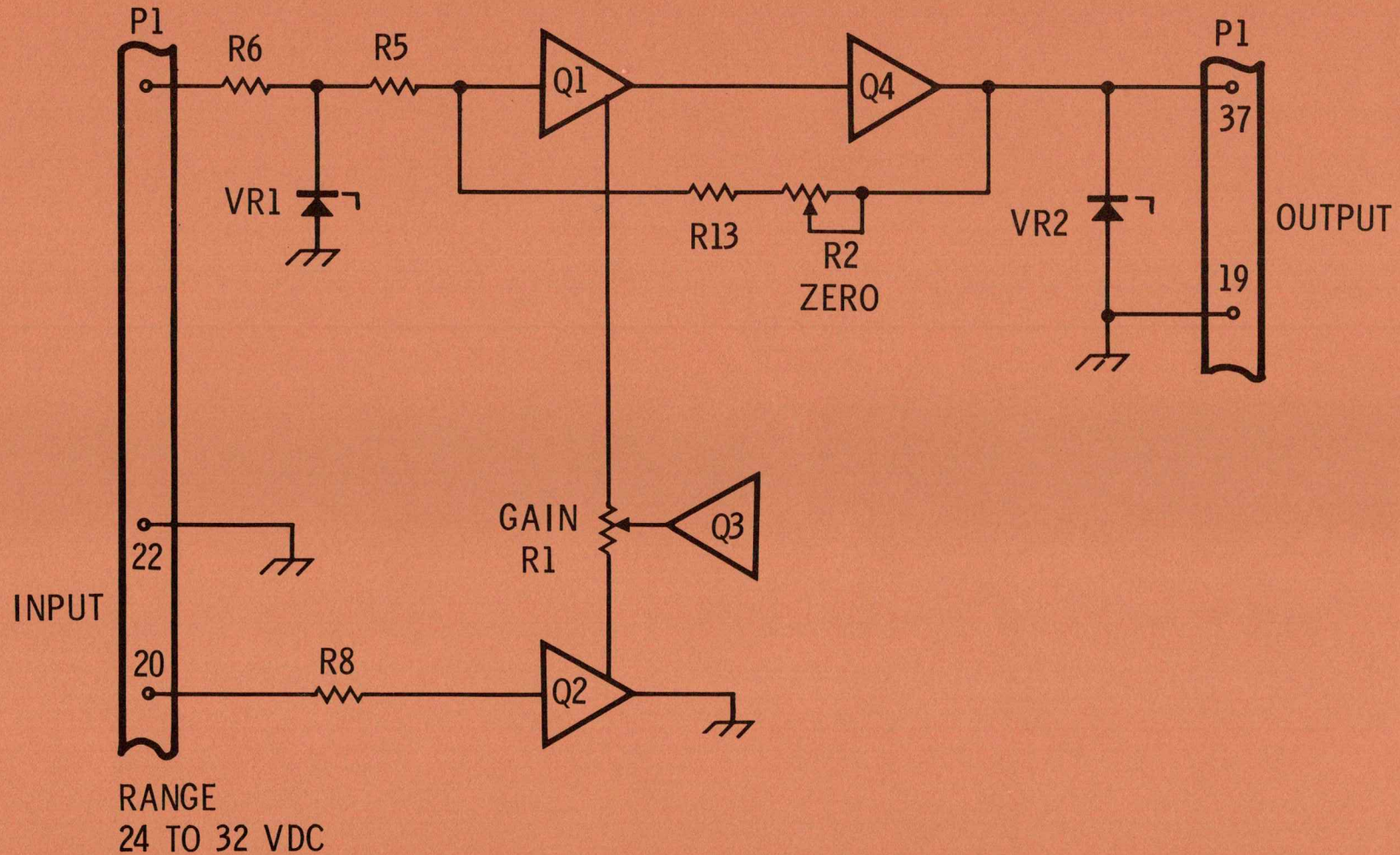


Figure 7-11

CD-175B



Zener diode VR2 in the output circuit limits the output voltage from rising above +6.2 volts dc and from falling below -0.8 volts dc.

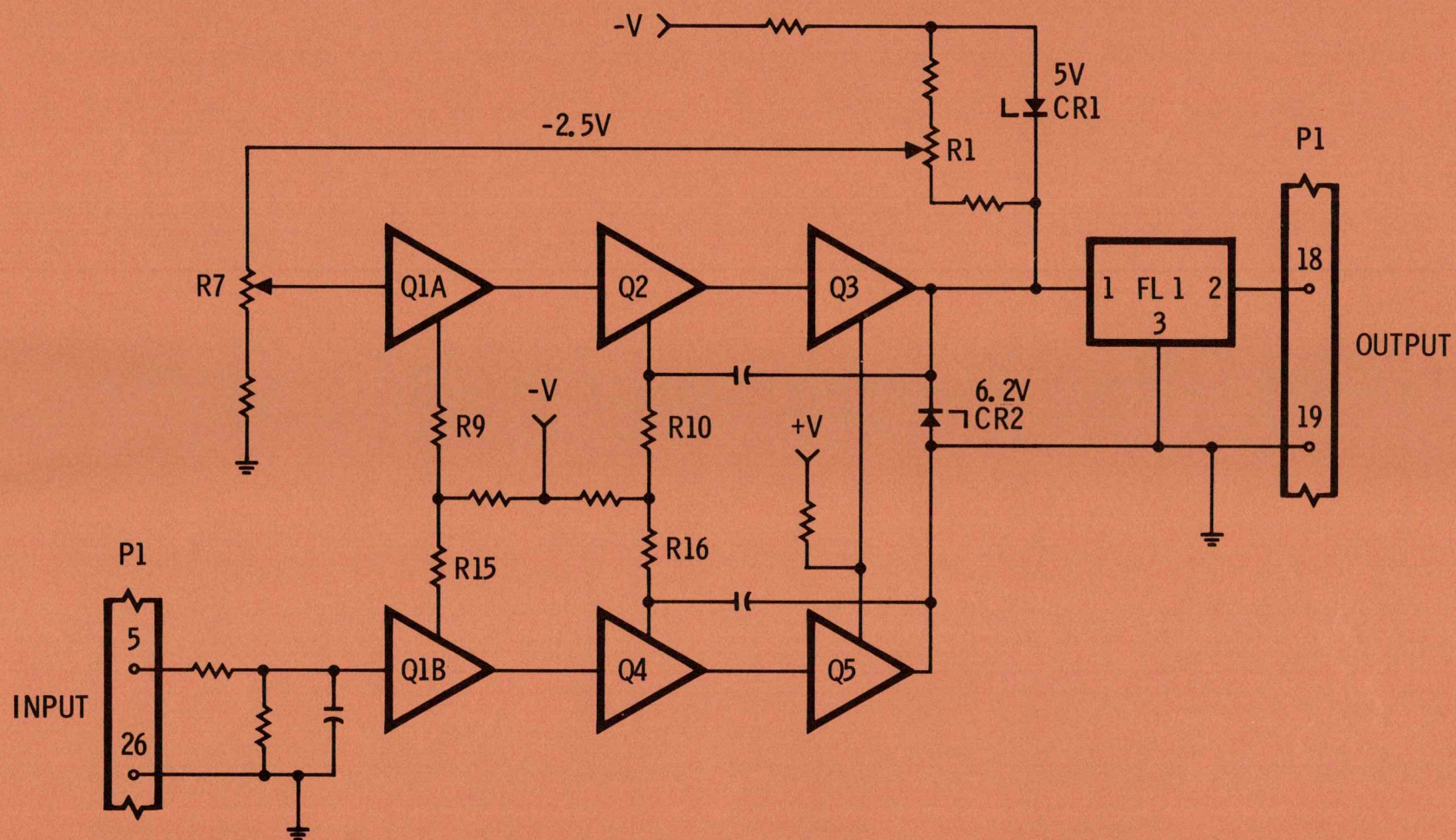
referenced to ground. Zener diode CR3 in the output circuit limits the output voltage from rising above +6.2 volts dc and from falling below -0.8 volts dc.

LOW GAIN DC AMPLIFIER

Refer to block diagram, Figure 7-11. The dc low gain amplifier module is a signal conditioning device used to accept dc voltages in the range of 0 to +2.5 volts dc and all intermediate values to +35 volts dc. The signals are then converted to an output of 0 to +5.0 volts dc. With no signal at the input the output of the module is +2.5 volts dc. A negative input signal causes the output voltage to decrease toward 0 volts dc and a positive input signal causes the output to increase toward +5.0 volts dc. The input impedance is greater than 20 k ohms and the output impedance is less than 500 ohms. Each module contains two identical circuits.

Power to operate the low gain dc amplifier is obtained from the +20 and -20 volts dc supplies. Input to the signal conditioner is of the single ended type. The dc input signal is applied to a single ended differential amplifier, Q1A and Q1B. R17 the gain control pot on the input stage is used to set the output voltage level for a specific input voltage range. R1 together with CR1 in parallel with R2 and R3 form a voltage divider network providing a fixed base bias for Q1A. With a positive signal voltage at the base of Q1B, the output of Q1A will also go more positive. With a negative signal voltage at the base of Q1B, the output of Q1A will also go more negative. The output of Q1A and Q1B is applied to another differential amplifier pair, Q2 and Q4. The differential output of Q2 and Q4 is applied to the output differential amplifier pair, Q3 and Q5. Q3 is in a single ended output configuration with the output of Q5

DC LOW GAIN AMPLIFIER



NOTE:
INPUT
 ± 2.5 VDC AND ALL INTERMEDIATE
RANGES TO ± 35 VDC

figure 7-12

SECTION VIII

PCM TELEMETRY EQUIPMENT

The Pulse Code Modulation (PCM) Telemetry Equipment, Unit number 906B-IE, Collins Radio Co. part number 512-2591-003, receives and converts data inputs from various sampling points throughout the Spacecraft, into a single serial digital output. This output is supplied to the Pre-Modulation Processor and Data Storage Equipment. The equipment is provided with several self check circuits for detection of major malfunctions. These circuits provide GO, NO-GO outputs to the IFTS system which isolates a failure to a replaceable module.

The equipment, including power supply, is contained in two Space Electronic Packages (SEP's) designated PCM Unit 1 and PCM Unit 2. Table 8-1 lists the units and their components. Each SEP is of modular construction to permit in-flight maintenance capability. Each unit is 9.3 inches wide, 4.4 inches high, and 16.5 inches deep, excluding front panel. Total weight of both units is 47.7 pounds.

The equipment is capable of processing 270 high-level (0 to 5 volts) analog inputs and 50 low-level (0 to 40 millivolts) analog inputs at sampling rates of 1 to 200 samples per second (sps). It is also capable of processing 32 parallel bit, and 1 serial bit digital inputs. Each analog and digital input to the PCM Telemetry Equipment is assigned to a channel. These inputs, or channels, will be combined to provide a serial digital output at one of two rates as determined by the mode of the equipment. The high bit rate mode has an output of 51,200 bits per second, and the low bit rate mode has an output of 1600 bits per second.

A fixed program is provided for sampling each channel and the rate at which it is sampled for each bit rate mode. Table 8-2 gives these rates and other characteristics of the input signals.

System timing is normally based on the Central Timing Equipment (CTE) 512 kc pulse train and 1 cps synchronizing pulse. However, if the external clock fails to provide timing pulses for 10 microseconds, timing is automatically switched to an internal timing source. The system recycles to the start of the sub frame with each positive transition of the 1 cps synchronizing pulse, while operating on the external clock. The CTE 1 cps synchronizing pulse is inhibited while operating on the internal clock timing.

The 512 kc signal is, in itself, the basic timing signal used in the PCM Telemetry System. It is called the period and has a duration of 1.95 microseconds. The period signal is sent to a 10:1 or 320:1 countdown chain, as determined by the bit rate mode. This provides bit times of 51.2 kbs or 1.6 kbs (kilobits per second). An 8:1 countdown of the bit time signal provides the word time signal. Thus, the two output rates will provide 6400 or 200 words per second out of the system. A 128:1 countdown of the word time supplies the prime frame time for the high bit rate mode. This bit rate mode has 50 prime frames per sub-frame, and one sub-frame per second. This is accomplished, as in the other divisions, by a countdown chain. The low bit rate mode has 200 words per prime frame and only one prime frame per second. The first four words of each prime frame are used for identification and synchronization.

Module No.	Official Nomenclature	Common Name Nomenclature
UNIT 2		
---	Bus Wiring Module	Bus Wiring
A9	Data Transfer Driver Module	Data Transfer Buffers
A2-A7	Digital Multiplexer Gate Module	Digital Multiplexer
---	Dummy Module	Dummy Module
---	Elapsed Time Indicator Module	Unit 2 Elapsed Time Meter
---	Module Mounting Chassis Assembly Unit 2	P. C. M. Unit 2 Chassis
A10	Output Register With Drivers Module	Output Register
A18-A20	Power Supply Module	Power Supply
A11	Programmer - Control Drivers Module	Programmer Control Drivers
A12	Programmer - Counter Matrix Module	Programmer Counter Matrix
A13	Programmer - Diode Matrix and Control Drivers - Type 1 Module	Programmer Matrix and Control Driver - Type 1
A14	Programmer Diode Matrix and Control Driver - Type 2 Module	Programmer Matrix and Control Driver - Type 2
A15-A16	Programmer - Diode Matrix Module	Programmer Matrix
A8	Synchronizer Select and Format Identification Module	Sync and Format ID Selector
A19	Power Supply	Power Supply

Table 8-1

Module No.	Official Nomenclature	Common Name Nomenclature
UNIT 1		
A5-A6	Analog Gate Driver Module	Analog Multiplexer Driver
A18	Coder - Analog to Digital Converter and Sample and Hold Module	Coder
---	Elapsed Time Indicator Module	Unit 1 Elapsed Time Meter
A7-A16	High Level Analog Gate Module	High-Level Analog Multiplexer
A17	High Speed Gates and Calibrator Module	High-Speed Gates and Calibrator
A4	Low Level Amplifier Module	Low Level Amplifier
A1-A3	Low Level Analog Gate Module	Low Level Analog Multiplexer
---	Module Mounting Chassis Assembly, Unit 1	P. C. M. Unit 1 Chassis

Table 8-1

INPUT SIGNAL CHARACTERISTICS

INPUT CHANNELS	NUMBER OF CHANNELS	SOURCE IMPEDANCE	SAMPLING RATE	BITS PER WORD	SIGNAL LEVEL
Low-Level Ana.	50	0 to 500 ohms	1 sps	8	0 to 40 millivolts
High-Level Ana.	270	0 to 5000 ohms	1 to 200 sps	8	0 to +5 volts
Parallel Digital Data	28	0 to 5000 ohms	18 sps high 1 sps low	8	"1" = +3.5 to 10 "0" = 0 \pm 0.5
	1	0 to 5000 ohms	200 sps high 0 sps low	16	same
	1	same	50 sps high 0 sps low	16	same
	1	same	10 sps high 0 sps low	24	same
	1	same	10 sps high 1 sps low	32	same
Serial Digital Data	1	100 ohms	50 sps high 10 sps low	40	"1" = +13.0 v "0" = -2.0 v

Table 8-2

BLOCK DIAGRAM OPERATION

Signals entering the PCM Telemetry System for processing are of four general types; low-level analog, high-level analog, parallel digital, and serial digital. Each input type is processed in a different manner which will be explained in the following paragraphs. References will be made to figure 8-1, a block diagram of the PCM Telemetry System.

The block diagram shows the basic signal flow in the equipment. In the overall operation the programmer section in unit 2 maintains primary control of this equipment. It provides the basic timing for sampling and processing of data from either an external or internal clock.

LOW-LEVEL ANALOG INPUTS. Fifty low-level analog inputs are fed into the low-level analog multiplexer, figure 8-1. All of these will be used during the high bit rate mode, while only ten of them will be used during the low bit rate mode. These inputs will be present continuously at the analog multiplexer input. They are gated into the multiplexer one at a time. The timing signals determine the inputs to be sampled at specific times and are provided by the programmer through the analog multiplexer drivers. These low-level signals will be sent out on a single line as a series of amplitude modulated pulses, each pulse being one word time in length. Because of their small voltage level, the pulses are amplified by the low-level amplifier. This changes the information range of the signals from 0-40 mv. to 0-5 volts. The pulse train is then fed to the coder which is an analog-to-digital converter. Each incoming analog pulse is converted to an eight parallel bit digital word by the coder and is then sent to the digital multiplexer. The digital multiplexer gates combine these eight bit words with other digital

words of various bit lengths, to form a series of eight parallel bit digital words which is sent to the output register. The output register converts the eight parallel bit digital words to eight serial bit digital words in non-return-to-zero form by sampling each input bit for one bit time. This signal containing all the information to be telemetered to the ground station is sent to the transmitter. The order of appearance, and number of samples per second, of each piece of information in the output signal is determined by the programmer.

HIGH-LEVEL ANALOG INPUTS. In the high bit rate mode 270 high-level signals are sequenced through the high-level analog multiplexer by row and column commands received from the programmer. During the low bit rate mode the programmer row and column commands select 100 of the 270 signals available. The signals selected are combined by the number of samples per second into five Pulse Amplitude Modulated (PAM) pulse trains and are sent to the high speed gates for pulse shaping. The high speed gate outputs are combined to form a single PAM signal to the coder. The coder handles the high-level inputs in the same manner as it does the low-level inputs. The output of the coder is, then, the combination of the high-level and low-level signals, converted to digital words which were discussed above.

PARALLEL DIGITAL INPUTS. The parallel digital inputs are of four different bit lengths; 8 bits, 16 bits, 24 bits, and 32 bits. Each word is broken into 8 bit sections and integrated into the digital data coming from the coder. When the information word consists of more than 8 bits, the eight most significant bits are integrated into the digital data first, followed by the eight next most significant bits, which make up the next output words, etc. The

PCM TELEMETRY, BLOCK DIAGRAM

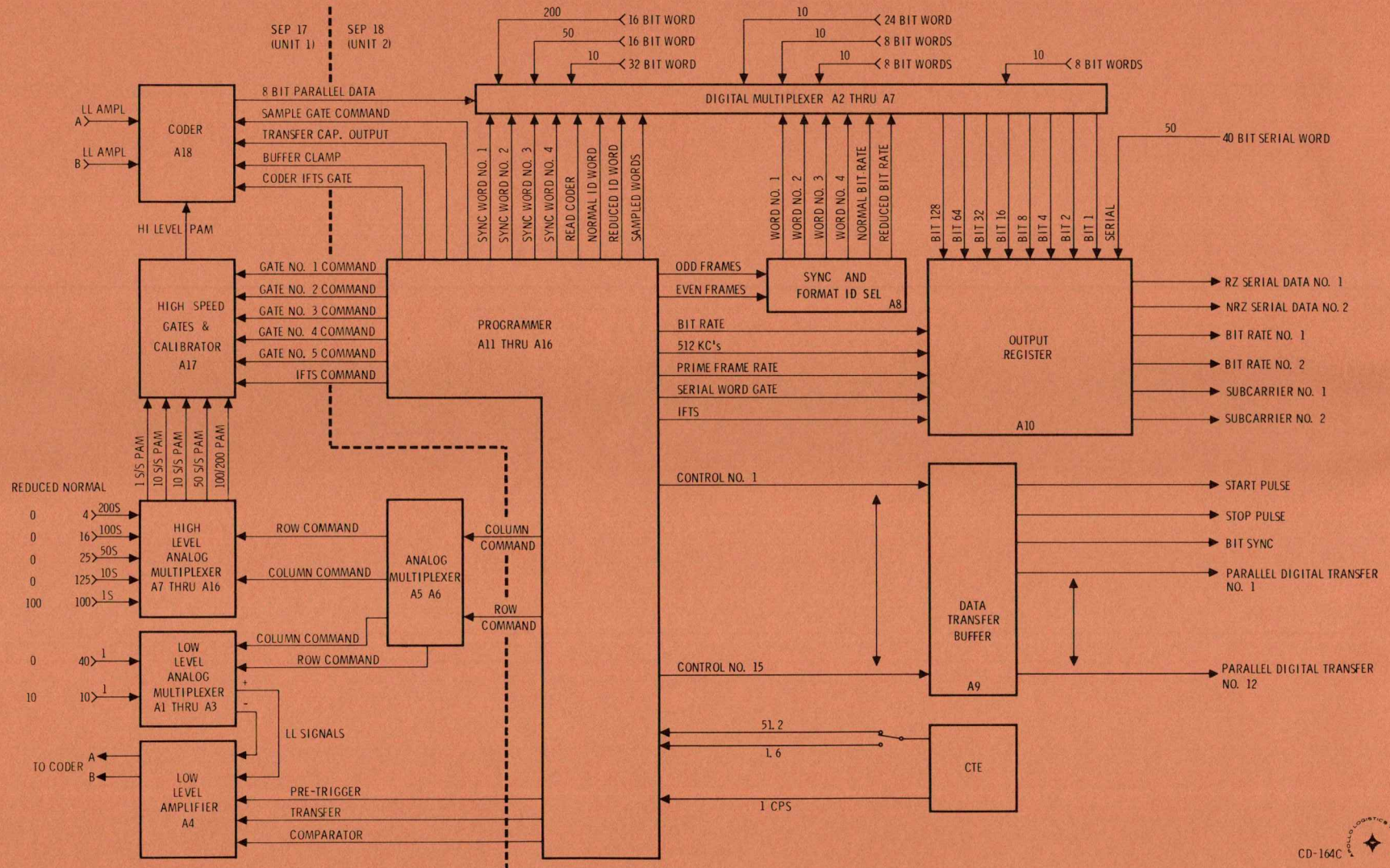


figure 8-1

digital data being sent out of the digital multiplexer to the output register contains all the information to be transmitted except the 40 bit serial word from the computer.

SERIAL DIGITAL INPUT The output register converts the 8 parallel bit words, that it receives, into a single serial pulse train output. The output register also receives one serial bit word from the computer which is 40 bits in length. The parallel bit words must be converted to serial bit words and then a further step is required to change the serial pulse train from return-to-zero (rz) form to non-return-to-zero (nrz) form. The serial digital input is gated into the 128 bit F/F of the parallel to serial converter and from there directly into the rz to nrz converter. The timing for this function is controlled by signals from the programmer.

To insure proper timing of the output signals the programmer supplies timing signals to every section of the telemetry system. To keep the ground station informed as to which prime frame is being transmitted at a specific time, the first four words of each prime frame contain codes indicating which frame is upcoming and whether it is an odd or an even number. This is provided by the programmer through the sync and format ID selector.

DETAILED FUNCTIONAL BLOCK ANALYSIS

A detailed functional block analysis of the units comprising the PCM Telemetry Equipment is contained in the subsequent paragraphs.

PROGRAMMER The programmer establishes the basic timing required for operation of the PCM Telemetry Equipment in the normal and reduced bit rate modes. It also provides a fixed program for sampling the

various channel inputs. Specifically the programmer accomplishes the following:

1. Performs the automatic selection of external or internal clock frequencies.
2. Establishes the basic intervals for periods, bits, words, prime frames, and subframes.
3. Generates the timed commands for signal sampling from a fixed program.
4. Generates the commands for low-level amplifier clamp operations, coder operations, and data transfer operations.
5. Generates sync and format identification words plus the commands for inserting these words into the output data.
6. Generates the commands and timing used to synchronize other spacecraft equipment with the PCM Telemetry Equipment.
7. Performs self checks to determine its own operational status.

Programmer Clock

Two externally generated timing inputs are received by the programmer clock logic, figure 8-2. They are a 512 kc square wave which is used as the basic clock timing, and a 1 cps square wave which provides real time synchronization. Two outputs are furnished by the clock logic, one to the initial stages of the counter in the programmer and a second to the output register. Timing is automatically switched from the external clock input to an internal clock oscillator by the level control

EXTERNAL CLOCK LOGIC CKT

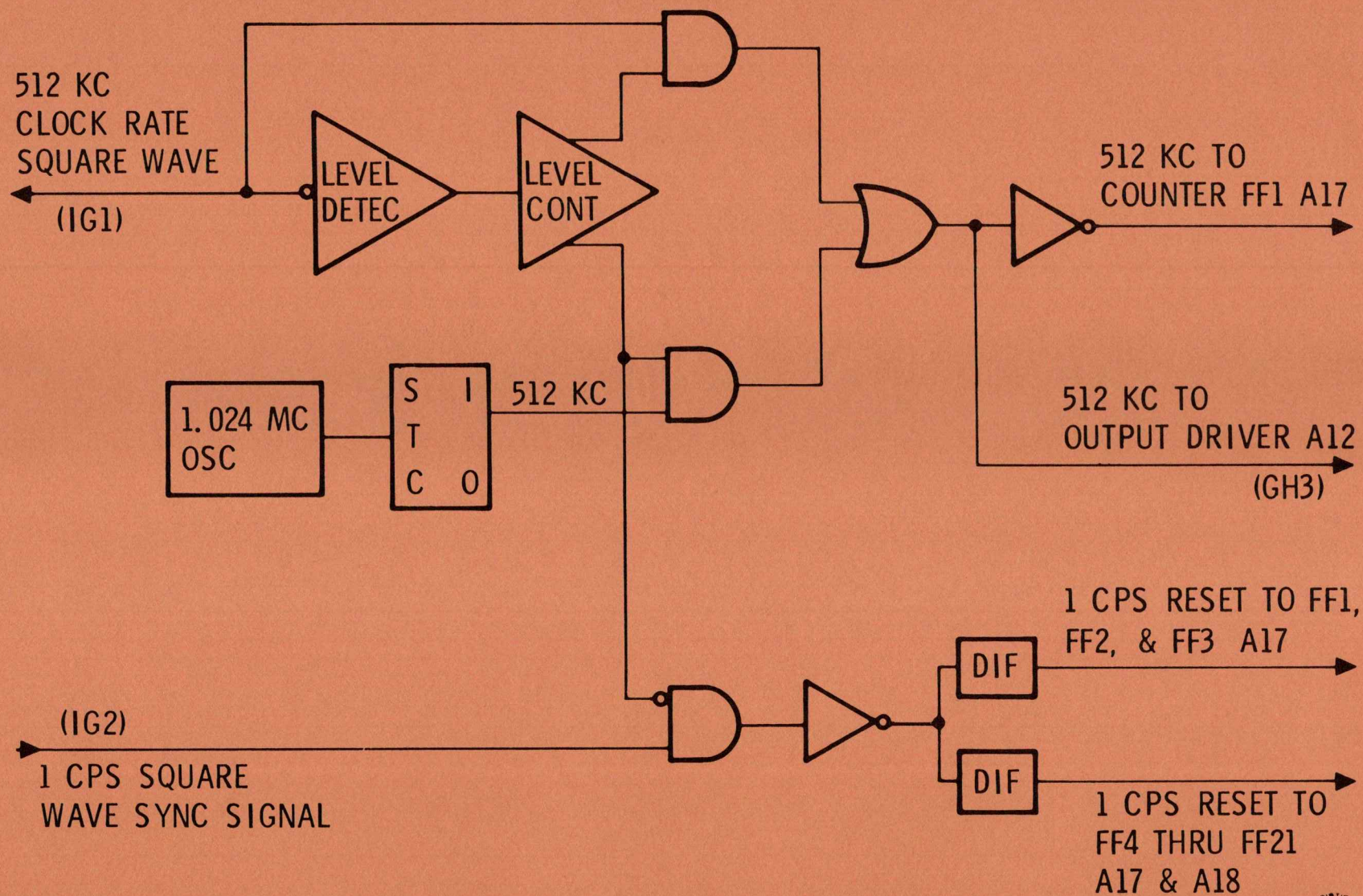


figure 8-2

CD-210



if the external clock input fails for 10 to 20 microseconds. When this occurs, the 1 cps sync input is inhibited and the telemetry equipment operates without external synchronization. If the external clock input is recovered, timing control is automatically switched back to the external clock within 1 microsecond by the level detector and level control. The programmer then recycles to the start of a subframe with the next positive transition of the 1 cps sync input.

The internal clock consists of a 1.024 megacycle oscillator and a single-stage counter flip flop for 2:1 frequency division. This circuit provides a continuous 512 kc square wave output to one of the AND gates which may be enabled by the level control. While the external clock input to the level detector is of sufficient amplitude, the level control enables a second AND gate to pass the external clock input. It is then coupled through an OR gate and an inverter to the first counter stage. The level control also enables a third AND gate to pass the 1 cps sync signal which resets all counter stages at the end of each subframe. If the external clock inputs fail for 10 to 20 microseconds, the level detector causes the level control to inhibit the external clock and 1 cps sync input. The internal clock signals are now passed to the first counter stage. If the external clock input recovers after the switchover to internal, the level detector causes the level control to revert to the external timing within 1 microsecond. After this switchover, all stages of the counter are reset by the next positive transition of the 1 cps square wave input.

Figure 8-3 provides a logic diagram of the programmer counter matrix. It is a flexible counter which provides submultiples of the basic 512 kc clock input. The outputs are subsequently decoded

to produce specific timing outputs. It consists of 28 bistable flip-flop stages with four stages allotted for a period counter, three for a bit counter, seven for a word counter, seven for a prime frame counter, six stages used for generation of prime frame ID and one additional stage which is as a word sync alternator. Each stage of the counter is assigned an "F" number. The outputs of these flip-flops have two logic levels. A logic ONE has a $+6.0 \pm 0.5$ volt level and a logic ZERO has a 0 ± 0.5 volt level. The flip-flops may be set or reset by applying a negative voltage transition to its respective set or reset lines. The differentiation circuit is a network which passes only negative voltage transitions, therefore, when the clock signal is fed in, the differentiation circuit (DIF) will send out a series of negative pulses. This output is used to trigger the flip-flops of the countdown chain.

Period Counter The first four stages of the period counter are connected to provide a 10:1 frequency division. A bit rate output of 51.2 kc is furnished by the final stage (F4).

Flip-flops 1,2, and 3 in figure 8-3 make up a modified counter which divides the input frequency by five. All three F/F's are initially reset. The first negative excursion of the clock pulse will cause all three F/F's to be set. As the reset outputs of F/F 1 and F/F 2 go false, each will cause the subsequent stage to change operating states. The second pulse will cause F/F 1 to be reset, but will have no effect on the other F/F's. The third pulse will cause F/F 1 to be set and F/F 2 to be reset. The fourth pulse will cause F/F's 1 and 2 both to be reset. The fifth pulse will cause F/F 1 to go to a set condition which in turn causes F/F 2 to be set. As a result of the negative going pulse at the reset side of F/F 2, F/F 3 will

PROGRAMMER COUNTER MATRIX

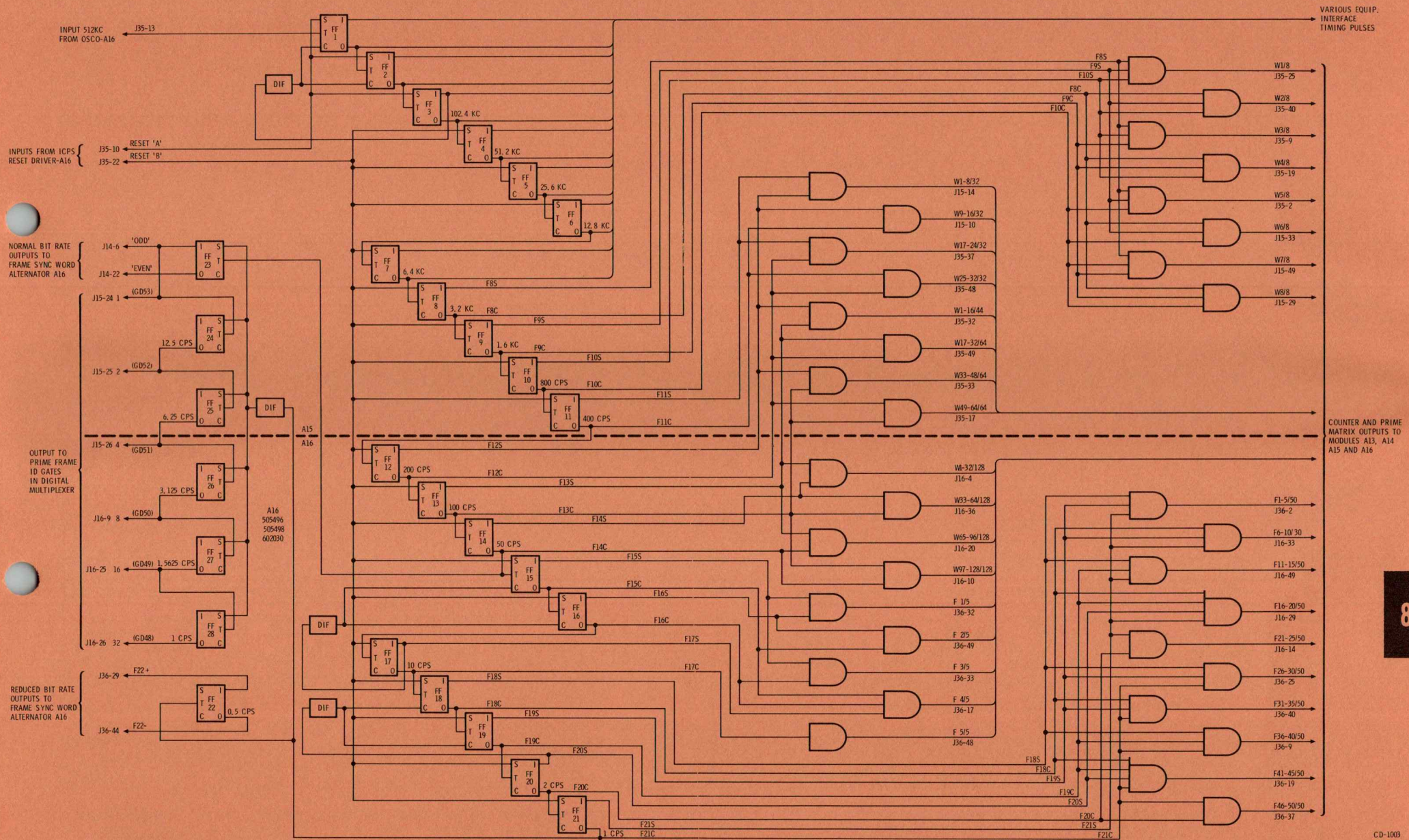


figure 8-3

change states by going to the reset state. The set output of F/F 3 will see a negative excursion which causes the DIF to send a reset pulse to F/F's 1 and 2. Thus, the three F/F's return to the reset, or initial, condition in five full cycles of the input clock. This type circuit is referred to as a modulus 5 counter.

Bit and Word Counters

The initial stage (F5) of the bit counter has an input of 19.5 microseconds, the interval allotted for a bit time. Since the bit counter is connected to provide an 8:1 countdown, stage F7 generates the word rate output of 6.4 kc. Stage F7 also drives the word counter stages which are connected to provide a 128:1 countdown. Thus, the final stage of the word counter (F14) produces a square wave output which has a cyclic interval equal to 128 word times or one prime frame during normal bit rate operation. Stages F5 through F14 act as a standard counter, each stage dividing its input by two.

Stage F9 provides the actual bit rate output during reduced bit rate operation and stage F10 provides the interval. Stage F13 provides an output whose interval is equal to a reduced bit rate word time (5 milliseconds).

Prime Frame And Subframe Counters

Stage F14 of the word counter drives the prime frame counter and the prime frame ID counter. The prime frame counter is connected to provide a 50:1 countdown of the word counter output. The output from stage F22 is a square wave whose half cycle interval is equal to 1 second, the interval allotted for a subframe.

Stage F21 produces a subframe rate output of 1 cps. This output is also differentiated and used to reset the prime frame ID counter stages once each second.

Prime Frame ID Counter

Flip-flops 23 through 28 make up the prime frame ID counter. This counter will progress through the binary count of 000001 (= 1 decimal) to 110010 (= 50 decimal) to correspond to the prime frame being transmitted. This six bit binary code will be transmitted during word four of each prime frame. The prime frame ID counter is cleared at the end of each subframe by the differentiated 1 cps input. The binary numbers are furnished to the digital multiplexer gates for insertion into the PCM data. During normal bit rate operation, the binary numbers are inserted into word 4 of the data output. During reduced bit rate operation, binary 000001 is inserted into word 4 of every frame, as there is only one frame per second.

Bit Rate Control

Figure 8-4 illustrates the normal and reduced bit rate control logic. This logic implements the switchover from normal to the reduced bit rate mode within the programmer. It also produces normal (GD6) and reduced (GD7) commands to the digital multiplexer gates which causes the bit rate format code to be inserted into the PCM serial train. This is accomplished by feeding the output of the bit rate selector switch to two memory flip-flops. When the normal bit rate mode is selected, the mode information is stored during the interval from words 33 to 64 of prime frame 1. The normal bit rate command is then generated during word time 100 and format ID word is inserted into

NORMAL & REDUCED BIT RATE CONTROL

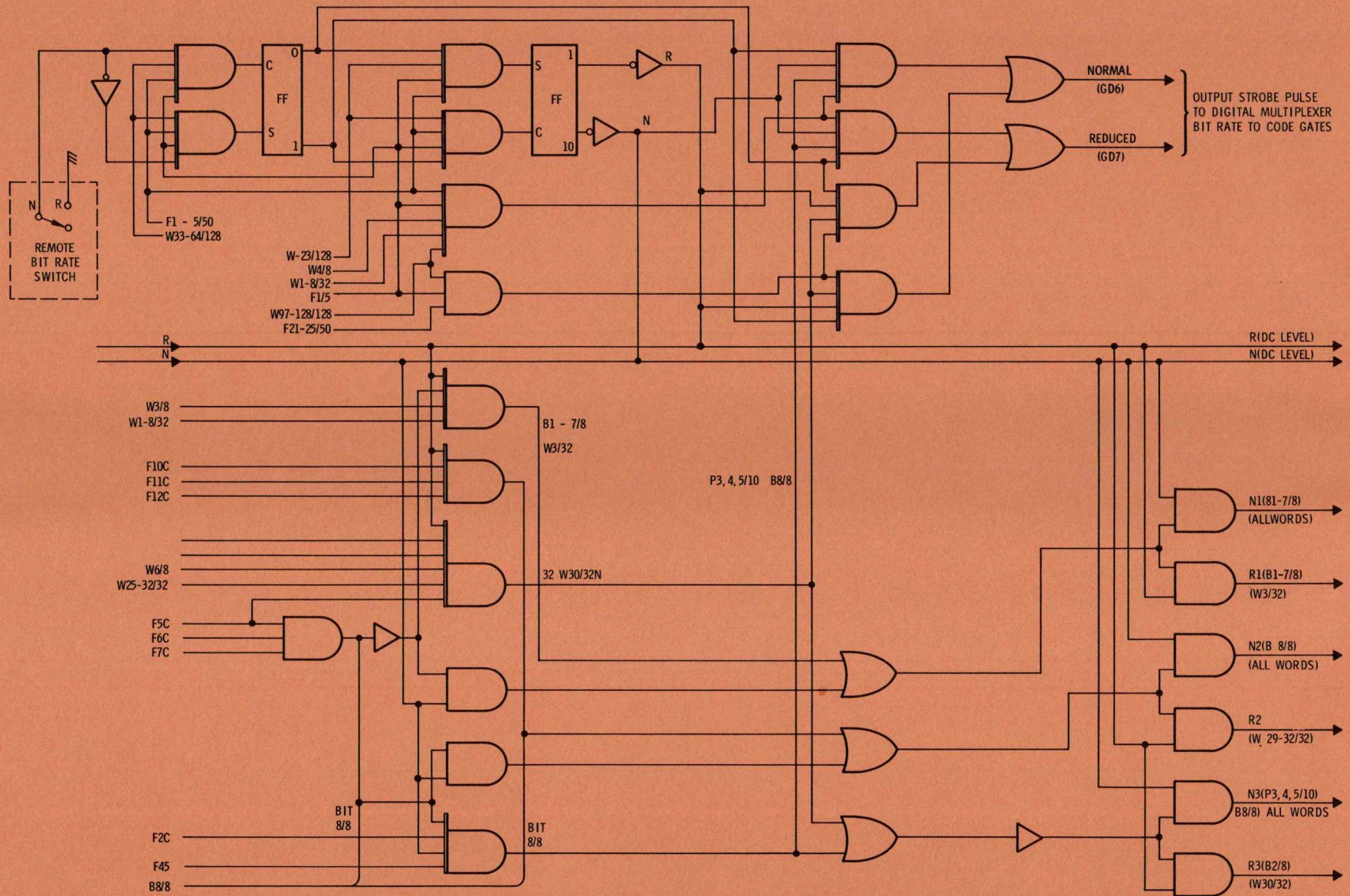


Figure 8-4

CD-1004

the PCM data at the digital multiplexer gates. Similarly, when the reduced bit rate mode is selected, the mode information is stored during word times 33 to 64, but the reduced bit rate command is generated during reduced bit rate word time 84. Switchover from normal to reduced mode will occur at the start of a subframe. If a change in bit rate mode is made after prime frame 1, word 64, has begun, the remainder of the subframe will operate at the original bit rate and switchover will occur at prime frame 1, word 33, of the next subframe.

Row and Column Commands

The row and column commands for the high-level and low-level analog gates is identified as the sampling rate control logic. Each row and each column command is generated by one AND gate except in the 1 sps channels. Table 8-3 shows the row and columns for each sampling rate.

The column commands for the 1 sps sampling rate in both the high-level and low-level analog gates are developed by an AND gate structure.

Associated AND-OR gate structures develop the word gates utilized in the digital multiplexer gates for all 8-bit parallel binary words, for the 32 bits of the prime frame sync word, and binary one's of the IFTS words. The sampling commands to the digital multiplexer gates for the 32 bit, 24 bit, and the 16 bit parallel binary words are also developed by similar associated AND-OR gate structures.

Coder Control

The coder control circuit provides four commands. They are: the IFTS command, the sample and hold gate command, the buffer clamp command, and the

transfer capacitor output gate command. An example discussion of one command is given below to illustrate the Boolean derivations and logic structure needed to develop these commands. Figure 8-5 illustrates the logic circuitry used to generate the sample and hold gate command.

W3/8 is read as "word three of eight" thus, AND gate W3/8 would have a logic one output for 156 microseconds out of every 1248 microseconds.

The term W1-8/32 indicates "a logic one will be present for words one through eight out of every thirty-two words". This logic one is present four times per prime frame, since there are four groups of thirty-two words in a prime frame.

Low Level Amplifier Commands

AND-OR gate structures similar to those in the example above, are used to produce the following commands for the low-level amplifier: the pretrigger commands, the comparator gate command, the transfer capacitor input command, and the bootstrap command.

Sampling Commands

Commands GB1 through GB5 for the five sampling gates used in the high-speed gates and calibrator are developed by logic structure in the programmer. The commands for IFTS gates 1 through 4 and GB10 are produced by separate AND gates.

The logic structure which develops the commands for the data transfer drivers and the output register are constructed as follows. The START and STOP pulses for twelve 8-bit parallel binary words are produced by the same AND-OR gate structures which produce their sampling commands to the digital

TABLE 8-3

SAMPLING RATE PER SECOND	NO. OF COMMANDS		NO. OF CHANNELS		Matrix Arrangement	NOTES
	Row	Column	Normal	Reduced		
200	1	4	4	0	1X5	1 gate not used
100	5	4	16	0	5X5	9 gates not used
50	7	4	25	0	5X7	10 gates not used
10	13	10	125	0	10X13 (4-5X5 and 6-1X5)	5 gates not used
1	5-AND (LL) 21-AND (HL) 10-OR (HL)	10	100	100	10X10 (4-5X5)	ALL gates used

SAMPLE AND HOLD GATE COMMAND

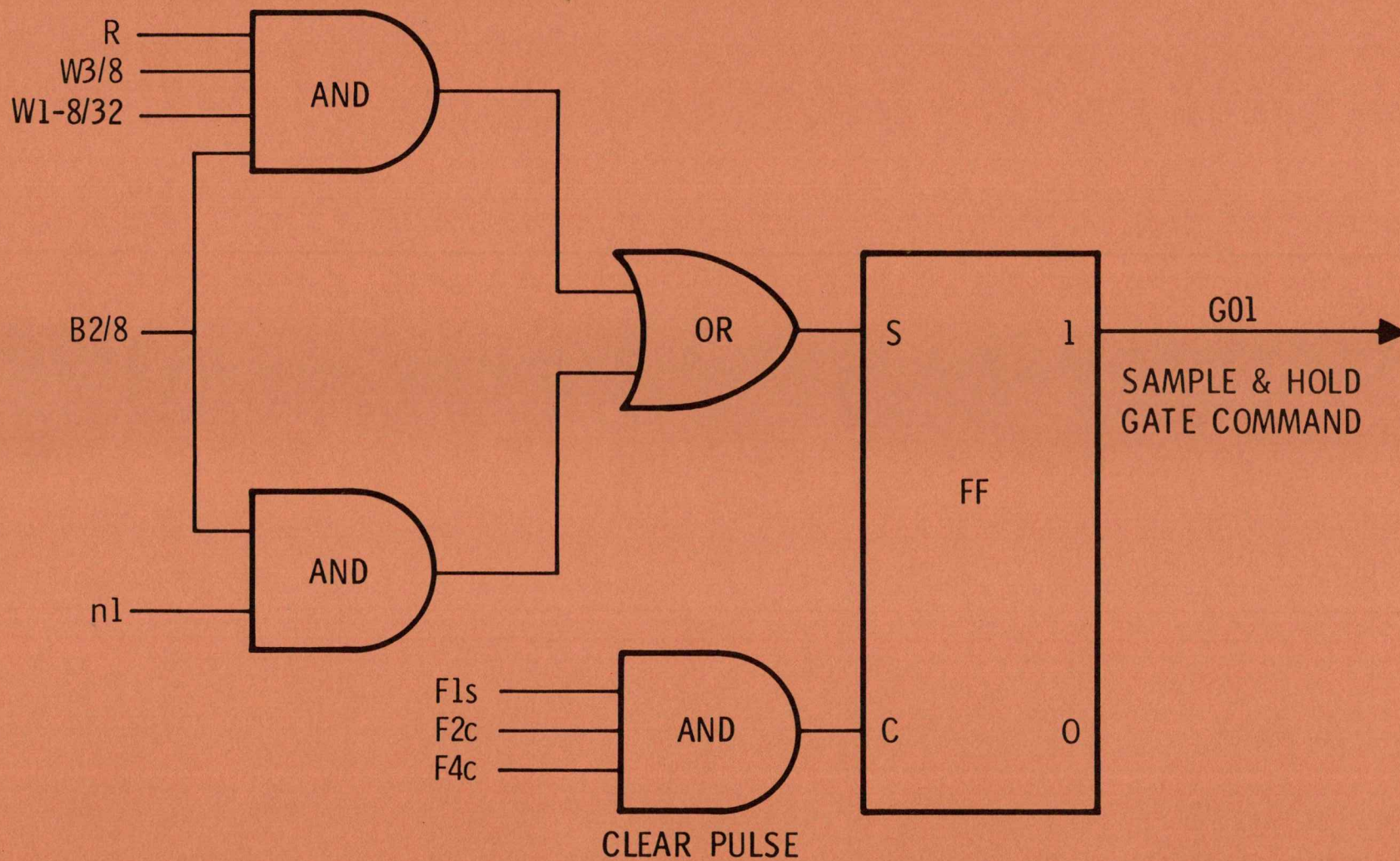


figure 8-5

multiplexer gates. The START and STOP pulses for the 40-bit serial binary word and bit sync pulse for the 40-bit serial binary word are produced by gating structures. The bit sync pulse for the 40-bit serial binary word is developed by three AND gates and a single OR gate. These three commands and the twelve START and STOP pulses are connected to the data transfer drivers for utilization with other spacecraft equipment. The two IFTS commands to the output register are produced by separate logic structures. The subframe rate signal, the bit rate signal, and the prime frame signal are also developed by separate logic structures.

HIGH LEVEL ANALOG MULTIPLEXER The high-level analog multiplexer samples the 270 high-level (0 to +5 volts) analog input channels from the spacecraft equipment. They form pulse amplitude modulated (PAM) outputs for each channel input. The pulses occur at the sampling rate of the channel while the amplitude of each pulse is representative of the analog input at the sampling time. The high-level analog gates are comprised of matrix combinations, basically arranged such that five channel inputs (columns) are provided per row with multiple rows used to form the desired matrices. The five gates in each row utilize a common sequencer gate. Table 3 lists the matrices required to handle the 270 channel inputs and supply five PAM outputs to the high-speed gates and calibrator.

Sequencer Gate

Five channels are passed through primary sampling gates and combined through a series sequencer gate. The sequencer gate prevents a shorted primary gate from causing loss of data from more than four gates. (The data through the shorted gate would not be affected.) This raises the overall

reliability. Use of a sequencer gate also lowers the shunt capacity across the active channel and lowers the leakage current through the active channel caused by inactive gates.

The disadvantage of the sequencer gate is that any offset error of the sequencer gates is added to the total error. Also, the chance of failure of any given channel is increased because of the additional series component although the overall reliability of the system, not considering the failure of less than five channels, is increased. A shorted sequencer gate will not cause a loss of data.

The high speed gates perform the function of sharply timing each of the pulses in the PAM train. The primary and secondary gates do not turn off sharply so the trailing edge of each PAM pulse at the input to the high speed gates gradually trails off to zero. If a PAM pulse were to appear in the sequencer gates before the preceding pulse decays, cross talk would occur. The high speed gates cut off each pulse sharply prior to combining all pulses into one serial PAM train.

Row And Column Matrix

A semi-block schematic is provided by Figure 8-6 of a typical 1x5 row and column matrix. It is shown that an individual gating element consists of a three-winding core and an integrated chopper. The sector-wound core is a small toroidal bobbin with one of its windings used for core reset. A second winding, controlled by the row and column drivers, is used to set the core while a third or output winding is used to control the switching of the integrated chopper. A specially constructed transistor with two emitters is used as the integrated

PCM PRIMARY MULTIPLEXER GATES

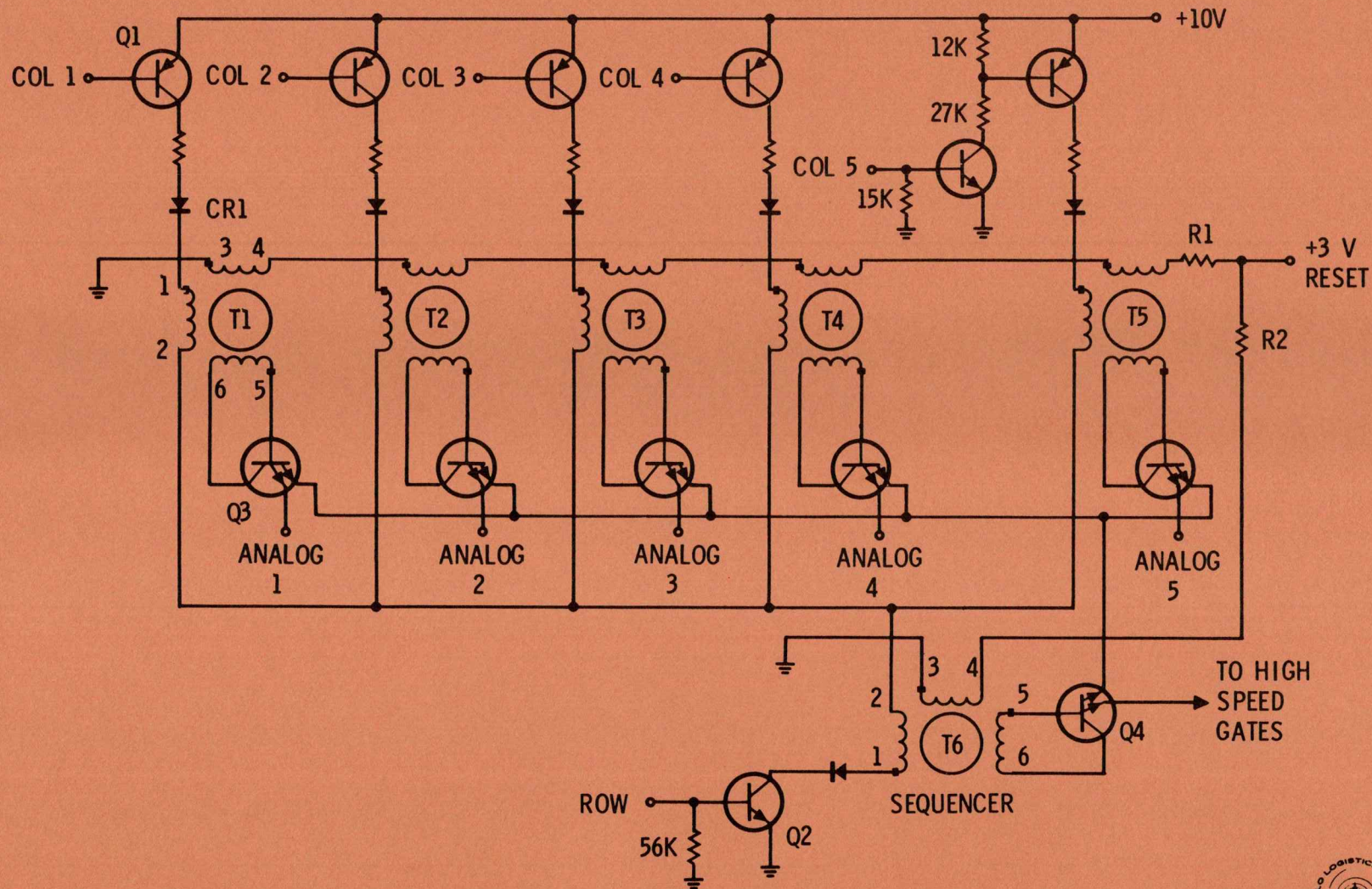


figure 8-6

CD-212A



chopper. The base-collector junction is driven by a core winding. One emitter is connected to an analog input. The second or output emitter is connected in common with the emitters of four other input gates and a sequencer gate.

In a non-sampling state, the core associated with each column is reset by the reset winding. The integrated chopper, in a non-conducting state, allows the dc reset current to bias the core such that a large flux transition occurs when sufficient current is passed through the set winding. A complete path for current through the set winding is provided by the column and row drivers when they are switched on by column and row inputs from the programmer. The column and row inputs must be active in coincidence for a period of 125 microseconds to cause a current to be induced into the output winding which is connected to the base-collector junction of the integrated chopper. This current forward biases the chopper which saturates and allows the analog voltage at the input emitter to appear at the output emitter. The saturation voltage drops of the two emitter-collector junctions of the chopper are cancelled, thus keeping error introduction to the analog voltages at a minimum. This type operation is similar to that of a bright switch. At the end of the 125-microsecond input switching pulse, the core is reset by the dc current through the reset winding and its associated resistor. A diode connected in series with the set winding eliminates sneak paths in the matrix.

Each input gating element, in a given matrix, is selected by pulsing all drivers in one column in coincidence then pulsing the row drivers sequentially. With the sequential operation of the various gating elements, a serial PAM output is gated to the high-speed gates and calibrator.

ANALOG MULTIPLEXER DRIVERS The analog gate drivers perform the switching required by the high and low-level analog gates for sampling the analog inputs upon command of the programmer. A row driver and a column driver are used for each analog input.

Row and Column Drivers

A row driver is switched on by a positive-going row command from the programmer. Each column driver is a two-stage, direct-coupled amplifier. When switched on by a positive-going column command from the programmer, it completes the path through the set winding of the analog gating toroid.

HIGH SPEED GATES AND CALIBRATOR The high-speed gates and calibrator consists of two functional areas which are interrelated only through the IFTS. The high-speed gates perform the gating operation of reducing the five high-level PAMs into the single PAM output furnished to the coder. The calibrator generates the voltage used for system calibration and checking of the high-speed gate operation.

High Speed Gates

Five high speed gates are used, one for each input from the high level analog gate. The operation of the high-speed gates is similar to that of the high-level analog gates; however, pulse widths are more closely controlled to insure against overlap of channel inputs. Figure 8-7 shows a block schematic of the high-speed gates. The circuit used differs from that of the high-level analog gates in that a four-winding core and two integrated choppers are used for each gating element. One chopper is used as the input gate and the second used as a buffer between input and output. Also included with each gating element is a command driver which is switched

PCM ANALOG MULTIPLEXER

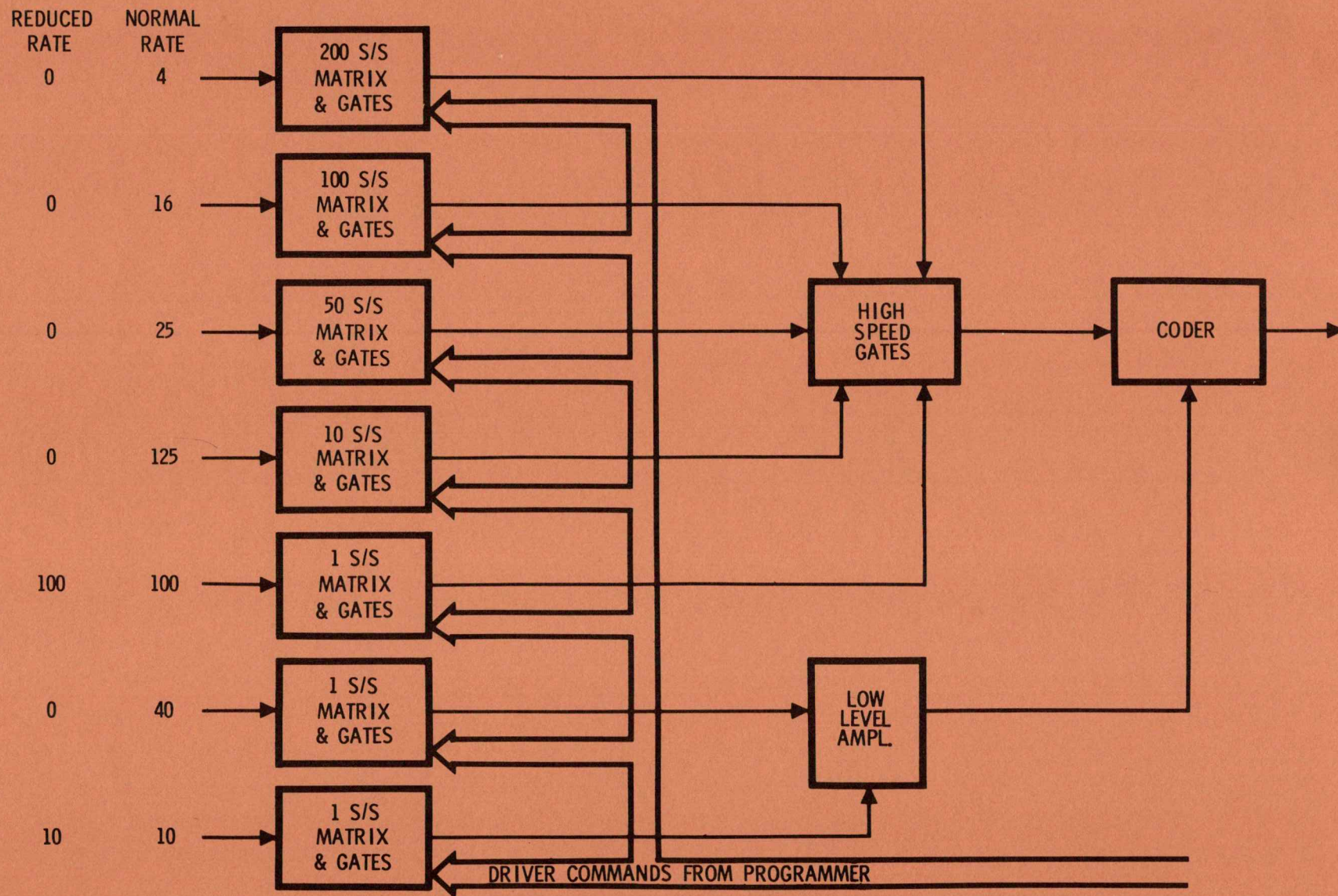


figure 8-7

on by a sample command from the programmer. When switched on, the driver completes the path for the set windings of the cores, allowing the analog input to be gated through a common output bus to the coder.

IFTS Circuits The high-speed gates IFTS circuits check the operation of each high-speed gate for proper operation. This is accomplished by using a precision voltage furnished by the calibrator. When a high-speed gate is to be checked, a corresponding IFTS check command is furnished to one of the structures by the programmer. As a result, the precision voltage is connected to the input of the corresponding high-speed gate and is passed to the coder as in normal operation. The voltage is then coded into a binary PCM word which is checked by a comparator circuit in the coder. If the binary pattern is incorrect for the precision voltage, the coder notifies the IFTS circuits of the high-speed gate. These circuits, in turn, set an error flip-flop and a NO-GO output is routed to the IFTS system.

Calibrator

The calibrator produces the precision ($\pm 0.2\%$) voltage outputs: +6.1 and 34.6 millivolts to the low-level amplifier, +0.755 and +4.331 volts to the high-speed gates, and +0.7555 and +4.331 volts to the sample and hold circuit of the coder. These voltages are used in the loop checks to determine the operational status of the low-level amplifier, the high-speed gates, and the coder, respectively. Generation of the precision voltages are generated by a series of reference current sources. The precision voltages are obtained by tapping the desired potentials from precision resistor network. In addition to generating these precision outputs, the calibrator also performs self checks to determine its own operational

status and supplies signals to the IFTS equipment if a failure occurs in the precision outputs. This is accomplished by generating a second precision source and comparing this output with the normal precision output of the calibrator. If the two differ by more than 2% an error signal is generated to the IFTS system.

LOW LEVEL ANALOG MULTIPLEXER The fifty low level analog channels are sampled by the low level analog multiplexer to form a single PAM output which is sent to the low level amplifier.

The low level analog multiplexer is similar to the high level analog multiplexer except that instead of one primary gate per channel, two are necessary because of the two wire (differential) inputs.

Sequencer Gate

As in the case of the high level analog multiplexer, groups of five channels are passed through sequencer gates. This has the same advantages and disadvantages as in the high level multiplexer except that the actual leakage current during sampling time is increased rather than decreased. This is because the addition of the sequencer subtracts from the ability of the current clamp at the output of the multiplexer to maintain zero leakage current. The current clamp is designed to balance the current through all closed gates to zero just prior to sampling time. However, when the sequencer gate and primary gates are opened the total leakage current is effected by the leakage current of the sequencer gate just prior to sampling and the leakage current of the four inactive primary gates in the sequencer group.

High speed gates are not necessary in that the low-level amplifier, will do the same job as the high speed gates associated with the high-level multiplexer.

Sampling Rate

The low-level analog gates sample 50 low-level (0 to 40 millivolts) differential analog inputs based upon commands from the programmer. The set inputs (row and column commands) to the gating elements are coincident for 250 microseconds, as compared with 125 microseconds for the high-level analog gate.

LOW LEVEL AMPLIFIER A block diagram of the low-level amplifier is shown in Figure 8-8. This amplifier converts the low-level (0 to 40 millivolt) differential inputs from the low-level analog gates into single-ended outputs having an amplitude of 0 to 5 volts. These outputs are then transferred to the sample and hold circuit of the coder for storage and subsequent coding into PCM words. The low-level amplifier also performs self-checks to determine its operational status. The low-level amplifier consists of:

1. voltage-to-current converter
2. voltage and current amplifier
3. timing and gating circuits
4. floating power supply
5. flying capacitor circuit
6. IFTS circuits (not to be confused with the IFTS System)
7. error circuits

The basic amplifying circuits consists of the voltage-to-current converter and the voltage and current amplifier. The voltage-to-current converter converts the low-level differential voltage to a current signal which is furnished to voltage and current amplifier. The converter consists of a differential pair of composite emitter followers; each emitter follower is comprised of three compound-connected transistors. The voltage and current amplifier produces the primary gain of the low-level amplifier. It consists of a differential pair of cascaded transistors with a negative feedback loop. The overall closed loop gain of the low-level amplifier is 125.

Clamping Operations

To insure that the low-level amplifier is balanced and biased correctly, three sequential clamp operations are performed during non-sampling of low-level inputs. They are the common clamp, the voltage clamp and the current clamp. The timing and gating circuits and the floating power supply are provided for these clamp operations.

The timing circuits initiate and control the clamp operations while the floating power supply provides the floating and fixed potentials and grounds. The error circuits perform any necessary corrections to the amplifier as a result of the conditions detected during the clamp operations. This is accomplished by three monostable multivibrators and various gating elements.

Common Mode Clamp

The common mode clamp operation biases the low-level analog gates to a fixed off potential and increases both common mode (all voltages not in phase with input) and crosstalk (inter-channel)

LOW-LEVEL AMPLIFIER

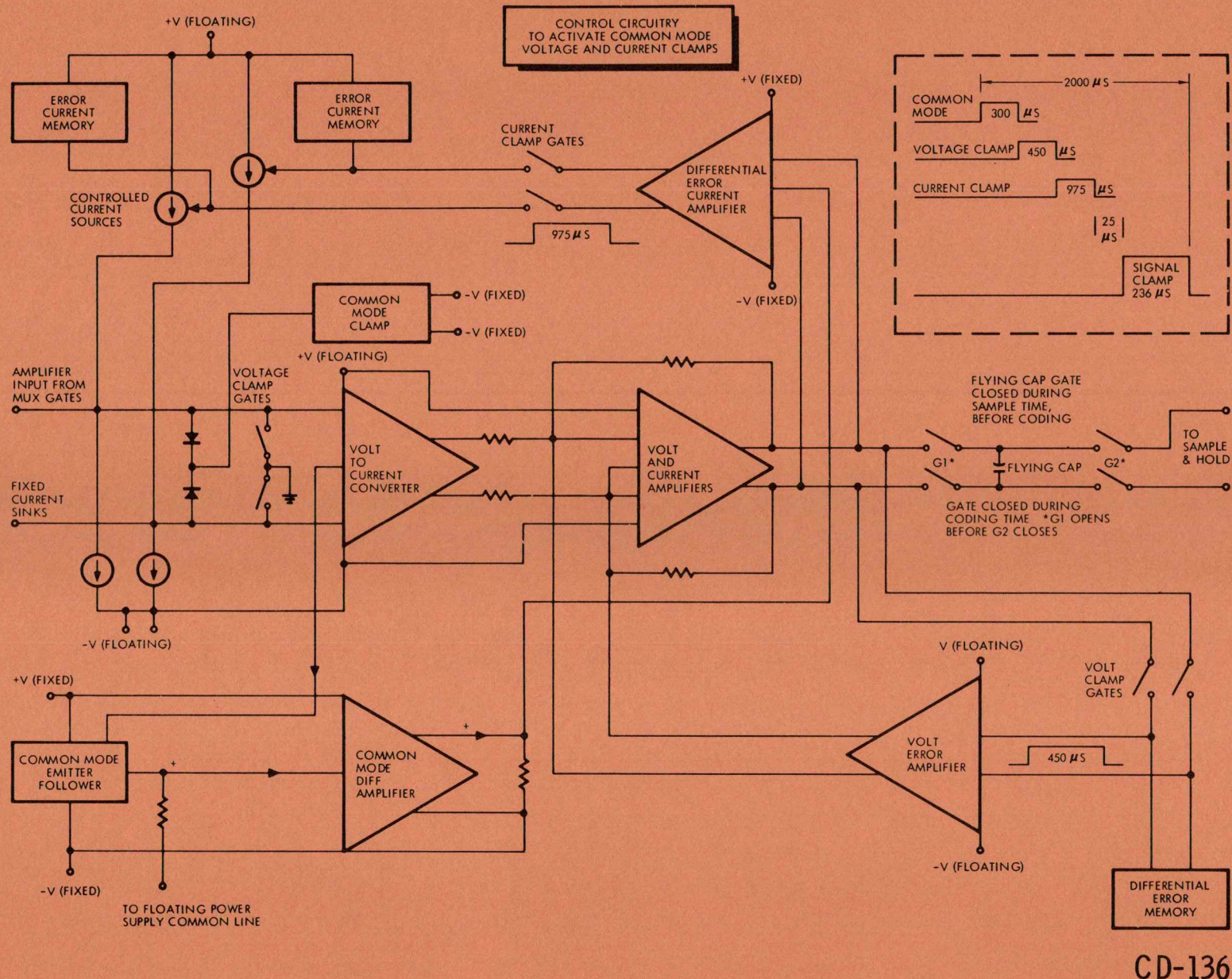


figure 8-8

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rejection. The common-mode clamp multivibrator produces a 300 microsecond interval during which diodes connect both input lines to -5 volts.

Voltage Clamp

The voltage clamp operation is performed after the common-mode clamp. It insures that the amplifier output is zero volts when the input is grounded. The operation is implemented by a second monostable multivibrator in the timing circuits approximately 4 microseconds after the end of the common-mode clamp operation. The duration of the voltage-clamp pulse is approximately 450 microseconds. During this interval, the floating power supply outputs are switched to fixed potentials and the floating power supply is charged to the fixed potentials. The voltage-clamp pulse enables signal ground to be connected to the amplifier input lines and connects the amplifier output lines to the voltage error amplifier and the differential error memory. If the output lines have a differential output other than zero, the error voltage is stored and is used to control a pair of current sources. The current sources add to or subtract from the collector currents of the voltage-to-current converter to compensate for output differential unbalance. Since the errors are stored, the final error can be maintained for correction during input sampling.

Approximately 5 microseconds after the voltage clamp operation ends, a current clamp operation begins. This operation is initiated by the third monostable in the timing circuits which produces a current clamp pulse for 975 microseconds. During this interval, fixed potentials are again supplied to the basic amplifier and the error circuits. In the current clamp operation the total current and the differential input current are both corrected.

Total current to the input stages of the voltage-to-current converter is provided by two constant current sources. Total current in the input stages is sensed by the common-mode emitter follower and is furnished to the common-mode differential amplifier. One side of this differential amplifier is referenced to signal ground causing the amplifier to produce an output unbalance proportional to the magnitude of total current, if any, flowing in the input stages. This output is used to control the emitter bias of the differential error current amplifier. The differential error current amplifier is also controlled by a feedback loop connected from the output stages of the voltage and current amplifier.

Current Clamp

During the current clamp operation, an error feedback path provides correction of the input and total current of the voltage-to-current converter. If the output lines of the voltage and current amplifier are not zero, for the existing input and total current, the error is stored. It is then used to control two constant current sources that change the input current of the voltage-to-current converters and a new error correction is created from the total current, and voltage and current amplifier output difference. As a result, the input and total current of the voltage-to-current converter is corrected until the inequalities of the basic amplifier have been overcome and the output lines have a difference output of zero. At the end of the current clamp pulse, the final error correction is stored in the error current memories. The error current memories continue to provide the correction currents for the voltage-to-current converter during dead time and input sampling time. Dead time is the time when the low-level amplifier is not sampling inputs.

At conclusion of the current clamp operation, the low-level amplifier is ready to accept a data input. The total amplifier has been corrected for all variations which could introduce a significant error into the sampled low-level input. The error memory circuits continue to provide corrections and all clamping gates are disabled.

Signal Sampling

Following the current clamp operation, input signal sampling is performed. During this operation, floating potentials and a floating ground are supplied to the basic amplifier and the error circuits by the floating power supply. For the input signal sampling, the low-level amplifier receives a command from the programmer which connects the common mode point of the voltage-to-current converter to floating ground for the entire sampling period. Next, the programmer furnishes the low-level amplifier with an input command which connects the flying capacitor circuit across the voltage and current amplifier output. The flying capacitor charges to the amplifier output voltage during the input command. The sample and hold portion of the coder transfers the flying capacitor output to the coder. There one side of the flying capacitor is connected to signal ground converting its output signal.

IFTS Circuits

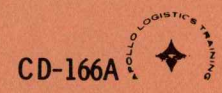
The IFTS circuits check the overall operation of the low-level amplifier based upon a precision input voltage furnished by the calibrator. This is accomplished by IFTS commands from the programmer. For the normal bit rate mode this operation is performed 50 times per second and for the reduced bit mode it is performed 10 times per second. During these checks 34.6 millivolts is gated to the input of the low-level amplifier. The voltage is amplified

and subsequently coded by the coder. The coder, in turn, checks the binary output for a known pattern and returns a signal indicating whether the code was correct for the IFTS voltage input. If the code was incorrect, an error flip-flop is turned on and a NO-GO signal is routed to other spacecraft equipment. The error flip-flop is reset by an external reset.

CODER The coder converts the PAM analog inputs from the high-speed gates and calibrator and the low-level amplifier into 8-bit PCM words. The block diagram of the coder is shown in figure 8-9. The 8 parallel bit PCM words are subsequently made available to the digital multiplexer gates. For a zero volt input, the coder generates the binary equivalent of decimal one (00000001). The binary code is increased by a binary ONE for each additional 19.7 millivolts of input voltage up to 5 volts; thus, at 4.98 volts, the binary equivalent of decimal 254 (11111110) is generated. For input voltages below zero volt a binary code of (00000000) is generated. For inputs of 5 volts or more, a binary code of (11111111) is generated.

The coder is a successive approximation type. The most significant bit of the PCM word is formed first with the less significant bits formed by successive approximations. For the coding operation, the analog input is stored and made available for each approximation. For the first approximation, a negative precision reference voltage is connected to one end of a precision summing network. This results in a half scale current. The analog voltage is connected to the other end of the summing network and the resultant current is furnished to a decision circuit. If the input voltage results in a current equal to or greater than the half-scale current, a binary one is generated for the most significant bit output and the half-scale current

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is left in the summation for the next approximation. If the input current is less than the half-scale current, a binary zero is generated for the most significant bit output and the half-scale current is switched out of the next approximation.

For the next most significant bit, a quarter-scale current is used in the summation. If the input current was greater than the half-scale current, the quarter-scale and half-scale currents are summed with the input current. If the input current was less than the half-scale current, only the quarter-scale current is summed with the input. In either instance, a decision is made causing a second binary bit to be generated. The process continues until the 8-bit PCM word is formed.

Coder Components

The coder consists of a sample and hold circuit, timing generator, eight weighted-current flip-flops, a differential error amplifier, reference voltage circuits, IFTS circuits, and various logic structures to implement gating and control.

Sample and Hold Circuit

The sample and hold circuit stores the analog inputs while the coding operations are performed. It is basically an input buffer amplifier with an input impedance greater than 100 megohms, a storage element to hold the analog input, and an output buffer amplifier for the coder summing network. As shown in figure 8-9, it consists of two command gating elements, a gating element for low-level amplifier inputs, a differential amplifier, a gated bridge, a holding capacitor, and a buffer amplifier.

The programmer supplies the timing to initiate the sample and hold operation. Before the sampling and coding of analog inputs, the programmer commands the sample and hold circuits to perform an input clamp operation. This operation clamps the input line from the high-speed gates to zero volts. During sampling time, an analog input is gated to this circuit. If the analog input is from the high-speed gates (high-level analog input), it is made available to the differential amplifier when the high-speed gates are closed.

If, however, the input to be coded is a low-level input from the low-level amplifier, the programmer furnished a transfer capacitor output command to the sample and hold circuits. This command causes the analog input to be passed to the differential amplifier.

Differential Amplifier

The differential amplifier forms a unity gain loop with the buffer amplifier, however, this loop is closed only during sampling time. When the programmer commands the sample and hold circuits to sample the output of the amplifier, the gated bridge closes the loop and it remains closed for the duration of the sample command. During this interval, the differential amplifier loop achieves a balanced condition and the holding capacitor is charged or discharged to input voltage. At the end of the sample command, the loop is again opened. Since the buffer amplifier has a very high input impedance, the holding capacitor retains its charge and acts as a constant voltage source to bias the buffer amplifier, causing it to act as a constant voltage source. Its output is furnished to the precision summing resistor

network to be coded into a PCM word. The coding process is initiated by the same sample command which closed the differential amplifier loop. This is furnished to the timing generator of the coder to initiate the internal timing required for the coding process.

Reference Voltage Circuits

In the coding operation, a negative reference voltage for the coding operation is provided by the reference voltage circuit. For a coder input of zero volts, it also furnishes a 19.7 millivolt input to the summing network for the insertion of a binary ONE into the least significant bit slot. Both voltages are derived by temperature-compensated constant current sources that provide precision outputs.

Timing Generator

Timing for the coding operation is supplied by the timing generator. It consists of a series of "half-shot" circuits which generate code sequential pulses from the sample command input. These pulses provide the sequential timing for successive approximations and are checked within the timing generator to provide differential error amplifier query pulses.

Weighted-Current Flip-Flops

With the sample command from the sample and hold circuit, the 128-bit flip-flop is set and the remainder of the weighted-current flip-flops are reset. As a result, the negative reference voltage is gated to the 128-bit summing resistor by the AND gate connected to the set output of the 128-bit

flip-flop. All other weighted-current flip-flops are reset by the input and gate signal ground to their respective summing resistors. With the resultant current flow in the summing network, the junction of the common summing resistor and the 128-bit summing resistor assumes a positive or negative polarity with respect to signal ground. If this junction is positive (analog input is greater than one-half scale), the differential error amplifier is unbalanced and sets an output flip-flop. One side of the differential error amplifier is referenced to signal ground. The output flip-flop furnishes normal and inverse outputs to two AND gates that control the digital reset flip-flop. Both AND gates receive a pulse from the timing generator. For the above conditions, the control flip-flop is reset and furnishes a binary zero on its set output. Since its set output is connected to an AND gate which controls the resetting of the weight flip-flops, the 128-bit weighted current flip-flop cannot be reset. Thus, a binary one is furnished as an output for the 128-bit and the half-scale current remains in the summation network.

If, however, the junction of summation network is negative, indicating the analog input was less than the one-half scale, the digital reset control flip-flop is set and the 128-bit weighted-current flip-flop is reset. As a result the 128-bit weighted-current flip-flop furnished a binary zero output, negates the reference voltage to the summing network, and switches signal ground to the 128-bit resistor. The second input signal approximation is initiated by code sequential pulse number one from the timing generator. In this approximation, a quarter-scale current is used in the summation with the resultant of that for the 128-bit decision.

However, an identical operation is performed for this approximation and subsequent bits. This process continues until a complete 8-bit PCM word appears in the weighted-current flip-flops. The PCM word is subsequently gated to the output register by the digital multiplexer gates.

Coder IFTS Circuits

The coder IFTS circuits check the operation of the coder based upon an IFTS command from the programmer. For this operation, the coder IFTS circuits gate a precision voltage (+4.331) from the calibrator to the sample and hold circuit. This voltage is subsequently coded and appears in the weight flip-flop as 11011101 if the coder and sample and hold is operating correctly. The five most significant bits (11011) are made available to a comparator in the IFTS circuits, bit 3 of 5 is inverted to make five bits binary one's. If the proper code is not present during the interval of the IFTS check command, an error indication is stored and a NO-GO output is routed to other spacecraft equipment. In addition to performing the above functions, the coder generates a comparator output signal which is routed to the high-speed gates and low-level amplifier IFTS circuits. This signal informs those circuits that the binary output is other than the fixed pattern.

DIGITAL MULTIPLEXER The Digital Multiplexer performs the gating of digital inputs from:

1. The coder
2. The sync and format ID selector
3. The programmer
4. Other spacecraft equipment based upon commands from the programmer

The multiplexer gates receive eighty-bit binary words from the coder. Four programmed sync words (three 8-bit words and a fourth containing two bits of sync) are received from the sync and format ID selector. Normal and reduced bit ID words are also received from the sync and format ID selector. From the programmer, the digital multiplexer gates receive six bits of frame ID (frame number) and eight bits of the IFTS word. The logic diagram for the digital multiplexer gates is shown in figure 8-10. The digital multiplexer gates also receive many digital inputs from other spacecraft equipment. They receive twenty-six 8-bit words, two 16-bit words, one 24-bit word and one 32-bit word. Each of the above inputs is gated to the output register on a time-share basis in the form of 8-bit words. When an input word consists of more than eight bits, the eight most significant bits are gated to the output register first, followed by the eight next most significant bits. In addition to multiplexing these inputs, the digital multiplexer gates also perform self-checks on the gating structures. In the event of a malfunction, it furnishes a NO-GO indication to other spacecraft equipment.

The digital multiplexer gates IFTS circuits compare the inputs and the outputs of the gate drivers to determine whether a malfunction exists. This is accomplished using OR gates, a comparator circuit, and an error flip-flop. The OR gates furnish the inputs and outputs of all gate drivers to the comparator circuit. The comparator circuit consists of two 2-input inhibit AND gates and a 2-input OR gate. As long as there is no malfunction in any of the gate drivers, the comparator circuit furnishes a binary zero output to the error flip-flop. Multiplexing of the word input is controlled by inputs

DIGITAL MULTIPLEXER GATES

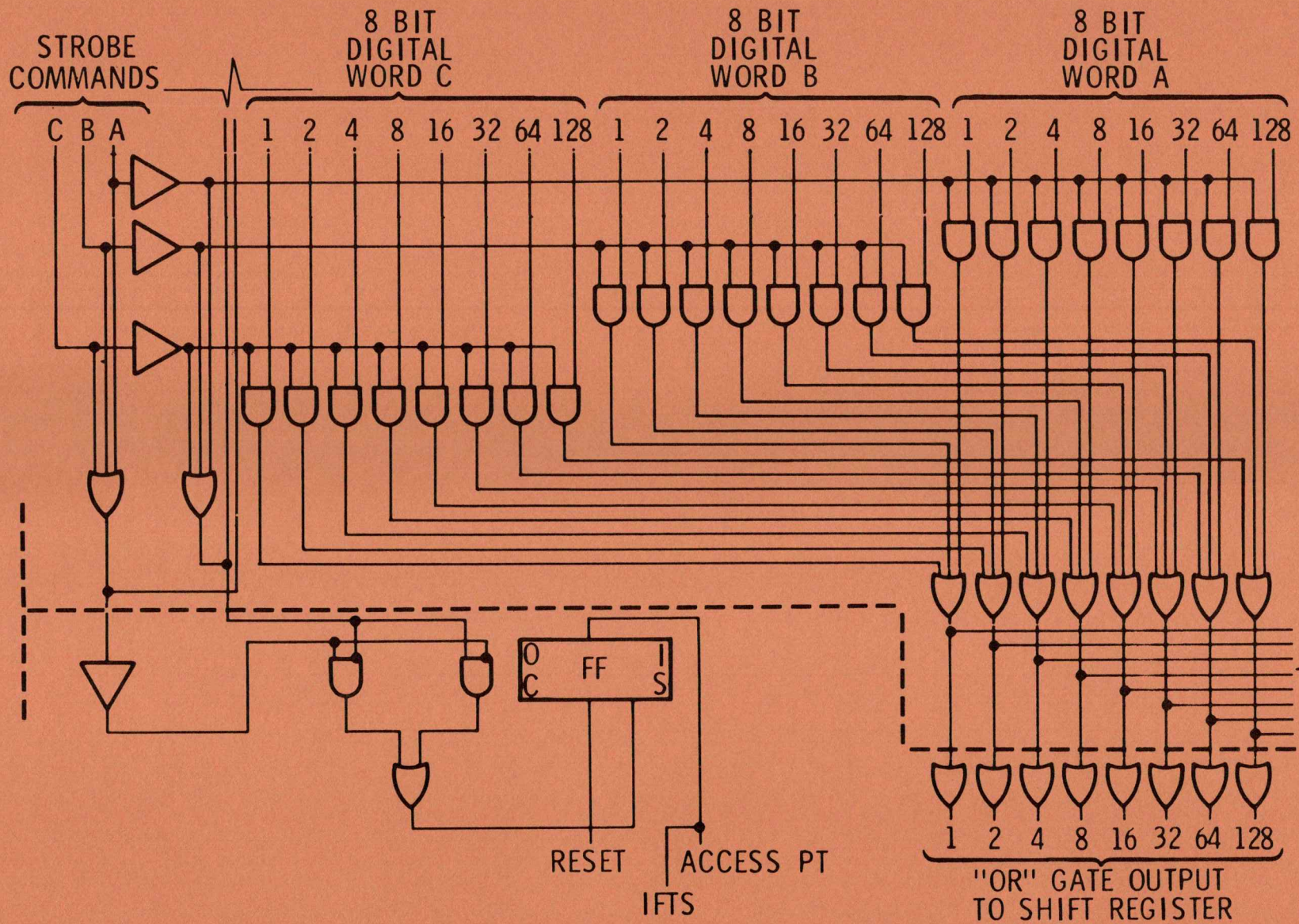


figure 8-10

CD-1006

from the programmer. When a word is to be gated to the output register, the 8-bit AND structure is strobed by a word command from the programmer and the input word configuration is passed to the output register through the OR gates. This is accomplished without inversion as discussed below.

SYNC AND FORMAT ID SELECTOR The sync and format ID selector provides the capabilities for generating the various sync word patterns inserted into the PCM pulse train at the digital multiplexer gate. Frame synchronization is inserted in the first 32 bits (4 words) of each prime frame. A diagram of the 32 bit frame synchronization break down appears in Figure 8-11. The first 5 bits and bits 21 through 26 in the sync pattern are selectable to any combination of binary ONE's and ZERO's by patch board logic. Circuits are also included to cause the 15-bit core (bits 6 through 20) to be complementary on alternate prime frames. Bits 27 through 32 are used to provide a binary count indicating the prime frame number.

OUTPUT REGISTER The output register receives 8 parallel bit PCM words from the digital multiplexer gates and converts this data into a serial nrz PCM output. It also receives a 40-bit serial binary input (channel 5IDS) from other spacecraft equipment and integrates it into the nrz PCM output. The nrz PCM output is furnished to the Pre-Modulation Processor and the GSE. The output register also generates two bit rate outputs, two subcarrier outputs, a prime frame sync. (50 pps.), and a subframe sync (1 cps). The output register checks itself for malfunction using its IFTS circuits. In the event of a malfunction, it furnishes a NO-GO indication to a remote error indicator. A diagram of the output register is shown in figure 8-12.

The output register logic consists of an 8-stage shift register, a shift pulse driver, an nrz output flip-flop, two data output drivers, timing output drivers, and IFTS circuits. Eight bit words are parallel-loaded into the shift register from the digital multiplexer gate. This is accomplished by a word command to the digital multiplexer gates from the programmer. The word command is active during the last period of each word time that an analog or parallel digital input is sampled. Each binary one sets a stage of the shift register. Each stage of the shift register is a saturable core flip-flop which uses an input driver and a negative pulse steering diode. During the next word time, the word is shifted out at the selected bit rate with the most significant bit shifted out first. This is accomplished by shift pulses developed by the shift pulse driver from a bit rate input furnished by the programmer. The final stage of the shift register drives the nrz output flip-flop. The nrz output flip-flop reverses operating states whenever a change occurs in the input binary level (i.e., from a zero to a one or a one to a zero). Two identical nrz output is furnished to the Pre-Modulation Processor and the GSE by two data output drivers, each having an output impedance of 100 ohms.

A 40-bit serial return-to-zero (rz) word (Channel 5IDS) is transferred from the computer by start, stop, and bit transfer pulses furnished by the data transfer drivers. Each bit of the word is combined with the word command from the programmer and furnished as an input to the final stage of the shift register. Each bit is entered into this stage and shifted out to the nrz output flip-flop by a shift pulse from the shift pulse driver. Channel 5IDS inputs are inserted in word slots 33 through 37 of each prime frame, or 50 times per second, during normal bit rate

PCM FRAME SYNCHRONIZATION

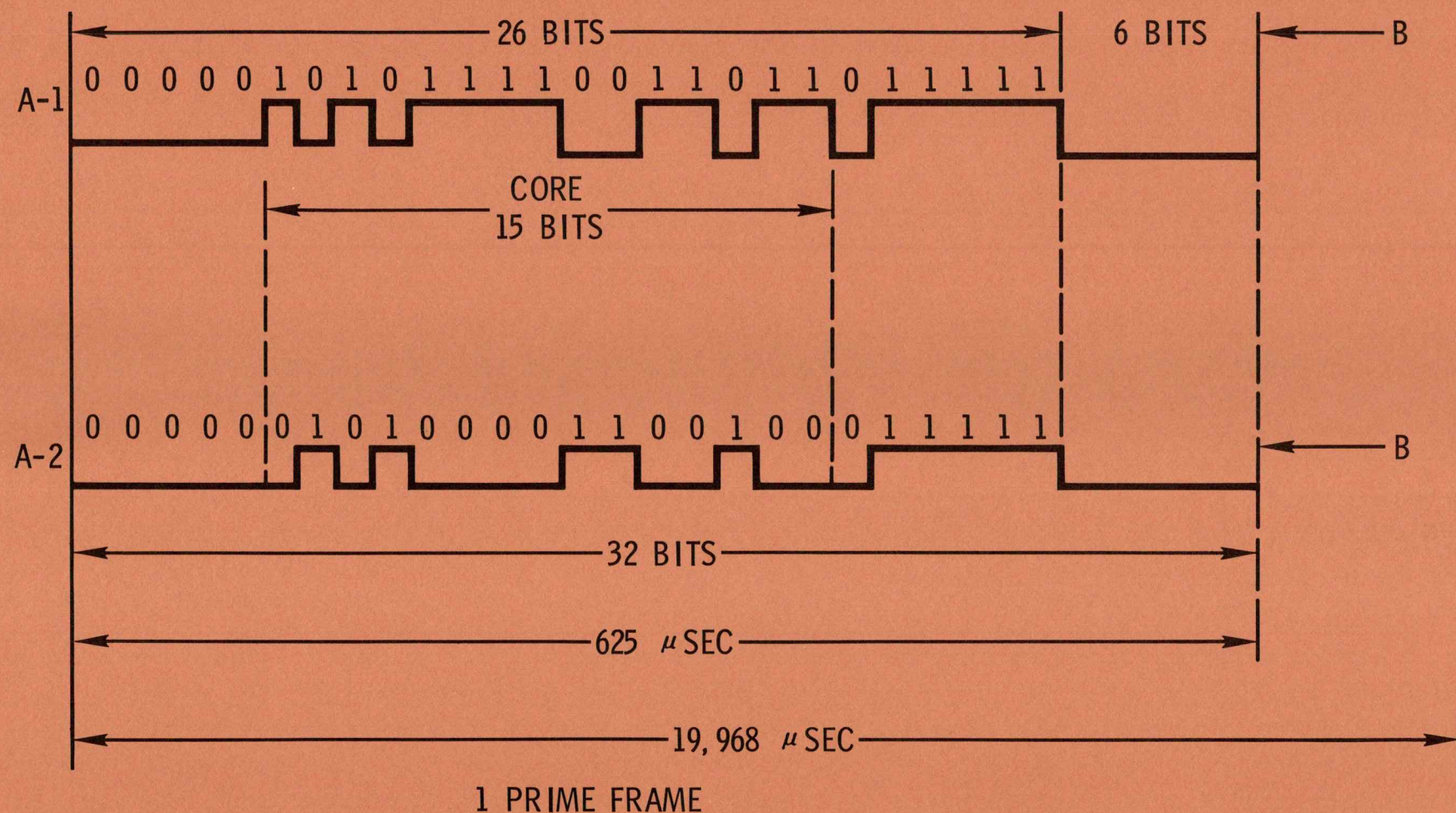
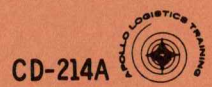


figure 8-11

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8-32

OUTPUT REGISTER IFTS

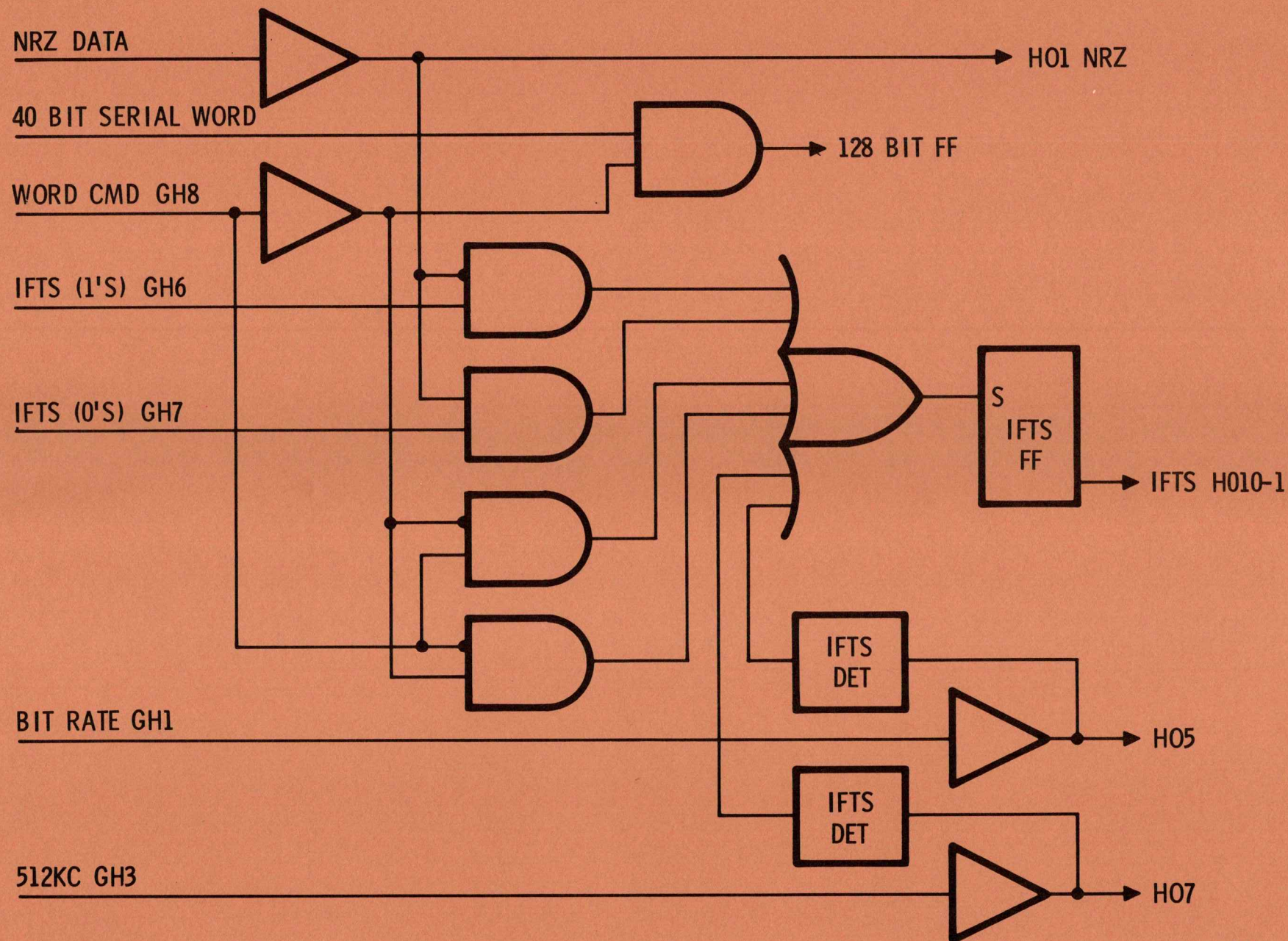


figure 8-12a

mode operation. When operating in the reduced rate mode, it is sampled only 10 times per second.

Output drivers are used for the bit rate outputs, each having 100 ohms output impedance. The subcarrier outputs, the prime frame sync (50 cps) and the subframe sync (1 cps); each come from a driver having an output impedance of 100 ohms. Each timing signal output driver provides non-inverting, push-pull outputs whose levels are closely regulated.

The IFTS circuits use the same principle for self checks as do other areas of the PCM Telemetry Equipment (i.e., outputs are compared against inputs). Four basic checks are made. They are:

1. a check of the 40-bit serial word AND gate
2. a check of IFTS words in specific word slots
3. a check for the absence of a bit rate output
4. a check for the absence of a subcarrier output

If a malfunction is detected, an error output is stored in the error flip-flop and a NO-GO signal is routed to the IFTS system.

A check of the 40-bit serial word AND gate is performed by combining the inverse of the word command from the programmer with the output of the 40-bit serial word AND gating structure in the computer. The output of 40-bit serial word AND gate is the inverse of the word command input; thus, the IFTS check gate generates an error output when:

1. the 40-bit serial word AND gate produces an output with a word command input zero (gating structure appears as an open)

2. if the 40-bit serial word AND gate produces an output with a word command input one (gating structure appears as a short)

The output of these IFTS check gates are fed to the OR gate, along with the results of the other IFTS checks. Thus, if either of the above malfunctions exist, a NO-GO output is generated by the error flip-flop which is set by the OR gate output.

Checks are performed on the IFTS word inserted in the normal data by the digital multiplexer gates. This is accomplished by monitoring the output of the nrz output flip-flop during specific word times allotted for IFTS checks. When using the normal bit rate mode, IFTS checks are performed during word 100 of the 2nd through 50th prime frame. During the even numbered frames, the IFTS circuits check for all binary one's in word 100. During the odd numbered frames, with the exception of frame 1, the IFTS circuits check all binary zero's in word slot 100. When the reduced bit rate mode is used, an all one's check is performed during word 64 and an all zero's check is performed during word 164. If all one's and all zero's are not found in these respective words or those for normal bit rate operation, a one out of the AND gate sets the error flip-flop and a NO-GO signal is generated. Since the IFTS word is inserted at the input of the output register, this NO-GO indicates a malfunction of the output register.

Two IFTS checks are made on timing outputs from the output register; one for bit rate output, and the second for subcarrier output. Each of these checks is performed by IFTS circuits which furnish outputs whenever the timing output drivers fail to provide outputs. An error output is furnished to the error flip-flop if a subcarrier output failure

exists for one cycle or more. An error output is also furnished to the error flip-flop if the bit rate output fails for 700 microseconds or more. As in the other checks, the detection of a malfunction sets the error flip-flop and a NO-GO output is furnished to the IFTS System. An external reset is required to clear the error flip-flop.

DATA TRANSFER BUFFERS The data transfer drivers, as seen in the block diagram, figure 8-1 and 8-13, generate the timing and transfer pulses required to synchronize other spacecraft equipment with the PCM Telemetry Equipment. These pulses are generated by command from the programmer. The pulse outputs include start, sync, and stop pulse for controlling the 40-bit serial data channel (designated 5LDS). Pulses are also generated for the parallel transfer of 12 digital channel inputs (designated channels 1LD3 through 1LD14). In addition to generating the above outputs, the data transfer drivers perform self checks to detect malfunctions. In the event of a malfunction, a NO-GO output is routed to the IFTS system.

The IFTS circuits associated with the data transfer drivers check the operation of each output driver for malfunction. This is accomplished by comparing the command inputs from the programmer with the outputs of the driver stages. If any error is detected, an error flip-flop furnishes a NO-GO output (binary zero) until reset by a reset command.

POWER SUPPLY The power supply produces the dc supply voltages required by the PCM Telemetry Equipment from a 115-volt, 3 phase, 4 wire, 400cps spacecraft input. It is comprised of a power transformer with a multi-tapped secondary, solid-state full-wave rectifier, choke input filter, a +6 volt regulator

and IFTS circuits. The following voltages are furnished by the power supply:

- (a) + 20 volts
- (b) + 15 volts
- (c) + 10 volts
- (d) + 3 volts
- (e) + 6 volts, regulated
- (f) + 6 volts, unregulated

The PCM Telemetry System is summarized in the detailed block diagram in figure 8-13. Many points brought up in this section are illustrated here with an overall system view.

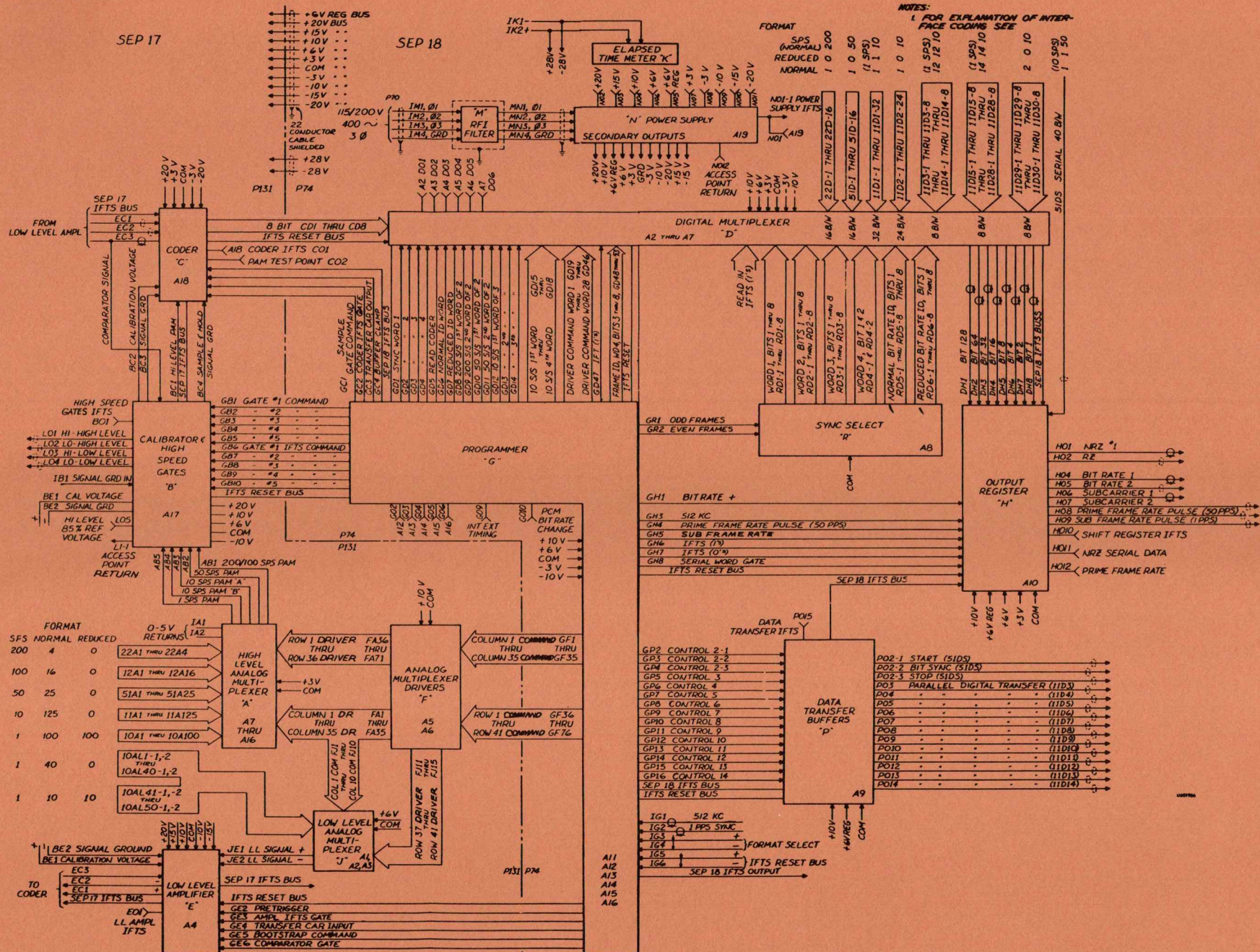


Figure 1. Block Diagram, PCM Telemetry Equipment

figure 8-13

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SECTION IX

DATA STORAGE EQUIPMENT

INTRODUCTION

The primary purpose of the Data Storage Equipment (DSE) is to record and playback data in parallel on nine direct analog and five digital channels. The Data Storage Equipment will operate with telemetry equipment and analog sources to record and playback 14 channels of data on one inch magnetic tape. At the normal speed the total recording time for one reel of tape is 30 minutes. Serial to parallel conversion circuitry will enable serial digital information to be recorded in parallel on four of the digital channels; the fifth channel will accept the clock signal. During playback, the parallel information will be converted back to serial format and released. The analog frequency response will be 50 cps - 10 kc at the normal tape speed. Conventional solid state electronics for all signal conditioning, power regulation and control is employed in the DSE; relay switching is used for control functions.

There is also a lower tape speed which will allow up to two hours of recording time, but at a reduced bit rate capability. The analog frequency response at the reduced bit rate is 12.5 cps to 2.5 kc.

MECHANICAL SYSTEM. The recording speed of 15 inches per second (ips) is used to insure sufficient pulse wave length for reliable readout. During long periods when no communication with earth is possible, information will be recorded at 3.75 ips. To provide this capability, 2250 feet of one inch mylar magnetic tape is used. To provide optimum reeling and tension control throughout all operating modes, separate reel and capstan drive systems are used. Two 400 cycle ac motors are used in the transport for reel and capstan

drive. In this system, tape tension is maintained throughout the reeling operation by a hysteresis clutch and a differential. Each reel is coupled to an outer leg of the differential. The output from the clutch is connected to the center leg of the differential, torquing the reels in opposite directions. This reversing action maintains a constant torque and, therefore, a constant tape tension throughout reeling.

The hysteresis clutch is magnetic device, with no sliding surfaces or physically contacting members except for the anti-friction bearings. The duel capstan drive method is utilized in the DSE. In this design, precision, endless mylar bets are used to drive the capstan pulleys. The tape wraps around 170° on each capstan to obtain driving friction and permit precise tape tracking.

The use of an electro-magnetic clutch in the capstan drive system permits the capstans to be accelerated to a stable speed in one second during the record mode, and provides a tape speed of 120 ips for fast forward and reverse operations. At this speed, the 2250 feet of tape will run approximately 3.75 minutes. Table 9-1 gives the run times for all recorder speeds.

CONTROL FUNCTIONS. Switches are provided on control panel 20 for the control of the DSE. A three position switch is provided for commanding record, reproduce or standby operation. When this switch is in standby, tape motion is stopped and power is removed from the electronics. When the switch is placed in either record or reproduce, tape motion is achieved in the direction and at a speed that is controlled by the position of the switches. Starting time is three seconds. The DSE is a bi-directional machine. It will record

TABLE 9-1

DATA STORAGE EQUIPMENT MODES OF OPERATION

Parameter	Digital Channels		Analog Channels	
Input Data Rate	51.2K Bit/Sec	1.6K Bit/Sec	50-10,000 cps	12.5-2500 cps
Record Speed	15 IPS	3.75 IPS	15 IPS	3.75 IPS
Playback Speed	15 IPS	120 IPS	15 IPS	15 IPS
Output Data Rate	51.2K Bit/Sec	51.2K Bit/Sec	50-10,000 cps	50-10,000 cps
Total Record Time	30 Minutes	2 Hours	30 Minutes	2 Hours
Total Playback Time	30 Minutes	3 3/4 Minutes	30 Minutes	30 Minutes

and playback data in both directions. The command switches located on the control panel number 20 are:

1. "SPEED" switch
HIGH (120 ips)
NORMAL (15 ips)
LOW (3.75 ips)
2. "TAPE RECORDER" switch
 - a. RECORD
 - b. OFF
 - c. PLAY
3. "DIRECTION" switch
 - a. FWD (in all speeds)
 - b. OFF
 - c. REV (in all speeds)

The speed switches will be utilized to select the speed at which the tape is to be driven by the tape drive mechanism.

FUNCTIONAL DESCRIPTION

The electronic specifications of the DSE are listed in table 9-2, and the system physical specifications are listed in table 9-3. A block diagram of the Data Storage Equipment appears in figure 9-1. From this diagram, the principle of operation of the DSE system will be discussed. The DSE operates from two power sources: 115 volts ac, three phase, 400 cycle, and +28 volts dc. The 28 volts dc source is used to perform operations such as energizing relays and pulse circuitry to accommodate particular commands. The 400 cycle source is used to operate drive motors and to supply power to operate the electronics.

DIGITAL PROCESSING. The digital data is coupled to the digital converter where it is converted from serial non-return to zero (nrz) information to parallel information. This serial data is divided into four separate and equal increments and coupled to the digital record

amplifiers. These amplifiers supply proper drive current to four separate digital record tracks on the recording head. At the same time, the rz clock signal enters the digital converter where it is conditioned, divided by four, and coupled through the fifth digital record amplifier and recorded on a separate track of the record head. The digital information continues to be divided and recorded on four separate record tracks while the clock signal is recorded on a separate track. Synchronization of the nrz data, as recorded, and the rz clock signal is maintained throughout the recording mode.

Digital Outputs

The recorded digital information from the five digital reproduce tracks is coupled to the input of the digital reproduce amplifiers. These amplifiers will provide the amplification necessary to operate the digital converter. Their outputs are coupled to the digital converter where the four parallel data channels are converted to serial information. At the same time, the reproduced clock signal from the fifth track is multiplied back to the original recorded clock bit rate. After the parallel-to-serial conversion and the proper clock synchronization is accomplished, the serial nrz data is fed out of the DSE.

ANALOG PROCESSING. Analog information is coupled from the patch panel to the desired channel to be recorded, and to one or a combination of record amplifiers. These amplifiers present the proper input impedance and provide the signal conditioning to drive a record head. The record amplifiers accept a bias signal of 100 kc from the bias oscillator. This bias signal is amplified and mixed with the analog data signal to be recorded. The combined signal is then coupled to the analog tracks.

Voice Signals

The voice signal is fed into the DSE through the audio transformer where the proper impedance matching

TABLE 9-2
ELECTRONICS SPECIFICATIONS

Item	Module	Name	Specification
1	Analog Record Amplifier	Input Level	0-5 Volts peak-to-peak
		Input Frequency	50 cps to 10,000 cps
		Input Impedance	100,000 ohms, minimum
2	Analog Reproduce Amplifier	Output Level	Within 2 db of Input level
		Freq. Response	50 cps-10,000 cps + 2 db
		Output Impedance	600 ohms + 10%
		Harmonic Distortion	Two percent maximum
		Signal-to-Noise Ratio	40 db, minimum referenced to a 1 kc, 5 volts peak-to-peak output
3	Digital Record Electronics	Serial Input Level	0 V dc + .5 vdc-0 vdc for binary zero
			6 v dc + .5 vdc for binary one
		Input Impedance	100,000 ohms, minimum
		Serial Input Bit Rate	51,200 bits per second
		Input Bit Rate to Record Amplifier	12,800 bits per second
4	Digital Reproduce Electronics	Serial Output Level	0 vdc + 0.5 vdc - 0 vdc for binary zero
			6 vdc + .5 vdc for binary one

TABLE 9-2 (continued)

ELECTRONICS SPECIFICATION

Item	Module	Name	Specification
4 (cont.)	Digital Reproduce Electronics	Output Impedance	
		Output Pulse Rise Time	2 Microseconds, maximum
		Error Rate	Less than 1 bit in 10^5
5	Bia's Oscillator	Output Level	2.5 volts rms, minimum
		Output Impedance	500 ohms, maximum
		Frequency	100 kc
		Frequency Stability	$\pm .5\%$ over temperature range
6	Power Supply	Input	115 volts, 400 cps, 3 phase
		Output	Regulated voltage to supply all electronics

TABLE 9-3

SYSTEM PHYSICAL SPECIFICATIONS

Item	Description	Specification
1	Size	20" x 9½" x 5 3/8" maximum
2	Recorder and four reels of tape	24.6 pounds, maximum
3	Mounting	20" x 9½" surface
4	Power	25 watts nominal; 70 watts for not more than three seconds

SYSTEM BLOCK DIAGRAM D.S.E.

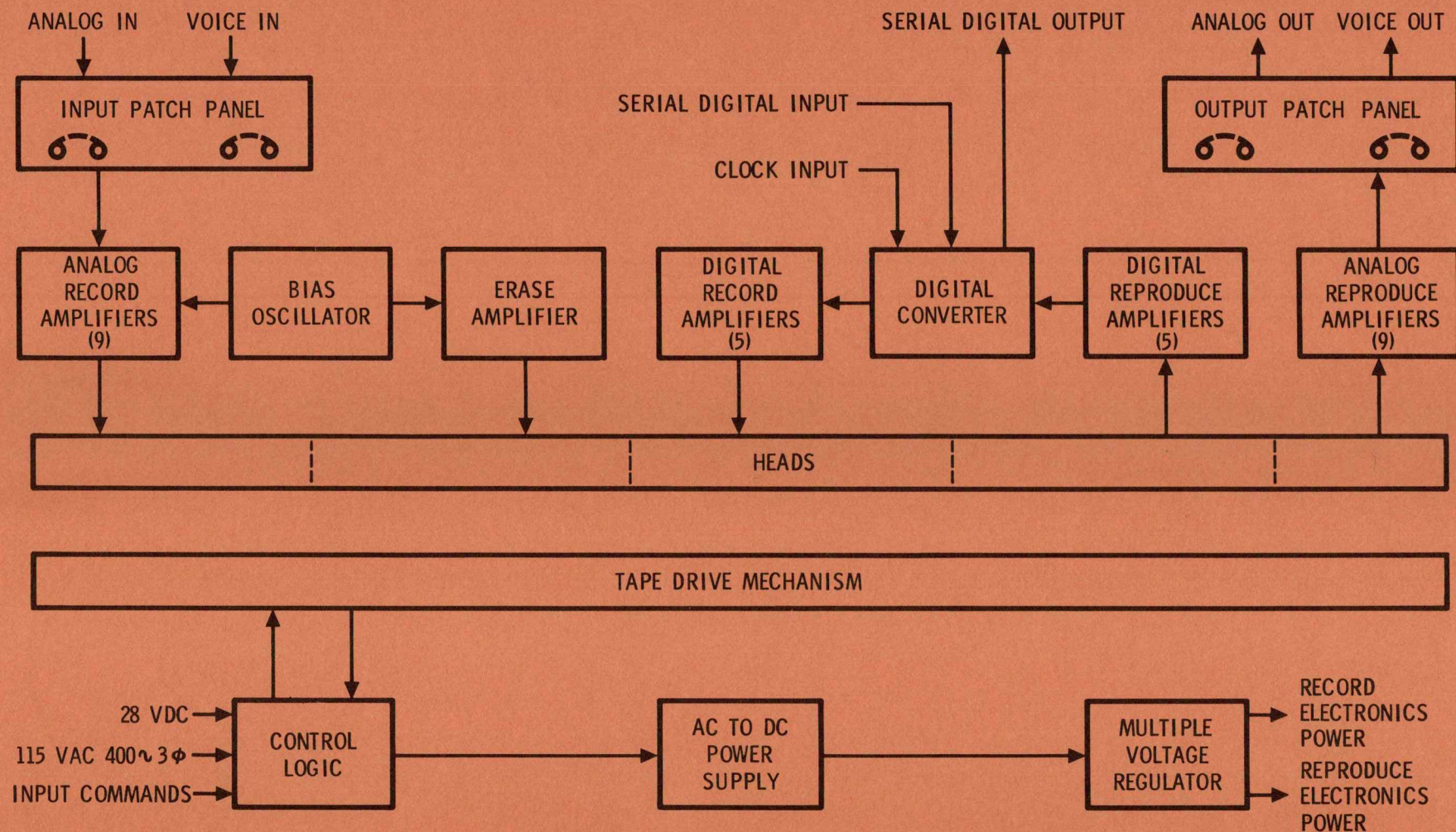



figure 9-1

CD-184  LOGISTICS TRAINING

is made, and coupled to the input patch panel. From the input patch panel, the voice signal may be connected to any one of the nine analog record amplifiers where it will be combined with the 100 kc bias. This 100 kc bias, having been properly conditioned through the record amplifier, will record linearly on the analog record track. The bias frequency is mixed with the data signal to prevent non-linearity and distortion of the recorded data.

Analog Reproduce

The erase amplifier is disabled in the reproduce mode by virtue of the bias oscillator being de-energized. In the reproduce mode, "TAPE RECORDER" switch in the PLAY position, the previously recorded signal on the tape will be coupled from the reproduce heads to the analog reproduce amplifiers. For the reproduce amplifiers, each of the nine analog tracks will be coupled to the respective analog amplifier where the signal is amplified and conditioned, (with proper output impedance) to deliver the reproduced signal to the output patch panel. The signals then become outputs of the DSE. From the output patch panel, the operator may couple a previously recorded voice signal to the audio transformer.

CORE LOGIC MODULE. To adequately understand the DSE logic operations, a brief discussion of the core logic module (clm) is in order. The clm is a basic logic element which is versatile in its application. In the serial shift register, its basic function is to receive a binary "1" bit, store the bit, and upon command of the shift pulse, discharge a single binary bit. There are four clm's used as serial shift registers; three, as "1" generators; two, as binary dividers; and one, as a re-clock gate. The serial shift register is bi-directional, which means that the series of four clm's can shift binary bits from right to left or from left to right, as required.

Logic Core

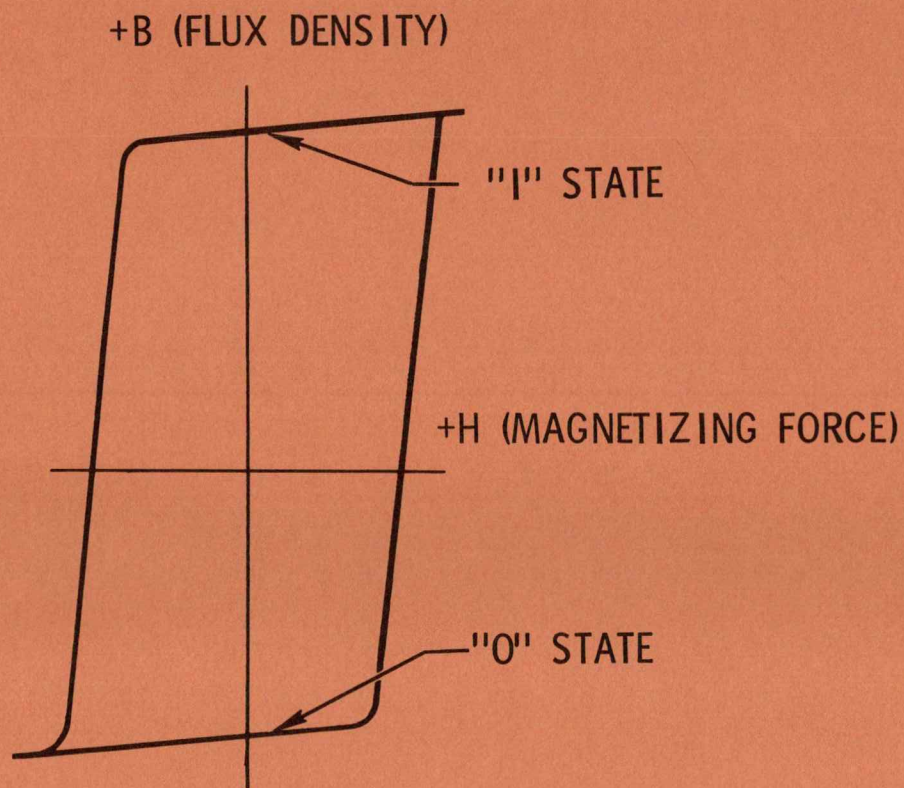
The basic logic element, a non-linear magnetic core, is the storage device used in the CLM. Its characteristic curve and a typical logic core are shown in figure 9-2. A core, cleared by the shift winding, will be magnetized with a flux density and polarity corresponding to the "0" state. A shift pulse applied to the core will always drive it to the "0" state which is a -B flux level. If the core is in the "0" state, a shift pulse will have no effect since the core is already magnetically saturated in this direction. However, if a "1" input pulse is delivered, the core will saturate in the opposite direction corresponding to the "1" state of the hysteresis curve. Upon receipt of a shift pulse, the core is transferred back to the "0" state, but in the process of doing so, the change of flux will induce a voltage in the output winding. Thus, the core stores information that an input signal has or has not been impressed upon it since the last shift pulse and reads out this information when interrogated by a shift pulse.

The simplified presentation is used here only to convey a basic understanding of the core logic module. The clm actually has two other windings; one serves as an additional input or as an inhibit winding; the other is necessary for regeneration. The clm also contains a current driver transistor and a network which delays the output.

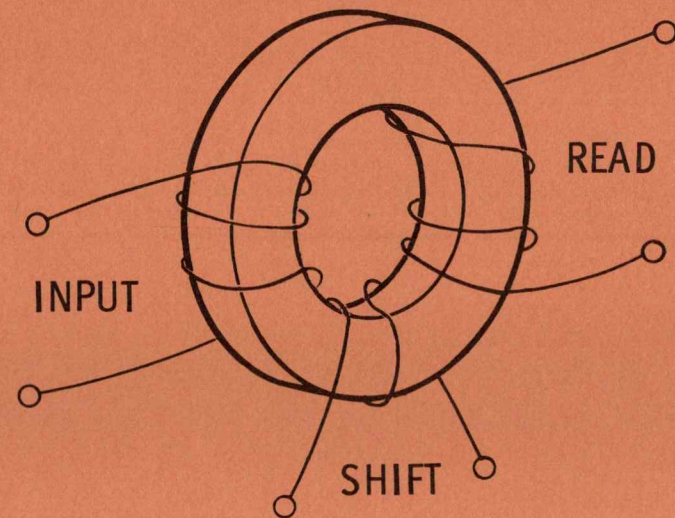
SYSTEM CONTROL LOGIC. Upon the initiation of an off command, a signal is coupled to the system control logic and routed to the appropriate relays to remove all power from the tape drive mechanism (reel and capstan drive motors) and the electronics. With the application of the standby command, all power is removed from the voltage regulator and the record and reproduce electronics.

Upon reaching the end of the tape in any pre-selected direction and mode, a command function is initiated by the end-of-tape logic to perform the same

CORE LOGIC




CORE CHARACTERISTIC

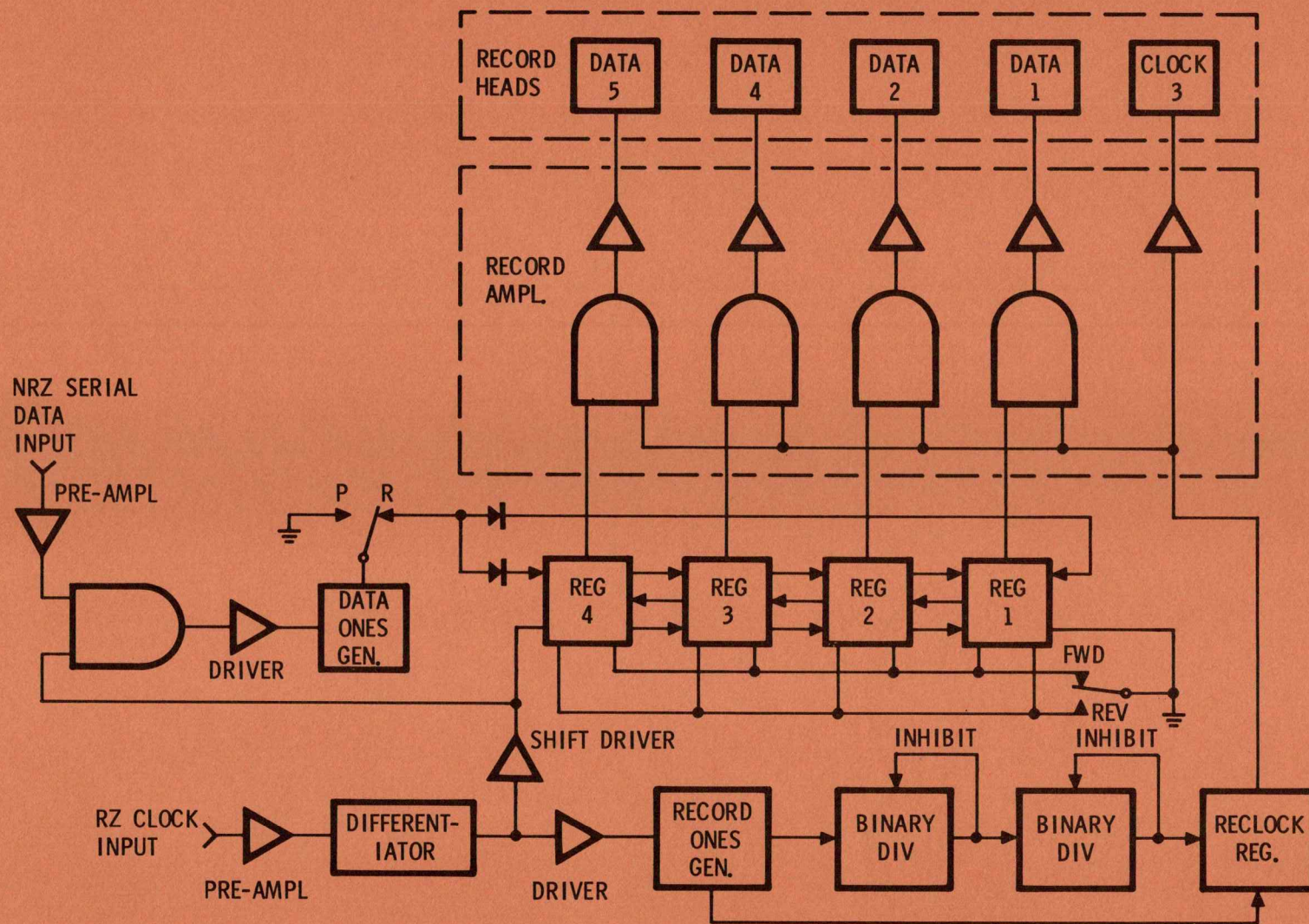


TYPICAL BASIC LOGIC CORE ELEMENT

figure 9-2

CD-186 

DIGITAL CONVERTER, DSE



CD-206A



figure 9-3

REPRODUCECONVERTER, DSE

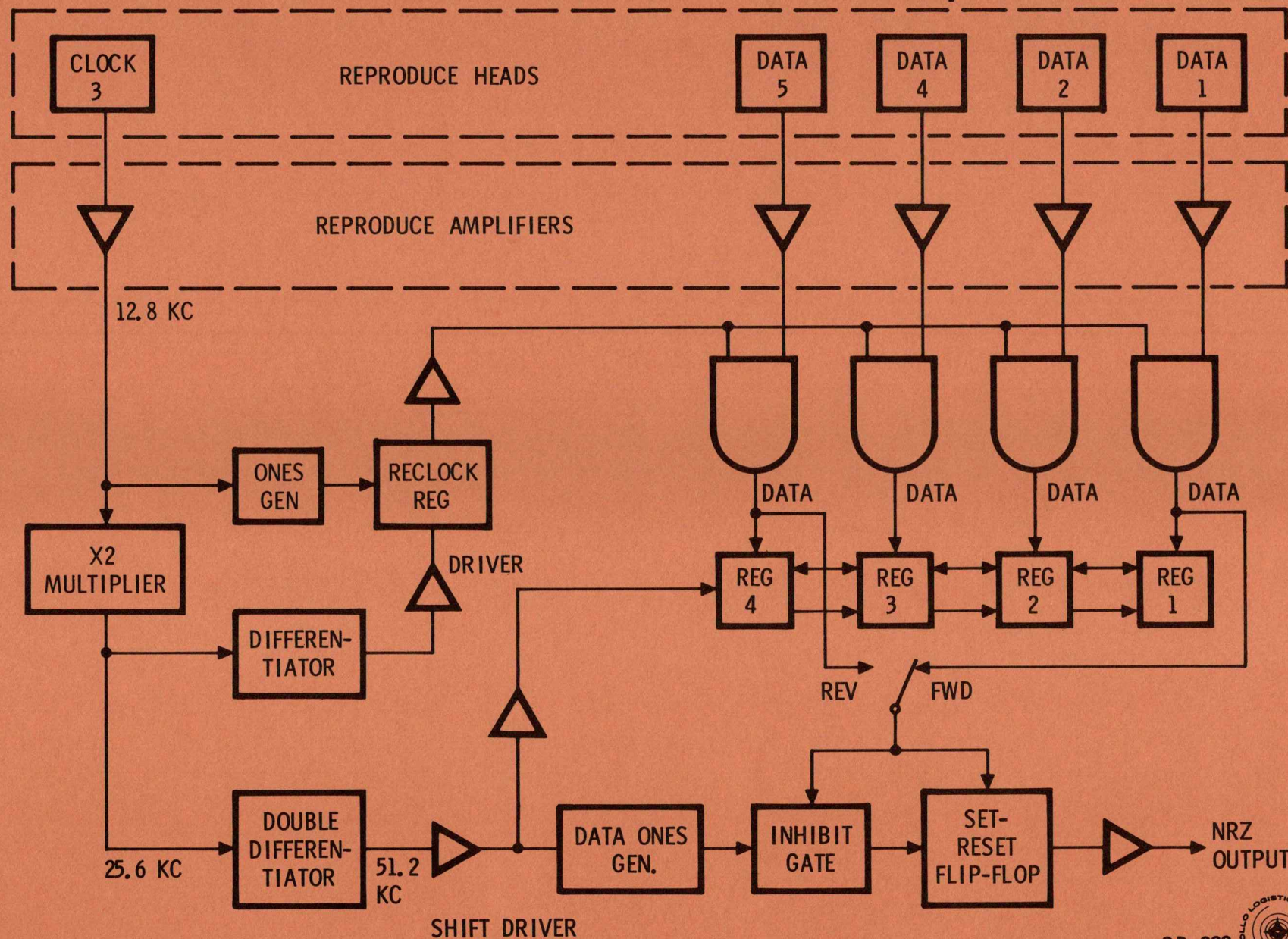


figure 9-3a

function as an off command; all power will be removed from the record or reproduce electronics, and the capstan and reel drive motors.

To perform a rewind function in the fast mode (120 ips) the proper direction switching (forward or reverse) will be selected. After the fast speed position has been selected a record or playback command must be applied to obtain the fast rewind condition of the tape. It should be noted that in the fast forward or reverse mode, all electronics are disabled for the duration of the rewind function.

FUNCTIONAL DATA FLOW

The functional data flow of the digital electronics of the DSE will be explained initially, followed by a discussion on the analog electronics and an analysis of the system control logic.

DIGITAL ELECTRONICS. The serial digital data is presented to the DSE from the PCM Telemetry Equipment. Block diagrams of the digital record and reproduce converter are shown in figure 9-3. The input is in serial form and at a rate of 51,200 or 1600 bits per second. To record serially would be impractical with these high input frequencies and available tape speeds, as the data packing density would exceed the state of the art of magnetic recording. To eliminate these problems and increase reliability, the serial train is divided into four parallel bits, each bit being four times its original length, one to each of four core logic modules (clm). This is accomplished by allowing the first bit from the serial train to set the first CIM. After the bit has been registered, it is shifted to the second clm by a shift pulse. Simultaneously, the first clm is cleared and the second serial bit is inserted into it. This process continues until four bits have progressed into the serial register, one bit to each clm. At this time, a pulse, which occurs at a quarter of the bit rate, is applied to WRITE gates, causing all four bits to be recorded on the tape

simultaneously. The cycle continues by having the second group of four bits registered and recorded.

The object of these processes is to take the 51,200 or 1600 bits per second data and break it up into groups of four, which are then recorded on four separate tape channels at a quarter of the rate of incoming data. This allows the individual tape tracks to record at a quarter of the data packing density allowing greater spacing between bits and increasing the data handling capability.

The playback or reproduce cycle reverses this process. The four bits are simultaneously read from the tape and registered in the four clm's. The shift pulses cause these bits to progressively move through the register, causing the bits to be presented one at a time at one end of the serial register.

Synchronization

The synchronizing or timing of events in digital systems is accomplished through the use of a continuous pulse train called the clock signal. The clock signal cycle rate is the same as the data rate of 51,200 bits per second and it is recorded on a fifth digital channel, after being divided down to a quarter of its incoming rate.

Most of the clock signals throughout the system will either be a full clock or quarter clock rate. Clock frequency in the record mode is dependent upon tape speed. The serial shift register clm's are all shifted simultaneously at a full clock rate. The digital read and write gates are turned on by a pulse train that is a quarter clock rate. The playback (divided-by-four) signal, in addition to triggering read gates, is multiplied-by-four and accompanies outgoing data as a clock train, and is used as shift pulses, which are necessary to cause a side progression of data through the register, are also provided by this multiplied-by-four signal.

Skew Correction

The READ gate in the converter and the WRITE gates in the digital record amplifiers are primarily for the purpose of skew and differential flutter correction. Skewing of the tape, that is, tape that is not traveling exactly perpendicular to the axis of the reproduce head alignment, will cause data that should be precisely parallel to be played back at slightly different times. This misalignment (Figure 9-4) also occurs during the record mode. By taking a one microsecond sample in the nominal center of the parallel data, it becomes possible to realign the timing of the four data channels so that they occur coincidentally. This allows the data to be further processed accurately.

DIGITAL CONVERTER RECORD MODE. In the diagram of the digital converter module shown in Figure 9-3, two inputs are shown; serial data in, and serial clock in. Serial nrz data is coupled through conventional transistor amplifiers and an AND gate. The second input to the gate is the clock-triggered shift pulse, which insures that data is recorded with precise timing and that no transient responses are recorded. When these two signals attain positive coincidence, and AND gate will bias the current driver amplifier into conduction. In turn, the current amplifier drives the shift winding of the ones generator. The ones generator has a dc voltage applied to its input winding which acts as a continuous "1" input. A logic "0" in on the shift winding will cause no output shift, whereas a logic "1" input will. There is a two microsecond delay circuit available in the output of each clm. Thus, after two microseconds the one generator will send in the first bit to be registered in clm (reg) number four. The next action in clm number 4 is the reception of the register shift pulse. Since the shift windings of all four registers are connected in parallel, they will be shifted simultaneously. At the reception of the shift pulse, the data is presented at the output of the clm, but at a time slightly following the

shift pulse. This delay allows for the clearing of the clm before it is permitted to register the data of the preceding module. This action is typical of all four clm's.

Each clm also has an undelayed output. When information is shifted out of a register clm it is fed, in parallel to the delayed and undelayed outputs. The undelayed outputs make up the four parallel outputs which are conducted to digital record, or write, amplifiers (W). This provides a true parallel output from what was previously serial data. Note the right to left progression of data through shift register, which would be effected by changing the "FORWARD-REVERSE" switch position, would enable the same operation as described here, but the parallel output would be presented in the reverse order.

The clocking circuits and signal flow, as they affect the record mode, will be explained later in this section.

DIGITAL CONVERTER REPRODUCE MODE. The parallel data, which is taken from the moving tape by the read heads (R), is shown in the lower section of Figure 9-3.

The parallel data is presented by digital reproduce amplifiers 1 through 5, to the register and switching converter module. The four parallel data inputs, received from the digital reproduce amplifiers, provide the inputs for the current driver AND gates. These gates are enabled by the reproduce sample pulse which is common to all four gates. This pulse occurs at the same rate as the recorded clock rate. The parallel data input lines feed clm registers.

The input pulses are applied to the delay networks within the clm's, and transferred to the clm output windings. The bits are registered in the next clm in sequence due to the shift pulse which occurs at the same time. The data presented to clm number one is not registered there, but in the following clm, number two.

SKEW CORRECTION

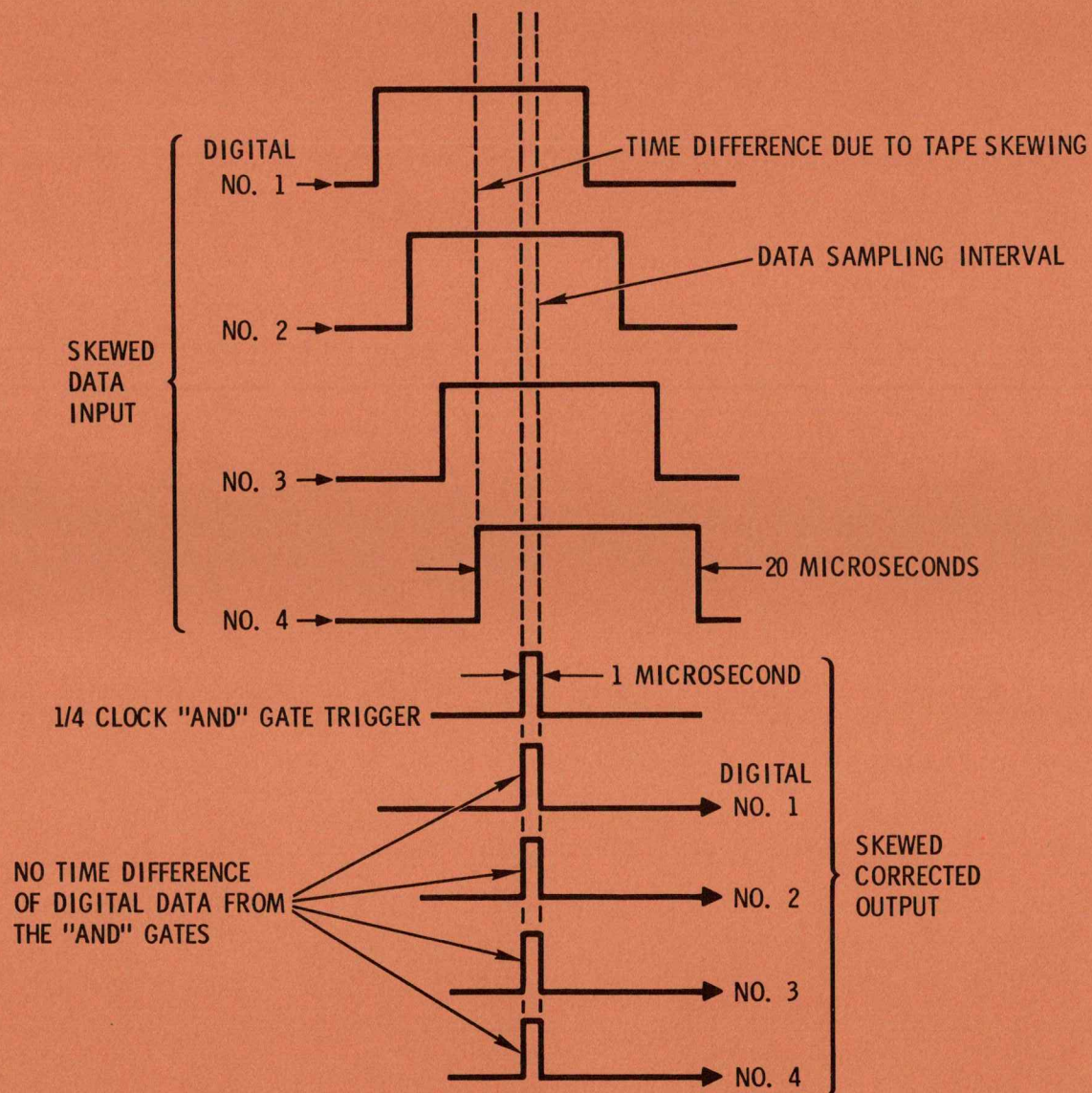


figure 9-4

This action is the same for the next two digital inputs to the clm's. The fourth clm, having no following clm, feeds directly into the serial line. The register shift trigger, occurring at four times the rate of the incoming signals and recorded clock, will present three more shift triggers to the clm's before the cycle repeats itself. These triggers will shift the bits to the left from clm to clm. This causes the remaining three bits to follow the first, in sequence, until all four bits have been presented at the output of the serial shift register. Immediately following this and at the next clock signal, a new set of four bits will be read and the cycle will be repeated. The action is the same regardless of the direction of progression except that the serial output is either presented at reg 4 or reg 1. The position of the TAPE RECORDER FWD-REV switch will determine the direction of playback, as well as the direction of register progression.

The serial train pulses are presented to two stages in this module. One stage is the amplifier, which provides the set pulse for the flip-flop circuit. The other stage is an exclusive OR gate. This circuit has two inputs, and its operation is such that it will provide an output if it receives either one of the inputs, but not both simultaneously. Receiving both inputs will have the effect of having no input at all. The other input, presents a continuous pulse train from the ones generator. Therefore, this circuit will have no output where a logic "1" is received from the register. In the event that the register does not present a "1", signifying the presence of a "0", the exclusive OR will provide a pulse output. The pulse, caused by the "0", is conducted to the flip-flop (f/f) resetting it. The on state of the f/f corresponds to a "1" pulse from the clm and the off state corresponds to a "0" pulse. The output of the flip-flop is then presented to the DSE interface equipment and is, essentially, nrz data.

CLOCK SIGNALS. The purpose of the clock signal will

be to provide a synchronized digital data flow. The clock signal provides internal gating of various digital amplifiers, turning them on only at times when data may be presented. This inhibits the circuits from responding to transient pulses which may be presented to the Data Storage Equipment.

Record Mode

The incoming clock signal provides a pulse coincident with each data bit that is received. (Like the data, it is being received at 51,200 or 1600 bits per second, and is reduced to one quarter of this rate before recording.) The clock signal provides the timing for the serial shift register as previously described. The reproduced clock signal is multiplied by four which is making it equal to the original clock frequency.

The serial clock signal is initially presented to the converter at the RECORD-PLAY switch. During the record mode the clock input is differentiated.

One destination of the clock signal is the AND gate depicted in Figure 9-3, upper left, and mentioned in the preceding discussion dealing with digital converter record mode. This output is the register shift pulse and the input AND gate pulse. The second destination for the clock is a differentiating network which feeds a current driver. The output of the current driver interfaces the four following clm's:

1. Ones generator (record)
2. Ones generator (reproduce)
3. Two binary divide
4. Reclock

During the record mode all of the above clm's are energized except the reproduce ones generator. The function of the binary divide clm's is to divide the clock train down to a quarter of the incoming clock signal. The binary divide clm through connection of inhibit and register windings, inhibits every other

clock pulse. This causes each divider clm to cut its input frequency in half. The overall effect will be an output from the second divider which is one fourth the rate of the input clock signal.

In the process of dividing the clock by four, considerable delay has been introduced in the one quarter clock train until it no longer coincides with the bit data presentation. To correct this, the second divider output is conducted into the re-clock gate clm and registered. The shift winding continues to be pulsed by the current driver via the ones generator. This causes the re-clock gate to shift out an undelayed output coincident with the incoming serial clock at one fourth its frequency.

The output of the clm re-clock gate has two destinations. At one of these destinations the signal drives the four parallel READ gates, and provides parallel data to the serial shift register during the reproduce mode (lower section Figure 9-3).

The second destination of the clm re-clock gate output is the WRITE gates of the four digital record amplifiers, and the clock record amplifiers where it is presented to a record head for registry on the data tape as nrz mark data (upper section Figure 9-3).

Reproduce Mode

The next operation to be considered will be the clock signal flow during the reproduce mode. Referring to Figure 9-3, the recorded clock is recovered from the tape as nrz mark data, processed in the clock reproduce amplifier, and presented to the converter. Here it drives a ringing circuit that is resonant at twice the reproduced clock rate. This clock train output is connected to a network of differentiators and diodes that provide full-wave rectification of the differentiated clock signal. This brings the rate to four times that of the reproduced clock. In this state, the clock signal frequency is the same

as it was during the record mode.

Clock Shift Pulse. In parallel with the double differentiation network is a second differentiation network which, through a current driver, provides the shift pulse for the clm re-clock gate at a quarter clock rate. This gate operates during both record and reproduce modes.

Clock Reproduce Set Pulse. The serial train of clock pulses received from the tape, after being differentiated in the reproduce clock buffer circuitry, is fed to a current driver. The output of the driver is the reproduce set pulse which drives the shift winding of the reproduce ones generator. The reproduce ones generator will produce a "1" pulse each time it is interrogated by the set pulse. This "1" will arrive at the re-clock gate after the shift pulse from the differentiation network. The re-clock gate will register the "1" which it received from the ones generator and produce an output upon receipt of the next shift pulse. During the record mode, the re-clock gate clm is operating at a quarter clock rate, and during the reproduce mode, the clm is operating at the full clock rate.

DIGITAL RECORD AMPLIFIER. The principal purpose of the circuitry shown in Figure 9-5 is to provide commutative selection of data from the serial shift register and condition it to a form suitable for tape recording. In the process of converting data from serial to parallel form in the serial shift register, it is necessary for a given digital record channel to recognize only every fourth bit of information as it is shifted from one register stage to the next. A unique situation exists in that each and every bit is presented to the record amplifier. The record amplifier is driven by an AND gate and a quarter clock train. The AND circuit will cause the trigger driver to conduct if, and only if, both the input data from the register and the quarter clock pulse occur coincidentally.

DIGITAL RECORD AMPLIFIER

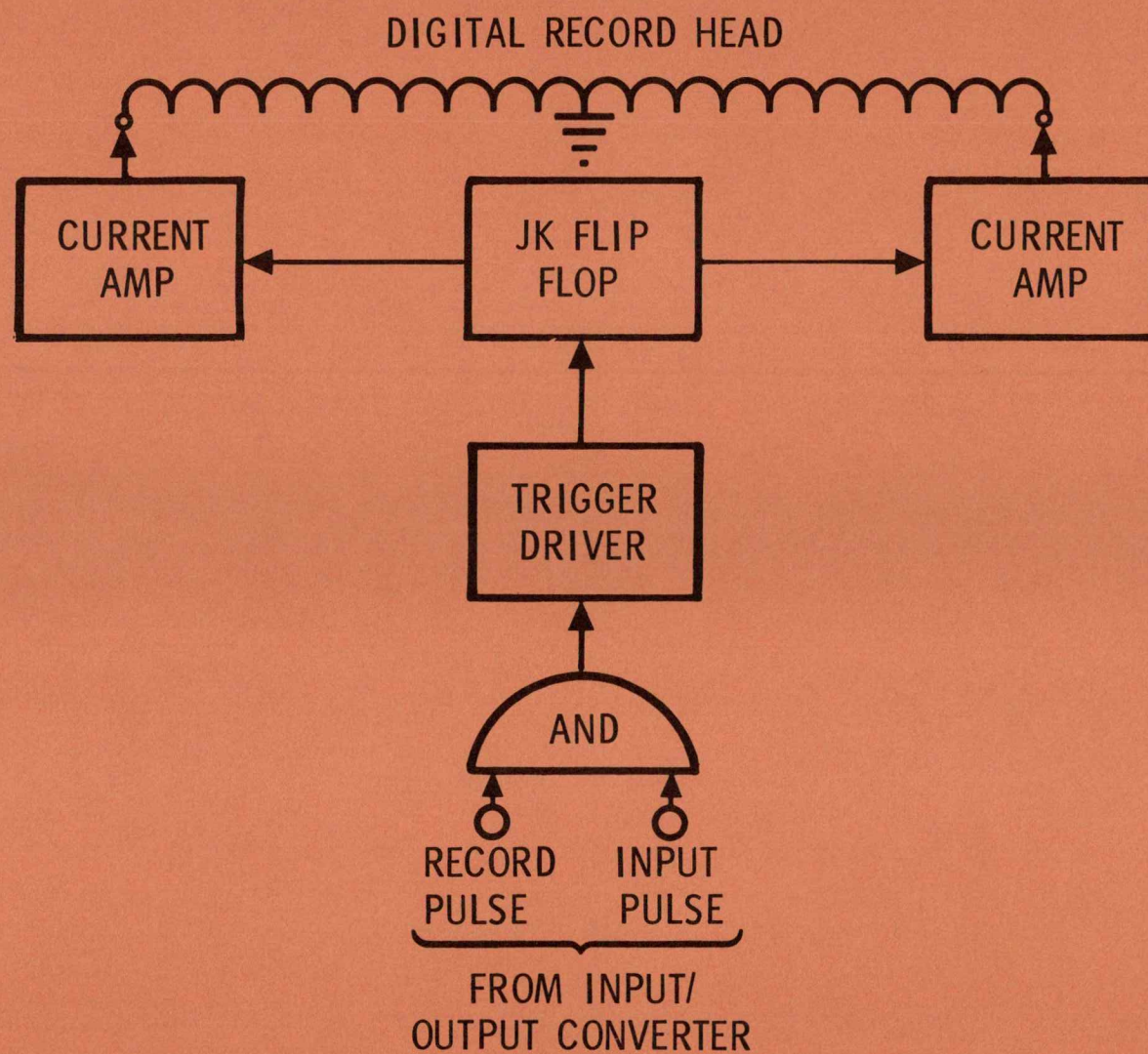


figure 9-5

Each of the digital record amplifiers reads in this fashion. But, because each is connected to a different register stage, a different one of the four bits is read at the time of the clock pulse. The data bits coming into the register are 20 microseconds apart so that the center pulse spacing, out of a given digital record amplifier gate, is 80 microseconds. The pulse width, itself, is approximately 3.2 microseconds.

If the input signal from the register was a "1", the resulting "1" is fed to a flip-flop circuit from the trigger driver stage. The flip-flop provides a change-of-state for each input driving pulse, regardless of the previous state.

The flip-flop has two outputs, each of which feeds a current driver. The current driver outputs are of opposite polarity and act in push-pull to feed a single, balanced, center tapped recording head.

The overall result on recording data is to provide an alternately polarized flux field for each data "1" bit to be recorded, with no change occurring for a data "0" bit. The alternate polarity of data "1" bits are adequate because the digital reproduce circuitry senses only a transition for a data "1" bit. It is important to note that there is no information carried in the direction of the recorded transition, only in the existence of the transition itself.

DIGITAL REPRODUCE AMPLIFIER. The primary purpose of the digital reproduce amplifier is to reconstruct digital data that has been recorded on tape and to drive the serial registers in order that parallel recorded nrz data may be reconstructed serially. This type circuit is used in each of the four digital channels and the clock channel. A block diagram of the digital reproduce amplifier is shown in Figure 9-6.

The digital data on a recorded tape exist only as reversals of magnetic flux polarity for each binary

"1" that has been recorded. Therefore, the direction of the transition has no meaning. The absence of any change coincident in time with a clock (timing) pulse indicates the existence of a binary "0". This recording method is called nrz mark data.

The pick-up head, like the record head, consists of a balanced center tapped winding which feeds a differential amplifier. This system provides a good driving signal, but includes undesirable elements (noise, induced transients). These appear as common mode voltages and are cancelled out by the balanced differential circuit. The differentiator consists of three differential amplifiers connected in a series. They provide for high gain and degenerative feedback, which controls the circuit gain. The signal, now single ended, is conducted through a differentiating network and coupled to a unique circuit, the tunnel diode Schmitt trigger, located in the level detector block shown in Figure 9-6. The pulse signal will be of alternating polarity for each binary "1" bit, since the transition from the tape heads is alternating. It can now be seen that the tunnel diode Schmitt trigger will be alternately driven from one state to the other, with each "1" bit received.

The Schmitt trigger output will drive an amplifier to an on or off state. The output of this amplifier interfaces a full-wave rectifier circuit. The rectifier circuit consists of a transistor stage where the double ended input is fed to both the emitter and collector circuits, providing simultaneous pulses of opposite polarity and equal amplitude. This provides a phase splitting action. These outputs drive a pair of full-wave rectifiers.

The output of the full-wave rectifier is conducted to a multivibrator circuit. The multivibrator provides generation of pulses of uniform amplitude and width. The first transistor section of the multivibrator provides an output which is the reconstructed clock pulse for synchronizing the serial shift when this module is

BLOCK DIAGRAM DIGITAL REPRODUCE AMPLIFIER

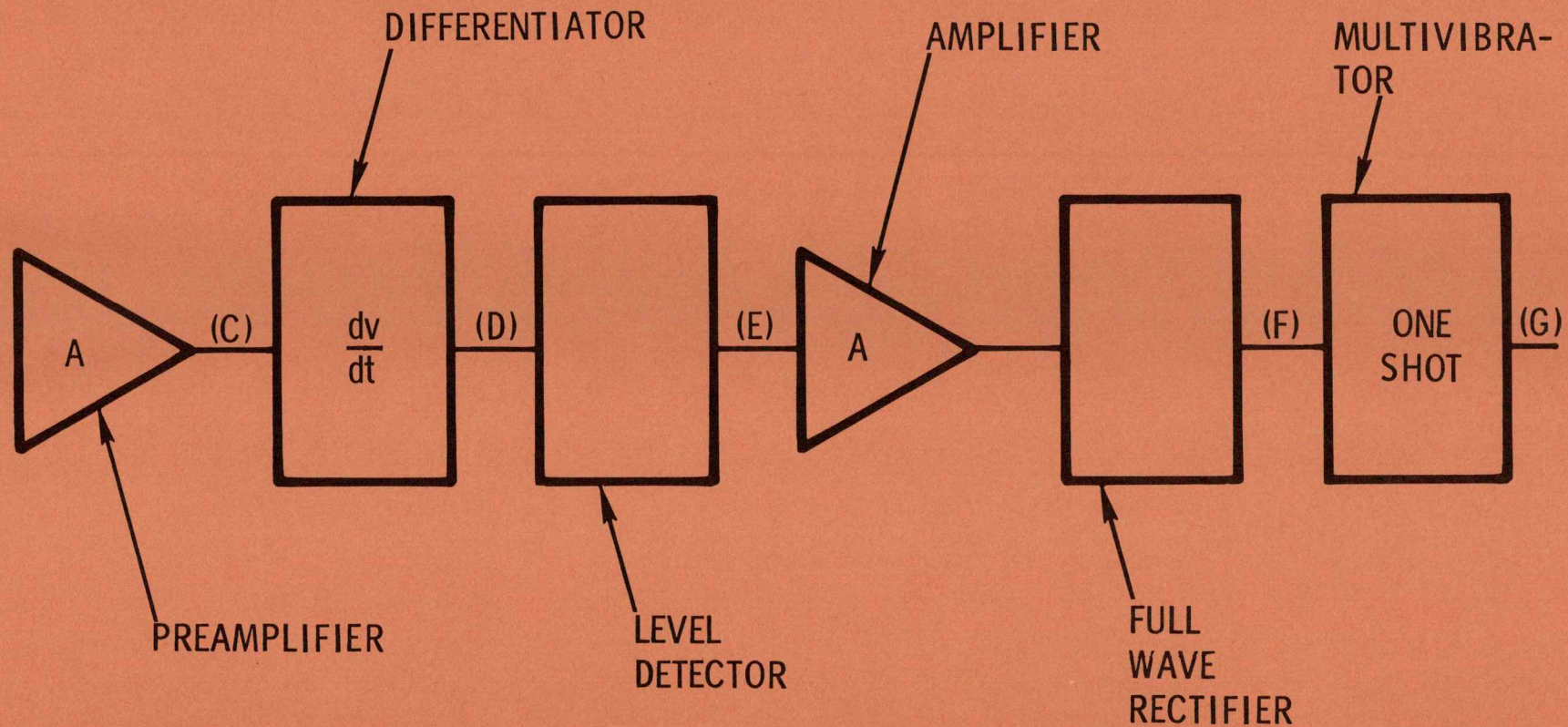


figure 9-6

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used in the clock channel. However, this output has no effect on the four digital channels. In the four digital channels, the signal is coupled from the first section of the multivibrator to the phase inverter section and provides an output pulse of the proper polarity for driving one of the four register stages in the serial shift register.

ANALOG RECORD AMPLIFIER. The Analog Record Amplifier, figure 9-7, consists of the bias amplifier, the data amplifier, and the bias rejection network. The bias amplifier accepts a 100 kc, low-distortion sine wave input from the bias oscillator. It amplifies this 100 kc wave and applies it directly to the analog record head. The bias amplifier consists of two stages; a buffer amplifier for isolation, and an output power amplifier to drive the head. Because the currents of the two signals (100 kc bias signal and analog input signal) are mixed in the heads and because of the inverse feedback properties of transistor circuitry, it is necessary to isolate the two currents with a bias rejection network. This network serves to prevent bias frequencies from feeding back through the data amplifier and appearing at its input terminals.

ANALOG REPRODUCE AMPLIFIER. The analog reproduce amplifier reproduces the signals recorded on tape with a 40 db minimum signal-to-noise ratio and a frequency response of ± 2 db from 50 cps to 10 kc. This figure includes both tape head and amplifier deviating. The input signal to the reproduce amplifier can be followed by referring to the block diagram, Figure 9-8.

The first portion of the reproduce amplifier is basically a differential amplifier consisting of four states. These provide high gain and high input impedance in a feedback loop configuration. When the signal from the reproduce head is applied to the first state amplifier, it is amplified and provided with common mode rejection. The second stage also ampli-

fies and provides common mode rejection to the input signal. The next amplifier provides for a single ended output and amplification. The single ended output signal is then fed to an emitter follower stage. The output from the emitter of this stage is routed through a negative feedback circuit to the input of the first differential amplifier. The negative feedback is designed with a slope similar to curve 2 of Figure 9-9 which has a frequency-to-amplitude slope characteristic inversely proportional to the frequency-to-amplitude response of the head. This provides the desired frequency response to accommodate the 6 db per octave slope of the leading edge of the head, accommodating approximately 50 cps to 7.5 kc. At frequencies above 7.5 kc, the negative feedback becomes almost inactive. At this point, the amount of negative feedback does not change appreciably and the output is fed through a lead (high frequency boost) network, to compensate for the high frequency roll-off characteristic of the head above the approximate 7.5 kc peak. Since this roll-off characteristic is approximately a 12 db per octave slope, the lead network must boost the high frequency signals at that rate to compensate for the head characteristic curve. Curve 3 of Figure 9-9 illustrates the combined head and amplifier response.

The output amplifier provides 600 ohm output impedance which matches the input impedance of the audio transformer which it feeds.

AUDIO TRANSFORMER. The audio transformer module has two purposes. With the maximum input of 4.4 volts peak-to-peak, the transformer converts the input voltage to 5 volts peak-to-peak in order to utilize the full range of the analog system while recording data. During the reproduce mode the output audio transformer circuit will receive 5 volts peak-to-peak from the DSE pre-amplifier through the patch panel. It converts this to 2 volts peak-to-peak. An emitter follower circuit is used to match the input impedance of the reproduce audio transformer.

ANALOG RECORD AMPLIFIER

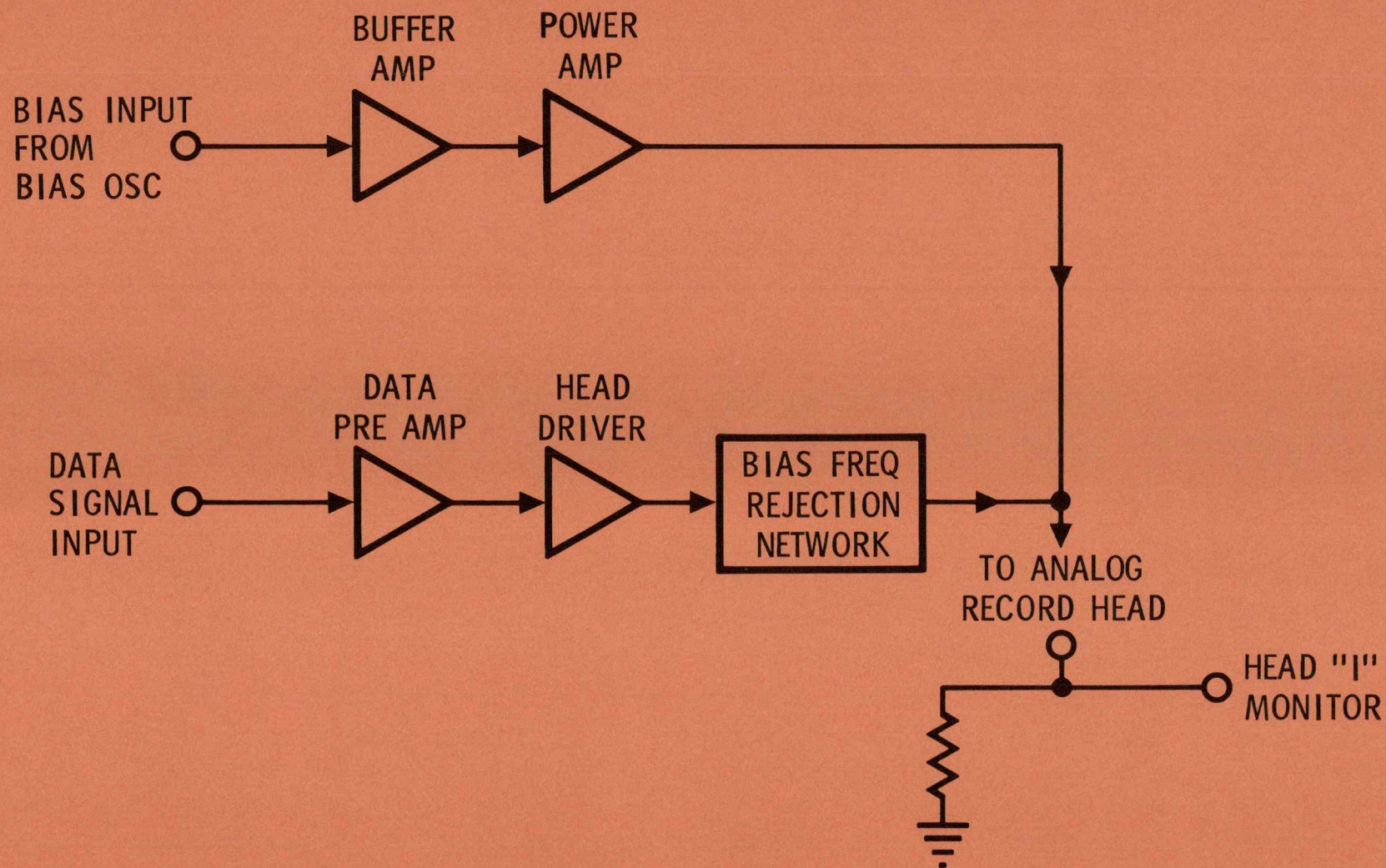


figure 9-7

CD-189



BLOCK DIAGRAM ANALOG REPRODUCE AMPL'F.

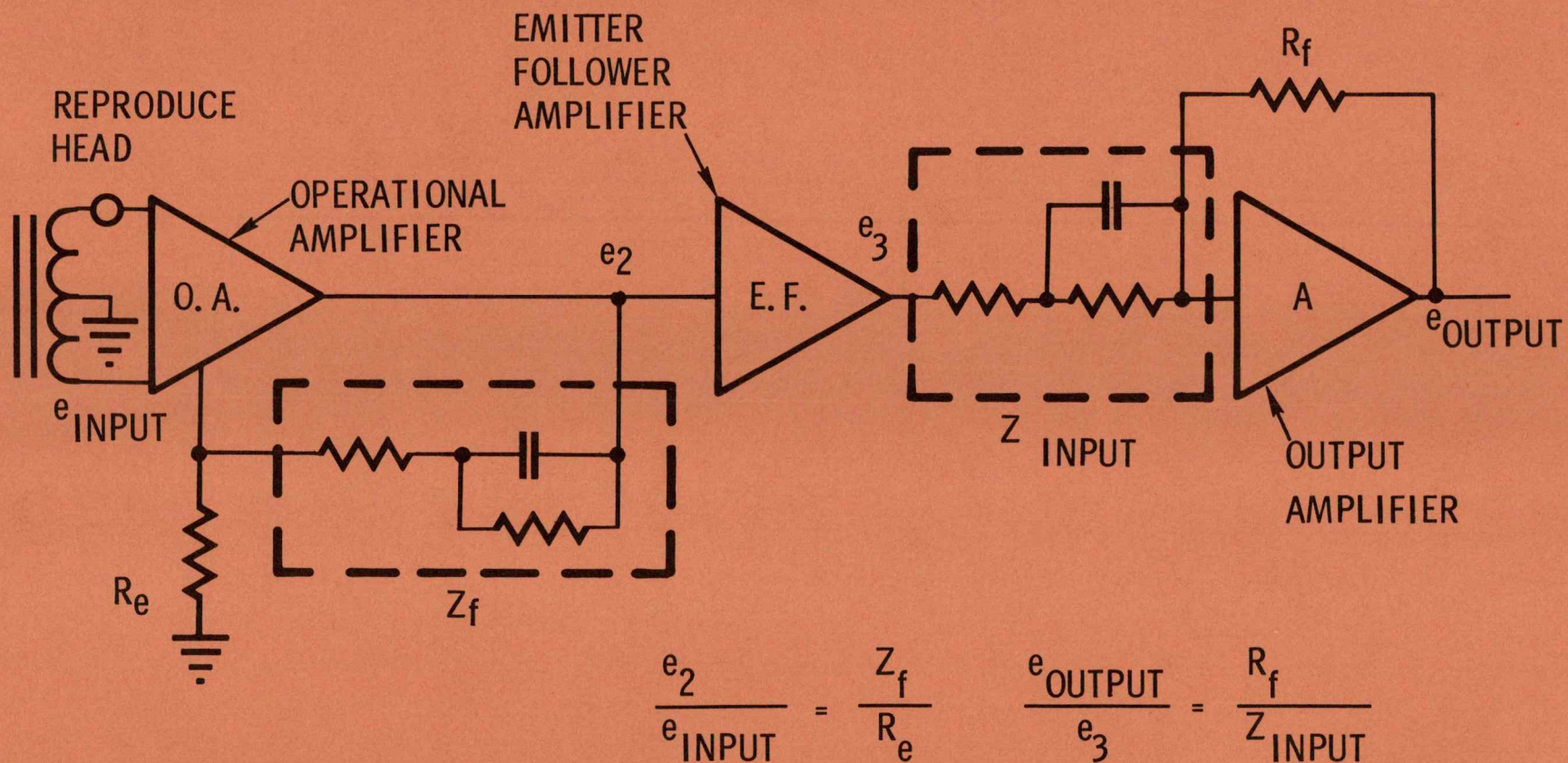


figure 9-8

TAPE TRANSPORT THEORY

The principle purpose of the tape transport is to provide the constant tape speeds past the record-reproduce heads during the record and reproduce modes. In addition, it provides higher speeds for fast-forward and fast reverse. In addition to the above, the transport system also provides near constant tape tension which minimizes tape flutter and skewing.

The drive system is powered by two 400 cps motors and associated systems. The two major systems of the transport are the tape drive system and the reel drive system.

REEL DRIVE SYSTEM. The reel drive motor, although powered by 400 cps, is not synchronous. Its characteristics are such that its speed and torque are in excess of that required at the output of the hysteresis clutch. This provides a drive system of higher efficiency than a system using conventional reel motors operating at near stalled conditions. The output of this motor is coupled to a hysteresis clutch with a torque step-up in the pulley and belt drive.

The hysteresis clutch makes use of the coupling that takes place when a steady state magnetic field is rotated adjacent to a conducting surface. The rotating field induces eddy currents to flow in the conducting material. The eddy currents flow in the conducting surface in what is essentially a shorted circuit. The short circuit eddy loops, requiring considerable power to induce current, reflect a load reactance to the rotating field. Since the conducting surface is free to rotate, it will do so as long as the loading is not greater than the slippage losses. Slippage will always occur because the moment the conductor is rotating at the same velocity as the field, there is no relative motion between the two and the induced field ceases to exist. Thus, the conductor's angular velocity decreases.

Since the magnetic coupling is never 100%, and there is some resistance in the conductor, the output loading of the hysteresis clutch can be completely stopped without stalling the driving source, but at the same time, maintaining a constant torque. This feature becomes most important when dealing with the differential and capstan drive explained below.

The output of the hysteresis clutch is pulley and belt coupled to the differential, again, providing a set-up in torque through the difference in pulley diameters. The differential produces two mechanical outputs from a single input. The two outputs are allowed to assume different rotational speeds. The differential characteristics are such that torque is applied equally to the two outputs without regard for their individual angular velocities, which may vary widely. The two outputs are belt coupled to the two hub pulleys on each of the two reels. The take-up pulley has two idler pulleys on either side, which allows the driving belt to "fold" back and drive the take-up reel in the opposite direction to the supply reel.

Observe that all of the driving gear mentioned above has the effect of applying equal and opposing torque to each of the two reels. This causes tension to be applied to the tape. A slight unbalance of tension exists when one reel has more tape than the other. If allowed to do so, the system will, because of this unequal loading, drive until the reels have equal amounts of tape, at which point it would stall in balanced state. Thus, the reel drive system provides no significant driving power to the tape.

A second force, the tape driver, will cause the tape to move across the heads. The reel drive differential will immediately sense an unbalanced loading condition and compensate by rotating the reel with "slack", until the loading is again balanced. The near balance of loading is maintained even when high rotational speeds are required.

In this manner the tape is held under near constant tension under all operating conditions, thus minimizing flutter, skew and "looping" tendencies.

TAPE DRIVE SYSTEM

The tape drive motor is also powered by a 400 cps source and is synchronous, providing a constant angular velocity output, dependant only upon the input power frequency. The motor output is belt coupled to the magnetic clutch. To reverse the motor's mechanical direction two of its three 400 cps phases are reversed.

The magnetic clutch unit is electrically operated and will couple the tape drive motor input through two, four or six pulley arrangements to give an output speed of 3.75 inches per second (ips), 15 ips, or 120 ips. The output speed is determined by the energized or deenergized condition of the two electromagnetic clutches.

The capstan drivers are the two larger shafts at either end of the recoding heads. Power is applied directly to only one capstan, the other is tightly belt coupled to the first. Between the capstan pulleys there are two passive idlers against the capstan coupling belt. The idler nearest the take-up reel is a canted pulley. Its axis of rotation is not perpendicular to the plane of belt travel, but has a slight angular displacement. The canted pulley provides a belt shifting function in conjunction with the two capstan pulleys. Each of the capstan pulleys has a variation in diameter between the ends, such that one end has a 0.2 percent greater diameter than the other end. Upon a change in direction of tape travel, the canted pulley will cause the belt to progress laterally across the capstan pulleys, allowing the lead pulley to have a 0.2 percent greater pulling force than the follow-up pulley. Because the capstan on the take-up side leads the capstan on the supply side, an increased tension is provided as the tape passes over the heads. To provide this tension with the

reels would require more electrical power in the reel motor. The capstan shafts provide the tape motion, while a pair of rollers at each end guide the tape prior to its passing over the capstan and heads.

The reel braking system is a fail safe operation which will immediately apply the brakes upon loss of electrical power. This precludes the possibility of tape looping if the power is removed. There are two electromagnetically operated brake shoes; one for each reel. They provide differential braking action. The energized solenoids hold the brakes off.

The differential braking feature is such that regardless of direction of tape travel, the supply reel braking is about three times as effective as the braking of the take-up reel. This prevents any slack, with associated looping, from occurring when the brakes are applied.

CONTROL LOGIC

The control logic of the DSE consist of latching relays and electronic circuitry to provide for power failure and end-of-tape shut down. Its main purpose is to choose a mode of operation of which the recorder will operate. By manipulating several switches, a combination of latching relays and electronics select a mode consistent with the data to be recorded. Any data which is recorded may be reproduced and played back. Switching will also be used to choose the speed of recording or playback and the direction of tape movement in each case. The recorder is a bi-directional machine. The recorder electronics contains an interlock circuit which insures against selection of an improper record or reproduce mode. An input from the telemetry equipment indicating a normal or reduced bit rate mode of operation will be used in this interlock circuitry. The data to be recorded and the speed at which it is recorded must, then, be consistent.

ANALOG REPRODUCE HEAD RESPONSE

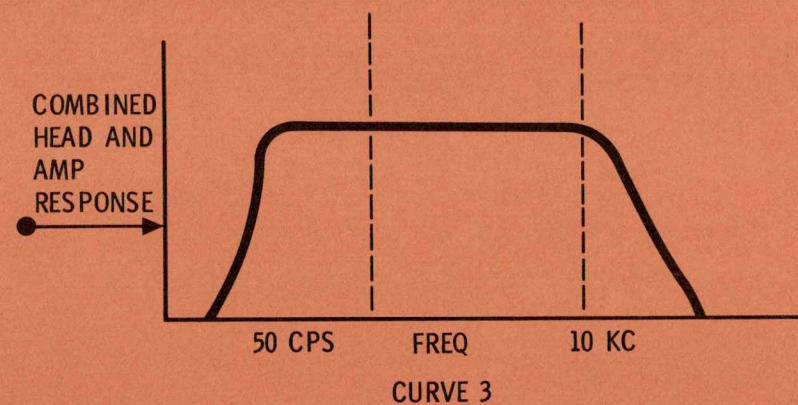
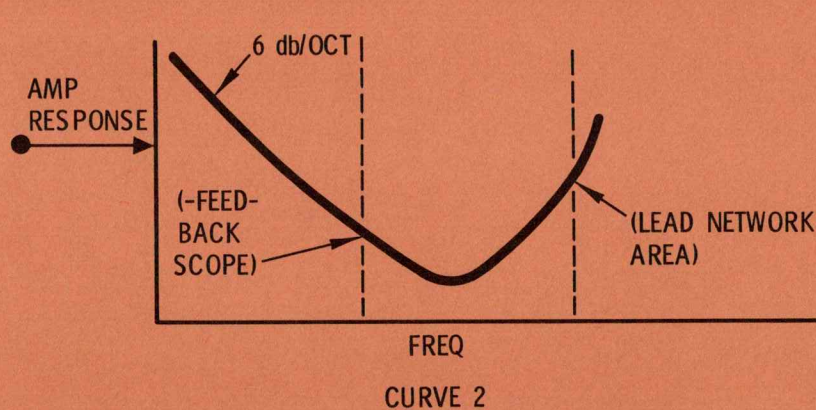
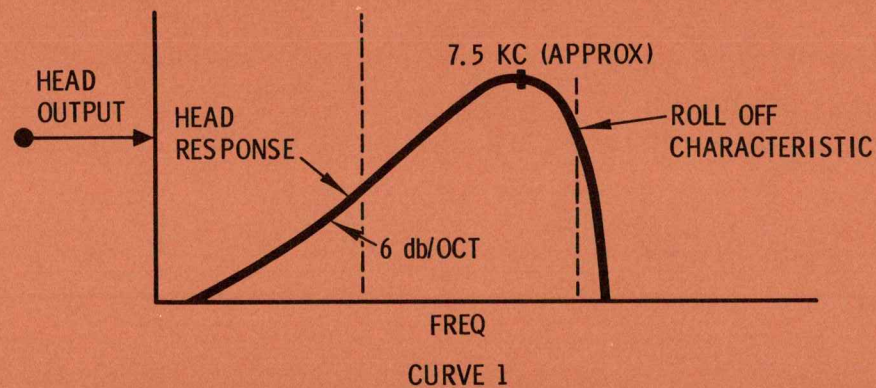


figure 9-9

In the introduction of this section it was stated that the recorder would playback and record both digital and analog information. The rate of the digital information will either be 1.6 K kbs or 51.2 K kbs. The 51.2 K bit mode will be considered the normal mode of operation. The analog information will consist of audio and low vibration frequencies. A block diagram of the DSE control logic is shown in Figure 9-10.

Looking at system control logic block diagram, note that 115 volts, 400 cps is fed to the POWER ON/OFF relay. It is this voltage that powers the two ac motors, which were introduced in the tape transport discussion. The power relay also provides dc voltages to the recorder's analog and digital electronics. The astronaut control panel will supply +28 vdc signal to the control logic to energize relays through switch manipulation for various operations.

NORMAL MODE. In the normal mode of operation, the High-Normal-Slow switch will be positioned to NORMAL. This means the tape speed is 15 ips. The RECORD-OFF-PLAYBACK switch will be moved to the RECORD position energizing the record electronics. The FORWARD-STOP-REVERSE switch is placed in the FORWARD position, meaning a record function will be performed with a forward movement of the tape across the heads.

A 115 volt 400 cps ac is seen at the Power on/off relay. Before this voltage is applied to the Power Supply Module block of the Drive on/off relay one of the two switches above must be placed to some position other than OFF.

When the RECORD-PLAYBACK switch is placed in the RECORD or PLAYBACK position, a 50 m sec ground is applied to the Power on/off relay, latching it in the energized position. A 50 m sec ground is also applied to the B+ on/off relay and the RECORD-PLAYBACK relay energizing them.

The ac is now passed through the Power on/off relay to the Power Supply Module where it is rectified to provide +14.5 v dc, + 34.5 v dc and -7.5 v dc. The B+ on/off relay being energized at the same instant provides a path for each of these voltages into the Multi-Regulator Block. Utilizing these voltages, the regulator generates +12 v dc and -5 v dc which it feeds to the analog and digital electronics through the record-playback relay. This relay provides a path for the dc bias voltages to the record or playback electronics.

In this CONTROL LOGIC functional analysis the next switch that will be positioned will be the HIGH-NORMAL-SLOW switch.

When the HIGH-NORMAL-SLOW switch is positioned to NORMAL the equipment will record at 15 ips and voltage will be applied to four different circuits. The first circuit seen on the block diagram is the command interlock circuit. This logic circuit will determine if the astronaut has selected a valid mode of recorder operation. If not, an output from this circuit will remove all dc voltage from the digital and analog electronics through the B+ on/off relay. At the same time, ac is disconnected from the two motors via the drive on/off relay. Before recorder operation is again restored a valid mode of operation must be chosen.

The second use of the HIGH-NORMAL-SLOW switch output is applied through an OR gate to a one second delay circuit. In the case of a change in recording speeds it is necessary to first bring the ac motors to a stop so that damage to the motor may be prevented. The delay circuit provides for this function by delaying power application through the drive on/off relay to the ac motors for one second.

The third use of the electrical signal is also felt on a 4:1 magnetic clutch assembly which provides 15 ips as the type speed when energized.

642B-IE DATA STORAGE EQUIPMENT

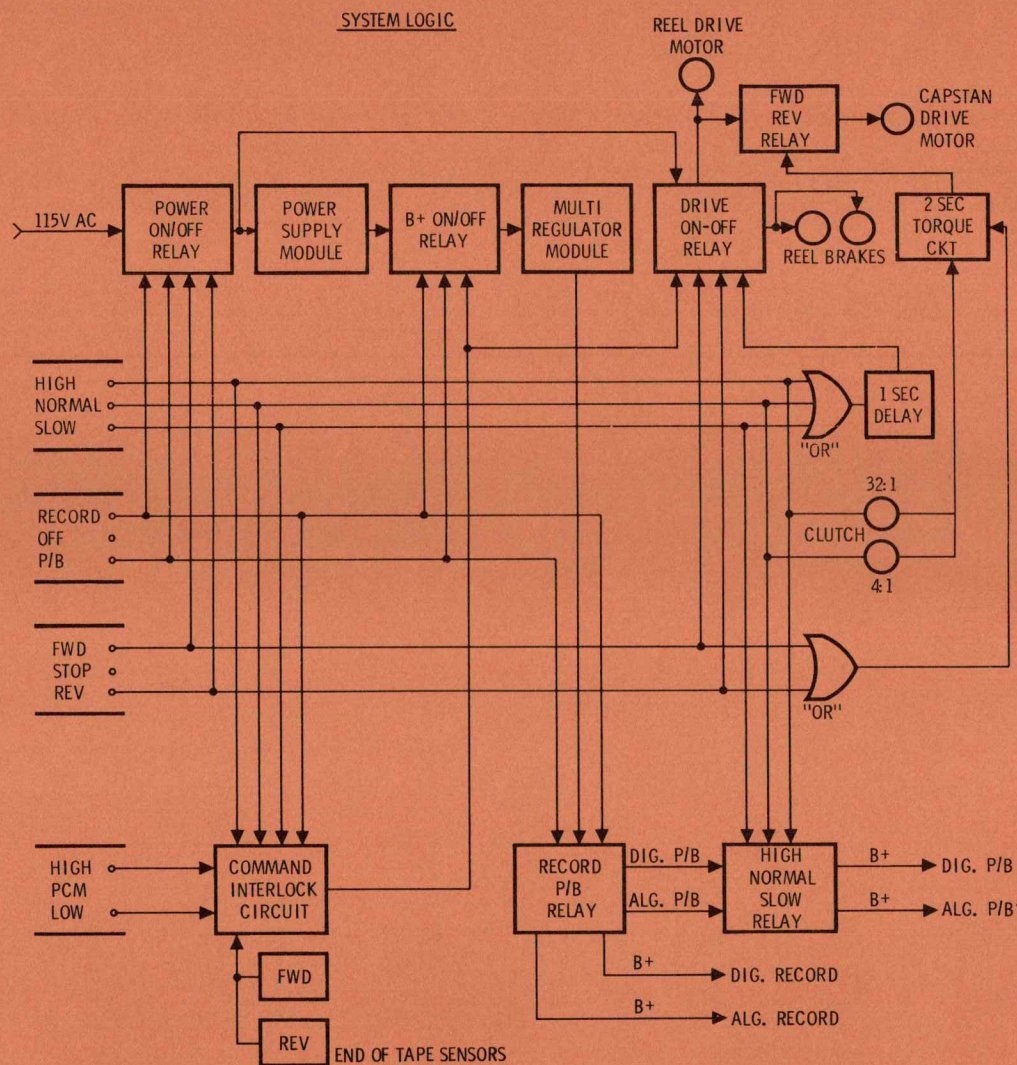
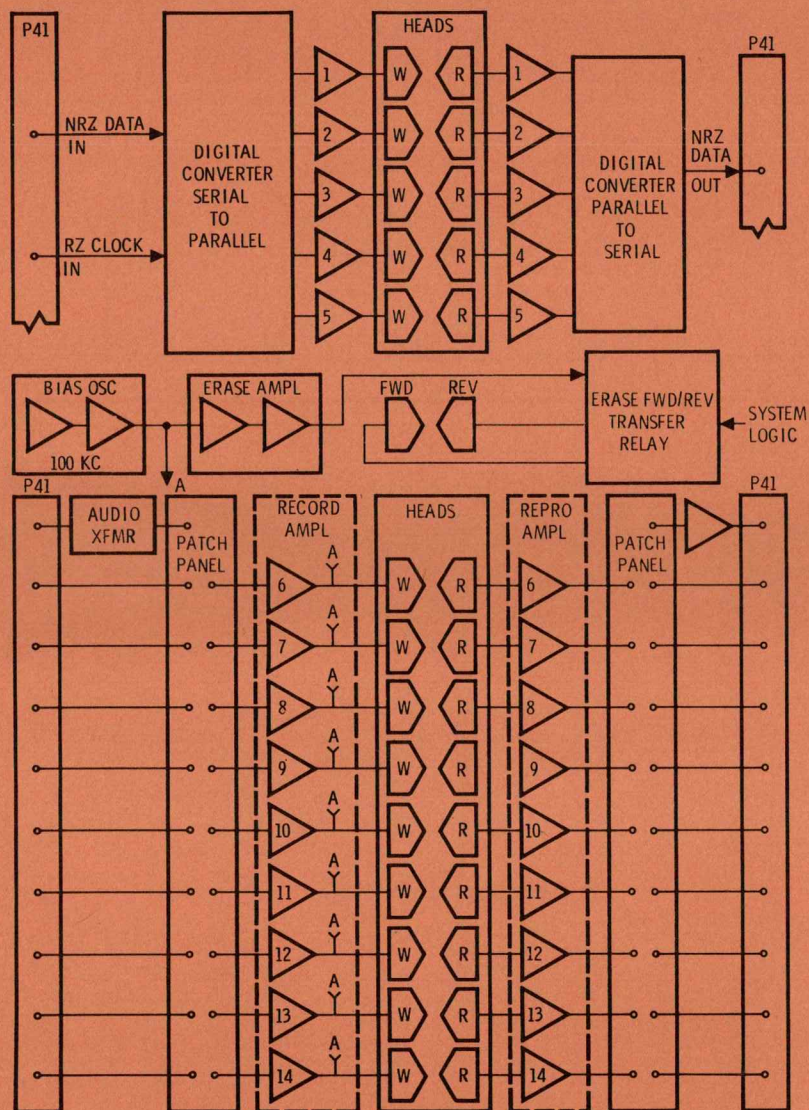



figure 9-10

CD-165A 

If the high speed mode had been selected, a 32:1 clutch would have been energized bringing the tape speed to 120 ips.

A fourth input is seen at the high-normal-slow relay. If the "RECORD-OFF-PLAYBACK" switch is in the PLAYBACK position the above input will energize the high-normal-slow relay so that dc voltage will be provided to the playback electronics. If either high or slow speed had been chosen dc power would not have been provided to the playback electronics through this relay.

The "FORWARD-STOP-REVERSE" switch will determine the direction of tape travel during a record or play-back mode. With the switch positioned to FORWARD, an input will be seen at the power on/off relay. The input also goes to the drive on/off relay and to the forward-reverse relay. The forward-reverse relay will be positioned to forward, but because of the 2 sec torque circuit, motor rotation will be gradually slowed and reversed. The forward and reverse blocks significant with the end of tape sensors function through the command interlock circuit. They are responsible for removing all dc power from either the Record or Playback electronics, depending on the mode of operation, and all ac power from the reel drive and capstan drive motors.

This completes the normal mode explanation. Other speeds and direction selections would cause similar operations to occur in the control logic, as would a change from record to playback.

Table 9-4 gives a brief summary of the tape transport specifications for the DSE. The electronic specifications are not included, as they were presented in an earlier table in this section.

Table 9-4. Tape Transport Specifications

Item	Title	Specifications
1	Tape Speed	15 i.p.s. record/reproduce mode 120 i.p.s. reproduce - fast Forward/Reverse 3.75 i.p.s. record
2	Flutter	Less than 3% peak-to-peak at 15 i.p.s. from 50 cps to 2500 cps
3	Tape capacity	2250 feet IMK mylar tape
4	Recording Time	30 Minutes, minimum
5	Tape width	One inch
6	Magnetic head stacks	Two record and two reproduce to provide 14 channel record/reproduce capability. Two erase heads, to provide erase before record in both directions.
7	Starting time	Three seconds, maximum
8	Power requirements	115 volts, 400 c.p.s., 3 phase and 28 v.d.c. The 28 v.d.c. source is utilized for relay control only.
9	Packing density	853 bits per inch
10	Control	Power on-off Record-Off-Reproduce Forward-Stop-Reverse High-Normal-Slow

SECTION X

PRE-MODULATION PROCESSOR EQUIPMENT, 960C-1

10.1 INTRODUCTION

This section contains a description and the theory of operation (block diagram level) of the Pre-Modulation Processor equipment, 960C-1. The equipment, when installed in the spacecraft, is an integral part of the Apollo Communications and Data Subsystem.

The Pre-Modulation Processor Equipment, 960C-1, (hereafter referred to as PMP) provides interface connections between the spacecraft data-gathering and voice-communication equipment and the rf transmitting and receiving equipment. Multiplexing circuits in the PMP combine the voice signals with certain of the data signals and apply the resulting complex output to the rf transmitting equipment. Detector circuits in the PMP demodulate up-voice and up-data signals (up-signals are signals transmitted from the ground MSFN stations to the spacecraft). The PMP also contains circuits which function in emergency operation in conjunction with the rf transmitting equipment.

10.2 PHYSICAL DESCRIPTION

The PMP is composed of 15 subassemblies, including an Electrical Equipment Chassis, 13 modules, and an Elapsed Time Indicator. Connectors mounted on the electrical equipment chassis provide electrical connections for normal operation. Access to signals within the PMP is made through a chassis mounted test connector for test and trouble-shooting. The subassemblies are listed below:

a.	Electrical Equipment Chassis	A1
b.	Power Supply Module	A2
c.	AF-RF Oscillator Module No. 1	A3
d.	AF-RF Oscillator Module No. 2	A4
e.	AF-RF Oscillator Module No. 3	A5
f.	Data Modulator Module	A6
g.	FM Data Detector Module	A7
h.	FM Voice Modulator Module	A8
i.	FM Voice Detector Module	A9
j.	Elapsed Time Indicator	A10
k.	Relay Module No. 1	A11
l.	Relay Module No. 2	A12
m.	Low Pass Filter Module	A13
n.	Speech Clipper Module	A14
o.	AGC Amplifier/Mixer Module	A15

10.3 LEADING PARTICULARS

The major characteristics of the PMP are listed below. Power listed is the maximum power required for any mode of operation.

a. Over-all Dimensions

1.	Width	10.3 inches
2.	Height	5.82 inches
3.	Length	13.42 inches

b. Weight 14.5 pounds

c. Electrical Power

1.	AC Voltage	115/200 v, 400 cps, 3-phase, 4-wire balanced, floating neutral
----	------------	---

2. DC Voltage	+28, +2, -4 v	9. Up-voice/data	0.2 to 5.0 v peak, 1.0 v peak nominal, complex waveform comprising FM voice signals at 30 kc and FM data signals at 70 kc center frequency
d. <u>Power Required</u>	12.5 watts max.		
e. <u>Inputs</u>			
1. Voice	300-3000 cps 1.1 v peak nominal, 2.5 v peak max.		
2. Analog sensors	18 channels, 0 to 5 v p-p, dc to 10 kc	f. <u>Outputs</u>	
3. Analog (P/B)	9 channels, 0 to 5 v p-p, dc to 10 kc	1. PM	Complex waveform comprising 2.2 v p-p, 1.024 mc, bi- phase modulated data signal, and 1.68 v p-p, 1.25 mc frequency mod- ulated voice sig- nal
4. PCM (R.T.)	NRZ, 51,200 bits per sec. max., 1,600 bits min., 6 \pm 0.6 v amplitude	2. FM	Complex waveform comprising 0.466 v p-p, 1.024 mc, bi- phase modulated data signal; 0.532 v p-p, 1.25 mc FM voice signal; and nine 0.135 v fre- quency modulated data signals of 14.5, 22, 30, 40, 52.5, 70, 95, 125, and 165 kc or 1.334 peak amplitude, 40 cps to 500 kc TV signal or 0.406 v p-p biomed signal
5. PCM (P/B)	Same as PCM (real time)		
6. PCM Clock	512 kc square wave unipolar, +6 \pm 0.6 v ampli- tude, rise and fall times less than 1% of the period, duty cycle 50%		
7. TV Camera	40 cps to 500 kc, 2 v p-p		
8. Biomed sensors	4.54 v p-p		

BLOCK DIAGRAM PMP

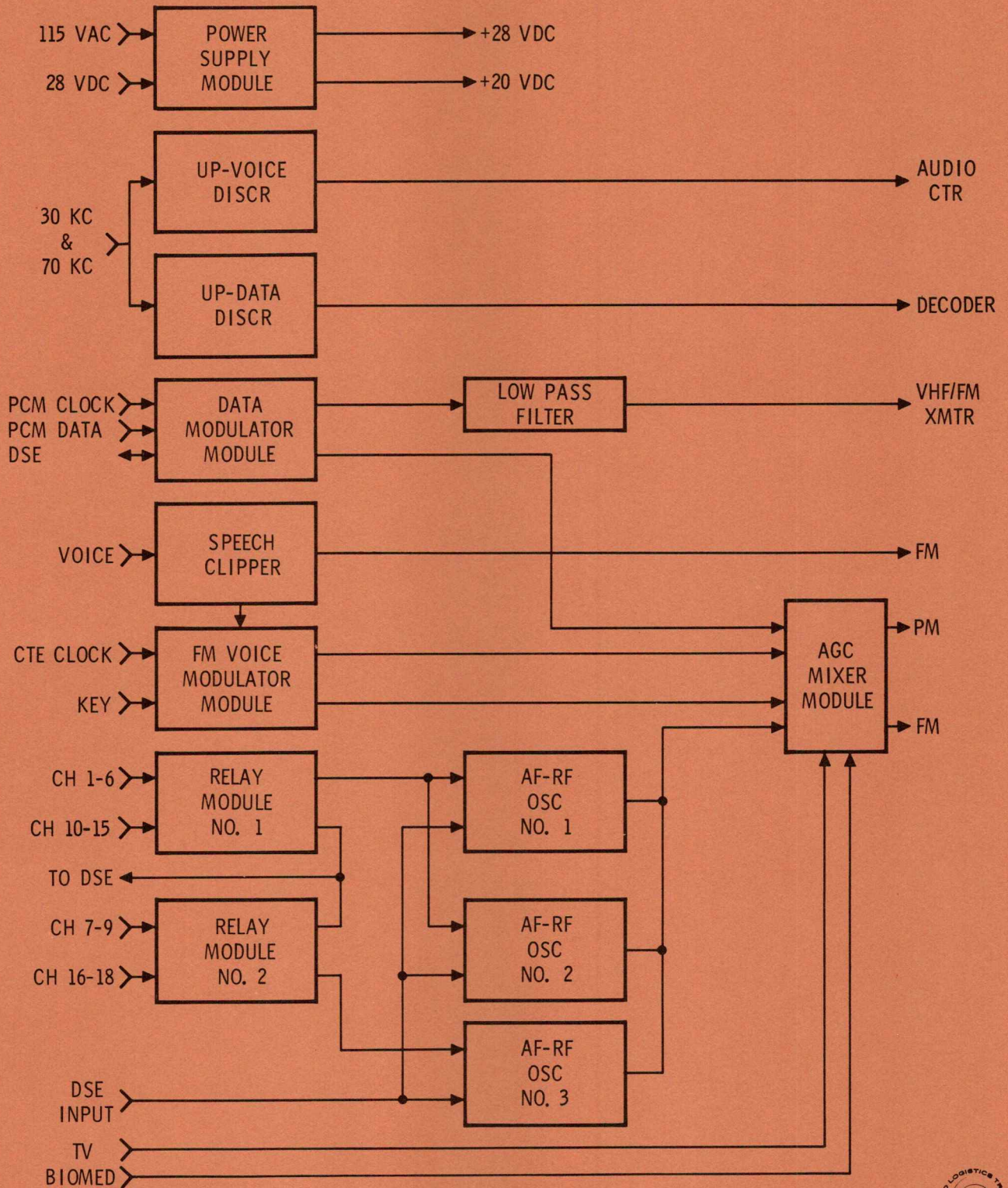


figure 10-1



- | | |
|--------------------|---|
| 3. VHF/FM | 51,200 bits per
sec. max., 1,600
bits per sec. min. |
| 4. Emergency Voice | 300-3000 cps |
| 5. Emergency Key | 512 kc sinusoidal
wave, 2.2 v p-p
amplitude |

Recorded NRZ PCM telemetry data from the data storage equipment bi-phase modulates a PCM telemetry subcarrier in the PMP and the modulated subcarrier is routed to the unified S-band equipment.

The PMP performs three independent functions in the normal transmission mode and two independent functions in the receive mode.

10.4 FUNCTIONAL DESCRIPTION (FIGURE 10-1)

The PMP is designed to provide interface connections between the spacecraft data-gathering and voice-communications equipments and the rf transmitting and receiving equipment. The unit also provides modulation and frequency multiplexing of voice and telemetry subcarriers and appropriate mode switching for all normal and emergency operation.

The PMP processes signals from the spacecraft analog sensors, VHF/AM Transmitter-Receiver (biomed), and TV camera in addition to the following equipments:

- a. PCM Telemetry Equipment
- b. Data Storage Equipment
- c. Audio Center Equipment
- d. Unified S-Band Equipment

The unit provides frequency modulation of a subcarrier by voice from the audio center and FM detection of an up-voice and up-data multiplexed signal from the unified S-band equipment. The voice subcarrier is conducted to the unified S-band equipment and the detected up-voice and up-data signals are routed to the audio center and UDL receiver-decoder equipment, respectively.

- a. In the transmit mode the following functions are performed:

1. The generation and bi-phase modulation of PCM telemetry subcarrier.
2. The generation and frequency modulation of a voice subcarrier.
3. The generation and frequency modulation of nine analog telemetry subcarrier oscillators.

- b. In the receive mode the following functions are performed:

1. FM detection of the up-voice modulated subcarrier.
2. FM detection of the up-data modulated subcarrier.

- c. In addition to the independent functions, the PMP performs frequency multiplexing of the voice and PCM telemetry subcarriers for PM mode transmission; frequency multiplexing of the voice and PCM telemetry subcarriers along with the nine analog

subcarriers or the television signal or the biomed signal for FM mode transmission.

10.4.1 Receive Operation

In the receive mode, signals are routed from the unified S-band equipment to the FM voice and data detectors. A band-pass filter in each detector separates the desired signal from the frequency multiplexed up-link signals prior to detection. The detected up-voice signal is routed to the audio center, and detected up-data is routed to the UDL receiver-decoder equipment.

10.4.2 Transmit Operation

Transmit modes of the PMP as follows:

a. PM Mode:

- | | |
|--------------|-------------|
| 1. Ranging | (PCM/Voice) |
| Off | (PCM/Voice) |
| Ranging Only | (Voice) |

b. FM Mode:

- | | |
|-------------|-----------------------------------|
| 1. Tape/PCM | (Play)(PCM playback/Analog/Voice) |
| Tape/Normal | (Play)(PCM-Analog playback/Voice) |
| Tape/ANLG | (Play)(Analog playback/PCM/Voice) |
| Off | (PM-PCM/Voice) |
| Analog | (Analog/PCM/Voice) |
| 2. TV | (TV/PCM/Voice) |
| Off | (PM-PCM/Voice) |
| PLSS | (Biomed/PCM/Voice) |

c. Emergency Mode:

- | | |
|----------|-------------------------|
| 1. Voice | (Voice Only) |
| Off | (Normal Voice) |
| Key | (Keyed subcarrier only) |

10.5 DATA TRANSMISSION

The PMP receives data inputs in real time from the PCM Telemetry Equipment and recorded PCM and/or analog telemetry data from the Data Storage Equipment. Either of the PCM telemetry inputs may be applied to the Data Modulator in the PMP by operation of the proper switches on the spacecraft communications control panel. The selected input bi-phase modulates the PCM telemetry subcarrier, which is generated by frequency doubling the 512 kc reference clock signal from the PCM Telemetry Equipment. The resulting phase-modulated 1.024 mc signal is filtered and routed to the AGC Amplifier/Mixer where it is frequency multiplexed with the voice and analog or the voice and TV or the voice and biomed signal. The frequency multiplexed signal is applied to the Unified S-Band Equipment (USBE).

10.6 VOICE TRANSMISSION

Voice transmission involving the voice subcarrier occurs during all normal modes of transmission. In the emergency voice mode, the Audio Center voice signal is routed through the Speech Clipper and then directly to the USBE. The emergency key mode is the only mode which does not include any voice communications.

10.6.1 Normal Voice

In all normal modes, voice signals are routed from the Audio Center to the Speech Clipper

in the PMP. The clipped output of the Speech Clipper is applied to the FM Voice Modulator where it is used to deviate the voice subcarrier oscillator in direct proportion to the amplitude of the voice signal. The voice modulated subcarrier is translated up in frequency by heterodyning with the 512 kc clock signal from the Central Timing Equipment (CTE). The signal is then filtered, frequency doubled, and filtered again to provide the voice modulated subcarrier at the proper frequency for the USBE.

In the PM mode, the voice modulated subcarrier is frequency multiplexed with the PCM telemetry subcarrier in the AGC Amplifier/Mixer. In the FM mode, the voice signal is frequency multiplexed with the PCM telemetry subcarrier and analog, or TV signal, or biomed signal. From the AGC Amplifier/Mixer the frequency multiplexed signal is routed to the USBE during both the PM and FM modes for transmission.

10.6.2 Emergency Voice

In the emergency voice mode, the Audio Center voice signal is routed directly through the Speech Clipper to the USBE for baseband modulation. During this mode, the PMP regulated power supply is de-energized by removing the 115 volt, 400 cps ac input. All transmit circuitry is inactive except the emergency key subcarrier tuned amplifier. The receive circuitry (FM voice and data detectors) which operates from the spacecraft primary plus 28 volts dc is operative.

10.7 EMERGENCY KEY

The emergency key mode is one of two emergency modes of transmission. In this mode,

the PMP regulated power supply is de-energized by removing the 115 volt, 400 cps ac input. This is accomplished through mode switching on the communications control panel. All transmit circuitry is inactive except the emergency key circuitry which operates from the spacecraft primary plus 28 volts dc supply. The emergency subcarrier is derived from the CTE clock input by amplitude limiting, isolation, amplification, and filtering the square-wave input. The resulting sinusoidal wave is switched out of the FM Voice Modulator and gated through the AGC Amplifier/Mixer to the USBE. The emergency key switch in the FM Voice Modulator is activated upon selecting the emergency key mode with the communications control panel switch.

10.8 ANALOG TELEMETRY

Eighteen real time analog telemetry inputs are routed to the PMP from the spacecraft analog sensors. One of two possible groups of nine are selected in the PMP for modulation of nine telemetry subcarrier oscillators. The analog telemetry can be routed to the DSE for recording purposes. The PMP, through mode switching, will select the nine real-time inputs or the nine recorded inputs from the DSE to modulate the subcarrier oscillators. The selections are accomplished with latching relays and are operated from the communications control panel mode switches. The relays which select the analog groups and the record relays which route signals to the DSE are located in two relay modules. The playback relays which select real-time or recorded analog telemetry for modulation of the SCO's are located in the sub-carrier oscillator modules.

The sub-carrier oscillator modules, of which there are three, each contain three subcarrier oscillators and a playback latching relay. The modules are identical except for the frequencies

of the oscillators. The analog signals are used to modulate the subcarrier oscillators in the three modules. The outputs of the three sub-carrier oscillator modules are linearly combined and frequency multiplexed with the voice and telemetry subcarriers. The multiplexed signal is routed to the USBE. The input channels, the modules used, and the SCO frequencies are listed below:

<u>Group 1</u>	<u>Group 2</u>	<u>Module</u>	<u>SCO Frequencies, (kc)</u>
1	10	A3	14.5
2	11	A3	22.0
3	12	A3	30.0
4	13	A4	40.0
5	14	A4	52.5
6	15	A4	70.0
7	16	A5	95.0
8	17	A5	125.0
9	18	A5	165.0

10.9 TELEVISION

The television camera provides a signal input to the PMP. The signal is suitably processed and multiplexed with the voice and telemetry subcarriers during the TV/PCM/Voice mode. The mode selection is controlled with communications control panel switching which operates a transistor switch to route the TV signal to the FM mixing network for multiplexing with PCM telemetry and voice subcarriers. The dc voltage is removed from all af-rf subcarrier oscillators during TV transmission.

10.10 BIOMED DATA

The received biomed signals from the VHF/AM Receiver is applied to the AGC Amplifier/

Mixer Module of the PMP. The biomed signals are attenuated and multiplexed with the PCM telemetry and the voice subcarrier during the PLSS/PCM/Voice mode. AGC provides for a constant output over the dynamic range of the input signals. The mode selection is controlled by communications control panel switching which operates a transistor switch to route the biomed signal to the FM mixing network.

10.11 VHF MODE

The PMP also interfaces with the VHF/FM Transmitter. The PMP receives NRZ PCM telemetry data from the PCM telemetry equipment and provides an internal hardwire connection to terminals which will interface with the DSE for recording and also routes the PCM telemetry data through an amplitude limiter to the Low Pass Filter Module. The filtered PCM telemetry data is routed to the VHF/FM Transmitter for transmission to MSFN ground stations during early orbital missions. This provides capability for recording and transmitting PCM telemetry data simultaneously. Recorded PCM telemetry data is routed from the DSE to the PMP for transmission of recorded data in the PCM playback mode. Diode switching, which is activated by communications control panel mode switches, provides the selection of real time or recorded PCM telemetry data for transmission.

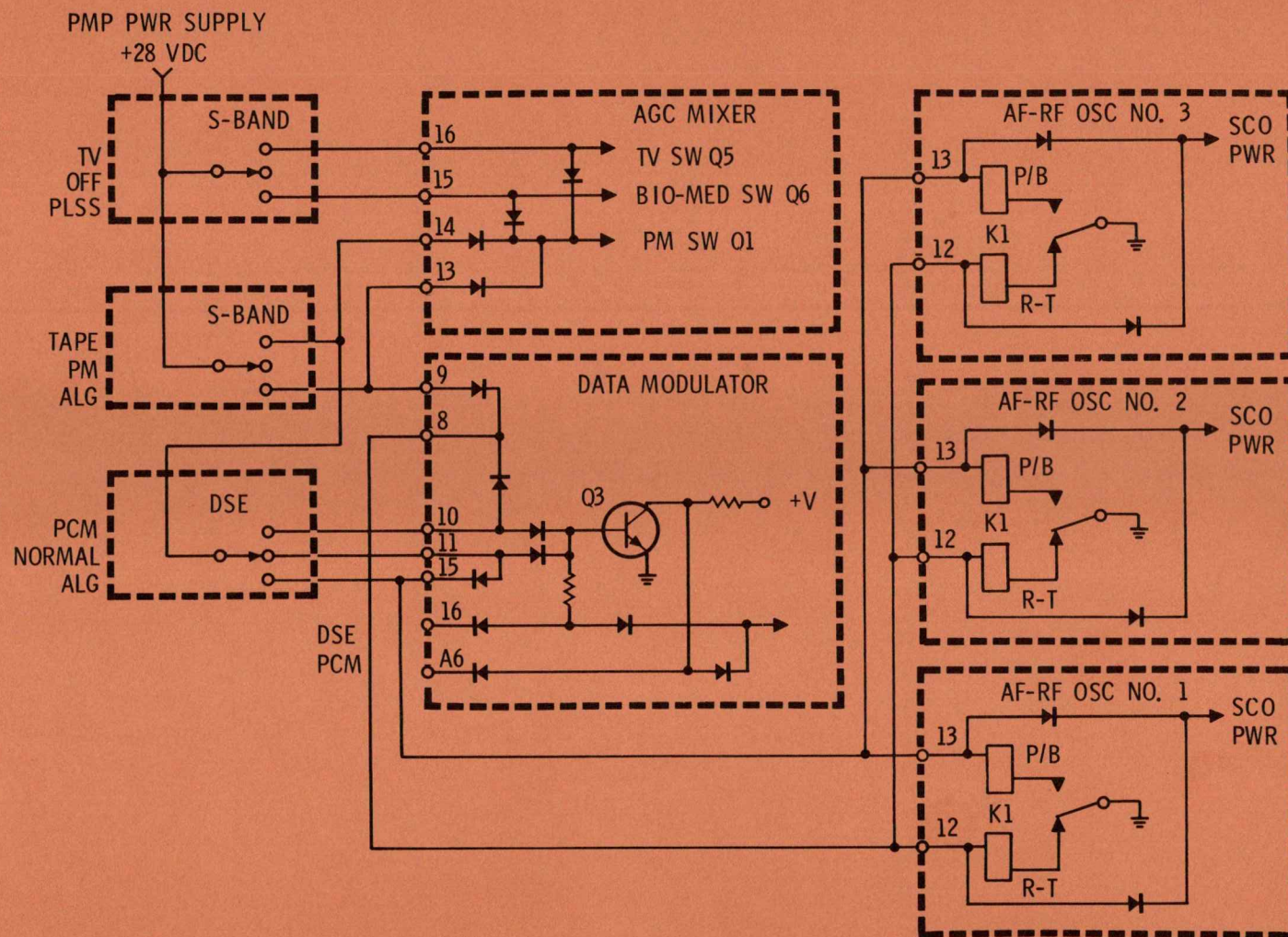
10.12 CONTROLS

The mode switches on communications control panel 20 which directly affect the switching modes in the PMP are tabulated below. The switching functions are depicted in Figures 10-2, 3 and 4.

a. S-Band Normal Switches

1. RANGING - OFF - RANGING ONLY

PMP SWITCHING



CD-161B

figure 10-2

2. TAPE - OFF - ANALOG
3. TV - OFF - PLSS

b. Tape Recorder

1. PLAY PCM - NORMAL - ANALOG
2. RECORD - OFF - PLAY

c. S-Band Emergency

1. VOICE - NORMAL - KEY

d. TLM Inputs

1. ANALOG 1 - ANALOG 2

e. POWER

1. PMP ON - OFF

10.12.1 Mode Switching

10.12.1.1 S-Band Normal Switches

a. RNG-OFF-RNG ONLY switch

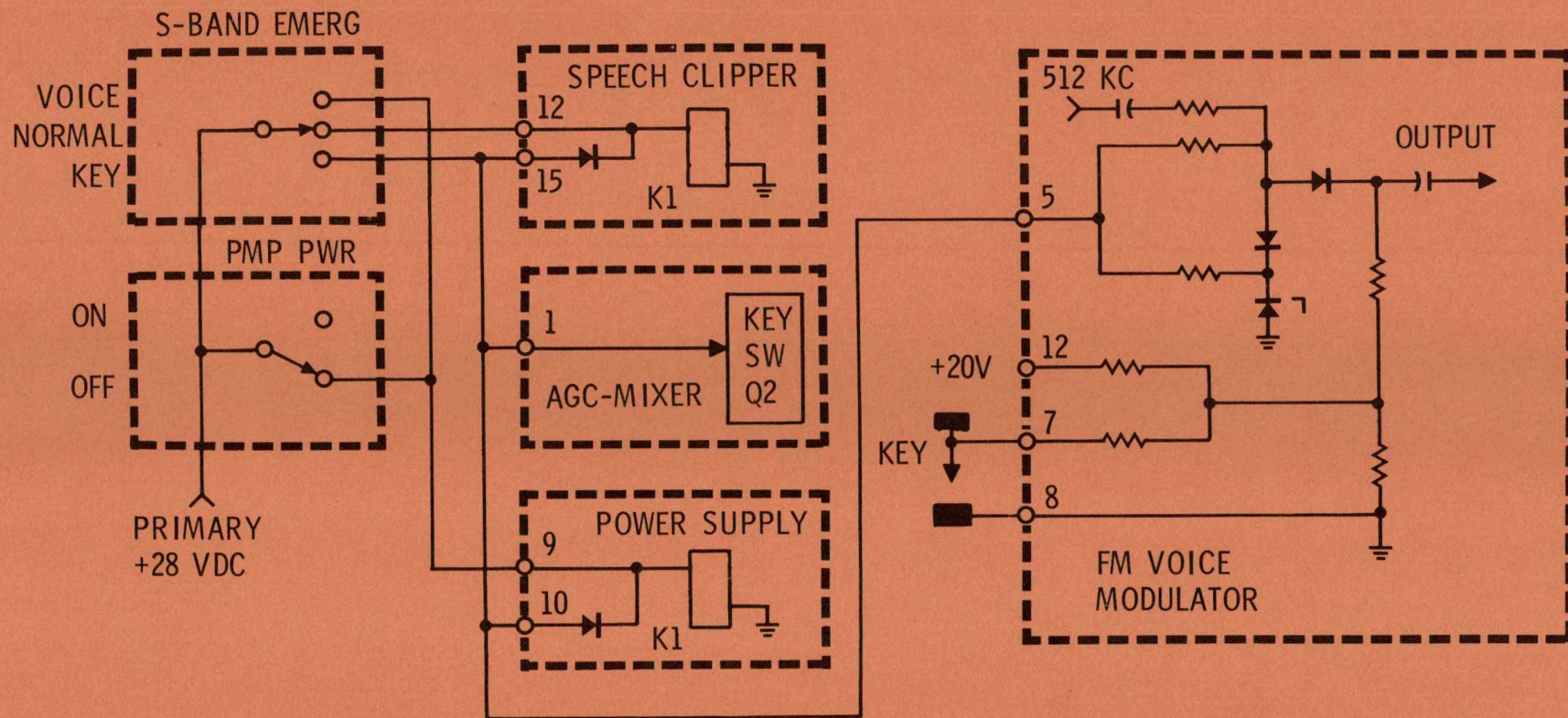
1. RNG ONLY is the only position of this switch that directly affects the operation of the PMP. With the switch in the RNG ONLY position, a ground is supplied to pin 14 of the Data Modulator Module turning off transistor switch Q9. Q9 is normally on, so that PCM data may be processed through the data modulator PCM channel. With Q9 turned off, the bi-phase modulator, clock input and output amplifier sections are disabled. PCM telemetry data may still be

processed through the input limiter stage and modulator to the Low Pass Filter Module to the VHF/FM Transmitter.

b. TAPE-OFF-ANLG Switch (Figure 10-2)

1. The OFF position of this switch enables the PM switch in the AGC Amplifier/Mixer Module and the real-time PCM data switches in the Data Modulator Module.
2. The TAPE position of this switch enables the Tape Recorder switch PCM-NORMAL-ANALOG. PM switch Q1 in the AGC Amplifier/Mixer Module is turned off, routing the voice and PCM data subcarriers to the FM mixing network.
3. The ANLG position of this switch turns off the PM switch Q1 in the AGC Amplifier/Mixer Module and routes the voice and PCM data subcarriers to the FM mixing network. The switch also supplies a dc bias voltage to the subcarrier oscillators in the af-rf oscillator besides switching the latching relays into the real-time analog mode. The outputs of the subcarrier oscillators are also applied to the FM mixing network in the AGC Amplifier/Mixer Module. Therefore, the output of the AGC Amplifier/Mixer Module to the FM input of the USBE consists of the voice subcarrier, data subcarrier, and the nine subcarrier oscillator frequencies.

PMP SWITCHING



CD-160B 

figure 10-3

c. TV-OFF-FLSS Switch

1. The OFF position of this switch enables the FM switch in the AGC Amplifier/Mixer Module and the real-time PCM data switches in the Data Modulator Module.
2. The TV position of this switch enables the TV switch Q5 in the AGC Amplifier/Mixer Module. PM switch Q1 in the AGC Amplifier/Mixer Module is turned off, routing the voice and PCM data subcarriers to the FM mixing network. The output of the AGC Amplifier/Mixer Module in this mode of operation consists of the TV signal, voice, and data subcarriers to the FM input of the USBE.
3. The PLSS (Personal Life Support System) position of this switch enables the Relay switch Q6 in the AGC Amplifier/Mixer Module. PM switch Q1 in the AGC Amplifier/Mixer Module is turned off, routing the voice and PCM data subcarriers to the FM mixing network. The output of the AGC Amplifier/Mixer Module in this mode of operation consists of the biomed signals, voice, and data subcarriers to the FM input of the USBE.

10.12.1.2 Tape Recorder Switches (Figure 10-2)

a. PCM-NORMAL-ANALOG

The PLAY switch is interlocked with the S-band NORMAL switch TAPE-OFF-ANLG. The only time the PLAY switch can be used is when the TAPE position is selected.

1. The PCM position of this switch enables the PCM playback switch Q3 and the PCM playback data switches. Playback switch Q3 inhibits the real-time PCM switches in the Data Modulator Module. This switch position also enables the real-time analog switches in the af-rf oscillator modules. This mode of operation permits recorded PCM and real-time analog information along with the voice subcarrier to be transmitted.
2. The NORMAL position of this switch enables the PCM playback switch Q3 and the PCM playback data switches. Playback switch Q3 inhibits the real-time PCM data switches in the Data Modulator Module. This switch position also enables the playback analog switches in the af-rf oscillator modules. This mode of operation permits recorded PCM and analog information along with the voice subcarrier to be transmitted.
3. The ANALOG position of this switch enables the PCM data real-time switches and the af-rf oscillator playback relays. This switch position permits recorded analog with real-time PCM data information along with the voice subcarrier to be transmitted.

PMP SWITCHING

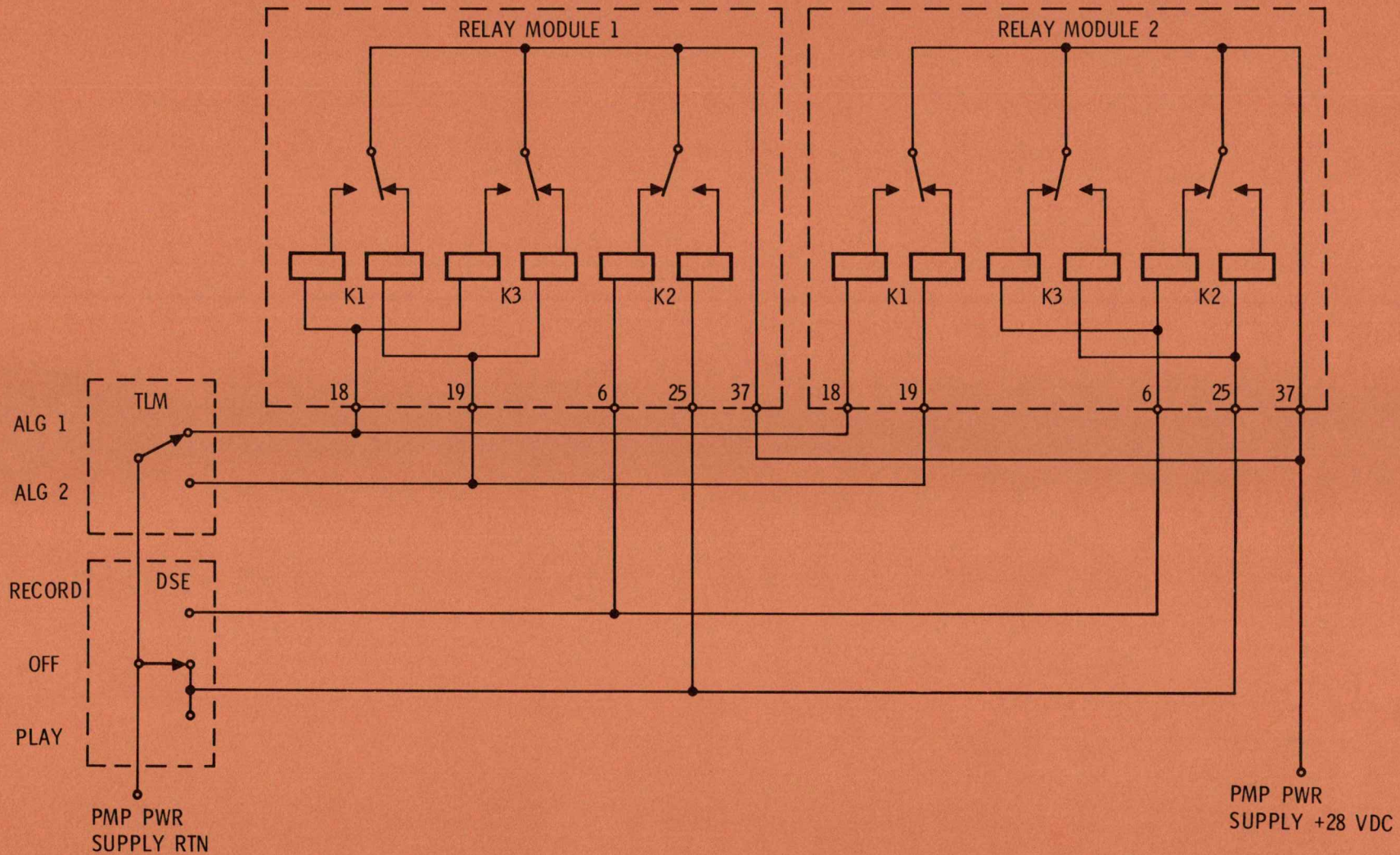


figure 10-4

10.12.1.3 S-Band Emergency Switch (Figure 10-3)

a. VOICE-NORMAL-KEY

1. The NORMAL position of this switch enables the emergency/normal voice relay in the Speech Clipper Module, routing voice signals to the FM Voice Modulator Module where they are translated to the voice subcarrier.
2. The VOICE position of this switch disables the emergency/normal voice relay in the Speech Clipper Module, routing the voice signals at the output of the Speech Clipper Module to the FM input of the USBE. This switch position also turns off the PMP 115 volts, 400 cps regulated power supply.
3. The KEY position of this switch enables keying switch Q2 in the AGC Amplifier/Mixer Module and also the PM switch Q1. This switch position also turns on the keying circuitry of the FM Voice Modulator Module and turns off the PMP 115 volt, 400 cps regulated power supply.

10.12.1.4 TLM Inputs Switch (Figure 10-4)

a. ANALOG 1-ANALOG 2

1. The ANALOG 1 position of this switch enables analog channels 1 through 9 in the PMP relay modules 1 and 2.

2. The ANALOG 2 position of this switch enables analog channels 10 through 18 in the PMP relay modules 1 and 2.

10.12.1.5 PMP Power Switch

a. ON-OFF

With the PMP Power switch in the OFF position, +28 volts dc from the EPS is supplied to the coil of the 115 volt ac relay in the PMP power supply module. Energizing this relay removes ac power to the equipment. With the switch in the ON position, the +28 volts dc is removed from the ac power relay in the power supply module, de-energizing the relay and permitting the 115 volts, 400 cps ac to be applied to the PMP rectifier circuits. This is a "fail safe" type circuit.

10.13 FUNCTIONAL DETAILED BLOCK DIAGRAM

10.13.1 Phase Modulated Mode of Operation

See Figure 10-5. To enable the Phase Modulated (PM) mode of operation, all the S-band normal switches on the communications control panel and the emergency switch have to be in the center position except the RNG-OFF-RNG ONLY switch can be in the RNG position.

The PCM telemetry data from the PCM Telemetry Equipment is presented to the PMP Data Modulator Module at pin A6. The output impedance of the PCM Telemetry Equipment is less than 100 ohms and the input impedance of the Data Modulator is 10,000 ohms minimum. The input is a NRZ type

DATA MODULATOR & LOW PASS FILTER MODULES, PMP

BLOCK DIAGRAM

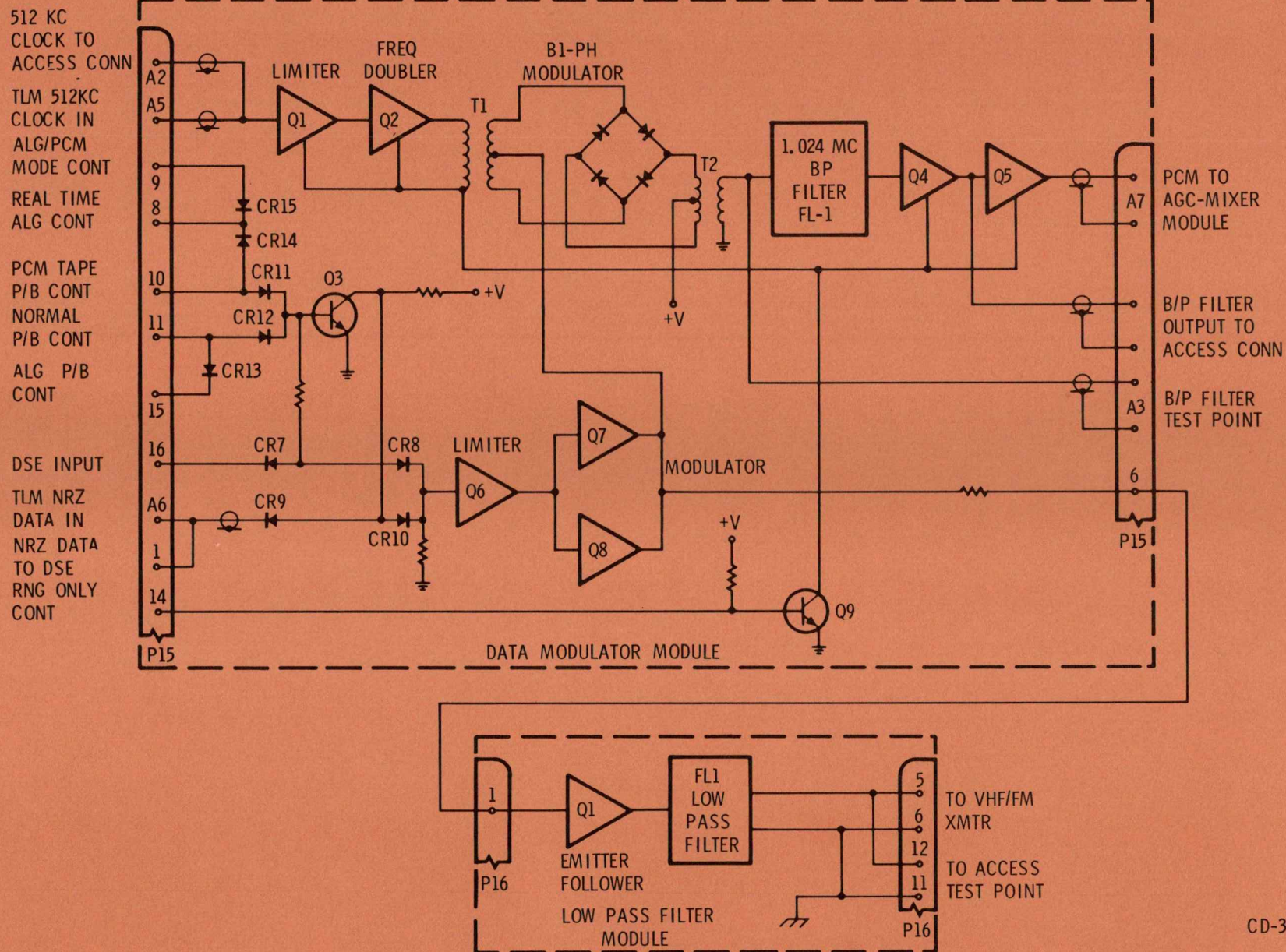


figure 10-5

signal in serial format in which a logic "zero" is 0 volts and a logic "one" is plus 6 volts. The input data signal at pin A6 is also connected to pin 1. Pin 1 is connected to the PCM data input stage of the Data Storage Equipment. The input impedance of the DSE is a minimum of 100 k ohms. With the DSE in the Record mode of operation, PCM telemetry data can simultaneously be recorded and transmitted real-time. CR9-10 are data switching diodes and are turned on by a positive voltage from the PMP regulated power supply. With CR9-10 turned on, real-time telemetry data is presented to the input of the limiter-amplifier stage Q6.

For playback PCM telemetry data from the DSE, mode control switches on the communications control panel provide a positive switching voltage at pins 10 and 11. With the TAPE-OFF-ANLG switch in the TAPE position, the Tape Recorder switch PLAY PCM-NORMAL-ANALOG is enabled. The PCM position applies plus 28 volts dc to pin 10. The NORMAL position applies plus 28 volts dc to pin 11. With plus 28 volts dc at pin 10, CR11 turns on applying base bias to Q3. Q3 turns on, turning off the real-time diode switches CR9-10 and enabling the playback diodes CR7-8. With the playback diodes CR7-8 on, the PCM telemetry data from the DSE is presented to the limiter-amplifier Q6.

The positive switching voltage at pin 10 also turns on CR14. With CR14 turned on, plus 28 vdc is presented to the real-time latching relays in the three oscillator modules so that real-time analog information will be sent simultaneously with recorded PCM telemetry data.

The NORMAL position of the switch

applies plus 28 volts dc to pin 11. The switching voltage at pin 11 turns on CR12. The turning on of CR12 performs the same functions as the turn on of CR11. The positive voltage at pin 11 also turns on CR13. With CR13 turned on, the plus 28 volts dc is applied to the playback latching relays in the three oscillator modules enabling them in the playback mode, so that playback analog information will be transmitted simultaneously with recorded PCM telemetry data.

The ANLG position of the Tape-Off-Analog switch applies plus 28 volts dc to pin 9, turning on CR15. With CR15 turned on, plus 28 volts dc is applied to the real-time analog latching relays in the oscillator modules enabling them in the real-time analog mode. This mode of operation also inhibits the PLAY PCM-NORMAL-ANALOG switch.

Either recorded or real-time PCM telemetry data is presented to the input of the amplitude-limiter Q6. The amplitude-limiter stage Q6 drives the modulator stage Q7-Q8. A logic "one" at the input of the limiter stage Q6 will turn on Q8 and logic "zero" at the input will turn on Q7. When Q8 is turned on for a logic "one", a ground is placed at the center tap of T1 and when Q7 is turned on for a logic "zero", plus 10 volts is placed at the center tap of T1. In this type of circuit configuration, one pair of diodes in the bi-phase modulator will conduct for a logic "one" and another pair of diodes will conduct for a logic "zero".

The PCM Telemetry Equipment also supplies a synchronous square-wave clock signal to the Data Modulator Module at pin A5. The clock signal has an amplitude of plus 6 volts with a 50 per cent duty cycle. The clock signal is passed through a limiter stage Q1 and a frequency doubler stage Q2.

The output of stage Q2 is a symmetrical sine wave signal at a frequency of 1.024 mc. The bi-phase modulator network will pass the 1.024 mc signal through to T2 with no change in phase for a logic "one" at the input of the limiter stage Q6 or will shift the phase of the 1.024 mc signal 180 degrees for a logic "zero" at the input of limiter stage Q6. The output of the bi-phase modulator is transformer coupled through the output transformer T2 to the band-pass filter FL1. The band-pass filter FL1 has a center frequency of 1.024 mc and a band-pass at the minus 3 db points from 949 to 1099 kc. The output of the band-pass filter is passed through a two-stage feedback amplifier Q4 and Q5. The phase shifted PCM telemetry data at pin A7 is connected to the input of the AGC Amplifier/Mixer Module at pin A7.

The modulators Q7 and Q8 also presents the PCM telemetry data to pin 6 of the output connector. The output at pin 6 is connected to the input connector of the Low Pass Filter Module at pin 1. The Low Pass Filter Module consists of an emitter follower stage Q1 and a low pass filter. The frequency response of the Low Pass Filter is from dc to 75 kc at the minus 3 db point with a maximally linear phase response. The PCM telemetry data signal at the output of the Low Pass Filter Module is 3 volts peak-to-peak with an output impedance of 3.3 k ohms. The output signal at terminals 5 and 6 are connected to the input stage of the VHF/FM Transmitter Equipment.

The PCM telemetry data channel composed of Q1, Q2, Bi-phase Modulator, Q4, and Q5 is activated by the application of the PMP power supply regulated voltage being applied to the base of Q9. The ground at the emitter of Q9 is the PMP power supply ground. The

limiter Q6 and the modulator ground is through the PCM Telemetry Equipment so that they can function even when switch Q9 is turned off. The RNG-OFF-RNG ONLY switch when activated in the RNG ONLY position will supply a ground to pin 14, thereby, turning off Q9. With the transistor switch Q9 turned off, the PCM data channel is disabled. PCM telemetry data may still be transmitted to the ground MSFN stations via the VHF/FM Transmitter Equipment.

10.13.2 Voice Mode of Communications

See Figure 10-6. S-band voice communications to the MSFN ground stations is possible in all modes except Emergency Key. For normal S-band communications the VOICE-NORMAL-KEY switch is placed in the NORMAL position. In this mode of operation, the emergency/normal voice relay in the Speech Clipper Module is energized by the application of plus 28 volts dc at pin 12 to the coil of relay K1. When K1 is energized, the audio output of the Speech Clipper Module (pins 13 and 14) is routed to the input of the FM Voice Modulator Module at pins 1 and 2.

The voice signals from the Audio Center are routed to the input of the Speech Clipper Module in the PMP. The input voice signal is 300 to 3000 cps at 1.1 volts peak nominal. The Speech Clipper stages Q1 and Q2 will provide 9 db of clipping at a voltage signal input of 0.73 volts peak. The output of the last stage of the clipper amplifier Q2 is transformer coupled to the arms of the emergency/normal voice relay K1. When K1 is energized as in the normal voice mode or de-energized as in the emergency voice mode, the audio output signal is at a 0.485 to 0.555 peak-to-peak level. In the emergency voice mode, the output is routed to the FM input of the USBE. The Speech Clipper Module operates from the spacecraft primary

SPEECH CLIPPER & VOICE MODULATOR MODULES, PMP S14-019

BLOCK DIAGRAM

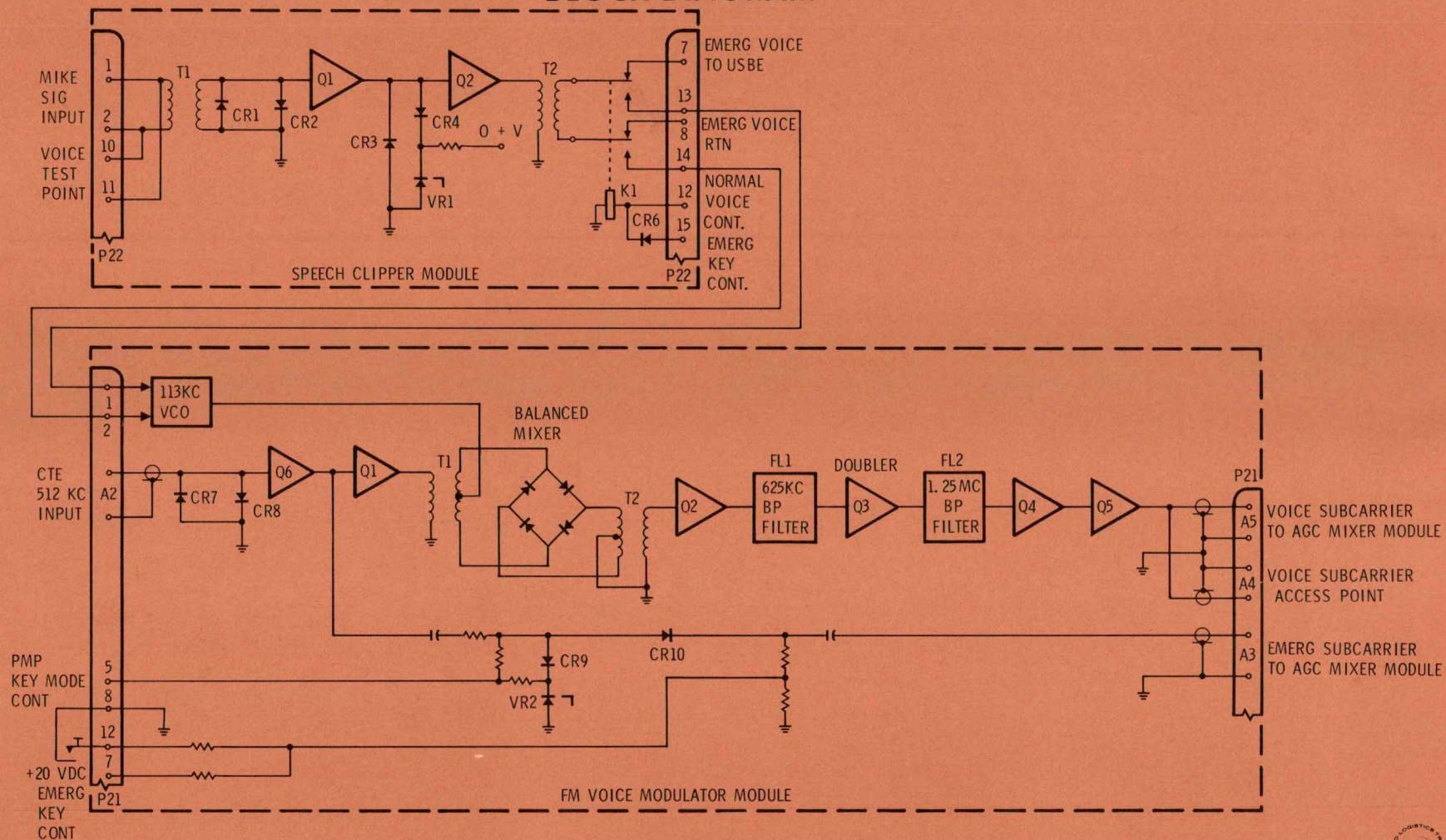


figure 10-6

plus 28 volt dc supply so is not affected when the PMP is turned off.

The center frequency of the voltage controlled oscillator (VCO) in the FM Modulator Module is nominally at 113 kc. The amplitude of the voice input signals from the Speech Clipper Module will cause the VCO to deviate around its center frequency. The modulation sensitivity of the VCO is 29 kc per volt peak input. The output of the VCO is applied to the center tap of T1, which is part of the balanced mixer circuit.

The Central Timing Equipment (CTE) supplies a 512 kc square-wave clock signal at pin A2 of the FM Voice Modulator Module. The clock signal is limited by CR7-8 and applied to a tuned amplifier stage Q6. The bias voltage for Q6 is from the spacecraft primary supply. The output of the tuned amplifier Q6 is a symmetrical sine wave at 512 kc. Q1 is used as an isolation stage and applies the clock signal to the primary of T1. The balanced mixer translates the VCO frequency of 113 kc into two new frequencies ($113 + 512 = 625$ kc and $512 - 113 = 399$ kc). These two new frequencies are called the upper and lower sidebands respectively. Stage Q2 presents the signals to a band-pass filter FL1. The band-pass filter accepts the upper sideband frequency of 625 kc but rejects the lower sideband frequency of 399 kc. The 625 kc output of the band-pass filter is applied to a frequency doubler stage Q3. The output of the frequency doubler stage is a new frequency of 1.25 mc. Band-pass filter FL2 accepts and passes the 1.25 mc. signal but rejects all others. The output of band-pass filter FL2 is passed through a two stage feedback amplifier (Q4-Q5) to the output of

the module. The 1.25 mc voice subcarrier at pin A5 is connected to the input connector of the AGC Amplifier/Mixer Module at pin A5.

10.13.3 Emergency Key Mode of Communications

See Figure 10-6. For emergency key mode of operation, the 512 kc clock signal at A2 from the CTE is required, the VOICE-NORMAL-KEY switch on the communications control panel placed in the KEY mode, and the emergency key switch on the astronaut's umbilical must be closed. The KEY position applies plus 28 volts dc from the spacecraft primary power supply to pin 5 of the FM Voice Modulator Module. The plus 20 volts dc applied at pin 12 is applied to a voltage divider network that keeps CR10, the keying diode, back biased off. The key is connected to pin 7. When the key is closed, applying a ground to pin 7, a resistor is placed in parallel with the original voltage divider resistor to forward bias CR10 to the on condition. When CR10 is biased on, the 512 kc sine wave from the tuned amplifier Q6 is applied to the output connector at A3. The 512 kc keyed signal at pin A3 is connected to the input connector of the AGC Amplifier/Mixer Module at pin A2.

10.13.4 Mixing and Switching Network (Figure 10-7)

The AGC Amplifier/Mixer Module provides the linear mixing, switching, and routing of the following inputs:

- a. TV signals
- b. PCM telemetry subcarrier
- c. Biomed signals
- d. Voice subcarrier
- e. Nine subcarrier oscillators
- f. Emergency key subcarrier

AGC-MIXER MODULE, 960C-1

BLOCK DIAGRAM

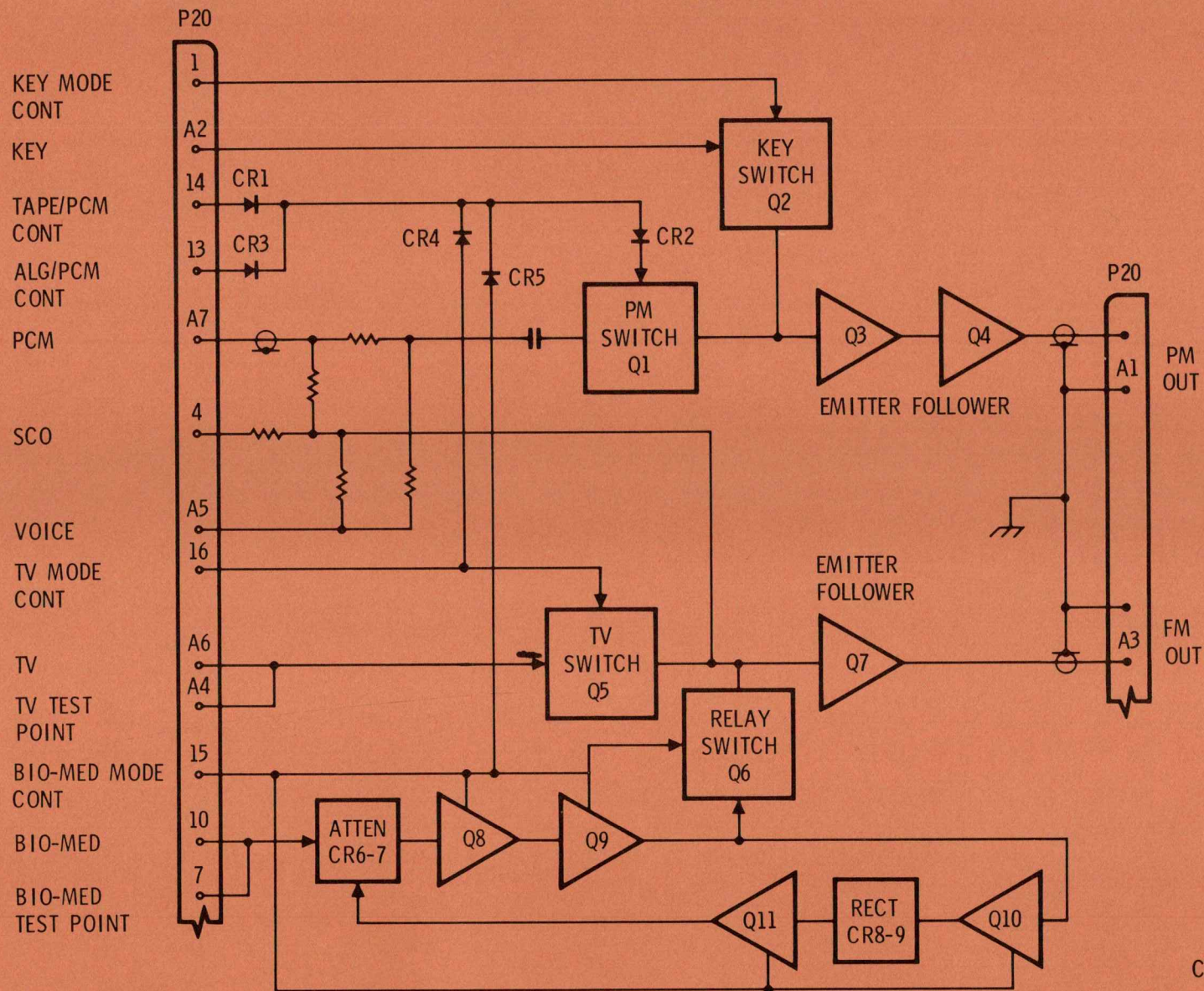


figure 10-7

The output signals of the AGC Amplifier/Mixer Module to the input stages of the unified S-band equipment is either a phase modulated signal input or a frequency modulated signal input.

The modes of operation in the AGC Amplifier/Mixer Module are controlled by the TV-OFF-PLSS or the TAPE-OFF-ANLG or the EMERG VOICE-NORMAL-KEY switches on the communications control panel. With the two normal S-band switches in the OFF position and the VOICE NORMAL KEY switch in the NORMAL position, PM mode switch Q1 is normally on. With PM switch Q1 in the on condition, the voice subcarrier at A5 and the PCM data subcarrier at pin A7 are routed to the output emitter follower stages Q3-Q4 to the output connector at A1. The signals at A1 are routed to the PM input of the USBE.

When the two S-band normal switches are in any mode but off, the input logic to the PM switch Q1 is comparable to a four input OR gate with CR1, CR3, CR4, and CR5 comprising the OR function. With the PM switch Q1 in the off mode, the PCM data and the voice subcarriers are routed to the input of the FM mixing network (Q7).

The biomed data from the VHF/AM Receiver is presented at pin 10 of the input connector. The biomed switch (relay switch Q6) is turned on when the TV-PLSS switch is placed in the PLSS mode. This also applies the bias voltage to the biomed amplifiers and AGC network. The biomed information is passed through an input attenuator network CR6-7 that is controlled by an AGC amplifier Q11. The biomed signals at the output of stage Q9 is conducted through relay switch Q6 to the FM mixing network Q7. The FM output at A3 is presented to the FM input of the USBE.

The FM outputs are:

- | | | |
|-----------|----------------|-----------------------|
| a. PCM | 1.024 mc | 0.466 \pm 0.03v p-p |
| b. Voice | 1.250 mc | 0.532 \pm 0.02v p-p |
| c. SCO's | 14.5 to 165 kc | 0.135 \pm 0.01v p-p |
| d. TV | .04 to 500 kc | 1.133 \pm 0.14v p-p |
| e. Biomed | 4 to 12 kc | 0.406 \pm 0.01v p-p |

The PM outputs are:

- | | | |
|----------|----------|----------------------|
| a. PCM | 1.024 mc | 2.2 \pm 0.1 v p-p |
| b. Voice | 1.250 mc | 1.68 \pm 0.08v p-p |
| c. Key | 512 kc | 2.2 \pm 0.1 v p-p |

The KEY position turns on key switch Q2. The 512 kc keyed subcarrier from the FM Voice Modulator Module at A2 is applied to the output connector at A1 through the emitter follower stages Q3 and Q4. The KEY mode turned off the PMP power supply; thereby, inhibiting the PCM, TV, SCO, and biomed inputs.

10.13.5 Analog Mode of Communications (Figure 10-8)

The selection of ANALOG 1 (channels 1 through 9) or ANALOG 2 (channels 10 through 18) is performed in relay modules one and two. The nine selected channels can also be routed to the Data Storage Equipment when the Tape Recorder switch RECORD-OFF-PLAY is activated in the RECORD position. Relay module one has three latching type relays. Two of these relays (K1 and K3) are used for selecting either channels one through six or channels ten through fifteen. Relay K2 is used for routing channels one through three to the DSE and the af-rf oscillator modules. Channels four through six are routed to relay module two. Relay module two is also composed of three latching type relays. Relay K1 selects

RELAY & S.C.OSC MODULES, PMP

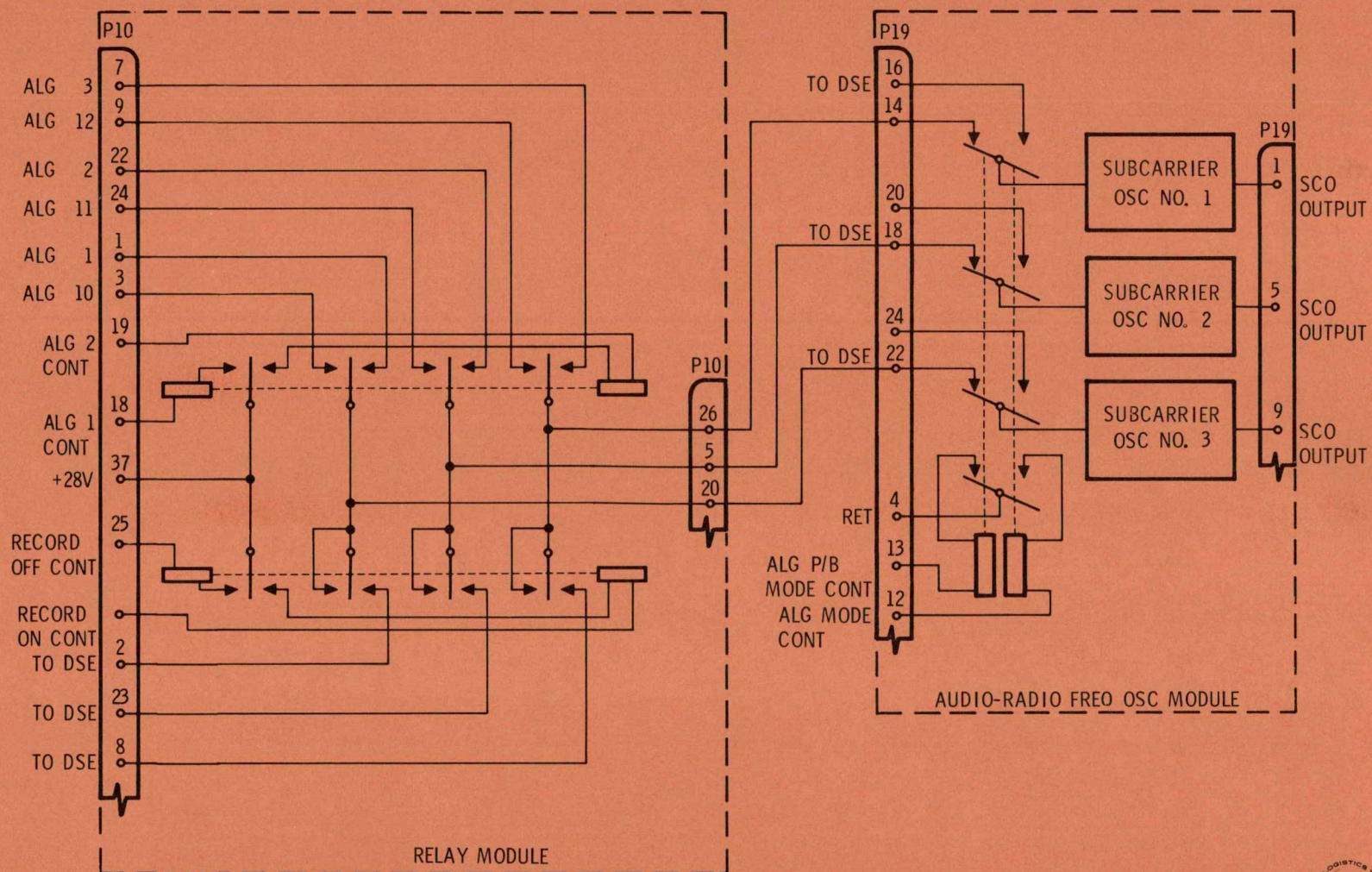



figure 10-8

SUBCARRIER OSCILLATOR CHARACTERISTICS

OSC. NO.	LOW FREQ. LIMIT	CENTER FREQ. f_c	UPPER FREQ. LIMIT	Δf	MAX. MOD. FREQ.	% DEV. OF f_c
1	13,412	14,500	15,588	1,088	435	$\pm 7.5\%$
2	20,350	22,000	23,650	1,650	660	$\pm 7.5\%$
3	27,750	30,000	32,250	2,250	895	$\pm 7.5\%$
4	37,000	40,000	43,000	3,000	1,200	$\pm 7.5\%$
5	48,562	52,500	56,438	3,938	1,575	$\pm 7.5\%$
6	64,750	70,000	75,250	5,250	2,100	$\pm 7.5\%$
7	87,875	95,000	102,125	7,125	2,850	$\pm 7.5\%$
8	115,625	125,000	134,375	9,375	3,750	$\pm 7.5\%$
9	152,625	165,000	177,375	12,375	4,950	$\pm 7.5\%$

TABLE 10-1

CD-1007 

either analog channels eight through ten or 16 through 18. Relay K2 is used for routing channels eight through ten or 16 through 18 to the DSE and to the af-rf oscillator modules. Relay K3 is used for routing channels four through six to the DSE and to the af-rf oscillator modules. Analog information can be recorded at the Data Storage Equipment and sent real-time to the MSFN ground stations simultaneously.

There are three identical (except for frequency) af-rf oscillator modules located in the PMP. Each of these modules contains three subcarrier oscillators, with each oscillator having a different center frequency. Latching relay logic, contained in each module, determines whether the real-time analog input information or the recorded analog information from the Data Storage Equipment will be used to modulate the subcarrier oscillators. The logic arrangement will not permit transmission of recorded and real-time analog information simultaneously. The latching relay logic functions only on that group of nine analog inputs previously selected by the switching logic in the relay modules.

The modulation characteristics of the SCO's is such that a zero amplitude analog signal input produces a deviation of minus 7.5%. A plus 5 volt amplitude analog signal produces a deviation of plus 7.5%.

Table 10-1 lists the characteristics of the SCO's. For example, in channel one, a zero voltage input signal will change the 14,500 cps to 13,412 cps and a plus 5 volt signal will change the 14,500 cps to 15,588 cps. The output filter characteristics of each SCO is such that

attenuation is 10 db or greater at all frequencies equal to or greater than $1.2 f_c$ and equal to or less than $0.8 f_c$. The attenuation of all signals greater than $2 f_c$ is 40 db. The output of each SCO is a sine wave at a level of 0.707 volts peak into a resistive load of 5.11 k ohms. The nine outputs of the subcarrier oscillators are sent simultaneously to the FM mixing network in the AGC Amplifier/Mixer Module. The mixing network linearly combines these inputs into a complex wave along with the PCM telemetry subcarrier and the voice subcarrier, and routed to the FM input of the USBE for transmission to the ground MSFN stations.

10.13.6 Up-Voice and Up-Data Communications

See Figure 10-9. A frequency modulated up-voice signal at 30 kc is accepted from the USBE receiver by the FM Voice Discriminator Module. The input dynamic range of the FM Discriminator Module is from 0.2 to 5.0 volts peak with a nominal peak input of 1.0 volt. The input stage is a band-pass filter with a center frequency of 30 kc. The filter has a 20 kc band-pass that is down 3 db at 20 kc and 40 kc. From the band-pass filter the signal passes through a two stage limiter amplifier Q1 and Q2. The amplitude limited signal out of Q2 drives a monostable multivibrator stage Q3-Q4. The multivibrator provides constant amplitude and width pulses, with variable spacings between pulses, that are synchronized with the FM input signal. FL-2 is a Low Pass Filter which rejects the 30 kc component, but passes the integrated spacing changes. The changes are identical to the frequency modulation. The Low Pass Filter is a constant amplitude type filter with a flat response from 300 to 3000 cps. The output of the Low Pass Filter is then fed through two amplifiers (Q5-Q6) which boost the audio signal to a usable level. The output voltage to the Audio Center Equipment is 1.13 volts into a

balanced 18 k ohm load for a deviation of 7.5 kc.

Power to operate the up-voice and up-data discriminators is the spacecraft plus 28 volt supply. With this configuration, the PMP power supply could be turned off and the two discriminators would still operate to supply voice and data signals.

The operation of the up-data discriminator is basically identical to the operation of the up-voice discriminator except the input band-pass filter has a center frequency of 70 kc. The filter has a flat response from 60 to 80 kc at the minus 3 db points. The output of the up-data discriminator is to the UDL decoder package.

FM VOICE & FM DATA DETECTORS, PMP

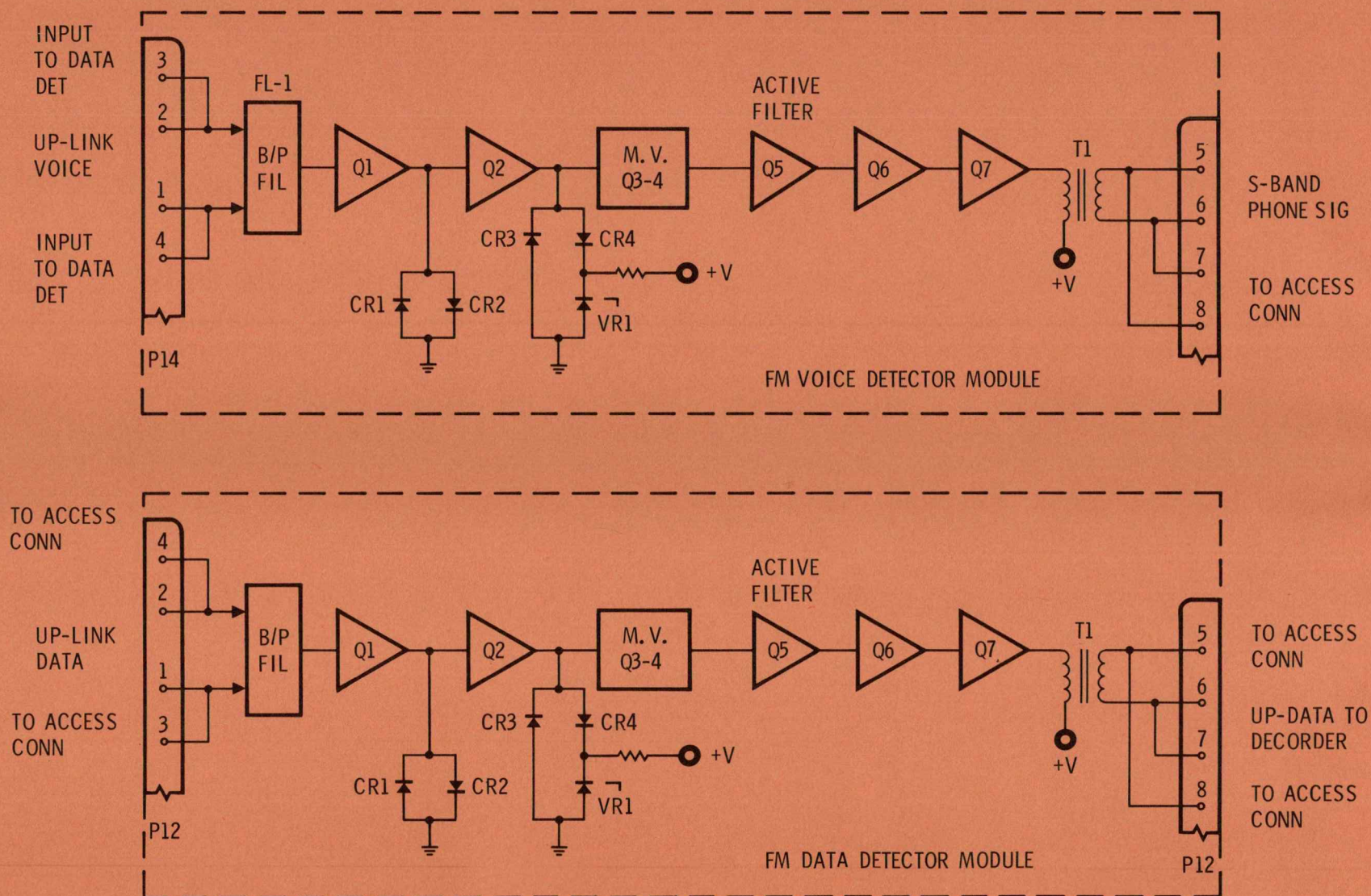


figure 10-9

CD-325 A



PMP POWER SUPPLY MODULE

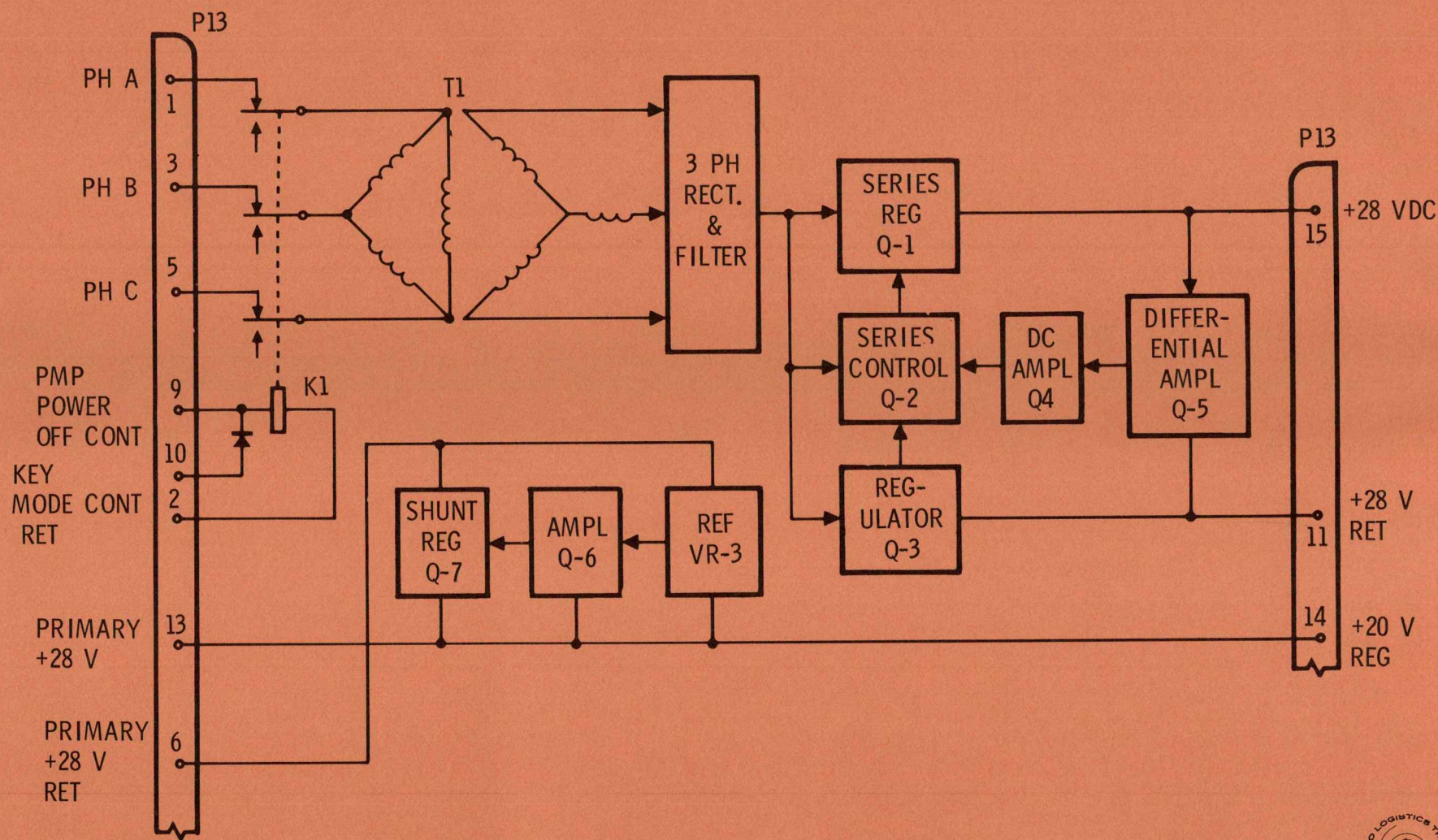


figure 10-10

SECTION XI

VHF/FM TRANSMITTER

The VHF/FM Transmitter, figure 11-1, is used to provide PCM telemetry data to ground receiving stations during launch, earth orbit, and the early phases of translunar injection.

INTRODUCTION

The input to the VHF/FM Transmitter is 51,200 or 1600 bits per second nrz data at a constant amplitude of three volts peak from zero volts reference. Because of the non-return-to-zero characteristic of the incoming data, the effective frequency may vary from 20 cps to 50 kc. The transmitter has a 3 db bandwidth of less than 500 kc. The carrier components more than 500 kc from the center carrier frequency will be down at least 55 db from the unmodulated carrier power level. In a system with a given bandwidth the maximum allowable deviation is one fourth of that bandwidth. Any deviation in excess of this will result in distortion of the information signal. In the case of the VHF/FM Transmitter, the bandwidth is 500 kc; therefore, the maximum deviation of the carrier signal will be 125 kc in either direction. For a given maximum deviation in carrier frequency, a broader bandwidth will be required for higher input frequencies. The modulation index is an expression of the ratio of peak deviation to highest modulating frequency. The modulation index, with peak deviation, will vary from 6250, at 20 cps, to 2.5, at 50 kc.

The transmitter operates at a center frequency of 237.8 mc. An input modulation signal of +3 volts will cause a deviation of +125 kc in the output frequency, while an input of 0 volts will cause a deviation of -125 kc.

The VHF/FM Transmitter requires an input of 35 watts of power to transmit 10 watts through the antenna.

BLOCK DIAGRAM OPERATION

The 0 to 3 volt signal is sent through a blocking capacitor to convert the signal from a pulsating dc to an ac. The signal at this point is sent to the varicaps as shown in figure 11-1. A varicap is a silicon P-N junction device designed for use as a voltage controlled variable capacitor. The varicap provides a means of changing circuit capacitance through bias voltage control, and thereby, controlling the L-C oscillator's frequency output. By this method, the unmodulated output of the L-C oscillator, 9.9083 mc, will be varied by 5.208 kc in either direction by the modulating signal's positive and negative extreme.

The frequency modulated output from the L-C oscillator then passes through a buffer amplifier stage to an X_4 frequency multiplier, where the fourth harmonic is removed and fed into a frequency tripler. In this stage, the third harmonic of the signal is removed and fed into a frequency doubler and then through two amplifier stages. The frequency at this point is 237.8 megacycles, and the power level has been increased from 10 milliwatts to 2.0 watts.

This signal drives the power amplifier which, with its 7.2 decibel gain, gives a power output of 14.0 watts. This output goes to the 50 Ω load of the vhf antenna after first passing through an LP filter and detector employed to obtain an analog signal for monitoring the output power. The power to the antenna drops to 13.4 watts due to an insertion loss of 0.2 decibels for the

VHF/FM TRANSMITTER

11

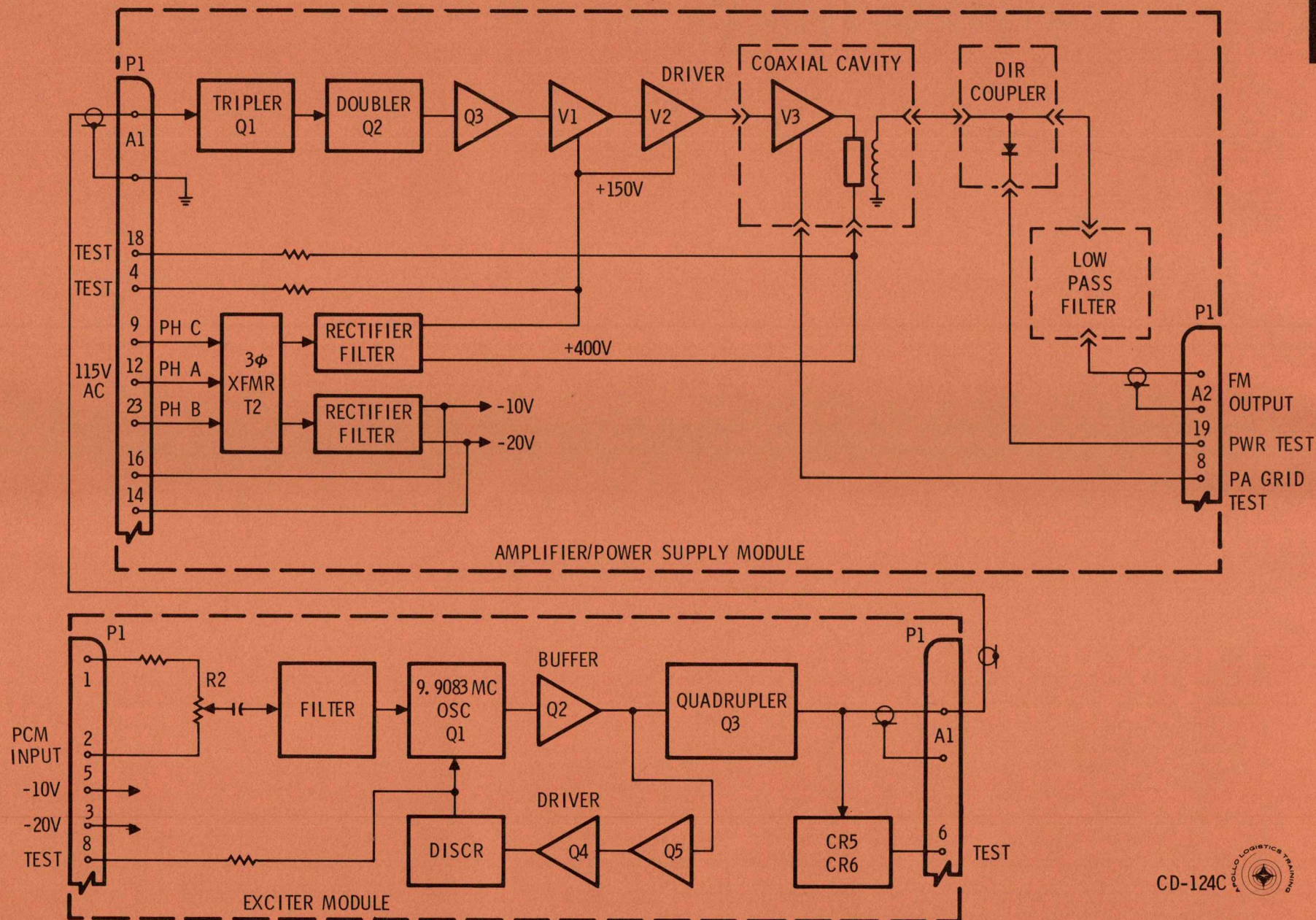


Figure 11-1

CD-124C



low-pass filter and detector circuitry.

A feedback loop from the output of the buffer amplifier to the varicaps associated with the carrier oscillator (which consists of an amplifier stage, a discriminator driver, and a crystal discriminator) is used to apply a biasing voltage to the varicap in the event that the carrier oscillator tends to drift off frequency, thereby ensuring automatic frequency control.

Components used throughout the transmitter are solid-state devices with the exception of the final power amplifier PA stage, which is a planar triode cavity amplifier, and the two preceding amplifier stages, which are subminiature triodes.

The transmitter power supply operates from a 115/200 volt, 400 cycle, three phase source. The line voltage is stepped down by a three phase transformer, and after rectification and filtering, the required inputs are supplied to the transmitter.

The unmodulated carrier frequency of the VHF/FM Transmitter will not vary more than ± 0.003 percent of the specified carrier center frequency.

The VHF/FM Transmitter shares a common chassis with the HF tranceiver. The space allocated to the VHF/FM Transmitter, not including connectors, measures 12 inches by 4.7 inches by 5.79 inches.

SECTION XII

UNIFIED S-BAND EQUIPMENT 621F-1E

12.1 INTRODUCTION

The primary function of the Unified S-Band Equipment (USBE) is to provide deep-space communications for the Apollo spacecraft, both to and from MSFN. The equipment also provides for the reception and retransmission of a pseudo-random-noise (PRN) code for turn-around ranging by the MSFN stations. The relative motion of the spacecraft is accomplished by the measurement of the double doppler frequency shifts.

The Unified-S-band equipment is a narrowband, double conversion superhetrodyne, automatic phase-tracking receiver that accepts a 2106.4 megacycle rf input signal and an integrally-related transmitter with a propagation frequency of 2287.5 megacycles. The equipment also includes a dc power supply that utilizes the spacecraft 115 vac, 400 cps power to provide plus 15 vdc and minus 15 vdc for receiver and transmitter operation.

The design of the equipment provides two types of configuration, single and dual. In the single configuration there are three removable active modules (a) receiver, (b) transmitter, and (c) power supply, plus three dummy modules. In the dual configuration there are six removable modules (a) two receivers, (b) two transmitters, and (c) two power supplies. In the present configuration the three spare modules are activated electrically by removing the front panel from one end of the equipment chassis and installing it on the opposite end.

12.2 LEADING PARTICULARS

- a. Over-all Dimensions:
 - 1. Width 10 3/10 in.
 - 2. Height 5 3/4 in.
 - 3. Length 24 inches
- b. Weight 30 pounds
- c. Power Requirements
 - 1. 115 vac, 4 wire, 400 cps
 - 2. 16 watts
- d. Input Frequency 2106.40625 mc.
- e. Static Phase Error
 - 1. Not greater than ± 6 degrees
- f. Output Frequency 2287.5 mc.

12.3 TRACKING SYSTEM

The tracking system is built around a reference servo receiver which uses an automatic phase control servo called the phase locked loop. In this servo system, the phase of a local oscillator (VCO) signal is automatically adjusted to be in phase with the input rf signal, within an acceptable error range. The automatic phase servo system is designed to provide unusually narrow bandpass filtering for signals whose frequency may vary over a range many times greater than the filter passband. Thus, in

order to find the signal in the noise, only a "slice" of the incoming frequency is used.

Measurement of the apparent doppler frequency shift is probably the most useful information for accurately determining the trajectory of the spacecraft, particularly at long ranges after powered maneuvers. Both the one-way and the two-way doppler techniques can be employed by the MSFN stations. However, because of the lack of frequency stability (22.875 kc) in the spacecraft oscillator, the one-way technique is only used as a low accuracy backup measure. In the two-way doppler system, a stable carrier signal is transmitted to the spacecraft, where it is received by a phase locked receiver, filtered, frequency multiplied by a 221/240 ratio, and then retransmitted to the MSFN stations. At the MSFN stations, the return carrier is received by a reference automatic phase controlled receiver and compared with the transmitter signal, appropriately multiplied, to determine the doppler frequency shift. To achieve the required accuracy, complete phase matching, and consequently, frequency matching must be maintained by using phase locked oscillators.

In the ranging system an rf carrier from the ground transmitter is phase modulated by a ranging code. This is a pseudo-random (PRN) binary code, consisting of several code components, generated in the ground transmitter coder. The spacecraft turn-around unified S-band equipment regenerates the carrier (at a different frequency, up frequency 2106.4, down frequency 2287.5 mc) but not the code. The unified S-band equipment detects the code from the ground-to-spacecraft carrier and directly phase modulates the code on the spacecraft-to-ground carrier.

A local model of the range code is generated in the ground receiver coder and is fed to the ground rf receiver. By suitably delaying the receiver code it can be made to coincide in time with the code as received from the spacecraft. The delay which must be inserted is kept track of in a unit called the range tally. The length of this delay is then equal to the round trip signal transit time, and thus is a measure of the range. Once range acquisition has been accomplished, range measurements and readout are kept current by continually tallying in the doppler obtained on a submultiple of the received carrier frequency.

The ranging subsystem implements precision ranging on the turn-around spacecraft transponder. Two sets of codes are provided in the subsystem. The long code, which permits ranging on lunar and circumlunar missions, has a maximum unambiguous range of 800,000 km. The short code, which permits somewhat more rapid acquisition, is chosen for spacecraft ranging missions and has an unambiguous range of 10,000 km.

The transmitter coder generates pseudo-random binary code components of lengths 11, 31, 63, and 127 for long ranges, and of lengths 7, 11, 15, and 31 for short ranges. The components are combined in a fixed manner to yield total code lengths of 2,728,351 bits and 35,805 bits, respectively. They are also combined with a clock code of length 2 bits, which doubles their respective lengths.

The receiver coder generates the same code components as the transmitter coder. The receiver coder is synchronized to the transmitter coder at the beginning of range acquisition. In the course of this acquisition, the code components

in the receiver coder are shifted in time with respect to their counterparts in the transmitter coder until they coincide with the counterpart portion of the code received from the spacecraft.

12.4 SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

12.4.1 Receiver (See Figure 12-1)

The balanced mixer heterodynes the receiver input signal (2106.4 mc) with a local oscillator signal (2058.75 mc) producing an i-f signal of 47.656 mc which is supplied to the 47.656 mc preamplifier. The preamplifier produces an output signal at a level of -29 to -109 dbm, depending on the input signal level. The preamplifier output signal is then supplied to the agc-controlled 47.656 mc i-f amplifier. The i-f amplifier produces a constant -60 dbm output (due to agc action) to the second mixer.

The second mixer heterodynes the 47.656 mc signal with a 38.125 mc signal from the X2 multiplier. The resultant signal (9.531 mc) is coupled through an isolation amplifier to a wideband and a narrowband 9.531 mc amplifier.

The wideband 9.5 mc amplifier amplifies the 9.531 mc i-f signal to a level of 0 dbm. The signal is then applied to the range phase detector which detects the 9.531 mc i-f signal and supplies the subcarriers. In addition, a signal (ranging) is supplied to the gating circuits in the transmitter section. A phase adjustable reference signal is applied to the range phase detector through the variable phase shift network.

The narrowband circuit receives the 9.531 mc signal from the second mixer, filters and amplifies it to a +10 dbm level, then couples the signal

to the loop phase detector. An amplified 9.531 mc signal is also supplied to the agc detector at -6 dbm. The phase detector compares a characteristic of the incoming signal with a reference signal from the divide by two multiplier. The detected dc output signal is used to control the frequency of the 19.0625 mc vco. The total loop is designed for a 318 cps bandwidth at threshold.

The voltage controlled oscillator generates a 19.0625 mc signal for use by other receiver circuits. Though crystal controlled, the oscillator frequency varies over a small range due to the action of the dc voltage from the loop phase detector. The change in net bias detunes the loop from resonance and creates a phase shift which causes the frequency to shift from the resonance point of the crystal. The 19.0625 mc vco output signal is applied to the divide-by-two frequency divider, the X2 multiplier, and the gating circuits in the transmitter section.

The divide-by-two frequency divider develops three 9.531 mc reference signals; two in phase and one displaced by 90 degrees. One reference signal is applied to the agc phase detector, one is applied to the range phase detector, and the third to the loop phase detector. The agc phase detector compares the reference signal with the signal from the 9.531 mc i-f amplifier and develops a dc output voltage proportional to the amplitude of the input signal. This output voltage is amplified and filtered, then applied to the 47.656 mc i-f amplifiers to become the receiver agc voltage.

12.4.2 Transmitter (See Figure 12-2)

The initial signal for transmitter operation is generated in one of two oscillators. The

621F-1E UNIFIED S-BAND RECEIVER

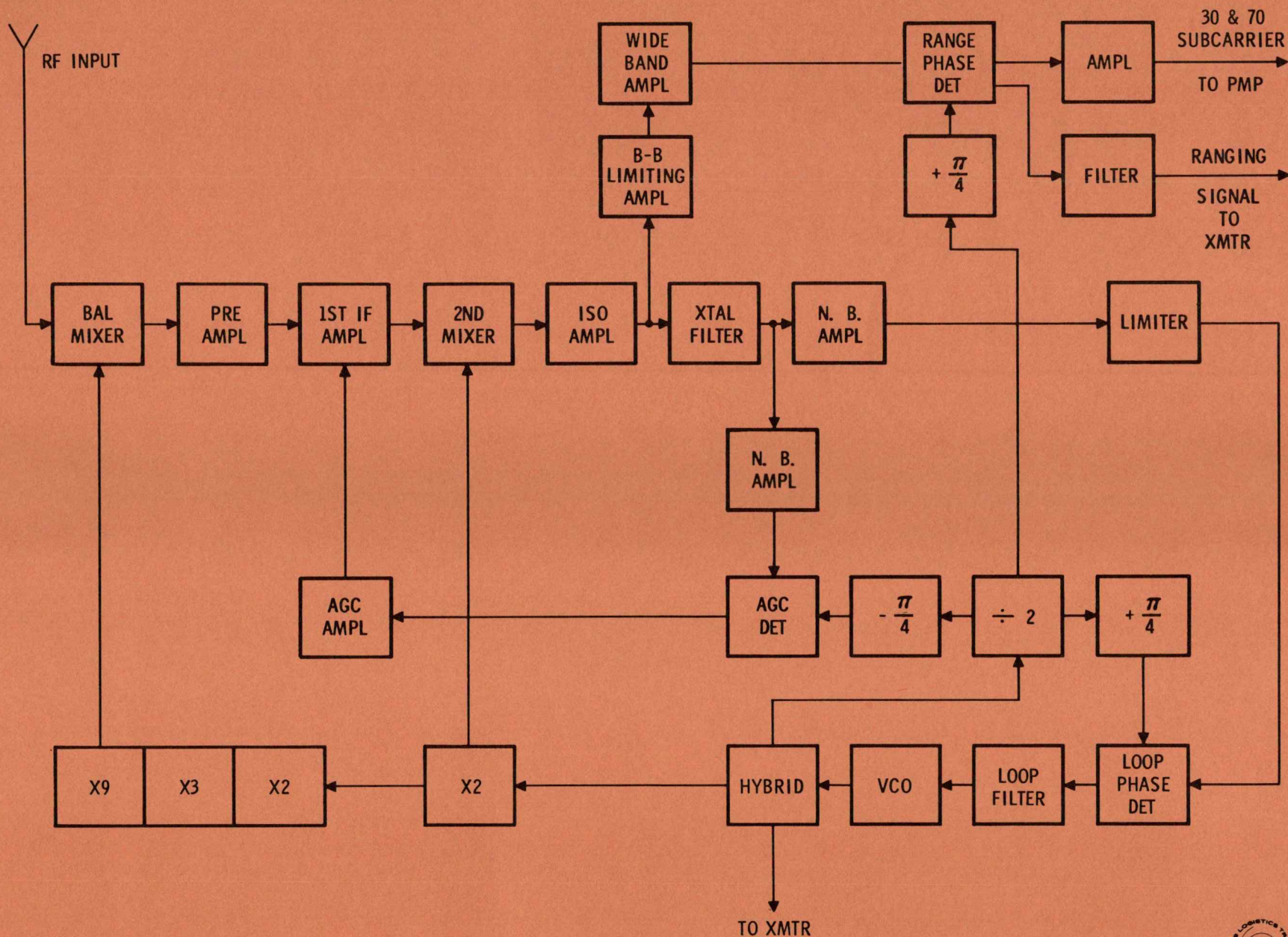


figure 12-1

621F-1E UNIFIED S-BAND TRANSMITTER

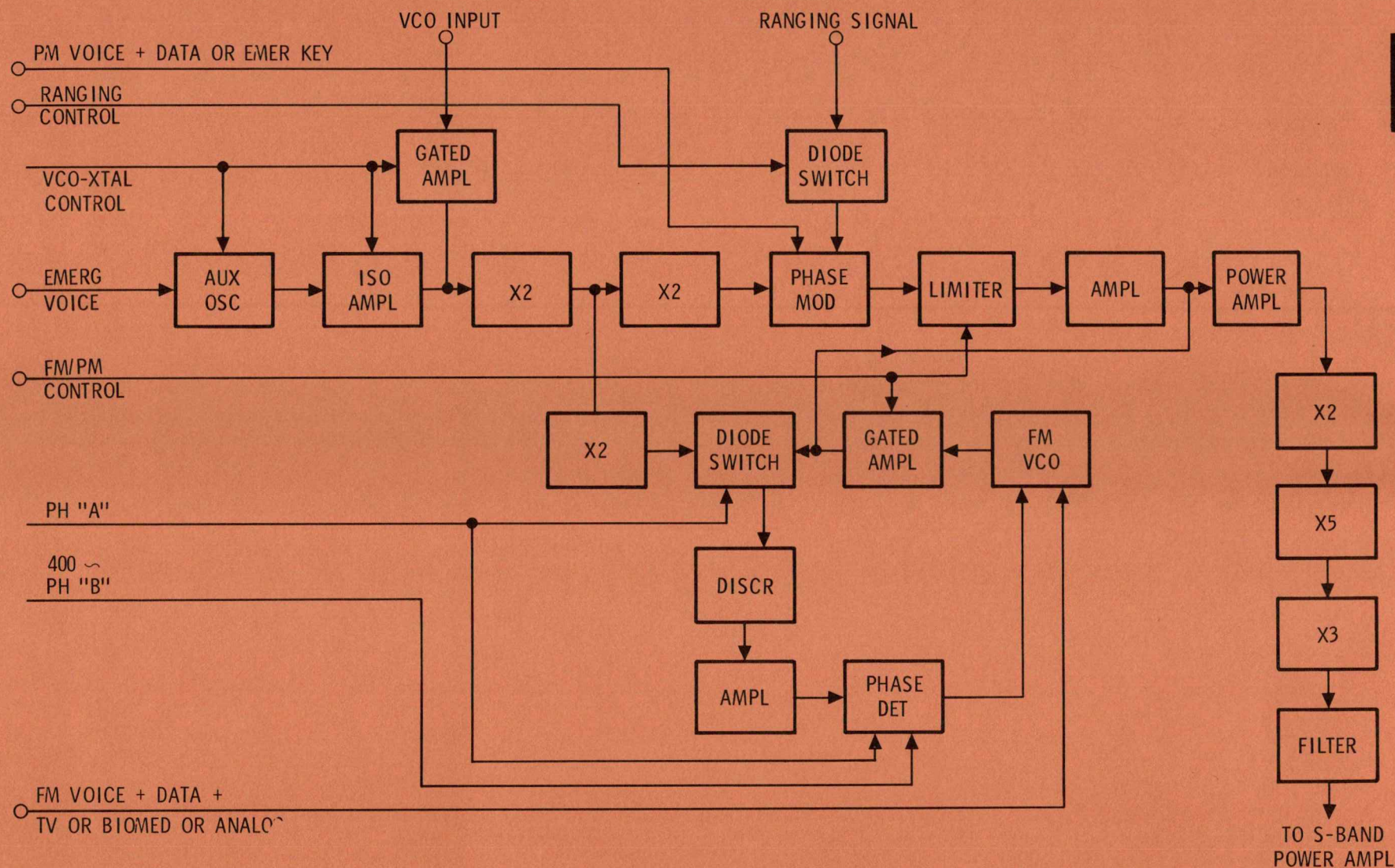


figure 12-2

first is located in the receiver module (receiver vco), and the second (auxiliary oscillator) is located in the transmitter module. Both operate at a frequency of 19.0625 mc. The PRI/SEC OSC Control selects the oscillator to be used. If this control is in the PRI position, the receiver vco is selected. The gated amplifier passes the receiver vco 19.0625 mc signal to the X2 multiplier and isolation amplifier, and the auxiliary vco is turned off. The signal is multiplied by two in the X2 multiplier. When the auxiliary oscillator is selected, the PRI/SEC OSC Control cuts off the gated amplifier, and starts the auxiliary oscillator. This signal is supplied to the X2 multiplier where it is multiplied to a frequency of 38.125 mc. In the SEC (auxiliary oscillator) mode, emergency voice modulation may be applied as a narrowband FM modulation.

Depending upon the setting of the controls on the communications control panel 20, the signal from the X2 multiplier may take one of two paths; (1) to the X2 multiplier and wideband phase modulator, or (2) to the X2 multiplier and gated diode network. The signal applied to the X2 multiplier and wideband phase modulator is multiplied by two, phase modulated, then passed to the power amplifier through a limiter. The signal frequency is now 76.25 mc. The signal applied to the X2 multiplier and gated diode circuit is multiplied to a frequency of 76.25 mc. The gating signal for the diode network is provided by the 400 cps reference signal. From the gated circuit, the 76.250 mc signal is applied through a limiter and isolation amplifier to the input of the FM discriminator. The detected ac signal from the FM discriminator is applied to a phase detector through a 400 cps ac amplifier. In the phase detector, the signal is phase compared with the 400 cps rf gating signal. The output of the phase detector is then applied

to a loop filter. From the loop filter, the signal is applied to the varactors of the FM oscillator. Frequency modulation from the video amplifier may be applied to the FM oscillator varactors.

The signal from the FM oscillator is applied to two circuits. The first circuit is the FM afc loop. In the second circuit, the signal from the FM oscillator is applied to the summing network, and then to the power amplifier. When the frequency modulator (FM oscillator) is not being used, a 76.250 mc signal is applied to the summing network from the X2 multiplier and wideband phase modulator. From the summing network, either signal is passed to the power amplifier.

From the phase modulator, the signal is passed to an isolation amplifier which isolates the frequency modulator and phase modulator from the power amplifier. The signal from the isolation amplifier is at a frequency of 76.250 mc. From the isolation amplifier, the 76.250 mc signal is applied to the power amplifier stage. The signal is amplified in the power amplifier stages and applied to the X2 multiplier where it is multiplied by two. It is then applied to an X5 varactor multiplier, multiplied by 5, and passed to an X3 varactor multiplier. Here the signal is multiplied by 3 and coupled to a 20 db load isolator. The signal is now at a frequency of 2287.5 mc. From the load isolator, the signal is passed through a bandpass filter to a power sampler and to the rf output connection. The power sampler provides a means of sampling the output power of the transmitter. The rf output signal is +24.5 dbm at 2287.5 mc.

12.4.3 Power Supply

The power supply for the Uniried S-Band Equipment consists of a power transformer, rectifiers, and associated filters. The input to the

power supply is 115 volts, 400 cps, three phase. An output of 400 cps is applied to the frequency modulator for gating purposes. The voltages supplied from the power supply are +15 vdc and -15 vdc.

12.5 DETAILED FUNCTION BLOCK DIAGRAM

12.5.1 Receiver (See Figure 12-3)

The Unified S-Band Equipment is designed to provide frequency modulation (FM) and phase modulation (PM) transmission at a frequency of 2287.5 megacycles and also provides coherent reception at 2106.40625 mc. The equipment accepts outputs from the Premodulation Processor Equipment and the S-Band Power Amplifier Equipment and also provides inputs to the S-Band Power Amplifier Equipment. The Unified S-Band Equipment is remotely controlled from Communications Control Panel 20. The Unified S-Band Equipment is completely solid state.

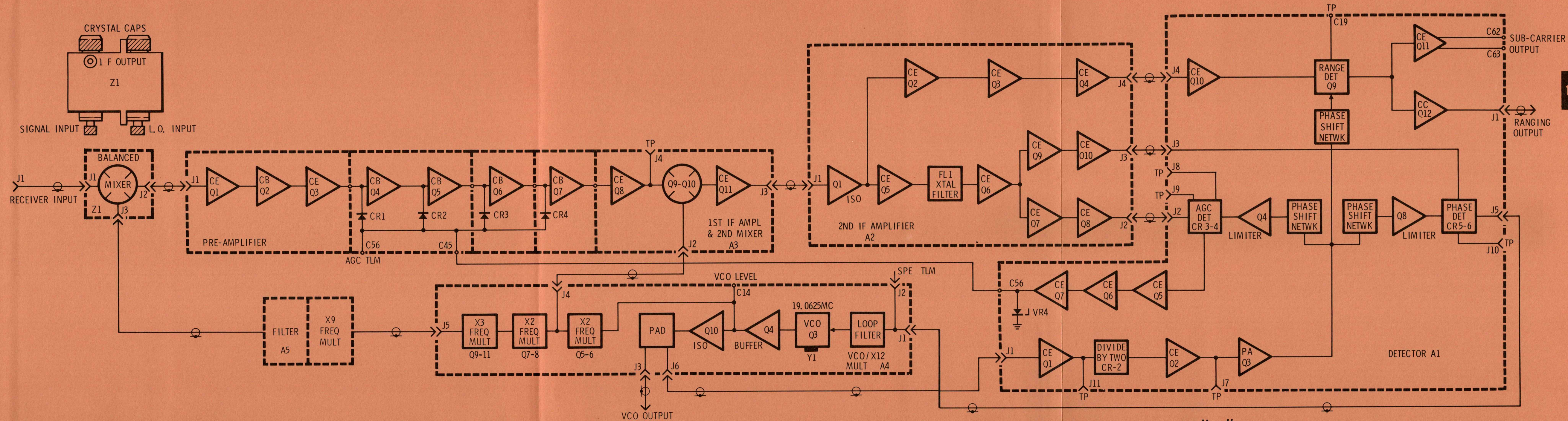
The phase modulated (PM) rf signal from the ground MSFN station is applied to the input rf connector of the spacecraft receiver, via the diplexer in the S-Band Power Amplifier Equipment. The diplexer permits the transmitter and receiver of the unified S-Band equipment to operate simultaneously from the same antenna without interference. The receiver arm and the transmitter arm of the diplexer have an isolation of 60 db minimum. The receivers nominal input carrier frequency is 2106.40625 mc (2287.5 mc times 221/240). The input impedance is 50 plus or minus 5 ohms with a voltage standing wave ratio (VSWR) of less than 1.5:1.

The receiver threshold signal level under which the unified S-Band receiver can maintain reliable phase coherence between the input signal and the transmitted output level -132.5 dbm. From the

input r-f connector the signal is applied to the input of the balanced mixer stage. The balanced mixer stage is in a self-contained package, utilizing matched crystals. The frequency response of the receiver front end is quite broad to accommodate the expected doppler shift in the r-f signals received from the MSFN ground stations. The balanced mixer converts the received 2106.40625 mc signal, with a local oscillator injection signal of 2058.75 mc, to the first i-f amplifier center frequency of 47.656 mc. The balanced mixer circuit has an r-f to i-f conversion loss of approximately 7 db.

The 47.656 mc i-f signal from the balanced mixer stage is applied to a three stage cascode preamplifier, Q1, Q2, and Q3. The preamplifier provides an i-f gain of 35 db, and a bandwidth of approximately 15 mc with a noise figure (NF) of not greater than 11 db. Noise figure is defined as the ratio of the available signal-to-noise ratio at the preamplifier output terminal.

The 47.656 mc i-f signal from the preamplifier is applied to the input of the first i-f amplifier. The 47.656 mc i-f amplifier section contains a four stage agc gain controlled wideband amplifier, consisting of Q4, Q5, Q6, and Q7, a single stage amplifier Q8, a balanced mixer Q9 and Q10, and an output amplifier stage Q11. The transistor balanced mixer, with an injection frequency of 38.125 mc, furnishes an output signal of 9.531 mc to the second i-f amplifier. The conversion gain from 47.656 mc to the second i-f amplifier frequency of 9.531 mc is controllable over the range from +40 db to -40 db with an agc voltage of 0 to -4 volts dc. When the agc voltage is -4 vdc, each amplifier has a gain of approximately 10 db. When the agc voltage is at a -1 vdc, each amplifier has a dynamic range of about 10 db. Thus the first i-f amplifier has a dynamic range of 80 db. This dynamic range compensates



UNIFIED S-BAND RECEIVER, "D" MODEL

Figure 12-3

for the expected signal level at the input to the balanced mixer which is from -132 dbm to -52 dbm. The 3 db bandwidth of the first i-f amplifier and second mixer is 6.0 mc. The 3 db points on the i-f amplifier bandwidth is 3.0 mc from the center frequency of 47.656 mc. The phase shift between the input and output of the first i-f amplifier varies linearly within plus or minus 3 degrees over the input frequency range from 45.94 mc to 49.37 mc. A plot of the phase shift versus frequency for the i-f amplifier shows it poses odd symmetry about 0 degrees at 47.656 mc within plus or minus 10 degrees.

The second i-f amplifier provides sufficient amplification to drive the phase, agc, and range detectors. The second i-f amplifier is basically a three channel device, operating at a center frequency of 9.531 mc. The three channels consist of a wideband amplifier, a narrow band linear amplifier, and a narrow band limiter amplifier. Q1 is an isolation amplifier used as an impedance match from the output of the first i-f amplifier to the input of the second i-f amplifier sections. The wideband amplifier channel consists of Q2, Q3, and Q4. The wideband amplifier has approximately 50 db of gain with limiting in Q4 so that the output is approximately 0 dbm. The bandwidth of the wideband amplifier is 6.0 mc. The limited signal path is Q5, FLI, Q6, Q9, and Q10. The gain of the limited signal path is approximately 60 db, with Q10 limiting the output to the loop phase detector to +10 dbm. In the linear signal path to the agc detector, gain is provided by Q5, Q6, Q7, and Q8. Approximately 45 db of gain is provided in this path, making the input to the agc detector at approximately -6 dbm. The bandwidth of the second i-f amplifier is established by the crystal filter FLI, which has a bandwidth of 10 to 20 kc. The second i-f amplifier is linear within plus or minus 0.5 db over a 20 db range from the

amplifier input at -50 dbm. The phase shift between the output of the second i-f amplifier and its input will vary linearly within plus or minus 3 degrees over the input frequency range of 9.529154 to 9.533347 mc. A plot of phase shift versus frequency for this amplifier shows odd symmetry about 0 degrees at a frequency of 9.53125 mc, within plus or minus 5 degrees.

The transponder contains two identically designed phase detectors that serve different purposes. Each compares a characteristic of the incoming 9.531 mc signal with a reference signal generated by the vco. The output of Q10, the signal limiter amplifier, is applied, at a +10 dbm level, to the input of the loop phase detector CR5 and CR6. Q8 is a reference signal limiter amplifier which supplies an input, at a frequency of 9.531 mc, from the receiver vco. The transfer function of the loop phase detector is a dc voltage per degree of error.

The low-pass filter at the output of the loop phase detector provides the required leading and lagging time constants for the phase-tracking loop. The low pass filter is an RC time constant network, with a lagging long time constant to maintain the bandwidth of the phase tracking loop and a leading short time constant to prevent loop oscillations. The noise bandwidth at receiver threshold is approximately 318 cps. The output of the low pass filter is applied to the varactors in the VCO, Q3.

The vco provides stable 19.0625 mc, stability 0.001%, signals for the transmitter, the frequency divider, and the local oscillator multiplier. The vco is controlled by the filtered dc output of the phase detector. The vco uses a ruggedized third overtone crystal in a series-tuned

feedback circuit. Frequency shifting is accomplished by changing the amount of capacitive reactance in the feedback circuit varactors.

The output of the vco is applied to a buffer stage Q4. The output of the buffer stage Q4 is applied to an isolation amplifier stage Q10 and also to a string of frequency multipliers. The buffer stage prevents the frequency multipliers from loading down the oscillator stage and possibly pulling it off frequency. The output of Q10, the isolation amplifier, is applied to Q1 via a hybrid network. The hybrid network also supplies a signal to the transmitter section of the unified S-Band equipment.

Q1, in the detector A1, amplifies the 19.0625 mc vco signal and applies it to a balanced diode divide-by-two circuit. The output of the divide-by-two circuit at a frequency of 9.531 mc is applied to two amplifiers, Q2 and Q3. The output of Q3 the power amplifier is applied to three phase shift networks. The phase shift network supplying a signal to Q8 has a leading phase of plus 45 degrees. The phase shift network supplying a signal to Q4 has a lagging phase shift of minus 45 degrees. The phase shift of the network feeding the range phase detector has a leading phase shift of plus 45 degrees.

The agc detector is an amplitude detector which is identical to the loop phase detector except in application. Operating in phase quadrature with the loop phase detector, it develops a d-c output voltage proportional to the amplitude of the input signal. The two signals applied to the agc phase detector are the output of Q8, of the second i-f amplifier, and Q4 which is the divided output of the vco. The output of the agc detector is applied to three dc amplifiers, Q5, Q6, and Q7.

The output of Q7 is applied across a 4 volt zener to the first i-f amplifier. An RC network provides an agc time constant of 5.7 seconds. The agc loop noise bandwidth is 0.35 cps at a receiver input of -132 dbm and the bandwidth is 3.5 cps at a receiver input signal level of -52 dbm. The variation in the agc channel of the second i-f amplifier output will not exceed 2 db for a receiver r-f input level variation from -132 dbm to -52 dbm. The agc maintains the rms variation in signal gain from the input of the first i-f amplifier to the output of the second i-f amplifier from exceeding 2 db at -132 dbm.

The 9.531 mc i-f signal output of the wideband i-f amplifier contains the ranging, voice, and up-data information. The output of the wideband amplifier is held at a level of 0 dbm by the agc system and the limiter output stage of the wideband amplifier. The ranging and subcarrier information is extracted in a modulation phase detector Q9 by comparing the 9.531 mc r-f signal with a reference 9.531 mc signal derived from the divide-by-two circuit and the phase shift network. The ranging information is amplified in Q12 and applied to the phase modulator in the transmitter section for turn-around retransmission to the MSFN tracking stations. The subcarrier information, 30 kc for voice, and 70 kc for up-data is amplified in Q11 and applied through the output connector of the SEP to the Pre-Modulation Processor Equipment.

The X108 frequency multiplier provides injection frequencies of 2058.75 mc and 38.125 mc. The 2058.75 mc is applied to the first mixer and the 38.125 mc is applied to the second mixer. The frequency multiplication scheme is X2, X2, X3, and X9. The X9 multiplier stage uses a tuned cavity in its output circuit to reduce the amplitude of sidebands applied to the input balanced mixer stage.

12.5.2 Transmitter (See Figure 12-4)

The unified S-Band transmitter has three modes of operation, with frequency control originating in the following locations:

- a. Receiver VCO
- b. Auxiliary crystal oscillator
- c. FM voltage controlled oscillator

The modes of operation are manually selected from the communications control panel 20. There are five toggle switches on panel 20 which affect the various modes of operation:

- a. OSC-PRI/SEC
- b. RNG-OFF-RNG ONLY
- c. TV-OFF-PLSS
- d. TAPE-OFF-ANALOG
- e. EMERG.-VOICE-NORMAL-KEY

These five S-Band switches on panel 20 determine whether the Unified S-Band Transmitter will be enabled for either Frequency Modulation (FM) or Phase Modulation (PM).

Spacecraft-to-earth communication is accomplished by PM or FM of a signal derived from either the receiver VCO, the transmitter auxiliary oscillator, or the FM VCO. To simplify the spacecraft equipment as much as possible a 1.024 mc subcarrier is used for telemetry in all modes in which it is transmitted and a 1.250 mc subcarrier is used for voice in all modes except emergency voice. The 1.024 mc telemetry subcarrier was chosen because it is easily derived from the output of the Central Timing Equipment and is above the second harmonic of the 500 kc TV signal. The choice of narrow-band PM as the

technique for ranging was due to the requirement for coherence between ground transmitted and ground receiver carriers. The narrow-band phase modulation will maintain phase coherence between the spacecraft received and transmitted carriers, and yet leave sufficient power in the carrier component to enable coherent carrier tracking by the ground receivers. Wideband frequency modulation is used for TV, SCO's, and Bio-Med because of the large information bandwidths transmitted in these modes.

The initial signal for operation of the unified S-Band transmitter is generated in one of two oscillators. The first (PRI) is located in the receiver section (receiver vco), and the second (SEC) (auxiliary oscillator) is located in the transmitter module as shown in Figure 12-4. Both oscillators are crystal controlled and operate on a center frequency of 19.0625 mc with a long time stability of plus or minus 0.001 percent. The oscillators have a symmetrical characteristic S-curve extending 0.0003 percent above and below the assigned frequency. The characteristic S-curve is linear within plus or minus 5 percent over a frequency range from 0.0002 percent below to 0.0002 percent above 19.0625 mc. The maximum deviation of the auxiliary oscillator is 40 cps (4,800/120). With an 0.20 peak voltage input the oscillator is from 300 to 3,200 cps. Selection of the desired oscillator is made from the "PRI-SEC" oscillator control or the Emergency "VOICE-NORMAL-KEY" switch on control panel 20. If the "PRI-SEC" control is in the "PRI" position, and the Emergency "VOICE-NORMAL-KEY" switch is in the "NORMAL" position, the receiver vco will be selected and the gated amplifier Q1 applies the 19.0625 mc receiver vco signal to the X2 multiplier Q4-Q5. The control line at C48, CRI

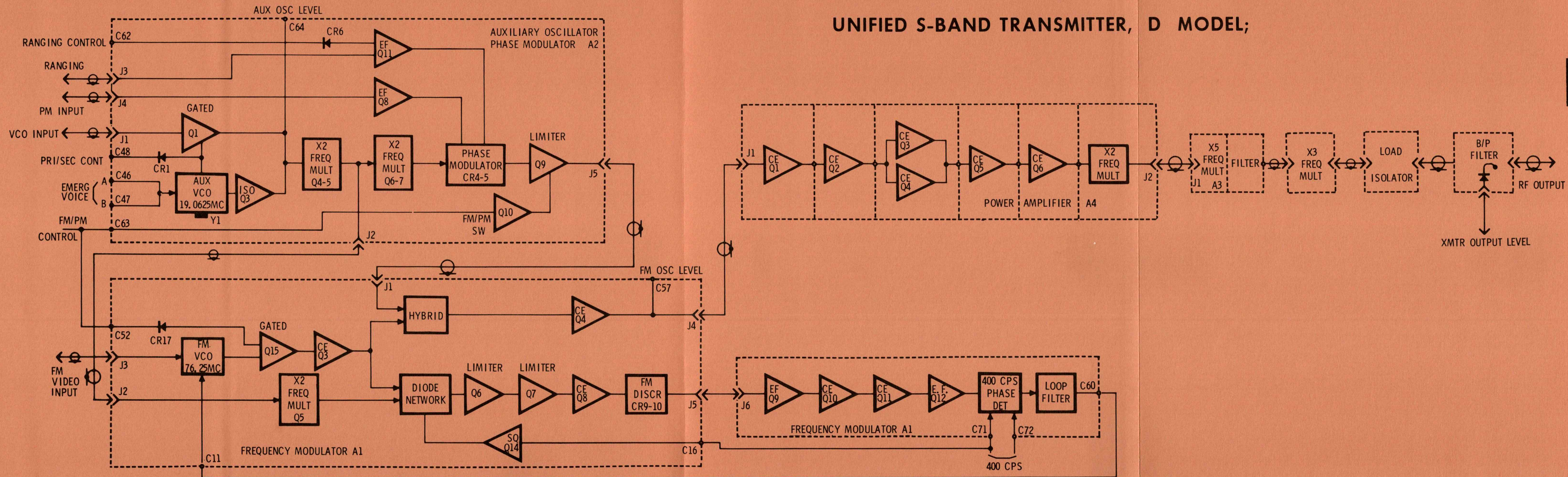


Figure 12-4

turns off the auxiliary oscillator vco when it turned on the gated amplifier Q1. The signal is multiplied by two in Q4, Q5 and applied to the second X2 multiplier Q6, Q7 and also to pin J2. When the operation of the auxiliary oscillator vco is desired, the "PRI-SEC" switch is placed in the "SEC" position or the "EMERGENCY VOICE-NORMAL-KEY" switch is placed in the "VOICE" position. This turns off the gated amplifier Q1 and starts the auxiliary oscillator. The signal from the auxiliary oscillator is then applied through Q3 and isolation amplifier to the same circuit network as the receiver vco signal. There is an oscillator test point connected to the input of the first X2 multiplier.

The output of the first X2 multiplier (Q4-Q5) is 38.125 mc. The 38.125 mc signal output of the first frequency multiplier is applied to the second X2 multiplier (Q6-Q7) and also to the X2 multiplier, Q5, via connector J2 in the frequency modulator module. The signal from the second X2 multiplier stage at a frequency of 76.25 mc is applied to the wideband phase modulator, CR4-5. There are two inputs to the phase modulator network; (a) the ranging signal from the modulation phase detector in the receiver module is applied through the gated transistor Q11, and (b) the phase modulated input (voice and data) from the Pre-Modulation Processor is applied through gated transistor Q8. The peak deviation of the phase modulator is .133 radians. In response to a 1 volt input signal at a frequency of 1 mc the phase modulator will yield 0.033 radians. The two inputs (Ranging and PM) are isolated from each other by approximately 20 db. The phase modulated output of the phase modulator is applied to a limiter Q9. The operation of the limiter Q9 is dependent upon the setting of the controls on control panel 20. Limiter Q9 is turned on by the

"RNG-OFF-RNG-ONLY" and the EMERG. "VOICE-NORMAL-KEY" switches, in all other modes of operation it is turned "OFF". The phase modulated output of the limiter Q9 is applied to a hybrid network in the frequency modulator module via J5 and J1.

In the frequency modulated mode (controlled by switches "TV-OFF-PLSS" or "TAPE-OFF-ANALOG"), the phase modulator limiter Q9 is turned "OFF" and the signal from the first X2 multiplier, Q4-Q5, is applied to the X2 frequency multiplier Q5 via J2. The FM VCO and the gated transistor Q15 are turned on in the FM mode. The FM VCO is frequency modulated by the FM video signals from the Pre-Modulation Processor FM mixing network (TV, SCO's, DATA, VOICE, and Bio-Med). After being modulated by the FM video input, the FM VCO output is applied through the gating circuit, Q15, to the hybrid network and the diode chopper network via Q3. The signals applied to the diode chopper network are the reference signal (76.25 mc) and the FM VCO signal (76.25 mc). The gating signal for the chopper diodes is provided by the 400 cps power supply. Q14 is a square-wave amplifier circuit that alternately switches the reference 76.25 mc signal or the FM VCO 76.25 mc signals to the AFC loop. This presents the two 76.25 mc signals riding on alternate half cycles of the 400 cps to the FM Discriminator via Q6, Q7, and Q8. A difference between the FM VCO frequency and the reference frequency develops an error voltage in the output of the FM discriminator. The output of the FM discriminator is applied to a synchronous detector via Q9, Q10, Q11, and Q12. In order to provide phase sensing with respect to error polarity, the phase detector is driven by the same 400 cps signal that operates the diode switching network through Q14. In this manner, the error signal is synchronously demodulated, providing an unfiltered dc signal, whose polarity is determined by the direction of

frequency error. This error voltage is applied to the loop filter. The afc loop filter has a one cycle bandwidth. The output of the loop filter is returned to the FM VCO with the proper polarity to cause a frequency change which will counteract the original error in frequency of the VCO. The FM VCO has a modulating sensitivity of 1.5 mc peak per 1 volt peak input, a bandwidth of 5 cps to 1.5 mc.

The input to the hybrid network is either the phase modulated output of the phase modulator or the frequency modulated output of the FM VCO. The output of the hybrid network is applied to the power amplifier section via Q4 and J4-J1. The power amplifier consists of five amplifier stages and an X2 frequency multiplier. The power amplifier provides approximately four watts at 76.25 mc to drive the final multipliers. The X2 multiplier is a varactor type circuit utilizing LC tuned circuits. The input signal drives the varactor diode to produce a second harmonic which, in turn, drives a X5 varactor type circuit. The output of the X5 multiplier is passed through a trough line filter to remove all harmonics except the fifth at a frequency of 762.50 mc. The output of the X5 multiplier is applied to a tuned cavity X3 multiplier circuit. The third harmonic of 762.50 mc (2287.5 mc) is applied to the output connector of the module via a load isolator and a bandpass filter. The load isolator following the final (X3) multiplier stage has an insertion loss of approximately 0.5 db. The front to back isolation of the load isolator is 20 db minimum with an input/output impedance of 50 ohms and a vswr of 1.2. The power sampler in the output bandpass filter provides a means of sampling the output power of the transmitter. The r-f output signal is 250 to 400 milliwatts at a

center frequency of 2287.5 mc.

12.5.3 Power Supply

The power supply for the USBE consists of a 3-phase, full-wave rectifier. The 3-phase power supply is used to take advantage of the reduced filter requirements of such a system. Each d-c supply is driven from wye secondaries on a single delta-wye transformer and uses a full-wave silicon rectifier. LC filters are used to reduce commutation spikes and ripple at the input to the series regulator circuits, caused by phase unbalance, to less than 2 millivolts rms. The 115 volt, 400 cps supply voltage is reduced to 25.5 volts ac by the step-down transformers connected across each phase of the supply transformers connected across each phase of the supply line. Full-wave rectification is provided by twelve silicon diodes. Ripple filtering is accomplished with a two section LC low pass filter consisting of two inductors and two capacitors connected on both the positive and negative outputs. The power supply furnishes both a +15 vdc and a -15 vdc with a 3 percent tolerance. The efficiency at the rated load of 12 watts is approximately 80 percent.

All input and output leads, both power and signal, are provided with filters to remove extraneous signals which may lead to radio frequency interference, (RFI).

All but four connections between the USBE and the Pre-Modulation Processor Equipment and the S-Band Power Amplifier Equipment are made through the front panel. The front panel contains a power connector, signal control connector, interface connector, and a test connector. The receiver input, PM input, FM video input, and r-f output connectors are all coaxial connectors and are not attached to the front panel, instead they are connected to the back panel.

SECTION XIII

S-BAND POWER AMPLIFIER

The 548N-1E S-Band Power Amplifier of the Apollo Communications and Instrumentation system is designed to provide increased RF power output during communications via the 621F-1E Unified S-Band Equipment. The unit may be operated in 5 watt, 20 watt or bypass operating modes. During the bypass mode of operation the power amplifier is turned off, and all signals from the USBE transmitter are routed through the power amplifier without amplification.

INTRODUCTION

The power amplifier makes use of a traveling-wave-tube (TWT) for amplification of the input signals. A drive signal from the USBE transmitter, operating at a level of 250 to 400 mw, is attenuated in the power amplifier before it is presented to the TWT.

The power amplifier weighs thirteen pounds with a volume of 444 cubic inches and is located in the Lower Equipment Bay at K-2, L-2. Input power to the unit comes from the 115/200 volt, 3 phase, 400 cps Essential and Non-Essential Bus. For the 20 watt mode of operation the power amplifier requires 90 watts, and for the 5 watt mode of operation the power consumption is 35 watts. During the 90 second warmup period the power used is only 10 watts.

There are two controls on the Communications Control panel which directly affect the operation of the power amplifier, the "XPONDER-OFF-PWR-AMP" switch and the "HI-LOW" switch. The power amplifier is only turned on when the "XPONDER-OFF-PWR AMP" switch is in the PWR AMP position. With the switch in the PWR AMP

position, the unit will be enabled in either the 5 watt or 20 watt mode, depending upon the selection made at the "HI-LOW" switch. When the power amplifier is in the PWR AMP position, there is no bypass function and the USBE transmitter output will be amplified to one of these two levels. Whenever the power amplifier is turned off, it automatically switches into the bypass mode of operation, permitting the output of the USBE transmitter to be presented to the antenna network. The power amplifier will be off in either the OFF or XPONDER position.

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

The Unified S-Band Transmitter provides the RF signal for transmission. This input to the power amplifier is routed through the unit in one of two ways, depending on the desired mode of operation. For the modes of transmission requiring only minimum power output, the S-Band Power Amplifier will not be turned on and the signal from the USBE transmitter will pass through a bypass switch, composed of two coaxial relays, and through a diplexer to the antenna for transmission. This is shown in figure 13-1, a block diagram of the S-Band Power Amplifier. When the power amplifier is operating, coaxial relays K-1 and K-2 are actuated so that the USBE transmitter RF signal passes through an attenuator, the traveling wave tube (TWT) and a signal sampler, before application to the diplexer. The attenuator reduces the drive level of the RF signal to the level needed for optimum operation of the traveling wave tube. The traveling wave tube provides the required amplification of the signal. A signal sampler is used so that an analog power indication may be obtained for use in the PCM TLM.

S-BAND POWER AMPLIFIER

BLOCK DIAGRAM

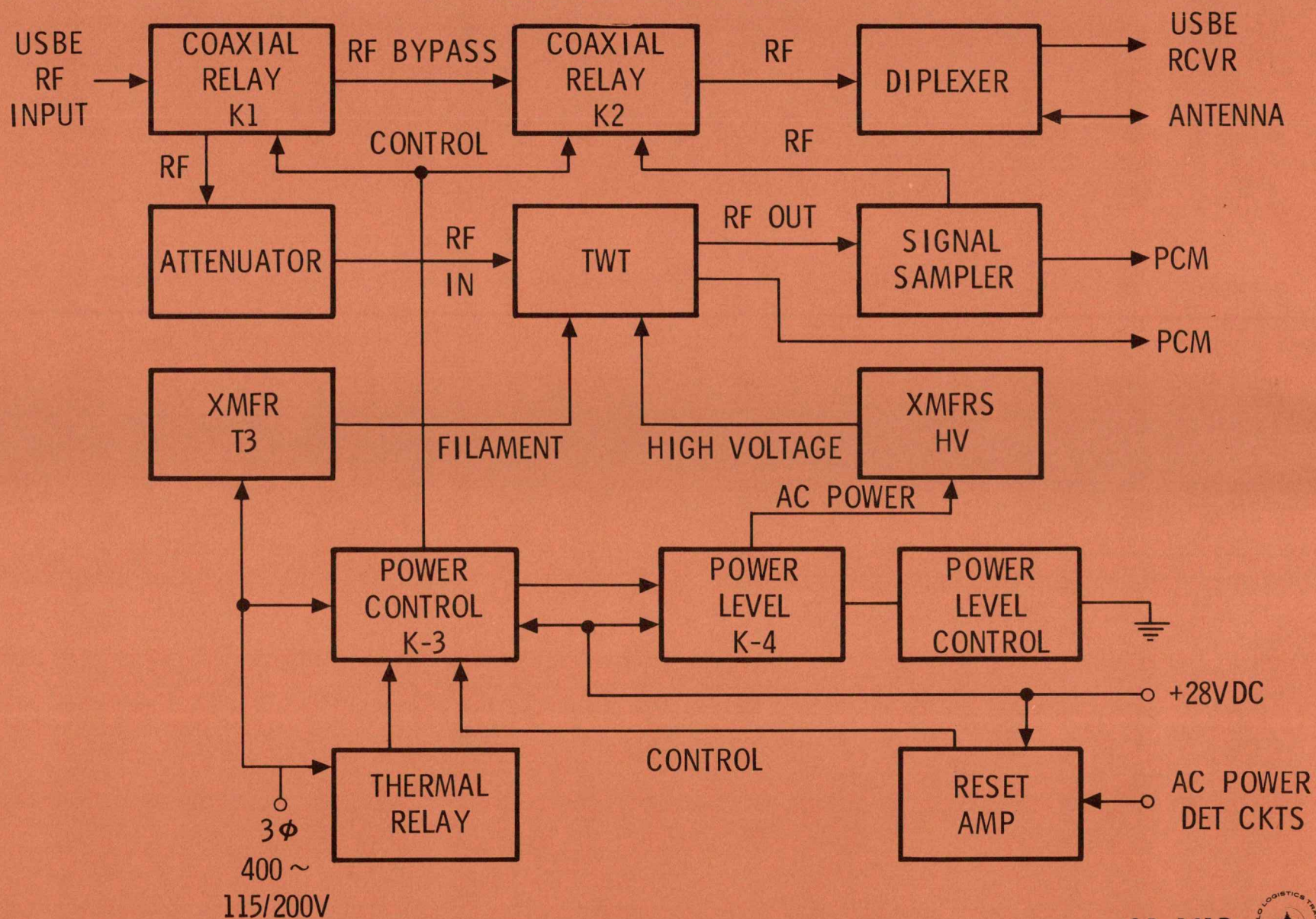


figure 13-1

CD-121B



In all modes the RF signal passes through the diplexer before it is routed to the selected antenna for transmission to earth by an external antenna switch which is controlled from the Antenna Control panel. The diplexer also passes the received signal from the antenna to the Unified S-Band Receiver.

A series of relays is used to control the application of ac power and the operating modes of the equipment. Coaxial relays K-1 and K-2 are used to place the equipment in the transmit or bypass mode of operation. The application of ac power to the **S-Band Power Amplifier** causes activation of these relays through power control relay K-3. This operation causes the RF signal from the transmitter to be routed through the traveling-wave-tube. In the absence of ac power, bypass relays K-1 and K-2 are placed in the bypass position by the +28 volts DC from the Flight and Post Landing bus. This voltage is always available to the power amplifier via K-3.

Power level relay, K-4 controls the power level of operation of the power amplifier by selection of the desired power level (HI-LOW) at the communications control panel. The "HI-LOW" control is a two position switch by which relay K-4 controls application of proper operating voltages to the traveling-wave-tube (TWT).

Thermal relay K-5 and power control relay K-3 are used to control the application of power to the TWT. When ac power is first applied to the power amplifier, K-5 causes a 90 second delay which prevents the application of high voltages to the TWT, with the exception of filament voltage. In this way, the TWT has the opportunity to warm up before operation. This prevents damage to the TWT at application of high voltages.

Relay reset amplifier Q-1 is used to reset relay K-3 when ac power is no longer present. When the power is turned off, or some malfunction occurs whereby the ac voltage on any phase of the input line is lost, peak detector circuits, which monitor the presence of ac, will cause Q-1 to conduct and reset relay K-3. Therefore, no voltage can be applied to power transformers T-1 and T-2.

Transformer T-3, and contacts of relays K-3 and K-5, receive 115/200 volts 3 ϕ , 400 cps ac power directly. The voltage applied to T-3 is transformed and applied to the filament of the TWT in order to heat the tube before the application of high operating voltages. One phase, upon application to relay K-5, initiates a 90 second time delay before the input ac power is passed through relay K-3 terminals to either transformer T-1 (20 watt mode) or transformer T-2 (5 watt mode). The ac is rectified in full wave rectifier circuits to the high operating voltages required in the TWT.

DETAILED BLOCK DIAGRAM DESCRIPTION

TRAVELING WAVE TUBE The main difference between the klystron amplifier and the TWT amplifier is that electrons in the klystron interact with a standing wave and the TWT electrons interact with a traveling wave. The TWT uses no high Q tank or resonant circuits and, therefore, is capable of operating over a broad range of frequencies.

Components

The TWT consists of six main sections: the electron gun, the RF interaction circuit, the focusing magnets, the collector, the attenuator, and the RF input and output couplers. Their functions are explained in the following paragraphs.

TWT SCHEMATIC

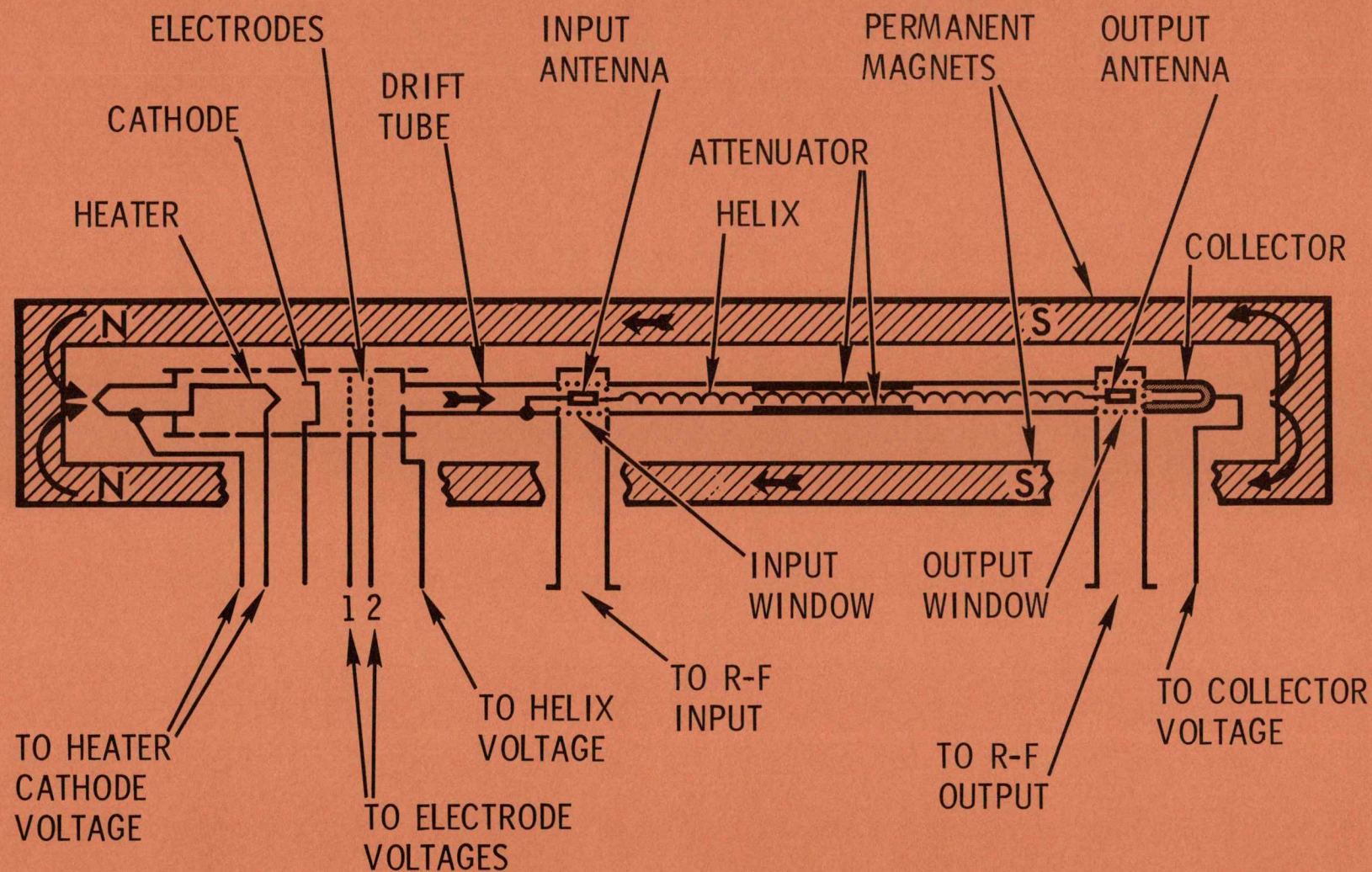


figure 13-2

CD-197



Electron Gun. The TWT uses the same type electron gun as the klystron and the cathode ray tube. It forms an electron beam which is attracted by the collector of the tube.

Collector. As mentioned above, the collector attracts the electrons which are sent out of the electron gun in a beam.

Focusing Magnets. These electro-magnets provide a strong magnetic field about the electron beam which constrains it, maintaining the electron path through the center of the RF interaction circuit.

RF Interaction Circuit. The RF interaction circuit consists of a helically wound coil which is fed by the RF signal to be amplified. Due to the high frequency of the signal, an RF wave will be propagated into the tube from the helix. Because of the impedance matching and lack of resonant circuits the wave will travel along the helix; hence, the name, traveling-wave-tube.

Attenuator. To prevent spurious oscillations, a lumped attenuator is placed around the electron beam, near the center of the tube. This will reduce the amplification of the RF somewhat but will also attenuate the reflected waves from the collector which could cause oscillations.

Input and Output Couplers. These coax couplings connect the incoming RF to the helix, and the output of the helix to the output coax.

Operation

If a beam of electrons can be made to travel through an RF wave, an interaction will take place

between the two. If the RF wave and the electrons in the beam are traveling in the same direction, and the electrons in the beam are moving at a higher rate of speed, they may be made to give up part of their kinetic energy to the RF wave. Figure 13-2 shows the TWT, its components, and operations.

The helix has two purposes in the TWT. First, the helix changes the forward direction of the RF wave so that its velocity vector, parallel to the electron beam is slightly less than the speed of the electrons in the beam. This allows the RF wave to have a maximum cumulative effect on the beam. Second, the helix causes the RF wave to be concentrated through its axis. The electron beam is focused through this same axis to obtain maximum interaction between the beam and the RF wave.

As the beam travels down the tube its electrons are accelerated or decelerated, as determined by the phase of the RF wave front produced in the helix. As the wave front reverses, it will cause alternate acceleration and deceleration of the electron beam, producing a bunching effect of the electrons and a general deceleration of the beam. As the beam decelerates, it gives up kinetic energy to the RF field. This appears in the helix as an amplification of the input RF signal.

The useful energy of the TWT is continually transferred from the helix to the electron stream, back to the helix, and eventually taken off the helix at the output end.

The gain of a TWT is influenced by voltage variations on the heater, the beam controlling electrodes, and the helix. Changes in helix voltage have the greatest effect upon the gain characteristics of the

tube. Adequate voltage control is required for optimum performance. In general, a variation of $\pm 0.5\%$ in helix voltage results in a ± 1 db variation in gain; similarly, a heater voltage variation of $\pm 5\%$ results in a ± 3 db variation in gain. Gain control of a TWT can be accomplished by variation of the voltage applied to the electron gain heater.

S-BAND POWER AMPLIFIER OPERATION A detailed block diagram of the S-Band Power Amplifier is shown in figure 13-3. In all modes of operation, the 2106.4 mc RF signal received from the ground DSIF station enters the S-Band Power Amplifier at the RF in/out antenna connection. The RF signal passes through the diplexer, and is then routed from the S-Band Power Amplifier to the input circuit of the Unified S-Band Receiver. The diplexer acts as a double-tuned circuit, through which the received frequency is passed from antenna to receiver, and the transmit frequency (2287.5 mc) is passed from the power amplifier to the antenna. The receiver arm of the diplexer has a center frequency of 2104.104 mc with a bandwidth of 10 mc to 95 mc. It has a VSWR of 1.2:1 maximum at 50 ohms and an insertion loss of 0.5 db maximum. The receiver arm is isolated from the transmitter arm by 60 db minimum. The transmitter arm has a pass band center frequency of 2285 mc. The pass band center frequency is defined as that frequency which is the arithmetic mean of the upper and lower 3 db frequencies, and there must be no less than 5 mc between either -3 db point and the pass band center frequency. The bandwidth at the -3 db points is 11.5 mc and at the -15 db points is 16.0 mc. maximum. The transmitter arm has a 2.1 db maximum insertion loss at 2285 \pm 3.75 mc. Power handling capability 20 watts minimum.

The S-Band Power Amplifier will probably be operated in the bypass mode of operation during most

of the actual mission to conserve power. In this mode, no power is applied to the amplifier, and the RF signals from the transmitter are routed through the amplifier without any signal processing. The 250 to 400 milliwatt signal from the transmitter is passed through a pair of coaxial relays, which act as a bypass switch, and the diplexer, before it is applied to the selected antenna for transmission to earth.

Coaxial relays K-1 and K-2 are held in the bypass position by the application of +28 volts dc from the Flight and Post Landing Bus, through contacts of power control relay K-3.

The S-Band Power Amplifier is capable of operating in the 5 watt or 20 watt mode, depending on the position of the "HI-LOW" switch on the communications control panel. HI position gives 20 watts output power, and LOW gives 5 watts output power. Signal processing in both cases is identical, with the only difference in operation being the amount of gain provided by the TWT in each of the two modes. When power is applied, coaxial relays K-1 and K-2 are switched, routing the 250 to 400 milliwatt RF input signal from the Unified S-Band Transmitter to an attenuator. The input RF signal is reduced to a level which will ensure maximum efficient operation of the TWT. With 300 milliwatt input the attenuator will offer 9 db of attenuation.

The RF signal out of the attenuator is fed to the input coupler circuit of the TWT where it is amplified to either 5 watts or 20 watts. The output coupler circuit of the TWT then passes the signal through a signal sampler circuit which is used to give an analog power indication for use in the IFTS system. From the signal sampler the signal passes through the closed contacts of the coaxial relay K-2,

13



13-7

through the diplexer, and to the antenna for transmission to earth.

The TWT is used to provide amplification of the transmitter signal to either the 5 watt or 20 watt level. The mode is varied by changing the nominal operating voltages on the cathode, first anode, and collector of the TWT. In the 5 watt mode, -1160 volts dc is applied to the cathode, -300 volts dc to the first anode, and -600 volts dc to the collector. In the 20 watt mode, -1400 volts dc is applied to the cathode, the first anode is grounded, and the collector potential is -300 volts dc. The second anode operates at +100 volts dc, the filament at +5 volts dc, and the helix is ground referenced in both modes.

Relays K-1 and K-2 are used in the selection of operating modes to route the transmitter RF signal through the amplifier. They are controlled by the operation of the power control relay K-3, and are designed so that when switching from the bypass mode to the power on mode, K-2 actuates slightly before K-1. This action prevents the transmit signal from being applied to the TWT before the output signal line is connected to the diplexer, thereby preventing undesired transient effects. When switching from the power on mode to the bypass mode, relay K-1 actuates before relay K-2.

Relay K-3 is a mechanical latching relay with two windings. A spike of current in either winding is sufficient to change the state of the relay.

Relay reset amplifier Q-1 and its associated circuitry provide a means to return relay K-3 to the bypass mode and to protect the TWT in case of 3 ϕ , 115 volts, 400 cps voltage failure. Figure 13-4 illustrates this operation in block diagram form. When K-3 operates, -28 volts DC is applied to the emitter

of Q-1. The collector is connected to ground through one of the coils of relay K-3.

The peak detector circuits are tied to the ac inputs through transformers T-3 and T-4. These circuits sense the presence of the ac input, and maintains a voltage of approximately +37 volts dc at the base of Q-1 whenever the correct ac input is applied to the S-Band Power Amplifier. This maintains Q1 in an off condition. If one of the input phases fails, the +37 volts dc level will drop sufficiently so that Q-1 will conduct, energize the coil of relay K-3 and return the relay to the bypass mode. This action removes the operating voltages from the unit, thus protecting the equipment from damage that might result from incorrect ac inputs. The same sequence occurs when the power is removed by turning of the "XPONDER-OFF-PWR AMP" switch on the Communications Control panel. This ensures that relay K-3 is always reset before initiating a new operating cycle.

Relay K-4 is the power relay controlled by the "HI-LOW" switch on the communications control panel. The "HI-LOW" switch places K-4 in a state which ensures that the correct operating voltages from the power transformers are applied to the TWT.

Relay K-5 is a 90 second delay thermal relay. When ac power is applied to the S-Band Power Amplifier, 115 volts AC, phase C, is applied to the relay. At the end of the delay period, the relay contacts close, applying +28 volts dc across the coil of power relay K-3. Relay K-3 activates, removing the ac power from K-5 and returning it to the initial state. The 90 second thermal relay insures that the TWT is sufficiently warmed-up before the high operating voltages are applied to it.

A +28 dc voltage from the Flight and Post Landing bus is applied to the S-Band Power Amplifier at

all times as power to operate the relays, with the exception of thermal relay K-5. Relay reset amplifier, Q-1, also receives emitter voltage from this supply when the power amplifier is operating.

The main power for the power amplifier is 115/200 volts, 3 ϕ , 400 cps.

When power relay K-3 operates, all three phases of the ac input are applied to power transformers T-1 (20W) and T-2 (5 W). The outputs of the power transformers are rectified in full-wave bridge rectifiers and sent to the TWT through relay K-4 at the proper operating levels.

TYPICAL SEQUENCE OF OPERATION

The following steps give a typical sequence of operation of the S-Band Power Amplifier when the equipment is turned on.

- a. "HI-LOW" switch on control panel number 20 in LOW, 5 watt mode.
- b. +28 volts dc is present for relay power.
- c. "XPONDER-OFF-PWR AMP" switch on control panel to "PWR AMP".
- d. Power is applied to T-3 and to thermal relay K-5.
- e. Filament voltage prepares TWT for operation, while 90 second delay in K-5 progresses.
- f. Thermal relay K-5 operates.
- g. Relay K-3 operates, applying ac power to power transformer and operating voltages to TWT.
- h. Peak detector circuits come into operation.
- i. Relay reset amplifier Q-1 is cut off.
- j. Relays K-1 and K-2 are switched from the bypass mode to the input/output circuits of the TWT.

- k. Signal from the unified S-Band Transmitter is passed through K-1, the attenuator, the TWT signal sampler, diplexer and then to the antenna.
- l. Switching to HI (20 watt) mode changes the application of input power from T-2 to T-1.
- m. "XPONDER-OFF-PWR AMP" switch OFF, relay reset amplifier Q-1 resets K-3 to initial condition, which switches K-1 and K-2 to the bypass mode.

SECTION XIV

HIGH GAIN ANTENNA

14.1 GENERAL

The Block II S-Band Hi Gain Antenna assembly is comprised of four parabolic and one conical dish reflectors with their associated feed horn. They are mounted on a gimbaled frame as shown, (figure 14-1) with the whole assembly weighing about 45 lbs. The prime function of this Hi Gain Antenna assembly is to provide the necessary propagation patterns and gain to allow the S-Band telecommunications system to function effectively at lunar distances.

14.2 DEPLOYMENT

The antenna assembly is deployed upon initiation of SLA panel deployment. As the SLA panels deploy, a mechanical trigger is tripped thus unlocking the boom upon which the antenna assembly is mounted. This boom is then deployed by a simple dampened spring mechanism. The antenna assembly, when deployed, is 39" from the service module skin.

14.3 ANTENNA ASSEMBLY CONFIGURATION

The antenna assembly consists of five separate antennas. Four of the five antennas, which comprise the assembly, are identical having 31 inch diameter parabolic reflectors which weigh approximately 2 lbs. each. The reflectors themselves are constructed of Rene' 41 stainless steel honeycomb with solar rib reinforcement. The feed horns are offset 10° to give the desired pattern of propagation.

The small center antenna has a conical reflector of about 9 inches diameter and is of similar construction as its larger counter parts. The feed horn on this smaller antenna is not offset and is proportionately shorter.

The antenna assembly operates with beam widths of 60° , 11.1° and 4.6° respectively. The wide beam width is obtained by using the small center antenna as the RF propagation device. For the medium beam width, the lower right 31 inch antenna is used. The narrow beam width is obtained by using all four of the 31 inch antennas as the RF propagation devices.

14.4 TRACKING MODES

The antenna assembly has the ability to be pointed towards the earth by two different operational modes, manual or automatic. In the manual mode, the astronaut can position the assembly for maximum signal with the yaw and pitch controls on the control panel. The relative position of the antenna assembly can be read out on the pitch and yaw position meters. Relative signal strength is monitored on the "tune for max", (AGC) meter on the same panel.

When automatic tracking is employed, one of two infrared sensors mounted on the antenna assembly come into play. At near earth distances, the wide view LR sensor is employed to provide the necessary position information to allow the antenna to track the earth. At longer distances, approximately 35000 miles, the narrow view LR sensor must first be manually pointed towards earth before automatic tracking can be

BLOCK II S-BAND HI GAIN ANTENNA

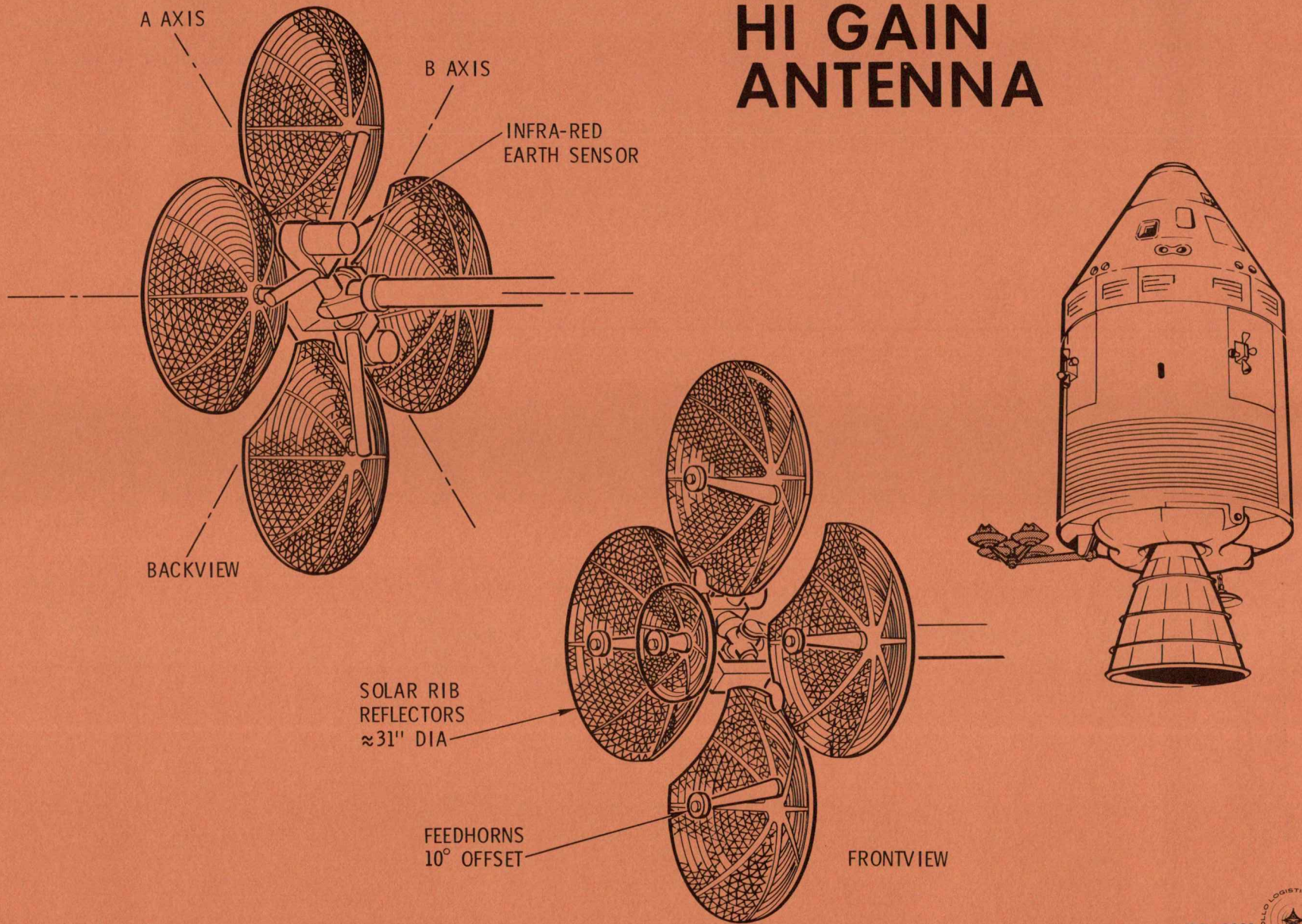


figure 14-1

initiated. When an LR sensor has locked on a source of sufficient magnitude the LR sensor signal flag will show a change to the normal or gray state.

SECTION XV

C-BAND TRANSPONDER, 621G-1

15.1 INTRODUCTION

This section contains a general and detailed description of the operation of the C-Band Transponder Equipment 621G-1. The spacecraft C-band system was designed to be compatible with instrumentation Radars AN/FPS-16 and AN/FPQ-6. The C-band system is capable of providing reliable tracking in range, bearing and elevation of the spacecraft relative to the Radar, during the launch, boost and orbital phases of the mission. The C-band transmitter provides sufficient power for reliable tracking to a slant range of 4,000 nautical miles. The radar reply from the spacecraft can be the energy reflected from the skin of the spacecraft (skin tracking), but the primary mode of operation employs the on-board C-band transponder to provide an amplified echo to a properly coded interrogation pulse (beacon-tracking). The transponder transmitter provides a return signal many times stronger than the skin-reflected reply, and thereby permits more accurate measurements at much greater distances.

The spacecraft transponder system consists basically of four independent receivers, each having its own antenna, and a single transmitter which replies on the antenna receiving the strongest signal.

The four spacecraft antennas are flush-mounted, with the ablative material, cavity-backed helix antennas spaced at 90 degree intervals about the spacecraft for maximum pattern coverage. Three of these antennas are mounted at station 20.7 on

the +Y, -Z, and -Y axes, and one is mounted at station 59, 14 degrees off the +Z to +Y axes. The antennas are circularly polarized since they must be capable of receiving the ground based interrogations independent of spacecraft attitude. If linearly polarized spacecraft antennas were used, an increase in gain would be realized when the polarization of the spacecraft antennas is aligned with the polarization of the ground radar; however, when the two polarizations are perpendicular, high losses would be incurred.

The outputs of the four receivers feed into a comparator circuit. The comparator circuit compares all four receiver outputs simultaneously and operates a four position coaxial switch to connect the transmitter output to the antenna having the strongest signal. The main advantage of this system is that continuous comparison of all four antenna elements provides complete continuous coverage. Another important advantage is that up to three receivers can fail and the system will still function, but at reduced coverage.

The transponder reply pulse will be transmitted after an over-all delay time, interrogation to reply, of 3 microseconds. This delay enables the ground radar operator to observe the skin track and transponder replies simultaneously on the same indicator during launch operations. This feature is useful as a back-up procedure. The delay also provides the

necessary time for the solid-state r-f switch in the transponder to operate to the correct antenna.

The transponder design permits interlaced interrogations; it will reply to two or more radars whose interrogations arrive sequentially at the transponder. The transponder will respond to these different signals so long as the interval between any two interrogations is greater than the transponder recovery time of 70 microseconds, and when the rate of interrogations is less than the maximum reply rate of the transponder. Radar operational procedures will have to be carefully observed to prevent beacon stealing and tracking interruptions. Beacon stealing could occur if two radars are interrogating simultaneously from two different directions.

15.2 LEADING PARTICULARS

The major characteristics of the transponder are listed below:

a. Frequency

- | | |
|----------------|---------|
| 1. Transmitter | 5765 mc |
| 2. Receiver | 5690 mc |

b. Stability

- | | |
|---------------------|---------------|
| 1. Local Oscillator | 0.002 percent |
| 2. Transmitter | ± 4 mc |

c. Sensitivity

-70 dbm

d. Transmitter

- | | |
|----------------|-------------------|
| 1. Pulse width | 0.75 ± 0.2 ec |
|----------------|-------------------|

- | | |
|-----------------|---------------|
| 2. Output power | 2.5 kw min. |
| 3. Pulse rate | 1 to 1300 pps |

- | | |
|-------------------|---------------|
| e. Power Required | 70 Watts max. |
|-------------------|---------------|

- | | |
|-----------|---------------|
| f. Length | 14.715 inches |
|-----------|---------------|

- | | |
|----------|-------------|
| g. Width | 10.3 inches |
|----------|-------------|

- | | |
|-----------|-------------|
| h. Height | 5.79 inches |
|-----------|-------------|

- | | |
|-----------|------------|
| i. Weight | 20.75 lbs. |
|-----------|------------|

The C-band transponder is controlled from control panel 20 by the "C-BAND" 1 Pulse-Off-2 Pulse switch. The switch, when either in the 1 pulse or 2 pulse position, applies +28 vdc to the armature of an a-c switching relay located external to the C-band transponder equipment. The voltage input is 115/200 volts, 3 phase, 400 cps at 70 watts when the transponder is being interrogated at a 500 pps rate.

15.3 SIMPLIFIED THEORY OF OPERATION

This section contains a general discussion of the operation of the C-Band Transponder.

15.3.1 Simplified Block Diagram (Figure 15-1)

The C-band transponder consists of four superhetrodyne receivers, including one common solid-state local oscillator, a comparator, a decoder-driver, a modulator, a r-f solid-state switch, a pulse-modulated transmitter, and power supply. The transponder circuitry is completely transistorized except for the magnetron in the transmitter.

C-BAND TRANSPONDER

BLOCK DIAGRAM

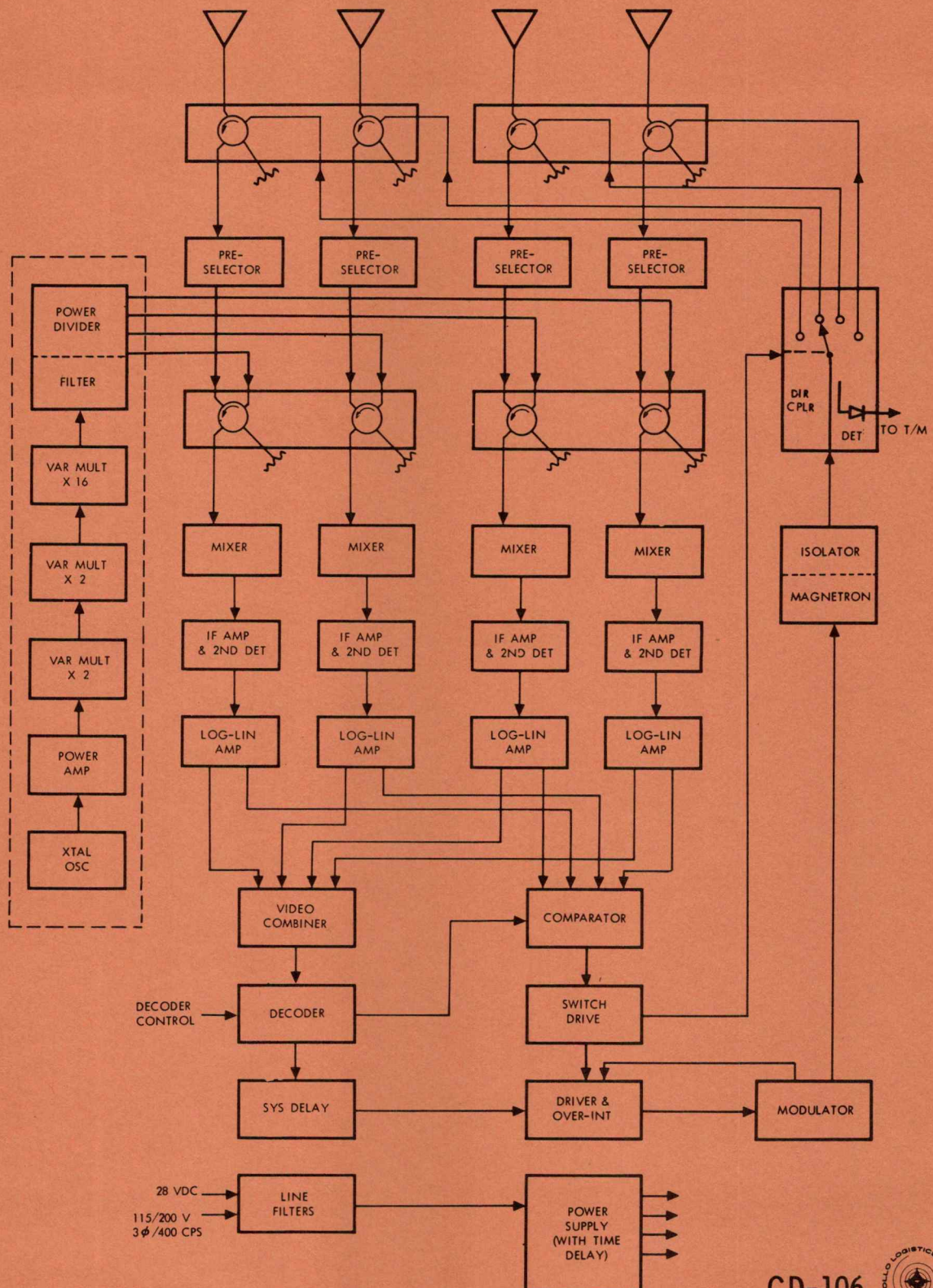


figure 15-1

The simplified diagram shows that the incoming signals from each antenna are mixed in the respective receiver front end with the local oscillator output to produce 60 mc difference frequency signals which are fed to the i-f and lin-log amplifiers. The signals are amplified by the i-f stages and then processed by the lin-log amplifiers to produce pulses that are proportional in amplitude to the input signal level (in dbm) at the antennas. These pulses are then fed to the comparator and video combiner.

The comparator determines which of the four received signals is the strongest and directs the switch driver to prepare the r-f solid-state switch to transmit through the antenna receiving that signal.

The output of the lin-log amplifiers is also presented to the video combiner. The video combiner consists of a pulse shaper, delay correction circuitry, and a strobe generator. The delay correction circuitry varies the signal response of the pulse shaper, causing an incoming signal, which varies from -70 to 0 dbm, to have the same amount of time between receipt of the interrogation signal and transmission of a reply. The pulse shaper receives a varying amplitude video pulse from each of the four lin-log amplifiers through the delay correction circuitry, and provides a single constant amplitude pulse output to the decoder.

If the decoder is set for two-pulse operation, it will only respond to double pulses with the proper code spacing. If the decoder is set for single pulse operation, it will respond to each pulse from the pulse shaper. The output

of the decoder is routed to the system delay.

The system delay inserts a delay that is added to the inherent delay of the transponder to provide the desirable overall transponder delay between the transmitter and receiver pulse. The pulse from the systems delay is presented to the driver and over-interrogation circuitry. The output of the over-interrogation circuitry triggers the driver. The driver, in turn, triggers the modulator. One output of the modulator is fed back to the over-interrogation circuitry. The over-interrogation circuitry monitors the modulator and if the interrogation rate exceeds 1300 pps, it disables the modulator driver. Also presented to the over-interrogation circuitry is the output of the switch driver. If the switch driver turns off all four switches in the r-f switch, a signal from the switch driver will turn off the modulator driver, disabling the modulator. Once triggered, the modulator delivers a pulse to the magnetron that enables the transmitter to deliver the required pulsed r-f signal through the r-f switch path which has been predetermined by the comparator. The r-f pulse is, therefore, routed to the antenna receiving the strongest input signal.

The power supply provides the various transponder voltages needed for operation. In addition, it provides a regulated and fail-safe output for the voltages. The fail-safe feature minimizes sequential failures within the power supply. An elapsed-time indicator provides a record of the on time of the transponder and is removed prior to launch.

15.4 FUNCTIONAL DETAILED BLOCK DIAGRAM

This section contains a detailed discussion of the operation of the C-band transponder. The description of each electronic assembly is provided in far more detail than in section 15.3.

15.4.1 Receiver (Figure 15-2)

15.4.1.1 Receiver Front End

There are four dual-diplexer microwave front ends in the C-band transponder, each composed of two 4-port circulators, a four stage preselector, and a mixer. In the diagram the antenna signal (5690 mc) is fed to the first 4-port circulator and channeled to the four stage preselector. The preselector determines the front end bandpass characteristics of the receiver. The output of the preselector is then delivered to the second 4-port circulator, which in turn delivers both the local oscillator CW signal and the preselector output signal to the mixer.

15.4.1.2 Circulator

The dual diplexer microwave front end is a unique, compact system. The heart of the system is a dual 4-port ferrite circulator which used a common magnetic biasing circuit. The circulator packaged in a single housing allows high performance to be attained in a very small volume.

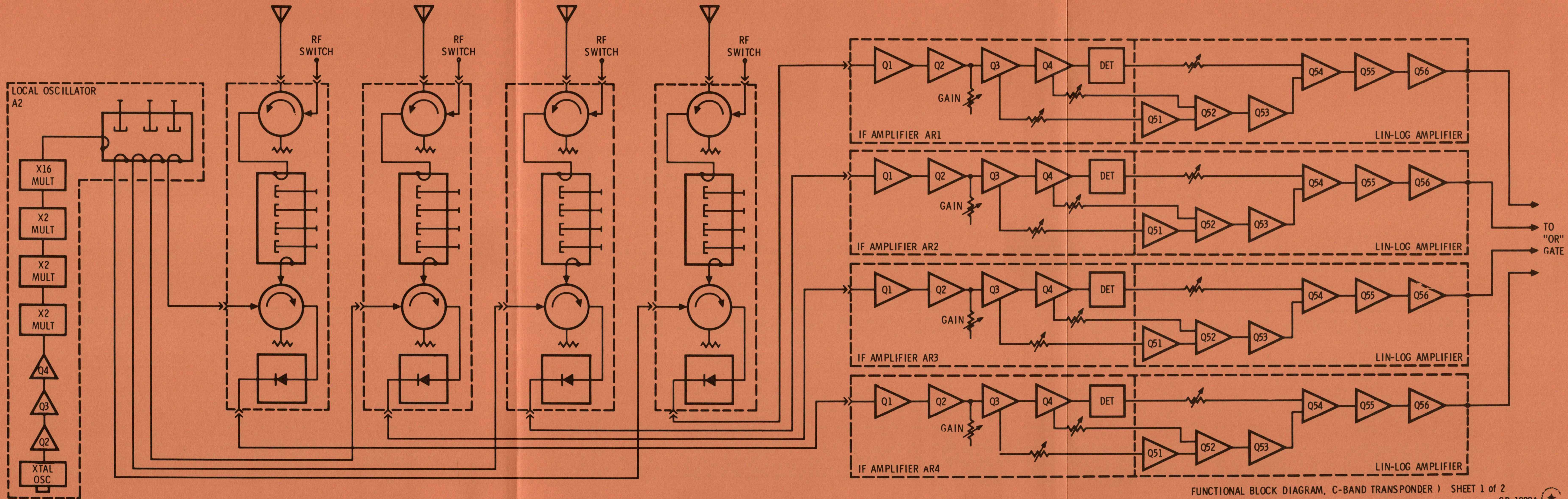
One-half of the dual 4-port circulator operates as a diplexer-isolator. It provides a diplexing action so that a single antenna can be utilized for both transmitting and receiving.

The diplexer also provides isolation between the antenna and transmitter and between the preselector and antenna to prevent mismatches from causing poor performance of the transmitter magnetron or preselector cavity. If isolation is not provided between the antenna and transmitter, any reflection from the antenna travels back to the magnetron. The magnetron sees this reflection as a reactance change at its output terminals that will change its resonant frequency.

In the receive mode, the signal entering the antenna port of the circulator is transmitted to the receiver port. Conversely in the transmit mode, the signal entering the circulator at the transmitter port is transferred to the antenna. The fourth port of the circulator is terminated in a matched load in order to absorb any power circulating around the device due to mismatches at any port.

Each 4-port circulator consists of two three-port circulators with a common arm internally connected. The three-port circulators are built in a Y-configuration in a balanced strip-line structure. A ferrite disc is placed on either side of the center conductor of the strip line. A d-c magnetic field is perpendicular to the plane of the strip-line structure. As a result of the interaction of the r-f magnetic and the d-c magnetic fields, the r-f wavefront is effectively bent or rotated as it travels through the ferrite medium.

The size and type of ferrite, together with the strength of the d-c magnetic field, are so chosen that the wavefront is perpendicular to the axis of the adjacent port as it leaves the ferrite medium. Thus, all power is coupled to this port with minimum attenuation; negligible



FUNCTIONAL BLOCK DIAGRAM, C-BAND TRANSPONDER) SHEET 1 of 2

Figure 15-2

power is rotated in the opposite direction; and power rotated to the common arm of the two three-port circulator is then rotated around the second circulator in the same manner.

15.4.1.3 Preselector

The receiver port of the antenna circulator is connected to a four-section preselector utilizing quarter-wavelength coaxial resonators. The signal is coupled into and out of the preselector with inductive loops; the individual sections are coupled together by means of inductive irises. The bandpass filter is tuned by adjusting the lengths of the center conductors of the coaxial resonators.

The output of the preselector is fed to the second half of the dual 4-port circulator. This half of the circulator is utilized as a diplexer-isolator between the local oscillator, the preselector, and the crystal mixer. The local oscillator signal is fed into one port of this circulator and directed toward the preselector port. Since the preselector is a reactive load at the local oscillator frequency, this signal is reflected back toward the circulator. Entering the circulator, it is transferred to the mixer port and then to the mixer crystal. Simultaneously, the received signal, after passing through the preselector, enters the circulator at the receiver port and is transferred to the mixer port. The circulator prevents local oscillator loading of the received signal, and at the same time provides a low loss path between the local oscillator and the crystal mixer. It also isolates the local oscillator and preselector cavity from mixer mismatches which could cause

degradation of receiver performance. As an adjunct, the circulator provides a matched termination for image frequency signals which are reflected back from the crystal mixer circuit due to the mixing action of the i-f and local oscillator signals. Therefore, variations in mixer performance which depend on image termination are not a function of the operating frequency.

15.4.1.4 Crystal Mixer

The mixer is a fixed tuned crystal holder. The crystal is matched to the transmission line by a short-circuited stub located in front of the crystal. R-F signals are bypassed to ground through a cylindrical capacitor located at the back of the crystal mouth. The i-f signals are fed through this capacitor and carried out in a miniature receptacle on the side of the mixer. Thus, access to the crystal can be obtained without removing the i-f cable.

15.4.2 Local Oscillator

15.4.2.1 44 mc Oscillator

The oscillator stage is a transistor used in the grounded-collector type configuration. Feedback is through a feedback transformer to the base of the transistor. A quartz crystal oscillator and a series LC circuit are in series with the primary of the feedback transformer. The secondary is a parallel resonant circuit connected to the base of the transistor. The output is transformer coupled to the first amplifier stage for amplification.

15.4.2.2 Power Amplifier

The power amplifier stages consists of Q2, Q3, and Q4. The three transistors are connected in a common collector configuration and are electrically and mechanically connected to the chassis to provide heat dissipation and to eliminate the collector-to-ground capacity that might otherwise exist. The three stages provide approximately 3 watts at 44 mc at the output amplifier Q3.

15.4.2.3 Frequency Doubler

The 44 mc from the power amplifier stage Q4 is applied to a X2, X2, and X2 frequency multiplier chain. The frequency multiplying chain is used to obtain a times 8 multiplication. This chain, which is fed from the 44 mc power amplifier, consists of a four-mesh network, each mesh separated by one of the three varactor diodes. The mesh has a circulating current of basically 44 mc, the second of 88 mc, the third of 176 mc, and the fourth of 352 mc.

15.4.2.4 Harmonic Generator - Times 16

The 350 mc output of the last X2 multiplier is fed into a high order multiplier circuit which utilizes a single varactor diode. The input frequency is multiplied by 16 to an output of 5630 mc. A graded junction silicon varactor diode housed in a microminature, ceramic pill package is used in the multiplier. The output of the X16 multiplier is inductively coupled into a bandpass filter and a resonant power divider. The bandpass filter is tuned to 5630 mc and provides spurious signal rejection. Simultaneously four-way power splitting is also provided by the power divider so that the

local oscillator signal may be fed to the four receiver mixers.

15.4.3 I-F and Lin-Log Amplifiers

15.4.3.1 I-F Amplifiers

The i-f amplifier has a center frequency of 60 mc, a bandwidth of 12 mc, and a gain of 90 db from input to output with a noise figure of 5 db. A gain control is used in each i-f amplifier strip to set the gain of each i-f amplifier nearly constant. The -3 db points of the passband are 54 mc and 66 mc. The -60 db points are 30 mc and 90 mc. The input to the i-f from the crystal mixer is resonated with an inductance to 60 mc. Four stages of amplification are used. The first stage frequency is tuned to 66 mc, the second stage to 54 mc, the third stage to 66 mc, and the fourth stage to 54 mc. Each of the four stages are neutralized to improve stability and reproducibility of the amplifiers. The i-f gain control is located between the second and third stage. The input signal is detected by rectification within the base-to-emitter junction of stage Q3 and Q4, this signal is then processed in the lin-log amplifier. The output of stage Q4 is also applied to a second detector. The second detector output is also applied to the lin-log amplifier network.

15.4.3.2 Lin-Log Amplifier

The lin-log amplifier develops a pulse amplitude (in volts) at its output which is proportional to the input signal strength (in dbm) at the antenna. This output is then utilized in the comparator for comparison with the other three lin-log outputs to determine the strongest of the four signals.

The second detector output produces a pulse voltage at the low signal levels between -70 and -55 dbm at a slope of 50 mv/dbm. The fourth stage emitter produces an output primarily in the range of -55 to -25 dbm at a slope of 60 mv/dbm. The third stage emitter produces an output essentially in the range of -25 to 0 dbm at a slope of 12 mv/dbm.

The desired linear function is derived from these three functions by the process of addition, the fourth stage emitter is added to the second detector output after amplification, and the third stage emitter output is added to the fourth stage emitter voltage after amplification. The third stage i-f emitter output is applied to a buffer amplifier Q51 and then to the input of Q52. At the input of Q52 this signal is combined with the output of the fourth stage i-f emitter. The combined modified signals, at Q52 represent a single slope from -55 to 0 dbm because of the appropriate scaling and amplification of the third i-f stage emitter input (representing -25 to 0 dbm) and appropriate scaling of the fourth stage emitter (representing -55 to -25 dbm).

The combined output is amplified by Q53 and then added at Q54 to the second detector output (representing -70 to -55 dbm). The resulting output of Q55 and Q56 represents a single slope from -70 dbm. Q56 acts as a buffer amplifier and provides a low output impedance for the comparator.

15.4.4 Comparator (Figure 15-3)

The comparator is composed of five main sections, the OR gate, the difference amplifier,

the strobe gate, the monostable multivibrator, the strobe gate generator, and logic gates.

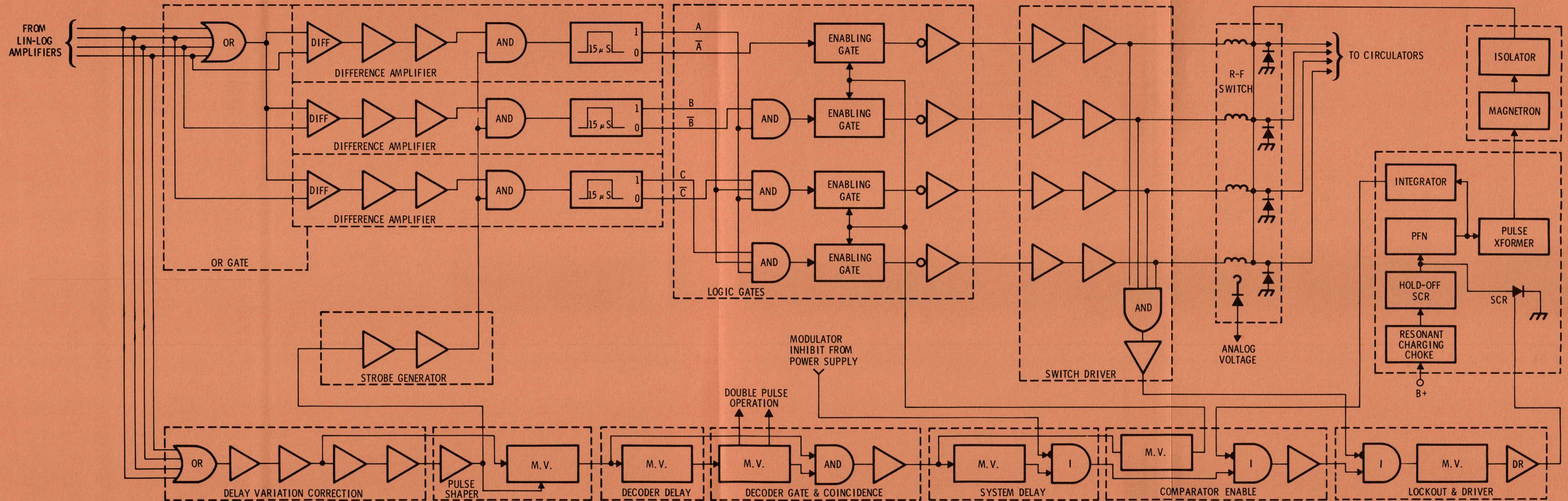
15.4.4.1 OR Gate

This simple four-diode positive gate provides an output which corresponds to the highest input pulse. The four gates are slightly biased on to achieve high sensitivity to low-level pulses. The output of the four-diode gate is fed to the input of the three difference amplifiers. Also feeding into the difference amplifier are the outputs of three of the receivers. The output of the OR gate represents the largest pulse.

15.4.4.2 Difference Amplifier

The function of the difference amplifier is to subtract a receiver channel signal from the output of the OR gate and amplify the subtracted signal sufficiently to trigger the monostable multivibrator. The difference amplifier is composed of three stages. The OR gate output is applied to the base of the first transistor. The output of one of the receiver channels is applied to the emitter. The difference in the two signals applied to the first amplifier is achieved by referencing one signal against the other across the base emitter junction and taking the output at the collector.

The first stage operates approximately linear with a gain of 2. The second stage serves as a voltage amplifier with an approximate gain of 10. The third stage acts as a buffer and provides sufficient gain to drive the "AND" gate. The overall gain of the three stages is approximately 20. For input differences of 100 mv, a 2



FUNCTIONAL BLOCK DIAGRAM, C-BAND TRANSPONDER SHEET 2 OF 2

Figure 15-3

volt signal will be generated at the output.

15.4.4.3 Strobe Gate

The strobe gate is actually an "AND" gate. The output of the difference amplifier and the strobe gate generator are applied as inputs to the "AND" gate. With the coincident arrival of these two signals, a positive pulse is developed and coupled into the monostable multivibrator as the triggering pulse.

15.4.4.4 Monostable Multivibrator

The monostable multivibrator is triggered by the "AND" gate output. The two outputs of the monostable are digital levels used to drive the logic gates which follow. In general the monostable multivibrator converts the analog pulse signal (generated in the difference amplifier and the "AND" gate) into the digital signals required for antenna selection.

15.4.4.5 Strobe Generator

The strobe generator consists of the input transistor and a resonant ringing circuit, with a pulse amplifier. The purpose of the strobe generator circuit is to "slice" or strobe a 0.15 usec pulse from the input pulse on the signal channels. The strobe is located 0.3 usec from the leading edge of the input signal pulse. The pulse is ANDed with the difference pulse in the strobe gate ("AND" gate) thereby ANDing only the center section of the difference pulse. As a consequence, any transients on the leading, or trailing edges of the difference pulse are not sensed. The strobe generator input is received from the shaper circuit. The input

pulse turns off the input transistor, which is normally ON. During the duration of this input pulse, the ringing circuit, at a resonant frequency of 1.6 mc, momentarily rings. At the start of the ring, a positive sinusoidal waveshape is initially developed, followed by the negative portion. The positive and negative signals are inverted in the output amplifier. The negative pulse out of the amplifier are clipped, the positive pulses, however, are allowed to pass to the "AND" gate in the difference amplifier section. Therefore, during the ringing time, the first pulse clipped by the output circuit of the pulse amplifier forms the delay time between the start of the ring and the output pulse. The second pulse is the strobing pulse.

15.4.4.5 Logic Gates

The logic gate assembly consists of four identical direct coupled logic gates. The input digital levels for the gates are derived from the monostable multivibrator outputs. An additional input fed commonly to all gates is derived from the comparator enable circuit and enables all gates for a discrete period of time, thereby setting the position and output pulse width of the gates. The output of the gates feed into the r-f switch drive to provide proper antenna selection.

The logic coupled with the signals present on the monostable multivibrator circuits has been designed to provide a predetermined channel preference. That is, should pulses exist at the input to the difference amplifiers that are equal in amplitude, or indistinguishable by the comparator, one channel will have preference

over the other channel, resulting in the selection of its antenna as follows:

- a. "A" will be selected if signal "A" is equal to "B", "C", "D", or any combination of these.
- b. If "A" is less than "B", then "B" will be selected if it is equal to "C" or "D", or any combination of "C" and "D".
- c. If "A" and "B" are less than "C", then "C" will be selected if it is equal to "D".

This logic network will always assure that one antenna will be "ON" whatever the combination of inputs.

15.4.5 Switch Driver and R-F Switch

The function of the r-f switch driver is to provide proper drive levels for the r-f switch. The switch is composed of four r-f driver stages, one for each pole of the four-pole r-f switch.

The input from the logic gate is a pulse that is present at the time the switch is to be operated. In this manner, a pulse input from the logic gate will be delivered to the r-f switch, turning it off. The magnetron output is connected to the proper antenna, as determined by the logic and switching in the comparator, by the r-f solid-state switch. The pulse supplied by the magnetron is delayed from the start of the drive pulses to provide adequate time for the switch to attain

its proper state. Each arm of the four-pole switch is controlled by an r-f diode, which is characterized by low r-f insertion loss and a capability for passing large amounts of r-f power with moderate back-biasing and without conducting. The switching times of the diodes are well below 0.5 usec, thus supplying a suitable means of rapidly switching to the desired antenna. Each diode is located one-quarter wavelength from the input. The diode when it is pulsed appears as an open to the transmitter input and no r-f transmission occurs in the line associated with the diode. By pulsing three diodes on, the transmitter input will be directed to the remaining line for transmission.

15.4.6 Delay Variation Correction

The problem of delay variation is a function of the r-f signal strength at the receiver input. When required to operate in conjunction with a fixed triggering device, pulses with a finite rise time produce a variation in delay as a function of amplitude. The delay variation correction circuit adds a variable voltage which is a function of the pulse amplitude, to achieve the necessary correction.

Input pulses (0.5 to 10 volts) from the lin-log amplifiers are applied to the input OR gate at the input of the delay variation. The signal is then amplified in the correction amplifier and applied to the emitter of the normally off transistor of the multivibrator. The other output (taken between the second and third stages of the correction amplifier) is applied to the base of the normally on stage of the multivibrator. The pulse applied to the base of

the normally on transistor of the multivibrator instantly turns it off. However, due to a long time constant RC circuit, a ramp function is generated. The ramp function is commuted to the base of the normally off transistor. The normally off transistor of the shaper multivibrator has two signals simultaneously applied, one at the emitter and one at the base. Triggering of the normally off transistor will not occur until the ramp function overcomes the effective back-bias placed on the emitter. In this manner the time location of the output of the normally off transistor is a function of the combined inputs. Since one of the inputs (on the emitter) is proportional to the varying signal amplitude from the lin-log amplifier, it follows that the output of the normally off transistor will be related to the receiver signal strength. The output of the normally off transistor is applied to the decoder. As the pulse on the emitter of the normally off transistor becomes large, thereby corresponding to a stronger r-f signal, the multivibrator triggers the ramp farther back (later in time); and so the multivibrator triggering time is controlled by the correction voltage applied to the emitter of the normally off transistor.

15.4.7 Decoder

The two-pulse decoder generates time slots (decoder gates) which are compared in time to the spacing between the interrogation pulses. An output is provided when properly spaced interrogation pulses appear at the input to a gate in the time coincidence circuit. The decoder will reject interrogation groups spaced outside the code spacing of plus or minus 0.8 microseconds. Pulse code spacing is the time interval from the

leading edge of one pulse of a group to the leading edge of the following pulse in the group. The decoder is adjustable (bench maintenance operation) between 5 and 9.5 microseconds.

During double-pulse operation, the shaper multivibrator output pulses are applied to the decoder delay multivibrator. The decoder multivibrator is a monostable circuit that has an adjustable output pulse. The width of this output pulse is determined by a potentiometer in conjunction with a capacitor that can be adjusted from 4 to 10 usec.

The output of the decoder delay is coupled to the decoder gate. The output of the decoder delay is a positive pulse and the decoder gate triggers on the negative going part of the positive pulse. The decoder operation is performed by: (1) triggering the decoder delay multivibrator with the shaper output, (2) triggering the decoder gate multivibrator with the trailing edge of the decoder delay multivibrator, and (3) obtaining time coincidence between the decoder gate multivibrator and the second shaper pulse in the "AND" gate.

For single pulse operation, an external switch removes the connection between the two lines connected at the decoder gate multivibrator, disabling the decoder gate multivibrator.

15.4.8 System Delay

The system delay permits the overall transponder delay between the r-f interrogation pulse and the transponder reply pulse to be set to 3.0 plus or minus 0.1 microseconds at -40 dbm input signal level.

The system delay serves two purposes: (1) provides the desired separation of the transponder reply from the radar (skin) return, and (2) provides the required delay to permit selection of the proper r-f switch path by the comparator. Variable system delay is obtained by: (1) triggering the monostable multivibrator from the decoder "AND" gate, (2) differentiating the resultant positive output pulse, (3) selecting the resultant negative pulse (trailing edge) and (4) triggering the monostable multivibrator in the lock-out and driver assembly.

A dc modulator inhibit function is provided at the output of the system monostable multivibrator circuit. The inhibit function is active during the 40 second magnetron filament warm-up time and during the power supply fail safe circuit.

15.4.9 Comparator Enable

The comparator enable circuit assures that antenna switching occurs only for properly coded signals. The comparator enable multivibrator is triggered from the decoder gate and prior to the time (due to system delay) the transmitter is triggered.

15.4.9.1 Overinterrogation

The inhibit gate in the comparator enable assembly protects the transponder from damage resulting from excessively high pulse repetition frequencies by initiating countdown at a PRF greater than the nominal 1500 pps rate. An integrator circuit is located in the modulator produces a dc voltage directly proportional to the PRF. If the PRF exceeds 1500 pps rate, sufficient voltage is

routed to the inhibit gate in the comparator enable assembly to enable the inhibit gate.

15.4.10 Lockout and Driver

The input to the lock-out multivibrator is a pulse modulator inhibit circuit. If through a malfunction four output "OFF" pulses are delivered from the comparator driver, the r-f switch can be damaged by the transmitter output. The pulse modulator inhibit prevents the triggering of the magnetron transmitter during this malfunction. The inhibit voltage which provides this protection is delivered by an "AND" gate connected to the output lines of the switch drivers.

The lockout multivibrator (a monostable circuit) prevents the modulator from being triggered during the transmitter recovery period. Once the multivibrator fires, it cannot be retriggered until it returns to the nonoperating state; adequate modulator lock-out is assured by setting the circuit time constant for 70 usec (modulator recovery time).

The output of the lock-out multivibrator is applied to the modulator driver. The output pulse of the lock-out multivibrator saturates the modulator driver supplying a pulse to the modulator.

15.4.11 Modulator

The modulator is composed of a dc resonant charging circuit, a pulse-averaging circuit, and an anti-leakage circuit.

The dc resonant charging circuit consists of a pulse forming network (PFN), dc

resonant charging choke, a hold-off SCR, a modulator transformer, and a pulse-forming network discharge SCR. The modulator B⁺ charges up the pulse forming network (the PFN is composed of series and parallel connected inductances and capacitors) to approximately twice the applied B⁺ voltage because of the dc resonant charging action. When the modulator driver turns on the discharge SCR, the PFN discharges and a large voltage is produced across the pulse transformer. The pulse transformer provides the necessary matching between the characteristic impedance of the PFN and the magnetron. The turns ratio produces approximately 5,000 volts and a current of approximately 4.5 amps to flow in the magnetron secondaries.

15.4.12 Transmitter

The transmitted pulse r-f energy is provided by a magnetron-isolator unit. The output of this unit is fed directly to the input port of the r-f solid-state switch. The power output is 5.0 kw minimum to assure minimum transponder output power of 2.5 kw. Insertion losses between the unit and the transponder output are presented by the r-f solid state-switch, the coaxial cabling, and the ferrite circulator.

15.4.13 Power Supply (Figure 15-4)

The simplified block diagram of the power supply is shown in Figure 15-3. The power supply transformer is a three-phase, 115 volt, 400 cps transformer. The primaries for each phase are connected in "Y". The large power secondary, such as the modulator supply, -27 and +6 volt filaments are connected in Delta.

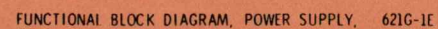
This permits the system to operate with one phase open.

The modulator supply is an adjustable transistor-regulated supply. The modulator leakage supply is a full-wave rectified supply added to the modulator B⁺ supply.

The short sensor is located on the modulator B⁺ supply which senses whether or not a short has developed on the line. If a short does occur, it immediately commands the modulator B⁺ return switch to turn off, thereby disconnecting the return loop of the supply. This return switch is also used to turn on the modulator supply only after the magnetron filaments have properly heated. The time delay and modulator inhibit circuits safeguard the modulator during warm-up of the magnetron filament.

The remaining voltages generated by the power supply are -27, -54, +10, -10 and 6 volts.

Consider the operation of the power supply at Turn-On. The voltages immediately present are the 6, -27, -54, +10, -10 and +20 volts. The modulator supply and the leakage supply are held off. The binary, or flip-flops, within the power supply are forced into a particular state, thus inhibiting the modulator. Two pulses are needed for the relaxation oscillator to change the inhibit state. After the initial warm-up time, the relaxation pulse oscillator is activated; and it turns on the modulator low-voltage and leakage supply. The first pulse from the relaxation oscillator causes a change of state in the flip-flops. Approximately 3 seconds later, a second pulse is emitted which causes the flip-flop to



CD-192 ◆

figure 15-4

again change state. This change of state removes the modulator inhibit. The short sensor, when activated, produces a reset pulse which once again changes the state of the flip-flops and pulses the modulator B+ return switch open.

The B+ to the modulator must be turned on prior to the trigger signal being applied to the modulator. This enables the dc resonant charging circuit within the modulator to charge the PFN. Once the PFN is charged, the modulator is set for operation. The PFN must be charged before the modulator inhibit pulse is removed. This is removed by the flip-flop after the finite delay which is caused by the first flip-flop in conjunction with the relaxation pulse oscillator.

SECTION XVI

DIGITAL UP-DATA LINK EQUIPMENT

16.1 INTRODUCTION

Up-data is a term given to information sent from the ground station to the spacecraft for the purpose of up-dating information in the S/C systems. The Digital Up-Data Link Equipment (UDL) receives digital data from the ground stations via the UHF/FM RCVR or USBE, verifies it, determines the system for which it is intended, and directs it to that system. The UDL System, Figure 16-1, consists of a receiver unit, detector circuitry, a decoder-buffer storage unit and output relay driver transistors.

The receiver reduces the 450 mc signal input to 0 to 4000 cps intelligence for processing in the detector and decoder units. High gain and low noise transference are the major advantages of the receiver.

In the detector, the digital information is separated from the signal sent in by the receiver. This is accomplished by two phase detectors and a vco.

Bits are fed from the detector to the decoder where vehicle and system addresses are recognized. Timing signals are generated here also. The output digital information is fed to the proper location as per system address.

16.2 OPERATION - NEAR EARTH

16.2.1 Receiver

The transistorized, double-conversion superheterodyne receiver accepts and demodulates

the 450 mc fm signals. The rf input signal is fed into a three-section preselector cavity which includes a tunable band-pass section and a low-pass filter. The band-pass section consists of two coupled coaxial cavities with adjustable capacitive loading for tuning. In Figure 16-2 these circuits are grouped under the general block labeled rf preamplifier. The first diode mixer converts the modulated signal to the first intermediate frequency of 72 to 81 mc. A crystal controlled oscillator, tuned to a frequency between 83 and 92 mc determines the frequency to which the receiver is tuned.

The first i-f amplifier consists of two stages with a 30 decibel gain. Insertion loss from the pre-selector and the first diode mixer, plus the first i-f amplifier noise figure, gives a noise figure to this point of about 12 db. The receiver's sensitivity is such that an rf input power of -129 dbm will yield a message error rate of not less than 1 error in 1000 input pulses. From this point the signal is mixed with the local oscillator basic frequency in the second mixer. This gives a second i-f frequency output of 10.7 mc to the i-f filter and the second i-f amplifier. The signal now passes through a limiter and the intelligence is detected in the discriminator circuit. The audio amplifier conditions the intelligence for further use by establishing a maximum frequency output of 4000 cps. Through the mode switch the signal is fed to the sub-bit detector.

16.2.2 Sub-bit Detector

The sub-bit detector, Figure 16-3, accepts the output of the receiver section, a phase modulated 2000 cps together with a 1000 cps sync tone as shown

UP-DATA LINK BLOCK DIAGRAM

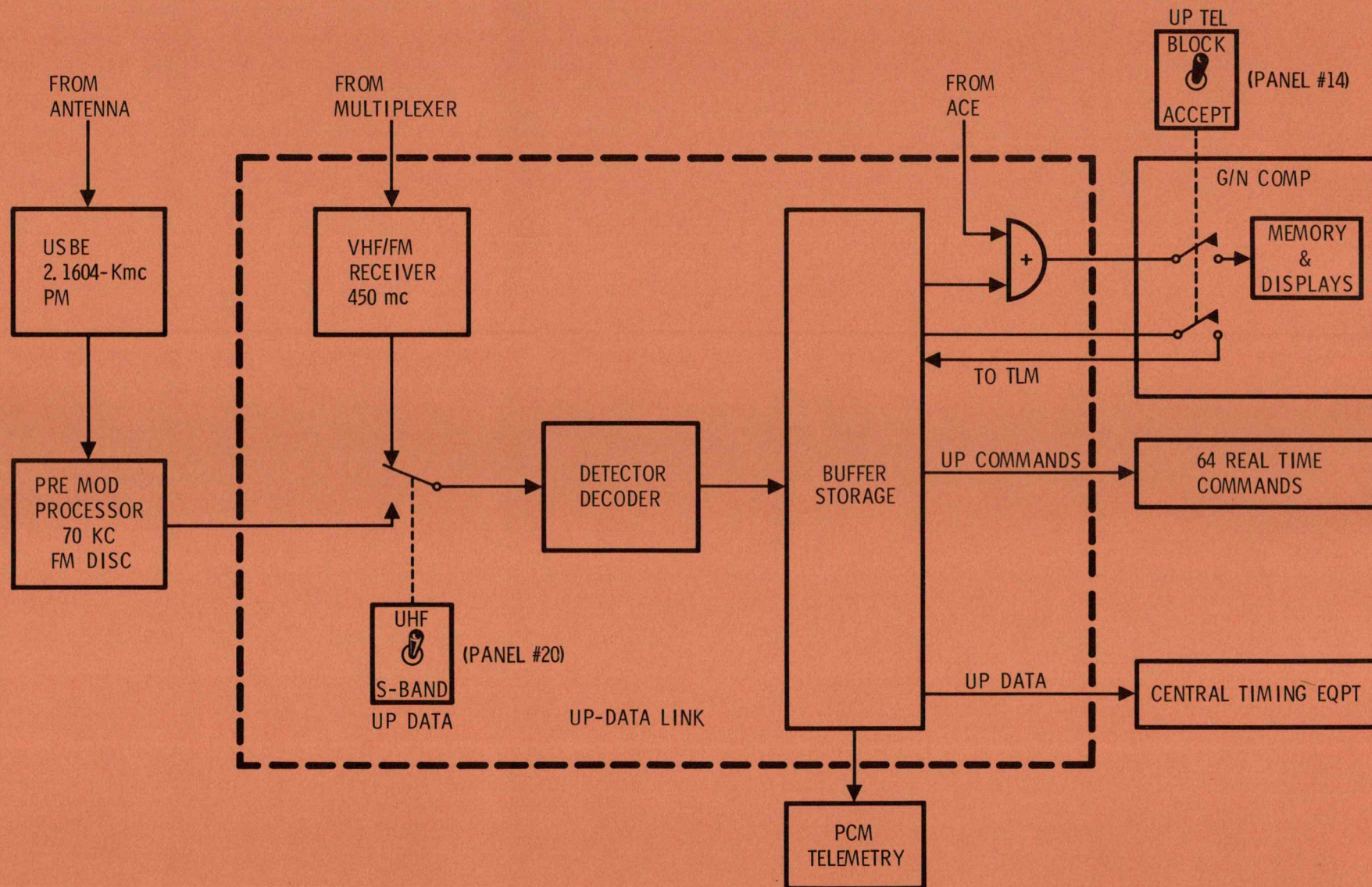


figure 16-1

CD-105C



UHF UP-DATA LINK RECEIVER

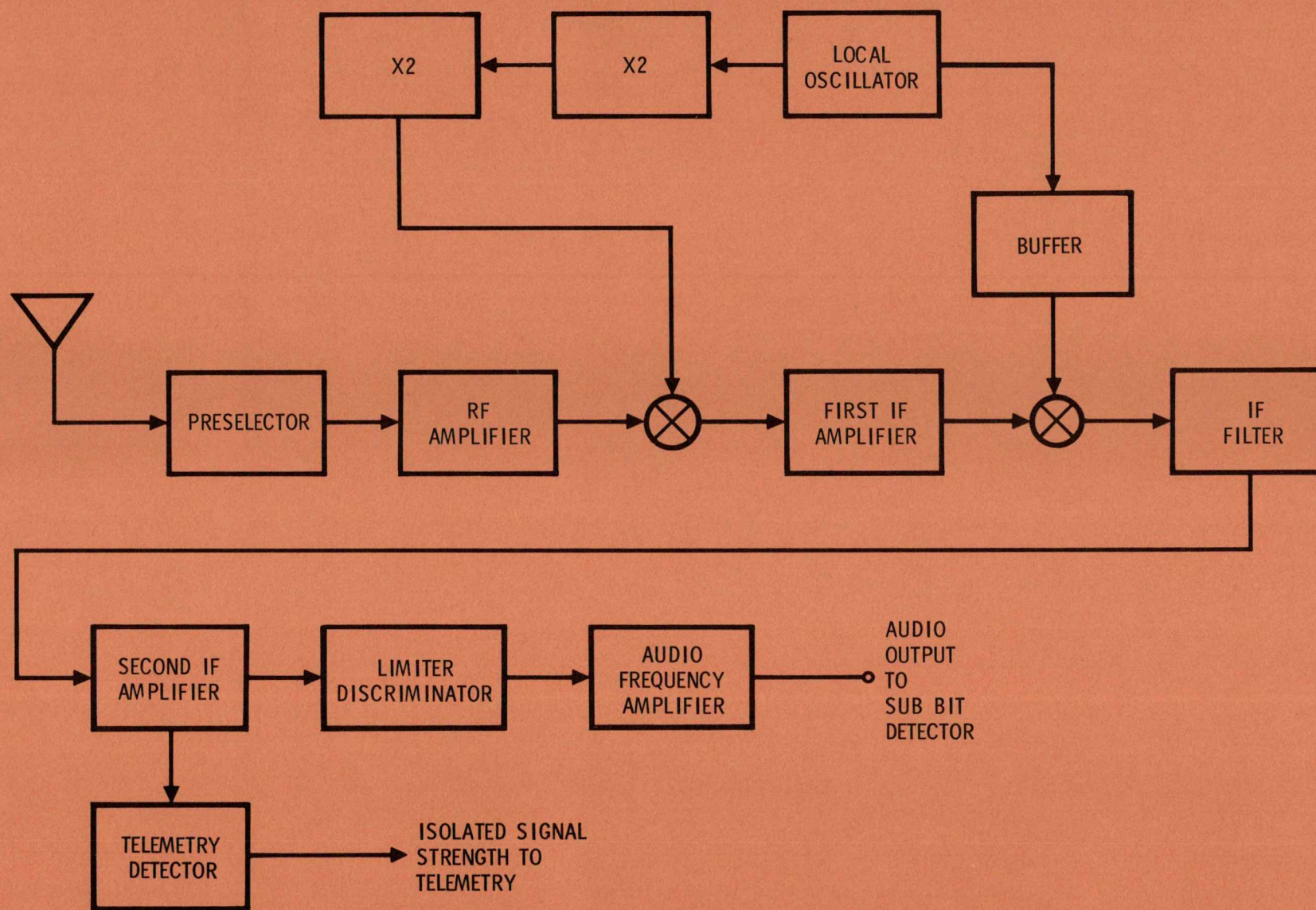
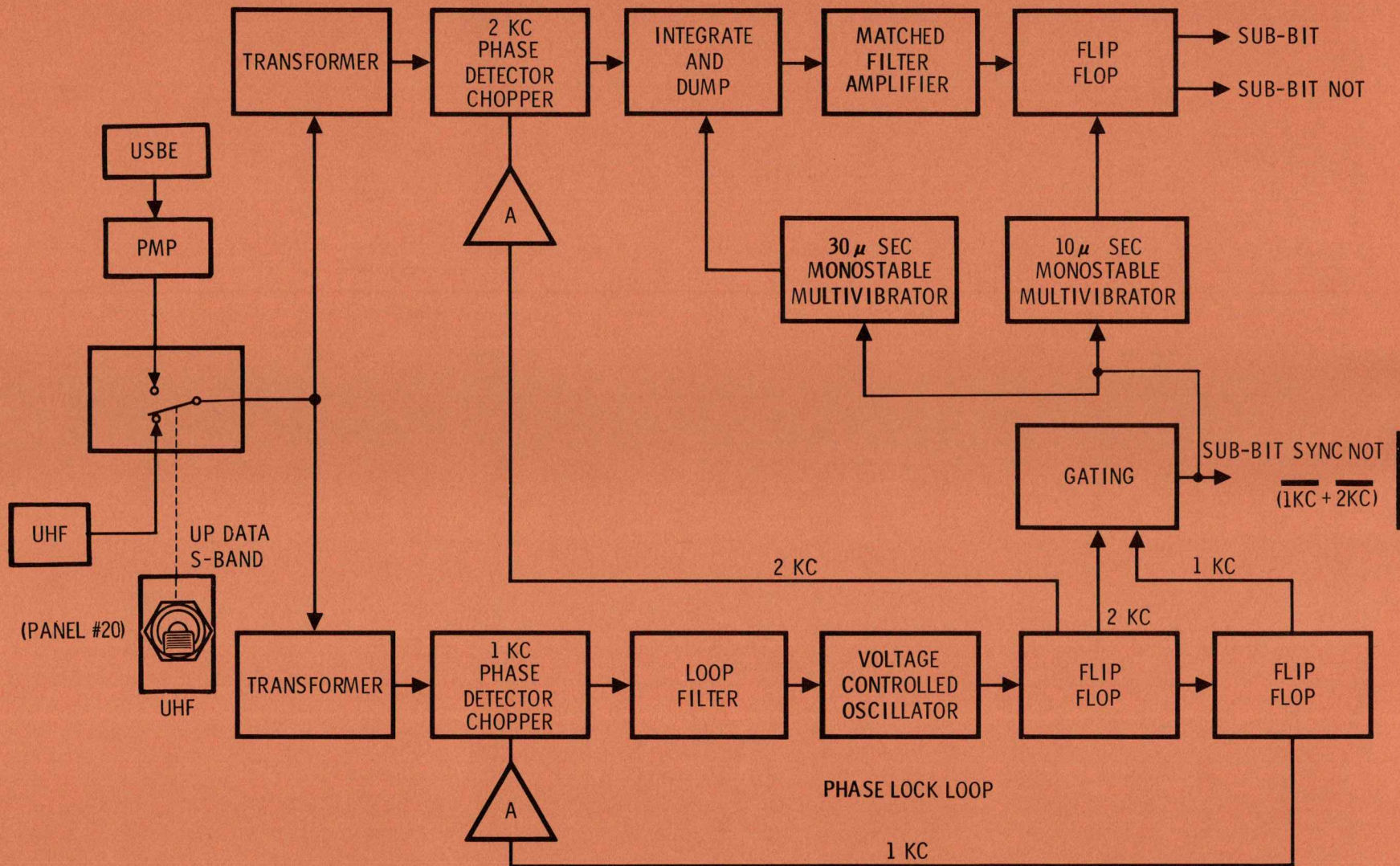


figure 16-2

SUB-BIT DETECTOR



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figure 16-3

CD-101C



16-4

in Figure 16-4. The signal feeds two phase detectors. The lower detector in the diagram compares the input signal to the one kc vco signal. The vco puts out four kc but the signal is divided by two in flip-flop circuits twice, bringing the signal to one kc. The phase detector controls the vco frequency through the loop filter. From the first divide by two flip-flop, a two kc signal is fed to the second phase detector. When the reference signal is in phase with the 2000 cps component of the input, a logic "1" will be sent out of the detector. When the input is out of phase with the reference, a logic "0" will be the output.

16.2.3 Decoder

The decoder detects the vehicle address and system address, stores and checks digital data and processes the data to the appropriate spacecraft system. The decoder has four functions:

1. Enters serial data into the Apollo Guidance and Navigation Computer (G/N)
2. Provides real time commands (RTC) to turn spacecraft equipment on or off by ground control.
3. Verify a test message (T/M) for UDL self-test.
4. Update time accumulator in (CTE).

All words, RTC, G/N, CTE, and T/M are composed of three vehicle address and three system address data bits. The remaining data bits, 6 for RTC, 16 for G/N, or 24 for T/M and CTE comprise respectively, the real time command, a computer

word, a CTE word or a test message. Each of the information bits are coded to a five sub-bit code. The decoder is divided into five basic sections:

1. Bit detection and basic timing generator
2. Address recognition
3. Programmable timing generator
4. Data buffer storage
5. Real time command detector

The functions of each section is described in the following paragraphs. Figure 16-5 shows the logic circuit for the decoder.

16.2.4 Bit Detection and Basic Timing Generator

The detected sub-bits (data and sync signals) are used to clock the nonreturn-to-zero (NRZ) sub-bit information into a five stage register. This register is sampled to determine if a bit "one", or "zero" is present. If the bit recognition occurs during an invalid time, the system will automatically be reset. Basic timing is used to generate program timing. Generation of basic timing consists of dividing the sync signal by five to produce a bit sync reference signal, starting at bit recognition time. Bit values "one" and "zero" are fed to the 24 bit storage data register.

16.2.5 Address Recognition

Vehicle address and system address are coded into six information bits (first three for vehicle address, next three for system address) allowing the selection of any one of eight possible vehicles and

UP-DATA LINK MODULATION

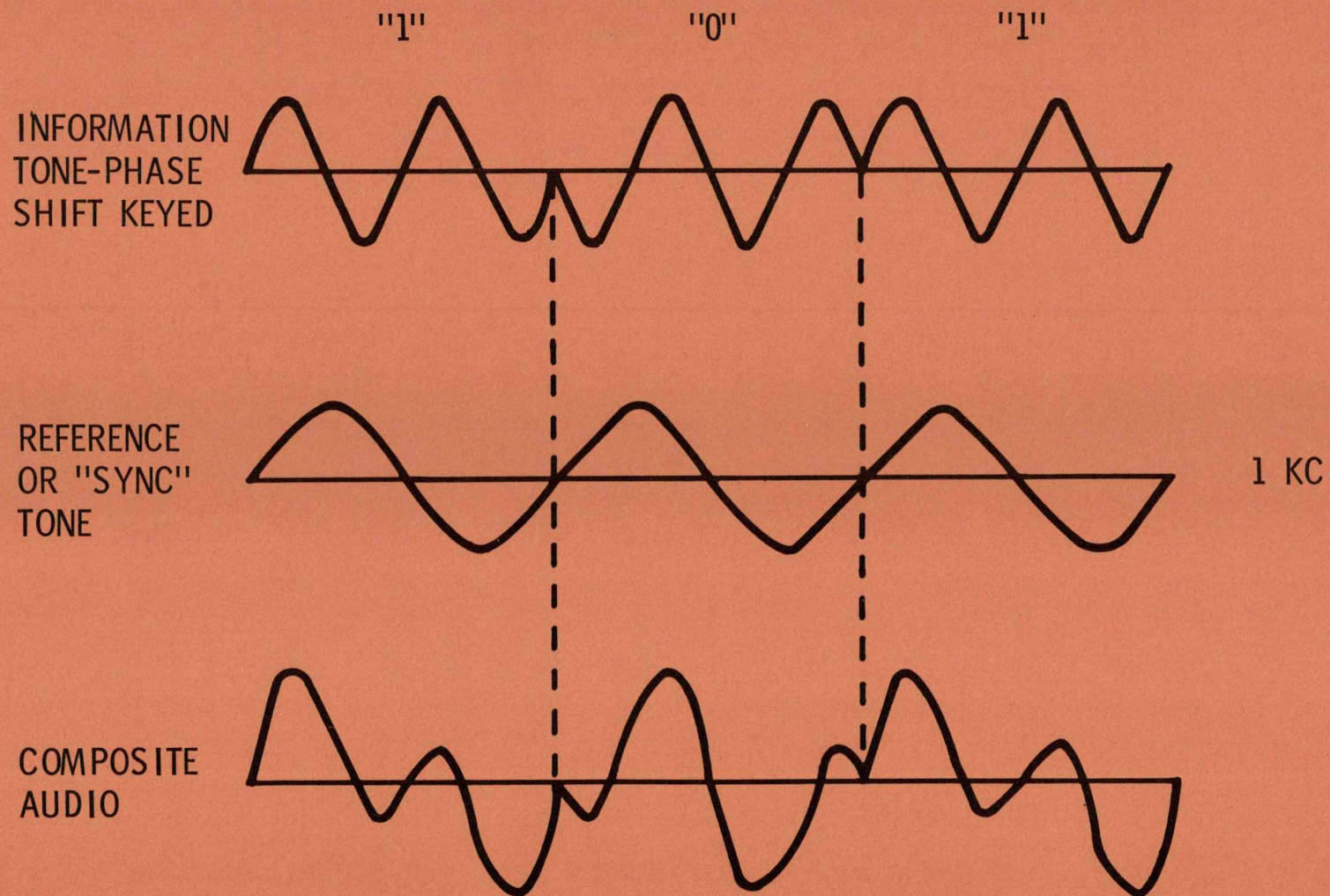


figure 16-4

CD-104A



16-6

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CD-102D

eight possible systems. System address is recognized after the proper vehicle address has been received and three information bits are stored in the data register. Decoding and storage of the system address is performed using clocked techniques. Stored system address determines program control operation and is required to enable data transfer function.

16.2.6 Programmable Timing Generator

The digital up-data-link has the capability of handling three different length commands; these may be 12, 22, or 30 bits long. The program timing system senses from the system address the correct command length and provides timing to control reception, data transfer and verification in the proper sequence.

16.2.7 Data Buffer Storage

Data storage is provided to hold an incoming command until processing and verification is complete. The data register also provides storage for addresses and real-time commands until decoding or output actuation is completed. Data bits are shifted serially into the 24 bit data storage register by clock and gating pulses received from the basic timing generator and program timing system. The data is serially shifted out to the using system at a 1 kc rate.

16.2.8 Real-Time Command Detector

The data register provides six bits to the real-time command decoder. The first four bits received select one of 16 relay drivers in the UDL and the last two bits determine the "on" or "off" condition selected. (The relays used in the BME are dual coil magnetic latching relays.) The set and reset drivers are capable of providing a minimum of 10 milliamperes into a load impedance between 900 and 1600 ohms.

16.3 CODING

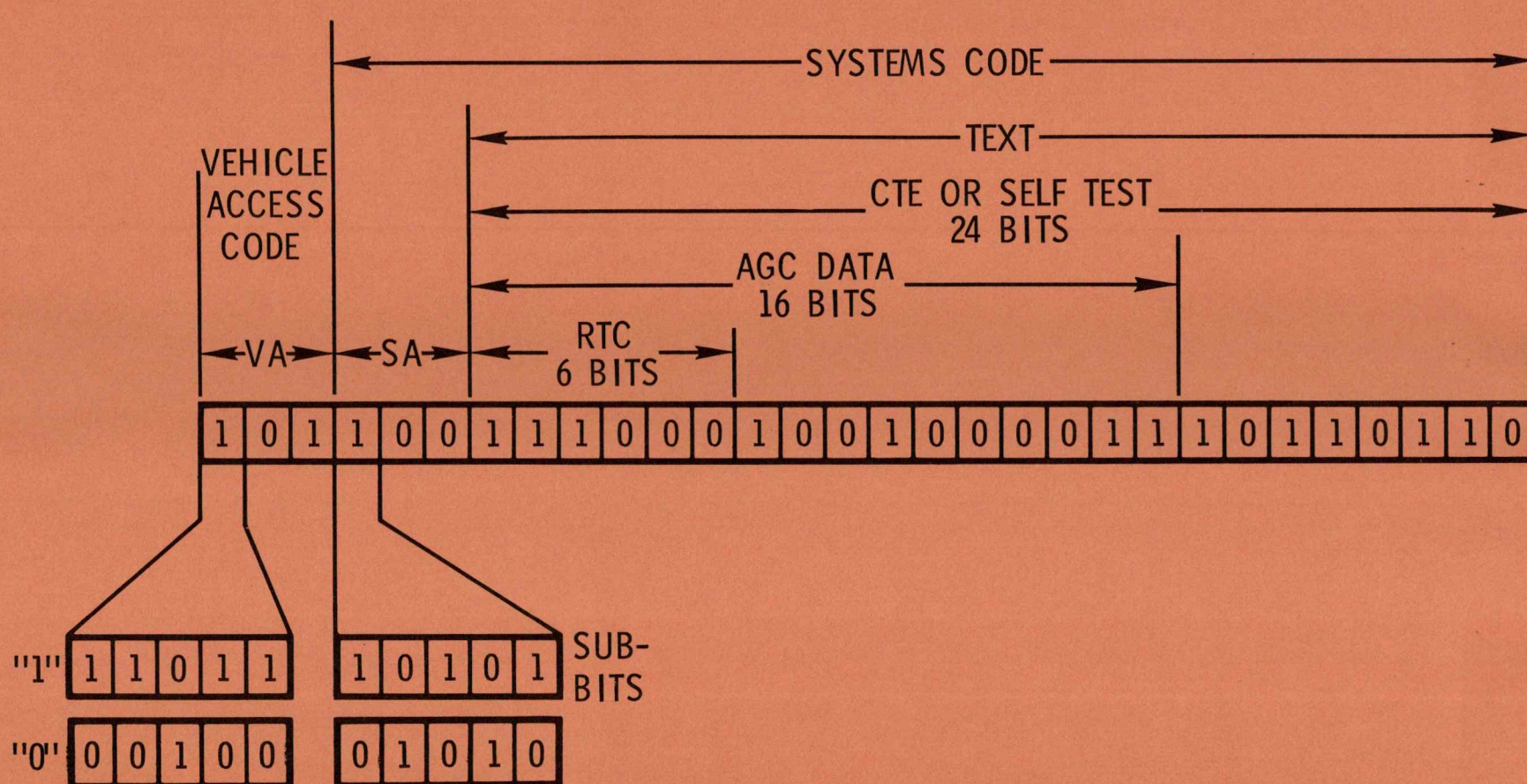
The UDL is capable of receiving a message composed of 150 sub-bits. As explained above, the code consists of five sub-bits per information bit. Each message addressed to the system contains up to 30 information bits. The first three information bits of each message are used as the vehicle address (VA). The next three information bits are used as the system address (SA), and the remainder of the bits in each message represent the data word. The VA code is termed the "access code". The SA code and data word are termed the "SYSTEMS CODE". (See figure 16-6 for clarification.)

The composite signal frequency which modulates the uhf carrier consists of the linear sum of a 2 kc information tone and a 1 kc coherent synchronization tone. The 2 kc tone is phase-shift keyed at a binary rate of 1 kc. Phase-shift keying consists of phase shifting the 2 kc tone by 180 degrees with respect to the 1 kc sync tone. If the 2 kc tone and the 1 kc tone are in phase, this represents a binary one. If the 2 kc tone is 180 degrees out of phase with the 1 kc tone, this represents a binary zero.

16.4 OPERATION - DEEP SPACE

The operational mode of the UDL just described is used for the earth-orbital and near-earth phases of the lunar mission. For the translunar and deep space operation, the 2 kmc Unified S-Band Equipment replaces the internal UDL receiver. The 2 kc information tone and the 1 kc sync tone are used to frequency modulate a 70 kc subcarrier. This subcarrier is then used to modulate the 2 kmc carrier from the S-Band Transmitter. On board the spacecraft, the frequency modulated 70 kc subcarrier is stripped from the 2 kmc carrier in the S-Band Transponder and

UP-DATA LINK MESSAGE FORMAT



16

figure 16-6

CD-162A



is then sent to the Pre-Modulation Processor. The Pre-Modulation Processor demodulates the 70-kc subcarrier; the resultant composite audio is sent to the UDL sub-bit detector and decoder. From this point, the operation of the UDL Equipment is identical to that described for the near-earth phase.

16.5 DETAILED CIRCUIT DESCRIPTION

The preceding section discussed the Apollo up-data link in fairly general terms, elaborating more on the functional aspect of the system rather than the system's physical operation. This section will describe the detailed operation of the circuits and subassemblies that make up the UDL.

16.5.1 UHF Receiver

The UHF receiver (shown in Figure 16-2), used on the Apollo command module as described in section 16.2.1 is a modified unit presently being used on the Gemini program. It consists basically of five assemblies. These are:

1. Tune cavity pre-selector.
2. RF Amplifier
3. First IF amplifier
4. Band-pass Filter
5. Second IF amplifier

The receiver is all transistorized and operates off of -18 and -6 volts d.c. The output is a composite audio signal of a linear summed 1 kc and 2 kc tone. In addition, the receiver signal strength is monitored in the second IF assembly and sent to the PCM/TLM system for transmission to ground stations.

16.5.1.1 Tuned Cavity Pre-Selector Assembly:

The tuned cavity pre-selector consists of two tunable bandpass sections are tuned to the receiver operating frequency while the low pass section is tuned to reject high frequencies. The coaxial connector to the receiver is an integral part of the pre-selector.

16.5.1.2 RF Amplifier Assembly:

The RF amplifier is an addition to the Gemini UHF receiver design. This amplifier allows a 6 dbm improvement in receiver sensitivity and yields approximately 4 db improvement in noise figure. This assembly is a two-stage amplifier using 2N2415 grounded emitter transistors. The amplifier is tuned by adjustable capacitors in a collector LC network. A resistor divider network is used to set bias levels of the amplifier stage and transformed coupling is employed between each stage and to the first IF.

16.5.1.3 First IF Amplifier Assembly:

The first IF assembly consists of a crystal controlled colpitts type local oscillator, two frequency doublers, three stages of amplification, a buffer amplifier, and mixer.

A crystal controlled local oscillator (LO) which can be tuned to any frequency in the range from 83 to 92 mc is used and the choice of the local osc crystal frequency determines the operating frequency to which the receiver is tuned (400-450mc). The LO frequency is quadrupled before injection at the first mixer. The exact IF frequency is therefore, determined by the Frequency of the incoming RF signal and the setting of the local Osc. Grounded base inductance tuned emitter and collector amplifiers are employed. The LO output is also fed to a buffer amplifier and to a second mixer to yield a second IF frequency of

10.7 mc. The output of the 10.7 mc amplifier is fed to a bandpass filter. The IF amplifiers are broad tuned while the bandpass filter is narrow band tuned. This means that the receiver selectivity is governed primarily by the filter characteristics. The IF bandwidth of the receiver is not less than 220 kc at the minus 3 db points and is not greater than 1200 kc at the minus 60 db points.

16.5.1.4 Bandpass Filter:

The bandpass filter is a lumped constant L-C filter with a 3 db bandwidth of approximately 200-250 kc. It has a 1 mc bandwidth at the 60 db point. The filter insertion loss is less than 15 db with a 50 ohm input impedance and loaded by a 20 ohm input impedance of the second IF amplifier.

16.5.1.5 Second IF Amplifier Assembly:

The second IF amplifier assembly consists of three stages of amplification prior to the limiter, a limiter and Foster-Seeley type discriminator and two stages of audio amplification. The 10.7 mc IF amplifiers provide approximately 60 db of gain to the limiter. The tuned circuit in the limiter collector serves as the discriminator. Two adjustable indicators (primary and secondary) are independently tunable to allow optimum sensitivity and linearity of design. The discriminator is followed by two stages of audio amplification using feedback techniques to insure stability. Provision is made to set the output audio voltage at 1 volt $\pm 10\%$ by selection of the gain resistor in the input circuit of the audio amplifier.

16.5.2 Sub-Bit Detector

The primary function of the sub-bit detector in the Apollo UDL is to separate the data from the

sync tones and transfer these sub-bits to the decoder for decoding, verification, and transfer to the user system. Inputs to the sub-bit detector may be from either the UHF receiver or from the pre-modulation processor. Both inputs are fed through a mode switch which can be externally controlled from the astronauts control panel.

16.5.2.1 Sync Signal Detection

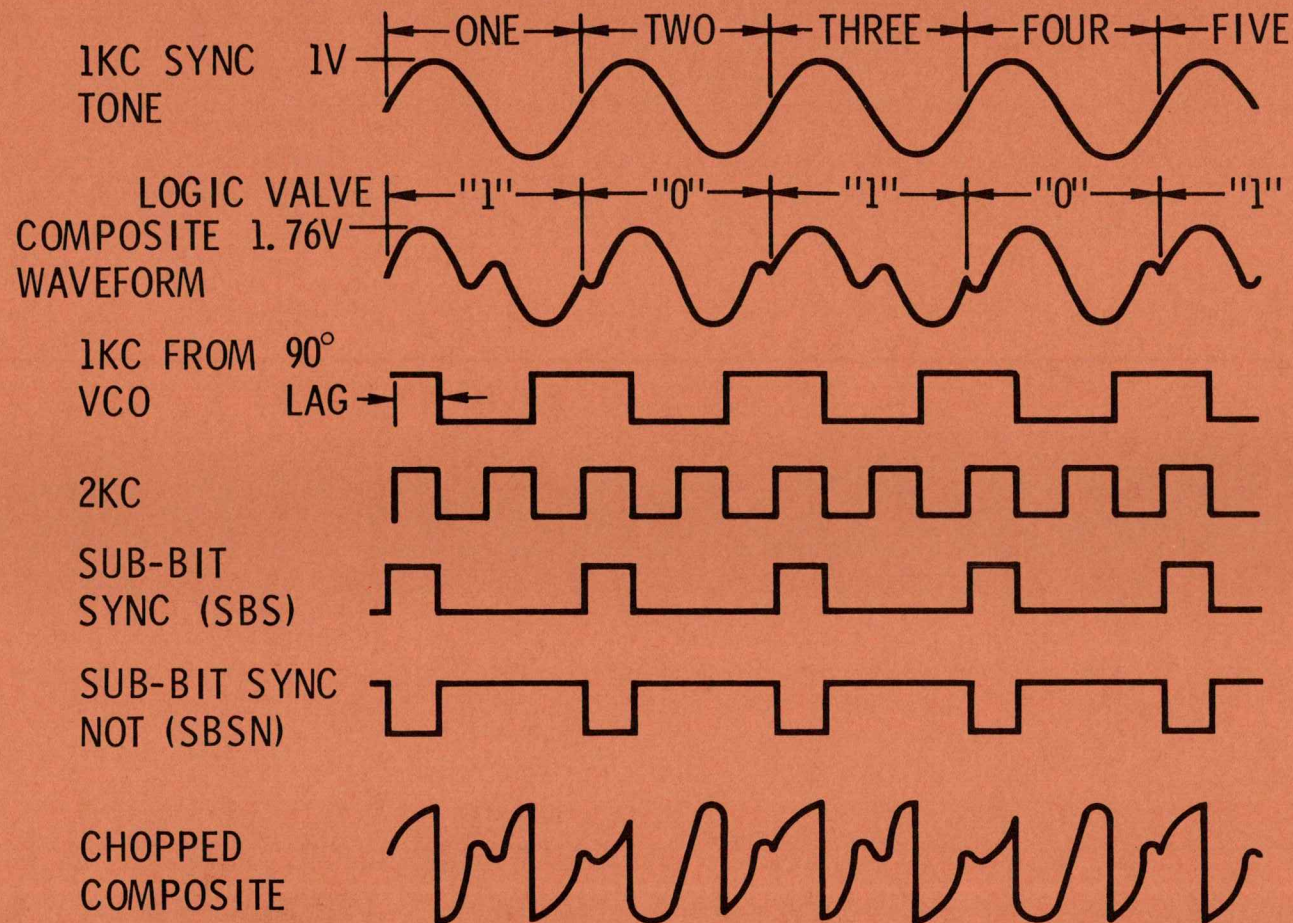
The sub-bit detector utilizes a 4 kc voltage controlled oscillator (VCO) which is used to mix with the incoming data and sync signals for detection. See Figure 16-7. The 4 kc is divided first by two and then again by two to yield a 1 kc square wave signal 90° out of phase with the incoming 1 kc sync signal. The phase detector in the sync circuit, made up of a transform (center tapped) and a chopper amplifier, detects the 1 kc reference and 1 kc sync signal. Any difference in phase will produce a d-c voltage at the center tap of the transformer which is fed to the loop filter. This voltage after being filtered is used to vary the VCO and correct for the phase difference. This lock of the VCO reference to the 1 kc sync must be accomplished prior to any data detection. Once lock is accomplished, the 1 kc reference signal is inverted and fed to the decoder for use there. The 2 kc square wave is fed to an OR Gate and gated to the decoder by the 1 kc square wave to generate the sub-bit-sync-not (SBSN) signal.

16.5.2.2 Information Signal Detection

The information signal detector also utilizes the transformer-chopper technique but now the 2 kc square wave generated by the VCO is in phase with the information signal (2 kc). See Figure 16-8. When the proper phase relationship is achieved, the data is fed to an integrator and dumped at a 1 kc repetition rate. This dump signal is generated by a

WAVEFORMS OF SUB-BIT DETECTOR

(PHASE LOCKED LOOP PORTION)



WAVEFORMS OF SUB-BIT DETECTOR

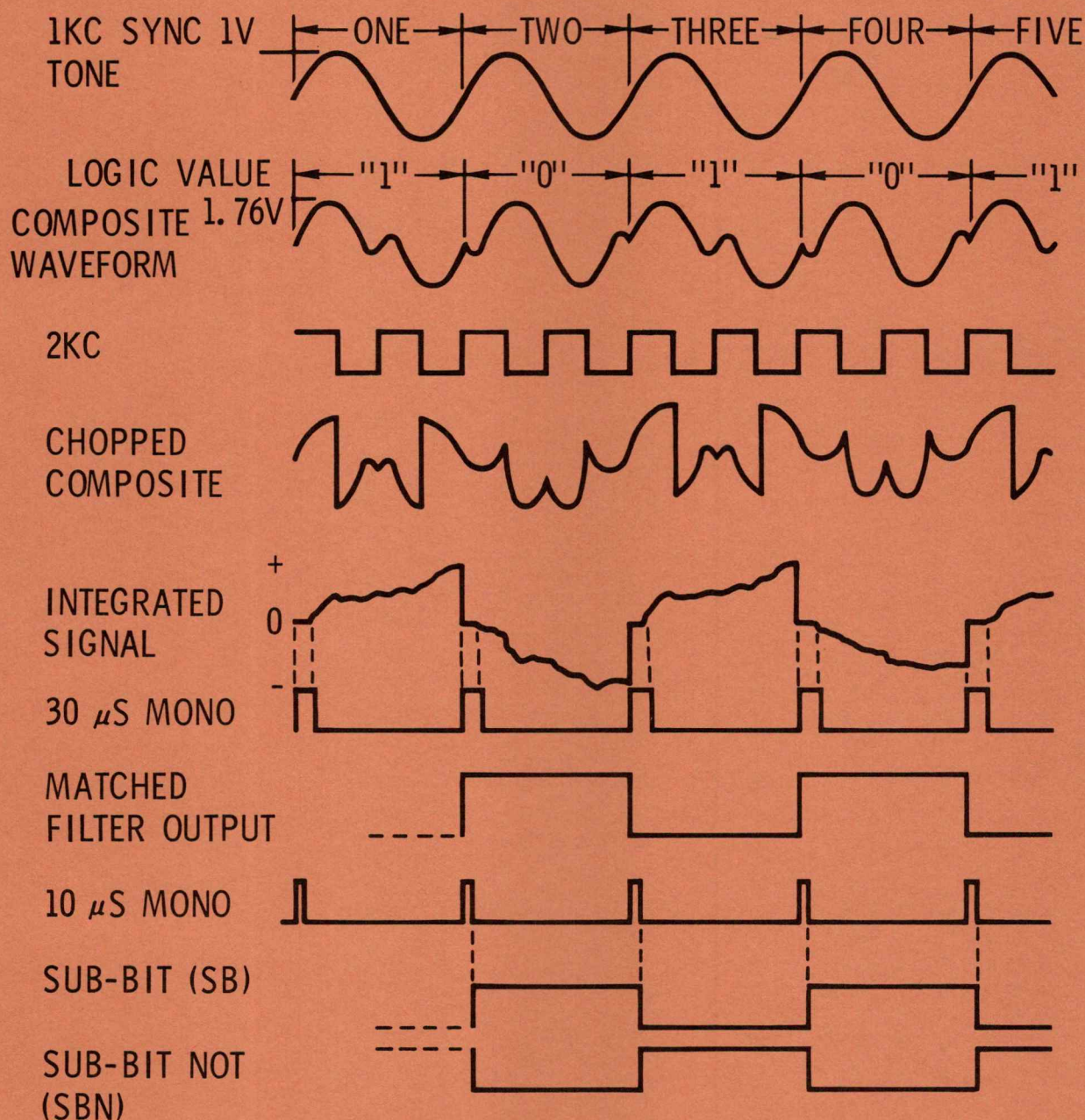


Figure 16-8

30 microsecond monostable multivibrator triggered by the SBSN. The input signal to the matched filter amplifier is a narrow pulse whose polarity is determined by the integrator voltage. The output of the matched filter is fed to the first stage of the sub-bit decoder register located in the sub-bit detector and triggered by a 10 microsecond monostable which in turn, is triggered by SBSN. This is a different design than that used by the Gemini sub-bit detector which does not use the sub-bit detector flip-flop as the first stage of the decoder register.

16.5.3 Decoder:

16.5.3.1 Description of Sub-Assembly Functions as they apply to the Integrated System:

Refer to Figure 16-9

16.5.3.2 Sub-bit Detector

Five sub-bits are necessary to decode each information bit. The sub-bits are shifted serially into the sub-bit register. As each group of five sub-bits are shifted into the register they are sampled in parallel form. Outputs of two NAND gates are used as steering levels to shift the bits into the main register. This sampling load pulse will shift the decoded levels into the main bit register.

The first three stages of the main bit register are continuously monitored by eight NAND gates. These gates monitor all eight possible states of the first three stages. Before the vehicle is launched, the output of one of these gates will be connected as a steering level to the vehicle flip-flop. If this unique vehicle address is properly decoded, a level will be established at the vehicle FF such that it is qualified to be set by a divide by 5 counter in the sub-bit decoder.

As the vehicle FF is set, it causes three things to occur:

1. It loads a count of three into the programmable counter.
2. It "enables" the gate which passes shift pulses to the programmable counter.
3. It switches the two sub-bit decoding gates to two other sub-bit decoding gates and consequently selects a different code for the logic one and zero bit levels.

The third count of the programmable counter causes a divide by two counter to count "one" which loads the system address into the main storage register. There are eight storage FF in the register and the one corresponding to the system selected will be set.

16.5.3.3 RTC System

The RTC system will be selected if S7 FF is set. The following sequence of events will occur. The programmable counter will be loaded with a count of six. As the programmable counter counts six, it causes a divide by two counter to count to two. This inhibits any further shift pulses to the main bit register. It also energizes the proper relay in the relay decoding matrix. It also resets the main bit register which loads a count of 32 into the programmable counter. The RTC relay selected will remain energized until the programmable counter reaches 32. At count 32, the programmable counter causes CR Count Rate not to make it's third negative transition. This enables A21 (reset gate) and as CR goes to +6 volts, it resets the sytem.

16.5.3.4 G/N Interface

The G/N operation is similar for the vehicle and system address as that described for an RTC word

UDL DECODER LOGIC

This figure will be given as a separate handout.

Figure 16-9

CD-1010

with the exception of the system selection. When the G/N system is selected, it loads the programmable counter with a count of 16. This clocks in the 16 information bits of the G/N word into the main bit register.

At the count of 16, the last data bit has been placed in the register and \overline{CR} from the programmable counter makes its second negative transition. Also, the generation of PG Pulse Generator pulses are changed from BSN Bit Sync Not (200 cps) to the 1 kc dependency and the programmable counter is reset to count 32 additional pulses of PG. The first 16 of these 32 pulses serially clocks out the data through DR16 at a 1 kc rate. At count 32 of the programmable counter, \overline{CR} makes it's third negative transition and resets the system.

16.5.3.5 CTE Operation::

The CTE operation is similar for the vehicle and system address, to that described for an RTC word with the exceptions of the system selection and also inhibiting the system resetting function at the third negative transition of \overline{CR} .

When the CTE system is selected, it loads the programmable counter with a count of 24. This clocks the 24 information bits of the CTE word into the main bit register at negative transitions of BSN (200 cps).

At the count of 24, the last information bit has been clocked into the register and \overline{CR} from the programmable counter makes it's second negative transition. Also, the generation of PG pulses are changed from BSN (200 cps) to the 20 kc astable dependency causing PG to have a 10 kc frequency rather than 200 cps.

As \overline{CR} returns to +6 V, it sets the RA FF. This causes the following events to occur: The output to the CTE "seconds" line is enabled; the shift pulses to the main bit register are disabled. The first six information bits which have been shifted into DR19 through DR24 are parallel dumped into the programmable counter.

The counter counts the 10 kc pulses until it reaches the programmed count. During this time these pulses are output over the CTE "seconds" line until \overline{CR} goes to 0 V, which causes the RA FF to be cleared. This inhibits all output to the CTE equipment, enables data to be shifted in the main bit register, again loads a parallel count of 6 into the programmable counter, and as the counter again counts to 6, the second 6 information bits are shifted into DR19 through DR24. As the count of 6, these information bits will be dumped into the programmable counter and \overline{CR} will make a negative transition which causes RA FF to be set.

As the RA FF is set, the second group of 6 information bits are parallel dumped into the programmable counter, the shift pulses are inhibited in the main bit register, and the "minutes" line to the CTE is enabled. As the counter counts, the 10 KC PG pulses are output on the "minutes" line to the CTE equipment. When the programmable counter reaches it's programmed count, \overline{CR} makes a negative transition which clears the RA FF.

Clearing the RA FF causes the output to be inhibited to the CTE equipment and, the main bit register shift pulse gates are enabled. The programmable counter is once again loaded with a count of 6 and the second count is given to TD1 and TD2 FF register.

As the programmable counter again counts to 6, the third group of 6 information bits are shifted into DR19 through DR24. At count six of the programmable counter, CR makes a negative transition which sets RA FF.

Again, as the RA FF is set, it causes the third 6 information bits to be parallel loaded into the programmable counter, the shift pulses are inhibited in the main bit register and the "hour" line to the CTE is enabled. As the counter counts the 10 kc PG pulses, they are output on the "hours" line to the CTE equipment. When the programmable counter reaches its programmed count, CR makes a negative transition which again clears the RA FF.

Clearing the RA FF causes the output to the CTE equipment to be inhibited, the main bit register shift pulse gates are enabled, the programmable counter is loaded with a count of 6, and the third count is given to TD1, TD2 FF register.

The fourth negative transition to TD1 and TD2 to both be +6 V which qualifies A12 pin 10 to reset the system.

16.5.4 Test Message (TM) Operation

The TM word is similar for the vehicle and system address to that discussed for the RTC word with the exception of the system selected is the TM system. When the TM system is selected, it loads the programmable counter with a count of 24. This clocks in the 24 information bits of the TM word into the main bit register. At the count of 24, the last data bit has been placed in the register and CR from the programmable counter makes it's second negative transition. Also, the generator of PG pulses are changed from BSN (200 cps) to the

1 kc dependency, and the content of the first six information bits are parallel dumped into the programmable counter. As the counter counts the programmed number of pulses, the remaining 18 bits are shifted into DR24. As this count is reached, the bit which is in DR24 will be output to the TLM system and an end of message reset is generated. The TLM output reflects the content of DR24 in either the set of clear status by generating a unique eight bit parallel code. This system permits the observation of any bit in the register and indicates the proper operation of the sub-bit section, main bit register, and programmable counter, and reset function.

16.5.5 Detailed Description of Functions Common to All Systems

16.5.5.1 Generation of PG Shift Pulses

The sub-bit levels are dumped into the sub-bit register in serial form as a bi-level signal from the sub-bit detector section. Other signals available from the sub-bit detector are 1 kc and 2 kc timing. A derivative of this timing which is also available is sub-bit-sync-not (SBSN). This signal makes negative transitions at a 1 kc rate and is phase locked to the data such that the negative transitions occur with the sub-bit data transition.

16.5.5.2 Bit-Sync-Not (BSN) Operation

The divide by five counter is triggered by the negative transitions of the SBSN. The output of this counter is "ANDED" with the 1 kc and 2 kc signals to generate an output which makes a negative transition mid-ban of one sub-bit data bit for each five sub-bits and remains at 0 V for the period of 250 usec then returns to +6 V. This timing signal is termed BSN and is used to generate the main bit timing PG. The main bit timing is PG. The A3 FF divide by two, divides

20 kc down to 10 kc as long as gate A7 pin 1 is enabled with pin 2 and 4 equal to +6 V. When either pin 2 or 4 is 0 V, the counter will lock up such that it is in the clear state. In this condition occurs when it is in the set state, the next negative transition of the 20 kc astable signal will clear it and then lock it up in the clear state. If it is in the clear state already, it will remain there.

16.5.5.3 PG Operation

PG has three modes of operation. The first mode will generate a negative transition signal which is 100 usec wide and returns to 0 V for 1/200 sec and then make another negative transition. For this mode, A7 pin 9 = 0V, A13 pin 9 = 0V, and A13 pin 8 inhibited = 0V. The negative transition of BSN causes the EPG FF to be set enabling A7 pin 1. PG will be clear from previous lock up; the first negative transition of the 20 kc sets PG. The second negative transition of 20 kc clears PG making Q go from +6V to 0V; this is a negative transition which resets FF EPG causing Pin Q to be 0V which inhibits A7 causing TS1 and TS2 of PG FF to be +6V, therefore, A13 pin 9 will remain 0V and PG will continue with negative transition of BSN.

The second mode of operation has a $\overline{\text{PG}}$ signal generating a negative transition signal which is 100 usec wide and returns to 0V for 1 ms and then makes another negative transition. For this mode of operation, A13 pin 8 has 1 kc signal, A13 pin 9 is +6V, and RC is 0V. The PG and EPG FF are both clear and BSN will have no effect since TS1 and TS2 are both +6V. The 1 kc signal causes EPG pin 3 to make a negative transition setting the EPG FF. This enables A7 pin 2. This applies +6V to TS2 and 0V to TS1 of PG FF. The first negative transition of the astable sets PG FF and

the second negative transition which clears it. EPG FF will remain clear, inhibiting A7 until the next negative transition of the 1 kc timing.

The third mode of operation has a $\overline{\text{PG}}$ signal which is a square wave 10 kc period. For this mode of operation, EPG FF has RC +6, TS1 +6V S = 0. This causes EPG FF to be disqualified for setting by BSN and also disqualifies EPG for resetting by negative transition at Pin R. Since EPG cannot be reset, it will remain in the set state and Q will be +6V. This leaves A7 enabled and PG FF will continue counting the 20 kc astable. This causes PG to have a 1/10 kc period.

16.5.5.4 Operation of Sub-Bit Shift Register and Decoding:

Sub-bits enter the bit detector/sub-bit synchronizer as two complementary d-c levels from the output FF in the sub-bit detector. A FF in the register is designed to contain a logic one if Q = +6V and a logic zero if Q = 0V.

The sub-bits are shifted into the register with negative transitions of SBSN. This is a +6V level which makes a negative transition just before the end of each data sub-bit time, remains at 0V for 250 usec and then returns to +6V until the end of the next data sub-bit time.

The five sub-bits are translated into a logic 0 bit or a logic one bit by Gates A4 and A14 respectively, before the vehicle address is decoded, and by A5 and A13 after the vehicle address is decoded. All inputs to these gates must be +6V for their output to be 0V. The outputs of A4 and A5 are in parallel, therefore, if either A4 or A5 have all inputs +6V, the common output line will be 0V. The common line between the output of A4 and A5 will be

0 V whenever a logic "one" is decoded.

The divide by 5 counter which controls the sub-bit sampling is composed by SBC0, SBC1, SBC2, and A19. The counter functions as a shift register with one unique section. That is, the two level inputs to the first FF SBO. These levels, after the first negative transition of SBSN, will both be +6V. SBO will not change states on the second negative transition because both level inputs are +6V. Figure #8 indicates the states of this counter. The BSN signal is created by "ANDING" \bar{Q} of SBC2 and \bar{Q} of SBC0 with the 1 kc and 2 kc clock output of the sub-bit detector. When all of these inputs are +6V, A26 pin 9 (BSN) will be 0V.

16.5.5.5 Errors which may occur in Sub-Bit Decoding:

Two types of errors occur in the sub-bit decoder sampling unit. They are both detected by the composite NAND gate A17. This gate indicates an error by its output going to 0V. This occurs when either inputs 2, 4, 6, or 5, 7, 9 are +6V. If both sets of inputs have one logic zero in each set, the output will remain +6V, indicating no error. One form of error occurs when a bit is decoded and a sampling pulse is not present. This type of error is termed EQT error wrong time and is detected by A17 when inputs 2, 4, 6 are +6V. Pin 6 will be +6V for all counts of the divide by 5 counter except sub-bit count 5 when it is 0V. Pin 2 will be +6V only when a bit is decoded. Therefore, if a bit decodes when there is no inhibit on pin 6, the output of FF A17 will be 0V indicating an error which resets the counter and the system. The second form of error occurs when the divide by 5 counter generates a sample pulse and a bit has not been decoded. This occurs when the inputs 5, 7, 9 to A17 are all +6V. During the period while no bit is detected, inputs 7 and 9 are +6V. Pin 5 will be 0V except

during the sample time when it goes to +6V. During the sample time, if no bit is detected, 7, 9 will be +6V and pin 5 will go to +6V causing the output of A17 to be 0V which indicates an error that resets the counter and system. This type of error is known as EBNC (error bit not correct).

An inhibit signal is provided by the divide by two counter at the second negative transition of CR. This inhibit signal disables the sub-bit error detection system after the information portion of the RTC or data word is shifted into the main bit register until the system is reset. The second negative transition of CR causes A29 pin 8 to be +6V. This disables the error detection circuits of the sub-bit detector A17 until reset time by making A17 pin 4, 7 equal to 0V.

16.5.5.6 Vehicle Address Decoding

The detected logic bits are shifted into the decoder register and at that time, A1 pin 3 makes a negative transition initiated by PG. This gate will be inhibited whenever A29 pin 7 and 10 are both +6V.

The first three detected bit levels represent the vehicle address. These levels are shifted into the main bit register with transitions of PG. The vehicle address is continuously decoded as the three bits are shifted into the register. There are eight "NAND" gates which decode all eight possible states of these three bits. These outputs are A0 through A7. Before the vehicle is launched, it is necessary to hard wire a connection from the output of one of the gates which represents that unique vehicle address to A24 pin 5. As the third bit is shifted into the register, one of the eight gates output level goes to 0V and stays at 0V until the fourth bit is shifted into the register. If the wire

was placed between the gate whose output goes to OV, it will place the OV on A24 pin 5. When A24 pin T makes a negative transition, the vehicle address FF is set. This FF will remain set until system reset occurs. The vehicle address FF serves three functions. Before the vehicle address FF is set, the sub-bit decoding is done by A4 and A14 because VA is +6V and VA is OV inhibiting A5 and A13. After the vehicle address is decoded, VA is OV inhibiting A4 and A14, and VA is +6V enabling A5 and A13. This causes the decoding to be done by A5 and A13. The vehicle address FF, after it is set, "enables" the shift gate for the programmable counter A25 pin 5 with VA being +6V. It also inhibits A34 pin 2.

Gate A34 pin 2 has been repeatedly setting DR23, DR24 which is loading a count three code into the programmable counter, however, the counter has been inhibited from shifting until the VA FF is set. The last count of three code which was loaded into the bit register will be dumped into the programmable counter. When enabled by VA, a count of three additional transitions of PG will then load the system address (three bits) into the register.

16.5.5.7 Divide by Two Counter Operation:

Before the system address is decoded, the divide by two counter is in the reset state. CR makes its first negative transition and the divide by 2 counter counts one, loading the system selected into the S register.

16.5.5.8 Decoding Sequence for System Selection:

The system is decoded by the same eight "NAND" gates which decoded the vehicle address. These eight gates remain at +6V until one of them decodes the particular system address. This gate outputs OV which is a d-c steering level to one of the eight storage FF.

The remaining S FF will have both levels (TS1 and TS2) equal to +6V. When the divide by two counter counts 1, it generates a negative transition trigger at pin T of all the storage FF in the register. All the FF which have both inputs +6V will not be affected. The FF which has OV applied to TS1 and +6V to TS2 will be set. This causes its output pin Q to be +6V. The other FF in the S register will remain clear.

16.5.5.9 Programmable Counter Operation

The sequence of loading the programmable counter in the main bit register has been operating continuously from reset time until the vehicle address FF has been set. Before the vehicle address is decoded, VA is +6V, therefore, each time PG is +6V, IO is OV. These negative transitions of IO set DR23, DR24 in the main bit register.

The programmable counter remains inactive except for parallel loading since the shift pulses are inhibited by VA being OV until the vehicle address is decoded. The reset state of the programmable counter causes pin 2 of A8 to be OV which causes CR to be +6V. Each time IO is OV, CR is +6V.

The loading of count 3 into the programmable counter is achieved when the vehicle address is decoded. This sets DR24, DR23 which is parallel loaded into the counter, however, as it is transferred it causes PC0 and PC1 to clear and PC2, PC3, PC4 and PC5 to set. This loading is accomplished by CR making a negative transition. The programmable counter has been inhibited prior to the vehicle address decoding, however, it will now begin to receive shift pulses since VA is decoded as +6V. On count three of the programmable counter, CR makes a negative transition which causes the divide by two counter to count one. This causes A24 pin 3 to make a negative transition which loads the S

register. This negative transition will last for 50 usec which causes CR to be +6V. CR goes to 0V which is a negative transition. This reloads the programmable counter to a reset state for a count determined by the state of DR19 through DR24.

16.5.6 Description of Functions Unique to Each System:

16.5.6.1 RTC Word Sequence:

The first negative transition of $\overline{\text{CR}}$ causes the divide by 2 counter to count 1 and load the RTC system into the S register. This causes S7 to be set and pin Q is +6V. This causes the programmable counter to be parallel loaded with the count of 6 which shifts the serial information into the main bit register, DR1 through DR6.

It should be noted that $\overline{\text{CR}}$ count 1 occurred at the time the system address was decoded and that CR count 2 will not occur until the end of 6 more bit times. The 6 additional shift pulses will load the register with the information portion of the RTC word. It can be seen from the preceding chart that A29 pin 1 is 0V from reset time until CR makes it's second negative transition. This inhibits the RTC relay matrix until the second negative transition of CR and will only occur if the RTC system has been selected.

At this time, $\overline{\text{CR}}$ of the programmable counter makes it's second negative transition which causes the divide by 2 counter to count 2. From Figure C-71, it can be seen at count 2, A29 pin 7 changes to +6V and A29 pin 10 has been +6V since the RTC selection at count 1. This causes A29 pin 9 to be 0V until system reset, inhibiting any further PG shift pulses from the main bit register.

The RTC relay selection is achieved by applying ground to one side of the relay coil, by causing a transistor switch to saturate, and +28V is applied to a 100 ohm resistor to the other side causing a transistor emitter follower to saturate. The relays are bi-polar latching type, with one coil for setting and another for resetting.

The real-time command is shifted into the main bit register with the most significant bit entering first. This causes the bits to be arranged with the most significant bit in DR6 and the least significant in DR1. Figure 13A, B, C, D indicates this relationship of the six bits shifted into the register with respect to the octal code which they represent.

After the six bits of the RTC command have been shifted into the register, the output of A29 pin 1 goes to +6V, enabling the emitter follower set, reset, drivers, and selecting the proper relay.

After the 6 information bits have been shifted into the register, CR makes it second negative transition and resets the programmable counter for a count of 32 by resetting DR19 through DR24. This clears the programmable counter loading a count of 32. The system is reset by a negative transition of A26 pin 10. For this condition, A26 pin 1, 4, and 6 will be +6V. At the third negative transition of $\overline{\text{CR}}$, the divide by 2 counter counts three and PRS1 and PRS2 will both be +6V, therefore, when CR returns to 0V, the system is reset.

The TLM output functions to supply data concerning the digital section to the TLM transmitter. It uses an 8 line output code which is up-dated by each EOMR (end of message reset) signal. As the

system is resetting, the EOMR makes a negative transition and if TSl of A15 is OV, it will be set or if TSl of A19 is OV, it will be set. EOMR also triggers a 55 ms one shot which will reset the FF's after 55 ms. This leaves the code on the output lines for 55 ms. If the RTC command was set, S3 will be OV and since SO is OV, then TSl of A15 will be OV and TSl of A19 will be OV. This will cause both A15, and A19 to be set by EOMR. The output will be:

Bit No:	1	2	3	4	5	6	7	8
Status:	0	+6	0	+6	+6	0	+6	+6

It will remain for 55 ms after the system is reset. It will then be reset to:

Bit No:	1	2	3	4	5	6	7	8
	+6	0	+6	0	0	+6	0	0

16.5.6.2 Computer Word Sequence:

The computer word sequence is identical to the RTC word for the sub-bit decoding, vehicle address, and system selection. The only difference is that the system selected is the G/N system instead of the RTC system.

The first negative transition of \overline{CR} causes the divide by 2 counter to count one and load the G/N system into the S register. This causes the programmable counter to be parallel loaded with the count of 16 which shifts the work in serial form through the main bit register through DRL3. At this time, CR of the programmable counter makes it's second negative transition which causes the divide by 2 counter to count 2. This causes A29 pin 8 to

be +6V.

This disables the error detection circuits of the sub-bit detector A17 until reset time by making A17 pin 7, 4 equal to OV. Since the RTC system has not been selected, A29 pin 9 will remain at +6V which permits PG pulses to continue shifting data into the main bit register through A1 pin 9.

At the time the G/N system is selected, the following conditions exist: S7 remains +6V, S4 remains OV, SO remains at OV, and since S3 was selected it goes from OV to +6V until reset time. Before the second negative transition of \overline{CR} , or count 2 of the divide by 2 counter, EPG pin TSl was OV which qualified BSN to set EPG with its negative transition. After count 2, PRS2 is +6V which causes EPG pin TSl to be +6V which inhibits any further transitions of BSN from setting EPG. EPG will be set after count 2, by the negative transition of 1 kc signal, through A13 pin 8. Each time EPG is set, A7 pin 2 goes to +6V qualifying the 20 kc astable to set PG, the second negative transition of the 20 kc astable clears PG, causing pin Q to make a negative transition, resetting EPG. This causes A7 pin 2 to inhibit PG until EPG is set again. The result of this action is that the computer word is clocked into the bit register at negative transitions of BSN (200 cps rate) and is clocked out of the bit register at negative transitions of 1 kc (1 kc rate).

When the programmable counter reaches a count of 16, \overline{CR} makes its second negative transition. This causes the programmable counter to be parallel loaded to a reset state.

This will require PG to make 32 negative transitions for CR to make a third negative transition and reset the system. After the 16 bits are shifted into the register, PG will run at a 1 kc rate.

The system will be reset after 32 additional counts of PG at a 1 kc rate. The resetting of the system is accomplished by A21 pin 9 going to +6V.

If an G/N word was transmitted, S3 will be +6V and the output of A10 pin 8 is OV. This causes A10 pin 9 and pin 1 to apply +6V to TS1 of A15 and TS1 of A19. After the computer word is accepted, A10 pin 5 goes to OV. At the end of message time, EOMR makes a negative transition which sets A15, A19. This outputs the following code:

Bit No:	1	2	3	4	5	6	7	8
Status:	0	+6	0	+6	+6	0	+6	+6

After 55 ms it will be reset, outputting:

Bit No:	1	2	3	4	5	6	7	8
Status:	+6	0	+6	0	0	+6	0	0

If the G/N data accept signal is not actuated, TS1 of A15, A19 will be +6V and the FF will remain reset at EOMR time, with the code being as follows:

Bit No:	1	2	3	4	5	6	7	8
Status:	+6	0	+6	0	0	+6	0	0

16.5.6.3 CTE Word Sequence

The CTE word sequence is identical to the RTC word sequence for the sub-bit decoding, vehicle address, and system selection. The only difference in the system selected is the CTE system instead of the RTC system.

The first negative transition of \overline{CR} causes the divide by 2 counter to count 1 and loads the

decoded CTE system address into the S register. This action causes PRS 1 to be +6V and also S4 to be +6V. This enables A 11 pin 6 so that as PG returns to +6V, the CTE system is reset. The CTE system will continue being reset with PG, making positive transitions, until CR makes a third negative transition causing PRS 1 to be OV, inhibiting this resetting function of A21 pin 9. Then the system will not be reset at the third negative transition of CR. The loading of the CTE system also causes the programmable counter to be parallel loaded with the count of 24 which shifts the information portion of the word into the main bit register. This is accomplished by setting DR20, DR21 which will be transferred in parallel to the programmable counter. This clears PC3, PC4 and sets PC0, PC1, PC2, PC5 which loads the count of 24. After 24 additional pulses of PG have been counted by the programmable counter, CR makes its second negative transition. This causes the divide by 2 counter to count 2.

The generation of PG pulses are controlled by S4 and PRS2. Before CR makes a second negative transition, PRS2 is OV which places OV on A8 RC. This qualifies EPG FF to be reset by Q of the PG FF making a negative transition. Before CR counts 2, the following voltages exist: S4 = +6V, S7 = +6V, PRS2 = OV, S3 = OV, S0 = OV. This applies to the following levels of EPG: TS1 = OV; S = OV, RC = OV.

Each negative transition of BSN sets EPG which enables A7 pin 2. The first negative transition of the 20 kc astable sets PG. The second transition of the 20 kc astable clears PG which causes a negative transition at pin R of EPG thereby clearing EPG. This inhibits A7 and no further 20 kc pulses will activate the PG FF until the next negative transition of BSN which sets EPG and repeats this sequence. After count 2 of CR, PRS2 is +6V which will apply the following levels to FF EPG:

RC = +6V, TS1 = +6V, S = OV. This causes EPG FF to be disqualified for setting by BSN and also disqualifies EPG for resetting by negative transitions at pin R. Since EPG cannot be reset, it will remain in the set state and Q will be +6V. This leaves A7 enabled and PG FF will continue counting the 20 kc astable. This causes PG to have a 1/10 kc period rather than a 1/200 cps period.

At count 2 of the divide by two counter, PRS2 goes to +6V. This causes the output of A7 pin 9 to be +6V. This enables A7 pin 5, therefore, when CR goes to OV, A7 pin 8 will make a negative transition setting the RA FF and loading the contents of the main bit register, DR19 through DR24, into the programmable counter. As the programmable counter is parallel loaded with these first 6 information bits, the main bit register is loaded with the count of 6 by setting DR22, DR23, and clearing DR19, DR20, DR21, and DR24. When the RA FF is set, RA goes to OV, this inhibits PG pulses from shifting data into the main bit register. Also, the RA FF enables the seconds line to the CTE equipment so that as PG pulses are counted by the programmable counter, they will be output on the seconds line to the CTE. This is accomplished by TD1, TD2 FF being in the reset state and FF RA pin Q = OV. When the programmable counter reaches its programmed count, CR makes its third negative transition. This clears the RA FF which loads the count of 6 into the programmable counter. RA goes to OV which enables the PG shift pulses to shift data in the main bit register. Also as RA FF is cleared, pin Q makes a negative transition giving count 1 to the TD1, TD2 shift register. Then Q of the RA FF goes to +6V which inhibits any pulses to the CTE Equipment.

As the programmable counter counts to 6, the second group of 6 information bits are shifted into the main bit register, DR19 through DR24. At the count of 6, CR makes its fourth negative transition which sets the RA FF. Then RA FF is set and RA goes to OV which inhibits shifting data in the main bit register. The Q goes to OV which enables the minutes output line to the CTE equipment. It also parallel loads the second 6 information bits into the programmable counter.

As the programmable counter counts the PG pulses they are output to the CTE on the minutes line. When the programmable counter reaches its programmed count, CR makes its fifth negative transition which clears the RA FF. As RA FF is cleared, the output to the CTE is inhibited and the shift pulses to the main bit register are enabled. Then the count of 6 is loaded into the programmable counter and TD1, TD2 receives the second count. The counter counts PG pulses until count 6 when CR makes its sixth negative transition which sets the RA FF. The RA FF is set and RA goes to OV which inhibits shifting data in the main bit register. The Q of the RA FF goes to OV and enables the hours output line to the CTE equipment. It also parallel loads the third 6 bit information bits into the programmable counter.

As the programmable counter counts the PG pulses, they are output to the CTE on the hours line. When the programmable counter reaches its programmed count, CR makes its seventh negative transition which clears the RA FF. As the RA FF clears, the output to the CTE is inhibited, the shift pulses to the main bit register are enabled. The count of 6 is loaded into the programmable counter and TD1, TD2 receive the third negative transition count. The counter counts PG pulses until count 6, when CR makes its eighth negative transition which sets the RA FF. The RA FF is set and

RA goes to OV which inhibits shifting data into the main bit register and Q goes to OV which enables the days output line to the CTE. It also parallel loads the fourth group of 6 information bits into the programmable counter. As the programmable counter counts the PG pulses, they are output on the CTE on the days line. When the programmable counter reaches its programmed count, CR makes its seventh negative transition which clears the RA FF. As the RA FF clears the output to the CTE is inhibited, the shift pulses to the main bit register are enabled. The count of 6 is loaded into the programmable counter and TD1, TD2 receive the fourth negative transition count. As TD1, TD2 receive the fourth negative transition count, TD1 and TD2 both become +6V. This qualifies A21 pin 9 to reset the system when R3 makes a negative transition.

When CR returns to OV, A24 pin 3 goes to +6V and A29 pin 8 goes to OV which is R3. This resets the system.

16.5.6.4 TM Word Sequence:

The TM word sequence is identical to the RTC word sequence for the sub-bit decoding, vehicle address, and system selection. The only difference in the system selected is the TM system instead of the RTC system.

The first negative transition of CR causes the divide by two counter to count 1 and load the S register by setting SO. This causes SO to be OV which sets DR20, DR21, loading the count of 24 into the programmable counter. As CR makes a negative transition, this count is parallel loaded into the programmable counter. As the counter counts to 24, the PG pulses are shifting the 24 information bits into the main register.

Before the 24th pulse is counted, the PG pulses are generated as follows: SO = OV, PRS2 = OV, S7 = +6V, S4 = OV. This places the following levels on EPG FF: RC = OV, TS1 = OV, S = OV. Assume PG and EPG FF are clear; BSN makes a negative transition which sets EPG FF making pin Q +6V. This enables A7 "NAND" gate which places OV on TS1 of PG. This qualifies PG FF to be set by the next negative transition of the 20 kc astable. The PG FF is set which causes Q to be +6V and Q to be OV. This applies OV to TS1 and +6V to TS2. The second negative transition of the 20 kc astable FF clears the PG FF which causes pin Q to make a negative transition which resets the EPG FF by pin R making a negative transition. Then EPG will remain reset until the next negative transition of BSN.

After the 24 information bits are shifted into the main bit register, and at the count of 24, CR makes its second negative transition which causes the divide by two counter to count 2. This causes PRS2 to become +6V and since the TM system was selected, SO will be +6V. This causes the PG pulses to be generated by the 1 kc negative transitions. At the second negative transition of CR, the following levels will be established at the EPG FF: TS1 will be +6V, RC = OV, S = 1 kc.

Assume both EPG and FF are cleared. The first negative transition of the 1 kc sets EPG FF. This causes pin Q to be +6V which enables A7 "NAND" gate. The first negative transition of the 20 kc astable will set PG FF. This applies OV to TS1 and +6V to TS2. This second negative transition of the 20 kc astable clears the PG FF causing pin Q of PG to make a negative transition. This will set EPG because RC is OV. Since EPG FF is cleared, A7 will remain disabled until EPG is set by the next negative transition of the 1 kc timing. This causes PG pulses to be dependent upon the negative transition of 1 kc timing after the second negative transition of CR.

The second negative transition of \overline{CR} dumps the first 6 bits of the 24 information bits into the programmable counter; which were shifted into DR19 through DR24. As the programmable counter counts to the programmed count, the remaining 18 information bits are shifted through DR19 to DR24. When the count is reached, CR makes its third negative transition; this causes A21 to produce an EOMR signal which resets the system.

As the system is reset, the contents of DR24 and DR24 are loaded into the TLM output storage FF A and B.

At the EOMR time, if DR24 is set, the TLM output will be:

Bit No:	1	2	3	4	5	6	7	8
Status:	+6	+6	+6	+6	+6	0	0	0

At the EOMR time, if DR24 is clear, the TLM output will be:

Bit No:	1	2	3	4	5	6	7	8
Status:	0	0	0	0	0	+6	0	0

After 55 ms, the one shot will reset the TLM and FF and the output code will be:

Bit No:	1	2	3	4	5	6	7	8
Status:	+6	0	+6	0	0	+6	0	0

These messages will remain at the TML output for 55 ms until A24 pin Q resets A15, A19. This is a verification that the sub-bit register, main bit register, vehicle decoding, and system decoding system are operational.

16.5.7 Summary of Functions Used in Decoder:

From the analysis, the following characteristics of word format can be established.

16.5.7.1 RTC Command:

Vehicle Address			System Address			Information Section					
1	2	3	4	5	6	7	8	9	10	11	12

The vehicle address is shifted with BSN, a 200 cps signal requiring 15 ms. The system address is shifted with BSN and requires 15 ms. The RTC information is shifted with BSN, a 200 cps signal requiring 30 ms. The RTC command actuation signal is present for 32 counts of the PG in the programmable counter which occurs at 200 cps. Time required is 160 ms. At the end of this time, the system is reset.

16.5.7.2 G/N Command:

Vehicle Address			System Address			Information Section					
1	2	3	4	5	6	7	8	9	10	11	12
						13	14	15	16	17	18
						19	20	21	22		

The vehicle address is shifted at negative transitions of BSN, a 200 cps signal, time required is 15 ms. The system address is shifted at negative transitions of BSN, a 200 cps signal, time required is 15 ms. The information section (16 bits) are shifted into the main bit register at negative transitions of BSN, a 200 cps signal, time required is 80 ms. The information section (16 bits) are shifted into the computer with 32 PG pulses at negative transitions of the 1 kc timing requiring 32 ms.

16.5.7.3 CTE Command:

Vehicle Address			System Address			Seconds Information							Minutes Information					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Hours Information						Days Information												
20	21	22	23	24	25	26	27	28	29	30								

The vehicle address is shifted at negative transisions of BSN, a 200 cps signal requiring 15 ms. The system address is shifted at negative transitions of BSN, a 200 cps signal requiring 15 ms. The 24 data bits are shifted at negative transisions of BSN, a 200 cps signal requiring 120 ms.

The first six information bits "seconds" are parallel loaded into the programmable counter. The counter runs with negative transition of PG whihc are occurring at a 10 kc rate. The length of time required will be (number programmed) 10^{-1} ms. A count of six will be programmed into the counter and loaded by the 10 kc PG pulses. This will require .6 ms.

The second six information bits "minutes" are parallel loaded into the programmable counter. These PG pulses also occur at a 10 kc rate. The length of time required will be (number programmed) 10^{-1} ms. A count of six will be programmed into the counter and the 10 kc PG pulses will be loaded. This requires .6 ms.

The third six information bits "hours" are parallel loaded into the programmable counter. These PG pulses occur at a 10 kc rate. The length of time

required will be (number programmed) 10^{-1} ms. A count of six will be programmed into the counter and the 10 kc PG pulses will be counted. This requires .6 ms.

The fourth set of six information bits "days" are parallel loaded into the programmable counter. These PG pulses occur at a 10 kc rate. The length of time required will be (number programmed) 10^{-1} ms. At the end of this time, the system will be reset. As each set of PG pulses were counted, the second, minute, hours, and days PG pulses were output on the appropriate lines to the CTE.

Significance of bits 7, 8, 9, 10, 11, and 12. These bits determine the number of pulses output on the seconds line. They will be parallel word loaded into the programmable counter.

Bit No:	7	8	9	10	11	12
Count No:	1	2	4	8	16	32

The same sequence applies to minutes, hours, and days outputs. A maximum count of 63 pulses is available if all FF are set.

16.5.7.4 TM Command:

Vehicle Address			System Address						Scan Information					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Information to be Scanned														
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

The vehicle address is shifted at negative transitions of BSN, a 200 cps signal requiring 15 ms. The system address is shifted at negative transitions of BSN, a 200 cps signal requiring 15 ms. The system address is shifted at negative transitions of BSN, a 200 cps signal requiring 15 ms. The 24 data bits are shifted at negative transitions of BSN, a 200 cps signal requiring 120 ms.

The first 6 information bits are loaded into the programmable counter. The CO counter counts PG pulses occurring at a 1 kc rate. The time required is the programmed count ms. At the end of the count, the system is reset and the contents of one of the remaining 18 information bits will be dumped from DR24 and DR24 FF. The bit selected depends on the number of shifted pulses programmed in the first 6 information bits. The TLM will output a unique load for a set or reset condition of DR24.

Significance of Bits 7, 8, 9, 10, 11 & 12:

These bits determine a parallel code which is loaded into the programmable counter and determine which of the following information bits will be shifted into DR24 at reset time.

Bit No: 7 8 9 10 11 12

Count No: 1 2 4 8 16 32

The set condition of +6V at pin Q is a logic one. A possible bound of 64 is available if all FF are set. At the EOMR time, if DR24 is set, TLM output will be:

Bit No: 1 2 3 4 5 6 7 8

Status: +6 +6 +6 +6 +6 0 0 0

If DR24 is clear, TLM output will be:

Bit No: 1 2 3 4 5 6 7 8

Status: 0 0 0 0 0 +6 0 0

SECTION XVII

TELEVISION CAMERA

17.1 INTRODUCTION

The Television Camera will provide real-time video information to the earth-based receiving stations. From the receiving station, the video will be relayed to Houston for processing and release to commercial television networks. The video will be carried by a hardline before launch and transmitted via the Unified S-band Equipment after launch. Launch and earth orbit will be transmitted over the 2-Kmc Omni-antennas.

Before launch, the raw video signal from the camera is routed directly to the ground station via hardline. After launch the television camera video is fed to the Pre-Modulation Processor where it is frequency-multiplexed with the telemetry data. The Pre-Modulation Processor then feeds the video to the S-band transmitter, where video directly frequency-modulates the S-band carrier for transmission to earth over the S-band antennas.

One camera and three semistationary locations are provided in the command module. One camera location is behind the head of the center seat, situated to view crew activities in the center of the crew compartment. The second camera location is at the base of the control panel to provide viewing of the astronauts from the front. The third camera location is by the right foot of the systems engineers cover to provide viewing of the activities in the lower equipment bay at the navigation station. Figure 7-1. The center viewing camera location is provided with a 5-foot cable for portable use throughout the command

module or for viewing out the windows. Because of its pistol grip construction, the camera can be hand-held by the crew for coverage of any accessible target, inside the command module or outside, through the windows.

The camera, supplied by RCA Astro-Electronics Division, weighs 4.5 pounds and has a volume of 85 cubic inches, excluding the two accessory lenses. Figure 17-2. The camera tube is a ruggedized, electrostatic focus, electromagnetic deflection, 1-inch Vidicon with a sensitivity of 0.1 foot-candle. The camera is capable of copying with an incident scene illumination of from 0.1 to 30 foot candles. Differences in illumination are accommodated by the incorporation of an automatic camera gain control, which is adjusted by a feedback loop from the camera processing chain. The camera has the capability of rendering a minimum of five gray scales on the Electronics Industry Association resolution chart with the above specified illumination levels.

17.2 CHARACTERISTICS

17.2.1 Television Camera

Bandwidth	500 kc
Frame rate	10 frames per second
Lines per frame	320 noninterlaced
Output Signal/Noise	43 decibels
Imaging tube	1 inch Vidicon
Sensitivity	0.1 foot-candle highlight illumination minimum

TV CAMERA LOCATIONS

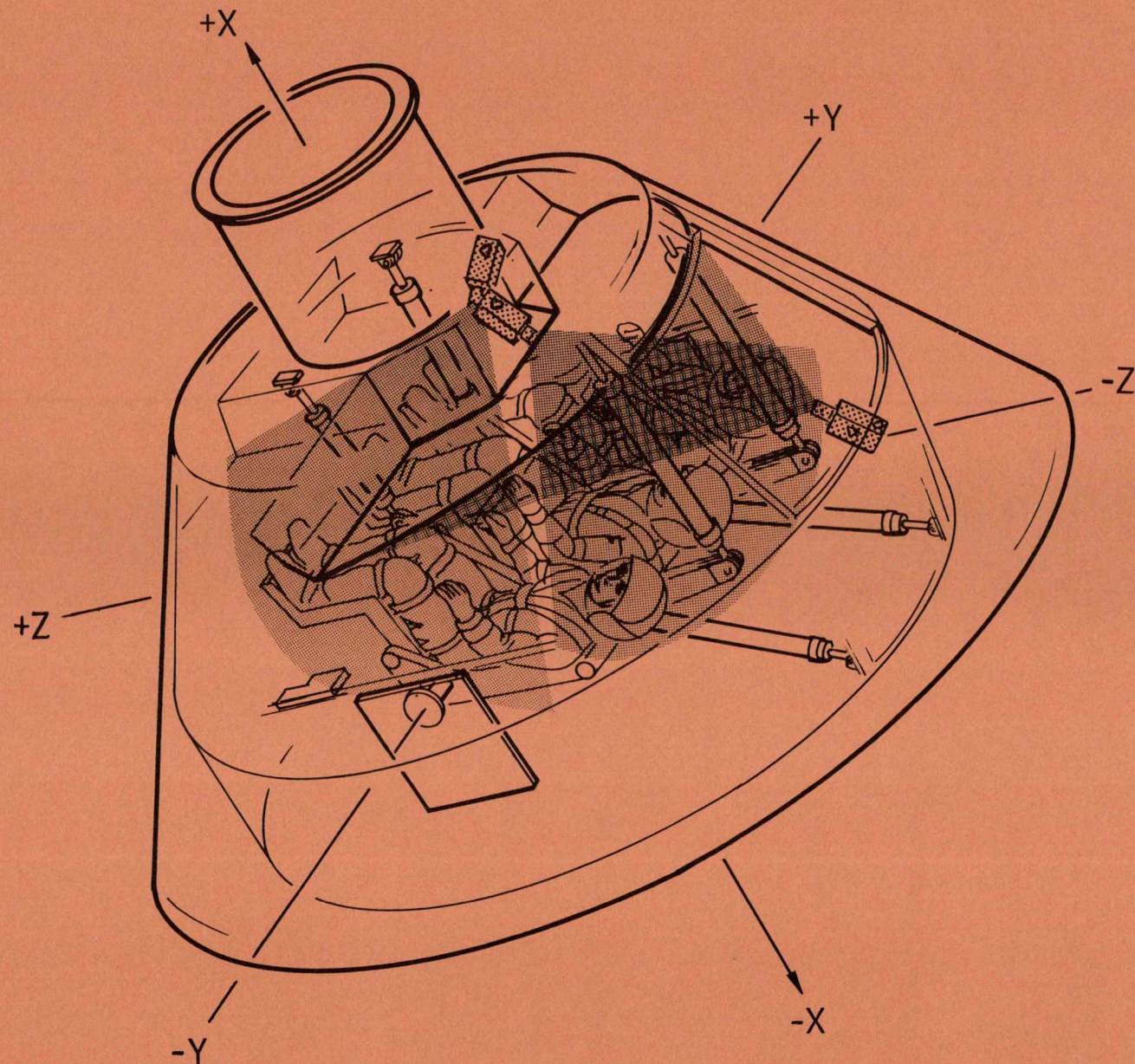


figure 17-1

CD-72



17-2

APOLLO TV CAMERA

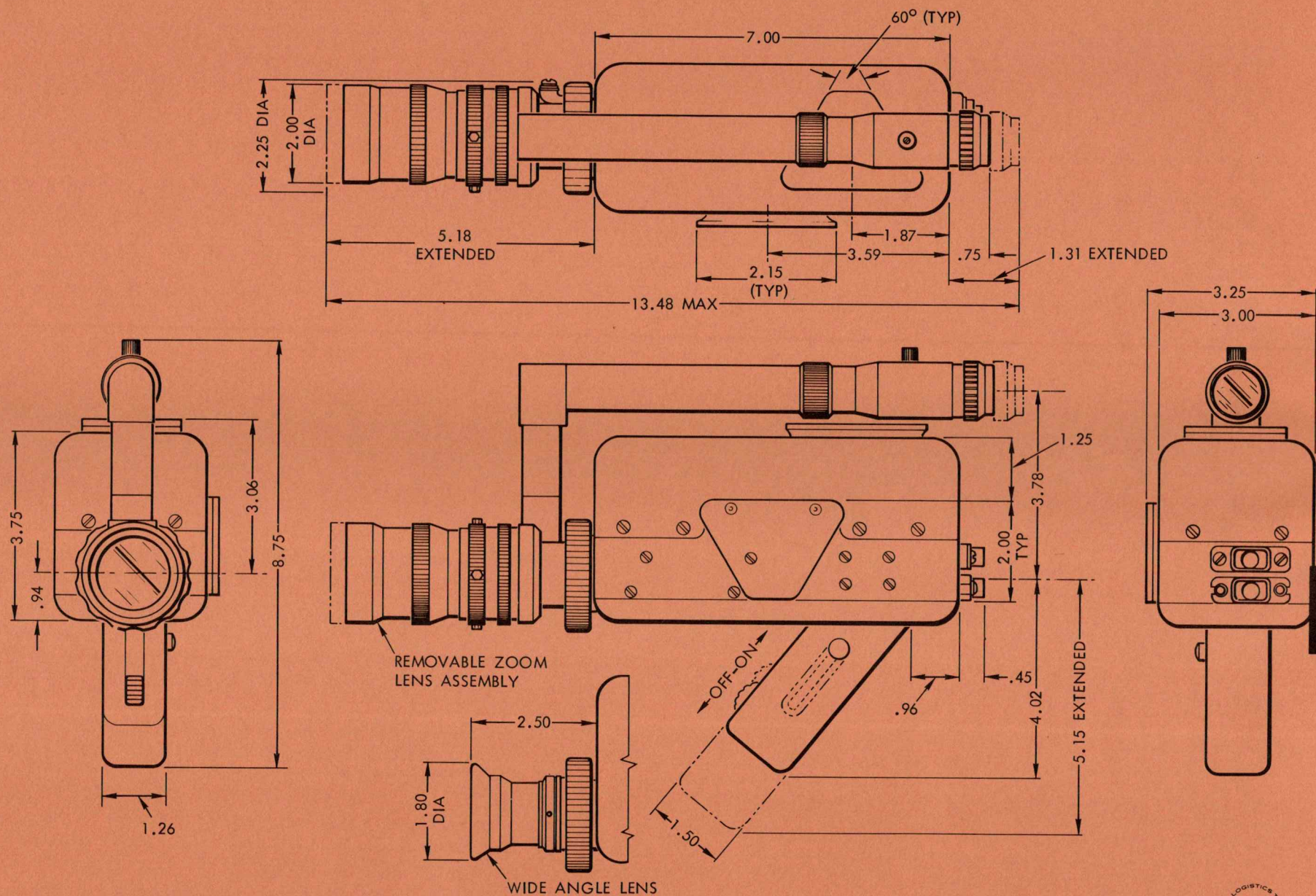


figure 17-2

CD-163A



Lenses	1. 7.5 mm f/1.9 (wide angle angle-78°)
	2. 20 mm to 80 mm f/2.5 (zoom) (9 to 30°)
Resolution	200 mm television lines on a EIA test pattern at .1 foot candle
Output Voltage	2 volts pp to Pre-Modulation Processor
Aspect ratio	4:3 horizontal to vertical
Gray Scale	5 minimum
Blanking Time	
Horizontal	30 microseconds
Vertical	2500 microseconds nominal

The camera requires 28 volts dc at 6.75 watts of power. It provides an analog output signal to the PMP. Two lenses are provided, the wide angle lens. The latter is fitted with a through-the-lens view finder. Both lenses are manually interchangeable.

17.3 DESCRIPTION OF THE APOLLO TV CAMERA

The Apollo TV camera is a self-contained unit which requires only unregulated dc power from the Apollo Command Module for proper operation. The major components comprising the TV camera are shown in the block diagram of Figure 17-3. The system parameters and electrical circuits of the TV camera are discussed in detail in the following paragraphs, as well as a mechanical description of the camera.

17.3.1 Electrical Description

17.3.1.1 Vidicon Picture Tube

The Apollo TV Camera will employ a one-inch, electrostatic-focus, magnetic-deflection

vidicon tube similar to the commercially available RCA vidicon tube, type 8134 manufactured by the RCA Electron Tube Division, Lancaster, Pa. This tube uses a small, low-power deflection yoke, a feature which makes it ideal for fulfilling the requirements of the Apollo mission.

In the operation of the TV camera, a lens is used to image light on the photoconductor surface of the vidicon tube. The image area of interest is described by a circle 0.500 inch in diameter, and concentric with the axis of the tube. The scanned area is a rectangle, the dimensions of its sides being a ratio of 4 to 3, circumscribed by the circle. The geometric relationship of the scanning system and the optical image is shown in Figure 17-4. The video signal is an electrical current which is a function of the variation in image brightness along the scanned lines. An increase in brightness corresponds to an increase in current. This current flow is between the cathode of the tube and the target electrode.

17.3.1.2 Video Amplifier

The video amplifier of the Apollo TV camera is a solid state circuit and comprises a preamplifier, hi-peaker, second gain stage, and clamp circuit. The video signal of the target electrode, which is in the nanoampere range, is ac coupled to a high-impedance circuit and converted to a voltage to provide a signal input to a transistor amplifier. This preamplifier has an amplification of approximately 29db. The capacitance of the input to this stage creates a rolloff of 6db per octave above approximately 80 kc. The hi-peaker stage following the preamplifier circuit compensates for this rolloff. The resultant output of the hi-peaker is flat for all frequencies of interest.

APOLLO TELEVISION CAMERA

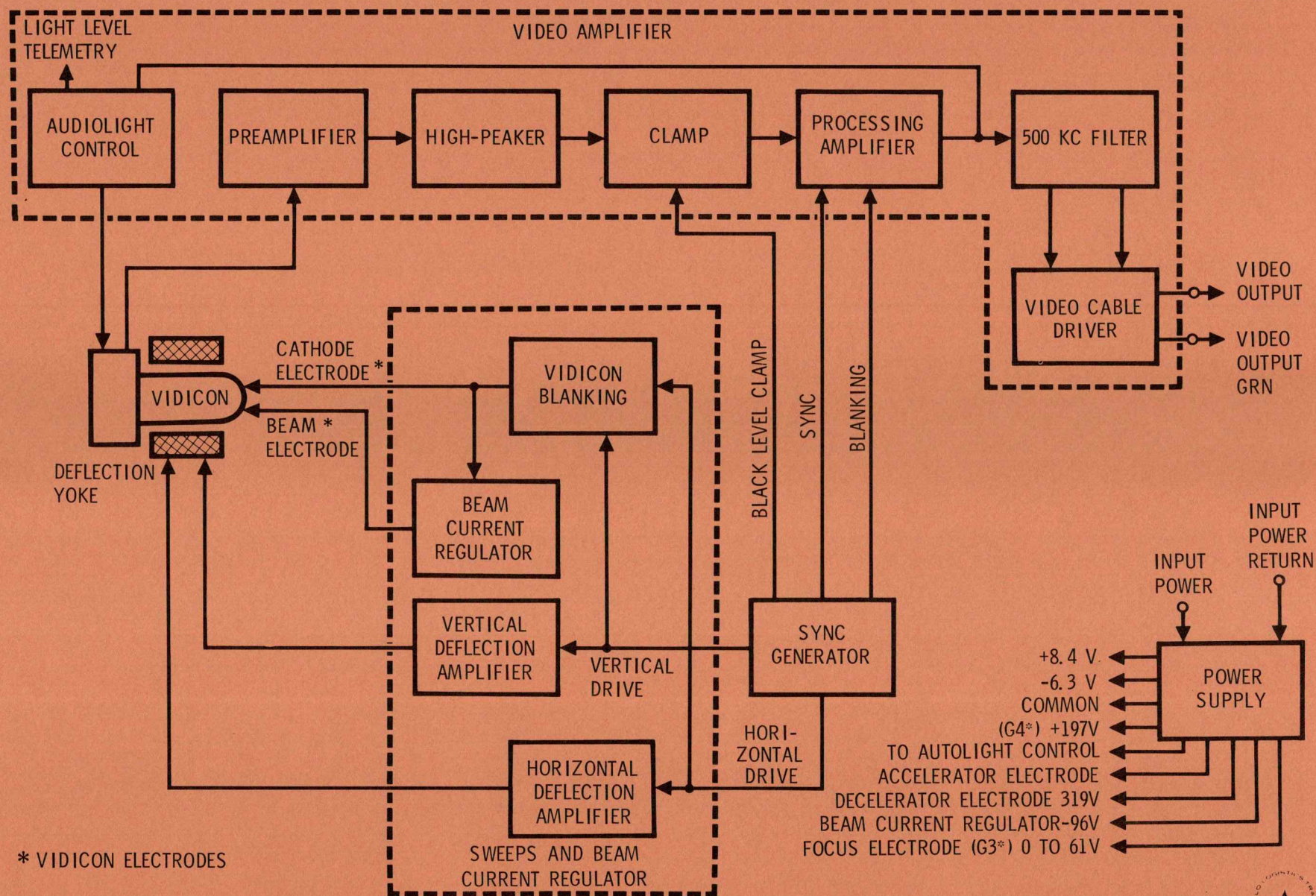


figure 17-3

CD-100B

IMAGE FORMAT FOR VIDICON TUBE

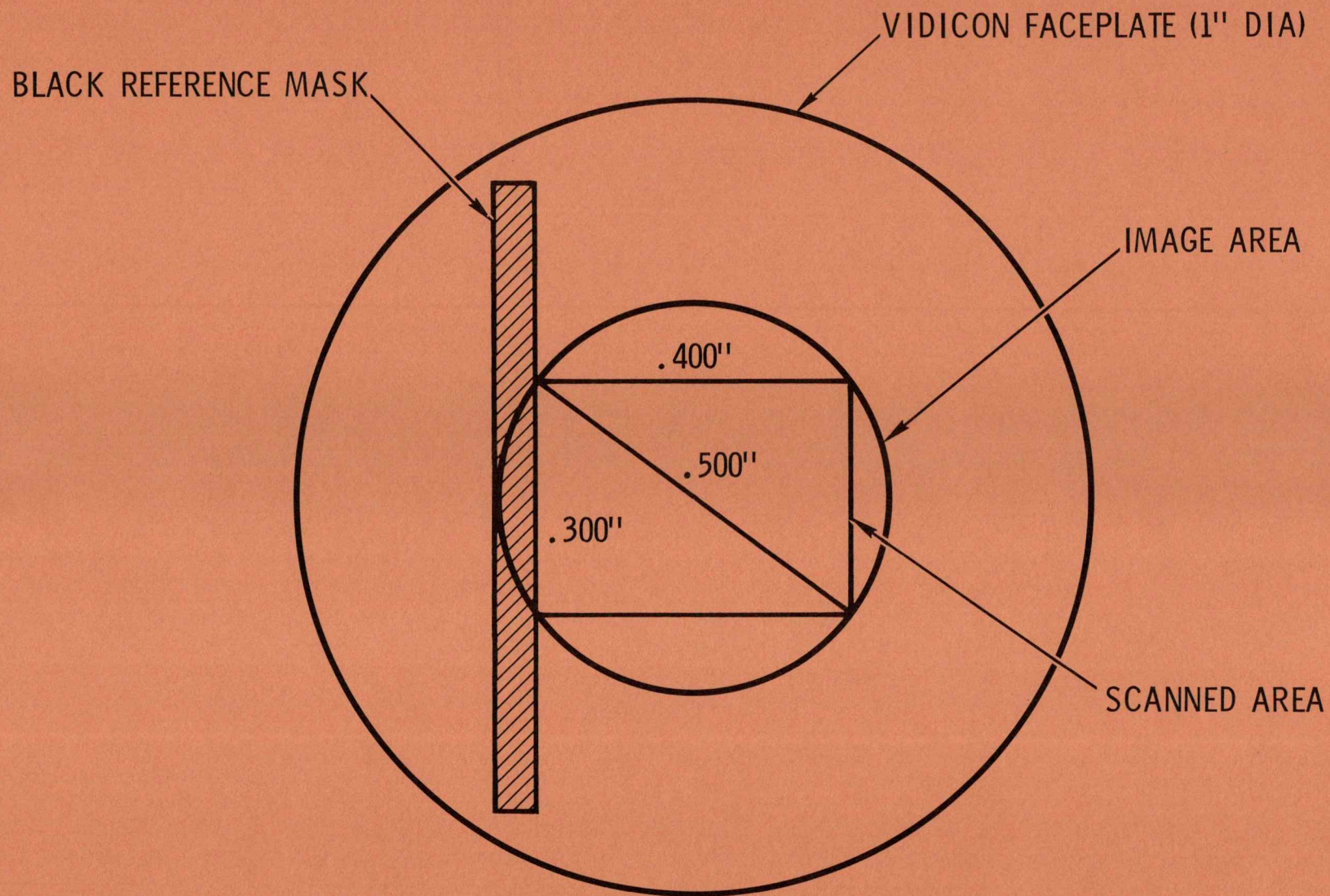


figure 17-4

CD-317A



The hi-peaker is followed by a second gain stage of approximately 17db. Gain adjustment is obtained by varying the voltage at the hi-peaker output using a voltage divider. The ac signal is clamped at the horizontal rate to establish a dc level relative to "scene black". This is accomplished by the voltage across the coupling capacitor in the output of the second gain stage such that the potential of the ac output is ground when the image is black. A black reference is established by making the photoconductor to the left of the edge of the scanned image. During the first part of scanned line, the beam is behind the reference mask. The coupling-capacitor voltage is also adjusted at this time by shorting it to ground through a switching transistor. This differential voltage is maintained with negligible leakage during the horizontal-line period. By clamping the horizontal line, the low-frequency response of the video amplifier will be down less than 3db at 40 cycles, resulting in a picture with no noticeable tilt.

17.3.1.3 Video Processing and Sync Insertion

The video processor circuit of the TV camera consists of a differential amplifier, transistor switching circuits, a filter, and a second gain stage. The output of the clamp circuit is used to drive one side of a differential amplifier having a gain of 10db. The other input to the differential is an adjustable reference to establish the correct output level corresponding to black (4.6 milliampere load current). The output from the differential amplifier is then fed into the sync-insertion circuit.

The composite video waveform is shown graphically in Figure 17-5. The sync pedestal tip corresponds to ground and is inserted by grounding the output of the differential amplifier. The front and back porches are inserted by adding a signal

corresponding to midway between sync tip and peak white (a load current of 10 ma). This is achieved by switching a reference voltage into the output amplifier while the differential amplifier is still grounded.

The output of the sync circuit is fed to a low-pass filter having a rolloff of 20db per octave above 500 kc. The output of this low-pass filter is used to drive the video-output stage. This stage consists of two transistors, and its output is the collector current of the second transistor. This allows the load to be either 50 or 100 ohms with a corresponding composite video voltage of one or two volts, respectively.

17.3.1.4 Sync Generator

The sync generator provides all of the timing functions required by the camera electronics for proper operation. The time base for the sync generator is generated by a 1.024 mc oscillator.

The sync generator is composed of flip-flops, gates, and OR and NOR gates to provide all timing pulses necessary. The generator is completely composed of integrated circuitry.

17.3.1.5 Deflection Circuits

The deflection circuits consist of a sawtooth generator driving a differential amplifier. The output of the differential amplifier drives an emitter follower, which, in turn, drives a complementary push-pull output stage. The yoke current is sampled across a small resistor and fed back to the other side of the differential amplifier. The sawtooth capacitor is discharged by a transistor switch to initiate fly back.

APOLLO TELEVISION CAMERA SYNC FORMAT

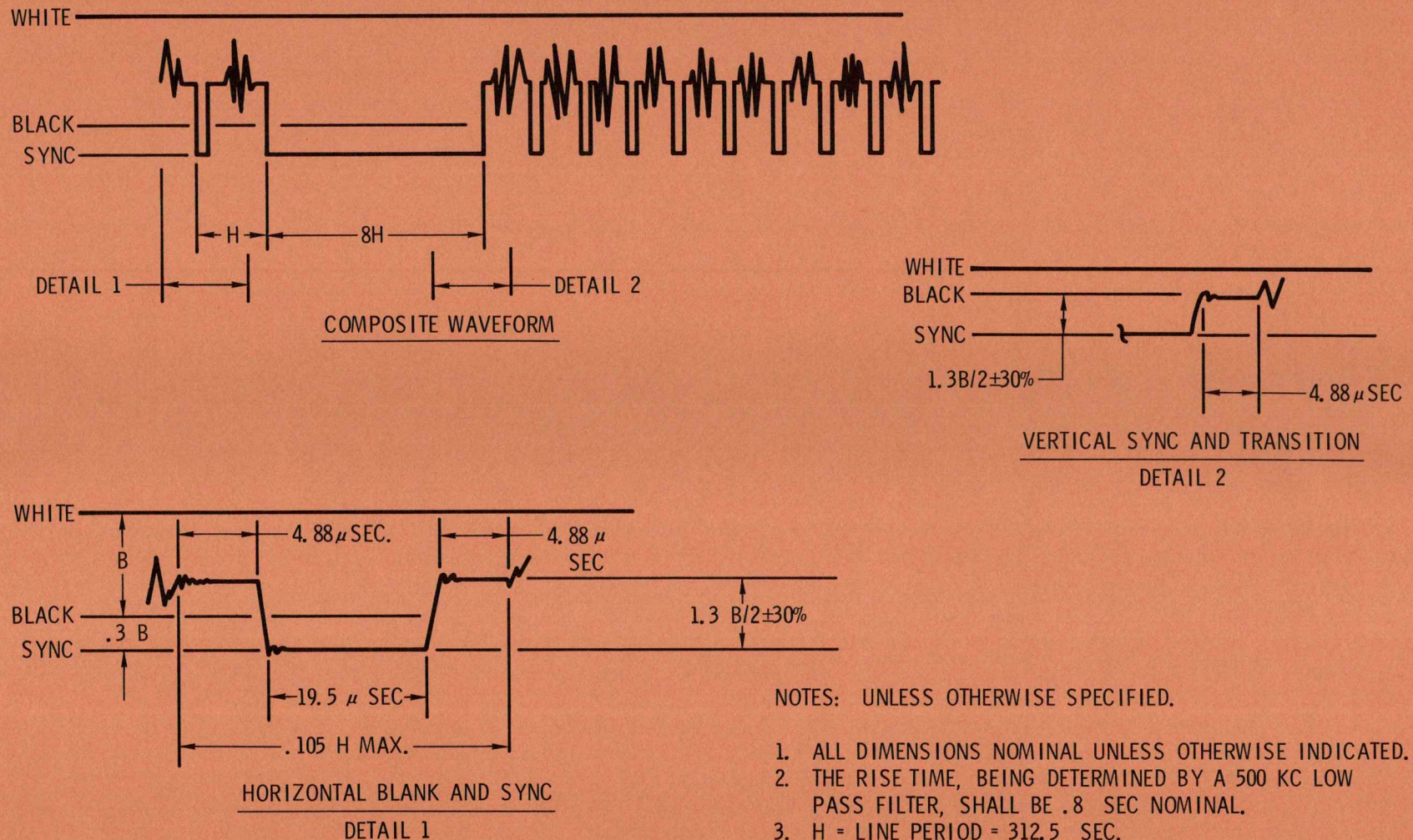


figure 17-5

CD-220A



Since the yoke current must be zero in the center of the sweep and since the sawtooth waveform starts at zero, a centering voltage will be applied to the yoke-current waveform before it is fed to the differential amplifier. The design of both the horizontal and the vertical deflection circuits will be essentially the same.

17.3.1.6 Beam Current Regulator and Blanking Circuit

To meet the long "operating life without adjustment" requirement of Specification MC-901-0090, it is necessary to automatically control the video READ beam current. The cathode current is proportional to the beam current, and is measured as a voltage across the cathode voltage, which in turn charges the beam current.

Blanking is effected by switching the cathode potential with a transistor switch driven from the sync generator.

17.3.1.7 Power Supply

The power supply consists of a voltage regulator supplying approximately 21 volts to a dc to dc converter. This converter transforms the primary power into voltages of +300, -90, +8.4 and -6.3 volts. The low voltages are regulated and used to supply power for all of the camera circuits as well as the vidicon filament. The high voltage supplies power for the vidicon electrodes.

The transformer in the power supply serves to decouple the power ground from the signal ground.

17.3.1.8 Automatic Light-Level Compensation

The scene brightness variation (300 to 1) will require control of the system gain as a function of scene illumination. The gamma of the photoconductor in the vidicon will provide some control, which will be augmented by adjusting the vidicon target voltage as a function of the scene brightness. Preliminary tests indicate that this technique will maintain picture quality with a minimum weight and power penalty, as compared to the penalty incurred with a mechanical iris or filter system.

The target voltage control is a closed-loop control that adjusts the target voltage as a function of the video output.

The target voltage will be telemetered as an indication of the actual scene brightness.

17.4 TV CAMERA OPTICS

The optics for the TV Camera is designed to accomplish four basic functions assigned to the camera for the Apollo mission.

- a. During a four hour period prior to launch, the camera will be mounted in a position from which it can view crew prelaunch activities.
- b. During powered flight, the camera will be mounted in a position from which it can view the crew members.

- c. After achieving earth orbit, a crew member will relocate the camera to a position above the center astronaut couch, from where the camera will view the working area.
- d. During either earth or moon orbit, the camera will be used to take pictures of the earth or moon, respectively.

The four functions impose different conditions of illumination and field of view.

The differences in illumination will be accommodated by incorporating an automatic camera gain control. The effect of this gain control will be essentially the same as that of an automatic iris, but this technique does not involve the inherent mechanical problems associated with an iris.

The camera will also include a pistol-type grip and a sighting device to simplify taking pictures of the earth or moon during hand-held operation.

17.4.1 Work-Area-Picture Taking

The lens used for taking pictures of the work area will be the same as that for taking pictures of the astronauts. Close-ups or zoom effects can be obtained by manually moving the camera closer to the subject. The hyperfocal distance, based upon a 200 TV line resolution, is less than 20 inches if the lens is focused at infinity. This depth of field makes manual adjustment of the focus by the astronaut unnecessary.

17.4.1.1 Lens Selection

Argus Corp. has developed the lenses for Apollo. The following are the parameters set down for the wide angle lens:

Effective Focal Length (EFL): 7.5 mm
f-number: 1.9
Diagonal Coverage: 78°
Weight: 4 oz

17.4.2 Earth and Moon Picture Taking

In order to afford optimal real-time pictorial coverage during the trans lunar, lunar orbit and trans earth phases of the Apollo mission a detachable zoom lens has been provided. This lens, shown in figure 7-2 has a variable focal length of 20 to 80 mm with a f-number of 2.5 and a total weight of approximately 24 ounces. This zoom lens has a through-the-lens view finder which allows the astronaut to see the same field of view as the camera. The entire zoom lens assembly must be stowed in an optics container during lift off or other acceleration periods since it cannot withstand high loadings while mounted on the camera.

One notable feature of both the zoom and wide angle lenses is the air drying provision. Both lenses have a removable desiccant cartridge which absorbs any moisture in the air trapped between the detachable lens and the camera. This cartridge is automatically sealed off when the lens is removed from the camera and then exposed again only when the lens is remounted. Thus, the desiccant will not be saturated between usage and will prevent fogging of the internal lenses for a much longer duration.

17.5 MECHANICAL DESCRIPTION OF THE TV CAMERA

The mechanical configuration of the proposed TV camera is shown in Figure 17-2 and will be approximately 7 by 3 by 3.75 inches. The vidicon will be potted in the yoke and then covered by magnetic shielding. This subassembly is mounted in a sleeve that attaches to the lens. Thus the lens, vidicon and yoke becomes a rigid subassembly in itself, and is mounted in the main housing of the camera. This mounting will constitute vibration isolation of the subassembly.

Vibration isolators are being developed in parallel with a tube-ruggedization effort by the vidicon tube manufacturers.

The electrical circuitry is mounted in the top section of the camera and is primarily packaged in the form of integrated circuits. Components that cannot be packaged in integrated circuit form will be mounted on the printed-circuit board with the integrated circuit.

The power supply will be packaged as a separate subsystem in a magnetic-shielded can. This will decrease the electromagnetic interference problem between the vidicon and the power supply as well as the other circuits.

SECTION XVIII

HF TRANSCEIVER EQUIPMENT, 718H-1E

18.1 INTRODUCTION

This section provides the necessary information to obtain an understanding of the basic operation of the HF Transceiver Equipment 718H-1E, Unit No. C281A13 of the Apollo Communications and Data Subsystem. The function of the HF Transceiver Equipment is to provide beyond line of sight direction finding and voice communication capabilities that will aid in the location of the spacecraft during the post landing and recovery phase of the mission, and will also be used on non-lunar orbital missions for HF communications with MSFN.

The HF Transceiver Equipment is mounted with VHF/FM Transmitter Equipment 56E-1 on a common electrical equipment chassis. The complete unit is designated VHF/FM Transmitter-HF Transceiver 718N-1 Unit No. C28-1A13. The HF Transceiver Equipment consists of the following four modules: (a) power amplifier, (b) radio-frequency translator, (c) if-rf oscillator, (d) radio receiver.

The HF Transceiver Equipment is capable of the following modes of operation on a carrier frequency of 10.006 megacycles: (a) single-sideband (SSB) transmit-receive, lower-sideband only, (b) compatible amplitude-modulation (AM) transmit-receive, lower-sideband voice modulation with full carrier, (c) beacon (CW) transmit only, full carrier with no modulation. The power output when operating in SSB mode is 20 watts peak envelope power (PEP). During AM and CW transmit operation, the carrier power output is 5 watts. Automatic gain control (agc) and automatic

load control (alc) are provided in the receiver and transmitter respectively to maintain a nearly constant operating level.

18.2 LEADING PARTICULARS

The major characteristics of HF Transceiver Equipment 718H-1E are:

a. Over-all Dimensions:

1. Width	10.19/64 inches
2. Height	5 51/64 inches
3. Length	12 inches

b. Weight (includes one half of chassis)

1. 8.0 pounds

c. Power Requirements (maximum values listed)

1. Receive (all modes)	1 watt
2. Transmit SSB (two tone test)	45 watts
3. Transmit AM (100% Mod.)	45 watts
4. Transmit CW	36 watts
5. T/R Relays	3.5 watts

d. Power Supply Voltages

1. Minimum	27 volts dc
2. Nominal	28 volts dc
3. Maximum	30 volts dc

18.3 CONTROLS

Power application to the HF Transceiver Equipment and mode selection are accomplished from Communications Control Panel No. 20. Transmit/receive or receive only modes are controlled from the Audio Control Panels of each astronaut. Operation of the RECOVERY-HF POWER switch to "ON" applies 28 volts dc to the equipment. The modes of operation are controlled from the RECEIVER HF MODE SWITCH. In the SSB position, the Transceiver operates on single-sideband, transmit and receive. In the AM position, the Transceiver operates in the AM mode, with a capability for CW transmission enabled by keying the push-to-talk (PTT) button. In the BCN position, the transmitter is constantly keyed in CW operation if the T/R-OFF-REC switch on the Audio Control Panel is placed in the T/R position. This position bypasses the PTT switch and Audio Center VOX circuits to supply the ground to the T/R relay in power amplifier module to key the transmitter.

18.4 SINGLE SIDEBAND DEFINITIONS

Single sideband in general practice, and as referred to in this section, is actually single sideband with a suppressed carrier. Carrier suppression techniques reduce the level of the carrier but do not eliminate it. This is a useful concept, since the carrier frequency is a reference around which the sidebands are produced in the transmitter and from which the nature of a single sideband signal may be defined. To visualize carrier suppression, consider an SSB transmitter rated at 100 watts output. With 50 db of carrier suppression, the output power contained in the carrier is 0.001 watt.

In essence, a single sideband signal is an AM signal with the non-essential elements, effectively removed. Figure 18-1 illustrates the spectrum occupied by a 3900 kc carrier with AM and SSB signals, each modulated by a single 1 kc tone. The AM signal

consists of a carrier and two identical sidebands which are spaced above and below the carrier by an amount equal to the frequency of the modulating tone. It is the sidebands which contain the intelligence of the signal. The SSB signal contains the same elements as does the AM signal, but there is a marked difference in their relative amplitudes. In SSB the carrier and upper sideband (USB) are suppressed to very low levels. In terms of the relative power contained in each, compared to the lower sideband (LSB), these elements, in effect, have been eliminated. The lower sideband (so called because it is lower in frequency than the carrier) is shown amplified to a level approximately equal to that of the AM carrier. The resulting SSB signal is referred to in terms of the desired sideband and, in this case, is an LSB signal. Suppression of the carrier and unwanted sidebands are generally expressed as power ratios (DB) relative to the peak level of the desired sideband.

18.4.1 Sideband Inversion

The sideband inversion term is used to indicate that, in the lower sideband, the highest modulating frequencies become the lower output frequencies. This is illustrated in Figure 18-2. Let us assume that a carrier wave, f_c , is modulated by two audio frequencies, af_1 and af_2 . The resulting upper and lower sidebands contain both of the modulating frequency components. The upper sideband components consist of the sum of each modulating frequency and the carrier frequency, and no inversion takes place. The lower sideband components consist of the inverted carrier frequency less the modulating frequencies. Inversion occurs in any frequency translating process when the mixing frequency is higher than the signal frequency. The difference products are selected in the output circuit.

FREQUENCY SPECTRUM HF TRANSCEIVER

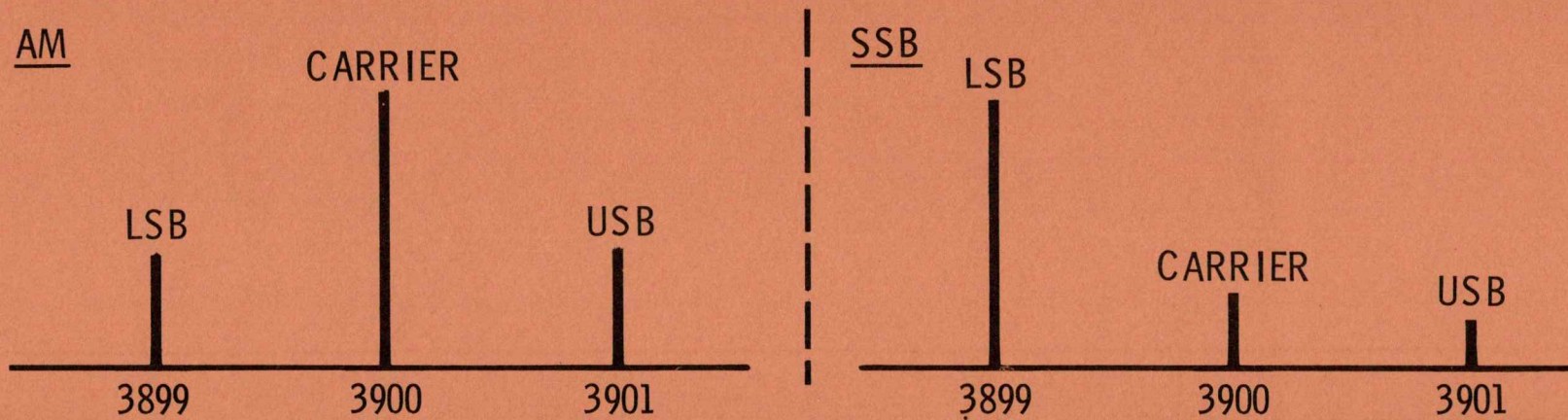


Figure 18-1

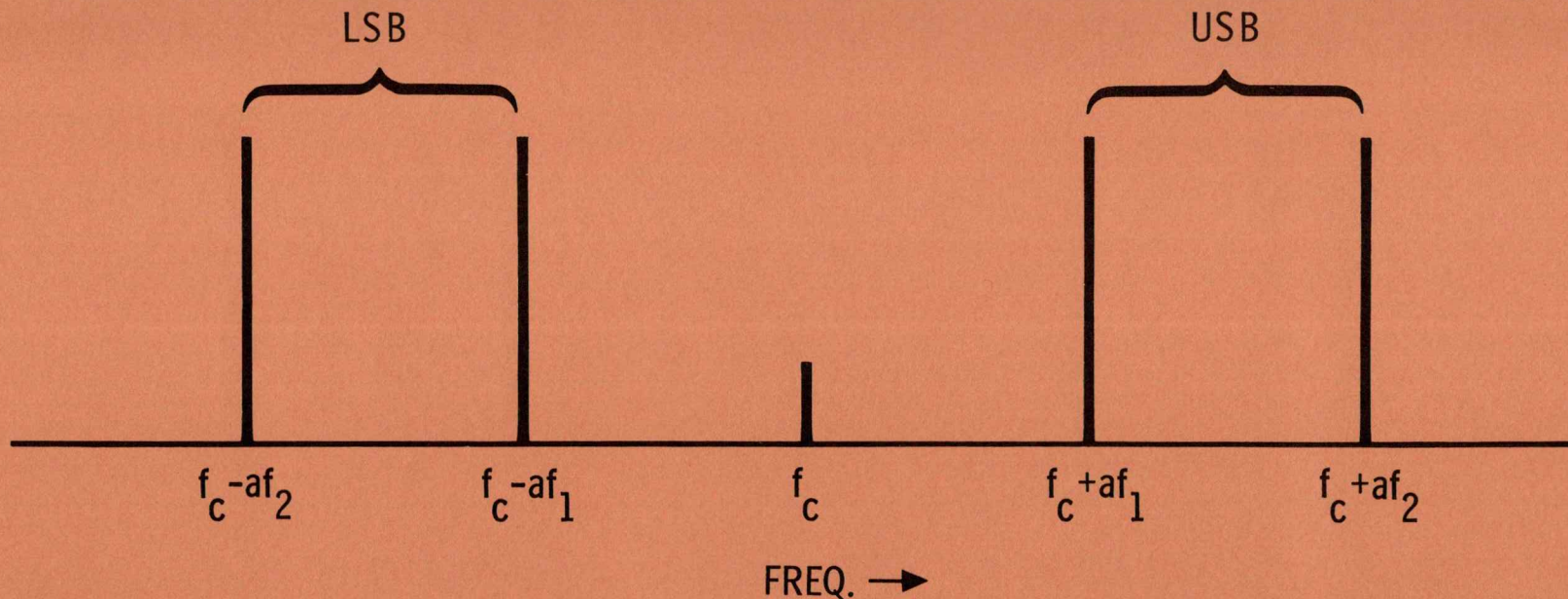


figure 18-2

18.5 FUNCTIONAL DESCRIPTION

See Figure 18-3, Simplified Block Diagram, HF Transceiver Equipment.

When dc power is applied to the SEP, by activation of the "ON-OFF" control on the communications control panel to "ON", 28 volts dc is applied to a voltage regulator in the radio receiver module, which provides a regulated 20 volts dc output. The output of the regulator is applied to circuits within the receiver module as well as to the IF-RF oscillator module. The oscillator module contains two crystal controlled oscillators, 455 kc and 4.7755 mc. The output of the 455 kc oscillator is applied to both the balanced mixer in the rf translator module and also through a carrier reinsert switch to the hf mixer in the translator module. The 455 kc oscillator also provides an output to the product detector in the receiver module. The output of the 4.7755 mc oscillator is doubled and provides a 9.551 mc output signal to the first mixer in the receiver module and also to the hf mixer in the rf translator module.

During receive operation, the rf input (received signal) to the SEP is applied to the receiver module via the T/R relay in the power amplifier (PA) module. The rf input to the receiver module is applied through a narrow bandpass crystal filter, which passes only the desired rf signal. The output of the crystal filter is applied to the rf automatic gain control bridge. This circuitry controls the level of the rf signal in response to an agc voltage supplied by the agc detector. The output of the rf agc bridge is applied to an rf amplifier. The output of the rf amplifier is applied to the mixer agc bridge which also controls the rf signal level in response to the agc voltage. The output of the mixer agc bridge is applied to the first mixer stage. A 9.551 mc signal from the

oscillator module is also applied to the first mixer stage. The first mixer provides an intermediate-frequency (i-f) signal output of 455 kc minus the modulation frequency. The output of the first mixer stage is applied to the input of a three stage i-f amplifier. A sample of the i-f signal at the last i-f stage is applied to the agc detector which provides the agc voltage used in the previous stages.

The i-f signal output of the last i-f stage is applied to the input of an AM detector and an SSB detector. During SSB receive operation, the switch "SSB-AM-BCN" on the communications control panel when in the "SSB" mode turns on the SSB detector. A 455 kc signal from the oscillator module is also applied to the SSB detector. The 455 kc signal is mixed with the i-f signal to provide the demodulated output. During AM, receive operation, the SSB detector is turned off by the "SSB-AM-BCN" switch on the communications control panel being placed in the "AM" position, and the i-f signal is detected by the AM detector. Regardless of which detector is used, the output is applied to the output audio amplifier. The output of the audio amplifier is applied through the SEP signal and control connector to the audio center equipment within the spacecraft.

During transmit operation, the audio input to the SEP is applied to a balanced modulator in the translator module. A 455 kc signal from the oscillator module is also applied to the balanced modulator and the carrier reinsert switch. The balanced modulator provides a double sideband (DSB) with suppressed carrier output signal. The lower sideband (LSB) signal is at a frequency of 455 kc minus the modulation frequency (300 to 3,000 cps) and the upper-sideband (USB) signal is at a frequency of 455 kc plus the modulation frequency (300 to 3,000 cps). The balanced modulator DSB signal is applied to a mechanical filter. The mechanical filter is a 3 kc

SIMPLIFIED BLOCK DIAGRAM HF TRANSCEIVER

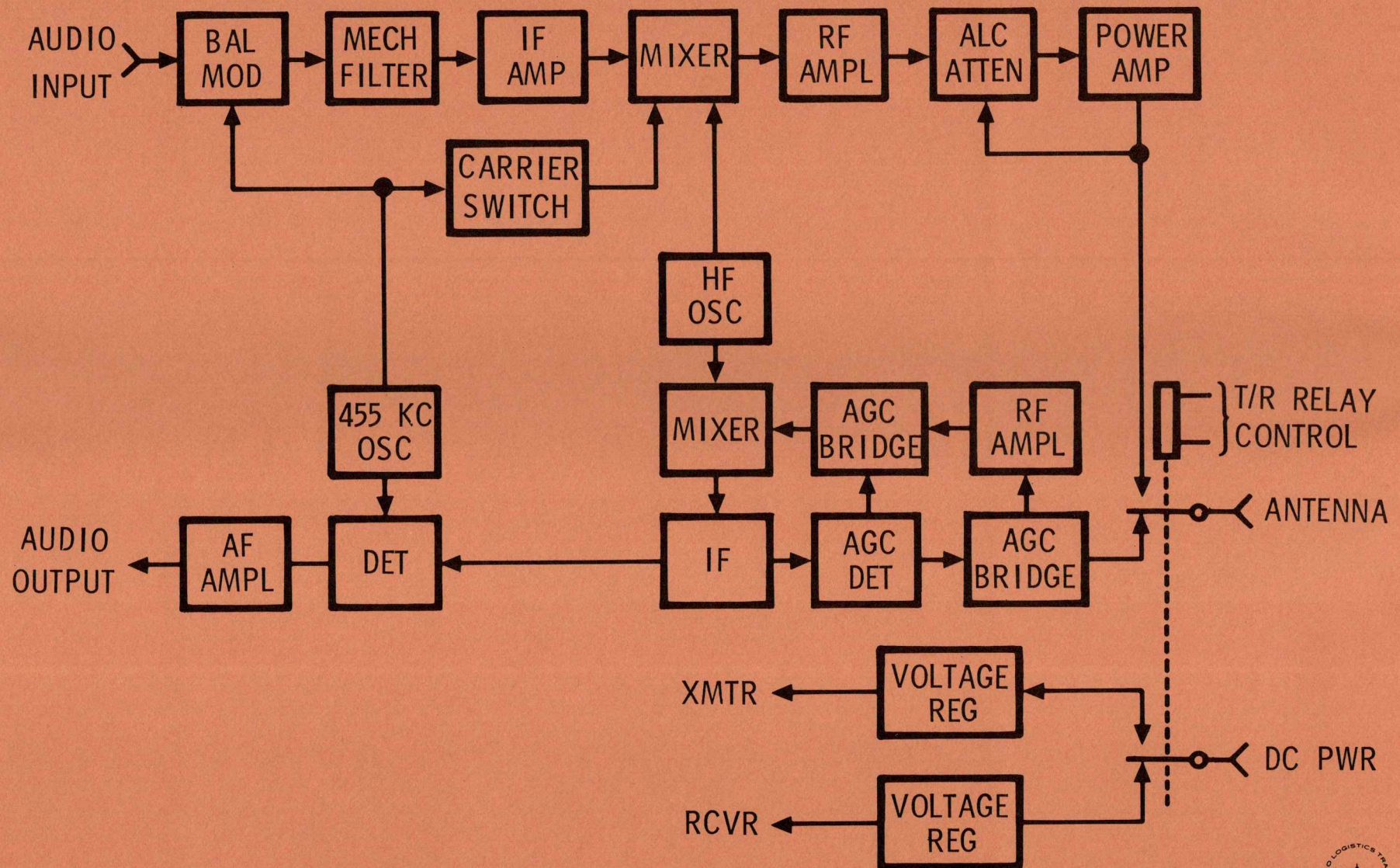


figure 18-3

CD-193



bandpass filter which passes only the LSB signal (455 kc minus audio) and rejects the USB and other out-of-band signals. The LSB signal is applied to a two stage i-f amplifier. The output of the i-f amplifier is applied to a diode clipper circuit which limits the LSB signal to provide nominal speech clipping. The output of the clipper is applied to the hf mixer circuit. A 9.551 mc signal from the oscillator module is also applied to the hf mixer circuit. When AM, operation is selected, (SSB-AM-BCN switch on the Comm Control Panel No. 20 is in the AM or BCN position), the carrier reinsert switch is turned on which causes the 455 kc signal to be applied to the hf mixer circuit. During AM transmit operation, the three signals (LSB, 455 kc and 9.551 mc) are combined in the hf mixer. The output of the mixer is a compatible AM signal at a carrier frequency of 10.006 mc plus the modulation frequency. In either mode of operation the output of the mixer is applied to a crystal filter. The filter is a 3.5 kc bandpass filter which passes the desired (LSB, or LSB + carrier) signal to the rf amplifier. The output of the rf amplifier is applied to the power amplifier via the alc bridge attenuator circuitry. The alc attenuator controls the rf signal level, which is applied to the power amplifier in response to a voltage supplied by a alc detector. The output of the power amplifier is applied to the SEP rf output via the T/R relay which is energized during transmit operation. A sample of the rf output is applied through an alc detector to the alc attenuator circuit to control the transmitter drive level and maintain the rf output voltage of the SEP at the proper level. The SSB-AM-BCN switch on the communications control panel also controls the output of the alc detector to provide the proper output level during AM and beacon operation.

18.6 DETAILED FUNCTIONAL DESCRIPTION

See Figure 18-4, Detailed Block Diagram, HF Transceiver Equipment.

18.6.1 Radio Receiver Module

When dc power is applied to the SEP, by activation of the "ON-OFF" control on Panel No. 20 to "ON", 28 volts dc is applied to voltage regulator Q9 in the radio receiver module, which provides a regulated 20 volts dc output. The 28 volts dc is applied to the receiver module continuously, regardless of whether the transmitter is on or not. This type of operation is required because the sidetone signal is fed back from the T/R relay when the transmitter is on to the input of the receiver module. The output of the regulator Q9 is applied to circuits within the receiver as well as to the circuits in the IF-RF oscillator module.

During receive operation, the rf input (received signal) at 10.006 mc to the SEP is applied to the receiver module via the T/R relay (K1) in the power amplifier module. The rf input to the receiver module is applied to a 3.75 kc bandpass crystal filter, FL1, which passes only the desired rf signal. The crystal input stage helps to prevent blocking and cross modulation. For example, when the rf input signal is weak with a strong signal close to the same frequency, an apparent decrease in receiver gain may be encountered. This loss of gain or reduction of the desired signal is called blocking. It commonly occurs when the voltage from the unwanted signal is sufficient to drive the rf amplifier into distortion. Another effect, produced by a strong signal close to the receiver frequency, is cross modulation. Here, the modulation of the unwanted signal is transferred to the desired signal. Both of these undesired conditions are controlled by the receiver selectivity at the receiver front end.

SCHEMATIC BLOCK DIAGRAM, HF TRANSCEIVER, "D MODEL"

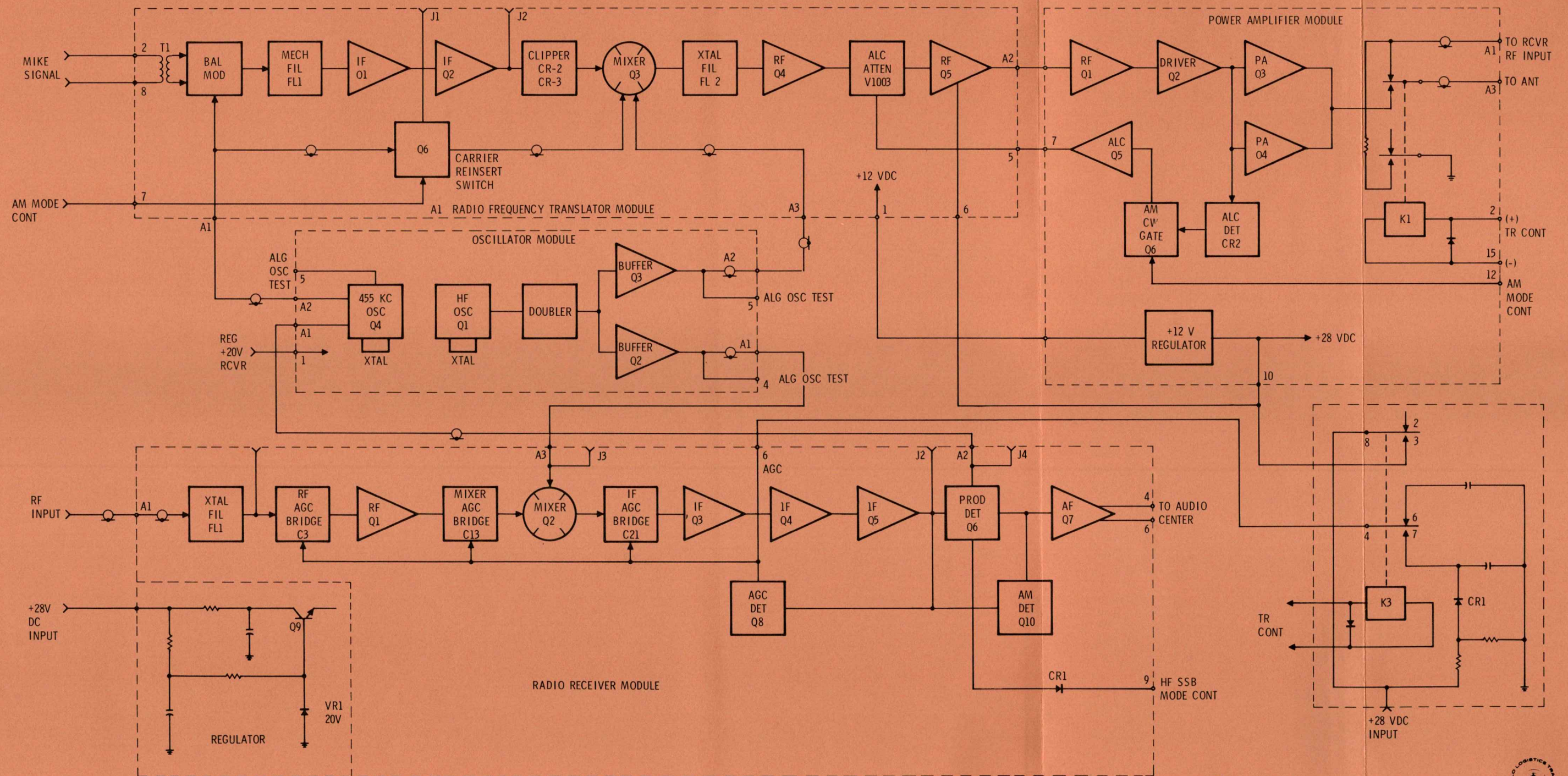


Figure 18-4

Lack of selectivity will allow an undesired signal to pass through the front end circuits without sufficient attenuation to drive the rf amplifier into a non-linear region. The characteristics of the input crystal filter are such that it passes only signals in the 10.002250 to 10.006 mc region, attenuating all signals outside this region. The input impedance of the filter matches the 50 ohm impedance of the receiver antenna. The filter output is transformer coupled to rf automatic gain control (agc) bridge. This circuitry controls the level of the rf signal in response to an alc voltage supplied by agc detector Q8. This bridge, since it is agc controlled, helps to make the first rf amplifier insensitive to strong adjacent signals that could result in cross modulation and blocking.

The output of the rf agc bridge is applied to rf amplifier stage Q1. The output of Q1 is applied through the agc mixer agc bridge and transformer coupled to the mixer stage Q2. The mixer agc bridge controls the rf signal level in response to the agc voltage. A 9.551 mc signal from the buffer stage (Q2) in the oscillator module is also applied to mixer stage Q2. The sum or difference signal of the local oscillator injection frequency and the input signal frequency is the desired output product from the receiver mixer. The difference product is used because it is more convenient to beat the signal down to a fixed lower intermediate frequency, and also because the input signal has to be compatible with the 455 kc signal supplied to the product detector. In this instance the input rf signal is from 10.003 mc to 10.0057 mc and the injection frequency is 9.551 mc. The output of the mixer is then 452.0 kc to 454.7 kc.

The i-f signal from the mixer Q2 is applied to the i-f agc bridge which controls the i-f signal level in response to the agc voltage. The output of the i-f agc bridge is applied to the input of a three stage i-f amplifier consisting of Q3, Q4, and Q5. The i-f amplifiers of the super heterodyne receiver provides the receiver amplification, selectivity and gain control. The type of i-f amplifier used in the receiver is a concentrated selectivity amplifier. Most of its selectivity is obtained from the agc bridges and the crystal filter front end. This arrangement provides protection against strong off-resonance signals, so that the only signals the i-f stage has to contend with are those in the receiver passband. Thus, the i-f amplifier is not subject to blocking and cross modulation. This also removes the requirement that interstage coupling be required to furnish selectivity, and simpler coupling circuits can be employed. A sample of the i-f signal output of Q5 is applied to agc detector Q8 which provides the agc voltage used in the previous stages. In the receiver, a control loop is included to automatically adjust the rf gain. Control of receiver gain will hold the output relatively constant despite changes in rf input levels. In SSB operation, the dc control voltage is derived from the composite signal. By application of this dc control voltage to the agc bridge networks, the desired degree of gain adjustment is realized. Since this is a suppressed carrier receiver, the control voltage must be generated rapidly to avoid transient overload at the beginning of each portion of a transmission. The gain adjusting action must take place rapidly to avoid a thump at the start of the first syllable in voice signals. The syllabic envelope of the SSB voice signal is similar to that of the original audio signal, that is, it fluctuates in amplitude at a low frequency rate. The agc voltage rises

rapidly with the start of the syllable and then maintains the level of control voltage with a longer time. To avoid rapid fluctuations in the receiver gain, the agc control is held at a value corresponding to the average of several syllabic undulations of the signal. This arrangement provides a fast attack-slow decay agc time constant circuit.

The i-f signal output of Q5 is applied to the input of AM detector Q10 and SSB detector Q6. During SSB operation, the mode control switch (SSB-AM-BCN) enables the product detector Q6 when the switch is in the SSB position. To demodulate the SSB signal, it is necessary to have a local carrier signal having the same frequency relationship to the SSB signal as the original carrier in the transmitter has to its generated sideband signal. The product detector produces an output that is the product of the carrier and the sideband voltages. For SSB demodulation, only the difference frequency is utilized. The carrier injection frequency, from the oscillator module, is 455 kc and the signal input frequency from the i-f amplifier is 452.0 to 454.7kc. Therefore, due to mixing action in the product detector, the difference frequencies from the product detector will be 300 cps to 3,000 cps (455 kc minus 452.0 to 454.7 kc). During AM operation, Q6 the product detector is back biased and the i-f signal is detected by AM detector Q10. Regardless of which detector is used, the output is filtered and applied to audio amplifier Q7. The output of Q7 is transformer coupled through the SEP signal and control connector to the audio center equipment. In the audio center equipment the signal is applied through isolation and diode switching networks to the earphone amplifier. The output of the earphone amplifier is applied through a master volume control to the astronaut's headset.

18.6.2 IF-RF Oscillator Module

The if-rf oscillator module receives its regulated dc voltage from the voltage regulator in the receiver module. The oscillator module contains two crystal controlled oscillators, Q1 and Q4. The output of crystal controlled oscillator Q4 is a 455 kc signal which is applied to both the receiver and rf translator modules. The output of crystal oscillator Q1 is a 4.7755 mc signal which is applied to a doubler circuit and then is applied to the inputs of buffer stages Q2 and Q3 to provide a 9.551 mc output signal. The output of Q2 is applied to the hf mixer in the receiver module. The output of Q3 is applied to the hf mixer in the translator module.

18.6.3 Radio Frequency Translator Module

During transmit operation, the audio input from the microphone amplifier in the audio center equipment, is applied to a balanced modulator in the translator module. A 455 kc signal from the if-rf oscillator module is also applied to the balanced modulator and the carrier reinsert switch. The balanced modulator is a basic diode ring type modulator that produces the two sideband signals but suppresses the carrier. The audio input signal (300 to 3,000 cps) along with the carrier (455 kc) is translated to two sideband frequencies. The upper sideband signal is 455.3 kc to 458 kc. The lower sideband signal is 454.7 kc to 452.0 kc. Since the carrier is suppressed or nearly eliminated only the sideband signals remain.

The balanced modulator DSB signal is applied to mechanical filter FL1. The mechanical filter will pass, without discrimination, the desired sideband, in this case 452 to 454.7 kc. The mechanical filter provides the almost ideal bandpass response, steep skirts and flat top. A mechanical filter consists of

a magnetostrictive transducer, (to convert electrical oscillations into mechanical oscillation and then convert mechanical oscillations back into electrical oscillations), and mechanically resonant discs and disc coupling rods. An electrical signal sent through the input transducer coil creates a magnetostrictive effect on its core. The core, attached to the resonant discs, alternately elongates and shortens, causing the discs to vibrate at their resonant frequency. A second transducer at the output end of the assembly converts the mechanical movement back to electrical variations. The effect is that of an elaborate multi-section L-C filter. Therefore, the output of the mechanical is only the LSB. The LSB signal is applied to a two stage i-f amplifier consisting of Q1 and Q2. These stages provide the first amplification for the signal before it is presented to a clipper circuit, CR2 and CR3, which limits the LSB signal to provide a nominal 16 db of speech clipping. The output of the speech clipper is applied to hf mixer Q3. A 9.551 mc signal from the if-rf oscillator module is also applied to the mixer Q3. The operation of the transmitter on all modes is the same to this point. In the mixer stage, however, the operation is determined by the type of emission desired. When AM operation is selected, a ground is applied to the 455 kc carrier reinsert switch circuitry in the translator module via the AM mode control line which causes the 455 kc signal to be applied to the mixer Q3. During AM transmit operation, the three signals (452 - 454.7 kc, LSB IF; 455 kc carrier, and 9.551 mc) are combined in mixer Q3. The output of Q3 is a compatible AM signal at a carrier frequency of 10.006 mc with lower sideband modulation only. During SSB transmit operation, only two signals (452-454.7 LSB, IF and 9.551 mc) are applied to mixer Q3. The output of Q3 is an LSB signal of 10.006 mc plus the modulation frequency. In either mode of operation, the output of Q3 is applied to crystal

filter FL2. FL2 is a 3.5 kc bandpass filter which passes the desired (LSB, or LSB + carrier) signal to rf amplifier Q4. The output of rf amplifier Q4 is applied to a second rf amplifier, Q5, via the alc bridge attenuator circuitry. The alc attenuator controls the rf signal level, which is applied to Q5, in response to a voltage supplied by the alc detector in the Power Amplifier module. The alc attenuator consists of a bridge that contains a voltage variable capacitor (varactor). The bridge normally operates in an unbalanced condition and allows the rf signal to pass with a minimum of attenuation. Automatic level control sensing is accomplished in the power amplifier module, and the dc signal from the alc detector is fed to the rf translator module. When the output of the power amplifier increases beyond the desired level, an alc generated voltage is fed to the alc attenuator. The alc voltage increases the reverse voltage of the varactor, reducing the capacitance. This reduction in capacitance causes the bridge to be moved closer to the balanced stage, resulting in an rf output which has been attenuated below the normal level. Thus the alc control maintains a constant power output from the power amplifier. The output from the alc attenuator is amplified in rf amplifier Q5 before it is applied to Q1 in the power amplifier module. DC power (+28 volts dc) is applied to the power amplifier module through relay K3, located in the SEP chassis, when the PTT or the VOX circuitry keys the transmitter. RF amplifier stage Q1 operates class A with a gain of approximately 20 db. The output of Q1 is applied to driver stage Q2. RF driver stage Q2 operates class AB with a gain of approximately 10 db. The output of Q2 drives the power amplifier stage Q3-Q4. The power amplifier stage operates class AB with the two transistors in a parallel arrangement, providing approximately 10 db of gain. The output of this final rf ampli-

fication stage is applied to the SEP output via the T/R relay K1 which is energized during transmit operation.

A sample of the rf output voltage at the driver stage is applied to the alc detector circuit consisting of CR2, Q5 and Q6. The alc detector provides a dc voltage to control the transmitter drive level and maintain the rf output voltage of the SEP at the proper level. A ground on the AM mode control line provides mode information to the alc detector to provide the proper output level during AM and beacon operation.

A portion of the power amplifier output is used to operate the sidetone circuitry. When keying T/R relay K1 is closed in the transmit position, a capacity exists between the open receiver contacts which feed a portion of the transmitted rf signal to the output stage of the receiver. The receiver processes this as it would a normally received signal and applies it to the audio center equipment earphone amplifier. Thus, to obtain sidetone, the hf transmitter would have to be on.

SECTION XIX

CENTRAL TIMING EQUIPMENT

19.1 INTRODUCTION

The Central Timing Equipment (CTE) is the basic clock of the Apollo Spacecraft. This clock is highly stable, as it is phase locked to the Guidance Computer's temperature controlled crystal oscillator. Discrete components being replaced by integrated circuits, and complete redundancy make the CTE extremely reliable.

The CTE is capable of supplying signals between 512,000 cps and one cycle per 20 days. These signals can be used for the purpose of synchronizing any digital or analog system in the spacecraft which depends on a regular frequency for proper operation. It also generates and stores the day of the month, the hour, the minute and the second. This time can be Greenwich Mean Time (GMT or zulu time); or, if it is found to be more usable, Eastern Standard Time. Time may also be counted from launch instead of GMT by the CTE. This time is stored in a binary coded decimal form--a standard, easily decoded form--in the time accumulator of the CTE. This time code can be handled easily by PCM Telemetry, digital type displays, or any digital system.

19.2 CTE FUNCTIONS

The CTE supplies a 512 kc signal to three systems in the spacecraft. This signal is supplied to the PCM Telemetry Equipment to synchronize its internal clock. The internal clock also has free-running capability but at reduced accuracy and reliability. The 512 kc is supplied to the Automatic Check-out Equipment (ACE) to synchronize the data

from the Apollo PCM, the LEM PCM, the Apollo Carry-On equipment, and LEM Carry-On equipment. The important function of data interleaving cannot be carried out without synchronization. The 512 kc is also supplied to the PMP equipment. This signal supplies the modulating frequency for the emergency key and normal voice.

Three signals at 6.4 kc are supplied to the three ac power inverters. These signals synchronize the 400 cycle frequency of the ac power. The stability of the ac power frequency in turn is passed on to the Data Storage Equipment and one section of the Stabilization and Control Equipment.

A signal at 4 kc is supplied to the delta V section of the Stabilization and Control Equipment. This signal provides the required time information to calculate change in velocity.

Synchronization, sequencing and time displays are all accomplished by 1 cps from the CTE. The PCM telemetry equipment uses this signal to synchronize the subframe of the PCM data. PACE uses 1 cps to synchronize the major subframe of the PACE data. This same signal is supplied to the display panel for use in the T-timer. The T-timer is a time interval display which counts seconds and can display up to 999 seconds. It is used during the first 999 seconds of the mission. The power programmer for AF-9, using 1 cps, sequences action in the electrical system and is used on AF-9 only.

SPACECRAFT CENTRAL TIMING EQUIPMENT (SCTE)

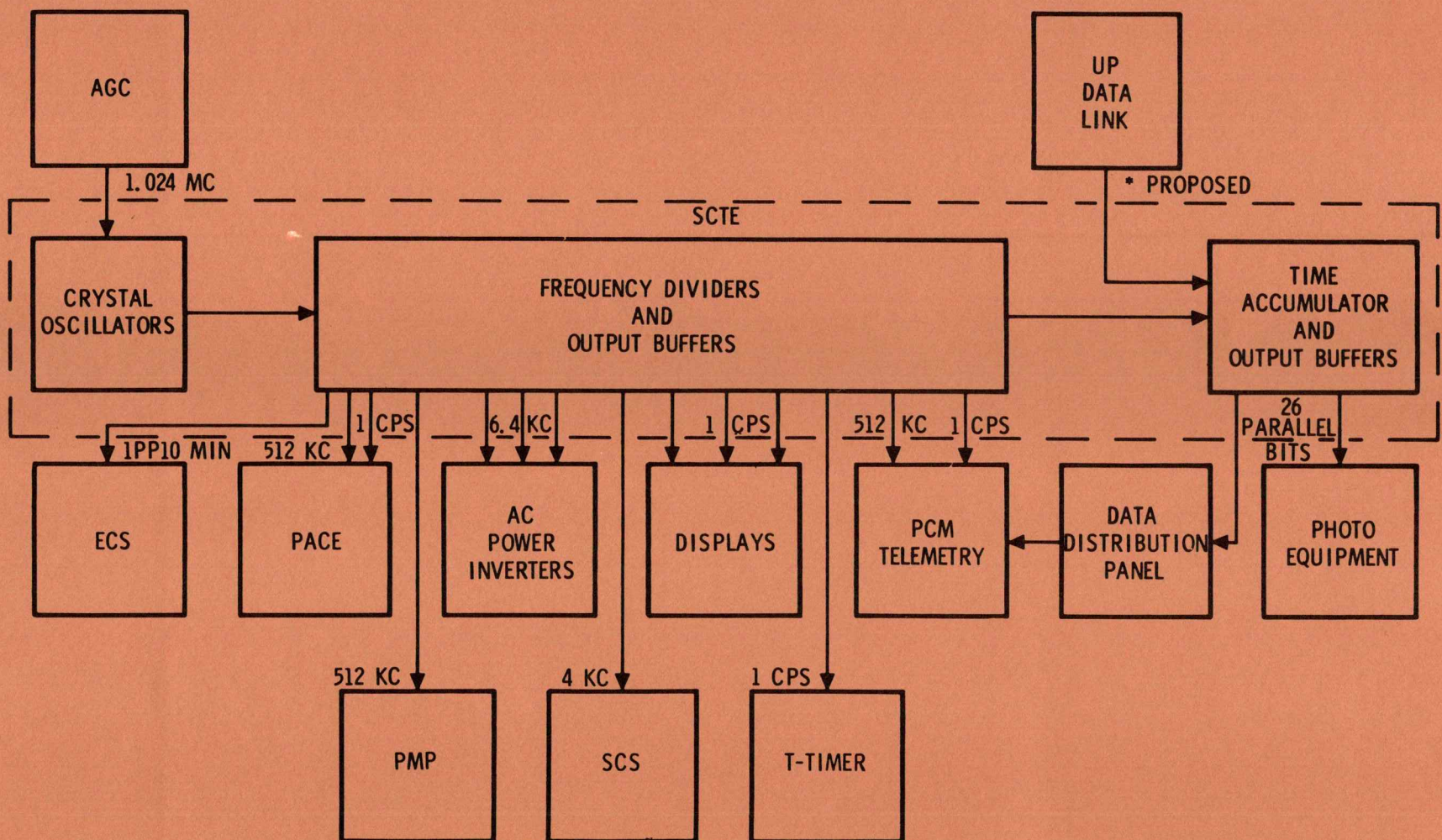


Figure 19-1

CD-132A



CENTRAL TIMING EQUIPMENT

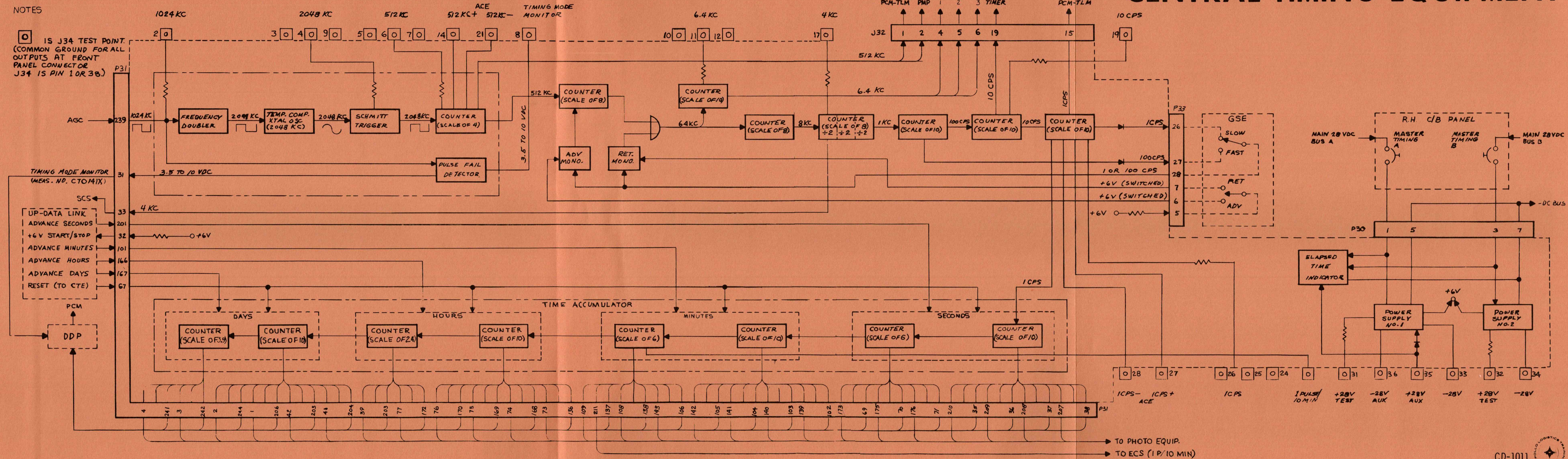


Figure 19-2

A signal at 1 cycle per 10 minutes is supplied to the Environmental Control equipment for use in the water separator accumulator. This signal is the stimulus to open a solenoid for 10 seconds of every 10 minutes to remove water from the space-suit.

A time code output, as mentioned above in GMT, EST, or launch time, is provided to the PCM Telemetry Equipment. This time code is treated as data and becomes part of the telemetry format. The photographic equipment, which varies from mission to mission, also receives the time code. The CTE time code will be displayed as part of the photographic data.

19.3 OPERATION

Figure 19-1 shows a block diagram of the CTE and its outputs. The redundant 1.024 mc crystal oscillator is pulsed each cycle by the AGC. The oscillator output feeds a series of nine frequency dividers which give an overall division of 1,024,000. This gives an output of 1 cps plus pick-off points between the dividers. The 1 cps output drives the time accumulator section. Twenty-six bits out of the time accumulator indicate the day, hour minute, and second to the PCM Telemetry, and photographic equipment. Each output frequency and bit is fed through an output buffer amplifier in the CTE.

19.4 GENERAL SYSTEM CONCEPT

The CTE can be divided into 5 basic components as follows: (refer to figure 19-2) crystal oscillator, frequency dividers, universal Time Accumulator, Power Supply and Output buffering circuitry. Each basic section shall be discussed in detail.

19.4.1 Power Supply System

The power supply system consists of two separate identical pulse width modulated power supplies. Each supply is designed to operate from separate power input lines at a nominal 28 VDC level. Input grounds are to be isolated from system grounds.

Each supply must be capable of handling full load when operating alone or sharing the load (not necessarily 50/50) when operating together. Power switchover must not affect system performance.

A single failure in either supply shall not cause a system failure. Short circuit and over voltage protection is required.

19.4.2 The Oscillator System

The oscillator system consists of primary and secondary modes. In the primary mode, a 1024 kc input signal is received from the guidance computer. The input pulse is doubled in frequency, shaped and fed to a divide by four majority logic network.

The output of the network comparator is 512 kc. Up to this point, SYSTEM REDUNDANCY has been used. The output pulse is then fed to a COMPONENT REDUNDANT amplifier circuit and out to component redundant buffers.

In the secondary mode, the 1024 kc pulse is doubled in frequency and phase locked to a temperature compensated oscillator. The oscillator has a stability of 2.2 parts per million over the ambient spec requirement of 0°F to 150°F. The oscillator dissipates about twenty milliwatts. The oscillator output is fed resistively to the divide by four majority logic network. The primary mode network always drives the divider network due to capacitive coupling.

A single failure of a component in either network will not cause the output 512 kc frequency to vary.

The output signal is phase locked to the input signal in the primary mode. In case the primary mode network fails, the secondary mode takes over and the output frequency is still controlled by an input signal. If the signal fails, then the secondary mode takes over, using the temperature compensated oscillator as a driving source.

19.4.3 The Frequency Divider System

The frequency divider system is comprised of various ripple and Johnson counters. The counter groves are comprised of INTEGRATED CIRCUIT FLIP-FLOPS AND NAND GATES.

The divider counter functions are SYSTEM REDUNDANT. A two out of three majority logic network is used. Each redundant network terminates at a COMPONENT REDUNDANT amplifier, which in turn drives the following counter chain, the output buffers, and resets the counter network.

Test points are all associated with the last flip-flop in each counter grove.

An advance and retard control circuit is associated with the front end of the frequency divider. Its function is to vary the leading edge of the cps output with respect to an external time standard such as the WWV one second pulse.

19.4.4 The Universal Time Accumulator System

The universal time accumulator system is comprised of a non-redundant 26-bit binary coded

decimal counter grove. The counter is completely comprised of INTEGRATED CIRCUIT Flip-Flops and NAND GATES.

Associated with the time accumulator are various control circuits which set the counter to Greenwich Mean Time before launch. Besides being used as a time accumulator, the counter is used to supply a special non-redundant frequency output of one 10-second cycle every 10 minutes.

19.4.5 Output Buffering Circuits

The output buffering circuits are both redundant and non-redundant, depending on the application. At the frequency divider, the reliability requirement is .999999 for each single buffer, which in turn requires component redundancy at the buffer and system redundancy behind it. In the time accumulator, each of the 26 bits must have three (3) buffered outputs. Each set of outputs has a reliability requirement of .999, which allows the system to be non-redundant using high rel parts.

19.5 POWER SUPPLY LOGIC DESCRIPTION

Figure 19-3 contains the power supply logic diagram.

The CTE power supply system is comprised of two identical power supplies. Each supply is capable of handling part of the load to complete full load under all environmental and voltage input conditions.

Each supply contains input and output ground isolation. The input and output grounds are transformer isolated through the power circuit and transformer isolated through the control circuit. The power requirement of the CTE is 25 watts or less.

POWER SUPPLY LOGIC DIAGRAM

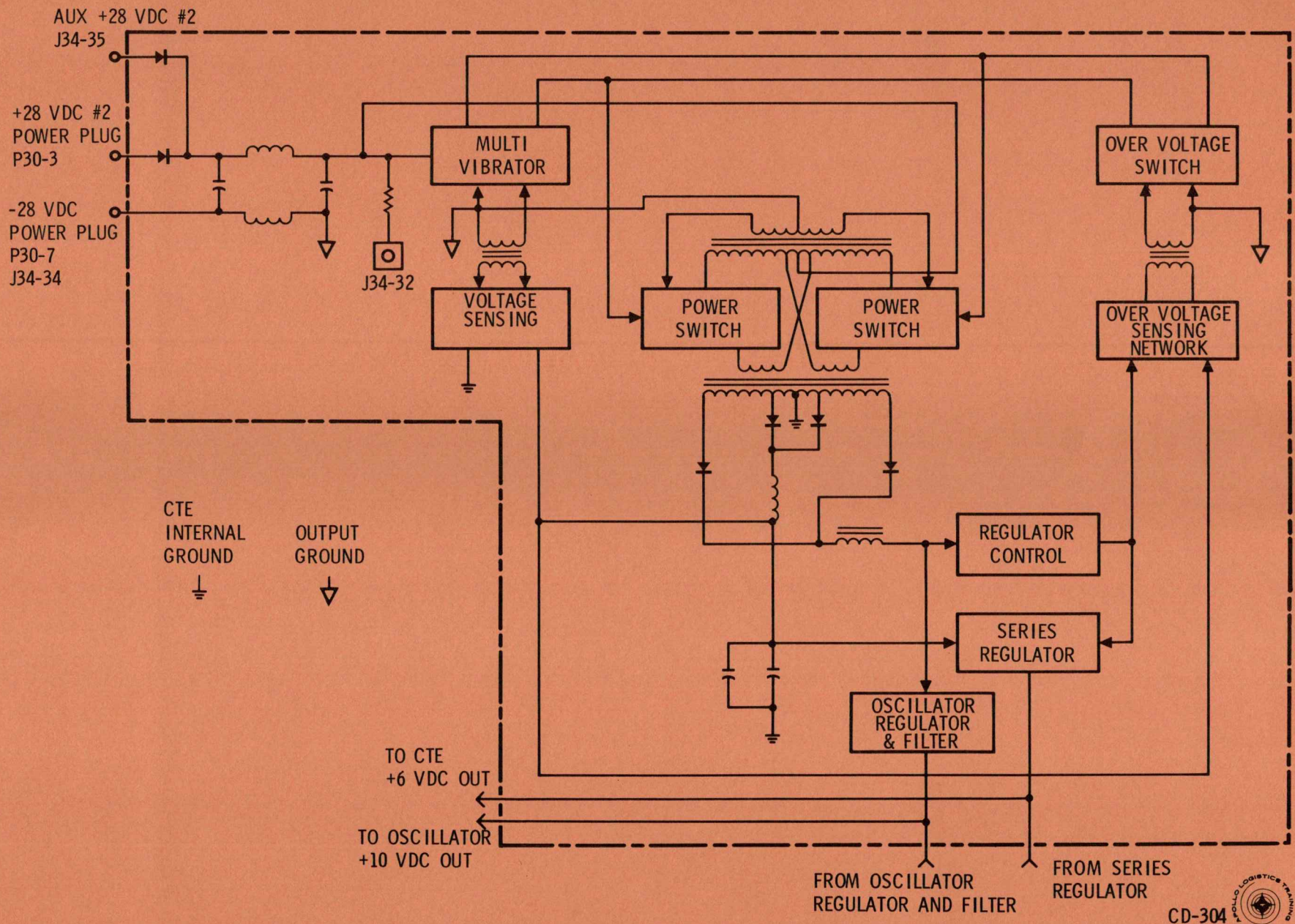


Figure 19-3

This requirement is easily met by the redundant power supply scheme with 10 to 13 watts to spare. The output circuit is designed for 6 volts at a 1.2 amp maximum load condition. This means that at average efficiencies, the CTE should be operating from 13 to 15 watts. The highest efficiency of the CTE power supply which contains the diode isolated inputs for polarity reversal is 65% at 25°C at 20 volts D.C. in, with a full load of 1.2 amps. The lowest efficiency is 52% at 85°C at 32 volts D.C. in, load sharing at 600 milliamps. Under normal operating conditions, the efficiency is 63% at 25°C at 28 volts D.C., with a full load of 1.2 amps. Without the input polarity reversal diodes and the output over-voltage protection circuit, the efficiency of a single supply could be easily increased 10% over the environmental range. The power supply system must operate if any single component fails. The major failure mode of a power supply is when the zener in the voltage sensing network opens and the voltage tends to rise. This is handled by utilizing an overvoltage protection circuit in each supply which contains the voltage to the spec requirement of a maximum of 6.3 volts D.C.

The operation of the system can best be described by referring to Figure 19-3. The power supply can operate from a voltage range of 20 to 32 volts under specified environmental conditions. The power supply is of the pulse width modulated design which insures maximum efficiency under varying input and output conditions. The supply is fundamentally a D.C. to D.C. standard flux oscillator with the exception that the frequency of oscillation is not dependent on voltage but is dependent on load requirements. Energy from the line is taken in short spurts only upon need rather than constantly regulating the input current to

the output requirements. A change in load requirement changes the energy level into the power supply. The power supply is comprised of the following circuits (refer to Figure 19-3):

1. An input circuit consisting of diode isolators and an RFI filter.
2. A triggering multivibrator which sets the oscillation frequency for the power supply.
3. A non-saturating square loop core transformer which drives the power switch.
4. The power switch which drives the output transformers. The power switch is a two transistor silicon device switching amplifier.
5. The output transformer is a non-saturating square loop core transformer.
6. The output filter which consists of a full wave bridge and an inductive input filter.
7. A series regulator which acts as the over-voltage protection circuit along with the regulator control circuit. This regulator circuit is driven from a 10 volt source which consists of a full wave bridge and an inductive input filter also. The output of the series regulator circuit is approximately 6 volts under normal operating conditions.
8. Over-voltage sensing network, which senses a voltage spread when the collector-to-base voltage of the series regulator goes above a pre-set level.

9. The over-voltage switch, which triggers when an over-voltage condition exists on the input of the series regulator.
10. The voltage sensing network which senses voltage variation due to load variation at the output of the LC filter on the primary output line. Any change in output voltage causes the voltage sensing network to fire, thereby changing the frequency of the multivibrator, which in turn triggers the power switch. The power switch causes energy to be transferred from line to output filter.

19.6 LOGIC DESCRIPTION OF OSCILLATOR

The oscillator is a one-out-of-two system redundant circuit (Refer to Figure 19-4). Both the primary and secondary modes are phase locked to a 1024 kc input signal from the guidance computer. In the normal operation, the signal is transmitted to Doubler "B", which doubles the 1024 kc signal to a 2048 kc signal, as can be noted at test point J34-2 and test point P31-119. The 2048 kc signal is transmitted to Schmitt trigger "D". The input wave form is squared up, as shown in test point P31-121. It is transmitted through the capacitive couple mixer through Schmitt triggers "A", "B", and "C". It should be noted that at test point J34-3, the output wave form follows the primary mode signal and not the secondary mode signal, even though the secondary mode signal is phase locked to the incoming signal.

In case of a failure in the primary mode, the 1024 kc pulse is fed to Doubler "A", which phase locks the temperature compensated crystal oscillator circuit to the 1024 kc input signal. The output of the doubler is shown at test point P-31-118, while the phase relationship of the oscillator to the input signal

is shown at test point P31-120. Referring again to the oscillator logic diagram, one should note the output signal to the resistive mixer in the secondary load and note that at test point J34-3, even though the secondary mode is present, the primary mode takes precedence.

Then, with either the primary or secondary modes operating, or both circuits operative, the output wave forms of Schmitts "C" and "B" are at a 2048 kc rate, which can be noted from test point J34-9 and test point J34-4 and J34-3. The outputs of the Schmitt triggers "A", "B", and "C" are fed to a divider by four shift counter, which has an output of 512 kc, which is noted at test point P31-51.

The circuit acts as a one-out-of-two redundant system up to the point of mixing, wherein the primary mode is capacitively coupled to a two-out-of-three majority logic switching system while the secondary mode is resistively coupled to the same logic system. It should be noted that no single failure in either the primary, secondary mode will cause the output of the comparator to vary from 512 kc.

19.7 FREQUENCY DIVIDER LOGIC DESCRIPTION

Figure 19-5 contains the frequency divider logic diagram.

The frequency divider system contains seven groves of two-out-of-three majority logic divider chains. The countdown circuits are comprised of integrated circuit logic. The 51 Series T1 integrated circuit is used extensively in the countdown logic.

The 512 kc signal is fed into three parallel divide by eight Johnson counters. The reason for using a shift register Johnson counter at this

OSCILLATOR LOGIC DIAGRAM

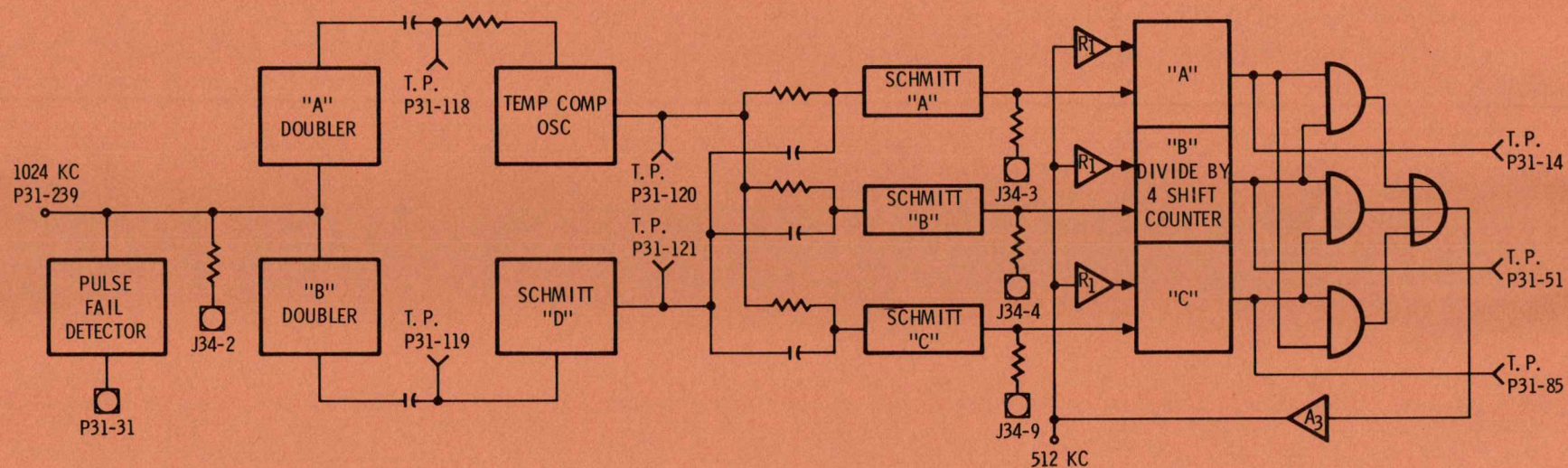


Figure 19-4

19



19-10

frequency is because the counters actually shift at the rate of the last counter, which would be 64 kc rather than at 512 kc. The outputs of the counter are fed to a majority logic AND gate; the output of the AND gate is fed through an OR gate to a quad redundant amplifier, which in turn feeds the signal to the next counter groove and also resets the preceding divide by eight Johnson counters. This reset is necessary in case one of the counters were to lost their phase relationship with each other due to a transient. The output of the 64 kc amplifier is fed to a divide by eight Johnson counter grove, which puts out an 8 kc signal and also to a divide by ten Johnson counter, which puts out a 6.4 kc signal to three quad redundant buffers. This is the first output of the frequency divider chain. The output of the 8 kc counter grove is fed to a divide by eight ripple counter chain, whose output is a 1 kc signal. A 4 kc signal is tapped off the first binary of the divide by eight ripple counter, and its output is to the 4 kc buffers.

The output of the 1 kc amplifier is fed to a divide by ten Johnson counter, whose output is 100 cps. The output of the 100 cps counter is fed to both a divide by ten Johnson counter grove and to the FAST switch, which controls the advance and retard monostable. All switch controls for advance and retard, both FAST and SLOW, are external switches to the Central Timing Equipment.

With the retard switch closed and the advance and retard switch in the FAST position, the one cycle per second pulse is advanced as follows:

1. Plus 6 volts D.C. is fed through Pin J35-7 through the retard switch, through P35-10, which supplies power to the 80 microsecond retard monostable.

2. The 100 cps pulses are fed through an isolation resistor to Pin P35-24 through the external switch to Pin P35-31. From Pin P35-31, the 100 cps pulses are fed through an isolation amplifier, which in turn triggers the retard monostable. The isolation amplifier buffers the monostable from transient triggering.
3. The output of the retard monostable blocks the 512 kc pulses from triggering the divide by eight Johnson counters for approximately 75 microseconds per trigger. As the control switch was set in the FAST position, the one second per cycle pulse is retarded at the rate of approximately 7500 microseconds per second.

The slow retard works in the same fashion as described above except the control pulses come from the one cycle per second output. The advance control system works in exactly the same manner except the period of the advance monostable is longer (550 microseconds) and the divide by eight Johnson counter is changed to a divide by seven during the monostable pulse period.

The frequency divider logic is broken up into divide by eight Johnson counter, divide by eight ripple counters, and divide by eight Johnson counters for two basic reasons.

1. The small increment provides for high reliability and interchangeability.
2. Many of the frequencies shown have been used in past models such as the 100 cps and 1 kc outputs that are not used in the present model. This system provides for maximum flexibility in case other outputs are required at these frequencies in the future.

19.8 THE TIME ACCUMULATOR LOGIC DESCRIPTION

Figure 19-6 contains the time accumulator logic diagram. The diagram is split into three basic sections, the 26-bit BCD counter, the control circuit, and the one pulse per 10 minute circuit.

The 26-bit BCD counter is comprised completely of Texas Instruments Series 51 Type integrated circuits. The counter is broken up into six basic sections, which are as follows:

1. The seconds counter, which is a divide by ten counter containing four bits.
2. The seconds x 10 counter, which is a BCD counter that divides by six.
3. The minutes counter, which is a BCD counter which divides by 10, containing four bits.
4. The minutes x 10 counter, which is a BCD counter dividing by six containing three bits.
5. The hours and hours x 10 counter, which is a divide by 24 counter containing six bits.
6. The days and days x 10 counter, which varies in count time depending on the day of the month, which is externally set into the time accumulator. This counter contains six bits.

The output of each bit of the time accumulator is an SN-514A type integrated circuit, which drives the output time accumulator buffers. Each bit drives three isolation buffers.

The time accumulator control circuits are comprised of a start-stop circuit, a reset circuit, and a set circuit. The start-stop circuit is a positive controlled binary which controls the one cycle input of the divide by 10 seconds counter. The binary either blocks or passes the one cycle per second pulses. The binary is positively controlled, requiring a closure of the start-stop switch and the switch leading from Pin J35-14 and J35-6; both closures are required for circuit operation. The reset switch sets the time accumulator counters to the zero position, except for the days counters, which is set to zero one.

Setting the time accumulator to the GMT Time is done by setting the control switch to either the seconds, minutes, hours, or days position, the control switch to the MANUAL position, and pulsing the set switch the appropriate number of times. The set switch triggers the monostable at Pin J35-28. The output of the monostable at Pin J35-27 pulses once for each depression of the set switch. The pulse is routed through the manual switch to the appropriate seconds, minutes, hours, or days counter.

By utilizing an external generator, the time accumulator can be turned over rapidly, setting the switch to the external position and the external control switch to either the seconds, minutes, hours, or days position. The ten second pulse for ten minute circuit derives its input from the divide by 6, seconds x 10 counters, and the divide by 10 minutes counters. The input circuit is a multiple AND Gate which decodes the binary coded decimal inputs and provides a 10 second per 10 minute isolated pulse output. The output has a rise and fall time of less than 10 microseconds, with a duty cycle of 10 seconds plus or minus less than $\frac{1}{2}$ a second.

No test points are required for the time accumulator as it is not redundant and all outputs are available at the CTE connectors. With each 26-bit set, there are four signal grounds and one chassis ground available.

TIME ACCUMULATOR LOGIC DIAGRAM

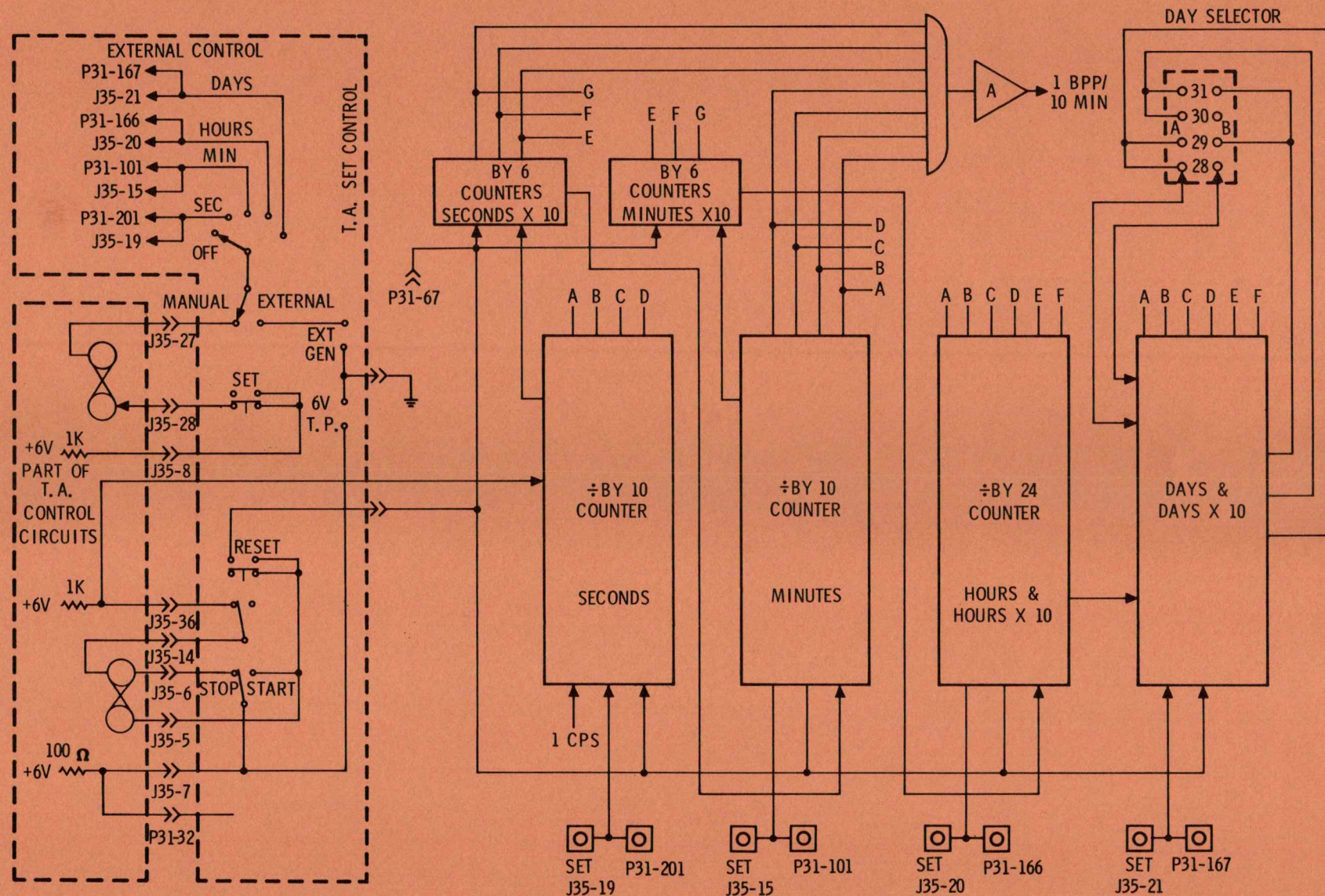


Figure 19-6

19.9 BUFFER SYSTEM LOGIC DESCRIPTION

Frequency divider buffers are all quad redundant, having a reliability of .99993 for 5000 hours. The goal is .999999 for 336 hours.

Each frequency divider buffer and the 1 PP/10 min. buffer has a test point associated with the output terminating at Plug J34. All frequency divider buffers are drivers from quad amplifiers.

The time accumulator buffers are non-redundant. Each set contains twenty-six buffers representing the 26-bit BCD, GMT code. The buffer set has a reliability requirement of .9993 for 336 hours. The goal is .999. There are no test points associated with the time accumulator buffers. Three buffers per bit are driven from an SN514A type integrated circuit (51 Series - Texas Instruments).

SECTION XX

VHF RECOVERY BEACON, 56F-1D

20.1 INTRODUCTION

This section provides the necessary information on the VHF Recovery Beacon Transmitter Equipment for a basic understanding of the operation of the equipment. The Recovery Beacon Equipment and the VHF/AM Transmitter-Receiver Equipment 718J-1D share a common electrical equipment chassis, which forms the VHF/AM Transmitter-Receiver-VHF Recovery Beacon Transmitter Equipment 718P-1D of the Apollo Communication and Data Subsystem. This equipment is installed in the lower equipment bay of the Apollo Spacecraft and is used with complementary airborne direction-finding equipment to provide line-of-sight direction-finding capabilities for recovery operations. After main parachute deployment, and for 72 hours thereafter, the VHF Recovery Beacon transmits an interrupted tone-modulated (AM) CW signal at 243.0 megacycles. The modulating tone is 1000 cps at 25 percent modulation, and the transmitting interruption cycle is three seconds off and two seconds on. The power of the signal during transmission is 3 watts. The equipment operates on +28 volts d-c at a maximum power dissipation of 10 watts.

20.2 LEADING PARTICULARS

The transmitter contains two plug-in modules; modulator-regulator A1, and r-f amplifier-oscillator module A2. The below leading particulars contain reference information pertaining to the features and characteristics of the Recovery-Beacon Transmitter:

- a. Weight 2 pounds max.
- b. Power dissipation . 10 watts max.
- c. Input voltage . . . +28 volts dc
(+25 to +30 vdc)
- d. Output signal . . . Interrupted tone-modulated cw signals
- e. Carrier Frequency . 243.0
- f. Stability 0.005 percent
- g. Modulation Square-wave amplitude modulated 15 to 25 percent at 1000 \pm 50 cps
- h. Transmitting cycle
 1. On 2 \pm 0.2 seconds
 2. Off 3 \pm 0.2 seconds
- i. VSWR 1.5:1

20.3 FUNCTIONAL BLOCK DIAGRAM

20.3.1 Modulator-Regulator Module (Figure 20-1)

The transmitter operates when the Recovery Beacon switch on control panel 20 is placed in the "ON" position. When the VHF Beacon switch is placed in the "ON" position +28 volts d-c from the Flight and Post Landing DC Bus is applied to the voltage-regulator circuit Q1-Q2 of Modulator-Regulator module A1 via pin 1. The input supply voltage may be monitored at pin 19 of test connector J101. The series connected voltage regulator reduces the +28 volts d-c and regulates the output voltage to +20 volts d-c. The regulated +20 volts d-c is applied to the interruption and modulation multivibrators. The +20 volts d-c is also applied to the r-f amplifier-oscillator module via

VHF RECOVERY BEACON

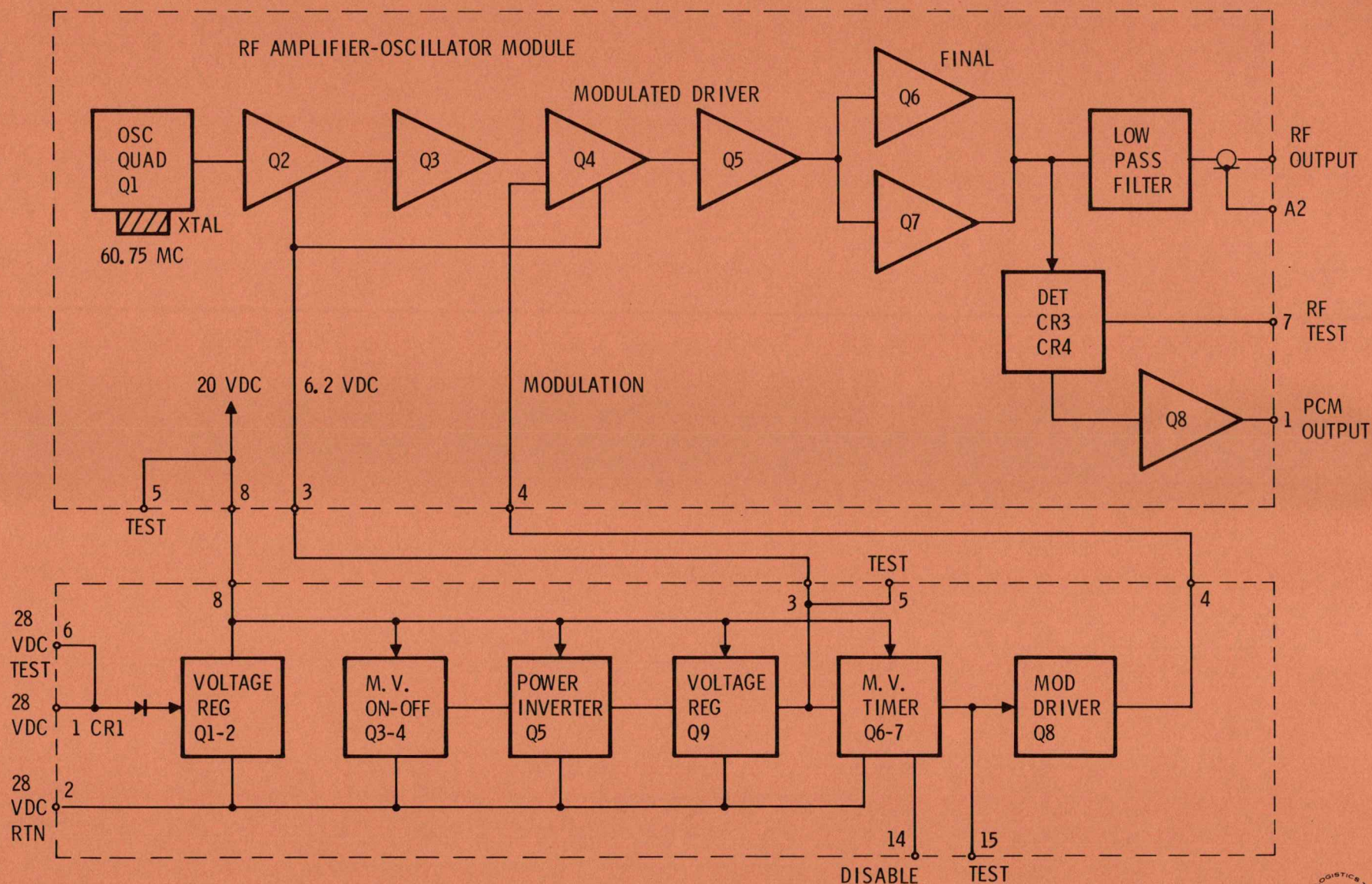


Figure 20-1

CD-125C



pin 8. The regulated d-c voltage is also routed to pin 34 of the front panel test jack (J101) for testing purposes.

The interruption multivibrator Q3-Q4 is a free running multivibrator that generates the basic timing to control the on time and off-time of the transmitter. The operation of Q3-Q4 controls the operation of Q5 and Q9. Q4 of the multivibrator is turned off for 2 seconds and turned on for 3 seconds. When Q4 is turned on it biases Q5 on. When Q5 is biased on Q9 is biased off. With Q9 biased off the 6.2 volts bias for Q2 and Q4 in the amplifier-oscillator is interrupted. With Q4 off Q5 turns off and Q9 turns on applying 6.2 volts dc bias to Q2 and Q4 permitting normal transmitter operation.

The interruption timing signal from Q3-Q4 is inverted by power inverter Q5 and applied to voltage regulator stage Q9. Only during the two second time when Q4 is turned off does the voltage regulator Q9 produce an output pulse of +6.2 volts dc to the amplifier stages Q2 and Q4 in the amplifier-oscillator module. This two second timing signal is routed to pin 25 of the output test jack (J101) for testing purposes. The interruption timer may be disabled by applying a ground to pin 36 of output test jack J101.

The 1000 cycle tone modulation is obtained from modulation multivibrator Q6-Q7, which operates upon application of the regulated +20 volts d-c from the voltage regulator Q1-Q2. This free-running multivibrator generates a 1000 cycle square-wave that is applied through driver Q8 to the modulation amplifier Q4, in the amplifier-oscillator module, via pin 4. The modulation multivibrator may be disabled by applying a ground to pin 14 of P1.

20.3.2 RF Amplifier-Oscillator Module

The output carrier signal of 243.0 megacycles is initiated in oscillator-quadrupler Q1. Transistor Q1 operates on a fundamental crystal controlled frequency of 60.75 megacycles. The oscillator-quadrupler supplies a 243.0 mc signal to the first amplifier Q2. Transistor Q2, in a common emitter configuration, is only enabled for 2 seconds out of every five seconds due to interruption timer Q3-Q4. The 6.2 volts dc from the timer supplies base bias to Q2. The output of amplifier Q2 is applied to amplifier Q3. Transistor amplifier Q3 is in a common emitter configuration and its output is applied to modulation amplifier Q4. Transistor Q4 is biased on by the +6.2 volts dc from the interruption timer and is modulated by the square-wave from the 1 kc modulator in the modulator-regulator module. The carrier is applied to the base and the square-wave modulation is applied to the emitter. The output of Q4 is a modulated square-wave and is applied to the transmitter driver Q5. Transistor Q5 is in a common emitter configuration and amplifies the signal sufficiently to drive the final amplifiers Q6-Q7. The final amplifiers Q6-Q7 are in a parallel configuration. The 1 kc tone modulated, pulsed r-f output signal is routed to the output connector A2 via the low pass filter. At the output of the transmitter, the pulsed r-f carrier, containing 15 to 25 percent modulation, has a minimum power output of 3 watts.

The signal sampler circuit CR3-CR4 and emitter follower Q8 converts the r-f carrier to an analog voltage for measurement at pin 20 or pin 13 at test connector J101. The output of the emitter follower Q8 is also applied to the equipment output connector.